SAMSUNG

Data Book

AHCT/HCTLS
(High Speed CMOS Logic IC)

1990



INTRODUCTION

Samsung Semiconductor is a broad-line manufacturer of semiconductors that range from VLSI circuits such as memories (DRAM, SRAM, EPROM and EEPROM), microprocessors, gate arrays and programmable logic to transistors, linear circuits and telecommunications products.

The KS54/74AHCT and the KS54/74HCTLS high-performance CMOS logic families are Samsung's entry into the general purpose digital logic area.

The KS54/74AHCT advanced high-speed CMOS family is designed to provide performance equivalent to or better than that of the bipolar 54/74ALS (Advanced Low-power Scholttky) family with the additional CMOS advantages of low power dissipation and high noise immunity. The AHCT parts can therefore be used as direct plug-in replacements for their ALS counterparts (and in most applications for FAST and Schottky) and improve the system performance.

The 54/74HCTLS high-speed CMOS family offers similar benefits as a replacement for industry-standard 54/74LS (Low-power Schottky), 54/74HCT and 54/74HC. While meeting all of the HCT electrical specifications, it also provides improved speed and drive capability, so that LS parts can be replaced with no performance degradation.

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Circuit diagrams utilizing SAMSUNG products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of SAMSUNG or others. SAMSUNG reserve the right to change device specifications.

High Performance CMOS Logic Data Book

KS54/74AHCT Advanced High-Speed CMOS

KS54/74HCTLS High-Speed CMOS

SAMSUNG DATA BOOK LIST

- I. Semiconductor Product Guide
- II. Transistor Data Book

Vol. 1: Small Signal TR

Vol. 2: Bipolar Power TR

Vol. 3: TR Pellet

III. Linear IC Data Book

Vol. 1: Audio/Video

Vol. 2: Telecom/Industrial/TOY

Vol. 3: Data Converter IC

- IV. CMOS Consumer IC Data Book
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 - X. Dot Matrix Data Book

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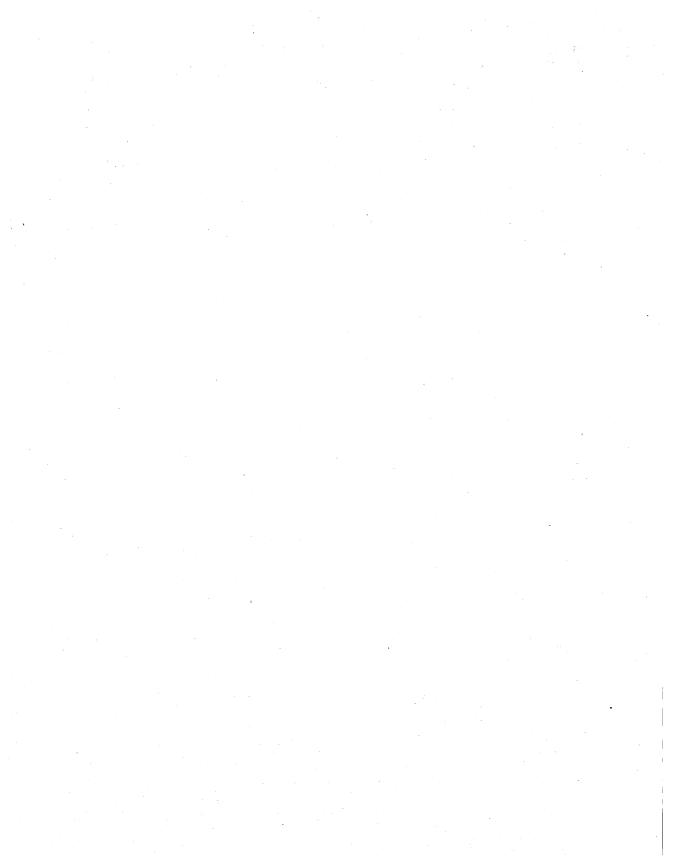
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PRODUCT GUIDE





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1) KS54/74AHCT Family

Device	Function
KS54/74AHCT00	Quad 2-Input NAND Gates
KS54/74AHCT01	Quad 2-Input NAND Gates with Open-Drain Outputs
KS54/74AHCT02	Quad 2-Input NOR Gates
KS54/74AHCT03	Quad 2-Input NAND Gates with Open-Drain Outputs
KS54/74AHCT04	Hex Inverters
KS54/74AHCT05	Hex Inverters with Open-Drain Outputs
KS54/74AHCT08	Quad 2-Input AND Gates
KS54/74AHCT09	Quad 2-Input AND Gates with Open-Drain Outputs
KS54/74AHCT10	Triple 3-Input NAND Gates
KS54/74AHCT11	Triple 3-Input AND Gates
KS54/74AHÇT12	Triple 3-Input NAND Gates with Open-Drain Outputs
KS54/74AHCT14	Hex Schmitt-Trigger Inverters
KS54/74AHCT20	Dual 4-Input NAND Gates
KS54/74AHCT21	Dual 4-Input AND Gates
KS54/74AHCT22	Dual 4-Input NAND Gates with Open-Drain Outputs
KS54/74AHCT27	Triple 3-Input NOR Gates
KS54/74AHCT30	8-Input NAND Gate
KS54/74AHCT32	Quad 2-Input OR Gates
KS54/74AHCT42	BCD-to-Decimal Decoder
KS54/74AHCT51	Dual AND-OR-Invert Gates
KS54/74AHCT58	Dual AND-OR Gates
KS54/74AHCT73	Dual J-K Negative-Edge-Triggered Filp-Flops with Clear
KS54/74AHCT74	Dual D-Type Positive-Edge-Triggered Filp-Flops with Preset and Clear
KS54/74AHCT75	Quad Bistable Transparent Latches
KS54/74AHCT76	Dual J-K Negative-Edge-Triggered Filp Flops with Preset and Clear
KS54/74AHCT77	Quad D-Type Latches
KS54/74AHCT78	Dual J-K Negative-Edge-Triggered Filp-Flops with Preset, Common Clear and Common Clock
KS54/74AHCT86	Quad 2-Input Exclusive-OR Gates
KS54/74AHCT90	Decade Counters
KS54/74AHCT92	Divide-by-Twelve Counter
KS54/74AHCT93	4 Bit Binary Counter Divide by Two and Divide by Eight
KS54/74AHCT107	Dual J-K Negative-Edge-Triggered Filp-Flops with Clear
KS54/74AHCT109	Dual J-K Positive-Edge-Triggered Filp-Flops with Preset and Clear
KS54/74AHCT112	Dual J-K Negative-Edge-Triggered Filp-Flops with Preset and Clear
KS54/74AHCT123	Dual Retriggerable Monostable Multivibrators
KS54/74AHCT125	Quad Buffers with 3-State Outputs
KS54/74AHCT126	Quad Buffers with 3-State Outputs
KS54/74AHCT132	Quad 2-Input NAND Gates with Schmitt-Trigger Inputs
KS54/74AHCT133	13-Input NAND Gate
KS54/74AHCT138	3-Line to 8-Line Decoders/Demultiplexers
KS54/74AHCT139	Dual 1 of 4 Decoders/Demultiplexers
KS54/74AHCT148	8-Line to 3-Line Priority Encoders
KS54/74AHCT151	1 of 8 Data Selectors/Multiplexers
KS54/74AHCT153	Dual 1 of 4 Data Selectors/Multiplexers
KS54/74AHCT154	4-Line to 16-Line Decoders/Demultiplexers
KS54/74AHCT155	Dual 2 to 4 Line Decoders/Demultiplexers
KS54/74AHCT157	Quad 2-Line to 1-Line Data Selectors/Multiplexers
KS54/74AHCT158	Quad 2-Line to 1-Line Data Selectors/Multiplexers
KS54/74AHCT160	Synchronous 4-Bit Decade Counters
KS54/74AHCT161	Synchronous 4-Bit Binary Counters
KS54/74AHCT162	Synchronous 4-Bit Decade Counters
KS54/74AHCT163	Synchronous 4-Bit Binary Counters
KS54/74AHCT164	8-Bit Serial-In/Paralle-Out Shift Registers
KS54/74AHCT165	8-Bit Parallel-In/Serial-Out Shift Registers
KS54/74AHCT166	8-Bit Parallel-In/Serial-Out Shift Registers with Clear

KS54/74AHCT Family (continued)

	Device	Function	
	KS54/74AHCT168	Synchronous 4-Bit Up/Down Decade Counters	
	KS54/74AHCT169	Synchronous 4-Bit Up/Down Binary Counters	
	KS54/74AHCT173	4-Bit D-Type Registers with 3-State Outputs	
ŀ	KS54/74AHCT174	Hex D-Type Filp-Flops with Clear	
ı	KS54/74AHCT175	Quad D-Type Filp-Flops with Clear	
l	KS54/74AHCT181	4-Bit Arithmetic Logic Unit	
	KS54/74AHCT182	Look-Ahead Carry Generator	
1	KS54/74AHCT183	Dual High Speed Adder	
	KS54/74AHCT190	Presettable Synchronous BCD Decade Up/Down Counter	
	KS54/74AHCT191	Synchronous 4-Bit Up/Down Binary Counters	
	KS54/74AHCT192	Presettable Synchronous BCD Decade Up/Down Counter	
1	KS54/74AHCT193	Synchronous 4-Bit Up/Down Binary Counters with Dual Clock	
1	KS54/74AHCT194	4-Bit Bidirectional Universal Shift Registers	
	KS54/74AHCT195	4-Bit Bidirectional Universal Shift Registers	
	KS54/74AHCT210	Octal Buffers and Line Drivers with 3-State Outputs	
	KS54/74AHCT238	3-Line to 8-Line Decoders/Demultiplexers	
	KS54/74AHCT239	Dual 1-of-4 Decoders/Demultiplexers	
1	KS54/74AHCT240	Octal Buffers and Line Drivers with 3-State Outputs	
1	KS54/74AHCT241	Octal Buffers and Line Drivers with 3-State Outputs	
	KS54/74AHCT242	Quad Bus Transceivers with 3-State Outputs	
	KS54/74AHCT243	Quad Bus Transceivers with 3-State Outputs	
	KS54/74AHCT244	Octal Buffers and Line Drivers with 3-State Outputs	
	KS54/74AHCT245	Octal Bus Transceivers with 3-State Outputs	
1	KS54/74AHCT251	1 of 8 Data Selectors/Multiplexers with 3-State Outputs	
	KS54/74AHCT253	Dual 1 of 4 Data Selectors/Multiplexers with 3-State Outputs	
	KS54/74AHCT257	Quad 2-Line to 1-Line Data Selectors/Multiplexers with 3-State Outputs	
	KS54/74AHCT258	Quad 2-Line to 1-Line Data Selectors/Multiplexers with 3-State Outputs	
	KS54/74AHCT259	8-Bit Addressable Latches	
	KS54/74AHCT266	Quad Exclusive-NOR Gatges with Open-Drain Outputs	
1	KS54/74AHCT273	Octal D-Type Filp-Flops	
	KS54/74AHCT280	9-Bit Parity Generators/Checkers with Clear	
	KS54/74AHCT299	8-Bit Universal Shift/Storage Registers with 3-State Outputs	
-	KS54/74AHCT322	8-Bit Shift Registers with Sign Extend	
	KS54/74AHCT352	Dual 4-Line to 1-Line Data Selectors/Multiplexers	
ľ	KS54/74AHCT353	Dual 1 of 4 Data Selectors/Multiplexers with 3-State Outputs	
	KS54/74AHCT365	Hex Bus-Drivers with 3-State Outputs	
	KS54/74AHCT366	Hex Bus-Drivers with 3-State Outputs	
	KS54/74AHCT367	Hex Bus-Drivers with 3-State Outputs	
	KS54/74AHCT368	Hex Bus-Drivers with 3-State Outputs	
	KS54/74AHCT373	Octal D-Type Transparent Latches with 3-State Outputs	
	KS54/74AHCT374	Octal D-Type Flip-Flops with 3-State Outputs	
	KS54/74AHCT377	Octal D-Type Flip-Flops with Clock Enable	
1	KS54/74AHCT390	Dual 4-Bit Decade Counters	
	KS54/74AHCT393	Dual 4-Bit Binary Counters	
	KS54/74AHCT399	Quad 2-Port Registers	
	KS54/74AHCT423	Dual Retriggerable Monostable Multivibrators	
	KS54/74AHCT465	Octal Buffers and Line Drivers with 3-State Outputs	
	KS54/74AHCT466	Octal Buffers and Line Drivers with 3-State Outputs	
1	KS54/74AHCT467	Octal Buffers and Line Drivers with 3-State Outputs	
	KS54/74AHCT468	Octal Buffers and Line Drivers with 3-State Outputs	
	KS54/74AHCT518	8-Bit Identity Comparators	
	KS54/74AHCT519	8-Bit Identity Comparators	
	KS54/74AHCT520	8-Bit Identity Comparators	
	KS54/74AHCT521	8-Bit Identity Comparators	
	KS54/74AHCT522	8-Bit Identity Comparators	
	KS54/74AHCT533	Octal D-Type Transparent Latches with 3-State Outputs	
1	KS54/74AHCT534	Octal D-Type Flip-Flops with 3-State Outputs	
- 1			

KS54/74AHCT Family (continued)

Device	Function
KS54/74AHCT541	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74AHCT563	Octal D-Type Transparent Latches with 3-State Outputs
KS54/74AHCT564	Octal D-Type Flip-Flops with 3-State Outputs
KS54/74AHCT573	Octal D-Type Transparent Latches with 3-State Outputs
KS54/74AHCT574	Octal D-Type Flip-Flops with 3-State Outputs
KS54/74AHCT590	8-Bit Binary Counters with 3-State Output Register
KS54/74AHCT591	8-Bit Binary Counters with 3-State Output Register
KS54/74AHCT592	8-Bit Binary Counters with Input Register
KS54/74AHCT593	8-Bit Binary Counters with Bidirectional Input Register Counter Output
KS54/74AHCT595	8-Bit Shift Registers with Output Latches
KS54/74AHCT596	8-Bit Shift Registers with Output Latches
KS54/74AHCT597	8-Bit Shift Registers with Input Latches
KS54/74AHCT640	Octal Bus Transceivers with 3-State Outputs
KS54/74AHCT643	Octal Bus Transceivers with 3-State Outputs
KS54/74AHCT645	Octal Bus Transceivers with 3-State Outputs
KS54/74AHCT646	Octal 3-State Bus Transceivers with Registers
KS54/74AHCT648	Octal 3-State Bus Transceivers with Registers
KS54/74AHCT651	Octal 3-State Bus Transceivers with Registers
KS54/74AHCT652	Octal 3-State Bus Transceivers with Registers
KS54/74AHCT658	Octal Bus Transceivers with Parity
KS54/74AHCT659	Octal Bus Transceivers with Parity
KS54/74AHCT664	Octal Bus Transceivers with Parity
KS54/74AHCT665	Octal Bus Transceivers with Parity
KS54/74AHCT670	4-By-4 Register Files with 3-State Outputs
KS54/74AHCT679	12-Bit Address Comparators
KS54/74AHCT680	12-Bit Address Comparators
KS54/74AHCT682	8-Bit Magnitude Comparators
KS54/74AHCT684	8-Bit Magnitude Comparators
KS54/74AHCT686	8-Bit Magnitude Comparators
KS54/74AHCT688	8-Bit Identity Comparators
KS54/74AHCT689	8-Bit Identity Comparators with Open-Drain Outputs
KS54/74AHCT793	Octal Latches with Readback
KS54/74AHCT794	Octal Registers with Readback
KS54/74AHCT821	10-Bit Bus Interface Registers with 3-State Outputs
KS54/74AHCT822	10-Bit Bus Interface Registers with 3-State Outputs
KS54/74AHCT823	9-Bit Bus Interface Registers with 3-State Outputs
KS54/74AHCT824	9-Bit Bus Interface Registers with 3-State Outputs
KS54/74AHCT825	8-Bit Bus Interface Registers with 3-State Outputs
KS54/74AHCT826	8-Bit Bus Interface Registers with 3-State Outputs
KS54/74AHCT841	10-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74AHCT842	10-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74AHCT843	9-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74AHCT844	9-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74AHCT845	8-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74AHCT846	8-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74AHCT4049	Hex Inverting Logic Level Down Converters
KS54/74AHCT4050	Hex Logic Level Down Converters

2) KS54/74HCTLS Family (continued)

Device	Function
KS54/74HCTLS00	Quad 2-Input NAND Gates
KS54/74HCTLS01	Quad 2-Input NAND Gates with Open-Drain Outputs
KS54/74HCTLS02	Quad 2-Input NOR Gates
KS54/74HCTLS03	Quad 2-Input NAND Gates with Open-Drain Outputs
KS54/74HCTLS04	Hex Inverters
KS54/74HCTLS05	Hex Inverters with Open-Drain Outputs
KS54/74HCTLS08	Quad 2-Input AND Gates
KS54/74HCTLS09	Quad 2-Input AND Gates with Open-Drain Outputs
KS54/74HCTLS10	Triple 3-Input NAND Gates
KS54/74HCTLS11	Triple 3-Input AND Gates
KS54/74HCTLS12	Triple 3-Input NAND Gates with Open-Drain Outputs
KS54/74HCTLS14	Hex Schmitt-Trigger Inverters
KS54/74HCTLS20	Dual 4-Input NAND Gates
KS54/74HCTLS21	Dual 4-Input AND Gates
K\$54/74HCTL\$22	Dual 4-Input NAND Gates with Open-Drain Outputs
KS54/74HCTLS27	Triple 3-Input NOR Gates
KS54/74HCTLS30	8-Input NAND Gate
KS54/74HCTLS32	Quad 2-Input OR Gates
KS54/74HCTLS42	BCD-to-Decimal Decoder
KS54/74HCTLS51	Dual AND-OR-Invert Gates
KS54/74HCTLS58	Dual AND-OR Gates
KS54/74HCTLS73A	Dual J-K Negative-Edge-Triggered Filp-Flops with Clear
KS54/74HCTLS74A	Dual D-Type Positive-Edge-Triggered Filp-Flops with Preset and Clear
KS54/74HCTLS75	Quad Bistable Transparent Latches
KS54/74HCTLS76A	Dual J-K Negative-Edge-Triggered Filp Flops with Preset and Clear
KS54/74HCTLS77	Quad D-Type Latches
KS54/74HCTLS78A	Dual J-K Negative-Edge-Triggered Filp-Flops with Preset, Common Clear and Common Clock
KS54/74HCTLS86	Quad 2-Input Exclusive-OR Gates
KS54/74HCTLS90	Decade Counters
KS54/74HCTLS92	Divide-by-Twelve Counter
KS54/74HCTLS93	4 Bit Binary Counter Divide by Two and Divide by Eight
KS54/74HCTLS107A	Dual J-K Negative-Edge-Triggered Filp-Flops with Clear
KS54/74HCTLS109A	Dual J-K Positive-Edge-Triggered Filp-Flops with Preset and Clear
KS54/74HCTLS112A	Dual J-K Negative-Edge-Triggered Filp-Flops with Preset and Clear
KS54/74HCTLS123	Dual Retriggerable Monostable Multivibrators
KS54/74HCTLS125	Quad Buffers with 3-State Outputs
KS54/74HCTLS126	Quad Buffers with 3-State Outputs
KS54/74HCTLS132	Quad 2-Input NAND Gates with Schmitt-Trigger Inputs
KS54/74HCTLS133	13-Input NAND Gate
KS54/74HCTLS138	3-Line to 8-Line Decoders/Demultiplexers
KS54/74HCTLS139	Dual 1 of 4 Decoders/Demultiplexers
KS54/74HCTLS148	8-Line to 3-Line Priority Encoders
KS54/74HCTLS151	1 of 8 Data Selectors/Multiplexers
KS54/74HCTLS153	Dual 1 of 4 Data Selectors/Multiplexers
KS54/74HCTLS154	4-Line to 16-Line Decoders/Demultiplexers
KS54/74HCTLS155	Dual 2 to 4 Line Decoders/Demultiplexers
KS54/74HCTLS157	Quad 2-Line to 1-Line Data Selectors/Multiplexers
KS54/74HCTLS158	Quad 2-Line to 1-Line Data Selectors/Multiplexers
KS54/74HCTLS160A	Synchronous 4-Bit Decade Counters
KS54/74HCTLS161A	Synchronous 4-Bit Binary Counters
KS54/74HCTLS162A	Synchronous 4-Bit Decade Counters
KS54/74HCTLS163A	Synchronous 4-Bit Binary Counters
KS54/74HCTLS164	8-Bit Serial-In/Paralle-Out Shift Registers
KS54/74HCTLS165	8-Bit Parallel-In/Serial-Out Shift Registers
KS54/74HCTLS166	8-Bit Parallel-In/Serial-Out Shift Registers with Clear
KS54/74HCTLS168	Synchronous 4-Bit Up/Down Decade Counters

KS54/74HCTLS Family (continued)

Device	Function
KS54/74HCTLS169	Synchronous 4-Bit Up/Down Binary Counters
KS54/74HCTLS173	4-Bit D-Type Registers with 3-State Outputs
KS54/74HCTLS174	Hex D-Type Filp-Flops with Clear
KS54/74HCTLS175	Quad D-Type Filp-Flops with Clear
KS54/74HCTLS181	4-Bit Arithmetic Logic Unit
KS54/74HCTLS182	Look-Ahead Carry Generator
KS54/74HCTLS183	Dual High Speed Adder
KS54/74HCTLS190	Presettable Synchronous BCD Decade Up/Down Counter
KS54/74HCTLS191	Synchronous 4-Bit Up/Down Binary Counters
KS54/74HCTLS192	Presettable Synchronous BCD Decade Up/Down Counter
KS54/74HCTLS193	Synchronous 4-Bit Up/Down Binary Counters with Dual Clock
K\$54/74HCTL\$194	4-Bit Bidirectional Universal Shift Registers
KS54/74HCTLS195	4-Bit Bidirectional Universal Shift Registers
KS54/74HCTLS210	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74HCTLS238	3-Line to 8-Line Decoders/Demultiplexers
KS54/74HCTLS239	Dual 1-of-4 Decoders/Demultiplexers
KS54/74HCTLS240	Octal Buffers and Line Drivers with 3-State Outputs Octal Buffers and Line Drivers with 3-State Outputs
KS54/74HCTLS241 KS54/74HCTLS242	Quad Bus Transceivers with 3-State Outputs
KS54/74HCTLS242 KS54/74HCTLS243	Quad Bus Transceivers with 3-State Outputs Quad Bus Transceivers with 3-State Outputs
KS54/74HCTLS243	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74HCTLS244	Octal Bus Transceivers with 3-State Outputs
KS54/74HCTLS251	1 of 8 Data Selectors/Multiplexers with 3-State Outputs
KS54/74HCTLS253	Dual 1 of 4 Data Selectors/Multiplexers with 3-State Outputs
KS54/74HCTLS257	Quad 2-Line to 1-Line Data Selectors/Multiplexers with 3-State Outputs
KS54/74HCTLS258	Quad 2-Line to 1-Line Data Selectors/Multiplexers with 3-State Outputs
KS54/74HCTLS259	8-Bit Addressable Latches
KS54/74HCTLS266	Quad Exclusive-NOR Gatges with Open-Drain Outputs
KS54/74HCTLS273	Octal D-Type Filp-Flops
KS54/74HCTLS280	9-Bit Parity Generators/Checkers with Clear
KS54/74HCTLS299 A	8-Bit Universal Shift/Storage Registers with 3-State Outputs
KS54/74HCTLS322	8-Bit Shift Registers with Sign Extend
KS54/74HCTLS352	Dual 4-Line to 1-Line Data Selectors/Multiplexers
KS54/74HCTLS353	Dual 1 of 4 Data Selectors/Multiplexers with 3-State Outputs
KS54/74HCTLS365A	Hex Bus-Drivers with 3-State Outputs
KS54/74HCTLS366A	Hex Bus-Drivers with 3-State Outputs
KS54/74HCTLS367A	Hex Bus-Drivers with 3-State Outputs
KS54/74HCTLS368A	Hex Bus-Drivers with 3-State Outputs
KS54/74HCTLS373	Octal D-Type Transparent Latches with 3-State Outputs
KS54/74HCTLS374	Octal D-Type Flip-Flops with 3-State Outputs
KS54/74HCTLS377	Octal D-Type Flip-Flops with Clock Enable
KS54/74HCTLS390	Dual 4-Bit Decade Counters
KS54/74HCTLS393	Dual 4-Bit Binary Counters
KS54/74HCTLS399	Quad 2-Port Registers
KS54/74HCTLS423	Dual Retriggerable Monostable Multivibrators
KS54/74HCTLS465 KS54/74HCTLS466	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74HCTLS466 KS54/74HCTLS467	Octal Buffers and Line Drivers with 3-State Outputs Octal Buffers and Line Drivers with 3-State Outputs
KS54/74HCTLS467 KS54/74HCTLS468	Octal Buffers and Line Drivers with 3-State Outputs Octal Buffers and Line Drivers with 3-State Outputs
KS54/74HCTLS466 KS54/74HCTLS518	8-Bit Identity Comparators
KS54/74HCTLS518	8-Bit Identity Comparators
KS54/74HCTLS520	8-Bit Identity Comparators
KS54/74HCTLS521	8-Bit Identity Comparators
KS54/74HCTLS522	8-Bit Identity Comparators
KS54/74HCTLS533	Octal D-Type Transparent Latches with 3-State Outputs
KS54/74HCTLS534	Octal D-Type Flip-Flops with 3-State Outputs
KS54/74HCTLS540	Octal Buffers and Line Drivers with 3-State Outputs

KS54/74HCTLS Family (continued)

Device	Function
KS54/74HCTLS563	Octal D-Type Transparent Latches with 3-State Outputs
KS54/74HCTLS564	Octal D-Type Flip-Flops with 3-State Outputs
KS54/74HCTLS573	Octal D-Type Transparent Latches with 3-State Outputs
KS54/74HCTLS574	Octal D-Type Flip-Flops with 3-State Outputs
KS54/74HCTLS590	8-Bit Binary Counters with 3-State Output Register
KS54/74HCTLS591	8-Bit Binary Counters with 3-State Output Register
KS54/74HCTLS592	8-Bit Binary Counters with Input Register
KS54/74HCTLS593	8-Bit Binary Counters with Bidirectional Input Register Counter Output
KS54/74HCTLS595	8-Bit Shift Registers with Output Latches
KS54/74HCTLS596	8-Bit Shift Registers with Output Latches
KS54/74HCTLS597	8-Bit Shift Registers with Input Latches
KS54/74HCTLS640	Octal Bus Transceivers with 3-State Outputs
KS54/74HCTLS643	Octal Bus Transceivers with 3-State Outputs
KS54/74HCTLS645	Octal Bus Transceivers with 3-State Outputs
KS54/74HCTLS646	Octal 3-State Bus Transceivers with Registers
KS54/74HCTLS648	Octal 3-State Bus Transceivers with Registers
KS54/74HCTLS651	Octal 3-State Bus Transceivers with Registers Octal 3-State Bus Transceivers with Registers
KS54/74HCTLS652	Octal 3-State Bus Transceivers with Registers Octal 3-State Bus Transceivers with Registers
	Octal Bus Transceivers with Parity
KS54/74HCTLS658	
KS54/74HCTLS659	Octal Bus Transceivers with Parity
KS54/74HCTLS664	Octal Bus Transceivers with Parity
KS54/74HCTLS665	Octal Bus Transceivers with Parity
KS54/74HCTLS670	4-By-4 Register Files with 3-State Outputs
KS54/74HCTLS679	12-Bit Address Comparators
KS54/74HCTLS680	12-Bit Address Comparators
KS54/74HCTLS682	8-Bit Magnitude Comparators
KS54/74HCTLS684	8-Bit Magnitude Comparators
KS54/74HCTLS686	8-Bit Magnitude Comparators
KS54/74HCTLS688	8-Bit Identity Comparators
KS54/74HCTLS689	8-Bit Identity Comparators with Open-Drain Outputs
KS54/74HCTLS793	Octal Latches with Readback
KS54/74HCTLS794	Octal Registers with Readback
KS54/74HCTLS821	10-Bit Bus Interface Registers with 3-State Outputs
KS54/74HCTLS822	10-Bit Bus Interface Registers with 3-State Outputs
KS54/74HCTLS823	9-Bit Bus Interface Registers with 3-State Outputs
KS54/74HCTLS824	9-Bit Bus Interface Registers with 3-State Outputs
KS54/74HCTLS825	8-Bit Bus Interface Registers with 3-State Outputs
KS54/74HCTLS826	8-Bit Bus Interface Registers with 3-State Outputs
KS54/74F CTLS841	10-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74HCTLS842	10-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74HCTLS843	9-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74HCTLS844	9-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74HCTLS845	8-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74HCTLS846	8-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74HCTLS4049	Hex Inverting Logic Level Down Converters
KS54/74HCTLS4050	Hex Logic Level Down Converters



2. Functional Selection Guide

Function	Part Number KS54/74AHCT KS54/74HCTLS	Description	Package
Gates and	00	Quad 2-Input NAND Gates	14 DIP/SOP
Inverters	01	Quad 2-Input NAND Gates with Open-Drain Outputs	14 DIP/SOP
	02	Quad 2-Input NOR Gates	14 DIP/SOP
	03	Quad 2-Input NAND Gates with Open-Drain Outputs	14 DIP/SOP
	04	Hex Inverters	14 DIP/SOP
	05	Hex Inverters with Open-Drain Outputs	14 DIP/SOP
	08 09	Quad 2-Input AND Gates Quad 2-Input AND Gates with Open-Drain Outputs	14 DIP/SOP 14 DIP/SOP
	10	Triple 3-Input NAND Gates	14 DIP/SOP
	11	Triple 3-Input AND Gates	14 DIP/SOP
	12	Triple 3-Input NAND Gates with Open-Drain Outputs	14 DIP/SOP
	14	Hex Schmitt-Trigger Inverters	14 DIP/SOP
	20	Dual 4-Input NAND Gates	14 DIP/SOP
	21	Dual 4-Input AND Gates	14 DIP/SOP
	22	Dual 4-Input NAND Gates with Open-Drain Outputs	14 DIP/SOP
	27	Triple 3-Input NOR Gates	14 DIP/SOP
	30	8-Input NAND Gate	14 DIP/SOP
	32 51	Quad 2-Input OR Gates Dual AND-OR-Invert Gates	14 DIP/SOP 14 DIP/SOP
	58	Dual AND-OR-Invert Gates	14 DIP/SOP
	86	Quad 2-Input Exclusive-OR Gates	14 DIP/SOP
	132	Quad 2-Input NAND Gates with Schmitt-Trigger Inputs	14 DIP/SOP
	133	13-Input NAND Gate	16 DIP/SOP
	266	Quad Exclusive-NOR Gatges with Open-Drain Outputs	16 DIP/SOP
Buffers	125	Quad Buffers with 3-State Outputs	14 DIP/SOP
and	126	Quad Buffers with 3-State Outputs	14 DIP/SOP
Line	210	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
Drivers	240	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
	241	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
	244 365	Octal Buffers and Line Drivers with 3-State Outputs Hex Bus-Drivers with 3-State Outputs	20 DIP/SOP 16 DIP/SOP
	366	Hex Bus-Drivers with 3-State Outputs	16 DIP/SOP
	367	Hex Bus-Drivers with 3-State Outputs	16 DIP/SOP
	368	Hex Bus-Drivers with 3-State Outputs	16 DIP/SOP
	465	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
	466	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
	467	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
	468	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
	540	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
	541	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
Level Shifters	4049 4050	Hex Inverting Logic Level Down Converters Hex Logic Level Down Converters	16 DIP/SOP 16 DIP/SOP
Flip-Flops	73	Dual J-K Negative-Edge-Triggered Filp-Flops with Clear	14 DIP/SOP
	74	Dual D-Type Positive-Edge-Triggered Filp-Flops with Preset and Clear	14 DIP/SOP
	76	Dual J-K Negative-Edge-Triggered Filp Flops with Preset and Clear	16 DIP/SOP
	78	Dual J-K Negative-Edge-Triggered Filip-Flops with Preset,	
		Common Clear and Common Clock	14 DIP/SOP
	107	Dual J-K Negative-Edge-Triggered Filp-Flops with Clear	14 DIP/SOP
*	109	Dual J-K Positive-Edge-Triggered Filp-Flops with Preset and Clear	16 DIP/SOP
	112	Dual J-K Negative-Edge-Triggered Filp-Flops with Preset and Clear	16 DIP/SOP
	173	4-Bit D-Type Registers with 3-State Outputs	16 DIP/SOP
	174	Hex D-Type Filp-Flops with Clear	16 DIP/SOP
	175 273	Quad D-Type Filp-Flops with Clear	16 DIP/SOP 20 DIP/SOP
	374	Octal D-Type Filp-Flops Octal D-Type Flip-Flops with 3-State Outputs	20 DIP/SOP
	514	Octar o Type i lip-i lops with o-otate Outputs	20 DIF/GOP

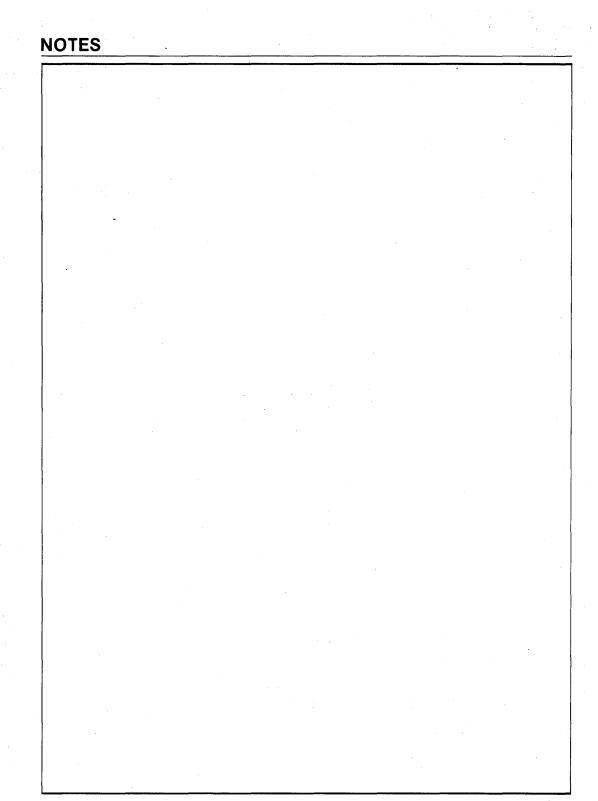
Functional Selection Guide (continued)

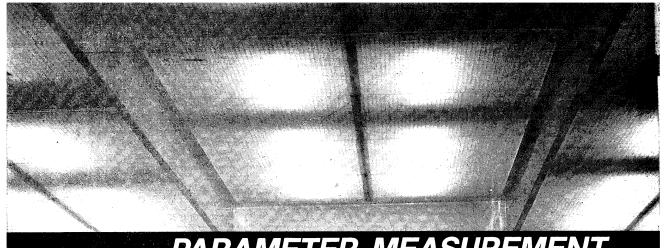
Function	Part Number KS54/74AHCT KS54/74HCTLS	Description	Package
	377 399 534 564 574 670 794 821 822 823 824 825 826	Octal D-Type Flip-Flops with Clock Enable Quad 2-Port Registers Octal D-Type Flip-Flops with 3-State Outputs Octal D-Type Flip-Flops with 3-State Outputs Octal D-Type Flip-Flops with 3-State Outputs 4-By-4 Register Files with 3-State Outputs Octal Registers with Readback 10-Bit Bus Interface Registers with 3-State Outputs 10-Bit Bus Interface Registers with 3-State Outputs 9-Bit Bus Interface Registers with 3-State Outputs 9-Bit Bus Interface Registers with 3-State Outputs 8-Bit Bus Interface Registers with 3-State Outputs 8-Bit Bus Interface Registers with 3-State Outputs	20 DIP/SOP 16 DIP/SOP 20 DIP/SOP 20 DIP/SOP 20 DIP/SOP 16 DIP/SOP 24 DIP/SOP 24 DIP/SOP 24 DIP/SOP 24 DIP/SOP 24 DIP/SOP 24 DIP/SOP 24 DIP/SOP 24 DIP/SOP
Latches	75 77 259 373 533 563 573 793 841 842 843 844 845	Quad Bistable Transparent Latches Quad D-Type Latches 8-Bit Addressable Latches Octal D-Type Transparent Latches with 3-State Outputs Octal Latches with Readback 10-Bit Bus Interface D-Type Latches with 3-State Outputs 10-Bit Bus Interface D-Type Latches with 3-State Outputs 9-Bit Bus Interface D-Type Latches with 3-State Outputs 8-Bit Bus Interface D-Type Latches with 3-State Outputs	16 DIP/SOP 14 DIP/SOP 16 DIP/SOP 20 DIP/SOP 20 DIP/SOP 20 DIP/SOP 20 DIP/SOP 20 DIP/SOP 24 DIP/SOP 24 DIP/SOP 24 DIP/SOP 24 DIP/SOP 24 DIP/SOP 24 DIP/SOP 24 DIP/SOP 24 DIP/SOP
Multiplexers	151 153 157 158 251 253 257 258 352 353	1 of 8 Data Selectors/Multiplexers Dual 1 of 4 Data Selectors/Multiplexers Quad 2-Line to 1-Line Data Selectors/Multiplexers Quad 2-Line to 1-Line Data Selectors/Multiplexers 1 of 8 Data Selectors/Multiplexers with 3-State Outputs Dual 1 of 4 Data Selectors/Multiplexers with 3-State Outputs Quad 2-Line to 1-Line Data Selectors/Multiplexers with 3-State Outputs Quad 2-Line to 1-Line Data Selectors/Multiplexers with 3-State Outputs Dual 4-Line to 1-Line Data Selectors/Multiplexers Dual 1 of 4 Data Selectors/Multiplexers	16 DIP/SOP 16 DIP/SOP 16 DIP/SOP 16 DIP/SOP 16 DIP/SOP 16 DIP/SOP 16 DIP/SOP 16 DIP/SOP 16 DIP/SOP 16 DIP/SOP
Shift Registers	164 165 166 194 195 299 322 595 596 597	8-Bit Serial-In/Paralle-Out Shift Registers 8-Bit Parallel-In/Serial-Out Shift Registers 8-Bit Parallel-In/Serial-Out Shift Registers with Clear 4-Bit Bidirectional Universal Shift Registers 4-Bit Bidirectional Universal Shift Registers 8-Bit Universal Shift/Storage Registers with 3-State Outputs 8-Bit Shift Registers with Sign Extend 8-Bit Shift Registers with Output Latches 8-Bit Shift Registers with Output Latches 8-Bit Shift Registers with Input Latches	14 DIP/SOP 16 DIP/SOP 16 DIP/SOP 16 DIP/SOP 20 DIP/SOP 20 DIP/SOP 16 DIP/SOP 16 DIP/SOP 16 DIP/SOP
Transceivers	242 243 245 640 643 645 646 648	Quad Bus Transceivers with 3-State Outputs Quad Bus Transceivers with 3-State Outputs Octal 3-State Bus Transceivers with Registers Octal 3-State Bus Transceivers with Registers	14 DIP/SOP 14 DIP/SOP 20 DIP/SOP 20 DIP/SOP 20 DIP/SOP 20 DIP/SOP 24 DIP/SOP 24 DIP/SOP

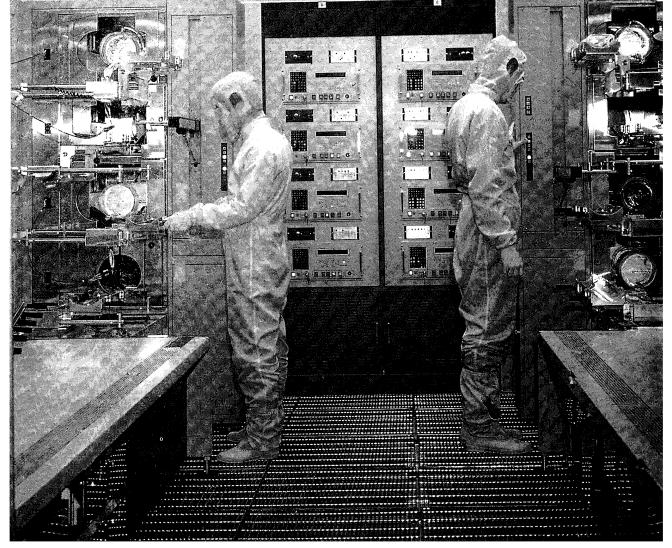


Functional Selection Guide (continued)

Function	Part Number KS54/74AHCT KS54/74HCTLS	Description	Package
	651 652	Octal 3-State Bus Transceivers with Registers Octal 3-State Bus Transceivers with Registers	24 DIP/SOP 24 DIP/SOP
	658	Octal Bus Transceivers with Parity	24 DIP/SOP
	659	Octal Bus Transceivers with Parity	24 DIP/SOP
	664	Octal Bus Transceivers with Parity	24 DIP/SOP
	665	Octal Bus Transceivers with Parity	24 DIP/SOP
Counters	90	Decade Counters	14 DIP/SOP
	92 93	Divide-by-Twelve Counter 4 Bit Binary Counter Divide by Two and Divide by Eight	14 DIP/SOP
	160	Synchronous 4-Bit Decade Counters	16 DIP/SOP
,	161	Synchronous 4-Bit Binary Counters	16 DIP/SOP
	162	Synchronous 4-Bit Decade Counters	16 DIP/SOP
	163	Synchronous 4-Bit Binary Counters	16 DIP/SOP
	168	Synchronous 4-Bit Up/Down Decade Counters	16 DIP/SOP
	169	Synchronous 4-Bit Up/Down Binary Counters	16 DIP/SOP
,	190	Presettable Synchronous BCD Decade Up/Down Counter	16 DIP/SOP
	191	Synchronous 4-Bit Up/Down Binary Counters	16 DIP/SOP
	192	Presettable Synchronous BCD Decade Up/Down Counter	16 DIP/SOP
	193	Synchronous 4-Bit Up/Down Binary Counters with Dual Clock	16 DIP/SOP
	390	Dual 4-Bit Decade Counters	16 DIP/SOP
	393	Dual 4-Bit Binary Counters	16 DIP/SOP
!	590 591	8-Bit Binary Counters with 3-State Output Register	16 DIP/SOP
	592	8-Bit Binary Counters with 3-State Output Register 8-Bit Binary Counters with Input Register	16 DIP/SOP
	593	8-Bit Binary Counters with Imput Register Counter Output	20 DIP/SOP
Decoders	42	BCD-to-Decimal Decoder	16 DIP/SOP
Encoders	138	3-Line to 8-Line Decoders/Demultiplexers	16 DIP/SOP
	139	Dual 1 of 4 Decoders/Demultiplexers	16 DIP/SOP
	148	8-Line to 3-Line Priority Encoders	16 DIP/SOP
	154	4-Line to 16-Line Decoders/Demultiplexers	24 DIP/SOP
	155	Dual 2 to 4 Line Decoders/Demultiplexers	16 DIP/SOP
	238	3-Line to 8-Line Decoders/Demultiplexers	16 DIP/SOP
	239	Dual 1-of-4 Decoders/Demultiplexers	16 DIP/SOP
Multivibrators	123 423	Dual Retriggerable Monostable Multivibrators Dual Retriggerable Monostable Multivibrators	16 DIP/SOP
Arithmetic	181	4-Bit Arithmetic Logic Unit	24 DIP/SOP
Circuits	182	Look-Ahead Carry Generator	16 DIP/SOP
Onounco	183	Dual High Speed Adder	14 DIP/SOP
	280	9-Bit Parity Generators/Checkers with Clear	14 DIP/SOP
	518	8-Bit Identity Comparators	20 DIP/SOP
	519	8-Bit Identity Comparators	20 DIP/SOP
	520	8-Bit Identity Comparators	20 DIP/SOP
	521	8-Bit Identity Comparators	20 DIP/SOP
	522	8-Bit Identity Comparators	20 DIP/SOP
	679	12-Bit Address Comparators	20 DIP/SOP
	680 682	12-Bit Address Comparators	20 DIP/SOP
	682 684	8-Bit Magnitude Comparators	20 DIP/SOP
	686	8-Bit Magnitude Comparators 8-Bit Magnitude Comparators	20 DIP/SOP 20 DIP/SOP
	000		
	688	8-Bit Identity Comparators	20 DIP/SOP

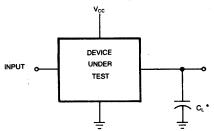




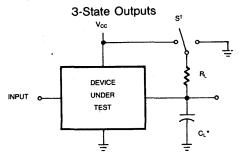


AC SWITCHING TEST CIRCUITS

Totem-Pole Outputs

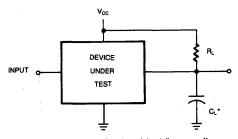


*C_L includes load and test jig capacitance



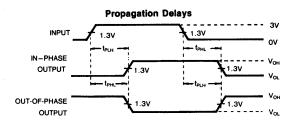
* C_L Includes load and test jig capacitance $S^{\dagger} = V_{CC}$ for t_{PZL} and t_{PLZ} measurements S = GND for t_{PZH} and t_{PHZ} measurements.

Open-Drain Outputs

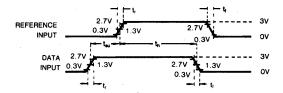


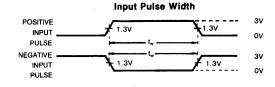
*CL includes load and test jig capacitance

TIMING WAVEFORMS

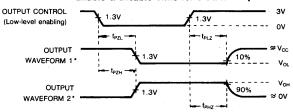


Setup & Hold Times, Input Rise & Fall Times





Enable & Disable Time for 3-State Outputs



- * Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. This waveform is applicable to both 3-state and open-drain outputs.
- Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

DEFINITIONS OF TERMS & SYMBOLS

FUNCTION TABLE SYMBOLS

- H = Steady state high level
- L = Steady state low level
- ↑ = Transition from low to high level
- ↓ = Transition from high to low level
- X = Don't care (high, low states or transitions)
- Z = High-impedance state of a 3-state output
- a..h = The level of steady-state inputs at inputs A thru H, respectively
- Q₀ = Level of Q before the indicated steady-state input conditions were established
- \bar{Q}_0 = Complement of Q_0 or level of \bar{Q} before the indicated steady-state conditions were established
- Q_n = Level of Q before the most recent active transition indicated by \(\) or \(\)
- T = One low-level pulse

TOGGLE = each output changes to the complement of its previous level on each active transition indicated by ↑ or ↓ If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as level (H, L, Q_0 , or $\overline{Q_0}$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as pulse, \Box or \Box , the pulse follows the indicated input transition and persists for an interval dependent on the circuit)

DC Characteristics Terms

VIH High-Level input voltage

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

VIL Low-Level input voltage

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum is specified that is the most-postive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} High-Level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

Vol Low-Level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

V_{T+} Positive-Going threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-} .



V_T_ Negative-Going threshold level

The voltage at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+} .

lo Output Current

The current into* an output with input conditions applied that, according to the product specification, will establish a high or a low level at the output.

I_{IN} Input Curent

The current into* an input when a high or a low level voltage is applied to that input.

Ioz Off-State (high-impedance-state) output current (of a three-state output)

The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output level voltage applied to the output.

This parameter is measured with other input conditions established that would cause the output to be at a low-voltage level (if it were enabled) when the externally applied voltage is high; or high-voltage level when the externally applied voltage is low.

Icc Supply current

The current into* the V_{CC} supply terminal of an integrated circuit.

*Current out of a terminal is given as negative value.

AC CHARACTERISTICS TERMS

t, Rise time

The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the high level.

t_f Fall time

The time interval between two reference points (90% and 10% unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level.

f_{max} Maximum clock frequency

The highest rate at which the cock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of a logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

t_{PLH} Propagation delay time, low-to-high-level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

tPHL Propagation delay time, high-to-low-level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PZH} Enable time (of a three-state output) to high level

The time interval between the specified reference points on the input and output voltage waveforms with the threestate outputs changing from a high-impedance (off) state to the defined high level.

tezi. Enable time (of a three-state output) to low level

The time interval between the specified reference points on the input and output voltage waveforms with the threestate outputs changing from a high-impedance (off) state to the defined low level.



t_{PHZ} Disable time (of a three-state output) from high level

The time interval between the specified reference points on the input and output voltage waveforms with the threestate outputs changing from the defined high level to high-impedance (off) state.

t_{PLZ} Disable time (of a three-state output) from low level

The time interval between the specified reference points on the input and output voltage waveforms with the threestate outputs changing from the defined high level to high-impedance (off) state.

tw Pulse width

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

t_{su} Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

- NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
 - The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

th Hold time

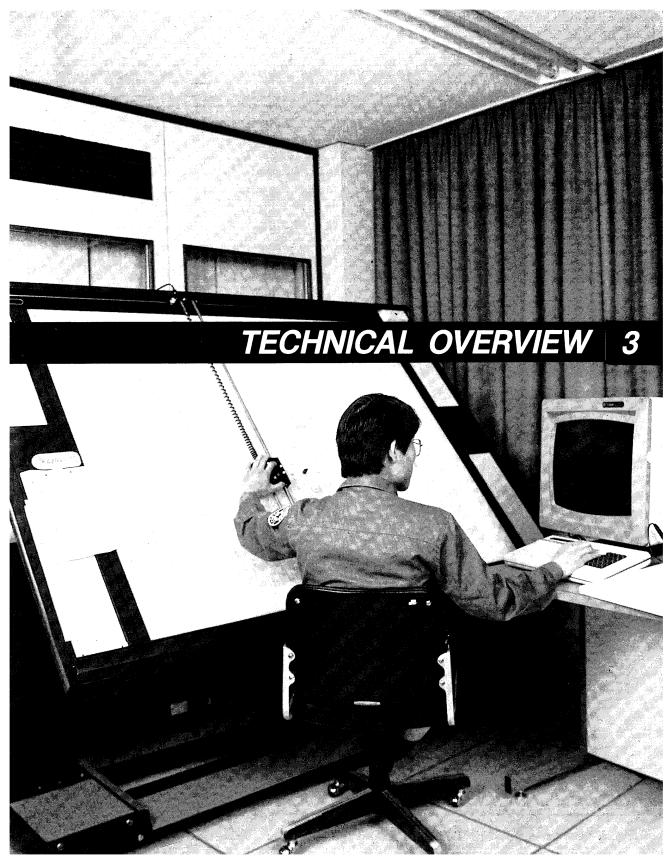
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

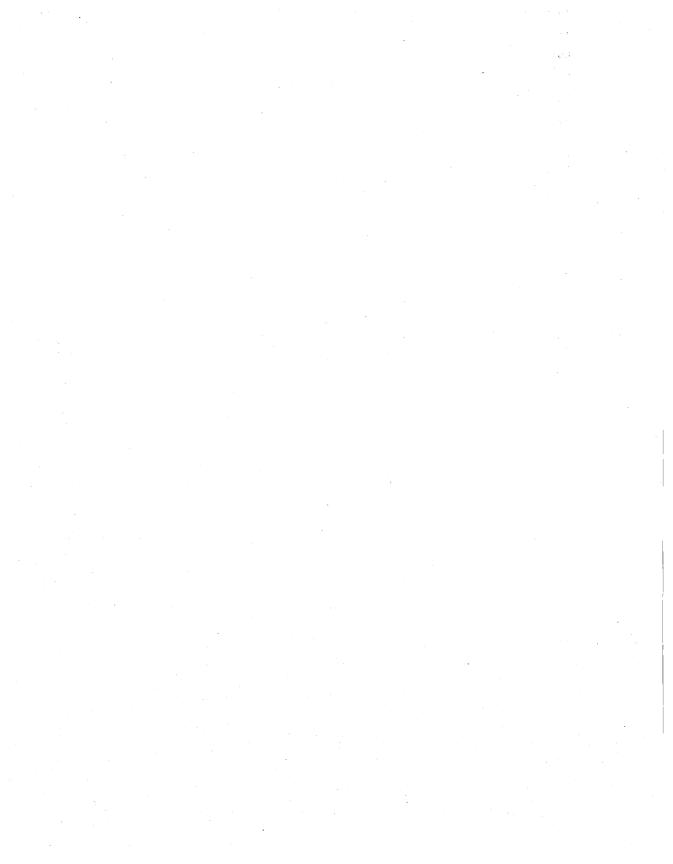
- NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
 - The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

C_{PD} Power dissipation capacitance

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{PD} V_{CC}^2 f$

NOTES





TECHNICAL OVERVIEW

INTRODUCTION

The 54/74AHCT Advanced High-Speed CMOS and the 54/74HCTLS High-Speed CMOS logic families were designed to offer the most desirable features of their CMOS and bipolar predecessors. They have the low power dissipation, superior noise immunity, wide voltage and temperature ranges and the very low input currents of the other high-speed CMOS logic families, in addition to the high speed and drive capability of LS and ALS bipolar logic.

The AHCT family is an equivalent of the bipolar ALS and can readily replace ALS in most existing applications to reduce power dissipation. In many applications, AHCT parts can also be used as replacements for FASTTM and S (Schottky). The HCTLS parts, on the other hand, meet and exceed all of industry-standard LS and HCT specifications, and can be used as replacements to these to lower the power dissipation and improve performance. The design tips section on page 53 gives specific details for direct replacement. Figure 1 shows how AHCT and HCTLS families rank with the other bipolar technologies in terms of speed and power dissipation.

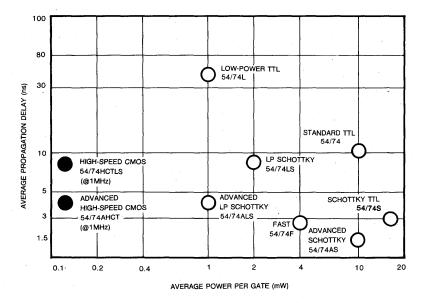


FIGURE 1. Power dissipation vs gate dely characteristics for a two-input NAND gate (74XXX00) implemented in various bipolar and CMOS technologies

Both families feature TTL input voltage levels which enable them to interface with all TTL, NMOS or CMOS outputs without any external components. All AHCT and HCTLS parts are fully characterized and specified over the 4.5 to 5.5V voltage range, and the industrial (-40 to 85° C) and military (-55 to 125° C) temperature ranges. This is a significant improvement over the older biploar logic families, where, for example LS would specify DC specs over 4.75V to 5.25V and AC specs only at 5V and room temperature. (ALS is specified over 4.5 to 5.5V and 0 to 70° C). A comparison of the key characteristics for an octal buffer illustrates these improvements clearly in Figure 2. The DC characteristics common to all AHCT and HCTLS parts are listed in Figure 3.

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		'	TTL		SAMSUN	G CMOS	OTHER CMOS	
		74LS244	74ALS244	74F244	74HCTLS244	74AHCT244	74HC244	74HCT244
Operating Voltage Range (Commercial)		4.75V to 5.25V	4.5V to 5.5V	4.75V to 5.25V	4.5V to 5.5V	4.5V to 5.5V	2V to 6 V	4.5V to 5.5V
Operating Temperature Range (Commercial)		0°C to 70°C	0°C to 70°C	0°C to 70°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C
Maximum Propagation Delay (C _L = 50 pF)		18 ns (V _{CC} = 5V, T _a = 25°C)	10 ns (Over Operating Conditions)	6.5 ns (Over Operating Conditions)	18 ns (V _{CC} = 5V, T _a = 25°C)	10 ns (Over Operating Conditions)	20 ns $(V_{CC} = 5V, T_a = 25^{\circ}C)$	18 ns (V _{CC} = 5V, T _a = 25°C)
Maximum Quiescent Current		54 mA	27 mA	90 mA	0.08 mA	0.08 mA	0.08 mA	0.08 mA
Typical Power Dissipation	Static	120 mW	70 mW	260 mW	0.004 mW	0.004 mW	0.004 mW	0.004 mW
	At 100 kHz (All inputs toggling)	120 mW	70 mW	260 mW	0.6 mW	0.6 mW	1.0 mW	1.8 mW
Output Drive Currents	Юн	-3 mA $(V_{OH} = 2.4V)$ -15 mA $(V_{OH} = 2.0V)$	-3 mA $(V_{OH} = 2.4V)$ -15 mA $(V_{OH} = 2.0V)$	-15 mA (V _{OH} 2.0V)	-6 mA (V _{OH} = 3.84V)	-6 mA (V _{OH} = 3.84V)	-6 mA (V _{OH} = 3.84V)	-6 mA (V _{OH} = 3.84V)
	lou	12 mA $(V_{OL} = 0.4V)$ 24 mA $(V_{OL} = 0.5V)$	12 mA (V _{OL} = 0.4V) 24 mA (V _{OL} = 0.5V)	64 mA (V _{OL} = 0.55V)	12 mA $(V_{OL} = 0.4V)$ 24 mA $(V_{OL} = 0.5V)$	12 mA $(V_{OL} = 0.4V)$ 24 mA $(V_{OL} = 0.5V)$	6 mA (V _{OL} = 0.33V)	6 mA (V _{OL} = 0.33V)
Input Threshold Voltages	V _{IL}	0.8V	0.8V	0.8V	0.8V	0.8V	0.9V (V _{CC} = 4.5V)	V8.0
	V _{IH}	2.0V	2.0V	2.0V	2.0V	2.0V	3.15V (V _{CC} = 4.5V)	2.0V
Input Currents	h∟	-0.2 mA (V _i = 0.4V)	-0.1 mA (V _I = 0.4V)	-1.6 mA (V _i = 0.5V)	-1.0 μA	−1.0 μA	-1.0 μA	-1.0 µA
	l _{IH}	$20 \mu A$ $(V_1 = 2.7V)$	20 μA (V _i = 2.7V)	20 μA (V _i = 2.7V)	1.0 μΑ	1.0 μΑ	1.0 μΑ	1.0 μΑ

FIGURE 2. Key performance characteristics for 74XXXX244 octal buffer

TECHNICAL OVERVIEW

The Samsung CMOS logic families include a comprehensive set of buffers, registers, latches and transceivers that are offered in 8, 9 and 10-bit versions. A wide variety of gates, flip-flops, multiplexers, shift registers, encoder/decoders, schmitt triggers and multivibrators complete the family of 157 part types. Each function is available in both AHCT and HCTLS version.

Characteristic	Symbol	Conditions		T _a = 25°C		Commercial T _a = -40°C to +85°C	Military T _a = -55°C to +125°C	Unit
				Тур		Guaranteed Li	mits	
Minimum High-Level Input Voltage	V _{iH}				2.0	2.0	2.0	v
Minimum Low-Level Input Voltage	V _{iL}				0.8	0.8	0.8	٧
Minimum High-Level Output Voltage			CMOS loads I _{OH} =-20µA	Vcc	V _{CC} -0.1	V _{CC} -0.1	V _{CC} -0.1	
	V _{OH}	V _{IN} =V _{IH} or V _{IL}	Standard Outputs f _{OH} =-4 mA	4.2	3.98	3.84	3.7	٧
·			Bus-Driver Outputs I _{OH} =-6 mA	4.2	3.98	3.84	3.7	
. ,		V _{OL} V _{IN} =V _{IH} or V _{IL}	CMOS loads lo _L =20 μA	0.1	0.1	0.1	0.1	v
Minimum Low-Level Output Voltage	V _{OL}		Standard Outputs I _{OL} =4 mA I _{OL} =8 mA	0.2 0.3	0.26 0.39	0.33 0.5	0.4	
			Bus-Driver Outputs I _{OL} =12 mA I _{OL} =24 mA	0.2 0.3	0.26 0.39	0.33 0.5	0.4	
Maximum Input Leakage Current	l _j	V _{CC} =Max, V _{IN} =V _{CC} or GND			±0.1	±1.0	1.0	μΑ
Maximum 3-State Leakage Current	loz	V _{CC} =Max, Enable=V _{IH} or V _{IL} V _{OUT} =V _{CC} or GND			±0.5	<u></u> ‡5.0	±10.0	μΑ
		GND All Outputs Open	SSI Circuits		2.0	20.0	40.0	μΑ
Maximum Quiescent	lcc		Dual and Quad Flip-Flops & Latches		4.0	40.0	80.0	
Supply Current			MSI Circuits & Circuits with High-Current Outputs		8.0	80.0	160.0	

FIGURE 3. DC characteristics of the 54/74AHCT and 54/74 HCTLS Families ($V_{CC} = 5.0V \pm 10\%$)



TECHNICAL OVERVIEW

PROCESS TECHNOLOGY

The high performance of the AHCT and HCTLS is a result of a unique self-aligned metal-gate CMOS process technology that features 1.2 μ m effective gate lengths and double metallization. The following table compares the general characteristics of this process with other existing CMOS and bipolar technologies used for logic circuits:

	SAMSUNG CMOS	INDUSTRY CMOS (HC & HCT)	INDUSTRY ALS
Number of Masking Steps	8	12-14	13
Number of Metal Layers	2	1	2
Minimum Feature Size (drawn)	2 μm	3-4 μm	4 μm
Interconnections	All Metal	Poly & Metal	All Metal
Relative Die Size	1X	2.5-5X	1.5-2X
Manufacturing Equipment	Standard	Standard	Standard

Samsung's CMOS process was designed from the ground up to be a scaled two-layer metal CMOS process (see *Figure 4* for a cross section). The goal was to make the process as simple as possible, and be able to readily control gate length and gate dielectric thickness. The process uses 8 masking steps. Other semiconductor manufactures, in trying to go to two-layer metal short-channel processes have generally embellished pre-existing silicon-gate processes and have wound up with 12-14 masking steps. More masking steps, of course, make wafers more costly, but most importantly, reduce yield because of more chances for random defects.

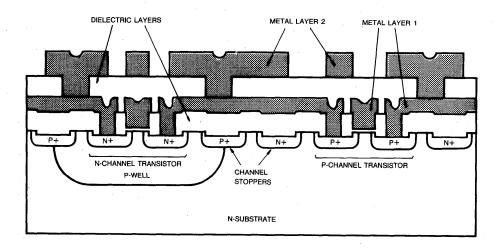
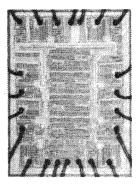


FIGURE 4. Samsung CMOS process cross section for an inverter stage

The Samsung process, with the short 2 μ m channel lengths (1.2 μ m effective), yields gate delays as fast as those of the bipolar LS and ALS processes, and the same short channel lengths allow high-current output drivers to occupy a modest silicon area. Generally, the AHCT and HCTLS logic chips are much smaller than their CMOS and bipolar equivalents (see *Figure 5*). In achieving this small size, two-layer metal is as important as having short channels. For example, in the on-chip busing of ground and V_{CC} to the output drivers, very wide metal lines have to be used that take considerable area. In this case, if these lines are in Metal 2, no extra area is wasted since the circuitry can be placed underneath.

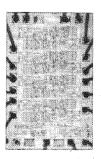


2.57X



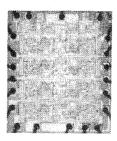
MM74HC240 National Semiconductor

1.42X



74F240 Fairchild

1.57X



SN74ALS240 Texas Instruments

1X



KS74AHCT240 KS74HCTLS240 Samsung

FIGURE 5. Die size comparison for a 74XXX244 from various technologies.

INPUT CHARACTERISITICS

The input stage of an AHCT or HCTLS circuit is illustrated in *Figure 6*. It consists of a diode protection network and a CMOS inverter stage that has very high input impedance. The ultra-low input current specified in the data sheets (1µA maximum) is due to the reverse leakage currents of the diodes and is not used for "driving" the CMOS transistors i.e. the inputs are voltage-driven. This makes AHCT and HCTLS inputs very easy to drive and results in a very high fan-in capability.

TTL-compatible input threshold voltages of 0.8V V_{IL} and 2.0V V_{IH} are accomplished by properly sizing the p- and n-channel transistors of the CMOS inverter stage. The actual logic transition takes place mid-way between these values, at 1.4V, and is very sharp compared to TTL logic due to the very high gain of the first inverter stage. This is illustrated in *Figure 7* for a two-input NAND gate. Note that the input threshold for CMOS is much more stable with temperature than that for LS.

While the AHCT and HCTLS parts are recommended as direct replacements for ALS and LS, one needs to pay attention to not leaving any inputs floating, i.e. unconnected. Since the inputs have very high impedance, they can easily pick up external noise which can result in random switching of the device and high power consumption. Therefore, all unused inputs must be terminated to either V_{CC} or ground.



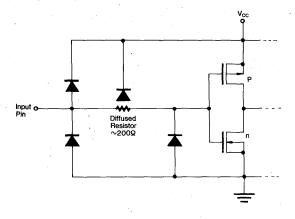


FIGURE 6. The input circuit of AHCT and HCTLS parts.

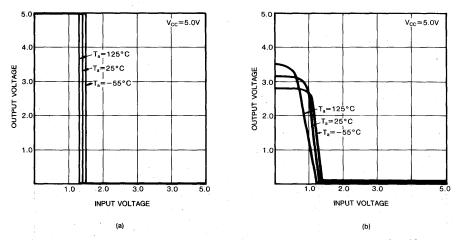


FIGURE 7. Input-Output transfer characteristics for (a) AHCT/HCTLS00, (b) LS00.

OUTPUT CHARACTERISTICS

A typical output stage of an AHCT or HCTLS part consists of a complementary pair of transistors and a diode protection network (see *Figure 8*). Unlike the bipolar outputs, the voltage swing is rail-to-rail, which is responsible for the improved noise margine of AHCT/HCTLS systems. The drive capability of these outputs is similar to the bipolar parts, i.e. 24mA or 8mA I_{OL} (at 0.5V V_{OL}) for bus-driver and standard outputs, respectively. This means that AHCT and HCTLS parts can drive as many loads or as large bus capacitances as their ALS and LS counterparts. *Figure 9* shows a comparison of the output drive capabilities of AHCT/HCTLS and LS/ALS outputs. *Figure 10* illustrates the variations of I_{OL} and I_{OH} with supply voltage and temperature for a standard output ('00) and a bus driver ('244).

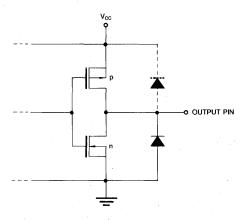
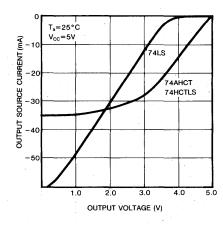


FIGURE 8. A typical output circuit of an AHCT or HCTLS part.

The upper diode is parasitic and embedded in the p-channel transistor.



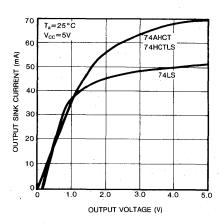
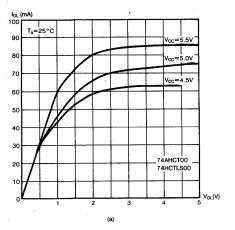
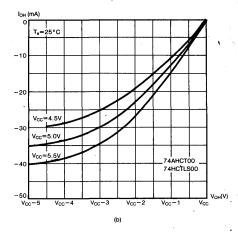
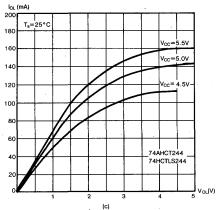
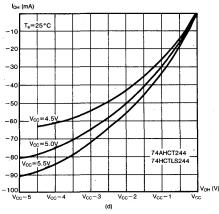


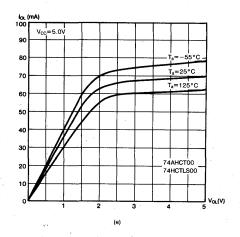
FIGURE 9. Comparison of standard AHCT/HCTLS and standard LS output (a) Source, and (b) sink currents.

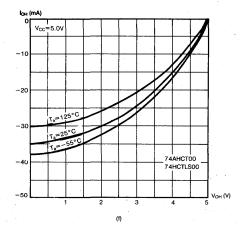












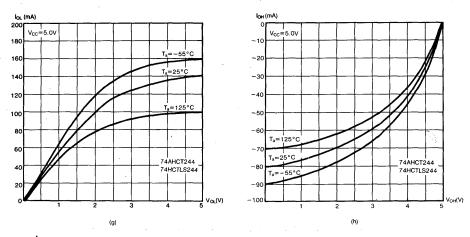


FIGURE 10. Output current variations with supply voltage and temperature for standard [(a), (b), (e) (f)] and bus driver [(c), (d), (g), (h)] outputs.

NOISE IMMUNITY & NOISE MARGINS

The term "noise" in the context of digital circuits and systems means unwanted transient variations of voltages and currents at logic nodes. Typically noise is transferred to logic nodes or interconnecting lines by unwanted capacitive or inductive coupling, as illustrated in *Figure 11*.

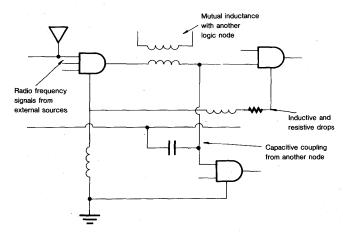
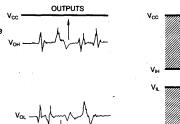


FIGURE 11. Sources of noise in digital systems.

Noise becomes a particularly critical issue in high-speed systems where fast voltage transitions accentuate these parasitic capacitances and inductances. Also, higher speeds allow the device to respond more quickly to noise transients. Therefore, special board layout and decoupling techniques have to be employed to confine noise to an "acceptable range". Obviously, the wider this range, the easier it is to design a clean system. This range is dictated by the input and output characteristics of the ICs in the system, as illustrated in Figure 12, and is measured in terms of "noise margins".



The output signals should be as close to the supply rails as possible. This allows more margin for noise to distort the output signal without violating the logic level requirements of the driven inputs.



The voltage range for each logic level should be as wide as possible. This relaxes the requirements for the cleanliness of incoming signals.

FIGURE 12. Requirements for good noise immunity.

GND

INPUTS

VALID HIGH

VALID LOW

Noise margins specify the maximum amplitude noise pulse that will not change the state of a driven stage, assuming the driving stage presents a worst-case logic level to the driven stage. Specifically, the high-level and the low-level noise margins (NM_H and NM_L) are defined as:

$$\begin{split} NM_H = & V_{OH} - V_{IH}, \\ NM_L = & V_{IL} - V_{OL}, \end{split}$$

where the voltage values are the guaranteed worst-case extremes for each case. Figure 13 shows the noise margins for several different interfaces.

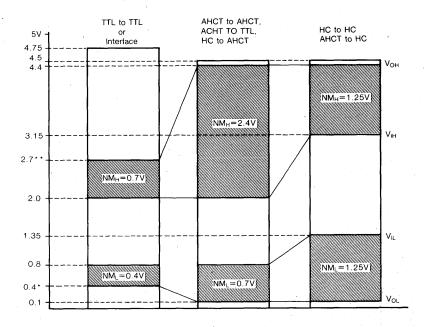


FIGURE 13. Noise margins for various interfaces. Noise margins for HCTLS are the same as those for AHCT.

- * When an AHCT output drives TTL loads the V_{OH} level will be dependent on how many loads are driven. For example if an AHCT244 drives 60LS loads, the V_{OH} will rise to 0.4V
- ** For some, TTL parts, VOH is 2.4V, instead of 2.7V



It is immediately obvious that the TTL-to-TTL interfaces have the poorest noise immunity and those driven by CMOS have the best. This is due to the rail-to-rail voltage swings of CMOS outputs.

Note the HC logic has almost symmetrical noise margins while AHCT (or HCTLS) has a very large noise margin for high level and a smaller low-level one. This is due to the fact that AHCT (or HCTLS) inputs are designed for direct interface with TTL and NMOS outputs as well as other CMOS. Notice, however, that the low-level noise margin (NML) for AHCT is only 0.1V less than that for HC, which means that it provides nearly as much immunity to ground noise. In addition, since AHCT drive capability is two to four times better than HC, it is less susceptible to noise currents coupled to its outputs. That is, lower stray voltages are induced for a given amount of current coupling than for HC.

ESD PROTECTION

Historically, MOS devices have always been considered to be more susceptible to damages due to electrostatic discharges (ESD), which can occur during handling and assembly procedures. However, the new protection circuitry, design, and special processing used for AHCT and HCTLS have improved the ESD immunity for these devices where it is now much better than that of bipolar logic.

Figure 6 and 8 show the input and output ESD protection circuitry employed. All AHCT and HCTLS pins are protected to ESD levels typically greater than ±2kV, the tests are conducted using the "human-body" model that is shown in Figure 14.

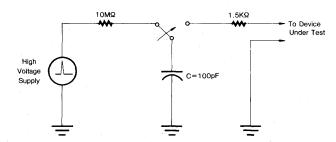


FIGURE 14. Test circuit used to measure ESD damage in AHCT and HCTLS circuits.

LATCHUP CHARACTERISTICS

SCR iatchup is an undesirable parasitic phenomenon which is inherent in circuits fabricated using bulk CMOS technology. A parasitic four-layer (P-N-P-N) SCR structure that appears between V_{CC} and ground can be triggered when voltages greater than V_{CC} or less than ground are applied to inputs or outputs. When this happens, V_{CC} gets effectively shorted to ground, and the only way to get the device off the latchup mode is to shut off the power supply. If large currents are allowed to flow through the chip, it may be destroyed. Samsung CMOS logic parts have been designed and processed to virtually eliminate this possibility in real-life situations where voltages out of the supply range many appear at the input or output pins (overshoots, undershoots, power-up & power-down situations).



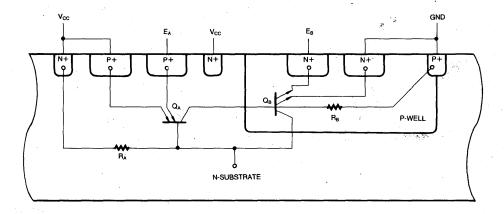


FIGURE 15. Simplified cross section of a CMOS inverter

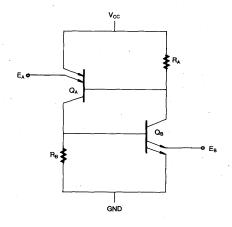


FIGURE 16. CMOS SCR structure

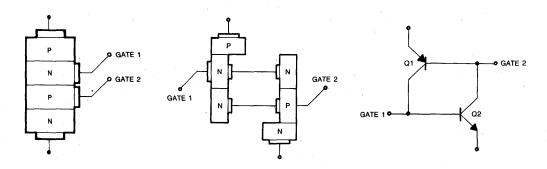


FIGURE 17. Simplified four layer SCR structure



The parasitic SCR structure in a CMOS inverter cross section is illustrated in Figure 15, where vertical and lateral NPN and PNP transistors are formed back-to-back by the N and P diffusions. R_A and R_B are the P-well and the N-substrate power supply connections. Figure 16 is a schematic representation of this parasitic structure that looks like a cross-coupled transistor model of an SCR (Figure 17). The exceptions are the R_A and R_B resistors and the fact that the real SCR is triggered at the gates, while the CMOS parasitic SCR is triggered at its emitters. This happens when either the E_A is raised above V_{CC} enough to turn on Q_A , or E_B is lowered below ground enough to turn on Q_B . When E_A is brought above V_{CC} , current is injected from the emitter of Q_A and is swept to its collector. This current, in turn, will increase the voltage at the Q_B gate and once it is above 0.7V, Q_B will turn on and feed current from its collector back into R_A and into Q_A . When 0.7V drop appears across R_A , Q_A will turn on even more.

If the two transistors have enough gain and enough current is provided by the supply to sustain the SCR, it will turn on and remain on even after E_A and E_B are returned to the rail voltages. Notice that low resistor values effectively reduce the gain of the transistors by stealing current away from their bases. Therefore, transistors should actually have much higher gains in order to have an overall SCR loop gain greater than one and enable SCR to trigger.

Samsung CMOS logic parts are designed and processed to have very low R_A, R_B values and low gains for the parasitic transistors. In addition, large diodes exist between each signal pin and the supply rails to shunt out voltages above V_{CC} and below ground. In fact, traditionally, one refers to the current that flows through these diodes as the element that triggers latchup, i.e. we talk of "latchup trigger currents", not voltages.

Measured on a static basis, i.e. by applying DC voltages above V_{CC} and below ground, Samsung parts can withstand currents typically well above 200mA-even under the worst-case conditions of 7V V_{CC} and +125°C operation. Figure 18 illustrates the test set-up used for static latchup tests.

A common occurence of voltages above V_{CC} and below ground in systems is overshoots and undershoots that are caused by signal line ringing and power supply transients. In this case, unlike the static operation, only short pulses cause forward-bias diode currents and hence possible latch-up. It turns out, fortunately, that the parasitic SCR has extremely slow response time to transients, i.e. very poor frequency characteristics. *Figure 19* shows the increased peak currents required to latch an AHCT or HCTLS device up when the pulse width is decreased. For pulse widths in the range of several tens of nanoseconds, it is virtually impossible to latch the device up.

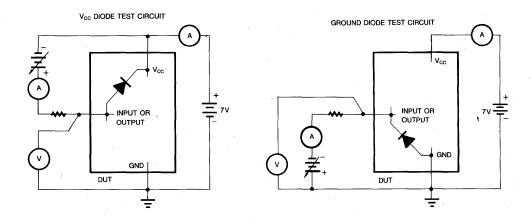


FIGURE 18. Test setup for measuring DC latch-up

T.=25°C

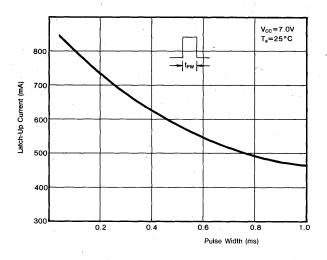


FIGURE 19. Pulsed latch-up characteristics

POWER DISSIPATION

Low power dissipation is by far the most important advantage of CMOS over any other technology. Particularly in the quiescent state, the AHCT and HCTLS circuits consume up to seven orders of magnitude less power than the equivalent TTL functions. This makes them ideal for battery-operated or ultra-low power systems where the system may be put to "sleep" by shutting off the system clock.

The dynamic power dissipation, however, depends on:

- 1. Cross-over currents of the internal CMOS transistors,
- 2. Internal load capacitances,
- 3. External load capacitances, and
- 4. Input voltage levels.

All of the above add up every time there is a logic transition and dynamic power dissipation is the sum of these contributions averaged at a given operating frequency. A practical formula is developed to calculate the dynamic power dissipation (P_D) resulting from the first three items: (input voltage transitions are rail-to-rail)

$$P_D = (C_L + C_{PD}) V_{CC}^2 f$$

where C_L is the load capacitance; C_{PD} is the "internal power dissipation capacitance", V_{CC} is the supply voltage and f is the operating frequency. The C_{PD} value, as specified in each data sheet, sums up the contributions of the first two factors (crossover currents and internal load capacitances) as a capacitance value for purposes of this calculation. The equation indicates that the dynamic power dissipation is directly proportional to frequency.

The contribution of the fourth factor listed above, the input voltage levels, can also be significant when AHCT or HCTLS inputs are driven by TTL outputs. Figure 20 shows the typical crossover currents generated at the input inverer stage as the input voltage swings from O to V_{CC} . This is because both the n-channel and the p-channel transistors turn on partially and provide a low-resistance current path between V_{CC} and ground when the input voltage is near the threshold voltage of the complementary pair. At 2.7V, which is the worst case V_{OH} for TTL parts, the I_{CC} can be as high as 0.5mA per input. This has to be taken into account when calculating the worst-case power dissipation of an AHCT or HCTLS part operating in a TTL environment.



Figure 21 shows the internal power dissipation for an AHCT244 (same for HCTLS244) and compares it with the dynamic power dissipation for LS, ALS and F244. It can be seen that the curves for the bipolar parts are essentially flat for frequencies up to 1 MHz where the quiescent currents mask out the dynamic effects. However, as the frequency goes up, the currents that charge the internal capacitances start adding to the quiescent currents and increase the overall power dissipation. The AHCT244 driven by worst-case TTL voltage levels (all inputs, 50% duty cycle) displays a similar trend but still dissipates an order of magnitude less power than the lowest-power TTL. When CMOS input voltage levels are used, however, the power dissipation is directly proportional to frequency as predicted by the above mentioned formula, and is less than those for the TTL parts, Although the power dissipation becomes comparable to ALS levels at around 10MHz, a crossover does not happen below 50MHz, which is already beyond the maximum clock frequencies of most systems. This behaviour is pretty much the same for all parts in the AHCT and HCTLS families.

In calculating the power dissipation of a system, however, note that only a small percentage of the devices operate at the maximum clock frequency while others operate at a fraction of that. Therefore the average operating frequency tends to be much lower where CMOS has a clear advantage.

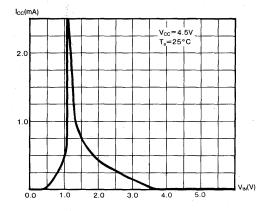


FIGURE 20. Typical crossover current of an AHCT or HCTLS input.

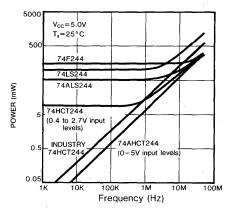


FIGURE 21. Typical dynamic power consumption (no-load) of the 74XXX240 octal buffer with all inputs toggling.

AC CHARACTERISTICS

All AHCT and HCTLS parts are designed to meet or exceed the ALS and LS propagation delay specifications, respectively. Coupled with the equivalent drive capability, this makes them ideal replacements for the ALS and LS in existing designs. In addition the AC specifications for AHCT and HCTLS parts are improved to reflect more realistic design situations. First of all, unlike LS, the AHCT & HCTLS propagation delays are specified with a 50pF load for all part types and guaranteed over the entire voltage and temperature ranges (5V±10%, -40°C to +85°C). Standard LS propagation delays are specified with a 15pF load and guaranteed only at room temperature and 5V V_{CC}. In addition, all bus drivers specify the propagation delays with a 150pF load capacitance to enable the designer to predict a worst-case maximum speed degradation due to capacitive loading.

The effect of the supply voltage variations on propagation delay is illustrated in *Figure 22* for a bus-driver (AHCT244). It can be seen that the parts are functional over a very wide range of voltages and that they slow down as V_{CC} goes down. However, propagation delays are specified and guaranteed only over the 4.5 to 5.5V range.

Figure 23 shows the effect of temperature on the propagation delays for the same part. As for all CMOS circuits, AHCT and HCTLS parts slow down as temperature goes up. Typically speeds derate linearly from 25°C at about 0.02 ns/°C. The propagation delay at any temperature (between -55°C and +125°C) can therefore be calculated using the following formula:

 $t_{PD}(T)=t_{PD}(25^{\circ}C)+k_{T}(T-25^{\circ}C)$

where:

tPD (T)=Propagation delay at the desired T temperature,

tpD (25°C)=Propagation delay at 25°C,

k_T=Temperature derating factor=0.02 ns/°C

The effect of capacitive loading of the outputs on the propagation delay is illustrated in *Figure 24*: the higher the load capacitance, the slower the propagation delay gets. To determine the maximum limit for propagation delay at any value of capacitive loading up to 500pF, the following equation is used:

$$t_{PD} (C_L) = t_{PD} (50pF) + k_C (C_L - 50pF)$$

where:

tpD (CL)=Maximum propagation delay at the desired CL,

tPD (50pF)=Maximum propagation delay from device data sheet,

k_C=Maximum multiplicative factor (ns/pF):

- 0.04 for standard outputs, and
- 0.02 for bus-drivers.

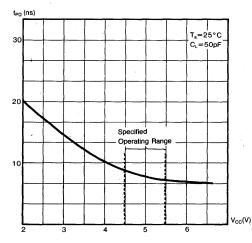


FIGURE 22. Propagation delay versus supply voltage for an AHCT244.

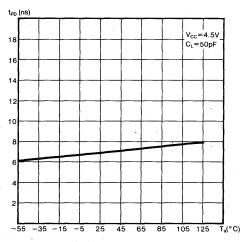
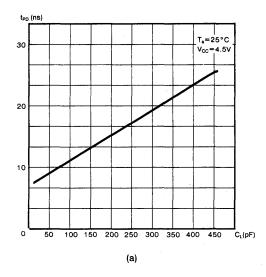


FIGURE 23. Propagation delay versus ambient temperature for an AHCT244.





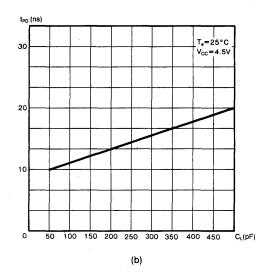


FIGURE 24. Propagation delay versus capacitive load for a (a) standard output (HCTLS00), (b) bus-driver output (HCTLS374)

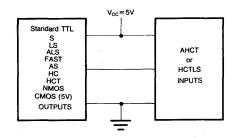
INTERFACING 54/74AHCT AND 54/74HCTLS WITH OTHER LOGIC FAMILIES AND LOADS

Speed and power, while paramount in the initial choice of a logic family, are not the only basis of decision. Another very important factor is the interface flexibility: the inherent capacity of a family to interface with other types of logic and to drive various loads. The Samsung CMOS logic families have this very attractive feature that they can easily be interfaced to all other kinds of digital logic with minimal or no external components.

AHCT and HCTLS parts can be coupled directly with all other TTL, NMOS and CMOS parts if they operate from the same supply voltage. The list includes Standard TTL, Schottky(S), Low-Power Schottky(LS), Advanced Low-Power Schottky(ALS), Advanced Schottky (AS and FAST); all industry-standard CMOS logic families (HC, HCT, CD4000, 14000); all bipolar, NMOS and CMOS microprocessors, microcontrollers, peripherals and memory circuits (see figure 25). This is due to the TTL-compatible input voltage levels coupled with CMOS (rail-to-rail) output voltage swings.

Interface with ECL logic, however, requires external components as shown in Figure 26.

Methods of interfacing with standard CMOS logic families (4000 and 14000), when supply voltages are different, are illustrated in *Figure 27* and *28*.



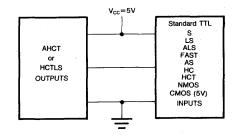


FIGURE 25. Interfacing with TTL, NMOS and other CMOS logic. No extra components are needed.



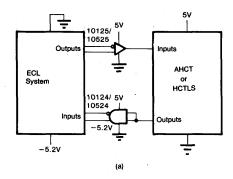
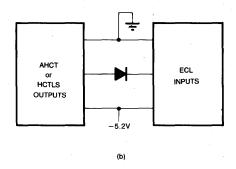


FIGURE 26. (a) General ECL interface



(b) Driving ECL from same power supply.

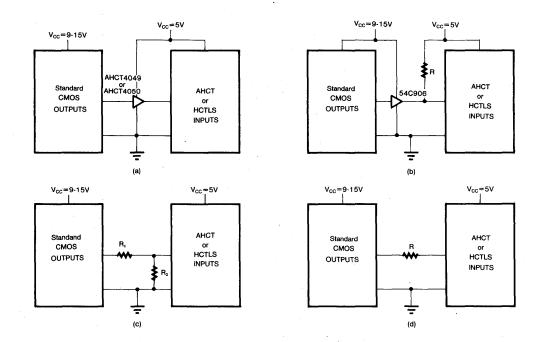


FIGURE 27. Methods of interfacing standard CMOS (4000 and 14000 series) outputs with AHCT and HCTLS inputs when supply voltages are different.

- (a) Using logic down converters,
- (b) Using Open-drain CMOS
- (b) Using resistor divider (V_{OH}·R₂/(R₁+R₂)≤5V)
- (d) Using series resistor



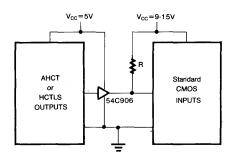


FIGURE 28. Interfacing AHCT and HCTLS outputs with standard CMOS (4000 and 14000) using an open-drain CMOS circuit.

High Voltage and Industrial Control Interfaces

Interfacing with high voltage industrial control circuitry where 4000 or 14000-type of CMOS logic is used has been described in *Figure 27* and *28*. In rugged industrial and automotive environments, more care may be required to prevent large transients from harming AHCT and HCTLS logic. *Figure 29* shows a typical connection that utilizes external diode clamps for input and output protection. The values of R₁ and R₂ depend on the output voltage of the driving circuit and C depends on the noise level and speed. The values of R₃ and R₄ depend on supply voltage and transistor type.

Driving Relays

The high-drive of AHCT and HCTLS outputs enable direct interface with relays, but additional isolation is recommended. Clamp diodes can be used to prevent spikes generated by the relay from harming the circuit. For higher current drive, an external transistor may be employed (*Figures 30* (a) and (b)). Alternatively, multiple gates may be connected in parallel to increase the current sinking and sourcing capability.

Driving LED's

Any AHCT or HCTLS output can be used to drive light-emitting diodes (LED's) directly. Figure 31 shows two methods of doing this. The resistor performs the founction of current limiter. The luminous intensity of the LED depends on the amount of forward current.

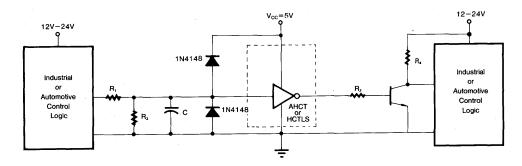


FIGURE 29. Interfacing between AHCT/HCTLS logic and high-voltage industrial and automotive circuitry in rugged environments.



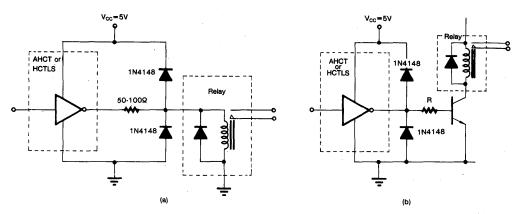


FIGURE 30. Methods of driving relays. (a) Direct and (b) Through a transistor for higher drive $(R = V_{CC} - 0.7)/I_C/\beta)$).

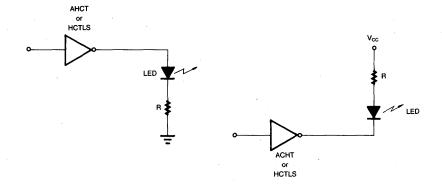


FIGURE 31. Methods of driving LED's

Design Tips

Although the AHCT and HCTLS families are functionally equivalent to the ALS and LS families, some conditions have to be satisfied in order to be able to simply replace them in existing designs. The AHCT and HCTLS families essentially integrate TTL and CMOS characteristics into one family. Therefore, in general, the do's and don'ts of both families apply to the AHCT and HCTLS.

- Don't leave any AHCT or HCTLS input floating. This is frequency overlooked problem with bipolar devices although it is discouraged by every bipolar manufacturer. CMOS inputs have extremely high input impedance and if left unterminated, can pick up noise that causes excursions through the threshold. The result is random switching of the device and high power consumption which can be excessive, especially if the inputs stay very close to the device threshold. Prolonged exposure to these conditions can damage the device. The thing to do is to simply tie the unused inputs to V_{CC} or ground (or they can be tied to nearest operational pin although this may cause more power consumption).
- Don't power up inputs before both V_{CC} and ground are connected, and don't plug boards into or out of powered connectors unless input currents are limited to the absolute maximum ratings specified for the device, and are short-lived. Both conditions can forward bias the input and output ESD protection diodes, resulting in excessive diode currents (see *Figure 32*). If these conditions cannot be avoided, one of the following methods should be used to prevent damage to the AHCT/HCTLS circuits:
- Use connectors that apply power before signals.
- Add series resistors at each input to limit currents to the absolute maximum ratings (Figure 33a).
- Add logic to board interfaces that forces all outputs to either ground or high-impedance state when they are connected
 to unpowered devices (Figure 33b).
- Add logic to board inputs to prevent direct interface with unpowered HCTLS inputs (Figure 33c). Circuits designed for this purpose are 74AHCT4049 (Hex Inverting Logic Level Down Converter) and 74AHCT4050 (Hex Logic Level Down Converter). These parts have a modified input protection structure that enables them to be used as logic level translators which convert high-level logic to low-level logic while operating from the low logic supply. In this case, since the low logic supply is zero (unpowered), the outputs of the 4049 and 4050 will always be zero regardless of the inputs.

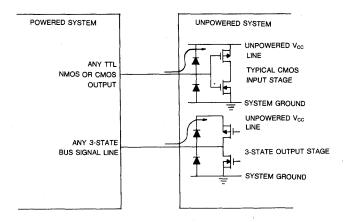


FIGURE 32. Direct interface to unpowered CMOS ICs presents a dangerous situation where high-level signals forward-bias input and output protection diodes and try to "power-up" the Vcc line.

Excessive currents at such an interface can cause damage to the circuitry.



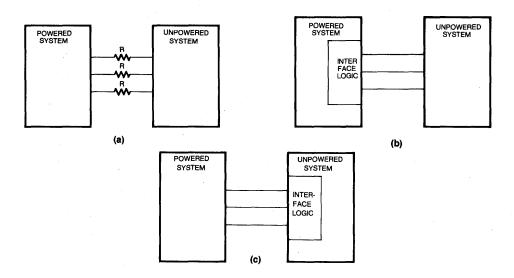


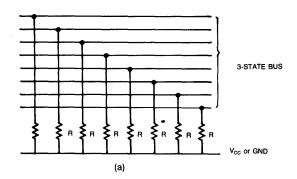
FIGURE 33. Methods of protection in power-down situations: (a) Use of series resistors to limit input currents to absolute maximum ratings, (b) Interface logic circuitry that forces all outputs to either ground or high-impedance state, (c) Interface circuitry at board inputs that acts as buffer between powered and unpowered devices; ideal components for this purpose are the 74AHCT4049 and 74AHCT 4050 Hex Logic Level Down Converters that lack the V_{CC} diode in their protection circuitry.

- In bus-oriented systems, don't allow the bus to stay in high-impedance state for extended periods of time if it is not terminated, because this will have the same effect as leaving inputs open. Two simple ways of terminating the bus are illustrated in *Figure 34*. Most microprocessor-based systems, however, do not keep the bus in 3-state for long periods, in which case, the bus capacitance can maintain valid logic levels. In these cases, pull-up or pull-down circuitry may not be necessary.
- •The edge-rates of the AHCT and HCTLS part are similar to the very high-speed TTL parts. Therefore, system grounding and supply-decoupling techniques normally employed in high-speed TTL designs should be duplicated in AHCT/HCTLS designs to ensure proper operation. A good rule of thumb to reduce the affects of PC board trace inductance is to place 0.01 to 0.1 µF RF-grade capacitors every two-to-five ICs (octal flip-flops and buffers may require more decoupling). This, of course, has to be accompanied by careful pc board layout to minimize these inductances.
- The testing problems encountered in ALS, LS and FAST apply also to AHCT and HCTLS. Most of these problems
 result from the noise produced by the interactions of the device being tested and the test system. Typical test fixtures
 have lead inductances several times that of a PC board socket. This inductance, especially in the device ground path is
 the source of these problems.

The outputs, for example, can cause transient currents in the 50 to 200 mA range within a couple of nanoseconds while changing state. These appear as changes in the voltage drop across the device ground lead. The test system's input and output reference voltages are set with respect to tester ground and are not affected by these transients. Consequently the effective input voltages to the device will vary. If the ground pin goes up 1 volt, all the inputs effectively go down 1 volt. This must be considered in selecting input and output voltage levels. In functional tests, for example, solid input logic levels should be applied, instead of 0.8 and 2.0 volts.

Furthermore, if TTL test programs are to be used, one must be particularly careful not to apply voltages to inputs and outputs that are below ground or above V_{CC} in excess of the absolute maximum limits specified in the data sheets.





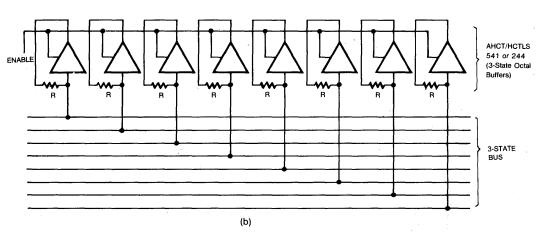
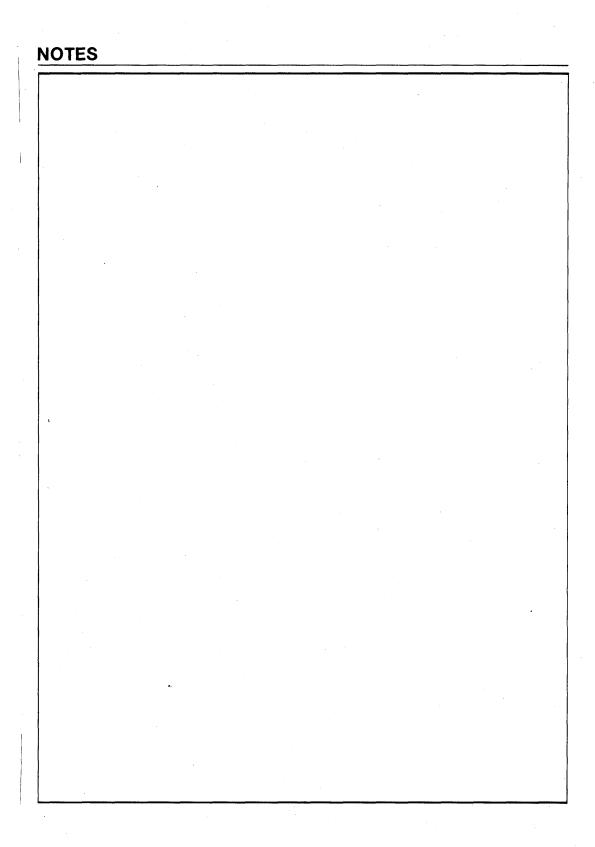
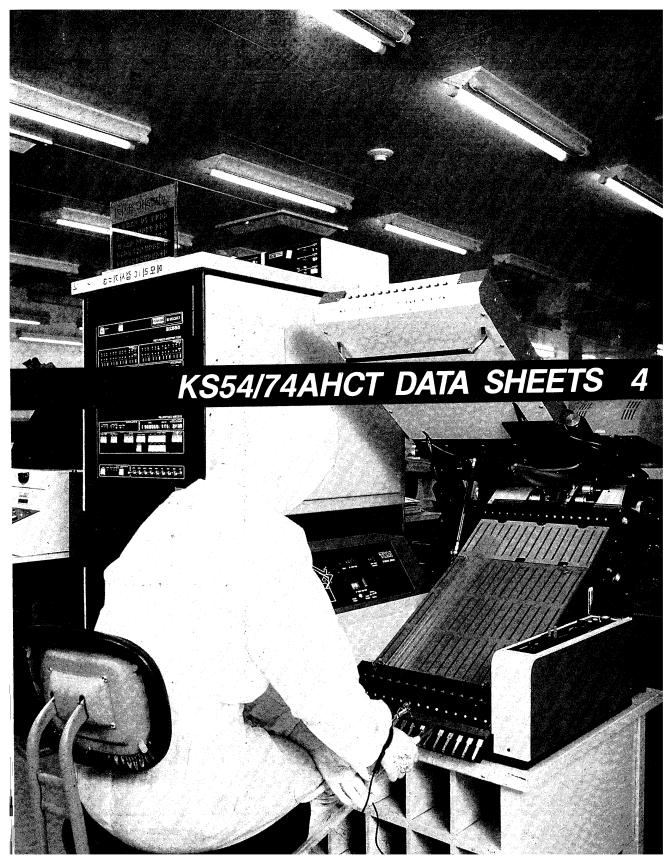
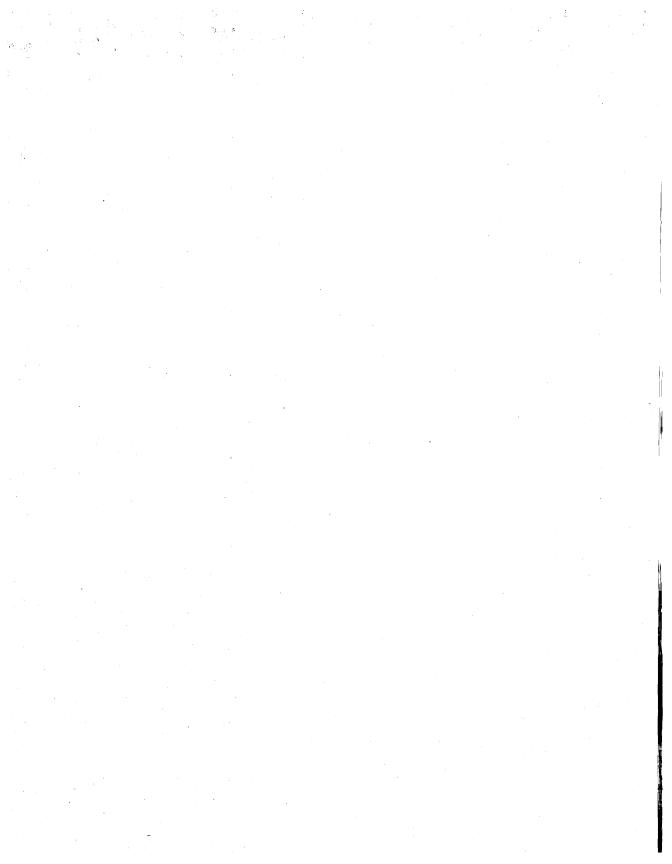


FIGURE 34. Methods of terminating 3-state buses; (a) Pullup or pulldown resistors (b) Use of 3-state buffers. The latter approach terminates the bus to the last active logic level and dissipates no static power.









FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

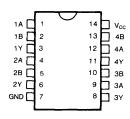
DESCRIPTION

These devices contain four independent 2-input NAND gates that perform the Boolean functions $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$

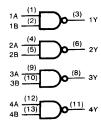
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



(Each Gate)

Inp	uts	Output
A	В	Υ
Н	Н	L
L	Χ	Н
X	L	H

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	p
Supply Voltage, Vcc	4.5V to 5.5V
DC Input & Output \	/oltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Temperatu	ıre
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall Tim	ies, t_r , t_f Max 500 ns
Unused inputs must voltage level (eithe	always be tied to an appropriate logicer V _{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	bol Test Conditions		a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit		
			Тур	yp Guaranteed Limits					
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧		
Minimum High-Level Output Voltage	VoH	V _{IN} =V _{IH} or V _{IL} I _O =-20μA I _O =-4mA	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} = 0.1	v		
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCTOO

Characteristic	Symbol	l Conditions†	T _a = 25°C V _{CC} = 5.0V Typ	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit
				Min	Max	Min	Max	1
Propagation Delay	tpLĤ	C ₁ = 50pF	7		11		14	ns
	t _{PHL}	OL-30bi	8		11		14] '''
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15				,	pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}$

[†] For AC switching test circuits and timing waveforms see section 2.



4

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 IoL = 8 mA @ Vol = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

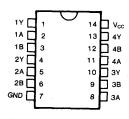
DESCRIPTION

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

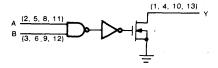
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



(Each Gate)

Inp	uts	Output
Α	В	Y
Н	Н	L
L	Χ	Н
Х	L	н

Supply Voltage Range $V_{CC}, \dots, -0.5V$ to +7V DC Input Diode Current, I_{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stq} 65°C to +150°C
Power Dissipation Per Package, P_d^{\dagger} 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V	cc	4.5V to 5.5V
DC Input & Output	t Voltages*, V _{IN} , V _{OL}	JT OV to Vcc
Operating Temper	ature	
Range	KS74AHCT: ~4	10°C to +85°C
	KS54AHCT: -55	5°C to +125°C
Input Rise & Fall	Fimes, $t_{r},\;t_{f}$	Max 500 ns
	ust always be tied to ar	n appropriate logic

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		7
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin $V_i = 2.4V$ other Inputs: at V_{CC} or GND $I_{OUT} = 0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT01

Characteristic	Symbol Conditions†	T _a = 25°C V _{CC} = 5.0V			to +125°C	Unit		
			Тур	Min	Max	Min	Max	
Propagation Delay	t _{PLH}	C _L =50pF	17		25		29	ns
ropagation belay	t _{PHL}	R _L =1kΩ	10		16		19	113
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}{}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.



FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

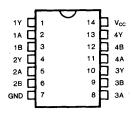
DESCRIPTION

These devices contain four independent 2-input NOR gates that perform the Boolean functions $Y = \overline{A + B}$ or $Y = \overline{A} \bullet \overline{B}$.

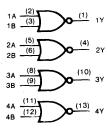
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



(Each Gate)

Inp	uts	Output
A	В	Ý
Н	Х	L
Х	Н	L
L	L	Н

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
(-0.5V < Vo < Vcc +0.5V) ±35 mA
Continuous Current Through
Vcc or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	Vcc		4.5V 1	to 5.5V
DC Input & Outp	ut Voltages*, V _{IN} , V	Vout .	. 00	to Vcc
Operating Tempe	erature			
D	KOZ ANIOT	400		

Range

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
	}		Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT02

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C OV ±10%	KS54 T _a = -55°C V _{CC} = 5.	Unit	
			Тур	Min	Max	Min	Max]
Propagation Delay	tpLH	C _L =50pF	7.		- 12		14	ns
Propagation Delay	t _{PHL}		7		12		14] ""]
Input Capacitance	Cin		5					рF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15					pF

^{*} CPD determines the no-load dynamic power dissipation: $P_D = C_{PD} |V_{CC}|^2 f_{in-}^2$

[†] For AC switching test circuits and timing waveforms see section 2



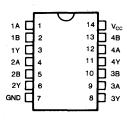
FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Rackage options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

(Each Gate)

inp	uts	Output
A	В	Y
Н	Н	L
L	Χ .	. H
Х	L	н

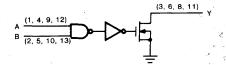
DESCRIPTION

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



Supply Voltage Range V _{CC} ,0.5V to +7V DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, Iok
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) + \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	Supply Voltage, V _{CC}	4.5V to	5.5V
•	DC Input & Output Voltages*, VIN, VOUT	OV t	o Vcc
	Operating Temperature		

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic S	Symbol	Test Conditions	Ta	= 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	Ö	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT03

Characteristic	Symbol	Conditions†	$T_a = 25^{\circ}C$ $V_{CC} = 5.0V$ Typ	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit
•				Min	Max	Min	Max	
Propagation Delay	tpLH	C _L =50pF	17		25	,	29	ns
Propagation Delay	tPHL	$R_L=1k\Omega$	10		16		19	113
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15	.,				pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-}

[†] For AC switching test circuits and timing waveforms see section 2.



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FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

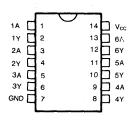
DESCRIPTION

These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

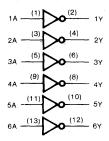
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Inverter)

Input	Output
Α	Y
Н	L
. , L	Н,

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, P_d^{\dagger} 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, V_{IN} , V_{OUT} . . 0V to V_{CC} Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_{r_1} t_{f_1} Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74AHCT $T_a = -40$ °C to +85°C	KS54AHCT $\Gamma_a = -55$ °C to $+125$ °C	Unit
			Тур		- Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCTO4

Characteristic	Symbol	T _a = 25°C Conditions [†] V _{CC} = 5.0V		KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	tpLH	C _L =50pF	7		11		14	ns
Propagation Delay	tPHL		7		11	1	14] '''
Input Capacitance	CiN		5				·	рF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15					pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin. Icc Vcc.

For AC switching test circuits and timing waveforms see section 2.



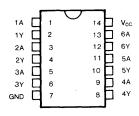
FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



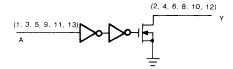
DESCRIPTION

These devices contain six independent inverters with opendrain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



(Each Inverter)

Input	Output
A	Υ
Н	L
L	H

Supply Voltage Range V_{CC} ,0.5V to +7V DC Input Diode Current, I_{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	,		4.5V	to 5.5V
DC Input & Output Vo	oltages*, V _{IN} ,	V_{OUT}	0\	to Vcc
Operating Temperatur	re			
_	MOTAL HOT	40		

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT KS54AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $T_a = -55^{\circ}\text{C to } +125^{\circ}$		
	İ		Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{iN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V_I =2.4V other inputs: at V_{CC} or GND I_{OUT} =0 μ A		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT05

Characteristic	Symbol	Symbol Conditions†	$T_a = 25^{\circ}C$ $T_a = -6^{\circ}C$		$T_a = -40^{\circ}$	KS74AHCT = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT $T_a = -55^{\circ}\text{C to } +125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Тур	Min	Max	Min	Max		
Propagation Delay	t _{PLH}	C _L =50pF	17		25		29	ns	
	t _{PHL}	$R_L=1k\Omega$	8		. 14		33	113	
Input Capacitance	CIN		5					рF	
Power Dissipation Capacitance*	C _{PD}	(per inverter)	15			_		pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in} cc V_{CC}

[†] For AC switching test circuits and timing waveforms see section 2.



4

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 One of the control of the con

and CMOS devices

- $I_{OL}=8$ mA @ $V_{OL}=0.5V$ Inputs and outputs interface directly with TTL, NMOS
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

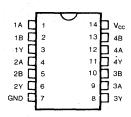
DESCRIPTION

These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$.

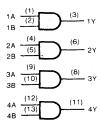
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



(Each Gate)

inp	uts	Output
A	В	Υ
Н	Н	Н
L	X	Ĺ.
X.	L	L

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IoK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{C0} DC Input & Output Operating Temperat	/oltages*, V_{IN} , V_{OUT} 0V to V_{CC}
Range	KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_t Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT $T_a = -40$ °C to +85°C	KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
	!				Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	ΔΙςς	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT08

Characteristic	Symbol	Symbol Co	Conditions†	T _a = 25°C V _{CC} = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C 0V ± 10%	$KS54$ $T_a = -55^{\circ}C$ $V_{CC} = 5.0$	Unit
			Тур	Min	Max	Min	Max]
Propagation Delay	tpLH	C _L =50pF	8		14	•	17	ns
	t _{PHL}	OL-30bi	8		14		17	113
Input Capacitance	CiN		5					pF
Power Dissipation Capacitance*	CPD	(per gate)	15					рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.



4

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- . Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 IoL = 8 mA @ Vol = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

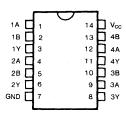
DESCRIPTION

These devices contain four independent 2-input AND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

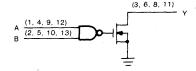
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



(Each Gate)

Inp	uts	Output
A	В	Y
Н	H,	Н
L	Χ	L
Х	L	L.

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, $t_{r},\;t_{f}$ Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
					Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Maximum Low-Level Output Voltage	V _{OL}	V_{IN} = V_{IH} or V_{IL} I_{O} = $20\mu A$ I_{O} = $4mA$ I_{O} = $8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	loc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCTO9

Characteristic	Symbol	$\begin{array}{c} \text{T}_a = 25^{\circ}\text{C} \\ \text{V}_{CC} = 5.0\text{V} \\ \end{array} \\ \begin{array}{c} \text{KS74AHCT} \\ \text{T}_a = -40^{\circ}\text{C to } + 85^{\circ}\text{C} \\ \text{V}_{CC} = 5.0\text{V} \pm 10\% \\ \end{array}$		KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V± 10%		Unit		
	1		Тур	Min	Max	Min	Max	
Propagation Delay	tPLH	$C_L=50pF$ $R_L=1k\Omega$	18		27		31	ns
	t _{PHL}		9		15		18	""
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15					pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

[†] For AC switching test circuits and timing waveforms see section 2.



- . Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

· Package options include "small outline" packages

(Available Tape & Reel), standard DIPs.

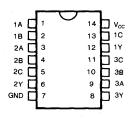
DESCRIPTION

These devices contain three independent 3-input NAND gates. They perform the Boolean functions Y=A•B•C or $Y = \overline{A} + \overline{B} + \overline{C}$.

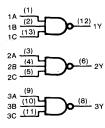
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

	Inputs	Output	
A	В.	С	Y
Н	Н	Н	L
L	X	×	н
X.	L	X	н
Х	×	L	Н

Supply Voltage Range V _{CC} , −0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I _{OK}
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
Vcc or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
 Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, 1	V _{CC} 4.5V to 5.5V
DC Input & Outp	ut Voltages*, V _{IN} , V _{OUT} 0V to V _{CC}
Operating Tempe	erature
Range	KS74AHCT: ~40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall	Times, $t_r,\;t_f$ Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	mbol Test Conditions	Ta = 25°C		KS74AHCT $T_a = -40$ °C to $+85$ °C	KS54AHCT T _a = -55°C to +125°C	Unit		
			Тур	yp Guaranteed Limits					
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	v		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧		
Minimum High-Level Output Voltage	V _{ОН}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V		
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧		
Maximum Input Current	IIN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ		
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input tr, tre2 ns), AHCT10

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit	
			Тур	Min	Max	Min	Max	1
Propagation Delay	tpLH	C _I =50pF	. 9		15		18	ns
Propagation Delay	tPHL	OL-30Pi	9		15		18] '''
Input Capacitance	CiN		5					pF
Power Dissipation Capacitance*	CPD	(per gate)	15					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \; V_{CC}{}^2 \; f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.



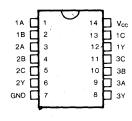
- · Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$
- . Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



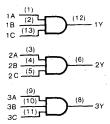
DESCRIPTION

These devices contain three independent 3-input AND gates. They perform the Boolean functions Y=A•B•C or $Y = \overline{A} + \overline{B} + \overline{C}$.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

	Inputs		Output
A	В	С	Y
Н	Н	Н	Н
L	·X	X	L
X	L	X	L
Х	X	L	L

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
Vcc or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Symbol Test Conditions		= 25°C	KS74AHCT T _{a=-40°C} to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
					Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	VoL	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tr<2 ns), AHCT11

Characteristic	Symbol	ol Conditions [†] $V_{CC} = 5.0V$	$T_a = -40^\circ$	AHCT C to +85°C 0V ± 10%	$KS54$ $T_a = -55^{\circ}C$ $V_{CC} = 5.0$	AHCT to +125°C V ± 10%	Unit	
			Тур	Min	Max	Min	Max	
Propagation Delay	tpLH	C _L =50pF	9		15		18	ns
Topagation Delay	t _{PHL}	$R_L=1k\Omega$	9		15		18	113
Input Capacitance	CIN		5					рF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15					рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.



4

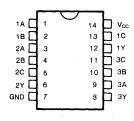
FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: IoL = 8 mA @ VoL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges;

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

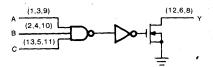
These devices contain three independent 3-input NAND gates with open-drain outputs. They perform the Boolean functions $Y = \overline{A \bullet B \bullet C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$.

Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

	Inputs	Output	
A	В	С	Ý
Н	Н	Н	Ĺ
L	X	Х	н
Χ	L	Х	н
Χ	X	L	Н

Supply Voltage Range V_{CC} ,0.5V to +7V DC Input Diode Current, I_{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vcc			4.	5V t	o 5	5.5V
DC Input & Output V	/oltages*, V _{IN} ,	Vout		0٧	to	V_{CC}
Operating Temperatu	ıre					
D	LOT ALLIOT	40		4 -		

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to.+125°C

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Τa	=25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}	·		2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	o	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT12

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	$T_a = -40^\circ$	4AHCT C to +85°C 0V±10%	$T_a = -55$ °C $V_{CC} = 5.0$	to +125°C	Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	t _{PLH}	C ₁ = 50pF	19		27		31	ns
1 Topagation Delay	tPHL	OL-SOPI	11		18		22	113
Input Capacitance	CIN		5		,			рF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15					рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

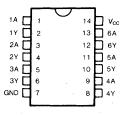


- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 (2744107) (2824107) (2824107)

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



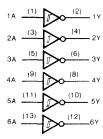
DESCRIPTION

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



FUNCTION TABLE

(Each Inverter)

Input	Output
A	Y
Н	L
L	Н

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
Vcc or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т	a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	VCC 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.11	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_0=20\mu A$ $I_0=4mA$ $I_0=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc -	V _{IN} =V _{CC} or GND Ι _{Ουτ} =ΟμΑ		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	T _a =	25°C	KS74	IAHCT C to +85°C	KS54	IAHCT to +125°C	Unit
Gharacteristic	- Cymbol	rest conditions	Min	Max	Min	Max	Min	Max].
Positive-Going	V _{T+}	V _{CC} =4.5V	1.2	1.9	1.2	1.9	1.2	1.9	V
Threshold Voltage	VI+	V _{CC} =5.5V	1.4	2.1	1.4	2.1	1.4	2.1	"
Negative-Going	V _T _	V _{CC} =4.5V	0.5	1.2	0.5	1.2	0.5	1.2	V
Threshold Voltage	• -	V _{CC} =5.5V	0.6	1.4	0.6	1.4	0.6	1.4	"
Hysteresis	VH	V _{CC} =4.5V	0.4	1.4	0.4	1.4	0.4	1.4	v
$(V_{T+}-V_{T-})$	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	V _{CC} =5.5V	0.4	1.5	0.4	1.5	0.4	1.5	1



AC ELECTRICAL CHARACTERISTICS (Input tr, tres 2 ns), AHCT14

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	$T_a = -40^{\circ}$ $V_{CC} = 5$.	IAHCT C to +85°C 0V ± 10%	$KS54$ $T_a = -55^{\circ}C$ $V_{CC} = 5.0$	AHCT to +125°C V ± 10%	Unit
	1		Тур	Min	Max	Min	Max	
Propagation Delay	t _{PLH}	C _I = 50pF	8		14		17	ns
Topagation Belay	t _{PHL}	OL-30pi	8		15		19	
Input Capacitance	C _{IN}		5					pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15				-	pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

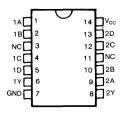
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 IoL = 8 mA @ Vol = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



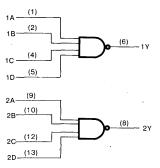
DESCRIPTION

These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \bullet B \bullet C \bullet D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



FUNCTION TABLE

(Each gate)

	INP	UTS	OUTPUT	
Α	В	С	D	Y
Н	Н	Н	Н	L
L	Χ	Χ	Χ	- н
Χ	L	Χ	Χ	. н
Х	Χ	L	X	. н
X	Χ	Χ	L	Н

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, IIK
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I _{OK}
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to V _{CC}
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r , t_t Max 500 ns Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a ≈ 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit	
			Тур		Guaranteed Lim	its	1	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V _{ОН}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v	
Maximum Low-Level Output Voltage	Vol	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT20

Characteristic	Symbol	Conditions	T _a = 25°C V _{CC} = 5.0V Typ	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
				Min	Max	Min	Max] . [
Propagation Delay, Any input to Y	telH	C _i = 50pF	7		11		13	ns
	teht	OL OOD!	7		11		13] '''
Input Capacitance	Cin		5		8			pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

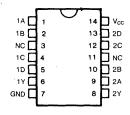


- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

(Each gate)

INP	UTS	OUTPUT	
В	С	D	Y
Н	Н	Н	Н
Χ	Х	Χ	L
, L	X	X	L
Χ	L	Χ	L
Χ	Х	L	L
	B H X L	H H X X L X X L	B C D H H H X X X L X X X L X

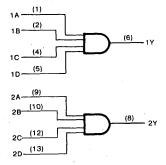
DESCRIPTION

These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y = A \bullet B \bullet C \bullet D$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, V_{IN} , V_{OUT} . OV to V_{CC} Operating Temperature

Range KS74AHCT: -40° C to $+85^{\circ}$ C KS54AHCT: -55° C to $+125^{\circ}$ C Input Rise & Fall Times, t_r , t_t Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT $T_a = -40$ °C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit	
			Тур		Guaranteed Lim	its		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	v	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input t_r , $t_f \leqslant 2$ ns), AHCT21

Characteristic	Symbol	Conditions†	$T_a = 25^{\circ}C$ $V_{CC} = 5.0V$	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^{\circ}\text{C to } +125^{\circ}\text{C}$ $V_{\text{CC}} = 5.0\text{V} \pm 10\%$		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay, Any input to Y	t _{PLH}	C ₁ = 50pF	8		14		17•	ns
	t _{PHL}	оц-зорі	. 8		14		17	
Input Capacitance	CIN		5					рF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

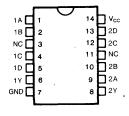


- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 8$ mA @ $V_{OL} = 0.5$ V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



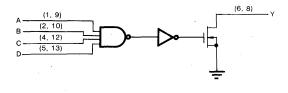
DESCRIPTION

These devices contain two independent 4-input NAND gates. These gates perform the Boolean fucntions $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic. The open-drain outputs require pull-up resistors to perform correctly. They may be connected to other open-drain outputs to implement active low wired-OR or active high wired-AND functions.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

	INP	OUTPUT		
Α	В	С	D	Y
Н	Н	Н	Ĥ	L
L	Χ	Χ,	X	н
×	L	Х	X	H.
X	Χ	L	·X	H
X	Χ	Χ	L .	Н

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, P_d^{\dagger} 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	Vcc		4.5V	to 5.5	٧
DC Input & Outp	out Voltages*, V _{IN} ,	V_{OUT}	0'	√ to Vo	С
Operating Temporating	erature				
Pango	KS74AHCT	-40	°C to	195 °	\sim

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t_r, t_t Max 500 ns Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _{a = -55°C} to +125°C	Unit
			Тур		Guaranteed Lim	its] !
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	\ \ \
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =OμA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT22

Characteristic	Symbol	l Conditions†	T _a = 25°C V _{CC} = 5.0V	KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	C _L =50pF	19		29		34	ns
Any input to Y	t _{PHL}	R _L =1kΩ	11		18		22	,,,5
Input Capacitance	CIN		. 5					pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15			-		pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \; V_{CC^2} \; f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

(Each Gate)

II	NPUT	s	OUTPUT
Α	В	С	Y
Н	Х	Х	· L
. X	Н	X	L
Х	X	Н	L
L	_ L_	L	н

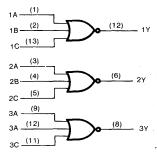
DESCRIPTION

These devices contain two independent 3-input NOR gates. They perform the Boolean functions $Y = \overline{A} + \overline{B} + \overline{C}$ or $Y = \overline{A} \bullet \overline{B} \bullet \overline{C}$ in positive logic.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

Power Dissipation Per Package, P_d† 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74AHCT: -40° C to $+85^{\circ}$ C KS54AHCT: -55° C to $+125^{\circ}$ C Input Rise & Fall Times, t_r , t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic Symb		Test Conditions	T _a = 25°0		KS74AHCT T _{a = -40°C to +85°C}	KS54AHCT T _a = -55°C to +125°C	Unit		
			Тур	Guaranteed Limits					
Minimum High-Level Input Voltage	V _{IH}	,		2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	٧		
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	μΑ		
Additional Worst Case Supply Current	ΔΙ _{CC}	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input t_r , $t_f \leqslant 2$ ns), AHCT27

Characteristic	Symbol Co	Conditions	$T_a = 25$ °C $V_{CC} = 5.0V$	11. = -40°C to +85°CH		KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
S. P. Service				Min	Max	Min	Max] [
Propagation Delay,	tpLH	C ₁ = 50pF	8		14		17	ns
Any input to Y	t _{PHL}	OL-30pi	10		16		20	113
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	CPD	(per gate)	15					рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \, V_{CC}{}^2 \, f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 CTANICT 4090 to 1.95500**

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs:

DESCRIPTION

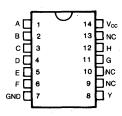
The '30 contains a single 8-input NAND gate. It performs the boolean functions (in positive logic):

Y=<u>A·B·C·D·E·F·G·H</u> Y=A+B+C+D+E+F+G+H

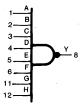
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

Inputs A Through	Output Y	
All Inputs	н	L
One or more inputs	L	Н

Supply Voltage Hange V_{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage,	Vcc	4.5V to 5.5V
DC Input & Out	put Voltages*, V _{IN} , V _O	UT OV to VCC
Operating Temp	erature	•
Range	KS74AHCT: -	40°C to +85°C
	KS54AHCT: -5	5°C to +125°C
Innut Rise & Fa	ll Times t. t.	May 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit	
			Тур	Guaranteed Limits				
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	V _{CC}	V _{CC} −0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1 3.7	v	
Maximum Low-Level Output Voltage	VoL	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA		0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μА	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input t_r , $t_f \!\!\! < \!\!\! < \!\!\! 2$ ns), AHCT30

Characteristic	Symbol	Conditions	T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	tpLH	C ₁ = 50pF	6		11		14	ns
Topagation Bolay	t _{PHL}	CL-30bi	6		11		14	
Input Capacitance	CIN		5					рF
Power Dissipation Capacitance*	CPD		15					рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.



[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · High-Drive-Current outputs: $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

• Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

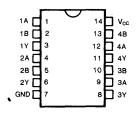
DESCRIPTION

These devices contain four independent 2-input OR gates. They perform the Boolean functions Y = A + B or $Y = \overline{A} \cdot \overline{B}$.

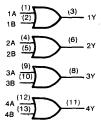
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL. NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damaged due to static discharge by internal diode clamps to Vcc and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

lnp	uts	Outputs
A	В	Y
Н	Х	Н
Х	H	н
L	L	L

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_t Max 500 ns
Unused inputs must always be tied to an appropriate logic
voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74AHCT $T_{a} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r , $t_l \leqslant 2$ ns), AHCT32

Characteristic	Symbol	Conditions	T _a = 25°C V _{CC} = 5.0V	T _a = -40°	IAHCT C to +85°C 0V±10%	$T_a = -55$ °C	AHCT to +125°C V ± 10%	Uni
			Тур	Min	Max	Min	Max	
Propagation Delay	t _{PLH}	C ₁ = 50pF	8	٠.,	14		17	ns
1 Topagation Bolay	t _{PHL}	OL-30bi	9		14		17	113
Input Capacitance	CiN		5					pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15					рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.

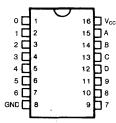


- Full decoding of Input Logic
- . All outputs are High for Invalid BCD Conditions
- Also for application as 3-Line to 8-Line Decoders
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

No.		Inp	uts					C	Out	put	s			
No.	D	С	В	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
1	L	L	L	Н	Н	L	٠Н	Н	Н	Н	Н	Н	Н	Н
2	L	L	Н	L	Н	Н	L	Н	н	Н	Н	Н	Н	Н
3	L	L	Н	Н	Н	Н	Н	L	Н	Н	H	Н	Н	Н
4	L	Н	L	Ł	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
5	L	Н	L	Н	Н	Н	Н	H	Н	L	Н	Н	Н	н
6	L	Н	·H	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н
7	L	Н	Н	H	Н	Н	Н	Н	Н	Н	Н	L	Н	Н
8	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
9	Н	L	L	Н	H	Н	Н	Н	Н	Н	Н	Н	Н	L
	Н	L	н	L	Н	Н	Н	Н	н	H	Н	Н	Н	Н
	Н	L	Н	н	Н	Н	Н	н	Н	Н	Н	Н	Н	Н
INVALID	Н	Н	L	L	н	Н	Н	Н	н	Н	Н	Н	Н	Н
IIIVALID	н	Н	L	Н	Н	Н	н	н	Н	Н	Н	н	Н	Н
	н	Н	Н	L	H.	Н	н	Н	н	Н	н	Н	Н	Н
	н	Н	Н	Η,	Н	Н	Н	н	Н	н	Н	Н	Н	Н

DESCRIPTION

The '42 decoder accepts for active-high BCD inputs and provides 10 mutually exclusive active-low outputs, as shown by logic symbol or diagram. The active-low outputs facilitate addressing other MSI units with active low input enables.

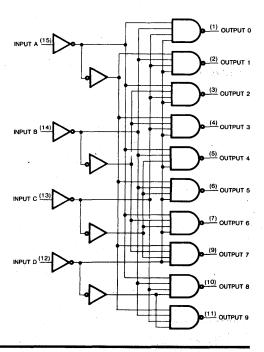
The logic design of the '42 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant input, D, produces a useful inhibit function when the '42 is used as a 1-of-8 decoder. The D input can also be used as the Data input in an 8-output demultiplexer application.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



Supply Voltage Range $V_{CC}, \ldots, -0.5V$ to +7V DC Input Diode Current, I_{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

Recommended Operating Conditions

	roa operaning commission
Supply Voltage, \	CC 4.5V to 5.5V
DC Input & Outpi	it Voltages*, V_{IN} , V_{OUT} 0V to V_{CC}
Operating Tempe	ature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall	Times, t _r , t _f Max 500 ns
	oust always be tied to an appropriate logic ther V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its]
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}	. •		0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{ОН}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	ų
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	l lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT42

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	$T_a = -40^{\circ}$	IAHCT C to +85°C 0V±10%	$T_a = -55$ °C	1AHCT C to +125°C 0V ± 10%	Unit
	1	:	Тур	Min	Max	Min	Max	
Propagation Delay,	tpLH	C _I = 50pF	11		18		22	ns
Any input to Y	t _{PHL}	OL-OOD!	11		18		22	
Input Capacitance	CIN		5					ρF
Power Dissipation Capacitance*	C _{PD}	(per gate)						рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \; V_{CC}{}^2 \; f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.



[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

 $I_{OL} = 8$ mA @ $V_{OL} = 0.5$ V

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs. The '51 performs the following Boolean functions:

 $1Y = (\overline{1A \cdot 1B \cdot 1C}) + (\overline{1D} \cdot 1E \cdot 1F)$

 $2Y = (\overline{2A \cdot 2B}) + (2C \cdot 2D)$

DESCRIPTION

The '58 performs:

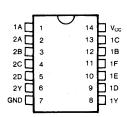
1Y=(1A+1B+1C)+(1D+1E+1F)

2Y=(2A•2B)+(2C•2D)

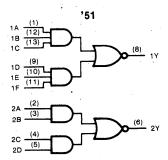
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAMS

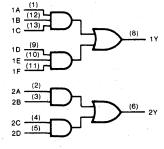


FUNCTION TABLES

	Inputs						ut 1Y
1A	1B	1C	1D	1E	1F	'51	'58
Η.	Н	Н	Х	X	Х	L	Н
Χ	×	X	Н	Н	н	L	Н
	Any	other o	ombina	ation		н	L

	Inp	Outp	ut 2Y		
2A	2B	2C	2D	'51	'58
Н	H	X	Х	L	Н
X	X	н	Н	L	H
An	y other o	ombinatio	on	н	L





Supply Voltage Range V _{CC} , −0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	P	
Supply Voltage, V	′cc	. 4.5V to 5.5V
DC Input & Output	it Voltages*, V _{IN} , V _{OU}	T OV to V _{CC}
Operating Temper	rature	
Range	KS74AHCT: -4	0°C to +85°C
_	KS54AHCT: -55	°C to +125°C
Input Rise & Fall	Times, t _r , t _f	Max 500 ns
	iust always be tied to an ither V_{CC} or GND)	appropriate logic

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т,	= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
		* * * * * * * * * * * * * * * * * * * *	Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	٧
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0µA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT51, AHCT58

Characteristic	Symbol	Ol Conditions†	T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	t _{PLH}	C _L =50pF	9		15		18	ns
r Tobagation Delay	t _{PHL}		9		15	-	18]
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: IoL = 8 mA @ VoL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

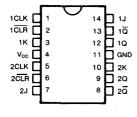
DESCRIPTION

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at $\overline{\text{CLR}}$ input resets the outputs regardless of the levels of the other inputs. When $\overline{\text{CLR}}$ is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

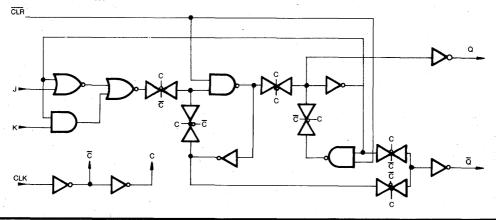
PIN CONFIGURATION



FUNCTION TABLE

	Input	S		Outp	outs .
CLR	CLK	J	K	Q	ā
L	X	X	×	L	Н
н	↓	L	L	Q _o	\overline{Q}_{o}
. н	↓	Н	L	н	L
н	1	L	н .	L	Η.
• н	↓ .	н	н	TOG	GLE
н	Ĥ	X	X	Q _o	$\bar{\mathbf{Q}}_{o}$

LOGIC DIAGRAM



Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

Storage lemperature Hange, Istg...-65°C to +150°C
 Power Dissipation Per Package, Pd[†]......500 mW
 Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND).

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	ymbol Test Conditions		a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit		
			Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $t_O=-20\mu\text{A}$ $t_O=-4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1 3,7	v		
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		4.0	40.0	80.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: at V _{CC} or GND l _{OUT} =0μA		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT73

Characteristic		Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Maximum Clock Fr	equency	f _{max}		45	. 30		25		MHz
Propagation Delay,		tpLH		10		17		20	ns
CLK to Q or Q		tpHL	C _L =50pF	1Ö		17		20	""
Propagation Delay,		tpLH		10		17		20	ns
CLR to Q or Q		tpHL		10		17		20	
Setup Time	J or K	t _{su}		8	13		15		ns
before CLK↓	CLR Inactive	'su		8	13		15		1115
Hold Time, J or K	after CLK↓	th		-3	0		0		ns
Pulse Width CLK High or Low		tw		8	13		15		
Fuise Width	CLR Low	l w		8	13	-	15		ns
Input Capacitance		CIN		5					pF
Power Dissipation	Capacitance*	CPD	(per flip-flop)	40					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

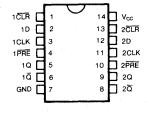
[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These devices contain two independent positive-edge-triggered D-type flip-flops. Each flip-flop has its own data, clock, preset and clear inputs and complementary Q and \overline{Q} outputs. The preset and clear inputs are active-low and operate independently of the clock. Data at the D input is transferred to the Q outputs on the positive transition of the clock, provided setup requirements have been met.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

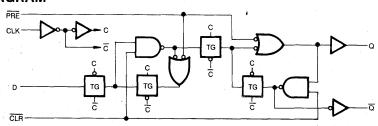
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

	Inpu	ts		Ou	tputs
PRE	CLR	CLK	D	Q	ā
L	H	X	Х	Н	L
H	Ĺ	X	Х	L	Н
L	L	X	. X	H*	H*
H	Н	†	. Н	Н	L
Н	H	†	L	L	Н
Н	Н	L	X	No C	hange
Н	H	Н	Х	No Ci	hange
н	Н	1	Х	No C	hange

^{*}Both outputs will remain high as long as PRE and CLR are low, but the output states are unpredictable if PRE and CLR go high simultaneously.

LOGIC DIAGRAM



Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, $P_d{}^{\dagger}$ 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.
posure to these conditions may affect device reliability.

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

11COOIIIIICIIAC	a operating contactions
Supply Voltage, Vcc	; 4.5V to 5.5V
DC Input & Output \	Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Temperati	ure
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall Tim	nes, t _r , t _f Max 500 ns
Unused inputs mus	t always be tied to an appropriate logic
voltage level (eithe	er V _{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T _{a = -40°C} to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4m A$	V _{CC}	V _{CC} −0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT74

Characteristic				$T_a = 25^{\circ}C$ $V_{CC} = 5.0V$ KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit	
				Тур	Min	Max	Min	Max	
Maximum Clock	Frequency	f _{max}		55	34		30		MHz
Propagation Dela	ay,	tpLH		13		18		19	ns
CLK to Q or Q		t _{PHL}	C _L =50pF	13		18		19	ns
Propagation Delay,		t _{PLH}		9		17		18	
PRE or CLR to	Q or Q	t _{PHL}		9		17		18	113
Setup Time	Data			7	12		15		ns
before CLK†	PRE or CLR Inactive	t _{su}		5	8		10		115
Hold Time, Data	after CLK†	th		0	0		0		ns
Pulse Width	CLK High or Low			9	14		17		
ruise vvidili	PRE or CLR Low	tw		9	15		17		ns
Input Capacitance		CIN		5					рF
Power Dissipation	n Capacitance*	CPD		40					рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - IOL = 8mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74AHCT: -40°C to +85°C

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

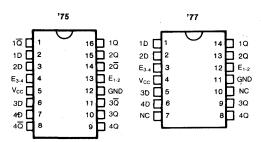
The '75 and '77 consist of 4 high-speed D-type latches that can be used as temporary storage for binary information between processing units. The '75 features complementary Q and $\overline{\rm Q}$ output while the '77 features single nail output. These devices are ideal for high component density application.

The latches are transparent: when the enable (E) is high, the Q output will follow the data input. When the enable goes low, the output latches at the level that was set up at the D-input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

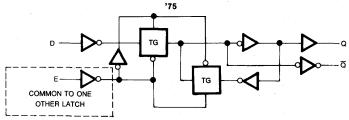


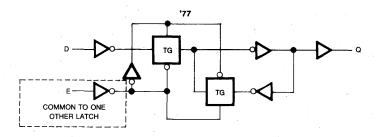
FUNCTION TABLE

inp	uts	Ou	tputs
D	E	Q	Q*
L	Н	L	Н
Н	Н	н	L
X	L	Q_0	$\overline{\mathbf{Q}}_{0}$

*Q: '75 only

LOGIC DIAGRAM





^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

•
Supply Voltage, V _{CC} 4.5V to 5.5V
DC Input & Output Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Temperature
Range KS74AHCT: -40°C to +85°C
KS54AHCT: -55°C to +125°C
Input Rise & Fall Times, tr, tf Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit			
			Тур		Guaranteed Lim	its				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	<			
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧			
Minimum High-Level Output Voltage	V _{OH}	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20\mu A$ $I_O = -4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} = 0.1	V _{CC} -0.1	V			
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v			
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ			
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND l _{OUT} =0μA		8.0	80.0	160.0	μА			
Additional Worst Case Supply Current	Δlcc	per input in V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA			

AC ELECTRICAL CHARACTERISTICS (Input tr. tr 2 ns), AHCT75

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	tpLH	C _L =50pF	10		16		20	ns
E to Q or Q	t _{PHL}	or cob.	10		16		20	1.0
Propagation Delay	tpLH	C _L =50pF	10.5		15		18	ns
D to Q or Q	t _{PHL}	OL COP!	9		15		18	113
Data Set up Time D to Enable	tsu		6	10		12		ns
Data Hold Time Enable to D	th		10		0	10		ns
Input Capacitance	CiN		5					рF
Power disipation Capacitance*	C _{PD}							pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input t_r , $t_l \leqslant 2$ ns), AHCT77

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10^{\circ}$		KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	.
Propagation Delay	t _{PLH}	C _L =50pF	8		14		17	ns
E to Q	t _{PHL}	OL COPI	8		14		17	
Propagation Delay	tpLH	C _i =50pF	8		13		15	ns
D to $\overline{\mathbf{Q}}$	t _{PHL}	OL-30pi	8		13		15	, ,,,
Data Set up Time D to Enable	tsu		6	10		12		ns
Data Hold Time Enable to D	th		0	0	. 5	0	6	ns
Input Capacitance	CIN		5					ρF
Power disipation Capacitance*	C _{PD}							pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

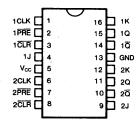
DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

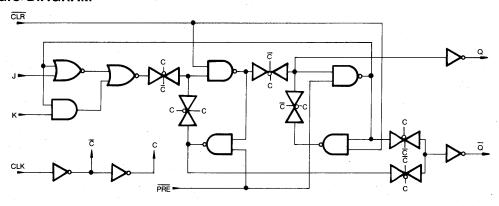


FUNCTION TABLE

	lı	Outputs				
PRE	CLR	CLK	J	K	Q	ā
L	Н	Х	Х	Х	Н	L
н	L	Χ	Х	Х	L	Н
L	L	Х	Х	Х	Н*	H*
н	H.	↓	L	L	Q _o	\overline{Q}_{o}
Н	Н	↓	н	L	н	L
H	Н	↓	L	н	L	н
Н	Н	+	н	н	TOG	GLE
Н	Н	Н	X	X	Q _o	Q,

*Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

LOGIC DIAGRAM



Supply Voltage Range V _{CC} , −0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I _{OK}
$(V_{O} < -0.5V \text{ or } V_{O} > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output V	$^\prime$ oltages * , $^\prime$ Ol $^\prime$ OV to $^\prime$ CO
Operating Temperatu	ire
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall Tim	ies, t _r , t _f Max 500 ns
	always be tied to an appropriate logic
voltage level (either	F VCC OF GINDI

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit	
			Тур	yp Guaranteed Limits				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	Ý	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		4.0	40.0	80.0	μΑ	
Additional Worst Case Supply Current		per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT76

Characteristic		Symbol Conditions		$\begin{array}{c c} T_a = 25 ^{\circ}\text{C} \\ \text{Conditions}^{\dagger} & V_{CC} = 5.0V \end{array} T$		KS74AHCT T _a = -40°C to +85°C V _{CC} =5.0V±10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	
				Тур	Min	Max	Min	Max	
Maximum Clock I	requency	f _{max}		45	30		25		MHz
Propagation Dela	у,	t _{PLH}		10		17		20	ns
CLK to Q or Q		t _{PHL}	C _L =50pF	10		17		20	ns
Propagation Delay,		t _{PLH}		10		17		20	
PRE or CLR to C		t _{PHL}		10		17		20	"
Setup Time	J or K			10	17		20		ns
before CLK↓	PRE or CLR Inactive	t _{su}		10	17		20		113
Hold Time, Data	after CLK↓	th		-3	0		0		ns
CLK High or Low				8	13		15		
Pulse Width	PRE or CLR Low	t _w		8	13		15		ns
Input Capacitance		CIN		5		-			pF
Power Dissipation	Capacitance*	C _{PD}	(per flip-flop)	40					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

IoL = 8 mA @ VoL = 0.5V

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 CTANICT 4090 Apr 18590

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

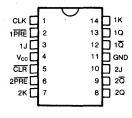
DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K and preset inputs and complementary outputs. The clear and clock inputs are common to both flip-flops. The J-K inputs are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

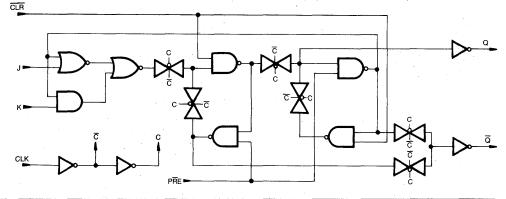


FUNCTION TABLE

	lı	nputs			Out	outs
PRE	CLR	CLK	j	K	Q	Q
L	Н	Х	Х	Х	Н	L
H	L	Х	X	Х	L	Н
L	L	Х	Χ	X	Н*	н*
Н	Н	↓	L	L	Q _o	Ō₀
Н	H	į.	Н	L	н	L
Н	Н	↓	L	Н	L	н
Н	Н	↓	Н	Н	TOG	GLE
Н	Н	Н	X	Х	Q ₀	.Q₀

*Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

LOGIC DIAGRAM



Supply Voltage Range V _{CC} , −0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I _{OK}
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vo	oc 4.5V to 5.5V
DC Input & Output	Voltages*, VIN, VOUT OV to VCC
Operating Tempera	ature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall T	imes, t _r , t _f Max 500 ns
Unused inputs mu voltage level (eit	ust always be tied to an appropriate logic her Vcc or GND)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit				
			Тур		Guaranteed Lim	its	1				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧				
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v				
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v				
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v				
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА				
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		4.0	40.0	80.0	μΑ				
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA				

Dual J-K Flip-Flops with Preset, Common Clear & Common Clock

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT78

Characteristic		Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	T _a = -40°0	AHCT C to +85°C OV ± 10%	KS54 T _a = -55°C V _{CC} = 5.0	Unit	
				Тур	Min	Max	Min	Max	
Maximum Clock F	requency	f _{max}		45	30		25	1	MHz
Propagation Dela	у,	tpLH		10		17		20	ns
CLK to Q or Q		t _{PHL}	C _L =50pF	10		1,7		20	ns
Propagation Delay,		t _{PLH}		10		17		20	
PRE or CLR to C		t _{PHL}		10		17		20	"
Setup Time	J or K			10	17		20		ns
before CLK↓	PRE or CLR Inactive	- t _{su}		10	17		20		113
Hold Time, J or I	Cafter CLK↓	th		-3	0		. 0		ns
CLK High or Low				8	13		15		
Pulse Width	PRE or CLR Low	t _w		8	13		15		ns
Input Capacitance		CIN		5					pF
Power Dissipation	Capacitance*	C _{PD}	(per flip-flop)	40					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$

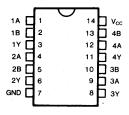
 $^{^{\}dagger}$ For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



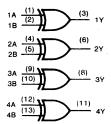
DESCRIPTION

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y = \overline{A} \oplus B$ or $Y = \overline{A} B + A \overline{B}$.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

	•	
Inp	uts	Output
A	В	Υ
L	L	L
L	Н	н
H	L	Н
Н	Н	L

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I _{OK}
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pdf 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	Vcc	4.5	5V to 5.5V
DC Input & Outp	out Voltages*, V _{IN} ,	Vout	OV to V _{CC}
Operating Temp	erature		
Donas	POTABLICT:	40°C	to 185°C

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t_r, t_t Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	v	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	. lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ	
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input tr., tres 2 ns), AHCT86

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54 T _a = -55°C V _{CC} = 5.0	Unit	
			Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	-	10		16		19	ns
A or B to Y (Other Input Low)	t _{PHL}	C _L =50pF	10		16		19	113
Propagation Delay,	t _{PLH}	CL-3061	10		16		20	ns
A or B to Y (Other Input High)	t _{PHL}	1	10		16		20	1113
Input Capacitance	CIN		5					рF
Power Dissipation Capacitance*	C _{PD}	(per flip-flop)	15					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in.}
† For AC switching test circuits and timing waveforms see section 2.

- . Various counting mode.
- Function, Pin-out, speed and drive compatibility with 54/74 ALS logic family.
- . Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

IoL = 8mA @ VoL = 0.5V

- Input and output interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to + 85°C KS54AHCT: -55°C to + 125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 360-mil DIPs

DESCRIPTION

These devices contain four master-slave flip-flops and addition gating to provide a divide by a counter and a three-stage binary counter for which the count cycle length is divide by five for the AHCT90, divide by six for the AHCT92, and divide by eight for the AHCT93, All of these counters have a gated zero reset and the AHCT90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four bit binary), the CKB input is connected to the $Q_{\rm A}$ output. The input count pulses are applied to CKA and the outputs are as described in the appropriate truth table. A symmetrical divide-by-the count can be obtained from the AHCT90 counters by connecting the $Q_{\rm D}$ output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output $Q_{\rm A}$.

PIN CONFIGURATION

,	90	'9:	2		'93
СКВ [] 1	14 CKA	скв 🖂 1	14 CKA	скв 1	14 CKA
MR1 2	13 NC	NC 2	13 NC	MR1 2	13 NC
MR2 🗌 3	12 Q	. NC 🔲 3	12 Q _A	MR2 🔲 3	. 12 🔲 Q _A
NC 4	11 🔲 Q ₀	NC 🗀 4	11 🔲 Q _B	NC 🗌 4	11 🗍 Q _D
V _{CC} _ 5	10 GND	Vcc 🔲 5	10 GND	V _{cc} 5	10 🗀 GND
MS1 ☐ 6	9 🗖 Q _B	MR1 ☐ 6	9 🔲 🔾	NC 🗖 6	9 🔲 Q _B
MS2 🔲 7	8 🗖 🔾 c	MR2 🔲 7	8 □ 0₀	NC 🔲 7.	8 Q _C
<u> </u>		L		Ļ	

FUNCTION TABLE

'90 BCD COUNT SEQUENCE (See Note A)

Output Count Q_{D} $\mathbf{Q}_{\mathbf{A}}$ Qc QB 0 L L L L 1 Н L L L 2 L L L 3 L L н н 4 L Н L L 5 Н Н 6 Н L 7 Н Н Н L 8 Н L L L 9 Н Н

'90 BI-QUINARY (5-2) (See Note B)

Count		Output							
Count	QA	Q_D	Qc	QB					
0	L	L	L	L					
1	L	L	L	Н					
2	L	L	Н	L					
3	L	L	Н	Н					
4	L	Н	Ļ	L					
5	н	L	L	L					
6	Ĥ	L	L	Н					
7	Н	L	Н	· L					
8 .	Н	L	Ή	Н					
9	Н	Н	L	L					

'92 COUNT SEQUENCE (See Note C)

Count		Output						
Journ	QD	Qc	QB	QA				
0	L	L	L	L				
1	L	L	L	Н				
2	L	L	Н	L				
3	L	L	Н	Н				
4	L	Н	LL	L				
5	L	Н	L	Н				
6	Н	L	L	L				
7	Н	L	L	Н				
8	Н	L	Н	L				
9	Н	L	Н	Н				
10	н	н	L	L				
11 .	Н	Н	L	Н				

'93 COUNT SEQUENCE (See Note C)

Count		Out	put	
Count	QD	Qc	QB	QA
0	L	L	L	L
1	L	L	L	н
2	L	L	Н	L
3	L	L	Н	н
-4	- L	Н	L	L
5	L	H	L	н
6	L	Н	Н	L
7	L	Н	H	н
8	Н	. L	L	L
9	Н	L	L	н
10	н	L	Н	L
11	н	L	Н	н
12	Н	Н	L	L
13	н	Н	L	н
14	н	н	н	L j
15	Н	Н	Н	Н

'90
RESET/COUNT TRUTH TABLE

	Reset		Out	put					
MR1	MR2	MS1	MS2	QD	Qc	QB	QA		
Н	Н	L	X	L	L.	L	L		
Н	H	X	L	L	Ľ	L	L		
X	X	H	Н	Н	L	L	Н		
X	L	Х	L	COUNT					
L	X	L	Х	COUNT					
L	X	X	L	COUNT					
Χ	L	L	X		COL	JNT			

Note A: Output Q_A is connected to input CKB for BCD count.

Note B: Output Q_D is connected to input CKA for bi-quinary count.

Note C: Output Q_A is connected to input CKB.

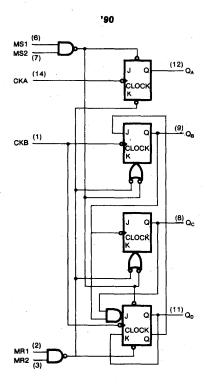
Note D: H=High Level, L=Low Level, X=Don't Care.

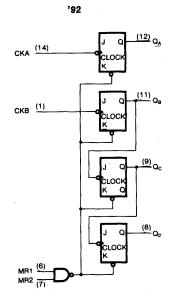
'92, '93 RESET/COUNT TRUTH TABLE

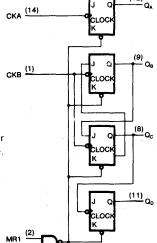
Reset	Inputs		Out	tput		
MR1	MR2	QD	Qc	QB	QA	
Н	Н	L	L	L	L	
L	Х	COUNT				
Χ	L		CO	UNT		



LOGIC DIAGRAMS







'93

Note: The J.K inputs shown without connection are for reference only and are functionally at a high state.

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
Vcc or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, $P_d{}^{\dagger}$ 500 mW

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
 These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_t Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	т	a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1. 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l _{IN} -	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT90

Characteristic		Characteristic		Symbol	Conditions [†]	T _A = 25°C V _{CC} = 5.0V	TA = -40°	AHCT C to +85°C 0V±10%	TA = -55°C	AHCT C to +125°C DV ± 10%	Unit
			* .	Тур	Min	Max	Min	Max	1		
Maximum clock	CKA to QA			50	40		35				
Frequency	CKB to Q _B	f _{max}		25	20		18		MHz		
Maximum Propagat	ion	tpLH		8		14		17	ns		
Delay, CKA to QA		tpHL		8		14		17	113		
Maximum Propagat	ion	tpLH		21		42		50	ns		
Delay CKA to QD		t _{PHL}	•	21		42		50	115		
Maximum Propagat	ion	tpLH		8		14		17	ns		
Delay CKB to QB		tpHL	C _L =50pF	9		15		18	115		
Maximum Propagation Delay CKB to Qc		tpLH	tPLH tPHL tpLH	14		28		33	ns		
		tPHL		14		28		33			
Maximum Propagation		tpLH		14		28		33			
Delay CKB to QD		t _{PHL}		14		28		33	113		
	Maximum Propagation Delay MS to Q _A , Q _D			13		25		30	ns		
Maximum Propagat Delay MS to Q _B , Q		tpHL		18		35		42	ns		
Maximum Propagat Delay MR to any C		t _{PHL}		18		35		42	ns		
	CKA			10	15		20				
Pulse Width	СКВ	t _w		20	30		40		ns		
Taloc Width	MS	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		10	15		20		113		
	MR			10	15		20				
Recovery Time MR to CKA, CKB		trec		17	24		29		ns		
Maximum Input Capacitance		CiN		5					pF		
Power Dissipation Capacitance		C _{PD}							pF		

 $^{^*}C_{PD}$ determines the no-load dynamic dissipation: $P_D = C_{PD} \ V_{CC}^2 f + I_{CC} \ V_{CC}$

[†] For AC Switching test circuits and timing waveforms see sections

AC ELECTRICAL CHARACTERISTICS (Input t_r , $t_l \leqslant 2$ ns), AHCT92

Characteristic		Symbol	Symbol Conditions†		KS74AHCT T _A = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _A = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit	
				Тур	Min	Max	Min	Max		
Maximum clock	CKA to QA	f _{max}		50	40		35		MHz	
Frequency	CKB to Q _B	· · · · · · · · · · · · · · · · · · ·		25	20		18		IVITIZ	
Maximum Propagatio	n	t _{PLH}		8		13		15	ns	
Delay, CKA to Q _A		t _{PHL}		8		14		17	110	
Maximum Propagatio	n	tpLH		21		42		48	ns	
Delay CKA to Q _D		t _{PHL}		21		42		48	113	
Maximum Propagation		t _{PLH}	C _L =50pF	8		14		16	ns	
Delay CKB to QB		t _{PHL}	CL=30pF	10		15		17		
Maximum Propagation		t _{PLH}		10		14		16		
Delay CKB to Q _C		t _{PHL}		11		16		21	ns	
Maximum Propagatio	n	t _{PLH}		14		28		33		
Delay CKB to Q _D		tpHL		14		20		24	110	
Maximum Propagatio Delay MR to any Q	n	t _{PHL}		18		35		42	ns	
	CKA			10	15		20			
Pulse Width	СКВ	tw		20	30		40		ns	
	MR			10 1			20			
Recovery Time MR to CKA, CKB		t _{rec}		17	24		29		ns	
Maximum Input Capacitance		CIN		5					рF	
Power Dissipation Capacitance		C _{PD}							pF	

^{*}CPD determines the no-load dynamic dissipation: PD=CPD VCC2f+ICC VCC

[†] For AC Switching test circuits and timing waveforms see sections

4-Bit Binary Counter Divide by Two and Eight

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT93

Characteristic		Symbol	Conditions†	T _A = 25°C V _{CC} = 5.0V	TA = -40°	NAHCT C to +85°C 0V±10%	TA=-55°C	AHCT to +125°C V± 10%	Unit	
				Тур	Min	Max	Min	Max		
Maximum clock	CKA to QA	f _{max}		50	40		35		MHz	
Frequency	CKB to Q _B	rmax		25	20		18		WITZ	
Maximum Propagation	n	tpLH		8		13		15	ns	
Delay, CKA to Q _A		tent		8		14		. 17	113	
Maximum Propagatio	n ·	tpLH		30		- 56		70	ns	
Delay CKA to Q _D		tpHL		30		56		70	•	
Maximum Propagatio	n	tpLH		8		14		17	ns	
Delay CKB to QB		t _{PHL}	C _L =50pF	9		15		18	ns	
Maximum Propagation		tPLH	OL-OOD!	16		29		34		
Delay CKB: to Q _C	:	tpHL		17		29		34		
Maximum Propagatio	n	tpLH		24		42		50	ns	
Delay CKB to QD		tenu		24		42		50		
Maximum Propagatio Delay MR to any Q	n	t _{PHL}		17		35		42	an,	
	CKA			10	15		20			
Pulse Width	СКВ	tw		20	30		40		ns	
	MR			10	15		20		[
Recovery Time MR to CKA, CKB		t _{rec}		17	24		29		ns	
Maximum Input Capacitance		CIN		5					pF	
Power Dissipation Ca	apacitance	C _{PD}							рF	

^{*} C_{PD} determines the no-load dynamic dissipation: $P_D = C_{PD} \ V_{CC}{}^2 f + I_{CC} \ V_{CC}$



[†] For AC Switching test circuits and timing waveforms see sections

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

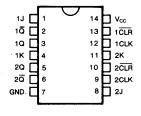
DESCRIPTION

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the $\overline{\text{CLR}}$ input resets the outputs regardless of the levels of the other inputs. When $\overline{\text{CLR}}$ is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

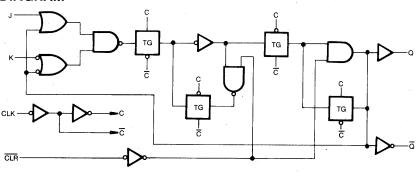
PIN CONFIGURATION



FUNCTION TABLE

	Input	\$		Outp	outs
CLR	CLK	J	K	Q	ā
L	Х	Х	Х	L	Н
Н	↓	L	L	Q _o	\overline{Q}_{o}
Н	†	Н .	. L	Н	L
Н	↓	L	Н	L	H.
H	1	H f	Н	TOG	GLE
H	Н	Х	X	Q _o	Q,

LOGIC DIAGRAM





Dual J-K Negative-Edge-Triggered Flip-Flops with Clear

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	aca operating contamone
Supply Voltage,	V _{CC} 4.5V to 5.5V
DC Input & Outp	out Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Temperating	erature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall	Times, t_r , t_f Max 500 ns
Unused inputs	must always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions		a = 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T _a = -55°C to +125°C	Unit
*			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	.3.0	mA

Dual J-K Negative-Edge-Triggered Flip-Flops with Clear

AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT107

Characteristic		Characteristic Symbol Condit		Conditione Vac = 5 0V -		AHCT C to +85°C 0V±10%	KS54 T _a = -55°C V _{CC} = 5.0	Unit	
				Тур	Min	Max	Min	Max] . [
Maximum Clock	Frequency	f _{max}		45	30		25		MHz
Propagation Dela	у,	tpLH		10		17		20	ns
CLK to Q or Q		t _{PHL}	C _L =50pF	10		17		20	
Propagation Delay,		tpLH		10		17		20	ns
CLR to Q or Q		t _{PHL}		10		17		20] ""3
Setup Time	J or K	t _{su}		10	17		20		ns
before CLK↓	CLR Inactive	¹ ¹su		10	17		20		115
Hold Time, J or I	K after CLK↓	th		-3	0		0		ns
Pulse Width	CLK High or Low	tw		8	13		15		ns
ruise widin	CLR Low	- LW		8	13		15		115
Input Capacitance		CIN		5					рF
Power Dissipation Capacitance*		C _{PD}	(per flip-flop)	40					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{lin}.
† For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

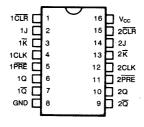
DESCRIPTION

These devices contain two positive-edge-triggered J- \overline{K} flipflops with independent preset and clear inputs and complementary Q and \overline{Q} outputs. The present and clear inputs are active-low and operate independently of the clock Data at the J and \overline{K} inputs are transferred to the ouptuts on the positive transition of the clock provided setup requirements have been met. These versatile flip-flops can perform as toggel flip-flops by grounding K and tying J high. They can also perform as D-type flops if J and \overline{K} are tied together.

These devices provide speeds and drive capability equivalent to their ALST. Lounterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

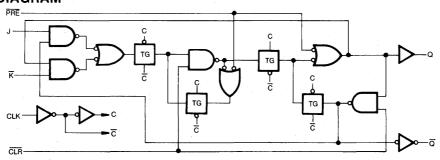


FUNCTION TABLE

	li	nputs			Outp	outs
PRE	CLR	CLK	J	ĸ	Q	ā
L	Н	X	Х	X	Н	L
н	L	Х	Χ	Х	L "	Н
L	L	. X	×	Х	H*	Н*
Н	Н	†	L	L	L	Н
Н	Н	†	Н	L	TOG	GLE
Н	Н	1	L	Н	Q _o	Q₀
Н	Н	↑	Н	н	Н	Ŀ
Н	Н	L	Х	Х	Q _o	Q̄₀

*Both outputs will remain high as long as \overline{PRE} and \overline{CLR} are low, but the output states are unpredictable if \overline{PRE} and \overline{CLR} go high simultaneously.

LOGIC DIAGRAM





Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to V _{CC}
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	Т	a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		4.0	40.0	80.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT109

Characteristic		1 1		T _a = 25°C V _{CC} = 5.0V	T _a = -40°0	AHCT C to +85°C DV ± 10%	KS54AHCT Ta = -55°C to +125°C Vcc=5.0V ± 10%		Unit	
			· .	Тур 55	Min	Max	Min 30	Max		
Maximum Clock	Frequency	f _{max}			34				MHz	
Propagation Dela	ıy,	tpLH		10		17		20	ns	
CLK to Q or Q		t _{PHL}	C _L =50pF	10		17		20		
Propagation Delay.		t _{PLH}		10		14		20	ns	
PRE or CLR to (Q or Q	t _{PHL}		10		14		20	"	
Setup Time	Data			7	12		15		ns	
before CLK1	PRE or CLR Inactive	t _{su}		5	8		10		1115	
Hold Time, Data	after CLK†	th		0	0		0		ns	
Pulse Width	CLK High or Low			9	14		17		T	
ruise widin	PRE or CLR Low	l w	t _w		15		17		ns	
Input Capacitance		C _{1N}		5	,				pF	
Power Dissipation Capacitance*		C _{PD}		40					pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 IoL = 8 mA @ Vol = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

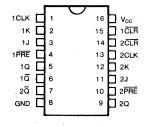
DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

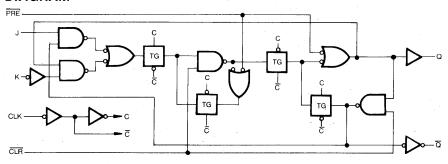


FUNCTION TABLE

	li	Out	outs			
PRE	CLR	CLK	J	K	Q	Q
L	Н	Х	Х	X	Н	L
Н	L	Χ	X	X	L	Н
L	L	Χ	X	X	H*	Н*
Н	н	↓	L	L	Q _o	\overline{Q}_{o}
н	H	↓	Н	L	Н .	L
Н	Н	↓	Ļ	H	L	H
н	Н	‡	Н	н	TOG	GLE
H	Н	Н	Χ	Χ	Q ₀	Q₀

*Both outputs will remain high as long as \overline{PRE} and \overline{CLR} are low, but the output states are unpredictable if \overline{PRE} and \overline{CLR} go high simultaneously.

LOGIC DIAGRAM



Supply Voltage Range V _{CC} ,0.5V to +7	7٧
DC Input Diode Current, I _{IK}	
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ m}$	nΑ
DC Output Diode Current, IOK	
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 m	nΑ
Continuous Output Current Per Pin, Io	
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ m}$	nΑ
Continuous Current Through	
V _{CC} or GND pins ±125 m	nΑ
Storage Temperature Range, T _{stg} 65°C to +150°	,C
Power Dissipation Per Package, Pd† 500 m	W

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	V _{CC} 4.5V to 5.5V
DC Input & Out	out Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Temp	erature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	Ta = 25°C		KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T _a = -55°C to +125°C	Unit
	L		Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	٧
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	٥.	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND 、		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	Δ1cc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT112

Characteristic		Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max]
Maximum Clock	Frequency	f _{max}		50 -	30		25		MHz
Propagation Dela	ay,	t _{PLH}		10		17		20	ns
CLK to Q or Q Propagation Delay,		t _{PHL}	C _L =50pF	10		17		20	
		t _{PLH}		10		17		20	ns
PRE or CLR to	Q or Q	t _{PHL}		10		17		20	1113
Setup Time	J or K			10	17		20		ns
before CLK↓	PRE or CLR Inactive	tsu		10	17		20		113
Hold Time, Data	after CLK↓	th		0	0		0		ns
Pulse Width CLK High or Low				10	17		20		
PRE or CLR Low		tw		6	10		15		ns
Input Capacitance		CIN		5					pF
Power Dissipation	n Capacitance*	C _{PD}	(per flip-flop)	40					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

- Simple pulse width formula tw = 0.45RC
- . DC triggered from active HIGH or active Low inputs
- Retriggerable for very long output pulses up to 100% duty cycle
- · Overriding clear terminates output pulse
- Schmitt trigger A & B inputs allow infinite rise and fall times on these inputs
- Functions, pin-out, speed and drive compativility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs:

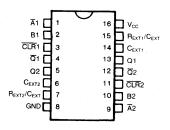
 $I_{OL} = 8mA @ V_{OL} = 0.5V$

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range; 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '123 contains dual retriggerable monostable multivibrators with output pulse width control by three methods.

The basic pulse time is programmed by selection of an external resistor (Rext) and capacitor (Cext). The external resistor and capacitor are normally connected as shown timing component.

Once triggered, the basic output pulse width may be extended by retriggering the gated active Low going edge input (Ai) or the active HIGH going edge input (Bi). By repeating this process, the output pulse period (nQ=HIGH, nQ=LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a Lowgoing edge on input CLR, which also inhibits the triggering. An internal connection from CLR to the input gates makes it possible to trigger the circuit by a positive-going signal at input CLR as shown in the function table when $C_{\text{EXT}} > 10\text{nF}$, the typical output pulse width is defined as; $t_{\text{W}} = 0.45 \times R_{\text{EXT}} \times C_{\text{EXT}}(typ)$.

Where t_w is in seconds. R is in ohm, and C is in fards. All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

	Inputs	Out	puts	
CLR	Ā	В	Q	ā
L	X	X	L	Н
×	Н	Х	L	Н
. X	X	L	L	Н
Н	L	1	Л	U
Н	1	Н	Л	IJ
↑	L	Н	л	T

H≔ HIGH voltage level

L= LOW voltage level

X= don't care

↑= LOW to HIGH transition

↓= HIGH to LOW transition

Π= one HIGH level output pulse

'I'= one LOW level output pulse

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOk
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous OUtput Current Per Pin, Io
(-0.5V <v<sub>O<v<sub>CC+0.5V) ±35 mA</v<sub></v<sub>
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} -65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package(N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	۷
DC Input & Output Voltages*, VIN, VOUT OV to Vo	CC
Operating Temperature	

ange KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20\mu A$ $I_O = -4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	\ \
Maximum Low-Level Output Voltage	Vol	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	l _{IŅ}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	Δlcc	per input in V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT123

Characteristic	Symbol	Conditions†	$\begin{array}{ccc} T_a = 25 ^{\circ} C \\ V_{CC} = 5.0 V \end{array}$		$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	
]	<u> </u>	Тур	Min Max		Min Max		
Propagation Delay	tpLH		-18		33		39	ns
A, B to Q, Q	tPHL	C _L =50pF	18		33		39	
Propagation Delay	tpLH	C _{ext} ≈0,	16		27		32	ns
CLR to Q, Q	t _{PHL}	$R_{ext}=5k\Omega$	16		27		32	'''
Output Pulse Width 1	twQ1		116		207		209	ns
Output Pulse Width 2	two2	C_L =50pF C_{ext} =10nF R_{ext} =10k Ω	45	38	52	38 ,	52	μs
Trigger Pulse Width	tw	C _L =50pF A _i =LOW	5		. 16		20	ns
Trigger Pulse Width	tw	C _L =50pF B _i =High	5		16		20	ns
Clear Pulse Width	t _w	C _L =50pF CLR _i =LOW	6		16		20	ns
External Timing Resistance	R _{ext}			2	100	2	100	kΩ
External Timing Capacitance	C _{ext}				no restri	ction		рF
Input Capacitance	Cin		5					рF
Power Dissipation Capacitance	C _{PD}							рF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

Application Information

The basic output pulse width is determined by the value of external capacitance and timing resistance. For output pulse widths greater than $100\mu s$ or external capacitance greater than 10nF the following equation should be used.

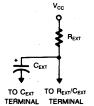
 $t_w = k \cdot R_{ext} \cdot C_{ext}$

Where

 t_W is in μ s K is the multiplying factor and is approximately 0.45 for Cext is in nF Rest is in k Ω

For best results, system ground should be applied to the C_{ext} terminal. These devices do not require a switching diode in series with the $R_{\text{ext}}/C_{\text{ext}}$ terminal (as required by some other monostable multivibrators)

TIMING COMPONENT



[†] For AC switching test circuits and timing waveforms see section 2.

Z

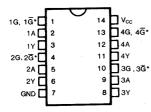
FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · 3-State outputs with drive current
 - ($I_{OL} = 24 \text{ mA}$ @ $V_{OL} = 0.5V$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



*G for '125: G for '126

FUNCTION TABLES

125

inį	puts	Output
A	. G	Y
Н	L	Н
L	L	L
X	Н	Z

'126

Inp	outs	Output
A	G	Υ
Н	Н	Н
· L	Н	L
Х	L	Z

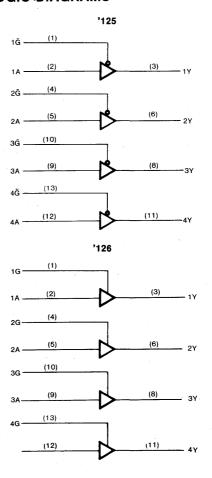
DESCRIPTION

These bus buffers feature four independent line drivers with 3-state outputs. The output enable functions for the '125 buffers are active-low, while those for '126 are active high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAMS



Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

1100011111101140	a operan	
Supply Voltage, Vcc		4.5V to 5.5V
DC Input & Output \	/oltages*, V _{IN} ,	$V_{\mbox{\scriptsize OUT}}$ OV to $V_{\mbox{\scriptsize CC}}$
Operating Temperatu	ıre	
Range	KS74AHCT:	-40°C to +85°C
	KS54AHCT:	-55°C to +125°C
Input Rise & Fall Tim	nes, t _r , t _f	Max 500 ns
Unused inputs must	t always be tied	to an appropriate logic
voltage level (eithe	er Voc or GND)	

Characteristic	Symbol	thol Test Conditions $T_a = 25^{\circ}C$ $T_a = -40^{\circ}C$ to $+85^{\circ}$			KS54AHCT T _a = -55°C to +125°C				
			Тур	yp Guaranteed Limits					
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1 3.7	V		
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA		

4

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT125, AHCT126

Characteristic	Symbol	Conditions [†]		ol Conditions†		T _a = 25°C V _{CC} = 5.0V		AHCT C to +85°C IV±10%	Ta= -55°C	AHCT to +125°C DV ± 10%	Unit
				Тур	Min	Max	Min	Max			
Propagation Delay,	tpLH	C _L =50pf C _L =150p	CL=50pF CL=150pF			10 15		12 . 18			
A to Y	C _L =50pF C _I =150pF		7 10		13 17		15 19	ns			
Output Enable Time	tpzH	$-R_L=1k\Omega$	C _L =50pF C _L =150pF	11 14		18 23		22 28	ns		
Enable to Y	t _{PZL}		C _L =50pF C _L =150pF	11 14		18 23		22 28	113		
Output Disable Time,	tpHZ	$R_L = 1 k\Omega$		13		18		22	ns		
Enable to Y	tPLZ	C _L =50pF	=	13		18		22	113		
Input Capacitance	CIN			5			-		pF		
Output Capacitance	Соит	Output di	Output disabled						pF		
Power Dissipation Capacitance* (per stage)	C _{PD}		G or G=V _{CC} G or G=GND						pF		

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

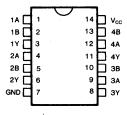
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

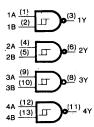
These Schmitt-trigger devices contain four independent NAND gates. They perform the Boolean function $Y=\overline{A}\bullet\overline{B}=\bar{A}+\bar{B}$ in positive logic.

The input threshold levels are temperature compensated and can be triggered from the slowest of input ranges and still give jitter-free output signals.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

_			
	INPUTS		OUTPUTS
	Α	В	Y Y
	L	L	Н
l	L	Н	н
	H	L	Н
	H	Н	L

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_l < -0.5V \text{ or } V_l > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} −65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to V_{CC}
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Symbol Test Conditions		= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit	
		·	Тур		Guaranteed Limits			
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	Vcc 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} =0.11	v	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	. V	
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	

DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	T _a =25°C		KS74AHCT T _a = -40°C to +85°C		KS54AHCT T _{a=} -55°C to +125°C		Unit
Characteristic	Symbol	rest Conditions	Min	Max	Min	Max	Min	Max	
Positive-Going	V _{T+}	V _{CC} =4.5V	1.2	1.9	1.2	1.9	1.2	1.9	v
Threshold Voltage	VT+	V _{CC} =5.5V	1.4	2.1	1.4	2.1	1.4	2.1	•
Negative-Going	V _T _	V _{CC} =4.5V	0.5	1.2	0.5	1.2	0.5	1.2	v
Threshold Voltage	VI-	V _{CC} =5.5V	0.6	1.4	0.6	1.4	0.6	1.4	"
Hysteresis	VH	V _{CC} =4.5V	0.4	1.4	0.4	1.4	0.4	1.4	v
$(V_{T+}-V_{T-})$	VH	V _{CC} =5.5V	0.4	1.5	0.4	1.5	0.4	1.5	"



AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT132

Characteristic	Symbol	Conditions [†]	$ T_a = 25 ^{\circ} C \\ s^{\dagger} V_{CC} = 5.0 V \\ V_{CC} = 5.0 V \\ V_{CC} = 5.0 V \pm 10 \% $ KS54AHCT $ T_a = -40 ^{\circ} C \text{ to } +85 ^{\circ} C \\ V_{CC} = 5.0 V \pm 10 \% $ $ V_{CC} = 5.0 V \pm 10 \% $			$= -40$ °C to $+85$ °C $T_a = -55$ °C to	to +125°C	Unit
·			Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	C ₁ =50pF	8		14		17	ns
Any input to Y	t _{PHL}	OL-OOD!	8		14		17] [
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

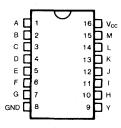
[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

INPUTS A THRU M		OUTPUT Y
All inputs	Н	L
One or more inputs	L	Н

DESCRIPTION

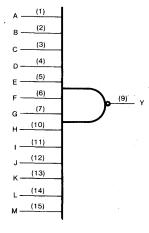
The '133 contains a single 13-input NAND gate. It performs the boolean functions (in positive logic): $Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$

 $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H} + \overline{I} + \overline{J} + \overline{K} + \overline{L} + \overline{M}$

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, IIK
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, lok
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, V_{IN} , V_{OUT} . . 0V to V_{CC} Operating Temperature

Range KS74AHCT: -40°C to +85°C

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit	
		*	Тур	,	Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v	
Maximum Low-Level Output Voltage	. V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT133

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C 0V ± 10%	$KS54$ $T_a = -55^{\circ}C$ $V_{CC} = 5.0$	Unit	
<u> </u>			Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	C ₁ =50pF	11		18		22	ns
Any input to Y	t _{PHL}	OL-30pi	11		18		22	
Input Capacitance	CiN		5					pF
Power Dissipation Capacitance*	C _{PD}		15					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² fin.

[†] For AC switching test circuits and timing waveforms see section 2.



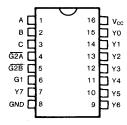
[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 3 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 No. 9 mA No. 0 5V
 - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KETANICT: 409C to 1959C

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

Enable Inputs		Select Inputs		Outputs								
G1	G2*	С	В	Α	Y0	Y1	Y2	Υ3	Y4	Y5	Υ6	Y 7
Х	Н	Х	Х	X	Н	Н	Н	Н	Η.	Н	Н	Н
L	Х	Х	Х	Χ	Н	Н	H	Н	Н	Н	Н	Н
Н	L	L	L	L	L	Н	Ĥ	Н	Н	Н	H	Н
н	L	L	L	Н	н	L	Н	Н	Н	Н	Н	Н
Н	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н
Н	L	L	н	н	Н	Н	Н	L	Н	Н	Н	Н
н	L	Н	Ľ	L	Н	H	Н	н	L	H	Н	H
н	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н
Н	L	Н	Н	Н	Н	Н	Н	Н	Ή	Н	Н	L

*G2=G2A+G2B

DESCRIPTION

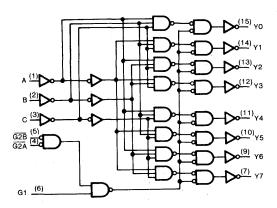
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is neoligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



3-Line to 8-Line Decoders/Demultiplexers

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	
Operating Temperature	* * * * * * * * * * * * * * * * * * * *

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH	•		2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	Усс 4.2	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	1	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	О	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_i≤2 ns), AHCT138

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	Ta = - 40°0	AHCT C to +85°C 0V ± 10%	KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
	ļ		Тур	Min	Max	Min	Max	
Propagation Delay, A, B, C or any Y	tPLH		12		20		24	ns
	t _{PHL}		12		20		24	"
Propagation Delay,	tpLH		12		18		20	ns
G1 to any Y	tpHL	C _L =50pF	12		18		20	115
Propagation Delay,	tpLH		12		18	-	20	ns
G2A or G2B to any Y	tehl		12		18		20	1115
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C _{PD}		50					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² fin-

[†] For AC switching test circuits and timing waveforms see section 2.

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

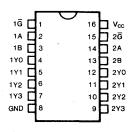
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory, this means that the effective system delay introduced by the decoder is negligible.

The '139 consists of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

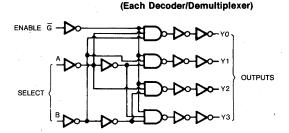
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

In	puts			Out	puts	
Enable G	B A		YO	Y1	Y2	Υ3
н	Х	X	н	Н	Н	Н
L.	L	L	L	Н	Н	Н
L	L	Н	Н	L	Н	Н
L	Н	L	н	Н	L	Н
L	Н	Н	H	Н	H	L

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
 These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		its		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL		-	0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC} 4.2	V _{CC} -0.1	V _{CC} -0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_i≤2 ns), AHCT139

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	$T_a = -40^\circ$	AHCT C to +85°C 0V±10%	KS54 T _a = -55°C V _{CC} = 5.0	Unit	
*			Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}		11		17		20	ns
A or B to Y	tpHL	C ₁ =50pF	11		17		20	1113
Propagation Delay,	t _{PL:H}	CL-SUPP	11		18		21	ns
G to any Y	t _{PHL}		11		18	1 -	21	1115
Input Capacitance	CiN		5					рF
Power Dissipation Capacitance*	C _{PD}		50					рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2$ f_{in} . For AC switching test circuits and timing waveforms see section 2.

- . Encodes eight data lines in priority
- · Provides 3-bit binary priority code
- . Input enable capability
- Easily cascadable
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

 $I_{OL} = 8$ mA @ $V_{OL} = 0.5V$

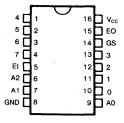
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

Package options include "small outline" packages.
 (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '148 provides three bits of binary coded output representing the position of the highest order active input, along with an output indicating the presence of any active input. It is easily expanded via input and output enables to provide priority encoding over many bits.

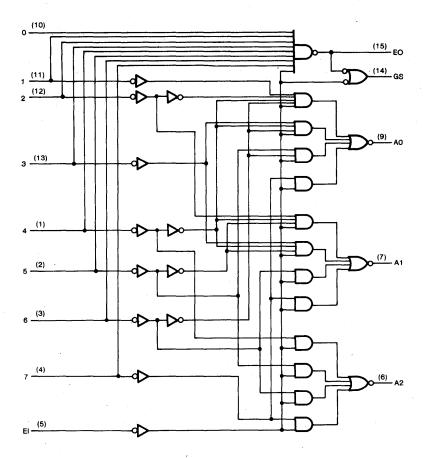
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

			Inj	out	s					(Outpu	ıts	
EI	0	1	2	3	4	5	6	7	A2	A 1	A0	GS	EO
Н	Х	Х	Х	Х	Х	Х	Х	Х	Н	Н	Н	Н	Н
L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	н	Н	L
L	X	Х	Х	Х	Χ	Х	Х	L	L	L	L	L	Н
L	Х	Х	Х	Χ	Х	Х	L	Н	L	L	Н	L	Н
L	Х	Х	Х	Χ	Χ	L	Н	Н	L	Н	L	L	Н
L	X	X	Χ	Χ	L	Н	Н	Н	L	Н	Н	L	H
L	Х	Х	Х	L	Н	Н	Н	Н	Н	L	L	L	Н
L	Х	X	L	Н	Н	Н	Н	Н	Н	L	Н	L	Н
L	Х	L	Н	Ή	Н	Н	Н	Н	Н	Н	L	L	Н
L	L	Н	Н	Н	Н	Н	Н	н	н	Н	н	L	Н

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, IIK
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC} Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit		
			Тур	p Guaranteed Limits					
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0 ·	2.0	V		
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	V.		
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V_I =2.4V other inputs: at V_{CC} or GND I_{OUT} =0 μ A		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT148

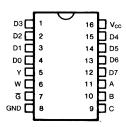
Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	Ta = - 40°0	AHCT C to +85°C DV ±10%	KS54 T _a = -55°C V _{CC} = 5.0	Unit	
			Тур	Min	Max	Min	Max	
Propagation Delay,	tpLH		10		17		20	ns
1-7 to AO, A1 or A2	t _{PHL}		10		- 17		20	
Propagation Delay,	t _{PLH}		11		18		22	ns
0-7 to EO	t _{PHL}		11		18		22	
Propagation Delay,	tplH	C _L =50pF	14		24		29	ns
0-7 to GS	t _{PHL}		14		24		29	
Propagation Delay,	tpLH	OL-30pi	10		16		19	ns
El to AO, A1 or A2	t _{PHL}		10		16		19	""
Propagation Delay,	t _{PLH}		10		17		20	ns
El to GS	t _{PHL}		10		17.		20	'''
Propagation Delay,	t _{PLH}		11		18		22	ns
EI to EO	t _{PHL}		11		18		22	115
Input Capacitance	C _{IN}		5					pF
Power Dissipation Capacitance*	C _{PD}		50					рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

- Can perform as:
 Boolean Function Generators
 Parallel-to-Serial Converters
 - Data Source Selectors
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High drive currents outputs
- ($I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
- KS74AHCT: -40°C to +85°C
- KS54AHCT: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, I _{OK}
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

DESCRIPTION

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input (\overline{G}) must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

		OUT	PUTS		
s	ELEC	т		144	
С	В	Α	Ğ	Y	W
Х	Х	Х	Н	L	Н
L	L	L	L	DO	DO
Ł	L	Н	L ·	D1	D1
L	Н	L	L	D2	D2
L	Н	Н	· L	D3	D3
н	L	L	Ĺ	D4	D4
н	L	Н	L	D5	D5
Н	Н	L	L	D6	D6
н	Н	H	L	D7	D7

H = high level, L = low level, X = irrelevant D0. D1 ... D7 = the level of the D respective input

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

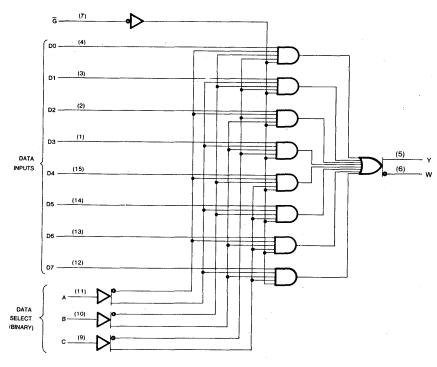
Recommended Operating Conditions

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	bol Test Conditions		a = 25°C	KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54AHCT T _a = -55°C to +125°C	Unit		
•			Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V		
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6 \text{ mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v		
Maximum Low-Level Output Voltage	V _{OL}	$V_{\text{IN}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $I_{\text{O}} = 20\mu\text{A}$ $I_{\text{O}} = 12\text{mA}$ $I_{\text{O}} = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA		



AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT151

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	Ta = -40°	IAHCT C to +85°C 0V±10%	K\$54 T _a = -55°C V _{CC} = 5.0	Unit	
	}		Тур	Min	Max	Min	Max	
Propagation Delay.	tpuH	C _L =50pF C _L =150pF	13 16		21 26		25 31	
A, B or C to Y	t _{PHL}	C _L =50pF C _L =150pF	13 16		21 26		25 31	ns
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	15 . 18		24 29		27 33	
A, B or C to W	t _{PHL}	C _L =50pF C _L =150pF	15 18		24 29		27 33	ns
Propagation Delay,	tpLH	C _L =50pF C _L =150pF	9 12		15 20		18 24	ns
Any D to Y	tpHL	C _L =50pF C _L =150pF	9 12		15 20		18 24	
Propagation Delay	t _{PLH}	C _L ≈50pF C _L ≈150pF	8 11		15 20		18 24	ns
Any D to W	tpHL	C _L =50pF C _L =150pF	8 11	-	15 20		18 24	
Propagation Delay,	tpLH	C _L =50pF C _L =150pF	12 15		19 24		23 29	ns
G to Y	tent	C _L =50pF C _L =150pF	12 15		19 24		23 29	
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	13 16		21 26		25 31	ns
G to W	t _{PHL}	C _L =50pF C _L =150pF	13 16		21 26		25 31	113
Input Capacitance	CiN		5					pF
Power Dissipation Capacitance*	CPD							pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}

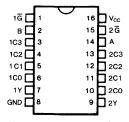
[†] For AC switching test circuits and timing waveforms see section 2.

- . Allows Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- '253 is the 3-State Version of this part
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · High drive currents Outputs
- ($I_{OL} = 24$ mA @ $V_{OL} = 0.5V$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges;

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

Each of these data selectors/multiplexers contains inverters and drives to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs (G) are provided for each of the two four-line sections.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

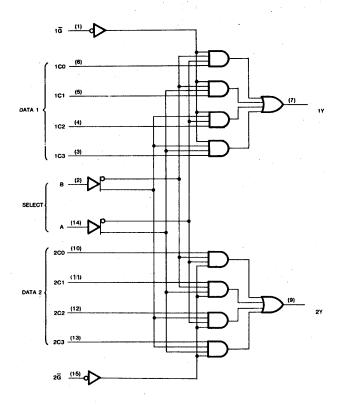
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

	ECT UTS	DA	ATA	INPU	тѕ	STROBE	OUTPUT		
В	A	CO	C1	C2	СЗ	Ğ	Y		
Х	Х	Х	Х	Χ	Х	Н	L		
L	L	L	Χ	Χ	Χ	L	L		
L	L	Н	. X	Х	Χ	L	Н		
L	H	х	L	Х	X	L	L		
L	H	Х	H:	Х	Х	L	Н -		
Н	L	X	Χ	L	Х	L	L		
Н	L	Х	Χ	Н	Х	L	н		
Н	Н	Х	Χ	Х	L	L	L		
Н	Н	Х	X	Х	Н	L	Н		

Select inputs A and B are common to both sections.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, V_{IN}, V_{OUT} . . . OV to V_{CC} Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, $t_{\text{r}},\,t_{\text{f}}$ Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit		
			Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	v		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V		
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =12mA I _O =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input tr, tre2 ns), AHCT153

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	T. = -40°	IAHCT C to +85°C 0V±10%	Ta = -55°C	AHCT to +125°C 0V± 10%	Unit	
			Тур	Min	Max	Min	Max		
Propagation Delay,	tpLH	C _L =50pF C _L =150pF	13 16		21 26		25 31	ns	
A or B to Y	t _{PHL}	C _L =50pF C _L =150pF	13 16		21 26		25 31	1113	
Propagation Delay,	tpLH	C _L =50pF C _L =150pF	9 12		15 20		18 24	ns	
Data (Any C) to Y	t _{PHL}	C _L =50pF C _L =150pF	9 12		15 20		18 24	113	
Propagation Delay,	t _{PLH}	t _{PLH} C _L =50pF C _L =150pF			18 23		22 28	ns	
G to Y	t _{PHL}	C _L =50pF C _L =150pF	11 14		18 23		22 28	115	
Input Capacitance	Cin		5					pF	
Power Dissipation Capacitance*	C _{PD}				-			pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data From One Input to Any One of 16 Outputs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 CTANICT* 409C to 1.959C

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION

οπ	1	24 D. Vcc
10	2	23 A
20	3	22 5 B
3.□	4	21 C
40	5	20 D
5□	6	19 🗖 🛱 2
6口	7	18 🗖 Ğ1
70	8	17 15
80	9	16 14
9.□	10	15 13
10□	11	14 12
GND	12	13 11

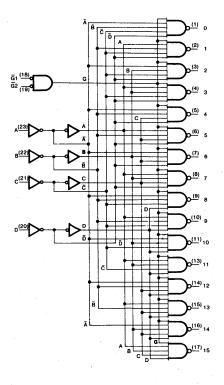
DESCRIPTION

These monolithic, 4-line to 16-line decoders decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs. G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are idenally suited for implementing high-performance memory decoders.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



FUNCTION TABLE

		Inputs	3			Outputs															
Ğ1	Ğ2	D	С	В	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L.	L	L	L	Н	н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Н	L	L	Н	H.	· H	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Н	Ļ	Н	н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	н	н
L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	H	Н	Н	Н	Н	Н	.H
L	L	L	Н	Н	Н	Н	Н	Н	H	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н
·L	L	н	L	L	L	Н	Н	Н	H	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н
L	L	Н	L	L	Н	Н	Н	Н	Н	Н	Н	H	Н	Н	L	Н	Н	Н	Н	Н	Н
L	Ŀ	Н	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
L	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
L	L	Н	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	H-
L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	H	Н	Н	Н	Н	Н	Н	Н	L	Н	Н
L	L	Н	H	Н	L	Н	Н	·H	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	H-	Н	L
L	н	Х	Χ	Χ	Χ	Н	н	Н	Н	Н	Н	Н	Н	Н	Н	Н	H	Н	Н	Н	Н
Н	L	Х	Х	Χ	X	н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
Н	Н	X	Х	Х	Χ	н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н

Absolute Maximum Ratings*

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC} Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	ibol Test Conditions		a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT Ta = -55°C to +125°C	Unit		
		S	Тур		Guaranteed Lim	Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-8mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	V		
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0µA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V_I =2.4V other inputs: at V_{CC} or GND I_{OUT} =0 μ A		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT154

Characteristic	Symbol Conditions [†]		T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54 T _a = -55°C V _{CC} = 5.0	Unit	
			Тур	Min	Max	Min	Max	
Propagation Delay,	tPLH	C _L =50pF	12		20		24	ns
A, B, C, D to Any Output	t _{PHL}		12		20		24	
Propagation Delay,	t _{PLH}	0[-30pi	12		20		24	ns
G1 or G2 to Any Output	tenc		12		20		24	115
Input Capacitance	CIN		-5				-	рF
Power Dissipation Capacitance*	C _{PD}		50					рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

- Typical applications:
 Dual 2-to-4 line decoder
 Dual 1-to-4 line demultiplexer
 3-to-8 line decoder
 1-to-8 line demultiplexer
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

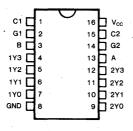
DESCRIPTION

The '155 consists of two 1-to-4 line demultiplexers with independent strobes and common binary address inputs. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied to C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8 line decoder, or 1-to-8 line demultiplexer, without gating.

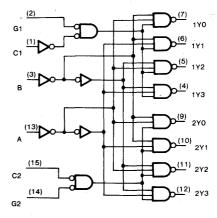
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLES

2-to-4 Line Decoder or 1-to-4 Line Demultiplexer

		Inputs		Outnute					
Sel	ect	Strobe	Data	Outputs					
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3		
Х	Х	Н	·x	Н	Н	Н	Н		
L	L	L	н	L	Н	Н	н		
L	Н	L	н	Н	Ĺ	н	. н		
Н	L	L	Н	Н	н	L	н		
Н	Н	L	Н	Н	н	н	L		
Х	Х	Х	L	Н	H	н	Н		

		Inputs			04		
Se	ect	Strobe	Data	Outputs			
В	A	G2	C2	2Y0	2Y1	2Y2	2Y3
Х	Х	Н	Х	Н	Н	Н	Н
L	L	L	L	l L	Н	н	Н
L	н	L	L	Н	L	н	н
н	L	L	L	Н	н	L	н
н	Н	L	L	Н	Н	Н	L
Х	Х	х	Н	Н	Н	н	Н

3-to-8 Line Decoder or 1-to-8 Line Demultiplexer

Select	Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
CT B A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
XXX	Н	Н	Н	Н	Н	Н	Н	· H	Н
LLL	L.	L	Н	Н	Н	Н	Н	Н	Н
LLH	L	Н	L	Н	Н	Н	Н	Н	Η.
LAL	L	н	Н	L	Н	Н	Н	Н	Н
LHH	L	Н	Н	Н	L	Н	Н	Н	Н
HLL	L	Н	Н	Н	Н	L	Н	Н	Н
H L'H	L	Н	Н	Н	Н	Н	L	Н	Н
HHL	L	Н	Н	Н	Н	Н	Н	L	Н
ннн	_ L _	Н	Н	Н	Н	Η.	Н	Н	L

†=Inputs C1 and C2 Connected together

t=Inputs G1 and G2 Connected together

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} , −0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 0.5V$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Retings are those values beyond

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74AHCT: $-40\,^{\circ}\text{C}$ to $+85\,^{\circ}\text{C}$ KS54AHCT: $-55\,^{\circ}\text{C}$ to $+125\,^{\circ}\text{C}$ Input Rise & Fall Times, t_r , t_t Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	s T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT155

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	Ta = -40°0	AHCT C to +85°C OV ±10%	KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Тур	Min	Max	Min	Max	
Maximum Propagation Delay,	t _{PLH}		12		20		24	ns
A, B, C2, G1 or G2 to any Output (2 levels of logic)	t _{PHL}		12		20		24	113
Maximum Propagation Delay,	t _{PLH}	C _L =50pF	14		23		28	ns
A or B to any Y (3 levels of logic)	t _{PHL}	CL=5UPF	14		23		28	113
Maximum Propagation Delay,	t _{PLH}		13		22		26	ns
C1 to any Y	tPHL		13		22		26	
Maximum Input Capacitance	CiN		5					рF
Power Dissipation Capacitance*	C _{PD}							рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These are data selectors multiplexers which select a 4-bit word from one of two sources via the control of a common select input (\overline{A}/B). A separate strobe input (\overline{G}) is provided. The '157 presents true data whereas the '158 presents inverted data at the outputs.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

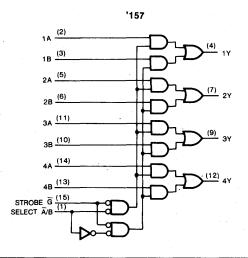
PIN CONFIGURATION

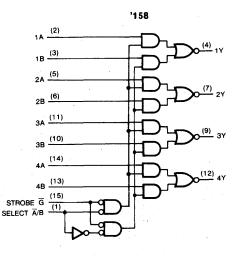
Ā/B	d -	\cup	16	_ v
1 A			15	□ē
1B	□3		14	□ 4A
1Y	□⁴		13	□ 4B
2A	□5		12	□ 4Y
28	□6		11	3A
2Y	1 7		10	3В
GND	□8		9] 3Y
	L			

FUNCTION TABLE

	Inputs	Output Y			
Strobe	Select	Da	ata	14.57	1450
Ğ	Ã/B	Α	В	'157	'158 H
Н	Х	Х	Х	٦	Н
L	L	L	Х	L.	Н
L	L	н	Х	H	L
.L	Н	X	L	L	Н
L	н	X	н	н	L

LOGIC DIAGRAMS







Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} −65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	l cc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT157, AHCT158

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	Ta = -40°	74AHCT		to +125°C	Unit
			Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}		11		15		18	ns
A or B to Y	t _{PHL}		11		15.5		18	""
Propagation Delay,	tpLH	C _L =50pF	13		22		26	ns
Ā/B to Y	t _{PHL}	CL=5UPF	13		22		26	113
Propagation Delay,	t _{PLH}		12		19		23	ns
G to Y	t _{PHL}		12		19		23	1115
Input Capacitance	CIN		5			1	1	pF
Power Dissipation Capacitance*	C _{PD}							pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in.}
† For AC switching test circuits and timing waveforms see section 2.

KS54AHCT 160/161 KS74AHCT 162/163

Synchronous 4-Bit Decade and Binary Counters

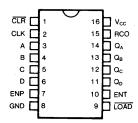
FEATURES

- Internal Look Ahead for Fast Counting
- · Carry Output for n-bit cascading
- Synchronous Counting
- Synchronously Programmable
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLES

160, 161

ſ	CLK	CLR	ENP	ENT	LOAD	Function
Γ	Х	L	Х	Х	×	Clear
	Х	н	Н	L	Н	Count & RC disabled
	Х	Н	L	Н	Н	Count disabled
1	X	Н	L	L	Н	Count & RC disabled
	† .	Н	Х	Х	L	Load
	1	Н	Н	Н	Н	Increment Counter

'162, '163

CLK	CLR	ENP	ENT	LOAD	Function
1	L	Х	Х	X	Clear
X	Н	. Н	L	Н	Count & RC disabled
X	H	L	Н	н	Count disabled
X	Н	L	L	н	Count & RC disabled
1	H	Х	Х	L	Load
1	Н	н	Н	H	Increment counter

DESCRIPTION

These are synchronous, presettable 4-bit binary counters featuring internal carry-look-ahead for high-speed counting. The '160 and '162 are decade counters, and the '161 and '163 are 4-bit binary counters. The buffered clock input triggers all flip-flops simultaneously on the rising edge of the input waveform. This eliminates the output counting spikes normally associated with asynchronous counters.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the '160 and '161 is asynchronous and a low level at the clear input sets all four of the flipflop outputs low regardless of the levels of the clock, load or enable inputs.

The clear function for the '162 and 163 is synchronous and a low level at the clear input sets all four of the flipflop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter.

Two enable inputs and a ripple carry output allow easy cascading of the counters. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

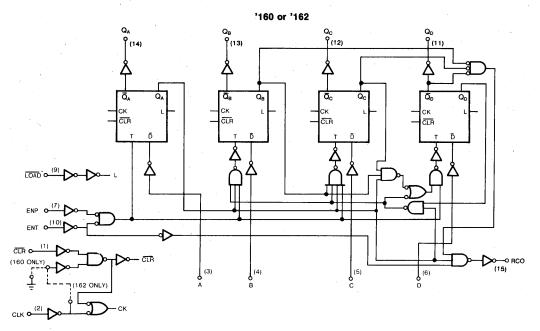
These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating model have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

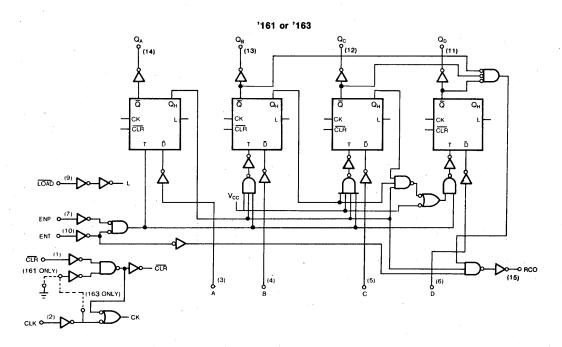
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to $V_{\rm cc}$ and ground.



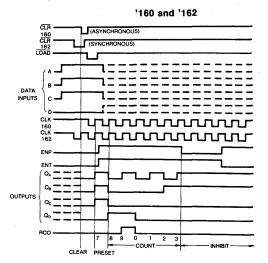
LOGIC DIAGRAMS





Synchronous 4-Bit Decade and Binary Counters

Typical Clear, Preset, Count and Inhibit Sequences



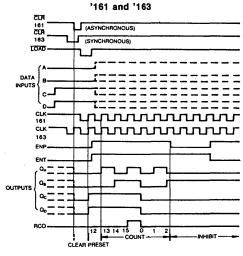
Sequence:

- (1) Clear outputs to zero
- (2) Preset to BCD seven
- (3) Count to eight, nine, zero, one, two, and three
- (4) Inhibit

Absolute Maximum Ratings*

Supply Voltage Range $V_{CC}, \ldots -0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ $\pm 20 \text{ mA}$
DC Output Diode Current, I _{OK}
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T_{stg} 65°C to +150°C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.



Sequence:

- (1) Clear outputs to zero
- (2) Preset to binary twelve
- (3) Count to thirteen, fourteen, fifteen, zero, one and two
- (4) Inhibit
- † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, VIN, VOUT ... OV to VCC Operating Temperature Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, tr, tf Max 500 ns Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	_a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
• .			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	Vін			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL	,		0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	٧
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT160, AHCT161

Cha	racteristic	Symbol	Conditions	T _a = 25°C V _{CC} = 5.0V	T _a = -40°C	AHCT C to +85°C OV ± 10%	$KS54.$ $T_a = -55^{\circ}C$ $V_{CC} = 5.0$	to +125°C	Unit
				Тур	Min	Max	Min	Max	
Maximum Cloc	k Frequency	f _{max}		50	40		35		MHz
Propagation De	elay,	t _{PLH}		15		20		24	ns
CLK to RCO		tpHL		15		20		24	
Propagation Delay,		t _{PLH}		10		16		19	ns
CLK to any Q		t _{PHL}	C _L =50pF	10		16		19	
Propagation De	elay,	t _{PLH}	OL-30pi	9		13		16	ns
ENT to RCO	• /	t _{PHL}		9		13		16	"
Propagation De	elay,	t _{PHL}		15		24		29	ns
Propagation De	elay,	t _{PHL}		17		23		33	ns
Pulse Width	CLK High or Low			8	12		16		ns
Fuise Width	CLR Low	t _w		10	15		20		113
	A, B, C, D			10	15		20		
Sotup Time	LOAD	t _{su}		10	15		20	•	ns
Setup Time before CLK1	ENP, ENT	- Lsu		10	15		20		113
	CLR inactive	1		6	10		- 10		
Hold time, All Synchronou	s Inputs after CLK†	t _h		0	0		0		ns
Input Capacita	nce	CIN		5					pF
Power Dissipat	tion Capacitance*	C _{PD}		80					pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin-

[†] For AC switching test circuits and timing waveforms see section 2.



Synchronous 4-Bit Decade and Binary Counters

AC ELECTRICAL CHARACTERISTICS (Input tr., tr<2 ns), AHCT162, AHCT163

Cha	aracteristic	Symbol	nbol Conditions†	T _a = 25°C V _{CC} = 5.0V	T _a = -40°C	AHCT C to +85°C OV±10%	$T_a = -55^{\circ}C$	NAHCT C to +125°C OV ± 10%	Unit
				Тур	Min	Max	Min	Max	
Maximum Clo	ck Frequency	f _{max}		50	40		35		MHz
Propagation D	elay,	t _{PLH}		15		20		24	ns
CLK to RCO	_	t _{PHL}		15		20	•	24	113
Propagation D	elay,	t _{PLH}	C _L =50pF	10		16		20	ns
CLK to any Q		t _{PHL}		10		16		20	'''
Propagation D	elay,	t _{PLH}		9		15		18	ns
ENT to RCO		t _{PHL}		9		15		18	'''
Pulse Width, CLK High or I	_ow	tw		8	12.5		20		ns
	A, B, C, D			10	15		20		
Setup Time	LOAD	t _{su}		10	15		20		ns
Setup Time before CLK1	ENP, ENT	•su		15	15		20] "
	CLR inactive			6	10		10]
	CLR Low	1		6	15		20		
Hold time, All Synchrono	us Inputs after CLK†	t _h		0	0		0		ns
Input Capacita	ince	CIN		5					pF
Power Dissipa	tion Capacitance*	C _{PD}		80					pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.



[†] For AC switching test circuits and timing waveforms see section 2.

- AND-Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Direct clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

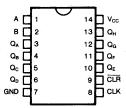
These are high-speed 8-bit registers with AND-gated serial inputs and an asynchronous clear. Data is entered serially through either one of the two inputs, A and B. A high on one input enables the other one, which will then determine the state of the first flip-flop. A low at either or both inputs inhibits data entry and resets the first flip-flop to a low level at the next positive clock transition.

Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of their clock input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLE

	Inputs		Outputs			
CLR	CLK	A	В	QA	Q _B .	Q _H
L	X	Х	Х	L	L	L
н	L	X	Х	QAO	Q _{BO}	Q_{HO}
Н	†	н	Н	н	Q_{An}	Q_{Gn}
н	↑	L	Χ	L	Q _{An}	Q_{Gn}
н	• 🕇	Х	L	L	Q _{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)

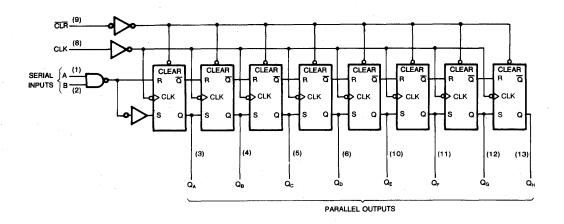
X = irrelevant (any input, including transitions)

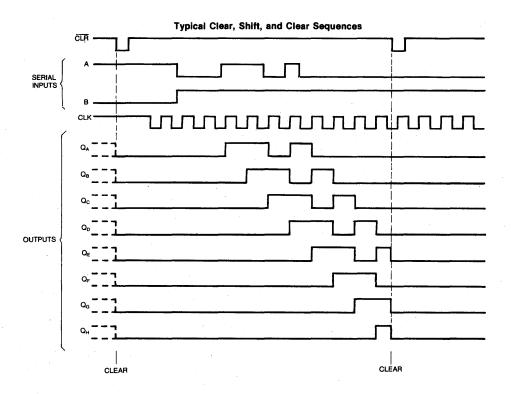
x = irrelevant (any input, including transit f = transition from low to high level.

 Q_{A0} , Q_{B0} , Q_{H0} =the level of Q_A , Q_B or Q_H , respectively, before the indicate steady-state input conditions were established.

 Q_{An} , Q_{Gn} = the level of Q_A or Q_G before the most-recent † transition of the clock; indicates a one-bit shift.

LOGIC DIAGRAMS





Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, P_d^{\dagger} 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	cc 4.5V to 5.5V
DC Input & Output	t Voltages*, V_{IN} , V_{OUT} OV to V_{CC}
Operating Temper	
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall 1	Times, t _r , t _f Max 500 ns
Unused inputs m	ust always be tied to an appropriate logic
voltage level (ei	ther V _{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

						· · · · · · · · · · · · · · · · · · ·	
Characteristic	Symbol	Symbol Test Conditions		= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_i≤2 ns), AHCT164

Charact	Characteristic Symbol Conditions		Conditions [†]	T _a = 25°C V _{CC} = 5.0V	1 1 = -40°C to +85°C		KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Maximum Clock Fr	equency	f _{max}		60	36		30		MHz
Propagation Delay, CLR to any Q		t _{PHL}	C _L =50pF	12		20		24	ns
Propagation Delay,		t _{PLH}	OL GOD!	11		18		21	ns
CLK to any Q		tpHL		11		18		21] "
Pulse Width	CLR Low	tw		8	12		15		ns
disc Width	CLK High or Low			8`	12		15		
Setup	Data			8	12		15		ns
Time before CLK1	CLR Inactive	- t _{su}		8	12		15		113
Hold Time Data after CLK†		t _h		0	4		5		ns
Input Capacitance		C _{IN}		5					pF
Power Dissipation	Capacitance*	C _{PD}	(per package)	120					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f_{in}$.



[†] For AC switching test circuits and timing waveforms see section 2.

- Complementary outputs
- · Direct overriding load (data) inputs
- · Gated clock inputs
- Parallel-to-Serial data conversion
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

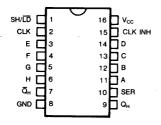
I_{OL} = 8 mA @ V_{OL} = 0.5V

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74AHCT: -40°C to 1.25°C

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These are high-speed 8-bit parallel-load or serial-in shift registers with complementary serial outputs available from the last stage. Parallel-in access is asynchronous and is enabled by pulling the SH/LD input low. When SH/LD is high, data is entered serially at the SER input and shifted one place to the right with each positive clock transition.

Clocking is accomplished through a 2-input NOR gate which permits one of the clocks to be used as a clock inhibit function. Holding either clock input high inhibits clocking. Either clock input is enabled by holding the other clock input low while the SH/LD input is high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

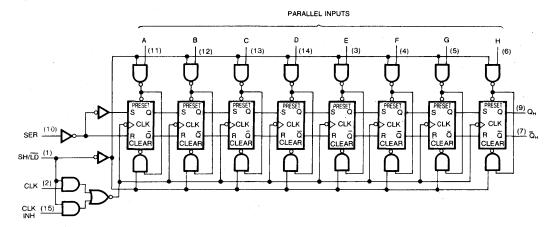
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

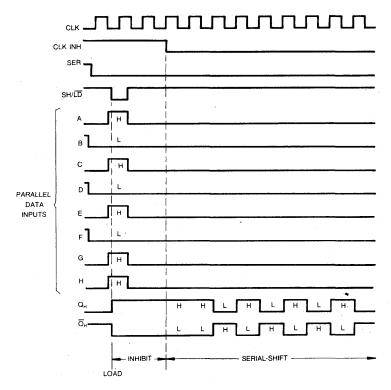
	Inputs		
SH/LD	CLK	CLK INH	Function
L	Х	Х	PARALLEL LOAD
H	H	х	NO CHANGE
Н	Х	н	NO CHANGE
Н	L	1	SHIFT*
Н	↑	L	SHIFT*

 $^{^{\}star}$ Content of each internal register shifts toward output Q_H. Data at serial input is shifted into first register.

LOGIC DIAGRAMS



Typical Shift, Load and Inhibit Sequences



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} , −0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур	Guaranteed Limits			
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0µA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT165

Characteristic		Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Maximum Clock Frequency		f _{max}		50	30		25		MHz
Propagation Delay, SH/LD to Q _H or Q _H		t _{PLH}		15		25		30	ns
		tpHL		15		25		30	
Propagation Delay, CLK to Q _H or Q _H		t _{PLH}	C _L =50pF	19		31		37	ns
		t _{PHL}	1	19		31		37	
Propagation Delay, H to Q _H or Q H		t _{PLH}		12		20		24	ns
		t _{PHL}		12		20		24	
Pulse Width	SH/LD Low	tw		8	12		15		ns
	CLK High or Low			8	12		15		
Setup Time	SH/LD High before CLK1			7	15		20		
	SER before CLK1			8	12		15		
	CLK INH Low before CLK1	tsu		7	15		20		ns
	CLK INH High before CLK↓			7	15		20		
	Data before SH/LD↑			5	8		10		
Hold Time	SER Data after CLK1	th		0	0		0		ns
	PAR Data after SH/LD1	ın		0	0		0		
Input Capacitance		CiN		- 5					рF
Power Dissipation Capacitance*		C _{PD}		100				,	ρF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin-

[†] For AC switching test circuits and timing waveforms see section 2.

FEATURES

- · Synchronous load
- · Direct overriding clear
- · Parallel to serial conversion
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

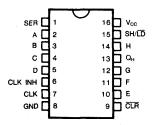
DESCRIPTION

These devices feature parallel-in or serial-in, serial-out registers, gated clock inputs and an overriding clear input. The paralled-in or serial-in modes are established by the shift/load input. When high, the input enables the serial data input and couples the eight fill-flops for serial shifting with each clock pulse. When low, the paralled data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running and the register can be stopped on command with the clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

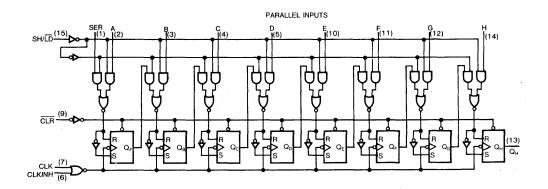
PIN CONFIGURATION



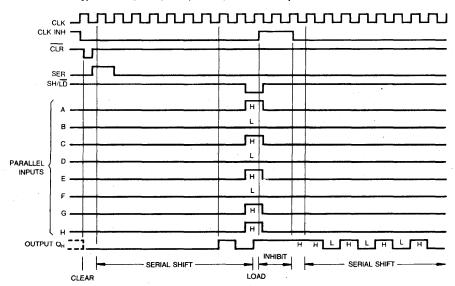
FUNCTION TABLE

		Intern	al Output				
CLR	SH/LD	CLK	01.4	SER	Parallel		
CLR	OH/LU	INH	CLK	SER	A H	Q _A C	В
L	Х	Х	Х	Х	X	LI	_ L
Н	X	L	L	X	X	Q _{A0} Q	во Оно
Н	L	L	1	X	a h	a i	h
Н	Н	L	†	H	X	НQ	An QGn
Н	H	L	↑	L	X		An QGn
Н	X	Н	1	X	X	G _{A0} Q	

LOGIC DIAGRAM



Typical Clear, Shift, Load, Inhibit, and Shift Sequences



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +/V
DC Input Diode Current, I _{IK}
$(V_l < -0.5V \text{ or } V_l > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage, \	/cc 4.5V to 5.5V
DC Input & Output	ut Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Tempe	rature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic
voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	_a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VıL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input tr, tr 42 ns), AHCT166

Characteristic		Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	T _a = -40°C	AHCT C to +85°C OV ± 10%	Ta = -55°C	AHCT to +125°C V ± 10%	Unit
				Тур	Min	Max	Min	Max	
Maximum Cl	ock Frequency	f _{max}		60	36		30		MHz
Propagation CLR to Q _H	Delay,	t _{PHL}	C _L =50pF	10		17		20	ns
Propagation	Delay,	tpLH	OL-20bi	13		21		25	
CLK to Q _H		t _{PHL}		13		21		25	ns
Pulse Width	CLR Low			8	12		15		ns
Puise width	CLK High or Low	tw		8	12		15		115
Setup Time	SH/LD High before CLK1			8	12		15		
	SER before CLK1	t _{su}		8	12		15		
	CLK INH before before CLK1			8	12		15		ns
	Data before SH/LD1			8	12		15		
	CLR Inactive before CLK			8	12		15		
	SH/LD High after CLK1			. 5	8		10		
	SER after CLK1			5	8		10		
Hold Time	CLK INH after CLK1	th		5	8		10		ns
	Data after SH/LD↑			5	8		10		
	CLR Active after CLK1			5	8		10		
Input Capac	itance	CiN		5					рF
Power Dissi	pation Capacitance*	C _{PD}							pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

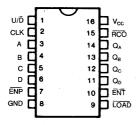
FEATURES

- Fully Synchronous Operation for Counting and Programming
- . Internal Look Ahead for Fast Counting
- . Carry Output for N-bit Cascading
- Fully Independent Clock Circuit
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74AHCT: --40°C to +85°C

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The '168 is a decade counter and the '169 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

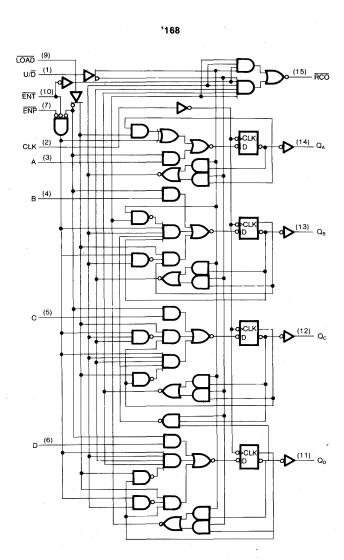
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{\text{ENP}}$ and $\overline{\text{ENT}}$) must be low to count. The direction of the count is determined by the level of the U/\overline{D} input. When U/\overline{D} is high, the counter counts up; when low, it counts down. Input $\overline{\text{ENT}}$ is fed forward to enable the carry output. The ripple carry output ($\overline{\text{RCO}}$) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transition at $\overline{\text{ENP}}$ or $\overline{\text{ENT}}$ are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, LOAD, U/D) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

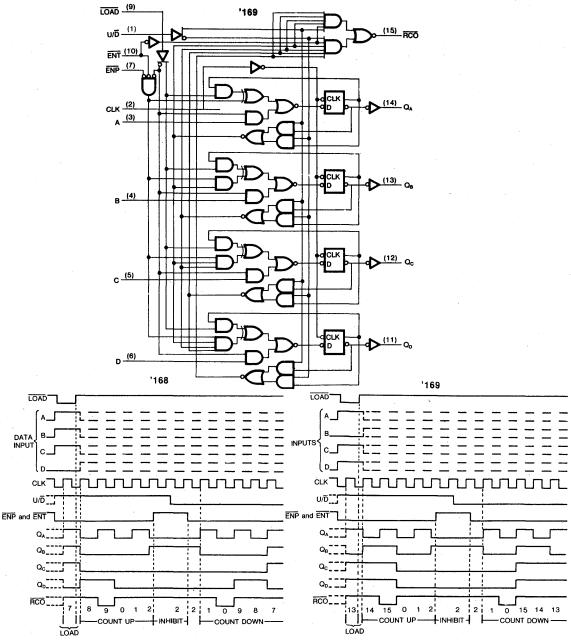
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAMS



LOGIC DIAGRAMS (continued)



Illstrated above is the following sequence:

- 1. Load (preset) to BCD seven
- 2. Count up to eight nine (maximum), zero, one, and two
- 3. Inhibit
- 4. Count down to one, zero (minimum), nine, eight, and seven

Illstrated above is the following sequence:

- 1. Load (preset) to BCD seven
- 2. Count up to eight nine (maximum), zero, one, and two
- Inhibit
- 4. Count down to one, zero (minimum), nine, eight, and seven



FUNCTION TABLE

OPERATING MODE			INP	OUTPUTS				
OPERATING MODE	CLK	U/D	ENP	ENT	LOAD	D _n	Qn	RCO
Parallel Load	↑	Х	Х	X	1	i	L	(1)
	†	X	· X	Х	i	h	Н	(1)
Count Up	1	h	1	1	h	Χ	Count Up	(1)
Count Down	1	ı	į.	i	h	Χ	Count Down	(1)
Hold	1	X	h	Х	h	X	q _n	(1)
	↑	X	X	h.	h	Χ	q _n	н

H=HIGH voltage level steady state

h=HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition

L=LOW voltage level steady state

I=LOW voltage level one setup time prior to the LOW-to-HIGH clock transition

X=Don't care

q=Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition

↑=LOW-to-HIGH clock transition

NOTE:

1. The RCO is LOW when ENT is LOW and the counter is at Terminal Count Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169.

The RCO is LOW when ENT is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for '168.

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} , −0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) + \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Abankuta Massimum Datinga ara thaga yakusa hayand

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур	Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3,84	V _{CC} -0.1	V
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	, ±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT168, AHCT169

Characteristic		Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C DV ± 10%	$KS54$ $T_a = -55^{\circ}C$ $V_{CC} = 5.0$		Unit
:				Тур	Min	Max	Min	Max	
Maximum Operating	g Frequency	f _{max}		50	40		35		MHz
Propagation Delay,		t _{PLH}		14		20		27	ns
CLK to RCO		t _{PHL}		14		20		27	HS
Propagation Delay,		t _{PLH}	*	12		18		22	
CLK to Any Q	•	t _{PHL}	0 50=5	12		18		22	ns
Propagation Delay, ENT to RCO		tpLH	C _L =50pF	10		16		19	
		t _{PHL}		10	-	16		19	ns
Propagation Delay,		t _{PLH}		13		19		24	
U/D to RCO				13		19		24	ns
Pulse Duration, CLK high or low		t _w		8	12		15		ns
Setup Time,	A, B, C or D			9	15		20		
Before CLK1	ENP or ENT			9	15		15		
	LOAD			9	15		20		ns
	U/D			9	15		, 20		
Hold Time, Data after CLK1	-	t _h		0	0		- 0		ns
Input Capacitance		CIN		5					pF
Power Dissipation (Capacitance*	C _{PD}							рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.



FEATURES

- Gated output control lines for enabling or disabling the outputs
- Fully independent clock for operation in parallel-load or hold modes
- · For application as bus buffer registers
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - I_{OL} = 24 mA @ V_{OL} = 0.5V for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These 4-bit registers contain D-type flip-flops with 3-state outputs, capable of driving highly-capacitive or low-impedance loads. This provides the device with the capability of being connected directly to and driving the bus lines in a busorganized system without need for interface or pull-up components.

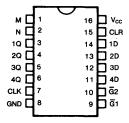
Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gated output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



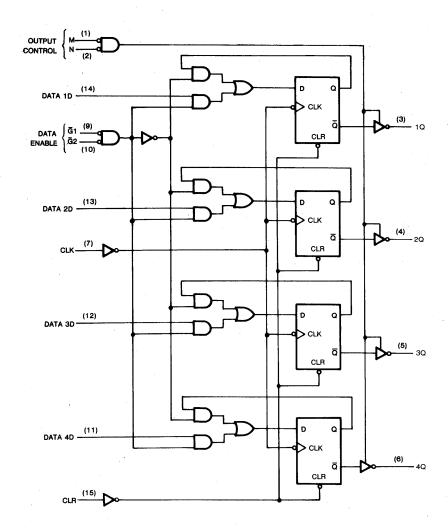
FUNCTION TABLE

	Output					
CLR	CLK	Data	Enable	Data	Q	
CER	OLK	Ğ1	G2	D	-	
Н	Х	Х	Х	Х	L	
L	L	X	X	X	Q ₀ Q ₀ Q ₀	
L	†	H	X	X	Qo	
L	†	X	н	Х	Q ₀	
L	1	L	L	L	L	
L	†	L	L	н	Н.	

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.



LOGIC DIAGRAM



4

Absolute Maximum Ratings*

posure to these conditions may affect device reliability.

Supply Voltage Range V_{CC}, -0.5V to +7V

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to V_{CC}
Operating Temperature	

Range KS74AHCT: $-40^{\circ}\text{C to } +85^{\circ}\text{C}$ KS54AHCT: $-55^{\circ}\text{C to } +125^{\circ}\text{C}$ Input Rise & Fall Times, t_r , t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit		
			Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} -0.1	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v		
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT173

Charact	Characteristic		Cond	litions†	T _a = 25°C V _{CC} = 5.0V	T. = -40°C to +85°C		KS54AH $T_a = -55^{\circ}C \text{ to}$ $V_{CC} = 5.0V$	Unit		
					Тур	Min	Max	Min	Max		
Maximum Cloc	k Frequency	f _{max}			50 .	30		25		MHz	
Propagation Delay, CLK to any Q		tpLH	C _L =50pF C _L =150pF		13 16		21 26		25 31	ns	
		t _{PHL}	C _L =50pF C _L =150pF		13 16		21 26		25 31	115	
Propagation D CLR to any Q		t _{PHL}	C _L =50pF C _I =150pF		15 18		25 30		30 36	ns	
Output Enable Time, M or N to any Q		t _{PZH}	5 41.0	C _L =50pF C _L =150pF	12 15		20 25		24 30		
		tpZL	$R_L = 1 k\Omega$	C _L =50pF C _L =150pF	12 15		20 25		24 30	ns	
Output Disable	e Time,	t _{PHZ}	R _L =1kΩ, C	0 = 50pF	10		17		20	ns	
M or N to any	Q	tpLZ			10		17		20		
Pulse Width	CLK High or Low	t _w			7	12		15		ns	
disc Widin	CLR High	· w			7	12		15			
	G1 and G2				8	15		20			
Setup Time,	Data	t _{su}			7	12		15		ns	
before CLKf	CLR Inactive	130			7	12		15		,,,	
Hold Time	G1 and G2	th			-3	0		0		ns	
After CLK1	Data	-11				0		0		,,,3	
Input Capacita	nce	CIN			5					рF	
Output Cipacit	ance	Соит	Output Disa	abled	10			,		pF	
Power Dissipation Capacitance*		C _{PD}								pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

KS54AHCT 174/175

Hex/Quad D-type Flip-Flops with Clear

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

The '174 contains six, and the '175 contains four D-type filp-flops all sharing a common clock and a common clear. The '174 features single nail outputs for every flip-flops whereas the '175 has complementary outputs.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATIONS

174 CLR ☐ V_{cc} <u></u> 60 2 15 1D [3 □ 6D 2D [5D 13 2Q 🗌 12 5Q зр 🗌 6 **□** 4D 3Q 🗆 **□** 40 10 GND 🗆 CLK

		175		
CLR 1Q 1Q 1Q 1D 2D 2Q 1Q 1D 1D 1D 1D 1D 1D 1	1 2 3 4 5 6 7 8		16 15 14 13 12 11 10 9	V _{cc} 4Q 4Q 4D 3D 3Q CLK
				•

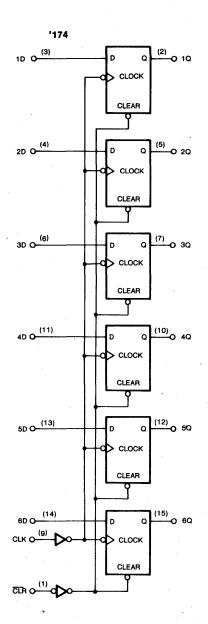
FUNCTION TABLE

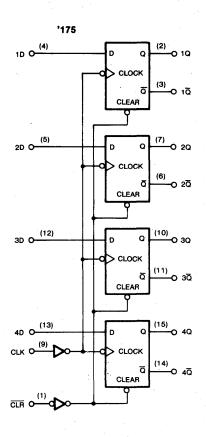
(Each Flip-Flop)

1	nputs	Out	puts	
CLR	CLK	D	Q	Q١
L	Х	Х	L	Н
Н	^ †	Н	н	L
н	1	L	L	Н
· H	L	Χ	Q ₀	\overline{Q}_0

† '175 only

LOGIC DIAGRAMS





KS54AHCT 174/175 KS74AHCT

Hex/Quad D-type Flip-Flops with Clear

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vcc	3		4.5V	to 5.5V
DC Input & Output	Voltages*, V _{IN} ,	Vout	0	to Vcc
Operating Temperat	ure			
D	LOTABLIOT			

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т	_a = 25°C	KS74AHCT T _a = -40°C to +85°C	K\$54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL		,	0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} −0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	V
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _i =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	, 3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT174, AHCT175

Charac	Symbol	l Conditions†	T _A = 25°C V _{CC} = 5.0V	TA = -40°0	AHCT C to +85°C DV ± 10%	KS54 T _A = -55°C V _{CC} = 5.0	Unit		
				Typ 70	Min	Max	Min	Max	
Maximum Clock Fr	requency	f _{max}			50		40		MHz
Propagation Delay		tpLH		11		17		20	ns
CLK to Q or Q		t _{PHL}	-	- 11		17		20	115
Propagation Delay,		telH		12		21		25	ns
CLR to Q or Q		t _{PHL}		12		21		25	113
Setup	Data			6	10		15		ns
Time before CLK1	CLR Inactive	t _{su}		4	6		8		IIS
Hold Time, Data after CLK1		t _h		0	0		0		ns
Pulse	CLK High or Low		`	6	10		15		ns
Width	CLR Low	- t _w		6	10		15		113
Input Capacitace		CIN		5					pF
Power Dissipation	Capacitance*	C _{PD}							рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES.

• Arithmetic operating modes:

Addition

Subtraction

Shift operand A one position

Magnitude comparison

Plus 12 other arithmetic operations

· Logic function modes:

Exclusive-OR

Comparator

AND, NAND, OR, NOR

Plus 10 other logic operations

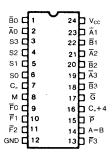
- Full look-ahead for high-speed operations on long words
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current Outputs:
 I_{OL} = 8mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATION



DESCRIPTION

The '181 is an Arithmetic Logic Unit (ALU)/Function Generator that performs 16 binary arithmetic operations on two 4-bit words as shown in table 1 and 2. These operations are selected by the four functions select lines (S0, S1, S2, S3) and include addition, subtraction, decrement and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low level voltage to the mode control input(M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of 2 cascadeoutputs (P and G) for the 4-bits in the package. When used in conjunction with AHCT182, high-speed arithmetic operation can be performed. The typical addition times shown in table below illustrates how little is required for addition of longer words when full carry look-ahead is employed.

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small lengths can be performed without external circuitry.

The '181 will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires and end-around or forced carry to provide A-B.

The '181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of the equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with C_n =H when performing the comparison. The A=B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subract mode by placing the function select input S3, S2, S1, S0 at L,H,H,L respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two boolean variables without the use of external circuitry. These logical functions are selected by use of the four function select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry.

The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, OR and NOR functions.

Pin number	2	1	23	22	21	20	19	18	9_	10	11	13	7	16	15	17
Active-Low Data (Table1)	Āo	Βo	Ã ₁	B ₁	Ā ₂	B ₂	Āз	Ē₃	Fo	F ₁	F ₂	F ₃	`C _n	C _n +4	P	G
Active-High Data (Table 2)	Ao	Bo	A ₁	B ₁	A ₂	B ₂	Аз	Вз	Fo	F ₁	F ₂	Fз		\overline{C}_n+4	Х	Υ



ALU SIGNAL DESIGNATION

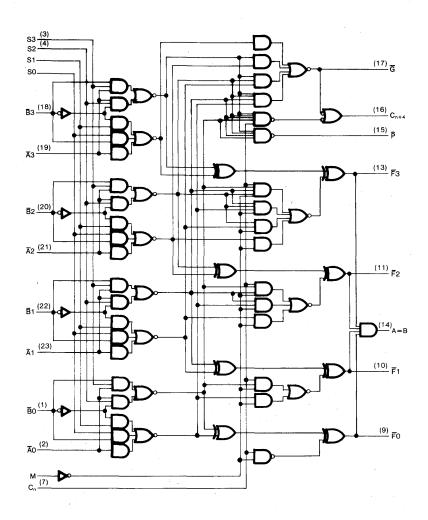
The '181 can be used with the signal designations. The logic functions and arithmetic operations obtained with signal designations as in Table 1.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels

allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM





O Table 1

	Sala	ction		Active-Low Data							
	3010	CHON		M = H	M = L; Arithmetic Operations						
S 3	S2	S1	S0	Logic Functions	C _n =L (no carry)	C _n = H (with carry)					
L	L	L	L	F=Ā	F=A Minus 1	F=A					
L	L	L	H	F=ÃB	F=AB Minus 1	F=AB					
L	L	н	L	F=A + B	F=AB Minus 1	F=AB					
L	L	н	н	F=1	F=Minus 1 (2's Comp)	F=Zero					
L	н	L	L	$F = \overline{A + B}$	F=A Plus (A + B)	F=A Plus (A + B) Plus 1					
L	Н	L	н	F=B	$F = AB Plus (A + \overline{B})$	F=AB Plus (A + B) Plus 1					
L	н	н	L	F=Ā⊕B	F=A Minus B Minus 1	F=A Minus B					
L	н	н	· H	F=A + B	F=A + B	F=(A + B) Plus 1					
. Н	L	L	L	F=\(\overline{A}B\)	F=A Plus (A + B)	F=A Plus (A + B) Plus 1					
Н	L	L	н	F=A⊕B	F=A Plus B	F=A Plus B Plus 1					
Н	L	н	L	F=B	F=AB Plus (A + B)	F=AB Plus (A + B) Plus 1					
Н	L	Н	н	F=A + B	F=(A + B)	F=(A + B) Plus 1 *					
н	Н	L	L	F=0	F=A Plus A*	F=A Plus A Plus 1					
Н	Н	L	н	F=AB	F=AB Plus A	F=AB Plus A Plus 1					
Н	н	H	L	F=AB	F=AB Plus A	F=AB Plus A Plus 1					
Ĥ	Н	Н	н	F=A	F=A	F=A Plus 1					

O Table 2

	Sala	ction		Active-High Data							
	7 3010	Ction		M = H	M = L; Arith	metic Operations					
S3	S2	S 1	S0	Logic Functions	C _n =L (no carry)	C _n = H (with carry)					
L	L	L	L	F=Ā	F=A	F=A Plus 1					
L	. L	L	Н	$F = \overline{A + B}$	F=A + B	F=(A + B) Plus 1					
L	L	H	L	F=ĀB	$F=A+\overline{B}$	F=(A + B) Plus 1					
L	L	Н	Н	F=0	F=Minus 1 (2's Comp)	F=Zero					
L '	Н	· L	L	F=AB	F=A Plus AB	F=A Plus AB Plus 1					
L	Н	L	Н	F= B	$F=(A + B) Plus A\overline{B}$	F=(A + B) Plus AB Plus 1					
L	н	Н	L	$F = \overline{A \oplus B}$	F=A Minus B Minus 1	F=A Minus B					
L	н	н	н	F=AB	F=AB Minus 1	F=AB					
Н	L	L	L	F=A + B	F=A Plus AB	F=A Plus AB Plus 1					
н	L	L	Н	F=A⊕B	F=A Plus B	F=A Plus B Plus 1					
н	L	H	L	F=B	F=(A + B) Plus AB	F=(A + B) Plus AB Plus 1					
Н	L	Н	Н	F=AB	F=AB Minus 1	F=AB					
Н	H	L	L	F=1	F=A Plus A*	F=A Plus A Plus 1					
н	H	L	Н	F=A + B	F=(A + B) Plus A	A=(A + B) Plus A Plus 1					
Н	Н	. н	L	F=A + B	F=(A + B) Plus A	F=(A + B) Plus A Plus 1					
Н	н	н	Н	F=A	F=A Minus 1	F=A					

^{*} Each bit is shifted to the next more significant position

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pdt 500 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	Vcc
Operating Tempe	rature
Range	KS74AHCT: -40°C to +85°C
-	KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH .			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{ОН}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0µA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

INPUT PAIRS HIGH/NOT HIGH TEST TABLE FUNCTION INPUTS: S2 = M = 4.5 V, S0 = S1 = S3 = 0 V

PARAMETER	INPUT			OTHER DA	TA INPUTS	OUTPUT	OUTPUT WAVEFORM
	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	TEST	
t _{PLH}	Τλi	Bi	None	Remaining	Remaining	Ē	In-Phase
t _{PHL}	1 4	ы	None	Ā, C _n	B	F	in-Phase
tpLH	Bi	Āi	None	Remaining	Remaining	P	In-Phase
t _{PHL}	В	A	None	₿, C _n	· Ā	F	in-Friase
t _{PHL}	Āi	Bi	NI	Remaining	Remaining	Cn+4	Out-of-Phase
t _{PHL}	A	В	None	A, Cn	B	Un ^{∓4}	Out-oi-Filase
tpLH	Bi	Āi	None	Remaining	Remaining	Cn+4	Out-of-Phase
t _{PHL}	1 51	A	None	B, C _n	Ā	UnT4	Out-Oi-Filase

PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE FUNCTION INPUTS: S0=S3=4.5 V, S1=S2=M=0 V

PARAMETER	INPUT UNDER	OTHER SAMI		OTHER DA	TA INPUTS	OUTPUT UNDER	OUTPUT WAVEFORM	
	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	TEST		
t _{PLH}	Āi	Bi	None	Remaining	Cn	Fi	In-Phase	
t _{PHL}	Λ'	J.	None	A and B.	On I		#11 Hade	
t _{PLH}	Bi	Āi	None	Remaining	Cn	Fi	In-Phase	
t _{PHL}	ы	^'	None	Ā and B̄	On On	''	iii i ilase	
tpLH	Āi	Bi	None	None	Remaining	P	In-Phase	
t _{PHL}	^'	. 5	None	None	\overline{A} and \overline{B} , C_n	F	III-FIIASE	
t _{PLH}	Bi	Αi	None	None	Remaining	Ē	In-Phase	
t _{PHL}	Ы	A	None		\overline{A} and \overline{B} , C_n			
t _{PLH}	Āi	None	Bi	Remaining	Remaining	G	In-Phone	
t _{PHL}	A	None	ы	B	Ā, Cn			
tpLH	Bi	NI	Āi	Remaining	Remaining	G		
t _{PHL}	ы	None	AI	B	⊼, C _n	G	In-Phase	
t _{PLH}	_	None	None	All	All	Any F	In-Phase	
t _{PHL}	C _n	None None	Ā	· B .	or C _n +4	iii-Pliase		
tpLH	Āi	None	Bi	Remaining	Remaining	C _n +4	Out-of-Phase	
t _{PHL}	Ai		Ā, C _n	Un∓4	Out-oi-Phase			
t _{PLH}	Bi	None	⊼;	Remaining	Remaining		Out-of-Phase	
t _{PHL}	В	None Āi		B Ā, Cn		C _n +4	Out-or-Phase	

AC ELECTRICAL CHARACTERISTICS (Input t, t <2 ns), AHCT181

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	Ta = -40°0	AHCT C to +85°C OV±10%	$T_a = -55$ °C	AHCT to +125°C V± 10%	Unit
		C _L = 50pF	Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	M=0V,	8		14		17	ns
C _n to C _n +4	tent	Sum or Diff Mode	8		14		17	
Propagation Delay,	tpLH	M=S1=S2=0V	16		24		29	ns
A or B to C _n +4	t _{PHL}	S0=S3=4.5V	16		24		29	
Propagation Delay,	T _{PLH}	M=S0=S3=0V	17		25		30	ns
A or B to C _n +4	tPHL	S1=S2=4.5V	17		25	,	30	,,,,
Propagation Delay	t _{PLH}	M=S1=S2=0V	17		25		30	ns
Ā or B to G	t _{PHL}	S0=S3=4.5V	·17		25		30	,,,5
Propagation Delay	t _{PLH}	M=S0=S3=0V	17		25		30	ns
A or B to G	t _{PHL}	S1=S2=4.5V	17		25		30	110
Propagation Delay	t _{PLH}	M=S0=S3=0V	15		23		27	ns
Ā or B to P	tpHL	S1=S2=4.5V	15		23		27	
Propagation Delay	t _{PLH}	M=S1=S2=0V	16		24		29	ns
Ā or B to P	t _{PHL}	S0=S3=4.5V	16		24		29	,,,
Propagation Delay	t _{PLH}	M=S1=S2=0V	20		29		35	ns
A or B to Fi	t _{PHL}	S0=S3=4.5V	20		29		35	110
Propagation Delay	tpLH	M=S0=S3=0V	19		27		32	ns
A or B to F	t _{PHL}	S1=S2=4.5V	19		27		32	""
Propagation Delay	tpLH	M=4.5V	16		24		29	ns
A or B to F	t _{PHL}	111 4.51	16		24		29	
Propagation Delay	t _{PLZ}	M=S0=S3=0V	19		27		32	ns
Ā or B to A=B	tpzL	S1=S2=4.5V	16		24		29	1.0
Propagation Delay	tPLH		15		23		24	ns
C _n to any F	t _{PHL}		15		23		27	
Input Capacitance	CIN		5 ·					рF
Power Dissipation Capacitance*	C _{PD}							pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.
† For AC switching test circuits and timing waveforms see section 2.

PARAMETER MEASUREMENT INFORMATION

LOGIC MODE TEST TABLE FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER	OUTPUT WAVEFORM			
	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	TEST				
ţрLН	Āi	Bi	None	None	None N	None None	None	Remaining	Fi	Out-of-Phase
t _{PHL}	_ AI	ы	None	None	\overline{A} and $\overline{\overline{B}}$, C_n	-	Out-or-rhase			
telh	Bi	Āi	None	None	Remaining	Fi	Out-of-Phase			
t _{PHL}	Ы	^	None.	None	\overline{A} and \overline{B} , C_n		Out-or-Friase			

INPUT BITS EQUAL/NOT EQUAL TEST TABLE FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V

PARAMETER	INPUT UNDER	1	OTHER INPUT SAME BIT		TA INPUTS	OUTPUT UNDER	OUTPUT WAVEFORM	
•	TEST APPLY 4.5 V APPLY GND		APPLY 4.5 V	APPLY GND	TEST	,		
tpLH	Āi	Bi	None	Remaining	None	Ē	Out-of-Phase	
t _{PHL}		ы	None	\overline{A} and \overline{B} , C_n	None		Out-OI-I Hase	
tpLH	Bi	Āi	None	Remaining	None	P	Out-of-Phase	
t _{PHL}) 5 i	^'	None	Ā and Ē, C _n	None	F	Out-or-riase	
t _{PLH}	Ãi	None	Bi	Remaining	None	P	In-Phase	
t _{PHL}	A	None	ы	Ā and █, C _n	None	F	III-I IIasc	
t _{PLH}	Bi	None	Remaining None	None	P	in-Phase		
t _{PHL}	ы	None	^'	A and B, C _n	None		III-Friase	
t _{PLH}	Āi	Bi	Ness	Remaining	Nana	C _n +4	In-Phase	
t _{PHL}	AI .	ы	None	\overline{A} and \overline{B} , C_n	None	Un ⁺ 4		
t _{PLH}	Bi	Āi	None	Remaining	None	C _n +4	In-Phase	
t _{PHL}	ы	Al	None	\overline{A} and \overline{B} , C_n	None	C _n T4	III-FIIASE	
t _{PLH}	Āi	None	Bi	Remaining	None	C _n +4	Out-of-Phase	
t _{PHL}	AI.	None	131	Ā and Ē, C _n	INONE	Un T4	Out-of-Filase	
t _{PLH}	Bi	None	Āi	Remaining	None	C +4	Out-of Phase	
t _{PHL}	DI	None	AI	\overline{A} and \overline{B} , C_n	None	C _n +4	Out-of Phase	

. DIFF MODE TEST TABLE FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER	OTHER SAMI		OTHER DA	TA INPUTS	OUTPUT	OUTPUT WAVEFORM
	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	TEST	
t _{PLH}	Āi	None	Bi	Remaining	Remaining	Fi	In-Phase
t _{PHL}	_ ^'	None	Di .	Ā	B, C _n	''	III-I Mase
t _{PLH}	Bi	Āi	None	Remaining	Remaining	Fi	Out-of-Phase
tenL		<u></u>	None	Ā	B̄, C _n	''	Out of I flase
tPLH	Ai	None	Bi	None	Remaining	P -	In-Phase
t _{PHL}	Α.	None	J	None	\overline{A} and \overline{B} , C_n	'	III I Hase
t _{PLH}	Bi	Āi	None	None	Remaining	P	Out-of-Phase
t _{PHL}	5,	<u> </u>	None	None	\overline{A} and \overline{B} , C_n		Out of Fridge
tPLH	· Āi	Bi None	None	Remaining	G	In-Phase	
t _{PHL}	A	, Di	140116	None	\overline{A} and \overline{B} , C_n	ŭ	iii i ilasc
tpLH	Bi	None	one Āi	None	Remaining	G	Out-of-Phase
t _{PHL}		None	Λ'	None	A and B, C _n	ŭ	Out-of-1 hase
t _{PLH}	Δi	Ti None Ei	Āi None Bi	Remaining	Remaining	A≔B	In-Phase
t _{PHL}	Α'	None		Ā	B, C _n	ΑΒ	III i ilase
tpLH	Bi	Āi	None	Remaining	Remaining	A=B	Out-of-Phase
t _{PHL}		0,	None	Ā	B, C _n	7-0	Out-or-mase
t _{PLH}	Cn	None	None	All	None	C _n +4	In-Phase
t _{PHL}	On .	140110	140HG	\overline{A} and \overline{B}	TTOTIC	or any F	III-FIIase
t _{PLH}	Āi	Bi	None	None	Remaining	Cn+4	Out-of-Phase
t _{PHL}		ы	NONE	NONE	A, B, C _n	On 1 7	Out OF Hase
t _{PLH}	Bi	None	Āi	None	Remaining	C _n +4	In-Phase
t _{PHL}	, id	None	. 8	None	A, B, C _n	On 14	iii-Filase



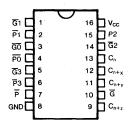
FEATURES

- Compatible Carry Functions for direct ALU connection
- Cascadable to perform look-ahead across n-bit adders.
- High output current drive: I_{OL} = 8mA @ V_{OL} = 0.5V
- Low power consumption characteristic of CMOS
- Direct interface capability to TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '182 is a high-speed, look-ahead carry generator, capable of anticipating a carry across four binary adders or group of adders. These devices can be cascaded to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjuction with the AHCT181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each 182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true from, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Logic equations for the 182 are:

Cn+x=G0 + P0 Cn Cn+y=G1 + P1 G0 + P1 P0 Cn Cn+z=G2 + P2 G1 + P2 P1 G0 + P2 P1 P0 Cn G=G3 + P3 G2 + P3 P2 G1 + P3 P2 P1 G0 P=P3 P2 P1 P0

PIN DESIGNATIONS

Designation	Pin No	Function
GO,G1,G2,G3 3,1,14,5		Active Low Carry Generate Inputs
PO,P1,P2,P3	4,2,15,6	Active Low Carry Propagate Inputs
Cn	13	Carry Input, Active HIGH
Cn+x, Cn+y, Cn+z	12,11,9	Carry Outputs
G	10	Active Low Carry Generate Output
P	- 7	Active Low Carry Propagae Output
Vcc	16	Supply Voltage
GND 8		Ground

FUNCTION TABLES

FOR GOUTPUT

	INPUTS							
ĞЗ	Ğ2	Ğ1	Gō	₽3	P2	P1	Ğ	
L	Х	Х	Х	Х	Х	Х	L	
Х	L	Χ	Χ	L	Χ	Х	L.	
X	Χ	L	Х	L	L	Х	L	
X	Χ	X	L	L	L	F.	L	
	All other combinations							

FOR P OU	TPUT
INPUTS	OUTPUT
P3 P2 P1 P0	Ē
LLLL	L
All other combinations	н

FOR	C _n +	DUTPUT	
1	IPUT	OUTPUT	
GΟ	ΡŌ	Cn	C _n + x
L	Х	Х	Н
Х	L	Н	н
	l othe binat	L	

Cn+y OUTPUT

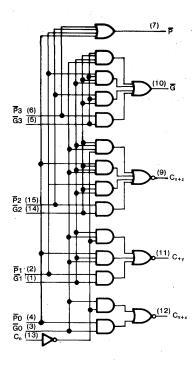
		INPUTS			OUTPUT
Ğ1	G0	₽1	PO	Cn	C _{n+y}
L	Х	Х	Х	Х	Н
'X	L	L	X	Х	н
X	X	L	L	H	н
	All othe	r combi	inations		L

Cn+z OUTPUT

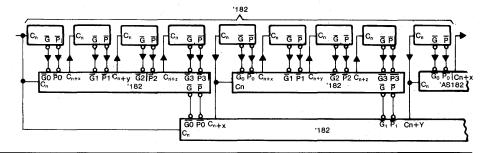
	INPUTS										
G2	G1	GΘ	Ē2	₽1∍	PO	Cn	C _n +z				
L	Х	Х	Х	Х	Х	Х	Н				
X	L	X	L	X	Х	Х	H				
X	Х	L	L	L	Х	Χ	Н				
X	X	X	L	L	L	Н	н				
	All	other c	ombin	ation	s		L				

H= high-level, L= low level, X= don't care Any inputs not shown in a given table are don't care with respect to that output.

LOGIC DIAGRAM



Figure; THE '182 IN A 64-BIT LOOK-AHEAD CARRY CIRCUIT



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IoK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	Voh	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20\mu A$ $I_O = -4mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tre2 ns), AHCT182

Characteristic	Symbol	Symbol	Symbol Conditions†		T _e = 25°C V _{CC} = 5.0V	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		KS54 T _a = -55°C V _{CC} = 5.0	Unit
			Тур	Min	Max	Min	Max		
Propagation Delay,	t _{PLH}	C _I = 50pF	12		20		24	ns	
Pi or Gi to C _{n+x} C _{n+y} , C _{n+z}	tpHL	OLOOPI	12		20		24	115	
Propagation Delay,	tpLH	C _L =50pF	12		20		24	ns	
Pi or Gi to G	t _{PHL}	оц-оорі	. 12		20		24		
Propagation Delay,	tpLH	C _L =50pF	15		21		26	ns	
C _n to C _{n+x} , C _{n+y} , C _{n+z}	t _{PHL}	OL-30pi	15		21		26	IIS	
Propagation Delay	t _{PLH}	C _L =50pF	11		18		21	ns	
Pi to P	tpHL	OL-30bi	11		18		21	113	
Input Capacitance	CiN		5					рF	
Power Dissipation Capacitance*	C _{PD}							рF	

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

 $^{^{\}dagger}$ For AC switching test circuits and timing waveforms see section 2.

FEATURES

- · For use in high-speed wallace-tree summing
- Fast addition operation
- Low power consumption characteristic of CMOS
- High output current drive: I_{OL} = 8mA @ V_{OL} = 0.5V
 Direct interface capability with TTL NMOS and
- Direct interface capability with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to + 85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

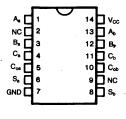
DESCRIPTION

The '183 is a dual full adder features an individual carry output from each bit for use in multiple-input, carry-save techniques to produce the true sum and true carry outputs with no more than 2 gate delays.

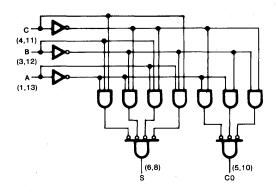
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Half)

	Inputs	Output			
A	В	С	s	C _o	
L	L	L	L	L	
Н	' L '	L	Н	L	
L	Н	L ·	н	. L	
L	L	. н	H	L	
H.	н	L.	Ł	Н	
н	L	н	L	H	
L	н	Н	L	` н	
Н	• н	Н	Н	Н	

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, \	/cc	4.5V to 5.5V
DC Input & Outpu	ıt Voltages*, V _{IN} ,	Vout OV to Vcc
Operating Temper	rature	
Range	KS74AHCT:	-40°C to +85°C

KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic
voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic Sy	Symbol	Test Conditions	T,	= 25°C	$ \begin{array}{c} \text{KS74AHCT} \\ \text{T}_{\text{a}} = -40^{\circ}\text{C to } +85^{\circ}\text{C} \end{array} $	$ \begin{array}{c} \text{KS54AHCT} \\ \text{T}_{a} = -55^{\circ}\text{C to } +125^{\circ}\text{C} \end{array} $	Unit
·			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in V _I =2.4V other inputs: at V _{CC} or GND lout=0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), AHCT183

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	t _{PLH}	CL=50pF	10		15		18	ns
	t _{PHL}	OL-OOP!	13		20		24	
Input Capacitance	CiN		5					рF
Power dissipation Capacitance*	C _{PD}							рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.



Synchronous 4-Bit Up/Down

FEATURES

- Single down/up count control line
- Look-ahead circuit enhances speed of cascaded
- Fully synchronous in count modes
- Asynchronously presettable with load control
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

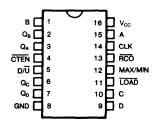
IOL = 8 mA @ VOL = 0.5V

- . Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

OPERATING MODE		OUTPUTS				
OPERATING MODE	LOAD	D/Ū	CTEN	CLK	Input	O _n
parallel load	L L	X	X X	X X	L H	L H
count up	н	L	L	t	Х	count up
count down	н	н	1	t	х	count down
hold (do nothing)	н	X	Н	X	х	no change

RCO AND MAX/MIN FUNCTION TABLE

	INPUTS		TERMINAL COUNT STATE					OUTPUTS		
D/Ū	CTEN	CLK	QA	QB	Qc	QD	MAX/MIN	RCO		
н	Н	х	Н	×	x	н	L	н		
L	H	Χ.	н	x	x	н	н	н		
L	L	IJ	н	x	х	н.	TL	ᄺ		
L	н	Х	L	L	L	L	L	н		
н	H	х	L	L	L	L	H	н		
н	L	1.5	L	L	L	L	T.	. 77		

- H = HIGH voltage level
- L = LOW voltage level
- LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition
- Don't care
- = LOW-to-HIGH CLK transition
- one LOW level pulse
- L = MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

DESCRIPTION

These are high-speed synchronous reversible 4-bit decade counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-tohigh-level transition of the clock input if the enable input (CTEN) is low. A high at CTEN inhibits counting. The direction of the count is determined by the level of the down/up (D/U) input. When D/U is low, the counter counts up and when D/U is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs (CTEN and D/U) that will modify the operating mode have no affect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

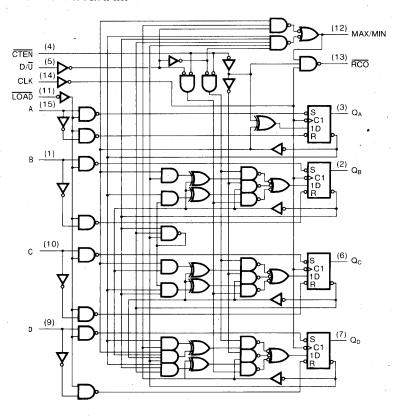
These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

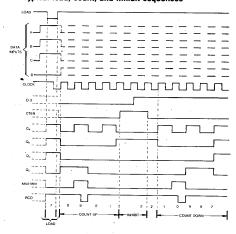
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and around.

LOGIC DIAGRAM



Typical load, count, and inhibit sequences



Sequence;

- (1) Load (preset) to BCD seven.
- (2) Count up to eight, mine(maximum) zero, one, and two.
- (3) Inhibit
- (4) Count down to one, zero (minimum), nine, egiht, and seven

NOTE A: Clear overrides load data, and count inputs.

Note B:When count up, count-down input must be high;
when counting down, countup intput must be high.

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	a = 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	$KS54AHCT$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit	
			Тур	Guaranteed Limits				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	V	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT190

Characteristic		Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Maximum Clo	ck Frequency	f _{max}		50	- 30		25		MHz
Propagation [Delay,	t _{PLH}		18		30		36	ns
LOAD to any	Q	t _{PHL}		18		30		36	113
Propagation [Delay,	t _{PLH}		13		21		25	ns
A,B,C, D to a	iny Q	t _{PHL}		13		21		25	
Propagation [Delay,	tpLH		12		20		24	ns
CLK to RCO		t _{PHL}		12		20		24	115
Propagation [Delay,	tpLH	1	11		18		22	ns ns
CLK to any C	1	tpHL	050-5	11		18		22	
Propagation [Delay,	telh	C _L =50pF	19		31		37	
	CLK to MAX/MIN			19		31		37	115
Propagation [Delay,	t _{PLH}		19		32		38	ns
D/U to RCO		t _{PHL}		19		32		38	
Propagation [Delay,	t _{PLH}		15		25		30	
D/U to MAX/	MIN	tpHL		15		25		30	ns
Propagation [Delay,	tpLH		11		18		22	
CTEN to RCC	5	t _{PHL}	1	11		18		22	
Pulse Width	CLK High or Low	tw		10		17		20	ns
i dise widin	LOAD Low	- lw		12		20		25	
	Data before LOAD1	t _{su}		10	17		20		
Setup Time	CTEN before CLK1			10	17		20		ns
Octup Time	D/Ū before CLK↑			10	17		20		113
	LOAD Inactive before CLK1			10	17	,	20		
Hold Time	Data after LOAD1			2	4		5		
	CTEN after CLK1] t _h		0	0		0		ns
	D/U after CLK†			0	0		0		
Input Capacitance		· CiN		5					pF.
Power Dissipation Capacitance*		CPD		80					pF

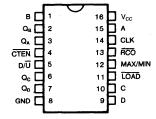
^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

FEATURES

- Single down/up count control line
- Look-ahead circultry enhances speed of cascaded counters
- Fully synchronous in count modes
- Asynchronously presettable with load control
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
- KS74AHCT: -40°C to +85°C
- KS54AHCT: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

OPERATING MODE	1	OUTPUTS				
OPERATING MODE	LOAD	D/Ū	CTEN	CLK	Input	O _n
parallel load	L	X	X	X X	L H	L H
count up	н	L	1	t	Х	count up
count down	н	Н		t	Х	count down
hold (do nothing)	н	X	н	X	×	no change

RCO AND MAX/MIN FUNCTION TABLE

INPUTS			TER	MINAL C	OUTPUTS			
D/Ū	CTEN	CLK	QA	QB	Qc	QD	MAX/MIN	RCO
Н	Н	Х	Н	Х	Х	Н	· L	Н
L	H	Х	Н	X	X	H	н	н
L	L	П	Н	Х	X	- н	1 TL	T
L	н	х	L	L	- Ł	L	L	н
н	Н :	Х	L	L	L.	L	H	н
н	L	J	L	L	L	L	1	П

- H = HIGH voltage level
- L = LOW voltage level
- I = LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition
- X = Don't care
- † = LOW-to-HIGH CLK transition
- T = one LOW level pulse
- L = MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

DESCRIPTION

These are high-speed synchronous, reversible 4-bit binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{\text{CTEN}}$) is low. A high at $\overline{\text{CTEN}}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/\overline{U}) input. When D/\overline{U} is low, the counter counts up and when D/\overline{U} is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs $(\overline{CTEN} \text{ and } D/\overline{U})$ that will modify the operating mode have no affect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

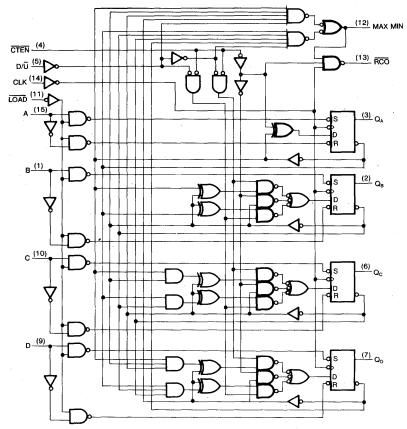
These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The nipple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

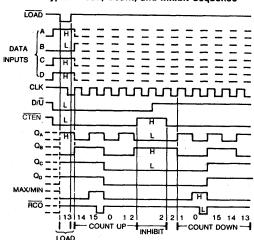
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



Typical Load, Count, and Inhibit Sequence



Sequence:

- (1) Load (preset) to binary thirteen
- (2) Count up to fourteen, fifteen, zero, one, and two
- (3) Inhibit
- (4) Count down to one, zero, fifteen, fourteen, and thirteen

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Gutput Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to $+150$ °C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

11000111111011	aca operating containens
Supply Voltage, \	/cc 4.5V to 5.5V
DC Input & Output	ut Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Tempe	rature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall	Times, t _r , t _f Max 500 ns
Unused inputs m	nust always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	v	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT191

Ch	Characteristic		Conditions [†]	T _a = 25°C V _{CC} = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C OV ±10%	$T_a = -55$ °C	AHCT to +125°C IV ± 10%	Unit	
				Тур	Min	Max	Min	Max		
Maximum Clo	ck Frequency	f _{max}		50	30		25		MHz	
Propagation [Delay,	t _{PLH}		18		30		36	ns	
LOAD to any	Q	tPHL		18		30		36		
Propagation [telH		13	-	21		25	ns	
A,B,C, D to a	ny Q	t _{PHL}		13		21		25		
Propagation [Delay,	tpLH		12		20		24	ns	
CLK to RCO		t _{PHL}		12		20		24		
Propagation [Delay,	t _{PLH}		11		18		22	ns	
CLK to any C)	t _{PHL}	C _L =50pF	11		18		22		
Propagation [Delay,	tpLH		19		31		37	ns	
CLK to MAX/MIN		t _{PHL}		19		31		37		
Propagation I	Delay,	t _{PLH}		19		32		38	ns	
D/Ū to RCO		t _{PHL}		19		32		38		
Propagation [Delay,	tpLH		15		25		30		
D/U to MAX/I	MIN	t _{PHL}		15		25		30		
Propagation [Delay,	t _{PLH}		11		18		22	200	
CTEN to RCC)	t _{PHL}		11		18		22	ns	
Pulse Width	CLK High or Low	t _w		10		17		20	ns	
r disc (vvidil)	LOAD Low	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		12		20		. 25	1113	
	Data before LOAD1			10	17		20			
Setup Time	CTEN before CLK1	t _{su}		10	17		20		ns	
Octup Time	D/Ū before CLK1	'su	-	10	17		20		1113	
	LOAD Inactive before CLK1		,	10	17		20			
	Data after LOAD1			2	4		5			
Hold Time	CTEN after CLK1	th		0	0		O		ns	
	D/U after CLK1			0	0		0			
Input Capacit	ance	CIN		5					pF	
Power Dissipa	ation Capacitance*	C _{PD}		80					рF	

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

KS54AHCT 192 KS74AHCT

Synchronous 4-Bit Up/Down Decade Counters with Dual Clock

FEATURES

- Look-ahead circuit enhances cascaded counters
- · Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- · Asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

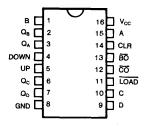
 $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

DESCRIPTION

These are high-speed synchronous reversible 4-bit decade counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-tohigh-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow output (\overline{BO}) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output (\overline{CO}) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and countup inputs, respectively, of the succeeding counter.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

OPERATING MODE	INPUTS									OUTPUTS				
OPERATING MODE	CLR	LOAD	UP	DOWN	A	В	С	D	QA	QB	Qc	QD	CO	BO
	Н	X	Х	L	Х	Х	Х	Х	L	L	L	L	Н	L
reset (clear)	н	X	X	н	X	Х	X	X	L	L	L	L	Н	Н
	L	L	Х	L	L	L	L	L	L	L	L	Ł	Н	L
and the latest	L	L	Х	Н	L	L	L	L	,L	L	L	L	Н	Н
paraiel load	L	L	L	Х	Н	Х	Х	Н	Α	В	С	D	L	Н
	L	L	Н	Х	Н	X	X	Н	Α	В	С	D	Н	Н
count up	L	Н .	1	Н	Х	Х	х	Х		cou	nt up		H*	Н
count down	L	Н	Н	1	Х	Х	Х			count	down		Н	H* *

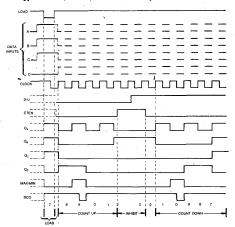
- * CO=Up at terminal count up (HHHH)
- ** BO=Down at terminal count down (LLLL)
 - H = HIGH voltage level

- L = LOW voltage level
- X = don't care
- ↑ = LOW to HIGH clock transition



CLR (14) UP (6) UP (4) DOWN (11) A (15) A (15) B (1) C (10) C (10

Typical load, count, and inhibit sequences



Sequence;

- (1) Load (preset) to BCD seven.
- (2) Count up to eight, mine(maximum) zero, one, and two.
- (3) Inhibit
- (4) Count down to one, zero (minimum), nine, egiht, and seven

NOTE A: Clear overrides load data, and count inputs.

Note B:When count up, count-down input must be high;
when counting down, countup intput must be high.



KS54AHCT **192** KS74AHCT

Synchronous 4-Bit Up/Down Decade Counters with Dual Clock

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	Vcc	4.5V to 5.5V
DC Input & Out	put Voltages*, V _{IN}	Vout OV to Vcc
Operating Temp	erature	
Range	KS74AHCT:	-40°C to +85°C
	KS54AHCT:	-55°C to +125°C
Input Rise & Fal	Times, t _r , t _f	Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т	a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit	
	İ		Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v	
Minimum High-Level Output Voltage	V _{OH}	V _{IN} =V _{IH} or V _{IL} I _O =-20μA I _O =-4mA	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v	
Maximum Low-Level Output Voltage	Vol	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	IN	V _{IN} ≔V _{CC} or GND		±0.1	±1.0	±1.0	μА	
Maximum Quiescent Supply Current	lcc	V _{IN} ≖V _{CC} or GND lout=0µA		8.0	80.0	160.0	μА	
Additional Worst Case Supply Current		per input in V _I =2.4V other Inputs: at V _{CC} or GND lout=0µA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT 192

Characteristic		Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	Ta = -40°C	AHCT C to +85°C DV±10%	T. = -55°C	AHCT to +125°C V± 10%	Unit
				Тур	Min	Max	Min	Max	
Maximum Ck	ock Frequency	f _{max}		50	30		25		MHz
Propagation	Delay,	tpLH		11		18		22	ns
UP to CO	JP to CO			11		18		22	
Propagation	Delay,	tpLH		11		18		22	ns
DOWN to an	y Q .	tpHL	C _L =50pF	11		18		22	
Propagation	Delay,	tPLH		11		19		23	ns
UP or DOWN	N to any Q	tpHL		11		19		23	
Propagation		tPLH		17		29		35	ns
LOAD to any	LOAD to any Q			17		29		35	
Propagation Delay, CLR to any Q		tpLH		10		17		20	ns
	CLR High			6	10	1	15		
	LOAD Low	tw		10	17		20		. ns
Pulse Width	UP or DOWN High or Low			10	17		20		
	Data before LOAD1			10	17	1	29		
	CLR Inactive before UP1 or DOWN1			10	17		20		
Setup Time	LOAD Inactive before UP1 or DOWN1	t _{su}		10	17		20		ns
	UP high before DOWNt			10	17		17		
	Down high before UP1	1		8	15		15		
	Data after LOAD†			0	0		0		
Hold Time UP High after DOWN1 DOWN High after UP1		th		0	0		0		ns
			}	3	8		6		
Input Capaci	tance	CIN		5					pF
Power Dissip	ation Capacitance*	CPD		80					pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

[†] For AC switching test circuits and timing waveforms see section 2.

KS54AHCT **193** KS74AHCT

Synchronous 4-Bit Up/Down Binary Counters with Dual Clock

FEATURES

- · Look-ahead circuitry enhances cascaded counters
- · Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- · Asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- . Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

 $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$

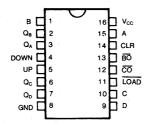
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

DESCRIPTION

These are high-speed synchronous reversible 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-tohigh-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow output (\overline{BO}) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output (\overline{CO}) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and countup inputs, respectively, of the succeeding counter.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

OPERATING MODE		INPUTS									OUTPUTS				
OI ENATING MODE	CLR	LOAD	UP	DOWN	Α	В	С	D	QA	QB	Qc	QD	co	BO	
	Н	Х	Х	L	Х	Х	Х	Х	L	L	L	· L	Н	L	
reset (clear)	Н	X	Х	Н	X	Х	X	Х	L	L	L	L	Н	Н	
	L	L	Х	L	L	L	L	L	L	L	L	L	Н	L	
	L	L	X	Н	L	L	L	L	L	L	L	L	Н	H	
parailel load	L.	L	L	Х	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	
	L	L	н	X	Н	н	Н	Н	Н	Ĥ	Н	H	Н	Н	
count up	L	Н	1	н	Х	Х	Х	Х		cou	nt up		Н*	Н	
count down	L	Ĥ	н.	1	Х	Х	Х			count	down		Н	H**	

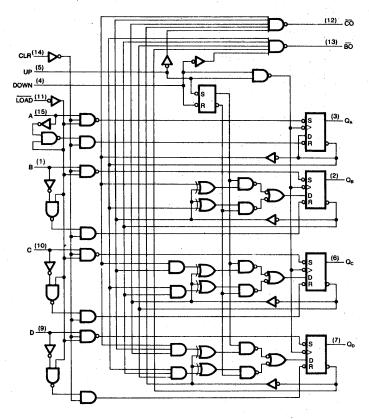
H= HIGH voltage level

↑= LOW-to-HIGH clock transition

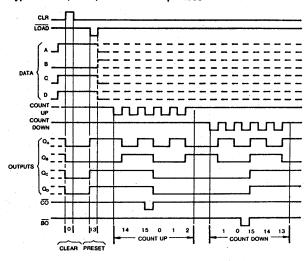
L= LOW voltage lovel X= don't care * \overrightarrow{CO} = UP at terminal count up (HHHH) ** \overrightarrow{BO} = DOWN at terminal count down (LLLL)

SAMSUNG Electronics

LOGIC DIAGRAM



Typical Clear, Load, and Count Sequences



Sequence:

- (1) Clear outputs to zero.
- (2) Load (preset) to binary thirteen.
- (3) Count up to fourteen, fifteen, carry, zero, one and two.
- (4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

Note A: Clear overrides load data, and count inputs.

Note B: When counting up, count-down input must be high; when counting down, counting up input must be high.

Absolute Maximum Ratings*

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

		•		
Supply Voltage, Vcc			4.5V to 5	5V
DC Input & Output V	/oltages*, V _{IN} ,	Vout	0V to \	/cc
Operating Temperatu	ıre			
Range	KS74AHCT:	-40°	°C to +85	°C
	KS54AHCT:	-55°C	to +125	°C
Input Rise & Fall Tim	es, t_r , t_f		Max 500	ns
Unused inputs must voltage level (eithe			propriate lo	gic

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	٧
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f<2 ns), AHCT193

Characteristic		Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	T _a ≈ -40°0	AHCT C to +85°C DV ±10%	Ta = - 55°C	AHCT to +125°C 0V± 10%	Unit	
	•			Тур	Min	Max	Min	Max	L	
Maximum Ck	ock Frequency	f _{max}		50	30		25		MHz	
	Propagation Delay,			11		18		22	ns	
UP to CO		t _{PHL}		11		18		22		
Propagation	Delay,	tPLH		11		18		22	ns	
DOWN to an	y Q	t _{PHL}	C _L =50pF	11		18		22	115	
Propagation	Delay,	tpLH		11		19		23	ns	
UP or DOW	N to any Q	t _{PHL}		11		19	l	23		
Propagation		tpLH		17		29		35	ns	
LOAD to any	LOAD to any Q			17		29		35	113	
Propagation Delay, CLR to any Q		tpLH		10		17		20	ns	
	CLR High			6	10		15			
	LOAD Low	t _w		10	17		20		ns	
Pulse Width	UP or DOWN High or Low			10	17		20			
	Data before LOAD1			10	17		29			
	CLR Inactive before UP1 or DOWN1			10	17		20			
Setup Time	LOAD Inactive before UP1 or DOWN1	t _{su}		10	17		20		ns	
	UP high before DOWN†			10	17		17			
	Down high before UP1	1		8	15		15			
	Data after LOAD↑			0	0		0			
Hold Time	UP High after DOWNt	th		0	0		0		ns	
	DOWN High after UP1]		3	8		6			
Input Capaci	tance	C _{IN}		5					pF	
Power Dissip	pation Capacitance*	C _{PD}		80					pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in.}
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- Parallel-to-Serial, Serial-to-Parallel Conversions
- Left or Right Shifts
- · Parallel Synchronous Loading
- Direct Overriding Clear
- Temporary Data Latching Capability
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

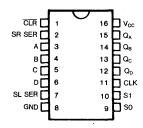
These bidirectional shift registers feature parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation:

- Inhibit clock (temporary data latch/do nothing)
- Shift-right (in the direction QA toward QD)
- Shift-left (in the direction QD toward QA)
- Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, SO and S1, high. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift-right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode control inputs are low.

PIN CONFIGURATION



FUNCTION TABLE

	INPUTS										OUTPUTS			
CLR	MODE		CLK	SERIAL		PARALLEL			QA	QB	Qc	QD		
S1	S1	S0	CLK	LEFT	RIGHT	Α	В	С	D	Q.A	шв	G(
L	Х	Х	X	Х	Х	Х	Χ	Х	Х	L	L	L :	L	
Н	X	Х	L	X	Χ	Х	Х	Х	Х	Q _{A0}	Q_{B0}	Q_{C0}	Q_{D0}	
Н	Н	н	↑ -	X	Χ	а	b	С	d	a	b	C	d	
Н	L	н -	. 1	X	Н	X	Х	Χ	Х	Н	Q_{An}	Q _{Bn}	Q_{Cn}	
Н	L	н	↑	Х	L	Х	Х	Х	Х	L	Q_{An}	Q_{Bn}	Q_{Cn}	
H	Н	L	↑	Н	Χ	Х	Χ	Х	Х	Q _{Bn}	Q_{Cn}	Q _{DN}	Н	
H	Н	L	1	L	Χ	X	Х	Х	Χ		Q _{Cn}		L	
Н	L	L	Χ	X	X	X	Χ	X	Χ	Q _{A0}	Q_{B0}	Q _{C0}	Q_{D0}	

H=high level (steady state)

L=low level (steady state)

X=irrelevant (any input, including transitions)

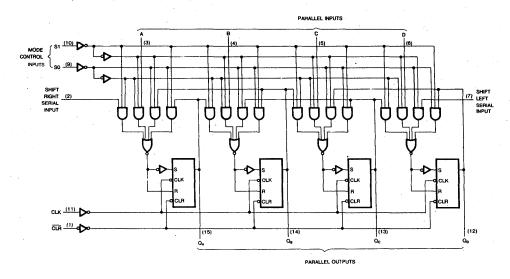
t=transition from low to high level

a,b,c,d=the level of steady-state input at inputs A,B,C, or D, respectively.

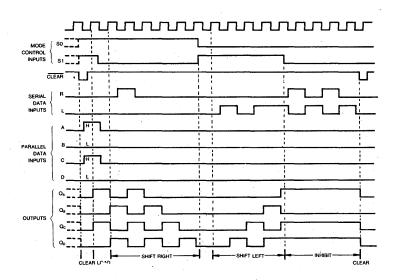
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}=the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}=the level of Q_A, Q_B, Q_C, respectively, before the mostrecent ↑ transition of the clock.

LOGIC DIAGRAM



typical clear, load, right-shift, inhibit, and clear sequences



Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

necommen	ded Operating Conditions
Supply Voltage, \	/ _{CC} 4.5V to 5.5V
DC Input & Output	it Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Tempe	rature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall	Times, t_r , t_f Max 500 ns
Unused inputs m	nust always be tied to an appropriate logic
voltage level (e	ither V _{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	ool Test Conditions		= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit				
			Тур	Guaranteed Limits							
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧				
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧				
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1	v				
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V				
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ				
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ				
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA				

AC ELECTRICAL CHARACTERISTICS (Input tr, tre2 ns), AHCT194

Characteristic		Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	Ta = -40°0	AHCT C to +85°C DV ± 10%	KS54 T _a = -55°C V _{CC} = 5.0	Unit	
				Тур	Min	Max	Min	Max	
Maximum Clo	ck Frequency	f _{max}		60	35		30		MHz
Propagation I	Propagation Delay,			10		17		20	ns
CLK to Q _H		t _{PHL}	C _L =50pF	10		17		20	1113
Propagation Delay, CLR to Q _H		t _{PHL}		11		19		22	ns
Pulse Width	CLR LOW	t _w		10	17		20		ns
ruise Wiutii	CLK High or LOW			10	17		20		
Setup Time, Any Input be	fore CLK1	ts		10	17		20		ns
Hold Time, Data after CLK1		ts	-	-3	0		0		ns
Input Capacitance		Cin		5					pF
Power Dissip	ation Capacitance*	C _{PD}		80					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

FEATURES

- Parallel-to-Serial, Serial-to-Parallel Conversions
- Parallel Synchronous Loading
- . J and K Inputs to First Stage
- Right-shift Only with Complementary Outputs on Last Stage
- Direct Overriding Clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

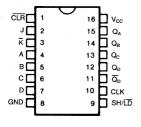
 $I_{OL} = 8$ mA @ $V_{OL} = 0.5$ V

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These 4-bit rigisters feature parallel inputs, parallel outputs, $J-\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

Parallel (broadside) load Shift (in the direction A_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

		INPUTS									OUTPOUTS				
	CLR S	SH/LD	CLK	SEF	SERIAL		PARALLEL			QA	Λ-	Λ.	^	Qp	
L		SH/LD	CLK	j	K	A	В	С	D	GA.	QB	Qc	QD	Œυ	
Γ	L	X	Х	X	X	Х	Х	Х	Х	L	Ļ	L	L	Н	
	Н	L	↑	X	X	а	b	С	d	а	b	С	d	d	
	Н	Н	L	Х	Х	Х	Χ	X	X	Q _{A0}	Q_{B0}	Q_{C0}	Q_{D0}	\overline{Q}_{D0}	
1	Н	Н.	↑	L	Н	Х	Χ	Х	Χ	Q _{A0}	Q _{A0}	QBn	Q _{Cn}	QCn	
	H	н	1	L	L	Х	Х	Х	Χ	L	Q_{An}	Q_{Bn}	Qcn	\overline{Q}_{Cn}	
	н	Н	↑	Н	Н	X	Х	Х	Χ	Н	Q_{An}	Q_{Bn}	Qcn	\bar{Q}_{Cn}	
	Н	Н	1	Н	L	X	Χ	Χ	X	QAn	Q_{An}	\mathbf{Q}_{Bn}	\mathbf{Q}_{Cn}	$\overline{\mathbf{Q}}_{Cn}$	

H=high level (steady state) L=low level (steady state)

X=irrelevant (any input, including transitions)

†=transition from low to high level

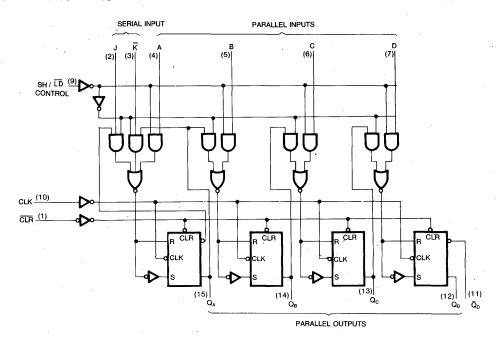
a,b,c,d=the level of steady-state input at A,B,C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}=the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

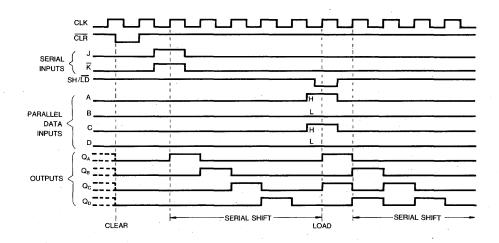
Q_{An}, Q_{Bn}, Q_{Cn}=the level of Q_A, Q_B or Q_C, respectively, before the mostrecent transition of the clock.



LOGIC DIAGRAMS



typical clear, shift, and load sequences



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
Vcc or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

DC Input & Output	C 4.5V to 5.5V Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Tempera	ture
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic
voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	mbol Test Conditions		₃ = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit		
			Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	. V _{IH}			2.0	2.0	2.0	v		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{ mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	v		
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	V		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input tr, ties ns), AHCT195

Cha	Characteristic		Conditions†	T _a = 25°C V _{CC} = 5.0V	T _a = -40°C	AHCT C to +85°C OV ± 10%	KS54. T _a = -55°C V _{CC} = 5.0	Unit	
			* .	Тур	Min	Max	Min	Max	i I
Maximum Clo	ck Frequency	f _{max}		60	35		30		MHz
Propagation I	Delay,	t _{PLH}		10		17		20	ns
CLK to Q _H		t _{PHL}	C _L =50pF	10		17		20	""
Propagation Delay, CLR to Q _H		t _{PHL}		11		19		22	ns
Pulse Width	CLR Low	t _w		10	17		20		ns
T dise Width	CLK High or Low			10	17		20		113
Cotus Time	SH/LD High			10	17		20		
Setup Time before CLK1	Serial or Parallel Data	t _{su}		. 10	17		20		ns
	CLR inactive	}		10	17		20		
Hold Time	SH/LD High			-3	0		0		ns
after CLK1	Serial or Parallel Data			-3	0		0		
Input Capacit	ance	C _{IN}		5		÷			pF
Power Dissip	ation Capacitance*	C _{PD}							рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.

KS54AHCT **210** KS74AHCT

Octal Buffers and Line Drivers with 3-State Outputs

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - IoL =24 mA @ VoL =0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

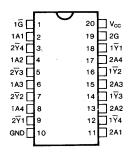
These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The designer has the choice of combinations of inverting non-inverting outputs and symmetrical complementary input control (both active-low, or one active-low, the other active-high).

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

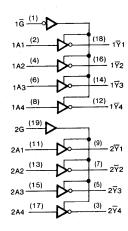
PIN CONFIGURATION



FUNCTION TABLE

In	out	Output
G	Α	. Y
L	٦	Н
L	н	L L
Н	Х	Z

LOGIC DIAGRAM



Octal Buffers and Line Drivers with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I_{IK} (V _I < -0.5V or V _I > V _{CC} +0.5V) \pm 20 mA
DC Output Diode Current, lok
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) + \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

110001111101140	a opolaning committee
Supply Voltage, Vcc	
DC Input & Output V	oltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Temperatu	ire
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall Tim	nes, t _r , t _f Max 500 ns
Unused inputs must voltage level (either	t always be tied to an appropriate logic er V _{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т,	a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit	
			Тур		Guaranteed Lim	its	1	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	, VIL			8.6	0.8	0.8	٧	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6m A$	V _{CC}	V _{CC} -0.1	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	

AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT210

Characteristic	Symbol	Conditions [†]		T _a = 25°C V _{CC} = 5.0V	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	,
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150p		6 9		10 15		12 18	ns
A to \overline{Y}	t _{PHL}	C _L =50pF C _L =150pF		7 11		10 16		12 19	118
Output Enable Time, Enable to \overline{Y}	tpzH	R _L =1kΩ	C _L =50pF C _L =150pF	12 15		20 25		24 30	ns
	tpzL		C _L =50pF C _L =150pF	12 15		20 25		24 30	
Output Disable Time,	t _{PHZ}	$R_L=1k\Omega$		13		18		22	ns
Enable to \overline{Y}	tPLZ	C _L =50pF		13		18		22	113
Input Capacitance	CIN								рF
Output Capacitance	Соит	Output Di	sabled	10					рF
Power Dissipation Capacitance*	C _{PD} *		Output Disabled Output Enabled						pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- Designed specifically for high-speed memory decoders and data transmission systems.
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These devices are designed to be used in highperformance memory-decoding or data-routing applications requiring very short propagation delay times. In highperformance memory systems, these decoders can be used with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

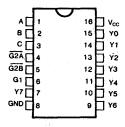
This conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding.

A 24-line decoder can be implemented without external inverters and a 31-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

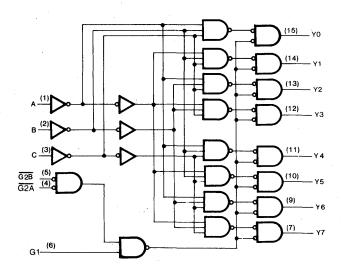


FUNCTION TABLE

En		ele					Out	puts	;			
G1	G2*	С	В	Α	Y0	Y1	Y2	Υ3	Y 4	Y5	Y6	Y7
х	Н	Х	Х	х	L	L	L	L	L	L	L	L
L	×	X	Х	Х	L	L	L	L	L	L	L	L
Н	L	L	L	L	H	L	L	L	L	L	L	L
н	·L	L	L	н	L	Н	L	L	L	L	L	L
Н	L	L	Н	L	L	L	Н	L	L	L	L	L
Н	L	Н	L	L	L	L	L	Н	L	L	L	L
Н	L	Н	L	L	L	L	L	L	Н	L	L	L
Н	L	н	L	н	Ĺ	L	L	L	L	Н	L	L
н	L	Н	Н	L	L	L	L	L	L	L	Н	L
н	L	н	Н	Н	L	L	Ĺ	L	L	L	Ĺ	Н

* G2=G2A+G2B

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , -0.5 V to $+7$ V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) + \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Abaduta Maximum Patings are those values beyond

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

KS54AHCT: -55°C to +125°C
Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	₄=25°C	KS74AHCT T _A = -40°C to +85°C	KS54AHCT T _A = -55°C to +125°C	Unit	
			Тур		Guaranteed Lim	its		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL		,	0.8	0.8	0.8	v	
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v	
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	ν	
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT238

Characteristic	Symbol	Conditions†	T _A = 25°C V _{CC} = 5.0V	KS74AHCT T _A = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _A = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay,	tpLH	C _L =50pF	12		20		24	ns
A, B, C or Y	tpHL		12		20		24	lis
Propagation Delay,	tpLH		10 -		17		20	ns
G1 to any Y	tent		10		17		20	
Propagation Delay,	tpLH		10		17		20	
G2A or G2B to any Y	tpHL	,	10		17		20	ns
Input Capacitance	CIN		5				· .	ъpF
Power Dissipation Capacitance*	C _{PD}		50					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \; V_{CC}{}^2 \; f_{in}$.



[†] For AC switching test circuits and timing waveforms see section 2.

FEATURES

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times in high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory.

This means that the effective system delay introduced by the decoder is negligible.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

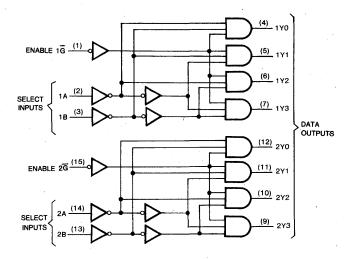
PIN CONFIGURATION

1Ğ [O	40	L
_	1		16	v _∞
1A 🗌	2		15	2G
1B [3		14	2A
1Y0	4		13	2B
1Y1	5		12	<u>2</u> Y0
1Y2	6		11	2Y1
1Y3 🗌	7		10	2Y2
GND	8		9	2Y3
				l

FUNCTION TABLE

. In	puts		Outputs				
Enable	Sel	ect			Vo	va	
Ğ	В	Α.	Y0	Y1	Y2	Y3	
Н	Х	Х	L	L	L	L	
L	L	L	Н	L	L	·L	
L	L	H	L	Н	L	L	
L	Н	L	L	L	· H	L	
L	Н	н	L	L	L	Н	

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) + \pm 20 \text{ mA}$
DC Output Diode Current, I _{OK}
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Patings are those values beyond

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V	cc 4.5V to 5.5V
DC Input & Output	t Voltages*, V _{IN} , V _{OUT} 0V to V _{CC}
Operating Temper	ature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall	Fimes, t_r , t_f Max 500 ns
•	ust always be tied to an appropriate logic ther V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Conditions T _a = 25		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	1
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1	V
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tres ns), AHCT239

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	KS74AHCT $T_a = -40$ °C to $+85$ °C $V_{CC} = 5.0V \pm 10$ %		KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	C _L =50pF	12		20		24	ns
A or B to any Y	t _{PHL}		12		20		24	
Propagation Delay,	tpLH		,	10		17		20
G to any Y	t _{PHL}		10		17		20	115
Input Capacitance	CiN		5					рF
Power Dissipation Capacitance*	C _{PD}		50					рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

KS54AHCT 240/241/244 Octal Buffers and Line Drivers KS74AHCT with 3-State Outputs

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current (loL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The designer has the choice of combinations of inverting/ non-inverting outputs and symmetrical complementary input control (both active-low, or one active-low, the other active-high).

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

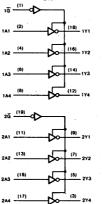
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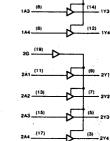
PIN CONFIGURATION

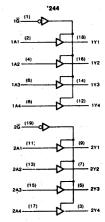
LOGIC DIAGRAMS



*2G for '240 and '244 2G for '241







FUNCTION TABLE

			'241, '244	'240
	Input		Output	Output
G	G	A	Y	Y
Н	L	L	L,	Н
н	. L	н	Н	L
, L	н	×	Z	Z



KS54AHCT **240/241/244**Octal Buffers and Line Drivers KS74AHCT with 3-State Outputs

Absolute Maximum Ratings*

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

necommen	ded Operating Conditions
Supply Voltage,	V _{CC} 4.5V to 5.5V
DC Input & Outp	out Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Temper	erature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall	Times, t_r,t_f Max 500 ns
•	must always be tied to an appropriate logic
voltage level (either V _{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	V _{IN} =V _{IH} or V _{IL} I _O =-20μA I _O =-6mA	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	٧
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٠V
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	- ±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ



[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

KS54AHCT 240/241/244Octal Buffers and Line Drivers KS74AHCT with 3-State Outputs

AC ELECTRICAL CHARACTERISTICS (Input tr., tr<2 ns), AHCT240, AHCT241, AHCT244

Characteristic	Symbol			T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Propagation Delay.	tpLH		C _L =50pF C _L =150pF			10 15		12 18	
A to Y	tpHL	C _L =50pF C _L =150pF		6 9		10 15		12 18	ns
Output Enable Time, Enable to Y	tpzH	Rı=1kΩ	C _L =50pF C _L =150pF	12 15		20 25		24 30	ns
	tpzL	IIL-IK	C _L =50pF C _L =150pF	12 15		20 25		24 30	
Output Disable Time,	t _{PHZ}	R _L =1kΩ		13		18		22	
Enable to Y	tPLZ	C _L =50pF		13		18		22	ns
Input Capacitance	CIN								рF
Output Capacitance	Cout	Output D	Output Disabled			ľ			pF
Power Dissipation Capacitance*	C _{PD}	Output D Output E		5 30					pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

[†] For AC switching test circuits and timing waveforms see section 2.

FEATURES

- 2-Way Asynchronous Communication Between Data Buses
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These four-data line transceivers are designed for asynchronous two-way communications between data buses.

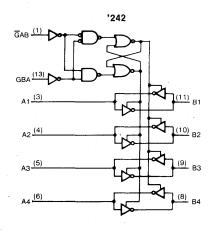
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

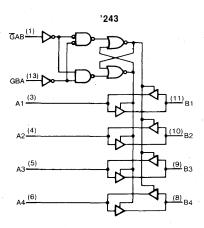
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

INP	UTS	'242		
ĜAB	GBA 242		'243	
L	L	Ā to B	A to B	
Н	Н	B to A	B to A	
Н	اد	Isolation	Isolation	
L	н	Isolation	Isolation	

LOGIC DIAGRAMS







Absolute Maximum Ratings*

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4,5V to 5,5V
DC Input & Output Voltages*, VIN, VOU	T . OV to Vcc
Operating Temperature	71

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±1,0% Unless Otherwise Specified)

Characteristic	Symbol	Symbol Test Conditions		= 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	$ \begin{array}{l} \text{KS54AHCT} \\ \text{T}_{a} = -55^{\circ}\text{C to } +125^{\circ}\text{C} \end{array} $	Unit		
			Тур	1	Guaranteed Limits				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v		
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА		
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND	-	±0.5	±5.0	±10.0	μΑ		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	ΔΙσ	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT242, AHCT243

Characteristic	Symbol	Conditions†		T _a = 25°C V _{CC} = 5.0V	KS74AHCT Ta = -40°C to +85°C Vcc=5.0V±10%		KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit
					Min Max		Min Max		
Propagation Delay, A to B or B to A	telH	C _L =50pF C _L =150pF C _L =50pF C _L =150pF		7 10		11 16		15 21	ns
	t _{PHL}			7 10	·	11 16		15 21	
Output Enable Time GAB to B, GBA to A	tezn	R _L =1kΩ	C _L =50pF C _L =150pF	12 15		20 25		25 21	ns
	t _{PZL}		C _L =50pF C _L =150pF	12 15		20 25		25 21	
Output Disable Time, GAB to B, GBA to A	tenz	R _L =1kΩ C _L =50pF		12		20		25	ns
	tPLZ			12		20		25	
Input Capacitance	CIN			5		41, 11			рF
Output Capacitance	Cout	Output Disabled		10					рF
Power Dissipation Capacitance*(per stage)	C _{PD}	Output Enabled Output Disabled		30 5					pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

[†] For AC switching test circuits and timing waveforms see section 2.

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
 - (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KEZANICT: 4000 Apr. 18500

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

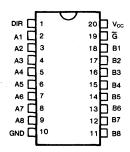
These high-speed octal bus transceivers are designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input (\overline{G}) can be used to disable the device so that the buses are effectively isolated.

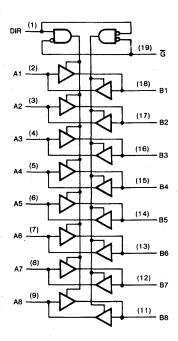
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

Inputs		0
Ğ	DIR	Operation
L	L	Bus B Data to Bus A
L	н	Bus A Data to Bus B
Н	Х	Isolation

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, IIK
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
 Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	V _{CC}	4.5V to 5.5V
DC Input & Out	put Voltages*, V _{IN} ,	Vout OV to Vcc
Operating Temp	perature	
Range	KS74AHCT:	-40°C to +85°C
	KCE AALIOT.	EE00 to 110500

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур	Guaranteed Limits			
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	Voh	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20\mu A$ $I_O = -6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1 3.7	V .
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT245

Characteristic	Symbol	Con	Conditions† Vo		T. = -40°	AHCT C to +85°C 0V±10%	Ta = -55°C	AHCT to +125°C V± 10%	Unit
				Тур	Min	Max	Min	Max	
Propagation Delay,	tpLH	C _L =50pl C _L =150	_=50pF _=150pF			1,1 15		14 20	ns
A to B or B to A	tpHL	C _L =50pf C _L =150p		7 9		10 15		14 20	113
Output Enable Time	tрzн	$R_L=1k\Omega$ $C_L=$ $C_L=$	C _L =50pF C _L =150pF	12 15		20 25		25 31	ns
G to A or B	tpzL		C _L =50pF C _L =150pF	12 17		20 25		25 31	113
Output Disable Time,	tpHZ	$R_L=1k\Omega$		13		18		22	กร
G to A or B	tpLZ	C _L =50pl	=	13		18		22	113
Input Capacitance	CiN			5					pF
Output Capacitance	Cout	Output D	isabled	10					pF
Power Dissipation Capacitance*	C _{PD}	G=V _{CC} G=GND	(per stage)	5 30					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in.}

[†] For AC switching test circuits and timing waveforms see section 2.

- Three-State Version of '151
- Three-State Outputs Interface Directly with System Bus
- Performs Parallel-to-Serial Conversion
- Complementary Outputs Provide True and Inverted
 Data
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
 (IoL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

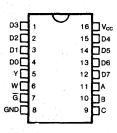
These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature strobe-controlled-complementary three-state outputs.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe (\overline{G}) . The outputs are disabled when \overline{G} is high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

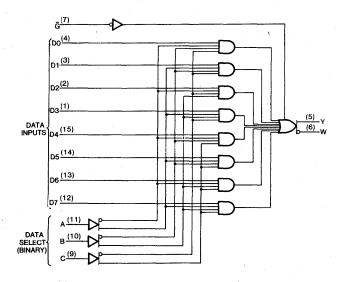
PIN CONFIGURATION



FUNCTION TABLE

	1	INP	OUT	PUTS	
SELECT		ЭТ	STROBE	Υ	w
С	В	A	Ğ		
Х	X	Χ	Н	Z	Z
L.	L	L	L	DO	Ďΰ
L	L	Н	L	D1	D1
Ľ	Н	L	L	- D2	D2
L	Ĥ	н	L	DЗ	Ď3
Н	L	L	L	D4	D4
Н	L	Ή	L	D5	D5
H	H.	L	L	D6	D6
Н	Н	н	L	D7	D7

LOGIC DIAGRAM



1-of-8 Data Selectors/Multiplexers with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to V_{CC}
Operating Temperature *	

Range KS74AHCT: -40° C to $+85^{\circ}$ C KS54AHCT: -55° C to $+125^{\circ}$ C Input Rise & Fall Times, t_r , t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either Vcc or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Characteristic Symbol		T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	t _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	loc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT251

Characteristic	Symbol	Symbol Condition		T _a = 25°C V _{CC} = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C 0V±10%	Ta = -55°C	AHCT to +125°C V ± 10%	Unit	
1			,	Тур	Min	Max	Min	Max		
Propagation Delay,	tpLH	C _L =50pf C _L =150p		13 16		21 26		25 31		
A, B or C to Y	tpHL	C _L =50pl C _L =150pl		13 16		21 26		25 31	ns	
Propagation Delay,	telh	C _L =50pl		15 18		24 29		27 33		
A, B or C to W	t _{PHL}	C _L =50pl		15 18	-	24 29		27 33	ns	
Propagation Delay,	tpLH	C _L =50pl		9 12		15 20		18 24		
Any D to Y	tpHL	C _L =50pl		9 12	-	15 20		18 24	ns	
Propagation Delay.	tpLH	C _L =50pl C _L =150pl		8 11		15 20		18 24		
Any D to W	t _{PHL}	C _L =50pl		8 11		15 20		18 24	ns	
Output Enable Time.	tezh	Rı=1kΩ	C _L =50pF C _L =150pF	11 14		18 23		22 28	ns	
Ğ to Y or W	tpzL	nt- ika	C _L =50pF C _L =150pF	11 14		18 23		22 28	113	
Output Disable Time,	tpHZ	$R_L=1k\Omega$	•	13		18		22	ns	
G to Y or W	tPLZ	C _L =50pl	=	13		18		22		
Input Capacitance	CiN			5					pF	
Output Capacitance	Соит	Output D	isabled	10					рF	
Power Dissipation Capacitance*	C _{PD}							-	pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

- Three-State Version of '153
- . Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
 (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

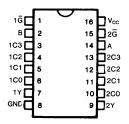
Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe (\overline{G}) . The output is disabled when its strobe is high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



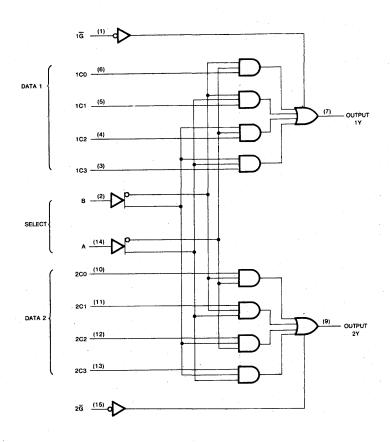
FUNCTION TABLE

SEL	SELECT		TA	INPL	ITS	OUTPUT CONTROL	ОИТРИТ
В	A	CO	C1	C2	СЗ	G	Υ
Х	Х	Х	Х	Х	Х	Н	Z
L	L	L	Х	Х	X	L	L
L	L	н	Х	Χ	Х	L	Н
L	Н	Х	L	Χ	Х	L	L
L	Н	X	Н	Χ	Х	L	Н
Н	L	Х	Χ	L	Х	L	L
Н	L	Х	Χ	٠Н	Χ	L	Н
Н	Н	Х	Х	Х	L	, L	L
Н	Н -	X	X	Χ	H	L	Н

Address inputs A and B are common to both sections.

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LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IoK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to $+150$ °C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating ConditionsSupply Voltage, Vcc 4.5V to 5.5V

DC Input & Output V	oltages*, VIN, VOUT OV to VCC
Operating Temperatu	re
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall Tim	es, t _r , t _f Max 500 ns
Unused inputs must voltage level (eithe	always be tied to an appropriate logic

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	1 1
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20\mu A$ $I_O = -6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} =0.1	V _{CC} -0.1	٧
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	. V
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_{r.} t_f≤2 ns), AHCT253

Characteristic Symbol		Conditions [†]		T _a = 25°C V _{CC} = 5.0V	_		KS54. T _a = ~55°C V _{CC} = 5.0	to +125°C	Unit
			Тур		Min	Max	Min	Max	
Propagation Delay	t _{PLH}		C _L =50pF C _L =150pF			21 26		25 31	ns
A or B to any Y	t _{PHL}	C _L =50pF C _L =150p		13 16		21 26		25 31	113
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150p		9 12		13 20		18 34	ns
Data (any C) to any Y	t _{PHL}	C _L =50pF C _L =150pF		9 12		13 20		18 34	
Output Enable Time	t _{PZH}	D1k0	C _L =50pF C _L =150pF	10 13		16 21		19 35	ns
G to Y	t _{PZL}	U[- 1K11	C _L =50pF C _L =150pF	10 13		16 21		19 35	115
Output Disable Time,	t _{PHZ}	$R_L = 1k\Omega$		13		18		22	ns
G to Y	tpiz	C _L =50pF	:	13		18		22	113
Input Capacitance	Cin			5 .					pF
Output Capacitance	Cout	Output D	isabled	10					pF
Power Dissipation Capacitance*	C _{PD}			i e					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.



KS54AHCT **257/258** Quad 2-Line to 1-Line Data Selector/ KS74AHCT **257/258** Quad 2-Line to 1-Line Data Selector/

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- . Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
 (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

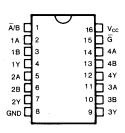
DESCRIPTION

The '257 and '258 multiplex signals from for-bit data sources to four-output data lines in bus organized systems. The data presented at the outputs is non-inverted for the '257, and inverted for the '258.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

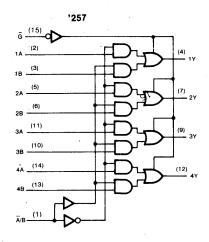
PIN CONFIGURATION

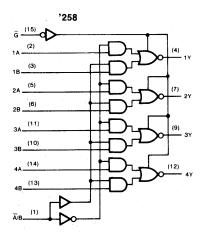


FUNCTION TABLE

	Outp	out Y				
Output Control	Select	Data		'257	'258	
Ğ	Ã/B	Α	В			
Н	Х	Х	Х	Z .	Z	
L	L	L	Х	L	Н	
L	L	н	Х	Н	L	
L	н	X	L	L	. н`	
L	H.	Х	н	Н	L	

LOGIC DIAGRAMS







KS54AHCT 257/258 Quad 2-Line to 1-Line Data Selector/ KS74AHCT 257/258 Quad 2-Line to 1-Line Data Selector/ Multiplexers with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
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^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	Vcc 4.5V to	5.5V
DC Input & Outp	out Voltages*, V _{IN} , V _{OUT} OV t	o Vcc
Operating Temper	erature	
Range	KS74AHCT: -40°C to +	85°C
	KS54AHCT: -55°C to +1	25°C
Input Rise & Fall	Times, tr, tr Max 5	00 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} =0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	V _{IN} =V _{IH} or V _{IL} I _O =20μA I _O =12mA I _O =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	·V
Maximum Input Current	IIN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



化 数据信息成绩

KS54AHCT 257/258 Quad 2-Line to 1-Line Data Selector/ KS74AHCT 257/258 Quad 2-Line to 1-Line Data Selector/ Multiplexers with 3-State Outputs

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT257

Characteristic	Symbol	Conditions†		T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit
angaran na ang marang at t				Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	C _L =50pf C _L =150pf		7 10		12 17		14 · · · 20	
A or B to any Y	t _{PHL}		C _L =50pF C _L =150pF			12 17		14 20	ns
Propagation Delay,	tpLH	C _L =50pF C _L =150pF		12 15		20 25		24 30	ns
Ā/B to any Y	t _{PHL}	C _L =50pl C _L =150pl		12 15		20 25		24 30) 11 0
Output Enable Time,	tpzH	$R_i = 1 k\Omega$	C _L =50pF C _L =150pF	13 16		18 23		22 28	ns
G to any Y	t _{PZL}		C _L =50pF C _L =150pF	13 16		18 23		22 28	
Output Disable Time,	t _{PHZ}	$R_L = 1 k\Omega$		12		15		22	- ns
G to any Y	tpLZ	C _L =50pF		12		15		22	110
Input Capacitance	CiN	1.		5				1. (1.5%/15%)	ρF
Output Capacitance	Cout	Output Disabled		10	,				pF.
Power Dissipation Capacitance*	C _{PD}							/cdsge	ρF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

AC ELECTRICAL CHARACTERISTICS (Input tr, tr 42 ns), AHCT258

Characteristic	Symbol	Conditions [†]		T _a = 25°C V _{CC} = 5.0V	Ta = -40°	IAHCT C to +85°C 0V±10%	$T_a = -55$ °C	IAHCT C to +125°C OV ± 10%	Unit
				Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	C _L =50pl C _L =150pl		6 9		8 13	-	141 19	ns
A or B to any Y	tpHL		C _L =50pF C _L =150pF			8 13		14 19	113
Propagation Delay,	tpLH	C _L =50pF C _{L=150pF}		14 17		23 28		28 34	ns
A/B to any Y	t _{PHL}	C _L =50pl C _L =150pl		14 17		23 28		28 34	
Output Enable Time,	t _{PZH}	$R_1 = 1 k\Omega$	C _L =50pF C _L =150pF	11 14		18 23		22 28	ns
G to any Y	t _{PZL}	11,2	C _L =50pF C _L =150pF	11 14		18 23	·	22 28	
Output Disable Time,	t _{PHZ}	R _L =1kΩ		13		18		22	ns
G to any Y	t _{PLZ}	C _L =50pf	:	13		18		22	
Input Capacitance	C _{IN}			5					рF
Output Capacitance	Cout	Output Disabled		10					ρF
Power Dissipation Capacitance*	C _{PD}								рF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin-

[†] For AC switching test circuits and timing waveforms see section 2.



[†] For AC switching test circuits and timing waveforms see section 2.

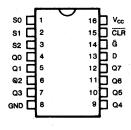
- 8-Bit parallel-out storage register performs serial-toparallel conversion with storage
- · Asynchronous parallel clear
- Active high decoder
- Enable/Disable input simplifies expansion
- Expandable for N-bit applications
- · Four distinct functional modes
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '259 is a high-speed addressable latch designed for general purpose storage applications in digital systems. It can be used for implementing working registers, serial-holding registers and active-high decoders or demultiplexers.

The '259 has four distinct modes of operation that are selected via the clear ($\overline{\text{CLR}}$) and enable ($\overline{\text{G}}$) inputs: 1) addressable latch; 2) memory; 3) active-high eight-channel demultiplexer; and 4) clear.

In the addressable latch mode, data on the data input (D) is written into the addressed latch. In this mode, data will be written into the addressed latch with all non-addressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous state and are unaffected by the data of address inputs.

In the demultiplexing mode, addressed outputs will follow the state of the D input and all other outputs will remain low.

In the clear mode, all outputs are low and unaffected by the address and data inputs.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

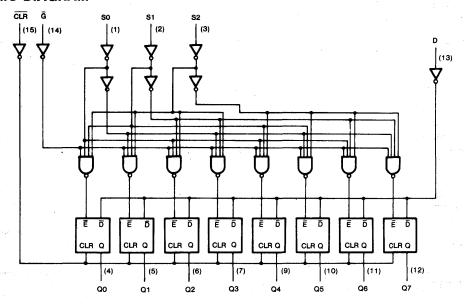
Inpu	ts	Output of Addressed	Each Other	Function
CLR	Ğ	Latch	Output	Function
Н	L	D	Qio	Addressable Latch
н	Н	Qio	Qio	Memory
L	L	D	L	8-Line Demultiplexer
L	Н	. L	L	Clear

D = the level at the data input. Q_{i0} = the level of Q_{i0} (i = Q, 1, ... 7, as appropriate) before the indicated steady-state input conditions were established.

LATCH SELECTION TABLE

Sel	ect Inp	Latch	
S2	S1	S0	Addressed
L	L	L	0
L	, L	н	1
L	Н	L	2
L	- H	н	3
Н	L	L	4
H	L	Н	5
Н	н	L	6
Н	н	Н	7

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Hange V _{CC} ,0.5V to +/V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vcc) [.] <i>.</i>	4.5V to 5.5V			
DC Input & Output	Voltages*, V _{IN} ,	Vout OV to Vcc			
Operating Temperat	ure	30 - 11 1 C 13			
Range	KS74AHCT:	-40°C to +85°C			
	KS54AHCT:	-55°C to +125°C			
Input Rise & Fall Tir	nes, t _r , t _f	Max 500 ns			
Unused inputs must always be tied to an appropriate logic					

voltage level (either V_{CC} or GND)





DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT $T_{a} = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit				
			Тур	Typ Guaranteed Limits							
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0%	V				
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧				
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	٧				
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧				
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ				
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ				
Additional Worst Case Supply Current	Δlcc	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA				

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT259

Characteristic		Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	KS74AHCT $T_a = -40$ °C to +85°C $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Тур	Min	Max	Min	Max	
Propagation Delay CLR to any Q		t _{PHL}		9		15		. 18	ns
Propagation Delay,		tplH		12		19		23	ns
Data to any Q		t _{PHL}		12		19		23	113
Propagation Delay,	Propagation Delay, Address to any Q		CL=50pF	13		22		27	ns
Address to any Q				13		22		27	
Propagation Delay,		tpLH		12		20		24	ns
G to any Q		t _{PHL}		12		20		24	113
Pulse Width	CLR Low	t _w		6	10		10		ns
T dise Width	G Low] 'w		9	15		20	,	113
Setup Time Data or Address before	ore Gt	t _{su}		10	15		20		ns
Hold Time, Data or Address before Gt		t _h		-3	0		0		ns
Input Capacitance		CIN		5					рF
Power Dissipation Ca	apacitance*	C _{PD}		80					pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.



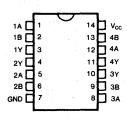
[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

inp	uts	Output
A	В	Υ
L	L	Н
L	Н	L
H	L	L
Н	Н	Н

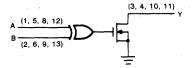
DESCRIPTION

These devices contain four independent exclusive-NOR gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



Quad Exclusive-NOR Gates with Open-Drain Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I _{OK}
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage, Vo	oc 4.5V to 5.5V
DC Input & Output	t Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Tempera	ature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall T	imes, t _r , t _f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT266

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V Typ	$T_a = -40^{\circ}$	AHCT C to +85°C 0V ± 10%	$KS54$ $T_a = -55^{\circ}C$ $V_{CC} = 5.0$	Unit	
				Min	Max	Min	Max	1
Propagation Delay	t _{PLH}	$C_L=50pF$ $R_L=1k\Omega$	19		29		35	200
- ropagation Bolay	tPHL		11		18		22	ns
Input Capacitance	CIN		5					рF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15					pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

[†] For AC switching test circuits and timing waveforms see section 2.



[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

- Eight positive-edge-triggered D-type flip-flops with single-rail outputs
- . Buffered common clock and asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 24mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

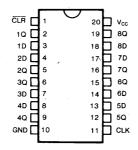
These devices are high-speed octal registers. They consist of eight positive-edge-triggered D-type flip-flops with individual D inputs and Q outputs. All flip flops are loaded and cleared simultaneously by the common buffered clock (CLK) and clear (CLR) inputs.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

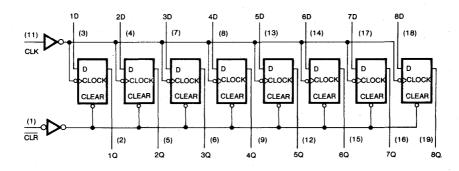
PIN CONFIGURATION



FUNCTION TABLE

(Each Flip-Flop) Inputs Output CLR CLK Q D L Х X L Н Н Н Н L Ĺ Q_0 Н

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic S	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_{O}=-20\mu\text{A}$ $I_{O}=-6\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =12mA I _O =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_i≤2 ns), AHCT273

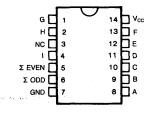
Characteristic		Symbol	ymbol Conditions†	T _a = 25°C V _{CC} = 5.0V	Ta = -40°0	AHCT C to +85°C OV ± 10%	KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Maximum Clo	ck Frequency	f _{max}	C _L =50pF	50	35		30		MHz
Propagation Delay, CLK to any Q		t _{PLH}	C _L =50pF C _L =150pF	13 13		18.5 20		19 34	ns
		t _{PHL}	C _L =50pF C _L =150pF	13 13		17.5 20		19 34	113
Propagation Delay, CLR to any Q		t _{PHL}	C _L =50pF C _L =150pF	13 14		18.5 23		22 28	ns
Pulse Width	CLR Low	tw	-	8	14		17		ns
i dise width	CLK High or Low	· •		8	14		17		115
Setup Time	Data	tsu		6	10		10		ns
before CLK1	Clear inactive State	, vsu		9	15		15		113
Hold time, Data after CLK1		th		-3	0		0		ns
Input Capacitance		CIN		5					pF.
Power Dissipa	tion Capacitance*	C _{PD}	(per package)	150					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

- Generates Odd or Even Parity for Nine Data Lines
- Cascadable for N-Bits Parity
- Can be used to Upgrade Existing Systems using MSI Parity Circuits
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $(I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5 \text{V})$ for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74HCTLS: -40°C to +85°C
 - KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These universal, nine-bit parity generators/checkers feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

The devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker, Although the '280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the '280 to be substituted for the '180 in existing designs to produce an identical function even if the devices are mixed with existing '180's.

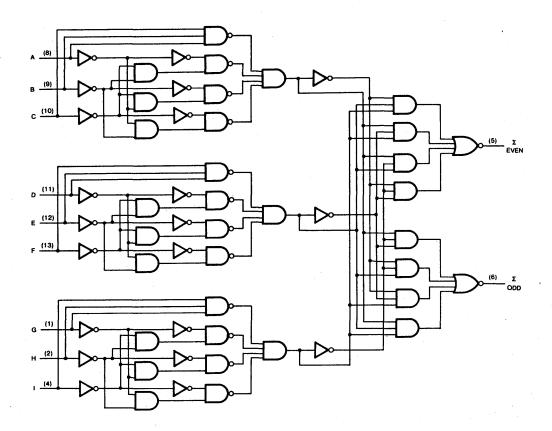
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTF	UTS
THRU I THAT ARE HIGH	Σ EVEN	Σ ODD
0,2,4,6,8	Н	L
1,3,5,7,9	L	Н

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, $P_{d}{}^{\dagger}$ 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic
voltage level (either V_{CC} or GND)



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT Ta = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0µA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT280

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	Ta = - 40°	IAHCT C to +85°C 0V±10%	KS54 T _a = -55°C V _{CC} = 5.0	Unit	
		-	Тур	Min	Max	Min	Max	
Propagation Delay,	tpLH	C _L =50pF C _L =150pF	12 15		21 25		24 30	ns
Any input to Σ Even	t _{PHL}	C _L =50pF C _L =150pF	12 15		21 25		24 30	
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	13 16		22 27		26 32	ns
Any input to Σ Odd	t _{PHL}	C _L =50pF C _L =150pF	13 16		22 27		26 32	
Input Capacitance	CIN		5					рF
Power Dissipation Capacitance*	C _{PD}						1	pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.

- Multiplexed I/O ports provides improved bit density
- Four modes of operation: hold (store), shift right, shift left, and load data
- Operates with outputs enabled or at high impedance
- · Can be cascaded for N-bit word lengths
- · Direct overriding clear
- Application:

Stacked or push-down registers, buffer storage, and accumulator registers

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · 3-State outputs with drive current
- ($I_{OL} = 24 \text{ mA}$ @ $V_{OL} = 0.5 \text{V}$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

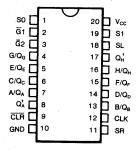
These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when $\overline{\text{CLR}}$ is low. Pulling either of the output controls, $\overline{\text{G1}}$ or $\overline{\text{G2}}$, high disables the outputs but this has no effect on clearing, shifting, or storage of data

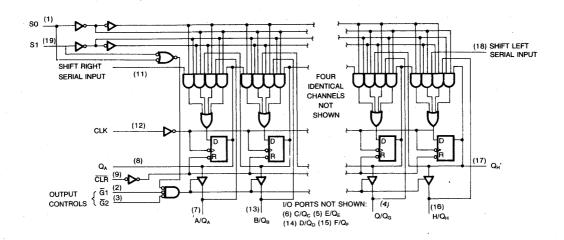
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

		Inputs							I/O Ports							Outputs		
Mode	CLR	S1	S0		put ntrol G2	CLK	SL	SR	A/Q _A	B/Q _B	C/Qc	D/Q _D	E/Q _E	F/Q _F	G/Q _G	H/Q _H	Q _A '	Q _H '
Clear	L L	X L H	L X H	L L X	L L X	×	X X X	X X X	L L X	L L X	L L X	L L X	L L X	L L X	L L X	L L X	L L	L L
Hold	Н	L	L X	L L	L L	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}		Q _{H0}
Shift Right	H	L	H	L L	L L	† †	X X	H L	H	Q _{An} Q _{An}	Q _{Bn} Q _{Bn}	Q _{Cn}	Q _{Dn} Q _{Dn}	Q _{En}	Q _{Fn} Q _{Fn}	Q _{Gn}	H	Q _{Gn} Q _{Gn}
Shift Left	H	H	L L	L	L	† †	H	X	Q _{Bn} Q _{Bn}	Q _{Cn} Q _{Cn}	Q _{Dn} Q _{Dn}	Q _{En} Q _{En}	Q _{Fn} Q _{Fn}	Q _{Gn} Q _{Gn}	Q _{Hn} Q _{Hn}	H	Q _{Bn} Q _{Bn}	H
Load	Н	Н	Н	Х	Χ	↑	Х	X	а	b	С	d	е	· f	g	h	а	h

When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) + 0.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, P_d^{\dagger} 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	bol Test Conditions		= 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T _a = -55°C to +125°C	Unit		
			Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V		
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	, v		
Minimum High		$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ Q'_A and Q'_H outputs:	V _{CC}	V _{CC} -0.1	V _{CC} -0.1	V _{CC} -0.1			
Minimum High- Level Output VOH Voltage		$I_O = -4mA$ Q_A thru Q_H outputs: $I_O = -6mA$	4.2	3.98	3.84	3.7			
Miximum		V _{IN} =V _{IH} or V _{IL} I _O =20μA Q' _A and Q' _H outputs:	0.	0.1	0.1	0.1			
Low-Level Output Voltage	VOL	I _O =4mA I _O =8mA Q _A thru Q _H outputs:		0.26 0.39	0.33 0.5	. 0.4	٧		
		I _O =12mA I _O =24mA		0.26 0.39	0.33 0.5	0.4			
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum 3-State Leakage Current	loz	Output Enable = V _{IN} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA		



8-Bit Universal Shift/Storage Registers with 3-State Outputs

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT299

Characteristic		Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	T. = -40°0	AHCT C to +85°C DV±10%	KS54 T _a = -55°C V _{CC} = 5.0		Unit
				Тур	Min Max		Min Max		floor
Maximum Clo	ock Frequency	f _{max}		50	30		25		MHz
Propagation	Delay.	tpLH		10		17		20	ns
CLK to Q'A		tPHL	C _L =50pF	10		17		20	
Propagation CLR to Q'A o		t _{PHL}		13		22		26	ns
D	D-1	t _{PLH}	C _L =50pF C _L =150pF	10 13		16 21		19 25	-
Propagation Delay, CLK to Q _A thru Q _H		t _{PHL}	C _L =50pF C _L =150pF	10 13		16 21		19 25	ns
Propagation Delay, CLR to Q _A thru Q _H		t _{PHL}	C _L =50pF C _L =150pF	13 16		22 27		26 31	ns
Output Enable Time,		tezn	$C_L=50pF$ $C_L=150pF$	11 14		19 24		23 29	ns
G1, G2, to 0	Q _A thru Q _H	t _{PZL}	C _L =50pF C _L =150pF	11 14		19 24		23 29	
Output Disab		t _{PHZ}	$R_L = 1 k\Omega$	11		18		22	ns ns
G 1, G 2 to Q	A thru QH	t _{PLZ}	C _L =50pF	11		18		22	
Pulse Width	CLK High or Low	t _w		9	15		20		
	CLR Low	.,,		5	8		10		
	S0 and S1			12	20		10		
Setup time	High-Level Inputs	t _{su}		8	13		15		ns
before CLK1	Low-Level Inputs	-30		8	13		15]
	CLR Inactive			8	13		15		
Hold Time after CLK1 All Inputs		th		0	0		0		ns
				0					113
Input Capacit	tance	CiN		5					pF
Output Capa	citance	Соит	Output Disabled	10					pF
Power Dissip	ation Capacitance*	C _{PD}				-			pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

- Multiplexed inputs/outputs provide improved bit density
- Sign extend function
- · Direct overriding clear
- . 3 state outputs drive bus lines directly
- Function pin-out, speed and drive compatibility with 54/74 ALS logic family
- Low power consumption characteristic of CMOS
- · High drive current output
- ($I_{OL} = 24mA$ @ $V_{OL} = 0.5V$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices.
- Wide Operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature range:

KS74AHCT: -40°C to +85°

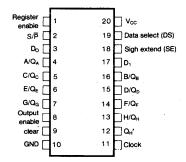
KS54AHCT: -55°C to +125°

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

DESCRIPTION

These 8 bit Shift registers have multiplexed input/output data ports to accomplish full 8-bit data handling in a single 20-pin package. Serial data may enter the shift-right register through either D_0 or D_1 input as selected by the data select pin. A serial output is also provided. Synchronous parallel loading is achieved by taking the register enable and the S/\bar{P} inputs low. This places the three-state input/output ports in the data input mode. Data are entered on the low-to-high clock transition. The data extend function repeats the sign in the Q_A flip flop during shifting. An overriding clear input clears the internal register when taken low whether the outputs are enabled or off. The output enable does not affect synchronous operation of the register.

PIN CONFIGURATION



FUNCTION TABLE

OPERATION				INPUT	ı							
	Clear	Register enable	SIP	Sign extend	Data select	Output enable	Clock	A/Q _A	B/Q _B	C/Qc -	·· H/Q _H	Output Q _H
Clear	L L	H X	X H	×	X	L L	×	L L	L L	L L	L .	L
Hold	Н	Н	х	×	Х	L	Х	Q _{AO}	Q _{BO}	Qco	Q _{HO}	Q _{HO}
Shift Right	Н ; Н	L L	H	H H	H	L L	†	D _O D _i	Q _{An} Q _{An}	Q _{Bn} Q _{Bn}	Q _{Gn} Q _{GN}	Q _{Gn}
Sign Extend	Н	L	Н	L	Х	·L	1	Q _{An}	QAn	Q _{Bn}	Q _{Gn}	Q _{Gn}
Load	Н	L	L.	Х	X	Х	1	а	b	С	h	h '

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state: however, sequential operation or clearing of the register is not affected. If both the register enable input and the S/\bar{P} input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

H= high level (steady state)

L= low level (steady state)

X= irrelevant (any inputs, including transitions)

↑ = transition from low to high level

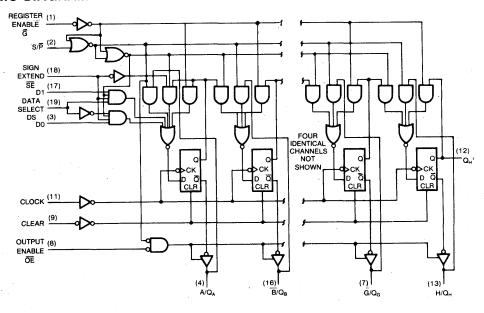
QAo...QHo= the level of QA through QH, respectively, before the indicated steady-state conditions were established.

Q_{An...Q_{Hn}= 'the level of Q_A through Q_H, respectively, before the most recent † transition of the clock.}

Do, D1 = the level of steady-state inputs at inputs Do and D1 respectively

a...h= the level of steady-state inputs at input A through H respectively.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V DC Input Diode Current, I _{IK}
$(V_{l} < -0.5V \text{ or } V_{l} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I_{OK} (Vo < -0.5V or Vo > Vcc +0.5V) ± 20 mA
Continuous Output Current Per Pin, Io $(-0.5V < V_O < V_{CC} + 0.5V) + 235 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins
Power Dissipation Per Package, Pd† 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, Vout	OV to Vcc
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т	= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} −0.1 3.98	V _{CC} −0.1. 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0µA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	Δlcc	per input in V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9		mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tr<2 ns), AHCT322

Characteristic		Symbol	Conditions†	T _A = 25°C V _{CC} = 5.0V	TA = -40°	AHCT C to +85°C OV±10%	KS54A T _A = - 55°C V _{CC} = 5.0V	Unit		
				Тур	Min	Max	Min	Max		
Maximum Clock Frequency	,	f _{max}		50	30		25		MHz	
Maximum Propagation		tpHL		12		20		24	ns	
Delay, Clock to Q _H		tpLH		12		20	w	24	1113	
Maximum Propagation Delay, Clear to Q _H '		tpHL	C _L =50pF	13		21		25	ns	
Maximum Propagation		tpHL		12		20		24	ns	
Delay, Clock to QA-QH		tpLH		12		20		24	""	
Propagation Delay Clear to Q _A -Q _H		t _{PHL}		13		21	r sale	25	ns	
Output Enable Time		tpzH	$R_L = 1k\Omega$	13		21		25	ns	
Output Enable Time		tpzL	C _L =50pF	13		21		25		
Output Disable Time		tpHZ	OL-SOPI	11		18		21	ns	
Cutput Disable Time		teLZ	•	11		18		21		
Clock Pulse Width	High	tw		7	12		15		ns	
Clock Pulse Wigth	Low	tw	1	7	12		15		'''	
Clear Pulse Width Low		tw		7	12		15		ns	
Data Set up Time		ts	-	8	15		20		ns	
Select Set up Time		ts		8	15		20		113	
Data Hold Time		th		-3	0		0	0	ns	
Select Hold Time		th		5	8		10			
Recovery Time		trec		10	17		20		ns	
Maximum Input Capacitance	Cin		5					pF		
Power Dissipation Capacita	nce	C _{PD}	-	100					pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f + I_{CC} V_{CC}.

[†] For AC switching test circuits and timing waveforms see section 2.

- Inverting Version of '153
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · High drive current outputs
- (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

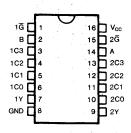
DESCRIPTION

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs $(\overline{\mathbf{G}})$ are provided for each of the two four-line sections.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

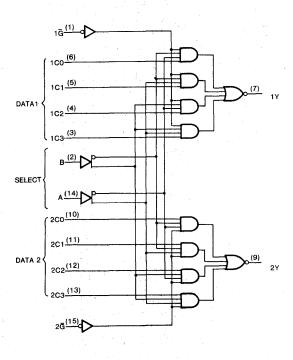


FUNCTION TABLE

SELECT INPUTS		DA	ΤA	INPL	ITS	STROBE	ОИТРИТ		
В	A	CO	C1.	C2	СЗ	Ğ	Y		
Х	Х	Х	Х	Х	Х	Н	Н		
L	·L	L	X	Χ	Х	L	H		
L	L	Н	Х	X	Х	L	L		
L	H	Х	L	X	X.	L	H		
Ļ	Н	Х	Н	Х	X	L	L		
Н	L	Х	Х	L	Х	L	Н		
, Н	L	X	Х	H	X	L	L		
Н	н	Х	Х	X	L	. L .	Н		
Н	Н	Х	X	X	Н	L	L		

Select inputs A and B are common to both sections.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, IIK
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Meximum Detines are these values have

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	V_{CC} 4.5V to 5.5V
DC Input & Out	out Voltages*, VIN, VOUT OV to VCC
Operating Temp	erature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic
voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	. V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =12mA I _O =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0µA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT352

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	KS74AHCT Ta = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	14 17		23 28		28 34	ns
A or B to Y	t _{PHL}	C _L =50pF C _L =150pF	14 17		23 28		28 34	115
Propagation Delay.	t _{PLH}	C _L =50pF C _L =150pF	11 14		18 23		21 27	ns
Data (Any C) to Y	t _{PHL}	C _L =50pF C _L =150pF	11 14		18 23		21 27	113
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	12 15		20 25		24 30	ns
G to Y	t _{PHL}	C _L =50pF C _L =150pF	12 15		20 25		24 30	
Input Capacitance	Cin		5					pF
Power Dissipation Capacitance*	CPD							рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in.}

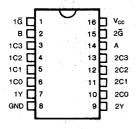
[†] For AC switching test circuits and timing waveforms see section 2.

- Inverting Version of '253
- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74AHCT: -40°C to +85°C

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

						* .	
	ELECT IPUTS DATA INP		INPU	ITS	OUTPUT CONTROL	ОИТРИТ	
В	A	CO	C1	C2	СЗ	Ğ	Y
Х	X	X	Х	Х	Х	Н	Z
L·	L	L	×	X	X	L	н
L	L	н	Х	Χ	X	L	L
L	Н	Х	L	Χ	X	L	н
L	Н	X	Н	· X	X	L	L
Н	L	X	X	L	Х	L .	Н
Н	L	Х	Х	Н	X	L	L
H	H	Х	Х	X	L	L	н
Н	H	X	Х	X	Н	L	L

Select inputs A and B are common to both sections.

DESCRIPTION

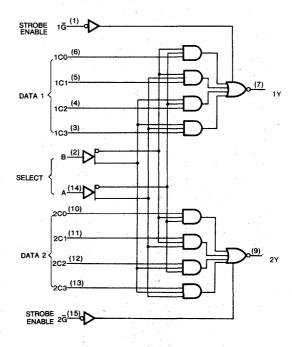
Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs (G) are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe $(\overline{\mathbf{G}})$. The output is disabled when its strobe is high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



KS54AHCT **353**

Dual 1-of-4 Data Selectors/Multiplexers with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IoK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

Storage Temperature Range, T_{stg} ... -65°C to +150°C Power Dissipation Per Package, P_d† 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, V_{IN}, V_{OUT} . . . OV to V_{CC} Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	rmbol Test Conditions		a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
~			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage		$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	l lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT353

Characteristic	Symbol	Symbol Conditions†		T _a = 25°C V _{CC} = 5.0V	KS74AHCT T ₀ = -40°C to +85°C V _{CC} =5.0V±10%		KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	C _L =50pf C _L =150p		14 17		24 29	•	28 34	ns
A or B to any Y	tpHL	C _L =50pF C _L =150pF		14 17		24 29		28 34	113
Propagation Delay, Data (Any C) to Any Y	tpLH	C _L =50pF C _L =150pF C _L =50pF C _L =150pF		10 13		18 23		21 27	ns
	t _{PHL}			10 13		18 23		21 27	
Output Enable Time, G to Y	t _{PZH}	RL=1kΩ	C _L =50pF C _L =150pF	10 13		16 21		19 25	ns
	tpzL		C _L =50pF C _L =150pF	10 13		16 21		19 25	
Output Disable Time,	t _{PHZ}	R _L =1kΩ		10		18		22	ns
Ğ to Y	tpLZ	C _L =50pF		10		18		22	1113
Input Capacitance	CIN			5					рF
Output Capacitance	Cout	Output D	isabled	10					pF
Power Dissipation Capacitance*	C _{PD}								pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
 (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

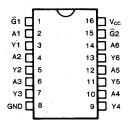
These high-speed Hex bus drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus oriented receivers and transmitters.

The '365 and '366 have two output enables ($\overline{G}1$ and $\overline{G}2$) NOR'ed together to control all six gates. The '367 and '368 have two output enables which are configured so that one enable ($\overline{G}1$) controls four gates and the other ($\overline{G}2$) controls the remaining two gates. The '366 and '368 have inverting data paths. The '365 and '367 have noninverting data paths.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLES

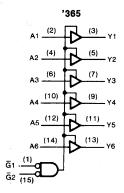
'365 and '366

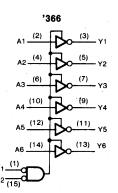
lr	puts	3	Y Outputs			
Ğ1	G2	A	'365	'366		
L	L	L	L	Н		
L	L	Н	Н	L		
Н	X	Х	z	Z		
X	Н	Х	Z	Z		

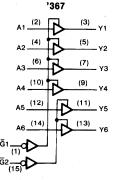
'367 and '368

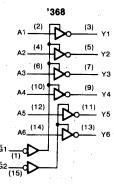
Inputs	;	Y Outputs			
G1 & G2	A	'367	'368		
L	L	L	Н		
L	ļΗ	Н	L		
Н	X	Z	Z		

LOGIC DIAGRAMS









Absolute Maximum Ratings*

Supply voltage Hange V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	Vcc	4.	5V to 5.5V
DC Input & Outp	out Voltages*, V _{IN} ,	Vout	OV to V _{CC}
Operating Temper	erature		
Range	KS74AHCT:	-40°C	to +85°C

KS54AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic
voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	onditions T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
	l		Тур	Typ Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V _{IL}	4 · · · ·		0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	٧
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc .	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

KS54AHCT 365/366 KS74AHCT 367/368

Hex Bus-Drivers with 3-State Outputs

AHCT365, AHCT366, AC ELECTRICAL CHARACTERISTICS (Input t, t,≤2 ns), AHCT367, AHCT368

Characteristic	Symbol			l Conditions†		T _a = 25°C V _{CC} = 5.0V	T _a = - 40°0	AHCT C to +85°C DV±10%	Ta = -55°C	AHCT to +125°C IV ± 10%	Unit
				Тур	Min	Max	Min	Max			
Propagation Delay,		C _L = 50pF C _L =150pF		8 11		14 19		17 33			
A to Y,	t _{PHL}	C _L = 50pF C _L =150pF		8 11		14 19		17 33	ns		
Output Enable Time, G to Y	tpzH	R _L =1kΩ	C _L = 50pF C _L =150pF	14 17		23 28		28 34	ns		
	t _{PZL}		C _L = 50pF C _L =150pF	14 17		23 28		28 34			
Output Disable Time,	t _{PHZ}	$R_L = 1k\Omega$		15		20		22	ns		
G to Y	tpLZ	C _L =50pF		15		20		22	,,,,		
Input Capacitance	CiN								pF		
Output Capacitance	Соит	Output Disabled		10					pF		
Power Dissipation Capacitance* (per driver)	C _{PD}	G=V _{CC} G=GND		5					pF		

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

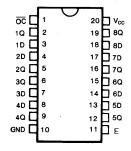
[†] For AC switching test circuits and timing waveforms see section 2.

- 8 latches in a single package
- · Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
 (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '373 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (E) is high, the Q outputs follow the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (\overline{OC}) which places the outputs at a high-impedance state when it is taken high. The \overline{OC} signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

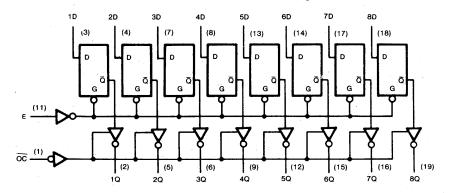
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(Each Latch)

	Inputs					
ос	E	D	Q			
L	Н	н	Н			
L	н	L	L			
L	L '	Х	Q_0			
н	X	x	Z			

LOGIC DIAGRAM



Absolute Maximum Ratings*

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Decommen	lued Operating Conditions
Supply Voltage,	V _{CC} 4.5V to 5.5V
DC Input & Out	out Voltages*, V _{IN} , V _{OUT} 0V to V _{CC}
Operating Temp	erature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fal	I Times, t _r , t _f Max 500 ns.
Unused inputs	must always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	Т	_a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit	
			Тур		Guaranteed Lim	its		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	· V	
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V _{ОН}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC}	V _{CC} -0.1	V _{CC} −0.1 3.84	V _{CC} -0.1	v	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	ΔΙ _{CC}	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	

Octal D-Type Transparent Latches with 3-State Outputs

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT373

Characteristic	Symbol	l Conditions†		T _a = 25°C V _{CC} = 5.0V	Ta = -40°0	AHCT C to +85°C DV ± 10%	T. = -55°C	AHCT to +125°C V ± 10%	Unit
				Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	C _L = 50p C _L =150p		11 14		16 19		19 23	ns
D to Q	t _{PHL}	C _L = 50p C _L =150p		11 14		16 19		19 23	115
Propagation Delay,	t _{PLH}	C _L = 50p C _L =150p		14 17		23 28		27 33	200
E to Q	t _{PHL}	C _L = 50pF C _I =150pF		14 17		23 28		27 33	ns
Output Enable Time, OC to any Q	tpzH	5 410	C _L = 50pF C _L =150pF	12 15		20 25		24 30	ns
	tpZL	$R_L = 1 k\Omega$	C _L = 50pF C _L =150pF	12 15	•	20 25		24 30	
Output Disable Time,	t _{PHZ}	$R_L = 1 k\Omega$		13		18	-	22	ns
OC to any Q	tpLZ	C _L =50pF		13		18		22	1,10
Pulse Width, E High	tw			9	15		18		ns
Setup Time, D before E↓	tsu			6	10		10		ns
Hold Time, D after E↓	t _h			3	5		7		ns
Input Capacitance	CIN			5					рF
Output Capacitance	Cout	Output Disabled		10					pΕ
Power Dissipation Capacitance* (per latch)	C _{PD}	OC=V _{CC} OC=GND		5 30			-		pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f_{in}$



[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

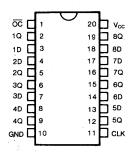
KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

• Package options include "small outling"

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



LOGIC DIAGRAM

DESCRIPTION

The '374 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

The flip-flops are edge-triggered on the positive transition of the clock. The Q outputs are set to the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal (\overline{OC}) which places the outputs at a high-impedance state when it is taken high. The OC signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

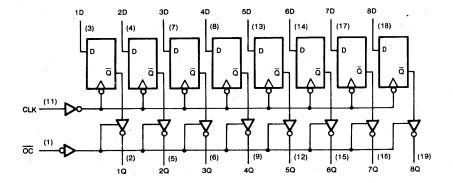
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(Each Flip-Flop)

ı	nputs	Output	
ОC	CLK	D	Q
L	1	٠Η	Н
. L	1	L	L
L	L	Χ	Q_0
Н	Χ	Χ	Z



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

d Operating Conditions
4.5V to 5.5V
/oltages*, V_{IN} , V_{OUT} OV to V_{CC}
ire
KS74AHCT: -40°C to +85°C
KS54AHCT: -55°C to +125°C
ies, t_r , t_f Max 500 ns
always be tied to an appropriate logic $P(C)$

Characteristic	Symbol	Test Conditions	T	a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	VoH	V _{IN} =V _{IH} or V _{IL} I _O =-20μA I _O =-6mA	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} = 0.1 3.7	V
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	IIN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT374

Characteristic	Symbol	Symbol Conditions $T_a = 25$ °C $V_{CC} = 5.0V$				KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	
				Min	Max	Min	Max		
Maximum Operating Frequency	f _{max}	C _L = 50p	C _L = 50pF		35		30		MHz
Propagation Delay,	t _{PLH}		C _L = 50pF C _L =150pF			15 19		17 23	ns
CLK to any Q	t _{PHL}	C _L = 50pF C _t = 150pF		10 13		15 19		17 23	IIS
Output Enable Time, OC to any Q	t _{PZH}		C _L = 50pF C _L =150pF	11		18 23		22 28	ns
	tpzL		$C_L = 50pF$ $C_L = 150pF$	11 14		18 23		22 28	
Output Disable Time,	t _{PHZ}	$R_L=1k\Omega$		13		18		22	ns
OC to any Q	t _{PLZ}	C _L =50pF		13		18		22	
Pulse Width, CLK High or Low	tw			7	15		18		ns
Setup Time, D before CLK†	t _{su}	-		9	14		13		ns
Hold Time, D after CLKt	th			-3	0		٥		ns
Input Capacitance	CIN								pF
Output Capacitance	Соит	Output Dis	sabled	10					рF
Power Dissipation Capacitance*		ÖC=V _{CC} ÖC=GND	(per stage)	5 30					

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

- Can be used for implementing
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

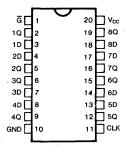
 $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '377 contains eight positive-edge-triggered D-type flip-flops with an enable ihput. This part is similar to '273 but features a latched clock enable (\overline{G}) instead of a common clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if $\overline{\bf G}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitioins at the $\overline{\bf G}$ input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

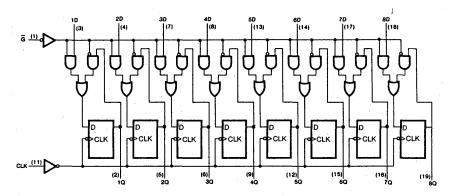
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(EACH FLIP-FLOP)

	INPUT	OUTPUT	
G	CLK	DATA	Q
Н	Х	X	Qo
L	†	Н	н
L	1	L.	L
Х	L	X	Q_0

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I _{OK}
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	V _{CC} 4.5V to 5.5V
DC Input & Outp	ut Voltages*, VIN, VOUT OV to VCC
Operating Temps	erature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall	Times, $t_r,\;t_f$ Max 500 ns
	nust always be tied to an appropriate logic
voltane level (e	either Voc or GND)

Characteristic	Symbol	Test Conditions	т	a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	<
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	· V
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT377

Characteristic		Characteristic Symbol Conditions		T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} =5.0V±10%		KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit
				Тур	Min	Max	Min 30	Max	
Maximum Clock Frequency		f _{max}		50	35				MHz
Propagation Delay, CLK to any Q		t _{PLH}	_	10		16		19	
		t _{PHL}	C _L =50pF	10		16		19	ns
Pulse	G Low	tw		8	14		17		
Width	CLK High or Low	ıw.		8	14		17		ns
Setup time	Data			6	10		10		
before CLKf	G High or Low	t _{su.}		9	15		15		ns
Hold Time, Data after CLK1		th		-3	0		O		ns
Input Capacitance		CIN		5					pF
Power Dissipati	on Capacitance*	C _{PD}	per package	50			-		pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in.}$ † For AC switching test circuits and timing waveforms see section 2.

- Individual clock for A and B flip-flops provide dual +2 and +5 counters
- · Direct clear for each 4-bit counter
- Significant improvement in system density through reduced counter package count.
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

 $(l_{OL} = 8 \text{ mA } @ V_{OL} = 0.5V)$

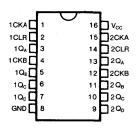
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These devices incorporate dual divide-by-two and divide-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiple of 2 and/or 5 up to divide-by-100. When connected as a biquinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square ware) at the final outpur stage. The '390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-tow circuit can be used to provide symmetry (a square wave) at the final outpur stage. The '390 has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground

FUNCTION TABLES

BCD COUNT SEQUENCE (EACH COUNTER) (See Note A)

COUNT		OUT	PUT	
	QD	Qc	QB	QA
0	L	L	L	L
1 -	L	L	L	Н
2	L	L	Н	L
. 3	L	L	Н	Н
4	L	Н	L	L
5	L	Н	L	Н
6	L	Н	Н	L
7	L	Н	Н	Н
8	Н	L	L	L
9	.H	L	L	Н

BIQUINARY (5-2) (EACH COUNTER) (See Note B)

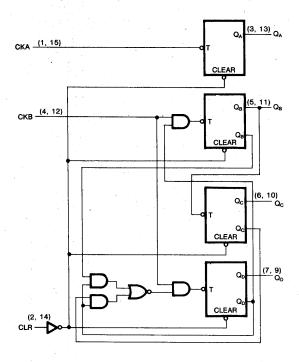
COUNT	OUTPUT					
COUNT	Q_D	Qc	Q_B	QA		
0	L	L	L	L		
1	L	L	L	Н		
2	L	L	Н	L		
. 3	L	L	Н	Н		
4	L	Н	L	L		
5	Н	L	L	L		
6	Н	L	L	H		
7	Н	L	Н	L		
8	Н	L	H	Н		
9	H.	Н	L	L		

NOTES A. Output QA is connected to input CKB for BCD count.

B. Output Q_D is connected to input CKA for biquinary count.



LOGIC DIAGRAM



Absolute Maximum Ratings*

Absolute maximum hatings
Supply Voltage Range V _{CC} , -0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V	cc 4.5V to 5.5V
	it Voltages*, V _{IN} , V _{OUT} 0V to V _{CC}
Operating Temper	ature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall	Times, t _r , t _f Max 500 ns
Unused inputs m	ust always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т,	a = 25°C	KS74AHCT T ₈ = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	1
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	o	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	l _{IN} .	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current		per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT390

Characteristic		Symbol			$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10^{\circ}$		KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Тур	Min	Max	Min	Max	
Propagation Delay, CKA to Q _A or CKB to	Q _B	f _{max}		50	30		25		MHz
Propagation Delay,		t _{PLH}		9	-	15		18	ns
CKA to Q _A		t _{PHL}		9		15		18	ns
Propagation Delay,		t _{PLH}		24		40		48	ns
CKA to Q _C		t _{PHL}		24		40		48	ns
Propagation Delay,	Propagation Delay, CKB to Q _B		C _L =50pF	10		17		21	ns
CKB to Q _B				10		17		21	ns
Propagation Delay,		t _{PLH}	-	16		27		33	ns
CKB to Q _C		t _{PHL}		16		27		33	ns
Propagation Delay,		tpLH		10		17		21	ns
CKB to Q _D		t _{PHL}		10		17		21	ns
Propagation Delay, CLR to Any Q		tenL		19		30		35	ns
Pulse Width	CKA or CKB High or Low	tw		. 7	12		15		ns
ruise wiutii	CLR High			7	12		15		
Minimum Setup Time, CLR inactive before CKA or CKB		tsu		5	8		10		ns
Input Capacitance		CIN		- 5					pF
Power Dissipation Car	ocitance	C _{PD}							pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.

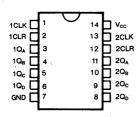


- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 IoL = 8 mA @ Vol. = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



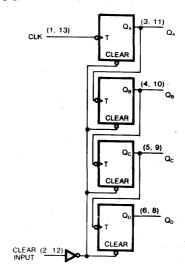
DESCRIPTION

The '393 consists of two independent 4-bit binary counters each with its own clear and clock inputs. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. parallel outputs from each counter stage provided any submultiple of the input count frequency for system timing signals.

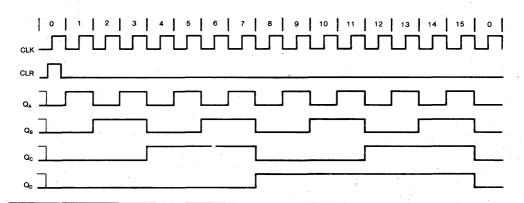
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



LOGIC TIMING WAVEFORMS



4

Absolute Maximum Ratings*

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74AHCT:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, $t_{r}, \, t_{f}$ Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	Ta	=25°C	KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	1
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	ViL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1	V _{CC} −0.1 3.84	V _{CC} -0.1	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0.	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT393

Characteristic		Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	T _a = -40°	IAHCT C to +85°C 0V±10%	$T_a = -55^{\circ}$	NAHCT C to +125°C OV ± 10%	Unit
				Тур	Min	Max	Min	Max	
Maximum Clo	ock Frequency	f _{max}		50	30		25		MHz
Propagation I	Delay,	tpLH		14		22		26	ns
A to Q _A		t _{PHL}		14		22		26	113
Propagation I	Delay,	tpLH		18		27		32	ns
A to Q _B		t _{PHL}	C ₁ = 50pF	18		27		` 32	115
Propagation I	Dealy,	tpLH		20		33		40	ns
A to Q _C		tpHL		20		33		40	
Propagation I	Delay,	t _{PLH}		26		40		48	
A to Q _D		tpHL		26		40		48	
Propagation Dealy, CLR to any Q		t _{PHL}		15		25		30	ns
Pulse	A Input High or Low			7	12		15		ns
Width	CLR High	t _w		7	12		15		115
Setup Time, CLR Inactive before A		t _{su}		5	8		10		ns
Input Capacitance		CiN		5					рF
Power Dissip	ation Capacitance*	C _{PD}	(per counter)	40					рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

 $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5V$

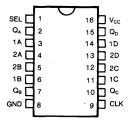
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

Package options include "small outline" packages.
 (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These are high-speed quad 2-port registers. They are the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A common select input (SEL) selects between two 4-bit input ports. The selected data is transferred to the output register on the low-to-high transition of the clock input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

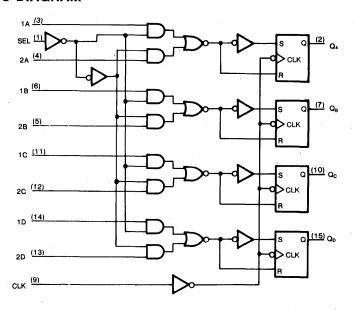
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

	Inputs					
SEL	Port 1	Port 2	Q			
ı	ı	Х	L			
1	h	Х	Н			
h	Х	1 1	L .			
h	×	h	Н			

- I = Low Voltage Level one setup time prior to the low-to-high clock transition
- h = High Voltage Level one setup time prior to the low-to-high clock transition

LOGIC DIAGRAM



Absolute Maximum Ratings*

rate in a man in a ma
Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_{I}<-0.5V \text{ or } V_{I}>V_{CC}$ +0.5V) $\pm 20 \text{ mA}$
DC Output Diode Current, I _{OK}
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.	5V to	5.5V
DC Input & Output Voltages*, V _{IN} , V _{OUT}			
Operating Temperature			

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т,	a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	1
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, ti≤2 ns), AHCT399

Characteristic		Symbol Conditions [†]	T _a = 25°C V _{CC} = 5.0V	KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit	
				Тур	Min	Max	Min	Max	
Propagation Delay,		tplH	C _L =50pF	12		19		23	ns
CLK to Q		t _{PHL}	OL-30bi	12		19		23	110
Pulse Width, CLK High or Low		tw		6	10		15		ns
Time Data		t _{su}		6	10		15		ns
	Word Select			6	10		15		
Hold Time, Data at	fter CLK1	th		-3	0		0		ns
Input Capacitance		C _{IN}		5					рF
Power Dissipation	Capacitance*	C _{PD}							pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin-

[†] For AC switching test circuits and timing waveforms see section 2.

Dual Retriggerable Monostable Multivibrator with Clear

FEATURES

- Simple pulse width formula tw = 0.45RC
- DC triggered from active HIGH or active Low inputs
- Retriggerable for very long output pulses up to 100% duty cycle
- . Overriding clear terminates output pulse
- Schmitt trigger A & B inputs allow infinite rise and fall times on these inputs
- Functions, pin-out, speed and drive compativility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- - $I_{OL} = 8mA @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range; 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

The '423 contains dual retriggerable monostable multivibrators with output pulsewidth control by two methods. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}). The external resistor and capacitor are normally connected as shown timing component.

Once triggered, the basic output pulse width may be extended by retriggering the gated active Low-going edge input (Ai) or the active High-going edge input (Bi). By repeating this process, the output pulse period (nQ=HIGH, $n\overline{Q}=LOW$) can be made as long as desired.

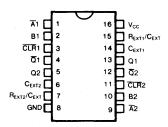
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques.

The output pulse equation is simply;

 $t_W=0.45\times(R_{EXT})$ (C_{EXT})

Where t_w is in seconds. R is in ohm, and C is in fards. All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLE

	Inputs	Out	puts	
CLR	Ā	В	Q	Q
L	Х	Х	L	Н
X	Н	X	L	н
X	Х	L	L	Н.
· H	L	↑	77	7.1
н	↓	Н	T	ᇺ

H= HIGH voltage level

L= LOW voltage level

X= don't care

↑= LOW to HIGH transition

↓= HIGH to LOW transition

□ one LOW level output pulse

Absolute Maximum Ratings*

Supply Voltage Range $V_{CC},\0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
(V _I <-0.5V or V _I >V _{CC} +0.5V) ±20 mA
DC Output Diode Current, IOk
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous OUtput Current Per Pin, Io
(-0.5V <v<sub>0<v<sub>CC+0.5V) ±35 mA</v<sub></v<sub>
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} -65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package(N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

DC Input & Out	, V_{CC}
Operating Temp	perature
Range	KS74AHCT: -40°C to +85°C
J	KS54AHCT: -55°C to +125°C
Input Rise & Fa	all Times, tr, tr Max 500 ns
Unused inputs	s must always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T	_a = 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			8.0	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{ОН}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr. tr 2 ns), AHCT 423

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} =5.0V±10%		KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	tpLH		18		33		40	ns
Ā, B to Q, Q	tpHL	C _L =50pF	18		33		40	
Propagation Delay	tpLH	C _{ext} =0,	16		27		33	ns
CLR to Q, Q	t _{PHL}	$R_{ext}=5k\Omega$	16		27		33	,,,3
Output Pulse Width 1	twq1		116		207		209	ns
Output Pulse Width 2	t _{WQ2}	C_L =50pF C_{ext} =10nF R_{ext} =10k Ω	45	38	52	38	52	μs
Trigger Pulse Width	tw	C _L =50pF A _i =LOW	5		- 16		20	ns
Trigger Pulse Width	t _w	C _L =50pF B _i =High	5		16		20	ns
Clear Pulse Width	tw	C _L =50pF CLR _i =LOW	6		16		20	ns
External Timing Resistance	Rext			2	100	2	100	kΩ
External Timing Capacitance	Cext				no restri	ction		
Input Capacitance	Cin		5					pF
Power Dissipation Capacitance	C _{PD}							pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

Application Information

The basic output pulse width is determined by the value of external capacitance and timing resistance. For output pulse widths greater than 100µs or external capacitance greater than 10nF the following equation should be used.

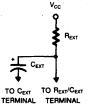
$$t_w = k \cdot R_{ext} \cdot C_{ext}$$

Where

 t_W is in μ s K is the multiplying factor and is approximately 0.45 for Cext is in nF Rest is in $k\Omega$

For best results, system ground should be applied to the C_{ext} terminal. These devices do not require a switching diode in series with the R_{ext}/C_{ext} terminal (as required by some other monostable multivibrators)

TIMING COMPONENT



[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

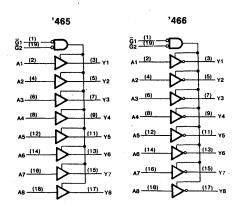
KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS

'467 and '468 '465 and '466 1Ğ∏ Ğ1□ □ v_{cc} 20 20 V_{CC} ∏ Ḡ2 1A1 19 🗖 2G 19 A1. 2 18 2A4 Y1 🗌 3 18 BA 🔲 1Y1 [___ Y8 2Y4 A2 [17 17 1A2 [Y2 5 16 1Y2 [16 2A3 __ A7 АЗ [6 15 1A3 6 15 2Y3 □ Y7 1Y3 🗖 γз 🗌 7 14 ☐ A6 7 14 2A2 A4 🗆 8 13 Y6 184 🗖 8 13 🛮 2Y2 Y4 □ 1Y4 🗆 12 A5 12 2A1 2Y1 GND | GND 🗌 10 Y5

LOGIC DIAGRAMS



DESCRIPTION

These high-speed octal buffers and drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and busoriented receivers and transmitters. The designer has the choice of inverting/ noninverting outputs and various types of output controls.

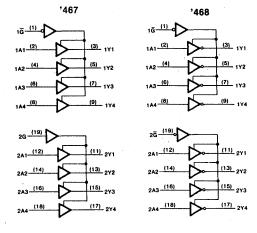
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

	Input	Output		
G,	G ₂	Α	'465	'466
L	L	L	L	Н
L	L	Н	H	L
Н	X	Х	Z	Z
Х	н	Χ.	Z	z

	Input	Output			
G	G	Α	'467	'468	
Н	L	L	L	Н	
Н	L	Н	н Н	L	
L	Н	X	Z	Z 2	



KS54AHCT 400/400 KS74AHCT 467/468

Octal Buffers and Line Drivers with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} , -0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Patings are those values havened

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability

† Power Dissipatión temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
		=	Тур	Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} -0.1	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _i =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



KS54AHCT 405/400 KS74AHCT 467/468

Octal Buffers and Line Drivers with 3-State Outputs

AC ELECTRICAL CHARACTERISTICS (Input tr., tr<2 ns), AHCT465, AHCT468

Parameter	Symbol	oi Conditions		T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		54AHCT T _a = +55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
'				Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}		C _L =50pF C _L =150pF			12 17		14 20	
A to Y	t _{PHL}	C _L =50pF C _L =150pF		7 10		12 17		14 20	ns
Output Enable Time, Enable to Y	t _{PZH}	R _L =1kΩ	C _L =50pF C _L =150pF	12 15		20 25 .		24 30	ns
	t _{PZL}		C _L =50pF C _L =150pF	12 15		20 25		24 30	
Output Disable Time,	tpHZ	$R_L=1k\Omega$	13		18		22		
Enable to Y	t _{PLZ}	C _L =50pF		13		18		22	ns
Input Capacitance	CIN			5					рF
Output Capacitance	Cout	Output D	isabled	10					ρF
Power Dissipation Capacitance* (per stage)	C _{PD}	Output D Output E		5 30					рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in.} For AC switching test circuits and timing waveforms see section 2.



- · Compares two 8-bit words
- '518, '520 and 522 have 20kΩ pull-up Resistors on Q Inputs

ТҮРЕ	INPUT PULL-UP RESISTOR	OUTPUT FUNCTION AND CONFIGURATION
'518	Yes	P=Q Open-Drain
'519	No	P=Q Open-Drain
'520	Yes	P=Q Totem-Pole
'521	No	P≕Q Totem-Pole
'522	Yes	P=Q Open-Drain

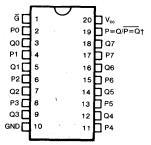
† '521 is identical to '688

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
 - (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



† P=Q for '518 and '519; P=Q for '520, '521, '522.

DESCRIPTION

These identity comparators perform comparisons on two eight-bit binary or BCD words. The '518 and '519 provide P=Q outputs, while the '520, 521, and '522 provide $\overline{P}=\overline{Q}$ outputs. The '518, '519, and '522 have open-drain outputs. The '518, '520, and '522 feature 20-k Ω inputs for analog or switch data.

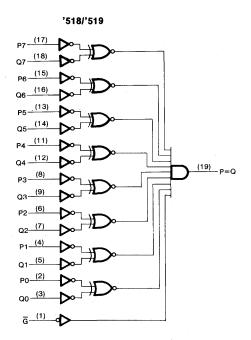
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

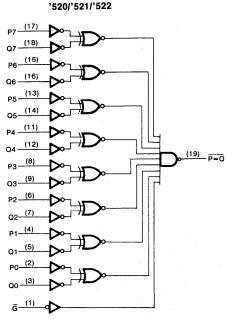
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

IN	PUTS	OUTPUTS		
DATA P, Q	ENABLE Ĝ	P=Q	P≃Q	
P=Q	L	Н	L	
P>Q	L	L	Н	
P <q< td=""><td>L</td><td>L</td><td>Н</td></q<>	L	L	Н	
×	Н	L	Н	

LOGIC DIAGRAMS





Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, lok
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	Vcc	4.5V to 5.5V
		Vout OV to Vcc
Operating Tempe	erature	
D	PC74AUCT	-40°C to +85°C

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns Unused inputs must always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

Parameter	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _A = -40°C to +85°C	54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limit	•	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage (Totem-pole Outputs)	Voh	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu$ A $I_O=-6$ mA	V _{CC} 4.2	V _{CC} −0.1 3.93	V _{CC} -0.1 3.84	V _{CC} -0.1	V
Maximum Low-Level Output Voltage (All Outputs)	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current, ('518, '520 and '522 Q input)		V _{CC} =Max V _{IN} =2.7V V _{IN} =0.4V		-0.2 -0.6	-0.2 -0.6	-0.2 -0.6	mA
Maximum Input Current (All other Inputs)	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current (Open-Drain Outputs)	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent	lcc	For '518, '520 and '522: V _{IN} =GND (Q0-Q7) V _{IN} =V _{CC} or GND (all other inputs)		3.5	3.5	3.5	mA
Supply Current		For '519 and '521: V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

KS54AHCT **518/519** KS74AHCT **520/521/522**

8-Bit Identity Comparators

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT518, AHCT519

Characteristic	Symbol	Conditions	54/74ACHT T _a = 25°C V _{CC} = 5V	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5V \pm 10^{\circ}$		54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
			Typical	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	20 23		30 35		35 41	
P or Q to P=Q	t _{PHL}	C _L =50pF C _L =150pF	15 18		25 30		30 36	ns
Propagation Delay,	t _{PLH}	C=50pF C _L =150pF	16 19		23 28		27 33	ns
G to P=Q	t _{PHL}	C _L =50pF C _L =150pF	11 14		18 23		22 28	
Input Capacitance	CiN		5					pF
Power Dissipation Capacitance*	C _{PD}							рF

AC ELECTRICAL CHARACTERISTICS (Input tr. ti≤2 ns), AHCT520, AHCT521

Characteristic	Symbol	Conditions	54/74ACHT T _A = 25°C V _{CC} = 5V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5V ± 10%		54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
•			Typical	Min	Max	Min	Max	
Propagation Delay, P or Q to P=Q	t _{PLH}	C _L =50pF C _L =150pF	12 15		19 24		23 29	ns
	t _{PHL}	C _L =50pF C _L =150pF	12 15		19 24		23 29	
Propagation Delay,	t _{PLH}	C=50pF C _L =150pF	11 14		17 22		20 26	
G to P=Q	tpHL	C _L =50pF C _L =150pF	11 14		17 22		20 26	ns
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	CPD							. pF

AC ELECTRICAL CHARACTERISTICS (Input tr, tr < 2 ns), AHC522

Characteristic	Symbol	Conditions	54/74ACHT T _A = 25°C V _{CC} = 5V	KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10^{\circ}$				Unit
			Typical	Min.	Max	Min	Max	ĺ
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	19 22		28 33		33 39	ns
P or Q to P=Q	t _{PHL}	C _L =50pF C _L =150pF	14 17	: .	23 28		28 34	
Propagation Delay,	tpĿH	C=50pF C _L =150pF	16 19		23 28		27 33	ns
G to P=Q	t _{PHL}	C _L =50pF C _L =150pF	11 14		18 27		22 33	
Input Capacitance	CiN		5					рF
Power Dissipation Capacitance*	C _{PD}							рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}{}^2 \ f_{in}$

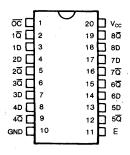
[†] For AC switching test circuits and timing waveforms see section 2.

- 8 latches in a single package
- · Full parallel access for loading
- · Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · 3-State outputs with high drive current $(I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5 \text{V})$ for direct bus interface
- . Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '533 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (E) is high. the Q outputs follow the complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (OC) which places the outputs at high-impedance state when it is taken high. The OC signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

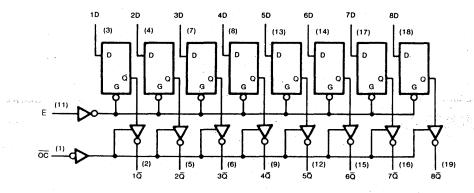
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and around.

FUNCTION TABLE

(Each Latch)

	Inputs		Output
<u>oc</u>	E	D	ā
L	н	н	L
L	H	L	н
L	L	x	\bar{Q}_0
Н	X	Х	Z

LOGIC DIAGRAM



KS54AHCT **533**

Octal D-Type Transparent Latches with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0:5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I _{OK} -
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage	V _{CC} 4.5V to 5.5V
	put Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Temp	
Range	KS74AHCT: -40°C to +85°C
•	KS54AHCT: -55°C to +125°C

Characteristic	Symbol	ol Test Conditions		= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit	
			Тур		Guaranteed Lim	its		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v	
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	



AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT533

Characteristic	Symbol			mbol Conditions†		T _a = 25°C V _{CC} = 5.0V	Ta = -40°	IAHCT C to +85°C 0V±10%	Ta = -55°C	AHCT to +125°C IV± 10%	Unit
					Min	Max	Min	Max			
Propagation Delay,	t _{PLH}	C _L =50pl C _L =150		10 13		16 21		19 25			
D to Q	t _{PHL}	C _L =50pl C _L =150		10 13		16 21		19 25	ns		
Propagation Delay,	t _{PLH}	C=50pF C _L =150		13 16		21 26		25 31			
E to Q	t _{PHL}	C _L =50pF C _L =150pF		13 16		21 26		25 31	ns		
Output Enable Time,	tpzH	$R_L=1k\Omega$	C _L =50pF C _L =150pF	11 14		18 23		22 28	ns		
OC to any Q	tpzL		C _L =50pF C _L =150pF	11 14		18 23		22 28			
Output Disable Time,	tpHZ	$R_L = 1 k\Omega$		13		18		22			
OC to any Q	tpLZ	C _L =50pF		13		18		22	ns		
Pulse Width, E High	tw			9	15		18		ns		
Setup Time, D before E↓	t _{su}			9	15		18		ns		
Hold Time, D after E↓	t _h	,		3	5		7		ns		
Input Capacitance	CiN			5					pF		
Output Capacitance	Cout	Output [oisabled	10					pF		
Power Dissipation Capacitance* (per stage)	C _{PD}	ÖC=V _{CC} ÖC=GNI		5 30					pF		

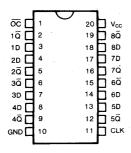
^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.
† For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (loL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '534 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

The flip-flops are edge-triggered on the positive transition of the clock: the $\bar{\mathbb{Q}}$ outputs are set to the complement of the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal (\overline{OC}) which places the outputs in high-impedance state when it is taken high, the OC signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

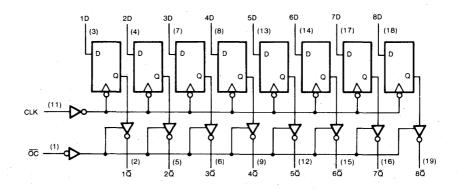
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(Each Latch)

ı	nputs	Output	
ōc	CLK	D	ā
L	1	Н	L
L	↑	L	Н
L	L	Χ	$\bar{\mathbf{Q}}_{0}$
Н	Χ	Χ	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

ricoonnii ii	aca operating containent
Supply Voltage,	V _{CC} 4.5V to 5.5V
DC Input & Outp	out Voltages*, V _{IN} , V _{OUT} 0V to V _{CC}
Operating Temper	erature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall	Times, t_r , t_f Max 500 ns
Unused inputs	must always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙςς	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tre2 ns), AHCT534

Characteristic	Symbol	Conditions†		T _a = 25°C V _{CC} = 5.0V Typ	KS74AHCT T _a = -40°C to +85°C V _{CC} =5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
·					Min	Max Min		Max	
Maximum Operating Frequency	f _{max}	C _L =50pl	F ,	50	35		30		MHz
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF		8 11		14 19		17 23	
CLK to any Q	t _{PHL}	C _L =50pl C _L =150		8 11		14 19		17 23	ns
Output Enable Time,	t _{PZH}	D -41-0	C _L =50pF C _L =150pF	11 14		18 23		22 28	ns
OC to any Q	t _{PZL}	U[- 1K77	C _L =50pF C _L =150pF	11 14		18 23		22 28	
Output Disable Time,	t _{PHZ}	$R_L=1k\Omega$		13		18		22	
OC to any Q	t _{PLZ}	C _L =50pF		13		18		22	ns
Pulse Width, CLK High or Low	tw			9	15		18		ns
Setup Time, D before CLK†	t _{su}			9	14		17		ns
Hold Time, D after CLK†	t _h			0	0		0		ns
Input Capacitance	CIN			. 5					рF
Output Capacitance	Cout	Output Disabled		10					рF
Power Dissipation Capacitance* (per stage)	C _{PD}	OC=V _{CC}		5 30					рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

Octal Buffers and Line Drivers with 3-State Outputs

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

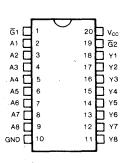
The '540 and '541 are general purpose high-speed octal line drivers/buffers with 3-state outputs. The inputs and outputs are located on opposite sides of the 20-pin package, thus improving circuit board density. The '540 provides inverted data and the '541 provides true data at the outputs.

The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

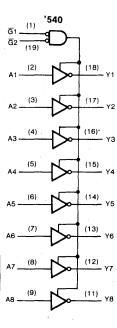
PIN CONFIGURATION



FUNCTION TABLE

	Input	Out	tput	
G ₁	G ₂	Α	'540	'541
L	L	L	Н	L
L) · L	H	L	' н
Н	×	x	Z	Z
X	н	X	Z	Z

LOGIC DIAGRAMS



Ğ1 (1) Ğ2 (19)	'541 ————————————————————————————————————	
A1(2)	F	(18) Y1
A2 (3)	-V	(17) Y2
A3(4)	-15	(16) Y3
A4(5)	F	(15) Y4
A5(6)	- 5	(14) Y5
A6	- 	(13) Y6
A7(8)	- 5	(12) Y7
A8(9)	S	(11) Y8

KS54AHCT **540/541** KS74AHCT

Octal Buffers and Line Drivers with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

Power Dissipation Per Package, Pd[†] 50° Ct of +150° Ct
Power Dissipation Per Package, Pd[†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage, Vo	c	4.	5V to 5.5V
DC Input & Output	Voltages*, V _{IN} ,	V_{OUT}	OV to V _{CC}
Operating Tempera	iture		
Range	KS74AHCT:	-40°C	to +85°C

Range KS74AHCT: $-40\,^{\circ}\text{C}$ to $+85\,^{\circ}\text{C}$ KS54AHCT: $-55\,^{\circ}\text{C}$ to $+125\,^{\circ}\text{C}$ Input Rise & Fall Times, t_r , t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74AHCT Ta = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ



[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT540, AHCT541

Characteristic	Symbol	' I		T _a = 25°C V _{CC} = 5.0V	Ta = -40°0	AHCT C to +85°C DV ±10%	KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Propagation Delay,	tpLH	C _L = 50pF C _L =150pF C _L = 50pF C _L =150pF		7 10	-	12 17		14 20	
A to Y	t _{PHL}			7 10		12 17		14 20	ns
Output Enable Time, G to Y	tpzH	R _L =1kΩ	C _L = 50pF C _L =150pF	12 15		20 25		24 30	ns
	t _{PZL}		C _L =50pF C _L =50pF	12 15		20 25		24 30	
Output Disable Time	t _{PHZ}	$R_L = 1 k\Omega$		14		19		23	
G to Y	•		C _L =50pF			19		23	ns
Input Capacitance	CiN			5					рF
Output Capacitance	Cout	Output D	isabled	10					pF
Power Dissipation Capacitance* (per stage)	C _{PD}	Ğ=V _{CC} Ğ=GND		5 30					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

- 8 latches in a single package
- · Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to + 85°C KS54AHCT: -55°C to + 125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '563 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer register, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (E) is high, the Q outputs follow complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (OC) which places the outputs at a high-impedance stage when it is taken high. The OC signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

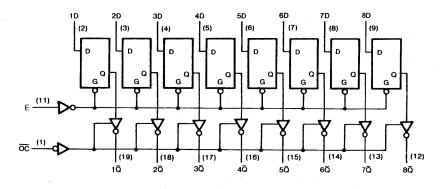
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(Each Latch)

	Inputs		Output
<u>oc</u>	E	Ď	Q
L.	Н	Н	L
L	Н.	L	Н
L	L .	Χ	\bar{Q}_{0}
• н	X	X	Z

LOGIC DIAGRAM



KS54AHCT **563**

Octal D-Type Transparent Latches with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, $t_{r},\,t_{f}$ Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	Voh	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20\mu A$ $I_O = -6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8,0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT563

Characteristic	Symbol	Conditions [†]		Conditions [†]		mbol Conditions†		T _a = 25°C V _{CC} = 5.0V	Ta = -40°0	AHCT C to +85°C DV ± 10%	Ta = -55°C	AHCT to +125°C 0V ± 10%	Unit
				Тур	Min	Max	Min	Max					
Propagation Delay,	tpLH -	C _L = 50 C _L =150		12 15		18 23		22 28					
D to Q	t _{PHL}	C _L = 50 C _L =150		12 15	<i>:</i>	18 23		22 28	ns				
Propagation Delay,	t _{PLH}	C= 50nF		14 17		22 27		27 33					
E to Q	t _{PHL}		C _L = 50pF C _L =150pF			22 27		27 33	ns				
Output Enable Time,	t _{PZH}	R _L =1kΩ	C _L = 50pF C _L =150pF	11 14		18 23		22 28	ns				
	t _{PZL}		C _L = 50pF C _L =150pF	11 14		18 23		22 28					
Output Disable Time,	t _{PHZ}	$R_L = 1 k\Omega$		13		19		22	Ī.,				
OC to any Q	tPLZ	C _L =50pl	=	13		.19		22	ns				
Pulse Width, E High	tw			9	15		18		ns				
Setup Time, D before E↓	t _{su}			6	10		10		ns				
Hold Time, D after E ↓	t _h			3	5		7		ns				
Input Capacitance	CIN		-	5					pF				
Output Capacitance	Cout	Output D	isabled	10					pF				
Power Dissipation Capacitance* (per stage)	C _{PD}	OC=V _{CC}		5 30					pF				

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

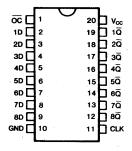
[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C + 85°C KS54HACT: -55°C + 125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '564 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

The flip-flops are edge-triggered: on the positive transition of the clock, the \bar{Q} outputs are set to the complement of the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal (\overline{OC}) which places the outputs at high impedance stat when it is taken high. The OC signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

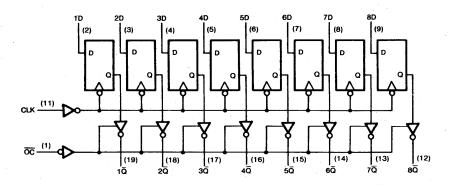
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(Each Flip-Flop)

ı	nputs	Output	
<u>oc</u>	CLK	Q	
L	†	Н	L
L	†	L	Н
L	L	Х	$\bar{\mathbf{Q}}_{0}$
н	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

		•
Supply Voltage, Vo	oc	4.5V to 5.5V
DC Input & Output	Voltages*, V _{IN} ,	Vout OV to Vcc
Operating Tempera	ature	
Range	KS74AHCT:	-40°C to +85°C
	KS54AHCT:	-55°C to +125°C
Input Rise & Fall T	imes, t _r , t _f	Max 500 ns
Unused inputs mu voltage level (eit	-	to an appropriate logic

Characteristic	Symbol	Test Conditions	Ta	=25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC} 4.2	V _{CC} −0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage		$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current		per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr., tr<2 ns), AHCT564

Characteristic	Symbol	Condition	Conditions [†]		$T_a = -40^{\circ}$	AHCT C to +85°C DV±10%	KS54 T _a = -55°C V _{CC} = 5.0		Unit
		1			Min	Max	Min	Max	
Maximum Operating Frequency	f _{max}	C _L = 50	pF	50	35	1	30		MHz
Propagation Delay,	t _{PLH}		C _L = 50pF C _L =150pF C _L = 50pF C _L =150pF			14 19		17 23	
CLK to any Q	t _{PHL}					14 19		17 23	ns
Output Enable Time,	t _{PZH}		C _L = 50pF C _L =150pF	11 14		18 23		22 28	_
OC to any Q	t _{PZL}	nL-186	C _L = 50pF C _L =150pF	11 14		18 23		22 28	ns
Output Disable Time,	tenz	R _L =1kΩ		13		19		22	ns
OC to any Q	tpLZ	C _L =50pl	F	13		19		28	
Pulse Width, CLK High or Low	t _w			9 .	15		18		ns
Setup Time, D before CLKt	t _{su}			9	14		17		ns
Hold Time, D after CLK†	t _h			0	0		0		ns
Input Capacitance	CIN			5					pF
Output Capacitance	Cout	Output D	isabled	10					pF
Power Dissipation Capacitance* (per stage)	C _{PD}	ŌC=V _{CC} ŌC=GNI		5 30					рF

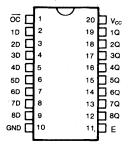
^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² fin-† For AC switching test circuits and timing waveforms see section 2.

- · 8 latches in a single package
- · Full parallel access for loading
- Function, pin-out, speed and drive compability with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- ($I_{OL} = 24$ mA @ $V_{OL} = 0.5$ V) for direct bus interface Inputs and outputs interface directly with TTL, NMOS
- and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to + 85°C KS54HACT: -40°C to + 125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '573 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing bufer registers, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable E is high, the Q outputs follow the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (OC) which places the outputs at a high-impedance state when it is taken high. The \overline{OC} signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

There devices provide speeds and drive capability equivalent of their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

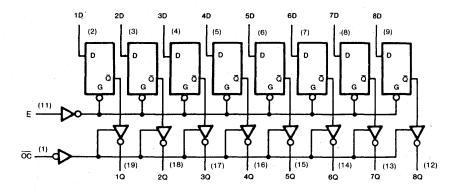
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(Each Latch)

	Inputs		Output
ос	E	D	Q
L	Н	Н	Н
L	H	L]	L
L	L	X	Q_0
Н	X	Х	Z

LOGIC DIAGRAM



Octal D-Type Transparent Latches with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
(-0.5V < V _O < V _{CC} +0.5V) ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, \	Vcc 4.5V to 5.5V
DC Input & Outpo	ut Voltages*, V _{IN} , V _{OUT} 0V to V _{CC}
Operating Tempe	rature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall	Times, t _r , t _f Max 500 ns
Unused inputs n	nust always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit	
			Тур		Guaranteed Lim	its		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6m A$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v,	
Maximum Low-Level Output Voltage	VoL	$V_{\text{IN}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $I_{\text{O}} = 20 \mu \text{A}$ $I_{\text{O}} = 12 \text{mA}$ $I_{\text{O}} = 24 \text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input t_r $t_f \leqslant 2$ ns), AHCT573

Characteristic	Symbol			T _a = 25°C V _{CC} = 5.0V	T _a = -40°0	AHCT C to +85°C 0V ± 10%	T _a = -55°C	AHCT to +125°C)V ± 10%	Unit
	1			Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}		C _L = 50pF C _L =150pF			16 19		20 23	
D to Q	t _{PHL}	C _L = 50 C _L =150		9 12		16 19		20 23	ns
Propagation Delay,	t _{PLH}	C=50pF C _L =150	C=50pF C _L =150pF			20 25		24 30	
E to Q	t _{PHL}	C _L = 50 C _L =150		12 15		20 25		24 30	ns
Output Enable Time	t _{PZH}	B140	C _L = 50pF C _L =150pF	11 14		18 23		22 28	
OC to any Q	t _{PZL}	NE – 1K22	C _L = 50pF C _L =150pF	11 14		18 23		22	ns
Output Disable Time	t _{PHZ}	$R_L = 1 k\Omega$		13		19		22	
OC to any Q	t _{PLZ}	C _L =50pl)pF	13		19		22	ns
Pulse Width, E High	t _w			9	15		18		ns
Setup Time, D before E↓	t _{su}		•	6	10		12		ns
Hold Time, D after E↓	t _h			4	7		9		ns
Input Capacitance	CIN			5					рF
Output Capacitance	Cout	Output D	isabled	10					pF
Power Dissipation Capacitance* (per stage)	C _{PD}	ÖC≃V _{CC} ÖC=GNI							pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.
† For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- ($I_{OL}=24$ mA @ $V_{OL}=0.5V$) for direct bus interface Inputs and outputs interface directly with TTL, NMOS
- and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

The '574 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

The flip-flops are edge-triggered on the positive transition of the clock. The Q outputs are set to the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal (\overline{OC}) which places the outputs at a high-impedance state when it is taken high. The \overline{OC} signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

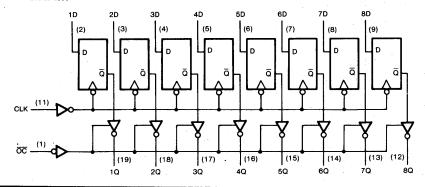
1	_	77		1	
∞ 🗆	1	_	20		Vcc
1D 🗆	2		19	Þ	1Q
2D 🗆	3		18	b	2Q
3D 🗖	4		.17	b	3Q
4D 🗆	5		16	Þ	4Q
5D 🔲	6		15	Þ	5Q
6D 🗌	7		14	D	6Q
7D 🗖	8		13		7Q
8D 🗌	9		12		ВQ
GND 🗌	10		11		CLK
				ı	

FUNCTION TABLE

(Each Flip-Flop)

ı	nputs	Output	
ОC	CLK	D	Q
L	†	Н	Н
L	†	L	L.
L	L	Χ	Q ₀
H	X	Х	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} , -0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 0.5V$ + $0.5V + 0.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Operating Temperatu	re				
Range	KS74AHCT: -40°C to +85°C				
	KS54AHCT: -55°C to +125°C				
Input Rise & Fall Times, tr, tf Max 500 ns					
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)					

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5,0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT574

Characteristic	Symbol	Condition	\ · •		$ T_a = 25^{\circ}C \\ V_{CC} = 5.0V \\ T_a = -40^{\circ}C \text{ to } +85^{\circ}C \\ V_{CC} = 5.0V \pm 10\% $		- KS54 T _a = -55°C V _{CC} = 5.0	Unit	
				Тур	Min Max		Min Max		
Maximum Operating Frequency	f _{max}	C _L = 50	pF	50	35		30		MHz
Propagation Delay,	t _{PLH}	C _L = 50 C _L =150		8 11		14 19		17 23	
CLK to any Q	t _{PHL}		C _L = 50pF C _L =150pF			14 19		17 23	ns
Output Enable Time,	t _{PZH}	$R_L = 1 k\Omega$	C _L = 50pF C _L =150pF	11 14		18 23		22 28	
OC to any Q	tezL		C _L = 50pF C _L =150pF	11 14		18 23		22 28	ns
Output Disable Time,	t _{PHZ}	$R_L = 1 k \Omega$		13		18		22	
OC to any Q	tpLZ	C _L =50pF		13		18		22	ns
Pulse Width, CLK High or Low	t _w			9	15		18		ns
Setup Time, D before CLK†	t _{su}			9	14		17		ns
Hold Time, D after CLK†	th			-3	0		0		ns
Input Capacitance	CIN			5					pF
Output Capacitance	Соит	Output D	Output Disabled						pF
Power Dissipation Capacitance* (per stage)	C _{PD}	OC=V _{CC}	DC=V _{CC}						pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

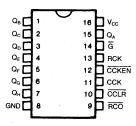
[†] For AC switching test circuits and timing waveforms see section 2.

- . Choice of 3-State ('590) and Open-Drain ('591) Outputs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These devices each consist of an 8-bit binary counter which feeds an 8-bit register. The counter is incremented on the rising edge of the CCK input, provided that clock enable, $\overline{\text{CCKEN}}$, is low. When the counter increments to the all ones condition, ripple carry out, $\overline{\text{RCO}}$, will go low. This enables either synchronus cascading of the counters by connecting the $\overline{\text{RCO}}$ of the first stage to the $\overline{\text{CCKEN}}$ of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the $\overline{\text{RCO}}$ of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The output register is loaded with the contents of the counter on the rising edge of the register clock, RCK. The outputs of this register feed the outputs which are enabled when the enable input, \overline{G} , is taken low. This enables connection of this part to a system bus. The Q outputs of the '590 are 3-State and those for '591 are Open-drain.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground

FUNCTION TABLE

		INPUTS			FUNCTION
G	RCK	CCLR	CCKEN	ССК	FUNCTION
Н	Х	Х	х	Х	Q Outputs disable
L	Х	X	X	Х	Q Outputs enable
L		Х	х	Х	Counter data is stored into register
- L	7_	Х	Х	Х	Register state is not changed
L	X	L	Х	Х	Counter clear
L	Х	Н	L		Advance one count
L	X	Н	L	ī	No count
L	Х	Н	Н	Х	No count

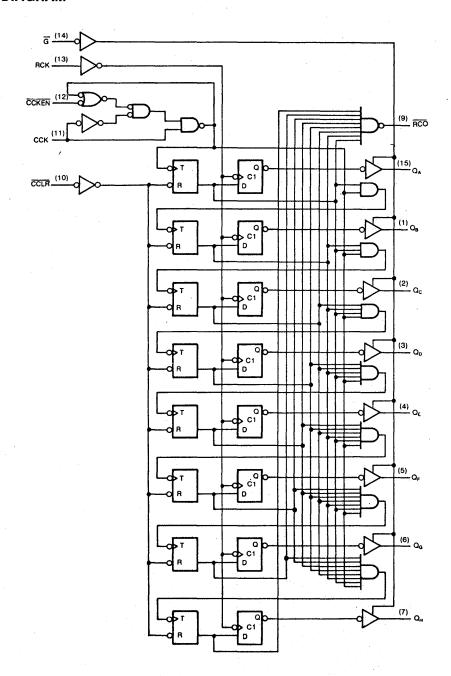
X: Don't care

 $RCO = Q_A' \cdot Q_B' Q_C' \cdot Q_D' Q_E' \cdot Q_F' Q_G' \cdot Q_H'$

 $(Q_A' \sim Q_{H'}$: Internal outputs of the counter)



LOGIC DIAGRAM



KS54AHCT **590/591** KS74AHCT

8-Bit Binary Counters with Output Registers

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

DC Input & Output	c 4.5V to 5.5V Voltages*, V_{IN} , V_{OUT} . OV to V_{CC}
Operating Tempera	ture
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C

Characteristic	Symbol	Test Conditions	st Conditions T _a = 25°		KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{iH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage (All '590 Outputs and '591 RCO Output)	VoH	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20\mu A$ $I_O = -6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1	V
Maximum Low-Level Output Voltage	Vol	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT590

Characteristic		Symbol	Conditions†	54/74ACHT T _a = 25°C V _{CC} = 5V	T _a = -40°0	AHCT C to +85°C V±10%	T _a = -55°C	AHCT C to +125°C DV ± 10%	Unit
				Typical	Min	Max	Min	Max	!
Maximum Cl	ock Frequency	f _{max}		50	30		25		ns
Propagation		t _{PLH}		15		25		29	ns
CCKt to RC	Ō	t _{PHL}		15		25		29	113
Propagation CCLR↓ to RC		t _{PHL}	C _L =50pF	17		28	•	33	ns
Propagation	Delay,	tpLH		10		16		19	
RCK1 to Q		t _{PHL}		10		16		19	ns
Output Enab	le Time,	tpzH		13		18		22	
G√ to Q		t _{PZL}	C _L =50pF	13		18		22	ns
Output Disak	ole Time,	t _{PHZ}	$R_L = 1 K\Omega$	13		18		22	ns
Gn to Q		t _{PLZ}		13		18		22	lis
Pulse Duration	CCK or RCK High or Low	t _w		10	15		20		ns
Duration	CCLR Low			10	15		20		
	CCKEN↓ before			10	15		20		
Setup Time	CCLRt before	t _{su}		6	10		10		ns
	CCK† to RCK†††			15	20		25		
Input Capacitance		CiN		5					pF
Output Capacitance (Q Outputs)		Соит	Output Disabled	10					pF
Power Dissip	ation Capacitance*	C _{PD}							рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.

^{††} This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT591

				54/74ACHT	i .	AHCT	54 A H			
Ch	Characteristic		Conditions†	T _a = 25°C V _{CC} = 5V	$T_a = -40$ °C to +85°C $V_{CC} = 5V \pm 10\%$		$T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit	
				Typical	Min	Max	Min	Max	1	
Maximum Clo	ock Frequency	f _{max}		50	30		25		MHz	
Propagation		t _{PLH}		15		25		29	ns	
CCK1 to RC	5	t _{PHL}		15		25		29	115	
Propagation CCLR↓ to RC		t _{PHL}	$C_L=50pF$ $R_I=1k\Omega$	17		28		33	ns	
Propagation	Delay,	t _{PLH}	115-187	18		31		37		
RCK1 to Q		t _{PHL}		10		16		19	ns	
Propagation Delay, G ↓ to Q		t _{PHL}		14		20		24	ns	
Propagation Delay,		t _{PLH}		14		20		24	ns	
Pulse Duration	CCK or RCK High or Low	tw	•	10	15		20		ns	
Duration	CCLR Low	·w		10	15		20			
	CCKEN↓ Low to			10	15		20			
Setup Time	CCLR† High to	t _{su}		6	10		10	*	ns	
	CCK† to RCK†††			15	20		25			
Input Capa	citance	C _{IN}		5					pF	
Power Dissip	ation Capacitance*	C _{PD}							pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.

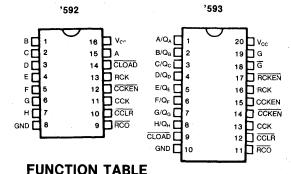
^{††} This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

- Parallel Register Inputs ('592)
- Parallel 3-State I/O: Register Inputs/Counter Outputs ('593)
- Counter Has Direct Overriding Load and Clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- ($I_{OL} = 24 \text{ mA}$ @ $V_{OL} = 0.5 \text{V}$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS



DESCRIPTION

The '592 and '593 both contain an 8-bit register which feeds an 8-bit binary counter. The counter is incremented on the rising edge of the CCK input, provided that clock enable, \overline{CCKEN} , is low. When the counter increments to the all ones condition, ripple carry out, \overline{RCO} , will go low. This enables either synchronous cascading of the counters by connecting the \overline{RCO} or the first stage to the \overline{CCKEN} of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the RCO of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The input register is loaded on the rising edge of the register clock, RCK. The outputs of this register feed the counter. The counter is loaded with the register's contents when the clock load, CLOAD, input is taken low.

The '592 differs from the '593 in that the latter device has bidirectional I input/output pins. The 3-state outputs of the counter can be enabled and are active when enable input, \overline{G} , is taken low and input G is taken high. The outputs of the counter then appear on the register inputs. This enables connection of this part to a system bus. The '593 also has a second clock enable pin, \overline{CCKEN} , which is active high and it also has an active low register clock enable, \overline{RCKEN} .

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

		INPUTS '	(592)		FUNCTION
RCK	CLOAD	CCLR	CCKEN	ССК	FUNCTION
Х	L	Н	X	×	Register data is loaded into counter
X	Н	L	- X	X	Counter clear
	н	Н	х	х	The data of a thru H inputs is stored into register
7_	Н	Н	Х	Х	Register state is not changed
Х	Н	Η	L	1	Counter advances the count
X	Н	н	L	· 7_ ·	No count
Х	Н	Н	Н	Х	No count

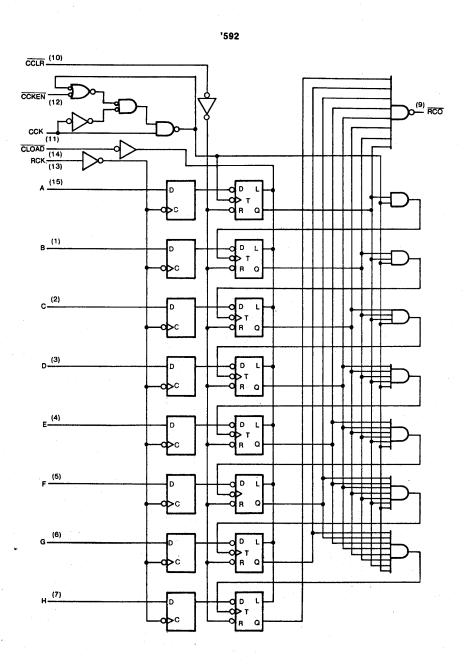
X: Don't care

 $RCO = Q_A' \cdot Q_B' Q_C' \cdot Q_D' Q_E' \cdot Q_F' Q_G' \cdot Q_H'$

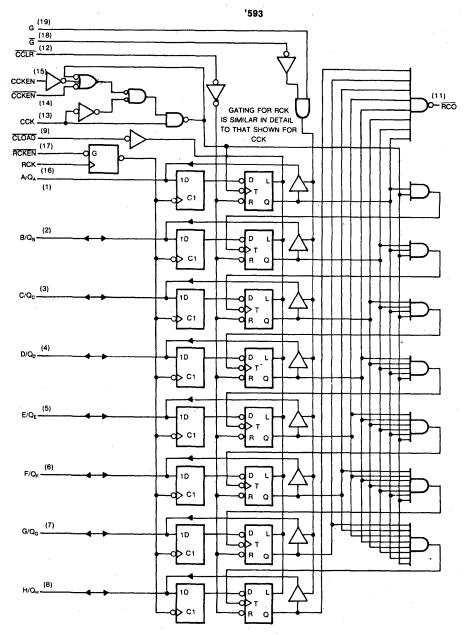
 $(Q_A' \sim Q_H'$: Internal outputs of the counter)



LOGIC DIAGRAMS



LOGIC DIAGRAMS (Continued)



Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) + \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to $+150$ °C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vcc .	4.5V to 5.5V					
DC Input & Output Voltages*, VIN, VOUT OV to Vcc						
Operating Temperature						
Range K	S74AHCT: -40°C to +85°C					
	S54AHCT: -55°C to +125°C					
Input Rise & Fall Times	i, t _r , t _f Max 500 ns					
Unused inputs must al	ways be tied to an appropriate logic					
voltage level (either \	Vcc or GND)					

Characteristic	Symbol	ol Test Conditions		= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
		-	Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	, N ^{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l _{iN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0µA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT592

Characteristic		Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	Ta = -40°C	AHCT C to +85°C OV±10%	Ta = - 55°C	AHCT to +125°C OV ± 10%	Unit
٠			-	Тур	Min Max		Min Max		
Maximum Ck	ock Frequency	f _{max}		50	30		25		MHz
Propagation	Delay,	t _{PLH}		15		25		29	
CCKt to RC	Ō	t _{PHL}		15		25		29	ns
Propagation	Delay,	t _{PLH}	C _L =50pF	15		25		29	
CLOAD↓ to F	ROO	tpHL	, o _L oop.	15		25		29	ns
	Propagation Delay,			15		25		29	ns
Propagation Delay,		tpLH	C _L =50pF	18	_	30		36	
RCKt to RC	RCK1 to RCO		CLOAD=GND	18		30		36	ns
Pulse	CCK or RCK High or Low			10	15		20		
Width	CCLR Low	t _w		10	15		20		ns
,	CLOAD Low			10	15		20		
	CCKEN↓ before CCK↑			10	15		20		
Setup Time	CCLR1 before	t _{su}		6	10		10		ns
,	RCK1 before CLOAD11			10	15		20		
	Data A-H1 before RCK1			10	15		20		
Hold Time		th		-3	0		. 0		ns
Input Capaci	tance	CIN		5					pF
Power Dissip	oation Capacitance*	CPD		•					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}{}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

¹¹ The RCK1 to CLOAD setup time ensures that the counter will see stable data from the register output.

KS54AHCT **592/593** KS74AHCT

8-Bit Binary Counters with Input Registers

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT593

					T. = 25°C		IAHCT	KS54AF		
Chi	aracteristic	Symbol Conditions†		V _{CC} = 5.0V			T _a = -55°C to		Unit	
		-	V _{CC} = 5.0V ± 10%		$\overline{}$	V _{CC} = 5.0V ± 10%		-		
	<u> </u>	<u> </u>			Тур	Min	Max	Min	Max	
Maximum (Clock Frequency	f _{max}			50	30		25		MHz
D	- D-I	tPLH	C _L =50pF C _L =150pF C _L =50pF C _L =150pF		15		25		29	
Propagatio					18		30		35	ns
OOK! to d		tpHL			15 18		25 30		29 35	
D	- B-I		0[-100	Pi	15	***************************************	25		29	+
Propagatio		tpLH	C _L =50pF				25		29	ns
		tpHL	0 50-		15			-		┼─
Propagation Delay,		t _{PLH}	C _L =50p C _L =150		15 18		25 30		29 35	
CLOAD↓ to			C ₁ = 50p		15		25		29	ns
		t _{PHL}	CL=150		18		30		35	
Propagatio	n Delay	tpLH			15		25		29	
CLOAD↓ to		tPHL	C _L =50p	F	15		25	-2.7	29	ns
Propagation Delay,		tPLH	0 -50-5		18		30		36	├
RCK1 to RCO			C _L =50pF CLOAD=GND		18		30	_		ns
Propagation Delay,		tpHL	020/10		10		30			
		t _{PHL}	C _L =50pF		15.		25		29	ns
CCLR↓ to 0	Ω		C _L =150	pF	18		30	·	35	
Propagation Delay, CCLR		t _{PLH}	C _L =50pl	F	15		25		29	ns
		t _{PZH}	C _L =50pF		13	•	20		24	
Enable Tim		IPZH	R _L =1kΩ	C _L =150pF	16		25		30	ns
Gf or Gil to	o Q	tezL		C _L =50pF	13		20		24	110
		-12L		C _L =150pF	16		25		30	
Disable Tim		t _{PHZ}	$R_L=1k\Omega$	_	13		20		24	ns
Gilor Gf to	Q '	tpLZ	C _L =50pl	-	13	One of the last of	20		24	
Pulse	CCK or RCK High or Low				10	15		20		ns
Width	CCLR Low	tw			10	15		20		115
	CLOAD Low				10	15		20		
	CCKEN↓ before		770		10	15		20		
	RCKEN∔ to									
Setup	RCKt				10	15		20		
Time	CCLR↓ before CCKf	t _{su}			6	10		10		ns
	RCK† before				10	15		20		
	Data A-H before RCKf				10	15		20		
Hold Time		th			-3	0		0		ns
Input Capa	citance	CIN			5					pF
			Output D	isabled	10					pF
Output Capacitance Power Dissipation		C _{PD}								pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-}

The RCK1 to CLOAD setup time ensures that the counter will see stable data from the register output.



[†] For AC switching test circuits and timing waveforms see section 2.

- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage.
- Choice of 3-State ('595) or Open-Drain ('596) Parallel Outputs.
- . Shift Register Has Direct Clear.
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
 (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

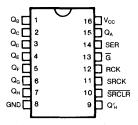
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('595) or opendrain ('596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



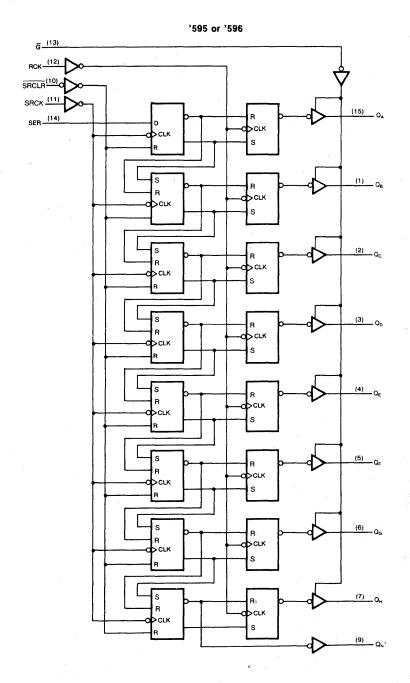
FUNCTION TABLE

		INPUTS			FUNCTION
SER	SRCK	SRCLR	RCK	Ğ	FUNCTION
Х	Х	Х	X	Н	Q _A thru Q _H outputs disable
Х	Х	×	X	L	Q _A thru Q _H outputs enable
X	Χ.	L	· X	Х	Shift register is cleared.
L		н	х	х	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
Н	1	Н	Х	X	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
X	I	Н	X	X	State of S.R. is not changed.
Х	X	×		Х	S.R. data is stored into storage register.
X	Х	Х	7_	Х	Storage register state is not changed.

X: DON'T CARE



LOGIC DIAGRAM



KS54AHCT 595/596 KS74AHCT 595/596

8-Bit Shift Registers with Output Latches

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Petings are those values havened

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V	cc 4.5V to 5.5V
DC Input & Outpu	t Voltages*, V _{IN} , V _{OUT} 0V to V _{CC}
Operating Temper	ature
Range	KS74AHCT: -40°C to +85°C
_	KS54AHCT: -55°C to +125°C
Input Rise & Fall 1	Times, t_r , t_f Max 500 ns
Unused inputs m	ust always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	Unit V V V μΑ μΑ
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage (All '595 Outputs and '596 QH' Output)	Voh	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{C}=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} = 0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lco .	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr., tre2 ns), AHCT595, AHCT596

Characteristic		Symbol	Condition	s†	T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		T. = -55°C	AHCT to +125°C V± 10%	Unit
					Тур	Min	Max	Min	Max	
Propagation Delay, SRCK1 to Q'H		tPLH	C = 505	=	15		17		20	
		t _{PHL}	C _L =50pF		15		. 17		20	ns
Propagation Delay, RCK1 to Q _A thru Q _H		t _{PLH}	C _L =50pl C _L =150		11 14		22 21		27 25	
		t _{PHL}	C _L =50pl C _L =150		11 14		17 22		20 26	ns
Output Enable Time, Gł to Q _A thru Q _H ('595 only)		tpzH		C _L =50pF C _L =150pF	14 17		20 25		24 30	
		tpzL	R _L =1kΩ	C _L =50pF C _L =150pF	14 17		20 25		24 30	ns
Output Disable Time, Gt to Q _A thru Q _H ('595 only)		t _{PHZ}	$R_L = 1 k\Omega$		14		20		24	
		tpLZ	C _L =50pl	F	14		20		24	ns
Propagation Delay, Gt to Q _A thru Q _H ('596 only)		tрLН	C _L =50pF C _L =150pF		14 17		20 25		24 30	ns
Propagatio G↓ to Q _A t ('596 only	thru Q _H	t _{PHL}	C _L =50pl C _L =150		14 17		20 25		24 30	ns
Pulse	SRCK or RCK	tw			10	15		20		
Width	SRCLR Low	1	ļ .		10	15		20		ns
Setup	SRCLRt to SRCKt				6	10	,	12		
Time	SER to SRCK1	tsu			10	15		20		ns
	SRCK† to RCK††				15	20		25		
Hold Time,		th			-3	0		0		ns
Input Capa	acitance	C _{IN}			5					рF
Output Ca	pacitance	Cour	Output D	isabled	10					рF
Power Dis Capacitan	•	C _{PD}	-							рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f_{in}$.

Note: The RCK1 to CCK1 setup time ensures that the counter will see stable data from the register output.

[†] For AC switching test circuits and timing waveforms see section 2.

- 8-Bit Parallel Storage Register Inputs
- shift Register has Direct Overiding Load and Clear.
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74AHCT: -40°C to +85°C
 - KS54AHCT: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

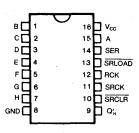
DESCRIPTION

The '597 consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

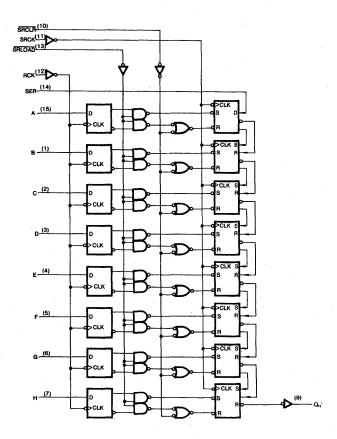
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



KS54AHCT **597** KS74AHCT

8-Bit Shift-Registers with Input Latches

FUNCTION TABLE

		INPUTS			FUNCTION
SER	SRCK	SRCLR	SRLOAD	RCK	FUNCTION
х	· X	L	Н	X	S.R. is cleared to "L"
х	Х	Н	J	x	Input register data is stored into S.R.
L	5	н	Н	х	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
Н		н	н	х	First stage of S.R. becomes "H". Other stages stores the data of previous stage, respectively.
Х	Х	X	Х		State of S.R. is not changed.
Χ	Х	Х	Х	5	Input data on A∼H line is stored into input register
X	Х	Х	Х	7_	Storage register state is not changed.

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} , −0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} −65 °C to +150 °C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	bol Test Conditions		= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v	
Maximum Low-Level Output Voltage	l	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O = 4 mA I _O = 8 mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	



AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT597

Characteristic		Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	T _a = -40°0	AHCT C to +85°C DV ±10%	KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Maximum Cl	ock Frequency	f _{max}		50	30		25		MHz
Propagation	Delay,	tplH		15		17		20	
SRCK1 to Q	SRCK↑ to Q'H			15		17		20	ns
Propagation	Delay,	tpLH	C _L =50pF	14		20	ţ	24	
SRLOAD↓ to Q'H		t _{PHL}		14		20		24	ns
Propagation Delay, SRCLR↓ to Q'H		ť _{PHL}		11		18		21	ns
Propagation Delay, RCK1 to Q'H		telh	C _L =50pF	15		25		29	ns
		t _{PHL}	SLOAD=Low	15		25	. ,	29	
Pulse	RCK or SRCK High or Low	t _w		10	15			20	70
Width	SRCLR or SRLOAD Low			10	15		20		ns
	SRCLRt before SRCKt			6	10		12		
Setup Time	RCK† before SRCK†††	t _{su}		15	20	i	25		ns
	SER before SRCK1		-	10	. 15		20		
	A thru H before RCK1			10	15		20		
Hold Time		th		-3	0		0		ns
Input Capaci	tance	CiN		5					pF.
Power Dissip	ation Capacitance*	C _{PD}							pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-}

[†] For AC switching test circuits and timing waveforms see section 2.

¹¹ The RCK1 to CCK1 setup time ensures that the counter will see stable data from the register output.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ($I_{OL}=24$ mA @ $V_{OL}=0.5V$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These high-speed octal/bus transceivers are designed for asynchronous two-way communication between data buses. A direction control input (DIR) controls the flow direction of data. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A. The '643 transfers inverted data from the A bus to the B bus and non-inverted data from the B bus to the A bus. The '640 transfers inverted data in both directions.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

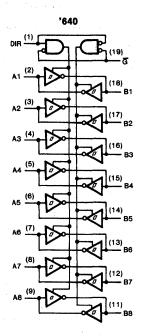
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

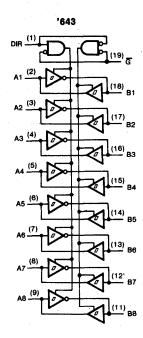
PIN CONFIGURATION

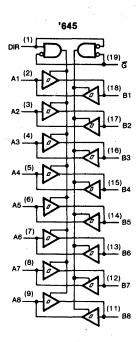
FUNCTION TABLE

Control Inputs		Operation						
G	DIR	'640	'643	'645				
L	L	Inverted data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A				
L	Н	Inverted data transmitted from Bus A to Bus B	Inverted data transmitted from Bus A to Bus B	Data transmitted from Bus A to Bus B				
н	х	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)				

LOGIC DIAGRAMS







Absolute Maximum Ratings*

Supply Voltage Range Vcc,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I _{OK}
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) + 2.5V + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply vollage,	VCC 4.5V to 5.5	٧
DC Input & Out	out Voltages*, V _{IN} , V _{OUT} OV to V _O	c
Operating Temp	erature	
Range	KS74AHCT: -40°C to +85°	C
	KS54AHCT: -55°C to +125°	С
Input Rise & Fal	Times, t _r , t _f Max 500 r	ıs
	must always be tied to an appropriate log	ic
voltage level (either Vcc or GND)	



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур	Guaranteed Limits			
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	V_{IN} = V_{IH} or V_{IL} I_O =20 μ A I_O =12 μ A I_O =24 μ A	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσσ	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT640, AHCT643

Characteristic	Symbol	Conditions†		T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF C _L =50pF C _L =150pF		7 10		12 17		14 20	ns
A to B, or B to A	t _{PHL}			7 10		12 17.		14 20	113
Output Enable Time.	tpzh	R _L =1kΩ	C _L =50pF C _L =150pF	12 15		20 25	S . 10 (1) (1)	25 31	ns
G to A or B	tpzL		C _L =50pF C _L =150pF	12 15		20 25		25 31	
Output Disable Time,	tenz	$R_L = 1 k\Omega$ $C_L = 50 pF$		13		18		22	ns
G to A or B	tPLZ			13		18		22	
Input Capacitance	CiN			5				1 1 1 1 1 1 1	рF
Output Capacitance	Cout	Output Disabled		10					рF
Power Dissipation Capacitance*	C _{PD} *	G=V _{CC} (per stage) G=GND		5 30				-	pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}



[†] For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT645

Characteristic			T _a = 25°C V _{CC} = 5.0V	$KS74AHCT$ $T_{a} = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit	
				Тур	Min	Max	Min	Max .	
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150p		6 9		10 19		14 25	20
A to B, or B to A	t _{PHL}	C _L =50pF C _L =150pF		6 9		10 19		14 25	ns
Output Enable Time	tpzH	Rı = 1kΩ	C _L =50pF C _L =150pF	12 18		20 29		25 36	ns
G to A or B	t _{PZL}	U[- 1K2	C _L =50pF C _L =150pF	12 18		20 29		25 36	
Output Disable Time,	t _{PHZ}	$R_L = 1k\Omega$		13		18		22	ns
G to A or B	tPLZ	C _L =50pF		13		18		22	115
Input Capacitance	CIN			5			,		рF
Output Capacitance	Cour	Output Di	sabled	10					pF
Power Dissipation Capacitance*	C _{PD} *	Ğ=V _{CC} Ğ=GND	(per stage)	5 30					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

KS54AHCT **646/648** KS74AHCT

Octal 3-State Bus Transceivers with Registers

FEATURES

- 8 bi-directional data paths
- . Transmits direct or stored data in either direction
- 24-pin slim DIP package
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · 3-State outputs with high drive current
- $(I_{OL} = 24 \text{ mA } @ V_{OL} = 0.5 \text{V})$ for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to + 85°C KS54HACT: -55°C to + 125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION

		_	
CAB□	1	24	J∨∞
SABC	2	23	СВА
DIR C	3	22	SBA
A1C	4	21	ΒĞ
A2 🗆	5	20	B 1
A3 🗆	6	19	□ B2
A4 🗆	7	18	В3
A5 □	8	17	□ 84
A6 🗀	9	16	B5
A7 🗆	10	15	_ B6
A8 🗆	11	14	B7
GND [12	13	□ B8

DESCRIPTION

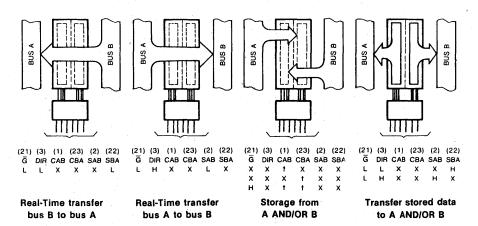
The '646 and '648 are bi-directional bus transceivers with D-type flip-flops and control circuitry to facilitate high speed multiplexed data transmission. The '646 transmits true data and the '648 transmits inverted data.

Data can be transmitted directly from one port to the other in either direction. It also can be stored in the flip-flops from either or both ports for subsequent transmission to the opposite port. Six control inputs govern the data flow:

- G (output enable) when high, all outputs are disabled, isolating the A and B ports. When low, one port is enabled at a time as determined by the DIR pin.
- DIR (direction control) disables A or B outputs permitting the pins to be used as inputs thus determining the direction of a data flow. When DIR=high, data flows from A to B.
- SAB,SBA (data source AB and BA) determines whether data transmitted is from the data inputs or the registers associated with those inputs.
- CAB,CBA (Clock AB and BA) clocks data from the A inputs and the B inputs, respectively, into their associated registers. Since the clocks are not gated with the G and DIR pins, data at the A and B pins can be clocked into the flip-flops at any time.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

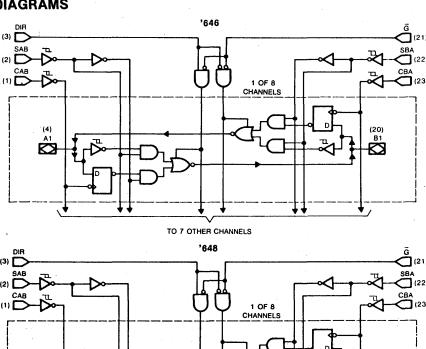


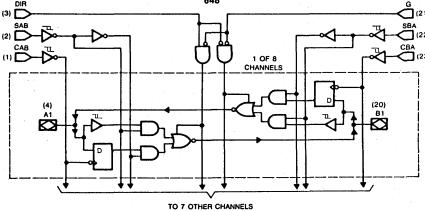
FUNCTION TABLE

Inputs Data I/0			1/0*	Operation or Function					
$\tilde{\mathbf{G}}$	DIR	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	'646	'648
1	X	† X	X ↑	X	X X	input Not specified	input Not specified	Store A, B unspecified Store B, A unspecified	Store A, B unspecified Store B, A unspecified
H	X	↑ HorL	↑ H or L	X	X	Input	Input	Store A and B data Isolation, hold storage	Store A and B data isolation, hold storage
L	L L	X	X H or L	X	L H	Output	Input	Real-Time B data to A bus Stored B data to A bus	Real-Time B data to A bus Stored B data to A bus
L L	H H	X H or L	X	L H	X X	Input	Output	Real-Time A data to B bus Stored A data to B bus	Real-Time Ā data to B bus Stored Ā data to B bus

^{*}The data output functions may be enabled or disabled by various signals at the \widetilde{G} and DIR inputs. Data input functions are always enabled, ie., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

LOGIC DIAGRAMS





KS54AHCT **646/648** KS74AHCT

Octal 3-State Bus Transceivers with Registers

Absolute Maximum Ratings*

•
Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	Vcc	4.5V to 5.5V
	put Voltages*, V _{IN} , V	
Operating Temp	erature	
Range	KS74AHCT: -	-40°C to +85°C
_	KS54AHCT: -	55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns Unused inputs must always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T _a = -55°C to +125°C	Unii
		·	Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	V _{IN} =V _{IH} or V _{IL} I _O =−20µA I _O =−6mA	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	٧
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20μA I _O =12mA I _O =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	IIN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =O _µ A		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



Octal 3-State Bus Transceivers with Registers

AC ELECTRICAL CHARACTERISTICS (Input tr., tr<2 ns), AHCT646, AHCT648

Characteristic	Symbol Condition		ditions†	T _a = 25°C V _{CC} = 5.0V	T AD'C to ARS'C!		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit	
				Тур	Min Max		Min Max			
Maximum Frequency	f _{max}	C _L =50pF		45		30		25	MHz	
Propagation Delay,	tPLH	C _L =50pf C _L =150p		11 14		18 23		22 28	ns	
A or B Input to B or A Output	t _{PHL}	C _L =50pf C _L =150p		11 14		18 23		22 28		
Propagation Delay,	t _{PLH}	C _L =50pl C _L =150pl		15 18		25 30		30 36		
CBA or CAB Input to A or B Output	t _{PHL}	C _L =50pF C _L =150p		15 18		25 30		30 36	ns	
Propagation Delay, ^{††} SBA or SAB Input to A or B Output (with A or High)	t _{PLH}	C _L =50pf C _L =150p		16 19	,	27 33		32 38	ns	
	t _{PHL}	C _L =50pf C _L =150p		16 19		27 33		32 38	113	
Propagation Delay,†† SBA or SAB Input to	t _{PLH}	C _L =50pF C _L =150pF C _L =50pF C _L =150pF		15 18		25 30		30 36	ns	
A or B Output (with A or Low)	t _{PHL}			15 18		25 30		30 36		
Out Enable Time,	tpzH	Rı=1kΩ	C _L =50pF C _L =150pF	14 17		22 27		26 32	ns	
G or DIR Input to A or B Output	tpzL	UL- IVE	C _L =50pF C _L =150pF	14 17		22 27		26 32	113	
Output Disable Time,	tpHZ	$R_L = 1 k\Omega$		13		22		26	ne	
G or DIR Input to A or B Output	t _{PLZ}	C _L =50pf	=	13		22		26	ns	
Pulse Duration, Clocks High or low	t _w			8	12		15		ns	
Set up Time, A before CABt or B before CBAt	t _{su}			8	12		15		ns	
Hold Time, A after CABt or B after CBAt	th			0	0		0		ns	
Input Capacitance	CIN			5					pF	
Output Capacitance	Соит	Output Di	sabled	10					pF	
Power Dissipation Capacitance*	C _{PD}								pF	

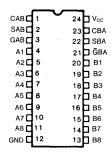
^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² fin-

[†] For AC switching test circuits and timing waveforms see section 2.

^{††} These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored-Data
- Choice of Time and Inverting Data Paths
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- . Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- ($I_{OL} = 24$ mA @ $V_{OL} = 0.5V$) for direct bus interface
 Inputs and outputs interface directly with TTL, NMOS
- Inputs and outputs interface directly with TTL, NMO and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74AHCT: -40°C to +85°C
 - KS54AHCT: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



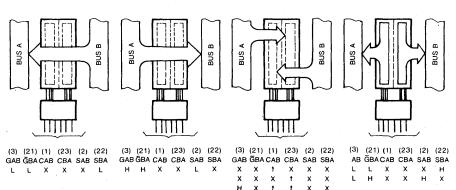
DESCRIPTION

These devices consist of bus transceiver circuits. D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and GBA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental busmanagement functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.



Real-Time transfer bus B to bus A

Real-Time transfer bus A to bus B

Storage from A AND/OR B

Transfer stored data

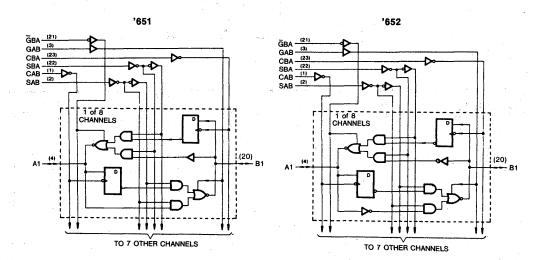


FUNCTION TABLE

	INPUTS					DATA	1/0*	OPERATION OR FUNCTION		
GAB	ĞBA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'651	'652	
L L	H H	H or L	H or L ↑		X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data	
X	H	† †	H or L	X X**	X	Input Input	Not specified Output*	Store A, Hold B Store A in both registers	Store A Hold B Store A in both registers	
L	X L	H or L ↑	. † †	X X	X X**	Not specified Output*	Input Input	Hold A, Store B Store B in both registers	Hold A, Store B Store B in both registers	
L L	L L	X X	X H or L	X X	L	Output	Input	Real-Time B Data to A Bus Stored B Data to A Bus	Real-Time B Data to a Bus Stored B Data to A Bus	
H	H	X H or L	X	L H	X	Input	Output	Real-Time Ā Data to B Bus Stored Ā Data to Bus	Real-Time A Data to B Bus Stored A Data to B Bus	
н	L	H or L	H or L	н	н	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus	

^{*} The data output functions may be enabled or disabled by various signals at the GAB and GBA inputs. Data input functions are always enabled, ie., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

LOGIC DIAGRAMS



^{**} Select control=L: clocks can occur simultaneously Select control=H: clocks must be staggered in order to load both registers

KS54AHCT **651/652** KS74AHCT

Octal 3-State Bus Transceivers with Registers

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, Iok
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
Vcc or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{ОН}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1	V
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



Octal 3-State Bus Transceivers with Registers

AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT651, AHCT652

Characteristic	Symbol	Con	ditions†	T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Clock Frequency	f _{max}	C _L =50pl	F	45	30	1	25		MHz
Propagation Delay, A or B Input to	tpLH	C _L =50pl C _L =150		11 14		18 23		22 28	
B or A Ouput	tpHL	C _L =50pl C _L =150		11 14		18 23		22 28	ns
Propagation Delay,	tpLH	C _L =50pl C _L =150		15 18		25 30		30 36	
CBA or CAB Input to A or B Output	tpHL	C _L =50pl C _L =150		15 18		25 30		30 36	ns
Propagation Delay, SBA or SAB Input to	tpLH	C _L =50pl C _L =150		16 19		27 32		32 38	
A or B Output (with A or B High)	tpHL	C _L =50pl C _L =150		16 19		27 32		32 38	ns
Propagation Delay, SBA or SAB Input to	t _{PLH}	C _L =50pl C _L =150		15 18		25 30		30 36	
A or B Output (with A or B Low)	tpHL	C _L =50pF C _L =150pF		15 18		25 30	·	30 36	ns
Output Enable Time,	tpzL		C _L =50pF C _L =150pF	19 22		32 37		38 44	
GBA to A or GAB to B	tpzn	R _L =1kΩ	C _L =50pF C _L =150pF	19 22		32 37		38 44	ns
Output Disable Time,	tpHZ	$R_L=1k\Omega$		13		22		26	
GBA to A or GAB to B	tpLZ	C _L =50pF		13		22		26	ns
Pulse Width Clocks High or Low	tw			8	12		15		ns
Setup Time, A before CAB1 or B before CBA1	t _{su}			8	12		15		ns
Hold Time, A after CAB1 or B after CBA1	t _h			0	0		0		ns
Maximum Input Capacitance	CIN			5					рF
maximum Output Capacitance	Cout	Output D	isabled	10					рF
Power Dissipation Capacitance*	C _{PD}								pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-}



Lefor AC switching test circuits and timing waveforms see section 2.

- Bus Transceivers with Inverting Outputs ('658) or True Outputs ('659)
- . Generates a Parity Bit for A Bus and B Bus
- · Easily Cascadable
- Internal Active Pull-Ups and Pull-Downs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
 - ($I_{OL} = 24 \text{ mA}$ @ $V_{OL} = 0.5 \text{V}$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION

GAB 🗖	1	24	D V _{cc}
A1 🗖	2	23	□ GBA
A2 🗖	3	22	⊐ B1
АЗ 🗖	4	21	□ B2
A4 🗖	5	20	□ B3
A5 🗖	6	19	□ B4
A6 🗖	7	18	□ B5
A7 🗖	8	17	□ B6
A8 🗖	9	16	B7
вы 🗖	10	15	3 B8
вро 🗖	11	14	API
GND 🗖	12	13	APO
		_	•

DESCRIPTION

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus, or from the B Bus to the A Bus, depending on the levels at the direction control inputs, GAB and $\overline{G}BA$. These devices also generate parity outputs. APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuits on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuits.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

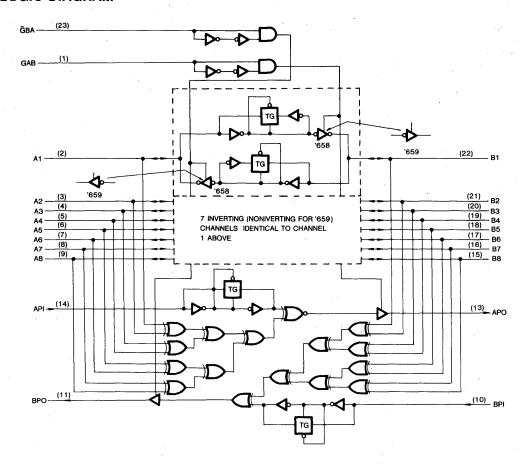
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

	TROL UTS	NUMBER OF HIGH INPUTS ON	NUMBER OF HIGH INPUTS ON	OUTPUTS		OPERATION		
ĞΒΑ	GAB	A BUS AND API			'658	'659		
L		X	0, 2, 4, 6, 8	Z	Н	B Data to A Bus	B Data to A Bus	
		X	1, 3, 5, 7, 9	Z	L	b Data to A bus	b Data to A bus	
Н	н	0, 2, 4, 6, 8	X	Н	Z	Ā Data to B Bus	A Data to B Bus	
- 17	l ii	1, 3, 5, 7, 9	X	L	Z	A Data to B Bus		
Н	L	X	X	Z	Z	Isolation	Isolation	
		X	0, 2, 4, 6, 8		Н			
L	н	X	1, 3, 5, 7, 9		L	B Data to A Bus,	B Data to A Bus,	
L.	L	0, 2, 4, 6, 8	X	Н		A Data to B Bus	A Data to B Bus	
		1, 3, 5, 7, 9	X .	L				



LOGIC DIAGRAM



Absolute Maximum Ratings*

Absolute maximum natings
Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ m/s}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

CC	
it Voltages*, V _{IN} , V _{OL}	JT . OV to Vcc
rature	
KS74AHCT: -4	40°C to +85°C
KS54AHCT: -58	5°C to +125°C
Times, t_r , t_f	Max 500 ns
ust always be tied to ar	n appropriate logic
ither V _{CC} or GND)	
	nt Voltages*, V _{IN} , V _{OL} rature KS74AHCT: -4 KS54AHCT: -55 Times, t _r , t _f



KS54AHCT 658/659 KS74AHCT

Octal Bus Transceivers with Parity

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit	
			Тур					
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	v	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	In	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT658, AHCT659

Characteristic	Symbol	ool Conditions†		$ T_a = 25^{\circ}C $ $ V_{CC} = 5.0V $		KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	
				Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	C _L =50pl C _L =150		11 14		18 23		22 28	ns -
A or B to B or A	t _{PHL}	C _L =50pl C _L =150pl		11 14		18 23		22 28	
Propagation Delay, A or B to APO or BPO	t _{PLH}		C _L =50pF C _L =150pF			27 32		32 38	- ns -
	t _{PHL}	C _L =50pF C _L =150pF		16 19		27 32		32 38	
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF C _L =50pF C _L =150pF		11 14		18 23		22 28	ns -
API or BPI to APO or BPO	t _{PHL}			11 14		18 23		22 28	
Enable Time, GAB or	t _{PZH}	Rı = 1kΩ	C _L =50pF C _L =150pF	16 19		27 32		32 38	ns
GBA to APO or BPO	t _{PZL}	INL - IKW	C _L =50pF C _L =150pF	16 19		27 32		32 38	
Disable Time, GAB or	tPLZ	$R_L = 1 k\Omega$		16		27		32	ns
GBA to APO or BPO	t _{PHZ}	C _L =50pl	F	16		27		32	
Input Capacitance	CIN			5				1 1 1 1	pF
Output Capacitance	Cour				Ĺ				pF
Power Dissipation Capacitance*	C _{PD}		-tiiAi		·		. 11		pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

[†] For AC switching test circuits and timing waveforms see section 2.



- Bus Transceivers with Inverting Outputs ('664) or True Outputs ('665)
- . Generates a Parity Bit for A Bus and B Bus
- Easily Cascadable
- Internal Active Pull-Ups and Pull-Downs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (loL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION

DIR 🗆	└	24 V _{CC}
A1 🗆	2	23 🗖 🛱
A2 🗆	3	22 🗖 B1
A3 🗆	4	21 B2
A4 🗆	5	20 🗖 B3
A5 🗆	6"	19 B4
A6 🗆	7	18 🗖 B5
A7 🗆	8	17 🗖 B6
A8 🗖	9	16 🗖 B7
вы 🗖	10	15 🗖 B8
вро 🗖	11	14 API
GND 🗖	12	13 APO

DESCRIPTION

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus or from the B Bus to the A Bus, depending on the level at the direction control input, DIR. The enable input, \overline{G} , can be used to disable the device so that the buses are isolated. These devices will also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuitry on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by the activity on the bus. The advantage of this arrangement is tht when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuitry.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

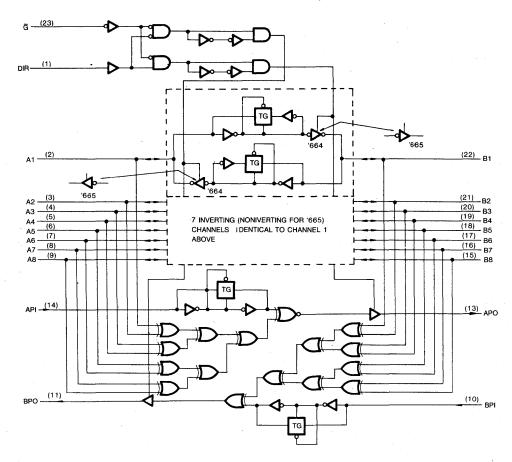
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to Vcc and ground.

FUNCTION TABLE

-	NTROL PUTS	NUMBER OF HIGH INPUTS ON	NUMBER OF HIGH INPUTS ON	OUT	PUTS	OPER	PERATION	
Ğ	DIR	A BUS AND API	B BUS AND BPI	APO	вро	'664	'665	
	1	* X	0, 2, 4, 6, 8	Z	Н	B Data to A Bus	B Data to A Bus	
	_	X	1, 3, 5, 7, 9	Z	L	b Data to A bus		
	н	0, 2, 4, 6, 8	X	Н	Z	à Data to B Bus	A Data to B Bus	
•		1, 3, 5, 7, 9	X	L	Z	A Data to B Bus	A Data to B Bus	
Н	X	X	X	Z	Z	Isolation	Isolation	



LOGIC DIAGRAM



Absolute Maximum Ratings*

, and other trees, and the state of the stat
Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, Iok
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)



Octal Bus Transceivers with Parity

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Symbol Test Conditions		= 25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
<u> </u>		* 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =12mA I _O =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND	-	±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA	-	2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tr<2 ns), AHCT664, AHCT665

Characteristic	Symbol Conditions†			T _a = 25°C V _{CC} = 5.0V	T. = -40°0	AHCT C to +85°C DV±10%	KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	C _L =50pi C _L =150		11 14		18 23		22 28	ns
A or B to B or A	tpHL	C _L =50pl C _L =150		11 14		18 23		22 28	ns
Propagation Delay,	tpLH	C _L =50pl C _L =150		16 19		27 32		32 38	ns
A or B to APO or BPO	tpHL	C _L =50pl C _L =150		16 19		27 32		32 38	ns
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF C _L =50pF C _L =150pF		11 14		18 23		- 22 28	ns
API or BPI to APO or BPO	t _{PHL}			11 14		18 23		22 28	ns
Output Enable Time,	tрzн	R _L =1kΩ	C _L =50pF C _L =150pF	16 19		27 32	_	32 38	ns
G to A or B	tpzL	UL-IKW	C _L =50pF C _L =150pF	16 19		27 32		32 38	ns
Output Disable Time,	tpHZ	$R_i = 1 k\Omega$		16		27		32	ns
G to A or B	tPLZ	C _L =50pl	. , j	16		27		32	ns
Output Enable Time,	t _{PZH}	$R_L = 1k\Omega$	C _L =50pF C _L =150pF	16 19		27 32		32 38	ns
DIR to A or B	tpzL	U[1K1	C _L =50pF C _L =150pF	16 19		27 32		32 38	ns
Output Disable Time,	t _{PHZ}	R _L =1kΩ		16		27		32	ns
DIR to A or B	tPLZ	C _L =50pl	F	16		27		32	ns
Input Capacitance	CIN			5					рF
Output Capacitance	Соит	Output D	isabled						рF
Power Dissipation Capacitance*	C _{PD}		•						pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

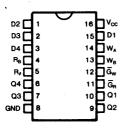
[†] For AC switching test circuits and timing waveforms see section 2.

- Seperate Read Write
 Addressing Permits Simultaneous Reading and
 Writing
- . Expandable to 512 Words of 7-bits
- · For use as:
 - Scratch pad memory
- Buffer Storage between processors
- Bit storage in fast multiplication designs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current
 - (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLES

WRITE MODE SELECT TABLE

OPERATING	INPL	JTS	INTERNAL LATCHES(*)	
MODE	Ğw	Dn		
Write Data	L	H	L H	
Data Latched	н	×	no change	

NOTE:

a. The Write Address (W_A and \overline{W}_B) to the "Internal latches" must be stable while \bar{G}_W is LOW for conventional operation.

DESCRIPTION

The '670 is a 16-bit 3-State Register File organized as 4 words of 4 bits each. Separate Read and Write Address and enable inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs (W_A and W_B) determine the location of the stored word. When the Write Enable (\overline{G}_W) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the \overline{G}_W is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-State outputs. Data and Write Address inputs are inhibited when \overline{G}_W is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A and R_B). The addressed word appears at the four outputs when the Read Enable ($\overline{\text{G}}_{\text{R}}$) is LOW. Data outputs are in the HIGH impedance "off" state when the read enable input is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-State outputs together. Since the limiting factor for expansion is the output HIGH current, further stacking is possible by tying pull-up resistors to the outputs to increase the l_{OH} current available. Design of the read enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the enable and address inputs of each device in parallel.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

READ MODE SELECT TABLE

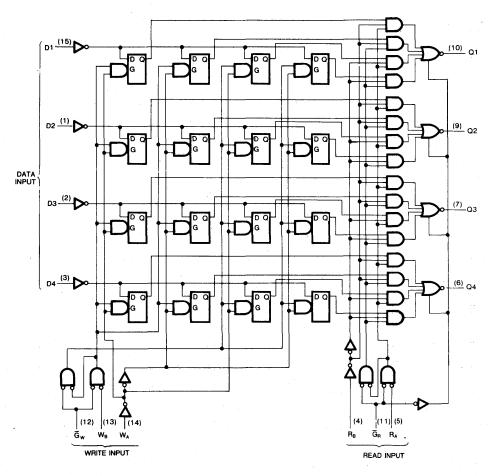
005047440	ı	NPUTS	OUTDUT	
OPERATING MODE	ĞR	INTERNAL LATCHES(b)	OUTPUT Q _n	
Read	L	L	L	
Head	L	н	Н	
Disabled	Н	Н	(Z)	

NOTE:

b. The selection of the "internal latches" by Read Address $(\overline{R_A} \text{ and } R_B)$ are not constrained by \overline{G}_W or \overline{G}_R operation.



LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} -65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	mbol Test Conditions		=25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit		
			Тур	, .	Guaranteed Lim	mits			
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v		
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} = 0.1 3.7	v		
Maximum Low-Level Output Voltage	VoL	V _{IN} =V _{IH} or V _{IL} I _O =20μA I _O =12mA I _O =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND	,	±0.5	±5.0	±10.0	μΑ		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT670

	Characteristic		Con			T 40°C		$KS54AHCT$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
					Тур		Max	Min	Max	} .
		tpLH	C _L =50pl		14 17		23 28		23 34	
Maximum Propagation Delay, RA or RB to Output			C _L =50pl	F	14		23 28		28 34	ns
Propagatio	n Delay.	t _{PLH}	C _L =50pl C _L =150		15 18		25 30		30 36	ns
Gw to Output			C _L =50pF C _L =150pF		15 18		25 30		30 36	
Propagation Delay,			$C_L=50pF$ $C_L=150pF$		14 17		23 28		28 34	ns
	Data to Output		$C_L=50pF$ $C_L=150pF$		14 17		23 28		28 34	1,19
Output En	able Time	t _{PZH}	B ₁ = 1 k0	C _L =50pF C _L =150pF	13 16		21 26		25 31	ns
GR to Outp		t _{PZL}	11.	$C_L=50pF$ $C_L=150pF$	13 16		21 26		25 31	
Output Dis	able Time	t _{PHZ}	$R_L = 1 k\Omega$		17		28		34	ns
G _R to Outp	out	tPLZ	C _L =150	ρF	17		28		39	110
Set up	D _n to G _W	tsu			6	10		12		ns
Time	W _A ,W _B to G _W		!		10	14		16		
Hold	D _n to G _W	th			0	0		0		ns
Time	W _A , W _B to G _W	•0			0	0		-0		
Input Capa	citance	CIN			5					pF
Output Cap	pacitance	Cout	Output di	sabled	10					рF
Power Dis	sipation Capacitance*	CPD								рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \, V_{CC}{}^2 \, f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.

- '679: 12-bit to 4-bit comparator with enable
- '680: 12-bit to 4-bit comparator with latch
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- $(I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5 \text{V})$ for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74AHCT: -40°C to +85°C
 KS54AHCT: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

The '679 and '680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The '679 features an enable inpu (\overline{G}) . When \overline{G} is low, the device is enabled. When \overline{G} is high, the device is disabled and the output is high regardless of the A and P inputs. The '680 features a transparent latch and a latch enable input (E). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATIONS

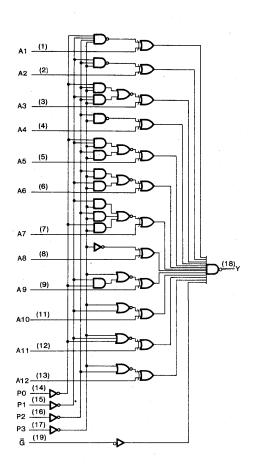
	'679	
A1	20 11 18 1 1	9
A7 7 7 A8 8 A9 9 GNC 10	14 14 13 12	P0 A12

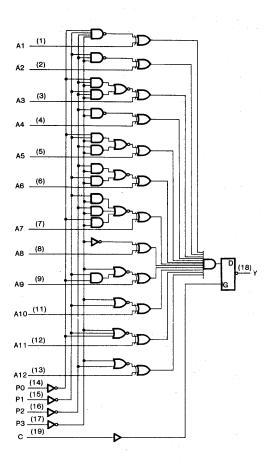
		'680		
A1	1 2 3 4 5 6 7 8 9	Ü	20 19 18 17 16 15 14 13 12	V _∞ E Y P3 P2 P1 P0 A12 A11
		4		

LOGIC DIAGRAMS

'679

'680





FUNCTION TABLE

'679	'680					INI	PUTS	CON	MON	I TO	'679	AND	'680				7 7 7	OUTPUT
G	Е	P3	P2	P1	PO	A1	A2	A3	A 4	A 5	A6	A7	A8	A9	A10	A11	A12	Y
L	н	L	L	L	L	Н	H	Н	Н	,H	Н	• Н	Н	Н	Н	н	н	L is
L	H	L	L	L	Н	L	Н	H	Н	H	Н	Н	Н	Н	Н	Н	Н	Ŀ
L	H 💚	L	L	Н	L Ì	L	L	Н	Н	H.	.H	Н	Н	Н	Н	Н	Н	L
L	Н	L	L	Н	Н	L	L	L	Н	Н	Н	H	Н	H	′ H	Н	H	L
L	Н	L.	Н	L	L	L	L	L	Ļ	Н	Н	Н	Н	Н	Н	Н	н	L
L	H	L	H	L	H	L	. L	L	L,	L	Н	Н	Н	Н	Н	Н	H	L
L	Н	L.	Н	Н	L	L	L	L	· L	L	L	Н	Н	Н	Н	Н	Н	L ''
LL	H	. L	Н	Н	Н	ıL.	L	L	L	L	L	L	Н	Н	. Н	Н	Н	L
L	н	Н	L	L	L	L	L	L	L	L	L	L.	L	Н	Н	Н	Н	L
L	H	Н	L	L	Н	L	L	L	L	L	L	L	L	L	н	н	H	L (2)
L	H ^{r €}	H.	L	Н	L	L	L	L	L	L	L	L	L	L	L	Н	H	L
L	н	Н	L	Н	Н	L	L	L	L	L	L	L	L	Ľ	L	L	Н	L
L	Н	Н	Н	Ļ	L	L	L	L	L	L	L	L	L	Н	Н	Н	L	L*
, L	н	Н	Н	L	Н	L	L	L	L	L	L	L	L	L	H	Н	L	L*
L	Н	Н	Н	H	L	L	L	L	L	L	L	L	.L	L	L	Н	L	L*
L	н	Н	Н	Н	Н	L	L	L	L	L	L	L	L	L	L	L	L	L
L	Н		All other combinations							Н								
Н			'679: Any combination							Н								
	L				-			'680	: Any	com	binati	ion						Latched

Note: These three rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for all combinations in which P=12, 13 and 14. If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change P≥9 to P=9 ... 11/13... 15, P≥10 to P=10/11/14/15, and P≥11 to P=11/15.

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t_r, t_r Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
	<u> </u>		Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V _{CC} 4.2	V _{CC} −0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	IIN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current		per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t, t <2 ns), AHCT679

Characteristic	Symbol	Conditions†				KS54 T _a = -55°C V _{CC} = 5.0	Unit	
			Тур	Min	Max	Min	Max	<u> </u>
Propagation Delay, Any P to Y	t _{PLH}	C _L =50pF C _L =150pF	18 21		30 35		36 42	ns
	t _{PHL}	C _L =50pF C _L =150pF	18 27		30 35		36 42	113
Propagation Delay,	tpLH	C _L =50pF C _L =150pF	16 19		26 31		31 37	ns
Any A to Y	tpHL	C _L =50pF C _L =150pF	16 19		26 31		31 37	
Propagation Delay.	tpLH	C _L =50pF C _L =150pF	12 15		19 24		23 29	ns
G to Y	t _{PHL}	C _L =50pF C _L =150pF	12 15		19 24		23 29	
Input Capacitance	CiN		5					pF
Power Dissipation Capacitance*	CPD						,	pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² fin.

[†] For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input tr., tr<2 ns), AHCT680

Characteristic	Symbol	Conditions [†]	$\begin{array}{c c} & & KS74AHCT \\ & & & V_{CC} = 5.0V \\ \end{array} \\ \begin{array}{c c} & & KS74AHCT \\ & & & V_{CC} = 5.0V \\ \hline \end{array} \\ \begin{array}{c c} & & & & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ \end{array}$				KS54AHCT T _a =-55°C to +125°C V _{CC} =5.0V± 10%		
-			Тур	Min	Max	Min	Max		
Propagation Delay,	tеин	C _L =50pF C _L =150pF	21 24		35 40		42 48	ns	
Any P to Y	t _{PHL}	C _L =50pF C _L =150pF	21 24		35 40		42 48	113	
Propagation Delay,	tецн	C _L =50pF C _L =150pF	18 21		30 35		36 42	ns	
Any A to Y	t _{PHL}	C _L =50pF C _L =150pF	18 21		30 35		36 42	113	
Propagation Delay,	tеин	C _L =50pF C _L =150pF	13 16		21 26		25 31	ns	
E to Y	tenL	C _L =50pF C _L =150pF	13 16		21 26		25 31		
Set up Time An before E	tsu .		6	10		12		ns	
Hold Time An after E	th	`	0	0		0		ns	
Input Capacitance	CiN		5					pF	
Power Dissipation Capacitance*	C _{PD}							рF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^z f_{in.}

[†] For AC switching test circuits and timing waveforms see section 2.

- Compares Two 8-Bit Words
- '682 has 20kΩ pullup Resistors on the Q inputs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- ($I_{OL} = 24 \text{ mA} \bigcirc V_{OL} = 0.5V$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

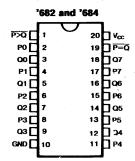
DESCRIPTION These magnitude comp

These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide $\overrightarrow{P=Q}$ and $\overrightarrow{P>Q}$ outputs. The '682 features 20-kQ pullup termination resistors on the Q inputs for analog or switch data.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATIONS



	'686	
P>Q C G1 C P0 C Q6 C P1 C Q1 C	1 2 3 4 5	24
NC [P2 [Q2 [7 8 9 10 11	18 Q6 17 P6 16 Q5 15 P5 14 Q4 13 P4

NC-No internal connection

FUNCTION TABLE

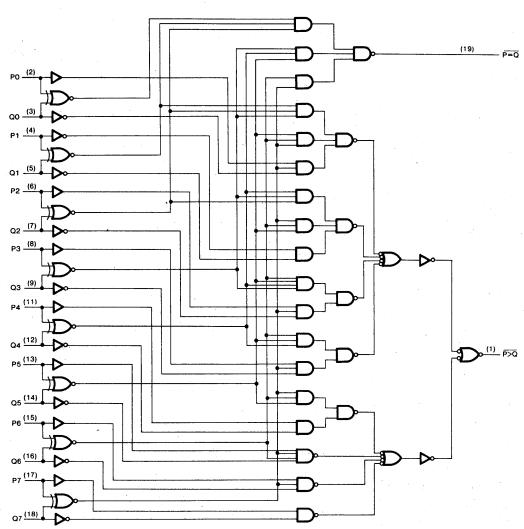
	NPUTS	OUTE	этк	
DATA	ENA	BLES	00	0.0
P, Q	Ğ1	Ğ2	P=Q	P>Q
P=Q	L	Х	L	Н
P>Q	Х	L	н	L
P <q< td=""><td>х</td><td>X</td><td>н</td><td>н</td></q<>	х	X	н	н
P=Q	Н	X	Н	н
P>Q	х	Н	н	Н
X	Н	Н	н	. H

NOTES: 1. The last 3 lines of the function table apply only to the device having enable inputs, i.e., '686.

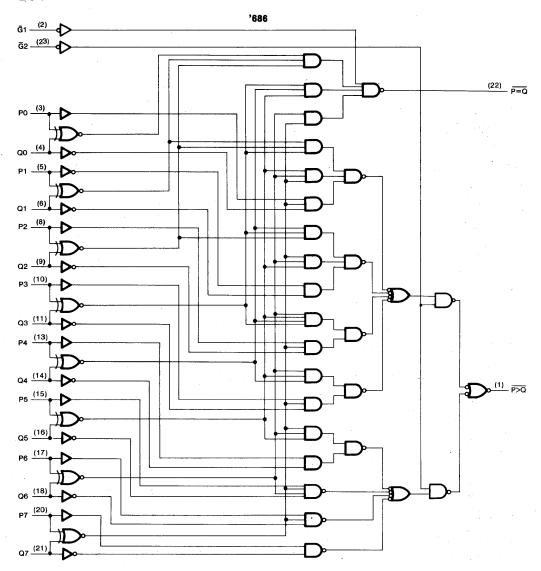
 The P<Q function can be generated by applying the P=Q and P>Q outputs to a 2-input NAND gate.

LOGIC DIAGRAMS

'682 or '684



LOGIC DIAGRAMS (continued)



Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, VIN, VOUT ... OV to VCC Operating Temperature

KS74AHCT: -40°C to +85°C Range KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, tr, tf Max 500 ns Unused inputs must always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Parameter	Symbol	Symbol Test Conditions T _a =25°C T		KS74AHCT T _a = -40°C to +85°C	54AHCT T _a = -55°C to +125°C	Unit		
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	v	
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v	
Minimum High-Level Output Voltage (Totem-pole Outputs)	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.93	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	٧	
Maximum Low-Level Output Voltage (All Outputs)	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	О	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
Maximum Input Current, ('682 Q Inputs)		V _{CC} =Max V _{IN} =2.7V V _{IN} =0.4V		-0.2 -0.4	-0.2 -0.4	-0.2 -0.4	mA	
Maximum Input Current (All other Inputs)	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА	
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ	
Maximum Quiescent	lcc	For '682: V _{IN} =GND (Q0-Q7) V _{IN} =V _{CC} or GND (all other inputs)		3.5	3.5	3.5	mA	
Supply Current		For '684 and '688 V _{IN} =V _{CC} or GND I _{OUT} =0µA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND IOUT=OµA	-	2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f<2 ns), AHCT682, AHCT684, AHCT686

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V	Ta = -40°	AHCT C to +85°C 0V±10%	$T_a = -55^{\circ}C$	AHCT to +125°C 0V± 10%	Unit
			Тур	Min	Max	Min	Max	
Maximum Propagation Delay,	tpLH	C _L =50pF C _L =150pF	17 16		22 27		27 33	ns
P or Q to P=Q	t _{PHL}	C _L =50pF C _L =150pF	17 16		22 27		27 33	113
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	16 19		27 32		32 38	ns
P or Q to P>Q	tpHL	C _L =50pF C _L =150pF	16 19		27 32		32 38	110
Propagation Delay,	tplH	C _L =50pF C _L =150pF	10 13		16 21		19 25	ns
G1 to P=Q ('686 Only)	tpHL	C _L =50pF C _L =150pF	10 13	-	16 21		19 25	113
Propagation Delay,	t _{PLH}	C=50pF C _L =150pF	11 14		19 24		23 29	ns
G2 to P <q ('686="" only)<="" td=""><td>t_{PHL}</td><td>C_L=50pF C_L=150pF</td><td>11 14</td><td></td><td>19 24</td><td></td><td>23 29</td><td>113</td></q>	t _{PHL}	C _L =50pF C _L =150pF	11 14		19 24		23 29	113
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	CPD							рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in.}

[†] For AC switching test circuits and timing waveforms see section 2.

WIRE!

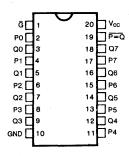
- Compares Two 8-Bit Words
- Choice of Totem-pole ('688) and open-drain ('689) outputs ('688 is identical to '521)
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · High output drive
 - ($I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

INI	PUTS	ОИТРИТ		
DATA P, Q	ENABLE G	P=Q		
P=Q	L	L		
P>Q	L	Н		
P <q< td=""><td>L</td><td>Н</td></q<>	L	Н		
Х	Н	Н.		

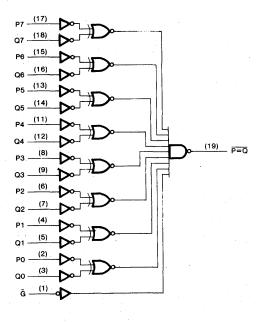
DESCRIPTION

These identity comparators perform comparisons of two 8-bit binary or BCD words. The outputs of the '688 are totempole, while '688's are open-drain.

These devices provide speeus and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_i < -0.5V \text{ or } V_i > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IoK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

1100011111101	idod opolating oonattono
Supply Voltage,	V _{CC} 4.5V to 5.5V
DC Input & Out	out Voltages*, VIN, VOUT OV to VCC
Operating Temp	erature
Range	KS74AHCT: -40°C to +85°C
100	KS54AHCT: -55°C to +125°C
Input Rise & Fal	l Times, t _r , t _f Max 500 ns
•	must always be tied to an appropriate logic

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	τ,	=25°C	KS74AHCT Ta = -40°C to +85°C	KS54AHCT Ta = -55°C to +125°C		
			Тур		Guaranteed Lim	its		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage ('688 only)	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1 3.7	v	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	lın	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА	
Maximum Output Leakage Current ('689 only)	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT688

Characteristic	Symbol	T _a = 25°C V _{CC} = 5.0V		KS74AHCT T _a = -40°C to +85°C V _{CC} =5.0V±10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
	te.		Тур	Min	Max	Min	Max	
Propagation Delay,	tpLH	C _L =50pF C _L =150pF	12 15		19 24		23 29	ns
P to P=Q	t _{PHL}	C _L =50pF C _L =150pF	12 15		19 24		23 29	113
Propagation Delay, Q to P=Q	tpLH	C _L =50pF C _L =150pF	12 15		19 24		23 29	ns
	t _{PHL}	C _L =50pF C _L =150pF	12 15	\ \	19 28		23 29	
Propagation Delay,	t _{PLH}	C; =50pF	11 14		17 22		20 26	ns
G to P=Q	t _{PHL}	C _L =50pF C _L =150pF	11 14		17 22		20 26	
Input Capacitance	CiN		5					рF
Power Dissipation Capacitance*	C _{PD}						1.0	рF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT689

Characteristic	Symbol	$\begin{array}{c} T_a = 25^{\circ}C \\ \text{Conditions}^{\dagger} & V_{CC} = 5.0V \end{array}$		KS74AHCT T _a = -40°C to +85°C V _{CC} =5.0V±10%		KS54AHCT T _a = -55°C to +125°C V _{CC} =5.0V± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	19 22		28 33		33 39	ns
P to P=Q	tpHL	C _L =50pF C _L =150pF	14 17		23 28		28 34	115
Propagation Delay,	tрин	C _L =50pF C _L =150pF	19 22		28 33		33 39	ns
Q to $\overline{P} = \overline{Q}$	t _{PHL}	C _L =50pF C _L =150pF	14 17		23 28		28 34	115
Propagation Delay,	telH	C _L =50pF C _L =150pF	16 19		23 28		27 33	ns
G to P=Q	tpHL	C _L =50pF C _L =150pF	11 16		18 23		22 28	,,,
Input Capacitance	CiN		5					pF
Power Dissipation Capacitance*	C _{PD}							pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

[†] For AC switching test circuits and timing waveforms see section 2.

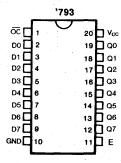
- I/O port configuration enables output data back onto input bus
- . Latch ('793) and and Register ('794) options
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current
 - $(l_{OL} = 24 \text{ mA } @ V_{OL} = 0.5V)$ for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

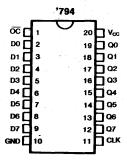
KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS





DESCRIPTION

These are 8-bit latches/registers that allow temporary storage and retrievel of data on a bus. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in a '793 or '794, for verification and/or updating.

The Data is loaded in the registers on the positive-edge of the clock (CLK) for the '794. The data is passed through the '793 when E is high, and it is latched when E goes low. The output control (\overline{OC}) is used to erable data on the D0-D7 pins. when \overline{OC} is low the output of the latches/registers is enabled on D0-D7, enabling D as an output bus so that the host can perform a read operation. When \overline{OC} is high, D0-D7 are inputs to the latches/registors configuring D as an input bus.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

793

E	ŌĊ	Q	D
L	L	Q ₀ **	Output, Q
L	н	Q ₀ **	Input
H†	L	D*	Output, Q*
н	н	D	Input

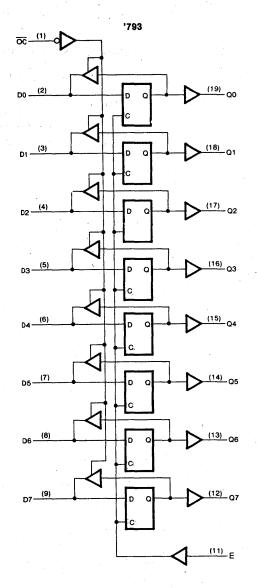
- In this case the output of the latch feeds the input, and a "race" condition results.
- * * Qo represents the previous "latched" state.
- † This transition is not a normal mode of operation and may produce hazards.

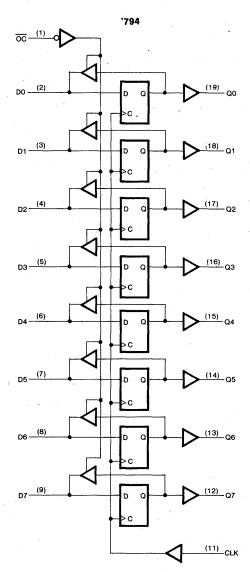
'794

CLK	ŌĊ	Q	D
L or H.or ↓	L	Qo	Output, Q
L or H or ↓	н	Qo	Input
1	L	Qo	Output, Q*
t	н	D	input

 In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Qo.

LOGIC DIAGRAMS





Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
Vcc or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage V	loc	4.5V to 5.5V
DC Input & Outpu	it Voltages*, V _{IN} ,	Vout OV to Vcc
Operating Temper	ature	
Range	KS74AHCT:	-40°C to +85°C
	KS54AHCT:	-55°C to +125°C
Input Rise & Fall	Γimes, t _r , t _f	Max 500 ns
	ust always be tied t ther V _{CC} or GND)	o an appropriate logic

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	1	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур	Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} −0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	+ ±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (t::put tr, te<2 ns), AHCT793, AHCT794

Characteristic		Symbo	voli Conditional M5 fivi		Ta=-40°	KS74AHCT T _a =-40°C to +85°C V _{CC} =5.0V±10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	
				Тур	Min	Mex	Min	Max	1
Maximum (('794 only)	Operating Frequency	t _{max}	C _L =50pF	60	40		35		MHz
Propagation	a Dologo	фин	C _L =50pF C _L =150pF	10 13		16 21		19 25	
	('793 only)	teral	C _L =50pF C _I =150pF	10 13		16 21		19 25	ns
Proposition	- Colore		C _L =50pF C _I =150pF	12 15		20 25		24 30	
Propagation Delage CLK/E to Any Q			C _L =50pF C _I =150pF	12 15		20 25		24 30	ns
Enable Tim	Fachla Van		RL=1kQ CL=50pF	11 14		18 23		22 28	
OC to D		tezı	(C=Low for '793) CL=50pF CL=150pF	11 13		18 23		22 28	ns
Disable Tim	ne	tenz	R _L =1KΩ	11		18		22	
OC to D		terz	C _L =50pF (C=Low for '793)	11		18		22	ns
Pulse Widtl CLK/C High		tw		9	. 14		19		ns
Setup time	D before E4 ('793)	tsu		6	10		12		ns
Setup time	D before CLKt('794)			10	15		20		l IB
Hold Time D after E + ('793) D after CLK† ('794)		tn		9	10		12		ns
		- un		0	0		0		
Input Capci	itance	CIN	•	5					рF
Output Cap	nacitance	Cour	OC=GND	10					рF
Power Diss	ipation Capacitance*	CPD							ns

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

- Functionally Equivalent to AMD's Am29821 and Am29822
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up-High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · 3-State outputs with high drive current
- (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V

(Available Tape & Reel), standard DIPs.

 Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

• Package options include "small outline" packages

PIN CONFIGURATIONS

7821								
oc d	, ~	24	Ь	V _{CC}				
10 🗖	2	23	Ь	1Q				
2D 🗆	3	22	þ:	2Q				
3D 🗖	4	21	þ:	3Q				
4D 🗖	5	20	þ.	4Q				
5D C	6	19	Ь	5Q				
6D 🗆	7	18	Ь	6Q				
7D 🗖	8	17	Ь	7Q				
8Ď C	9	16	Ь	BQ				
9D [10	15	Ь	9Q				
100 🖸	11	14	Ь	10Q				
GND [12	13	Ь٩	CLK				
	·		•					

٠,	'822		
οc c		24	bv∝
1Ď C	2	23	þ 1Q
2D 🗀	3	22	D 2Q
3Ď [1	21	D 300
4Ď C	-	20	140
5Ď C		19	D 5Q
6D C	1	18	3 60
7Ď C	8	17] 7Q
8Ď €	9	16	3 8Q
.9Ď 🛚	10	15] 9Q
10Ď (11	14	100
CINIÓ 🗆	12	13	р стк

DESCRIPTION

These 10-bit bus-interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

All of the flip-flops are edge-triggered and D-type. On the positive transition of the clock the Q outputs on the '821 will be true, and on the '822 will be complementary to the data input.

A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control (\overline{OC}) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

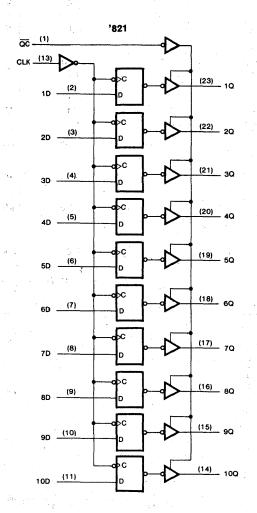
(Each Flip-Flop)

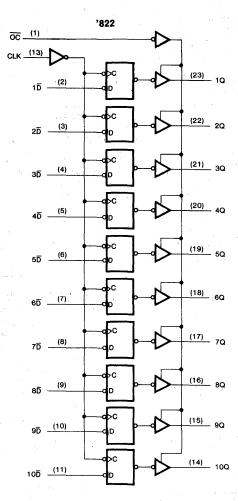
			'821	
		Inputs	Output	
	<u>oc</u>	CLK	D	Q
	L	t	Н	Н
252	L	· †	L	L
	Ł	L	X	Q ₀ Q ₀
	L	Н	X	
	H	X	X	Z

'822

	Inputs	Output	
ŌĈ	CLK	Ď	Q
L	Ť	Н	L
L	†	L	н
Ĺ	L	X	Q ₀
L	н	- X	Q ₀
H	X	X	Z

LOGIC DIAGRAMS





KS54AHCT **821/822** KS74AHCT

10-Bit Bus Interface Flip-Flops with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	Vcc	4.5V to 5.5V
DC Input & Outp	out Voltages*, V _{IN} ,	Vout OV to Vcc
Operating Temp	erature	•
Range	KS74AHCT:	-40°C to +85°C

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	=25°C	$\begin{aligned} \text{KS74AHCT} \\ \text{T}_{a} = -40^{\circ}\text{C to } +85^{\circ}\text{C} \end{aligned}$	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	Vol	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT821, AHCT822

Characteristic	Symbol	Conditions† V _{CC}		T _a = 25°C V _{CC} = 5.0V	K\$74AHCT Ta = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Maximum Operating Frequency	f _{max}	C _L =50pl	F,	50	35		30		MHz
Propagation Dolay		C _L =50pl		13 16		15 20		18 23	
Propagation Delay CLK to any Q	*	C _L =50pF C _L =150pF		13 16		15 20		18 23	ns
Output Enable Time,	tpzL	-R _L =1kΩ	C _L =50pF C _L =150pF	11 14	-	18 23		22 28	ns
OC to any Q	t _{PZL}		C _L =50pF C _L =150pF	11 14		18 23		22 28	
Output Disable Time,	t _{PHZ}	$R_L = 1 k\Omega$		13		18		22	ns
OC to any Q	tpLZ	C _L =50pF		13		18		22	1115
Pulse Width, CLK High or Low	t _w		,	9	15		18		ns
Setup Time, Data before CLK†	tsu			9	14		17		ns
Hold Time, Data after CLK†	th			. 0	0		0		ns
Input Capacitance	Cin			5					pF
Output Capacitance	Cour	Output D	isabled	10					рF
Power Dissipation Capacitance* (per stage)	C _{PD}	ÖC≃Vcc ÖC≃GNI	; D	5 30					pF pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.



[†] For AC switching test circuits and timing waveforms see section 2.

- Functionally Equivalent to AMD's Am29823 and Am29824
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up-High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- ($I_{OL} = 24$ mA @ $V_{OL} = 0.5V$) for direct bus interface • Inputs and outputs interface directly with TTL, NMOS
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

and CMOS devices

KS54AHCT: -55°C to +125°C

Package options include "small outl

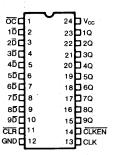
 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS

'823

ōc d ₁	24 V _{CC}
1DC 2	23 🗖 1Q
2D 口 3	22 🗖 2Q
3D 🗖 4	21 🗖 3Q
4D 🗖 5	20 🗖 4Q
5D 口 6	19 月 5Q
6D 🗖 7	18 🗖 6Q
7D 口 8	17 🗖 7Q
8D 🗖 9	16 🗖 80
9D 🗖 10	15 🗖 9Q
CLR C 11	14 CLKEN
GND 12	13 CLK

'824



DESCRIPTION

These 9-bit bus interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

With the clock enable ($\overline{\text{CLKEN}}$) low, the D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high will disable the clock buffer, thus latching the outputs. The '823 has noninverting D inputs and the '824 has inverting $\overline{\text{D}}$ inputs. Taking the $\overline{\text{CLR}}$ input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input (\overline{OC}) can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

'823

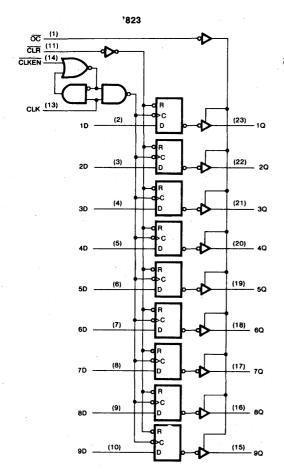
	INPUT						
ŌC	Q						
L	L	X	X	Х	L		
L	, H	L	†	Н	н		
L	. H	L	↑	L	L		
L	Н	Н	X	X	· Q ₀		
Н	X	X	X	X	· Z		

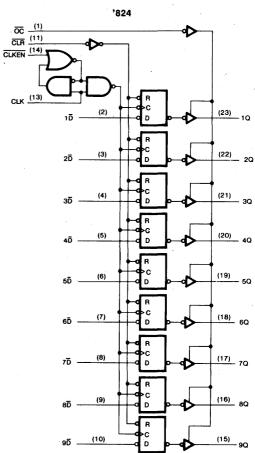
'824

		OUTPUT			
ŌC	CLR	Q			
L	Ĺ	Х	Х	Х	L
L	Н	· L	↑	Н	L
L	Н	. L	↑	L	H
L	Н	Н	X	Χ	Q_0
Н	X	X	X	Х	Z



LOGIC DIAGRAMS





KS54AHCT **823/824** KS74AHCT

9-Bit Bus Interface Flip-Flops with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

Storage Temperature Range, T_{stg}...-65°C to +150°C Power Dissipation Per Package, P_d†......500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	• • • • • • • • • • • • • • • • • • • •
Supply Voltage, Vc	c 4.5V to 5.5V
DC Input & Output	Voltages*, VIN, VOUT OV to VCC
Operating Temperat	ure
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall Tir	mes, t_r , t_f Max 500 ns
Unused inputs mus	st always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	=25°C	KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Ünit				
			Тур	Typ Guaranteed Limits							
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧				
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v				
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v				
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v				
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μA				
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ				
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ				
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA				



9-Bit Bus Interface Flip-Flops with 3-State Outputs

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT823, AHCT824

Characteristic		Symbol	Conditions [†]		i ,		i i		T _a = 25°C V _{CC} = 5.0V	T. = -40°	IAHCT C to +85°C 0V±10%	T. = -55°C	AHCT to +125°C V± 10%	Unit
		ļ				Min	Max	Min	Max					
Maximum Op	erating Frequency	f _{max}	C _L =50pl	F	50	35		30		MHz				
Propagation (Delav	t _{PLH}	C _L =50pl C _L =150		17 20		19 24		23 28	ns				
CLK to any (t _{PHL}	C _L =50pl C _L =150		17 20		19 24		23 28					
Propagation CLR to Any		t _{PHL}	C _L =50pF C _L =150pF		17 20		20 25		25 31	ns				
Output Enabl	le Time,	tpzH	$R_i = 1 k\Omega$	C _L =50pF C _L =150pF	-11 14		18 23		22 28	ns				
OC to any Q		t _{PZL}		C _L =50pF C _L =150pF	11 14		18 23		22 28					
Output Disab	le Time,	t _{PHZ}	$R_L = 1 k\Omega$	$B_i = 1k\Omega$			20		25	ns				
OC to any Q		t _{PLZ}	C _L =50p	F	17		20		25	1113				
Pulse Width	CLR low	tw			9	15		18		ns				
l dide Width	CLK high or low				9	15		18						
	CLR inactive			•	9	14		17						
Setup Time before	Data	t _{su}			9	14		17		ns				
CLK†	CLKEN high or low				9	14		17						
Hold Time, CLKEN or data after CLKf		t _h			0	0		0		ns				
Input Capacit	ance	Cin			5			[.		рF				
Output Capa	citance	Cout	Output D	isabled	10				•	pF				
Power Dissip Capacitance		C _{PD}	OC=V _{CC} OC=GNI	; D	5 30					pF pF				

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in.}



[†] For AC switching test circuits and timing waveforms see section 2.

- Functionally Equivalent to AMD's Am29825 and Am29826
- Improved I_{OH} Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- 'nputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

 KSZANIOT: 4000 As a conse

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS

'825

ŌC1 □		24	Vcc
ŌC2 □		23	<u>ос</u> з
1D 🗀	3	22	1Q
2D 🗖		21	2Q
3D 🗖	5	20	3Q
4D 🗖	6	19	4Q
. 5D 🗖	7	18	5Q
6D 🗖	8	17	6Q
7D 🗖	9	16	7Q
8D 🗖	10	15	8Q
CLR	11 .	14	CLKEN
GND 🗆	12	13	CLK

'826

OC1C	\vdash	24 V _{CC}
ŌC2 □	2	23 5 oc3
1D 🗖	3	22 1 1Q
2D 🕻		21 20
3Ď ┏		20 30
4D		19 40
5D̄ □	7	18 🗖 5Q
6Ď ☐	8	17 60
7D 🗖	9	16 1 7Q
8 ⊡ □	10	15 8Q
CLR C	11	14 CLKEN
GND 🗖	12	13 CLK

DESCRIPTION

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing multi-user buffer registers, I/O ports, bus drivers and working registers.

With the clock enable ($\overline{\text{CLKEN}}$) low, all D-type edge-triggered flip-flops enter data on the low-to-high transition of the clock. Taking $\overline{\text{CLKEN}}$ high will disable the clock buffer, thus latching the outputs. The '825 has non-inverting D inputs and the '826 has inverting $\overline{\text{D}}$ inputs. Taking the $\overline{\text{CLR}}$ inputs low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

'825

	Inputs								
ÖC*	CLR	CLKEN	CLK	D	Output Q				
L	L	· X	Х	Χ	L				
L	H	L'	↑	. н	Н				
L	Н	L	↑	L	L				
L	Н	Н	Х	X	Q ₀				
Н	×	Χ	X	X	Z				

^{*} \overline{OC} = H if any of $\overline{OC}1$, $\overline{OC}2$, or $\overline{OC}3$ are high. \overline{OC} = L if all of $\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$ are low.

'826

		Inputs										
	ŌĈ⁺	CLR	CLKEN	CLK	D	a						
I	L	L	Х	Χ.	X	L						
	L	Н	L	↑	Н	L.						
1	L	Н	L	↑	Ļ	H						
ĺ	L	Н	Н	X	X	Q_0						
ŀ	Н	Χ	X	X	Χ	Z						

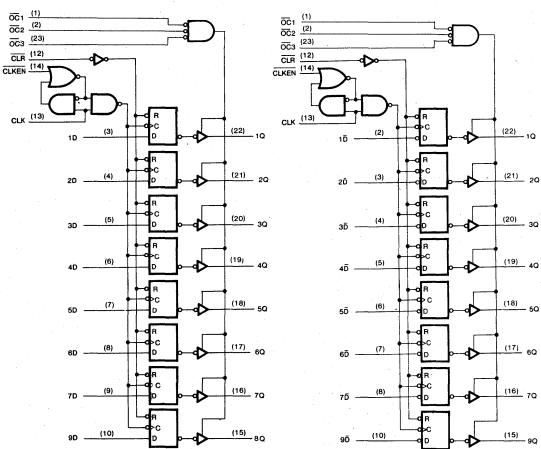
* \overline{OC} = H if any of $\overline{OC}1$, $\overline{OC}2$, or $\overline{OC}3$ are high. \overline{OC} = L if all of $\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$ are low.

LOGIC DIAGRAMS



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KS54AHCT **825/826** KS74AHCT

8-Bit Bus Interface Flip-Flops with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) + 0.5V + 0.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} −65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Meximum Detines are these culture become

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT Ta = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		its		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	ViL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC}	V _{CC} −0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	٧
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Outprit Enable =VIH VOUT=VCC or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	100	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσ	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



8-Bit Bus Interface Flip-Flops with 3-State Outputs

AC ELECTRICAL CHARACTERISTICS (Input tr. tr 2 ns), AHCT825, AHCT826

Characteristic		Symbol	Conditions [†]		mbol Conditions†		T _a = 25°C V _{CC} = 5.0V	Ta = -40°	AHCT C to +85°C 0V±10%	KS54. T _a = -55°C V _{CC} = 5.0		Unit
						Min	Min Max		Max	1		
Maximum Op	erating Frequency	f _{max}	C _L =50p	F	50	35	1.	30	1 .	MHz		
Propagation	Delav	tpLH	C _L =50p C _L =150		17 20		19 24		23 · 28	ns		
CLK to any		tpil	C _L =50p C _L =150		17 20		19 24		23 28	115		
Propagation CLR to Any		t _{PHL}		C _L =50pF C _L =150pF			19 22		23 27	ns		
Output Enab	Output Enable Time, OC to any Q		$R_L = 1 k\Omega$	C _L =50pF G _L =150pF	11 14		18 23		22 28	ns		
			112 1144	C _L =50pF C _L =150pF	11 14		18 23		22 28			
Output Disab	le Time,	tpHZ	$R_L = 1 k\Omega$	$R_l = 1 k\Omega$			18		22	ns		
OC to any Q	l i	t _{PLZ}	C _L =50p	F	13		18		22	113		
Pulse Width	CLR low	tw			9	15		18		ns		
i dido virdin	CLK high or low				9	15		18				
	CLR inactive				9	14		17				
Setup Time before	Data	tsu			9	14		17		ns		
CLK1	CLKEN high or low				9	14		17				
Hold Time, CLKEN or da	ita after CLK†	t _h			0	0		0		ns		
Input Capacit	ance	CIN			. 5					pF		
Output Capa	citance	Cout	Output D	isabled	-10					рF		
Power Dissip Capacitance		C _{PD}	ÖC=V _{CC} ÖC=GNI		5 30					pF pF		

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.



[†] For AC switching test circuits and timing waveforms see section 2.

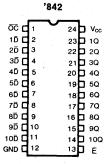
- Bus-Structured Pinout
- Provides Extra Bus Driving Latches
- Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS





DESCRIPTION

These 10-bit bus interface latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type. The '841 has noninverting data (D) inputs and the '842 has inverting (\overline{D}) inputs.

A buffered output control (\overline{OC}) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

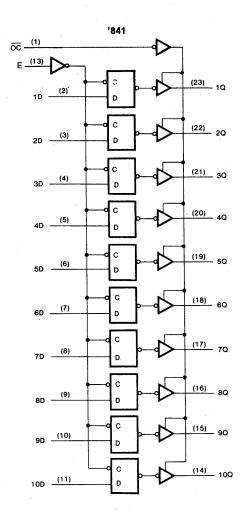
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

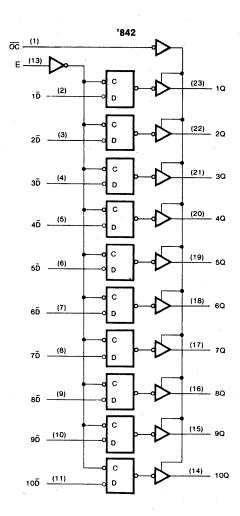
FUNCTION TABLES

put
Put
)
1
_
0
<u>-</u>
1

			842	
ĺ	lı	nputs	;	Output
	ŌC	E	D	Q
i	L	Н	Н	L
	L	Н	L	н
	· L	L	X	Q_0
ı	н	Y	Ÿ	7

LOGIC DIAGRAMS





KS54AHCT **841/842** KS74AHCT

10-Bit Bus Interface D-Type Latches with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IoK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to $+150$ °C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

necommen	ded Operating Conditions						
Supply Voltage, V	/ _{CC} 4.5V to 5.5V						
DC Input & Outpo	ut Voltages*, V_{IN} , V_{OUT} OV to V_{CC}						
Operating Tempe							
Range	KS74AHCT: -40°C to +85°C						
	KS54AHCT: -55°C to +125°C						
Input Rise & Fall	Times, t _r , t _f Max 500 ns						
Unused inputs must always be tied to an appropriate logic voltage level (either Voc or GND)							

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур	Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}	·		2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	ViL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	٧
Maximum Low-Level Output Voltage	Vol	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	l _{IN} .	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT841, AHCT842

Characteristic	Symbol	Conditions [†]		T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
					Min	Max	Min	Max	
Propagation Delay,	t _{PLH}	C _L =50pl C _L =150		10 13		13 21		19 25	ns
Data to Q	t _{PHL}	C _L =50pl C _L =150		10 13		13 21		19 25	,,,,
Propagation Delay,	t _{PLH}	C _L =50pl C _L =150		15 18		24 29		29 35	ns
E to any Q	tpHL	C _L =50pF C _L =150pF		15 18		24 29		29 35	113
Output Enable Time,	tрzн	$R_L = 1 k\Omega$	C _L =50pF C _L =150pF	13 16		18 23	and the second second	22 28	ns
OC to any Q	t _{PZL}	111 - 1142	C _L =50pF C _L =150pF	13 16		18 23		22 28	113
Output Disable Time,	t _{PHZ}	$R_L = 1 k\Omega$		13		18		22	ns
OC to any Q	tPLZ	C _L =50pF		13		18		. 22	
Pulse Width, E High	tw			12	20		25		ns
Setup Time, Data before E↓	t _{su}		- Allia	6	-10		12		ns
Hold Time, Data after E↓	th			3	5		7		ns
Input Capcitance	Cin		`	5					рF
Output Capacitance	Соит	Output D	isabled	10					рF
Power Dissipation Capacitance* (per stage)	C _{PD}	ŌC=Vcc ŌC=GNI		5 30	-				pF pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

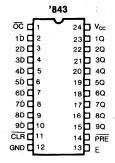
[†] For AC switching test circuits and timing waveforms see section 2.

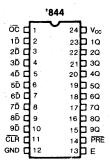
- Bus-Structured Pinout
- Provide Extra Bus Driving Latches
 Necessary for Wider Address/Data Paths or Buses
 with Parity
- · Power-Up High Impedance
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · 3-State outputs with high drive current
- ($I_{OL} = 24 \text{ mA}$ @ $V_{OL} = 0.5V$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS





DESCRIPTION

These 9-bit bus interface latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers and working registers.

The nine latches are transparent D-type. The '843 has noninverting data (D) inputs and the '844 has inverting \overline{D} inputs.

A buffered output control (\overline{OC}) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control (\overline{OC}) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

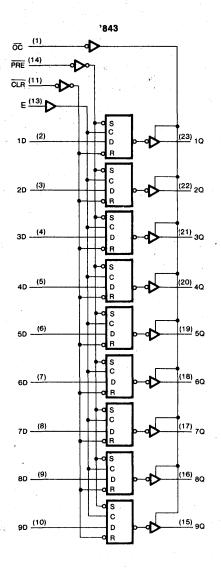
'843

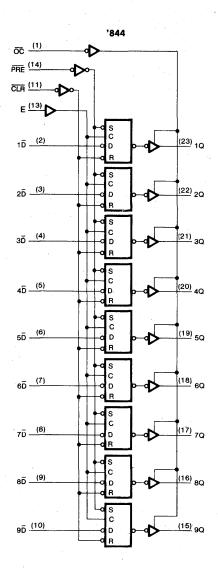
	INF	OUTPUT	I			
PRE	CLR	ŌĊ	Е	D	Q	
L	Х	L	Х	Х	Н	
Н	L	L.	Х	Χ	L	
Н	Н	L	Н	L	L	ı
Н	Н	L	H-	Н	Н	
н	Н	L.	L	Χ	Q ₀	
Х	X	Н	Х	X	Z	

'844

	IN	ОИТРИТ			
PRE	CLR	ŌĊ	E	Ď	Q
L	Х	L	X	Х	Ξ
Н	L	L	Χ	X	L
Н	Н	L	Н	L	н
н	н	L	Н	Н	L
Н	Н	L	L	Χ	Q_0
X	X	Н	Χ	Χ	Z

LOGIC DIAGRAMS





KS54AHCT **843/844** KS74AHCT

9-Bit Bus Interface D-Type Latches with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_i < -0.5V \text{ or } V_i > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output V	oltages*, VIN, VOUT OV to VCC
Operating Temperatu	ire
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall Tim	es, t_r , t_f Max 500 ns
Unused inputs must voltage level (eithe	always be tied to an appropriate logic
vollage level (ellile	I VCC OF CHICH

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta = 25°C		KS74AHCT T _a = -40°C to +85°C	KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT843, AHCT844

Characteristic	Symbol	ol Conditions†		T _a = 25°C V _{CC} = 5.0V	KS74AHCT T _a = -40°C to +85°C V _{CC} =5.0V±10%		KS54 T _a = -55°C V _{CC} = 5.0	Unit	
				Тур	Min	Max	Min	Max	į l
Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF		13 16		18 23		22 28	ns
Data to Q	t _{PHL}	C _L = 50p C _L = 150		13 16		18 23		22 28	115
Propagation Delay.	tpLH	C _L =50pi C _L =150		16 19		26 31		31 37	
E to any Q	t _{PHL}	C _L =50pF C _L =150pF		16 19		26 31		31 37	ns
Propagation Delay, PRE to Q	t _{PLH}		C _L =50pF C _L =150pF			27 32		32 38	ns
Propagation Delay, CLR to Q	t _{PHL}	CL=50pl CL=150		17 20		27 32		32 38	ns
Output Enable Time,	t _{PZL}	Rι=1kΩ	C _L =50pF C _L =150pF	11 14		18 23		22 28	ns
OC to any Q	tpzL	11[-164	C _L =50pF C _L =150pF	11 14		18 23		22 28	113
Output Disable Time,	t _{PHZ}	$R_L = 1.k\Omega$		13		18		22	ns
OC to any Q	tpLZ	C _L =50pF		13		18		22	113
Pulse Width, E High	tw			12	20		25		ns
Setup Time, Data before E↓	tsu			8	10		12		ns
Hold Time, Data after ↓	th			3	5		7		ns
Input Capacitance	CiN			5					pF
Output Capacitance	Cout	Output D	isabled	10					pF
Power Dissipation Capacitance* (per stage)	C _{PD}	ÖC=V _{CC} ÖC=GNI		5 30					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

KS54AHCT **845/846** KS74AHCT

8-Bit Bus Interface D-Type Latches with 3-State Outputs

FEATURE

- 3-state buffer-type outputs drive bus-lines directly
- Bus-structured pinout
- Provides extra bus driving latches necessary for wider address/data paths or buses with parity
- Low power consumption characteristic of CMOS devices
- 3-state outputs with high drive current (I_{OL} = 24mA @ V_{OL} = 0.5V) for direct bus interface
- Direct interface capability with TTL, NMOS and CMOS devices
- Wide operating volage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 (2744)

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to 125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS

	'845			
ŌĈ1 [<u></u>	24	Ь	Vcc
ŌĈ2 □	2	23	þ	ос з
1D 🗀	3	22	þ	1Q
2D 🗆	4	21	þ	2Q
3D 🗀	5	20	Þ	3Q ·
4D 🗀	6	19	þ	4Q
5D 🗀	7	18	þ	5Q
6D 🗀	8	17	þ	6Q
39 ⊏	9	16	Ь	7Q
8D 🗀	10	15	Ь	8Q
CLR [11	14	Ь	PRE
GND [12	13	þ	Ε

•	•	^
•	ш	n

oc1 년	<u> </u>	24	Ь	Vcc
5 62 ☐		23	_	ō c 3
100			_	10
20	2			2Q
3₫ 🗖				30
40			_	4Q
50		18	ĸ	5Q
60	8	17	Б	6Q
75 🗗		16	F	70
85	10	15	Б	8Q
ᅋ		14	Б	PRE
GND 3	12	13	Б	E
			_	_

DESCRIPTION

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type. The '845 has noninverting data(D) inputs. The '846 has inverting D inputs. Since CLR and PRE are independent of the clock, taking the CLR input low will cause the eight Q outputs to go low. Taking the PRE input low will cause the eight Q outputs to go high. When both PRE and CLR are taken low, the outputs will follow the preset condition.

The buffered output control inputs ($\overline{OC1}$, $\overline{OC2}$, and $\overline{OC3}$) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impendance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

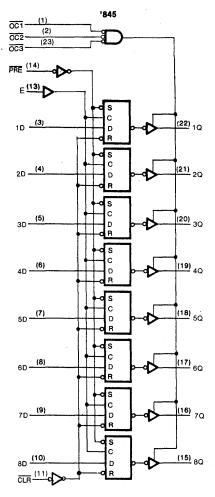
FUNCTION TABLE,845

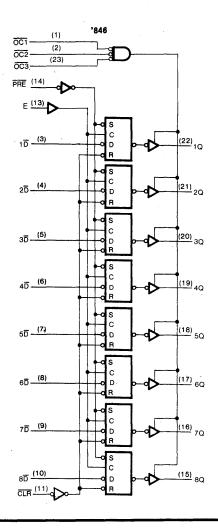
	INPUTS								
PRE	CLR	OC1	ŌC2	OC3	E	D	a		
L	Н	L	L	L	Χ	Χ	, н		
Н	L	L	L	L	Χ.	X	L		
L	L	L	L	L	Х	Х	Н		
H	Н	L	L	L	Н	L	L		
Н	Н	L	L	L	Н	Н	н		
Н	. н	L	L	L	L	Х	Q_0		
Х	Х	Х	Х	Н	Х	Х	z		
X	X	Х	Н	Х	Х	Х	z		
X	X	Н	Х	Х	Х	Х	Z		

	,	8	4	I
٠.		_		

	INPUTS							
PRE	CLR	OC1	OC2	OC3	E	Đ	Q	
L	Н	L	L	L	Х	Χ	Н	
ļ н	L	L	L	L	Х	X	L	
L	L	L	L	L	Х	Х	Н	
Н	Н	L	L	L	Н	L	' н	
H	Н	L	Ł	L	Н	Н	L	
Н	н	L	L	L	L	Х	Q_0	
X	X	Х	Х	Н	Х	X	Z	
x	Х	Х	Н	Х	Χ	Х	z	
X	Х	Н	Х	X	Х	Χ	Z	

LOGIC DIAGRAMS





KS54AHCT **845/846** KS74AHCT

8-Bit Bus Interface D-Type Latches with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IoK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, V_{IN}, V_{OUT} . . OV to V_{CC} Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, tr, tr Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	a = 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	· .
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0µA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT845

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C OV±10%	KS54 T _a = -55°C V _{CC} = 5.0	to +125°C	Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	tpLH		13		22		26	ns
E to Q	t _{PHL}		13		22		26	
Propagatio Delay	tplH		8		15		20	ns
D to Q	tent		8		15		20	
Propagation Delay CLR to Q	t _{PLH}		16		26		31	ns
	tpHL		16		26		31	
Propagation Delay	tpLH		16		26		31	ns
PRE to Q	tpHL		16		26		31	
Output Enable Time	tpzh		12		20		24	ns
OC to Q	tpzL		12		20		24	113
Output Disable Time	tpHZ		12		20		24	ns
OC to Q	tpLZ	1	12		20		24	, ,,,
Set up Time Dn before E	tsu		8	10		12		ns
Hold Time Dn after E	th		0	0		0		ns
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	CPD				-			pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT846

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	T _a = -40°C	AHCT C to +85°C DV ± 10%	$T_a = -55$ °C	AHCT to +125°C 0V ± 10%	Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	t _{PLH}		14		24		32	ns
E to Q	t _{PHL}		14		24		32	,,,
Propagation Delay	tpLH		10		17		22	ns
D̄ to Q	t _{PHL}		10		17		22	113
Propagation Delay	tplH	,	13		22		26	ns
CLR to Q	tpHL	1	13		22		26	
Propagation Delay	tpLH		13		22		26	ns
PRE to Q	tpHL	}	13		22		26	
Output Enable Time	tpzh		12		20		24	ns
OC to Q	tezu		12		20		24	113
Output Disable Time	tpHZ		12		20		24	ns
OC to Q	tpLZ		12		20		24	''3
Set up Time Dn before E	tsu		8	10		12		ns
Hold Time Dn after E	th		0	0		0		ns
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	CPD							pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

[†] For AC switching test circuits and timing waveforms see section 2.



[†] For AC switching test circuits and timing waveforms see section 2.

- Modified input structure allows voltages up to 15V
- High-Drive-current Outputs:
 IoI = 8mA @ VoL = 0.5V
- Low power consumption characteristic of CMOS
- Inputs and outputs Interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KSZANICT: --40°C to 1-85°C

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

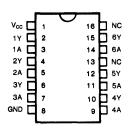
DESCRIPTION

The '4049 and '4050 have a modified input protection structure that enable them to be used as logic level translators which will convert high level logic to a low level logic while operating from the low logic supply. For example, 0-15V logic can be corverted to 0-5V logic when using a 5V supply. The modified input protection has no diode connected to $V_{\rm cc}$, thus allowing the input voltage to exceed the supply. The lower zener diode protects the input from both positive and negative static voltages. In addition the '4049 and '4050 can be used as simple buffers or inverters without level translation.

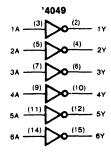
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

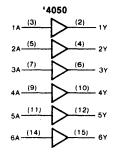


LOGIC DIAGRAMS



FUNCTION TABLE

Input A	Output Y					
	'4049	'4050				
н	L	Н				
L	Н	. L				



Absolute Maximum Ratings*

Supply Voltage Range Vcc, -0.5V to +7V
DC Input Diode Current, IIK
$(V_1 < -0.5V \text{ or } V_1 > +15.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
Vcc or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, P_d^{\dagger} 500 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_t Max 500 ns
Unused inputs must always be tied to an appropriate logic
voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT $T_a = -40$ °C to +85°C	KS54AHCT T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	Vон	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND V _{IN} =15V		±0.1	±1.0 ±10.0	±1.0 ±10.0	μΑ
Maximum Quiescent Supply Current	loc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

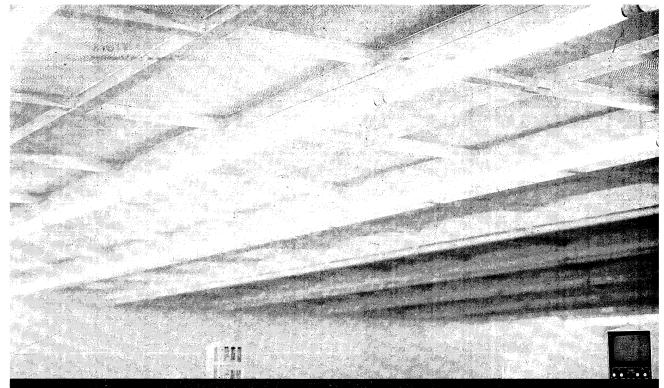
AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT4049, AHCT4050

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C OV ± 10%	KS54 T _a = -55°C V _{CC} = 5.0	AHCT to +125°C OV ± 10%	Unit
			Тур	Min	Max Min	Max		
Propagation Delay	tpLH	C _I =50pF	7		12		14	ns
	tpHL	0[=30pi	7		12		14	
Input Capacitance	CiN		5					pF
Power Dissipation Capacitance*	CPD	(per gate)	15					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-}

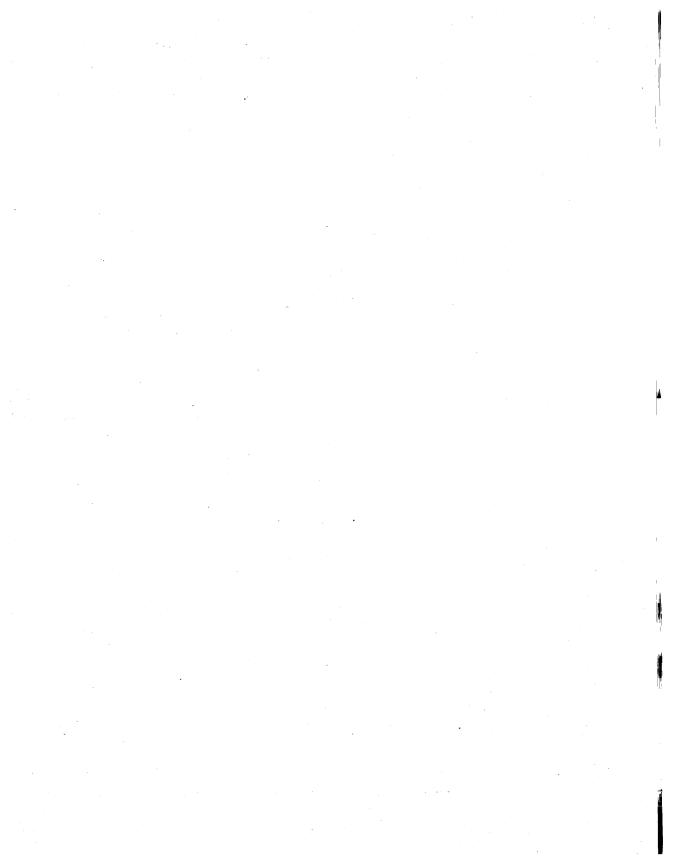
[†] For AC switching test circuits and timing waveforms see section 2.





KS54/74HCTLS DATA SHEETS 5





- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These devices contain four independent 2-input NAND gates that perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$.

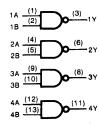
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

1A 1B | 2 13 🗖 4B 1Y 🗀 12 AA 3 2A [11 □ 4Y □.зв 2B [5 10 6 2Y [□ 3A 3Y GND [

LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inp	uts	Output
Α	В	Y
Н	Н	L
L	Χ	Н
Х	L	н

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Mauteum Dellane are those values become

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vcc	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic Sym	Symbol	Test Conditions	Τ,	= 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} =0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr. tr 6 ns), HCTLS00

Characteristic	Symbol	Conditions†	T _a = 2 V _{CC} =		KS74 HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit	
			Тур		Guaranteed	Limits		
Maximum Propagation Delay	t _{PLH}	C ₁ = 50pF	10	15	18	22	ns	
	tPHL	OL-OOP!	10	15	18	22	113	
Maximum Input Capacitance	C _{IN}		5				pF	
Power Dissipation Capacitance*	C _{PD}	(per gate)	15				рF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-}

[†] For AC switching test circuits and timing waveforms see section 2.

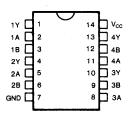


- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



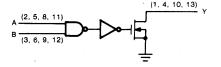
DESCRIPTION

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inp	uts	Output
Α	В	Y
Н	Н	L
L	Χ	Н
Χ	L	Н

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
Abaduka Marrianan Datinga ara Maga yakinga barrand

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, \	/cc 4.5V to 5.5V
DC Input & Outpu	it Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Tempe	
Range	KS74HCTLS: -40°C to +85°C
•	KS54HCTLS: -55°C to +125°C
Input Rise & Fall	Times, t_r , t_f Max 500 ns
Unused inputs n	nust always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Та	= 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit		
			Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v		
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Output Leakage Current	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =ΟμΑ		2.0	20.0	40.0	μΑ		
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS01

Characteristic	Symbol	Conditions [†]	T _a = :	25°C 5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay	tpLH	C _L =50pF	24	30	36	43	ns
Waximum Fropagation Delay	tPHL	R _L =1kΩ	15	20	25	30	113
Maximum Input Capacitance	C _{IN}		5				pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15				рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8mA @ V_{OL} = 0.5V
- Inputs and outputs Interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

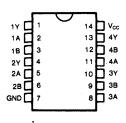
DESCRIPTION These devices contain

These devices contain four independent 2-input NOR gates that perform the Boolean functions $Y=\overline{A}+\overline{B}$ or $Y=\overline{A}+\overline{B}$.

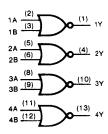
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inp	uts	Output
A	В	Y
Н	X	L
X	Н	L
L	L	Н

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ m/s}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ m/s}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V)$ ±35 m/s
Continuous Current Through
V _{CC} or GND pins ±125 m/
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mV

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	V _{CC} 4.5V to 5.5V
DC Input & Outp	out Voltages*, VIN, VOUT OV to VCC
Operating Temp	erature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic
voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit	
			Тур		Guaranteed Lim	its		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v	
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS02

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit	
			Тур		Guaranteed	Limits		
Maximum Propagation Delay	tpLH	C _L =50pF	9	15	18	22	ns	
	t _{PHL}		10	15	18	22		
Maximum Input Capacitance	CiN		5				pF	
Power Dissipation Capacitance*	C _{PD}	(per gate)	15 .				рF	

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current Outputs: $I_{OL} = 8mA @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



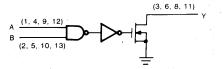
DESCRIPTION

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground

LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

(22011 2210)						
Inputs		Output				
Α	В	Y -				
Н	Н	L .				
L	Χ	H				
X	L	н				

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
A AL A A A A B B B B B B B B B B B B B B

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Input Rise & Fall Times, t_r , t_f Max 500 ns Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	= 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin $V_1=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr 46 ns), HCTLS03

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} =5.0V±10%	KS54HCTLS $T_a = -55^{\circ}\text{C to } +125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay	tpLH	$C_L=50pF$ $R_L=1k\Omega$	24	28	30	38	ns
Waximum Fropagation Belay	t _{PHL}		15	28	30	38	1113
Maximum Input Capacitance	C _{IN}		5				pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15				pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-}

[†] For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- . Low power consumption characteristic of CMOS
- High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

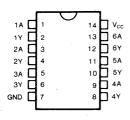
DESCRIPTION

These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$

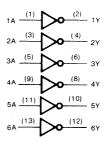
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Inverter)

,,	
Input	Output
Α	Y
н .	L
L	. н

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage, Vo	c	 4.5V	to 5.5V
DC Input & Output			
Operating Tempera	ture .		
· · ·	MOTAL OTLO	 00 1-	

Range KS74HCTLS: -40°C to +85°C

 $\label{eq:KS54HCTLS:} -55^{\circ}\text{C to } +125^{\circ}\text{C}$ Input Rise & Fall Times, t_{r}, t_{t}, \ldots Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T _a = -55°C to +125°C	Unit	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	<	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1	V _{CC} -0.1 3.7	v	
Maximum Low-Level Output Voltage	. V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND	i	±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0µA		2.0	20.0	40.0	μΑ	
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input tr., tr 66 ns), HCTLS04

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54 HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay	t _{PLH}	C _L =50pF	9	15	18	22	ns
Maximum Fropagation Belay	t _{PHL}	0[-30pi	10	15	- 18	22	
Maximum Input Capacitance	CIN		5				pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15				pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in.}

[†] For AC switching test circuits and timing waveforms see section 2.



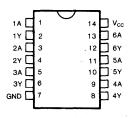
[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS7AHCTIS: -40°C to +85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



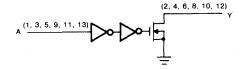
DESCRIPTION

These devices contain six independent inverters with opendrain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



FUNCTION TABLE

(Each Inverter)

(Eddit Involter)						
Input	Output					
A	Y					
н	L					
L L	Н					

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, V_{IN} , V_{OUT} . . 0V to V_{CC} Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r , t_t Max 500 ns Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	mbol Test Conditions		=25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit		
			Тур	Guaranteed Limits					
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v		
Maximum Low-Level Input Voltage	VIL	,		8.0	0.8	0.8	V,		
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V		
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Output Leakage Current	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ		
Maximum Quiescent Supply Current	loç	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input t_r , $t_r \!\!\! < \!\!\! < \!\!\! 6$ ns), HCTLS05

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54 HCTLS $T_a = -55^{\circ}\text{C to } +125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay	t _{PLH}	$C_L=50pF$ $R_L=1k\Omega$	24	30	36	43	ns
Waximum Propagation Belay	t _{PHL}		16	22	28	33	
Maximum Input Capacitance	CIN		5				рF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15				рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-}

[†] For AC switching test circuits and timing waveforms see section 2.



[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 Order
 - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

1A 🗖 J V_{cc} 1в 🛚 ☐ 4B 13 14 E ☐ 4A 3 12 ____ 4Y 2A [2B [⊐ зв] ЗА 2Y [GND [____ 3Y

LOGIC DIAGRAM

(Each Gate)

Inp	uts	Output
A.	В	Y
Н	Н	н
L	Χ	' L.
Х	L	L

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) + \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} −65°C to +150°C
Power Dissipation Per Package, Pdf 500 mW
and the second s

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic
voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic Sy	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	•
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	ViL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} ~0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr 6 ns), HCTLS08

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V		KS74 HCTLS $T_a = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C}$ $V_{\text{CC}} = 5.0 \text{V} \pm 10 \%$	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
	1		Тур		Guaranteed	Limits	
Maximum Propagation Delay	t _{PLH}	C ₁ = 50pF	10	15	18	22	ns
	t _{PHL}	оц-оорі	10	20	25	30	113
Maximum Input Capacitance	C _{IN}		5	-			рF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15				pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS7AHCTI S: -40°C to +85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

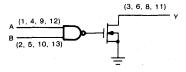
These devices contain four independent 2-input AND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

LOGIC DIAGRAM



(Each Gate)

Inputs		Output
A	В	Y
Н	Н	н
L	Χ	L
Х	L	L

Supply Voltage Range V _{CC} , −0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vo.	c 4.5V to 5.5V						
DC Input & Output Voltages*, ViN, Vout OV to Vo							
Operating Temperat	- · · · · · · · · · · · · · · · · · · ·						
	KS74HCTLS: -40°C to +85°C						
Range							
	KS54HCTLS: -55°C to +125°C						
Input Rise & Fall Tir	mes, t _r , t _f Max 500 ns						
Unused inputs mus voltage level (eith	st always be tied to an appropriate logic er V _{CC} or GND)						

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Symbol Test Conditions	T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =ΟμΑ		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mΑ

AC ELECTRICAL CHARACTERISTICS (Input tr, tr <6 ns), HCTLS09

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	$KS54HCTLS$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay	t _{PLH}	C _L =50pF	26	32	38	45	ns
Maximum 1 Topagation Delay	t _{PHL}	$R_L=1k\Omega$	16	22	28	33	
Maximum Input Capacitance	C _{IN}		5				рF
Power Dissipation Capacitance*	CPD	(per gate)	15				рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-}

[†] For AC switching test circuits and timing waveforms see section 2.



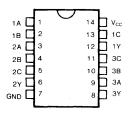
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - IOL =8 mA @ VOL =0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



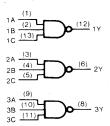
DESCRIPTION

These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y = \overline{A} \cdot B \cdot C$ or $Y = \overline{A} + \overline{B} + \overline{C}$.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

	(cii Gat	٠,
	Inputs		Output
Α	В	С	Y
Н	Н	Н	L
L	X	X	н .
Χ	L	. X	H
Χ	X	L	. н

Supply Voltage Range V _{CC} , −0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, V_{IN} , V_{OUT} . . OV to V_{CC} Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic Sy	Symbol	ool Test Conditions	T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lın	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr. tres 6 ns), HCTLS10

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V		KS74 HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay	tpLH	C _L =50pF	11	15	19	23	ns
	t _{PHL}	ОЦ-ООРІ	11	15	19	23	"
Maximum Input Capacitance	CIN		5				рF
Power Dissipation Capacitance*	CPD	(per gate)	15				pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.

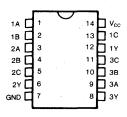


9

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: $I_{OL} = 8$ mA @ $V_{OL} = 0.5$ V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C
 KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



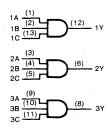
DESCRIPTION

These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{A + B + C}$.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



(Each Gate)

	Inputs	Output	
Α	В	С	Y
Н	Ή	Н	Н
L	Х	Х	L
Χ	L	X	L
Х	Χ	L	L

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vo	ос	4.5V to 5.5V
DC Input & Output	Voltages*, V _{IN}	, V _{OUT} OV to V _{CC}
Operating Tempera	ature	
Range	KS74HCTLS:	-40°C to +85°C
	KS54HCTLS:	-55°C to +125°C
Input Rice & Fall T	imae t. t.	May 500 ne

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	ditions $T_a = 25^{\circ}C$		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
					Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} = 0.1	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tie6 ns), HCTLS11

Characteristic	Symbol	Conditions†	T _a = :	25°C : 5.0V	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10^{\circ}\text{M}$	KS54 HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit	
	2	-	Тур		Guaranteed	Limits		
Maximum Propagation Delay	t _{PLH}	C ₁ =50pF	13	18	22	26	ns	
	t _{PHL}		13	18	22	26	1115	
Maximum Input Capacitance	: CIN		5				рF	
Power Dissipation Capacitance*	C _{PD}	(per gate)	15				pF	

 $^{^{\}star}$ C_{PD} determines the no-load dynamic power dissipation: $P_{D}\!=\!C_{PD}\,V_{CC^{2}}\,f_{in}.$

[†] For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- . Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

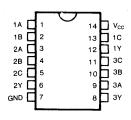
These devices contain three independent 3-input NAND gates with open-drain outputs. They perform the Boolean functions $Y = \overline{A} \bullet \overline{B} \bullet \overline{C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$.

Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

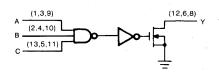
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



(Each Gate)

	Inputs	Output	
A	В	С	Y
Н	Н	Н	L
L	X	Х	Н
X	L	Х	Н
Χ	Χ	L	Н

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, $t_{r},\;t_{f}$ Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
					Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f<6 ns), HCTLS12

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74 HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay	t _{PLH}	C _L =50pF	26	32	38	45	ns
	t _{PHL}	$R_L=1k\Omega$	16	22	28	33	1 113
Maximum Input Capacitance	CiN		5				pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15				pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin-

[†] For AC switching test circuits and timing waveforms see section 2.

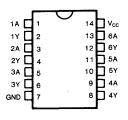


- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- . Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



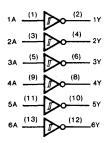
DESCRIPTION

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



(Each Inverter)

Input	Output
Α _	Y
Н	L
L	Н

•	Supply voltage Hange V_{CC} , $-0.5V$ to $+7V$
- 1	DC Input Diode Current, I _{IK}
	$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
	DC Output Diode Current, IOK
	$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±20 mA
1	Continuous Output Current Per Pin, Io
	$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
1	Continuous Current Through
	V _{CC} or GND pins ±125 mA
	Storage Temperature Range, T _{stg} 65°C to +150°C
	Power Dissination Per Package P.† 500 mW

Power Dissipation Per Package, P_d† 500 mW
 Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

Range

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Symbol Test Conditions		a=25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS $T_{a} = -55^{\circ}\text{C to } +125^{\circ}\text{C}$	Unit
	1		Тур		Guaranteed Limits		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	Vcc 4.2	V _{CC} -0.1	V _{CC} −0.1 3.84	V _{CC} -0.11	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_0=20\mu$ A $I_0=4m$ A $I_0=8m$ A	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =ΟμΑ		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	T _a =	25°C	KS74	KS74HCTLS $T_8 = -40^{\circ}C \text{ to } +85^{\circ}C$		KS54HCTLS T _a = -55°C to +125°C		
Onaracteristic	Symbol	rest Conditions	Min	Max	Min	Max	Min	Max		
Positive-Going	V _{T+}	V _{CC} =4.5V	1.2	1.9	1.2	1.9	1.2	1.9	v	
Threshold Voltage	VI+	V _{CC} =5.5V	1.4	2.1	1.4	2.1	1.4	2.1		
Negative-Going	V _T _	V _{CC} =4.5V	0.5	1.2	0.5	1.2	0.5	1.2	V	
Threshold Voltage	VI-	V _{CC} =5.5V	0.6	1.4	0.6	1.4	0.6	1.4	"	
Hysteresis	VH	V _{CC} =4.5V	0.4	1.4	0.4	1.4	0.4	1.4	v	
$(V_{T+}-V_{T-})$	VH	V _{CC} =5.5V	0.4	1.5	0.4	1.5	0.4	1.5	٧.	



[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS14

Characteristic	Symbol			25°C 5.0V	KS74 HCTLS $T_a = -40$ °C to +85°C $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits]
Maximum Propagation Delay	tpLH	C _L =50pF	15	20	25	30	ns
Waximum Fropagation Belay	tpHL		16	22	28	33	1113
Maximum Input Capacitance	CIN		5				pF
Power Dissipation Capacitance*	CPD	(per gate)	15				рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

 $I_{OL} = 8$ mA @ $V_{OL} = 0.5$ V

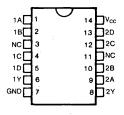
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



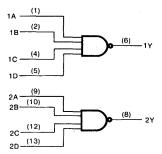
DESCRIPTION

These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



(Each gate)

	INP	UTS	OUTPUT	
Α	В	С	D	Υ Υ
Н	Н	Н	Н	L
L	Χ	Х	Χ	н
X	L	Х	X	Н
Х	Χ	L	X	Н.
X	Х	Х	L	Н

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, \	/cc	4.5V to 5.5V
DC Input & Outp	ut Voltages*, V _{IN} ,	Vout OV to Vcc
Operating Tempe		
Range	KS74HCTLS:	-40°C to +85°C

Range KS74HCTLS: -40°C to +85°C K\$54HCTLS: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	I Test Conditions	T _a = 25°C		KS74HCTLS KS54HCTLS $T_a = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}$ $T_a = -55^{\circ}\text{C} \text{ to } +12^{\circ}$		Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	. V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS20

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10^{\circ}\text{M}$	KS54 HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
		*	Тур		Guaranteed Limits		
Maximum Propagation Delay	t _{PLH}	C _L =50pF	11	.15	19	23	ns
Any Input to Y	t _{PHL}		11	15	19	23	113
Maximum Input Capacitance	CIN		5		:		рF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15		•		pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \; V_{CC}{}^2 \; f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.

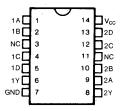


- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

(Each gate)

	INP	UTS		OUTPUT
A	В	С	D	Y
Н	Н	Н	н	Н
L	Х	Χ.	Χ	L
Х	L	Х	Χ	L
X	X	L	Х	L .
X	Χ	Х	L	L.

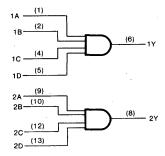
DESCRIPTION

These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y=A \cdot B \cdot C \cdot D$ or $Y=\overline{A}+\overline{B}+\overline{C}+\overline{D}$ in positive logic.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



Supply Voltage Range V _{CC} , −0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, I _{OK}
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ $\pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	•	•		
Supply Voltage, Vcc			4.5V to	5.5V
DC Input & Output	Voltages*, V _{IN} ,	Vout	OV to	Vcc
Operating Temperat	ure			
Range	KS74HCTLS:	-40	°C to +8	5°C
	KS54HCTLS:	-55°0	C to +12	5°C
Input Rise & Fall Tir	nes, t _r , t _f		Max 50	0 ns
Unused inputs mus voltage level (eith	•	•	propriate	logic

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	ymbol Test Conditions		a = 25°C	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V _{IL}			0.8	8.0	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	IIN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tres ns), HCTLS21

Characteristic	Symbol	Conditions†	T _a = :	25°C : 5.0V	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ Guaranteed Limits		Limits		
Maximum Propagation Delay	t _{PLH}	C _I =50pF	12	1.8	22	27	ns
Any Input to Y	tpHL	O[-30pi	12	18	22 ′	27	115
Maximum Input Capacitance	CIN		5				pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15				ρF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

[†] For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - IOL =8 mA @ VOL =0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

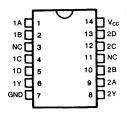
DESCRIPTION

These devices contain two independent 3-input NOR gates gates. These gates perform the Boolean fucntions $Y=\overline{A}\bullet\overline{B}\bullet\overline{C}\bullet\overline{D}$ or $Y=\overline{A}+\overline{B}+\overline{C}+\overline{D}$ in positive logic. The open-drain outputs require pull-up resistors to perform correctly. They many be connected to other open-drain outputs to implement active low wired-OR or active high wired-AND functions.

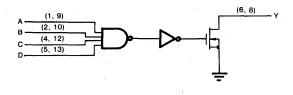
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



(Each gate)

	INP	UTS		OUTPUT
Α	В	C	D	Y
Н	Н	Н	Н	L
L	X	X	ΧÍ	н
Χ	L	Х	Χ	Н
X	Χ	L	Χ.	н
Х	Х	Χ	L	н

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	V _{CC}
Operating Tempe	rature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall	Times, $t_r, t_f \ldots Max 500 ns$
	nust always be tied to an appropriate logic either V _{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	= 25°C	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур	Guaranteed Limits		its	
Minimum High-Level Input Voltage	V _{iH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr 46 ns), HCTLS22

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74 HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10^{\circ}\text{M}$	KS54 HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
					Guaranteed	Limits	
Maximum Propagation Delay	t _{PLH}	C ₁ = 50pF	26	33	40	47	ns
Any Input to Y	t _{PHL}	OL-30bi	15	20	25	30	113
Maximum Input Capacitance	C _{IN}		5				рF
Power Dissipation Capacitance*	CPD	(per gate)	15				pF

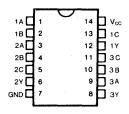
^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

[†] For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C
 KS54HCTLS: -55°C to +125°C
- Rackage options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



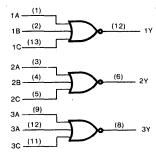
DESCRIPTION

These devices contain two independent 3-input NOR gates. They perform the Boolean functions $\overline{Y=A+B+C}$ or $Y=\overline{A}\bullet\overline{B}\bullet\overline{C}$ in positive logic.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



(Each Gate)

Į.	NPUT	s	OUTPUT
Α	В	С	Υ
Н	Х	Х	L
Χ	Н	X	L
Χ	X	Н	L
L	, F	· L	н

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I _{OK}
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ $\pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) = \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

		9
Supply Voltage, Vo	c	4.5V to 5.5V
DC Input & Output	Voltages*, V _{IN} ,	V_{OUT} OV to V_{CC}
Operating Tempera	iture	
Range .	KS74HCTLS:	-40°C to +85°C
	KS54HCTLS:	-55°C to +125°C
Input Rise & Fall T	imes, t_r , t_f	Max 500 ns
Unused inputs mu voltage level (eitl	•	to an appropriate logic

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т	a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55$ °C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	· l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	^

AC ELECTRICAL CHARACTERISTICS (Input tr, tie6 ns), HCTLS27

Characteristic	Symbol	Conditions†	Conditions $\begin{bmatrix} T_a = 25^{\circ}C \\ V_{co} = 5^{\circ}DV \end{bmatrix}$ $T_a = -40^{\circ}C$ to $+85^{\circ}C$ $T_a = -40^{\circ}C$		KS54 HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit			
* 1.					Тур		Guaranteed	Limits	
Maximum Propagation Delay	tpLH	C ₁ = 50pF	.11	15	19	23	ns		
Any Input to Y	t _{PHL}	OL=30pi	13	15	19	26	113		
Maximum Input Capacitance	C _{IN}		5				рF		
Power Dissipation Capacitance*	C _{PD}	(per gate)	15				рF		

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

[†] For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

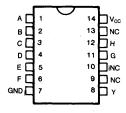
The '30 contains a single 8-input NAND gate. It performs the boolean functions (in positive logic):

Y=Ā·B·C·D·Ē·F·G·H Y=Ā+B+Ĉ+Ď+Ē+F+Ğ+Ĥ

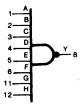
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



Inputs A Through	H	Output Y
All Inputs	Н	L
One or more inputs	L	H

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

11CCOIIIIIC	nueu operanny contantons
Supply Voltage,	V _{CC} 4.5V to 5.5V
DC Input & Out	put Voltages*, VIN, VOUT 0V to VCC
Operating Temp	perature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fa	Il Times, t_r , t_f Max 500 ns
•	must always be tied to an appropriate logic

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	ool Test Conditions		_a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٠٧	
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v	
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	v	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$		0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS30

Characteristic	Symbol	Conditions†	T _a =: V _{CC} =	25°C 5.0V	$KS74HCTLS$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10^{\circ}$	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit		
			Тур		Guaranteed	Limits			
Propagation Delay	t _{PLH}	C _L =50pF	11	15	19	22	ns		
1 Topagation Delay	t _{PHL}	CL-SUPF	11	15	19	22	1 113		
Input Capacitance	CiN		5				рF		
Power Dissipation Capacitance*	C _{PD}		15				рF		

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These devices contain four independent 2-input OR gates. They perform the Boolean functions Y = A + B or $Y = \overline{A \cdot B}$.

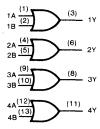
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL. NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damaged due to static discharge by internal diode clamps to V_{cc} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



(Each Gate)

Inp	uts	Output
Α	В	Υ Υ
Н	Х	Н.
Х	Н	н
L	L	L

Supply Voltage Range V_{CC} ,0.5V to +7V DC Input Diode Current, I_{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit		
•			Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1 3.7	V		
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin $V_i = 2.4V$ other inputs: at V_{CC} or GND $I_{OUT} = 0\mu A$		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input tr., tr 6 ns), HCTLS32

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{\text{CC}} = 5.0\text{V} \pm 10\%$	KS54 HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit	
			Тур		Guaranteed	l Limits		
Maximum Propagation Delay	t _{PLH}	C _L = 50pF	13	22	25	28	ns	
Waximum Fropagation Delay	t _{PHL}	OL-30pi	13	22	25	$V_{CC} = 5.0V \pm 10\%$ eed Limits	115	
Maximum Input Capacitance	C _{IN}		5				рF	
Power Dissipation Capacitance*	C _{PD}	(per gate)	15				рF	

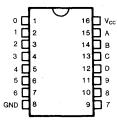
^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}

[†] For AC switching test circuits and timing waveforms see section 2.



- Full decoding of Input Logic
- . All outputs are High for Invalid BCD Conditions
- Also for application as 3-Line to 8-Line Decoders
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C
 KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

No.		Inp	uts		Outputs									
NO.	D	С	В	Α	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	Н	Н	Н	Н	Н	Н	Н	Н
1	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	н	Н
2	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Ĥ	Н	Н
3	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н
. 4	L	Н	L	L	Н	Н	Н	Н	L	Н	$_{\rm H}$	Н	Н	Н
5	L	Н	L	Н	Н	Н	H	Н	Н	L	Н	Н	Н	Н
6	L	Н	Н	L	H	Η,	Н	Н	Н	Н	L	H.	Н	Н
7	L	Н	Η	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н
8	Н	L	L	L	Н	Н	Н	н	Н	Н	Н	Н	L	Н
. 9	Н	L	L	Н	Н	Н	Н	Н	Н	Ή	Н	Н	Н	L
	Н	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
	Н	L	Н	Н	Н	Н	Н	Н	Н	Ĥ	Н	Н	Н	Н
IND CALLED	Н	Н	Ľ	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	н
INVALID	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Ή	Н	Н
	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	H	Н	Н

DESCRIPTION

The '42 decoder accepts for active-high BCD inputs and provides 10 mutually exclusive active-low outputs, as shown by logic symbol or diagram. The active-low outputs facilitate addressing other MSI units with active-low input enables.

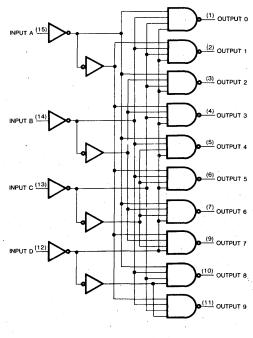
The logic design of the '42 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant input, D, produces a useful inhibit function when the '42 is used as a 1-of-8 decoder. The D input can also be used as the Data input in an 8-output demultiplexer application.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_i < -0.5V \text{ or } V_i > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

necommended operating our	
Supply Voltage, V _{CC} 4.9	5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to V _{CC}
Operating Temperature	
Range KS74HCTLS: -40°C	to +85°C
KS54HCTLS: -55°C to	o +125°C
Input Rise & Fall Times, t _r , t _f	1ax 500 ns
Unused inputs must always be tied to an appr	opriate logic

voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a =25°C		KS74HCTLS $T_a = -40$ °C to +85°C	KS54HCTLS $T_a = -55$ °C to +125°C	Unit
					Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _i =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r , $t_f \leqslant 6$ ns), HCTLS42

Characteristic	Symbol	Conditions [†]	$T_a = 25^{\circ}\text{C}$ $T_a = -40^{\circ}\text{C to } + 85^{\circ}\text{C}$ $T_a = -55^{\circ}\text{C to}$		$T_a = -40$ °C to $+85$ °C	KS54 HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
					l Limits		
Maximum Propagation Delay	t _{PLH}	C ₁ = 50pF	19	25	32	38	ns
Any Input to Y	t _{PHL}	оц-оорг	19	25	32	38 .	113
Maximum Input Capacitance	CIN		5		•		рF
Power Dissipation Capacitance*	C _{PD}	(per gate)					рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC^2} \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLES

Inputs							ut 1Y
1 A	1B	1C	1D	1E	1F	'51	'58
Н	Н	. Н	X	Х	Х	L	Н
X	Х	X	H	Н	н	L	Н
	Any o	ther co	ombina	tion		Н	L

	Inp	Outp	ut 2Y		
2A	2B	2C	2D	'51	'58
Н	н	X	Х	L	Н
Χ.	X	Н	Н	L	н
An	v other	combinati	ion	Н	L

DESCRIPTION

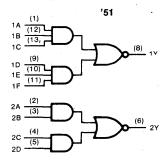
The '51 performs the following Boolean functions: $1Y = (1A \circ 1B \circ 1C) + (1D \circ 1E \circ 1F)$ $2Y = (2A \circ 2B) + (2C \circ 2D)$

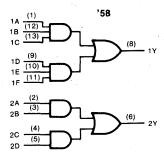
The '58 performs: 1Y=(1A•1B•1C)+(1D•1E•1F) 2Y=(2A•2B)+(2C•2D)

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAMS





Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, \	/cc	4.5V to 5.5V
DC Input & Output	ut Voltages*, V _{IN} , V	OUT OV to Vcc
Operating Tempe	rature	
Range	KS74HCTLS: -	-40°C to +85°C
	KS54HCTLS: -	55°C to +125°C
Input Rise & Fall	Times, t_r , t_f	Max 500 ns
•	nust always be tied to ither V _{CC} or GND)	an appropriate logic

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		its		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS51, HCTLS58

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		$KS74HCTLS$ $T_a = -40 ^{\circ}C \text{ to } +85 ^{\circ}C$ $V_{CC} = 5.0V \pm 10 \%$	KS54 HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit			
		İ	Тур		Guaranteed	l Limits				
Maximum Propagation Delay	t _{PLH}	C _L =50pF	13	18	23	27	ns			
Maximum i Topagation Delay	t _{PHL}		13	18	23	27 .				
Maximum Input Capacitance	CiN		5				pF			
Power Dissipation Capacitance*	CPD	(per gate)	15				рF			

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-}

[†] For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 IoL = 8 mA @ Vol = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C
 KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

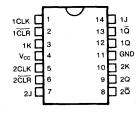
DESCRIPTION

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at $\overline{\text{CLR}}$ input resets the outputs regardless of the levels of the other inputs. When $\overline{\text{CLR}}$ is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to trise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle filp-flops by tying J and K high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

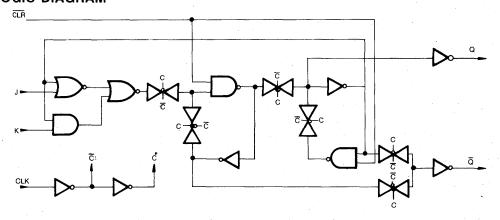
PIN CONFIGURATION



FUNCTION TABLE

	Input	s		Outp	outs
CLR	CLK	J	K	Q	Q
L	X	Х	Х	L	Н
н .	↓	L	L	Q _o	ā₀
Н	↓	Н	L ·	Н	L
Н	↓	L	Н	L	н
Н	↓	н	Н	TOG	GLE
Н	Н	X	X	Q,	\overline{Q}_{o}

LOGIC DIAGRAM



KS54HCTLS 73A

Dual J-K Negative-Edge-Triggered Flip-Flops with Clear

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I _{OK}
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	V _{CC} 4.5V to 5.5V
DC Input & Outp	ut Voltages*, V _{IN} , V _{OUT} 0V to V _{CC}
Operating Tempe	erature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall	Times, t_r , t_f Max 500 ns
•	nust always be tied to an appropriate logic either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55$ °C to +125°C	Unit
			Тур		Guaranteed Limits		1
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	*0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



Dual J-K Negative-Edge-Triggered Flip-Flops with Clear

AC ELECTRICAL CHARACTERISTICS (Input tr, tr 6 ns), HCTLS73A

Characteristic		Symbol	Conditions [†]	T _a = 1		$KS74HCTLS$ $T_a = -40 ^{\circ}C \text{ to } +85 ^{\circ}C$ $V_{CC} = 5.0V \pm 10 \%$	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
:				Тур		Guaranteed Limits		
Maximum Clock Fi	requency	f _{max}		40	30	25	21	MHz
Maximum Propaga	tion Delay,	t _{PLH}	tpLH		20	25	30	ns
CLK to Q or Q		t _{PHL}	C _L =50pF	15	20	25	30	ns
Maximum Propagation Delay, CLR to Q or Q		tplH		15	20	25	30	
		tpHL		15	20	25	30	
Minimum Setup	J or K			10	13	17	20	ns
Time before CLK↓	CLR Inactive	t _{su}		10	13	17	20	113
Minimum Hold Time, J or K after CLK↓		t _h		0	0	0	0	ns
Minimum Pulse	CLK High or Low			10	13	17	20	ns
Width	CLR Low	t _w		10	13	17	20	
Maximum Input Capacitance		C _{IN}		5				рF
Power Dissipation	Power Dissipation Capacitance*		(per flip-flop)	40				pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

 $^{^{\}dagger}$ For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- . Low power consumption characteristic of CMOS
- High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

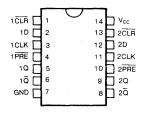
DESCRIPTION The second

These devices contain two independent positive-edgetriggered D-type flip-flops. Each flip-flop has its own data, clock, preset and clear inputs and complementary Q and Q outputs. The preset and clear inputs are active-low and operate independently of the clock. Data at the D input is transferred to the Q outputs on the positive transition of the clock, provided setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

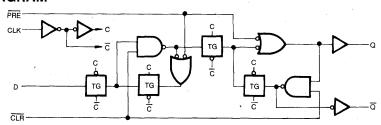


FUNCTION TABLE

	Inpu	Ou	tputs		
PRE	CLR	CLK	D	Q	ā
L	Н	X	X	Н	L
Н	L	X	Х	L	Н
L	L	X	Χ	.H*	H*
Н	Н	· 1	Н	Н	L
H	Н	↑	L	L	Н
, н	Н	L	Χ	No Ch	nange
Н	H	Н	Х	No Ch	nange
Н	Н	4	X	No Ch	nange

*Both outputs will remain high as long as PRE and CLR are low, but the output states are unpredictable if PRE and CLR go high simultaneously.

LOGIC DIAGRAM



KS54HCTLS **74A** KS74HCTLS

Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear

Absolute Maximum Ratings*

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	V _{CC}	4.5V to 5.5	5V
	out Voitages*, V _{IN} ,		
Operating Temporating	erature		
Range	KS74HCTLS:	-40°C to +85°	, C

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_t Max 500 ns
Unused inputs must always be tied to an appropriate logic
voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	Т,	a = 25°C	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr., tr<6 ns), HCTLS74A

Characteristic				T _a = 25°C V _{CC} = 5.0V		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10^{\circ}\text{M}$	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit	
				Тур		Guaranteed Li	mits		
Maximum Clock Fr	equency	f _{max}		40	30	25	20	MHz	
Maximum Propagat	tion Delay,	tpLH		18	25	31	37	ns	
CLK to Q or Q		t _{PHL}	C _L =50pF	18	25	31	37	1115	
Maximum Propagation Delay,		t _{PLH}		18	25	31	37	ns	
PRE or CLR to Q	PRE or CLR to Q or Q			18	25	31	37	1115	
Minimum Setup	Data			10	13	17	20	ns	
Time before CLK↑	PRE or CLR Inactive	t _{su}		10	13	17	20	115	
Minimum Hold Time, J or K after CLK↓		· t _h		0	0	0	0	ns	
Minimum Pulse	CLK High or Low			8	15	20	25	ns	
Width	PRE or CLR Low	- t _w		8	15	20	25	115	
Maximum Input Capacitance		CIN		5				рF	
Power Dissipation Capacitance*		C _{PD}	(per flip-flop)	40				рF	

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \, V_{CC}^2 \, f_{in}$.
† For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 8mA @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 (COMMON ASSESSED ASSESSED)

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

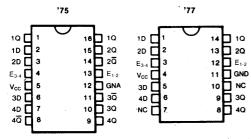
The '75 and '77 consist of 4 high-speed D-type latches that can be used as temporary storage for binary information between processing units. The '75 features complementary Q and $\overline{\rm Q}$ output while the '77 features single nail output. These devices are ideal for high component density application.

The latches are transparent: when the enable (E) is high, the Q output will follow the data input. When the enable goes low, the output latches at the level that was set up at the D-input.

These device provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

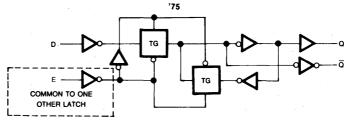


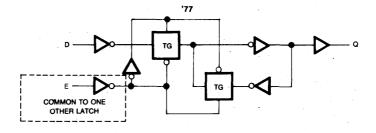
FUNCTION TABLE

Inp	uts	Outputs			
D	E	Q	Q٠		
L	Н	L	Н		
н	Н	Н	L Q₀		
Х	L	Qo	\overline{Q}_0		

*Q: '75 only

LOGIC DIAGRAM





Absolute Maximum Ratings*

Supply Voltage Range Vcc,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
(-0.5V < V _O < V _{CC} +0.5V) ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stq} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage	V _{CC} 4.5V to 5.5V
DC Input & Out	out Voltages*, VIN, VOUT OV to VCC
Operating Temp	erature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic
voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	Т,	_a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
	_		Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}	•		0.8	0.8	0.8	ν
Minimum High-Level Output Voltage	Voн	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1	V _{CC} −0.1 3.84	V _{CC} -0.1	V
Maximum Low-Level Output Voltage	Vol	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3,0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS75

Characteristic	Symbol	nbol Conditions†	T _a =25°C V _{CC} =5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
· _			Тур		Guaranteed	Limits	
Propagation Delay, E to Q or Q	tpLH	C _L =50pF	19	25	31	38	ns
	tpHL	OL-30pi	19	25	31	. 38	
Propagation Delay,	tpLH	C _L =50pF	13	21	26	32	ns
D to Q or Q	tpHL		13	21	26	32	
Data Set up Time D to E	tsu		12	15	. 18	22	ns
Data Hold Time E to D	th		0	0	0	0	ns
Input Capacitance	CiN		5				рF
Power Dissipation Capacitance*	C _{PD}						рF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS77

Characteristic	Symbol	ol Conditions†	$T_a = 25$ °C $V_{CC} = 5.0$ V		KS74HCTLS T _a = -40°C to +85°C V _{CC} =5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
	1		Тур	1	Guaranteed	Limits]]
Propagation Delay, E to Q	tpLH	C _L =50pF	13	18	23	27	ns
	t _{PHL}		13	18	23	27	
Propagation Delay,	tpLH	C _L =50pF	13	18	23	27	ns
D to Q or Q	t _{PHL}		13	18	25	27	. 113
Data Set up Time D to E	t _{SU}		12	15	18	22	ns
Data Hold Time E to D	th		0	0	0	. 0	ns
Input Capacitance	CIN		5				pF
Power Dissipation Capacitance*	C _{PD}						pF

[†] For AC switching test circuits and timing waveforms see section 2.

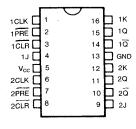
^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \, V_{CC}^2 \, f_{in}$.
† For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KSZAHCTIS = 40°C to +85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

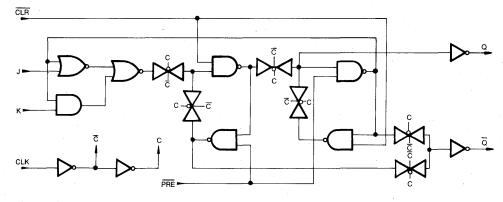
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

	ir	Outputs			
PRE	CLR	CLK	J	K	a ā
L	Н	Χ	- X	Х	H L
Н	L	X	Χ	X	L H
L	L	Χ	Χ	Χ	H* H*.
Н	Н	↓	L	· L	$Q_0 = \overline{Q}_0$
H	Н	1	Н	L	H L
Н	Н	↓	L	Н	L H
Н	Н	↓	Н	Н	TOGGLE
Н	Н	Н	Χ	Χ	$Q_0 \overline{Q}_0$

*Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

LOGIC DIAGRAM





Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V t	o +7V
DC Input Diode Current, I _{IK}	
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} +0.5V) \dots \pm$	20 mA
OC Output Diode Current, IOK	
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±	20 mA
Continuous Output Current Per Pin, Io	
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm$	35 mA
Continuous Current Through	
V _{CC} or GND pins ±1	25 mA
Storage Temperature Range, $T_{stg} \dots -65^{\circ}C$ to $+$	
Power Dissipation Per Package, Pd [†] 50	00 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to V_{CC}
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	Т	_a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T _a = -55°C to +125°C	Unit		
			Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	VIL	-		0.8	0.8	0.8	v		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	٧		
Maximum Low-Level Output Voltage	Vol	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		4.0	40.0	80.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS76A

Characteristic		Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		$KS74HCTLS$ $T_a = -40 ^{\circ}C \text{ to } +85 ^{\circ}C$ $V_{CC} = 5.0V \pm 10 \%$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Тур	Typ Guaranteed Limits			
Maximum Clock Fr	equency	f _{max}		40	30	25	21	MHz
Maximum Propagat	tion Delay,	tpLH		15	20	25	30	ns
CLK to Q or Q		`t _{PHL}	C _L =50pF	15	20	25	30	1 ns
Maximum Propagation Delay, PRE or CLR to Q or Q		tplH		15	20	25	30	ns
		t _{PHL}]	15	20	25	30	113
Minimum Setup Data		t _{su}		10	13	17	20	ns
Time before CLK↓	PRE or CLR Inactive	Lsu		10	13	17	20	115
Minimum Hold Time, J or K after CLK↓		t _h		0	0	0	0	ns
Minimum Pulse	CLK High or Low	tw		10	13	17	20	no
Width	PRE or CLR Low	ιw		10	13	17	20	ns
Maximum Input Capacitance		C _{IN}		5				рF
Power Dissipation	Capacitance*	C _{PD}	(per flip-flop)	40				рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f_{in}$.

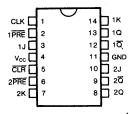
[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: IoL = 8 mA @ VoL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These parts consist of two negative-edge-triggered J-K flipflops with independent J, K and preset inputs and complementary outputs. The clear and clock inputs are common to both flip-flops. The J-K inputs are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

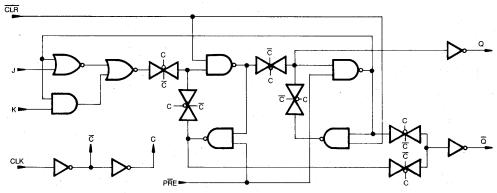
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

Γ		Ir	Outputs				
	PRE	CLR	CLK	J	K	Q	Q
Г	L	Н	Χ	X	Х	Н	L
	Н	L	X	Х	X	L	Н
	Ĺ	, L	Χ	X	X	Н٠	H٠
1	н	н	1	L	L	Q ₀	\overline{Q}_0
	Н	Н	1	H	L	Н	L
	Н	Н	↓	L	Н	L	Н
	Н	Н	↓	Н	H	TOG	GLE
	Н	н	Н	X	Χ	Q_{0}	\overline{Q}_0

^{*}Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} −65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Symbol Test Conditions		_a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}	-		0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	О	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS78A

Char	Characteristic Symbol Co		. 1		25°C 5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} =5.0V±10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
			,	Тур		Guaranteed Li	mits	
Maximum Clock Fi	requency	f _{max}		40	30	25 21		MHz
Maximum Propaga	tion Delay,	tpLH		15	20	25	30	ns
CLK to Q or Q		t _{PHL}	C _L =50pF	15	20	25	30	115
Maximum Propagation Delay, PRE or CLR to Q or Q		t _{PLH}		15	20	25	30	ns
		t _{PHL}		15	20	25	30	113
Minimum Setup J or K				10	13	17	20	ns
Time before CLK↓	PRE or CLR Inactive	t _{su}		10	13	17	20	115
Minimum Hold Time, J or K after CLK↓		t _h		0	o	D	0	ns
Minimum Pulse CLK High or Low		tw	,	10	13	17	20	
Width	PRE or CLR Low	, tw		10	13	17	20	ns
Maximum Input Capacitance		CIN		5				рF
Power Dissipation	Capacitance*	C _{PD}	(per flip-flop)	40				pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$. f_{in} . † For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



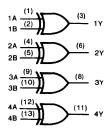
DESCRIPTION

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inp	uts	Output
A	В	Y
L.	L	L
L	Н	н
Н	L	H
н	Н	L.

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vo	c 4.5V to 5.5	٥٧
DC Input & Output	Voltages*, VIN, VOUT OV to Vo	cc
Operating Tempera		
Range	KS74HCTLS: -40°C to +85°	С
	KS54HCTLS: -55°C to +125°	С
Input Rise & Fall Ti	mes, t _r , t _f Max 500	กร
Unused inputs mu voltage level (eitl	st always be tied to an appropriate \log er V_{CC} or GND)	jic

Characteristic	Symbol	mbol Test Conditions		a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{1H}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS86

Characteristic	Symbol	Conditions [†]	T _a = :	25°C 5.0V	KS74 HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54 HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
		:	Тур		Guaranteed	l Limits]
Maximum Propagation Delay, A or B to Y (Other Input Low)	tpLH	C _L =50pF	15	20	25	30	ns
	t _{PHL}		15	20	25	30	
Maximum Propagation Delay,	t _{PLH}		18	25	31	37	ns
A or B to Y (Other Input High)	tPHL		18	25	31	37	1,3
Maximum Input Capacitance	CiN		5				рF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15				рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-1} For AC switching test circuits and timing waveforms see section 2.

- · Various counting mode.
- Function, Pin-out, speed and drive compatibility with 54/74 ALS logic family.
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: I_{OL} = 8mA @ V_{OL} = 0.5V
- Input and output interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74HCTLS: -40°C to + 85°C

KS54HCTLS: -55°C to + 125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

DESCRIPTION

These devices contain four master-slave flip-flops and addition gating to provide a divide by a counter and a three-stage binary counter for which the count cycle length is divide by five for the HCTLS90, divide by six for the HCTLS92, and divide by eight for the HCTLS93, All of these counters have a gated zero reset and the HCTLS90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four bit binary), the CKB input is connected to the QA output. The input count pulses are applied to CKA and the outputs are as described in the appropriate truth table. A symmetrical divide-by-the count can be obtained from the HCTLS90 counters by connecting the QD output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output QA.

PIN CONFIGURATION

	'90		'92		'93		
скв 🗌	1 14	ска скв	1 14	CKA CK	(B 1 1	4 CKA	
MR1	2 13	Duc nc	2 13	∏ NC MR	11 2 1	3 F NC	
MR2	3 12	O _A NC	3 12	Q _A MR	2 3 1	2 6 0,	
NC [4 . 11		4 11	□ Q _B N	c	1 🗖 😋	
V _{cc} [5 10	GND Vcc	5 10	GND V	cc 🛚 5 1	0 🔲 GND	
MS1 🗌	6 9	Q _B MR1	6 9	□ Q _c N	c □ 6	9 🗖 Q ₈	
MS2	7 8	□'Q _C MR2 [7 8	Q _D N	C 🗖 7	8 🔲 Q _C	
		5			L	_1	

FUNCTION TABLE

'90
BCD COUNT SEQUENCE
(See Note A)

Output Count Qc $\mathbf{Q}_{\mathbf{A}}$ $\mathbf{Q}_{\mathbf{D}}$ Q_B L 0 L 1 L L L н 2 L Ĺ Н L 3 L L Н 4 L Н L 5 L Н L Н 6 н 7 L н

Н

8

9

'90 BI-QUINARY (5-2) (See Note B)

Count	Output					
Count	QA	Q_D	Qc	Q_{B}		
0	Ĺ	L	L	L		
1	L	L	L	Н		
2	L	L	Н	L		
3	L	L	Н	Н		
4	L	Н	L	L		
5	Н	L	L.	L		
6.	Н	L.	L	Н		
7	. н	L	Н	L		
8	H	L	Н	н		
9	Н	Н	L	L		

'92 COUNT SEQUENCE (See Note C)

Count		Output					
Ount	QD	Qc	QB	QA			
0	L	L	L	L			
1	L	L	L	Н			
2 3	L	L	Н	Ĺ			
3	L	L	Н	Н			
4	L	Н	L	L			
5	L	Н	L	Н			
6	н	L	L	L			
7	H	L	L	Н			
8	Н	L	Н	L			
9	H	L	Н	Н			
10	Н	Н	L	Ł			
11,	Н	Н	L	Н			

'93 COUNT SEQUENCE (See Note C)

L L

L H

Count		Out	tput		
Count	QD	Qc	QB	QA	
0	L	L	L	L	_
1,	L	L	L	Н	
2	L	L	Н	L	
3) · L	L	н	Н	
4	L	н	L	· L	
5	L	Н	. L	н	
6	L	. н	Н	L	
7	L	Н	Н	Н	
8	Н -	L	L	L	
9	н	L	L	н	
10	. н	L	H	L	
11 .	н	L	H	Н	
12	н	н	L	L	
13	Н	н	L	Н	
14	Н	Н	Н	L	
15	H	Ή	н	H	

'90
RESET/COUNT TRUTH TABLE

	Reset	Output							
MR1	MR2	MS1	MS2	QD	Qc	Qв	QA		
Н	Н	L	X	L	L	L	L		
н	н	Х	L	L	L	L	L		
Х	Х	Н	Н	н	L	L	н		
X	L	X	L		COUNT				
L	Х	L	Χ	COUNT					
L	Х	Х	L	COUNT					
X	1 <u>L</u>	L	X	1	COL	JNT			

'92, '93 RESET/COUNT TRUTH TABLE

Reset	Inputs		Out	Output			
MR1	MR2	QD	Qc,	QB	QA		
Н	Н	L	L	L	L		
L	Χ	COUNT					
X	L		CO	JNT			

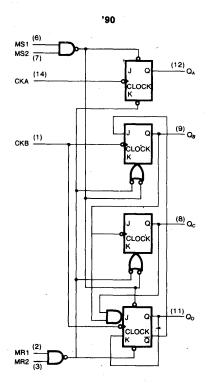
Note A: Output Q_{A} is connected to input CKB for BCD count.

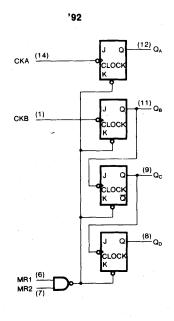
Note B: Output Q_D is connected to input CKA for bi-quinary count

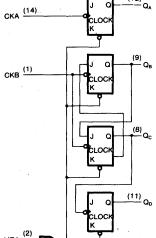
Note C: Output QA is connected to input CKB.

Note D: H=High Level, L=Low Level, X=Don't Care.

LOGIC DIAGRAMS







'93

Note: The J.K inputs shown without connection are for reference only and are functionally at a high state.

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} , −0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
 Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
or the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, ViN, Vout	OV to Vcc
Operating Temperature	

Range KS74HCTLS: $-40\,^{\circ}$ C to $+85\,^{\circ}$ C KS54HCTLS: $-55\,^{\circ}$ C to $+125\,^{\circ}$ C Input Rise & Fall Times, t_r , t_f Max 500 ns

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its]
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	ν
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_0=-20\mu\text{A}$ $I_0=-4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1	V _{CC} -0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA _.

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

AC ELECTRICAL CHARACTERISTICS (Input tr, ties 6 ns), HCTLS90

Characteristic		Symbol	Conditions†	-	25°C = 5.0V	KS74HCTLS T _A = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _A = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
			·	Тур	Limits			
Maximum Clock	CKA to QA	f _{max}	,	42	32	26	21	MHz
Frequency	CKB to Q _B	max		20	16	13	11	1411 12
Maximum Propagation	on	tpLH		10	16	20	24	ns
Delay, CKA to Q _A		t _{PHL}		12	18	23	27	113
Maximum Propagation	on	tpLH		32	48	60	72	ns
Delay CKA to Q _D		tpHL	C _L =50pF	34	48	60	72	115
Maximum Propagation		tpLH		10	16	20	24	ns
Delay CKB to QB		t _{PHL}	 -	14	21	26	32	
Maximum Propagation		tplH		21	32	40	48	
Delay, CKB to Qc		t _{PHL}		23	35	43	52	
Maximum Propagation Delay MS to Q _A , Q _D		t _{PLH}		20	30	37	45	ns
Maximum Propagation Delay MS to QB, Qc		t _{PHL}		26	40	50	60 ,	ns
Maximum Propagation Delay MR to any Q	on	t _{PHL}		26	40	50	60	ns
	CKA			12	15	18	22	
Pulse Width	СКВ	tw		24	30	36	44	ns
Tuise Width	MS	"		12	15	18	22	115
	MR			12	15	18	22	
Recovery Time MR to CKA, CKB		t _{rec}		20	25	31	37	ns
Maximum Input Capa	acitance	CiN		5				рF
Power Dissipation C	apacitance	CPD						рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input tr, tr 66 ns), HCTLS92

Characteristic		Symbol	Conditions [†]	T _A = 25°C V _{CC} = 5.0V		KS74HCTLS $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS T _A = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
				Тур		Guaranteed Limits		
Maximum Clock	CKA to QA	f _{max}	<u> </u>	42	32	26	21	MHz
Frequency	CKB to QB	imax		20	16	13	11	
Maximum Propagatio	n	tpLH		10	16	20	24	ns
Delay, CKA to QA		tpHL		12	18	23	27	113
Maximum Propagatio	n	tpLH		32	48	60	72	ns
Delay CKA to QD		tpHL	-	34	48	60	72	ns
Maximum Propagation		tpLH		10	16	20	24	ns
Delay CKB to Q _B		tpHL	C _L =50pF	14	21	26	32	113
Maximum Propagation		tpLH		10	16	20	24	ns
Delay, CKB to Qc		tpHL		14	21	26	32	ns
Maximum Propagatio	n	t _{PLH}		21	30	40	48	
Delay CKB to QD		tpHL		23	35	43	52	
Maximum Propagatio Delay: MR to Any Q	n	t _{PHL}		26	40	50	60	ns
	CKA			12	15	18	22	
Pulse Width	СКВ			24	30	36	44	
	MR			12	15	18	22	ns
Recovery Time MR to CKA, CKB		t _{rec}		20	25	31	37	ns
Maximum Input Capa	citance	CIN		5				рF
Power Dissipation Ca	pacitance	C _{PD}						рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

 $[\]ensuremath{^{\dagger}}$ For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS93

Characteristic		Symbol	Conditions	T _A = 25°C V _{CC} = 5.0V		KS74HCTLS T _A = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _A = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
		i		Тур		Guaranteed Limits		
Maximum Clock	CKA to QA	f _{max}		42	32	26	21	MHz
Frequency	CKB to Q _B			20	16	13	11	1011 12
Maximum Propagati	on	tpLH		10	16	20	24	ns
Delay, CKA to QA		tpHL		12	18	23	27	113
Maximum Propagati	on	tpLH		46	70	87	105	
Delay CKA to QD		tehr	46	70	. 87	105	ns	
Maximum Propagation		tpLH	C _L =50pF	10	16	20	24	ns
Delay CKB to QB		t _{PHL}		14:	21	26	32	
Maximum Propagation		tpLH		21	32	40	48	
Delay, CKB to Q _C		t _{PHL}		23	35	44	53	ns
Maximum Propagati	on	t _{PLH}		34	50	60	70	
Delay CKB to QD		t _{PHL}		34	50	60	70	
, , ,	Maximum Propagation Delay: MR to Any Q			26	40	50	60	ns
	CKA			12	15	. 18	22	
Pulse Width	СКВ	tw		24	30	36	44	ns
	MR	1		12	15	18	22	
Recovery Time MR to CKA, CKB		t _{rec}	,	20	25	31	37	ns
Maximum Input Cap	acitance	CIN		5				pF
Power Dissipation C	apacitance	C _{PD}						pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current Outputs:
- I_{OL} = 8mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: __40°C to _+85°C

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

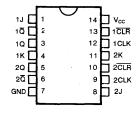
DESCRIPTION

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the $\overline{\text{CLR}}$ input resets the outputs regardless of the levels of the other inputs. When $\overline{\text{CLR}}$ is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

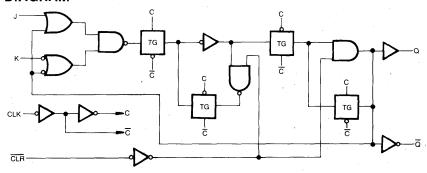
PIN CONFIGURATION



FUNCTION TABLE

	Input	Outp	outs		
CLR	CLK	J	К	Q	ā
L	X	X	Х	L	Н
H	↓	L	L	Q _o	Q.
Н		Н	L	н	Ŀ
. H	↓	L	н	L	Н
Н	↓	Н	H	TOG	GLE
Н	Н	Х	Х	Q _o	\overline{Q}_{α}

LOGIC DIAGRAM



KS54HCTLS 107A

Dual J-K Negative-Edge-Triggered Flip-Flops with Clear

Absolute Maximum Ratings*

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vo	cc 4.5V to 5.5V
DC Input & Output	Voltages*, V_{IN} , V_{OUT} OV to V_{CC}
Operating Tempera	ature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	Т	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	V _{CC}	V _{CC} -0.1	V _{CC} −0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V ₁ =2.4V other inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tie6 ns), HCTLS107A

Characteristic		Symbol Conditions†		T _a = 25°C V _{CC} = 5.0V		$KS74HCTLS$ $T_a = -40 °C to +85 °C$ $V_{CC} = 5.0V \pm 10 %$	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
				Тур		Guaranteed Li	mits	1 . [
Maximum Clock Fr	equency	f _{max}		40	30 25		21	MHz
Maximum Propagat	tion Delay,	t _{PLH}		15	20	25	30	ns
CLK to Q or Q		t _{PHL}	C _L =50pF	15	20	25	30	115
Maximum Propagation Delay, CLR to Q or Q		tpLH		15	20	25	30	ns
		t _{PHL}	1	15	20	25	30	115
Minimum Setup	J or K	t _{su}		10	13	17	20	ns
Time before CLK↓	CLR Inactive	¹su		10	13	17	20	113
Minimum Hold Time, J or K after CLK↓		th		0	0	0	0	ns
Minimum Pulse	CLK High or Low	t _w		10	13	17	20	ne
Width	CLR Low	ı w		10	13	17	. 20	ns
Maximum Input Capacitance		CIN		5		-		pF
Power Dissipation Capacitance*		C _{PD}	(per flip-flop)	40				ρF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-1} For AC switching test circuits and timing waveforms see section 2.

Dual J-K Positive Edge-Triggered Flip-Flops with Preset and Clear

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current Outputs: I_{OL}=8mA @ V_{OL}=0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V

KS54HCTLS: -55°C to +125°C

- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These devices contain two positive-edge-triggered J- \overline{K} flipflops with independent preset and clear inputs and complementary Q and \overline{Q} outputs. The present and clear inputs are active-low and operate independently of the clock Data at the J and \overline{K} inputs are transferred to the outputs on the positive transition of the clock provided setup requirements have been met. These versatile flip-flops can perform as toggel flip-flops by grounding \overline{K} and tying J high. They can also perform as D-type flops if J and \overline{K} are tied together.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

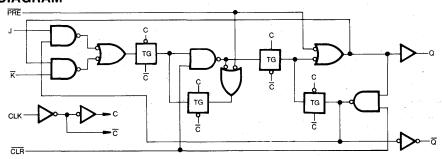
PIN CONFIGURATION

FUNCTION TABLE

	Out	puts				
PRE	CLR	CLK	J	ĸ.	Q	ā
L	Н	Х	Х	Х	н	L
H	L	Χ	Х	×	L	Н
L	L	Χ	Х	X	H*	Н*
H	Η 1	†	L	L	L	Н
Н	Н	. 🕇	Н	, L	TOG	GLE
Н	Н	†	Ĺ	Н	Q _o	ā,
Н	Н	†	Н	Н	н	L
ŀН	Н	L	X	Х	Q	ā₀

*Both outputs will remain high as long as \overline{PRE} and \overline{CLR} are low, but the output states are unpredictable if \overline{PRE} and \overline{CLR} go high simultaneously.

LOGIC DIAGRAM





Dual J-K Positive Edge-Triggered Flip-Flops with Preset and Clear

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

Power Dissipation Per Package, Pd[†] 500 mW
 Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

oa opolanny contamono
C 4.5V to 5.5V
Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
ture
KS74HCTLS: -40°C to +85°C
KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r , t_f Max 500 ns Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	τ	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its]]
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	· V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤6 ns), HCTLS109A

Characteristic		Symbol	Conditions [†]	T _a = :		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10^{\circ}\text{M}$	KS54HCTLS T _a = - 55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
				Тур	Typ Guaranteed Limits			
Maximum Clock Fre	equency	f _{max}		40	30	25	20	MHz
Maximum Propagat	ion Delay,	tpLH		18	25	31	37	ns
CLK to Q or Q		tpHL	C _L =50pF	18	25	31	37	115
Maximum Propagation Delay,		tpLH		18	25	31	37	ns
PRE or CLR to Q	or Q	t _{PHL}		18	25	31	37	1115
Minimum Setup	Data	t _{su}		10	13	17	20	ns
Time before CLK1	PRE or CLR Inactive	ı su		10	13	17	20	1115
Minimum Hold Time, Data after CLK↓		th		0	0	0	0	ns
Minimum Pulse CLK High or Low PRE or CLR Low		tw	,	8	·15	20	25	ns
] 'w		8	15	20	25	
Maximum Input Capacitance		CIN		5		-		рF
Power Dissipation Capacitance*		C _{PD}	(per flip-flop)	40				рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current Outputs:
 I_{OL} = 8mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

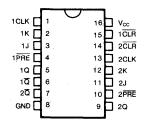
DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

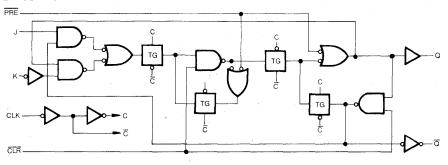


FUNCTION TABLE

-	, li		Out	outs		
PRE	CLR	CLK	J	K	Q	ā
L	Н	Х	X	Х	Н	L
Н	L	Х	Х	X	L	н
L	L	Χ	Х	Х	H*	H*.
н	Н	1 -	L	L	Q _o	Q۰
Н	- H	↓	Н	L	н	L
Н	н	↓	L	Н	L	Н
Н	Н	↓	н	н	TOG	GLE
Н	Н	Н	Χ	Χ	Q _o	\bar{Q}_{o}

*Both outputs will remain high as long as \overline{PRE} and \overline{CLR} are low, but the output states are unpredictable if \overline{PRE} and \overline{CLR} go high simultaneously.

LOGIC DIAGRAM



Absolute Maximum Ratings*

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage,	V_{CC} 4.5V to 5.5V
DC Input & Out	out Voltages*, VIN, VOUT OV to VCC
Operating Temp	erature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

[†] Power Dissipation temperature derating:
-Plastic Package (N): -12mW/°C from 65°C to 85°C

5

AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS112A

Characteristic		Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V		$KS74HCTLS$ $T_a = -40 °C to +85 °C$ $V_{CC} = 5.0V \pm 10 %$	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
			,	Тур		Guaranteed	l Limits	
Maximum Clock Fr	equency	f _{max}		40	30	25	21	MHz
Maximum Propagat	tion Delay,	t _{PLH}		15	20	25	30	ns
CLK to Q or Q		t _{PHL}	C _L =50pF	15	20	25	30	115
Maximum Propagation Delay,		t _{PLH}		15	20	25	30	ns
CLR to Q or Q	•	t _{PHL}		15	20	25	30] "3
Minimum Setup	J or K	+.		10	13	17	20	ns
Time before CLK↓	CLR Inactive	- t _{su}		10	13	17	20	115
Minimum Hold Tim Data after CLK↓	ie,	t _h		0	0	0	0	ns
Minimum Pulse CLK High or Low		tw		10	13	17	20	ns
Width	PRE or CLR Low	l w		10	13	17	20	1 113
Maximum Input Capacitance		CIN		5				рF
Power Dissipation	Capacitance*	C _{PD}	(per flip-flop)	40				рF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

[†] For AC switching test circuits and timing waveforms see section 2.

Dual Retriggerable Monostable Multivibrator with Clear

FEATURES

- Simple pulse width formula tw = 0.45RC
- . DC triggered from active HIGH or active Low inputs
- Retriggerable for very long output pulses up to 100% duty cycle
- . Overriding clear terminates output pulse
- Schmitt trigger A & B inputs allow infinite rise and fall times on these inputs
- Functions, pin-out, speed and drive compativility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs:

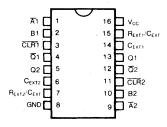
 $I_{OL} = 8mA @ V_{OL} = 0.5V$

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range; 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Package options include "small outline" packages
 (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '123 contains dual retriggerable monostable multivibrators with output pulse width control by three methods.

The basic pulse time is programmed by selection of an external resistor (Rext) and capacitor (Cext). The external resistor and capacitor are normally connected as shown timing component.

Once triggered, the basic output pulse width may be extended by retriggering the gated active Low going edge input (Ai) or the active HIGH going edge input (Bi). By repeating this process, the output pulse period (nQ=HIGH, n $\overline{\rm Q}$ =LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a Lowgoing edge on input CLR, which also inhibits the triggering. An internal connection from CLR to the input gates makes it possible to trigger the circuit by a positive-going signal at input CLR as shown in the function table when CEXT>10nF, the typical output pulse width is defined as; tw=0.45×REXT×CEXT(typ).

Where t_w is in seconds. R is in ohm, and C is in fards. All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

	Inputs	Out	puts	
CLR	Ā	В	Q	Q
L	Х	Х	L	Н
Χ	Н	X	L	Н
Χ	Х	L	L	Н
H	L	↑	Л	L
H	. ↓	Н	Л	7.
↑	L	Н	n	T

H= HIGH voltage level

L= LOW voltage level

X= don't care

↑= LOW to HIGH transition

↓= HIGH to LOW transition

□= one HIGH level output pulse

∪ = one LOW level output pulse

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOk
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots, \pm 20 \text{ mA}$
Continuous OUtput Current Per Pin, Io
(-0.5V <v<sub>O<v<sub>CC+0.5V) ±35 mA</v<sub></v<sub>
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} -65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package(N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	Community Voltages*, V _{IN} , V _{OUT} OV to V _{CC}					
•	·					
Operating Tempera	iture					
Range	KS74HCTLS: -40°C to +85°C					
	KS54HCTLS: -55°C to +125°C					
Input Rise & Fall T	imes, t _r , t _f Max 500 ns					
Unused inputs mu	st always be tied to an appropriate logic					
voltage level (either V _{CC} or GND)						

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55$ °C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			. 2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL		-	0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	loc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤6 ns), HCTLS123

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		$KS74HCTLS$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit	
					Guaranteed	Limits		
Propagation Delay	tpLH		23	33	41	50	ns	
\overline{A},B to Q, \overline{Q}	t _{PHL}	C _L =50pF	23	33	41	50	113	
Propagation Delay	tpLH	C _{ext} =0,	20	27	34	41	ns	
CLR to Q, Q	t _{PHL}	R _{ext} =5kΩ	20	27	34	41		
Output Pulse Width 1	twQ1		116	200	' 207	209	ns	
Output Pulse Width 2	twQ2	C_L =50pF C_{ext} =10nF R_{ext} =10k Ω	45	40 50	38(min) 52(max)	38(min) 52(max)	μs	
Trigger Pulse Width	t _w	C _L =50pF A _i =LOW	7	20	25	30	ns	
Trigger Pulse Width	tw	C _L =50pF B _i =High	7	20	25	30	ns	
Clear Pulse Width	tw	C _L =50pF CLR _i =LOW	8	20	25	30	ns	
External Timing Resistance	R _{ext}			2 100	2(min) 100 (max)	2(min) 100 (max)	kΩ	
External Timing Capacitance	C _{ext}				no restriction	n	pF	
Input Capacitance	Cin		5				pF	
Power Dissipation Capacitance	C _{PD}						pF	

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin-

Application Information

The basic output pulse width is determined by the value of external capacitance and timing resistance. For output pulse widths greater than $100\mu s$ or external capacitance greater than 10nF the following equation should be used.

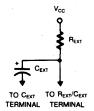
$$t_w = k \cdot R_{ext} \cdot C_{ext}$$

Where

 t_W is in μ s K is the multiplying factor and is approximately 0.45 for Cext is in nF Rest is in k Ω

For best results, system ground should be applied to the C_{ext} terminal. These devices do not require a switching diode in series with the $R_{\text{ext}}/C_{\text{ext}}$ terminal (as required by some other monostable multivibrators)

TIMING COMPONENT



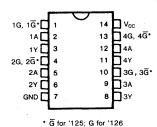
[†] For AC switching test circuits and timing waveforms see section 2.

- · Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- · 3-State outputs with high drive current
- ($I_{OL} = 24 \text{ mA}$ @ $V_{OL} = 0.5 \text{V}$) for direct bus interface
- · Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

· Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLES

125

i	nputs	Output						
Α	G	Y						
Н	L	Н						
L	L	L						
X	Н	Z						

126

Inputs		Output
Α	G	Υ Υ
Н	Н	Н
L	н	L
Х	L	Z

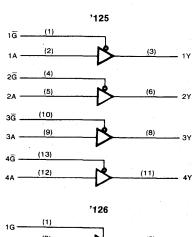
DESCRIPTION

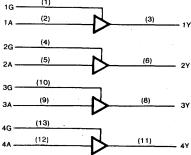
These bus buffers feature four independent line drivers with 3-state outputs. The output enable functions for the '125 buffers are active-low, while those for '126 are active high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to Vcc and ground.

LOGIC DIAGRAMS





Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS T _a = -55°C to +125°C	Unit
•			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	. 2.0	>
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8 ·	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20\mu A$ $I_O = -6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} = 0.1	٧
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS125, HCTLS126

Characteristic	Symbol	Conditions†		T _e = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} =5.0V±10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit	
				Тур	Typ Guaranteed Limits				
Maximum Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF C _L =50pF C _L =150pF		13 16	18 21	22 27	27 33	ns	
A to Y	t _{PHL}			13 16	18 21	22 27	27 33	115	
Maximum Output Enable	tpzH	$R_L=1k\Omega$	C _L =50pF C _L =150pF	17 20	23 26	29 34	34 40	ns	
Time, Enable to Y	tpZL		C _L =50pF C _L =150pF	17 20	23 26	29 34	34 40		
Maximum Output Disable	t _{PHZ}	$R_L = 1 k\Omega$		16		26	32	ns	
Time, Enable to Y	tPLZ	C _L =50pF		16		26	32	Ins	
Maximum Input Capacitance	Cin			5				рF	
Maximum Output Capacitance	Cour	Output D	isabled	10				рF	
Power Dissipation Capacitance* (per stage)	C _{PD} *		Output Disabled Output Enabled					рF	

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.
† For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

İN	IPUTS	OUTPUTS
Α	В	Y
L	L	Н
L	Н	Н
н	L	Н
Н	Н	L

DESCRIPTION

These Schmitt-trigger devices contain four independent NAND gates. They perform the Boolean function $Y = \overline{A \cdot B} = \overline{A + B}$ in positive logic.

The input threshold levels are temperature compensated and can be triggered from the slowest of input ranges and still give jitter-free output signals.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM

1A (1) 1B (2) 1Y
2A (4) 2B (5) (6) 2Y
3A (9) (10) (8) 3Y
4A (12) 4B (13) [] (11) 4)

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, $T_{stg}\ldots -65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

Recommended Operating Conditions

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a =25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	$KS54HCTLS$ $T_{a} = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit	
			Тур		Guaranteed Lim	eed Limits		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	VCC 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.11	v	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_0=20\mu A$ $I_0=4mA$ $I_0=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ	
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	

DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	T _a =	25°C	KS74I T _a = - 40°0	HCTLS C to +85°C	KS54 T _a = - 55°C	HCTLS to +125°C	Unit
Onal actor Istic		rest Collultions	Min	Max	Min	Max	Min	Max	
Positive-Going	V _{T+}	V _{CC} =4.5V	1.2	1.9	1.2	1.9	1.2	1.9	v
Threshold Voltage	V 1 +	V _{CC} =5.5V	1.4	2.1	1.4	2.1	1.4	2.1] •
Negative-Going	V _T _	V _{CC} =4.5V	0.5	1.2	0.5	1.2	0.5	1.2	v
Threshold Voltage	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	V _{CC} =5.5V	0.6	1.4	0.6	1.4	0.6	1.4]
Hysteresis	VH	V _{CC} =4.5V	0.4	1.4	0.4	1.4	0.4	1.4	V
(V _{T+} -V _{T-})	VH .	V _{CC} =5.5V	0.4	1.5	0.4	1.5	0.4	1.5	



[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS132

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74 HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54 HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
tana ara-			Тур		Guaranteed	Limits	
Maximum Propagation Delay	t _{PLH}	C ₁ = 50pF	17	22	28	33	ns
Any Input to Y	tent	QL-30pi	17	22	28	33	113
Maximum Input Capacitance	CIN		5				рF
Power Dissipation Capacitance*	CPD	(per gate)					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

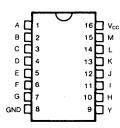
[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

INPUTS A THRU M	OUTPUT Y
All inputs H	L
One or more inputs L	Н

DESCRIPTION

The '133 contains a single 13-input NAND gate. It performs the Boolean functions (in positive logic):

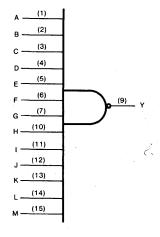
 $Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$

 $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H} + \overline{I} + \overline{J} + \overline{K} + \overline{L} + \overline{M}$

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode olamps to V_{CC} and ground.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7\	/
DC Input Diode Current, I _{IK}	
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ m/s}$	4
DC Output Diode Current, IOK	
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ m/s}$	٩
Continuous Output Current Per Pin, Io	
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ m/s}$	٩
Continuous Current Through	
V _{CC} or GND pins ±125 m/	٩
Storage Temperature Range, T _{stg} 65°C to +150°C)
Power Dissipation Per Package, Pd† 500 mV	۷

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage,	V _{CC} 4.5V to 5.5V
DC Input & Outr	out Voltages*, V _{IN} , V _{OUT} 0V to V _{CC}
Operating Temp	erature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall	I Times, t_r , t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т,	= 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_{O}=-20\mu\text{A}$ $I_{O}=-4\text{mA}$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.ó	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tie 6 ns), HCTLS133

Characteristic	Symbol	Conditions [†]	$T_a = 25^{\circ}C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10 \%$	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
			Тур		Guaranteed Limits		
Maximum Propagation Delay	t _{PLH}	C _i =50pF	18	24	30	36	ns
Any Input to Y	t _{PHL}	OL-30bi	18	25	30	36	
Maximum Input Capacitance	CIN		5				pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15				рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in.}

[†] For AC switching test circuits and timing waveforms see section 2.



[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 3 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

 $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5V$

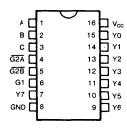
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KSZANCTI St. 409C to 1.959C

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

	able puts	_	ele pu					Out	puts	,		
G1	G2*	С	В	A	Y0	Y 1	Y2	Υ3	Y4	Y5	Y6	Y 7
X	Н	Х	Х	Х	н	Н	Н	Н	Н	Н	Н	Н
Ŀ	X	Х	Х	Χ	н	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	.H
Н	L	L	Н	L	Н	Н	L	Н	н	Н	Н	Н
Н	L	L	Н	H	Н	Н	·H	L	н	Н	Н	Н
н	L	Н	L	L	н	Н	н	Н	L	Н	Н	Н
Н	L	Н	L	н	Н	Н	H	н	Н	L	Н	H
Н	L	Н	Н	L	н	Н	Ή	Н	Н	Н	L	H
Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

 $[\]cdot \overline{G2} = \overline{G2A} + \overline{G2B}$

DESCRIPTION

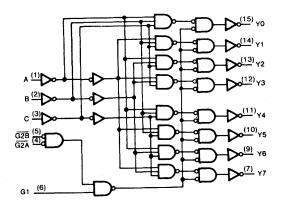
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



KS54HCTLS 138

3-Line to 8-Line Decoders/Demultiplexers

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

		4.5V to 5.5 V _{OUT} OV to V _O	
Operating Tempe			_
Range	KS74HCTLS:	-40°C to +85°	С

KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit	
			Тур	Guaranteed Limits				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4m A$	V _{CC}	V _{CC} ~0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1	v	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA	-	2.7	2.9	3.0	mA	



[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS138

Characteristic	Symbol	Conditions [†]	T _a = 2		KS74 HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54 HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
	1		Тур		Guaranteed	Limits	1
Maximum Propagation Delay, A or B to Y	tpLH		22	30	37	45	ns
	t _{PHL}	C ₁ = 50pF	22	30	37	45	1 115
Maximum Propagation Delay,	tpLH	OL-30PF	24	32	40	48	ns
G1 to any Y	tpHL		24	32	40	48	115
Maximum Propagation Delay,	tpLH		18	25	31	37	ns
G2A or G2B to any Y	t _{PHL}		18	25	31	37	113
Maximum Input Capacitance	CiN		5		,		рF
Power Dissipation Capacitance*	C _{PD}	(;	50				pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}

[†] For AC switching test circuits and timing waveforms see section 2.

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 IoL = 8 mA @ Vol = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

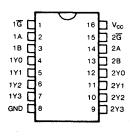
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiriring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The '139 consists of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

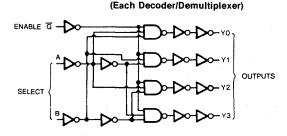
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

İnj	outs		Outputs						
Enable G	Sel B	lect A	YO	Y1	Y2	Y3			
Н	Х	X	Н	н	Н	Н			
L,	L	L	L	Н	. н	Н			
. L	L	Н	н	L	Н	н			
L	H	L	н	Н	Ļ	Н			
' L	Н	. H	н	Н	Н	L			

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vo	c	4.5V to 5.5V
DC Input & Output	Voltages*, V _{IN} ,	Vour OV to Vcc
Operating Tempera	ture	•
Range	KS74HCTLS:	-40°C to +85°C
	KS54HCTLS:	-55°C to +125°C
Input Rise & Fall Ti	mes to to	Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т,	_a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур	Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS139

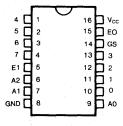
Characteristic	Symbol	Conditions†	T _a = 1	25°C 5.0V	KS74 HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Тур		Guaranteed Limits		
Maximum Propagation Delay, A or B to Y	t _{PLH}	C _L =50pF	22	30	37	45	ns
	t _{PHL}		22	30	37	45	
Maximum Propagation Delay,	t _{PLH}		21	28	35	42	ns
G to any Y	t _{PHL}		21	28	35	42	113
Maximum Input Capacitance	C _{IN}		5				pF
Power Dissipation Capacitance*	C _{PD}		50				pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.
† For AC switching test circuits and timing waveforms see section 2.



- . Encodes eight data lines in priority
- · Provides 3-bit binary priority code
- Input enable capability
- · Easily cascadable
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C
 KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '148 provides three bits of binary coded output representing the position of the highest order active input, along with an output indicating the presence of any active input. It is easily expanded via input and output enables to provide priority encoding over many bits.

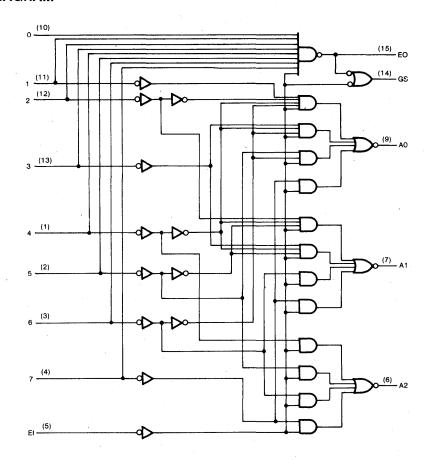
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

	Inputs										Outpu	ıts	
EI	0	1	2	3	4	5	6	7	A2	A 1	A0	GS	EO
Н	Х	Х	Х	Х	Х	Х	Х	Х	Н	Н	Н	Н	Н
L	Н	н	н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Х	Х	Х	Х	Х	Х	Х	L	L	L	L	L	Н
L	Х	Х	Х	Х	Х	Х	L	Н	L	L	Н	L	Н
L	Х	Х	Χ	Χ	Х	L	Н	H	L	Н	L	L	Н
L	Х	Х	X	Χ	L	Н	Н	Н	L	Н	Н	L	Н
L	Х	X	Х	L	Н	Н	Н	Н	Н	L	L	L	Н
L	Х	Х	L	Н	Н	Н	Н	Н	Н	L	Н	, L	Н
L	Х	L	Н	Н	Н	Н	Н	Н	H.	Н	L	L	Н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} −65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	0V to V_{CC}
Operating Temperature	

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	_a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VıL			0.8	0.8	0.8	ν
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} = 0.1 3.84	V _{CC} -0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	Icc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=O\mu A$		8.0	80.0	, 160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin $V_1=2.4V$ other inputs: at V_{CC} or GND $I_{OUT}=O\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS148

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS $T_a = -40$ °C to $+85$ °C $V_{CC} = 5.0V \pm 10\%$	KS54 HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit	
	}		Тур	Typ Guaranteed Limits				
Maximum Propagation Delay,	t _{PLH}		20	27	34	41	ns	
1-7 to A0, A1 or A2	t _{PHL}		20	27	34	41	110	
Maximum Propagation Delay,	t _{PLH}		22	29	36	44	ns ns	
0-7 to EO	t _{PHL}	C _L =50pF	22	29	36	44		
Maximum Propagation Delay,	t _{PLH}		28	38	47	57		
0-7 to GS	t _{PHL}		28	38	47	57		
Maximum Propagation Delay,	t _{PLH}	- OL - 30pi	19	25	31	38	ns	
El to AO, A1 or A2	t _{PHL}		19	25	31	38		
Maximum Propagation Delay,	t _{PLH}		20	26	33	39	ns ns	
El to GS	t _{PHL}		20	26	33	39		
Maximum Propagation Delay,	t _{PLH}		21	28	35	42		
El to EO	t _{PHL}		21	28	35	42		
Maximum Input Capacitance	CIN		5				рF	
Power Dissipation Capacitance*	C _{PD}	(per gate)	50				рF	

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

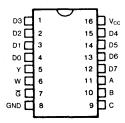
[†] For AC switching test circuits and timing waveforms see section 2.

- Can perform as:
 Boolean Function Generators
 Parallel-to-Serial Converters
 Data Source Selectors
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- . High-Drive-Current outputs:
- (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
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KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



Absolute Maximum Ratings*

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

DESCRIPTION

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input (\overline{G}) must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

		OUT	PUTS		
S	ELEC	т	STROBE		
С	В	Α	G	Y	W
Х	Х	Х	Н	L	Н
L	L	L	L	DO	\overline{DO}
L	L	н	L.	D1	D1
L	Н	L	L	D2	D2
L	Н	Н	L	D3	D3
Н	Ł	L	L	D4	D4
Н	L	Н	L	D5	D5
H	Н	L	L	D6	D6
Н	Н	H	L	D7	D7

H = high level, L = low level, X = irrelevant D0, D1 ... D7 = the level of the D respective input

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, V_{IN}, V_{OUT} 0V to V_{CC} Operating Temperature

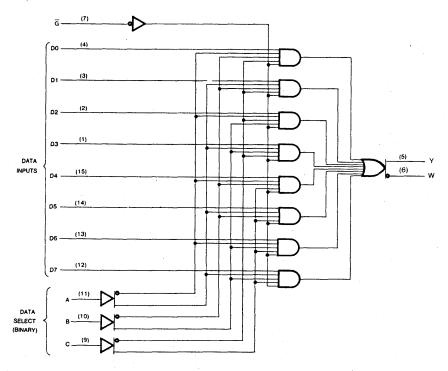
Range KS74HCTLS: -40°C to +85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_F, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т,	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH} -	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =12mA I _O =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input t_r , $t_i \leqslant 6$ ns), HCTLS151

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS $T_a = -40$ °C to +85°C $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit
			Тур		Guaranteed	Limits	
		C _L =50pF	24	32	40	48	
Maximum Propagation Delay,	tpLH	C _L =150pF	27	35	45	54	ns
A, B or C to Y	t =	C _L =50pF	24	32	40	48	'''
<u> </u>	tpHL	C _L =150pF	27	35	45	54	
	tpLH	C _L =50pF	27	36	45	54	
Maximum Propagation Delay,	IPLH	C _L =150pF	30	39	50	60	ns
A, B or C to W	tehl	C _L =50pF	27	36	45	54	113
	PHL	$C_L = 150pF$	30	39	50	60	
	tplH	C _L =50pF	20	26	33	39	ns
Maximum Propagation Delay,	IPLH .	C _L =150pF	23	29	38	45	
Any D to Y	tpHL	C _L =50pF	20	26	33	39	
	LPHL	C _L =150pF	23	29	38	45	
	t _{PLH}	C _L =50pF	16	21	26	32	ns
Maximum Propagation Delay,		C _L =150pF	19	24	31	38	
Any D to W		C _L =50pF	16	21	26	32	
	TPHL	$C_L = 150pF$	19	24	31	38	
	tpLH	C _L =50pF	20	26	. 33	39	
Maximum Propagation Delay,	IPLH	C _L =150pF	23	29	38	45	ns
G to Y	tehl	C _L =50pF	20	26	33	39	
	VENL	C _L =150pF	23	29	38	45	
	tpLH	C _L =50pF	20	26	33	39	ĺ
Maximum Propagation Delay,	·FLFI	C _L =150pF	23	29	38	45	ns
G to W	t _{PHL}	C _L =50pF	20	26	33	39	
	YPAL	C _L =150pF	23	29	38	45	
Maximum Input Capacitance	CIN		5				рF
Power Dissipation Capacitance*	C _{PD}					*	рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC^2} f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.

- . Allows Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- · '253 is the 3-State Version of this port
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- . Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

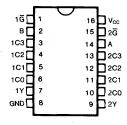
DESCRIPTION

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs $(\overline{\mathbf{G}})$ are provided for each of the two four-line sections.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

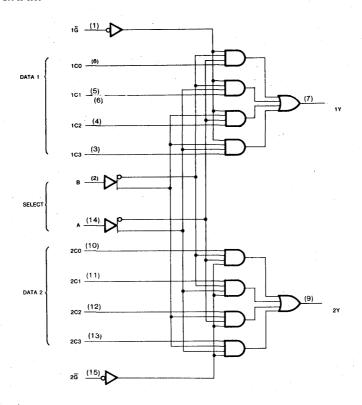
PIN CONFIGURATION



FUNCTION TABLE

	SELECT INPUTS		ΛTΑ	INPU	TS	STROBE	ОИТРИТ	
В	A	CO	C1	C2	СЗ	G	Y	
Х	X	Х	X	Х	Х	Н	L	
L	L	L	Х	Χ	Χ	L	L.	
L	L	Н	Χ	Χ	Χ	L	H	
L	Н	Х	L	Χ	X	· L	L	
L	Н	Х	Н	Χ	Χ	L	Н	
H	L	Х	Х	L	Χ	L	L	
Н	L	· X	Χ	Н	Χ	L	н	
Н	Н	Х	X	Χ	L·	L.	L	
Н	Н	Х	Χ	Х	Н	L	Н *	

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} , −0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) + \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. ¹ Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vo	2 4.5V to 5.5V					
DC Input & Output	Voltages*, V _{IN} , V _{OUT} 0V to V _{CC}					
Operating Tempera	ure					
Range	KS74HCTLS: -40°C to +85°C					
	KS54HCTLS: -55°C to +125°C					
Input Rise & Fall Times, t _r , t _f Max 500 ns						
Unused inputs must always be tied to an appropriate logic						
voltage level (either V _{CC} or GND)						



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit			
<u> </u>			Тур	Typ Guaranteed Limits						
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧			
Maximum Low-Level Input Voltage	VIL	-		0.8	0.8	0.8	٧			
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v			
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V			
Maximum Input Current	In	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ			
Maximum Quiescent Supply Current	lcc _,	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ			
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA			

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS153

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
			Тур		Guaranteed Limits		
Maximum Propagation Delay,	t _{PLH}	$C_L = 50pF$ $C_L = 150pF$	·23 26	30 33	38 43	45 51	ns
A or B to Y	t _{PHL}	C _L =50pF C _L =150pF	23 26	30 33	38 43	45 51	115
Maximum Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	15 18	20 23	25 30	30 36	ne
Data (Any C) to Y	t _{PHL}	C _L =50pF C _L =150pF	15 18	20 23	25 30	30 36	ns
Maximum Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	21 24	28 31	35 40	42 48	ns
G to Y	t _{PHL}	C _L =50pF C _L =150pF	21 24	28 31	35 40	42 48	113
Maximum Input Capacitance	Cin		5		<u>.</u>		pF
Power Dissipation Capacitance*	C _{PD}						рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.

- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data From One Input to Any One of 16 Outputs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These monolithic, 4-line to 16-line decoders decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs. $\overline{G}1$ and $\overline{G}2$, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited | for implementing high-performance memory decoders.

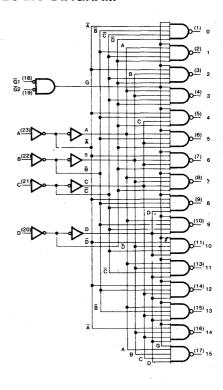
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

0 1	24 □ ٧؞؞
10 2	23 🗖 A
2 🗖 3	22 🗖 B
3 🗖 ⁴	21 🗖 C
4다 5	20 🗖 D
5₫6	19 🗖 🔂
- 6口 7	18 🗖 🗗
7₫8	17 🗖 15
8口9	16 🗖 14
9월10	15 🗖 13
10011	14 🗖 12
GND 12	13 11

LOGIC DIAGRAM



FUNCTION TABLE

		Inputs	3										C	utpu	ıts						
G1	Ğ2	D	С	В	Α	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	н .
L	L	L	L	L	Н	Н	L	Н	H	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	H	Н
L	L	L	L.	Н	L	н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	н
L	L	L	L	Н	Н	н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	H	Н	Н	н
L	L	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	H	Н	Н	Н	Н
L	L	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	H	Н	Н
L	L	L	Н	Н	L	Н	H	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	н
L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	H	Н	H,
L	L	Н	L	L	L	Н	Н	H	Н	Н	Н	Н	Н	L	Н	ļΗ	ıН	Н	Н	Н	н
L	L	Н	L	L	Н	Н	Н	H	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	н
L	L	. н	L	Н	L	H	Н	Н	Н	Н	Н	H	Н	Н	Н	L	Н	Н	Н	Н	H
L	L	Н	L	Н	Н	H	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	H
L	L	Н	Н	L	L	H	Н	Н	Η.	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	н
L	L	H	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	H	Н	Н	L	Н	н
L	L	Н	Н	Н	L	H	Н	Н	Н	Н	Н	H	H.	Н	Н	Н	Н	Н	Н	L	н
L	L	Н	Н	Н	Н	H	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	H.	Н	Н	L
L	Н	Х	Χ	Χ	Χ	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	H	Н	Н	Н	Н	н
H	L	X	Х	Х	X .	Н	Н	Н	Н	Н	H	Н	Н	Н	Н	Н	Н	Н	• н	Н	Н
Н	Н	Х	Х	X	Х	Н	Н.	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н

Absolute Maximum Ratings*

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/° C from 65° C to 85° C

Recommended Operating Conditions

KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	ol Test Conditions		_a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{ОН}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS154

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74 HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54HCTLS $T_a = -55^{\circ}\text{C to } +125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit	
			Тур		Guaranteed Limits			
Maximum Propagation Delay,	t _{PLH}		21	28	35	42	ns	
A, B, C or D to Any Output	t _{PHL}	C ₁ = 50pF	21	28	35	42		
Maximum Propagation Delay,	t _{PLH}	О[-30рі	21	28	35	42	ns	
G1 or G2 to Any Output	tenl		21	28	35	42		
Maximum Input Capacitance	CIN		5				рF	
Power Dissipation Capacitance*	C _{PD}						рF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.



[†] For AC switching test circuits and timing waveforms see section 2.

- Typical applications:
 Dual 2-to-4 line decoder
 Dual 1-to-4 line demultiplexer
 3-to-8 line decoder
 1-to-8 line demultiplexer
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

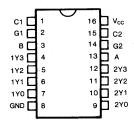
DESCRIPTION

The '155 consists of two 1-to-4 line demultiplexers with independent strobes and common binary address inputs. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied to C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8 line decoder, or 1-to-8 line demultiplexer, without gating.

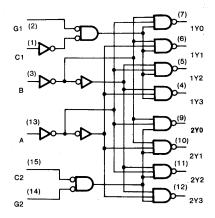
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLES

2-to-4 Line Decoder or 1-to-4 Line Demultiplexer

		Inputs		Outputs					
Sel	ect	Strobe	Data	Outputs					
В	A	G1	C1	1Y0	1Y1	1Y2	1Y3		
Х	Х	Н	Х	Н	Н	н	Н		
L	L	L	Н	L	Η .	Н	Н		
L	Н	L	Н	Н	L	Н	H		
H-	L	L	Н	Н	Н	L	H		
Н	Н	L	Н	Н	Н	Ή	L		
Х	X	Х	L	н	Н	Н	н		

		Inputs			04		
Sel	ect Strobe		Data		Qut	puts	
В	A	G2	C2	2Y0	2Y1	2Y2	2Y3
Х	Х	Н	X	Н	Н	Н	Н
L	L	L	L	L	H	Н	Н
L	Н	L	L	Н	L	Н	H
Н	L	L	L	Н	Н	L	Н
Н	Н	L	L	Н	н	Н	L
Х	Χ	X	Н	Н	Н	Η.	н

3-to-8 Line Decoder or 1-to-8 Line Demultiplexer

Select	Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
CT B A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
XXX	• Н	Н	Н	Н	Н	Н	Н	Н	Н
LLL	L	L	Н	Н	Н	·H	Н	Н	Н
LLH	F	Н	L	Н	Н	Н	Н	Н	Н
LHL	L	Н	Н	L	Н	Н	Н	Н	Н
LHH	L.	Н	Н	Н	L	Н	Н	Н	Н
HLL	L	Н	H	Н	Н	L	Н	Н	Н
HLH	L	Н	Н	Н	Н	Н	L	Н	Н
HHL	L	Н	Н	Н	Н	Н	Н	L.	Н
ннн	L	Н	Н	Н	Н	Н	Н	Н	L

†=Inputs C1 and C2 Connected together

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{sto} 65°C to +150°C

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Power Dissipation Per Package, Pd[†] 500 mW

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

 $\label{eq:KS54HCTLS:} \text{KS54HCTLS:} -55^{\circ}\text{C to } +125^{\circ}\text{C}$ Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

^{‡=}Inputs G1 and G2 Connected together

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧.
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	>
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	\ \
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{EC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V_I =2.4V other Inputs: at V_{CC} or GND I_{OUT} =0 μ A		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS155

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74 HCTLS $T_a = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C}$ $V_{CC} = 5.0 \text{V} \pm 10 ^{\circ}\text{M}$	KS54 HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit			
			Тур		Guaranteed	d Limits				
Maximum Propagation Delay, A, B, C2, G1 or G2 to any Output (2 levels of logic)	t _{PLH}		17	23	29	35	ns			
	t _{PHL}		17	23	29	35				
Maximum Propagation Delay, A or B to any Y	t _{PLH}	C _L =50pF	21	28	35	42	ns			
(3 levels of logic)	t _{PHL}	OL-00bi				21	28	35	42	
Maximum Propagation Delay,	t _{PHL}		20	27	34	41	ns			
C1 to any Y	t _{PHL}		20	27	34	41	110			
Maximum Input Capacitance	C _{IN}		5				pF			
Power Dissipation Capacitance*	C _{PD}						pF			

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC^2} \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

Quad 2-Line to 1-Line Data Selectors/Multiplexers

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

IoL = 8 mA @ VoL = 0.5V

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These are data selectors/multiplexers which select a 4-bit word from one of two sources via the control of a common select input (\overline{A}/B). A separate strobe input (\overline{G}) is provided. The '157 presents true data whereas the '158 presents inverted data at the outputs.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

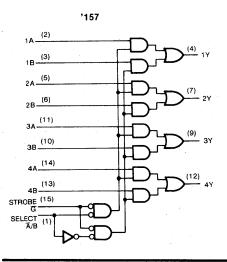
PIN CONFIGURATION

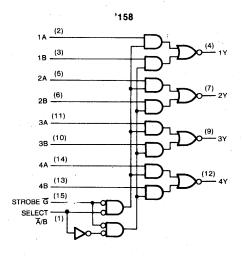
1				ı
Ã/B ☐	1	\cup	16	ן ע _{ככ}
1A 🗖	2		15	Ğ
1B 🗖	3		14	☐ 4A
17 🗆	4		13	□ 4B
2A 🗆	5		12	□ 4Y
2B 🗌	6		11	□ ЗА
2Y 🗌	7		10] 3B
GND 🗌	8		9	□ 3Y
	L			J

FUNCTION TABLE

	Inputs	Outp	out Y			
Strobe	Select	Da	ıta	'157	1450	
Ğ	Ā/B	A	В	157	'158	
Н	Х	Х	·X	L	н	
L.	L	L	Х	L	н	
L	L	Н	X	н	L	
L	н	X	L	L	Н	
L	Н	X	H.	Н	L	

LOGIC DIAGRAMS







KS54HCTLS **157/158** KS74HCTLS

Quad 2-Line to 1-Line Data Selectors/Multiplexers

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, P _d † 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

	•	•					
Supply Voltage, V	cc	4.5V to 5.5V					
DC Input & Outpu	it Voltages*, V _{IN} ,	Vout OV to Vcc					
Operating Temper							
Range	KS74HCTLS:	-40°C to +85°C					
	KS54HCTLS: -	-55°C to +125°C					
Input Rise & Fall Times, tr, tr Max 500 r							
Unused inputs m	ust always be tied t	o an appropriate logic					

voltage level (either V_{CC} or GND)

DC FLECTRICAL CHARACTERISTICS (Voc=5V+10% Unless Otherwise Specified

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 . 3.84	V _{CC} -0.1	V	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	V	
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA	-	2.7	2.9	3.0	mA	



[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS157, HCTLS158

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54 HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
	1.0		Тур		Guaranteed	Limits	
Maximum Propagation Delay,	telH		11	15	19	22	ns
A or B to Y	t _{PHL}		11	15	19	22	115
Maximum Propagation Delay,	tpLH		17	23	29	34	ns
Ā/B to Y	t _{PHL}		17	23	29	34	
Maximum Propagation Delay,	t _{PLH}		15	20	25	30	ne
G to Y	tent		15	20	25	30	ns
Maximum Input Capacitance	C _{IN}		5				pF
Power Dissipation Capacitance*	C _{PD}						рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

KS54HCTLS 160A/161A KS74HCTLS 162A/163A

Synchronous 4-Bit Decade and Binary Counters

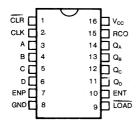
FEATURES

- Internal Look Ahead for Fast Counting
- · Carry Output for n-bit cascading
- Synchronous Counting
- Synchronously Programmable
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLES

'160, '161

CLK	CLR	ENP	ENT	LOAD	Function
Х	L	Х	Х	X	Clear
×	Н	Н	L	• н	Count & RC disabled
X	Н	L	Н	Н	Count disabled
X	н	L	L	H	Count & RC disabled
1	Н	X	Х	L	Load
† ∙	H	Ĥ	Н	Н	Increment Counter

'162, '163

CLK	CLR	ENP	ENT	LOAD	Function
†	L	Х	Х	Х	Clear
Х	Н	Н	L	Н	Count & RC disabled
Χ	Н	L	Н	Н	Count disabled
Χ	H.	L	L	H	Count & RC disabled
↑	Н	Х	Х	L	Load
1	Н	Н	Н	Н	Increment Counter

DESCRIPTION

These are synchronous, presettable 4-bit binary counters featuring internal carry-look-ahead for high-speed counting. The '160 and '162 are decade counters, and the '161 and '163 are 4-bit binary counters. The buffered clock input triggers all flip-flops simultaneously on the rising edge of the input waveform. This eliminates the output counting spikes normally associated with asynchronous counters.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the '160 and '161 is asynchronous and a low level at the clear input sets all four of the flipflop outputs low regardless of the levels of the clock, load or enable inputs.

The clear function for the '162 and 163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter.

Two enable inputs and a ripple carry output allow easy cascading of the counters. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

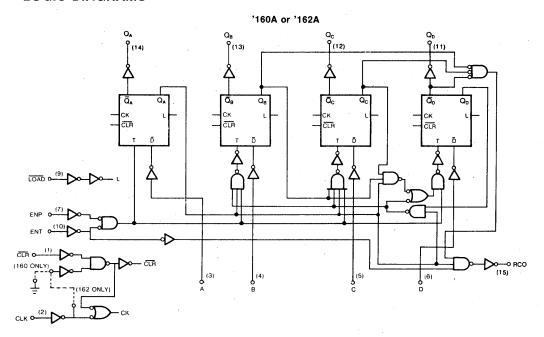
These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating model have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

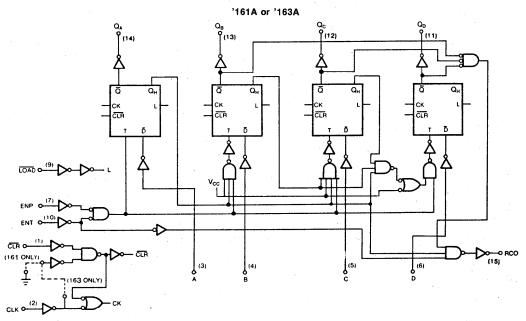
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{cc} and ground.



LOGIC DIAGRAMS

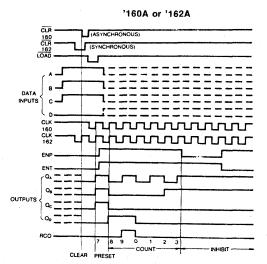




KS54HCTLS 160A/161A KS74HCTLS 162A/163A

Synchronous 4-Bit Decade and Binary Counters

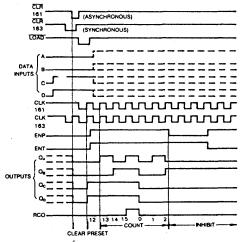
Typical Clear, Preset, Count and Inhibit Sequences



Sequence:

- (1) Clear outputs to zero
- (2) Preset to BCD seven
- (3) Count to eight, nine, zero, one, two, and three
- (A) Inhih

'161A or '163A



Sequence

- (1) Clear outputs to zero
- (2) Preset to binary twelve
- (3) Count to thirteen, fourteen, fifteen, zero, one and two
- (4) Inhit

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions



Synchronous 4-Bit Decade and Binary Counters

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т,	a = 25°C	KS74HCTLS $T_8 = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{ОН}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0 .	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: at V _{CC} or GND iout=0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS160A, HCTLS161A

Characteristic		Symbol	Conditions†	T _a = :		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10^{\circ}\text{M}$	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit
				Тур		Guaranteed	Limits	
Maximum Clock	Frequency	f _{max}		40	30	25	_ 20	MHz
Maximum Propag	gation Delay,	t _{PLH}		26	35	44	53	ns
CLK to RCO		tpHL		26	35	44	53	
Maximum Propag	gation Delay,	t _{PLH}		20	26	33	39	ns
CLK to any Q	<u> </u>	tPHL	C ₁ = 50pF	20	26	33	39	
Maximum Propag	gation Delay,	tpLH	J 00 00p.	11	14	18	21	ns
ENT to RCO		t _{PHL}		1.1	14	18	21	
Maximum Propag	Maximum Propagation Delay, CLR to any Q			21	28	35	42	ns
Maximum Propag	gation Delay,	t _{PHL}		21	28	35	42	ns
Minimum Pulse	CLK High or Low			10	13	17	20	
Width	CLR Low	tw		10	13	17	20	ns
	A, B, C, D			10	13	17	20	
Minimum Setup	LOAD			10	13	17	20	ns
Time before	ENP, ENT	t _{su}		10	13	17	20]
CLK1	CLR inactive			10	13	17	20	
Minimum⊨ Hold Time, All Synchronous Inputs after CLK↑		th		0	0	0	0	ns
Input Capacitano	e	CIN		5				рF
Power Dissipatio	n Capacitance*	C _{PD}		80				pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.



KS54HCTLS 160A/161A KS74HCTLS 162A/163A

Synchronous 4-Bit Decade and Binary Counters

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤6 ns), HCTLS162A, HCTLS163A

Characteristic		Symbol	Conditions†	T ₈ = 25°C V _{CC} = 5.0V		$KS74HCTLS$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55$ °C to +125°C $V_{CC} = 5.0V \pm 10\%$	Unit
				Тур		Guaranteed Limits		
Maximum Clock Frequency		f _{max}		40	30	25	20	MHz
Maximum Propagation Delay, CLK to RCO		tPLH	C _L =50pF	26	35	44	53	ns
		t _{PHL}		26	35	44	53	
Maximum Propagation Delay, CLK to any Q		t _{PLH}		20	26	33	39	ns
		t _{PHL}		20	26	33	39	
Maximum Propagation Delay, ENT to RCO		t _{PLH}		11	14	18	21	ns
		t _{PHL}		11	14	18	21	
Maximum Propagation Delay, CLR to any Q		t _{PHL}		21	28	35	42	ns
Maximum Propagation Delay, CLR to RCO		t _{PHL}		21	28	35	42	ns
Minimum Pulse Width	CLK High or Low	t _w		10	13	17	20 .	ns
	CLR Low			10	13	17	20	
Minimum Setup Time before CLK†	A, B, C, D	tsu		10	13	17	20	ns
	LOAD			10	13	17	20	
	ENP, ENT			10	13	17	20	
	CLR inactive			10	13	17	20	
	CLR Low			10	13	17	20	
Minimum Hold Time, All Synchronous Inputs after CLK1		t _h		.0	0	0	0	ns
Input Capacitance		CiN		5				pF
Power Dissipation Capacitance*		C _{PD}		80				pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-}



[†] For AC switching test circuits and timing waveforms see section 2.

FEATURES

- · AND-Gated (enable/disable) serial inputs
- . Fully buffered clock and serial inputs
- Direct clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- . Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 CONTROL * **CO

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

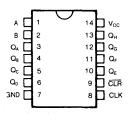
These are high-speed 8-bit registers with AND-gated serial inputs and an asynchronous clear. Data is entered serially through either one of the two inputs, A and B. A high on one input enables the other one, which will then determine the state of the first flip-flop. A low at either or both inputs inhibits data entry and resets the first flip-flop to a low level at the next positive clock transition.

Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of their clock input.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLE

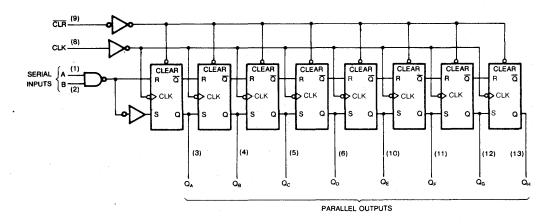
	Inputs	Outputs				
Clear	Clock	A	В	QA	QB.	Q _H
L	Х	Х	Х	Ĺ	L	L
Н	L	X	Χ	Q'AO	Q_{B0}	Q _{H0}
Н	1	Н	Н	Н	Q_{An}	QGn
Н	†	L	Χ	L	Q_{An}	Q_{Gn}
Н	1	X	L	L	Q_{An}	Q_{Gn}

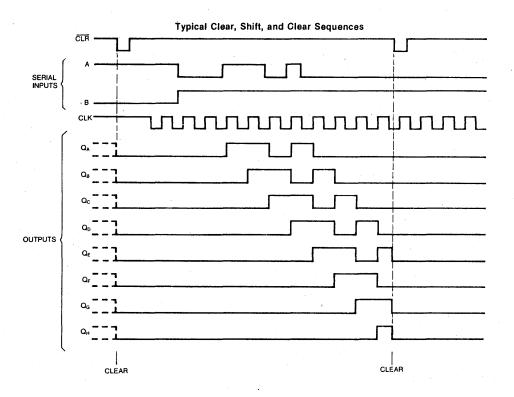
- H = high level (steady state), L = low level (steady state)
- X = irrelevant (any input, including transitions)
- t = transition from low to high level.

 Q_{A0} , Q_{B0} , Q_{H0} =the level of Q_A , Q_B or Q_H , respectively, before the indicate steady-state input conditions were established.

 Q_{An} , Q_{Gn} = the level of Q_A or Q_G before the most-recent t transition of the clock; indicates a one-bit shift.

LOGIC DIAGRAM





Absolute Maximum Ratings*

DC Input Diode Current, I _{IK}
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Supply Voltage Range V_{CC} , -0.5V to +7V

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	V _{CC}	4.5V to 5.5V
		Vout OV to Vcc
Operating Tempe	erature	
Pongo	KS74HCTI S	-40°C to +85°C

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r , t_f Max 500 ns Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т,	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its]
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin $V_1=2.4V$ other inputs: at V_{CC} or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tres ns), HCTLS164

Characteristic		Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V		$KS74HCTLS$ $T_a = -40 ^{\circ}C \text{ to } +85 ^{\circ}C$ $V_{CC} = 5.0V \pm 10 \%$	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
				Тур		Guaranteed	1 Limits	
Maximum Clock Fr	equency	f _{max}		40	30	25	20	MHz
Maximum Propagation Delay, CLR to any Q		t _{PLH}	Ct=50pF	27	36	45	54	ns
Maximum Propagat	ion Delay,	tpLH	OL-Sope	22	30	37	45	ns
CLK to any Q		t _{PHL}		22	30	37	45	
Minimum	CLR Low	_ t _w		10	13	17	20	ns
Pulse Width	CLK High or Low			10	13	17	20	113
Minimum Setup	Data			8	10	13	15	ns
Time before CLK†	CLR Inactive	t _{su}		8	10	13	15	115
Minimum Hold Time Data after CLK1		t _h		0	5	5	5	ns
Maximum Input Capacitance		CiN		5				pF
Power Dissipation	Capacitance*	C _{PD}	(per package)	120				рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-1} For AC switching test circuits and timing waveforms see section 2.

FEATURES

- · Complementary outputs
- Direct overriding load (data) inputs
- · Gated clock inputs
- Parallel-to-Serial data conversion
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These are high-speed 8-bit parallel-load or serial-in shift registers with complementary serial outputs available from the last stage. Parallel-in access is asynchronous and is enabled by pulling the SH/LD input low. When SH/LD is high, data is entered serially at the SER input and shifted one place to the right with each positive clock transition.

Clocking is accomplished through a 2-input NOR gate which permits one of the clocks to be used as a clock inhibit function. Holding either clock input high inhibits clocking. Either clock input is enabled by holding the other clock input low while the SH/\overline{LD} input is high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

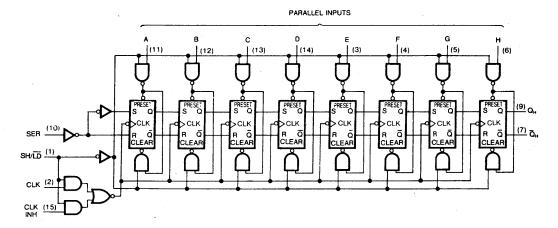
	
SH/LD 🗖 1	16 Vcc
CLK 🔲 2	15 CLK INH
E 🗖 3	14 🗖 D
F 🗖 4	13 C
G 🗖 5	12 🗖 B
н 🗖 6	11 🗖 A
Q _H 7	10 SER
GND 🔲 8	9 🗖 Q _H
L	

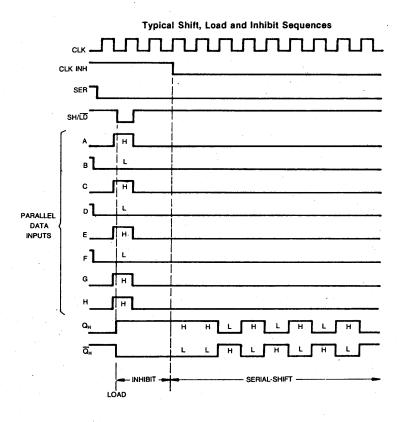
FUNCTION TABLE

		Inputs	1	
	SH/LD	CLK	CLK INH	Function
T	L	X	Х	PARALLEL LOAD
1	. H	H.	X	NO CHANGE
	H	X	Н	NO CHANGE
-	н	L	1	SHIFT*
	Н	1	L	SHIFT*

*Content of each internal register shifts toward output Q_H. Data at serial input is shifted into first register.

LOGIC DIAGRAM







Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IoK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vcc			4.5\	/ to 5	5.5V
DC Input & Output	Voltages*, V _{IN} ,	ν_{out}	0	V to	Vcc
Operating Temperat	ure				
	MOTALIOTI O		00.		

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r , t_f Max 500 ns Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{ОН}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	′±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =OμA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr 46 ns), HCTLS165

Characteristic		Sumbol Conditione V E OV "		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit		
				Тур		Guaranteed	l Limits	
Maximum Cl	ock Frequency	f _{max}		40	30	25	20	MHz
Maximum Pr	opagation Delay,	tpLH		26	35	44	53	ns
SH/LD to Q	ı or Q _H	t _{PHL}		26	35	44	53	110
Maximum Pr	opagation Delay,	t _{PHL}	C _L =50pF	30	40	50	60	ns
CLK to Q _H o	or Q _H	t _{PHL}		30	40	50	60	
Maximum Pr	opagation Delay,	t _{PLH}		20	27	34	41	ns
H to Q _H or $\overline{0}$	Ώн	t _{PHL}		20	27	34	41	
Minimum	SH/LD Low	tw	111131111111111111111111111111111111111	7	10	13	15	ns
Pulse Width	CLK High or Low	·w		13	16	20	25	110
	SH/LD High before CLK1			13	16	20	25	
	SER before CLK1			10	13	17	20	
Minimum Setup Time	CLK INH Low before CLK1	t _{su}		13	16	20	25	ns
	CLK INH High before ÇLK↓			13	16	20	25	
	Data before SH/LDt	1	-	5	7	8	10	
Minimum	SER Data after CLK1	th		-3	0	0	0	ns
Hold Time	PAR Data after SH/LD1			-3	0	0	0	
Maximum In	out Capacitance	CIN		5				pF
Power Dissi	oation Capacitance*	C _{PD}		100				pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

FEATURES

- · Synchronous load
- · Direct overriding clear
- Parallel to serial conversion
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

 $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

 **COMMOTION 1000 to

KS74HCTLS: -40° C to $+85^{\circ}$ C KS54HCTLS: -55° C to $+125^{\circ}$ C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

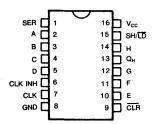
DESCRIPTION

These devices feature parallel-in or serial-in, serial-out registers, gated clock inputs and an overriding clear input. The paralled-in or serial-in modes are established by the shift/load input. When high, the input enables the serial data input and couples the eight fill-flops for serial shifting with each clock pulse. When low, the paralled data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running and the register can be stopped on command with the clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

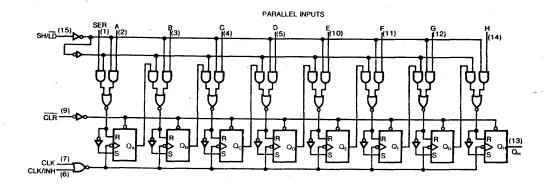
PIN CONFIGURATION



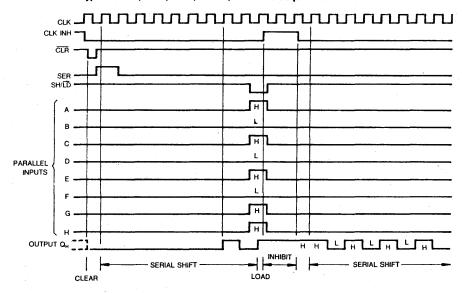
FUNCTION TABLE

			interna	Output				
1	CLR	SH/	CLK	01.14	SER	Parallel Outputs		
	CLK	LD	INH	CLK	SER	A H	Q _A Q _B	
	L	Х	Х	Х	Х	х	LL	L
	Н	Х	L	L	X	X	Q _{AO} Q _{BO}	Q _{H0}
	Η.	L	L	†	Х	a h	a b	h
	Н	Н	L	†	Н	X	H QA	QGn
	Η.	Н	L	†′	L	X	L QA	QGn
-	н	X	Н	1	X.	X	G _{A0} Q _{B0}	

LOGIC DIAGRAM



Typical Clear, Shift, Load, Inhibit, and Shift Sequences



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
. $(V_I < -0.5 V \text{ or } V_I > V_{CC} + 0.5 V)$ $\pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	pormany		
Supply Voltage	V _{CC} 4.5V to 5.5V		
DC Input & Out	put Voltages*, V _{IN} , V _{OUT} OV to V _{CC}		
Operating Temp	erature		
Range	KS74HCTLS: -40°C to +85°C		
_	KS54HCTLS: -55°C to +125°C		
C Input & Output Voltages*, V _{IN} , V _{OUT} 0V to V _{CC} Operating Temperature Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Oput Rise & Fall Times, t _r , t _f Max 500 ns			
I Inused innuts	must always be tied to an appropriate logic		

voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Symbol Test Conditions		_a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
	ļ	-	Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH	·		2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	ViL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	Vон	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} −0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	ΔΙσ	per input pin V _i =2.4V other inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS166

		Symbol	$T_a = 25^{\circ} \text{C}$ Conditions [†] $V_{\text{CC}} = 5.0 \text{V}$			KS74HCTLS $T_a = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C}$ $V_{\text{CC}} = 5.0 \text{V} \pm 10 \%$	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
				Тур		Guaranteed	Limits	
Maximum Cl	ock Frequency	f _{max}		40	30	25	20	MHz
Maximum Pr CLR to Q _H	opagation Delay,	t _{PHL}	C _L =50pF	22	30	37	45	ns
Maximum Pr	opagation Delay,	t _{PLH}	OL COPI	26	36	44	53	ns
CLK to Q _H		t _{PHL}		26	35	44	53	
Minimum	CLR Low	tw		10	13	17	20	ns
Pulse Width	CLK High or Low	ı w		10	13	17	20	113
Minimum Setup Time				10	13	17	20	
	SER before CLK1			10	13	17	20	
	CLK INH before CLK1	t _{su}		10	13	17	20	ns
	Data before SH/LD†			10	13	17	20	
	CLR Inactive before CLK ↑			10	13	17	20	
	SH/LD High after CLK1			7	10	12	15	
Minimum	SER after CLK1]		7	10	12	15	
Hold Time	CLK INH after CLK1	t _h		7.	10	12	15	ns
	Ďata after SH/LD↑			7	10	12	15	
CLR Active after CLK1				7	10	12	15	1
Maximum In	put Capacitance	CiN		5				pF
Power Dissip	pation Capacitance*	C _{PD}					-	pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

Synchronous 4-Bit Up/Down Decade and Binary Counters

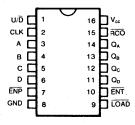
FEATURES

- Fully Synchronous Operation for Counting and Programming
- Internal Look Ahead for Fast Counting
- . Carry Output for N-bit Cascading
- · Fully Independent Clock Circuit
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- - $I_{OL} = 8$ mA @ $V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The '168 is a decade counter and the '169 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (rip-ple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

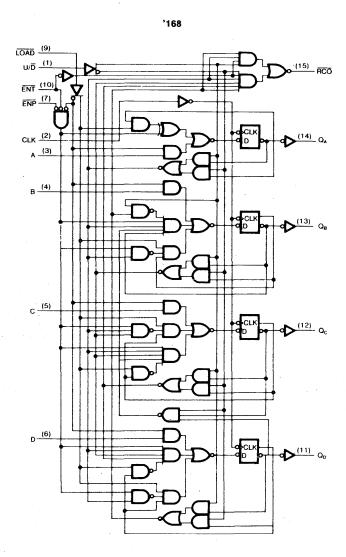
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{\text{ENP}}$ and $\overline{\text{ENT}}$) must be low to count. The direction of the count is determined by the level of the U/ $\overline{\text{D}}$ input. When U/ $\overline{\text{D}}$ is high, the counter counts up; when low, it counts down. Input $\overline{\text{ENT}}$ is fed forward to enable the carry output. The ripple carry output ($\overline{\text{RCO}}$) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transition at $\overline{\text{ENP}}$ or $\overline{\text{ENT}}$ are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, LOAD, U/D) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAMS



LOGIC DIAGRAMS (Continued) LOAD (9) 169 U/\(\overline{D} \) (15) RCO ENT (10) ENP (7) (14) Q_A CLK (2) A (3) в (4) c (5) D (6) 168 169 LOAD LOAD DATA **INPUTS** INPUTS U/D U/D ENP and ENT ENP and ENT 2 COUNT UP --**∤** INHIBIT -- COUNT DOWN-- INHIBIT Illstrated above is the following sequence: Illstrated above is the following sequence: 1. Load (preset) to BCD seven 1. Load (preset) to BCD seven 2. Count up to eight nine (maximum), zero, one, and two 2. Count up to eight nine (maximum), zero, one, and two Inhibit 3. Inhibit 4. Count down to one, zero (minimum), nine, eight, and seven Count down to one, zero (minimum), nine, eight, and seven

FUNCTION TABLE

ORERATING MODE			OUTPUTS					
OPERATING MODE	CLK	U/D	ENP	ENT	LOAD	Dn	Qn	RCO
	1	X	X	Х	ı	i	L	(1)
Parallel Load	1	X	X	Х	i	h	н	(1)
Count Up	. 1	h	1	1	h	Х	Count Up	(1)
Count Down	1	ı	1	i	h .	Х	Count Down	(1)
Hold	1	Х	h	Х	h	Х	qn	(1)
	T	Χ	X	<u>h</u>	h [Х	q _n	. Н

H=HIGH voltage level steady state

h=HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition

L=LOW voltage level steady state

I=LOW voltage level one setup time prior to the LOW-to-HIGH clock transition

X=Don't care

q=Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition

↑=LOW-to-HIGH clock transition

NOTE:

 The RCO is LOW when ENT is LOW and the counter is at Terminal Count Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169.

The RCO is LOW when ENT is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for '168.

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through ,
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Detings are those values have

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, V_{IN}, V_{OUT} OV to V_{CC} Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, tr, tf Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	Ý
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	У _{СС} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	٧
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc '	V _{IN} =V _{CC} or GND I _{OUT} =0µA		8.0	80:0	160.0	μΑ
Additional Worst Case Supply Current	00	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS168, HCTLS169

Characteristic		Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
				Тур		Guaranteed	Limits	
Maximum Operati	ng Froguency	f _{max}		35	30	25	20	MHz
Maximum Propaga	ation Delay,	tplH		26	35	44	52	
CLK to RCO		t _{PHL}	C _L =50pF	26	35	44	52	ns
Maximum Propaga	ation Delay,	tpLH		17	22	28	33	
CLK to Ary Q	•	t _{PHL}		17	22	28	33	ns
Maximum Propagation Delay,		tpLH		15	20	25	30	
ENT to RCO		t _{PHL}		15	20	25	30	ns
Maximum Propaga	ation Delay,	tpLH		20	27	34	40	
U/D to RCO		t _{PHL}		20	27	34	40	ns
Minimum Pulse D CLK high or low	ouration,	t _w		12	16	20	24	ns
	A, B, C or D			12	16	20	24	ns
Minimum	ENP or ENT	t _{su}		12	1.6	20	24	
Setup Time	LOAD	เรน		12	16	20	24	ns ns
Before CLK1	U/D			12	16	20	24	ns
Minimum Hold Time, Data after CLKt		t _h		0	0	0	0	ns
Maximum Input C	apacitance	CIN		5				рF
Power Dissipation	Capacitance*	C _{PD}						рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \; V_{CC}^2 \; f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.



FEATURES

- Gated output control lines for enabling or disabling the outputs
- Fully independent clock for operation in parallel-load or hold modes
- For application as bus buffer registers
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 24$ mA @ $V_{OL} = 0.5V$ for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges: KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These 4-bit registers contain D-type flip-flops with 3-state outputs, capable of driving highly-capacitive or low-impedance loads. This provides the device with the capability of being connected directly to and driving the bus lines in a busorganized system without need for interface or pull-up com-

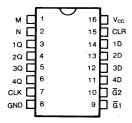
Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gated output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



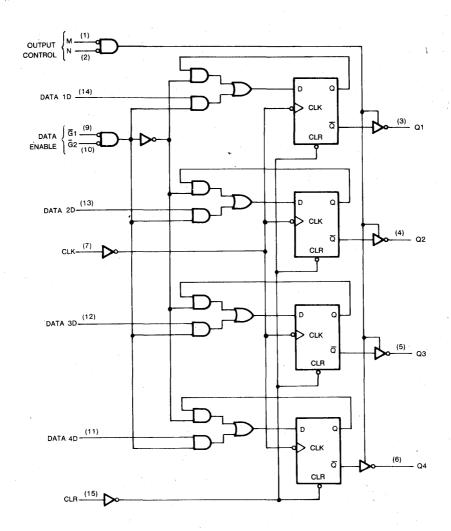
FUNCTION TABLE

	Input									
Clear	Clock	Data I	Enable	Data	Output					
0.00.	0,00m	Ğ1	G2	D	L					
Н	Х	X	Х	Х	L					
L	L	X	Х	Χ	Q ₀					
L	1	Н	X	Χ	Q ₀ Q ₀					
L	1	X	н	X	Q ₀					
L	1	L	L	Ł	L					
L	1	L	L,	Н	н					

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.



LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ $\pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 0.5V + 0.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, P_d^{\dagger} 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

Recommended Operating Conditions

1100011111101144	a operaning commissions
Supply Voltage, Vcc	; 4.5V to 5.5V
DC Input & Output \	Voltages*, V_{IN} , V_{OUT} OV to V_{CC}
Operating Temperat	ure
Range	KS74HCTLS: -40°C to +85°C
•	KS54HCTLS: -55°C to +125°C
Input Rise & Fall Tin	nes, t _r , t _f Max 500 ns
Unused inputs mus voltage level (eithe	It always be tied to an appropriate logic V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
·			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS173

Charac	Characteristic		Con	Conditions [†]			KS74HCTLS $T_a = -40$ °C to +85°C $V_{CC} = 5.0V \pm 10$ %	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$	Unit			
					Тур	Typ Guaranteed Limits						
Maximum Clo	ck Frequency	f _{max} .			45	30	25	20	MHz			
Maximum Pro	onagation	t _{PLH}	C _L =50pl C _L =150		20 23	27 30	. 34 39	41 47	ns			
Delay, CLK to		t _{PHL}	C _L =50pl C _L =150	20 23	27 30	34 39	41 47	113				
Maximum Pro	. •	t _{PHL}	C _L =50pF C _i =150pF		22 25	30 33	37 42	45 51	ns			
Maximum Output Enable		t _{PZH}	D - 110	C _L =50pF C _L =150pF	18 21	25 28	31 36	37 43	ns			
Time, M or N		t _{PZL}	LIF— LVII	C _L =50pF C _L =150pF	18 21	25 28	31 36	37 43	113			
Maximum Output Disable Time, M or N to any Q		t _{PHZ}	R _L =1kΩ	, C _L =50pF	15 15	20 20	25 25	30 30	ns			
Minimum	CLK High or Low	t _{PLZ}		-	10	13	17	20				
Pulse Width	CLR High	t _w			10	13	.17	20	ns			
Minimum	G1 and G2				15	20	25	30				
before CLK†	Data	t _{su}			8	11	14	17 ·	ns			
	CLR Inactive				5	7	8	10				
Minimum Hold Time After CLK†	G1 and G2	t _h			0	0	0 .	0	ns			
	Data	ın ın			0	0	0	0	110			
Maximum Input Capacitance		CIN			5				pF			
Maximum Output Capacitance		Cout	Output D	isabled	10				pF			
Power Dissipation Capacitance*		C _{PD}							рF			

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.
† For AC switching test circuits and timing waveforms see section 2.

KS54HCTLS **174/175** KS74HCTLS

Hex/Quad D-type Flip-Flops with Clear

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

The '174 contains six, and the '175 contains four D-type flip-flops all sharing a common clock and a common clear. The '174 features single rail outputs for every flip-flops whereas the '175 has complementary outputs.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATIONS

174 CLR 16 ∨cc 1Q 15 GQ 14 6D 1D 13 5D 2D Г **1** 50 2Q 12 3D [1 4D 11 ЗQ 10 40 GND [CLK

175 CLR [16 V_{cc} 1Q 🔲 2 □ 4Q 1ত 🗆 3 4Q 1D 🗌 4 13 🔲 4D 2D 🗌 5 DЗD 20 🗆 6 11 30 2Q 🛮 10 30 GND [CLK

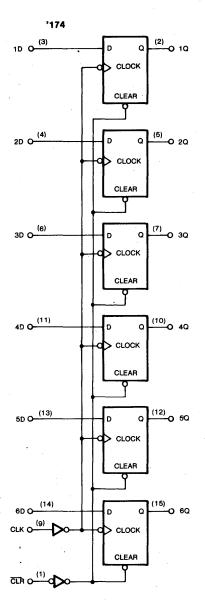
FUNCTION TABLE

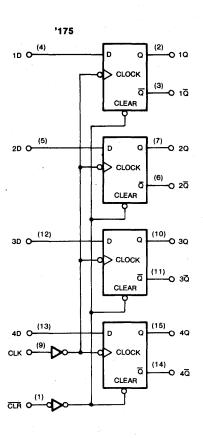
(Each Flip-Flop)

	li	nputs		Out	puts
i	CLR	CLK	D	Q	Qۤ [†]
	L	Ϋ́	Х	L	Н
	н	↑	н	Н	L
l	Н	↑	L	L	Н
Į	Н	L	Χ	Qo	$\overline{\mathbf{Q}}_0$

† '175 only

LOGIC DIAGRAMS





KS54HCTLS **174/175** KS74HCTLS

Hex/Quad D-type Fli-Flops with Clear

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
Vcc or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage,	V _{CC} 4.5V to 5.5V
DC Input & Outp	out Voltages*, V_{IN} , V_{OUT} OV to V_{CC}
Operating Temporating	erature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall	I Times, t_r , t_f Max 500 ns
	must always be tied to an appropriate logic
voltage level (either Voc or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Τ,	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	ĺ
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage		$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA



[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input tr, tie6 ns), HCTLS174, HCTLS175

Charac	Characteristic		Conditions [†]	T _A =2 V _{CC} =		KS74HCTLS T _A = -40°C to +85°C V _{CC} = 5.0V ± 10%	T _A = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
				Тур		Guaranteed	Limits	
Maximum Clock Fr	equency	f _{max}		40	30	25	20	MHz
Maximum Propagat	tion Delay,	t _{PLH}	C ₁ =50pF	22	30	37	45	
CLK to Q or Q		t _{PHL}	OL-SOPE	22	30	37	35	
Maximum Propagation Delay,		tplH		26	35	43	52	ns
CLR to Q or Q	ion boldy,	t _{PHL}		26	35	43	52	
Minimum Setup	Data			10	13	17	20	
Time before CLK1	CLR Inactive	t _{su}		12	16	20	25	ns
Minimum Hold Time, Data after CLK1		t _h		0	0	0	0	ns
Minimum Pulse	CLK High or Low	tw		10	13	17	20	ns
Width	CLR Low	¹w		10	13	17	20	115
Maximum Input Capacitace		CIN		5				рF
Power Dissipation	C _{PD}				-		рF	

 $^{^{\}dagger}$ C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-1} For AC switching test circuits and timing waveforms see section 2.

FEATURES

· Arithmetic operating modes:

Addition
Subtraction
Shift operand A one position
Magnitude comparison

Plus 12 other arithmetic operations

· Logic function modes:

Exclusive-OR
Comparator
AND, NAND, OR, NOR

Plus 10 other logic operations

- Full look-ahead for high-speed operations on long words
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current Outputs:
 I_{OL} = 8mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION

Во □ 1	24 Vcc
ĀO 🗖 2	23 A Ā1
s3 🗖 3	22 D B1
S2 🗖 4	21 🗖 Ā2
S1 🗖 5	20 🗖 🛱 2
so ⊈ 6	19 🗖 🗚
C. 🗖 7	18 🗖 🗟 3
мфв	17 b G
FC 🗖 9	16 C.+4
Ē1, Д 10	15日 戸
F2 C 11	14D A=B
GND 🗖 12	13 🗖 🗗

DESCRIPTION

The '181 is an Arithmetic Logic Unit (ALU)/Function Generator that performs 16 binary arithmetic operations on two 4-bit words as shown in table 1 and 2. These operations are selected by the four functions select lines (SO, S1, S2, S3) and include addition, subtraction, decrement and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low level voltage to the mode control input(M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of 2 cascadeoutputs (P and G) for the 4-bits in the package. When used in conjunction with HCTLS182, high-speed arithmetic operation can be performed. The typical addition times shown in table below illustrates how little is required for addition of longer words when full carry look-ahead is employed.

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small lengths can be performed without external circuitry.

The '181 will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires and end-around or forced carry to provide A-B.

The '181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of the equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with $C_n=H$ when performing the comparison. The A=B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subract mode by placing the function select input S3, S2, S1, S0 at L,H,H,L respectively.

These circuits have been d to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two boolean variables without the use of external circuitry. These logical functions are selected by use of the four function select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry.

The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, OR and NOR functions.

Pin number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-Low Data (Table1)	Āo	Bo	Ā ₁	B ₁	\overline{A}_2	B ₂	Ā ₃	B ₃	Fo	F ₁	F ₂	Fз	Cn	C _n +4	P	G
Active-High Data (Table 2)	Ao	Bo	A ₁	B ₁	A ₂	B ₂	Аз	Вз	Fo	Fi	F ₂	F ₃	Ĉ _n	$\overline{C}_n + 4$	Х	Υ



ALU SIGNAL DESIGNATION

The '181 can be used with the signal designations.

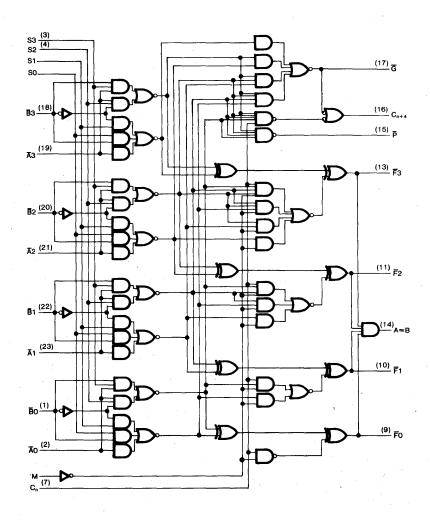
The logic functions and arithmete operations obtained with signal designations as in Table 1.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels

allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



○ Table 1

	Sala	ction		Active-Low Data						
	3616	CHOIL		M = H	M = L; Arithmetic Operations					
S3	S3 S2 S1 S0 Logic Function		Logic Functions	C _n = L (no carry)	C _n = H (with carry)					
L	L	L	L	F=Ā	F=A Minus 1	F=A				
L	L	L	Н	F=AB	F=AB Minus 1	F=AB				
L	L	н	L	F=⊼ + B	F=AB Minus 1	F=AB				
L	L	Η´	Н	F=1	F=Minus 1 (2's Comp)	F=Zero				
L	н	L	L	$F = \overline{A + B}$	F=A Plus (A + B)	F=A Plus (A + B) Plus 1				
L	н	Ł	н	F=B	F=AB Plus (A + B)	F=AB Plus (A + B) Plus 1				
L	н	Н	L	F=Ā⊕B	F=A Minus B Minus 1	F=A Minus B				
L	Н	н	н	F=A + B	F=A + B	F=(A + B) Plus 1				
н	L	L	L	F=\(\bar{A}B\)	F=A Plus (A + B)	F=A Plus (A + B) Plus 1				
н	L	L	н	F=A⊕B	F=A Plus B	F=A Plus B Plus 1				
н	L	н	L	F=B	F=AB Plus (A + B)	F=AB Plus (A + B) Plus 1				
Н	L	Н	н	F=A + B	F=(A+B)	F=(A + B) Plus 1				
Ĥ	н	L	L	F=0	F=A Plus A*	F=A Plus A Plus 1				
н	Н	L	н	F=AB	F=AB Plus A	F=AB Plus A Plus 1				
Н	н	Н	Ĺ	F=AB	F=AB Plus A	F=AB Plus A Plus 1				
н	н	н	H	F=A	F=A	F=A Plus 1				

O Table 2

	Cala	ction		Active-High Data						
	3616	CHOII		M = H	M = L; Arith	metic Operations				
S3 S2 S1 S0 Logic Functions		C _n = L (no carry)	C _n =H (with carry)							
L	L	L	L	F=Ā	F=A	F=A Plus 1				
L	L	L	н	F=A+B	F=A + B	F=(A + B) Plus 1				
Ł	L	Н	L	F=ĀB	F=A + B	F=(A + B) Plus 1				
L	L	Н	н	F=0	F=Minus 1 (2's Comp)	F=Zero				
L	Н	L	Ł	F=AB	F=A Plus AB	F≔A Plus AB Plus 1				
L	· H	L	Н	F=B	F=(A + B) Plus AB	F=(A + B) Plus AB Plus 1				
L	н	Н	L	F=Ā⊕B	F=A Minus B Minus 1	F=A Minus B				
L	. н	н	н	F=AB	F=AB Minus 1	F=AB				
н	L	L	L	F=Ā + B	F=A Plus AB	F=A Plus AB Plus 1				
н	L	L	н	F=A⊕B	F=A Plus B	F=A Plus B Plus 1				
н	L	н	Ł	F=B	F=(A + B) Plus AB	F=(A + B) Plus AB Plus 1				
Н	L	н	Н	F=AB	F=AB Minus 1	F=AB				
н	H	L	L	F=1	F=A Plus A*	F=A Plus A Plus 1				
н	н	L	H	$F=A+\overline{B}$	F=(A + B) Plus A	A=(A + B) Plus A Plus 1				
н	Н	н	L	F=A + B	F=(A + B) Plus A	F=(A + B) Plus A Plus 1				
н	н	н	н	F=A	F=A Minus 1	F=A				

^{*} Each bit is shifted to the next more significant position

Absolute Maximum Ratings*

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.	5V 1	o 5.5V
DC Input & Output Voltages*, VIN, VOUT		0٧	to V _{CC}
Operating Temperature			

Range KS

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, tr, tr Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T _a = -55°C to +125°C	Unit
-			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	o	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

INPUT PAIRS HIGH/NOT HIGH TEST TABLE FUNCTION INPUTS: S2 = M = 4.5 V, S0 = S1 = S3 = 0 V

PARAMETER	INPUT UNDER	OTHER INPUT SAME BIT		OTHER DATA INPIT		OTHER DATA INPUTS		OTHER DATA INDITS		OUTPUT	OUTPUT ⁻ WAVEFORM
_	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	TEST					
tpLH	Āi	Ēi	None	Remaining	Remaining	P	In-Phase				
t _{PHL}	7	6	None	A, C _n	B						
t _{PLH}	Bi	Āi	None	Remaining	Remaining	P	In-Phase				
t _{PHL}	ы	^'	None	B, C _n	. Ā	-					
t _{PHL}	Āi	Bi	None	Remaining	Remaining	C _n +4	Out-of-Phase				
t _{PHL}	A 1	ы	None	Ā, C _n	₿	Cn T4					
t _{PLH}	Bi	Āi	None	Remaining	Remaining	C _n +4	Out-of-Phase				
t _{PHL}	1 131	^	None	B, Cn	A .	Un™4					

PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER	OTHER SAMI		OTHER DATA IN		OUTPUT UNDER	OUTPUT WAVEFORM		
	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	TEST			
t _{PLH}	Āi	Bi	None	Remaining	Cn	Fi	In-Phase		
t _{PHL}).	Ā and B) ·		III IIIGG		
tpLH	Bi	Āi	None	Remaining	Cn	Fi	In-Phase		
t _{PHL}	Ы	^'	None	\overline{A} and \overline{B}	O _n	''	IIITIASE		
t _{PLH}	Āi	Bi	None	None	Remaining	Ρ̈́	In-Phase		
t _{PHL}	^	Di	None	None	A and B, C _n				
t _{PLH}	Bi	Āi	None	None None		P	In-Phase		
t _{PHL}	, DI	. ^:	None	None	A and B, C _n		iii-i riase		
t _{PLH}	Āi	None Bi	Remaining	Remaining	G	In-Phone			
t _{PHL}	· ~	None	ы	B	A, Cn	G	III-FIIONE		
t _{PLH}	Bi	a			None Āi	Remaining	Remaining	G	In-Phase
t _{PHL}	В	None	AI	B	A, Cn	G	in-Phase		
tpLH		None	None	All	All	Any F	In-Phase		
tPHL	Cn	None	None	Ā	B	or Cn+4	III-FIIdSE		
tpLH	Āi	Nana	Bi	Remaining	Remaining	Cn+4	Out-of-Phase		
tPHL	Al	None	81	B	Ā, C _n	Un ^{™4}	Out-or-Phase		
tpLH	Bi	None	Āi	Remaining	Remaining		Out-of-Phase		
tpHL	. 51	None	A	B	A, C _n				

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS181

Characteristic	Symbol	Conditions [†]	T _a = 2 V _{CC} =		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit	
		CL = 50pF	Typ Guaranteed Limits					
Propagation Delay,	t _{PLH}	M=0V	14	18	23	27	ns	
C _n to C _n +4	tpHL	Sum or Diff Mode	14	18	23	27	113	
Propagation Delay,	tplH	M=S1=S2=0V	20	28	35	42	ns	
A or B to Cn+4	tpHL	S0=S3=4.5V	20	28	35	42	110	
Propagation Delay,	tplH	M=S0=S3=0V	25	34	42	50	ns	
\overline{A} or \overline{B} to C_n+4	tpHL	S1=S2=4.5V	25	34	42	50	""	
Propagation Delay Ā or B to G	t _{PLH}	M=S1=S2=0V	22	31	39	47	ns	
	tpHL		22	31	39	47	110	
Propagation Delay A or B to G	tpLH	M=S0=S3=0V	23	32	40	48	ns	
	t _{PHL}	S1=S2=4.5V	23	32	40	48		
Propagation Delay Ā or B to P	tplH	M=S0=S3=0V	25	34	43	51	ns	
	tphL	S1=S2=4.5V	25	34	43	51		
Propagation Delay	tplH	M=S1=S2=0V	25	34	42	50	ns	
Ā or B to P	t _{PHL}	S0=S3=4.5V	25	34	42	50	"	
Propagation Delay	t _{PLH}	M=S1=S2=0V	25	34	42	50	ns	
A or B to Fi	t _{PHL}	S0=S3=4.5V	25	34	42	50		
Propagation Delay	tpLH	M=S0=S3=0V	25	34	42	50	ns	
A or B to Fi	tpHL	S1=S2=4.5V	25	34	42	50	110	
Propagation Delay	t _{PLH}	M=4.5V	20	29	35	42		
Ā or B to A=B	tpHL	W-4.5V	20	28	35	42	ns	
Propagation Delay	tplH	M=S0=S3=0V	25	34	42	50		
A or B to A=B	tpHL	S1=S2=4.5V	25	34	42	50	ns	
Propagation Delay	tpLH		20	28	35	42	ns	
Cn to any F	t _{PHL}		20	28	35	42	113	
Input Capacitance	CIN		5				рF	
Power Dissipation Capacitance*	C _{PD}						pF	

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin-

[†] For AC switching test circuits and timing waveforms see section 2.

PARAMETER MEASUREMENT INFORMATION

LOGIC MODE TEST TABLE
FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER	1	OTHER INPUT SAME BIT		OTHER DATA INDITS		OUTPUT WAVEFORM
	TEST	APPLY 4.5 V	APPLY GND APPLY 4.5 V		APPLY GND	TEST	
telH	Āi	Bi	None	None	Remaining	Fi	Out-of-Phase
t _{PHL}	1 ^1		None	None	\overline{A} and \overline{B} , C_n		
t _{PLH}	Bi	Āi	None	None	Remaining	Fi	Out-of-Phase
t _{PHL}		A	NOTE	None	A and B, C _n		

INPUT BITS EQUAL/NOT EQUAL TEST TABLE FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V

PARAMETER	INPUT UNDER	OTHER SAMI		OTHER DATA		THER DATA INPUTS OUTPUT UNDER	
	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	TEST	
t PLH	Āi	В́і	None	Remaining	None	P	Out-of-Phase
t _{PHL}	Α'	. B'	None	Ā and ₺, C _n	None		Out-or-mase
t _{PLH}	Bi	Āi	None	Remaining	None	P	Out-of-Phase
t _{PHL}	В	A1	None	\overline{A} and \overline{B} , C_n	None		Out-or-Phase
tецн	Āi	None	Bi	Remaining	None	P	In-Phase
t _{PHL}] ^1.	None	В	Ā and B, C _n	None		
t _{PLH}	Bi	None	Āi	Remaining	None	Ē	In-Phase
t _{PHL}		None	^	Ā and B̄, C _n	None		
t _{PLH}	Āi	Bi	None	Remaining	None	Cn+4	In-Phase
t _{PHL}	_ ^i	Br Br	None	\overline{A} and \overline{B} , C_n	None	On 1 4	111 11000
t _{PLH}	Bi	Āi	None	Remaining	None	Cn+4	In-Phase
t _{PHL}	Ы		None	\overline{A} and \overline{B} , C_n	None	On 1 4	III-I IIase
t _{PLH}	Āi	None	Bi	Remaining	None	Cn+4	Out-of-Phase
t _{PHL}		None	ы	\overline{A} and \overline{B} , C_n	NOHE	Un™4	Out-or-rhase
t _{PLH}	Bi	None.	Āi	Remaining	None	Cn+4	Out-of Phase
t _{PHL}	151	None.	<u> </u> ^	A and B, C _n	None	Un * 4	

DIFF MODE TEST TABLE FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER	OTHER SAMI		OTHER DA	TA INPUTS	OUTPUT	OUTPUT WAVEFORM	
	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	TEST		
t _{PLH}	Āi	None	Bi	Remaining	Remaining	Fi	In-Phase	
tpHL	7	None	В	Ā	B, Cn	.,,	iii ii ii ii ii ii ii ii ii ii ii ii ii	
tpLH	Bi	Āi	None	Remaining	Remaining	Fi	Out-of-Phase	
tpHL		^'	None	Ā	B, Cn	''	Out-of-Fliase	
tpLH	Āi	None	Bi	None	Remaining	Ē	In-Phase	
t _{PHL}	^ .	None	6	None	A and B, C _n	F	in-rhase	
tpLH	Бi	Āi	None	None	Remaining	Ē	Out-of-Phase	
t _{PHL}			None	None	\overline{A} and \overline{B} , C_n			
tpLH	Āi	Bi	None	None	Remaining	G	In-Phase	
t _{PHL}		Ы .	None	None	Ā and B, C _n		iii-r iiase	
t _{PLH}	Bi	None	Āi	None	Remaining	G	Out-of-Phase	
t _{PHL}		None	~	None	A and B, C _n			
tpLH	Āi	None	Bi	Remaining	Remaining	A=B	In-Phase	
t _{PHL}		None	DI DI	Ā	B, Cn	A-B	III-FIIdse	
t _{PLH}	Bi	Āi	None	Remaining	Remaining	A=B	Out-of-Phase	
t _{PHL}		. "	None	Ā	B̄, C _n	7-6	Out-of-Flase	
t _{PLH}	Cn	None	None	All	None	C _n +4	In-Phase	
t _{PHL}	On .	THORE	ITONE	A and B	, Tone	or any F	WITT HOSE	
t _{PLH}	Āi	Bi	None	None	Remaining	Cn+4	Out-of-Phase	
t _{PHL}	~	Di	None	None	A, B, Cn	Un T 4	Out-or-Phase	
t _{PLH}	Bi	None	āi	None	Remaining	0.14	In-Phase	
tpHL	1 51	None	di di	None	\overline{A} , \overline{B} , C_n C_n+4		in-rnase	

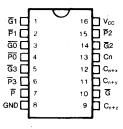
FEATURES

- Compatible Carry Functions for direct ALU connection
- Cascadable to perform look-ahead across n-bit adders.
- High output current drive: IoL = 8mA @ VoL = 0.5V
- Low power consumption characteristic of CMOS
- Direct interface capability to TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '182 is a high-speed, look-ahead carry generator, capable of anticipating a carry across four binary adders or group of adders. These devices can be cascaded to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjuction with the AHCT181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each 182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true from, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the 182 are:

Cn+x=G0 + P0 Cn Cn+y=G1 + P1 G0 + P1 P0 Cn Cn+z=G2 + P2 G1 + P2 P1 G0 + P2 P1 P0 Cn G=G3 + P3 G2 + P2 G1 + P3 P2 P1 G0 P=P3 P2 P1 P0

PIN DESIGNATIONS

Designation	Pin No	Function			
<u>G</u> 0,G1,G2,G3	3,1,14,5	Active Low Carry Generate Inputs			
P0,P1,P2,P3	4,2,15,6	Active Low Carry Propagate Inputs			
Cn	13	Carry Input, Active High			
Cn+x, Cn+y, Cn+z	12,11,9	Carry Outputs			
Ğ	10	Active Low Carry Generate Output			
P	7	Active Low Carry Propagae Output			
V _{CC} 16		Supply Voltage			
GND	8	Ground			

FUNCTION TABLES

FOR G OUTPUT

	OUTPUT						
GЗ	Ğ2	Ğ1	ĞŌ	P3	P2	₽1	G
L	Χ.	Х	Х	Х	х	х	L
Х	L	Χ	X	L	Χ	Х	Ŀ
Х	Х	L	X	L	L.	Х	L
Х	Х	Х	L	L	L	L	L
	Al	l other	comb	inatio	าธ		н

FOR P OUTPUT						
INPUTS	OUTPUT					
P3 P2 P1 P0	P					
L L L L	L					
All other combinations	н					

FOR	Cn+	DUTPUT	
11	IPUT	OUTPUT	
GO	PO	C _n + x.	
L	Х	Х	Н
X	L	Н	н
	ll othe binat		L

Cn+y OUTPUT

			OUTPUT		
G1	G0	P1	PO	Cn	C _{n+y}
L	×	Х	X	X	Н
Χ	L	L	Х	Х	н
Χ·	Х	L	L	Н	Н
	All othe	er comb	inations		L

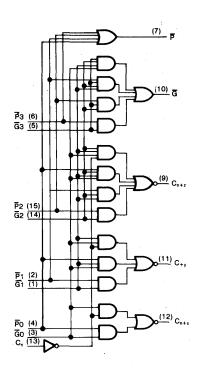
Cn+z OUTPUT

INPUTS							OUTPUT
G2	G1	GŌ	Ē2	₽1	PŌ	Cn	C _n +z
L	Х	Х	Х	Х	Х	Х	Н
х	L	Х	L	Х	Х	Х	н
Х	Х	L	L	L	Х	X	Н
х	X	X	L	L	L	Н	Н
All other combinations							L

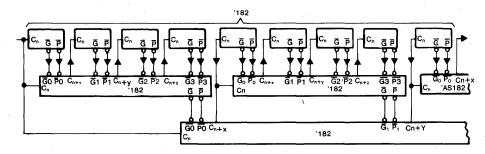
H = high-level, L = low level, X = dont' care

Any inputs not shown in a given table are don't care
with respect to that output.

LOGIC DIAGRAM



Figure; THE '182 IN A 64-BIT LOOK-AHEAD CARRY CIRCUIT



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} →65°C to +150°C
Power Dissipation Per Package Pat 500 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to V_{CC}
Operating Temperature	

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} =0.1 3.84	V _{CC} −0.1 3.7	٧
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: iat V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, t 6 ns), HCTLS182

Characteristic	Symbol	Conditions†	T _a =25°C V _{CC} =5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCLTS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit	
	1		Тур		Guaranteed	Limits	l .	
Propagation Delay Pi or Gi to	tplH	C _I = 50pF	19	26	32	39	ns	
C _{n+x} C _{n+y} , C _{n+z}	tpHL	OL COP	19	26	32	39	113	
Propagation Delay	tpLH	C _L =50pF	19	26	32	39	ns	
Pi or Ĝi to G	tpHL		19	26	32	39		
Propagation Delay C _n to	tpLH	C ₁ = 50pF	25	27	34	41	ns	
C_{n+x} , C_{n+y} , C_{n+z}	tpHL	OL-OOD!	25	27	34	41	1115	
Propagation Delay	· t _{PLH}	C ₁ =50pF	15	20	25	30	ns	
Pi to P	tpHL	C[=30bi	15	20	25	30	113	
Input Capacitance	CIN		5				pF	
Power Disipation Capacitance*	C _{PD}						pF	

 $^{^{\}star}C_{PD}$ determines the no-load dynamic power dissipation: PD= C_{PD} $V_{CC}{}^{2}$ f_{in} .

[†]For Acc switching test circuits and timing waveforms see section 2.

- · For use in high-speed wallace-tree summing
- · Fast addition operation
- Low power consumption characteristic of CMOS
- High output current drive: IoL = 8mA @ Vol = 0.5V
- Direct interface capability with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C
- KS54HCTLS: -55°C to +125°C
 Package options include "small outline" packages
 (Available Tape & Reel), standard DIPs.

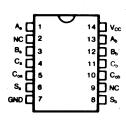
DESCRIPTION

The '183 is a dual full adder features an individual carry output from each bit for use in multiple-input, carry-save techniques to produce the true sum and true carry outputs with no more than 2 gate delays.

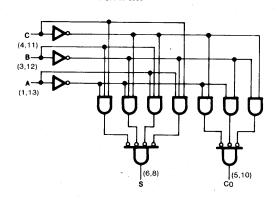
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Half)

	Inputs		Out	put
Α	. В		S	Co
L	L	L	L	L
н	L	L	н	· L
L	н	L	Н	L
L	L	Н	Н	L
· H	н	L	L	н
- H	, L	н	L	н
L	н	Н	L	н
н	Н	н	н	н

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, I _{OK}
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, V_{IN} , V_{OUT} . . OV to V_{CC} Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	т	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
,	1		Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1	V _{CC} -0.1 3.7	٧
Maximum Low-Level Output Voltage	VoL	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in V _I =2.4V other Inputs: at V _{CC} or GND Iout=0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tr 6 ns), HCTLS 183

Characteristic	Symbol	Conditions [†]	T _a = 2 V _{CC} =	5°C 5.0V	$KS74HCTLS$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
-			Тур		Guarantee	d Limits	
Propagation Delay	t _{PLH}	C _I = 50pF	15	22	27	33	ns
Tropagation Delay	tpHL	OL-30bi	17	23	29	. 35	113
Input Capacitance	CiN						рF
Power dissipation Capacitance*	C _{PD}						pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

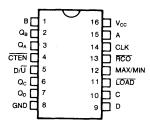


- · Single down/up count control line
- Look-ahead circuitry enhances speed of cascaded counters
- Fully synchronous in count modes
- Asynchronously presettable with load control
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

OPERATING MODE		INPUTS							
OPERATING MODE	LOAD	D/Ū	CTEN	CLK	Input	On			
	L	x	X	X	L	L			
parallel load	L	Х	· x	Х	н	н			
count up	н	L	1	t	Х	count up			
count down	н	н	1	t	Х	count down			
hold (do nothing)	н	Х	Н	Х	х	no change			

RCO AND MAX/MIN FUNCTION TABLE

	INPUTS		TER	OUTPUTS				
D/Ū	CTEN	CLK	QA	QB	Qc	QD	MAX/MIN	RCO
н	н	X	Н	х	×	н	L	н
L	н	X	H	х	×	н	н	н
L	L	Т.	н	x	X	Н	1 7	U
L	Н ,	Х	L	L	L	L	L	н
н	H	X	L	L	L	L	н	н
н	L	T	L	L	L	L	7_	77

- H = HIGH voltage level L = LOW voltage level
- I = LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition
- X = Don't care
- † = LOW-to-HIGH CLK transition
- ປ = one LOW level pulse
- "L = MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

DESCRIPTION

These are high-speed synchronous reversible 4-bit decade counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with a synchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{\text{CTEN}}$) is low. A high at $\overline{\text{CTEN}}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/\overline{U}) input. When D/\overline{U} is low, the counter counts up and when D/\overline{U} is high, it counts down.

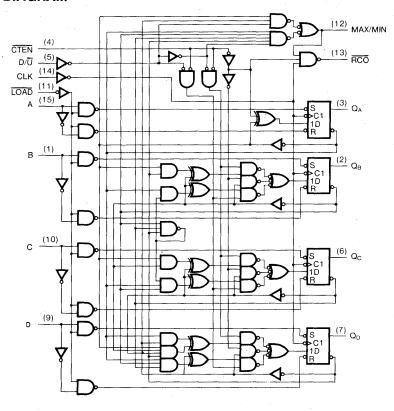
These counters feature a fully independent clock circuit. Changes at the control inputs $(\overline{CTEN} \text{ and } D/\overline{U})$ that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

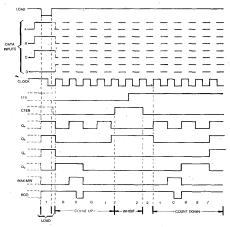
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.



Typical load, count, and inhibit sequences



Sequence;

- (1) Load (preset) to BCD seven.
- (2) Count up to eight, mine(maximum) zero, one, and two
- (3) Inhibit
- (4) Count down to one, zero (minimum), nine, egiht, and seven

NOTE A: Clear overrides load data, and count inputs.

Note B:When count up, count-down input must be high;
when counting down, countup intput must be high.

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): ~12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	•	
Supply Voltage,	Vcc	4.5V to 5.5V
DC Input & Out	out Voltages*, Vin,	Vout . OV to Vcc
Operating Temp	erature	
Range	KS74HCTLS:	-40°C to +85°C
-	KS54HCTLS:	-55°C to +125°C
Input Rise & Fal	l Times, t _r , t _f	Max 500 ns
•	must always be tied either V _{CC} or GND)	to an appropriate logic

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	1
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	VoH	V _{IN} =V _{IH} or V _{IL} I _O =-20μA I _O =-4mA	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1 3.7	v
Maximum Low-Level Output Voltage	Vol	V _{IN} =V _{IH} or V _{IL} I _O =20μA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	In	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =OμA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input in V _I =2.4V other Inputs: at V _{CC} or GND Iout=0µA		2.7	2.9	3.0	mA



Synchronous 4-Bit Up/Down Decade Counters

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS190

Cha	Characteristic		Conditions [†]	T _a =2 V _{CC} ≈		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit	
			Тур		Guaranteed	l Limits	<u></u>		
Maximum Clock	Frequency	f _{max}	•	30	20	16	14	MHz	
Maximum Propa	agation Delay,	tpLH		30	40	50	60	ns	
LOAD to any C	<u> </u>	tpHL		30	40	50	60		
Maximum Propa	agation Delay,	tpLH		27	36	45	64	ns	
A,B,C, D to any	y Q	tpHL		27	36	45	54		
Maximum Propa	agation Delay,	TPLH		17	22	28	33	ns	
CLK to RCO		t _{PHL}		17	22	28	33	,,,,	
Maximum Propa	agation Delay,	tpLH		23	30	37	45	ns	
CLK to any Q		t _{PHL}	C _L =50pF	23	30	37	45		
Maximum Propa	agation Delay,	tpLH			47	59	70	ns	
CLK to MAX/MIN		t _{PHL}		35	47	59	70		
Maximum Propa	agation Delay,	tPLH		33	45	56	67	ns	
D/U to RCO	•	tpHL		33	45	56 -	67		
Maximum Propa	agation Delay,	tpLH		25	33	41	50		
D/U to MAX/MI	N	tpHL		25	33	41	50		
Maximum Propa	agation Delay,	tplH		25	33	41	50	ns	
CTEN to RCO		tpHL		25	33	41	50	1 ns	
Minimum	CLK High or Low	tw		13	17	21	25	ne	
Pulse Width	LOAD Low	•		13	17	21	25	ns	
	Data before LOAD1			10	13	17	20		
Minimum	CTEN before CLKt	t _{su}		20	26	34	40	ns	
Setup Time	D/Ū before CLKf	*80		10	.13	17	20	110	
	LOAD Inactive before CLK1			15	20	25	30		
Minimum Hold				1	3	5	5		
Time				0	0	0	0	ns	
				0	0	0	0]	
Maximum Input	Capacitance	CiN		5				pF	
Power Dissipati	on Capacitance*	CPD		80				pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}



[†] For AC switching test circuits and timing waveforms see section 2.

- Single down/up count control line
- Look-ahead circuitry enhances speed of cascaded counters
- · Fully synchronous in count modes
- Asynchronously presettable with load control
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

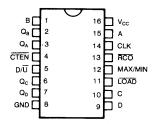
IOL = 8 mA @ VOL = 0.5V

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

OPERATING MODE		INPUTS								
OF ENATING MODE	LOAD	D/Ū	CTEN	CLK	Input	O _n				
parallel load	L L	×	X	X	L H	L H				
count up	н	L	1	t	Х	count up				
count down	н	Н	i i	Ť	Х	count down				
hold (do nothing)	Н	X	Н	X	x	no change				

RCO AND MAX/MIN FUNCTION TABLE

	INPUTS		TERM	MINAL C	OUNT S	TATE	OUTP	UTS
D/Ū	CTEN	CLK	$Q_{\mathbf{A}}$	QB	Qc	QD	MAX/MIN	RCO
Н	Н	X	Н	Х	×	. Н	L	Н
L	H	X	н	Х	x	Н	н	н
L	L	ľ	Н	x	X	н	TL.	T
L	Н	Х	L	L	L	L	L	н
н	H	X	L	L	L	L	н	н
н	L	П.	L	L	, L	l L	1 7L	\Box

- H = HIGH voltage level
- L = LOW voltage level
- I = LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition
- X = Don't care
- † = LOW-to-HIGH CLK transition
- ∪ = one LOW level pulse
- L = MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

DESCRIPTION

These are high-speed synchronous, reversible 4-bit binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with a synchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{\text{CTEN}}$) is low. A high at $\overline{\text{CTEN}}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/\overline{U}) input. When D/\overline{U} is low, the counter counts up and when D/\overline{U} is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs (CTEN and D/Ū) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

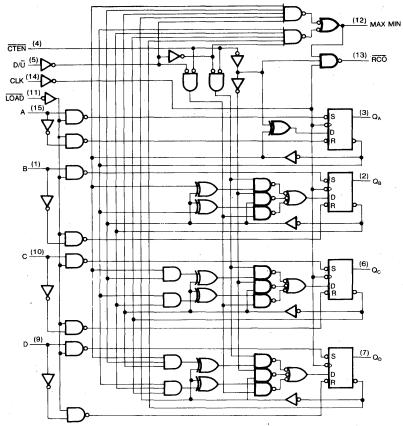
These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

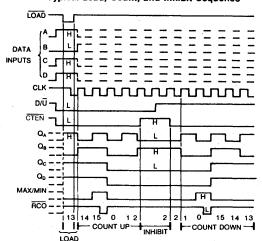
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.





Typical Load, Count, and Inhibit Sequence



Sequence:

- (1) Load (preset) to binary thirteen
- (2) Count up to fourteen, fifteen, zero, one, and two
- (3) Inhibit
- (4) Count down to one, zero, fifteen, fourteen, and thirteen

Absolute Maximum Ratings*

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

•
Supply Voltage, V _{CC} 4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT 0V to VCC
Operating Temperature
Range KS74HCTLS: -40°C to +85°C
KS54HCTLS: -55°C to +125°C
Input Rise & Fall Times, t_{r} , t_{f} Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	mbol Test Conditions		a = 25°C	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS T _a = -55°C to +125°C	Unit	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	V	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
Maximum Input Current	In	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA	



AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS191

Cha	Symbol	Conditions [†]	T _a =2 V _{CC} =		$KS74HCTLS$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_{a} = -55^{\circ}\text{C to } +125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit		
				Тур		Guaranteed	l Limits		
Maximum Clock	k Frequency	f _{max}		30	20	16	14	MHz	
Maximum Prop		t _{PLH}		30	40	50	60	ns	
LOAD to any C		t _{PHL}		30	40	50	60		
Maximum Prop	agation Delay,	t _{PLH}		27	36	45	64	ns	
A,B,C, D to an	y Q	t _{PHL}	C _L =50pF	27	36	45	54		
Maximum Prop	agation Delay,	T _{PLH}		17	22	28	33	ns	
CLK to RCO		t _{PHL}		17	22	28	33	"	
Maximum Prop	agation Delay,	tPLH		23	30	. 37	45	ns	
CLK to any Q		t _{PHL}		23	30	37	45	113	
Maximum Prop	agation Delay,	t _{PLH}		35	47	59	70	ns	
CLK to MAX/M	CLK to MAX/MIN			35	47	59	. 70	113	
Maximum Propagation Delay,		tplH		33	45	56	67	ns	
D/Ū to RCO		tpHL		33	45	56	67	113	
Maximum Prop	agation Delay,	tpLH		25	33	. 41	50	-	
D/Ū to MAX/MI	N	t _{PHL}		25	33	41	50	1	
Maximum Prop	agation Delay,	tpLH		25	33	41	50	ns	
CTEN to RCO	-	t _{PHL}		25	33	41	50	113	
Minimum	CLK High or Low	tw		13	17	21	25	ns	
Pulse Width	LOAD Low	- w		13	17	21	25	113	
	Data before LOAD↑			10	13	17	20		
Minimum	CTEN before CLK1	t _{su}		20	26	34	40	ns	
Setup Time	D/Ū before CLK↑	1 450		10	13	17	20	110	
	LOAD Inactive before CLK1			15	20	25	30		
Minimum Hold	Data after LOAD↑			1	3	5	5		
Time	CTEN after CLK1	th		0	0	0	٠0	ns	
	D/Ū after CLK†			0	0	0	0		
Maximum Input	Capacitance	CIN		5				pF	
Power Dissipat	ion Capacitance*	CPD		80				pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.



[†] For AC switching test circuits and timing waveforms see section 2.

- · Look-ahead circuit enhances cascaded counters
- · Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- I_{OL} = 8 mA @ V_{OL} = 0.5V Inputs and outputs interface directly with TTL, NMOS
- and CMOS devices

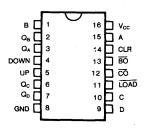
 Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These are high-speed synchronous reversible 4-bit decade counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting-spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-tohigh-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

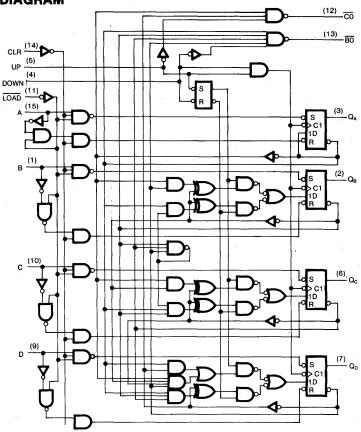
All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

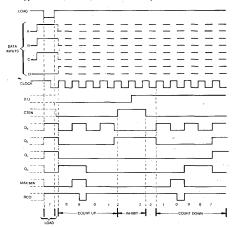
These counters were designed to be cascaded without the need for external circuitry. The borrow output (\overline{BO}) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output (\overline{CO}) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and countup inputs, respectively, of the succeeding counter.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.



Typical load, count, and inhibit sequences



Sequence;

- (1) Load (preset) to BCD seven.
- (2) Count up to eight, mine(maximum) zero, one, and two.
- (3) Inhibit
- (4) Count down to one, zero (minimum), nine, egiht, and seven

NOTE A: Clear overrides load data, and count inputs.

Note B:When count up, count-down input must be high;
when counting down, countup intput must be high.



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

Recommended Operating Conditions

Recommen	ided Operating Conditions
Supply Voltage,	V _{CC} 4.5V to 5.5V
DC Input & Outp	out Voltages*, VIN, VOUT OV to VCC
Operating Temporating	erature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall	Times, t _r , t _f Max 500 ns
Unused inputs	must always be tied to an appropriate logic
voltage level (either Vcc or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit		
			Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	VIL	-		0.8	0.8	0.8	v		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1 3.7	v		
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	ΔΙςς	per input in V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA		



[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Synchronous 4-Bit Up/Down Decade Counters with Dual Clock

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS192

Cha	1 1		T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit		
	V.	1		Тур		Guarantee	d Limits	1	
Maximum Clock	Frequency	f _{max}		35	25	20	18	MHz	
Maximum Propa	gation Delay,	t _{PLH}		18	25	31	37	ns	
UP to CO		tpHL		18	25	31	37		
Maximum Propa	gation Delay,	tpLH		18	24	30	36	ns	
DOWN to BO		t _{PHL}	C _L =50pF	18	24	30	36		
Maximum Propa	gation Delay,	TPLH		32	42	52	63	ns	
UP or DOWN to	any Q	t _{PHL}		32	42	52	63	113	
Maximum Propagation Delay, LOAD to any Q		tpLH		30	40	50	60	ns	
		tPHL		30	40	50	60		
Maximum Propagation Delay, CLR to any Q		t _{PHL}		18	24	30	36	ns	
	CLR High			10	13	17	20		
Minimum Pulse	LOAD Low	t _w		10	13	1.7	20	ns	
Width	UP or DOWN High or Low			10	13	17	20		
	Data before LOAD1			10	13	17	20	١.	
	CLR Inactive before UP1 or DOWN1			10	13	. 17	20	ns	
Minimum Setup Width	LOAD Inactive before UP1 or DOWN1	t _{su}		10	13	17	20	ns ·	
	UP high before DOWNt			10	13	17	20		
	DOWNhigh before UPt			10	13	17	20	1	
Minimum Hold	Data after LOAD↑			1	3	5	5 ,		
Time	UP High after DOWN1	th		С	0	0	0	ns	
	DOWN High after UP1			0	0	0	0		
Maximum Input	Capacitance	CIN		5				pF	
Power Dissipation	on Capacitance*	C _{PD}		80				pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \; V_{CC}^2 \; f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

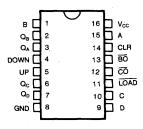
KS54HCTLS 193 KS74HCTLS

Synchronous 4-Bit Up/Down Binary Counters with Dual Clock

FEATURES

- Look-ahead circuitry enhances cascaded counters
- Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear
- · Function, pin-out, speed and drive compatibility with 54/74LS logic family
- · Low power consumption characteristic of CMOS
- High-Drive-Current outputs: $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C
- · Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

DESCRIPTION

These are high-speed synchronous reversible 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-tohigh-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow output (BO) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output (CO) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and countup inputs, respectively, of the succeeding counter.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and around.

OPERATING MODE		INPUTS								OUTPUTS				
OI ENATING MODE	CLR	LOAD	UP	DOWN	Α	В	С	D	QA	QB	Qc	QD	co	BO
accet (close)	Н	Х	Х	L	X	Х	Х	Х	L	L	L	L	Н	L
reset (clear)	Н	Х	Х	Н	X	X	X	X	L	L	L	L	Н	Н
	L	L	X	L	L	L	L	L	L	L	L	L.	Н	L
	L	L	×	Н	L	L	L	L	L	L	L	L	∖ н	Н
parailel load	L	L] L	Х	Н	Н	Н	Н	Н	J - H	н	Н	L	ુ #ાં
	L	L	Н	X	Н	Н	Н	Н	Н	Н	Н	Н	Н	н
count up	L	Н	1	Н	Х	Х	X	Х	count up		H*	Н		
count down	L	H	Н	1	X	Х	Х			count	down		Н	H**

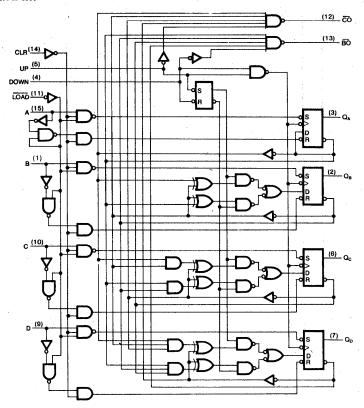
H= HIGH voltage level

↑= LOW-to-HIGH clock transition * CO = UP at terminal count up (HHHH) L= LOW voltage lovel

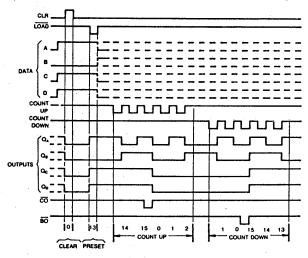
X= don't care

** BO = DOWN at terminal count down (LLLL)





Typical Clear, Load, and Count Sequences



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} , -0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, IO
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values boyond

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns Unused inputs must always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1	V _{CC} -0.1 3.84	V _{CC} =0.1	V
Maximum Low-Level Output Voltage	Vol	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	V
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V_i =2.4V other inputs: at V_{CC} or GND I_{OUT} =0 μ A		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS193

Ch	aracteristic	Symbol	Conditions [†]	T _a =		KS74HCTLS $T_a = -40$ °C to +85°C $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
				Тур		Guarantee	d Limits	
Maximum Clock	Frequency	f _{max}		35	25	20	18	MHz
Maximum Propa	gation Delay,	tpLH		18	25	31	37	ns
UP to CO		t _{PHL}		18	25	31	37	
Maximum Propa	gation Delay,	tpLH		18	24	30	36	ns
DOWN to BO		tPHL	C _L =50pF	18	24	30	36	113
Maximum Propa	gation Delay,	T _{PLH}		32	42	52	63	ns
UP or DOWN to	any Q	t _{PHL}		32	42	52	63	ns
Maximum Propa	gation Delay,	tplH		30	40	50	60	
LOAD to any Q		t _{PHL}]	30	40	50	60] "
Maximum Propagation Delay, CLR to any Q		t _{PHL}		18	24	30	36	ns
	CLR High	t _w		10	13	17	20	ns
Minimum Pulse	LOAD Low			10	13	17	20	
Width	UP or DOWN High or Low			10	13	17	. 20	
	Data before LOAD1			10	13	17 .	20	
	CLR Inactive before UP1 or DOWN1			10	13	17	20	ns
Minimum Setup Width	LOAD Inactive before UP1 or DOWN1	t _{su}		10	13	17	20	ns
	UP high before DOWNt			10	13	17	20	
	DOWNhigh before UP1			10	13	17	20	
Minimum Hold	Data after LOAD↑			1.	3	5	5	ns
Time	UP High after DOWNt	th		0	0	0	0	
	DOWN High after UP1			0	0	0	0	
Maximum Input Capacitance		C _{IN}		5				pF
Power Dissipation	on Capacitance*	C _{PD}		80				pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \; V_{CC^2} \; f_{in}$



[†] For AC switching test circuits and timing waveforms see section 2.

- · Parallel-to-Serial, Serial-to-Parallel Conversions
- Left or Right Shifts
- Parallel Synchronous Loading
- Direct Overriding Clear
- Temporary Data Latching Capability
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

IOL = 8 mA @ VOL = 0.5V

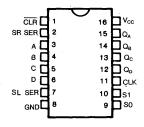
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These bidirectional shift registers feature parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation:

- Inhibit clock (temporary data latch/do nothing)
- Shift-right (in the direction QA toward QD)
- Shift-left (in the direction QD toward QA)
- Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, SO and S1, high. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift-right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode control inputs are low.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

	INPUTS									OUTPUTS					
CLR	MODE		MC MC		OI K	SE	RIAL	P	\R/	ALL	EL	QA	0-	Qc	Qp
CLN	S1	S0	CLK	LEFT	RIGHT	A	В	С	D	GA.	QB	u.	Cab		
L	X	Х	Х	·x	Х	Х	X	Х	Х	L	L	L	L		
Н	X	Χ	L	X	Χ	X	Х	Х	Х	QAO	Q_{B0}	Q_{C0}	Q_{D0}		
Н	Н	Н	↑	X	Χ	a	b	С	d	a	b	С	đ		
Н	L	Н	†	X	н	X	Х	Χ	Х	Н	Q_{An}	Q_{Bn}	Q _{Cn}		
н	L	Н	1	X	L	X	Χ	Χ	Χ	L	Q_{An}	Q_{Bn}	Qçn		
Н	Н	L	↑	Н	X	X	Х	Χ	Χ	QBn	Qcn	Q_{Dn}	н		
Н	H	L	↑	L	X	X	Х	X	Χ	Q _{Bn}	Q _{Cn}	Q_{Dn}	L		
Н	L	L	Х	×	Х	X	Χ	Χ	X	Q _{AO}	Q_{B0}	Q_{CO}	Q_{D0}		

H=high level (steady state) L=low level (steady state)

X=irrelevant (any input, including transitions)

t=transition from low to high level

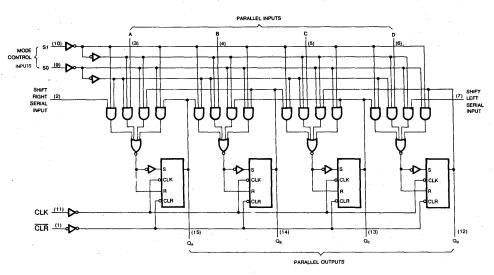
a,b,c,d=the level of steady-state input at inputs, A,B,C, or D, respectively.

Q_{AO}, Q_{BO}, Q_{CO}, Q_{DO}=the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

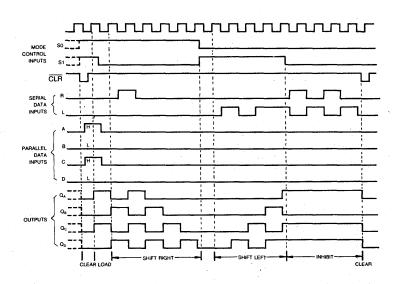
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}=the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.



(positive logic)



typical clear, load, right-shift, inhibit, and clear sequences



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} , −0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ $\pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ $\pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 0.5V + 0.5V$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to $+150$ °C
Power Dissipation Per Package, P_d^{\dagger} 500 mW
* Absolute Maximum Ratings are those values beyond
which normanant dames at the device were every

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	F
Supply Voltage, Vo	2 4.5V to 5.5V
DC Input & Output	Voltages*, V_{IN} , V_{OUT} . 0V to V_{CC}
Operating Temperat	ure
Range	KS74HCTLS: -40°C to +85°C
e e e e e e e e e e e e e e e e e e e	KS54HCTLS: -55°C to +125°C
Input Rise & Fall Til	mes, t _r , t _f Max 500 ns
Unused inputs mus voltage level (eith	at always be tied to an appropriate logic V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T _a = -55°C to +125°C	Unit
	:		Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	Уон	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤6 ns), HCTLS194

Characteristic		Symbol	Conditions†	T _a = 2		KS74HCTLS $T_a = -40$ °C to $+85$ °C $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55^{\circ}\text{C to } +125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit	
				Тур		Guaranteed	Limits		
Maximum Clo	ck Frequency	f _{max}		40	30	30 25 20			
Maximum Pro	pagation Delay,	tpLH	1	18	24	30	36	ns	
CLK to Q _H		tpHL	C _L =50pF	18	24	30	36	1113	
Maximum Propagation Delay, CLR to Q _H		t _{PHL}		21	28	35	42	ns	
Minimum	CLR to Low			12	16	20	24		
Pulse Width	CLK High or Low	t _w		12	16	20	24	ns	
	Minimum Setup Time, Any Input before CLK†			10	17	20	20	ns	
Minimum Hold Time, Data after CLK†		ts		0	.0	0	0	ns	
Maximum Inp	Maximum Input Capacitance			5				pF	
Power Dissip	ation Capacitance*	C _{PD}						pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in.}

[†] For AC switching test circuits and timing waveforms see section 2.

- Parallel-to-Serial, Serial-to-Parallel Conversions
- Parallel Synchronous Loading
- . J and K Inputs to First Stage
- Right-shift Only with Complementary Outputs on Last Stage
- . Direct Overriding Clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

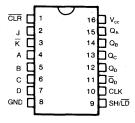
 $I_{OL} = 8$ mA @ $V_{OL} = 0.5$ V

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These 4-bit registers feature parallel inputs, parallel outputs, $J-\bar{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

Parallel (broadside) load Shift (in the direction A_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associate flip-flops and appears at the outputs after the positive transition of the clock input. During loading serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Sexial data for this mode is entered at the $J \cdot \overline{K}$ inputs. These inputs permit the first stage to perform as a $J \cdot \overline{K}$, D-, or T-type flip-flop as shown in the function table.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

-	INPUTS								OUTPOUTS				
CLR SHIFT/LOAD		CLK	SEF	RIAL	PA	RA	\LL	EL	0.	Λ-	٥-	^	Qσ
CLI	SHIF I/LOAD	CLK	J	K	A	В	С	D	QA	QB	Qc	UD	ωŋ
L	Х	, X,	Х	Х	Х	х	Х	Х	L	L	L	L	Н
Н	L	†	X	Х	a	b	С	đ	a	b	С	d	d
H	Н	L	X	Х	X	Χ	Х	Χ	Q _{AO}	Q_{B0}	Qco	Qpo	\overline{Q}_{DO}
Н	н	†	L	Н	X	Х	Х	Χ	QAO	QAO	Q_{Bn}	Qcn	\overline{Q}_{Cn}
Н	н	†	L	L.	X	Х	Х	Χ	L	Q_{An}	Q_{Bn}	Qcn	Q _{Cn}
Н	н	†	H	н	×	Χ	X	Χ	Н	Q_{An}	Q_{Bn}	Qcn	Q _{Cn}
н	н	1	H	L	X	Х	Х	Х	QAn	Q_{An}	Q_{Bn}	Qcn	Q _{Cn}

H=high level (steady state)

L=low level (steady state)

X=irrelevant (any input, including transitions)

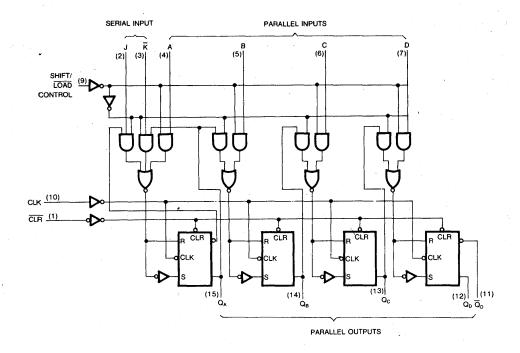
↑=transition from low to high level

a,b,c,d=the level of steady-state input at A,B,C, or D, respectively.

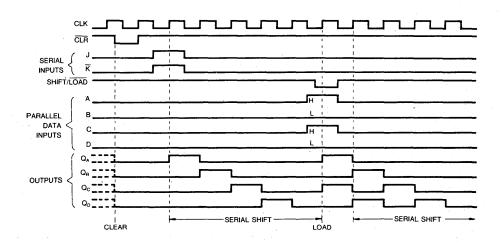
Q_{AO}, Q_{BO}, Q_{CO}, Q_{DO}=the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}=the level of Q_A, Q_B or Q_C, respectively, before the mostrecent transition of the clock.





typical clear, shift, and load sequences





Absolute Maximum Ratings*

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

. 1000 iiiiii ciiac	a operating conditions
Supply Voltage, Vcc	4.5V to 5.5V
DC Input & Output \	Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Temperate	ure
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall Tin	nes, t_r , t_f Max 500 ns
Unused inputs mus voltage level (eithe	t always be tied to an appropriate logic V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit	
	1		Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	v	
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND	į	±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μА	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS195

Characteristic		Symbol	Conditions [†]	T _a = 2		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
				Тур		Guaranteed	l Limits	
Maximum Cloc	k Frequency	f _{max}		50	30	25	20	МНz
Maximum Proj	pagation Delay,	tpLH	0 -50-5	18	24	30	36	ns
CLK to Q _H		t _{PHL}	C _L =50pF	18	24	30	36	ns
Maximum Propagation Delay, CLR to Q _H		t _{PHL}		21	28	35	42	ns
Maximum	CLR Low	t _w		10	12	15	20	ns
Pulse Width	CLK High or Low			12	16	20	24	
Minimum	SH/LD High			15	20	25	25	
Setup Time	Serial or Parallel	t _{su}		12	15	20	24	ns
before CLK†	CLR inactive	1	,	15	20	25	25	
Minimum	SH/LD High			0	0		0	
Hold Time after CLK1	Serial or Parallel Data	t _h		0	0		0	ns
Maximum Inpu	t Capacitance	CiN		5				рF
Power Dissipation Capacitance*		C _{PD}						рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.



[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - IOL = 24mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION

			1	
1 G 🗀	1	_	20	□ V _{cc}
1A1 [2		19	2G
2Ÿ4	3		18	1√1
1A2 [4		17	2A4
2¥3 [5		16] 1\(\overline{Y}2\)
1A3 [6		15	2A3
2¥2	7		14	1₹3
1A4 [8		13	2A2
2Y1	9		12	□ 1Ÿ4
GND [10		.11] 2A1
	L			l

FUNCTION TABLE

In	put	0	utput
G	Α	4	Y
L	L		H
L	Н	-	L ·
Н	Χ		Z

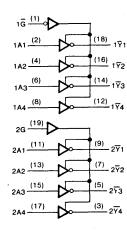
DESCRIPTION

These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



KS54HCTLS 210 KS74HCTLS

Octal Buffers and Line Drivers with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _C DC Input & Output		
Operating Tempera	ture	
Range	KS74HCTLS: -	40°C to +85°C
-	KS54HCTLS: -5	5°C to +125°C

Input Rise & Fall Times, tr, tr Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either Vcc or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55$ °C to +125°C	Unit
	}		Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	Im	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ

AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS210

Characteristic	Symbol	Conditions†		_	25°C - 5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit	
	-		Тур		Guarantee	d Limits			
Maximum Propagation Delay,	C _L =50pF C _L =150pF		13 16	18 21	22 27	27 33			
A to \overline{Y}	t _{PHL}	C _L =50pF C _L =150pF		13 16	18 21	22 27	27 33	ns	
Maximum Output Enable	t _{PZH}	Rı = 1kΩ	$C_L = 50pF$ $C_L = 150pF$	17 20	23 26	29 34	34 40	ns	
Time, Enable to Y	t _{PZL}	11[-172	C _L =50pF C _L =150pF	17 20	23 26	29 34	34 40	113	
Maximum Output Disable	t _{PHZ}	$R_L=1k\Omega$		16	21	26	32	ns	
Time, Enable to Y	t _{PLZ}	C _L =50pF		16	21	26	32	"	
Maximum Input Capacitance	CIN			5				pF	
Maximum Output Capacitance	Cour	Output Disabled		10				рF	
Power Dissipation Capacitance* (per stage)	C _{PD}		Output Disabled Output Enabled					рF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in.}

[†] For AC switching test circuits and timing waveforms see section 2.

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C
 KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These devices are designed to be used in highperformance memory-decoding or data-routing applications requiring very short propagation delay times. In highperformance memory systems, these decoders can be used with high-speed memories utilizing a fast enable circuit. The delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

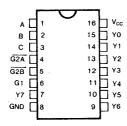
The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding.

A 24-line decoder can be implemented without external inverters and a 31-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

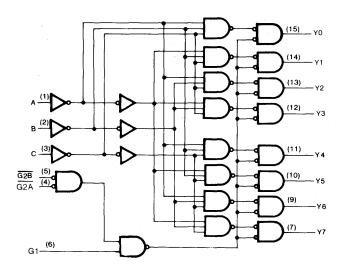
PIN CONFIGURATION



FUNCTION TABLE

	able outs	_	Select Inputs				(Out	outs			
G1	G2⁺	С	В	A	YO	Υ1	Y2	ΥЗ	Υ4	Y5	Y6	Y7
X	Н	Х	Х	. X	L	L	L	L	L	L	L	L
L	X	X	Х	Χ	L	L	L	L	L	L	L	L
Н	L	L	L	L	Н	L	L	L	L	L	L	L
Н	L	L	L	Н	L	Н	L	L	L	L	L	L
H	L	L	Н	L	L	L	Н	L	L	$\mathbf{L}^{\mathcal{L}}$	L	L.
Н	Ł	Н	L	L	L	L	L	Н	L	L	L	L
Н	L	Н	L	L	L	L	L	L	Н	Ŀ	L	L
н	L	Н	L	Н	L	L	L	L	L	Н	L	L
Н	L	Н	Н	L	L	L	L	L	L	L	Н	L
· H	L	Н	Н	Н	L.	L	L	L	L	L	L	Н

^{*}G2=G2A+G2B



Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} −65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

voltage level (either V_{CC} or GND)



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $t_O=-20\mu\text{A}$ $t_O=-4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	o	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or'GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin Vz=2.4V Other Inputs: At V _{CC} or GND I _O =0		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input to, to 6 ns), HCTLS238

Characteristic	Symbol	Conditions [†]	T _a =	25°C 5.0V	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit
			Typ Guaranteed Limits				
Maximum Propagation Delay,	t _{PLH}		22	30	37	45	ns
A, B, C or any Y	t _{PHL}		22	30	37	45	113
Maximum Propagation Delay,	t _{PLH}	C _L =50pF	24	32	40	48	ns
G1 to any Y	t _{PHL}	ı	24	32	40	48	
Maximum Propagation Delay,	t _{PLH}		18	25	31	37	ns
G2A or G2B to any Y	t _{PHL}		18	25	31	37	
Maximum Input Capacitance	C _{IN}		5				рF
Power Dissipation Capacitance*	C _{PD}		50				pF.

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$. † For AC switching test circuits and timing waveforms see section 2.

- · Designed specifically for high-speed memory decoders and data transmission systems
- . Incorporates 2 enable inputs to simplify cascading and/or data reception
- · Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

IOL = 8 mA @ VOL = 0.5V

- . Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges: KS74HCTLS: -40°C to +85°C
- KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These devices are designed to be used in highperformance memory-decoding or data-routing applications requiring very short propagation delay times. In highperformance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory.

This means that the effective system delay introduced by the decoder is negligible.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

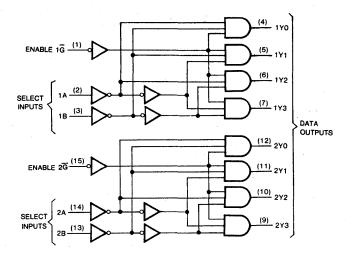
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and

PIN CONFIGURATION



FUNCTION TABLE

1n ₁	outs			Out	puts	
Enable	I			Y1	Y2	Υ3
Ğ	В	Α	Y0	YI	12	13
Н	Х	X	L	L	L	L
L	L	L	Н	L	L	L
L	L	Н	L.	Н	L.	L
L	Н	L	L	L	Н	L
L ·	н	Н	L	L	L	Н



Absolute Maximum Ratings*

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Power Dissipation Per Package, Pd[†] 500 mW

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V	cc 4.5V to 5.5V
DC Input & Outpu	t Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Temper	ature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall 1	imes, t _r , t _f Max 500 ns
•	ust always be tied to an appropriate logic her V_{CC} or GND)



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _s = -55°C to +125°C	Unit	
			Тур		its			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	<	
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	>	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	v	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN} = V_{IH}$ or V_{IL} $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input tr., tr<6 ns), HCTLS239

Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
			Тур	Typ Guaranteed Limits			
Maximum Propagation Delay,	tpLH		22	30	37	45	ns
A or B any Y	t _{PHL}		22	30	37	45	
Maximum Propagation Delay,	tplH	C _L =50pF	21	8	35	42	ns
G to any Y	t _{PHL}		22	8	35	42	
Maximum Input Capacitance	CIN		5				рF
Power Dissipation Capacitance*	C _{PD}		50				рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$. For AC switching test circuits and timing waveforms see section 2.

KS54HCTLS **240/241/244** Octal Buffers and Line KS74HCTLS **240/241/244** Octal Buffers and Line Drivers with 3-State Outputs

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (loL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

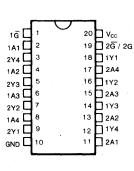
The designer has the choice of combinations of inverting/ non-inverting outputs and symmetrical complementary input control (both active-low, or one active-low, the other active-high).

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

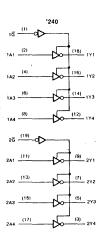
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

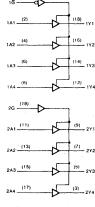
PIN CONFIGURATION

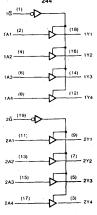
LOGIC DIAGRAMS



*2G for '240 and '244 2G for '241







FUNCTION TABLE

			'241, '244	'240
	In	out	Output	Output
G	Ō	ā A	Y	Y
Н		_ L	L	Н
Н.	. .	_ Н	. H	L
L	H	-	Z	Z



KS54HCTLS **240/241/244** Octal Buffers and Line KS74HCTLS **240/241/244** Octal Buffers and Line Drivers with 3-State Outputs

Absolute Maximum Ratings*

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified).

Characteristic	Symbol	Test Conditions	T _a = 25°C		$KS74HCTLS$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55$ °C to +125°C	Unit
·			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	ViL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	٧
Maximum Low-Level Output Voltage	V _{OL}	V_{IN} = V_{IH} or V_{IL} I_O =20 μ A I_O =12 μ A I_O =24 μ A	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ



KS54HCTLS **240/241/244** Octal Buffers and Line KS74HCTLS **240/241/244** Octal Buffers and Line Drivers with 3-State Outputs

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS240 . HCTLS241, HCTLS244

Characteristic	Symbol	Conditions†		T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS $T_{a} = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit	
	[!				Typ Guaranteed Limits				
Maximum Propagation Delay,	ţрLН	C _L =50pF C _L =150pF C _L =50pF C _L =150pF		13 16	18 21	22 27	27 33	ns	
A to Y	t _{PHL}			13 16	18 21	22 27	27 33		
Maximum Output Enable	tрzн	Rı=1kΩ	C _L =50pF C _L =150pF	17 20	23 26	29 34	34 40	ns	
Time, Enable to Y	t _{PZL}	11[174	C _L =50pF C _L =150pF	17 20	23 26	29 34	34 40		
Maximum Output Disable	t _{PHZ}	$R_L = 1 k\Omega$		16	21	26	32	ns	
Time, Enable to Y	tPLZ	C _L ≈50pF		16	21	26	32	1115	
Maximum Input Capacitance	CiN			5				рF	
Maximum Output Capacitance	Cout	Output D	isabled	10				рF	
Power Dissipation Capacitance* (per stage)	C _{PD}	Output Disabled Output Enabled		5 30				рF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f.

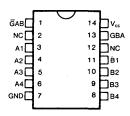
[†] For AC switching test circuits and timing waveforms see section 2.

- 2-Way Asynchronous Communication Between Data Buses
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- . 3-State outputs with high drive current
- ($I_{OL} = 24 \text{ mA}$ @ $V_{OL} = 0.5 \text{V}$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These four-data line transceivers are designed for asynchronous two-way communications between data buses.

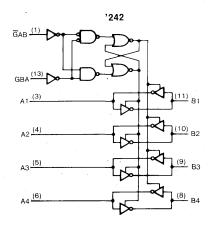
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

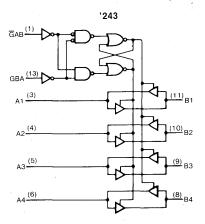
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

INPUTS		'242	'243
GAB	GBA	242	243
L	L	Ā to B	A to B
Н	Н	B to A	B to A
Н	L	Isolation	Isolation
L	Н	Isolation	Isolation

LOGIC DIAGRAMS





Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. [†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, V _{IN} , V _{OUT}	OV to V _{CC}
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns Unused inputs must always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

DC FLECTRICAL CHARACTERISTICS (Voc=5V+10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55$ °C to +125°C	Unit	
			Тур	Guaranteed Limits				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA \ V_{IR}$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА	
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ	
Maximum Quiescent Supply Current	lcc.	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mΑ	



AC ELECTRICAL CHARACTERISTICS (Input t_r, t_i≤6 ns), HCTLS242, HCTLS243

Characteristic	1 1		T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit	
				Тур	Typ Guaranteed Limits			
Maximum Propagation Delay.	tpLH	C _L =50pF C _L =150pF C _L =50pF C _L =150pF		14 17	18 21	22 27	27 33	ns
A to B or B to A	t _{PHL}			14 17	18 21	22 27	27 33	
Maximum Output Enable Time	tрzн	R _i = 1kΩ	C _L =50pF C _L =150pF	23 26	30 33	38 43	45 51	ns
GAB to B, GBA to A	tpzL		C _L =50pF C _L =150pF	23 26	30 33	38 43	45 51	110
Maximum Output Disable	tpHZ	$R_L = 1 k\Omega$ $C_L = 50 pF$		18	25	31	37	ns
Time, GAB to B, GBA to A	tPLZ			18	25	31	37	1115
Maximum Input Capacitance	Cin			5			1	pF
Maximum Output Capacitance	Cour	Output Disabled		10				рF
Power Dissipation Capacitance* (per stage)	C _{PD}	Output Disabled Output Enabled		5 30			200 Mari Mari Mari Mari Mari Mari Mari Mari	pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-state outputs with high drive current
 (I_{OL} = 24mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

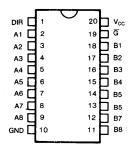
These high-speed octal bus transceivers are designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input (\overline{G}) can be used to disable the device so that the buses are effectively isolated.

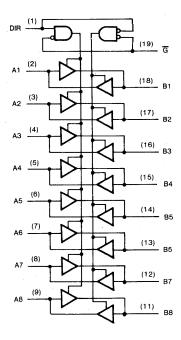
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Oneration
G	DIR	Operation
L	L	Bus B Data to Bus A
L	Н	Bus A Data to Bus B
Н	Х	Isolation

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} −65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Τ,	a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1 3.7	٧
Maximum Low-Level Output Voltage	Vol	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr. tr<6 ns), HCTLS245

Characteristic	Symbol	Condition	Conditions [†]		25°C : 5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
				Тур		Guaranteed Limits		
Maximum Propagation Delay	t _{PLH}	C_L =50pF C_L =150pF C_L =50pF C_L =150pF		1 - 1 -	12 15	15 20	18 34	ns
A to B or B to A	t _{PHL}			9	12 15	15 20	18 34	115
Maximum Output Enable	t _{PZH}	Rı = 1kΩ	C _L =50pF C _L =150pF	30 33	40 43	50 55	60 66	ns
Time, G to A or B	t _{PZL}		C _L =50pF C _L =150pF	30 33	40 43	50 55	60 66	
Maximum Output Disable	tpHZ	$R_L = 1 k\Omega$		18	25	31	· 37	1
Time, G to A or B	t _{PLZ}	C _L =50p	F	18	25	31	37	ns
Maximum Input Capacitance	CIN			5				рF
Maximum Output Capacitance	Cout	Output Disabled		10				рF
Power Dissipation Capacitance* (per stage)	C _{PD}	G=V _{CC} G=GND		5 30				рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.

- . Three-State Version of '151
- Three-State Outputs Interface Directly with System Bus
- Perrorms Parallel-to-Serial Conversion
- Complementary Outputs Provide True and Inverted Data
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- . 3-State outputs with high drive current
- ($I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5 \text{V}$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

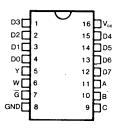
These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature strobe-controlled complementary three-state outputs.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe $(\overline{\bf G})$. The outputs are disabled when $\overline{\bf G}$ is high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

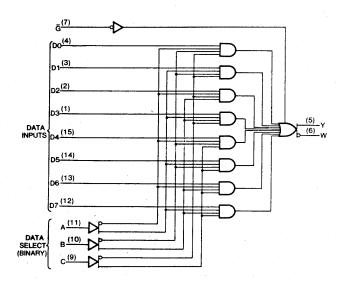
PIN CONFIGURATION



FUNCTION TABLE

		INP	OUT	PUTS	
SE	LEC	T	STROBE	٧	w
С	В	A	Ğ	·	••
Х	Х	Х	Н	Z	Z
Ŀ	L	L	L	DO	DO
L	L	Н	L	D1	D1
L	Н	L	L	D2	D2
L	Н	H	L	D3	ĎЗ
Н	L	L	L	D4	D4
H:	L	Н	L	D5	D5
Н	H	L	L	D6	D̄6
н	Н	Н	L	D7	D7

LOGIC DIAGRAM



KS54HCTLS **251** KS74HCTLS

1-of-8 Data Selectors/Multiplexers with 3-State Outputs

Absolute Maximum Ratings*

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vcc	;	4.5V to 5.5V
DC Input & Output '	Voltages*, V _{IN} ,	$V_{\mbox{\scriptsize OUT}}$ OV to $V_{\mbox{\scriptsize CC}}$
Operating Temperat	ure	
Range	KS74HCTLS:	-40°C to +85°C
	KS54HCTLS:	-55°C to +125°C
Input Rise & Fall Tin	nes, t _r , t _f	Max 500 ns

Unused inputs must always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55$ °C to +125°C	Unit
	-		Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr, tr 66 ns), HCTLS251

Characteristic	Symbol Conditions [†]		$T_a = 25^{\circ}0$ Conditions [†] $V_{CC} = 5.0$			KS74HCTLS $T_{a} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit	
			i.	Тур		Guarantee	d Limits		
Maximum Propagation Delay,	t _{PLH}	$C_L = 50p$ $C_L = 150$			40 46				
A, B or C to Y	t _{PHL}	C _L =50p C _L =150		20 23	26 29	33 38	40 46	ns	
Maximum Propagation Delay,	f _{PLH}	C _L =50p C _L =150		25 28	34 37	42 47	50 56		
A, B or C to W	t _{PHL}	C _L =50pF C _i =150pF		25 28	34 37	42 47	50 56	ns	
Maximum Propagation Delay,	t _{PLH}	$C_L=50pF$ $C_L=150pF$		11 14	15 18	19 24	22 28	ns	
Any D to Y	t _{PHL}	$C_L=50pF$ $C_L=150pF$		11 14	15 18	19 24	22 28		
Maximum Propagation Delay,	t _{PLH}	C_L =50pF C_L =150pF C_L =50pF C_L =150pF		17 20	22 25	28 33	33 39	ns	
Any D to W	t _{PHL}			17 20	22 25	28 33	33 39		
Maximum Output Enable Time,	t _{PZH}	$R_l = 1 k\Omega$	$C_L = 50pF$ $C_L = 150pF$	24 27	32 35	40 45	48 54	ns	
G to Y or W	t _{PZL}		C _L =50pF C _L =150pF	24 27	32 35	40 45	48 54		
Maximum Output Disable Time,	t _{PHZ}	$R_1 = 1 k\Omega$	C _L =50pF C _L =150pF	24 27	32 35	40 45	48 54	ns	
G to Y or W	t _{PLZ}		C _L =50pF C _L =150pF	24 27	32 35	40 45	48 54		
Maximum Input Capacitance	CIN			5				рF	
Maximum Output Capacitance	Cour	Output Disabled		10				рF	
Power Dissipation Capacitance*	C _{PD}			0				рF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in.}

[†] For AC switching test circuits and timing waveforms see section 2.

- . Three-State Version of '153
- . Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

 KSTAHOTI St. = 40°C to ± 85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe (\overline{G}) . The output is disabled when its strobe is high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

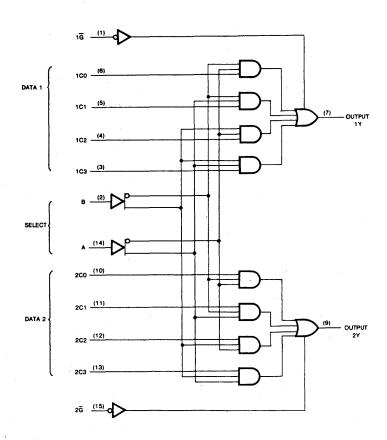
1Ğ	1 .	16	Vcc
в	2	15	□2Ğ
1C3 🗖	3	14	☐A
1C2	4	13	2 C3
101	5	12	202
1C0	6	11	201
17 🗖	7	10	2C0
GND	8	9]2Y
L			1

FUNCTION TABLE

SEL	SELECT		DATA INPUTS		OUTPUT CONTROL	ОИТРИТ	
В	Α	C0	C1	C2	C3	Ğ	Y
X	Х	Х	Х	Х	Х	Н	Z
L	L	L	Х	X	X	L.	L
L	L	Н	X	Х	X	L	н
L	Н	Х	L	Χ	Х	L	. L
L	H	Х	Н	Χ	X	Ł	H
Н	L	X	Х	L	X	L	L.
Н	L	X	X	Н	Х	44 L	н
Н	Н	Х	Χ	Х	L	L	· L
н	Н	X	Х	Χ	Н	L	. н

Address inputs A and B are common to both sections.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) + \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ $\pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vo	0	4.5V to 5.5	٧
DC Input & Output	Voltages*, V _{IN} ,	Vout OV to Vo	С
Operating Temperat	ure		
Range	KS74HCTLS:	-40°C to +85°	С
•	KS54HCTLS:	-55°C to +125°	С
Input Rise & Fall Tir	nes, t _r , t _f	Max 500 r	าร
Unused inputs mus	st always be tied	to an appropriate log	ic
voltage level (eith	er V _{CC} or GND)		



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Τ,	= 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH	20 - 50 21 - 50 2		2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20\mu A$ $I_O = -6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	VIN=VCC or GND		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS253

Characteristic	Symbol			T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
				Тур		Guarantee	d Limits	
Maximum Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF C _L =50pF C _L =150pF		24 27	32 35	40 45	48 54	200
A or B to Any Y	tpHL			24 27	32 35	40 45	48 54	ns
Maximum Propagation Delay, Data (any C) to any Y	tpLH	C _L =50pF C _L =150pF C _L =50pF C _L =150pF		15 18	20 23	25 30	30 36	- ns
	t _{PHL}			15 18	20 23	25 30	30 36	
Maximum Output Enable	t _{PZH}	Ri = 1kΩ	C _L =50pF C _L =150pF	17 20	22 25	28 33	33 39	
Time, G to Y		LIC IKE	C _L =50pF C _L =150pF	17 20	22 25	28 33	33 39	ns
Maximum Output Disable	tpHZ	$R_L = 1 k\Omega$		17	22	28	33	ns
Time, G to Y	tpLZ	C _L =50pi	F	17	22	28	33	
Maximum Input Capacitance	CiN			.5				pF
Maximum Output Capacitance	Cout	Output Disabled		10				pF
Power Dissipation Capacitance*	C _{PD}							pF

 $^{^{\}star}$ C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC} 2 f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.



KS54HCTLS **257/258** Quad 2-Line to 1-Line Data Selectors/KS74HCTLS **4 Multiplexers with 3-State Outputs**

FEATURES

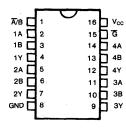
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface ■ Inputs and outputs interface directly with TTI NMOS
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '257 and '258 multiplex signals from for-bit data sources to four-output-data lines in bus organized systems. The data presented at the outputs is non-inverted for the '257 and inverted for the '258.

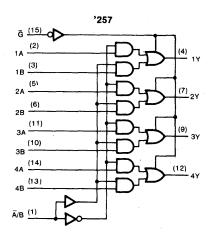
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

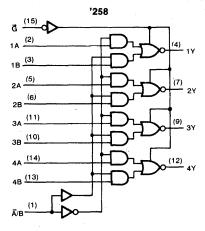
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

	Output Y				
Output Control	select	Da	ata	'257	'258
Ğ	Ā/B	Α.	В		
Н	Х	X	Х	Z	Z
L	L	L	Х	L	Н
L	L	H	Х	н	L
L	н	X	L	L	Н
L	н	X	н	H	L

LOGIC DIAGRAMS







KS54HCTLS **257/258** KS74HCTLS

Quad 2-Line to 1-Line Data Selectors/ Multiplexers with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to ± 150 °C
Power Dissipation Per Package, P _d [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V	cc 4.5V to 5.5V
DC Input & Output	it Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Temper	ature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall	Times, t _r , t _f Max 500 ns
•	ust always be tied to an appropriate logic
voitage level (ei	ther V _{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	ool Test Conditions		_a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	loc	V _{IN} =V _{CC} or GND I _{OUT} =0µA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA



KS54HCTLS **257/258** Quad 2-Line to 1-Line Data Selectors/KS74HCTLS **257/258** Quad 2-Line to 1-Line Data Selectors/

AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS257, HCTLS258

Characteristic	Symbol	Conditions†		T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Vnit
				Тур		Guarantee	Limits	
Maximum Propagation Delay,	t _{PLH}	C _L =50pl C _L =150		14 17	18 21	23 28	27 33	ns
A to B to any Y	t _{PHL}	C _L =50pl C _L =150		14 17	18 21	23 28	27 33	ns
Maximum Propagation Delay, Ā/B to any Y	tpLH	C _L =50pl C _L =150		16 19	21 24	26 31	31 37	ns
	t _{PHL}	C _L =50pl C _L =150		16 19	21 24	26 31	31 37	
Maximum Output Enable	t _{PZH}	$R_L = 1 k\Omega$	$C_L = 50pF$ $C_L = 150pF$	22 25	30 33	37 42	45 51	ns
Time, \overline{G} to any Y	tpzL		$C_L=50pF$ $C_L=150pF$	22 25	30 33	37 42	4 5 51	
Maximum Output Disable	t _{PHZ}	$R_L = 1 k\Omega$		20	27	34	41	ns
Time, G to any Y	tpLZ	C _L =50pl	=	20	27	34	41	
Maximum Input Capacitance	CIN			5				рF
Maximum Output Capacitance	C _{OUT}	Output D	isabled	10				ρF
Power Dissipation Capacitance*	C _{PD}							pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}{}^2 \ f_{in}$.



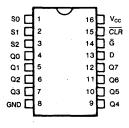
[†] For AC switching test circuits and timing waveforms see section 2.

- 8-Bit parallel-out storage register performs serial-toparallel conversion with storage
- · Asynchronous parallel clear
- Active high decoder
- Enable/Disable input simplifies expansion
- Expandable for N-bit applications
- Four distinct functional modes
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

inputs		Output of Addressed	Each Other	Function		
CLR	G	Latch	Output	ruiction		
Н	L	D	Qio	Addressable Latch		
н	Н	Q _{iO}	Qio	Memory		
L	L	D	L	8-Line Demultiplexer		
L	Н	L	L	Clear		

D = the level at the data input.

 Q_{iQ} = the level of Q_{iQ} (i = Q, 1, ... 7, as appropriate) before the indicated steady-state input conditions were established.

DESCRIPTION

The '259 is a high-speed addressable latch designed for general purpose storage applications in digital systems. It can be used for implementing working registers, serial-holding registers and active-high decoders or demultiplexers.

The '259 has four distinct modes of operation that are selected via the clear (CLR) and enable (G) inputs: 1) addressable latch; 2) memory; 3) active-high eight-channel demultiplexer; and 4) clear.

In the addressable latch mode, data on the data input (D) is written into the addressed latch. In this mode, data will be written into the addressed latch with all non-addressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous state and are unaffected by the data of address inputs.

In the demultiplexing mode, addressed outputs will follow the state of the D input and all other outputs will remain low.

In the clear mode, all outputs are low and unaffected by the address and data inputs.

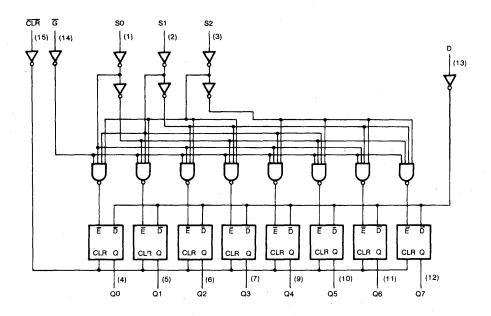
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LATCH SELECTION TABLE

Sel	ect Inp	Latch	
S2	S1	SO	Addressed
L	L	L	0
L	L	Н	1
L	Н	L	2
L	Н	Н	3
·H	L	L	4
н	L	н	5
Н	Н	L	6
Н	H .	Н	7

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Power Dissipation Per Package, Pd[†] 500 mW

Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	. •	
Supply Voltage, Vo	cc 4.5V to 5.5V	V
DC Input & Output	Voltages*, VIN, VOUT OV to VC	С
Operating Tempera	iture	
Range	KS74HCTLS: -40°C to +85°C	2
	KS54HCTLS: -55°C to +125°C	Э
Input Rise & Fall T	imes, t _r , t _f Max 500 ns	s
Unused inputs mu voltage level (eit	ist always be tied to an appropriate logic ner V_{CC} or GND)	С



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	tions T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit	
		<u> </u>	Тур		Guaranteed Lim	its		
Minimum High-Level Input Voltage	V _{iH}			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	Voh	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	V _{CC} 4.2	V _{CC} -0.1	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V .	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	o	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	. I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin $V_1=2.4V$ other inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS259

Characteristic				T _a = 25°C V _{CC} = 5.0V		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit
	•			Тур	Typ Guaranteed Limits			
Maximum Propagation	n Delay	t _{PHL}		22	30	37	45	ns
Maximum Propagation	n Delay,	t _{PLH}		20	27	34	41	ns
Data to Any Q		t _{PHL}		20	27	34	41	113
Maximum Propagation	Maximum Propagation Delay, Address to any Q		C _L =50pF	26	34	43	51	ns
Address to any Q				26	34	43	51	
Maximum Propagation	n Delay,	t _{PLH}		22	30	37	45	ns
G to any Q	·	t _{PHL}		22	30	37	45	
Minimum Pulse	CLR LOW	tw		8	10	13	15	ns
Width	G Low	"		8	10	13	15	
	Minimum Setup Time, Data or Address before G1			8	10	13	15	ns
Minimum Hold Time, Data or Address before G↑		t _h		-3	0	0	0	ns
Maximum Input Capa	acitance	CIN		5				pF
Power Dissipation C	apacitance*	C _{PD}		80				рF

 $^{^{\}star}$ C_{PD} determines the no-load dynamic power dissipation: PD=C_{PD} V_{CC²} f_{in}.



[†] For AC switching test circuits and timing waveforms see section 2.

Quad Exclusive-NOR Gates with Open-Drain Outputs

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74HCTLS: -40°C to +85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

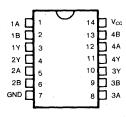
DESCRIPTION

These devices contain four independent exclusive-NOR gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

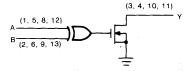
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

Inp	uts	Output			
A	В	Y			
L	L	Ή			
L	н	L			
Н	L	L			
Н	Н	Н			

Quad Exclusive-NOR Gates with Open-Drain Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
Vcc or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	V _{CC}	
DC Input & Outp	out Voltages*, V _{IN} , V _{OUT}	OV to Vcc
Operating Tempe		
Range	KS74HCTLS: -40	°C to +85°C
	KS54HCTLS: -55°	C to +125°C
Input Rise & Fall	Times, t_r , t_f	. Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	=25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
	•		Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	ViL			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА
Maximum Output Leakage Current	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tr 6 ns), HCTLS266

Characteristic	Symbol	Conditions†	$T_a = 25^{\circ}C$ $V_{CC} = 5.0V$		KS74 HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54 HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay	tpLH	C _L =50pF	18	25	31	37	ns
	tPHL	$R_L=1k\Omega$	16	22	28	33	
Maximum Input Capacitance	CiN		5				pF
Power Dissipation Capacitance*	C _{PD}	(per gate)	15				pF

CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

[†] For AC switching test circuits and timing waveforms see section 2.

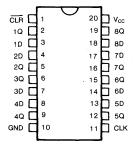


- Eight positive-edge-triggered D-type flip-flops with single-rail outputs
- . Buffered common clock and asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $(I_{OL} = 24mA @ V_{OL} = 0.5V)$ for direct bus Interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These devices are high-speed octal registers. They consist of eight positive-edge-triggered D-type flip-flops with individual D inputs and Q outputs. All flip flops are loaded and cleared simultaneously by the common buffered clock (CLK) and clear (CLR) inputs.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

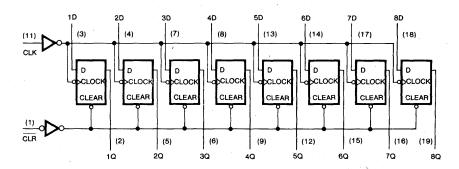
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(Each Flip-Flop)

li li	nputs	Output			
CLR	CLK	D	Q		
L	X	Χ	L		
н	1	н	н		
Н	↑	L	L		
н	L	Χ	Qo		

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} −65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long ex- posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vo	c 4.5V to 5.5V
DC Input & Output	Voltages*, VIN, VOUT OV to VCC
Operating Tempera	lure
Range	KS74HCTLS: -40°C to +85°C
-	KS54HCTLS: -55°C to +125°C
Input Rise & Fall Ti	mes, t _r , t _f Max 500 ns
Unused inputs mu voltage level (eith	st always be tied to an appropriate logic ner V _{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	1. [
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr 46 ns), HCTLS273

Chara	ncteristic	Symbol	Conditions†	T _a = 2 V _{CC} =		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
				Тур		Guaranteed	Limits	
Maximum Clock	Frequency	f _{max}	C _L =50pF	40	30	25	20	MHz
Maximum Propagation Delay,		t _{PLH}	C _L =50pF C _L =150pF	20 23	27 30	33 38	40 46	ns
		t _{PHL}	C _L =50pF C _L =150pF	20 23	27 30	33 38	40 46	115
Maximum Propa	agation Delay,	t _{PHL}	C _L =50pF C _L =150pF	20 23	27 30	33 38	40 46	ns
Minimum Pulse	CLR Low	tw	-	10	13	17	20	ns
Width	CLK High or Low	\ \w		10	13	17	20	113
Minimum Setup	Data	tsu		10	13	17	20	ns
Time before CLK†	Clear inactive State	'su		13	17	21	25	113
Minimum Hold Ti	me, Data after CLKf	th		-3	0	0	0	ns
Maximum Input	Capacitance	CIN		5				pF
Power Dissipati	on Capacitance*	C _{PD}	(per package)	150				рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in.}

 $[\]dagger$ For AC switching test circuits and timing waveforms see section 2.

- Generates Odd or Even Parity for Nine Data Lines
- Cascadable for N-Bits Parity
- Can be used to Upgrade Existing Systems using MSI Parity Circuits
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - ($I_{OL} = 24$ mA @ $V_{OL} = 0.5$ V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

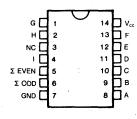
These universal, nine-bit parity generators/checkers feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

The devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker, Although the '280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the '280 to be substituted for the '180 in existing designs to produce an identical function even if the devices are mixed with existing '180's.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

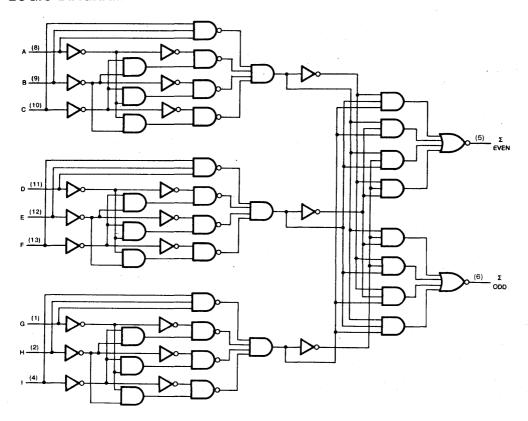
PIN CONFIGURATION



FUNCTION TABLE

NUMBER OF INPUTS A	OUTPUTS			
THRU I THAT ARE HIGH	Σ EVEN	ΣODD		
0,2,4,6,8	н	L		
1,3,4,5,9	L	Н		

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply voltage Hange V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, IIK
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS Ta = -55°C to +125°C	Unit			
			Тур		Guaranteed Limits					
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧			
Maximum Low-Level Input Voltage	VIL			ა.8	ა.8	0.8	٧			
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v			
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =12mA I _O =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v			
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ			
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ			
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs; at V _{CC} or GND I _{OUT} ≈0μA		2.7	2.9	3.0	mA			

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS280

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit	
	1		Тур		Guaranteed	Limits		
Maximum Propagation Delay,	PLH	C _L =50pF C _L =150pF	30 33	40 43	50 55	60 66	ns	
Anyinput to Σ Even	t _{PHL}	C _L =50pF C _L =150pF	30 33	40 43	50 55	60 66	,,,5	
Maximum Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	30 33	40 43	50 55	60 66	ns	
Any input to ΣOdd	t _{PHL}	C _L =50pF C _L =150pF	30 33	40 43	50 55	60 66	IIS	
Minimum Input Capacitance	CiN		5				pF	
Power Dissipation Capacitance*	CPD						pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-}



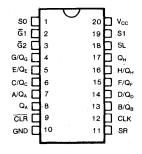
[†] For AC switching test circuits and timing waveforms see section 2.

- . Multiplexed I/O ports provides improved bit density
- Four modes of operation: hold (store), shift, shift left, and load data
- · Operates with outputs enabled or at high impedance
- · Can be cascaded for N-bit word lengths
- · Direct overriding clear
- Application:
 - Stacked or push-down registers, buffer storage, and accumulator registers
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- . Low power consumption characteristic of CMOS
- · 3-State outputs with drive current
- ($I_{OL} = 24 \text{ mA}$ @ $V_{OL} = 0.5 \text{V}$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

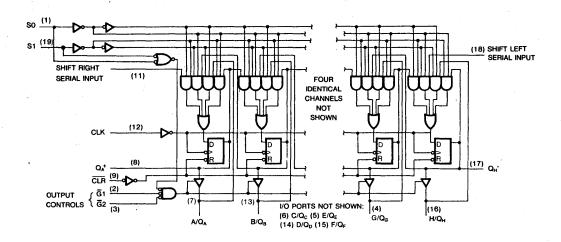
These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when $\overline{\text{CLR}}$ is low. Pulling either of the output controls, $\overline{\text{G1}}$ or $\overline{\text{G2}}$, high disables the outputs but this has no effect on clearing, shifting, or storage of data.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



FUNCTION TABLE

		Inputs								I/O Ports							Outputs	
Mode	CLR	S1	S0		put ntrol G2	CLK	SL	SR	A/Q _A	B/Q _B	C/Qc	D/Q _D	E/Q _E	F/Q _F	G/Q _G	H/Q _H	Q _A '	Q _H '
Clear	L L	X L	L X H	L L X	L L X	X X	X	X X X	L L X	L L X	L L X	L X	L L X	L X	L L X	L L X	L L L	L L
Hold	H	L X	L X	L L	L L	X L	X	X	Q _{AO}	Q _{BO}	Q _{C0}	Q_{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{но}		Q _{H0}
Shift Right	H	L L	H H	L L	L L	↑ ↑	X	H L	H L	Q _{An} Q _{An}	Q _{Bn} Q _{Bn}		Q_{Dn}		Q _{Fn} Q _{Fn}	Q _{Gn} Q _{Gn}	H	Q _{Gn} Q _{Gn}
Shift Left	H	HH	L	L	L	†	HL	X	Q _{Bn} Q _{Bn}	Q _{Cn} Q _{Cn}	Q _{Dn} Q _{Dn}	Q _{En} Q _{En}	Q _{Fn} Q _{Fn}	Q _{Gn} Q _{Gn}	Q _{Hn} Q _{Hn}	H L	Q _{Bn} Q _{Bn}	H
Load	Н	Н	Н	Х	Χ	1	Х	Χ	а	b	С	d	е	f	g	h	а	h

When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, V_{IN} , V_{OUT} . . OV to V_{CC} Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic S	Symbol	Test Conditions	T,	=25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T _a = -55°C to +125°C	Uni
			Тур		Guaranteed Limi	its	1
Minimum High-Level Input Voltage	V _{iH}			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-		V _{IN} =V _{IH} or V _{IL} I _O =-20μA Q' _A and Q' _H outputs:		V _{CC} -0.1	V _{CC} -0.1	V _{CC} -0.1	
	Voн	$I_O = -4mA$ $Q_A \text{ thru } Q_H \text{ outputs:}$ $I_O = -6mA$	4.2	3.98	3.84	3.7	\ \ \
Miximum		V _{IN} =V _{IH} or V _{IL} I _O =20μA Q' _A and Q' _H outputs:	0	0.1	0.1	0.1	
Low-Level Output Voltage	V _{OL}	I _O =4mA I _O =8mA Q _A thru Q _H outputs:		0.26 0.39	0.33 0.5	0.4	٧
		I _O =12mA I _O =24mA		0.26 0.39	0.33 0.5	0.4	
Maximum Input Current	IIN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА
Maximum 3-State Leakage Current	loz	Output Enable = V _{IN} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	ΔΙςς	per input pin V _I =2.4V other inputs: at V _{CC} or GND lout=0µA		2.7	2.9	3.0	mA



8-Bit Universal Shift/Storage Registers with 3-State Outputs

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS299

Cha	racteristic	Symbol	Con	Conditions [†]			KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit		
					Тур	Typ Guaranteed Limits					
Maximum Clo	ck Frequency	f _{max}	1		35	25	20	18	MHz		
Maximum Pro	pagation Delay.	tpLH			26	35	4	53	ns		
CLK to Q'A o		tpHL	C _L =5	60pF /	26	35	44	53	''3		
Maximum Pro	ppagation Delay, or Q' _H	t _{PHL}			30	40	50	60	ns		
		•	C _L =5	0pF	24	32	40	48			
Maximum Pro	pagation Delay,	tpLH	C _L =150pF		27	35	45	54	ns		
CLK to QA thru QH		tpHL	C _L =5	•	24	32	40	48			
		VENL	C _L =150pF		27	35	45	54	ļ		
Maximum Propagation Delay,		tpHL	$C_L = 50pF$ $C_1 = 150pF$		30	40	50	60	ns		
CLR to Q _a thru Q _H			C _L =1		33	43	55	66			
		tezn		C _L =50pF C _L =150pF	20	26 29	33 38	39 45	` *		
Maximum Ou G1, G2, to C	tput Enable Time,		$R_L=1k\Omega$	C ₁ = 50pF	20	26	33	39	ns		
G1, G2, 10 G	ex uno cen	t _{PZL}		$C_l = 50pF$ $C_l = 150pF$		29	38	45			
Maximum Ou	tput Disable Time.	tpHZ	$R_1 = 1k\Omega$		13	17	21	26			
G1, G2 to Q		tplZ	$R_L = 1 k u$ $C_1 = 50 pF$		13	17	21	26	ns		
Minimum	CLK High or Low				10	13	17	20			
Pulse Width	CLR Low	t _w			10	13	17	20	ns		
	S0 and S1				13	17	21	25			
Minimum	High-Level Inputs	.			10	13	17	20	1		
Setup time before CLK1	High-Level Inputs	t _{su}			10	13	17	20	ns		
Deloie CLK	CLR Inactive				10	13	17	20	1.		
Minimum Hold Time	S0 and S1	th			5	7	8	10	ns		
after CLK† All Inputs					0	0	0	0			
Maximum Inp	ut Capacitance	CIN				5			pF		
Maximum Ou	tput Capacitance	Cout	Outpo	ut Disabled		10			рF		
Power Dissip	ation Capacitance*	C _{PD}						1	pF		

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-}

[†] For AC switching test circuits and timing waveforms see section 2.

5

FEATURES

- Multiplexed inputs/outputs provide improved bit density
- Sign extend function
- . Direct overriding clear
- · 3 state outputs drive bus lines directly
- Function pin-out, speed and drive compatibility with 54/74 LS logic family
- Low power consumption characteristic of CMOS
- · High drive current output
- $(I_{OL} = 24 \text{mA} \otimes V_{OL} = 0.5 \text{V})$ for for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices.
- Wide Operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature range:

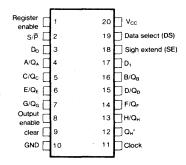
KS74HCTLS: -40°C to +85° KS54HCTLS: -55°C to +125°

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

DESCRIPTION

These 8 bit Shift registers have multiplexed input/output data ports to accomplish full 8-bit data handling in a single 20-pin package. Serial data may enter the shift-right register through either D_0 or D_1 input as selected by the data select pin. A serial output is also provided. Synchronous parallel loading is achieved by taking the register enable and the S/P inputs low. This places the three-state input/output ports in the data input mode. Data are entered on the low-to-high clock transition. The data extend function repeats the sign in the Q_A flip flop during shifting. An overriding clear input clears the internal register when taken low whether the outputs are enabled or off. The output enable does not affect synchronous operation of the register.

PIN CONFIGURATION



FUNCTION TABLE

•				INPUT	1							
OPERATION	Clear	Register enable	S/P	Sign extend	Data select	Output enable	Clock	A/Q _A	B/Q _B	C/Qc ·	H/Q _H	Output Q _H '
Clear	L	Н	Х	х	Х	L	Х	L	L	L	L	L
<u>.</u>	L	X	H	X	X	L	X	L	L	L	L	L
Hold	Н	Н	х	х	X	L	Х	Q _{AO}	Q _{BO}	Qco	Q _{HO}	Q _{HO}
Shift Right	Н	L	Н	Н	L	L	Ť	Do	Q _{An}	Q _{Bn}	Q _{Gn}	Q _{Gn}
Shirt right	Н	L	Н	Н	Н	L	1	Dı	Q_{An}	Q_{Bn}	Q_{GN}	Q _{Gn}
Sign Extend	Н	L	Н	L	X	L	1	Q _{An}	Q _{An}	Q _{Bn}	Q _{Gn}	Q _{Gn}
Load	н	L	L	Х	Х	Х	1	а	b	С	h	h

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state: however, sequential operation or clearing of the register is not affected. If both the register enable input and the S/P input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

H= high level (steady state)

L= low level (steady state)

X= irrelevant (any inputs, including transitions)

↑ = transition from low to high level

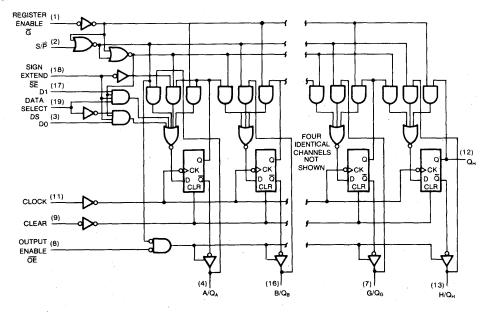
QAo...QHo= the level of QA through QH, respectively, before the indicated steady-state conditions were established.

Q_{An...Q_{Hn}= the level of Q_A through Q_H, respectively, before the most recent † transition of the clock.}

Do, D1= the level of steady-state inputs at inputs Do and D1 respectively

a...h= the level of steady-state inputs at input A through H respectively.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_i < -0.5V \text{ or } V_i > V_{CC} + 0.5V) \dots \pm 20 \text{ r}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Patings are those values bound

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Range KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	nditions T _a :		KS74AHCT T _a = -40°C to +85°C	KS54AHCT Ta = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	Vон	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1. 3.84	V _{CC} -0.1	٧
Maximum Low-Level Output Voltage	VoL	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l _{IN}	VIN=VCC or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS322A

Characteristic		Symbol	Conditions [†]	1 "	25°C = 5.0V	KS74HCTLS T _A = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _A = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit		
			ı	Тур		Guaranteed	Limits	7		
Maximum Clock Frequenc	у	f _{max}	,	40	30	25	20	MHz		
Maximum Propagation		tpHL		22	33	41	50	ns		
Delay, Clock to QH'		t _{PLH}		22	33	41	50 -	113		
Maximum Propagation Delay, Clear to Q _H '		t _{PHL}	C _L =50pF	27	35	44	53	ns		
Maximum Propagation		t _{PHL}		22	33	41	50	ne		
Delay, Clock to QA-QH		tpLH		16	25	31	38	ns		
Propagation Delay Clear to Q _A -Q _H		tpHL	IL I	22	35	44	53	ns		
Output Enable Time		tpzH	$R_1 = 1 k \Omega$	15	35	44	53	ns		
Output Enable Time		tpZL	C _L =50pF	15	35	. 44	53			
Output Disable Time		t _{PHZ}	OL-30bi	15	25	31	38	ns.		
Output Disable Time		tpLZ		15	25	31	38	113.		
Clock Pulse	High	tw		12	16	20	24	ns		
Width	Low	tw		12	16	20	24	113		
Clear Pulse Width Low		tw		12	16	20	. 24	ns		
Minimum Data Set up Time	e	ts		13	16	20	25	ns		
Minimum Select Set up Time		ts		13	16	20	25	113		
Minimum Data Hold Time		th		-3	0	0	0	ns		
Minimum Select Hold Time		th		7	10	12	15	113		
Minimum Recovery Time		t _{rec}		15	20	25	30	ns		
Maximum Input Capacitano	ce	Cin		5				ρF		
Power Dissipation Capacit	ance	C _{PD}		100				рF		

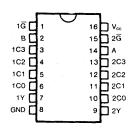
^{*} Cpp determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

- Inverting Version of '153
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

SEL	ECT	DA	DATA INPUTS		STROBE	OUTPUT		
В	A	CO	C1	C2	СЗ	Ğ	Υ	
X	Χ	Х	Х	Χ	Х	Н	Н	
L	L	L	Χ	X	X	L	H	
L	L.	Н	Χ	Χ	Χ	L	: L	
L	Н	X	L	X	Χ	L	Н	
L	Н	Х	Н	Х	Χ	L	L	
H	L.	Х	Х	L	X	L	н	
H	L	X	Х	Н	Χ.	L	L	
Н	·H	X	Х	Х	L	L	H	
Н	Н	X	Χ	Χ	Н	L	. L	

Select inputs A and B are common to both sections.

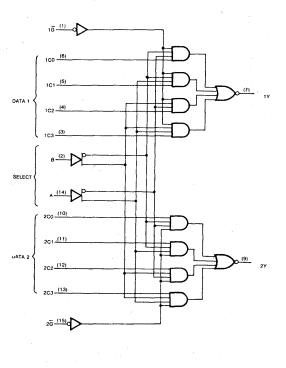
DESCRIPTION

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\bar{\mathbf{G}}$) are provided for each of the two four-line sections.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} , -0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
Vcc or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vo	c 4.5V to 5.5V
DC Input & Output	Voltages*, V _{IN} , V _{OUT} 0V to V _{CC}
Operating Tempera	ture
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall Ti	nes, t _r , t _f Max 500 ns
	st always be tied to an appropriate logic

Characteristic	Symbol	ymbol Test Conditions		a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit		
			Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	v		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_{O}=-20\mu\text{A}$ $I_{O}=-6\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1 3.7	v		
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μА		
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_i≤6 ns), HCTLS352

Characteristic	Symbol	ol Conditions†		25°C = 5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay, A or B to Y	t _{PLH}	$C_L = 50pF$ $C_L = 150pF$	23 26	30 33	38 43	45 51	ns
	t _{PHL}	C _L =50pF C _L =150pF	23 26	30 33	38 43	45 51	113
Maximum Propagation Delay,	t _{PLH}	$C_L = 50pF$ $C_L = 150pF$	19 21	26 29	32 37	39 45	ns
Data (Any C) to Y	t _{PHL}	$C_L=50pF$ $C_L=150pF$	19 21	26 29	32 37	39 45	115
Maximum Propagation Delay,	t _{PLH}	$C_L=50pF$ $C_L=150pF$	19 21	26 29	32 37	39 45	- ns
G to Y	t _{PHL}	$C_L=50pF$ $C_L=150pF$	19 21	26 29	32 37	39 45	
Maximum Input Capacitance	CiN			5			pF
Power Dissipation Capacitance*	C _{PD}						pF

 $^{^{\}star}$ C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-}

 $[\]uparrow$ For AC switching test circuits and timing waveforms see section 2.

- Inverting Version of '253
- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

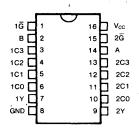
Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs $(\bar{\mathbf{G}})$ are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe (\vec{G}) . The output is disabled when its strobe is high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

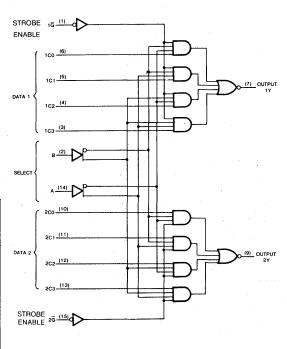


FUNCTION TABLE

SEL	SELECT		DATA INPUTS		OUTPUT CONTROL	ОИТРИТ	
В	A	CO	C1	C2	СЗ	Ğ	Y
×	X	X	Χ	X	Х	Н	Z
L	L	L	Χ	Χ	Х	L	Н
L	L	Н	Χ	X	X	L	L
L	Н	Х	L	Х	X	L	Н
L	Н	X	Н	Х	Χ	' L	L
Н	· L	X	X	L	Χ	L	Н
Н	L	X	Χ	H	Χ	L	L
Н	H.	X	X	Χ	L	L	H
H	Н	X	Χ	Χ	Н	L	L

Select inputs A and B are common to both sections.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, Inc
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I _{OK}
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
 Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, Vo	cc 4.5V to 5.5V
DC Input & Output	Voltages*, VIN, VOUT OV to VCC
Operating Tempera	
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall T	imes, t _r , t _f Max 500 ns
Unused inputs mu voltage level (eit	st always be tied to an appropriate logic ner V _{CC} or GND)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_O = -20\mu\text{A}$ = -6mA	V _{CC} 4.2	V _{CC} −0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current		per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr. tre6 ns), HCTLS353

Characteristic	Symbol	Condition	_	25°C = 5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit	
						Guarantee	d Limits	1
Maximum Propagation Delay,	t _{PLH}	C _L =50pl C _L =150		24 27	32 35	40 45	48 54	ne
A or B to Any Y	t _{PHL}	C _L =50pl C _L =150	24 27	32 35	40 45	48 54	ns	
Maximum Propagation Delay,	t _{PLH}	C _L =50pl C _L =150	15 18	20 23	25 30	30 36	ns	
Data (any C) to any Y	t _{PHL}	C _L =50p C _L =150	15 18	20 23	26 31	31 37		
Maximum Output Enable	t _{PZH}	$R_L = 1 k\Omega$	C _L =50pF C _L =150pF	17 20	23 26	29 34	35 41	- ns
Time, G to Y	t _{PZL}		C _L =50pF C _L =150pF	17 20	23 26	29 34	35 41	
Maximum Output Disable Time, G to Y	t _{PHZ}	$R_L = 1 k\Omega$ $C_L = 50 pc$	_		27 27	34	41	ns
Maximum Input Capacitance	Cin			20 5				pF
Maximum Output Capacitance				10				pF
Power Dissipation Capacitance*	C _{PD}							pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

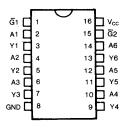
These high-speed Hex bus drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus oriented receivers and transmitters.

The '365 and '366 have two output enables ($\overline{G}1$ and $\overline{G}2$) NOR'ed together to control all six gates. The '367 and '368 have two output enables which are configured so that one enable ($\overline{G}1$) controls four gates and the other ($\overline{G}2$) controls the remaining two gates. The '366 and '368 have inverting data paths. The '365 and '367 have noninverting data paths.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLES

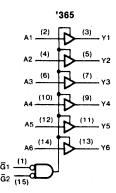
'365 and '366

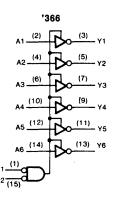
	Inputs	3	Y Outputs		
Ğ	ı Ğ2	A	'365	'366	
L	L	L	L	Н	
L	L	Н	н	L	
Н	Х	X	Z	Z	
X	Н	X	Z	Z	

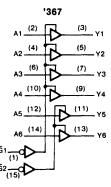
'367 and '368

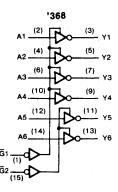
	Inp	outs		Y Outputs				
Ğ1	&	Ğ2	A	'367	'368			
	L	,	L	L	Н			
	L		Н	н	L			
	Н		Х	Z	Z			

LOGIC DIAGRAMS











KS54HCTLS 365A/366A KS74HCTLS 367A/368A

Hex Bus-Drivers with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage,	Vcc		4.5V	to 5.5V
DC Input & Outp	out Voltages*, V _{IN} ,	V_{OUT}	0\	/ to V _{CC}
Operating Tempe	erature			
Dongo	KCZALICTI C.	40	00 4-	10500

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

KS54HCTLS 365A/366A KS74HCTLS 367A/368A

Hex Bus-Drivers with 3-State Outputs

AC ELECTRICAL CHARACTERISTICS (Input tr., tres ns), HCTLS365A, HCTLS367A

Characteristic	Symbol	Symbol Conditions†		T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
				Тур		Guarantee	d Limits	
Maximum Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF C _L =50pF C _L =150pF		14 17	19 22	24 29	28 34	ns
A to Y	t _{PHL}			14 17	19 22	24 29	28 34	
Maximum Output Enable	t _{PZH}	$R_i = 1 k\Omega$	C _L =50pF C _L =150pF	26 29	35 38	44 49	52 58	ns
Time, G to Y	· t _{PZL}	11[-1142	C _L =50pF C _L =150pF	26 29	35 38	44 49	52 58	113
Maximum Output Disable	t _{PHZ}	$R_L = 1 k\Omega$		26	35	44	52	ns
Time, G to Y	t _{PLZ}	C _L =50pF		26	35	44	52	113
Maximum Input Capacitance	CIN			5				рF
Maximum Output Capacitance	Cout	Output disabled		10				рF
Power Dissipation Capacitance* (per driver)	C _{PD}	G=V _{CC} G=GND		5 30				pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$

AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS366A, HCTLS368A

Characteristic	Symbol	Conditions ¹		T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS $T_{a} = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit
·				Тур		Guarantee	d Limits	
Maximum Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF C _L =50pF C _I =150pF		13 16	17 20	21 26	25 31	ns
A to Y	t _{PHL}			13 16	17 20	21 26	25 31	
Maximum Output Enable	t _{PZH}	B. = 1k0	C _L =50pF C _L =150pF	26 29	35 38	44 49	52 58	ns
Time, G to Y	t _{PZL}	11[-1/42	C _L =50pF C _L =150pF	26 29	35 38	44 49	52 58	113
Maximum Output Disable	t _{PHZ}	R _L =1kΩ C _L =50pF		26	35	44	52	ns
Time, \overline{G} to Y	tPLZ			26	35	44	52	
Maximum Input Capacitance	CIN			5				pF
Maximum Output Capacitance	Cout	Output disabled		10				pF
Power Dissipation Capacitance* (per driver)	C _{PD}	$\overline{G} = V_{CC}$ $\overline{G} = GND$		5 30				pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD}$, $V_{CC}{}^2$ f_{in} .



[†] For AC switching test circuits and timing waveforms see section 2.

[†] For AC switching test circuits and timing waveforms see section 2.

Octal D-Type Transparent Latches with 3-State Outputs

FEATURES

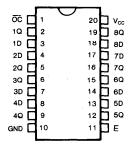
- · 8 latches in a single package
- · Full parallel access for loading
- · Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- · 3-State outputs with high drive current
- · Inputs and outputs interface directly with TTL. NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '373 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (E) is high, the Q outputs follow the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (OC) which places the outputs at a high-impedance state when it is taken high. The $\overline{\text{OC}}$ signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL. NMOS and CMOS devices without any external components.

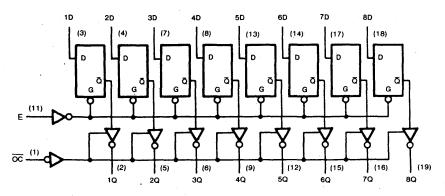
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(Each Latch)

	Inputs	Output	
oc	E	D	Q
L	Н	н	Н
L	Н	Ĺ	L
L	L	Х	Q_0
Н	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage, '	/cc 4.5V to 5.5V
DC Input & Outp	ut Voltages*, VIN, VOUT OV to VCC
Operating Tempe	rature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall	Times, t_r , t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	ymbol Test Conditions		A = 25°C	KS74HCTLS $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_A = -55$ °C to +125°C	Unit	
			Тур	Guaranteed Limits				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	v	
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	V _{CC}	V _{CC} -0.1	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	V	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN} = V_{IH}$ or V_{IL} $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
Maximum Input Current	Jin	V _{IN} =V _{CC} or GND		±0.1	±1.0′	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin Vz=2.4V Other Inputs: At Vcc or GND Io=0		2.7	2.9	3.0	mA	

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS373

Characteristic	Symbol	Cenditions†		T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _e = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
				Тур		Guarantee	d Limits	1
Maximum Propagation Delay,	tpLH	C _L = 50 C _L ∓150		14 17	18 21	23 28	27 33	ns
D to Q	t _{PHL}	C _L =50p C _L =150		14 17	18 21	23 28	27 33	
Maximum Propagation Delay.	tplH	C _L =50pt C _L =150		22 25	30 33	37 42	45 51	
E to any Q	t _{PHL}	C _L =50pF C _L =150pF		22 25	30 33	37 42	45 51	ns
Maximum Output Enable	t _{PZH}	$B_L = 1 k\Omega$	C _L =50pF C _L =150pF	24 27	32 35	40 45	48 54	ns
Time, OC to any Q	t _{PZL}		C _L =50pF C _L =150pF	24 27	32 35	40 45	48 54	
Maximum Output Disable Time, OC to any Q	t _{PHZ}	R _L =1kΩ C _L =50p		19 19	25 25	31 31	37 37	ns
Minimum Pulse Width, E High	tw			6	10	12	15	ns
Minimum Setup Time, D before E↓	t _{su}			2	3	4	5	ns
Minimum Hold Time, D after E↓	th		,	6	10	12	15	ns
Maximum Input Capacitance	CIN			5				рF
Maximum Output Capacitance	Соит	Output D	isabled	10				pF
Power Dissipation Capacitance* (per latch)	C _{PD}	OC=Vcc		5 30				рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in-}



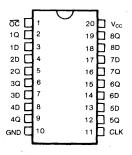
[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
 (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '374 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

The flip-flops are edge-triggered on the positive transition of the clock. The Q outputs are set to the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal (\overline{OC}) which places the outputs at a high-impedance state when it is taken high. The \overline{OC} signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

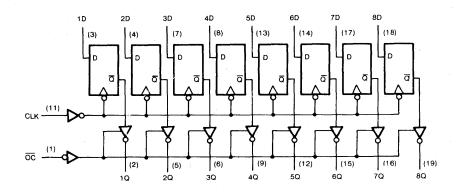
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(Each Flip-Flop)

1	nputs	Output	
ōc	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	Χ	Q_0
Н	X	Х	Z

LOGIC DIAGRAM





Absolute Maximum Ratings*

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage	, V _{CC}	. 4.5V to 5.5V
DC Input & Out	tput Voltages*, V _{IN} , V _{OUT}	OV to Vcc
Operating Temp	perature	
Range	KS74HCTLS: -40	0°C to +85°C
	KS54HCTLS: -55	°C to +125°C
Input Rise & Fa	all Times, t _r , t _f	Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS KS54HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $T_a = -55^{\circ}\text{C to } +125^{\circ}\text{C}$		Unit
			Тур		its		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	٧
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0µA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS374

Characteristic	Characteristic Symbol Co				25°C 5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit	
				Тур	p Guaranteed Limits				
Maximum Operating Frequency	f _{max}	C _L =50pF		45	35	30	25	MHz	
Maximum Propagation Delay,	t _{PLH}	C _L =50p C _L =150		21 24	28 31	35 40	42 48	ns	
CLK to any Q	t _{PHL}		C _L =50pF C _L =150pF		28 31	35 40	42 48	113	
Maximum Output Disable Time, OC to any Q	t _{PZH}	$R_{L} = 1 k\Omega$	C _L =50pF C _L =150pF	21 24	28 31	35 40	42 48	ns	
	t _{PZL}	HI - IKI	C _L =50pF C _L =150pF	21 24	28 31	35 40	42 48	"15	
Maximum Output Disable	t _{PHZ}	R _L =1kΩ C _L =50pF		19	25	31	37	ns	
Time, OC to any Q	t _{PLZ}			19	25	31	37	113	
Minimum Pulse Width, CLK High or Low	t _w			7	10	12	15	กร	
Minimum Setup Time, D before CLKt	t _{su}			10	13	17	20	ns	
Minimum Hold Time, D after CLK†	t _h			-3	0	0	0	ns	
Maximum Input Capacitance	CIN			5				pF	
Maximum Output Capacitance	Соит	Output Disabled		10				рF	
Power Dissipation Capacitance* (per stage)	C _{PD}	OC=V _{CC} OC=GNI		5 30				pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

- · Can be used for implementing
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5 \text{V}$
- . Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges: KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

· Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

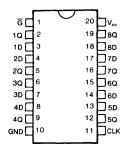
The '377 contains eight positive-edge-triggered D-type flipflops with an enable input. This part is similar to '273 but features a latched clock enable (G) instead of a common

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positivegoing edge of the clock pulse if G is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitioins at the G input.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

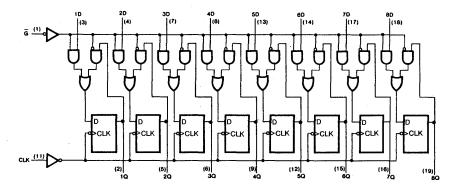


FUNCTION TABLE

(EACH FLIP-FLOP)

	INPU	OUTPUT	
Ğ	CLK	DATA	Q
Н	Х	X	Qo
L	Ť	н	н
L	†	L	L
X	L,	X	Qo

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, P _d [†] 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to V_{CC}
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
.Unused inputs must always be tied to an appropriate logic

unused inputs must always be tied to an appropriate ic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	Т	_a = 25°C	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{ОН}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δl _{CC}	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA



[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS377

Characteristic		Symbol	l Conditions [↑]	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
		1		Typ Guaranteed Limits				
Maximum Clock Fr	equency	f _{max}		45	35	30	25	MHz
Maximum Propaga	Maximum Propagation Delay, CLK to Any Q		C ₁ = 50pF	18	27	32	38	ns
CLK to Any Q			CL-30pi	18	27	32	38	
Minimum	G Low	t _w		12	16	20	25	ns
Pulse Width	CLK high or Low			12	16	20	25	115
Minimum Setup	Data			6	10	15	20	ns
Time before CLK1	G high or LOW	tsu		15	20	25	25	1115
Minimum Hold Time Data after CLK1	e,	th		-3	0	0	0	ns
Maximum Input Capacitance		CIN		5				рF
Power Dissipation	Capacitance*	C _{PD}						pF

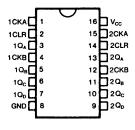
^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$. † For AC switching test circuits and timing waveforms see section 2.

- Individual clock for A and B flip-flops provide dual ÷2 and ÷5 counters
- · Direct clear for each 4-bit counter
- Significant provement in system density through reduced counter package count.
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These devices incorporate dual divide-by-two and divide-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiple of 2 and/or 5 up to divide-by-100. When connected as a biquinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square ware) at the final outpur stage. The '390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-tow circuit can be used to provide symmetry (a square wave) at the final outpur stage. The '390 has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

BCD COUNT SEQUENCE (Each Counter) (See Note A)

COUNT		OUTPUT						
000111	QD	$\mathbf{Q}_{\mathbf{C}}$	QB	QA				
0	L	L	L	L				
1	L	L	L	Н				
2	L	L	Н	L				
3	L	L	Н	H				
4	L	Н	L	L				
5	'L	Н	L	Н				
6		Н	Н	L				
7	L	Н	Н	Н				
8	Н	Ĺ	L	L				
9	Н	L	L	Н				

BIQUINARY (5-2) (Each Counter) (See Note B)

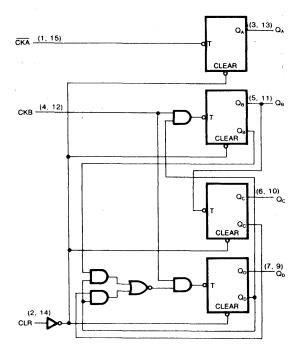
COUNT		OUTPUT						
COOM	QD	Qc	QB	QA				
0	L	L	L	L				
1	L	L	L	Н				
2	L	L	Н	L				
3	L	L	Н	Н				
4	L	Н	L	L				
5 .	Н	L	L	L				
6	Н	L	L	Н				
7	Н	L	Н	· L				
8	Н	L	Н	ıΗ				
9	Н	Н	L	L				

NOTES A. Output QA is connected to input CKB for BCD count.

B. Output QD is connected to input CKA for biquinary count.



LOGIC DIAGRAM



Absolute Maximum Ratings*

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output V	$'$ oltages * , V_{IN} , V_{OUT} OV to V_{CC}
Operating Temperatu	ıre ·
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55 °C to $+125$ °C
Input Rise & Fall Tim	es, t _r , t _f Max 500 ns
Unused inputs must	always be tied to an appropriate logic

voltage level (either V_{CC} or GND)



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic S	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	. V _{CC} -0.1	V _{CC} -0.1 3.7	٧
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr 66 ns), HCTLS390

Characteristic		Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		$KS74HCTLS$ $T_a = -40 °C to +85 °C$ $V_{CC} = 5.0 V \pm 10 %$	$KS54HCTLS$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit	
				15 15 36 36 36 0pF		Guaranteed	l Limits		
1	ock Frequency or CKB to Q _B	f _{max}		35	25	20	20	MHz	
Maximum Pr	opagation Delay,	tpLH		15	20	25	30	ns	
CKA to Q _A		t _{PHL}		15	20	25	30	110	
Maximum Pr	opagation Delay,	t _{PLH}		36	48	60	72	ns	
CKA to Q _C		t _{PHL}	Cı =50pF	36	48	60	72	"	
Maximum Pr	Maximum Propagation Delay, CKB to Q _B			16	21	26	31	ns	
CKB to Q _B			OL GOD!	16	21	26	31		
Maximum Pr	opagation Delay,	t _{PLH}		24	32	40	48	ns	
CKB to Q _C		t _{PHL}		24	32	40	48		
Maximum Pr	opagation Delay,	t _{PLH}	,	16	21	26	31		
CKB to Q _D		t _{PHL}		16	21	26	31		
Maximum Pr CLR to Any	opagation Delay, Q	t _{PHL}		24	32	40	48	ns	
Minimum	CKA or CKB high or low	t _{su}		12	16	20	24	ns	
Pulse Width	ulse Width CLR high			12	16	20	24	113	
Minimum Setup Time, CLR inactive before CKA or CKB		t _{su}		15	20	25	30	ns	
Maximum Inp	out Capacitance	CIN		5				рF	
Power Dissip	oation Capocitance	C _{PD}						рF	

 $^{^{\}star}$ C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC} 2 f_{in-}

[†] For AC switching test circuits and timing waveforms see section 2.



KS54HCTLS 393

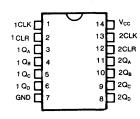
FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 - IoL = 8 mA @ VoL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

• Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



LOGIC TIMING WAVEFORMS

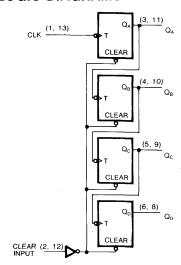
DESCRIPTION

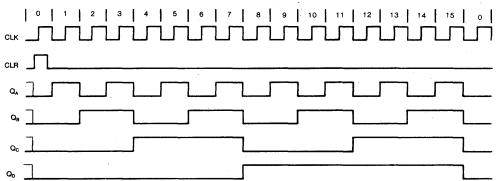
The '393 consists of two independent 4-bit binary counters each with its own clear and clock inputs. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. Parallel outputs from each counter stage provide any submultiple of the input count frequency for system timing signals.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAMS





Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.
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[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage,	V _{CC} 4.5V to 5.5V
DC Input & Outp	out Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Temp	erature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic
voltage level (either V_{CC} or GND)

Characteristic	Symbol	Symbol Test Conditions		a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T _a = -55°C to +125°C	Unit
		-	Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =ΟμΑ		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _i =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_{r.} t_f<6 ns), HCTLS393

Characteristic		Symbol				$KS74HCTLS$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTL\$ T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
				Тур		Guarantee	d Limits	
Maximum Clock	Frequency	f _{max}		40	30	25	20	MHz
Maximum Propa	agation Delay,	tpLH		15	20	25	30	ns
A to Q _A		tpHL		15	20	25	30	113
Maximum Propa	agation Delay,	tpLH	·	26	35	44	53	ns
A to Q _B		tpHL	C _L =50pF	26	35	44	53	115
Maximum Propagation Delay,		tpLH	OL-SOPE	34	45	56	67	ns
A to Q _C		t _{PHL}		34	45	56	67	113
Maximum Propa	agation Delay,	t _{PLH}		45	60	75	90	ns
A to Q _D		t _{PHL}		45	60	75	90	113
Maximum Propa	agation Delay,	t _{PHL}		29	39	49	58	ns
Minimum Pulse	A Input High or Low	tw		10	13	17	20	ns
Width				10	13	17	20	113
Minimum Hold Time, CLR Inactive before A		t _{su}		10	13	17	20	ns
Maximum Input	Capacitance	CIN		5				pF
Power Dissipati	on Capacitance*	C _{PD}	(per counter)	40				рF

 $^{^{\}star}$ C_{PD} determines the no-load dynamic power dissipation: PD=C_{PD} V_{CC} 2 fin.

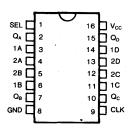
[†] For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These are high-speed quad 2-port registers. They are the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A common select input (SEL) selects between two 4-bit input ports. The selected data is transferred to the output register on the low-to-high transition of the clock input.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

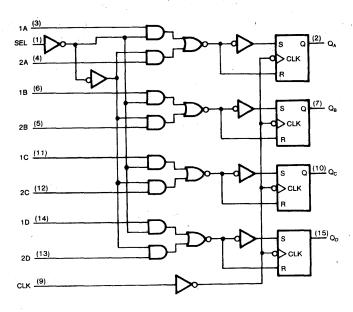
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

	Inputs						
SEL	Port 1	Port 2	Q				
. 1	1 .	х	L				
1	h	Х	Н				
h	Х	1	L				
h	×	h	Н				

- I = Low Voltage Level one setup time prior to the low-to-high clock transition
- h = High Voltage Level one setup time prior to the low-to-high clock transition

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_l < -0.5V \text{ or } V_l > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, Iok
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, V _{IN} , V _{OUT}	OV to Vcc
Operating Temperature	

voltage level (either V_{CC} or GND)



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta = 25°C		KS74HCTLS KS54HCTLS T _a = -40°C to +85°C T _a = -55°C to +		Unit
	77		Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	٧
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, ti 6 ns), HCTLS399

Character	istic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	$KS54HCTLS$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Тур		Guaranteed	Limits	
Propagation Delay,		t _{PLH}	C _L =50pF	22	30	37	45	ns
CLK to Q or Q		t _{PHL}	CL-SOPE	22	30	37	45	115
Minimum Pulse Width, CLK High or Low		t _w		10	13	17	20	ns
Minimum Setup	Data			10	13	17	20	
Time before CLK1	Word Select	t _{su}		10	13	17	20	ns
Minimum Hold	Data			-3	0	0	0	
Time after CLK1	Word Select	t _h		-3	0	0	0	ns
Maximum Input Capacitance		CIN		5				pF
Power Dissipation Capacitance*		C _{PD}					. 25	рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

- Simple pulse width formula tw = 0.45RC
- . DC triggered from active HIGH or active Low inputs
- Retriggerable for very long output pulses up to 100% duty cycle
- . Overriding clear terminates output pulse
- Schmitt trigger A & B inputs allow infinite rise and fall times on these inputs
- Functions, pin-out, speed and drive compativility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs:
 - IOL = 8mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range; 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

The '423 contains dual retriggerable monostable multivibrators with output pulsewidth control by two methods. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}). The external resistor and capacitor are normally connected as shown timing component.

Once triggered, the basic output pulse width may be extended by retriggering the gated active Low-going edge input (Ai) or the active High-going edge input (Bi). By repeating this process, the output pulse period (nQ=HIGH, $n\overline{Q}=LOW$) can be made as long as desired.

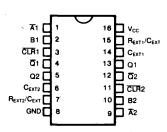
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques.

The output pulse equation is simply;

 $t_W=0.45\times R_{EXT}\times C_{EXT}(typ)$.

Where t_w is in seconds. R is in ohm. and C is in fards. All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLE

	Inputs	Out	puts	
CLR	Ā	В	Q	ত
L	Х	X	L	Н
Χ	• н	Х	L	н
Χ	x	L	[· L	н
Н	L	†	1	Ծ.
Н	↓ ↓	Н		ᅶ

H= HIGH voltage level

L= LOW voltage level

X= don't care

↑= LOW to HIGH transition

↓= HIGH to LOW transition

□ one LOW level output pulse

Absolute Maximum Ratings*

† Power Dissipation temperature derating: Plastic Package(N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	, V _{CC} 4.5V to 5.5V
DC Input & Out	put Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Temp	perature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fa	Ill Times, t _r , t _f Max 500 ns
Unused inputs	must always be tied to an appropriate logic
voltage level	(either V _{CC} or GND)

Characteristic	Symbol	Symbol Test Conditions		nbol Test Conditions		= 25°C	KS74HCTLS KS54HCTLS T _a = -40°C to +85°C T _a = -55°C to +125°		
			Тур		Guaranteed Lim	its			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	,V		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v		
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	o	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА		
Maximum Quiescent Supply Current	1 100	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input in V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤6 ns), HCTLS423

Characteristic	Symbol	Conditions†	$T_a = 25$ °C $V_{CC} = 5.0$ V		KS74AHCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54AHCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
					Guaranteed	Limits	7
Propagation Delay	t _{PLH}		23	33	41	50	ns
Ā, B to Q, Q	t _{PHL}	C ₁ = 50pF	23	33	41	50]
Propagation Delay	tpLH	C _{ext} =0,	20	27	34	41	ns
CLR to Q, Q	t _{PHL}	R _{ext} =5k Ω	20	27	34	41] '''
Output Pulse Width 1	twq1		116	200	207	209	ns
Output Pulse Width 2	two2	C_L =50pF C_{ext} =10nF R_{ext} =10k Ω	45	40 50	38(min) 52(max)	27(min) 75(max)	μS
Trigger Pulse Width	t _w	C _L =50pF A _i =LOW	7	20	25	30	ns
Trigger Pulse Width	t _w	C _L =50pF B _i =High	7	20	25	30	ns
Clear Pulse Width	t _w	C _L =50pF CLR _i =LOW	8	20	25	30	ns
External Timing Resistance	Rext			2 100	2(min) 100 (max)	2(min) 100 (max)	kΩ
External Timing Capacitance	Cext				no restriction	1	
Input Capacitance	Cin		5				pF
Power Dissipation Capacitance	C _{PD}						pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}{}^z \ f_{in}$.

Application Information

The basic output pulse width is determined by the value of external capacitance and timing resistance. For output pulse widths greater than $100\mu s$ or external capacitance greater than 10nF the following equation should be used.

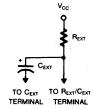
$$t_w = k \cdot R_{ext} \cdot C_{ext}$$

Where

 t_W is in μ s K is the multiplying factor and is approximately 0.45 for Cext is in nF Rest is in k Ω

For best results, system ground should be applied to the C_{ext} terminal. These devices do not require a switching diode in series with the $R_{\text{ext}}/C_{\text{ext}}$ terminal (as required by some other monostable multivibrators)

TIMING COMPONENT



[†] For AC switching test circuits and timing waveforms see section 2.

- . Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- . 3-State outputs with high drive current ($I_{OL} = 24 \text{ mA}$ @ $V_{OL} = 0.5 \text{V}$) for direct bus interface
- . Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges:

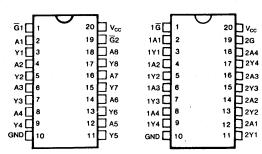
KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

· Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

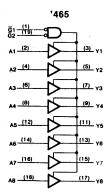
PIN CONFIGURATIONS

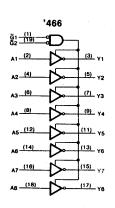
'465 and '466

'467 and '468



LOGIC DIAGRAMS





DESCRIPTION

These high-speed octal buffers and drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and busoriented receivers and transmitters. The designer has the choice of inverting/ noninverting outputs and various types of output controls.

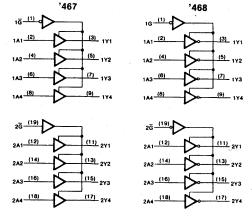
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

	Input	Out	put	
G,	G ₂	Α	'465	'466
L	L	L	L	Н
L	L	Н	Н	L
Н	X	Х	Z	Z
X	Н	Х	Z	Z

	Input	Ou	tput	
G	G	A	'467	'468
Н	L	L	L	Н
Н	L	Н	Н	L
L	H .	Χ	Z	z



Octal Buffers and Line Drivers with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, IIK
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current-Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

		•
Supply Voltage,	Vcc	4.5V to 5.5V
		V _{OUT} OV to V _{CC}
Operating Temp	erature	
Range	KS74HCTLS:	-40°C to +85°C
		-55°C to +125°C
Input Rise & Fal	l Times, t _r , t _f	Max 500 ns
Unused inputs	must always be tied to	o an appropriate logic
	either Vcc or GND)	

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit	
			Тур		Guaranteed Lim	its] .	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	v	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} −0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA	-	8.0	80.0	160.0	μĄ	
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	



KS54HCTLS 465/466 KS74HCTLS 467/468

Octal Buffers and Line Drivers with 3-State Outputs

AC ELECTRICAL CHARACTERISTICS (Input tr., tr<6 ns), HCTLS465, HCTLS466, HCTLS467, HCTLS468

Characteristic	cteristic Symbol Conditions		8		ACHT 25°C = 5V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5V ± 10%	54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
	<u></u>			Тур		Guar	anteed Limits	
Maximum Propagation Delay,	t _{PLH}	C _L =50pl C _L =150		11 14	15 18		22 28	
A to Y	1 Tour	C _L =50pF C _I =150pF		11 14	15 18	19 24	22 28	ns
t _{PZH}		$R_i = 1 k\Omega$	C _L =50pF C _L =150pF	2 4 27	32 35	40 45	48 54	ns
Enable to Y	t _{PZL}		C _L =50pF C _L =150pF	24 27	32 35	40 45	48 54	113
Maximum Output disable Time,	t _{PHZ}	$R_L = 1 k\Omega$		24	32	40	48	
Enable to Y		C _L =50pl	=	24	32	40	48	ns
Maximum Input Capacitance	C _{IN}			4				рF
Maximum Output Capacitance	Cout	Output D	isabled	10				рF
Power Dissipation Capacitance* (per stage)	C _{PD}	Output D Output E		5 30	-			рF

C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}



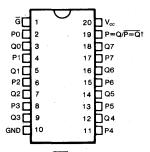
[†] For AC switching test circuits and timing waveforms see section 2.

- Compares two 8-bit words
- '518, '520 and '522 have 20KΩ Pull-up resistors on Q inputs

TYPE	INPUT PULL-UP RESISTOR	OUTPUT FUNCTION AND CONFIGURATION
'518	Yes	P=Q open-drain
'519	No	P=Q open-drain
'520	Yes	P=Q totem-pole
'521	No	P=Q totem-pole
'522	Yes	P=Q open-drain

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- . 3-State outputs with high drive current
- (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C
 - KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



 \uparrow P=Q for '518 and '519; $\overrightarrow{P}=\overrightarrow{Q}$ for '520, '521, '522.

DESCRIPTION

These identity comparators perform comparisons on two eight-bit binary or BCD words. The '518 and '519 provide P=Q outputs, while the '520, '521, and '522 provide $\overline{P=Q}$ outputs. The '518, '519, and '522 have open-drain outputs. The '518, '520, and '522 feature 20-kQ inputs for analog or switch data.

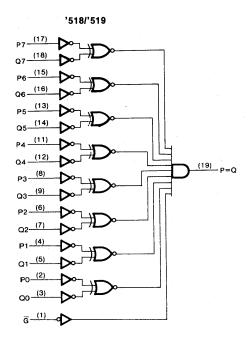
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

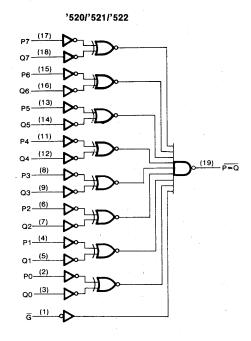
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and around.

FUNCTION TABLE

INPUTS		OUTPUTS	
DATA P, Q	ENABLE G	P=Q	P=Q
P=Q	L	Н	L
P>Q	L	L	Н
P <q< td=""><td>L.</td><td>L</td><td>Н</td></q<>	L.	L	Н
Х	Н	L	Н

LOGIC DIAGRAMS





Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pa† 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions



Parameter	Parameter Symbol		т	_ = 25°C	KS74HCTLS T _A = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
f 4	-	Y .	Тур		Guaranteed Limits		1
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage (Totem-pole Outputs)	V _{OH}	V _{IN} =V _{IH} or V _{IL} I _O =-20μA I _O =-6mA	V _{CC} 4.2	V _{CC} -0.1	V _{CC} 0.1 3.84	V _{CC} -0.1 3.7	v
Maximum Low-Level Output Voltage (All Outputs)	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	С	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current, ('518, '520 and '522 Q input)		V _{CC} =Max V _{IN} =2.7V V _{IN} =0.4V		-0.2 -0.6	-0.2 -0.6	-0.2 -0.6	mA
Maximum Input Current (All other Inputs)	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current (Open-Drain Outputs)	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent	lcc	For '518, '520 and '522: V _{IN} =GND (Q0-Q7) V _{IN} =V _{CC} or GND (all other inputs)		3.5	3.5	3.5	mA
Supply Current		For '519 and '521: V _{IN} =V _{CC} or GND I _{OUT} =0µA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS518, HCTLS519

Characteristic	Symbol	Conditions	54/74/ T _a = 2 V _{CC} =	25°C	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5V ± 10%	54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
			Typ Guaranteed		anteed Limits		
Maximum Propagation Delay,	tpLH	C _L =50pF C _L =150pF	26 29	33 36	40 45	47 53	
from P or Q to P=Q	t _{PHL}	C _L =50pF C _L =150pF	21 24	28 31	35 40	42 48	ns
Maximum Propagation Delay,	t _{PLH}	C=50pF C _L =150pF	23 26	29 32	35 40	41 47	
from \bar{G} to P=Q	t _{PHL}	C _L =50pF C _L =150pF	18 21	24 27	30 35	36 42	ns
Maximum Input Capacitance	CiN		5				рF
Maximum Output Capacitance	Cout						рF
Power Dissipation Capacitance*	C _{PD}				-		рF

AC ELECTRICAL CHARACTERÍSTICS (Input tr., tre6 ns), HCTLS520, HCTLS521

Characteristic	Symbol	Conditions	T. =	ACHT 25°C = 5V	KS74HCTLS T _a = -40°C to +85°C V _{CC} =5V±10%	54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
			Тур	-	Guar	anteed Limits	
Maximum Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	12 15	22 25	28 33	33 39	
from P or Q to P=Q	tpHL	C _L =50pF C _L =150pF	16 19	22 25	28 33	33 39	ns
Maximum Propagation Delay, from \overline{G} to $\overline{P}=\overline{Q}$	t _{PLH}	C=50pF C _L =150pF	15 18	20 23	25 30	30 36	
	t _{PHL}	C _L =50pF C _L =150pF	15 18	20 23	25 30	30 36	ns
Maximum Input Capacitance	CIN		5				pF
Maximum Output Capacitance	Соит						рF
Power Dissipation Capacitance*	C _{PD}						pF

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f<6 ns), HCTLS522

Characteristic	Symbol	Conditions	54/74ACHT T _a = 25°C V _{CC} = 5V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5V ± 10%	54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
		Typ Guaranteed Li				anteed Limits	
Maximum Propagation Delay,	tpLH	C _L =50pF C _L =150pF	24 27	31 34	37 42	43 49	
from P or Q to P=Q	t _{PHL}	C _L =50pF C _L =150pF	19 22	26 29	32 37	38 44	ns
Maximum Propagation Delay,	t _{PLH}	C=50pF C _L =150pF	23 27	29 32	35 40	41 47	
from \overline{G} to $\overline{P}=\overline{Q}$	t _{PHL}	C _L =50pF C _L =150pF	18 21	24 27	30 35	36 42	ns
Maximum Input Capacitance	CIN		5				рF
Power Dissipation Capacitance*	C _{PD}						рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.



Octal D-Type Transparent Latches with 3-State Outputs

FEATURES

- · 8 latches in a single package
- Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (loL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: __40°C to __485°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION

ᅈᄆ	1	20	□ v _{cc}
1₫ 🗆	2	19	8₫
10 🗆	3	18	BD 8D
2D 🗌	4	17	70
20 □	5	16	্র ব
3₫ 🗆	6	15	⊟ 6ত
3D 🗀	7	14	□ 6D
4D 🗌	8	13	5D
4₫ 🗆	9	12	5Q
GND 🗌	10	11	DΕ
			l

DESCRIPTION

The '533 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (E) is high, the $\overline{\mathbf{Q}}$ outputs follow the complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (\overline{OC}) which places the outputs at high-impedance state when it is taken high. The \overline{OC} signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

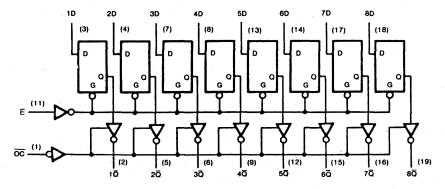
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(Each Latch)

	Inputs		Output
<u>oc</u>	E	D	Q
L	Н	Н	L
L	Н	L	Н
. L	L	X	$\bar{\mathbf{Q}}_{0}$
Н	Χ ,	Х	Z

LOGIC DIAGRAM





Absolute Maximum Ratings*

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

• •
Supply Voltage, V _{CC} 4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT OV to VCC
Operating Temperature
Range KS74HCTLS: ~40°C to +85°C
KS54HCTLS: -55°C to +125°C
Input Rise & Fall Times, tr, tf Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	nbol Test Conditions		a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS Ta = -55°C to +125°C	Unit	
			Тур	Guaranteed Limits				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_0=-20\mu A$ $I_0=-6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v,	
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	



Octal D-Type Transparent Latches with 3-State Outputs

AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS533

Characteristic	Symbol	Conditions†		Conditions†		Symbol Conditions†		-	25°C : 5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
				Тур		Guaranteed	Limits	1				
Maximum Propagation	tpLH	C _L =50pF C _L =150pF		14 17	18 21	23 28	27 33					
Delay, D to Q	tpHL	C _L =50pl		14 17	18 21	23 28	27 33	ns				
Maximum Propagation	t _{PLH}	C=50pF C _L =150		22 25	30 33	37 43	45 41					
Delay E to Q	t _{PHL}	C _L =50pF C _i =150pF		22 25	30 33	37 43	48 54	ns				
Maximum Output Enable Time, OC to any Q	t _{PZH}	$R_i = 1k\Omega$	C _L =50pF C _L =150pF	24 27	32 35	40 45	48 54	ns				
	tpzL	U[= IKW	C _L =50pF C _L =150pF	24 27	32 35	40 45	48 54					
Maximum Output Disable	tpHZ	R _L =1kΩ		19	25	31	37					
Time, \overline{OC} to any \overline{Q}	t _{PL} z	C _L =50pl	F	19	25	31	37	ns				
Minimum Pulse Width, E High	tw			6	10	12	15	ns				
Minimum Setup Time, D before E↓	t _{su}			2	3	4	5	ns				
Minimum Hold Time, D after E↓	tn			6	10	12	15	ns				
Maximum Input Capacitance	C _{IN}			5				pF				
Maximum Output Capacitance	C _{OUT}	Output D	isabled	10				pF				
Power Dissipation Capacitance* (per stage)	C _{PD}	ÖC=V _{CC} ÖC=GNI		5 30				рF				

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

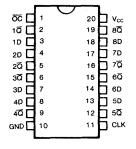
FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (loL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '534 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

The flip-flops are edge-triggered on the positive transition of the clock: the \overline{Q} outputs are set to the complement of the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal (\overline{OC}) which places the outputs in high-impedance state when it is taken high. The OC signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

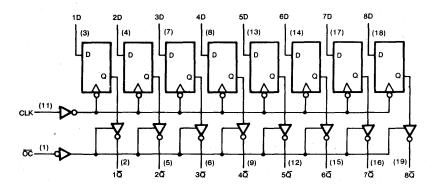
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(Each Latch)

1	nputs	Output	
ŌĊ	CLK	D	ā
L	†	Н	L
L	†	L	Н
L	L	Х	\bar{Q}_{0}
Н	X	Х	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, IIK
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, $T_{stg} \dots -65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	.ou oboraniig oonianiiono
Supply Voltage, V	cc 4.5V to 5.5V
DC Input & Output	t Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Temper	ature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall 1	imes, t _r , t _f Max 500 ns
•	ust always be tied to an appropriate logic ther V _{CC} or GND)

Characteristic S	Symbol	Test Conditions	itions T _a =		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS534

Characteristic	Symbol	ibol Conditions†		T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V± 10%	Unit
				Тур	Guaranteed Limits			
Maximum Operating Frequency	f _{max}	C _L =50pF		50	35	30	25	MHz
Maximum Propagation	t _{PLH} C _L =50 C _L =15			21 24	28 31	35 40	42 48	
Delay, CLK to any Q	t _{PHL}	C _L =50pl C _L =150		21 24	28 31	35 40	42 48	ns
Maximum Output Enable Time, OC to any Q	t _{PZH}	R _L =1kΩ	C _L =50pF C _L =150pF	21 24	28 31	35 40	42 48	ns
			C _L =50pF C _L =150pF	21 24	28 31	35 40	42 48	
Maximum Output Disable Time, OC to any Q		$R_L = 1k\Omega$ $C_L = 50pl$	F	19 19	25 25	31 31	37 37	ns
Minimum Pule Width, CLK High or Low	t _{PLZ}	OL GOD!		9	13	15	18	ns
Minimum Setup Time, D before CLK†	t _{su}			10	13	17	20	ns
Minimum Hold Time, D after CLK†	t _h			-3	0	0	0	ns
Maximum Input Capacitance	CIN			5				рF
Maximum Output Capacitance	Cout	Output D	Output Disabled					рF
Power Dissipation Capacitance* (per stage)	C _{PD}	OC=V _{CC} OC=GNI		5 30				рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

KS54HCTLS **540/541** KS74HCTLS

Octal Buffers and Line Drivers with 3-State Outputs

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74L\$ logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
 Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

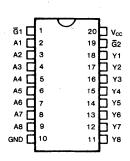
The '540 and '541 are general purpose high-speed octal line drivers/buffers with 3-state outputs. The inputs and outputs are located on opposite sides of the 20-pin package, thus improving circuit board density. The '540 provides inverted data and the '541 provides true data at the outputs.

The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high impedance state.

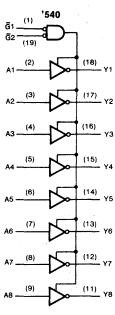
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground

PIN CONFIGURATION



LOGIC DIAGRAMS



G1_(1)	'541 —d	
G2 (19)		
A1 (2)	V	(18) Y1
A2 (3)	-	(17) Y2
A3(4)	V	(16) Y3
A4(5)	- 5	(15) Y4
A5(6)	-	(14) Y5
A6-(7)	<u>-</u> -	(13) Y6
A7(8)	- 	(12) Y7
A8(9)	<u>-</u>	(11)

FUNCTION TABLE

Input			Output			
Ğ,	G ₂	A	'540	'541		
L	L	L	Н	L		
L	L	• н	L	н		
Н	x	X	Z	Z		
Х	H	Х	Z	Z		

KS54HCTLS **540/541** KS74HCTLS

Octal Buffers and Line Drivers with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to $+150$ °C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
, ,
posure to these conditions may affect device reliability.

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic
voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	· V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ



Octal Buffers and Line Drivers with 3-State Outputs

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS540, HCTLS541

Characteristic	Symbol	Condition	Conditions†		25°C :5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit	
				Тур	Typ Guaranteed Limits				
Maximum Propagation Delay, A to Y	t _{PLH}	C _L = 50 C _L =150	•	11 14	15 18	19 24	23 29		
	t _{PHL}		C _L = 50pF C _L =150pF		15 18	19 24	23 29	ns	
Maximum Output Enable Time, G to Y	tpzH	R _L =1kΩ	C _L = 50pF C _L =150pF	l	25 28	25 30	37 43	ns	
	tpzL		C _L =50pF C _L =50pF	18 21	25 28	31 36	37 43		
Maximum Output Disable	t _{PHZ}	R _L =1kΩ		13	18	23	27		
Time, G to Y	tpLZ	C _L =50pF		13	18	23	27	ns	
Maximum Input Capacitance	CIN							рF	
Maximum Output Capacitance	Соит	Output [Output Disabled					рF	
Power Dissipation Capacitance* (per stage)	C _{PD}	G=V _{CC} G=GND		5 30				pF	

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

[†] For AC switching test circuits and timing waveforms see section 2.

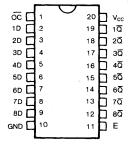
FEATURES

- . 8 latches in a single package
- Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- . Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 (CTANIOT: 4000 to 1000)

KS74AHCT: -40°C to + 85°C KS54AHCT: -55°C to + 125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '563 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer register, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent; when the enable (E) is high, the Q outputs follow complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (OC) which places the outputs at a high-impedance stage when it is taken high. The OC signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and cutput voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

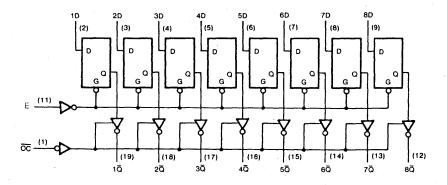
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(Each Latch)

	Inputs		Output
ōc	·E	D	ā
L	Н	Н	L
L	н	L	Н
L	Ļ	Χ	$\bar{\mathbf{Q}}_{0}$
н	X	Χ	Z

LOGIC DIAGRAM



KS54HCTLS 563

Octal D-Type Transparent Latches with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range $V_{CC}, \ldots -0.5V$ to $\pm 7V$
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, $T_{stg} \dots -65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	с	
DC Input & Output	Voltages*, VIN, VO	UT OV to VCC
Operating Tempera		
Range	KS74HCTLS: -	40°C to +85°C
	KS54HCTLS: -5	5°C to +125°C
Input Rise & Fall Ti	mes, t _r , t _f	Max 500 ns
Unused inputs mu voltage level (eith	st always be tied to al ner V _{CC} or GND)	n appropriate logic

Characteristic S	Symbol	Test Conditions	Τ,	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	١. ١
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr, tree ns), HCTLS563

Characteristic	Symbol	Conditions†			25°C = 5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit	
				Тур	_	Guaranteed	1 Limits		
Maximum Propagation	t _{PLH}	C _L = 50pF C _L =150pF		14 17	18 21		27 33		
Delay, D to Q	t _{PHL}	C _L = 50 C _L =150		14 17	18 21		27 33	ns	
Maximum Propagation	t _{PLH}	C= 50p C _L =150		22 25	30 33		45 51		
Delay E to Q	t _{PHL}	C _L = 50 C _L =150		22 25	30 33		45 51	ns	
Maximum Output Enable Time, OC to any Q	tpzH	Rı=1kΩ	C _L = 50pF C _L =150pF		32 35		48 54		
	tpzL	UL- 1KM	C _L = 50pF C _L =150pF		32 35		48 54	ns	
Maximum Output Disable Time, OC to any Q	t _{PHZ}	R _L =1kΩ C _L =50pl	F	19 19	25 25		37 37	ns	
Minimum Pulse Width, E High	t _w			9	13	15	18	ns	
Minimum Setup Time, D before E↓	t _{su}	-		6	8	10	10	ns	
Minimum Hold Time, D after E↓	t _h			6	10	12	15	ns	
Maximum Input Capacitance	CiN			5			-	рF	
Maximum Output Capacitance	Соит	Output D	isabled	10				рF	
Power Dissipation Capacitance* (per stage)	C _{PD}	OC=V _{CC} OC=GNI		5 30				рF	

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \; V_{CC}{}^2 \; f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION

			_	1
ōō	1	\cup	20	□ v _{cc}
1D 🗀	2		19	10
2D 🗆	3		18	2Q
3D 🗆	4		17	ЗQ
4D 🗀	5		16	⊿ 4 🖸
5D 🗀	6		15	 5α
6D, 🗀	7		14	🗖 ପ୍ରେ
7D 🗆	8		13	70
BD ☐	9		12	🛚 ୫ଦି
GND 🗌	10		11	CLK
, l	Ļ			

DESCRIPTION

The '564 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

The flip-flops are edge-triggered: on the positive transition of the clock, the \overline{Q} outputs are set to the complement of the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal (\overline{OC}) which places the outputs at high impedance state when It is taken high. The \overline{OC} signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

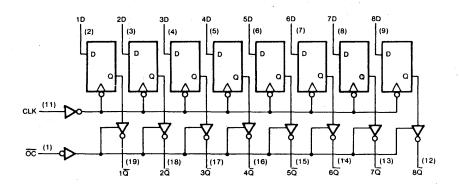
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(Each Flip-Flop)

ı	nputs		Output
ОC	CLK	D	Ğ.
L	t	Н	L '
L	↑	L.	н
L	L	Χ	Q ₀
Н	Χ	Χ	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Recomme	naea Operating Conditions
Supply Voltage	V _{CC} 4.5V to 5.5V
DC Input & Out	put Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Temp	perature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fa	Il Times, t _r , t _f Max 500 ns
Unused inputs	must always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	est Conditions		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	1
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	Ņ
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1	V _{CC} -0.1	٧
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tr 46 ns), HCTLS564

Characteristic	Symbol	bol Conditions†		T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit	
				Тур	p Guaranteed Limits				
Maximum Operating Frequency	f _{max}	C _L = 50	C _L = 50pF		35	30	25	MHz	
Maximum Propagation Delay,	t _{PLH}	1		21 24	28 31	35 40	42 48		
CLK to any Q	t _{PHL}	C _L = 50 C _L =150	•	21 24	28 31	35 40	42 48	ns	
Maximum Output Enable Time, OC to any Q	t _{PZH}	$R_L = 1 k\Omega$	C _L = 50pF C _L =150pF	l	28 31		42 48		
		IN	C _L = 50pF C _L =150pF		28 31	35 40	42 48	ns	
Maximum Output Disable	t _{PHZ}	R _L =1kΩ		19	25	31	37	ns	
Time, OC to any Q	tPLZ	C _L =50p	F	19	25	31	37		
Minimum Pulse Width, CLK High or Low	t _w			9	12	15	18	ns	
Minimum Setup Time, D before CLK1	t _{su}			10	13	17	20	ns	
Minimum Hold Time, D after CLK1	th			-3	0	. 0	O	ns	
Maximum Input Capacitance	CiN			5				pF	
Maximum Output Capacitance	Соит	Output D	Output Disabled					pF	
Power Dissipation Capacitance* (per stage)	C _{PD}	OC=Vcc		5 30	,	·		pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}

[†] For AC switching test circuits and timing waveforms see section 2.

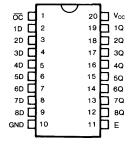
FEATURES

- . 8 latches in a single package
- Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- . Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ($I_{OL} = 24$ mA @ $V_{OL} = 0.5V$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to + 85°C KS54HACT: -40°C to + 125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '573 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (E) is high, the Q outputs follow the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (\overline{OC}) which places the outputs at a high-impedance state when it is taken high. The \overline{OC} signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

There devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

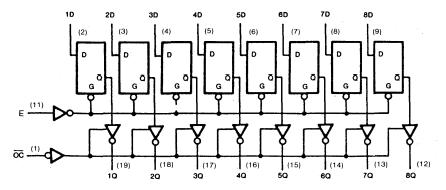
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(Each Latch)

	Inputs		Output
OC	3	D	Q
L	Н	Н	Н
L	н	L	, L
L	L	Χ	Q_0
. н	Х	Х	Z

LOGIC DIAGRAM





Absolute Maximum Ratings*

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	V _{CC} 4.5V to 5.5V but Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Tempe	
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall	Times, $t_{\text{r}},\;t_{\text{f}}$ Max 500 ns
	must always be tied to an appropriate logic either Voc or GND)

Characteristic	Symbol	Test Conditions	st Conditions		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙςς	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr 46 ns), HCTLS573

Characteristic	Symbol	Conditions†		Conditions [†]		T _a = : V _{CC} =		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
· · · · · · · · · · · · · · · · · · ·				Тур		Guarantee	1 Limits	<u> </u>		
Maximum Propagation	tpLH	C _L = 50 C _L =150		14 17	18 21	23 28	27 33			
Delay, D to Q	t _{PHL}	C _L = 50 C _L =150	•	14 17	18 21	23 28	27 33	ns		
Maximum Propagation	tpLH	C=50pF C _L =150		22 25	30 33	37 42	45 51			
Delay E to Q	t _{PHL}	C _L = 50pF C _L =150pF		22 25	30 33	37 42	45 51	ns		
Maximum Output Enable Time, OC to any Q	t _{PZH}	R _L =1kΩ	C _L = 50pF C _L =150pF	I .	32 35	40 45	48 54			
	t _{PZL}		C _L = 50pF C _L =150pF		32 35	40 45	48 54	ns		
Maximum Output Disable Time, OC to any Q	t _{PHZ}	$R_L = 1 k\Omega$ $C_L = 50 pl$	F	19 19	25 25	31 31	37 37	ns		
Minimum Pulse Width, E High	tw			9	12	15	18	ns		
Minimum Setup Time, D before E↓	t _{su}	,		6	8	10	12	ns		
Minimum Hold Time, D after E↓	t _h			6	10	12	15	ns		
Maximum Input Capacitance	CIN			5				рF		
Maximum Output Capacitance	Cout	Output D	isabled	10				рF		
Power Dissipation Capacitance*	C _{PD}	OC=V _{CC}	(per stage)	5 30				рF		

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.



[†] For AC switching test circuits and timing waveforms see section 2.

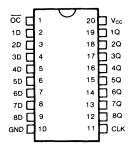
FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- ($I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5V$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C

KS54HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

The '574 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

The flip-flops are edge-triggered on the positive transition of the clock. The Q outputs are set to the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal (\overline{OC}) which places the outputs at a high-impedance state when it is taken high. The \overline{OC} signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

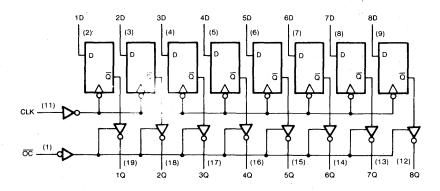
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(Each Flip-Flop)

1	nputs	Output	
ОC	CLK	D	Q
L	1	Н	н
L	†	L	L
L	L	X	Q_0
· H	X	Х	Z

LOGIC DIAGRAM



1



Absolute Maximum Ratings*

Absolute Maximum Ratings, rsig.
 Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
 These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	Vcc					
DC Input & Outp	out Voltages*, V _{IN} , V _{OU}	T OV to Vcc				
Operating Temporating	erature					
Range	KS74HCTLS: -4	0°C to +85°C				
	KS54HCTLS: -55	°C to +125°C				
Input Rise & Fall	l Times, t _r , t _f	Max 500 ns				
The state of the s						

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
		<u> </u>	Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}	,		2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0,26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	ΔΙσς	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS574

Characteristic	Symbol	Conditions†		T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit	
				Тур		Guarantee	l Limits		
Maximum Operating Frequency	f _{max}	C _L = 50	pF	45	35	30	25	MHz	
Maximum Propagation	t _{PLH}	C _L = 50 C _L =150		21 24	28 31	35 40	42 48		
Delay, CLK to any Q	t _{PHL}	C _L = 50 C _L =150		21 24	28 31	35 40	42 48	ns	
Maximum Output Enable	t _{PZH}	$R_i = 1 k\Omega$	C _L = 50pF C _L =150pF	1	28 31	35 40	42 48	ns	
Time, ÖC to any Q	t _{PZL}	nt- ikn	C _L = 50pF C _L =150pF		28 31	35 40	42 48		
Maximum Output Disable	t _{PHZ}	$R_L = 1 k\Omega$	19	25	31	37	ns		
Time, OC to any Q	tPLZ	C _L =50pF		19	25	31		37	
Minimum Pulse Width, CLK High or Low	t _w		,	9	12	15	18	ns	
Minimum Setup Time, D before CLKf	t _{su}			10	13	17	20	ns	
Minimum Hold Time, D after CLK†	t _h			-3	0	0 *	0	ns	
Maximum Input Capacitance	CIN		,	5				pF	
Maximum Output Capacitance	Cout	Output D	isabled	10				pF	
Power Dissipation Capacitance* (per stage)	C _{PD}	OC=V _{CC}		5 30				рF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

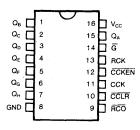
FEATURES

- . Choice of 3-State ('590) and Open-Drain ('591) Outputs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs
 - (I_{OL} = 24mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

These devices each consist of an 8-bit counter which feeds an 8-bit register. The counter is incremented on the rising edge of the CCK input, provided that clock enable, CCKEN, is low. When the counter increments to the all ones condition, ripple carry out, RCO, will go low. This enables either synchronous cascading of the counters by connecting the RCO of the first stage to the CCKEN of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the RCO of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The output register is loaded with the contents of the counter on the rising edge of the register clock, RCK. The outputs of this register feed the outputs which are enabled when the enable input, G, is taken low. This enables connection of this part to a system bus. The Q outputs of the '590 are 3-State and those for '591 are Open-drain.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

		INPUTS			FUNCTION		
G	RCK	CCLR.	CCKEN	ССК	FUNCTION		
н	Х	Х	Х	Х	Q Outputs disable		
L	Х	Х	Х	Х	Q Outputs enable		
L		X	×	Х	Counter data is stored into register		
L	T_	Х	х	Х	Register state is not changed		
L	X	L	X	Х	Counter clear		
L	X	Н	L	ſ	Advance one count		
L	Х	Н	L	ī	No count		
L	Х	н	н	Х	No count		

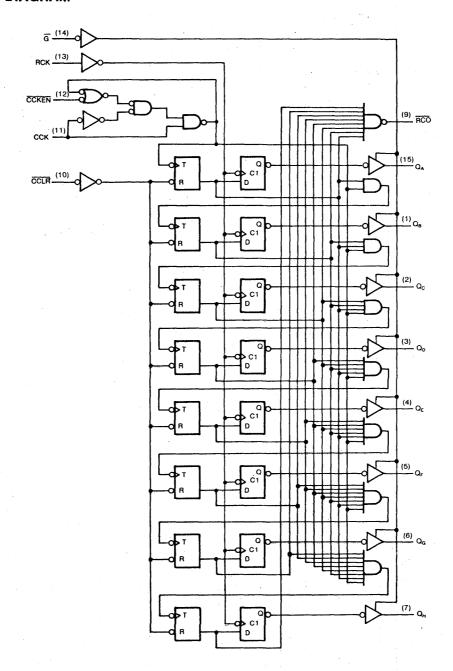
X: Don't care

 $RCO = Q_{A}' \bullet Q_{B}' Q_{C}' \bullet Q_{D}' Q_{E}' \bullet Q_{F}' Q_{G}' \bullet Q_{H}'$

(QA' ~ QH': Internal outputs of the counter)



LOGIC DIAGRAM



8-Bit Binary Counters with Output Registers

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74HCTLS: -40°C to $+85^{\circ}\text{C}$ KS54HCTLS: -55°C to $+125^{\circ}\text{C}$ Input Rise & Fall Times, t_r , t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур	i	Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _I L	·.		0.8	0.8	0.8	٧
Minimum High-Level Output Voltage (All '590 Outputs and '591 RCO Outputs)	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V _{CC} 4.2	V _{CC} =0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1	V
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0µA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

8-Bit Binary Counters with Output Registers

AC ELECTRICAL CHARACTERISTICS (Input tr, tie6 ns), HCTLS590

Characteristic		Symbol	Conditions†	$T_a = 25^{\circ}C$ onditions [†] $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Тур		Guaranteed	Limits	
Maximum Clock	Frequency	f _{max}		35	25	20	20	ns
Maximum Propa	agation Delay,	tplH		24	32	40	48	
CCK1 to RCO		t _{PHL}		24	32	40	48	ns
Maximum Propa CCLR↓ to RCO	agation Delay,	t _{PLH}	C _L =50pF	26	35	44	52	ns
Maximum Propa	agation Delay,	t _{PLH}	1	16	21	26	31	
RCK1 to Q		tpHL		16	21	26	31	ns
Maximum Outpo	ut Enable Time,	tpzh		18	24	30	36	
Ḡ↓ to Q		t _{PZL}	R _L =1kΩ	18	24	30	36	ns
Maximum Outpi	ut Disable Time,	t _{PHZ}	CL=50pF	18	24	30	36	
G↑ to Q		tpLZ		18	24	30	36	ns
Minimum Pulse Width	CCK or RCK High or Low	tw		12	16	20	24	ns
	CCLR Low			12	16	20	24	ĺĺ
	CCKEN↓ before CCK↑			12	16	20	24	
Minimum CCLR† before Setup Time CCK†	CCLRt before CCKt	t _{su}		12	16	20	24	ns
	CCK† to RCK†††			24	32	40	48	
Maximum Input	Capacitance	CIN		5				рF
Maximum Outpu	ut Capacitance	Cout	Output Disabled	10				рF
Power Dissipati	on Capacitance*	C _{PD}						рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

For AC switching test circuits and timing waveforms see section 2.

^{††} The RCK† to CCK† setup time ensures that the counter will see stable data from the register output.

AC ELECTRICAL CHARACTERISTICS (Input t, tie6 ns), HCTLS591

Characteristic		Symbol	Conditions†	$T_a = 25^{\circ}C$ onditions [†] $V_{CC} = 5.0V$		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Únit
				Тур		Guarantéed	Limits	
Maximum Clock	Frequency	f _{max}		35	25	20	20	ns
Maximum Propa	agation Delay,	t _{PLH}		24	32	40	48	
CCKf to RCO		tpHL	ľ	24	32	40	48	ns
Maximum Propa CCLR↓ to RCO	agation Delay,	tр∟н	$C_L=50pF$ $R_L=1k\Omega$	26	35	44	52	ns
Maximum Propa	agation Delay,	tpLH	IIL—IKW	27	37	46	55	
RCK1 to Q		tpHL		16	21	26	31	ns
Maximum Output Enable Time, G↓ to Q		tpzL		18	24	30	36	ns
Maximum Outp	ut Disable Time,	t _{PLZ}		18	24	30	36⁄	ns
Minimum Pulse Duration	CCK or RCK High or Low	tw		12	16	20	24	ns
	CCLR Low		8	12	16	20	24	
	CCKEN ↓ before CCK↑			12	16	20	24	
Minimum Setup Time	CCLRt before CCKt	t _{su}		12	16	20	24	ns
	CCK1 to RCK111			24	32	40	48	
Maximum Input	Capacitance	CIN		5				рF
Maximum Outpu	ut Capacitance	Соит	Output Disabled					рF
Power Dissipati	on Capacitance*	CPD						рF

 ^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}², f_{in-}
 * For AC switching test circuits and timing waveforms see section 2.



^{††} The clocks may be tied together, in which case the register state will be one clock pulse behind the counter.

8-Bit Binary Counters with Input Registers

FEATURES

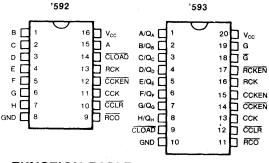
- Parallel Register Inputs ('592)
- Parallel 3-State I/O: Register Inputs/Counter Outputs ('593)
- Counter Has Direct Overriding Load and Clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- · 3-State outputs with high drive current
 - ($I_{OL} = 24 \text{ mA}$ @ $V_{OL} = 0.5V$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS



DESCRIPTION

The '592 and '593 both contain an 8-bit register which feeds an 8-bit binary counter. The counter is incremented on the rising edge of the CCK input, provided that clock enable, \overline{CCKEN} , is low. When the counter increments to the all ones condition, ripple carry out, \overline{RCO} , will go low. This enables either synchronous cascading of the counters by connecting the \overline{RCO} of the first stage to the \overline{CCKEN} of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the \overline{RCO} of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The input register is loaded on the rising edge of the register clock, RCK. The outputs of this register feed the counter. The counter is loaded with the register's contents when the clock load, CLOAD, input is taken low.

The '592 differs from the '593 in that the latter device has bidirectional input/output pins. The 3-state outputs of the counter can be enabled and are active when enable input, \overline{G} , is taken low and input G is taken high. The outputs of the counter then appear on the register inputs. This enables connection of this part to a system bus. The '593 also has a second clock enable pin, \overline{CCKEN} , which is active high and it also has an active low register clock enable. \overline{RCKEN} .

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

		INPUTS ('592)		FUNCTION
RCK	CLOAD	CCLR	CCKEN	ССК	FONCTION
Х	L	Н	Х	Х	Register data is loaded into counter
Х	н	L	X	х	Counter clear
\int	Н	H	×	х	The data of a thru H inputs is stored into register
-L	Н	Н	Х	Х	Register state is not changed
Х	Н	Н	L		Counter advances the count
Х	Н	н	L	7_	No count
X	Н	Н	Н	х	No count

X: Don't care

 $RCO = Q_A' \cdot Q_B' Q_C' \cdot Q_D' Q_E' \cdot Q_F' Q_G' \cdot Q_H'$

(QA' ~ QH': Internal outputs of the counter)

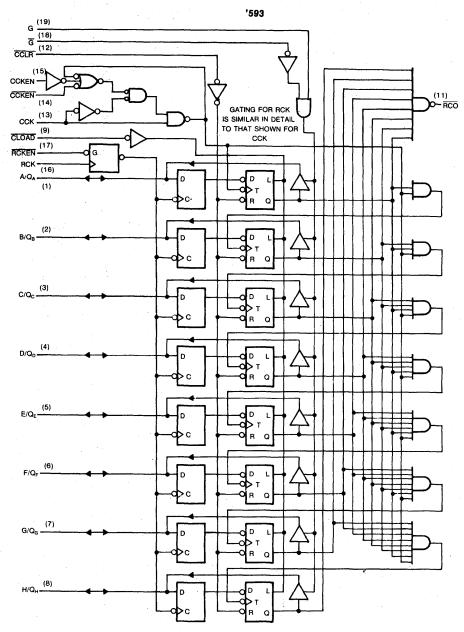


LOGIC DIAGRAMS

'592 CCLR (10) RCK (13) A (15) B (1) c-(2) D (3) E (4) F (5) G _____(6) H_____(7)



LOGIC DIAGRAMS (Continued)



Absolute Maximum Ratings*

posure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage,	Supply Voltage, V _{CC} 4.5V to 5.5V						
DC Input & Outp	out Voltages*, VIN, VOUT OV to VCC						
Operating Temperature							
Range	KS74HCTLS: -40°C to +85°C						
	KS54HCTLS: -55°C to +125°C						
Input Rise & Fall Times, $t_r, \ t_f \ \ldots \ Max \ 500 \ ns$							
Unused inputs must always be tied to an appropriate logic voltage level (either V _{CC} or GND)							

Characteristic	Symbol	Test Conditions	Ta = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} = 0.1	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	\ \ \
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μА
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input tr, tr 42 ns), HCTLS592

Characteristic		Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit		
				Тур		Guaranteed	Limits	-		
Maximum Clock	Frequency	f _{max}		35	25	20	20	MHz		
Maximum Propa	agation Delay,	tpLH		24	32	40	48	ns		
CCKt to RCO		tpHL		24	32	40	48			
Maximum Propa	agation Delay,	tpLH	C _L =50pF	24	32	40	48	ns		
CLOAD↓ to RC	Ō	tpHL		24	32	40	48			
Maximum Propa CCLR↓ to RCO	agation Delay,	t _{PHL}		24	32	40	48	ns		
Maximum Propa	agation Delay,	tpLH	C _L =50pF CLOAD=GND	26	35	44	52	ns		
RCK1 to RCO		t _{PHL}		26	35	44	52			
Minimum Pulse CCK or RC High or Lov				12	16	20	24			
vviatn	Width CCLR Low		·	12	16	20	24	ns		
	CLOAD Low			12	16	20	24	1		
	CCKEN↓ before CCK†			12	16	20	24			
Minimum Setup Time	CCLRt before CCKt	t _{su}		12	16	20	24	ns		
	RCK† before CLOAD††			24	32	40	48			
	Data A-H1 before			12	16	20	24			
Minimum Hold	Time	th	:	0	0	0	0	ns		
Maximum Input	Capacitance	CiN		5		-		pF		
Power Dissipati	on Capacitance*	C _{PD}						рF		

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

The RCKt to CLOAD setup time ensures that the counter will see stable data from the register output.

AC ELECTRICAL CHARACTERISTICS (Input tr., tr 6 ns), HCTLS593

Characteristic		Symbol	bol Conditions†		T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	
					Тур		Guaranteed	Limits	1
Maximum Clock Frequency		f _{max}			35	25	20	20 .	МН
Maximum Pr	ropagation Delay,	t _{PLH}	C _L =150pF		24 27	32 35	40 45	48 54	ns
CCK1 to Q	, opaganon a oraș	t _{PHL}			24	32 35	40 45	48 54	
	ropagation Delay,	t _{PLH}	C _L =50p		24	32	40	48	ns
CCKf to RC	:O	t _{PHL}			24	32	40	48	113
Maximum Pr	ropagation Delay,	tpLH	C _L =50p C _L =150		24 27	32 35	40 45	48 54	
CLOAD↓ to	Q	t _{PHL}	C _L =50p C _L =150		24 27	32 35	40 45	48 54	ns
Maximum Pr	opagation Delay.	tpLH			24	32	40	48	t-
CLOAD↓ to		t _{PHL}	C _L =50p	۲	24	32	40	48	ns
Maximum Pr	opagation Delay,	tpLH	C _L =50p	F	26	35	44	52	
RCK1 to RC		tpHL	CLOAD=		26	35	44	52	ns
	opagation Delay,	t _{PHL}	C _L =50pF		24	32	40	48	ns
CCLR↓ to Q Maximum Propagation Delay,		t _{PLH}	$C_L = 150 pF$ $C_L = 50 pF$		27	35 32	45 40	54 48	ns
CCLR↓ to RCO Maximum Enable Time, Gf or G↓ to Q		tpzL	$R_L = 1 k\Omega$	C _L =50pF C _L =150pF	21 24	28 31	39 44	42 48	ns
		t _{PZL}	n[- 1 <i>ku</i>	C _L =50pF C _L =150pF	21 24	28 31	35 44	42 48	ns
Maximum Disable Time G↓ or G↑ to Q		t _{PLH}	$R_L = 1 k\Omega$ $C_L = 50 pl$		24 21	28 28	35 35	42 42	ns
Minimum	CCK or RCK		OL GOD!	<u> </u>	12	16	20	24	ns
Pulse Width		twi			12	16	20	24	
	CLOAD Low				12	16	20	24	1
	CCKEN↓ before				12	16	20	24	
Minimum	RCKEN↓ to RCK1					12	16	24	
Setup Time	CCLRI before CCK† RCK† before CLOAD††	t _{su}			12	16	20	24	ns
					24	32	40	48	
	Data A-H before RCK1			-	12	16	20	24	
Hold Time		th			0	0	0	0	ns
Maximum Inp	out Capacitance	CiN			5				рF
Maximum Ou	tput Capacitance	Соит	Output D	isabled	10	10			рF
Power Dissipa	tion Capacitance*	C _{PD}							рF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin-

^{††} The RCK1 to CLOAD setup time ensures that the counter will see stable data from the register output.



[†] For AC switching test circuits and timing waveforms see section 2.

8-Bit Shift Registers with Output Latches

FEATURES

- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Choice of 3-State ('595) or Open-Drain ('596) Parallel Outputs
- Shift Register Has Direct Clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
 (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

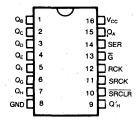
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('595) or opendrain ('596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



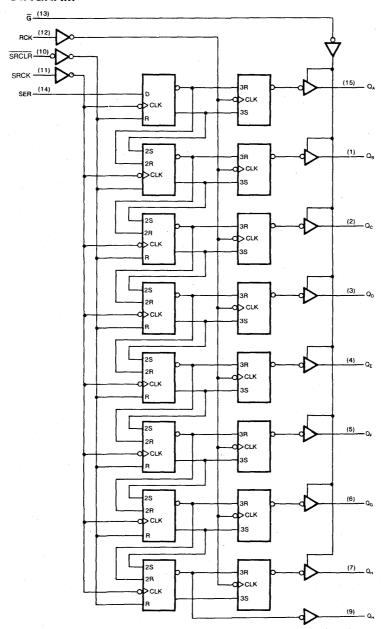
FUNCTION TABLE

		INPUTS			FUNCTION		
SER	SRCK	SRCLR	RCK	G	FUNCTION		
Х	Х	Х	X	Н	Q _A thru Q _H outputs disable		
Х	X	i x	X	L	Q _A thru Q _H outputs enable		
X	X	L	X	Х	Shift register is cleared.		
L		Н	X	x	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.		
Н		н	×	x	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.		
X	7_	Н	X	X.	State of S.R. is not changed.		
Х	X	X		Х	S.R. data is stored into storage register.		
Х	X	Х	L	X	Storage register state is not changed.		

X: DON'T CARE



LOGIC DIAGRAM



KS54HCTLS 595/596 KS74HCTLS 595/596



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, $P_d{}^{\dagger}$ 500 mW

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V	/cc	4.5V to 5.5V
DC Input & Outpu	ıt Voltages*, V _{IN} ,	Vout OV to Vcc
Operating Temper	rature	
Range	KS74HCTLS:	-40°C to +85°C
	KSEAHCTI S	-55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns
Unused inputs must always be tied to an appropriate logic
voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage (All '595 Outputs and '596 Q' _H Output)	V _{OH} .	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} ~0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tr<6 ns), HCTLS595, HCTLS596

Characteristic		$T_a = 25^{\circ}C$ $V_{ab} = 50V$ $T_a = -40^{\circ}C \text{ to}$		ymbol Conditions†		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit	
					Тур		Guaranteed	Limits	
Maximum Pi		tpLH	C ₁ = 50pf	=	15	18	25	30	ns
Delay, S RC I	Kf to Q'H	tpHL	O[-30pi		15	18	25	30	113
Maximum Pi		tpLH	C _L =50pi C _L =150		17 20	22 25	28 33	33 39	
Delay, RCK	t to QA thru QH	t _{PHL}	C _L =50pl		17 20	22 25	28 33	33 39	ns
	utput Enable	tpzH		C _L =50pF C _L =150pF	18 21	24 27	30 35	36 42	
Time, G↓ to ('595 only)	Q _A thru Q _H	tpzL	$R_L = 1 k\Omega$	C _L =50pF C _L =150pF	18	24 27	30 35	36 42	ns
Maximum Output Disable Time, Gt to Q _A thru Q _H ('595 only)		t _{PHZ}	$R_L=1k\Omega$		18 21	24 27	30 35	36 42	
		t _{PLZ}	C _L =50pl	F	18 21	24 27	30 35	36 42	ns
Maximum Pi Delay, Gt to	ropagation O Q _A thru Q _H	t _{PLH}	C _L =50pF		18	24	30	36	ns
('596 only)			C _L =150pF		21	27	35	42	
Maximum Pi			C _L =50pl	F	18	24	30	36	
Delay, G↓ to ('596 only)	Q _A thru Q _H	t _{PHL}	C _L =150	pF	21	27	35	42	ns
M inimum Pulse Width	SRCK or RCK	t _w			12	16	20	24	ns
- uise wiutii	SRCLR Low				12	16	20	24	113
Minimum	SRCLRt to SRCKt				12	16	20	24	
Setup Time	SER to SRCKt	t _{su}			12	16	20	24	ns
	SRCK† to RCK††				24	32	40	48	
Minimum Hold Time		t _h			-3	0	0	0	ns
Maximum In	put Capacitance	CiN			5				pF
Maximum O Capacitai	•	Cout	Output D	isabled	10				pF
Power Diss Capacitai		C _{PD}							рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

^{††} This setup time ensures the register will see stable data from the register output.

- 8-Bit Parallel Storage Register Inputs
- shift Register has Direct Overiding Load and Clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

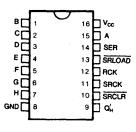
DESCRIPTION

The '597 consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

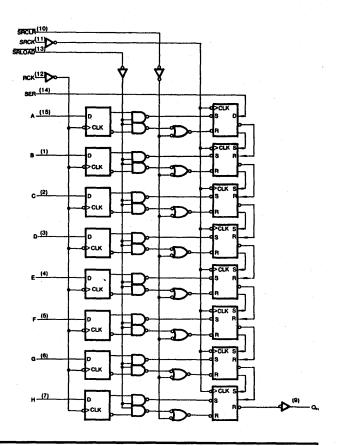
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

		INPUTS			FUNCTION
SER	SRCK	SRCLR	SRLOAD	RCK	FONCTION
Х	Х	L	Н	X	S.R. is cleared to "L"
х	X	Н	J	Х	Input register data is stored into S.R.
L	5	Н	Н	х	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
Н	5	Н	Н	х	First stage of S.R. becomes "H". Other stages stores the data of previous stage, respectively.
Х	· X	Х	Х		State of S.R. is not changed.
Х	Х	Х	Х	5	Input data on A∼H line is stored into input register
Х	Х	Х	Х	T-L	Storage register state is not changed.

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Por Packago P. t 500 W

Power Dissipation Per Package, Pd[†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage, V	′cc	4.5V to 5.5V
DC Input & Output	it Voltages*, V _{IN} ,	Vour OV to Vcc
Operating Temper	ature	
Range	KS74HCTLS:	-40°C to +85°C
	KS54HCTLS:	-55°C to +125°C
Input Rise & Fall	Fimes, t_r , t_f	Max 500 ns
•	ust always be tied ther V _{CC} or GND)	to an appropriate logic

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	ol Test Conditions		_a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V _{CC}	V _{CC} -0.1	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙ _{CC}	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS597

Characteristic		Symbol	Conditions†	1 -	25°C = 5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
1				Тур		Guaranteed	Limits	
Maximum Clo	ock Frequency	f _{max}		35	25	20	20	MHz
Maximum Pro	pagation Delay,	t _{PLH}		15	18	25	30	
SRCK1 to Q'	н .	tPHL		15	18	25	30	ns
Maximum Pro	pagation Delay,	tpLH	$C_L = 50pF$	18	24	30	36	
SRLOAD↓ to	Q'H	tPHL		18	24	30	36	ns
Maximum Propagation Delay, SRCLR♭ to Q'H		t _{PHL}		17	22	28	33	ns
Maximum Pro	pagation Delay,	tpLH	C _L =50pF	21	29	35	42	
RCK† to Q'H		tPHL	SLOAD=Low	21	29	35	42	ns
Minimum	RCK or SRCK High or Low			12	16	20	24	ns
Pulse Width	SRCLR or SRLOAD Low	t _w		12	16	20	24	115
	SRCLR† before SRCK†			12	16	20	24	
Minimum Setup Time	RCK1 before SRCK111	t _{su}		24	32	40	48	ns
	SER before SRCK1			12	16	20	24	
·	A thru H before RCK1			12	16	20	24	
Minimum Hol	d Time	t _h		0	0	, 0	0	ns
Maximum Inp	out Capacitance	C _{IN}		5			1	ρF
Power Dissip	ation Capacitance*	CPD						pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

[†] For AC switching test circuits and timing waveforms see section 2.

^{††} The RCK† before SRCK† setup time ensures that shift register will see stable data comming from the register output.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
 (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

These high-speed octal/bus transceivers are designed for asynchronous two-way communication between data buses. A direction control input (DIR) controls the flow direction of data. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A. The '643 transfers inverted data from the A bus to the B bus and non-inverted data from the B bus to the A bus. The '640 transfers inverted data in both directions.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

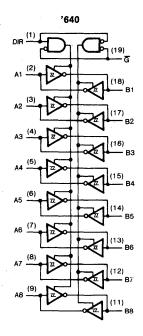
PIN CONFIGURATION

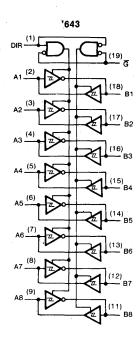
20 Vcc DIR 🗌 <u>ច</u> A1 [A2 🔲 B1 18 ☐ B2 АЗ **□** B3 Α4 Α5 15 □ B4 A6 □ B5 13 Α7 □ B6 8A Г 12 □ B7 B8 11 GND [

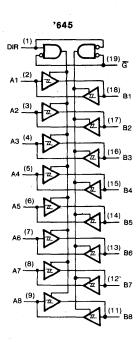
FUNCTION TABLE

	ontrol puts			
G	DIR	'640	'640 '643	
L	L	Inverted data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A
L	Н	Inverted data transmitted from Bus A to Bus B	Inverted data transmitted from Bus A to Bus B	Data transmitted from Bus A to Bus B
н	x	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)

LOGIC DIAGRAMS







Absolute Maximum Ratings*

Supply Voltage Range V _{CC} , −0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ $\pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} ... 4.5V to 5.5V DC Input & Output Voltages*, V_{IN} , V_{OUT} ... 0V to V_{CC} Operating Temperature Range KS74HCTLS: -40° C to $+85^{\circ}$ C KS54HCTLS: -55° C to $+125^{\circ}$ C Input Rise & Fall Times, t_r , t_t ... Max 500 ns Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т	= 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
		÷,	Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage		$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	tin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δίος	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tie6 ns), HCTLS640, HCTLS643, HCTLS645

Characteristic	Symbol	Conditions	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit	
				Тур		Guarantee	d Limits	
Maximum Propagation	t _{PLH}	C _L =50pf C _L =150p		9 12	12 15	16 21	19 25	ns
Delay, A to B, or B to A	t _{PHL}	C _L =50pF C _L =150p	9 12	12 15	16 21	19 25	ns	
Maximum Output Enable	tpzH	$R_i = 1 k\Omega$	C _L =50pF C _L =150pF	30 33	40 43	50 55	60 65	ns
Time, G or DIR to A or B	t _{PZL}	110-174	C _L =50pF C _L =150pF	30 33	40 43	50 55	60 65	113
Maximum Output Disable	tpHZ	$R_L = 1 k\Omega$		20	27	34	40	ne
Time, G or DIR to A or B	tpLZ	C _L =50pF	:	20	27	34	40	ns
Maximum Input Capacitance	CiN			5				рF
Maximum Output Capacitance	Cour	Output di	sabled	10				рF
Power Dissipation Capacitance* (per stage)	C _{PD}	Ğ=V _{CC} Ğ=GND	-	5 30				рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC^2} t_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

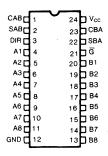
- . 8 bi-directional data paths
- · Transmits direct or stored data in either direction
- 24-pin 0.3" slim DIP package
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
 Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to + 85°C

KS54HACT: -55°C to + 125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



DESCRIPTION

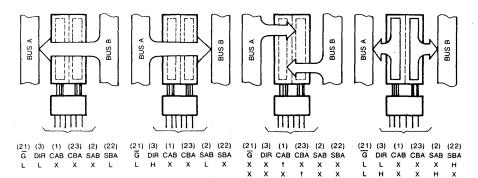
The '646 and '648 are bi-directional bus transceivers with D-type flip-flops and control circuitry to facilitate high speed multiplexed data transmission. The '646 transmits true data and the '648 transmits inverted data.

Data can be transmitted directly from one port to the other in either direction. It also can be stored in the flip-flops from either or both ports for subsequent transmission to the opposite port. Six control inputs govern the data flow:

- G
 (output enable) when high, all outputs are disabled, isolating the A and B ports. When low, one port is enabled at a time as determined by the DIR pin.
- DIR (direction control) disables A or B outputs per mitting the pins to be used as inputs thus determining the direction of a data flow. When DIR=high, data flows from A to B.
- SAB,SBA (data source AB and BA) determines whether data transmitted is from the data inputs or the registers associated with those inputs.
- CAB,CBA (Clock AB and BA) clocks data from the A inputs and the B inputs, respectively, into their associated registers. Since the clocks are not gated with the \overline{G} and DIR pins, data at the A and B pins can be clocked into the flip-flops at any time.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.



Real-Time transfer bus B to bus A

Real-Time transfer bus A to bus B Storage from A AND/OR B

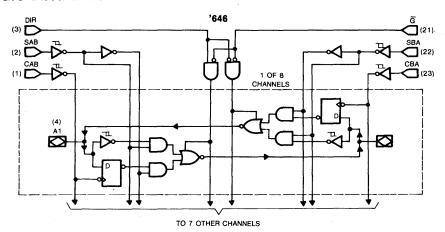
Transfer stored data to A AND/OR B

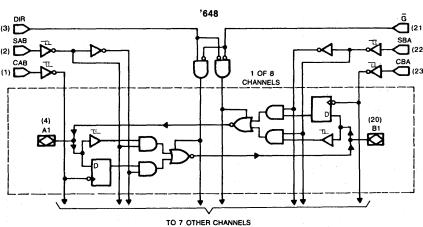
FUNCTION TABLE

Inputs						Data	1/0*	Operation or Function			
Ĝ	DIR	CAB	СВА	SAB	SBA	A1 thru A8	B1 thru B8	'646	'648		
	X	† X	X	X X	X X	input Not specified	input Not specified	Store A, B unspecified Store B, A unspecified	Store A, B unspecified Store B, A unspecified		
H H	X	↑ H or L	↑ H or L	X	X	Input	Input	Store A and B data Isolation, hold storage	Store A and B data isolation, hold storage		
L	L L	X	X H or L	X	L H	Output	Input	Real-Time B data to A bus Stored B data to A bus	Real-Time \bar{B} data to A bus Stored \bar{B} data to A bus		
L	Н	X H or L	X	L	X	Input	Output	Real-Time A data to B bus Stored A data to B bus			

^{*}The data output functions may be enabled or disabled by various signals at the \widetilde{G} and DIR inputs. Data input functions are always enabled, ie., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

LOGIC DIAGRAMS







KS54HCTLS **646/648** KS74HCTLS

Octal 3-State Bus Transceivers with Registers

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	p
Supply Voltage, V	V _{CC} 4.5V to 5.5V
DC Input & Outp	ut Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Tempe	rature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall	Times, t _r , t _f Max 500 ns
Unused inputs n	nust always be tied to an appropriate logic

voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T _a = -55°C to +125°C	Unit		
			Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	V _{IH}	,		2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v		
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6m A$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} = 0.1	٧		
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА		
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA		



Octal 3-State Bus Transceivers with Registers

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS646, HCTLS648

Characteristic	Symbol	Condition	s†		25°C 5.0V	V _{CC} = J.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
Maximum Clock Frequency	f _{max}	C _L =50pl	C _L =50pF		30	Guaranteed 25	20	MHz
Maximum Propagation	t _{PHL}	C _L =50pl		14 17	19 22	24 29	29 35	ns
Delay, A or B Input to B or A Output	t _{PHL}	C _L =50pl	=	14	19	24 29	29 35	113
Maximum Propagation	tpLH	C _L =50pf C _L =150pf	=	22 25	30 33	37 42	45 51	
Delay, CBA or CAB Input to A or B Output	t _{PHL}	C _L =50pF C _L =150p		22 25	30 33	37 42	45 51	ns
Maximum Propagation Delay,†† SBA or SAB input		C _L =50pf C _L =150p		26 29	35 38	44 49	53 59	ns
to A or B Output (with A or B High)	tpHL	C _L =50pF C _L =150pF		26 29	35 38	44 49	53 59	
Maximum Propagation Delay, SBA or SAB Input	tpLH	C _L =50pF C _L =150p		26 29	35 38	44 49	53 59	ns
to A or B Output (with A or B Low)	tpHL	$C_L = 50pF$ $C_L = 150pF$		26 29	35 38	44 49	53 59	
Maximum Output Enable Time, \overline{G} or DIR Input to	tpzL	$R_L = 1 k\Omega$	C _L =50pF C _L =150pF	33 36	45 48	56 61	67 73	ns
A or B Output	t _{PZH}	110 1110	C _L =50pF C _L =150pF	33 36	45 48	56 61	67 73	
Maximum Output Disable Time, G or DIR Input to A or B Output	t _{PHZ}	$R_L = 1 k\Omega$ $C_L = 50 pF$		26 26	35 35	44 44	53 53	ns
Pulse Duration, Clocks High or Low	tw			10	13	17	20	ns
Setup Time, A before CABt or B before CBAt	t _{su}	-		10	13	17	20	ns
Hold Time, A after CAB† or B after CBA†	th			0	0		0	ns
Maximum Input Capacitance	CIN			. 5				рF
Maximum Output Capacitance	Соит	Output Di	sabled	10				pF
Power Dissipation Capacitance*	C _{PD}							pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

^{††} These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

- . Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of Time and Inverting Data Paths
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
 (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION

CAB□	1	24	⊃v _{cc}
SAB	2	23	СВА
GAB 🗆	3	22	□ SBA
A1 🗆	4	21	₿ĞBA
A2 🗆	5	20	B1
A3 🗀	6	19	B2
A4 🗖	7	18	□ вз
A5 🗖	8	17	□ B4
A6 🗆	9	16	□ B5
A7 🗆	10	15	□ B6
A8 🗆	11	14	В7
GND 🗖	12	13	□ B8
			,

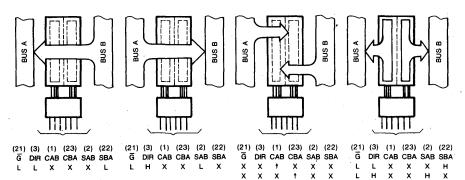
DESCRIPTION

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and GBA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.



Real-Time transfer bus B to bus A

Real-Time transfer bus A to bus B

Storage from A AND/OR B

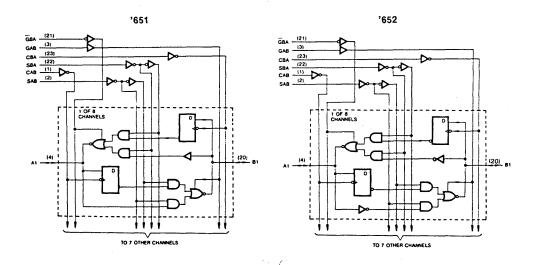
Transfer stored data to A and/or B

FUNCTION TABLE

		INP	UTS			DATA I/O* OPERATION OR FUNCTION				
GAB	ĞBA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'651	'652	
L L	H H	H or L	H or L	X X	X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data	
X H	H	† †	H or L	X**	X	Input Input	Not specified Output*	Store A, Hold B Store A in both registers	Store A Hald B Store A in both registers	
L L	X L	H or L	† †	X X	X X**	Not specified Output*	Input Input	Hold A, Store B Store B in both registers	Hold A, Store B Store B in both registers	
L	L	X X	X H or L	X	L	Output	Input	Real-Time B Data to A Bus Stored B Data to A Bus	Real-Time B Data to a Bus Stored B Data to A Bus	
H H	Н	X H or L	X	L H	X	Input	Output	Real-Time Ā Data to B Bus Stored Ā Data to Bus	Real-Time A Data to B Bus Stored A Data to B Bus	
Н	L	H or L	H or L	Ι	Н	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus	

^{*} The data output functions may be enabled or disabled by various signals at the GAB and GBA inputs. Data input functions are always enabled, ie., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

LOGIC DIAGRAMS



^{**} Select control=L: clocks can occur simultaneously
Select control=H: clocks must be staggered in order to load both registers

KS54HCTLS 651/652 KS74HCTLS

Octal 3-State Bus Transceivers with Registers

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

		•
Supply Voltage,	V _{CC}	4.5V to 5.5V
DC Input & Out	put Voltages*, V _{IN} ,	Vout OV to Vcc
Operating Temp	erature	
Range	KS74HCTLS:	-40°C to +85°C
	KS54HCTLS:	-55°C to +125°C
Input Rise & Fa	ll Times, t _r , t _f	Max 500 ns
•	must always be tied either V _{CC} or GND	to an appropriate logic

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
		* * * *	Тур	Guaranteed Limits			
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	ViL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} =0.1 3.84	V _{CC} = 0.1 3.7	٧
Maximum Low-Level Output Voltage	VoL	V_{IN} = V_{IH} or V_{IL} I_{O} =20 μ A I_{O} =12 μ A I_{O} =24 μ A	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	tin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_i≤6 ns), HCTLS651, HCTLS652

Characteristic	Symbol	conditions†			25°C = 5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit	
						Guaranteed Limits			
Maximum Clock Frequency	f _{max}	C _L =50pl	40	30	25	20	MHz		
Maximum Propagation Delay, A or B Input to	t _{PLH}	C _L =50pl		14 17	19 22	24 29	29 35		
B or A Ouput	t _{PHL}	C _L =50pl C _L =150		14 17	19 22	21 26	20 26	ns	
Maximum Propagation	t _{PLH}	C _L =50pl		22 25	30 33	37 42	45 51		
Delay, CBA or CAB Input to A or B Output	t _{PHL}	C _L =50pl C _L =150		22 25	30 33	37 42	45 51	ns	
Maximum Propagation Delay, SBA or SAB Input to	t _{PLH}	C _L =50pl C _L =150		26 29	35 38	44 49	53 59		
A or B Output (with A or B High)	t _{PHL}	C _L =50pF C _L =150pF		26 29	35 38	44 49	53 59	ns	
Maximum Propagation Delay, SBA or SAB Input to	t _{PLH}	C _L =50pl C _L =150	26 29	35 38	44 49	53 59			
A or B Output (with A or B Low)	t _{PHL}	C _L =50pl C _L =150		26 29	35 38	44 49	53 59	ns	
Maximum Output Enable Time. GBA to A or	t _{PZL}		$C_L=50pF$ $C_L=150pF$	33 39	45 48	56 61	67 73		
GAB to B	t _{PZH}	$R_L = 1 k\Omega$	C _L =50pF C _L =150pF	33 39	45 48	56 61	67 73	ns	
Maximum Output Disable Time, GBA to A or GAB to	t _{PHZ}	R _L =1kΩ		26	35	44	53	ns	
В	tPLZ	C∟=50pl	F	26	35	44	53	}	
Minimum Pulse Width Clocks High or Low	tw			10	13	17	20	ns	
Minimum Setup Time, A before CAB† or B before CBA†	t _{su}			10	13	17	20	ns	
Minimum Hold Time, A after CAB† or B after CBA†	th	•		0	. 0	0	0	ns	
Maximum Input Capacitance	CIN			5				рF	
Maximum Output Capacitance	Cout	Output D	isabled		10			рF	
Power Dissipation Capacitance*	C _{PD}							ρF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

 $^{^{\}dagger}$ For AC switching test circuits and timing waveforms see section 2.

- Bus Transceivers with inverting Outputs ('658) or True Outputs ('659)
- . Generates a Parity Bit for A Bus and B Bus
- Easily Cascadable
- · Internal Active Pull-Ups and Pull-Downs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- · 3-State outputs with high drive current
- (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KSTANCTI St. ... 409C to ... 459C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION

GAB 🗖	1	24 Vcc
A1 🗆	2	23 GBA
A2 🗀	3 .	22 🗖 B1
A3 🗆	4	21 B2
A4 🗆	5	20 🗆 B3
A5 🗖	6	19 🗖 B4
A6 🗖	7	18 🗆 B5
A7 🗆	8	17 86
A8 🗆	9	16. 🗆 B7
BPI 🛚	10	15 B8
вро 🗆	11	14 API
GND 🗖	12	13 APO

DESCRIPTION

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus, or from the B Bus to the A Bus, depending on the levels at the direction control inputs, GAB and GBA. These devices also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuits on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptiblity to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuits.

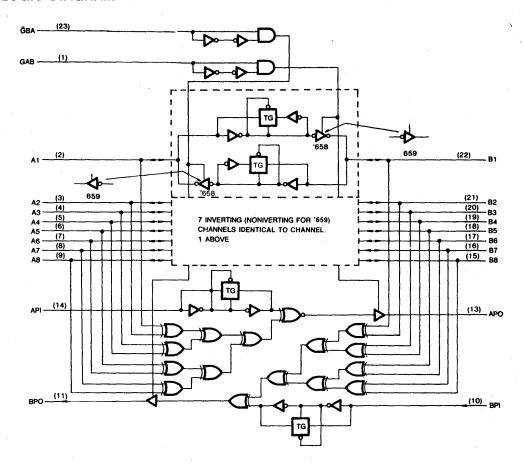
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

CONTROL INPUTS		NUMBER OF HIGH INPUTS ON	NUMBER OF HIGH INPUTS ON	ОШТ	PUTS	OPERATION		
ĞВА	GAB	A BUS AND API	B BUS AND BPI	APO	BPO	HCTLS658	HCTLS659	
L	1	X	0, 2, 4, 6, 8	Z	Н	B Data to A Bus	B Data to A Bus	
		X	1, 3, 5, 7, 9	Z	L	D Data to A Bus	D Data to A bus	
Н	н	0, 2, 4, 6, 8	X	Н	Z	A Data to B Bus	A Data to B Bus	
	''	1, 3, 5, 7, 9	X	L	Z	A Data to B Bus	A Data to B Bus	
Н	L	X	X	Z	Z	Isolation	Isolation	
		X	0, 2, 4, 6, 8		Н			
	н	X	1, 3, 5, 7, 9		L	B Data to A Bus,	B Data to A Bus,	
	''	0, 2, 4, 6, 8	X	Н		A Data to B Bus	A Data to B Bus	
		1, 3, 5, 7, 9	X	L			•	

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} , −0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C



Octal Bus Transceivers with Parity

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т,	a = 25°C	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS T _a = -55°C to +125°C	Unit	
		• •	Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1	v	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	ΔΙσο	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA.	

AC ELECTRICAL CHARACTERISTICS (Input tr. tr<6 ns), HCTLS658, HCTLS659

Characteristic	Symbol	Conditions†		$\begin{array}{c c} T_a = 25^{\circ}C \\ V_{co} = 5.0V \end{array}$		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
	<u> </u>			Тур		Guaranteed	Limits	
Maximum Propagation	teun	C _L =50pl C _L =150		20 23	25 28	30 35	39 45	
Delay, A or B to B or A	t _{PHL}	C _L =50pl C _L =150		20 23	25 28	30 35	39 45	ns
Maximum Propagation	tpLH	C _L =50pl		24 27	32 35	40 45	48 54	
Delay, A or B to B or A	tpHL	C _L =50pF C _t =150pF		24 27	32 35	40 45	48 54	ns
Maximum Propagation	tpLH	C _L =50pF C _L =150pF C _L =50pF C _L =150pF		20 23	25 28	30 35	39 45	ns
Delay A or B to APO or BPO	t _{PHL}			20 23	25 28	30 35	39 45	
Maximum Enable Time,	tpzH	Rı=1kΩ	C _L =50pF C _L =150pF	20 23	25 28	30 35	39 45	ne
GAB or GBA to APO or BPO	tpzL	HL=1KU	C _L =50pF C _L =150pF	20 23	25 28	30 35	39 45	ns
Maximum Disable Time, GAB or GBA to	tpLZ	R _L =1kΩ		20	25	30	39	ns
APO or BPO	tpHZ	C _L =50pF		20	25	30	39	ns
Maximum Input Capacitance	CIN			5				pF
Maximum Output Capacitance	Соит							рF
Power Dissipation Capacitance*	C _{PD}							рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.

Octal Bus Transceivers with Parity

FEATURES

- Bus Transceivers with Inverting Outputs ('664) or True Outputs ('665)
- . Generates a Parity Bit for A Bus and B Bus
- Easily Cascadable
- . Internal Active Pull-Ups and Pull-Downs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION

DIR C	1 -	24	J v _{cc}
A1 C	2	23	ΒĜ
A2 🗖	3	22	⊒ B1
A3 🗖	4	21	B2
A4 🗖	5	20	□ B3
A5 🗖	6	19	□ B4
A6 🗖	7	18	B 5
A7 🗖	8	17	□ B6
A8 🗖	9	16	□ B7
ВРІ 🗖	10	15	□B8
вро 🗖	11	14	API
GND 🗖	12	13	D APO

DESCRIPTION

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus or from the B Bus to the A Bus, depending on the level at the direction control input, DIR. The enable input, \overline{G} can be used to disable the device so that the buses are isolated. These devices will also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuitry on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by the activity on the bus. The advantage of this arrangement is tht when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuitry.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

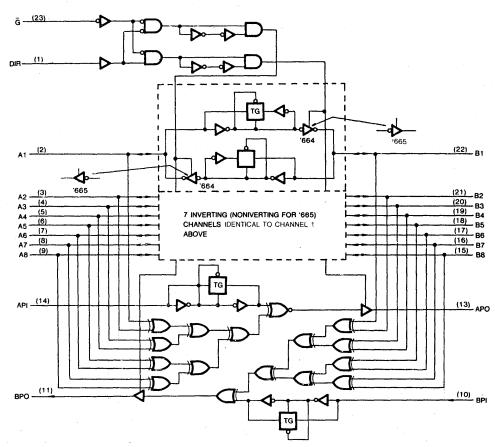
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

CONTROL		NUMBER OF HIGH INPUTS ON	NUMBER OF HIGH INPUTS ON	OUTPUTS		OPERATION		
G DIR	A BUS AND API	B BUS AND BPI	APO	вро	'664	'665		
	1	X	0, 2, 4, 6, 8	·Z	Н	B Data to A Bus	B Data to A Bus	
L	- L	X	1, 3, 5, 7, 9	Z	L	B Data to A Bus		
1	н	0, 2, 4, 6, 8	X	Н	Z	Ā Data to B Bus	A Data to B Bus	
L	11	1, 3, 5, 7, 9	X	L	Z.	A Data to B Bus	A Data to B Bus	
Н	X	X	X	Z	Z	Isolation	Isolation	



LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diodé Current, IIK
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply vollage, vcc		· · · · · · · · · · · · · · · · · · ·	30 10 3.3	٧
DC Input & Output Vo	oltages*, V _{IN} ,	Vout	QV to Vo	С
Operating Temperatur	е			
Range K	S74HCTLS:	-40°C	to +85°	C
K	S54HCTLS:	-55°C t	o +125°	Ç
Input Rise & Fall Time	es, t_r , t_f		1ax 500 r	ıs
Unused inputs must a	always be tied	to an appr	opriate logi	ic
voltage level (either	V _{CC} or GND))		



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=U\mu A$		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS664/655

** Characteristic	Symbol	Conditions†		conditions†			25°C = 5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
		1.		Тур		Guaranteed	Limits	1		
Maximum Propagation	tецн	C _L =50pt C _L =150		20 23	25 28	30 35	39 45	ns		
Delay, A or B to B or A	t _{PHL}	C _L =50pl C _L =150		20 23	25 28	30 35	38 36			
Maximum Propagation	t _{PLH}	C _L =50pl C _L =150		24 27	32 35	40 45	48 54			
Delay, A or B to APO or BPO	t _{PHL}	C _L =50pl C _L =150		24 27	32 35	40 45	48 54	ns		
Maximum Propagation	t _{PLH}	C _L =50pF C _L =150pF		20 23	25 28	30 35	39 45	ns		
Delay, API or BPI to APO or BPO	t _{PHL}		C _L =50pF C _i =150pF		25 28	30 35	39 45	113		
Maximum Output Enable	t _{PZH} F	Rı=1kΩ	C _L =50pF C _L =150pF	24 27	32 35	40 45	48 54	ns		
Time, G to A or B		nt-ive	C _L =50pF C _L =150pF	24 27	32 35	40 45	48 54	113		
Maximum Output Delay	t _{PHZ}	$R_L = 1 k\Omega$		24	32	40	48			
Time, G to A or B	tpLZ	C _L =50pF		24	22	40	50	ns		
Maximum Output Enable	t _{PZH}	Rı=1kΩ	C _L =50pF C _L =150pF	24 27	32 35	40 45	48 54			
Time DIR to A or B	t _{PZH}	וון – ואנו	C _L =50pF C _L =150pF	24 27	32 35	40 45	48 54	ns		
Maximum Output Disable	t _{PHZ}	$R_L = 1 k\Omega$		20	32	40	48	ns		
Time, DIR to A or B	tHLZ	t _{HLZ} C _L =50pF		24	32	40	48	113		
Maximum Input Capacitance	CIN			5				рF		
Maximum Output Capacitance	Cout	Output D	Output Disabled					pF		
Power Dissipation Capacitance*	C _{PD}							pF		

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \, V_{CC}^2 \, f_{in}$.
† For AC switching test circuits and timing waveforms see section 2.

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Expandable to 512 Words of N-bits
- · For use as:
 - Scratch pad memory
 - Buffer storage between processors
 - Bit storage in fast multiplication designs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

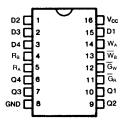
IoL = 8 mA @ VoL = 0.5V

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLES

WRITE MODE SELECT TABLE

OPERATING	INPU	ITS	INTERNAL	
MODE	Ğω	Dn	LATCHES(a)	
Write Data	L	L H	L H	
Data Latched	н	х	no change	

11 3

NOTE:

a. The Write Address (W_A and W_B) to the "Internal latches" must be stable while \bar{G}_W is LOW for conventional operation.

DESCRIPTION

The '670 is a 16-bit 3-State Register File organized as 4 words of 4 bits each. Separate Read and Write Address and Enable Inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs (W_A and W_B) determine the location of the stored word. When the write enable (\overline{G}_W) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the \overline{G}_W is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-State outputs. Data and Write Address inputs are inhibited when \overline{G}_W is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs $(\overline{R}_A$ and $R_B). The addressed word appears at the four outputs when the read enable <math display="inline">(\overline{G}_{R})$ is LOW. Data outputs are in the HIGH impedance "off" state when the read enable input is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-State outputs together. Since the limiting factor for expansion is the output HIGH current, further stacking is possible by tying pull-up resistors to the outputs to increase the l_{OH} current available. Design of the read enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the Enable and Address inputs of each device in parallel.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

READ MODE SELECT TABLE

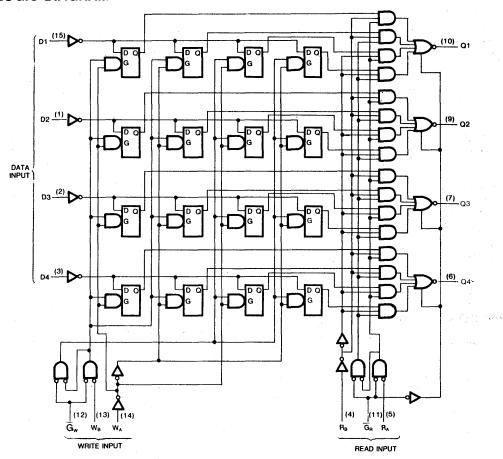
OPERATING	ı	NPUTS	OUTDUT		
MODE	ĞR	INTERNAL LATCHES(b)	OUTPUT Q _n		
Read	L	L	L		
neau	L	н	H H		
Disabled	н	н	(Z)		

NOTE:

b. The selection of the "internal latches" by Read Address $(\overline{R}_A$ and $R_B)$ are not constrained by \overline{G}_W or \overline{G}_R operation.



LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , $-0.5V$ to $+7V$
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} −65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, V_{IN} , V_{OUT} . OV to V_{CC} Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r , t_t . Max 500 ns Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit	
			Тур	Guaranteed Limits				
Minimum High-Level Input Voltage	∖ V _{IH} √.			2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1	٧	
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	ν	
Maximum Input Current	IN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА	
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	ΔΙσο	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (Input tr., tr 6 ns), HCTLS670

Characteristic S		Symbol	Con	ditions†	-	25°C = 5.0V	$KS74HCTLS$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10^{\circ}$	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
				Тур		Guarante	eed Limits		
			C _L =50pf		20	32	40	48	
Maximum F	Propagation Delay,	tpLH	$C_L = 150$	oF	23	35	45	54	ns
R _A or R _B to	o Output		C _L =50pf		20	32	40	48	
			$C_L = 150$		23	35	45	54	ļ.,
			$C_L = 50pf$		27	36	45	59	
	Propagation Delay,	·rLn	$C_L = 150$	oF	30	39	50	65	ns
Gw to Outp	out		C _L =50pF		27	36	45	59	
			C _L =150		30	39	50	65	
			C _L =50pF		27	38	45	59	
	Propagation Delay,	<u></u>	C _L =150		30	39	50	65	ns
Data to Ou	tput		C _L =50pf		27	36	45	54	
			C _L =150 _l		30	39	50	60	<u> </u>
		t _{PZH}	ļ	C _L =50pF	24 27	32 35	40 45	48 54	
Maximum (Output Enable Time		$R_L = 1 k\Omega$			<u> </u>			ns
GR to Outp	out ·	tpZL		$C_L = 50 pF$ $C_I = 150 pF$	24 27	32 35	40 45	48 54	
	Outside Disable Time	tour	D = 41.0	[С[—130рі	24	32	40	48	
G _R to Outp	Output Disable Time		$R_L = 1 k\Omega$ $C_L = 150 \mu$	· ·	24	32	40	48	ns
ļi		I IPLZ	0[100]						
Set up	D _n to G _W	tsu			9	12	15	18	ns
Time	W _A ,W _B to G _W				15	18	23	27	
Hold	D _n to G _W	th			0	0	0	0	ns
Time	W _A , W _B to G _W				0	0	0	0	
Maximum I	nput Capacitance	CIN			5				pF
Maximum (Output Capacitance	Cout	Output di	sabled	10				pF
Power Diss	sipation Capacitance*	C _{PD}							рF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \; V_{CC}{}^2 \; f_{in}$



For AC switching test circuits and timing waveforms see section 2.

- '679: 12-bit to 4-bit comparator with enable
- '680: 12-bit to 4-bit comparator with latch
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- · High-Drive-Current outputs:
- (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C
 - KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

The '679 and '680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The '679 features an enable input (\overline{G}) . When \overline{G} is low, the device is enabled. When \overline{G} is high, the device is disabled and the output is high regardless of the A and P inputs. The '680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

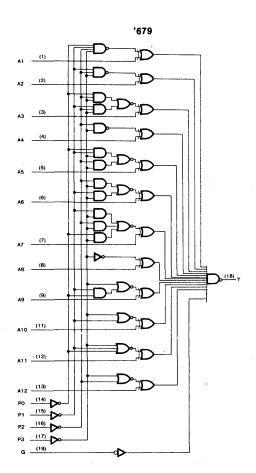
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

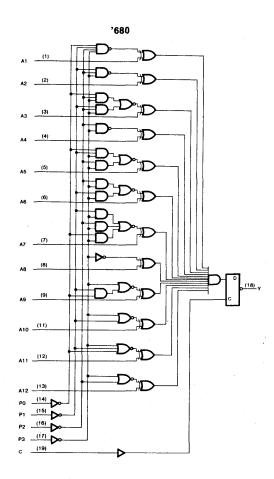
PIN CONFIGURATIONS

	'679
A1	20 V _{cc} 19 G
A4 4 A5 5	18 U Y 17 P3 16 P2
A6	15 P1 14 P0 13 A12
A9 9 GND 10	12 A11 11 A10

٠.		'680		
A1	1 2 3 4 5 6 7	'680	20 19 18 17 16 15 14	V _{cc} C Y P3 P2 P1 P0 A12
A9 GND	9 10		12 11	A11 A10

LOGIC DIAGRAMS





FUNCTION TABLE

679	'680					IN	PUTS	CON	MON	1 TO	'679	AND	'680					OUTPUT
Ğ	С	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	Y
L	Н	L	L	·L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	н	Н	L
L	Н	L	L	L	Н	L	Н	Н	Н	Н	Н	Н	H	Н	Н	Н	Н	L
L	н	L	L	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	н	L	L	Н	Н	· L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Н	L	Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L
L '	Н	L	Н	L	н	L	L	L	, L	L	Н	Н	Н	Н	Н	Н	Н	L
L	Н	L	Н	Н	L	L	L	L	L	L	L	Н	H	Н	н	H.	Н	L
L	Н	L	Н	Н	Н	L	L	L	L	L	L	L	Н	Н	Н	Н	н	L
L	Н	Н	L	L	L	L	L	L	L	L	L	L	L	Н	Н	Н	Н	L
L	Н	н	L	L	н	L	L	L	L	L	L	L	L	L	H.	н	Н	L
L	Н	Н	L	Н	L	L	L	L	L.	L	L	L	L	L	L	Н	Н	. L
L	н	н	L	Н	Н	L	L	L	L	L	L	Ĺ	L	L	L	L	Н	L
L	Н	Н	Н	L	L	L	L	L	L	L	L	L	L	Н	Н	Н	L	L*
L	,H	Н	Н	L	Н	L.	L	L	L	L	L	L	L	L	Н	Н	L	L*
L	Н	Н	Н	Н	L	L	L	L	L	L	L	L	Ļ	L	L	Н	L	L*
L	Н	Н	Н	Н	Н	L	L	L	L	L	L	L	L	L	L	L	L	L
L	Н							All o	ther o	combi	natio	าธ						Н
Н								'679	: Any	com	binati	on						Н
	L							'680	: Any	com	binati	on	£ 1					Latched

Note: These three rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for all combinations in which P=12, 13 and 14. If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change P≥9 to P=9 ... 11/13 ... 15, P≥10 to P=10/11/14/15, and P≥11 to P=11/15.

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ m/s}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ m/s}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 1.5V + 1.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond

^{*} Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V _{CC}	4.5V to 5.5V
DC Input & Output Voltages*, V _{IN} , V _{OUT}	OV to Vcc
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	v
Maximum Low-Level Output Voltage		$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tr<6 ns), HCTLS679

Characteristic	Symbol	Symbol Conditions [†]		25°C = 5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	<u> </u>
Maximum Propagation Delay, Any P to Y	t _{PLH}	C _L =50pF C _L =150pF	24 27	32 35	40 4 5	48 54	ns
	ŧрнL	C _L =50pF C _L =150pF	27 30	32 35	40 45	48 54	113
Maximum Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	21 24	28 31	35 40	42 48	ns
Any A to Y	t _{PHL}	C _L =50pF C _L =150pF	21 24	28 31	35 40	42 48	115
Maximum Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	18 21	24 27	30 35	36 42	ns
G to Y	t _{PHL}	C _L =50pF C _L =150pF	18 21	24 27	30 35	36 42	113
Maximum Input Capacitance	C _{IN}		·5		,		pF
Power Dissipation Capacitance*	C _{PD}						pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

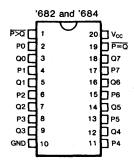
AC ELECTRICAL CHARACTERISTICS (Input t_r , $t_i \!\!\!\! < \!\!\! < \!\!\! < \!\!\! < ns$), HCTLS680

Characteristic	Symbol	Conditions†		25°C : 5.0V	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit
,		**	Тур		Guaranto	eed Limits	
Maximum Propagation Delay,	tpLH	$C_L=50pF$ $C_L=150pF$	27 ⁻ 30	36 39	45 50	54 60	ns
Any P to Y	t _{PHL}	C _L =50pF C _L =150pF	27 30	32 35	40 45	48 64	
Maximum Propagation Delay, Any A to Y	t _{PLH}	C _L =50pF C _L =150pF	24 27	32 35	40 45	48 64	ns
	t _{PHL}	C _L =50pF C _L =150pF	24 27	32 35	40 45	48 64	
Maximum Propagation Delay.	t _{PLH}	C _L =50pF C _L =150pF	19 22	26 29	32 37	38 44	ns
C to Y	t _{PHL}	$C_L = 50pF$ $C_L = 150pF$	19 22	26 29	32 37	38 44	115
Set up Time An before E	tsu		9	12	15	18	ns
Hold Time An after E	t _h		0	0	0	0	ns
Input Gapacitance	CIN		5				pF
Power Dissipation Capacitance*	C _{PD}						pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.
† For AC switching test circuits and timing waveforms see section 2.

- Compares Two 8-Bit Words
- '682 has 20kΩ pull-up Resistors on the Q Inputs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs:
- (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C
- KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS



	'686		
į P>Ω α	, ~	24	bv∞
Ğ١Д	2	23	.G2
PO C	3	22	P≅Q
ᅃᄃ	4	21	Q7
P1 C	5	20	P7
입다	6	19	D NC
NC [7	18	Q6
P2 🗖	8	17	₽6
Q2 C	9	16	Q5
P3 🗖	10	15	P5
Q3 🗖	11	14	Q4
GND 🗆	12	13	P4

NC-No internal connection

DESCRIPTION

These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide $\overline{P=Q}$ and $\overline{P>Q}$ outputs. The '682 features 20-k Ω pull-up termination resistors on the Q inputs for analog or switch data.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

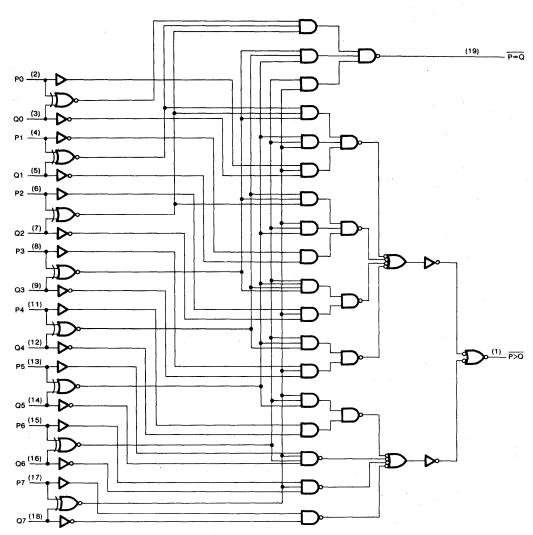
INPUTS			OUTPUTS		
DATA	ENABLES		0011 010		
P, Q	Ğ1	Ğ2	P=Q	P>Q	
P=Q	L	X	L	Н	
P>Q	X	L	н	L	
P <q< td=""><td>X</td><td>Х</td><td>H</td><td>Н</td></q<>	X	Х	H	Н	
P=Q	Н	Х	Н	Н	
P>Q	X	Η.	H	Н	
X	н	Н	н	н	

NOTES: 1. The last 3 lines of the function table apply only to the device having enable inputs, i.e., '686.

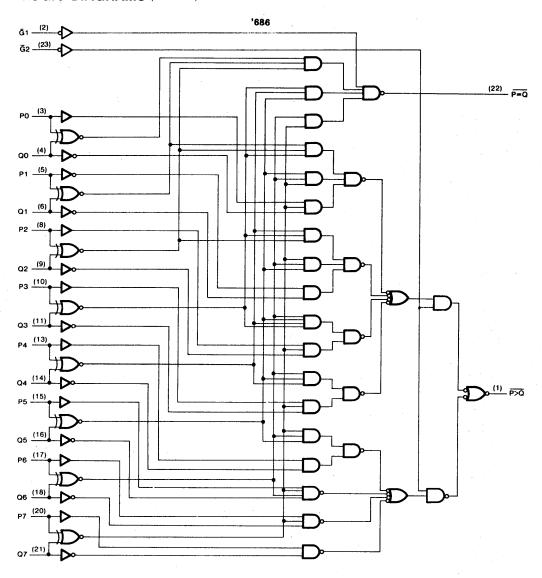
 The P<Q function can be generated by applying the P=Q and P>Q outputs to a 2-input NAND gate.

LOGIC DIAGRAMS

'682 or '684



LOGIC DIAGRAMS (continued)



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	•	•
Supply Voltage,	V _{CC}	4.5V to 5.5V
DC Input & Outp	ut Voltages*, V _{IN}	, V _{OUT} OV to V _{CC}
Operating Tempe	erature	
Range	KS74HCTLS:	-40°C to +85°C
	KS54HCTLS:	-55°C to +125°C
Input Rise & Fall	Times, t_r , t_f	Max 500 ns
Unused inputs r	nust always be tied	I to an appropriate logic
voltage level (e	either V _{CC} or GND))

1916

Parameter	Parameter Symbol Te		Test Conditions T _A = 25°C		KS74AHCT T _A = -40°C to +85°C	54AHCT T _A = -55°C to +125°C	Unit
		. 1	Тур		Guaranteed Limit		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage (Totem-pole Outputs)	VoH	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V _{CC} 4.2	V _{CC} -0.1	V _{CC} -0.1 3.84	V _{CC} −0.1 3.7	٧
Maximum Low-Level Output Voltage (All Outputs)	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current, ('682 Q Inputs)		V _{CC} =Max V _{IN} =2.7V V _{IN} =0.4V		-0.2 -0.4	-0.2 -0.4	-0.2 -0.4	mA
Maximum Input Current (All other Inputs)	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent	Icc	For '682: V _{IN} =GND (Q0-Q7) V _{IN} =V _{CC} or GND (all other inputs)		3.5	3.5	3.5	mA
Supply Current		For '684 and '688 V _{IN} =V _{CC} or GND I _{OUT} =0µA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin $V_1=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS682, HCTLS684, HCTLS686

Characteristic	Symbol	Symbol Conditions [†] $V_{CC} =$			KS74HCTLS T _a = -40°C to +85°C V _{CC} =5.0V±10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	1
Maximum Propagation Delay,	t _{PLH} *	C _L =50pF C _L =150pF	18 21	25 28	31 36	38 44	ns
P or Q to P=Q	tpHL	C _L =50pF C _L =150pF	18 21	25 28	31 36	38 44	
Maximum Propagation Delay, P or Q to P>Q	tpLH	C _L =50pF C _L =150pF	22 25	32 35	38 43	45 51	ns
	t _{PHL}	C _L =50pF C _L =150pF	22 25	30 33	38 43	45 51	,,,,
Maximum Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	15 18	20 23	25 30	30 36	ns
G1 to P=Q ('686 Only)	t _{PHL}	C _L =50pF C _L =150pF	15 18	20 23	25 30	30 36	
Maximum Propagation Delay, G2 to P <q ('686="" only)<="" td=""><td>t_{PLH}</td><td>C=50pF C_L=150pF</td><td>18 21</td><td>25 28</td><td>31 36</td><td>38 44</td><td>ns</td></q>	t _{PLH}	C=50pF C _L =150pF	18 21	25 28	31 36	38 44	ns
	t _{PHL}	C _L =50pF C _L =150pF	18 21	25 28	31 36	38 44	113
Maximum Input Capacitance	CIN		- 5				pF
Power Dissipation Capacitance*	C _{PD}						pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

FEATURES

- Compares Two 8-Bit Words
- Choice of Totem-pole ('688) and open-drain ('689) outputs ('688 is identical to '521)
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- . Low power consumption characteristic of CMOS
- · High drive current outputs:
- ($l_{OL} = 24 \text{ mA } @ V_{OL} = 0.5 \text{V}$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74HCTLS: -40°C to +85°C
- KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

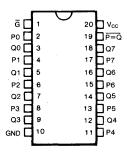
DESCRIPTION

These identity comparators perform comparisons of two 8-bit binary or BCD words. The output of '688 is totempole while '689's are open-drain.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

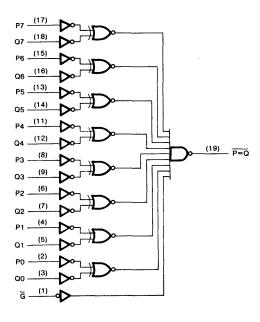
PIN CONFIGURATION



FUNCTION TABLE

IN	PUTS	OUTPUT
DATA P.Q	ENABLE G	P=Q
P=Q	L	L
P>Q	L	Н
P <q< td=""><td>L</td><td>Н</td></q<>	L	Н
X	Н	Н

LOGIC DIAGRAM (Positive Logic)



Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, IIK
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IoK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V + 2.5V$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pdt 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V DC Input & Output Voltages*, V_{IN} , V_{OUT} . . OV to V_{CC} Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t_r, t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit		
	<u>.</u>		Тур	Typ Guaranteed Limits					
Minimum High-Level Input Voltage	. V _{IH}			2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v		
Minimum High-Level Output Voltage ('688 only)	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v		
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ		
Maximum 3-State Leakage Current ('689 only)	loz	V _{IN} =V _{IH} or V _{IL} V _{OUT} =V _{CC}		±0.5	±5.0	±10.0	μΑ		
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA		

AC ELECTRICAL CHARACTERISTICS (input tr. tre6 ns), HCTLS688

Characteristic	Symbol	Conditions [†]	-	25°C 5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V ± 10%	Unit
-			Тур		Guaranteed	Limits	
Maximum Propagation Delay,	tpLH	C _L =50pF C _L =150pF	16 19	22 25	28 33	33 39	ns
P to P=Q	t _{PHL}	C _L =50pF C _L =150pF	16 19	22 25	28 33	33 39	110
Maximum Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	16 19	22 25	28 33	33 39	ns
Q to P=Q	t _{PHL}	C _L =50pF C _L =150pF	16 19	22 25	28 33	33 39	1113
Maximum Propagation Delay.	t _{PLH}	C _L =50pF C _L =150pF	15 18	20 23	25 30	30 36	ns
G to P=Q	t _{PHL}	C _L =50pF C _L =150pF	15 18	20 23	25 30	30 36	"
Maximum Input Capacitance	CIN		5				рF
Power Dissipation Capacitance*	C _{PD}						pF

^{*} CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 fin.

AC ELECTRICAL CHARACTERISTICS (Input tr. tre6 ns), HCTLS689

Characteristic	Symbol	Conditions [†]	ı	25°C :5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} =5.0V± 10%	Unit
			Тур		Guaranteed	Limits	7
Maximum Propagation Delay,	t _{PLH}	C _L =50pF C _L =150pF	24 27	31 34	37 42	43 49	ns
P to P=Q	t _{PHL}	C _L =50pF C _L =150pF	19 22	26 29	32 37	38 44	113
Maximum Propagation Delay, Q to P=Q	t _{PLH}	C _L =50pF C _L =150pF	24 27	31 34	37 42	43 49	ns
	t _{PHL}	C _L =50pF C _L =150pF	19 22	26 29	32 37	38 44	113
Maximum Propagation Delay, G to P=Q	t _{PLH}	C _L =50pF C _L =150pF	23 27	29 32	35 40	41 47	ns
	t _{PHL}	C _L =50pF C _L =150pF	18 21	24 27	30 35	36 42	115
Maximum Input Capacitance	CIN		5				рF
Power Dissipation Capacitance*	C _{PD}						рF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.



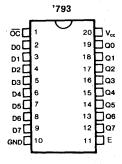
[†] For AC switching test circuits and timing waveforms see section 2.

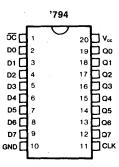
[†] For AC switching test circuits and timing waveforms see section 2.

FEATURES

- I/O port configuration enables output data back onto input bus
- . Latch ('793) and and Register ('794) options
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- · Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (loL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C
 KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS





DESCRIPTION

These are 8-bit latches/registers that allow temporary storage and retrieval of data on a bus. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in a '793 or '794, for verification and/or updating.

The data is loaded in the registers on the positive-edge of the clock (CLK) for the '794. The data is passed through the '793 when E is high, and it is latched when E goes low The output control (\overline{OC}) is used to enable data on the D0-D7 pins. when \overline{OC} is low the output of the latches/registers is enabled on D0-D7, enabling D as an output bus so that the host can perform a read operation. When \overline{OC} is high, D0-D7 are inputs to the latches/registers configuring D as an input bus.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

'793

E	ос	Q	D
L	L	Q ₀ **	Output, Q
L	н	Qo**	Input
H†	L	D*	Output, Q*
Н	Н	D	Input

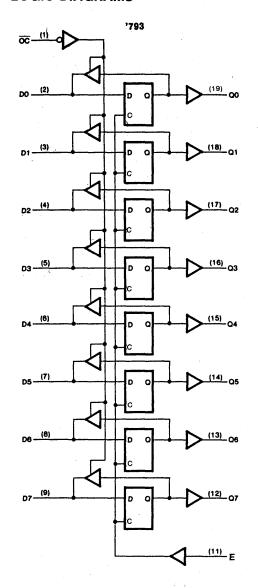
- In this case the output of the latch feeds the input, and a "race" condition results.
- ** Qo represents the previous "latched" state.
- † This transition is not a normal mode of operation and may produce hazards.

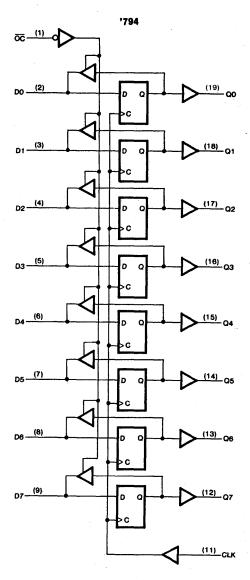
•	7	9	4

CLK	ŌĈ	Q	D
L or H or ↓	L	Qo	Output, Q
L or H or ↓	Н	Qo	Input
, †	L	Qo	Output, Q*
↑	н	D	Input

* In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Qo.







Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_l < -0.5V \text{ or } V_l > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Recommended Operating Conditions

		•
Supply Voltage, V	cc	4.5V to 5.5V
DC Input & Outpu	t Voltages*, V _{IN} ,	V_{OUT} OV to V_{CC}
Operating Temper	ature	•
Range	KS74HCTLS:	-40°C to +85°C
	KS54HCTLS:	-55°C to +125°C
Input Rise & Fall T	limes, t_r , t_f	Max 500 ns
•	•	to an appropriate logic
voitage ievei (ei)	ther Vcc or GND	· ·

Characteristic	Symbol	Test Conditions	est Conditions T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур	Guaranteed Limits			1
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	٧
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20µA I _O =12mA I _O =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

Plastic Package (N): -12mW/°C from 65°C to 85°C

AC ELECTRICAL CHARACTERISTICS (Input tr., tr 46 ns), HCTLS793, 794

Ch	Characteristic Symbol Conditions†		T _a = 2 V _{CC} =		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit		
							Guaranteed Limits		
Maximum C ('794 only)	lock Frequency	t _{max}	C _L =50pF	=	50	40	35	30	MHz
Maximum P	ropagation Delay,	tpLH	C _L =50pF C _L =150p		14 17	18 21	23 28	27 33	ns
	('793 only)	t _{PHL}	C _L =50pf C _L =150p		14 17	18 21	23 28	27 33	113
Maximum P	Propagation Delay	t _{PLH}	C _L =50pF C _L =150g		15 18	20 23	25 30	30 36	
	Maximum Propagation Delay, CLK/E to Any Q			C _L =50pF C _L =150pF		20 23	25 30	30 36	ns
Maximum F	nable Time.	tpzH	B ₁ = 1k0	C _L =50pF C _L =150pF	15 18	20 23	25 30	30 36	ns
OC to D			(C=Low	C _L =50pF C _L =150pF	15	20 23	25 30	30 36	lis
Maximum D	Disable Time,	t _{PHZ}		C _L =50pF for '793)	15 15	20 20	25 25	30 30	ns
Minimum Po		tw			10	15	18	20	ns
Minimum Setup Time	D before E↓ ('793) D before CLK†('794)	t _{su}			10	10	13	15	ns
Minimum	D after E↓ ('793)	th			8	10	13	15	ns
Hold Time D after CLK1 ('794)		ייי			0	0	0	0	7113
Maximum Inp	ut Capacitance	CiN			5				pF
Maximum Ou	tput Capacitance	Соит			10				рF
Power Dissip	ation Capacitance*	CPD				<u> </u>			ns

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}{}^z \ f_{in}$

[†] For AC switching test circuits and timing waveforms see section 2.

KS54HCTLS **821/822** KS74HCTLS

10-Bit Bus Interface Flip-Flops with 3-State Outputs

Preliminary Specifications

FEATURES

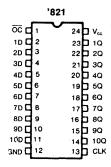
- Functionally Equivalent to AMD's Am29821 and Am29822
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
 - ($I_{OL} = 24$ mA @ $V_{OL} = 0.5V$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS





DESCRIPTION

These 10-bit bus-interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

All of the flip-flops are edge-triggered and D-type. On the positive transition of the clock the Q outputs on the '821 will be true, and on the '822 will be complementary to the data input.

A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control (\overline{OC}) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

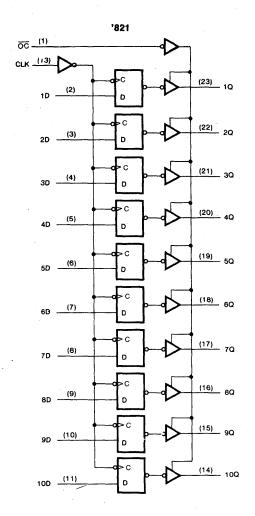
FUNCTION TABLES

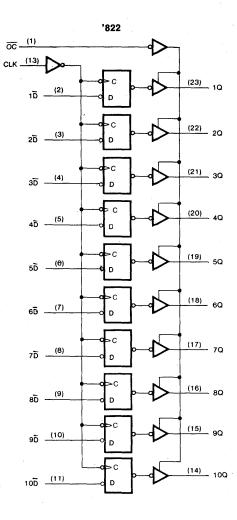
(Each Flip-Flop)

			'821	
		Inputs		Output
	ŌĊ	CLK	D	Q
Ī	L	1	Н	Н
	L	. 1	L	L
	L	, L	X	Q ₀ Q ₀
	L	Ή	X	Q_0
	Н	Х	X	Z

'822

	Inputs	Output		
OC	CLK	D	Q	
L	†	Н	L	
L	†	L	н	
L	L	Χ	Qo	
Ł	Н	Х	Q ₀ Q ₀	
Н	Χ	X	Z	





Absolute Maximum Ratings*

Supply voltage Hange VCC,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ $\pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, $P_{d}{}^{\dagger}$ 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

• • • •
Supply Voltage, V _{CC} 4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT OV to Voc
Operating Temperature
Range KS74HCTLS: -40°C to +85°C
KS54HCTLS: -55°C to +125°C
Input Rise & Fall Times, $t_r, t_f \ldots \ldots Max 500 ns$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T _a = -55°C to +125°C	Unit
					Guaranteed Limits		
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	>
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙος	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr, tr 66 ns), HCTLS821, HCTLS822

Characteristic	Symbol			Conditions†		T _a = 25°C V _{CC} = 5.0V		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10^{\circ}\text{M}$	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
				Тур		Guaranteed Limits				
Maximum Operating Frequency	f _{max}			40	35	30	25	MHz		
Maximum Propagation Delay,	t _{PLH}		C _L =50pF C _L =150pF		20 23	25 30	30 36	ns		
CLK to any Q	t _{PHL}	C _L =50pl C _L =150pl		15 18	20 23	25 30	30 36	1,0		
Maximum Output Enable Time, OC to any Q	tezu	R _i = 1 kΩ	C _L =50pF C _L =150pF	18 21	24 27	30 35	36 42	ns		
	tpZL	11[-172	C _L =50pF C _L =150pF	18 21	24 27	30 35	36 42	113		
Maximum Output Disable	t _{PHZ}	$R_L = 1 k\Omega$!	18	24	30	36	ns		
Time, OC to any Q	t _{PLZ}	C _L =50pl	F	18	24	30	36	113		
Minimum Pulse Width, CLK High or Low	t _w			12	16	20	24	ns		
Minimum Setup Time, Data before CLK1	t _{su}	-		12	16	20	24	ns		
Minimum Hold Time, Data after CLK†	th		10 mm 10 mm	0	0	0	0	ns		
Maximum Input Capacitance	CiN			5				рF		
Maximum Output Capacitance	Соит	OC=Vcc		10				рF		
Power Dissipation Capacitance* (per stage)	C _{PD}	$\overline{OC} = V_{CC}$ $\overline{OC} = GNI$		5 20				рF		

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}

[†] For AC switching test circuits and timing waveforms see section 2.

FEATURES

- Functionally Equivalent to AMD's Am29823 and Am29824
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- . Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS

'823

<u></u>	24 DVcc
1002	23 10
2003	22 5 20
3DC 4	21 30
400 5	20 140
5D 6	19 50
6D 7	18 60
7DC 8	17 570
8D d 9	16 180
9D 🗖 10	15 90
ਟਜ਼ ਹੈ 11	14 CLKEN
GND 12	13 CLK

'824

$\overline{\infty}d$,	24	V _{cc}
1DC	2	23	1Q
2Ď 🗖	3	22	2Q
зБД		21	3Q
4Ď□	5	20	1 4Q
5 D C	6	19	⊃ 5Q
65년	7	18	3 60
750	8	17	7 0
85 C	9	16	⊒ 80
9 D [10	15	⊒ 9Q
CLRC	11	14	CLKEN
GND 🛚	12	13	CLK

DESCRIPTION

These 9-bit bus interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

With the clock enable (CLKEN) low, the D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high will disable the clock buffer, thus latching the outputs. The '823 has noninverting D inputs and the '824 has inverting D inputs. Taking the CLR input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input (\overline{OC}) can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

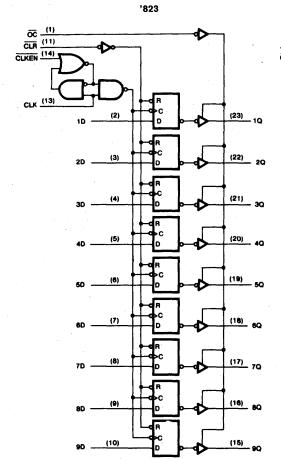
FUNCTION TABLES

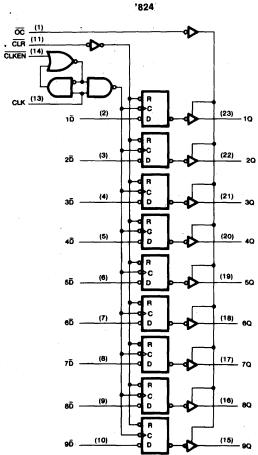
'823

		INPUT			OUTPUT
ōc	CLR	CLKEN	CLK	D	Q
L	L	Х	X	Х	L
L	H	L	- ↑	Н	н
L	Н	L	†	L	L
L	Н	Н	Χ	X	Q ₀
Н	X	Χ	X	X	Z

'824

		OUTPUT			
ōc	CLR	CLKEN	CLK	D	Q
L	L	X	Х	X	L
L	Н	L	†	Н	L
L	Н	L	†	L	н
L	н	Н	X	X	Q_0
Н	Χ	Х	X	Χ	Z





KS54HCTLS **823/824** KS74HCTLS

9-Bit Bus Interface Flip-Flops with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5 to +7V
DC Input Diode Current, I _{IK}
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IoK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	•	-
Supply Voltage, Vo	oc	4.5V to 5.5V
		V _{OUT} 0V to V _{CC}
Operating Tempera	ature	
Range	KS74HCTLS:	-40°C to +85°C
	KS54HCTLS:	-55°C to +125°C
Input Rise & Fall T	imes, t _r , t _f	Max 500 ns
Unused inputs mu	ust always be tied	to an appropriate logic

voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
					Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6mA$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} -0.1 3.7	v
Maximum Low-Level Output Voltage	V _{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin $V_{I}=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA



9-Bit Bus Interface Flip-Flops with 3-State Outputs

AC ELECTRICAL CHARACTERISTICS (Input tr., tr<6 ns), HCTLS823, HCTLS824

Cha	racteristic	Symbol	nbol Conditions†		T _A = :		KS74HCTLS T _A = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _A = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
					Тур		Guarantee	d Limits	1
Maximum Op	erating Frequency	fmex	C _L =50pl	F	40	35	30	25	MHz
Maximum Pr	opagation Delay.	t _{PLH}	C _L =50pl C _L =150		15 18	20 23	25 30	30 36	ns
CLK to any		t _{PHL}	C _L =50pF C _L =150pF		15 18	20 23	25 30	30 36	113
Maximum Pr CLR to Any	opagation Delay, Q	tеин	C _L =50p C _L =150		17 20	22 25	28 33	34 40	ns
Maximum O	utout Enable	tpzL		C _L =50pF C _L =150pF	18 21	24 27	30 35	36 42	ns
	Time, OC to any Q			C _L =50pF C _L =150pF	18 21	24 27	30 35	36 42	
Maximum O	utput Disable	tpHZ	$R_L = 1 k\Omega$		18	24	30	36	ns
Time, OC to	any Q	tpLZ	C _L =50pF		18	24	30	36	""
Minimum Pulse Width	CLR Low CLK high or Low	t _w			12	16 16	20 20	24	ns
Minimum	CLR Inactive		-		12	16	20	24	
Setup Time	Data	tsu			12	16	20	24	ns
Before CLK	CLKEN high or Low				12	16	20	24	
Minimum Hold Time, CLKEN or data after CLK†		tn			0	0	0	0	ns
Maximum Input Capacitance		CiN			5				рF
Maximum Output Capacitance		Cout	Output D	isabled	10				рF
Power Dissip Capacitance	pation * (per stage)	C _{PD}	OC=V _{CC} OC=GN		5 30				pF

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}

[†] For AC switching test circuits and timing waveforms see section 2.

FEATURES

- Functionally Equivalent to AMD's Am29825 and Am29826
- Improved I_{OH} Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- . Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS

	'825		
0C1 CC2 CC2 CC2 CC2 CC2 CC2 CC2 CC2 CC2 C	1 2 3 4 5 6 7 8 9 10	24 D 23 D 22 D 21 D 20 D 19 D 18 D 17 D 16 D 15 D 14 D	V _{cc} OC3 1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q CLKEN CLK
GND L	<u> </u>	برد	OL.

	OL.		
		_	1
ōc₁ ぱ		24	□ ∨ _{cc}
ōc₂ ¤		23	DOCЗ
10 🗖	3	22	10
2D 🗖			2 Q
зō 🗖		20	3 0
_		19	4 0
5Ď 🗖	7	18	5 0
6∄ ₫	8	17	1 60
7Ď 🗖	9	16	1 70
8D 🗆	10.	15	D 8Q
CLR C	11	14	CLKEN
GND 🗖	12	13	CLK
			-

'826

DESCRIPTION

These 8-bit bus interface flip-flops leature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing multiuser buffer registers, I/O ports, bidirectional bus drivers and working registers.

With the clock enable ($\overline{\text{CLKEN}}$) low, all D-type edgetriggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high will disable the clock buffer, thus latching the outputs. The '825 has non-inverting D inputs and the '826 has inverting $\overline{\text{D}}$ inputs. Taking the $\overline{\text{CLR}}$ inputs low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

'825

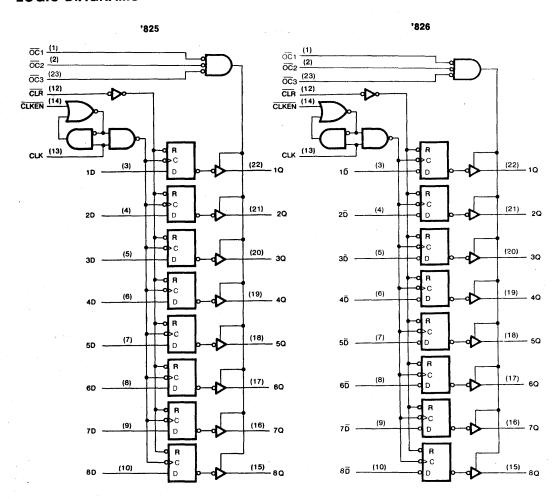
	Inputs					
<u>oc</u> .	CLR	CLKEN	CLK	D	Q	
L	L	X	X	Х	L	
L	H	L	. 1	Н	Н	
L	Н	L	1	L	L	
L	Н	н	Х	X	Qo	
H	X	X	Х	Х	Z	

^{*} OC=H if any of OC1, OC2, or OC3 are high. OC=L of OC1, OC2, and OC3 are low.

'826

	Inputs					
ÖC⁺	CLR	CLKEN	CLK	D	Q	
L	L	Х	Х	X	L	
L	Н	L	†	Н	L	
L	Н	L	†	L	Н	
L	Н	. н	X	X	Qo	
Н	X	X	X	×	Z	

^{*} OC = H if any of OC1, OC2, or OC3 are high. OC = L of OC1, OC2, and OC3 are low.



KS54HCTLS **825/826** KS74HCTLS

8-Bit Bus Interface Flip-Flops with 3-State Outputs

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, P_d^{\dagger} 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V	cc	4.5V to 5.5V
DC Input & Output	t Voltages*, V _{IN} ,	Vout 0V to Vcc
Operating Temper	ature	
Range	KS74HCTLS:	-40°C to +85°C
	KS54HCTLS: -	-55°C to +125°C
Input Rise & Fall	Γimes, t _r , t _f	Max 500 ns
•	ust always be tied t	o an appropriate logic

Characteristic	Symbol	Test Conditions	Т	a = 25°C	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{iH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} =0.1 3.84	V _{CC} -0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr., tres 6 ns), HCTLS825, HCTLS826

Characteristic		Symbol	Conditions [†]		T _a = 2		KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit	
							Guarantee	Limits		
Maximum Op	erating Frequency	f _{max}	C _L =50p	F	40	35	30	25	MHz	
Maximum Pr	opagation Delay,	t _{PLH}	C _L =50pl C _L =150		15 18	20 23	25 30	30 36	ns	
CLK to any		t _{PHL}	C _L =50pl C _L =150		15 18	20 23	25 30	30 36	113	
Maximum Pr CLR to Any	opagation Delay, Q	t _{PLH}	C _L =50pl C _L =150		17 20	22 25	28 33	34 40	ns	
Maximum O	utput Enable	t _{PZL}	R _i = 1kΩ	C _L =50pF C _L =150pF	18 21	24 27	30 35	36 42	ns	
	Time, OC to any Q		111_11	C _L =50pF C _L =150pF	18 21	24 27	30 35	36 42	113	
Maximum O	utput Disable	t _{PHZ}			18	24	30	36	ns	
Time, OC to	any Q	t _{PLZ}			18	24	30	36	113	
Minimum Pulse Width	CLR Low CLK high or Low	tw			12 12	16 16	20 20	24	ns	
Minimum	CLR Inactive	ļ			12	16	20	24	_	
Setup Time		t _{su}			12	16	20	24	ns	
Before CLK1	CLKEN high or Low				12	16	20	24		
Minimum Ho CLKEN or d	ld Time, ata after CLK†	t _h			0	0	0	0	ns	
Maximum In	put Capacitance	CIN			5				рF	
Maximum O	utput Capacitance	C _{OUT}			10				pF	
Power Dissip Capacitance	pation * (per stage)	C _{PD}			5 30				pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}² f_{in}.

[†] For AC switching test circuits and timing waveforms see section 2.

KS54HCTLS **841/842** KS74HCTLS

10-Bit Bus Interface D-Type Latches with 3-State Outputs

FEATURES

- Bus-Structured Pinout
- · Provides Extra Bus Driving Latches
- Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- . Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- ($I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS

		841			
ōc c	1	~	24	Ь	V _{cc}
1D 🖸	2		23	þ	1Q
2D 🕻	3		22	þ	2Q
3D	14		21	Ь	3Q '
4D 🕻	5		20	Ь	4Q
5D 🕻	6		19	Ь	5Q
6D 🕻	7		18	Ь	6Q
7D 🕻	8		17	Ь	7Q
8D [9		16	Ь	8Q
9D [10		15	ь	9Q
10D E	11		14	Ь	10Q
GND [12		13	þ	E

'842								
oc c	<u></u> ~	24	Ь	V _{cc}				
1Ō 🗀		23	Ь	1Q				
2D 🕻	3	22	Þ	2Q				
3Ď Œ	4	21	þ	ЗQ				
4Ō 🖸		20	Þ	4Q				
5Ď 🕻	6	19	Þ	5Q				
6D C		18	Þ	6Q				
7D 🗀		17	Þ	70				
8D C		16	Ь	8Q				
9D 🔼	10	15	Þ	9Q				
10D 🗀	11	14	Þ	10Q				
GND C	12	13	Þ	Ε				

DESCRIPTION

These 10-bit bus interface latches feature three state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers. I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type. The '841 has noninverting data (D) inputs and the '842 has inverting (\overline{D}) inputs.

A buffered output control (\overline{OC}) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

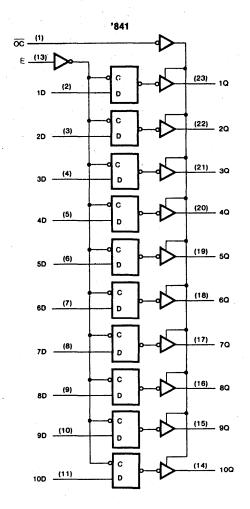
FUNCTION TABLES

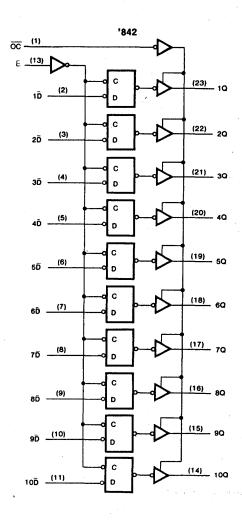
'841

IN	PUT	OUTPUT	
ōċ	E	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q_0
Н	Χ	X	Z

'842

	INPUT	OUTPUT	
OC	E	D	Q
L	н	Н	L
L	Н	L	Н
L	L	Χ	Q_0
Н	Χ	Χ	Z





10-Bit Bus Interface D-Type Latches with 3-State Outputs

Absolute Maximum Ratings*

•
Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage	V _{CC} 4.5V to 5.5V
DC Input & Ou	put Voltages*, V _{IN} , V _{OUT} 0V to V _{CC}
Operating Tem	perature
Range	KS74HCTLS: -40°C to +85°C
-	KS54HCTLS: ~55°C to +125°C

Input Rise & Fall Times, t_r , t_t Max 500 ns Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	bol Test Conditions		_a = 25°C	KS74HCTLS T _a = -40°C to +85°C	KS54HCTLS T _a = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	1 [
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-6m A$	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} =0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	In	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	Icc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS841, HCTLS842

Characteristic	Symbol	Conditions†		_	25°C 5.0V		KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
				Тур		Guarantee	d Limits	
Maximum Propagation Delay,	t _{PLH}	C _L = 50 C _L =150		15 18	20 23	25 30	30 36	ns
Data to Q	t _{PHL}	C _L =50pl C _L =150		15 18	20 23	25 30	30 36	.,0
Maximum Propagation Delay,		C _L =50pl C _L =150		21 24	28 31	35 40	42 48	-
E to any Q	tpHL	C _L =50pl C _L =150	21 24	28 31	35 40	42 48	ns	
Maximum Output Enable	t _{PZH}	Rı = 1kΩ	C _L =50pF C _L =150pF	18 21	24 27	30 35	36 42	ns
Time, OC to any Q	t _{PZL}	11,2	C _L =50pF C _L =150pF	18 21	24 27	30 35	36 42	110
Maximum Output Disable Time, OC to any Q	t _{PHZ}	R _L =1kΩ C _L =50pl	=	18 18	24	30 30	36 36	ns
Minimum Pulse Width, E High	t _w		-1	15	20	25	30	ns
Minimum Setup Time, Data before E↓	t _{su}			12	16	20	24	ns
Minimum Hold Time, Data after E↓	th			6	8	10	12	ns
Maximum Input Capacitance	CIN			5				pF
Maximum Output Capacitance	Cout	,		10				pF
Power Dissipation Capacitance* (per stage)	C _{PD}	ŌC=V _{CC} ŌC=GNI		5 30				рF

 $^{^{\}star}$ C_{PD} determines the no-load dynamic power dissipation: $P_{D}\!=\!C_{PD}\;V_{CC}{}^{z}\;f_{in\cdot}$

 $[\]uparrow$ For AC switching test circuits and timing waveforms see section 2.

- Bus-Structured Pinout
- Provide Extra Bus Driving Latches
 Necessary for Wider Address/Data Paths or Buses
 with Parity
- · Power-Up High Impedance
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- · 3-State outputs with high drive current
- (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS





DESCRIPTION

These 9-bit bus interface latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

The nine latches are transparent D-type. The '843 has noninverting data (D) inputs and the '844 has inverting \overline{D} inputs.

A buffered output control (\overline{OC}) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control (\overline{OC}) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

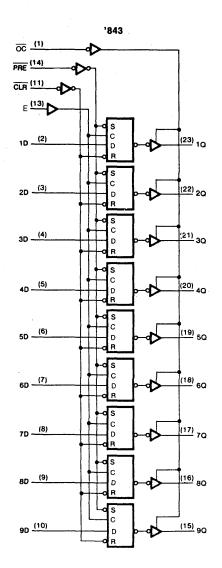
'843

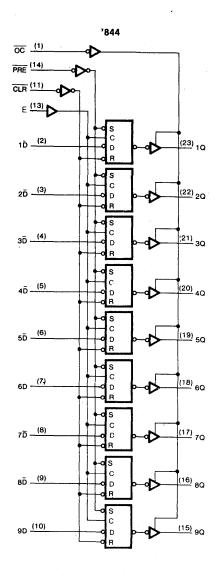
	INF		OUTPUT		
PRE	CLR	ŌC	Е	D	Q
L	X	L	Χ	X	н
Н	L	L	Х	Χ	L
Н	Н	L	H	L	L
Н	Н	L	Н	Н	Н
Н	н	L	L	Χ	Q_0
Х	Х	Н	X	Χ	z

'844

	INF		OUTPUT		
PRE	CLR	<u>oc</u>	E	D	Q
L	X	L	Х	X	Н
Н	L	L	Χ	Χ	L
H,	Н	L	Н	L	Н
H	Н	L	Н	H	L
н	Н	L	L	Х	Qo
Х	Х	Н	X	X	Z







KS54HCTLS **843/844** KS74HCTLS

9-Bit Bus Interface D-Type Latches with 3-State Outputs

Absolute Maximum Ratings*

_
Supply Voltage Range V _{CC} ,
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V _{CC} or GND pins ±250 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Necommen	ded Operating Conditions
Supply Voltage, \	V _{CC} 4.5V to 5.5V
DC Input & Outpo	ut Voltages*, V _{IN} , V _{OUT} OV to V _{CC}
Operating Tempe	rature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall	Times, t_r , t_f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T _a = -55°C to +125°C	Unit
	Typ Guaranteed Limits				its		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	V _{CC} 4.2	V _{CC} −0.1 3.98	V _{CC} -0.1 3.84	V _{CC} −0.1 3.7	٧
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =OμA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin V ₁ =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA



9-Bit Bus Interface D-Type Latches with 3-State Outputs

AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS843, HCTLS844

Characteristic	Symbol	nbol Conditions†			25°C : 5.0V	KS74HCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
			Тур		Guarantee	d Limits		
Maximum Propagation Delay.	tpLH	C _L = 50 C _L =150		18 21	24 27	30 35	36 42	ns
to	t _{PHL}	C _L =50pl C _L =150		18 21	24 27	30 35	36 42	113
Maximum Propagation Delay,	tpLH	C _L =50pl C _L =150		21 24	28 31	35 40	42 48	ns
E to any Q	t _{PHL}	C _L =50pl C _L =150		21 24	28 31	35 40	42 48	113
Maximum Propagation Delay, PRE to Q	tpLH	C _L =50pl C _L =150	23 26	30 33	38 43	46 52	ns	
Maximum Propagation Delay, CLR to Q	t _{PHL}		C _L =50pF C _L =150pF		30 33	38 43	46 52	ns
Maximum Output Enable	tpzH	$R_i = 1 k\Omega$	C _L =50pF C _L =150pF	18 21	24 27	30 35	36 42	ns
Time, OC to any Q	t _{PZL}	1112	C _L =50pF C _L =150pF	18 21	24 27	30 35	36 42	113
Maximum Output Disable	t _{PHZ}	$R_L = 1 k\Omega$		18	24	30	36	ns
Time, OC to any Q	tPLZ	C _L =50pl	-	18	24	30	36	
Minimum Pulse Width, E High	tw			15	20	25	30	ns
Minimum Setup Time, Data after E↓	tsu			12	16	20	24	ns
Minimum Hold Time, Data before E↓	t _h			6	8	10	12	ns
Maximum Input Capacitance	CIN			5				рF
Maximum Output Capacitance	Cout			10				pF
Power Dissipation Capacitance (per stage)	C _{PD}	OC=V _{CC} OC=GNI		5 30				pF

 $^{^{\}star}$ C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC} 2 f_{in-}

[†] For AC switching test circuits and timing waveforms see section 2.

FEATURE

- · 3-state buffer-type outputs drive bus-lines directly
- · Bus-structured pinout
- Provides extra bus driving latches necessary for wider address/data paths or buses with parity
- Low power consumption characteristic of CMOS devices
- 3-state outputs with high drive current ($I_{OL} = 24mA$ @ $V_{OL} = 0.5V$) for direct bus interface
- Direct interface capability with TTL, NMOS and CMOS devices
- Wide operating volage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 **Total Control of the Co

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to 125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATIONS

	'845			
OC1	<u></u>	24	Ь	Vcc
OC2 C	2	23	Б	ō€3
1D 🗀	3	22	þ	1Q
2D 🕻	4	21	þ	2Q
3D 🗀	5	20	þ	3Q
4D [19	Þ	4Q
5D C	7	18	þ	5Q
6D C	8	17	Þ	6Q
7D 🗀	9	16	Þ	7Q
8D C		- 15	þ	80
CLR C		14	Þ	PRE
GND [12	13	р	Ε

		040			
ō€1 d	1	√	24	Ь	Voc
<u>ō</u> c₂ □	2		23	Б	ос з
10 □	3		22	Þ	1Q
2D 🕻	4		21	Ь	2Q
3Ō Ⴀ	5		20	Ь	3Q
4D □	6		19	Ь	4Q
50 ₫	7		18	Ь	5Q
6 D ☐	8		17	Ь	6Q
7₫ 🗖	9		16	Ь	7Q
	10		15	Ь	8Q
CLR [11		14	Ь	PRE
GND [12		13	Ь	Е

,016

DESCRIPTION

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type. The '845 has noninverting data(D) inputs. The '846 has inverting D inputs. Since $\overline{\text{CLR}}$ and $\overline{\text{PRE}}$ are independent of the clock, taking the $\overline{\text{CLR}}$ input low will cause the eight Q outputs to go low. Taking the $\overline{\text{PRE}}$ input low will cause the eight Q outputs to go high. When both $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are taken low, the outputs will follow the preset condition.

The buffered output control inputs ($\overline{OC1}$, $\overline{OC2}$, and $\overline{OC3}$) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impendance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

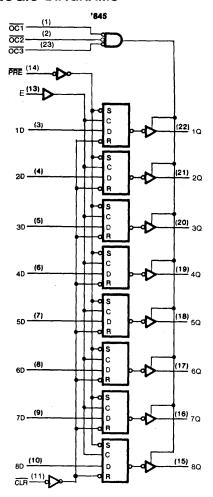
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

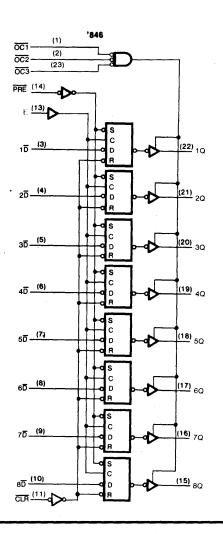


FUNCTION TABLE

		IN	PUTS				OUTPUT
PRE	CLR	OC1	OC2	OC3	E	Đ	Q
L	Н	L	L	L	Χ	Χ	Н
) н	L	L	L	L	Х	Х	L
L	Ł	L	L	L	Х	Х	н
] н	Н	L	L	L	Н	L	L
H	Н	L	L	L	Н	H	н
H	Н	L	L	L	L	X	Qo
X	Х	Х	Х	Н	Х	X	Q₀ Z
X	Х	Х	Н	Х	X	Х	Z
X	Х	н	X	X	Χ	X	Z

	'846									
				OUTPUT						
PRE	CLR	OC1	OC2	OC3	E	ā	Q			
L	Н	L	L	Ł	X	Χ	Н			
н	L	L	L	Ł	Χ	Х	L			
L	L	L	L	L	Χ	Х	н			
н	Н	L	L	Ł	Н	L	Н			
Н.	н	L.	L	L	Н	Н	L			
н	н	L	L	L	Ł	Х	Q ₀			
×	X	Х	Х	Н	Х	Х	Z			
x	X	Х	H	Х	Х	Х	Z			
Х	X	н	Х	Х	Х	Х	Z			





Absolute Maximum Ratings*

[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

Recommended Operating Conditions

	. •
Supply Voltage, \	/cc 4.5V to 5.5V
DC Input & Output	ıt Voltages*, V _{IN} , V _{OUT} . ∴ 0V to V _{CC}
Operating Tempe	rature
Range	KS74HCLTS: -40°C to +85°C
	KS54HCLTS: -55°C to +125°C
Input Rise & Fall	Times, tr, tr Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	= 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{1H}			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VıL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	o	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	-:00	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2,9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤6 ns), HCTLS845

Characteristic	1 1		, -	25°C :5.0V	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10^{\circ}\text{M}$	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit	
			Тур		Guarante	ed Limits		
Propagation Delay	tpLH		23	30	38	46	ns	
E to Q	t _{PHL}		23	30	38	46	115	
Propagation Delay	tpLH		18	24	30	36	ns	
D̄ to Q	t _{PHL}		18	24	30	.36	115	
Propagation Delay CLR to Q	t _{PLH}		27	36	45	54		
	t _{PHL}		27	36	45	54	ns	
Propagation Delay	tpLH		27	36	45	54	ns	
PRE to Q	tpHL		27	36	45	54		
Output Enable Time	t _{PZH}		23	30	38	46		
OC to Q	t _{PZL}		23	30	38	46	ns	
Output Disable Time	t _{PHZ}		16	21	26	• 31		
OC to Q	t _{PLZ}	 	16	21	26	31	ns	
Set up Time Dn before E	tsu		12	16	20	24	ns	
Hold Time Dn after E	th		0	0	0	0	ns	
Input Capacitance	C _{IN}		5				рF	
Power Dissipation Capacitance*	C _{PD}						pF	

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \; V_{CC^2} \; f_{in}$.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS846

Characteristic	Symbol	Conditions [†]	T _a = 25°C V _{CC} = 5.0V		KS74HCTLS $T_a = -40 ^{\circ}\text{C to } + 85 ^{\circ}\text{C}$ $V_{CC} = 5.0 \text{V} \pm 10 ^{\%}$	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit			
			Тур		Guarante	eed Limits				
Propagation Delay	t _{PLH}		25	34	42	65	ns			
E to Q	t _{PHL}		25	34	42	65	'''			
Propagation Delay	t _{PLH}		20	27	34	40	ns			
□ to Q	t _{PHL}		20	27	34	40	""			
Propagation Delay	tplH		26	35	44	53	ns			
	tPHL		26	35	44	53				
Propagation Delay PRE to Q	tpLH		26	35	44	52	ns			
	t _{PHL}		26	35	44	52				
Output Enable Time	tpzH		19	26	32	38	ns			
	tpZL		19	26	32	38	'''			
Output Disable Time	t _{PHZ}		14	19	24	30	ns			
	t _{PLZ}	ĺ	14	19	24	30	113			
Set up Time Dn before E	tsu		12	16	20	24	ns			
Hold Time Dn after E	t _h		0	0	0	0	ns			
Input Capacitance	- C _{IN}		5				рF			
Power Dissipation Capacitance*	C _{PD}						рF			

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.



FEATURES

- . Modified input structure allows voltages up to 15V
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs:
- IoL = 8mA @ VoL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

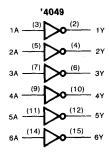
The '4049 and '4050 have a modified input protection structure that enable them to be used as logic level translators which will convert high level logic to a low level logic while operating from the low logic supply. For example, 0-15V logic can be corverted to 0-5V logic when using a 5V supply. The modified input protection has no diode connected to $V_{\rm cc}$, thus allowing the input voltage to exceed the supply. The lower zener diode protects the input from both positive and negative static voltages. In addition the '4049 and '4050 can be used as simple buffers or inverters without level translation.

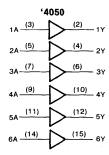
PIN CONFIGURATION



FUNCTION TABLE

INPUT	OUTPUT Y				
A	'4049	'4050			
Н	L	Н			
L	н	L			





KS54HCTLS 4049/4050 KS74HCTLS

Hex Logic Level Down Converters

Absolute Maximum Ratings*

Supply Voltage Range V _{CC} ,0.5V to +7V
DC Input Diode Current, I _{IK}
$(V_1 < -0.5V \text{ or } V_1 > +15.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
. Vcc or GND pins ±125 mA
Storage Temperature Range, T _{stg} 65°C to +150°C
Power Dissipation Per Package, Pd [†] 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

Recommended Operating Conditions

	. •
	oc 4.5V to 5.5V
DC Input & Output	Voltages*, VIN, VOUT OV to VCC
Operating Tempera	ature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall T	imes, t _r , t _f Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		25°C KS74HCTLS KS54HCTL $T_a = -40$ °C to +85°C $T_a = -55$ °C to +		Unit
	1		Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VıL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V _{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=-20\mu A$ $I_{O}=-4m A$	V _{CC}	V _{CC} -0.1 3.98	V _{CC} −0.1 3.84	V _{CC} −0.1	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or V_{IL} $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	l _{IN}	V _{IN} =V _{CC} or GND V _{IN} =15V		±0.1	±1.0 ±10.0	±1.0 ±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V _{IN} =V _{CC} or GND I _{OUT} =0µA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0µA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS4049, HCTLS4050

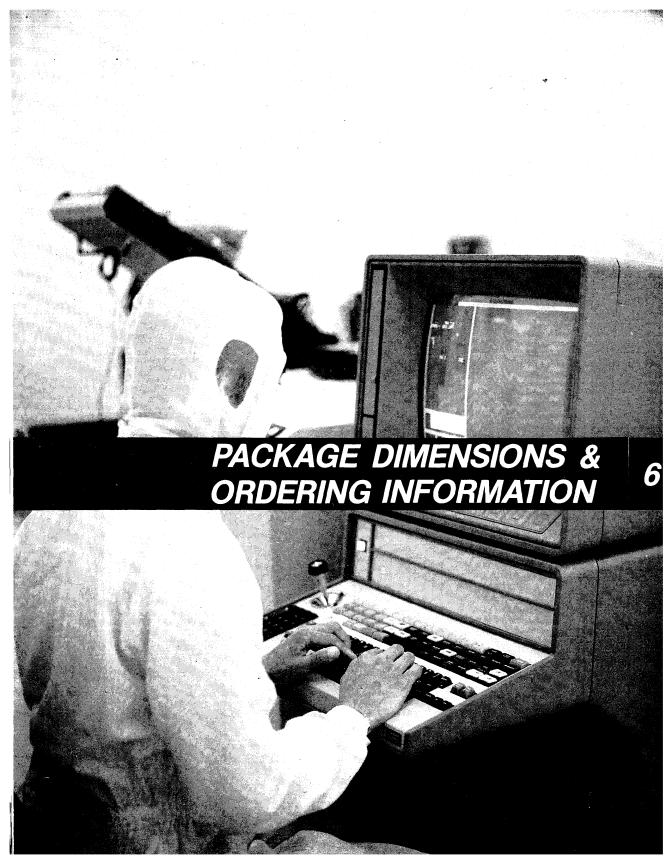
Characteristic	Symbol	$T_a = 25$ Conditions [†] $V_{CC} = 5$			KS74AHCTLS T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%	KS54HCTLS T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%	Unit
		}	Тур		Guaranteed	l Limits	1
Maximum Propagation Delay	t _{PLH}	Cı =50pF	13	17	21	26	ns
	t _{PHL}	OL-CODI	13	17	21	26	113
Maximum Input Capacitance	CIN		5				рF°
Power Dissipation Capacitance*	C _{PD}	(per gate)					pF

^{*} C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} \ V_{CC}^2 \ f_{in}$.

[†] For AC switching test circuits and timing waveforms see section 2.



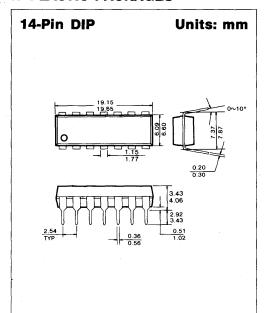
[†] Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C

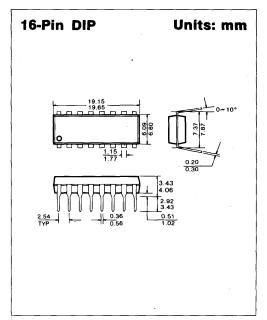


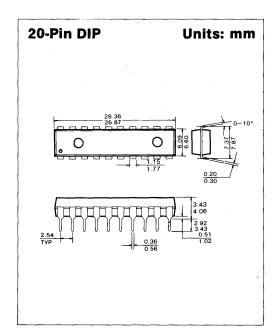


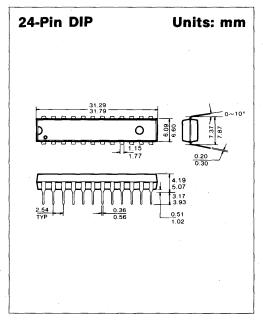
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1. PLASTIC PACKAGES

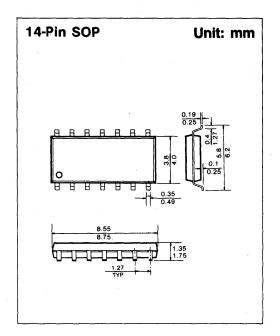


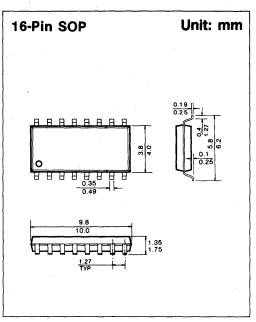


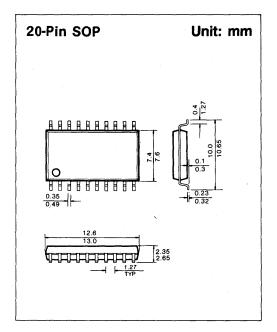


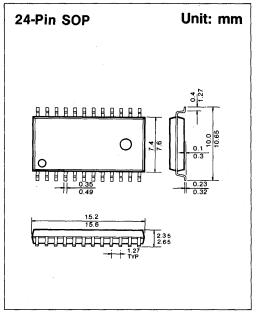


PACKAGE DIMENSIONS



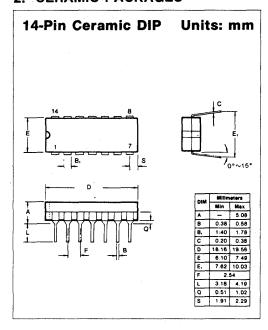


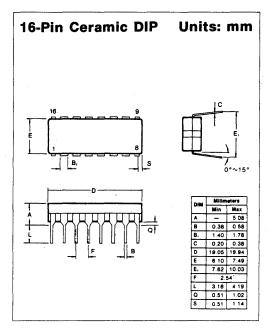


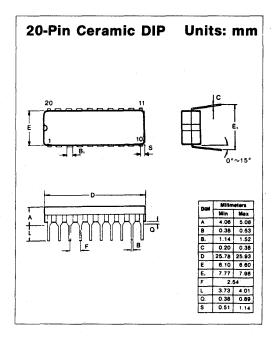


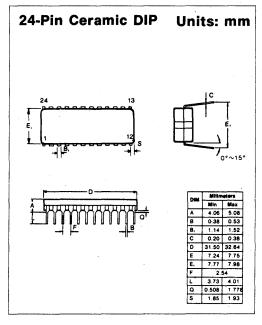
PACKAGE DIMENSIONS

2. CERAMIC PACKAGES



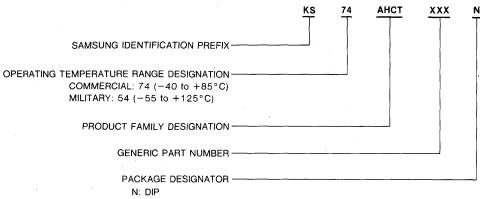






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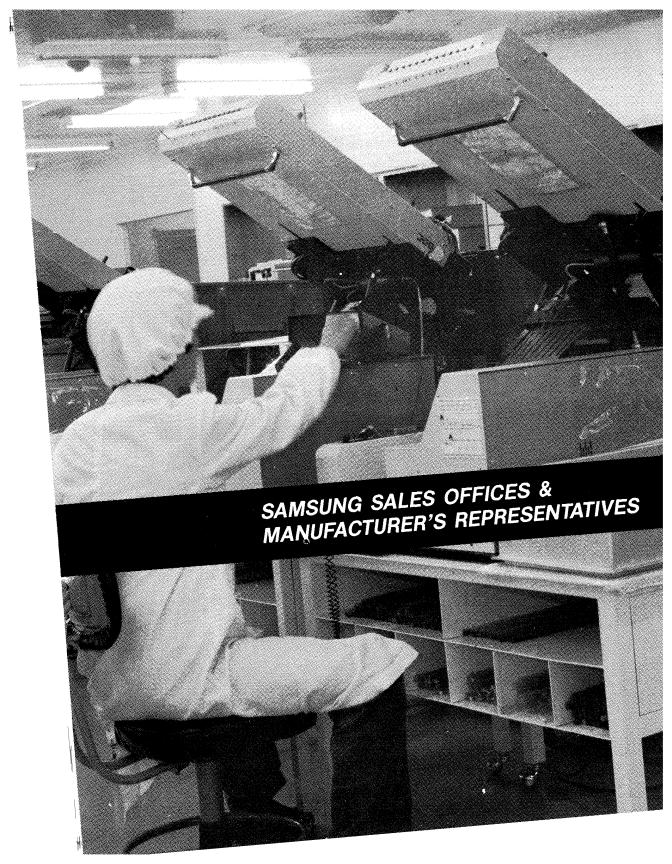
The ensure prompt and accurate processing of your order, please use the product code system as described in the following example.

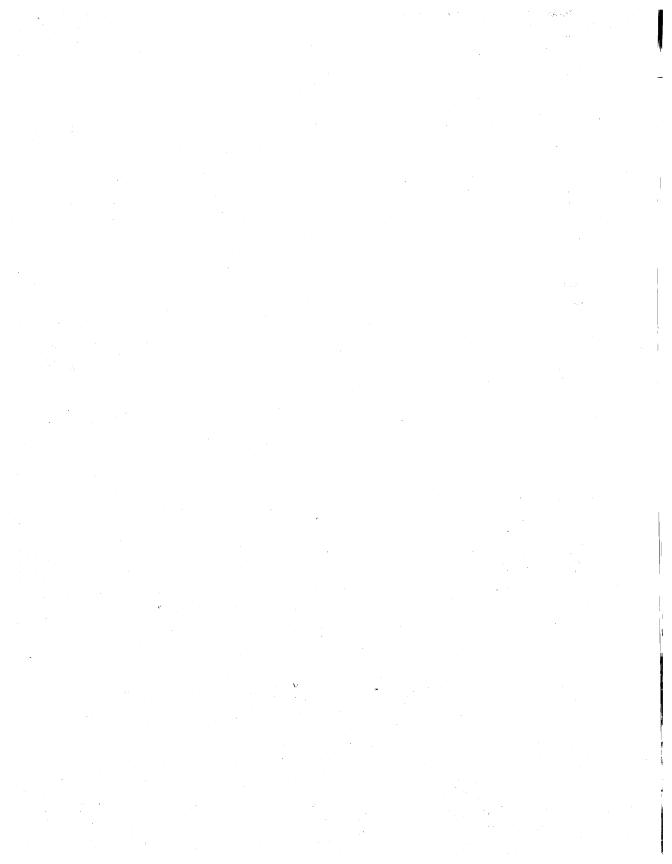


D: SOP

DT: SOP(Tape & Reel)

Pin	Quantity/Reel	
SO-14	3000	
SO-16	3000	
SO-20	1000	
SO-24	1000	





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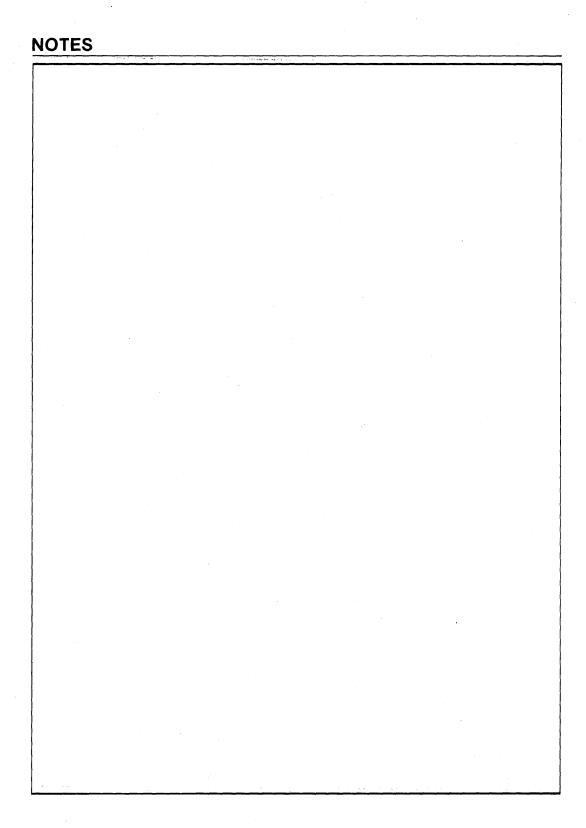
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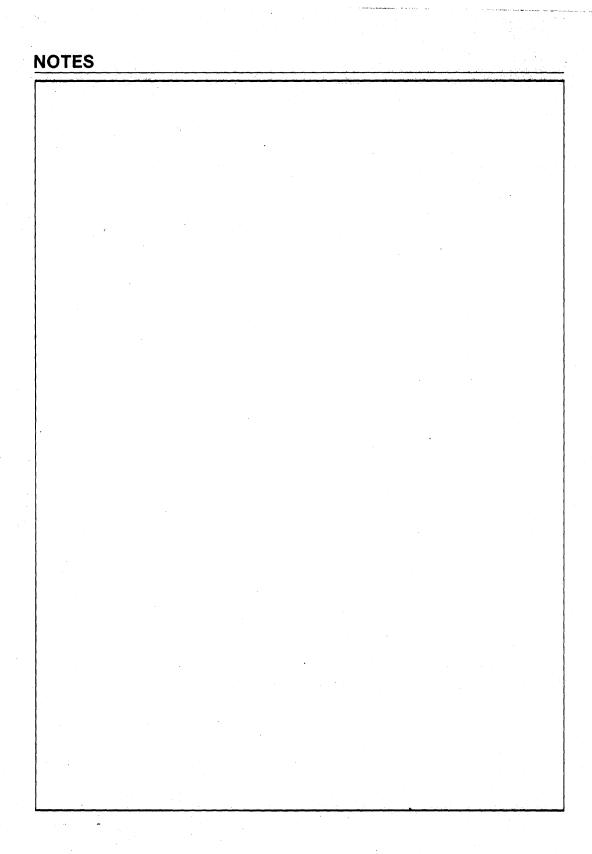
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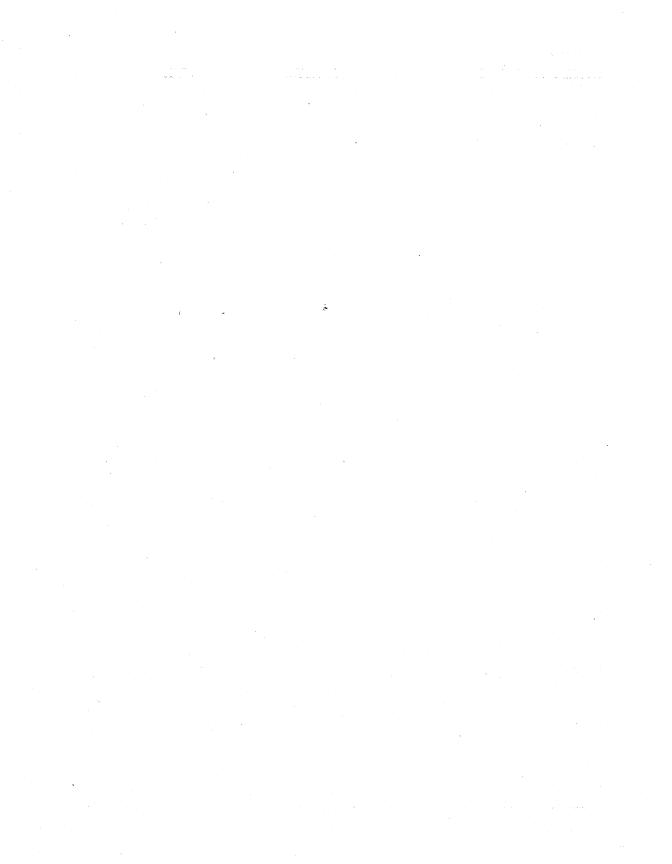
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