SAMSUNG

DRAM DATA BOOK

1996

LORI STEINTHAL

I² INCORPORATED

MANUFACTURERS REPRESENTATIVES

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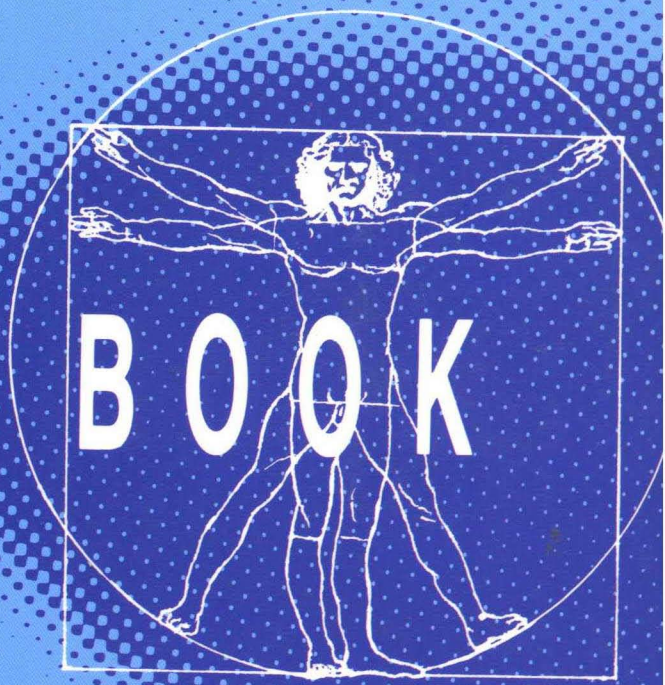
1110-5121
Dec. 1995



1996 DATA BOOK

DRAM

SAMSUNG

PRINTED IN KOREA

Certified ISO 9001

Certificate No FM 24651

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* The D-version is under development and will take the place of B-version from March 1996.

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* The B-version is under development and will take the place of A-version from May 1996.

64M DRAM

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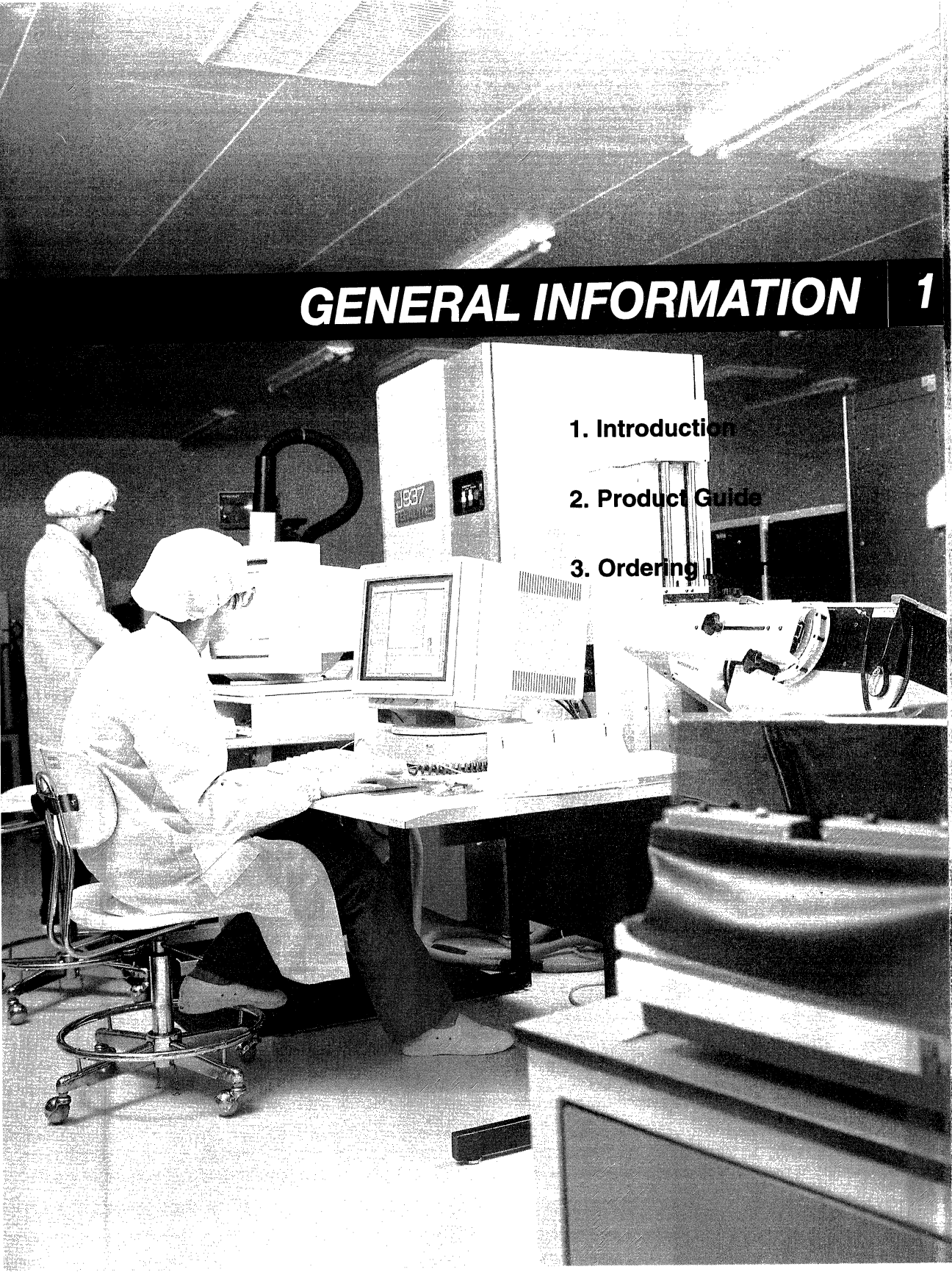
III. Timing Chart

Changed Point in '96 DRAM Databook
(Compared with '95 databook)

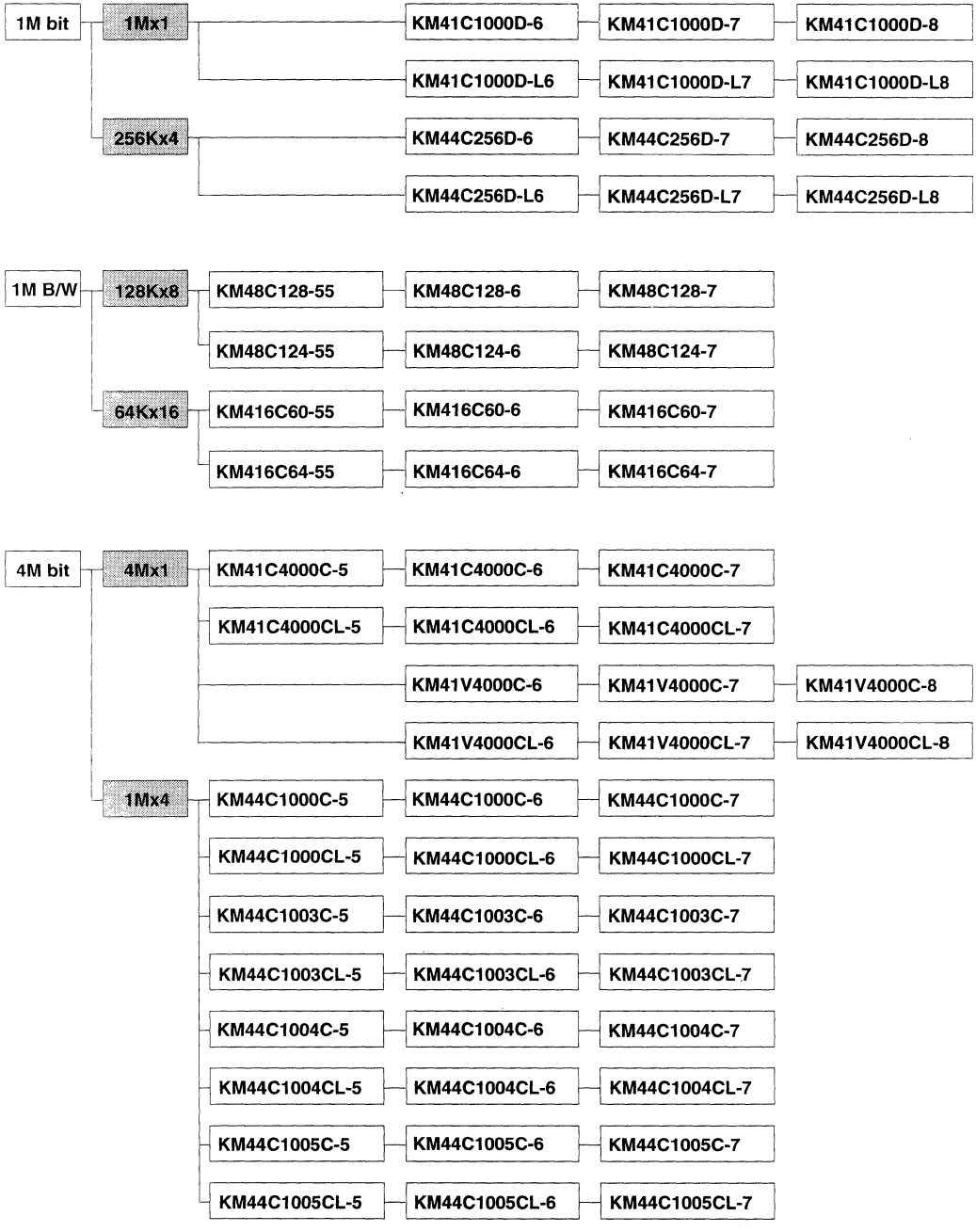
	Changed Point in '96 DRAM databook			Remarks
General	- Remove TSOP II(reverse) package - Remove 80ns version in 5V product - Remove SC Mode, WPB Mode product - Remove 512Kx9 and 256Kx18 product			
Generation Change	**Device**	**in '95**	**in '96**	
	- 128Kx8, 64Kx16	- None	- 1st gen.	- Add EDO Quad $\overline{CAS}$ product
	- 4Mx1, 1Mx4	- C-version	- C-Version	- Remove x9 & x18 product
	- 512Kx8, 256Kx16	- B-version	- D-Version	- Add EDO Quad $\overline{CAS}$ product
	- 16Mx1, 4Mx4, 2Mx8	- A-version	- B-Version	- B-ver. will be available from 3Q '96
	- 1Mx16	- A-version	- A-Version & B-version	- Add 5V 64M DRAM : x4(4K) and x8(K)
	- 16Mx4, 8Mx8	-1st gen.	- A-version (2nd gen.)	
	- 4Mx16	- None	- A-version	
1M	- Add 128Kx8(FP/EDO), 64Kx16(2$\overline{WE}$, FP/EDO)			
4M C-ver	- Add EDO Quad $\overline{CAS}$ product - Remove DIP and ZIP package - Remove SC, WPB Mode product			
4M B/W	- Remove 512Kx9 and 256Kx18 product			
16M (x1,x4,x8)	- Remove SC Mode WPB Mode product - Add EDO Quad $\overline{CAS}$ product - Change the CMOS Standby current(ICC5) of Normal-power version from 1mA to 0.5mA			- Changed package size from 400mil to 300mil
16M (1Mx16)	- 50ns version will be available in B-version(3rd gen.) from May 1996. - Change the CMOS Standby current(ICC5) of Normal-power version from 1mA to 0.5mA			
64M (x4,x8,x16)	- Add 4Mx16 product - Add 5V product - Change the Refresh cycle of Low -power version from 256ms to128ms			

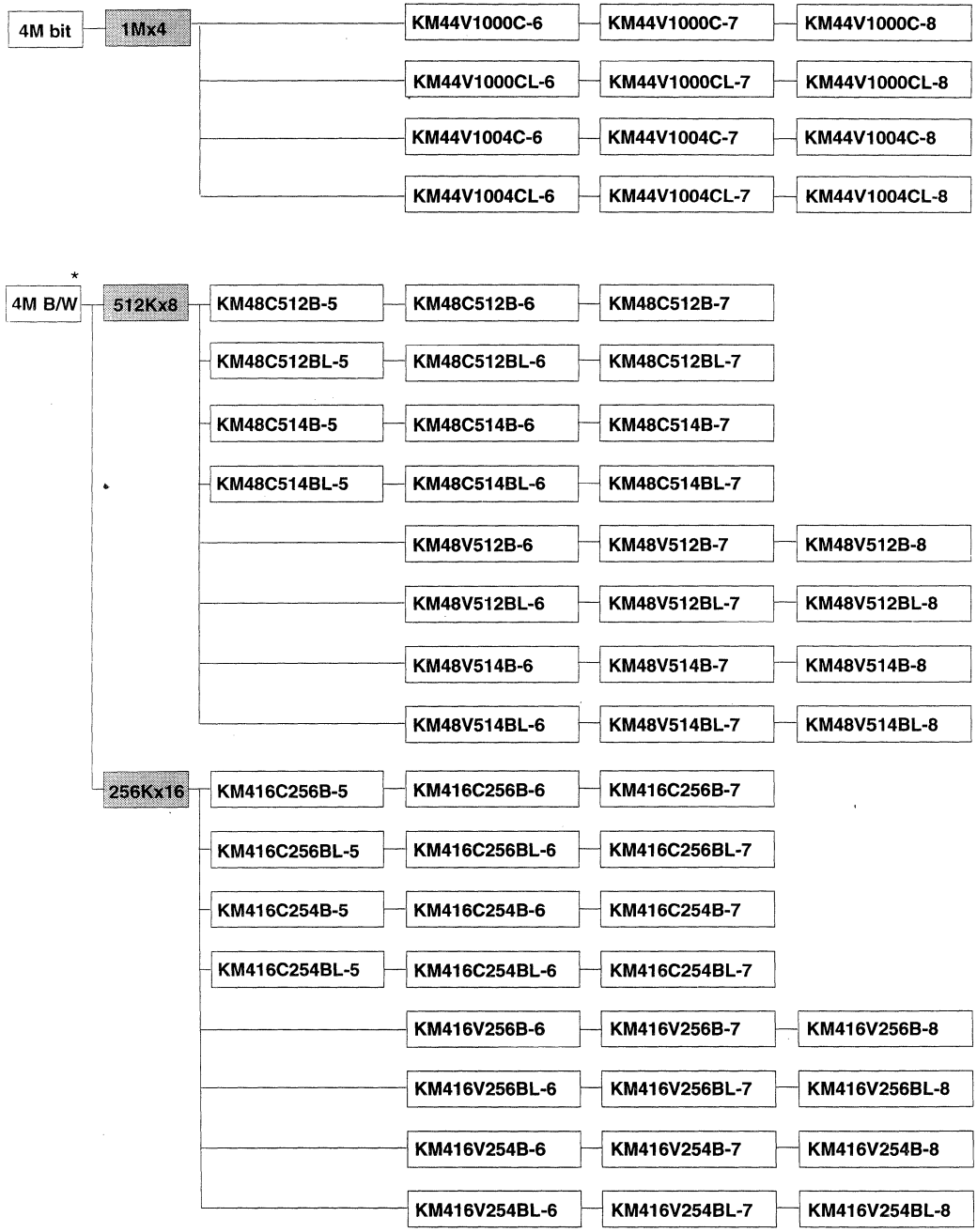
In "Remove ~ ", " ~ " means that "~" is not supported anymore.
In "Add ~ ", "~" means that "~" is new product and is available from '96.

GENERAL INFORMATION 1

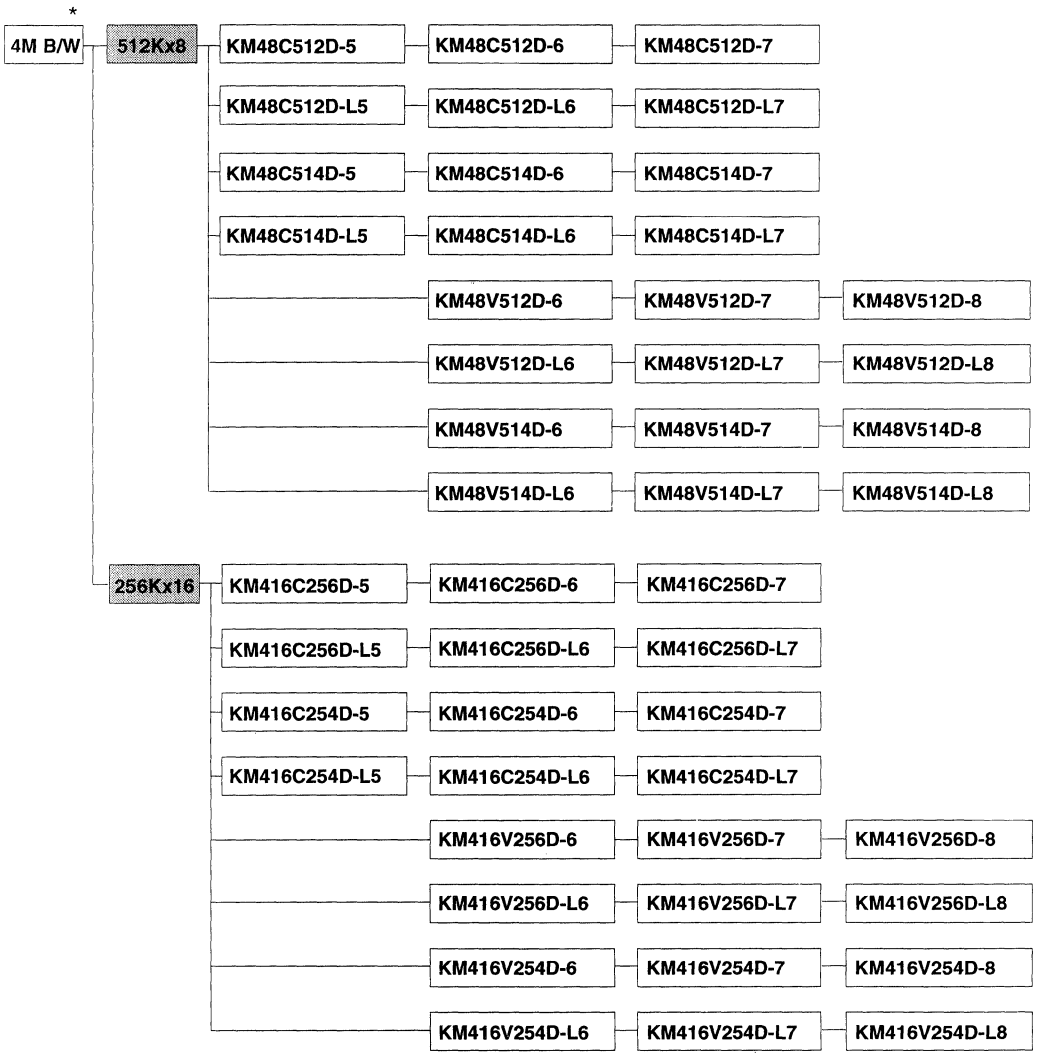


1. Introduction

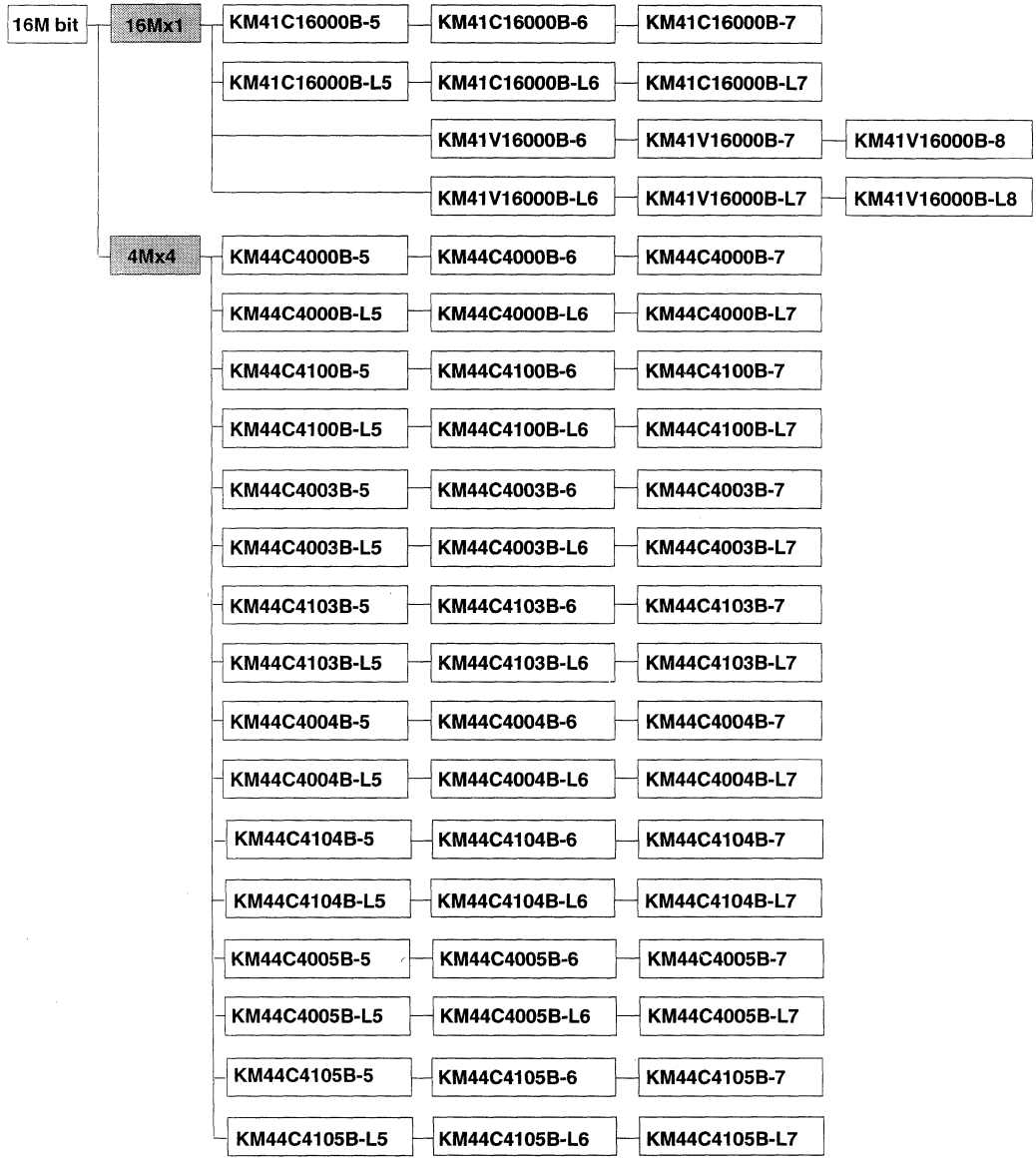




* The next version(D-version) is under development and will take a place of B-version from March 1996. Please refer to the next page about D-version.



* D-version is under development and will take a place of B-version from March 1996.
Please refer to the previous page about B-version.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4Mx4
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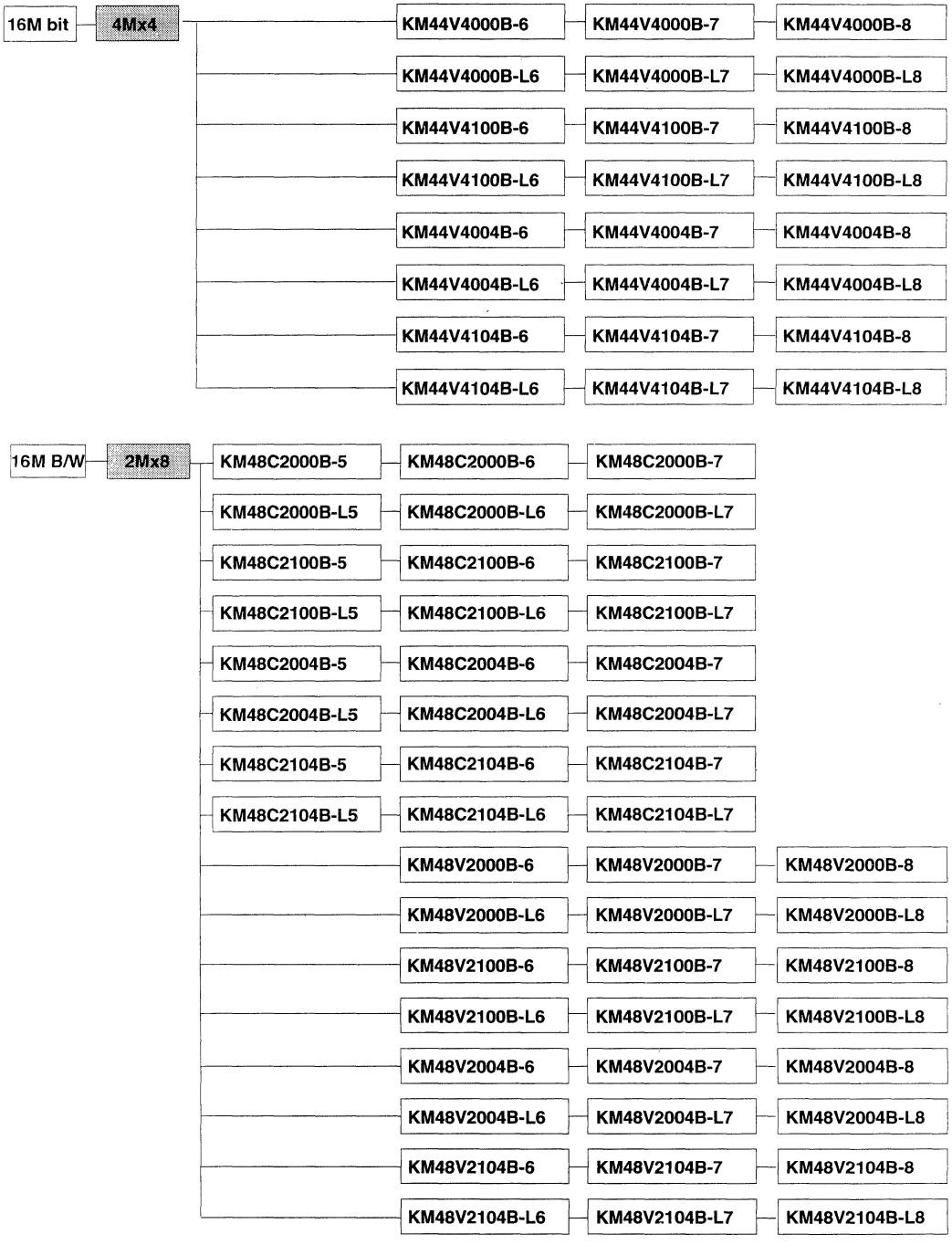
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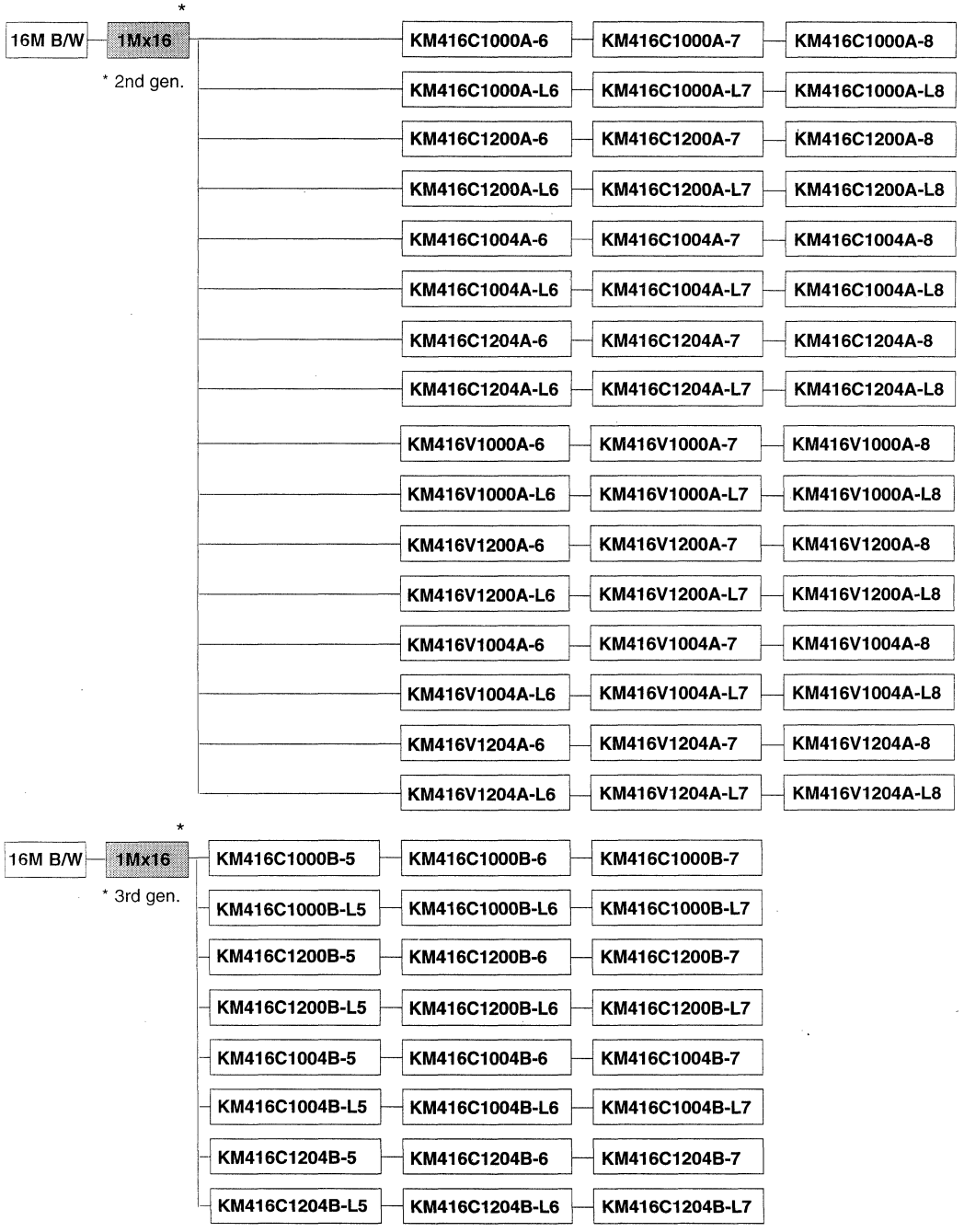
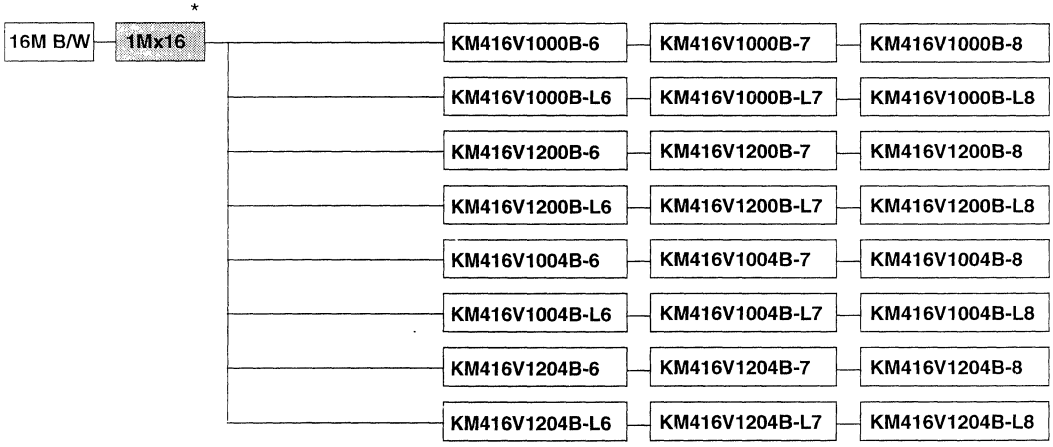
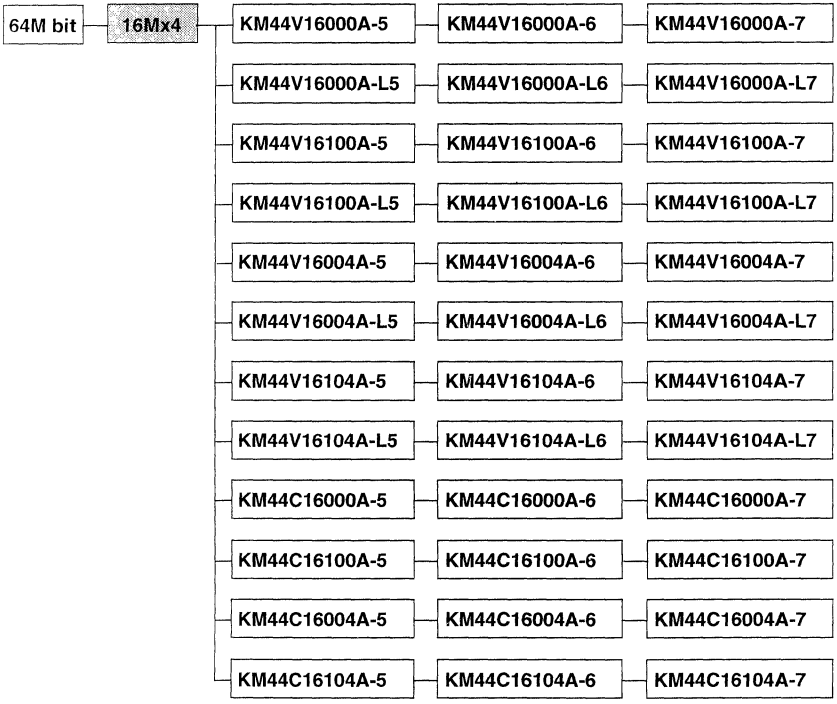
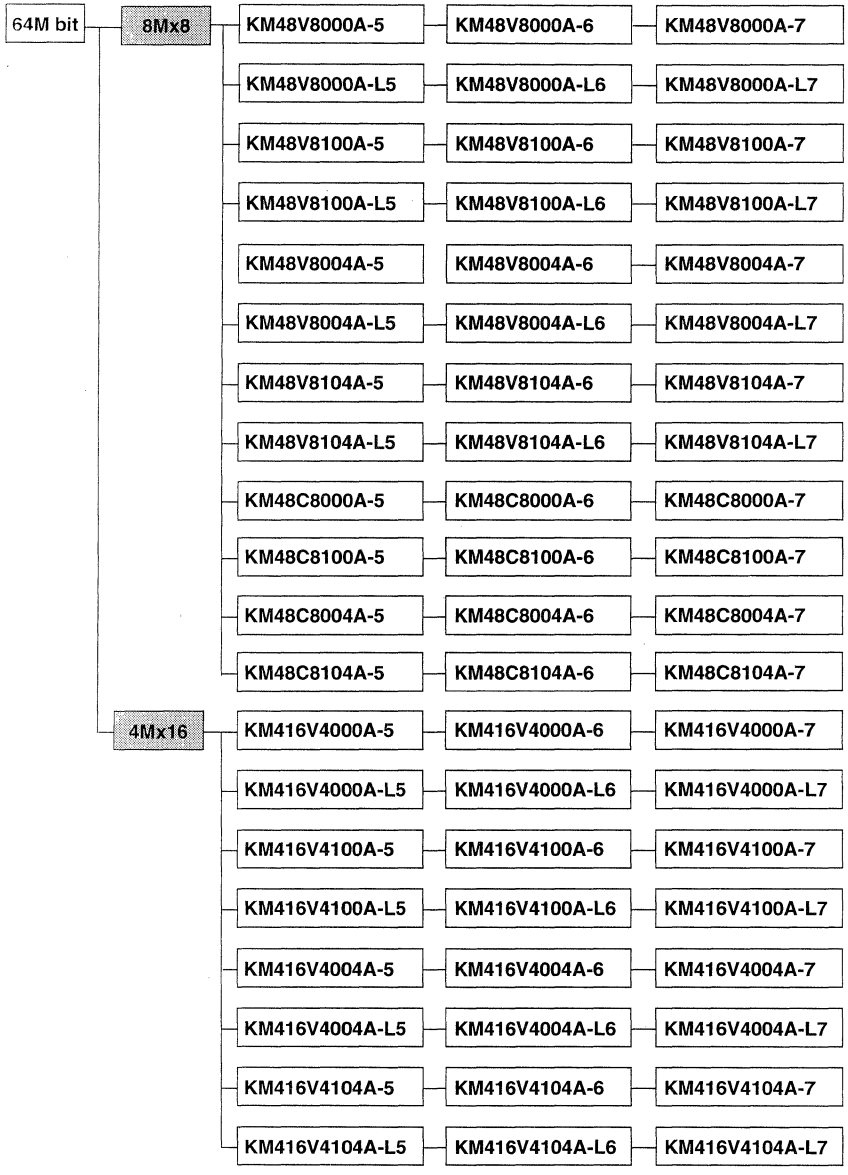


* The 3rd gen.(B version) of 1Mx16 is under development and will take a place of A-version from 3Q 1996.



* B version is under development and will be available from 3Q 1996.

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2. Product Guide

Density	Org.	Power Supply	Part Number	Speed (ns)	Features	Packages (#)
1M bit	1Mx1	5V±10%	KM41C1000D# KM41C1000D-L#	60/70/80	Fast Page	P:18 Pin DIP (1Mx1) 20 Pin DIP (256Kx4)
	256Kx4	5V±10%	KM44C256D# KM44C256D-L#	60/70/80	Fast Page	J:20 Pin SOJ Z:20 Pin ZIP
	128Kx8	5V±10%	KM48C128# KM48C128#-L KM48C124# KM48C124#-L	55/60/70	Fast Page EDO	J:24 Pin SOJ
	64Kx16	5V±10%	KM416C60# KM416C60#-L KM416C64# KM416C64#-L	55/60/70	Fast Page EDO	J:40 Pin SOJ T:40 Pin TSOP
4M bit	4Mx1	5V±10%	KM41C4000C# KM41C4000CL#	50/60/70	Fast Page	P:20 Pin DIP J:20 Pin SOJ
		3.3V±0.3V	KM41V4000C# KM41V4000CL#	60/70/80	Fast Page	T:20 Pin TSOP-II (Forward)
	1Mx4	5V±10%	KM44C1000C# KM44C1000CL# KM44C1003C# KM44C1003CL# KM44C1004C# KM44C1004CL# KM44C1005C#	50/60/70	Fast Page Quad CAS FP EDO Quad CAS EDO	*Quad CAS J:24 Pin SOJ T:24 Pin TSOP-II (Forward)
		3.3V±0.3V	KM44V1000C# KM44V1000CL# KM44V1004C# KM44V1004CL#	60/70/80	Fast Page EDO	
4M B/W	512Kx8	5V±10%	KM48C512B# KM48C512BL# KM48C514B# KM48C514BL#	50/60/70	Fast Page EDO	J:28 Pin SOJ T:28 Pin TSOP-II(Forward)
		3.3V±0.3V	KM48V512B# KM48V512BL# KM48V514B# KM48V514BL#	60/70/80	Fast Page EDO	

Density	Org.	Power Supply	Part Number	Speed (ns)	Features	Packages (#)
4M B/W	256Kx16	5V±10%	KM416C256B#	50/60/70	Fast Page	J:40 Pin SOJ
			KM416C256BL#			T:40 Pin TSOP-II(Forward)
			KM416C254B#		EDO	
			KM416C254BL#			
		3.3V±0.3V	KM416V256B#	60/70/80	Fast Page	
			KM416V256BL#			
			KM416V254B#		EDO	
			KM416V254BL#			
16M bit	16Mx1	5V±10%	KM41C16000B#	50/60/70	Fast Page(4K)	K:24 Pin SOJ (300mil)
			KM41C16000B#-L			S:24 Pin TSOP-II(Forward)
		3.3V±0.3V	KM41V16000B#	60/70/80		(300mil)
			KM41V16000B#-L			
	4Mx4	5V±10%	KM44C4000B#	50/60/70	Fast Page(4K)	
			KM44C4000B#-L			
			KM44C4100B#		Fast Page(2K)	
			KM44C4100B#-L			
			KM44C4003B#		Quad CAS FP(4K)	*Quad CAS
			KM44C4003B#-L			K:28 Pin SOJ [300mil]
			KM44C4103B#		Quad CAS FP(2K)	S:28 Pin TSOP-II(Forward)
			KM44C4103B#-L			[300mil]
			KM44C4004B#		EDO(4K)	
			KM44C4004B#-L			
			KM44C4104B#		EDO(2K)	
			KM44C4104B#-L			
			KM44C4005B#		Quad CAS EDO(4K)	
			KM44C4105B#		Quad CAS EDO(2K)	
		3.3V±0.3V	KM44V4000B#	60/70/80	Fast Page(4K)	
			KM44V4000B#--L			
			KM44V4100B#		Fast Page(2K)	
			KM44V4100B#-L			
			KM44V4004B#		EDO(4K)	
			KM44V4004B#-L			

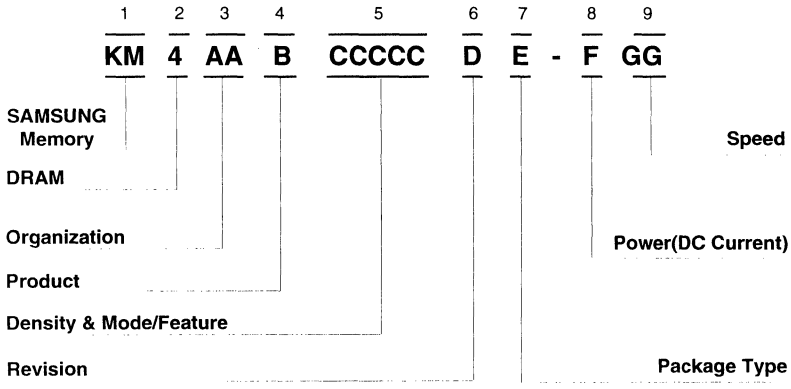
Density	Org.	Power Supply	Part Number	Speed (ns)	Features	Packages (#)
16M bit	4Mx4	3.3V±0.3V	KM44V4104B#	60/70/80	EDO(2K)	K:24 Pin SOJ(300mil)
			KM44V4104BL#			S:24 Pin TSOP-II(300mil)
16M B/W	2Mx8	5V±10%	KM48C2000B#	50/60/70	Fast Page(4K)	K:28 Pin SOJ [300mil]
			KM48C2000B-L#			S:28 Pin TSOP-II[Forword]
			KM48C2100B#		Fast Page(2K)	[300mil]
			KM48C2100B#-L			
			KM48C2004B#		EDO(4K)	
			KM48C2004B#-L			
			KM48C2104B#		EDO(2K)	
			KM48C2104B#-L			
		3.3V±0.3V	KM48V2000B#	60/70/80	Fast Page(4K)	
			KM48V2000B#-L			
			KM48V2100B#		Fast Page(2K)	
			KM48V2100B#-L			
			KM48V2004B#		EDO(4K)	
			KM48V2004B#-L			
			KM48V2104B#		EDO(2K)	
			KM48V2104B#--L			
	1Mx16 *	5V±10%	KM416C1000A#	60/70/80 *	Fast Page(4K)	J:42 Pin SOJ [400mil]
			KM416C1000A#-L	(50/60/70		T:44 Pin TSOP-II (Forward)
			KM416C1200A#	in B ver.)	Fast Page(1K)	[400mil]
			KM416C1200A#-L			
			KM416C1004A#		EDO(4K)	
			KM416C1004A#-L			
			KM416C1204A#		EDO(1K)	
			KM416C1204A#-L			
		3.3V±0.3V	KM416V1000A#	60/70/80	Fast Page(4K)	
			KM416V1000A#-L			
			KM416V1200A#		Fast Page(1K)	
			KM416V1200A#-L			
			KM416V1004A#		EDO(4K)	
			KM416V1004A#-L			
			KM416V1204A#		EDO(1K)	
			KM416V1204A#-L			

* The 3rd gen.(B version) of 1Mx16 is under development and will take a place of this version(A version) from 3Q 1996.

Density	Org.	Power Supply	Part Number	Speed (ns)	Features	Packages (#)
64M bit	16Mx4	5V±10%	KM44C16000A#	50/60/70	Fast Page(8K)	K : 32 Pin SOJ [400mil]
			KM44C16100A#		Fast Page(4K)	S : 32 pin TSOP II(Forward)
			KM44C16004A#		EDO(8K)	[400mil]
			KM44C16104A#		EDO(4K)	
		3.3V±0.3V	KM44V16000A#	50/60/70	Fast Page(8K)	
			KM44V16000A#-L			
			KM44V16100A#		Fast Page(4K)	
			KM44V16100A#-L			
			KM44V16004A#		EDO(8K)	
			KM44V16004A#-L			
			KM44V16104A#		EDO(4K)	
			KM44V16104A#-L			
	8Mx8	5V±10%	KM48C8000A#	50/60/70	Fast Page(8K)	
			KM48C8100A#		Fast Page(4K)	
			KM48C8000A#		EDO(8K)	
			KM48C8100A#		EDO(4K)	
		3.3V±0.3V	KM48V8000A#	50/60/70	Fast Page(8K)	
			KM48V8000A#-L			
			KM48V8100A#		Fast Page(4K)	S : 50 pin TSOP II(Forward)
			KM48V8100A#-L			[400mil]
			KM48V8004A#		EDO(8K)	
			KM48V8004A#-L			
			KM48V8104A#		EDO(4K)	
			KM48V8104A#-L			
	4Mx16	3.3V±0.3V	KM416V4000A#	50/60/70	Fast Page(8K)	
			KM416V4000A#-L			
			KM416V4100A#		Fast Page(4K)	
			KM416V4100A#-L			
			KM416V4004A#		EDO(8K)	
			KM416V4004A#-L			
			KM416V4104A#		EDO(4K)	
			KM416V4104A#-L			

3. DRAM Ordering System

This DRAM ordering system is being used from 2H1995.



1. SAMSUNG Memory

2. DRAM(4)

3. Organization

1	x 1
4	x 4
8	x 8
16	x 16
32	x 32

4. Product

C	5V
V	3.3V

5. Density & Mode/Feature

Refer to "Chapter 2. Product Guide."

6. Revision

Blank	1st Gen.
A	2nd Gen.
B	3rd Gen.
C	4th Gen.
D	5th GEn.

7. Package Type

J	SOJ
T	TSOP II (Forward)
P	DIP
Z	ZIP
K	SOJ(Shrinked PKG,SOJ)
S	TSOP II (Shrinked PKG,Forward)

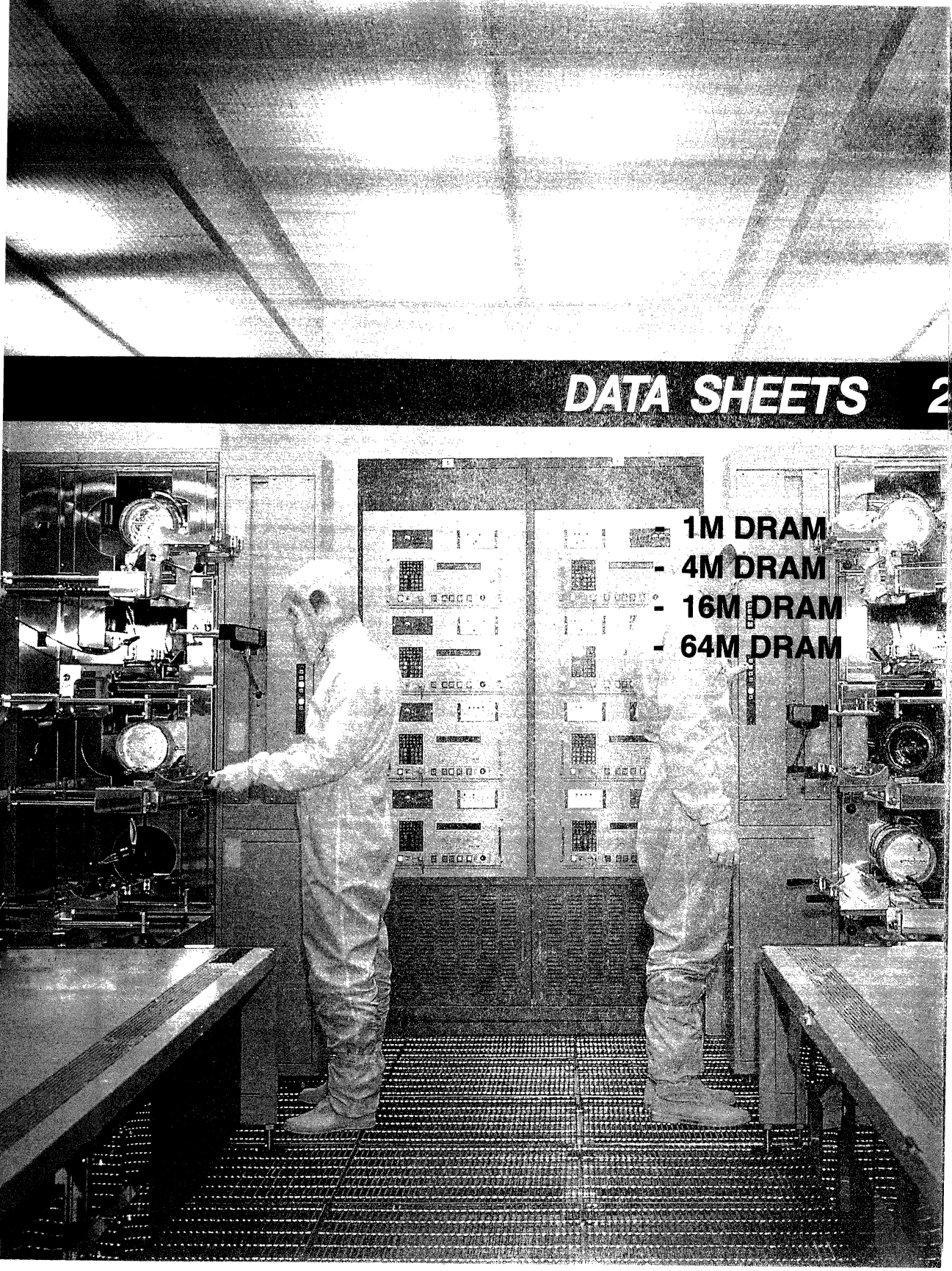
8. Power(DC Current)

Blank	Normal
L	Low power with Self refresh

9. Speed

- 5	50 ns
-55	55ns
- 6	60 ns
- 7	70 ns
- 8	80 ns

DATA SHEETS 2



- 1M DRAM
- 4M DRAM
- 16M DRAM
- 64M DRAM

1M DRAM

- KM41C1000D
- KM44C256D
- KM48C128
- KM48C124
- KM416C60
- KM416C64

1M x 1 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 1,048,576 x 1 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Access time(-6, -7 or -8), power consumption (Normal or Low power) , and package type (SOJ, ZIP,DIP) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities.
This 1Mx1 Fast Page Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM41C1000D/D-L(5V)
- Active Power Dissipation

Unit : mW

Speed	Active Power Dissipation
-6	385
-7	358
-8	330

- Refresh cycles

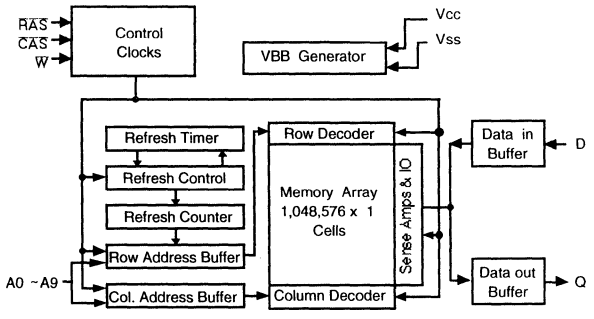
Part No.	Refresh Cycle	Refresh period	
		Normal	L
KM41C1000D	512	8ms	128ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns
-8	80ns	20ns	150ns	50ns

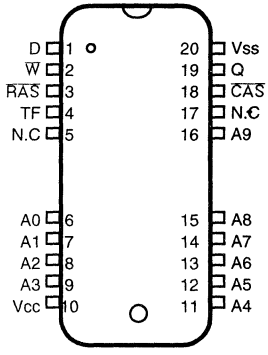
- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL(5V) compatible inputs and outputs
- 256K x 4 fast test mode
- JEDEC Standard pinout
- Available in Plastic SOJ, ZIP and DIP packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM

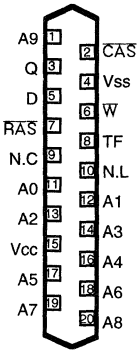


PIN CONFIGURATION (Top Views)

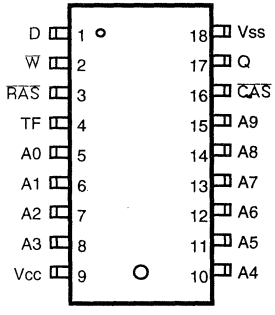
• **KM41C1000DJ**



• **KM41C1000DZ**



• **KM41C1000DP**



Pin Name	Pin Function
A0 - A9	Address Inputs
D	Data In
Q	Data Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power(+5.0V)
N.C	No Connection
TF	Test Function
NL	No Lead

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage temperature	Tstg	-55 to +150	°C
Power dissipation	P_D	600	mW
Short circuit output current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	Vcc+1*1	V
Input low voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤ 20ns (pulse width is measured at Vcc)

*2 : -2.0V at pulse width ≤ 20ns (pulse is measured at Vss)

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input leakage current (Any input 0≤V_{IN}≤Vcc+0.5V all other pins not under test=0 volts.)	$I_{I(L)}$	- 5	5	μA
Output leakage current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output high voltage level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output low voltage level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max	Units
			KM41C1000D	
I_{CC1}	Don't care	-6 -7 -8	60 55 50	mA mA mA
I_{CC2}	Don't care	Don't care	2	mA
I_{CC3}	Don't care	-6 -7 -8	60 55 50	mA mA mA
I_{CC4}	Don't care	-6 -7 -8	50 45 40	mA mA mA
I_{CC5}	Normal L	Don't care	1 100	mA μA
I_{CC6}	Don't care	-6 -7 -8	60 55 50	mA mA mA
I_{CC7}	L	Don't care	100	μA

I_{CC1}* : Operating current ($\overline{RAS}$ and $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V

D_{IN}=$\overline{W}$=A0 ~ A9 = V_{CC}-0.2V or 0.2V , T_{RC}= 125μs(L-ver), T_{RAS}=T_{RAS}min~300 ns

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [D]	C_{IN1}	-	5	pF
Input capacitance [A0 - A9]	C_{IN2}	-	6	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$]	C_{IN3}	-	7	pF
Output capacitance [Q]	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	130		150		170		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,9
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	50		55		60		ns	14
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	14
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	15		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	50		55		60		ns	14
Refresh period(Normal)	tREF		8		8		8	ms	
Refresh period(L -ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	15		20		20		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	60		70		80		ns	7
Column address to $\overline{W}$ delay time	tAWD	30		35		40		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	35		40		45		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	15		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		35		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	60		60		65		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	40		45		50		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD(max) is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min),the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. Normal operation requires the "TF" pin to be connected to Vss or TTL logic low level or left unconnected on the printed wiring board.
12. When the "TF" pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung for specific operational details of the "test function".
13. In a test mode cycle, the value of tRAC, tCAC, tAA is delayed for 3ns.
14. tAR, tWCR, and tDHR are referenced to $t_{RAD(MAX)}$.

256K x 4 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 262,144 x 4 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Access time(-6, -7 or -8), power consumption (Normal or Low power), and package type (SOJ, ZIP,DIP) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities.
This 256Kx4 Fast Page Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM44C256D/D-L(5V)

- Active Power Dissipation

Unit : mW

Speed	Active Power Dissipation
-6	385
-7	358
-8	330

- Refresh cycles

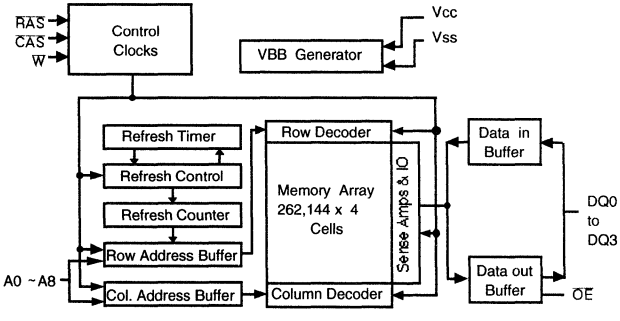
Part No.	Refresh Cycle	Refresh period	
		Normal	L
KM44C256D	512	8ms	128ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns
-8	80ns	20ns	150ns	50ns

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL(5V) compatible inputs and outputs
- Early write or Output Enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ, ZIP, and DIP packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



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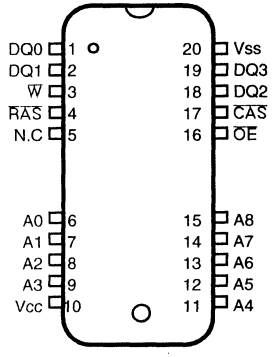
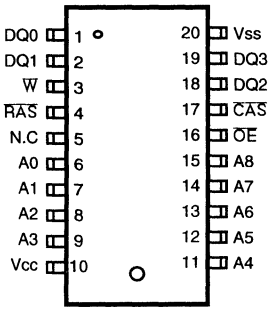
SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top Views)

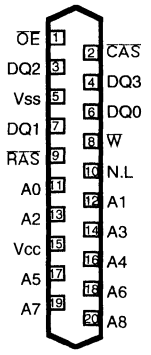
• KM44C256DJ



• KM44C256DP



• KM44C256DZ



Pin Name	Pin Function
A0 - A8	Address Inputs
DQ0~3	Data In/out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
V_{CC}	Power(+5.0V)
N.C	No Connection
NL	No Lead

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage temperature	Tstg	-55 to +150	°C
Power dissipation	P_D	600	mW
Short circuit output current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	V_{CC}+1[*1]	V
Input low voltage	V_{IL}	-2.0[*2]	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤ 20ns (pulse width is measured at Vcc)

*2 : -2.0V at pulse width ≤ 20ns (pulse is measured at Vss)

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input leakage current (Any input 0≤V_{IN}≤Vcc+0.5V all other pins not under test=0 volts.)	$I_{I(L)}$	- 5	5	μA
Output leakage current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output high voltage level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output low voltage level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max	Units
			KM44C256D	
I_{CC1}	Don't care	-6 -7 -8	60 55 50	mA mA mA
I_{CC2}	Don't care	Don't care	2	mA
I_{CC3}	Don't care	-6 -7 -8	60 55 50	mA mA mA
I_{CC4}	Don't care	-6 -7 -8	50 45 40	mA mA mA
I_{CC5}	Normal L	Don't care	1 100	mA μA
I_{CC6}	Don't care	-6 -7 -8	60 55 50	mA mA mA
I_{CC7}	L	Don't care	100	μA

I_{CC1}* : Operating current ($\overline{RAS}$ and $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V

D_{IN}=$\overline{W}$=A0 ~ A8= V_{CC}-0.2V or 0.2V , T_{RC}= 125μs(L-ver), T_{RAS}=T_{RAS}min~300 ns

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C, V_{CC}=5V , f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A8]	C_{IN1}	-	6	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$,$\overline{OE}$]	C_{IN2}	-	7	pF
Output capacitance [DQ0~DQ3]	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition : V_{CC}=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		175		195		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,9
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	50		55		60		ns	11
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	11
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	15		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	50		55		60		ns	11
Refresh period(Normal)	tREF		8		8		8	ms	
Refresh period(L -ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		45		45		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	15		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		35		40	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		85		90		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	40		45		50		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD(max) is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min),the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. tAR, tWCR, and tDHR are referenced to $t_{RAD(MAX)}$.

128K x 8 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 131,072 x 8 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Access time (55, 60, or 70) and power consumption (Normal or Low power) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in Low power version.

This 128Kx8 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for personal computer and portable machines.

FEATURES

- Part Identification
  - KM48C128/L

- Active power consumption

Unit : mW

Speed	Active power consumption
-55	413
-6	385
-7	360

- Refresh cycles

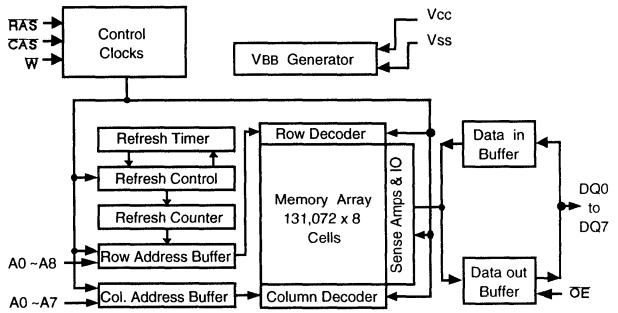
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
48C128	5V	512	8ms	64ms

- Performance range

Speed	tRAC	tCAC	tRC	tPC
-55	55ns	15ns	110ns	40ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns

- Fast Page Mode operation
- Byte Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- Available in plastic SOJ packages
- Single+5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



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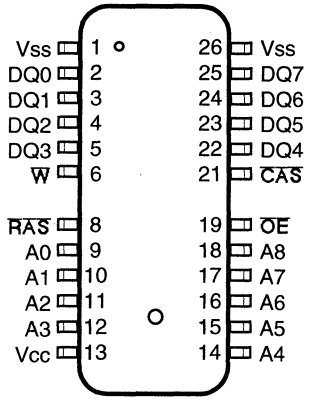
PIN CONFIGURATION (Top Views)

• KM48C128J



(SOJ)

Pin Name	Pin Function	Pin Name	Pin Function
A0 - A8	Address Inputs	$\overline{W}$	Read/Write Input
DQ0 -7	Data In/Out	$\overline{OE}$	Data Output Enable
Vss	Ground	Vcc	Power (+5V)
$\overline{RAS}$	Row Address Strobe		
$\overline{CAS}$	Column Address Strobe	N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1.0 *1	V
Input Low Voltage	V_{IL}	-1.0 *2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.

*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max	Units
I_{CC1}	Don't care	-55 -6 -7	65 65 55	mA mA mA
I_{CC2}	Don't care	Don't care	2	mA
I_{CC3}	Don't care	-55 -6 -7	65 65 55	mA mA mA
I_{CC4}	Don't care	-55 -6 -7	60 60 55	mA mA mA
I_{CC5}	Normal L	Don't care	1 150	mA μA
I_{CC6}	Don't care	-55 -6 -7	65 65 55	mA mA mA
I_{CC7}	L	Don't care	300	μA
I_{CCS}	L	Don't care	200	μA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH}, $\overline{W}$=Don't care)

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=Vcc-0.2V, $\overline{W}$=Don't care)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V

Din = Don't care, T_{RC}=125μs, T_{RAS}=T_{RAS} min~300 ns

I_{CCS} : Self refresh current

$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A8 = V_{CC}-0.2V or 0.2V,

DQ0 ~ DQ7= V_{CC}-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE (T_A=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 ~ A8]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0~ DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V

Parameter	Symbol	- 55		- 6		- 7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		110		130		ns	
Read-modify-write cycle time	tRWC	155		155		185		ns	
Access time from $\overline{RAS}$	tRAC		55		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		15		20	ns	3,4,5
Access time from column address	tAA		30		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		15		20		ns	
$\overline{CAS}$ hold time	tCSH	60		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		10		10		ns	
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Parameter	Symbol	-55		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	10		10		15		ns	9
Refresh period (Normal)	tREF		8		8		8	ms	
Refresh period (L-ver)	tREF		64		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		40		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		85		95		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		55		60		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		60		65		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		35		40	ns	3
Fast Page mode cycle time	tPC	40		40		45		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		80		95		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	60	100K	60	100K	70	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		35		40		ns	
$\overline{OE}$ access time	tOEA		15		15		20	ns	
$\overline{OE}$ to data delay	tOED	15		15		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	20	ns	6
$\overline{OE}$ command hold time	tOEH	15		15		20		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		µs	11
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		110		130		ns	11
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	11

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 50pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. For all of the refresh mode except the distributed $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 512 cycles of burst refresh must be executed within 4ms before and after self refresh, in order to meet refresh specification.(L-version).

128K x 8 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 131,072x 8 bit Extended Data Out CMOS DRAMs. Extended Data Out offers high speed random access of memory cells within the same row. Access time (55, 60, or 70) and power consumption (Normal or Low power) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in Low power version.

This 128Kx8 Extended Data Out DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for personal computer and portable machines.

FEATURES

- Part Identification
  - KM48C124/L

- Active power consumption

Unit : mW

Speed	Active power consumption
-55	413
-6	385
-7	358

- Refresh cycles

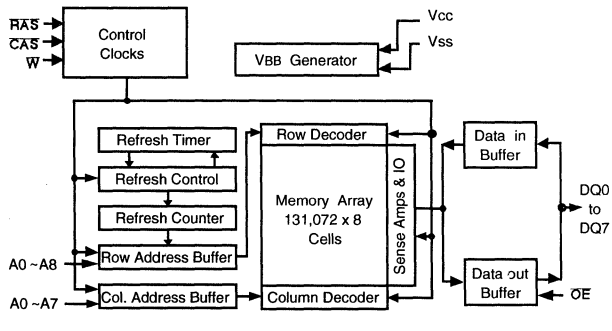
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
48C124	5V	512	8ms	64ms

- Performance range

Speed	tRAC	tCAC	tRC	tHPC
-55	55ns	17ns	104ns	25ns
-6	60ns	17ns	104ns	25ns
-7	70ns	20ns	124ns	30ns

- Extended Data Out operation
- Byte Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- Available in plastic SOJ packages
- Single +5V±10% power supply

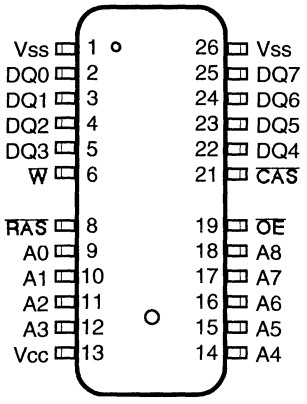
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top Views)

• KM48C124J



(SOJ)

Pin Name	Pin Function	Pin Name	Pin Function
A0 - A8	Address Inputs	$\overline{W}$	Read/Write Input
DQ0 -7	Data In/Out	$\overline{OE}$	Data Output Enable
Vss	Ground	Vcc	Power (+5V)
$\overline{RAS}$	Row Address Strobe		
$\overline{CAS}$	Column Address Strobe	N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to Vss	V_{CC}	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1.0 *1	V
Input Low Voltage	V_{IL}	-1.0 *2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.

*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \le V_{IN} \le Vcc+0.5V$, (Any input $0 \le V_{IN} \le Vcc+0.5V$, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	-5	5	μA
Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max	Units
I_{CC1}	Don't care	-55 -6 -7	65 65 55	mA mA mA
I_{CC2}	Don't care	Don't care	2	mA
I_{CC3}	Don't care	-55 -6 -7	65 65 55	mA mA mA
I_{CC4}	Don't care	-55 -6 -7	85 85 75	mA mA mA
I_{CC5}	Normal L	Don't care	1 150	mA µA
I_{CC6}	Don't care	-55 -6 -7	65 65 55	mA mA mA
I_{CC7}	L	Don't care	300	µA
I_{CCS}	L	Don't care	200	µA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH}, $\overline{W}$=Don't care)

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=Vcc-0.2V, $\overline{W}$=Don't care)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V

Din = Don't care, T_{RC}=125µs, T_{RAS}=T_{RAS} min~300 ns

I_{CCS} : Self refresh current

$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A8 = V_{CC}-0.2V or 0.2V,

DQ0 ~ DQ7 = V_{CC}-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle time, tHPC

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 ~ A8]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 ~ DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition : V_{CC}=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-55		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	104		104		124		ns	
Read-modify-write cycle time	tRWC	135		140		165		ns	
Access time from $\overline{RAS}$	tRAC		55		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		17		17		20	ns	3,4,5
Access time from column address	tAA		30		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	15	3	15	3	15	ns	6, 13
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	17		17		20		ns	
$\overline{CAS}$ hold time	tCSH	50		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	10	10K	10	10K	15	10K	ns	11
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	43	20	43	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		ns	7
Write command hold time	tWCH	10		10		10		ns	
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	tCWL	10		10		15		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Parameter	Symbol	-55		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	10		10		15		ns	9
Refresh period (Normal)	tREF		8		8		8	ms	
Refresh period (L-ver)	tREF		64		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		36		44		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	74		79		94		ns	7
Column address to $\overline{W}$ delay time	tAWD	49		49		59		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	54		54		64		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		35		40	ns	3
Hyper Page mode cycle time	tHPC	25		25		30		ns	11
Hyper Page mode read-modify-write cycle time	tHPRWC	56		56		71		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	60	100K	60	100K	70	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		35		40		ns	
$\overline{OE}$ access time	tOEA		15		15		20	ns	3
$\overline{OE}$ to data delay	tOED	15		15		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	15	3	15	3	20	ns	6
$\overline{OE}$ to output in low-Z	tOLZ	3		3		3		ns	
$\overline{OE}$ command hold time	tOEH	15		15		20		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	15	3	20	ns	6, 13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	15	3	15	3	20	ns	6
$\overline{W}$ to data delay	tWED	15		15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width (hyper page cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		µs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		110		130		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	12

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 50pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. tASC≥6ns, Assume tT=2.0ns.
12. For all of the refresh mode except the distributed $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 512 cycles of burst refresh must be executed within 4ms before and after self refresh, in order to meet refresh specification. (L-version).
13. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

64K x 16 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 65,536 x 16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Access time(55,60 or 70) power consumption (Normal or Low power) and package type(SOJ or TSOP) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in Low power version.

This 64Kx16 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

FEATURES

- Part Identification
  - KM416C60/L
- Active power consumption

Unit : mW

Speed	Active power consumption
-55	495
-6	440
-7	385

- Refresh cycles

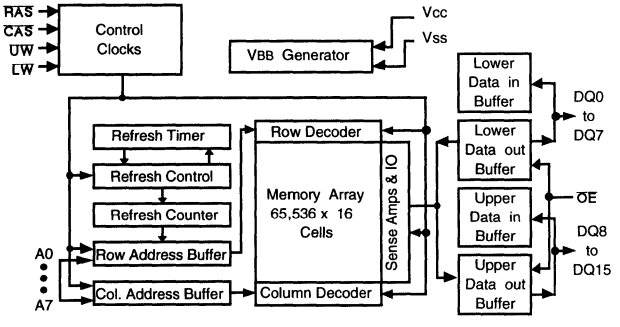
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
416C60	5V	256	4ms	32ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-55	55ns	15ns	110ns	40ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns

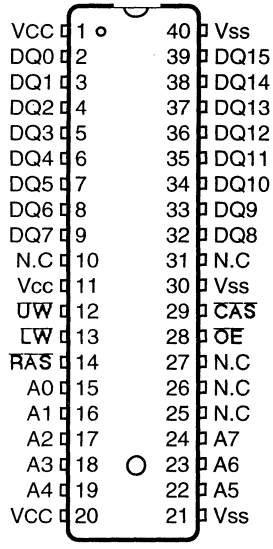
- Fast Page Mode operation
- 2 $\overline{WE}$ Byte/Word Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- Available in plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



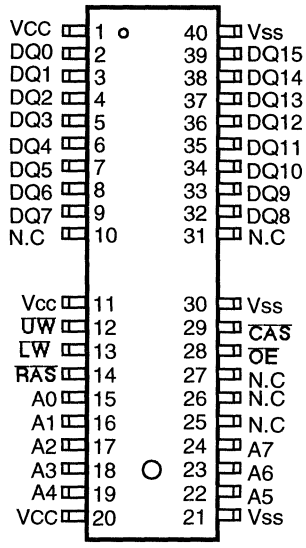
PIN CONFIGURATION (Top Views)

• KM416C60J



(SOJ)

• KM416C60T



(TSOP(II)-Forward Type)

Pin Name	Pin Function
A0 - A7	Address Inputs
DQ0 -15	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{LW}$	Lower Write Input
$\overline{UW}$	Upper Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power (+5V)
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1.0 *1	V
Input Low Voltage	V_{IL}	-1.0 *2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.

*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
Output High Voltage Level (I_{OH}=-2.5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2.1mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max KM416C60	Units
I_{CC1}	Don't care	-55 -6 -7	75 75 65	mA mA mA
I_{CC2}	Don't care	Don't care	2	mA
I_{CC3}	Don't care	-55 -6 -7	75 75 65	mA mA mA
I_{CC4}	Don't care	-55 -6 -7	65 65 60	mA mA mA
I_{CC5}	Normal L	Don't care	1 150	mA μA
I_{CC6}	Don't care	-55 -6 -7	75 75 65	mA mA mA
I_{CC7}	L	Don't care	300	μA
I_{CCS}	L	Don't care	200	μA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH}, $\overline{LW}$=$\overline{UW}$=Don't care)

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode current ($\overline{RAS}$=V_{IL} or $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=Vcc-0.2V, $\overline{LW}$=$\overline{UW}$=Don't care)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$ or $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V

Din = Don't care, T_{RC}= 125μs, T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self refresh current

$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{LW}$=$\overline{UW}$=$\overline{OE}$=A0 ~ A7 = Vcc-0.2V or 0.2V,

DQ0 ~ DQ15= Vcc-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE (T_A=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A7]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{LW}$, $\overline{UW}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, See note 1,2)

Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V

Parameter	Symbol	-55		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		110		130		ns	
Read-modify-write cycle time	tRWC	150		155		180		ns	
Access time from $\overline{RAS}$	tRAC		55		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		15		20	ns	3,4,5
Access time from column address	tAA		30		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		15		20		ns	
$\overline{CAS}$ hold time	tCSH	60		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		ns	7
Write command hold time	tWCH	10		10		10		ns	
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Parameter	Symbol	-55		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	10		10		15		ns	9
Refresh period (Normal)	tREF		4		4		4	ms	
Refresh period (L-ver)	tREF		32		32		32	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		40		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		85		95		ns	7
Column address to $\overline{W}$ delay time	tAWD	55		55		60		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	50		60		65		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		35		40	ns	3
Fast Page mode cycle time	tPC	40		40		45		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		80		95		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	60	100K	60	100K	70	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		35		40		ns	
$\overline{OE}$ access time	tOEA		15		15		20	ns	
$\overline{OE}$ to data delay	tOED	15		15		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	20	ns	6
$\overline{OE}$ command hold time	tOEH	15		15		20		ns	
Masked write Set-up time	tMCS	0		0		0		ns	
Masked write hold time referenced to $\overline{RAS}$	tMRH	0		0		0		ns	
Masked write hold time referenced to $\overline{CAS}$	tMCH	0		0		0		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		µs	11
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	100		110		130		ns	11
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	11

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 50pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. For all of the refresh mode except the distributed $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 256 cycles of burst refresh must be executed within 4ms before and after self refresh, in order to meet refresh specification.(L-ver.)

KM416C60/L Truth Table

$\overline{RAS}$	$\overline{CAS}$	$\overline{LW}$	$\overline{UW}$	$\overline{OE}$	DQ0 -DQ7	DQ8 - DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	X	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	L	H	X	DQ-IN	-	Byte Write
L	L	H	L	X	-	DQ-IN	Byte Write
L	L	L	L	X	DQ-IN	DQ-IN	Word Write

64K x 16 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 65,536 x 16 bit Extended Date Out CMOS DRAMs. Extended Date Out Mode offers high speed random access of memory cells within the same row. Access time (55, 60 or 70), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further- more, Self-refresh operation is available in Low power version.

This 64Kx16 Extended Date Out Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

FEATURES

- Part Identification
  - KM416C64/L
- Active power consumption

Unit : mW

Speed	Active power consumption
-55	495
-6	440
-7	385

- Refresh cycles

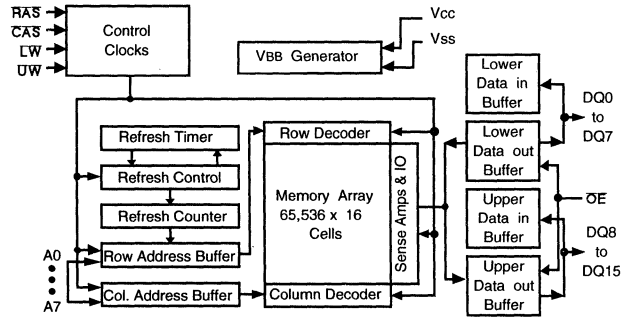
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
416C64	5V	256	4ms	32ms

- Performance range:

Speed	tRAC	tCAC	tRC	tHPC
-55	55ns	17ns	104ns	25ns
-6	60ns	17ns	104ns	25ns
-7	70ns	20ns	124ns	30ns

- Extended Date Out Mode operation
- 2 $\overline{WE}$ Byte/Word Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- Available in plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



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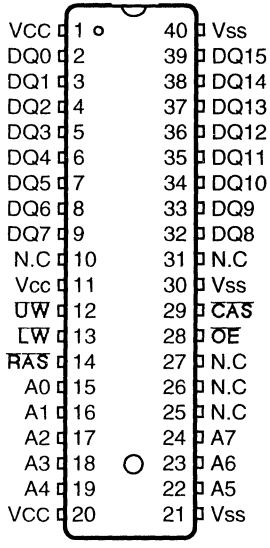
SAMSUNG ELECTRONICS

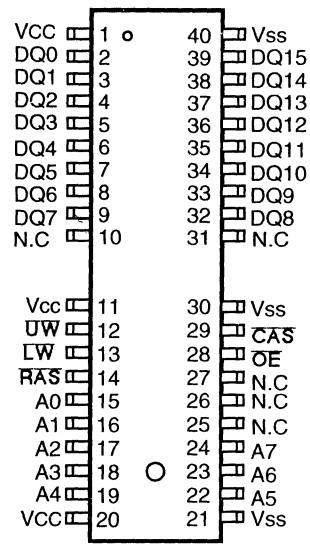
PIN CONFIGURATION (Top Views)

• **KM416C64J**



(SOJ)

• **KM416C64T**



(TSOP(II)-Forward Type)

Pin Name	Pin Function
A0 - A7	Address Inputs
DQ0 -15	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{LW}$	Lower Read/Write Input
$\overline{UW}$	Upper Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power (+5V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to Vss	V_{CC}	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.

*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
Output High Voltage Level (I_{OH}=-2.5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2.1mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max	Units
I_{CC1}	Don't care	-55 -6 -7	75 75 65	mA mA mA
I_{CC2}	Don't care	Don't care	2	mA
I_{CC3}	Don't care	-55 -6 -7	75 75 65	mA mA mA
I_{CC4}	Don't care	-55 -6 -7	90 90 80	mA mA mA
I_{CC5}	Normal L	Don't care	1 150	mA μA
I_{CC6}	Don't care	-55 -6 -7	75 75 65	mA mA mA
I_{CC7}	L	Don't care	300	μA
I_{CCS}	L	Don't care	200	μA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH}, $\overline{LW}$=$\overline{UW}$=Don't care)

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode current ($\overline{RAS}$=V_{IL} **or** $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V, $\overline{LW}$=$\overline{UW}$=Don't care)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$ **or** $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V

Din = Don't care, T_{RC}= 125μs, T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self refresh current

$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{LW}$=$\overline{UW}$=$\overline{OE}$=A0 ~ A7 = V_{CC}-0.2V or 0.2V,

DQ0 ~ DQ15= V_{CC}-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Hyper page mode cycle time, tHPC.

CAPACITANCE (T_A=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 ~ A7]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{LW}$,$\overline{UW}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 ~ DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	- 55		- 6		- 7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	104		104		124		ns	
Read-modify-write cycle time	tRWC	135		140		165		ns	
Access time from $\overline{RAS}$	tRAC		55		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		17		17		20	ns	3,4,5
Access time from column address	tAA		30		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	15	3	15	3	15	ns	6, 13
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	17		17		20		ns	
$\overline{CAS}$ hold time	tCSH	50		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	10	10K	10	10K	15	10K	ns	11
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	43	20	43	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		ns	7
Write command hold time	tWCH	10		10		10		ns	
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	tCWL	10		10		15		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Parameter	Symbol	-55		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	10		10		15		ns	9
Refresh period (Normal)	tREF		8		8		8	ms	
Refresh period (L-ver)	tREF		64		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		36		44		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	74		79		94		ns	7
Column address to $\overline{W}$ delay time	tAWD	49		49		59		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	54		54		64		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		35		40	ns	3
Hyper Page mode cycle time	tHPC	25		25		30		ns	11
Hyper Page mode read-modify-write cycle time	tHPRWC	56		56		71		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	60	100K	60	100K	70	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		35		40		ns	
$\overline{OE}$ access time	tOEA		15		15		20	ns	3
$\overline{OE}$ to data delay	tOED	15		15		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	15	3	15	3	20	ns	6
$\overline{OE}$ to output in low-Z	tOLZ	3		3		3		ns	
$\overline{OE}$ command hold time	tOEH	15		15		20		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	15	3	20	ns	6, 13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	15	3	15	3	20	ns	6
$\overline{W}$ to data delay	tWED	15		15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width (hyper page cycle)	tWPE	5		5		5		ns	
Masked write Set-up time	tMCS	0		0		0		ns	
Masked write hold time referenced to $\overline{RAS}$	tMRH	0		0		0		ns	
Masked write hold time referenced to $\overline{CAS}$	tMCH	0		0		0		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		µs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		110		130		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	12

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 50pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. tASC≥6ns. Assume tT=2.0ns
12. For all of the refresh mode except the distributed $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 256 cycles of burst refresh must be executed withen 4ms before and after self refresh, in order to meet refresh specification.(L-ver.)
13. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before RAS high going, the open circuit condition of the output is achieved by $\overline{RAS}$ going

KM416C64/L Truth Table

$\overline{RAS}$	$\overline{CAS}$	$\overline{LW}$	$\overline{UW}$	$\overline{OE}$	DQ0 -DQ7	DQ8 - DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	X	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	L	H	X	DQ-IN	-	Byte Write
L	L	H	L	X	-	DQ-IN	Byte Write
L	L	L	L	X	DQ-IN	DQ-IN	Word Write

4M DRAM

- KM41C4000C
  KM41V4000C
- KM44C1000C
  KM44V1000C
- KM44C1003C
- KM44C1004C
  KM44V1004C
- KM44C1005C

- KM48C512B
  KM48V512B
- KM48C514B
  KM48V514B
- KM416C256B
  KM416V256B
- KM416C254B
  KM416V254B

- KM48C512D
  KM48V512D
- KM48C514D
  KM48V514D
- KM416C256D
  KM416V256D
- KM416C254D
  KM416V254D

4M x 1 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 4,194,304 x 1 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time(-5, -6, -7 or -8), power consumption (Normal, Low power) , and package type (SOJ, ZIP, TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in Low power version.
This 4Mx1 Fast Page Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory for main frames ,mini computers, personal computer and high performance microprocessor systems.

FEATURES

- Part Identification
  - KM41C4000C/CL(5V)
  - KM41V4000C/CL(3.3V)

- Active Power Dissipation Unit : mW

Speed	3.3V	5V
-5	-	470
-6	220	415
-7	200	360
-8	180	-

- Refresh cycles

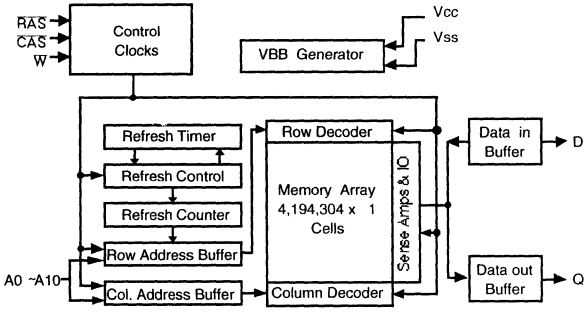
	Vcc	Refresh cycle	Refresh time	
			Normal	L
C1000C	5V	1K	16ms	128ms
V1000C	3.3V			

- Performance range:

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	13ns	90ns	35ns	5V Only
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	3.3V

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (3.3V,L-ver only)
- Fast parallel test mode capability
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Common I/O using early write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +5V±10% power supply(5V product)
- +3.3V±0.3V power supply(3.3V product)

FUNCTIONAL BLOCK DIAGRAM



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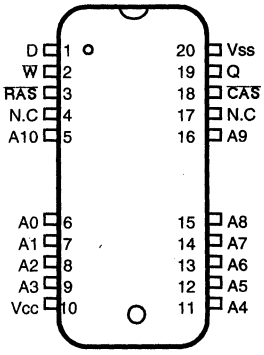
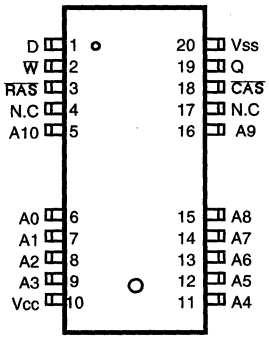
PIN CONFIGURATION (Top Views)

• KM41C/V4000CJ



• KM41C/V4000CT



Pin Name	Pin Function
A0 - A10	Address Inputs
D	Data In
Q	Data Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
N.C	No Connection
Vcc	Power(+5.0V)
	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage temperature	Tstg	-55 to +150	-55 to +150	°C
Power dissipation	P_D	600	600	mW
Short circuit output current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input high voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1*1	V
Input low voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V),Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V),Pulse width is measured atVss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input leakage current (Any input 0≤V_{IN}≤Vcc+0.3V , all other pins not under test=0 volts.)	$I_{I(L)}$	-5	5	μA
	Output leakage current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output high voltage level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output low voltage level(I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input leakage current (Any input 0≤V_{IN}≤Vcc+0.5V all other pins not under test=0 volts.)	$I_{I(L)}$	-5	5	μA
	Output leakage current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output high voltage level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output low voltage level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM41V4000C	KM41C4000C	
I_{CC1}	Don't care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
		-8	50	-	mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
		-8	50	-	mA
I_{CC4}	Don't care	-5	-	65	mA
		-6	45	55	mA
		-7	40	45	mA
		-8	35	-	mA
I_{CC5}	Normal	Don't care	0.5	1	mA
	L		100	200	μA
I_{CC6}	Don't care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
		-8	50	-	mA
I_{CC7}	L	Don't care	200	300	μA
I_{CCS}	L	Don't care	150	-	μA

I_{CC1} *: Operating current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} *: $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4} *: Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} *: $\overline{CAS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=0.2V

D_{IN} = Don't care, T_{RC}= 125μs(L-ver), T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self refresh current

$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A10= D= Vcc-0.2V or 0.2V

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [D]	C_{IN1}	-	5	pF
Input capacitance [A0 - A10]	C_{IN2}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$]	C_{IN3}	-	7	pF
Output capacitance [Q]	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition(5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition(3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	108		130		155		175		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	35	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	15
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	15
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	

Note) *1 : 5V only, *2 : 3.3V only

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 2)

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time	tDH	10		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	15
Refresh period(Normal)	tREF		16		16		16		16	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	13		15		20		20		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	50		60		70		80		ns	7
Column address to $\overline{W}$ delay time	tAWD	25		30		35		40		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	30		35		40		45		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	53		60		70		75		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		µs	14
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	14
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	14

Note) *1 : 5V only, *2 : 3.3V only

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	113		135		160		180		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	18		20		25		25		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	55		65		75		85		ns	7
Column address to $\overline{W}$ delay time	tAWD	30		35		40		45		ns	7
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	58		65		75		80		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3

Note) *1 : 5V only, *2 : 3.3V only

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD(max) is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min),the cycles is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 1024cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.(3.3V L-ver.)
15. tAR , tWCR, tDHR are referenced to tRAD(max.).

1M x 4 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 1,048,576 x 4 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time(-5, -6, -7 or -8), power consumption (Normal or Low power) , and package type (SOJ , DIP, ZIP or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in 3.3V Low power version.

This 1Mx4 Fast Page Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory for main frames and mini computers, personal computer and high performance microprocessor systems.

FEATURES

- Part Identification
  - KM44C1000C/CL(5V)
  - KM44V1000C/CL(3.3V)

- Active Power Dissipation

Unit : mW

Speed	3.3V	5V
-5	-	470
-6	220	415
-7	200	360
-8	180	-

- Refresh cycles

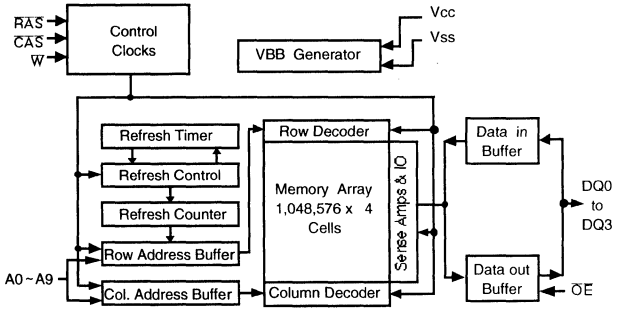
	Vcc	Refresh cycle	Refresh time	
			Normal	L
C1000C	5V	1K	16ms	128ms
V1000C	3.3V			

- Performance range:

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	13ns	90ns	35ns	5V
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	3.3V

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (3.3V,L-ver only)
- Fast parallel test mode capability
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V$\pm$10% power supply(5V product)
- Single +3.3V$\pm$0.3V power supply(3.3V product)

FUNCTIONAL BLOCK DIAGRAM



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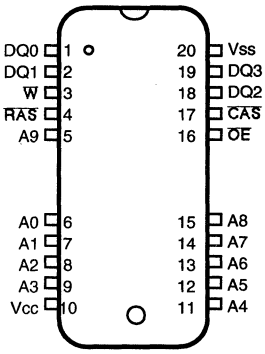
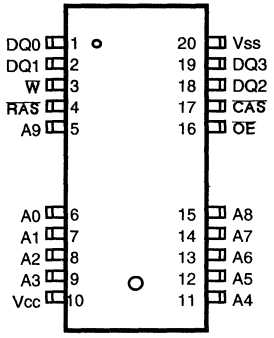
SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top Views)

• KM44C/V1000CJ



• KM44C/V1000CT



Pin Name	Pin Function
A0 - A9	Address Inputs
DQ0 -3	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
V_{CC}	Power(+5.0V)
	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage temperature	Tstg	-55 to +150	-55 to +150	°C
Power dissipation	P_D	600	600	mW
Short circuit output current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input high voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input low voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V),Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V),Pulse width is measured atVss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input leakage current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volts.)	$I_{I(L)}$	-5	5	μA
	Output leakage current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output high voltage level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output low voltage level(I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input leakage current (Any input 0≤V_{IN}≤Vcc+0.5V all other pins not under test=0 volts.)	$I_{I(L)}$	-5	5	μA
	Output leakage current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output high voltage level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output low voltage level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM44V1000C	KM44C1000C	
I_{CC1}	Don't care	-5 -6 -7 -8	- 60 55 50	85 75 65 -	mA mA mA mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5 -6 -7 -8	- 60 55 50	85 75 65 -	mA mA mA mA
I_{CC4}	Don't care	-5 -6 -7 -8	- 45 40 35	65 55 45 -	mA mA mA mA
I_{CC5}	Normal L	Don't care	0.5 100	1 200	mA μA
I_{CC6}	Don't care	-5 -6 -7 -8	- 60 55 50	85 75 65 -	mA mA mA mA
I_{CC7}	L	Don't care	200	300	μA
I_{CCS}	L	Don't care	150	-	μA

I_{CC1} *: Operating current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} *: $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4} *: Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} *: $\overline{CAS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=0.2V

DQ_{0-3} = Don't care, T_{RC}= 125μs(L-ver) ,T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self refresh current

$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A9= V_{CC}-0.2V or 0.2V,

DQ0 ~ DQ3= V_{CC}-0.2V, 0.2V or OPEN

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition(5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition(3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	15
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	15
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead tim	tRWL	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	

Note) *1 : 5V only, *2 : 3.3V only

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 2)

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time	tDH	10		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	15
Refresh period(Normal)	tREF		16		16		16		16	ms	
Refresh period(L-ver)	tREF		128		128		128	0	128	ms	
Write command set-up time	tWCS	0		0		0		50		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		110		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		70		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		65		75		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		10		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		15		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		5		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		30		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25				ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	50	45	ns	3
Fast Page mode cycle time	tPC	35		40		45		105		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		10		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		80		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	45	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40				ns	
$\overline{OE}$ access time	tOEA		13		15		20	20	20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		0		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	20	20	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		20		10		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		100		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		150		us	14
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		-50		ns	14
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50				ns	14

Note) *1 : 5V only, *2 : 3.3V only

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	7
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

Note) *1 : 5V only, *2 : 3.3V only

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD(max) is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min),the cycles is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 1024cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.(3.3V L-ver.)
15. tAR, tWCR , tDHR are referenced to tRAD(max).

1M x 4 Bit CMOS Quad CAS DRAM with Fast Page Mode

DESCRIPTION

This is a family of 1,048,576 x 4 bit Fast Page Mode Quad CAS CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Access time(-5, -6, -7 or -8), power consumption (Normal, Low power) , and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities.
All inputs and outputs are fully TTL compatible and four seperate $\overline{CAS}$ pins provide for seperate I/O operation allowing this device to operate in parity mode.
This 1Mx4 Fast Page Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM44C1003C/CL(5V)

- Active Power Dissipation

Unit : mW

Speed	Active power dissipation
-5	470
-6	415
-7	360

- Refresh cycles

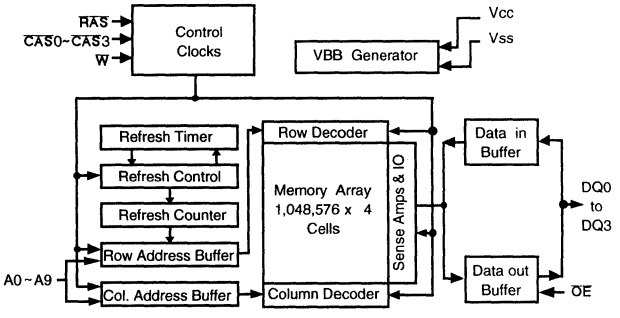
Part NO.	Refresh Cycle	Refresh Period	
		Normal	L
C1003C	1K	16ms	128ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns

- Fast Page Mode operation
- Four seperate $\overline{CAS}$ pins provide for seperate I/O operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- RAS-only and Hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



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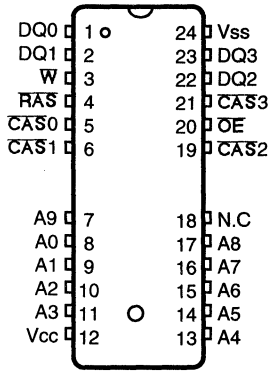
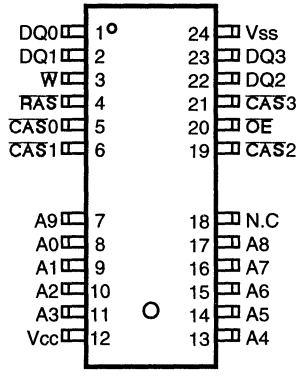
PIN CONFIGURATION (Top Views)

• KM44C1003CJ



• KM44C1003CT



Pin Name	Pin Function
A0 - A9	Address Inputs
DQ0 -3	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS0}$-$\overline{CAS3}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage temperature	Tstg	-55 to +150	°C
Power dissipation	P_D	600	mW
Short circuit output current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	Vcc+1.0*1	V
Input low voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc
*2 : -2.0V/20ns(5V),Pulse width is measured at Vss

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input leakage current (Any input 0≤V_{IN}≤Vcc+0.5V all other pins not under test=0 volts.)	$I_{I(L)}$	-5	5	μA
Output leakage current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
Output high voltage level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output low voltage level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max	Units
			KM44C1003C	
I_{CC1}	Don't care	-5 -6 -7	85 75 65	mA mA mA
I_{CC2}	Normal L	Don't care	2 1	mA mA
I_{CC3}	Don't care	-5 -6 -7	85 75 65	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	65 55 45	mA mA mA
I_{CC5}	Normal L	Don't care	1 200	mA μA
I_{CC6}	Don't care	-5 -6 -7	85 75 65	mA mA mA
I_{CC7}	L	Don't care	300	μA

I_{CC1} *: Operating current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} *: $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4} *: Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} *: $\overline{CAS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=0.2V

DQ0~3 = Don't care, T_{RC}= 125μs(L-ver), T_{RAS}=T_{RAS}min~300 ns

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc=5V , f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$0-$\overline{CAS}$3, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	133		155		185		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,18
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3,18
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	ns	6,18
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	16
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	17
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4,16
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	17
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	16
Column address hold time	tCAH	10		10		15		ns	16
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	26
Read command set-up time	tRCS	0		0		0		ns	16
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8,17
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	10		10		15		ns	24
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		ns	26
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		ns	17

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 2)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		10		15		ns	10
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		ns	26
Refresh period(Normal)	tREF		16		16		16	ms	
Refresh period(L-ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7,16
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		ns	7,16
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	16
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	17
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	3,18
Fast Page mode cycle time	tPC	35		40		45		ns	19
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		ns	19
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	20
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	21
$\overline{OE}$ to data delay	tOED	13		15		20		ns	21
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		ns	
Write command hold time(Test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	5		5		5		ns	
Hold time $\overline{CAS}$ low to $\overline{CAS}$ high	tCLCH	5		5		5		ns	14,25

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		ns	
Read-modify-write cycle time	tRWC	138		160		190		ns	
Access time from $\overline{RAS}$	tRAC		60		65		75	ns	3,4,10,12
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5,12
Access time from column address	tAA		30		35		40	ns	3,10,12
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		60		70		ns	7
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
$\overline{OE}$ access time	tOEA		20		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD(max) is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min),the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. In order to hold the address latched by the first $\overline{CAS}$x going low, the parameter tCLCH must be met.
15. If at least one $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, all four $\overline{CAS}$ must be pulsed high for tCP.
16. The first $\overline{CAS}$x edge to transition low.
17. The last $\overline{CAS}$x edge to transition low.
18. Output parameter is referenced to corresponding $\overline{CAS}$x input.
19. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
20. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
21. First DQx controlled by the first $\overline{CAS}$x to go low.
22. Last DQx controlled by the first $\overline{CAS}$x to go low.
23. Each $\overline{CAS}$x must meet minimum pulse width.
24. Last $\overline{CAS}$x to go low.
25. The last falling $\overline{CAS}$x edge to the first rising $\overline{CAS}$x edge
26. tAR,tWCR,tDHR are referenced to tRAD(max).

1M x 4 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 1,048,576 x 4 bit Extended Data Out CMOS DRAMs. Extended Data Out offers high speed random access of memory cells within the same row. Power supply voltage(+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities.

This 1Mx4 Extended Data Out DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

It may be used as main memory unit for microcomputer, personal computer and portable machines.

FEATURES

- Part Identification
  - KM44C1004C/CL (5V)
  - KM44V1004C/CL (3.3V)

- Active Power Dissipation

Unit : mW

Speed	3.3V	5V
-5	-	468
-6	220	413
-7	200	358
-8	180	-

- Refresh cycles

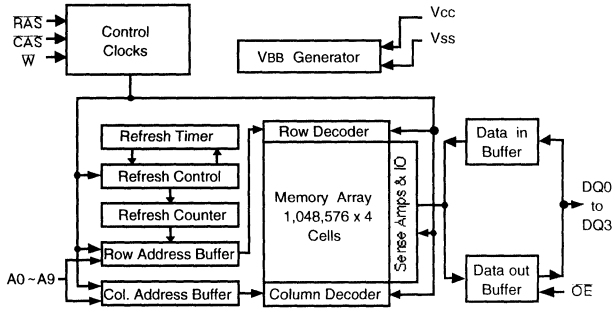
	Vcc	Refresh cycle	Refresh Period	
			Normal	L
C1004C	5V	1K	16ms	128ms
V1004C	3.3V			

- Performance range:

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	15ns	84ns	35ns	5V
-6	60ns	15ns	104ns	40ns	5V/3.3V
-7	70ns	20ns	124ns	45ns	5V/3.3V
-8	80ns	20ns	144ns	50ns	3.3V

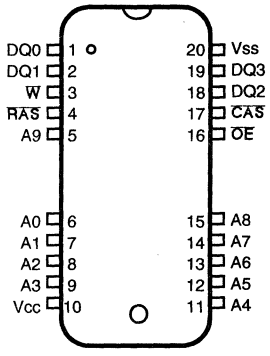
- Extended Data Out operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (3.3V,L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM

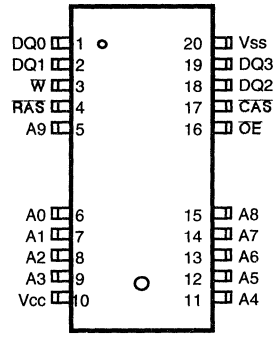


PIN CONFIGURATION (Top Views)

• KM44C/V1004CJ



• KM44C/V1004CT



Pin Name	Pin Function
A0 - A9	Address Inputs
DQ0 -3	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
V_{CC}	Power(+5.0V)
	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	600	600	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V),Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V),Pulse width is measured atVss

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM44V1004C	KM44C1004C	
I_{CC1}	Don't care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
		-8	50	-	mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
		-8	50	-	mA
I_{CC4}	Don't care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
		-8	50	-	mA
I_{CC5}	Normal	Don't care	0.5	1	mA
	L		100	200	µA
I_{CC6}	Don't care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
		-8	50	-	mA
I_{CC7}	L	Don't care	200	300	µA
I_{CCS}	L	Don't care	150	-	µA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : EDO Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V

DQ0~3 = Don't care, T_{RC}=125µs, T_{RAS}=T_{RAS} min~300 ns

I_{CCS} : Self refresh current

$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A9 = V_{CC}-0.2V or 0.2V,

DQ0 ~ DQ3= V_{CC}-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} , I_{CC3} and I_{CC6}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 ~ A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 ~ DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8 *2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		144		ns	
Read-modify-write cycle time	tRWC	116		140		165		190		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	3	20	ns	7,13
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	40		50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	11
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	33	20	43	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	35		42		52		57		ns	17
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	37		42		52		57		ns	17
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	

Note) *1 : 5V only, *2 : 3.3V only

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time	tDH	8		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	35		42		52		57		ns	17
Refresh period(Normal)	tREF		16		16		16		16	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	30		34		44		44		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		89		99		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		49		59		64		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		69		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40		45	ns	3
Hyper Page mode cycle time	tHPC	20		25		30		35		ns	15
Hyper Page mode read-modify-write cycle time	tHPRWC	47		56		71		81		ns	
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	6,13
$\overline{OE}$ to output in low-Z	tOLZ	3		3		3		3		ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	6,13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	6,13
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width (hyper page cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		µs	16
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	16
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	16

Note) *1 : 5V only, *2 : 3.3V only

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	89		109		129		149		ns	
Read-modify-write cycle time	tRWC	121		145		170		195		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	45		55		65		75		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	35		39		49		49		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	72		84		94		104		ns	7
Column address to $\overline{W}$ delay time	tAWD	47		54		64		69		ns	7
Hyper Page mode cycle time	tHPC	25		30		35		40		ns	15
Hyper page mode read-modify-write cycle time	tPRWC	52		61		76		86		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		33		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

Note) *1 : 5V only, *2 : 3.3V only

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tCEZ(max),tREZ(max),tOEZ(max) and tWEZ(max) define the time at which the output achives the open circuit condition and are not referenced to output voltage level.
14. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. tASC≥6ns, Assume tT=2.0ns.
16. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 1024 cycles of burst refresh must be executed within 16ms before and after self refresh,in order to meet refresh specification.(3.3V L-Ver.)
17. tAR , tWCR ,tDHR are referenced to tRAD(max).

1M x 4 Bit CMOS Quad CAS DRAM with Extended Data Out

DESCRIPTION

This is a family of 1,048,576 x 4 bit Extended Data Out Quad CAS CMOS DRAMs. Extended Data Out offers high speed random access of memory cells within the same row. Access time (-5, -6, -7 or -8), power consumption (Normal, Low power) , and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in Low power version.
Four seperate $\overline{CAS}$ pins provide for seperate I/O operation allowing this device to operate in parity mode.
This 1Mx4 Extended Data Out DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM44C1005C/CL(5V)

- Active Power Dissipation

Unit : mW

Speed	5V
-5	468
-6	413
-7	358

- Refresh cycles

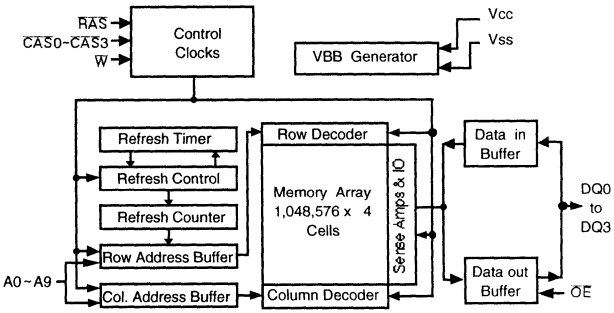
	Vcc	Refresh cycle	Refresh Period	
			Normal	L
C1005C	5V	1K	16ms	128ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	15ns	84ns	35ns
-6	60ns	15ns	104ns	40ns
-7	70ns	20ns	124ns	45ns

- Extended Data Out mode operation (Fast Page Mode with Extended data out)
- Four seperate $\overline{CAS}$ pins provide for seperate I/O operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- RAS-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ, TSOP(II) packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



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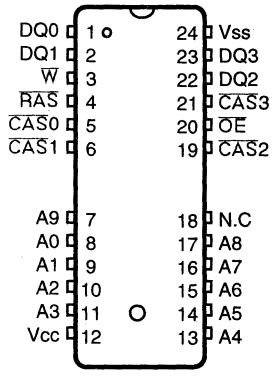
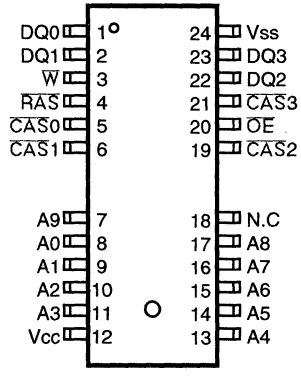
PIN CONFIGURATION (Top Views)

• KM44C1005CJ



• KM44C1005CT



Pin Name	Pin Function
A0 - A9	Address Inputs
DQ0 -3	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS0}$-$\overline{CAS3}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤ 20ns, Pulse width is measured at Vcc.

*2 : - 2.0V at pulse width ≤ 20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max	Units
			KM44C1005C	
I_{CC1}	Don't care	-5 -6 -7	85 75 65	mA mA mA
I_{CC2}	Don't care	Don't care	2	mA
I_{CC3}	Don't care	-5 -6 -7	85 75 65	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	85 75 65	mA mA mA
I_{CC5}	Normal L	Don't care	1 200	mA µA
I_{CC6}	Don't care	-5 -6 -7	85 75 65	mA mA mA
I_{CC7}	L	Don't care	300	µA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : EDO Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V
DQ0~3 = Don't care, T_{RC}=125µs, T_{RAS}=T_{RAS} min~300 ns

I_{CC5} : Self refresh current
$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A9 = V_{CC}-0.2V or 0.2V,
DQ0 ~ DQ3= V_{CC}-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} , I_{CC3} and I_{CC6}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle.

CAPACITANCE (T_A=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 ~ A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 ~ DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		ns	
Read-modify-write cycle time	tRWC	116		140		165		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,5,20
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3,20
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	ns	6,13,20
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	18
$\overline{CAS}$ hold time	tCSH	40		50		60		ns	19
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	ns	11,25
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	33	20	43	20	50	ns	4,18
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	19
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	18
Column address hold time	tCAH	8		10		15		ns	18
Column address hold time referenced to $\overline{RAS}$	tAR	35		42		52		ns	29
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	10		10		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	37		42		52		ns	29
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		ns	19
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Test condition : V_{cc}=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	8		10		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	35		42		52		ns	29
Refresh period(Normal)	tREF		16		16		16	ms	
Refresh period(L-ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7,18
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	30		34		44		ns	7,18
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		89		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		49		59		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	18
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40	ns	3,20
Hyper Page mode cycle time	tHPC	20		25		30		ns	15,21
Hyper Page mode read-modify-write cycle time	tHPRWC	47		56		71		ns	21
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		ns	22
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	23
$\overline{OE}$ to data delay	tOED	13		15		20		ns	23
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	ns	6,13
$\overline{OE}$ to output in low-Z	tOLZ	3		3		3		ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	ns	6,13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	ns	6,13
$\overline{W}$ to data delay	tWED	15		15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width (hyper page cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		µs	28
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		ns	28
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)Write	tCHS	-50		-50		-50		ns	28

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Test condition : V_{cc}=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
Hold time $\overline{CAS}$ low to $\overline{CAS}$ high	tCLCH	5		5		5		ns	16,27

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	89		109		129		ns	
Read-modify-write cycle time	tRWC	121		145		170		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,10,12
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5,12
Access time from column address	tAA		30		35		40	ns	3,10,12
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	45		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	35		39		49		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	72		84		94		ns	7
Column address to $\overline{W}$ delay time	tAWD	47		54		64		ns	7
Hyper Page mode cycle time	tHPC	25		30		35		ns	15
Hyper page mode read-modify-write cycle time	tPRWC	52		61		76		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		33		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD(max) is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min),the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles, and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tCEZ(max),tREZ(max),tOEZ(max) and tWEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. tASC≥6ns, Assume tT=2.0ns.
16. In order to hold the address latched by the first $\overline{CAS}$x going low, the parameter tCLCH must be met.
17. If at least one $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, all four $\overline{CAS}$ must be pulsed high for tCP.
18. The first $\overline{CAS}$x edge to transition low.
19. The last $\overline{CAS}$x edge to transition low.
20. Output parameter is referenced to corresponding $\overline{CAS}$x input.
21. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
22. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
23. First DQx controlled by the first $\overline{CAS}$x to go low.
24. Last DQx controlled by the first $\overline{CAS}$x to go low.
25. Each $\overline{CAS}$x must meet minimum pulse width.
26. Last $\overline{CAS}$x to go low.
27. The last falling $\overline{CAS}$x edge to the first rising $\overline{CAS}$x edge
28. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 1024 cycles of burst refresh must be executed within 16ms before and after self refresh,in order to meet refresh specification.(L-Ver.)
29. tAR,tWCR,tDHR are referenced to tRAD(max).

512K x 8 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 524,288 x 8 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage(+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in Low power version.

This 512Kx8 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

It may be used as main memory unit for personal computer and portable machines.

FEATURES

- Part Identification
  - KM48C512B/BL (5V, 1K Ref.)
  - KM48V512B/BL (3.3V, 1K Ref.)

- Active power dissipation

Unit : mW

Speed	3.3V (1K Ref.)	5V (1K Ref.)
-5	-	470
-6	255	385
-7	235	360
-8	220	-

- Refresh cycles

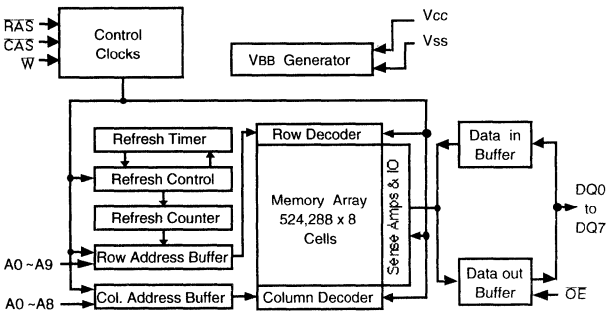
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
C512B	5V	1K	16ms	128ms
V512B	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	15ns	90ns	35ns	5V
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	3.3V

- Fast Page Mode operation
- Byte Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages
- Dual+5V±10% power supply (5V product)
- Dual +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM



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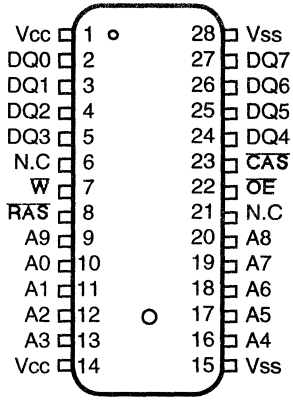
SAMSUNG ELECTRONICS

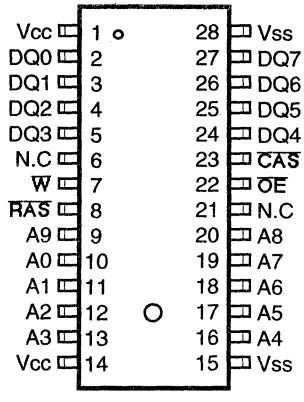
PIN CONFIGURATION (Top Views)

• KM48C/V512BJ



(SOJ)

• KM48C/V512BT



(TSOP(II)-Forward Type)

Pin Name	Pin Function	Pin Name	Pin Function
A0 - A9	Address Inputs	$\overline{W}$	Read/Write Input
DQ0 -7	Data In/Out	$\overline{OE}$	Data Output Enable
Vss	Ground	Vcc	Power (+5V)
$\overline{RAS}$	Row Address Strobe		Power (+3.3V)
$\overline{CAS}$	Column Address Strobe	N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM48V512B	KM48C512B	
I_{CC1}	Don't care	-5	-	85	mA
		-6	70	70	mA
		-7	65	65	mA
		-8	60	-	mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5	-	85	mA
		-6	70	70	mA
		-7	65	65	mA
		-8	60	-	mA
I_{CC4}	Don't care	-5	-	65	mA
		-6	55	55	mA
		-7	50	50	mA
		-8	45	-	mA
I_{CC5}	Normal	Don't care	0.5	1	mA
	L		100	150	µA
I_{CC6}	Don't care	-5	-	85	mA
		-6	70	70	mA
		-7	65	65	mA
		-8	60	-	mA
I_{CC7}	L	Don't care	200	300	µA
I_{CCS}	L	Don't care	100	200	µA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V

Din = Don't care, T_{RC}=125µs, T_{RAS}=T_{RAS} min~300 ns

I_{CCS} : Self refresh current

$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A9 = Vcc-0.2V or 0.2V,

DQ0 ~ DQ7= Vcc-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 ~ A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0~ DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition (3.3V device): Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	135		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	35	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time (5V)	tCAH	10		10		15		15		ns	
Column address hold time (3.3V)	tCAH	-		15		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		10		10		ns	
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		20		ns	

Note) *1 : 50ns product : Vcc=5V±5%, Output Loading(C_L)=50pF, *2 : 3.3V only

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time (5V)	tDH	10		10		15		15		ns	9
Data hold time (3.3V)	tDH	-		15		15		15		ns	9
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		40		50		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	75		85		95		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	50		55		60		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	55		60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		80		95		105		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	20	0	20	ns	6
$\overline{OE}$ command hold time	tOEH	15		15		20		20		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	11
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	11
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	11

Note) *1 : 50ns product : Vcc=5V±5%, Output Loading(C_L)=50pF, *2 : 3.3V only

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 1024 cycle of burst refresh must be executed within 16ms before and after self refresh in order to meet refresh specification (L-version).

512K x 8 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 524,288 x 8 bit Extended Data Out CMOS DRAMs. Extended Data Out offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in Low power version.

This 512Kx8 Extended Data Out DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

It may be used as main memory unit for personal computer and portable machines.

FEATURES

- Part Identification
  - KM48C514B/BL (5V, 1K Ref.)
  - KM48V514B/BL (3.3V, 1K Ref.)

- Active power dissipation

Unit : mW

Speed	3.3V (1K Ref.)	5V (1K Ref.)
-5	-	470
-6	255	385
-7	235	360
-8	220	-

- Refresh cycles

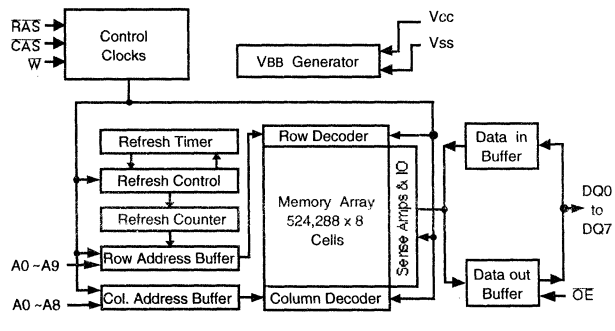
Part NO.	Vcc	Refresh cycle	Refresh Period	
			Normal	L
C514B	5V	1K	16ms	128ms
V514B	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tHPC	Remark
-5	50ns	15ns	84ns	20ns	5V Only
-6	60ns	15ns	104ns	25ns	5V/3.3V
-7	70ns	20ns	124ns	30ns	5V/3.3V
-8	80ns	20ns	144ns	35ns	3.3V Only

- Extended Data Out operation
- Byte Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages
- Dual +5V±10% power supply (5V product)
- Dual +3.3V±0.3V power supply (3.3V product)

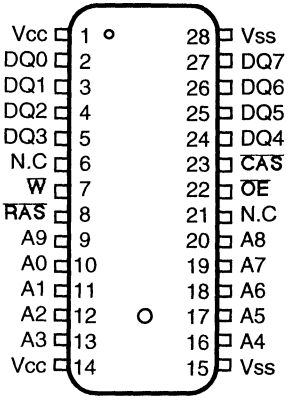
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

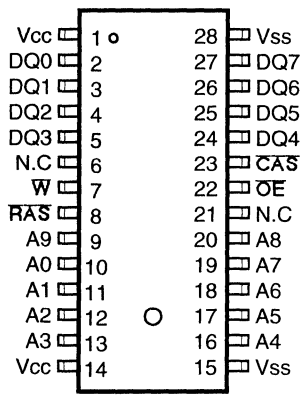
PIN CONFIGURATION (Top Views)

• **KM48C/V514BJ**



(SOJ)

• **KM48C/V514BT**



(TSOP(II)-Forward Type)

Pin Name	Pin Function	Pin Name	Pin Function
A0 - A9	Address Inputs	$\overline{W}$	Read/Write Input
DQ0 -7	Data In/Out	$\overline{OE}$	Data Output Enable
Vss	Ground	Vcc	Power (+5V)
$\overline{RAS}$	Row Address Strobe		Power (+3.3V)
$\overline{CAS}$	Column Address Strobe	N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM48V514B	KM48C514B	
I_{CC1}	Don't care	-5	-	85	mA
		-6	70	70	mA
		-7	65	65	mA
		-8	60	-	mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5	-	85	mA
		-6	70	70	mA
		-7	65	65	mA
		-8	60	-	mA
I_{CC4}	Don't care	-5	-	65	mA
		-6	55	55	mA
		-7	50	50	mA
		-8	45	-	mA
I_{CC5}	Normal	Don't care	0.5	1	mA
	L		100	150	µA
I_{CC6}	Don't care	-5	-	85	mA
		-6	70	70	mA
		-7	65	65	mA
		-8	60	-	mA
I_{CC7}	L	Don't care	200	300	µA
I_{CCS}	L	Don't care	100	200	µA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V
Din = Don't care, T_{RC}=125µs, T_{RAS}=T_{RAS} min~300 ns

I_{CCS} : Self refresh current
$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A9 = Vcc-0.2V or 0.2V,
DQ0 ~ DQ7 = Vcc-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle time, tHPC

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 ~ A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 ~ DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		144		ns	
Read-modify-write cycle time	tRWC	116		140		165		190		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		17		17		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	15	3	15	ns	6, 13
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	17		17		20		20		ns	
$\overline{CAS}$ hold time	tCSH	40		50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	11
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	33	20	43	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time (5V)	tCAH	8		10		15		-		ns	
Column address hold time (3.3V)	tCAH	-		15		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		10		10		ns	
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	

Note) *1: 50ns product : Vcc=5V±5%, Output Loading(C_L)=50pF, *2 : 3.3V only

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time (5V)	tDH	8		10		15		-		ns	9
Data hold time (3.3V)	tDH	-		15		15		15		ns	
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	34		36		44		44		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		94		104		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		49		59		64		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		69		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40		45	ns	3
Hyper Page mode cycle time	tHPC	20		25		30		35		ns	11
Hyper Page mode read-modify-write cycle time	tHPRWC	47		56		71		81		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		15		20		20	ns	3
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	6
$\overline{OE}$ to output in low-Z	tOLZ	3		3		3		3		ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	6, 13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	6
$\overline{W}$ to data delay	tWED	13		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width (hyper page cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		µs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

Note) *1: 50ns product : Vcc=5V±5%, Output Loading(C_L)=50pF, *2 : 3.3V only

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. tASC≥6ns, Assume tT=2.0ns.
12. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 1024 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (L-version).
13. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

256K x 16 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 262,144 x 16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in Low power version.

This 256Kx16 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

2

FEATURES

- Part Identification
  - KM416C256B/BL (5V, 512 Ref.)
  - KM416V256B/BL (3.3V, 512 Ref.)

- Active power dissipation

Unit : mW

Speed	3.3V (512 Ref.)	5V (512 Ref.)
-5	-	605
-6	325	495
-7	290	440
-8	270	-

- Refresh cycles

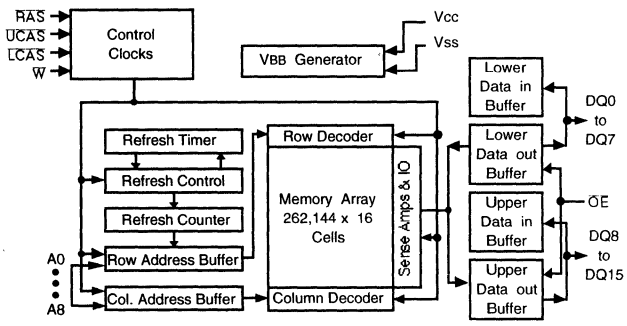
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
C256B	5V	512	8ms	128ms
V256B	3.3V			

- Performance range:

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	15ns	90ns	35ns	5V
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	3.3V

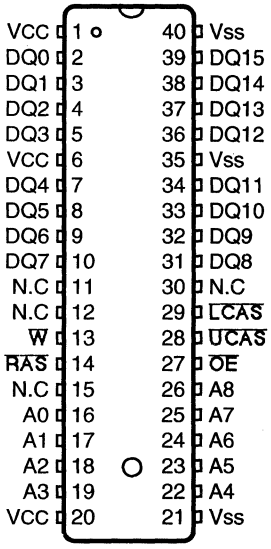
- Fast Page Mode operation
- 2 $\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages
- Triple +5V±10% power supply (5V product)
- Triple +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM



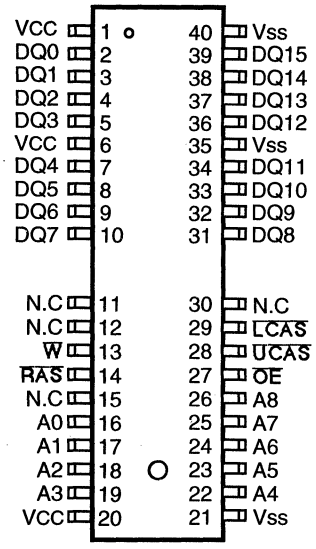
PIN CONFIGURATION (Top Views)

• KM416C/V256BJ



(SOJ)

• KM416C/V256BT



(TSOP(II)-Forward Type)

Pin Name	Pin Function
A0 - A8	Address Inputs
DQ0 -15	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power (+5V)
	Power (+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM416V256B	KM416C256B	
I_{CC1}	Don't care	-5	-	110	mA
		-6	90	90	mA
		-7	80	80	mA
		-8	75	-	mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5	-	110	mA
		-6	90	90	mA
		-7	80	80	mA
		-8	75	-	mA
I_{CC4}	Don't care	-5	-	70	mA
		-6	60	60	mA
		-7	55	55	mA
		-8	50	-	mA
I_{CC5}	Normal	Don't care	0.5	1	mA
	L		100	150	μA
I_{CC6}	Don't care	-5	-	110	mA
		-6	90	90	mA
		-7	80	80	mA
		-8	75	-	mA
I_{CC7}	L	Don't care	200	300	μA
I_{CCS}	L	Don't care	100	200	μA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$, $\overline{LCAS}$= 0.2V

Din = Don't care, T_{RC}= 125μs, T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self refresh current

$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A8 = V_{CC}-0.2V or 0.2V,

DQ0 ~ DQ15= V_{CC}-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A8]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	135		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	35	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	12
Column address hold time (5V)	tCAH	10		10		15		15		ns	12
Column address hold time (3.3V)	tCAH	-		15		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		0		ns	
Write command hold time	tWCH	10		10		10		10		ns	
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		20		ns	15

Note) *1: 50ns product : Vcc=5V±5%, *2 : 3.3V only

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9,18
Data hold time (5V)	tDH	10		10		15		15		ns	9,18
Data hold time (3.3V)	tDH	-		15		15		15		ns	9,18
Refresh period (Normal)	tREF		8		8		8		8	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		40		50		50		ns	7,14
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	75		85		95		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	50		55		60		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	55		60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	16
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	17
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		80		95		105		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	13
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	20	0	20	ns	6
$\overline{OE}$ command hold time	tOEH	15		15		20		20		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	11
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	11
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	11

Note) *1: 50ns product : Vcc=5V±5%, *2 : 3.3V only

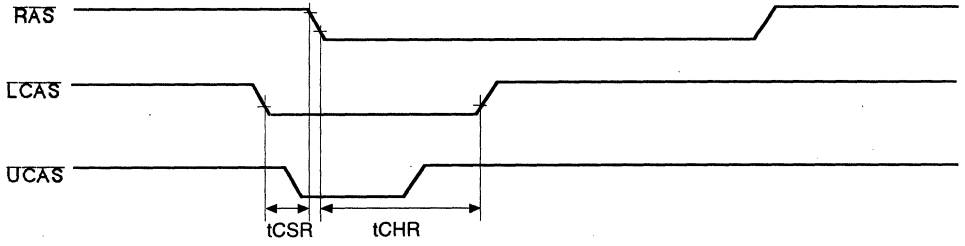
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 50pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

KM416C/V256B/BL Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8 - DQ15	STATE
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

11. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 512 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (L-version).
12. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
13. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
16. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
17. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



18. tDS, tDH is independently specified for lower byte D_{IN}(0~7), upper byte D_{IN}(8~15).

256K x 16 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 262,144 x 16 bit Extended Data Out CMOS DRAMs. Extended Data Out offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in Low power version.

This 256Kx16 Extended Data Out DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

FEATURES

- Part Identification
  - KM416C254B/BL (5V, 512 Ref.)
  - KM416V254B/BL (3.3V, 512 Ref.)

- Active power dissipation

Unit : mW

Speed	3.3V (512 Ref.)	5V (512 Ref.)
-5	-	605
-6	255	495
-7	235	440
-8	220	-

- Refresh cycles

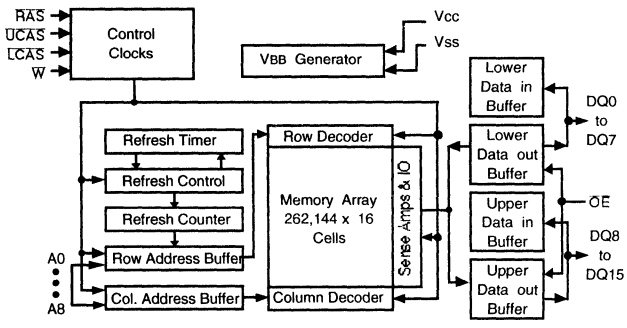
Part NO.	Vcc	Refresh cycle	Refresh Period	
			Normal	L
C254B	5V	512	8ms	128ms
V254B	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tHPC	Remark
-5	50ns	17ns	84ns	20ns	5V Only
-6	60ns	17ns	104ns	25ns	5V/3.3V
-7	70ns	20ns	124ns	30ns	5V/3.3V
-8	80ns	20ns	144ns	35ns	3.3V Only

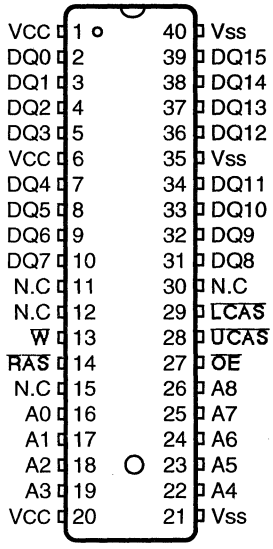
- Extended Data Out operation
- 2 $\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages
- Triple +5V±10% power supply (5V product)
- Triple +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM



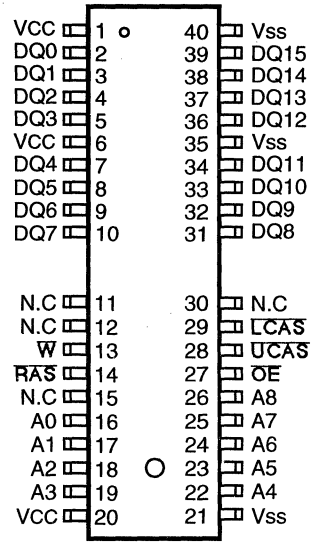
PIN CONFIGURATION (Top Views)

• KM416C/V254BJ



(SOJ)

• KM416C/V254BT



(TSOP(II)-Forward Type)

Pin Name	Pin Function
A0 - A8	Address Inputs
DQ0 -15	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power (+5V)
	Power (+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM416V254B	KM416C254B	
I_{CC1}	Don't care	-5	-	110	mA
		-6	70	90	mA
		-7	65	80	mA
		-8	60	-	mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5	-	110	mA
		-6	70	90	mA
		-7	65	80	mA
		-8	60	-	mA
I_{CC4}	Don't care	-5	-	70	mA
		-6	60	60	mA
		-7	55	50	mA
		-8	50	-	mA
I_{CC5}	Normal	Don't care	0.5	1	mA
	L		100	150	µA
I_{CC6}	Don't care	-5	-	110	mA
		-6	70	90	mA
		-7	65	80	mA
		-8	60	-	mA
I_{CC7}	L	Don't care	200	300	µA
I_{CCS}	L	Don't care	100	200	µA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$= 0.2V

Din = Don't care, T_{RC}= 125µs, T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self refresh current

$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A8 = V_{CC}-0.2V or 0.2V,

DQ0 ~ DQ15= V_{CC}-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle time, tHPC.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A8]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		144		ns	
Read-modify-write cycle time	tRWC	116		140		165		190		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		17		17		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output Buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	3	20	ns	6, 13
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	17		17		20		20		ns	
$\overline{CAS}$ hold time	tCSH	40		50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	33	20	43	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	14
Column address hold time (5V)	tCAH	8		10		15		-		ns	14
Column address hold time (3.3V)	tCAH	-		15		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		10		10		ns	
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	17

Note) *1: 50ns product : Vcc=5V±5%, *2 : 3.3V only

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9,20
Data hold time (5V)	tDH	8		10		15		-		ns	9,20
Data hold time (3.3V)	tDH	-		15		15		15		ns	
Refresh period (Normal)	tREF		8		8		8		8	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	34		36		44		44		ns	7,16
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		94		104		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		49		59		64		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		69		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	18
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40		45	ns	3
Hyper Page mode cycle time	tHPC	20		25		30		35		ns	11
Hyper Page mode read-modify-write cycle time	tHPRWC	47		56		71		81		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		10		ns	15
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		15		20		20	ns	3
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	15	3	20	3	20	ns	6,13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	6
$\overline{W}$ to data delay	tWED	13		15		20		20		ns	
$\overline{OE}$ to CAS hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		µs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

Note) *1 : 50ns product : Vcc=5V±5%, *2 : 3.3V only

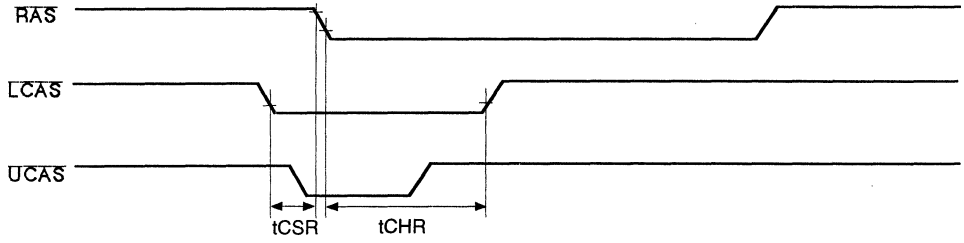
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 50pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. tASC ≥ 6ns, Assume tT=2.0ns.

KM416C/V254B/BL Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8 - DQ15	STATE
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

12. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 512 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (L-version).
13. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ going.
14. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
15. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
16. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
17. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge
18. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
19. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



20. tDS, tDH is independently specified for lower byte D_{IN}(0~7), upper byte D_{IN}(8~15).

512K x 8 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 524,288 x 8 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage(+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in Low power version.

This 512Kx8 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

It may be used as main memory unit for personal computer and portable machines.

FEATURES

- Part Identification
  - KM48C512D/DL (5V, 1K Ref.)
  - KM48V512D/DL (3.3V, 1K Ref.)

- Active power dissipation

Unit : mW

Speed	3.3V (1K Ref.)	5V (1K Ref.)
-5	-	470
-6	255	385
-7	235	360
-8	220	-

- Refresh cycles

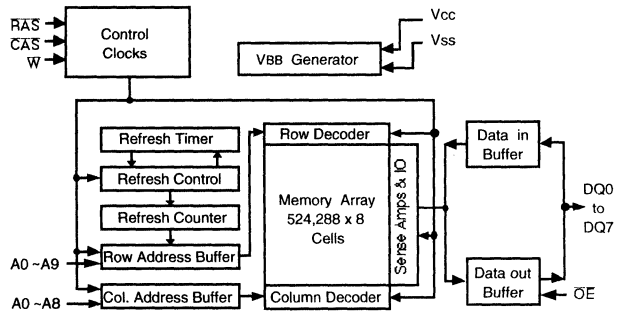
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
C512D	5V	1K	16ms	128ms
V512D	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	15ns	90ns	35ns	5V
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	3.3V

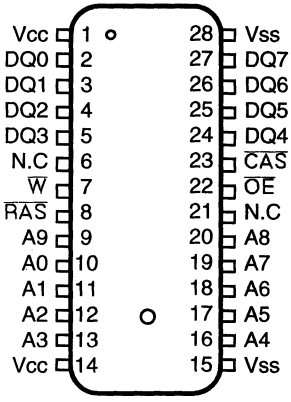
- Fast Page Mode operation
- Byte Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages

FUNCTIONAL BLOCK DIAGRAM



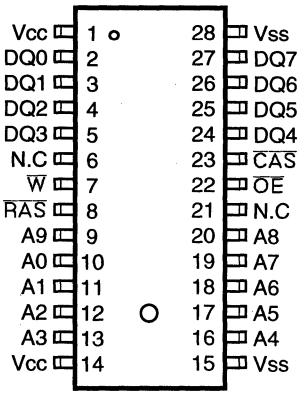
PIN CONFIGURATION (Top Views)

• KM48C/V512DJ



(SOJ)

• KM48C/V512DT



(TSOP-II)

Pin Name	Pin Function
A0 - A9	Address Inputs
DQ0 -7	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
Vcc	Power (+5V)
	Power (+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM48V512D	KM48C512D	
I_{CC1}	Don't care	-5	-	85	mA
		-6	70	70	mA
		-7	65	65	mA
		-8	60	-	mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5	-	85	mA
		-6	70	70	mA
		-7	65	65	mA
		-8	60	-	mA
I_{CC4}	Don't care	-5	-	65	mA
		-6	55	55	mA
		-7	50	50	mA
		-8	45	-	mA
I_{CC5}	Normal	Don't care	0.5	1	mA
	L		100	150	μA
I_{CC6}	Don't care	-5	-	85	mA
		-6	70	70	mA
		-7	65	65	mA
		-8	60	-	mA
I_{CC7}	L	Don't care	200	300	μA
I_{CCS}	L	Don't care	100	200	μA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V

Din = Don't care, T_{RC}=125μs, T_{RAS}=T_{RAS} min~300 ns

I_{CCS} : Self refresh current

$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A9 = Vcc-0.2V or 0.2V,

DQ0 ~ DQ7= Vcc-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 ~ A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0~ DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition (3.3V device): Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	135		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	35	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time (5V)	tCAH	10		10		15		15		ns	
Column address hold time (3.3V)	tCAH	-		15		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		10		10		ns	
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		20		ns	

Note) *1 : 5V only , *2 : 3.3V only

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time (5V)	tDH	10		10		15		-		ns	9
Data hold time (3.3V)	tDH	-		15		15		15		ns	9
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		40		50		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	75		85		95		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	50		55		60		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	55		60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		80		95		105		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	20	0	20	ns	6
$\overline{OE}$ command hold time	tOEH	15		15		20		20		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		µs	11
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	11
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	11

Note) *1 : 5V only , *2 : 3.3V only

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 1024 cycle of burst refresh must be executed within 16ms before and after self refresh in order to meet refresh specification (L-version).

512K x 8 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 524,288 x 8 bit Extended Data Out CMOS DRAMs. Extended Data Out offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in Low power version.

This 512Kx8 Extended Data Out DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

It may be used as main memory unit for personal computer and portable machines.

FEATURES

- Part Identification
  - KM48C514D/DL (5V, 1K Ref.)
  - KM48V514D/DL (3.3V, 1K Ref.)

- Active power dissipation

Unit : mW

Speed	3.3V (1K Ref.)	5V (1K Ref.)
-5	-	470
-6	255	385
-7	235	360
-8	220	-

- Refresh cycles

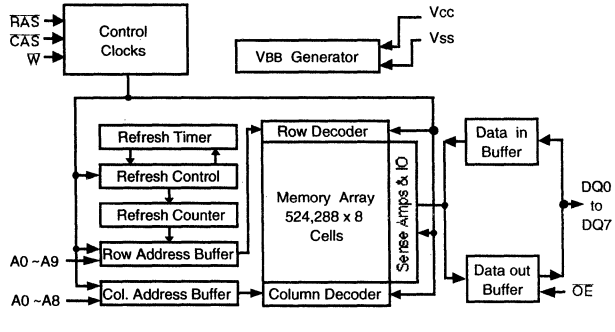
Part NO.	Vcc	Refresh cycle	Refresh Period	
			Normal	L
C514D	5V	1K	16ms	128ms
V514D	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tHPC	Remark
-5	50ns	15ns	84ns	20ns	5V Only
-6	60ns	15ns	104ns	25ns	5V/3.3V
-7	70ns	20ns	124ns	30ns	5V/3.3V
-8	80ns	20ns	144ns	35ns	3.3V Only

- Extended Data Out operation
- Byte Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages
- Dual +5V±10% power supply (5V product)
- Dual +3.3V±0.3V power supply (3.3V product)

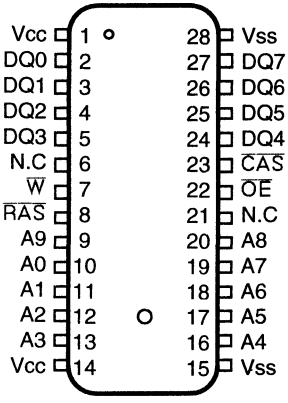
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

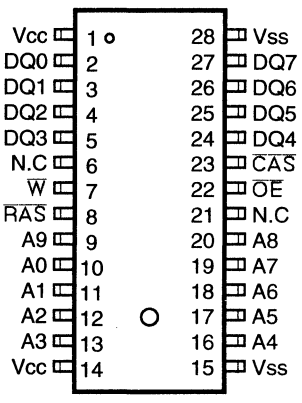
PIN CONFIGURATION (Top Views)

• KM48C/V514DJ



(SOJ)

• KM48C/V514DT



(TSOP-II)

Pin Name	Pin Function
A0 - A9	Address Inputs
DQ0 -7	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power (+5V)
	Power (+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM48V514D	KM48C514D	
I_{CC1}	Don't care	-5	-	85	mA
		-6	70	70	mA
		-7	65	65	mA
		-8	60	-	mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5	-	85	mA
		-6	70	70	mA
		-7	65	65	mA
		-8	60	-	mA
I_{CC4}	Don't care	-5	-	65	mA
		-6	55	55	mA
		-7	50	50	mA
		-8	45	-	mA
I_{CC5}	Normal	Don't care	0.5	1	mA
	L		100	150	µA
I_{CC6}	Don't care	-5	-	85	mA
		-6	70	70	mA
		-7	65	65	mA
		-8	60	-	mA
I_{CC7}	L	Don't care	200	300	µA
I_{CCS}	L	Don't care	100	200	µA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V

Din = Don't care, T_{RC}=125µs, T_{RAS}=T_{RAS} min~300 ns

I_{CCS} : Self refresh current

$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A9 = V_{CC}-0.2V or 0.2V,

DQ0 ~ DQ7 = V_{CC}-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle time, tHPC

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 ~ A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 ~ DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		144		ns	
Read-modify-write cycle time	tRWC	116		140		165		190		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	15	3	15	ns	6, 13
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	40		50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	11
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	35	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time (5V)	tCAH	8		10		15		-		ns	
Column address hold time (3.3V)	tCAH	-		15		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		10		10		ns	
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	

Note) *1 : 5V only , *2 : 3.3V only

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time (5V)	tDH	8		10		15		-		ns	9
Data hold time (3.3V)	tDH	-		15		15		15		ns	
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	34		36		44		44		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		94		104		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		49		59		64		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		69		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40		45	ns	3
Hyper Page mode cycle time	tHPC	20		25		30		35		ns	11
Hyper Page mode read-modify-write cycle time	tHPRWC	47		56		71		81		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		15		20		20	ns	3
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	6
$\overline{OE}$ to output in low-Z	tOLZ	3		3		3		3		ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	6, 13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	6
$\overline{W}$ to data delay	tWED	13		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width (hyper page cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		µs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

Note) *1 : 5V only , *2 : 3.3V only

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. tASC≥6ns, Assume tT=2.0ns.
12. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 1024 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (L-version).
13. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

256K x 16 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 262,144 x 16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in Low power version.

This 256Kx16 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

FEATURES

- Part Identification
  - KM416C256D/DL (5V, 512 Ref.)
  - KM416V256D/DL (3.3V, 512 Ref.)

- Active power dissipation

Unit : mW

Speed	3.3V (512 Ref.)	5V (512 Ref.)
-5	-	605
-6	325	495
-7	290	440
-8	270	-

- Refresh cycles

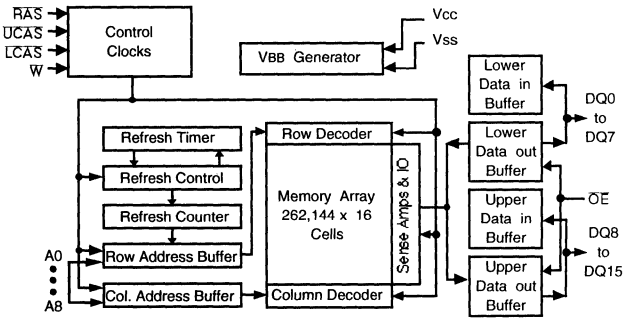
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
C256B	5V	512	8ms	128ms
V256B	3.3V			

- Performance range:

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	15ns	90ns	35ns	5V
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	3.3V

- Fast Page Mode operation
- 2 $\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages

FUNCTIONAL BLOCK DIAGRAM



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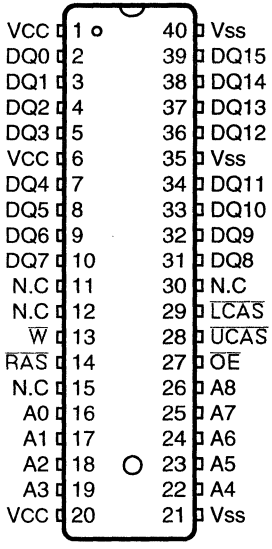
SAMSUNG ELECTRONICS

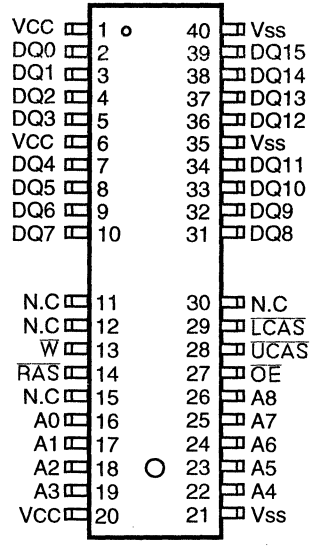
PIN CONFIGURATION (Top Views)

• KM416C/V256DJ



(SOJ)

• KM416C/V256DT



(TSOP-II)

Pin Name	Pin Function
A0 - A8	Address Inputs
DQ0 -15	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power (+5V)
	Power (+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM416V256D	KM416C256D	
I_{CC1}	Don't care	-5	-	110	mA
		-6	90	90	mA
		-7	80	80	mA
		-8	75	-	mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5	-	110	mA
		-6	90	90	mA
		-7	80	80	mA
		-8	75	-	mA
I_{CC4}	Don't care	-5	-	70	mA
		-6	60	60	mA
		-7	55	55	mA
		-8	50	-	mA
I_{CC5}	Normal	Don't care	0.5	1	mA
	L		100	150	μA
I_{CC6}	Don't care	-5	-	110	mA
		-6	90	90	mA
		-7	80	80	mA
		-8	75	-	mA
I_{CC7}	L	Don't care	200	300	μA
I_{CCS}	L	Don't care	100	200	μA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$, $\overline{LCAS}$= 0.2V

Din = Don't care, T_{RC}= 125μs, T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self refresh current

$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A8 = Vcc-0.2V or 0.2V,

DQ0 ~ DQ15= Vcc-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A8]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	135		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	35	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	12
Column address hold time (5V)	tCAH	10		10		15		15		ns	12
Column address hold time (3.3V)	tCAH	-		15		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		0		ns	
Write command hold time	tWCH	10		10		10		10		ns	
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		20		ns	15

Note) *1: 5V only , *2 : 3.3V only

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9, 18
Data hold time (5V)	tDH	10		10		15		-		ns	9, 18
Data hold time (3.3V)	tDH	-		15		15		15		ns	9
Refresh period (Normal)	tREF		8		8		8		8	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		40		50		50		ns	7,14
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	75		85		95		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	50		55		60		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	55		60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	16
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	17
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		80		95		105		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	13
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	20	0	20	ns	6
$\overline{OE}$ command hold time	tOEH	15		15		20		20		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		µs	11
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	11
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	11

Note) *1: 5V only , *2 : 3.3V only

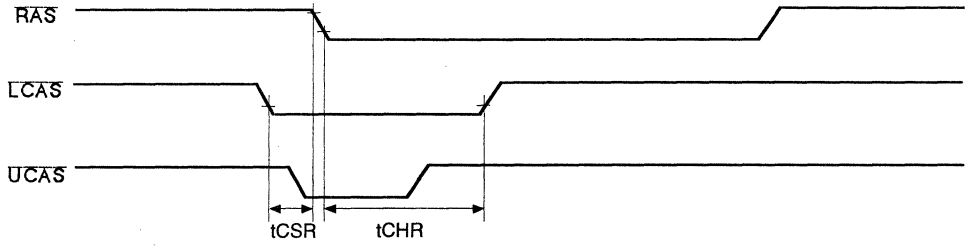
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 50pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

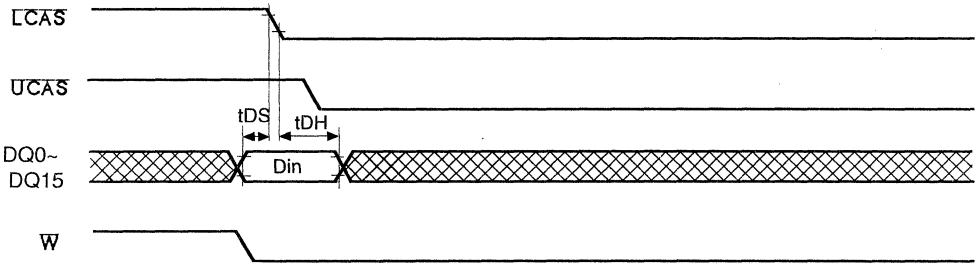
KM416C/V256D/DL Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8 - DQ15	STATE
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

11. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 512 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (L-version).
12. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
13. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
16. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
17. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



18. tDS, tDH are specified by the earlier $\overline{CAS}$ falling edge.



256K x 16 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 262,144 x 16 bit Extended Data Out CMOS DRAMs. Extended Data Out offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in Low power version.

This 256Kx16 Extended Data Out DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

FEATURES

- Part Identification
  - KM416C254D/DL (5V, 512 Ref.)
  - KM416V254D/DL (3.3V, 512 Ref.)

- Active power dissipation

Unit : mW

Speed	3.3V (512 Ref.)	5V (512 Ref.)
-5	-	605
-6	255	495
-7	235	440
-8	220	-

- Refresh cycles

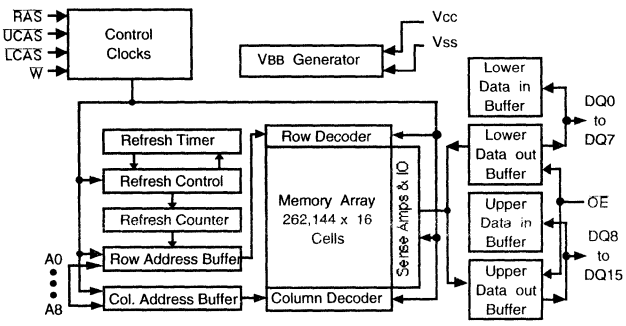
Part NO.	Vcc	Refresh cycle	Refresh Period	
			Normal	L
C254D	5V	512	8ms	128ms
V254D	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tHPC	Remark
-5	50ns	15ns	84ns	20ns	5V Only
-6	60ns	15ns	104ns	25ns	5V/3.3V
-7	70ns	20ns	124ns	30ns	5V/3.3V
-8	80ns	20ns	144ns	35ns	3.3V Only

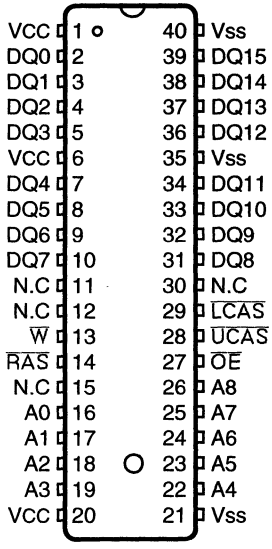
- Extended Data Out operation
- 2 $\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages
- Triple +5V±10% power supply (5V product)
- Triple +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM



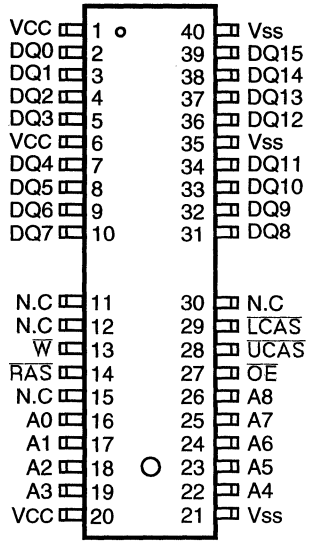
PIN CONFIGURATION (Top Views)

• KM416C/V254DJ



(SOJ)

• KM416C/V254DT



(TSOP-II)

Pin Name	Pin Function
A0 - A8	Address Inputs
DQ0 -15	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power (+5V)
	Power (+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM416V254D	KM416C254D	
I_{CC1}	Don't care	-5	-	110	mA
		-6	70	90	mA
		-7	65	80	mA
		-8	60	-	mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5	-	110	mA
		-6	70	90	mA
		-7	65	80	mA
		-8	60	-	mA
I_{CC4}	Don't care	-5	-	70	mA
		-6	60	60	mA
		-7	55	50	mA
		-8	50	-	mA
I_{CC5}	Normal	Don't care	0.5	1	mA
	L		100	150	µA
I_{CC6}	Don't care	-5	-	110	mA
		-6	70	90	mA
		-7	65	80	mA
		-8	60	-	mA
I_{CC7}	L	Don't care	200	300	µA
I_{CCS}	L	Don't care	100	200	µA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$= 0.2V

Din = Don't care, T_{RC}= 125µs, T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self refresh current

$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A8 = Vcc-0.2V or 0.2V,

DQ0 ~ DQ15= Vcc-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle time, tHPC.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A8]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$,$\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		144		ns	
Read-modify-write cycle time	tRWC	116		140		165		190		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output Buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	3	20	ns	6, 13
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	40		50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	35	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	14
Column address hold time (5V)	tCAH	8		10		15		-		ns	14
Column address hold time (3.3V)	tCAH	-		15		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		10		10		ns	
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	17

Note) *1: 5V only , *2 : 3.3V only

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9, 20
Data hold time (5V)	tDH	8		10		15		-		ns	9, 20
Data hold time (3.3V)	tDH	-		15		15		15		ns	
Refresh period (Normal)	tREF		8		8		8		8	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	34		36		44		44		ns	7,16
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		94		104		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		49		59		64		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		69		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	18
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40		45	ns	3
Hyper Page mode cycle time	tHPC	20		25		30		35		ns	11
Hyper Page mode read-modify-write cycle time	tHPRWC	47		56		71		81		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		10		ns	15
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		15		20		20	ns	3
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	15	3	20	3	20	ns	6,13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	6
$\overline{W}$ to data delay	tWED	13		15		20		20		ns	
$\overline{OE}$ to CAS hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		µs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

Note) *1: 5V only , *2 : 3.3V only

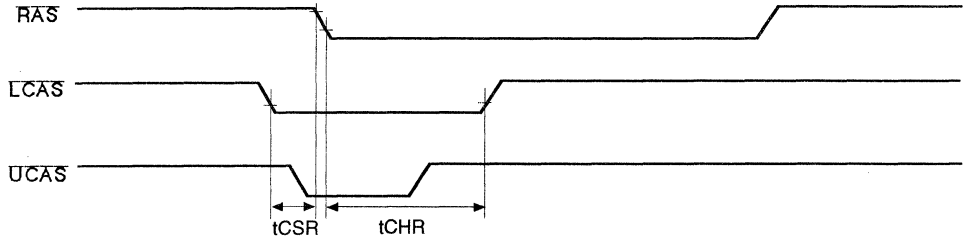
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 50pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. tASC ≥ 6ns, Assume tT=2.0ns.

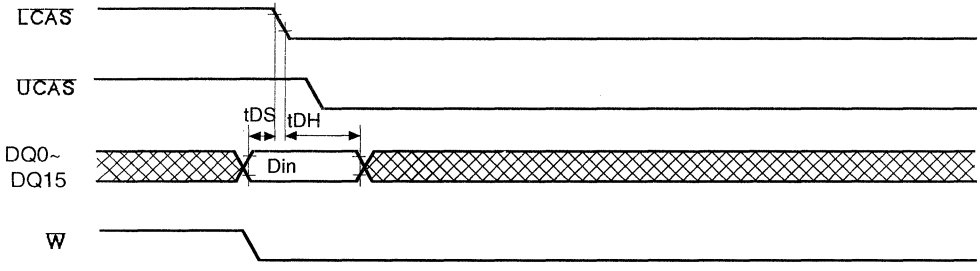
KM416C/V254D/DL Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8 - DQ15	STATE
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

12. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 512 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (L-version).
13. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ going.
14. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
15. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
16. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
17. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge
18. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
19. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



20. tDS, tDH are specified by the earlier $\overline{CAS}$ falling edge.



16M DRAM

- KM41C16000B
  KM41V16000B
- KM44C4000B, KM44C4100B
  KM44V4000B, KM44V4100B
- KM44C4003B, KM44C4103B
- KM44C4004B, KM44C4104B
  KM44V4004B, KM44V4104B
- KM44C4005B, KM44C4105B
- KM48C2000B, KM48C2100B
  KM48V2000B, KM48V2100B
- KM48C2004B, KM48C2104B
  KM48V2004B, KM48V2104B
- KM416C1000A, KM416C1200A
  KM416V1000A, KM416V1200A
- KM416C1004A, KM416C1204A
  KM416V1004A, KM416V1204A
- KM416C1000B, KM416C1200B
  KM416V1000B, KM416V1200B
- KM416C1004B, KM416C1204B
  KM416V1004B, KM416V2104B

16M x 1 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 16,777,216 x 1 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal, Low power) and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in L-version.

This 16Mx1 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for high level computer and microcomputer.

FEATURES

- Part Identification
  - KM41C16000B/B-L (5V, 4K Ref.)
  - KM41V16000B/B-L (3.3V, 4K Ref.)

- Active Power Dissipation

Unit : mW

Speed	3.3V	5V
-5	-	495
-6	288	440
-7	252	385
-8	216	-

- Refresh cycles

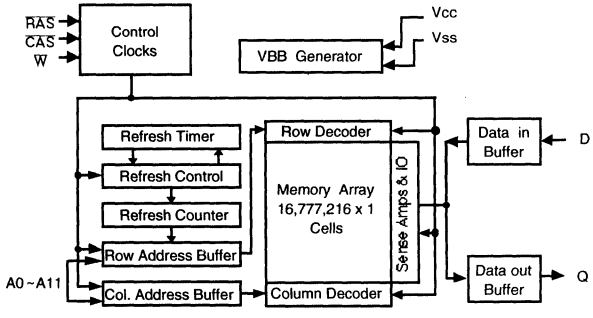
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
C16000B	5V	4K	64ms	128ms
V16000B	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	13ns	90ns	35ns	5V
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	3.3V

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver)
- Fast parallel test mode capability
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM



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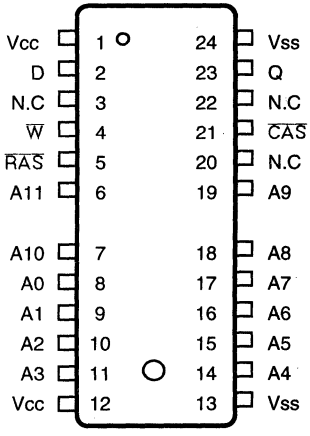
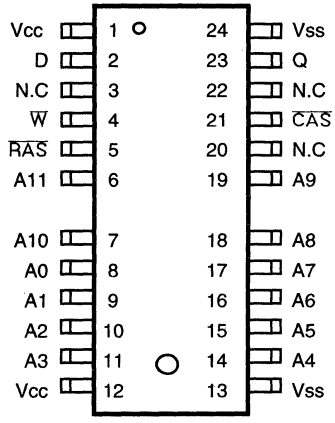
SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top Views)

• KM41C/V16000BK



• KM41C/V16000BS



K : 300 mil 26(24) SOJ

S : 300 mil 26(24) TSOP II

Pin Name	Pin Function
A0 - A11	Address Inputs
D	Data in
Q	Data out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5.0V)
	Power (+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM41V16000B	KM41C16000B	
I_{CC1}	Don't care	-5	-	90	mA
		-6	80	80	mA
		-7	70	70	mA
		-8	60	-	mA
I_{CC2}	Normal	Don't care	1	2	mA
	L		1	1	mA
I_{CC3}	Don't care	-5	-	90	mA
		-6	80	80	mA
		-7	70	70	mA
		-8	60	-	mA
I_{CC4}	Don't care	-5	-	80	mA
		-6	70	70	mA
		-7	60	60	mA
		-8	50	-	mA
I_{CC5}	Normal	Don't care	0.5	1	mA
	L		0.3	0.3	mA
I_{CC6}	Don't care	-5	-	90	mA
		-6	80	80	mA
		-7	70	70	mA
		-8	60	-	mA
I_{CC7}	L	Don't care	450	450	μA
I_{CCS}	L	Don't care	250	300	μA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V

Din = Don't care, T_{RC}= 31.25μs(L-ver), T_{RAS}=T_{RAS}min ~ 300ns

I_{CCS} : Self Refresh Current

$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=A0 ~ A11 = V_{CC}-0.2V or 0.2V, D,Q = V_{CC}-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [D]	C_{IN1}	-	7	pF
Input capacitance [A0 - A11]	C_{IN2}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$]	C_{IN3}	-	7	pF
Output Capacitance [Q]	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition(3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	110		130		155		175		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4
Access time from column address	tAA		25		30		35		40	ns	3,9
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	5
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	7
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		15		15		ns	
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	

Note) *1 : 5V only, *2 : 3.3V only

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, Vih/Vil=2.4/0.8V, Voh/Vol =2.4/0.4V
Test condition(3.3V device) : Vcc=3.3V±0.3V, Vih/Vil=2.0/0.8V, Voh/Vol =2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	8
Data hold time	tDH	10		10		15		15		ns	8
Refresh period (Normal)	tREF		64		64		64		64	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	6
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	13		15		20		20		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	50		60		70		80		ns	6
Column address to $\overline{W}$ delay time	tAWD	25		30		35		40		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	30		35		40		45		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	53		60		70		80		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	10
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	10
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		us	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

Note) *1 : 5V only, *2 : 3.3V only

TEST MODE CYCLE

(Note. 10, 11)

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	115		135		160		180		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4
Access time from column address	tAA		30		35		40		45	ns	3,9
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	18		20		25		25		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	55		65		75		85		ns	6
Column address to $\overline{W}$ delay time	tAWD	30		35		40		45		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	35		40		45		50		ns	6
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	58		65		75		85		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3

Note) *1 : 5V only, *2 : 3.3V only

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
6. tWCS, tRWD, tCWD, tAWD and tCPWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥tCWD(min), tRWD≥tRWD(min), tAWD≥tAWD(min) and tCPWD≥tCPWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{CAS}$ falling edge in early write cycles and to the $\overline{W}$ falling edge in read-modify-write cycles.
9. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
10. These specifications are applied in the test mode.
11. In test mode read cycle, the values of tRAC, tAA and tCAC are delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding 5ns to the specified value in this data sheet.
12. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 4096 cycles of burst refresh must be executed within 16ms before and after self refresh in order to meet refresh specification.

4M x 4 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 4,194,304 x 4 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), refresh cycle (2K Ref. or 4K Ref.), access time (-5, -6, -7 or -8), power consumption (Normal, Low power) and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in L-version.

This 4Mx4 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for high level computer, microcomputer and personal computer.

FEATURES

- Part Identification
  - KM44C4000B/B-L (5V, 4K Ref.)
  - KM44C4100B/B-L (5V, 2K Ref.)
  - KM44V4000B/B-L (3.3V, 4K Ref.)
  - KM44V4100B/B-L (3.3V, 2K Ref.)

- Active Power Dissipation Unit : mW

Speed	3.3V		5V	
	4K	2K	4K	2K
-5	-	-	495	605
-6	288	360	440	550
-7	252	324	385	495
-8	216	288	-	-

- Refresh cycles

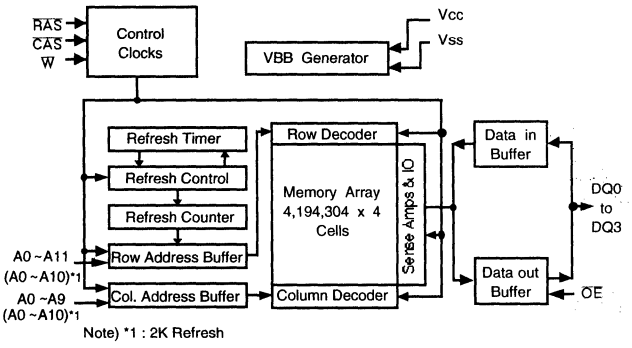
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
C4000B	5V	4K	64ms	128ms
V4000B	3.3V			
C4100B	5V	2K	32ms	
V4100B	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	13ns	90ns	35ns	5V
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	3.3V

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver)
- Fast parallel test mode capability
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM

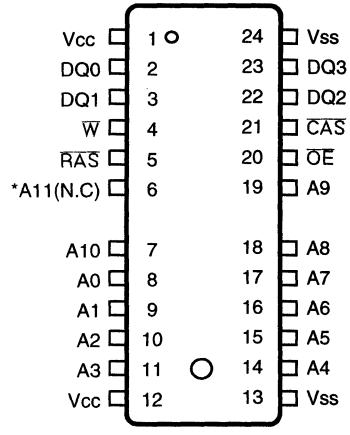


Note) *1 : 2K Refresh

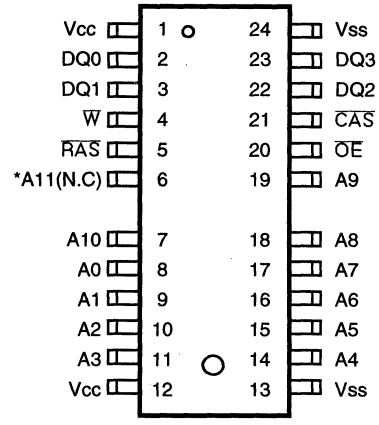
SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top Views)

• KM44C/V40(1)00BK



• KM44C/V40(1)00BS



* A11 is N.C for KM44C/V4100B (5V/3.3V, 2K Ref. product)

K : 300mil 26(24) SOJ
S : 300mil 26(24) TSOP II

Pin Name	Pin Function
A0 - A11	Address Inputs (4K Product)
A0 - A10	Address Inputs (2K Product)
DQ0 -3	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power (+5.0V)
	Power (+3.3V)
N.C	No Connection (2K Ref. product)

ABSOLUTE MAXIMUM RATINGS *

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max				Units
			KM44V4000B	KM44V4100B	KM44C4000B	KM44C4100B	
I_{CC1}	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	-	-	mA
I_{CC2}	Normal	Don't care	1	1	2	2	mA
	L		1	1	1	1	mA
I_{CC3}	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	-	-	mA
I_{CC4}	Don't care	-5	-	-	80	90	mA
		-6	70	80	70	80	mA
		-7	60	70	60	70	mA
		-8	50	60	-	-	mA
I_{CC5}	Normal	Don't care	0.5	0.5	1	1	mA
	L		0.3	0.3	0.3	0.3	mA
I_{CC6}	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	-	-	mA
I_{CC7}	L	Don't care	450	400	450	400	μA
I_{CCS}	L	Don't care	250	250	300	300	μA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V
Din = Don't care, T_{RC}= 31.25μs(4K/L-ver), 62.5μs(2K/L-ver)
T_{RAS}=T_{RAS}min~300ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = Vcc-0.2V or 0.2V, DQ0 ~ DQ3= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition(5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition(3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4
Access time from column address	tAA		25		30		35		40	ns	3,9
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	5
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	7
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		15		15		ns	
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	

Note) *1 : 5V only, *2 : 3.3V only

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Test condition (5V device) : V_{CC}=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition(3.3V device) : V_{CC}=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	8
Data hold time	tDH	10		10		15		15		ns	8
Refresh period (2K, Normal)	tREF		32		32		32		32	ms	
Refresh period (4K, Normal)	tREF		64		64		64		64	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	6
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	6
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		75		ns	6
$\overline{CAS}$ set-up time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	10
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	10
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		us	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

Note) *1 : 5V only, *2 : 3.3V only

TEST MODE CYCLE

(Note. 10, 11)

Parameter	Symbol	-5 *1		-6		-7		-8 *2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4
Access time from column address	tAA		30		35		40		45	ns	3,9
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	6
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	58		65		75		80		ns	6
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

Note) *1 : 5V only, *2: 3.3V only

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
6. tWCS, tRWD, tCWD, tAWD and tCPWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥tCWD(min), tRWD≥tRWD(min), tAWD≥tAWD(min) and tCPWD≥tCPWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{CAS}$ falling edge in early write cycles and to the $\overline{W}$ falling edge in read-modify-write cycles.
9. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
10. These specifications are applied in the test mode.
11. In test mode read cycle, the values of tRAC, tAA and tCAC are delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding 5ns to the specified value in this data sheet.
12. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 4096(4K Ref.)/2048(2K Ref.) cycles of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.

4M x 4 Bit CMOS Quad CAS DRAM with Fast Page Mode

DESCRIPTION

This is a family of 4,194,304 x 4bit Quad $\overline{CAS}$ with Fast Page Mode DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle (2K Ref. or 4K Ref.), access time (-5, -6 or -7), power consumption (Normal, Low power) and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in L-version. Four seperate $\overline{CAS}$ pins provide for seperate I/O operation allowing this device to operate in parity mode.

This 4Mx4 Fast Page mode Quad $\overline{CAS}$ DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM44C4003B/B-L (5V, 4K Ref.)
  - KM44C4103B/B-L (5V, 2K Ref.)

- Active Power Dissipation Unit : mW

Speed	Refresh Cycle	
	4K	2K
-5	495	605
-6	440	550
-7	385	495

- Refresh cycles

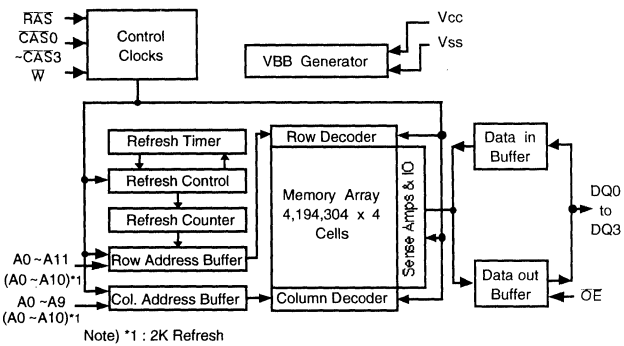
Part NO.	Refresh cycle	Refresh period	
		Normal	L
C4003B	4K	64ms	128ms
C4103B	2K	32ms	

- Performance range

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns

- Fast Page Mode operation
- Four separate $\overline{CAS}$ pins provide for separate I/O operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver)
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 2K Refresh

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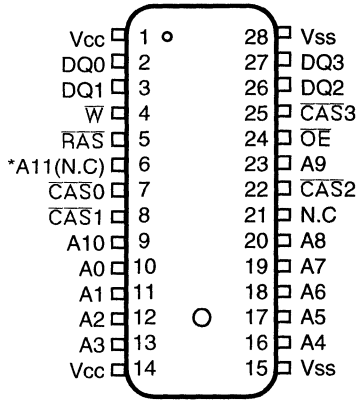
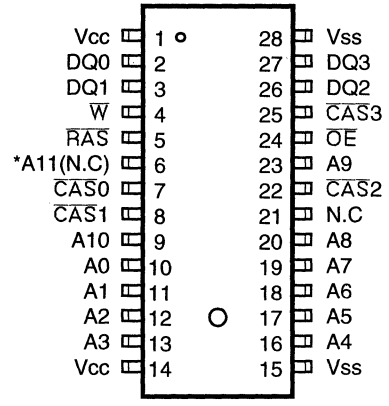
SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top Views)

• KM44C40(1)03BK



• KM44C40(1)03BS



* A11 is N.C for KM44C4103B (5V, 2K Ref. product)

K : 300mil 28 SOJ

S : 300mil 28 TSOP II

Pin Name	Pin Function
A0 ~ A11	Address Inputs (4K product)
A0 ~ A10	Address Inputs (2K product)
DQ0 ~ 3	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS0~CAS3	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
Vcc	Power (+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V /20ns, Pulse width is measured at Vcc.
*2 : - 2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM44C4003B	KM44C4103B	
I_{CC1}	Don't care	-5 -6 -7	90 80 70	110 100 90	mA mA mA
I_{CC2}	Normal L	Don't care	2 1	2 1	mA mA
I_{CC3}	Don't care	-5 -6 -7	90 80 70	110 100 90	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	80 70 60	90 80 70	mA mA mA
I_{CC5}	Normal L	Don't care	1 300	1 300	mA μA
I_{CC6}	Don't care	-5 -6 -7	90 80 70	110 100 90	mA mA mA
I_{CC7}	L	Don't care	450	400	μA
I_{CCS}	L	Don't care	300	300	μA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Static Column Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V
Din = Don't care, T_{RC}= 31.25μs (4K/L-ver), 62.5μs (2K/L-ver)
T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = Vcc-0.2V or 0.2V, DQ0 ~ DQ3= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE (T_A=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$x, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	133		155		185		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,16
Access time from column address	tAA		25		30		35	ns	3,9
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3,16
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	ns	5
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	14
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	15
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	22
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4,14
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	15
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	14
Column address hold time	tCAH	10		10		15		ns	14
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	14
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	7,15
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	7
Write command hold time	tWCH	10		10		15		ns	22
Write command pulse width	tWP	10		10		55		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		ns	15

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Test condition : V_{cc}=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	8
Data hold time	tDH	10		10		15		ns	8
Refresh period(2K, Normal)	tREF		32		32		32	ms	
Refresh period(4K, Normal)	tREF		64		64		64	ms	
Refresh period(L -ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	6,14
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		ns	6,14
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		ns	6
Column address to $\overline{W}$ delay time	tAWD	48		55		65		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		ns	6
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	14
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	15
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	3,16
Fast Page mode cycle time	tPC	35		40		45		ns	17
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		ns	17
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	18
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	19
$\overline{OE}$ to data delay	tOED	13		15		20		ns	20
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	ns	5
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	10
Write command hold time (Test mode in)	tWTH	10		10		10		ns	10
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	12
Hold time $\overline{CAS}$ low to $\overline{CAS}$ high	tCLCH	5		5		5		ns	13,23

TEST MODE CYCLE

(Note. 10, 11)

Parameter	Symbol	-5		-6		-7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		ns	
Read-modify-write cycle time	tRWC	138		160		190		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4
Access time from column address	tAA		30		35		40	ns	3,9
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		ns	6
Column address to $\overline{W}$ delay time	tAWD	53		60		70		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	58		65		75		ns	6
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
6. tWCS, tRWD, tCWD, tAWD and tCPWD are non restrictive operating parameters. They are included in thedata sheet as electric characteristics only. If tWCS≥tWCS(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥tCWD(min), tRWD≥tRWD(min), tAWD≥tAWD(min) and tCPWD≥tCPWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{CAS}$ falling edge in early write cycles and to the $\overline{W}$ falling edge in read-modify-write cycles.
9. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
10. These specifications are applied in the test mode.
11. In test mode read cycle, the values of tRAC, tAA and tCAC are delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding 5ns to the specified value in this data sheet.
12. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 4096(4K Ref.)/2048(2K Ref.) cycles of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.
13. In order to hold the address latched by the first $\overline{CAS}$ going low, the parameter tCLCH must be met.
14. The first falling $\overline{CAS}$x edge to go low.
15. The last rising $\overline{CAS}$x edge to go high.
16. Output parameter is referenced to corresponding $\overline{CAS}$x input.
17. The last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
18. The last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
19. The first DQx controlled by the first $\overline{CAS}$x to go low.
20. The last DQx controlled by the last $\overline{CAS}$x to go high.
21. Each $\overline{CAS}$x must meet minimum pulse width.
22. The last $\overline{CAS}$x to go low.
23. The last falling $\overline{CAS}$x edge to the first rising $\overline{CAS}$x edge.

4M x 4 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 4,194,304 x 4 bit Extended Data Out CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Power supply voltage (+5.0V or +3.3V), refresh cycle (2K Ref. or 4K Ref.), access time (-5, -6, -7 or -8), power consumption (Normal, Low power) and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in L-version.

This 4Mx4 EDO DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for high level computer, microcomputer and personal computer.

FEATURES

- Part Identification
  - KM44C4004B/B-L (5V, 4K Ref.)
  - KM44C4104B/B-L (5V, 2K Ref.)
  - KM44V4004B/B-L (3.3V, 4K Ref.)
  - KM44V4104B/B-L (3.3V, 2K Ref.)

- Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	2K	4K	2K
-5	-	-	495	605
-6	288	360	440	550
-7	252	324	385	495
-8	216	288	-	-

- Refresh cycles

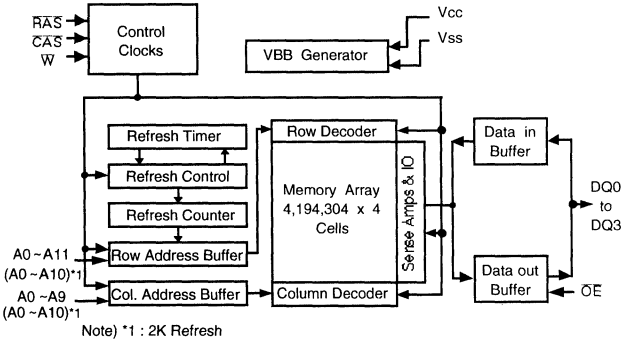
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
C4004B	5V	4K	64ms	128ms
V4004B	3.3V			
C4104B	5V	2K	32ms	
V4104B	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tHPC	Remark
-5	50ns	13ns	84ns	20ns	5V
-6	60ns	15ns	104ns	25ns	5V/3.3V
-7	70ns	20ns	124ns	30ns	5V/3.3V
-8	80ns	20ns	144ns	35ns	3.3V

- Extended Data Out mode operation (Fast Page Mode with Extended Data Out)
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver)
- Fast parallel test mode capability
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM



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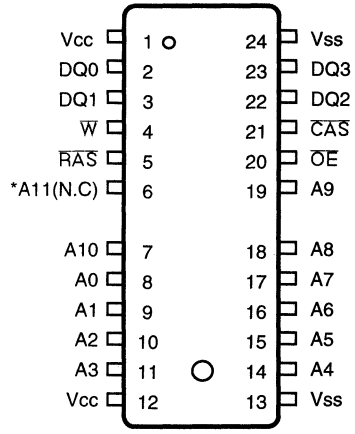
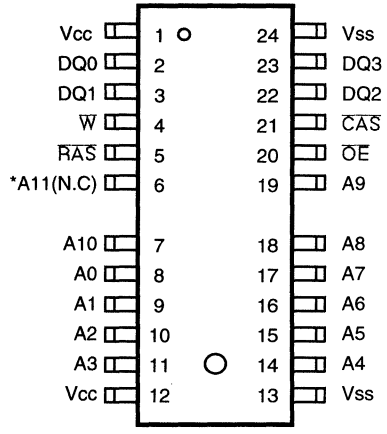
SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top Views)

• KM44C/V40(1)04BK



• KM44C/V40(1)04BS



* A11 is N.C for KM44C/V4104B (5V/3.3V, 2K Ref. product)

K : 300mil 26(24) SOJ

S : 300mil 26(24) TSOP II

Pin Name	Pin Function
A0 ~ A11	Address Inputs (4K Product)
A0 ~ A10	Address Inputs (2K Product)
DQ0 ~ 3	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power (+5.0V)
	Power (+3.3V)
N.C	No Connection (2K Ref. product)

ABSOLUTE MAXIMUM RATINGS *

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max				Units
			KM44V4004B	KM44V4104B	KM44C4004B	KM44C4104B	
I_{CC1}	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	-	-	mA
I_{CC2}	Normal	Don't care	1	1	2	2	mA
	L		1	1	1	1	mA
I_{CC3}	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	-	-	mA
I_{CC4}	Don't care	-5	-	-	100	110	mA
		-6	90	100	90	100	mA
		-7	80	90	80	90	mA
		-8	70	80	-	-	mA
I_{CC5}	Normal	Don't care	0.5	0.5	1	1	mA
	L		0.3	0.3	0.3	0.3	mA
I_{CC6}	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	-	-	mA
I_{CC7}	L	Don't care	450	400	450	400	µA
I_{CCS}	L	Don't care	250	250	300	300	µA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V
Din = Don't care, T_{RC}= 31.25µs(4K/L-ver), 62.5µs(2K/L-ver),
T_{RAS}=T_{RAS}min~300ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = V_{CC}-0.2V or 0.2V, DQ0 ~ DQ3= V_{CC}-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle time, tHPC.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		144		ns	
Read-modify-write cycle time	tRWC	116		140		170		190		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4
Access time from column address	tAA		25		30		35		40	ns	3,9
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	3	20	ns	5,13
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		3		ns	3
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	38		45		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	7
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		15		15		ns	
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	

Note) *1 : 5V only, *2 : 3.3V only

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Test condition (5V device) : V_{CC}=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : V_{CC}=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8 *2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	8
Data hold time	tDH	8		10		15		15		ns	8
Refresh period(2K, Normal)	tREF		32		32		32		32	ms	
Refresh period(4K, Normal)	tREF		64		64		64		64	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	6
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	30		34		44		44		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		94		104		ns	6
Column address to $\overline{W}$ delay time	tAWD	42		49		59		64		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	47		54		64		69		ns	6
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		25		30		35		ns	14
Hyper Page read-modify-write cycle time	tHPRWC	47		56		71		81		ns	14
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	5
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	10
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	10
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	5,13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	5
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulth width (Hyper Page Cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		us	12

Note) *1 : 5V only, *2 : 3.3V only

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Test condition (5V device) : V_{CC}=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : V_{CC}=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

TEST MODE CYCLE

(Note. 10, 11)

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	89		109		129		149		ns	
Read-modify-write cycle time	tRWC	121		145		175		195		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4
Access time from column address	tAA		30		35		40		45	ns	3,9
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	43		50		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	35		39		49		49		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	72		84		99		109		ns	6
Column address to $\overline{W}$ delay time	tAWD	47		54		64		69		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	52		59		69		74		ns	6
Hyper Page cycle time	tHPC	25		30		35		40		ns	14
Hyper page read-modify-write cycle time	tHPRWC	53		61		76		86		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		33		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

Note) *1 : 5V only, *2 : 3.3V only

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
6. tWCS, tRWD, tCWD, tAWD and tCPWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥tCWD(min), tRWD≥tRWD(min), tAWD≥tAWD(min) and tCPWD≥tCPWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{CAS}$ falling edge in early write cycles and to the $\overline{W}$ falling edge in read-modify-write cycles.
9. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
10. These specifications are applied in the test mode.
11. In test mode read cycle, the values of tRAC, tAA and tCAC are delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding 5ns to the specified value in this data sheet.
12. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 4096(4K Ref.)/2048(2K Ref.) cycles of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.
13. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
14. tASC ≥ 6ns , Assume tT = 2.0 ns

4M x 4 Bit CMOS Quad CAS DRAM with Extended Data Out

DESCRIPTION

This is a family of 4,194,304 x 4bit Quad $\overline{CAS}$ with Extended Data Out Mode DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Refresh cycle (2K Ref. or 4K Ref.), access time (-5, -6 or -7), power consumption (Normal, Low power) and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in L-version. Four seperate $\overline{CAS}$ pins provide for seperate I/O operation allowing this device to operate in parity mode.

This 4Mx4 Extended Data Out Quad $\overline{CAS}$ DRAM family is fabricated using Samsung's advanced CMOS process to realize high bandwidth, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM44C4005B/B-L (5V, 4K Ref.)
  - KM44C4105B/B-L (5V, 2K Ref.)

- Active Power Dissipation Unit : mW

Speed	Refresh Cycle	
	4K	2K
-5	495	605
-6	440	550
-7	385	495

- Refresh cycles

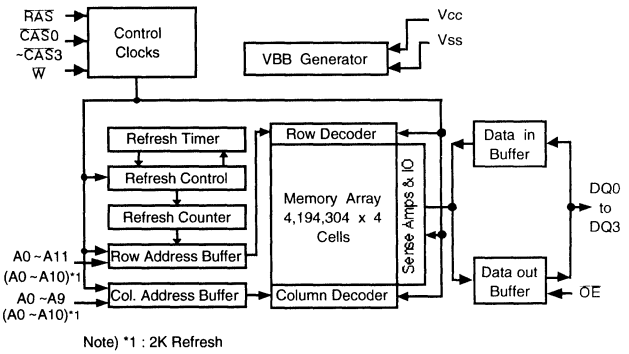
Part NO.	Refresh cycle	Refresh period	
		Normal	L
C4005B	4K	64ms	128ms
C4105B	2K	32ms	

- Performance range

Speed	tRAC	tCAC	tRC	tHPC
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns
-7	70ns	20ns	124ns	30ns

- Extended Data Out mode operation (Fast Page Mode with Extended Data Out)
- Four seperate $\overline{CAS}$ pins provide for seperate I/O operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver)
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply

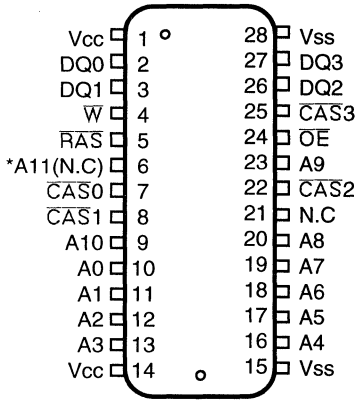
FUNCTIONAL BLOCK DIAGRAM



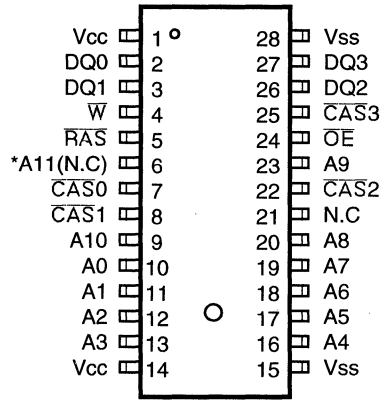
Note) *1 : 2K Refresh

PIN CONFIGURATION (Top Views)

• KM44C40(1)05BK



• KM44C40(1)05BS



* A11 is N.C for KM44C4105B (5V, 2K Ref. product)

K : 300mil 28 SOJ

S : 300mil 28 TSOP II

Pin Name	Pin Function
A0 ~ A11	Address Inputs (4K product)
A0 ~ A10	Address Inputs (2K product)
DQ0 ~ 3	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power (+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1 *1	V
Input Low Voltage	V_{IL}	-1.0 *2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.
*2 : - 2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM44C4005B	KM44C4105B	
I_{CC1}	Don't care	-5 -6 -7	90 80 70	110 100 90	mA mA mA
I_{CC2}	Normal L	Don't care	2 1	2 1	mA mA
I_{CC3}	Don't care	-5 -6 -7	90 80 70	110 100 90	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	80 70 60	90 80 70	mA mA mA
I_{CC5}	Normal L	Don't care	1 300	1 300	mA μA
I_{CC6}	Don't care	-5 -6 -7	90 80 70	110 100 90	mA mA mA
I_{CC7}	L	Don't care	450	400	μA
I_{CCS}	L	Don't care	300	300	μA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V

Din = Don't care, T_{RC}= 31.25μs (4K/L-ver), 62.5μs (2K/L-ver)

T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current

$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = Vcc-0.2V or 0.2V, DQ0 ~ DQ3= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle time, tHPC.

CAPATANCE (T_A=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$x, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1, 2)

Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		ns	
Read-modify-write cycle time	tRWC	106		140		170		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,18
Access time from column address	tAA		25		30		35	ns	3,9
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3,18
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	ns	5,13
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	16
$\overline{CAS}$ hold time	tCSH	38		45		50		ns	17
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4,16
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	17
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	14
Column address hold time	tCAH	8		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	7,17
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	7
Write command hold time	tWCH	10		10		15		ns	24
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		ns	17
Data set-up time	tDS	0		0		0		ns	8
Data hold time	tDH	8		10		15		ns	8

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1, 2)

Test condition : Vcc=5.0V±10%, Vih/Vil=2.4/0.8V, Voh/Vol=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Refresh period (2K, Normal)	tREF		32		32		32	ms	
Refresh period (4K, Normal)	tREF		64		64		64	ms	
Refresh period (L-ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	6,16
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	30		34		44		ns	6,16
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		94		ns	6
Column address to $\overline{W}$ delay time	tAWD	42		49		59		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	47		54		64		ns	6
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	16
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	17
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}B\overline{R}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40	ns	3,16
Hyper Page cycle time	tHPC	20		24		29		ns	14,19
Hyper Page read-modify-write cycle time	tHPRWC	62		71		86		ns	14,19
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		ns	20
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	21
$\overline{OE}$ to data delay	tOED	13		15		20		ns	22
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	ns	5
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	10
Write command hold time (Test mode in)	tWTH	10		10		10		ns	10
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	ns	5,13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	ns	5
$\overline{W}$ to data delay	tWED	15		15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulth width(Hyper Page Cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	12
Hold time $\overline{CAS}$ low to $\overline{CAS}$ high	tCLCH	5		5		5		ns	15,25

TEST MODE CYCLE

(Note. 10, 11)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	89		109		129		ns	
Read-modify-write cycle time	tRWC	121		145		175		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4
Access time from column address	tAA		30		35		40	ns	3,9
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	43		50		55		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	35		39		49		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	72		84		99		ns	6
Column address to $\overline{W}$ delay time	tAWD	47		54		64		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	52		59		69		ns	6
Hyper Page cycle time	tHPC	25		30		35		ns	
Hyper page read-modify-write cycle time	tHPRWC	52		61		76		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		33		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR **or** CBR cycles beforeproper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
6. tWCS, tRWD, tCWD, tAWD and tCPWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min), tAWD≥tAWD(min) and tCPWD≥tCPWD(min) then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{CAS}$ falling edge in early write cycles and to the $\overline{W}$ falling edge in read-modify-write cycles.
9. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
10. These specifications are applied in the test mode.
11. In test mode read cycle, the values of tRAC, tAA and tCAC are delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding 5ns to the specified value in this data sheet.
12. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 4096(4K Ref.)/2048(2K Ref.) cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
13. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
14. tASC ≥ 6ns, Assume tT=2.0 ns
15. In order to hold the address latched by the first $\overline{CAS}$ going low, the parameter tCLCH must be met.
16. The first $\overline{CAS}$x edge to transition low.
17. The last $\overline{CAS}$x edge to transition high.
18. Output parameter is referenced to corresponding $\overline{CAS}$x input.
19. The last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
20. The last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
21. The first DQx controlled by the first $\overline{CAS}$x to go low.
22. The last DQx controlled by the last $\overline{CAS}$x to go high.
23. Each $\overline{CAS}$x must meet minimum pulse width.
24. The last $\overline{CAS}$x to go low.
25. The last falling $\overline{CAS}$x edge to the first rising $\overline{CAS}$x edge.

2M x 8 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 2,097,152 x 8 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), refresh cycle (2K Ref. or 4K Ref.), access time (-5, -6, -7 or -8), power consumption (Normal, Low power) and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in L-version.

This 2Mx8 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for high level computer, microcomputer and personal computer.

2

FEATURES

- Part Identification
  - KM48C2000B/B-L (5V, 4K Ref.)
  - KM48C2100B/B-L (5V, 2K Ref.)
  - KM48V2000B/B-L (3.3V, 4K Ref.)
  - KM48V2100B/B-L (3.3V, 2K Ref.)

- Active Power Dissipation Unit : mW

Speed	3.3V		5V	
	4K	2K	4K	2K
-5	-	-	495	605
-6	288	360	440	550
-7	252	324	385	495
-8	216	288	-	-

- Refresh cycles

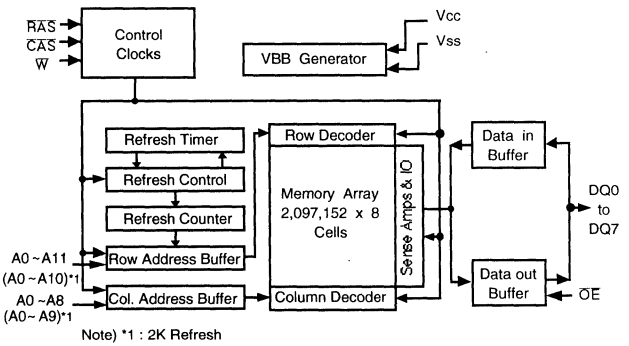
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
C2000B	5V	4K	64ms	128ms
V2000B	3.3V			
C2100B	5V	2K	32ms	
V2100B	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	13ns	90ns	35ns	5V
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	3.3V

- Fast Page Mode operation
- Byte Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver)
- Fast parallel test mode capability
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM

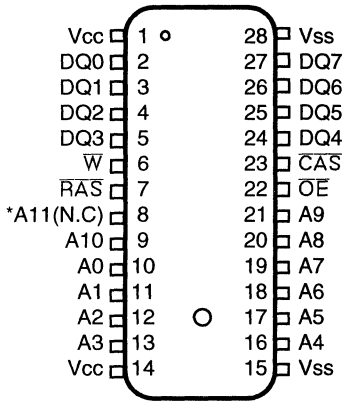


Note) *1 : 2K Refresh

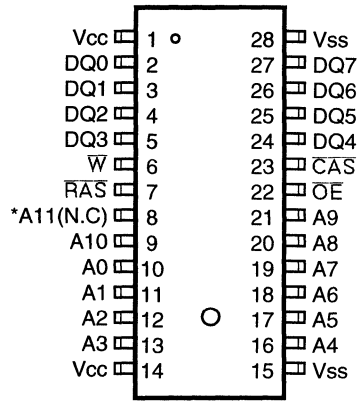
SAMSUNG ELECTRONIC CO. , LTD. reserves the right to change products and specifications without notice.

PIN CONFIGURATION (Top Views)

• KM48C/V20(1)00BK



• KM48C/V20(1)00BS



* A11 is N.C for KM48C/V2100B (5V/3.3V, 2K Ref. product)

K : 300mil 28 SOJ

S : 300mil 28 TSOP II

Pin Name	Pin Function
A0 ~ A11	Address Inputs (4K product)
A0 ~ A10	Address Inputs (2K product)
DQ0 ~ 7	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Outputs Enable
Vcc	Power (+5.0V)
	Power (+3.3V)
N.C	No Connection (2K Ref. product)

ABSOLUTE MAXIMUM RATINGS *

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max				Units
			KM48V2000 B	KM48V2100B	KM48C2000B	KM48C2100B	
I_{CC1}	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	-	-	mA
I_{CC2}	Normal	Don't care	1	1	2	2	mA
	L		1	1	1	1	mA
I_{CC3}	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	-	-	mA
I_{CC4}	Don't care	-5	-	-	80	90	mA
		-6	70	80	70	80	mA
		-7	60	70	60	70	mA
		-8	50	60	-	-	mA
I_{CC5}	Normal	Don't care	0.5	0.5	1	1	mA
	L		0.3	0.3	0.3	0.3	mA
I_{CC6}	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	-	-	mA
I_{CC7}	L	Don't care	450	400	450	400	µA
I_{CCS}	L	Don't care	250	250	300	300	µA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V

Din = Don't care, T_{RC}= 31.25µs(4K/L-ver), 62.5µs(2K/L-ver),

T_{RAS}=T_{RAS}min~300ns

I_{CCS} : Self Refresh Current

$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = Vcc-0.2V or 0.2V, DQ0 ~ DQ7= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$ =V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8 *2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4
Access time from column address	tAA		25		30		35		40	ns	3,9
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	5
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	7
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		15		15		ns	
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	

Note) *1 : 5V only, *2 : 3.3V only

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Test condition (5V device) : V_{CC}=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition (3.3V device) : V_{CC}=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	8
Data hold time	tDH	10		10		15		15		ns	8
Refresh period (2K, Normal)	tREF		32		32		32		32	ms	
Refresh period (4K, Normal)	tREF		64		64		64		64	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	6
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	6
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		75		ns	6
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}B\overline{R}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	0	20	ns	5
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	10
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	10
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		us	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

Note) *1 : 5V only, *2 : 3.3V only

TEST MODE CYCLE

(Note. 10, 11)

Parameter	Symbol	-5 *1		-6		-7		-8 *2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4
Access time from column address	tAA		30		35		40		45	ns	3,9
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	6
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	58		65		75		80		ns	6
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

Note) *1 : 5V only, *2 : 3.3V only

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
6. tWCS, tRWD, tCWD, tAWD and tCPWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥tCWD(min), tRWD≥tRWD(min), tAWD≥tAWD(min) and tCPWD≥tCPWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{CAS}$ falling edge in early write cycles and to the $\overline{W}$ falling edge in read-modify-write cycles.
9. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
10. These specifications are applied in the test mode.
11. In test mode read cycle, the values of tRAC, tAA and tCAC are delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding 5ns to the specified value in this data sheet.
12. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 4096(4K Ref.)/2048(2K Ref.) cycles of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.

2M x 8 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 2,097,152 x 8 bit Extended Data Out CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Power supply voltage (+5.0V or +3.3V), refresh cycle (2K Ref. or 4K Ref.), access time (-5, -6, -7 or -8), power consumption (Normal, Low power) and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in L-version.

This 2Mx8 EDO DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for high level computer, microcomputer and personal computer.

2

FEATURES

- Part Identification
  - KM48C2004B/B-L(5V, 4K Ref.)
  - KM48C2104B/B-L(5V, 2K Ref.)
  - KM48V2004B/B-L(3.3V, 4K Ref.)
  - KM48V2104B/B-L(3.3V, 2K Ref.)

- Active Power Dissipation Unit :mW

Speed	3.3V		5V	
	4K	2K	4K	2K
-5	-	-	495	605
-6	288	360	440	550
-7	252	324	385	495
-8	216	288	-	-

- Refresh cycles

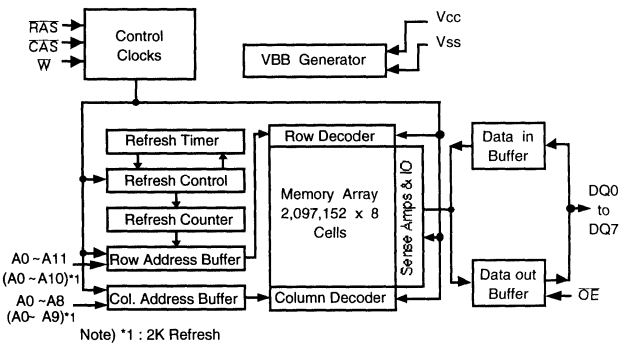
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
C2004B	5V	4K	64ms	128ms
V2004B	3.3V			
C2104B	5V	2K	32ms	
V2104B	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tHPC	Remark
-5	50ns	13ns	84ns	20ns	5V
-6	60ns	15ns	114ns	25ns	5V/3.3V
-7	70ns	20ns	124ns	30ns	5V/3.3V
-8	80ns	20ns	144ns	35ns	3.3V

- Extended Data Out mode operation (Fast Page mode with Extended Data Out)
- Byte Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver)
- Fast parallel test mode capability
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

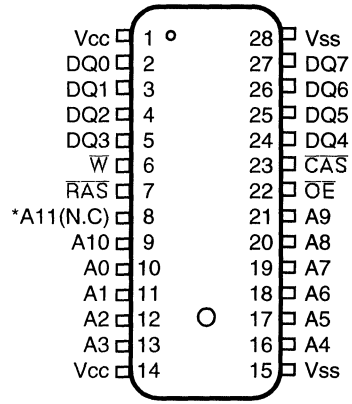
FUNCTIONAL BLOCK DIAGRAM



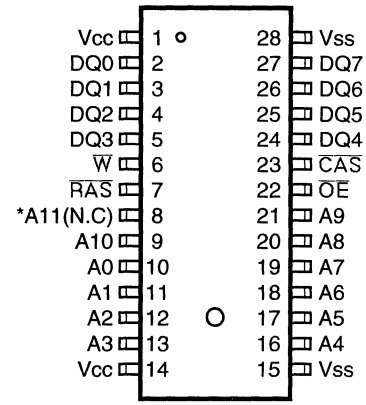
Note) *1 : 2K Refresh

PIN CONFIGURATION (Top Views)

• KM48C/V20(1)04BK



• KM48C/V20(1)04BS



* A11 is N.C for KM48C/V2104B (5V/3.3V, 2K Ref. product)

K : 300mil 28 SOJ

S : 300mil 28 TSOP II

Pin Name	Pin Function
A0 ~ A11	Address Inputs (4K product)
A0 ~ A10	Address Inputs (2K product)
DQ0 ~ 7	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Outputs Enable
Vcc	Power (+3.3V)
	Power (+5.0V)
N.C	No Connection (2K Ref. product)

ABSOLUTE MAXIMUM RATINGS *

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max				Units
			KM48V2004B	KM48V2104B	KM48C2004B	KM48C2104B	
I_{CC1}	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	-	-	mA
I_{CC2}	Normal	Don't care	1	1	2	2	mA
	L		1	1	1	1	mA
I_{CC3}	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	-	-	mA
I_{CC4}	Don't care	-5	-	-	100	110	mA
		-6	90	100	90	100	mA
		-7	80	90	80	90	mA
		-8	70	80	-	-	mA
I_{CC5}	Normal	Don't care	0.5	0.5	1	1	mA
	L		0.3	0.3	0.3	0.3	mA
I_{CC6}	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	-	-	mA
I_{CC7}	L	Don't care	450	400	450	400	μA
I_{CCS}	L	Don't care	250	250	300	300	μA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=0.2V

Din = Don't care, T_{RC}= 31.25μs(4K/L-ver), 62.5μs(2K/L-ver)

T_{RAS}=T_{RAS}min~300ns

I_{CCS} : Self Refresh Current

$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = Vcc-0.2V or 0.2V, DQ0 ~ DQ7= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle time, tHPC.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		144		ns	
Read-modify-write cycle time	tRWC	116		140		170		190		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4
Access time from column address	tAA		25		30		35		40	ns	3,9
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	3	20	ns	5,13
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		3		ns	3
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	38		45		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	7
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		15		15		ns	
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	

Note) *1 : 5V only, *2 : 3.3V only

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, Vih/Vil=2.4/0.8V, Voh/Vol=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, Vih/Vil=2.0/0.8V, Voh/Vol=2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8 *2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	8
Data hold time	tDH	8		10		15		15		ns	8
Refresh period (2K, Normal)	tREF		32		32		32		32	ms	
Refresh period (4K, Normal)	tREF		64		64		64		64	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	6
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	30		34		44		44		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		94		104		ns	6
Column address to $\overline{W}$ delay time	tAWD	42		49		59		64		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	47		54		64		69		ns	6
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}\overline{B}\overline{R}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		25		30		35		ns	14
Hyper Page read-modify-write cycle time	tHPRWC	47		56		71		81		ns	14
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	5
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	10
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	10
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	6,15
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	5
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulth width (Hyper Page Cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		us	12

Note) *1 : 5V only, *2 : 3.3V only

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, Vih/Vil=2.4/0.8V, Voh/Vol=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, Vih/Vil=2.0/0.8V, Voh/Vol=2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8 *2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

TEST MODE CYCLE

(Note. 10, 11)

Parameter	Symbol	-5 *1		-6		-7		-8 *2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	89		109		129		149		ns	
Read-modify-write cycle time	tRWC	121		145		175		195		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4
Access time from column address	tAA		30		35		40		45	ns	3,9
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	43		50		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	35		39		49		49		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	72		84		99		109		ns	7
Column address to $\overline{W}$ delay time	tAWD	47		54		64		69		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	52		59		69		74		ns	7
Hyper Page cycle time	tHPC	25		30		35		40		ns	14
Hyper page read-modify-write cycle time	tHPRWC	53		61		76		86		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		33		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

Note) *1 : 5V only, *2 : 3.3V only

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
6. tWCS, tRWD, tCWD, tAWD and tCPWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥tCWD(min), tRWD≥tRWD(min), tAWD≥tAWD(min) and tCPWD≥tCPWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{CAS}$ falling edge in early write cycles and to the $\overline{W}$ falling edge in read-modify-write cycles.
9. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
10. These specifications are applied in the test mode.
11. In test mode read cycle, the values of tRAC, tAA and tCAC are delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding 5ns to the specified value in this data sheet.
12. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 4096(4K Ref.)/2048(2K Ref.) cycles of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.
13. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
14. tASC ≥ 6ns , Assume tT = 2.0 ns

1M x 16Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 1,048,576 x16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage(+5.0V or +3.3V), refresh cycle(1K Ref. or 4K Ref.), access time(-6, -7 or -8), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in self-refresh version.

This 1Mx16 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memroy unit for microcomputer, personal computer and portable machines.

FEATURES

- Part Identification
  - KM416C1000A/A-L (5V, 4K Ref.)
  - KM416C1200A/A-L (5V, 1K Ref.)
  - KM416V1000A/A-L (3.3V, 4K Ref.)
  - KM416V1200A/A-L (3.3V, 1K Ref.)

- Active Power Dissipation Unit : mW

Speed	3.3V		5V	
	4K	1K	4K	1K
-6	324	540	550	880
-7	288	504	495	825
-8	252	468	440	770

- Refresh cycles

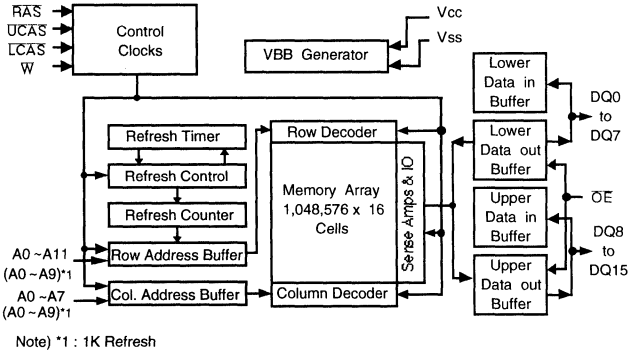
Part NO.	Vcc	Refresh cycle	Refresh time	
			Normal	L-ver
C1000A	5V	4K	64ms	128ms
V1000A	3.3V			
C1200A	5V	1K	16ms	
V1200A	3.3V			

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns
-8	80ns	20ns	150ns	50ns

- Fast Page Mode operation
- 2 $\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability(L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Triple +5V±10% power supply(5V product)
- Triple +3.3V±0.3V power supply(3.3V product)

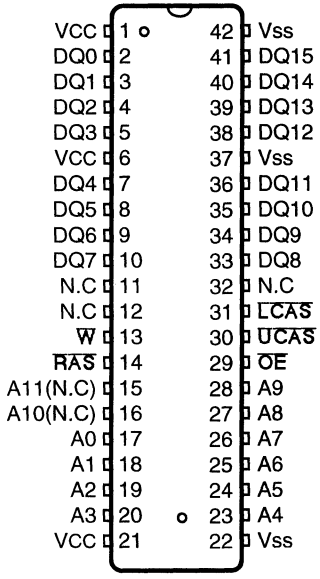
FUNCTIONAL BLOCK DIAGRAM



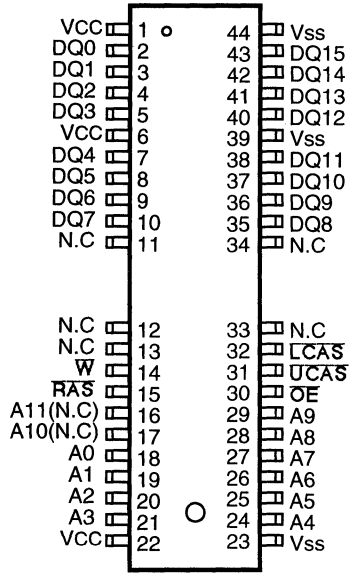
Note) *1 : 1K Refresh

PIN CONFIGURATION (Top Views)

• KM416C/V10(2)00AJ



• KM416C/V10(2)00AT



* Note : ( ) --> 1K Product

Pin Name	Pin Function
A0 - A11	Address Inputs(4K Product)
A0 - A9	Address Inputs(1K Product)
DQ0 -15	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
VCC	Power(+5.0V)
	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3*1	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc + 1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max				Units
			KM416V1000A	KM416V1200A	KM416C1000A	KM416C1200A	
I_{CC1}	Don't care	-6 -7 -8	90 80 70	150 140 130	100 90 80	160 150 140	mA mA mA
I_{CC2}	Normal L	Don't care	1 1	1 1	2 1	2 1	mA mA
I_{CC3}	Don't care	-6 -7 -8	90 80 70	150 140 130	100 90 80	160 150 140	mA mA mA
I_{CC4}	Don't care	-6 -7 -8	90 80 70	100 90 80	100 90 80	110 100 90	mA mA mA
I_{CC5}	Normal L	Don't care	0.5 0.2	0.5 0.2	1 0.2	1 0.2	mA mA
I_{CC6}	Don't care	-6 -7 -8	90 80 70	150 140 130	100 90 80	160 150 140	mA mA mA
I_{CC7}	L	Don't care	400	300	450	350	µA
I_{CCS}	L	Don't care	200	200	250	250	µA

I_{CC1}* : Operating Current ($\overline{RAS}$,$\overline{UCAS}$,$\overline{LCAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-Only Refresh Current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$= 0.2V,
Din = Don't care, T_{RC}= 31.25µs(4K/L-ver), 125µs(1K/L-ver), T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = V_{CC}-0.2V or 0.2V,
DQ0 ~ DQ15= V_{CC}-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$,$\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition(5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition(3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	11
Column address hold time	tCAH	10		15		15		ns	11
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		ns	7
Write command hold time	tWCH	10		15		15		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		20		ns	

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9,17
Data hold time	tDH	10		15		15		ns	9,17
Refresh period(1K, Normal)	tREF		16		16		16	ms	
Refresh period(4K, Normal)	tREF		64		64		64	ms	
Refresh period(L -ver)	tREF		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		50		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	15
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	16
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		95		100		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	3
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	20	0	20	ns	6
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	18
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	18
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	18

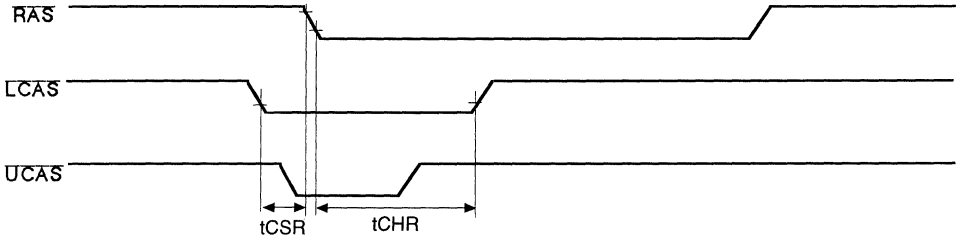
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL (5V device)/ 1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

KM416C/V10(2)00A/A-L Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8 - DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

11. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
12. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
13. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
14. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
15. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
16. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



17. tDS, tDH is independently specified for lower byte D_{IN}(0~7), upper byte D_{IN}(8~15).
18. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 4096 cycle(1024 cycle) of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification(L-version).

1M x 16Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 1,048,576 x16 bit Dxtended Data Out CMOS DRAMs. Dxtended Data Out mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Power supply voltage(+5.0V or +3.3V), refresh cycle(1K Ref. or 4K Ref.), access time(-6, -7 or -8), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in Low power version.

This 1Mx16 Extended Data Out mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memroy unit for microcomputer, personal computer and portable machines.

FEATURES

- Part Identification
  - KM416C1004A/A-L (5V, 4K Ref.)
  - KM416C1204A/A-L (5V, 1K Ref.)
  - KM416V1004A/A-L (3.3V, 4K Ref.)
  - KM416V1204A/A-L (3.3V, 1K Ref.)
- Active Power Dissipation Unit : mW

Speed	3.3V		5V	
	4K	1K	4K	1K
-6	324	540	550	880
-7	288	504	495	825
-8	252	468	440	770

- Refresh cycles

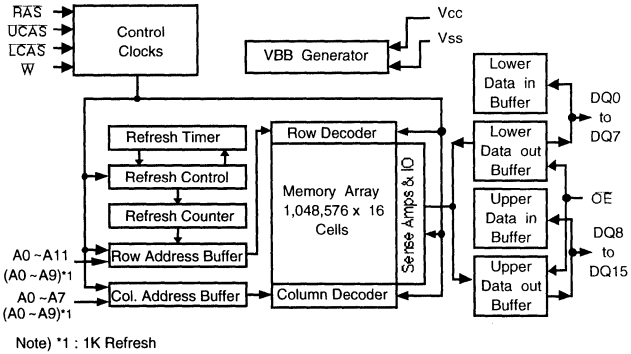
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L-ver
C1004A	5V	4K	64ms	128ms
V1004A	3.3V			
C1204A	5V	1K	16ms	
V1204A	3.3V			

- Performance range:

Speed	tRAC	tCAC	tRC	tHPC
-6	60ns	17ns	104ns	25ns
-7	70ns	20ns	124ns	30ns
-8	80ns	20ns	144ns	35ns

- Extended Data Out mode operation (Fast Page mode with Extended Data Out)
- 2$\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability(L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Triple +5V±10% power supply(5V product)
- Triple +3.3V±0.3V power supply(3.3V product)

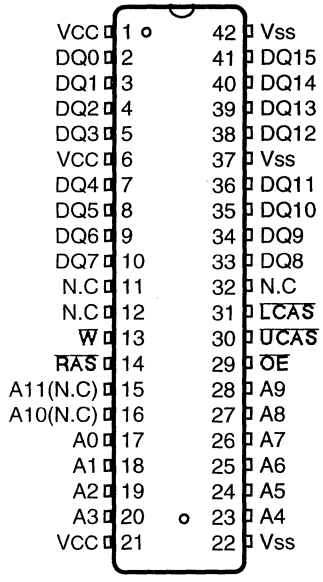
FUNCTIONAL BLOCK DIAGRAM



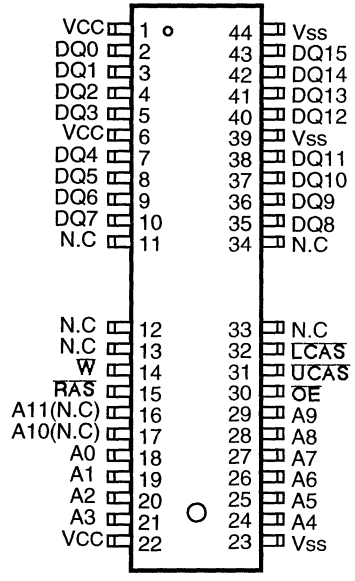
Note) *1 : 1K Refresh

PIN CONFIGURATION (Top Views)

• KM416C/V10(2)04AJ



• KM416C/V10(2)04AT



* Note : (N.C) --> 1K Product

Pin Name	Pin Function
A0 - A11	Address Inputs(4K Product)
A0 - A9	Address Inputs(1K Product)
DQ0 -15	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
V_{CC}	Power(+5.0V)
	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3*1	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc + 1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max				Units
			KM416V1004A	KM416V1204A	KM416C1004A	KM416C1204A	
I_{CC1}	Don't care	-6 -7 -8	90 80 70	150 140 130	100 90 80	160 150 140	mA mA mA
I_{CC2}	Normal L	Don't care	1 1	1 1	2 1	2 1	mA mA
I_{CC3}	Don't care	-6 -7 -8	90 80 70	150 140 130	100 90 80	160 150 140	mA mA mA
I_{CC4}	Don't care	-6 -7 -8	110 100 90	120 110 100	120 110 100	130 120 110	mA mA mA
I_{CC5}	Normal L	Don't care	0.5 0.2	0.5 0.2	1 0.2	1 0.2	mA mA
I_{CC6}	Don't care	-6 -7 -8	90 80 70	150 140 130	100 90 80	160 150 140	mA mA mA
I_{CC7}	L	Don't care	400	400	450	350	µA
I_{CCS}	L	Don't care	200	200	250	250	µA

I_{CC1}* : Operating Current ($\overline{RAS}$,$\overline{UCAS}$,$\overline{LCAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-Only Refresh Current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$= 0.2V,
Din = Don't care, T_{RC}= 31.25µs(4K/L-ver), 125µs(1K/L-ver), T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = V_{CC}-0.2V or 0.2V,
DQ0 ~ DQ15= V_{CC}-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle time tHPC.

CAPACITANCE(T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$,$\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition(5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition(3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	104		124		144		ns	
Read-modify-write cycle time	tRWC	140		170		190		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		17		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	15	3	20	3	20	ns	6,13
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	17		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	10	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	43	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	14
Column address hold time	tCAH	10		15		15		ns	14
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		ns	7
Write command hold time	tWCH	10		15		15		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write command to $\overline{CAS}$ lead time	tCWL	10		15		20		ns	17
Data set-up time	tDS	0		0		0		ns	9,20
Data hold time	tDH	10		15		15		ns	9,20
Refresh period(1K, Normal)	tREF		16		16		16	ms	
Refresh period(4K, Normal)	tREF		64		64		64	ms	
Refresh period(L -ver)	tREF		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		44		44		ns	7,16
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	79		94		104		ns	7
Column address to $\overline{W}$ delay time	tAWD	49		59		64		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	54		64		69		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		10		ns	18
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Hyper Page mode cycle time	tHPC	25		30		35		ns	11
Hyper Page mode read-modify-write cycle time	tHPRWC	56		71		81		ns	11
$\overline{CAS}$ precharge time Hyper page cycle)	tCP	10		10		10		ns	15
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	3
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	6
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	20	3	20	ns	6,13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	15	3	20	3	20	ns	6
$\overline{W}$ to data delay	tWED	15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	12

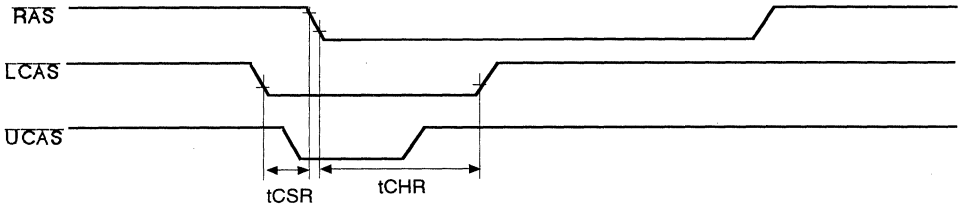
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL (5V device)/ 1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

KM416C/V10(2)04A/A-L Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8- DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

11. tASC≥ 6 ns, Assume tT = 2.0 ns
12. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 4096 cycle(1024 cycle) of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification(L-version).
13. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
14. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
15. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
16. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
17. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
18. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
19. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



20. tDS, tDH is independently specified for lower byte D_{IN}(0~7), upper byte D_{IN}(8~15).

1M x 16Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 1,048,576 x16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), refresh cycle (1K Ref. or 4K Ref.), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in L-version.

This 1Mx16 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memroy unit for microcomputer, personal computer and portable machines.

FEATURES

- Part Identification
  - KM416C1000B/B-L (5V, 4K Ref.)
  - KM416C1200B/B-L (5V, 1K Ref.)
  - KM416V1000B/B-L (3.3V, 4K Ref.)
  - KM416V1200B/B-L (3.3V, 1K Ref.)

- Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	1K	4K	1K
-5	-	-	605	880
-6	360	540	550	825
-7	324	504	495	770
-8	288	468	-	-

- Refresh cycles

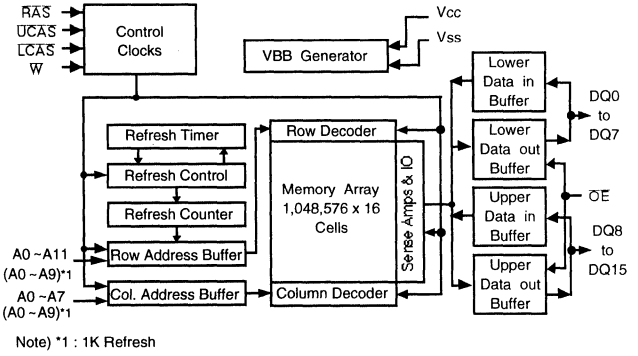
Part NO.	Vcc	Refresh cycle	Refresh time	
			Normal	L-ver
C1000B	5V	4K	64ms	128ms
V1000B	3.3V			
C1200B	5V	1K	16ms	
V1200B	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	15ns	90ns	35ns	5V
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	3.3V

- Fast Page Mode operation
- 2 $\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 1K Refresh

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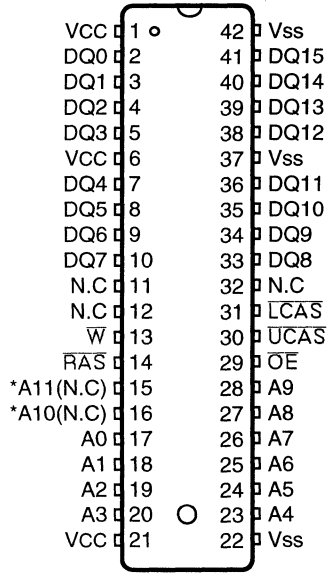
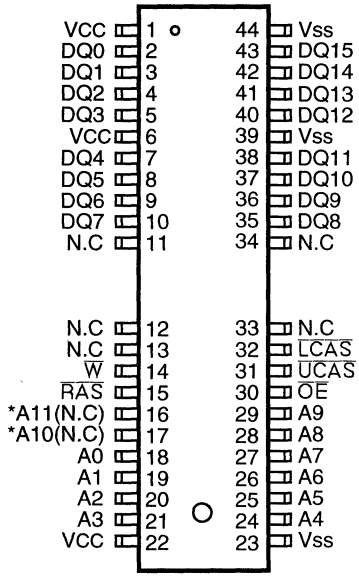
PIN CONFIGURATION (Top Views)

• KM416C/V10(2)00BJ



• KM416C/V10(2)00BT



* A10 and A11 are N.C for KM416C/V1200B (5V/3.3V, 1K Ref. product)

J : 400mil 42 SOJ
T : 400mil 50(44) TSOP II

Pin Name	Pin Function
A0 - A11	Address Inputs (4K Product)
A0 - A9	Address Inputs (1K Product)
DQ0 -15	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
VCC	Power (+5.0V)
	Power (+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS *

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3 *1	2.4	-	Vcc+1 *1	V
Input Low Voltage	V_{IL}	-0.3 *2	-	0.8	-1.0 *2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max				Units
			KM416V1000B	KM416V1200B	KM416C1000B	KM416C1200B	
I_{CC1}	Don't care	-5	-	-	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
		-8	80	130	-	-	mA
I_{CC2}	Normal	Don't care	1	1	2	2	mA
	L		1	1	1	1	mA
I_{CC3}	Don't care	-5	-	-	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
		-8	80	130	-	-	mA
I_{CC4}	Don't care	-5	-	-	100	100	mA
		-6	90	90	90	90	mA
		-7	80	80	80	80	mA
		-8	70	70	-	-	mA
I_{CC5}	Normal	Don't care	0.5	0.5	1	1	mA
	L		0.2	0.2	0.2	0.2	mA
I_{CC6}	Don't care	-5	-	-	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
		-8	80	130	-	-	mA
I_{CC7}	L	Don't care	400	300	450	350	µA
I_{CCS}	L	Don't care	200	200	250	250	µA

I_{CC1}* : Operating Current ($\overline{RAS}$,$\overline{UCAS}$,$\overline{LCAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-Only Refresh Current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$= 0.2V,
Din = Don't care, T_{RC}= 31.25µs(4K/L-ver), 125µs(1K/L-ver), T_{RAS}=T_{RAS}min~300ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = Vcc-0.2V or 0.2V,
DQ0 ~ DQ15= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$,$\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1, 2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		15		15		20		20	ns	3,4
Access time from column address	tAA		25		30		35		40	ns	3,9
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	5
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	10
Column address hold time	tCAH	10		10		15		15		ns	10
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	7
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		15		15		ns	
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	13

Note) *1 : 5V only, *2 : 3.3V only

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 2)

Test condition (5V device) : V_{CC}=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition (3.3V device) : V_{CC}=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8 *2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	8, 16
Data hold time	tDH	10		10		15		15		ns	8, 16
Refresh period (1K, Normal)	tREF		16		16		16		16	ms	
Refresh period (4K, Normal)	tREF		64		64		64		64	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	6
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	6, 12
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		95		105		ns	6
Column address to $\overline{W}$ delay time	tAWD	48		55		60		65		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		65		75		ns	6
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	14
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	15
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		80		95		100		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	11
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	3
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		us	17
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	17
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	17

Note) *1 : 5V only, *2 : 3.3V only

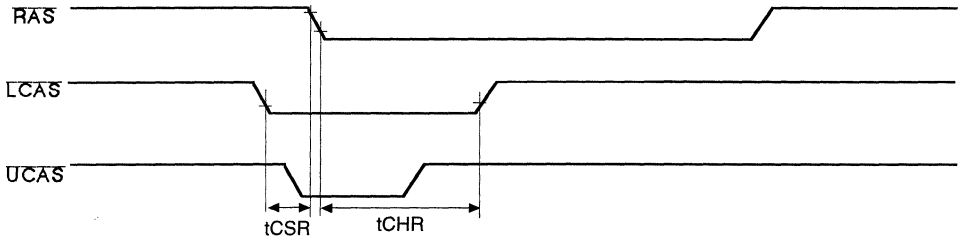
NOTES

1. An initial pause of 200us is required after power-up followed by any 8 ROR or CBR refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL (5V device)/ 1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
6. tWCS, tRWD, tCWD. tAWD and tCPWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥tCWD(min), tRWD≥tRWD(min), tAWD≥tAWD(min) and tCPWD≥tCPWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
9. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

KM416C/V10(2)00B/B-L Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8 - DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

10. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
11. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
12. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
13. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
14. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
15. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



16. tDS, tDH is independently specified for lower byte D_{IN}(0~7), upper byte D_{IN}(8~15).
17. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 4096(4K Ref.)/21024(1K Ref.) of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification (L-version).

1M x 16Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 1,048,576 x16 bit Extended Data Out CMOS DRAMs. Dxtended Data Out mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Power supply voltage (+5.0V or +3.3V), refresh cycle (1K Ref. or 4K Ref.), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in L-version.

This 1Mx16 Extended Data Out mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memroy unit for microcomputer, personal computer and portable machines.

2

FEATURES

- Part Identification
  - KM416C1004B/B-L (5V, 4K Ref.)
  - KM416C1204B/B-L (5V, 1K Ref.)
  - KM416V1004B/B-L (3.3V, 4K Ref.)
  - KM416V1204B/B-L (3.3V, 1K Ref.)

- Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	1K	4K	1K
-5	-	-	605	880
-6	360	540	550	825
-7	324	504	495	770
-8	288	468	-	-

- Refresh cycles

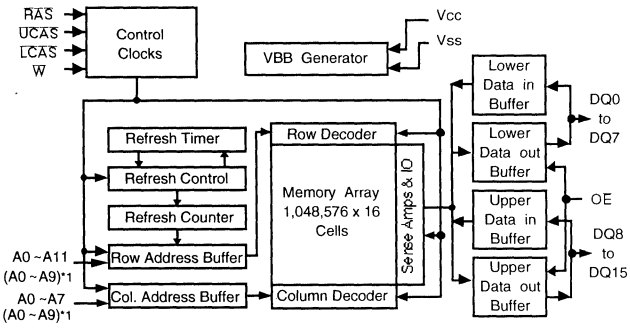
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L-ver
C1004B	5V	4K	64ms	128ms
V1004B	3.3V			
C1204B	5V	1K	16ms	
V1204B	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tHPC	Remark
-5	50ns	17ns	84ns	20ns	5V
-6	60ns	17ns	114ns	25ns	5V/3.3V
-7	70ns	20ns	124ns	30ns	5V/3.3V
-8	80ns	20ns	144ns	35ns	3.3V

- Extended Data Out mode operation (Fast Page mode with Extended Data Out)
- 2$\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

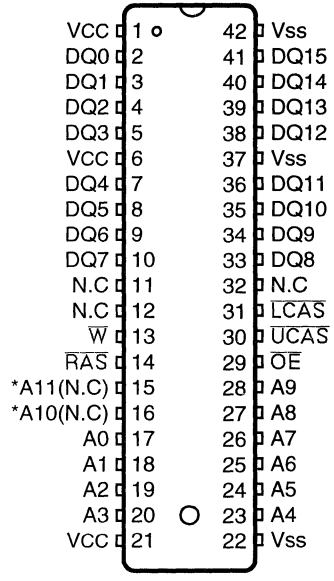
FUNCTIONAL BLOCK DIAGRAM



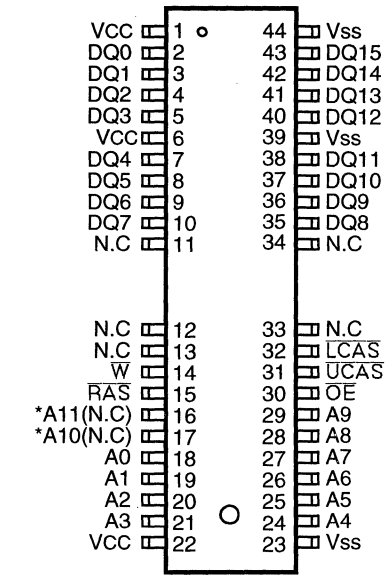
Note) *1 : 1K Refresh

PIN CONFIGURATION (Top Views)

• **KM416C/V10(2)04BJ**



• **KM416C/V10(2)04BT**



* A10 and A11 are N.C for KM416C/V1204B (5V/3.3V, 1K Ref. product)

J : 400mil 42 SOJ
T : 400mil 50(44) TSOP II

Pin Name	Pin Function
A0 - A11	Address Inputs (4K Product)
A0 - A9	Address Inputs (1K Product)
DQ0 -15	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
V_{CC}	Power (+5.0V)
	Power (+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3 *1	2.4	-	Vcc+1 *1	V
Input Low Voltage	V_{IL}	-0.3 *2	-	0.8	-1.0 *2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	µA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	µA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	µA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	µA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max				Units
			KM416V1000B	KM416V1200B	KM416C1000B	KM416C1200B	
I_{CC1}	Don't care	-5	-	-	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
		-8	80	130	-	-	mA
I_{CC2}	Normal	Don't care	1	1	2	2	mA
	L		1	1	1	1	mA
I_{CC3}	Don't care	-5	-	-	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
		-8	80	130	-	-	mA
I_{CC4}	Don't care	-5	-	-	120	120	mA
		-6	110	110	110	110	mA
		-7	100	100	100	100	mA
		-8	90	90	-	-	mA
I_{CC5}	Normal	Don't care	0.5	0.5	1	1	mA
	L		0.2	0.2	0.2	0.2	mA
I_{CC6}	Don't care	-5	-	-	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
		-8	80	130	-	-	mA
I_{CC7}	L	Don't care	400	300	450	350	μA
I_{CCS}	L	Don't care	200	200	250	250	μA

I_{CC1}* : Operating Current ($\overline{RAS}$,$\overline{UCAS}$,$\overline{LCAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-Only Refresh Current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$=0.2V,
Din = Don't care, T_{RC}= 31.25μs(4K/L-ver), 125μs(1K/L-ver), T_{RAS}=T_{RAS}min~300ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = V_{CC}-0.2V or 0.2V,
DQ0 ~ DQ15= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle time, tHPC.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		144		ns	
Read-modify-write cycle time	tRWC	115		140		170		190		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		15		17		20		20	ns	3,4
Access time from column address	tAA		25		30		35		40	ns	3,9
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	3	20	ns	5,12
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		3		ns	3
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		17		20		20		ns	
$\overline{CAS}$ hold time	tCSH	40		50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	35	20	43	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	13
Column address hold time	tCAH	8		10		15		15		ns	13
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	7
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		15		15		ns	
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	16

Note) *1 : 5V only, *2 : 3.3V only

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Test condition (5V device) : V_{CC}=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : V_{CC}=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8 *2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	8, 19
Data hold time	tDH	8		10		15		15		ns	8, 19
Refresh period (1K, Normal)	tREF		16		16		16		16	ms	
Refresh period (4K, Normal)	tREF		64		64		64		64	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	6
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	32		36		44		44		ns	6, 15
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		94		104		ns	6
Column address to $\overline{W}$ delay time	tAWD	42		49		59		64		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	47		54		64		69		ns	6
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		10		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	18
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		25		30		35		ns	10
Hyper Page read-modify-write cycle time	tHPRWC	47		56		71		81		ns	10
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		10		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	3
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	5, 12
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	5
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulth width (Hyper Page Cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		us	11
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	11
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	11

Note) *1 : 5V only, *2 : 3.3V only

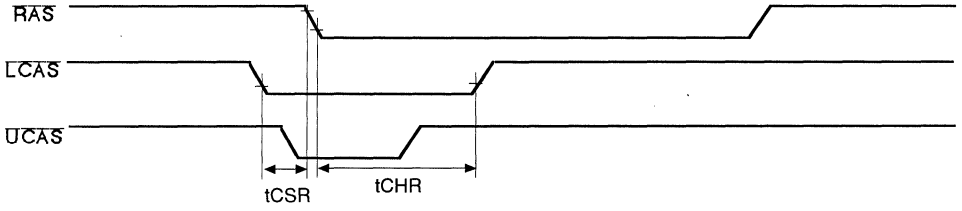
NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
6. tWCS, tRWD, tCWD, tAWD and tCPWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥tCWD(min), tRWD≥tRWD(min), tAWD≥tAWD(min) and tCPWD≥tCPWD(min) then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
9. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

KM416C/V10(2)04B/B-L Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8- DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

10. tASC≥ 6 ns, Assume tT = 2.0 ns
11. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 4096(4K Ref.)/1024(1K Ref.) of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification(L-version).
12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
13. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
14. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
15. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
16. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
17. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
18. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



19. tDS, tDH is independently specified for lower byte D_{IN}(0~7), upper byte D_{IN}(8~15).

64M DRAM

- KM44V16000A, KM44V16100A
- KM44V16004A, KM44V16104A
- KM44C16000A, KM44C16100A
- KM44C16004A, KM44C16104A
- KM48V8000A, KM48V8100A
- KM48V8004A, KM48V8104A
- KM48C8000A, KM48C8100A
- KM48C8004A, KM48C8104A
- KM416V4000A, KM416V4100A
- KM416V4004A, KM416V4104A

16M x 4 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 16,777,216 x 4 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time(-5, -6, or -7), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further- more, Self-refresh operation is available in L- version. This 16Mx4 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM44V16000A/A-L(3.3V, 8K Ref.)
  - KM44V16100A/A-L(3.3V, 4K Ref.)

- Active Power Dissipation

Unit : mW

Speed	8K	4K
-5	360	540
-6	324	504
-7	288	468

- Refresh cycles

Part NO.	Refresh cycle	Refresh time	
		Normal	L-ver
KM44V16000A*	8K	64ms	128ms
KM44V16100A	4K		

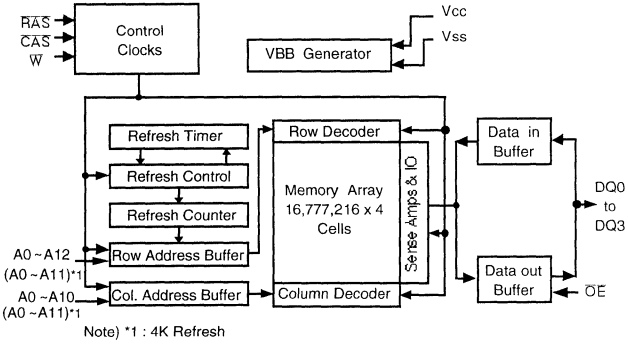
* Access mode & $\overline{RAS}$ only refresh mode
: 8K cycle/64ms
$\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
: 4K cycle/64ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$ only and Hidden refresh capability
- Self-refresh capability(L-ver only)
- Fast parallel test mode capability
- LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +3.3V±0.3V power supply

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 4K Refresh

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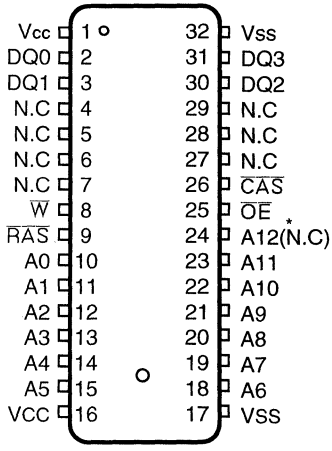
SAMSUNG ELECTRONICS

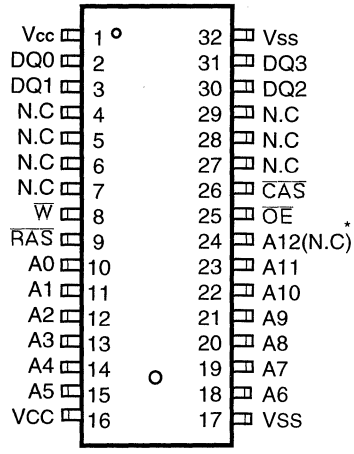
PIN CONFIGURATION (Top Views)

• KM44V160(1)00AK



(K: 400mil SOJ)

• KM44V160(1)00AS



(S: 400mil TSOP(II))

* (N.C) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 -3	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width ≤ 15ns which is measured at Vcc
*2 : -1.3V at pulse width ≤ 15ns which is measured at Vss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued.)

Symbol	Power	Speed	Max		Units
			KM44V16000A	KM44V16100A	
I_{CC1}	Don't care	-5 -6 -7	100 90 80	150 140 130	mA mA mA
I_{CC2}	Normal L	Don't care	1 1	1 1	mA mA
I_{CC3}	Don't care	-5 -6 -7	100 90 80	150 140 130	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	70 60 55	80 70 65	mA mA mA
I_{CC5}	Normal L	Don't care	500 300	500 300	µA µA
I_{CC6}	Don't care	-5 -6 -7	150 140 130	150 140 130	mA mA mA
I_{CC7}	L	Don't care	550	550	µA
I_{CCS}	L	Don't care	450	450	µA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V

$\overline{W}$, $\overline{OE}$ = VIH, Address = Don't care, DQ = Open, T_{RC}= 31.25µs

T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current

$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A12(A11) = Vcc-0.2V or 0.2V, DQ0 ~ DQ3= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc= 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 2)
Test condition : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol} =2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	133		153		180		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	13	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	10		10		15		ns	9
Refresh period(4K, Normal)	tREF		64		64		64	ms	
Refresh period(8K, Normal)	tREF		64		64		64	ms	
Refresh period(L-ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		38		45		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		83		95		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		53		60		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	14
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	3
Fast Page mode cycle time	tPC	35		40		45		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		13		15		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	13	0	15	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	15		15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	13
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		ns	13
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	13

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		ns	
Read-modify-write cycle time	tRWC	138		160		190		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,10,12
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5,12
Access time from column address	tAA		30		35		40	ns	3,10,12
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		43		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		88		100		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		58		65		ns	7
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		18		20		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL load and 100pF
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. For all of the refresh mode except the distributed $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096(8192) cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
14. It can get less $\overline{CAS}$-before-$\overline{RAS}$ current loss if tCHR≥tRAS or $\overline{CAS}$≤0.2V at $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.

16M x 4 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 16,777,216 x 4 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time(-5, -6, or -7), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further- more, Self-refresh operation is available in L- version. This 16Mx4 EDO mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM44V16004A/A-L(3.3V, 8K Ref.)
  - KM44V16104A/A-L(3.3V, 4K Ref.)

- Active Power Dissipation

Unit : mW

Speed	8K	4K
-5	360	540
-6	324	504
-7	288	468

- Refresh cycles

Part NO.	Refresh cycle	Refresh time	
		Normal	L-ver
KM44V16004A*	8K	64ms	128ms
KM44V16104A	4K		

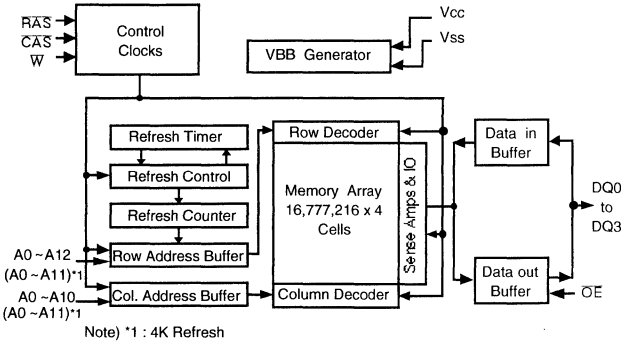
* Access mode & $\overline{RAS}$ only refresh mode
: 8K cycle/64ms
$\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
: 4K cycle/64ms

- Performance range:

Speed	tRAC	tCAC	tRC	tHPC
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns
-7	70ns	20ns	124ns	30ns

- Extended Data Out Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$ only and Hidden refresh capability
- Self-refresh capability(L-version)
- Fast parallel test mode capability
- LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +3.3V±0.3V power supply

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 4K Refresh

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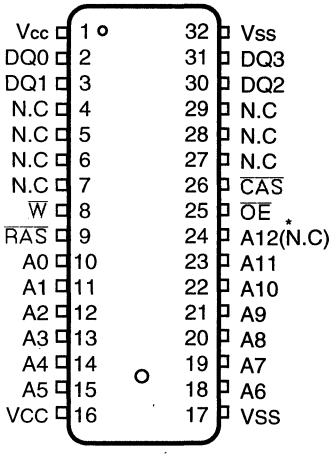
SAMSUNG ELECTRONICS

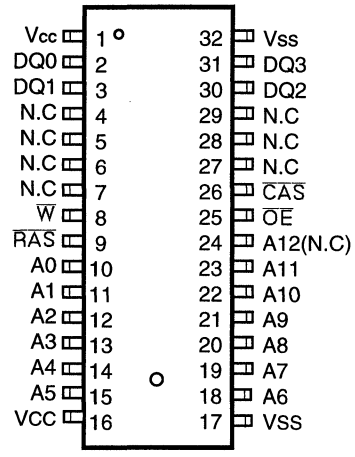
PIN CONFIGURATION (Top Views)

• KM44V160(1)04AK



(K: 400mil SOJ)

• KM44V160(1)04AS



(S: 400mil TSOP(II))

* (N.C) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 -3	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width ≤ 15ns which is measured at Vcc
*2 : -1.3V at pulse width ≤ 15ns which is measured at Vss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued.)

Symbol	Power	Speed	Max		Units
			KM44V16004A	KM44V16104A	
I_{CC1}	Don't care	-5 -6 -7	100 90 80	150 140 130	mA mA mA
I_{CC2}	Normal L	Don't care	1 1	1 1	mA mA
I_{CC3}	Don't care	-5 -6 -7	100 90 80	150 140 130	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	110 100 90	120 110 100	mA mA mA
I_{CC5}	Normal L	Don't care	500 300	500 300	µA µA
I_{CC6}	Don't care	-5 -6 -7	150 140 130	150 140 130	mA mA mA
I_{CC7}	L	Don't care	550	550	µA
I_{CCS}	L	Don't care	450	450	µA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Extended Data Out Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V

$\overline{W}$, $\overline{OE}$ = VIH, Address = Don't care, DQ = Open, T_{RC}= 31.25µs

T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current

$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A12(A11) = V_{CC}-0.2V or 0.2V, DQ0 ~ DQ3= V_{CC}-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time tHPC.

CAPACITANCE(T_A=25°C, V_{CC}= 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition : V_{CC}=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		ns	
Read-modify-write cycle time	tRWC	116		138		165		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	13	3	15	ns	6,13
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	
$\overline{CAS}$ hold time	tCSH	38		45		50		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	ns	15
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	8		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	8		10		15		ns	9
Refresh period(4K, Normal)	tREF		64		64		64	ms	
Refresh period(8K, Normal)	tREF		64		64		64	ms	
Refresh period(L-ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	30		32		39		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		77		89		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		47		54		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	17
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40	ns	3
Hyper Page cycle time	tHPC	20		25		30		ns	16
Hyper Page read-modify-write cycle time	tHPRWC	47		56		71		ns	16
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		13		15		ns	
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	13	3	15	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	10		10		10		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	15	3	20	ns	6,15
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	ns	6
$\overline{W}$ to data delay	tWED	15		15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulth width(Hyper Page Cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	14
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		ns	14
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	14

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	89		109		129		ns	
Read-modify-write cycle time	tRWC	121		145		175		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	43		50		55		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	35		37		44		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	72		82		94		ns	7
Column address to $\overline{W}$ delay time	tAWD	47		52		59		ns	7
Hyper Page cycle time	tHPC	25		30		35		ns	
Hyper page read-modify-write cycle time	tHPRWC	53		61		76		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		33		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 1 TTL load and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. For all of the refresh mode except the distributed $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096(8192) cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
15. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
16. tASC ≥ 6 ns , Assume tT = 2.0 ns
17. It can get less $\overline{CAS}$-before-$\overline{RAS}$ current loss if tCHR≥tRAS or $\overline{CAS}$≤0.2V at $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.

16M x 4 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 16,777,216 x 4 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time(-5, -6, or -7) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. This 16Mx4 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM44C16000A/A-L(5.0V, 8K Ref.)
  - KM44C16100A/A-L(5.0V, 4K Ref.)

- Active Power Dissipation

Unit : mW

Speed	8K	4K
-5	550	825
-6	495	770
-7	440	715

- Refresh cycles

Part NO.	Refresh cycle	Refresh time
		Normal
KM44C16000A*	8K	64ms
KM44C16100A	4K	

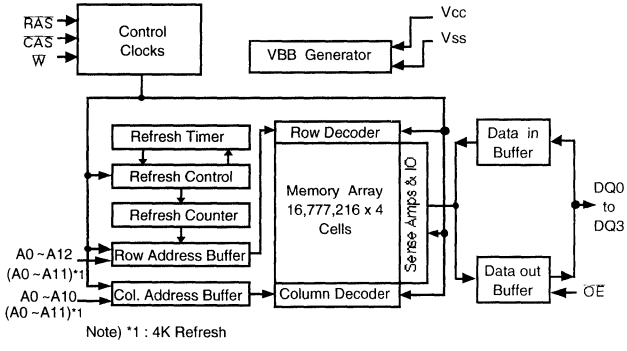
* Access mode & $\overline{RAS}$ only refresh mode
: 8K cycle/64ms
$\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
: 4K cycle/64ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$ only and Hidden refresh capability
- Fast parallel test mode capability
- TTL(5.0V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +5.0V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 4K Refresh

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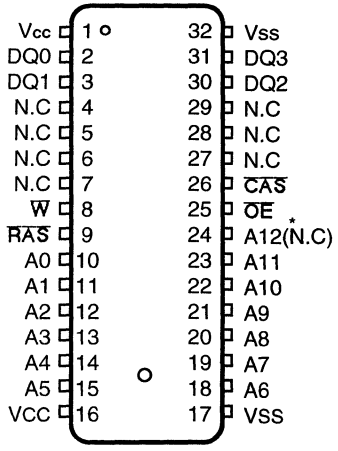
SAMSUNG ELECTRONICS

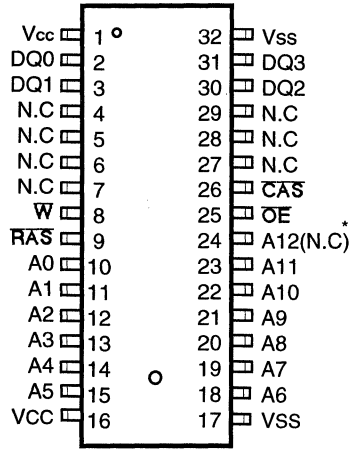
PIN CONFIGURATION (Top Views)

• KM44C160(1)00AK



(K: 400mil SOJ)

• KM44C160(1)00AS



(S: 400mil TSOP(II))

* (N.C) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 -3	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc *1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤ 20ns which is measured at Vcc
*2 : -2.0V at pulse width ≤ 20ns which is measured at Vss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued.)

Symbol	Power	Speed	Max		Units
			KM44C16000A	KM44C16100A	
I_{CC1}	Don't care	-5 -6 -7	100 90 80	150 140 130	mA mA mA
I_{CC2}	Normal	Don't care	2	2	mA
I_{CC3}	Don't care	-5 -6 -7	100 90 80	150 140 130	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	70 60 55	80 70 65	mA mA mA
I_{CC5}	Normal	Don't care	1	1	mA
I_{CC6}	Don't care	-5 -6 -7	150 140 130	150 140 130	mA mA mA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Extended Data Out Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time tHPC.

CAPACITANCE(T_A=25°C, Vcc=5.0V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	133		155		185		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	10		10		15		ns	9
Refresh period(4K, 8k, Normal)	tREF		64		64		64	ms	
Write command set-up time	tWCS	0		0		0		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	
Fast Page mode cycle time	tPC	35		40		45		ns	3
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	6
Write command set-up time(Test mode in)	tWTS	10		10		10		ns	
Write command hold time(Test mode in)	tWTH	15		15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		ns	
Read-modify-write cycle time	tRWC	138		160		190		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,10,12
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5,12
Access time from column address	tAA		30		35		40	ns	3,10,12
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		43		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		88		100		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		58		65		ns	7
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		18		20		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL load and100pF
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a re ference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. It can get less $\overline{CAS}$-before-$\overline{RAS}$ current loss if tCHR≥tRAS or $\overline{CAS}$≤0.2V at $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.

16M x 4 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 16,777,216 x 4 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time(-5, -6, or -7) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. This 16Mx4 EDO mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM44C16004A(5V, 8K Ref.)
  - KM44C16104A(5V, 4K Ref.)

- Active Power Dissipation

Unit : mW

Speed	8K	4K
-5	550	825
-6	495	770
-7	440	715

- Refresh cycles

Part NO.	Refresh cycle	Refresh time
		Normal
KM44C16004A*	8K	64ms
KM44C16104A	4K	

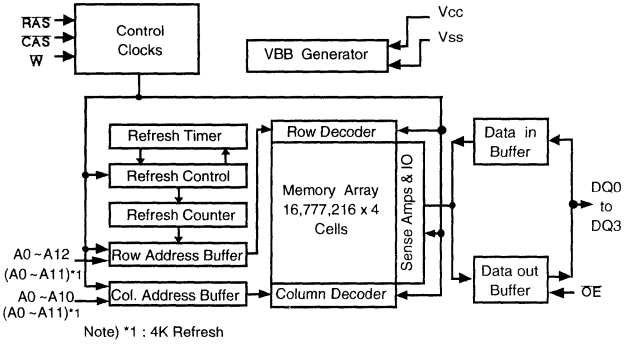
* Access mode & $\overline{RAS}$ only refresh mode
: 8K cycle/64ms
$\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
: 4K cycle/64ms

- Performance range:

Speed	tRAC	tCAC	tRC	tHPC
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns
-7	70ns	20ns	124ns	30ns

- Extended Data Out Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$ only and Hidden refresh capability
- Fast parallel test mode capability
- TTL(5.0V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +5.0V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 4K Refresh

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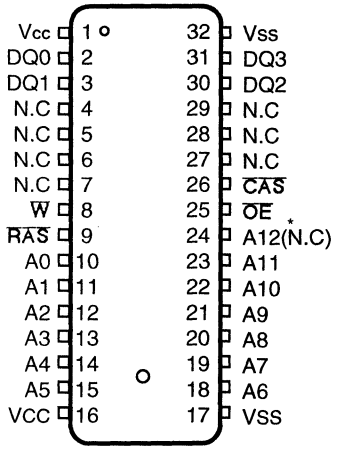
SAMSUNG ELECTRONICS

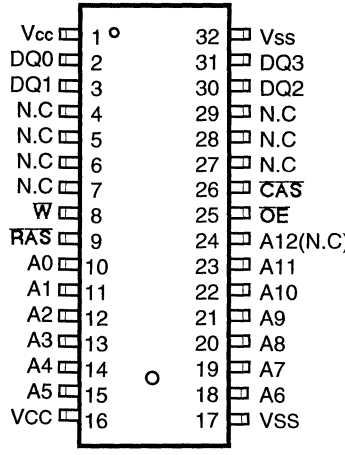
PIN CONFIGURATION (Top Views)

• KM44C160(1)04AK



(K: 400mil SOJ)

• KM44C160(1)04AS



(S: 400mil TSOP(II))

* (N.C) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 -3	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to Vss	V_{CC}	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : V_{CC}+2.0V at pulse width ≤ 20ns which is measured at Vcc
*2 : -2.0V at pulse width ≤ 20ns which is measured at Vss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued.)

Symbol	Power	Speed	Max		Units
			KM44C16004A	KM44C16104A	
I_{CC1}	Don't care	-5 -6 -7	100 90 80	150 140 130	mA mA mA
I_{CC2}	Normal	Don't care	2	2	mA
I_{CC3}	Don't care	-5 -6 -7	100 90 80	150 140 130	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	110 100 90	120 110 100	mA mA mA
I_{CC5}	Normal	Don't care	1	1	mA
I_{CC6}	Don't care	-5 -6 -7	150 140 130	150 140 130	mA mA mA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Extended Data Out Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time tHPC.

CAPACITANCE(T_A=25°C,Vcc= 5.0V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		ns	
Read-modify-write cycle time	tRWC	116		138		165		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	13	3	15	ns	6,13
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	
$\overline{CAS}$ hold time	tCSH	38		45		50		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	ns	15
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	8		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	8		10		15		ns	9
Refresh period(4K/8K, Normal)	tREF		64		64		64	ms	
Write command set-up time	tWCS	0		0		0		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	30		32		39		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		77		89		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		47		54		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	7
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	16
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40	ns	3
Hyper Page cycle time	tHPC	20		25		30		ns	15
Hyper Page read-modify-write cycle time	tHPRWC	47		56		71		ns	15
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		13		15		ns	
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	13	3	15	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	10		10		10		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	15	3	20	ns	6,14
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	ns	6
$\overline{W}$ to data delay	tWED	15		15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulth width(Hyper Page Cycle)	tWPE	5		5		5		ns	

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	89		109		129		ns	
Read-modify-write cycle time	tRWC	121		145		175		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	43		50		55		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	35		37		44		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	72		82		94		ns	7
Column address to $\overline{W}$ delay time	tAWD	47		52		59		ns	7
Hyper Page cycle time	tHPC	25		30		35		ns	
Hyper page read-modify-write cycle time	tHPRWC	53		61		76		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		33		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR **or** CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. tASC ≥ tCPmin , Assume tT = 2.0 ns
16. It can get less $\overline{CAS}$-before-$\overline{RAS}$ current loss if tCHR≥tRAS or $\overline{CAS}$≤0.2V at $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.

8M x 8 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 8,388,608 x 8 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time(-5, -6, or -7), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further- more, Self-refresh operation is available in L - version. This 8Mx8 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM48V8000A/A-L(3.3V, 8K Ref.)
  - KM48V8100A/A-L(3.3V, 4K Ref.)

- Active Power Dissipation

Unit : mW

Speed	8K	4K
-5	360	540
-6	324	504
-7	288	468

- Refresh cycles

Part NO.	Refresh cycle	Refresh time	
		Normal	L-ver
KM48V8000A*	8K	64ms	128ms
KM48V8100A	4K		

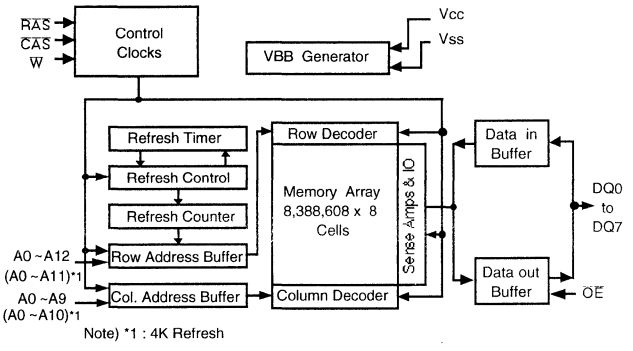
* Access mode & $\overline{RAS}$ only refresh mode
: 8K cycle/64ms
$\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
: 4K cycle/64ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$ only and Hidden refresh capability
- Self-refresh capability(L-ver only)
- Fast parallel test mode capability
- LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +3.3V±0.3V power supply

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 4K Refresh

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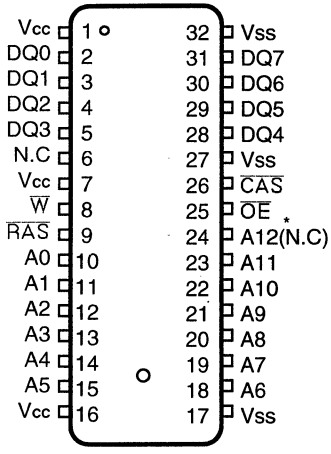
SAMSUNG ELECTRONICS

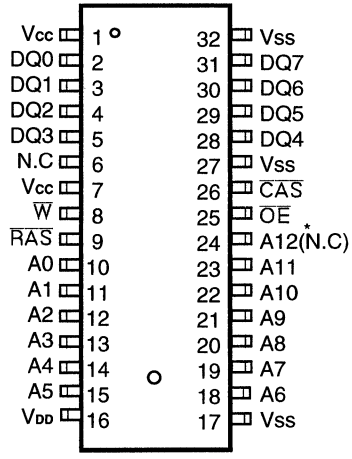
PIN CONFIGURATION (Top Views)

• KM48V80(1)00AK



(K: 400mil SOJ)

• KM48V80(1)00AS



(S: 400mil TSOP(II))

* (N.C) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 -7	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width ≤ 15ns which is measured at Vcc
*2 : -1.3V at pulse width ≤ 15ns which is measured at Vss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued.)

Symbol	Power	Speed	Max		Units
			KM48V8000A	KM48V8100A	
I_{CC1}	Don't care	-5 -6 -7	100 90 80	150 140 130	mA mA mA
I_{CC2}	Normal L	Don't care	1 1	1 1	mA mA
I_{CC3}	Don't care	-5 -6 -7	100 90 80	150 140 130	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	70 60 55	80 70 65	mA mA mA
I_{CC5}	Normal L	Don't care	500 300	500 300	µA µA
I_{CC6}	Don't care	-5 -6 -7	150 140 130	150 140 130	mA mA mA
I_{CC7}	L	Don't care	550	550	µA
I_{CCS}	L	Don't care	450	450	µA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V

$\overline{W}$, $\overline{OE}$ = VIH, Address = Don't care, DQ=Open, T_{RC}= 31.25µs

T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current

$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A12(A11) = V_{CC}-0.2V or 0.2V, DQ0 ~ DQ7= V_{CC}-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc= 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	133		153		180		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	13	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	10		10		15		ns	9
Refresh period(4K, Normal)	tREF		64		64		64	ms	
Refresh period(8K, Normal)	tREF		64		64		64	ms	
Refresh period(L -ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		38		45		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		83		95		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		53		60		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	14
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	3
Fast Page mode cycle time	tPC	35		40		45		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		13		15		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	13	0	15	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	15		15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	13
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		ns	13
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	13

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		ns	
Read-modify-write cycle time	tRWC	138		160		190		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,10,12
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5,12
Access time from column address	tAA		30		35		40	ns	3,10,12
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		43		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		88		100		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		58		65		ns	7
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		18		20		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL load and100pF
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS ≥ tWCS (min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read- modify -write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC, tOEA, and tCPA is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. For all of the refresh mode except the distributed $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096(8192) cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
14. It can get less $\overline{CAS}$-before-$\overline{RAS}$ current loss if tCHR≥tRAS or $\overline{CAS}$≤0.2V at $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.

8M x 8 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 8,388,608 x 8 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time(-5, -6, or -7), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further- more, Self-refresh operation is available in L- version. This 8Mx8 EDO mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM48V8004A/A-L(3.3V, 8K Ref.)
  - KM48V8104A/A-L(3.3V, 4K Ref.)

- Active Power Dissipation

Unit : mW

Speed	8K	4K
-5	360	540
-6	324	504
-7	288	468

- Refresh cycles

Part NO.	Refresh cycle	Refresh time	
		Normal	L-ver
KM48V8004A*	8K	64ms	128ms
KM48V8104A	4K		

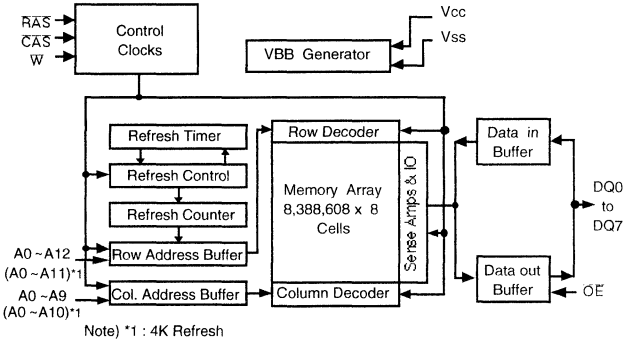
* Access mode & $\overline{RAS}$ only refresh mode
: 8K cycle/64ms
$\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
: 4K cycle/64ms

- Performance range:

Speed	tRAC	tCAC	tRC	tHPC
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns
-7	70ns	20ns	124ns	30ns

- Extended Data Out Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$ only and Hidden refresh capability
- Self-refresh capability(L-version)
- Fast parallel test mode capability
- LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +3.3V±0.3V power supply

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 4K Refresh

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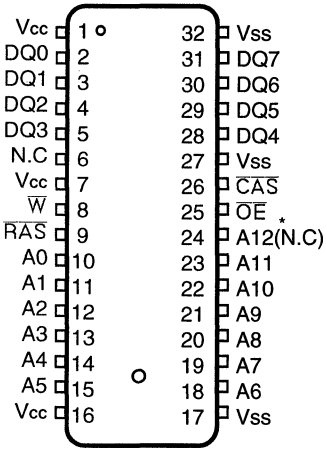
SAMSUNG ELECTRONICS

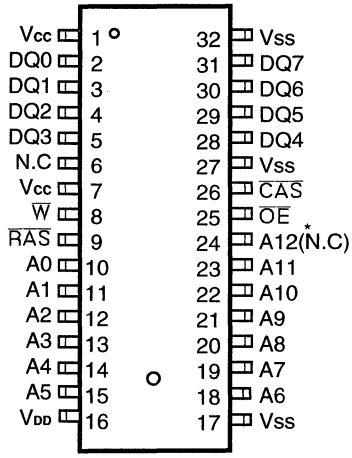
PIN CONFIGURATION (Top Views)

• KM48V80(1)04AK



(K: 400mil SOJ)

• KM48V80(1)04AS



(S: 400mil TSOP(II))

* (N.C) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 -7	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Outputs Enable
Vcc	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width ≤ 15ns which is measured at Vcc
*2 : -1.3V at pulse width ≤ 15ns which is measured at Vss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued.)

Symbol	Power	Speed	Max		Units
			KM48V8004A	KM48V8104A	
I_{CC1}	Don't care	-5 -6 -7	100 90 80	150 140 130	mA mA mA
I_{CC2}	Normal L	Don't care	1 1	1 1	mA mA
I_{CC3}	Don't care	-5 -6 -7	100 90 80	150 140 130	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	110 100 90	120 110 100	mA mA mA
I_{CC5}	Normal L	Don't care	500 300	500 300	μA μA
I_{CC6}	Don't care	-5 -6 -7	150 140 130	150 140 130	mA mA mA
I_{CC7}	L	Don't care	550	550	μA
I_{CCS}	L	Don't care	450	450	μA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Extended Data Out Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V

$\overline{W}$, $\overline{OE}$ = VIH, Address = Don't care, DQ=Open, T_{RC}= 31.25μs

T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current

$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A12(A11) = Vcc-0.2V or 0.2V, DQ0 ~ DQ7= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time tHPC.

CAPACITANCE(T_A=25°C,Vcc= 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 2)
Test condition : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol} =2.0/0.8V

Parameter	Symbol	- 5		- 6		- 7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		ns	
Read-modify-write cycle time	tRWC	116		138		165		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	13	3	15	ns	6,13
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	
$\overline{CAS}$ hold time	tCSH	38		45		50		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	ns	15
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	8		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	8		10		15		ns	9
Refresh period(4K, Normal)	tREF		64		64		64	ms	
Refresh period(8K, Normal)	tREF		64		64		64	ms	
Refresh period(L-ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	30		32		39		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		77		89		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		47		54		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	17
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40	ns	3
Hyper Page cycle time	tHPC	20		25		30		ns	16
Hyper Page read-modify-write cycle time	tHPRWC	47		56		71		ns	16
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		13		15		ns	
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	13	3	15	ns	6,13
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	10		10		10		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	ns	6,13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	ns	6,13
$\overline{W}$ to data delay	tWED	15		15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulth width(Hyper Page Cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	14
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		ns	14
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	14

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	89		109		129		ns	
Read-modify-write cycle time	tRWC	121		145		175		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	43		50		55		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	35		37		44		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	72		82		94		ns	7
Column address to $\overline{W}$ delay time	tAWD	47		52		59		ns	7
Hyper Page cycle time	tHPC	25		30		35		ns	16
Hyper page read-modify-write cycle time	tHPRWC	53		61		76		ns	16
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		33		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 1 TTL load and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. For all of the refresh mode except the distributed $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096(8192) cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
15. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
16. tASC ≥ 6 ns , Assume tT = 2.0 ns
17. It can get less $\overline{CAS}$-before-$\overline{RAS}$ current loss if tCHR≥tRAS or $\overline{CAS}$≤0.2V at $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.

8M x 8 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 8,388,608 x 8 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cucye(4K Ref. or 8K Ref.), access time(-5, -6, or -7), package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$ only refresh and Hidden refresh capabilities. This 8Mx8 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM48C8000A(5V, 8K Ref.)
  - KM48C8100A(5V, 4K Ref.)

- Active Power Dissipation

Unit : mW

Speed	8K	4K
-5	550	825
-6	495	770
-7	440	715

- Refresh cycles

Part NO.	Refresh cycle	Refresh time
		Normal
KM48C8000A*	8K	64ms
KM48C8100A	4K	

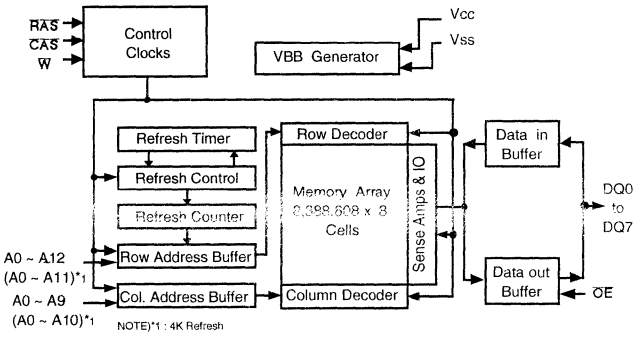
* Access mode & $\overline{RAS}$ only refresh mode
: 8K cycle/64ms
$\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
: 4K cycle/64ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$ only and Hidden refresh capability
- Fast parallel test mode capability
- TTL(5V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- 5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



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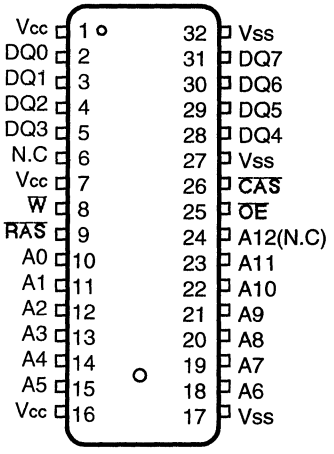
SAMSUNG ELECTRONICS

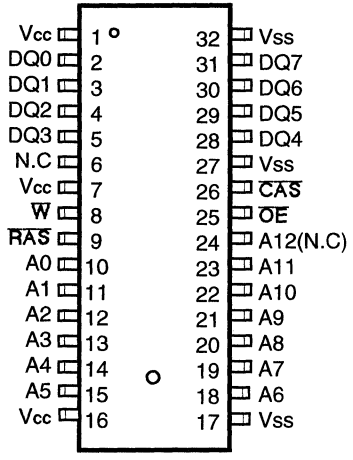
PIN CONFIGURATION (Top Views)

• KM48C80(1)00AK



(K: 400mil SOJ)

• KM48C80(1)00AS



(S: 400mil TSOP(II))

*(N.C) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 - 7	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Outputs Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc *1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤ 20ns which is measured at Vcc
*2 : -2.0V at pulse width ≤ 20ns which is measured at Vss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued.)

Symbol	Power	Speed	Max		Units
			KM48C8000A	KM44C8100A	
I_{CC1}	Don't care	-5 -6 -7	100 90 80	150 140 130	mA mA mA
I_{CC2}	Normal	Don't care	2	2	mA
I_{CC3}	Don't care	-5 -6 -7	100 90 80	150 140 130	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	70 60 55	80 70 65	mA mA mA
I_{CC5}	Normal	Don't care	1	1	mA
I_{CC6}	Don't care	-5 -6 -7	150 140 130	150 140 130	mA mA mA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 2)
Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	133		155		185		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	10		10		15		ns	9
Refresh period(4K/8K, Normal)	tREF		64		64		64	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	3
Fast Page mode cycle time	tPC	35		40		45		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	15		15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		ns	
Read-modify-write cycle time	tRWC	138		160		190		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,10,12
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5,12
Access time from column address	tAA		30		35		40	ns	3,10,12
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		60		70		ns	7
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2TTL loads and100pF
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS ≥ tWCS (min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read- modify -write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC, tOEA, and tCPA is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. It can get less $\overline{CAS}$-before-$\overline{RAS}$ current loss if tCHR≥tRAS or $\overline{CAS}$≤0.2V at $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.

8M x 8 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 8,388,608 x 8 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time(-5, -6, or -7), package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. This 8Mx8 EDO mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM48C8004A(5V, 8K Ref.)
  - KM48C8104A(5V, 4K Ref.)

- Active Power Dissipation

Unit : mW

Speed	8K	4K
-5	550	825
-6	495	770
-7	440	715

- Refresh cycles

Part NO.	Refresh cycle	Refresh time
KM48C8000A*	8K	64ms
KM48C8100A	4K	

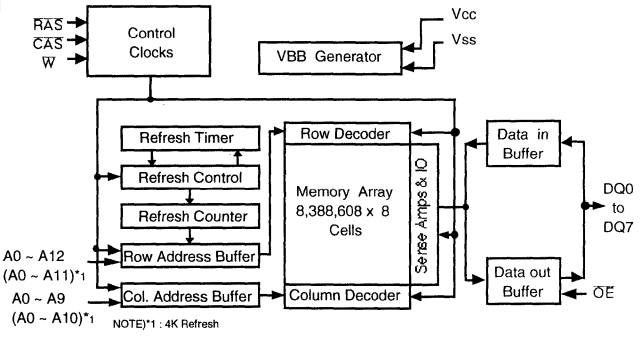
* Access mode & $\overline{RAS}$ only refresh mode
: 8K cycle/64ms
$\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
: 4K cycle/64ms

- Performance range:

Speed	tRAC	tCAC	tRC	tHPC
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns
-7	70ns	20ns	124ns	30ns

- Extended Data Out Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$ only and Hidden refresh capability
- Fast parallel test mode capability
- TTL(5V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



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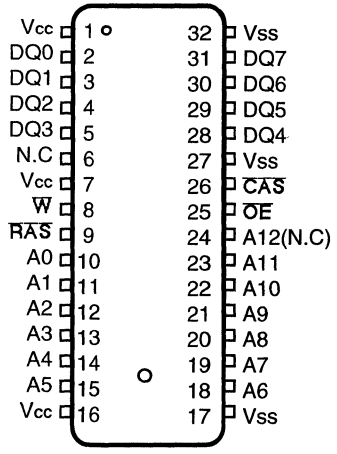
SAMSUNG ELECTRONICS

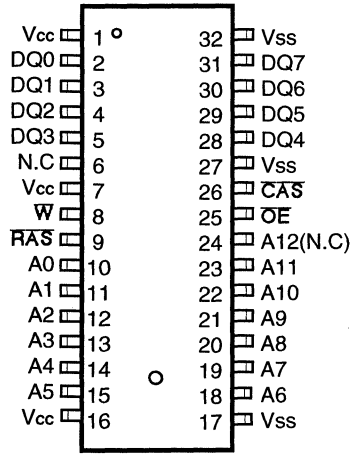
PIN CONFIGURATION (Top Views)

• KM48C8004AK



(K: 400mil SOJ)

• KM48C8004AS



(S: 400mil TSOP(II))

*(N.C) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 - 7	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC} *1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : V_{CC}+2.0V at pulse width ≤ 20ns which is measured at Vcc
*2 : -2.0V at pulse width ≤ 20ns which is measured at Vss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued.)

Symbol	Power	Speed	Max		Units
			KM48C8000A	KM44C8100A	
I_{CC1}	Don't care	-5 -6 -7	100 90 80	150 140 130	mA mA mA
I_{CC2}	Normal	Don't care	2	2	mA
I_{CC3}	Don't care	-5 -6 -7	100 90 80	150 140 130	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	110 100 90	120 110 100	mA mA mA
I_{CC5}	Normal	Don't care	1	1	mA
I_{CC6}	Don't care	-5 -6 -7	150 140 130	150 140 130	mA mA mA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Extended Data Out Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time tHPC.

CAPACITANCE(T_A=25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		ns	
Read-modify-write cycle time	tRWC	116		138		165		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	13	3	15	ns	6,13
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	
$\overline{CAS}$ hold time	tCSH	38		45		50		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	ns	14
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	8		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	8		10		15		ns	9
Refresh period(4k/8K, Normal)	tREF		64		64		64	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	30		32		39		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		77		89		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		47		54		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	16
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40	ns	3
Hyper Page cycle time	tHPC	20		25		30		ns	15
Hyper Page read-modify-write cycle time	tHPRWC	47		56		71		ns	15
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		13		15		ns	
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	13	3	15	ns	6,13
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	10		10		10		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	ns	6,13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	ns	6,13
$\overline{W}$ to data delay	tWED	15		15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulth width(Hyper Page Cycle)	tWPE	5		5		5		ns	

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	89		109		129		ns	
Read-modify-write cycle time	tRWC	121		145		175		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	43		50		55		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	35		37		44		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	72		82		94		ns	7
Column address to $\overline{W}$ delay time	tAWD	47		52		59		ns	7
Hyper Page cycle time	tHPC	25		30		35		ns	15
Hyper page read-modify-write cycle time	tHPRWC	53		61		76		ns	15
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		33		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a re ference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. tASC ≥ tCPmin , Assume tT = 2.0 ns
16. It can get less $\overline{CAS}$-before-$\overline{RAS}$ current loss if tCHR≥tRAS or $\overline{CAS}$≤0.2V at $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.

4M x 16Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 4,194,304 x16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time(-5, -6 or -7) and power consumption(Normal or Low power) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further- more, self-refresh operation is available in L- version. This 4Mx16 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification

  - KM416V4000A/A-L (3.3V, 8K Ref.)
  - KM416V4100A/A-L (3.3V, 4K Ref.)

- Active Power Consumption Unit : mW

Speed	8K	4K
-5	396	540
-6	360	504
-7	324	468

- Refresh cycles

Part NO.	Refresh cycle	Refresh time	
		Normal	L-ver
KM416V4000A*	8K	64ms	128ms
KM416V4100A	4K		

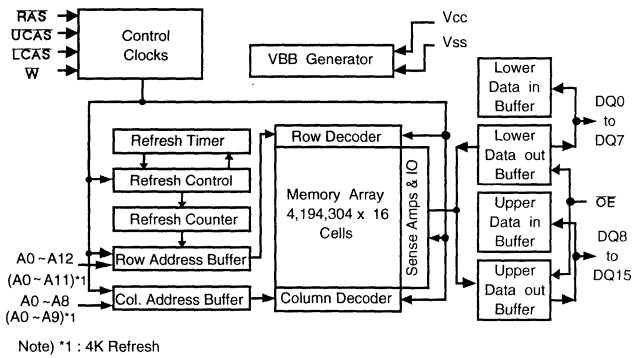
* Access mode & $\overline{RAS}$ only refresh mode
: 8K cycle/64ms
$\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
: 4K cycle/64ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns

- Fast Page Mode operation
- 2 $\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability(L-ver only)
- LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic TSOP(II) package
- +3.3V±0.3V power supply

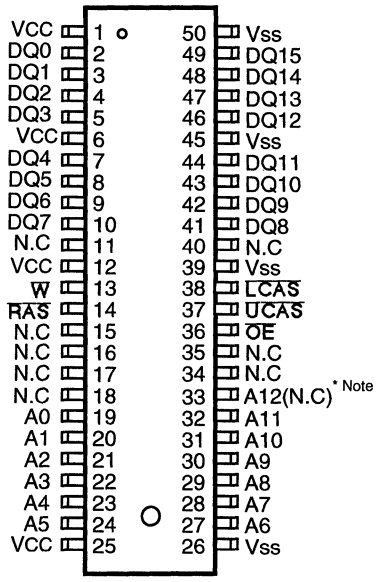
FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 4K Refresh

PIN CONFIGURATION (Top Views)

• **KM416V40(1)00AS**



* Note : A12 --> 8K Product(KM416V4000A)
N.C --> 4K Product(KM416V4100A)

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 -15	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
VCC	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc + 1.3V at pulse width≤15ns which is measured at Vcc.
*2 : - 1.3V at pulse width≤15ns which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM416V4000A	KM416V4100A	
I_{CC1}	Don't care	-5 -6 -7	110 100 90	150 140 130	mA mA mA
I_{CC2}	Normal L	Don't care	1 1	1 1	mA mA
I_{CC3}	Don't care	-5 -6 -6	110 100 90	150 140 130	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	90 80 70	90 80 70	mA mA mA
I_{CC5}	Normal L	Don't care	500 300	500 300	µA µA
I_{CC6}	Don't care	-5 -6 -7	150 140 130	150 140 130	mA mA mA
I_{CC7}	L	Don't care	550	550	µA
I_{CCS}	L	Don't care	450	450	µA

I_{CC1}* : Operating Current ($\overline{RAS}$,$\overline{UCAS}$,$\overline{LCAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-Only Refresh Current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$= 0.2V,

Din = Don't care, T_{RC}= 31.25µs, T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current

$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = V_{CC}-0.2V or 0.2V,

DQ0 ~ DQ15= V_{CC}-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C, Vcc= 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	133		153		180		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	13	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	13
Column address hold time	tCAH	10		10		15		ns	13
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		ns	16

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9,19
Data hold time	tDH	10		10		15		ns	9,19
Refresh period(4K, Normal)	tREF		64		64		64	ms	
Refresh period(8K, Normal)	tREF		64		64		64	ms	
Refresh period(L -ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		38		45		ns	7,15
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		83		95		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		53		60		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	18,21
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	3
Fast Page mode cycle time	tPC	35		40		45		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	14
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		13		15		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	13	0	15	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	15		15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	20
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		ns	20
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	20

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		ns	
Read-modify-write cycle time	tRWC	138		160		190		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,10,12
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5,12
Access time from column address	tAA		30		35		40	ns	3,10,12
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		43		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		88		100		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		58		65		ns	7
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		18		20		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

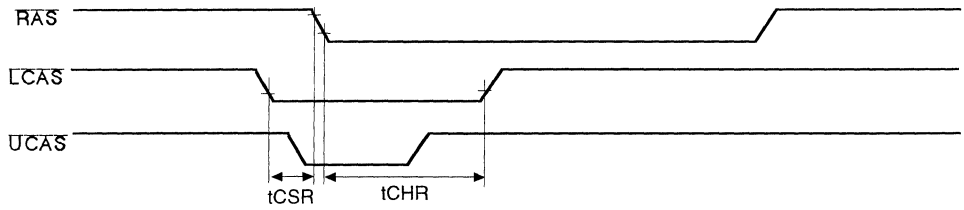
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR **or** CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL load and100pF
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a re ference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and are not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a re ference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.

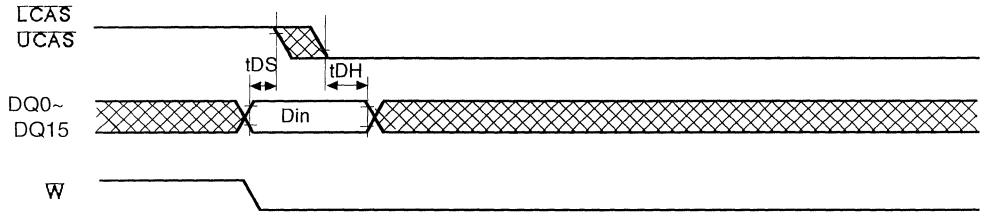
KM416V40(1)00A/A-L Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8 - DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
14. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
15. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
16. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
17. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
18. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



19. tDS is specified by the earlier $\overline{CAS}$ falling edge and tDH is specified by the later $\overline{CAS}$ falling edge.



20. For all of the refresh mode except the distributed $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096(8192) cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
21. It can get less $\overline{CAS}$-before-$\overline{RAS}$ current loss if tCHR≥tRAS or $\overline{CAS}$≤0.2V at $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.

4M x 16Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 4,194,304 x16 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time(-5, -6 or -7) and power consumption(Normal or Low power) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further- more, self-refresh operation is available in L- version. This 4Mx16 EDO Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

• Part Identification

- KM416V4004A/A-L (3.3V, 8K Ref.)
- KM416V4104A/A-L (3.3V, 4K Ref.)

• Active Power Consumption Unit : mW

Speed	8K	4K
-5	396	504
-6	360	432
-7	324	396

• Refresh cycles

Part NO.	Refresh cycle	Refresh time	
		Normal	L-ver
KM416V4004A*	8K	64ms	128ms
KM416V4104A	4K		

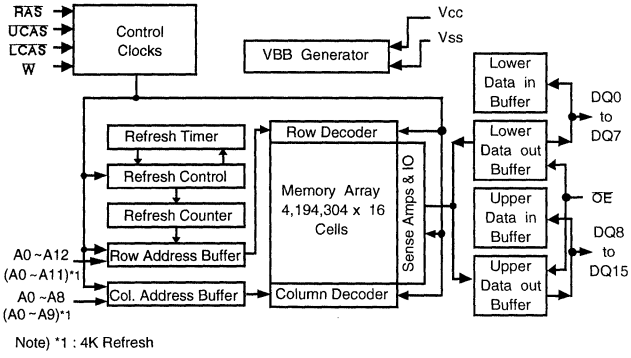
* Access mode & $\overline{RAS}$ only refresh mode
: 8K cycle/64ms
$\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
: 4K cycle/64ms

• Performance range:

Speed	tRAC	tCAC	tRC	tHPC
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns
-7	70ns	20ns	124ns	30ns

• Extended Data Out Mode operation
• 2 $\overline{CAS}$ Byte/Word Read/Write operation
• $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
• $\overline{RAS}$-only and Hidden refresh capability
• Self-refresh capability(L-ver only)
• LVTTL(3.3V) compatible inputs and outputs
• Early Write or output enable controlled write
• JEDEC Standard pinout
• Available in Plastic TSOP(II) package
• +3.3V±0.3V power supply

FUNCTIONAL BLOCK DIAGRAM

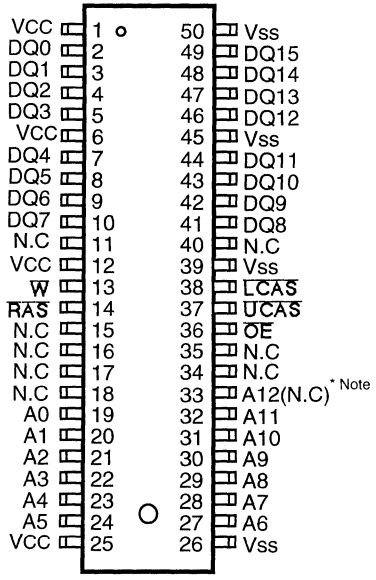


Note) *1 : 4K Refresh

SAMSUNG ELECTRONIC CO. , LTD. reserves the right to change products and specifications without notice.

PIN CONFIGURATION (Top Views)

• **KM416V40(1)04AS**



* Note : A12 --> 8K Product(KM416V4004A)
N.C --> 4K Product(KM416V4104A)

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 -15	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
VCC	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
		3.3V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3 *1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width ≤ 15ns which is measured at Vcc
*2 : -1.3V at pulse width ≤ 15ns which is measured at Vss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM416V4004A	KM416V4104A	
I_{CC1}	Don't care	-5 -6 -7	110 100 90	150 140 130	mA mA mA
I_{CC2}	Normal L	Don't care	1 1	1 1	mA mA
I_{CC3}	Don't care	-5 -6 -6	110 100 90	150 140 130	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	110 100 90	120 110 100	mA mA mA
I_{CC5}	Normal L	Don't care	500 300	500 300	µA µA
I_{CC6}	Don't care	-5 -6 -7	150 140 130	150 140 130	mA mA mA
I_{CC7}	L	Don't care	550	550	µA
I_{CCS}	L	Don't care	450	450	µA

I_{CC1}* : Operating Current ($\overline{RAS}$,$\overline{UCAS}$,$\overline{LCAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-Only Refresh Current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$= 0.2V,

Din = Don't care, T_{RC}= 31.25µs, T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current

$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A12 (11)= V_{CC}-0.2V or 0.2V,

DQ0 ~ DQ15= V_{CC}-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time tHPC.

CAPACITANCE(T_A=25°C, Vcc= 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		ns	
Read-modify-write cycle time	tRWC	116		140		170		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	ns	6
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	
$\overline{CAS}$ hold time	tCSH	38		45		50		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	ns	15
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	13
Column address hold time	tCAH	8		10		15		ns	13
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		ns	16

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9,19
Data hold time	tDH	8		10		15		ns	9,19
Refresh period(4K, Normal)	tREF		64		64		64	ms	
Refresh period(8K, Normal)	tREF		64		64		64	ms	
Refresh period(L-ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	30		34		44		ns	7,15
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		94		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		49		59		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	18,22
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40	ns	3
Hyper Page cycle time	tHPC	20		25		30		ns	20
Hyper Page read-modify-write cycle time	tHPRWC	47		56		71		ns	20
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		ns	
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	10		10		10		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	ns	6
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	ns	6
$\overline{W}$ to data delay	tWED	15		15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulth width(Hyper Page Cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	21
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		ns	21
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	21

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	89		109		129		ns	
Read-modify-write cycle time	tRWC	121		145		175		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	43		50		55		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	35		39		49		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	72		84		99		ns	7
Column address to $\overline{W}$ delay time	tAWD	47		54		64		ns	7
Hyper Page cycle time	tHPC	25		30		35		ns	
Hyper page read-modify-write cycle time	tHPRWC	53		61		76		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		33		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

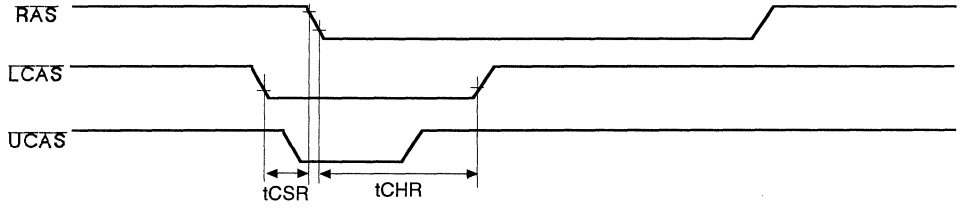
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL load and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. This parameter is referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.

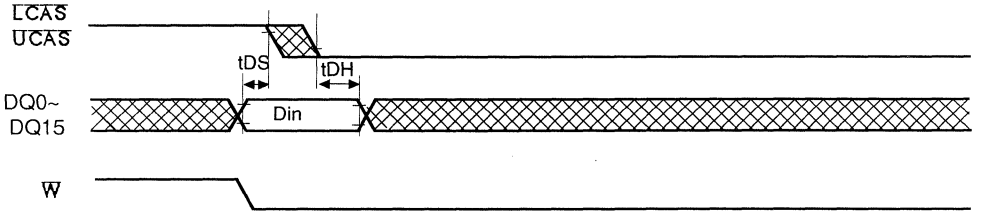
KM416V40(1)04A/A-L Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8 - DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
14. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
15. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
16. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
17. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
18. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



19. tDS is specified by the earlier $\overline{CAS}$ falling edge and tDH is specified by the later $\overline{CAS}$ falling edge.



20. tASC ≥ 6 ns , Assume tT = 2.0 ns
21. For all of the refresh mode except the distributed $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096(8192) cycles of burst refresh must be executed immediately before and after self refresh, in order to meet refresh specification.
22. It can get less $\overline{CAS}$-before-$\overline{RAS}$ current loss if tCHR≥tRAS or $\overline{CAS}$≤0.2V at $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.

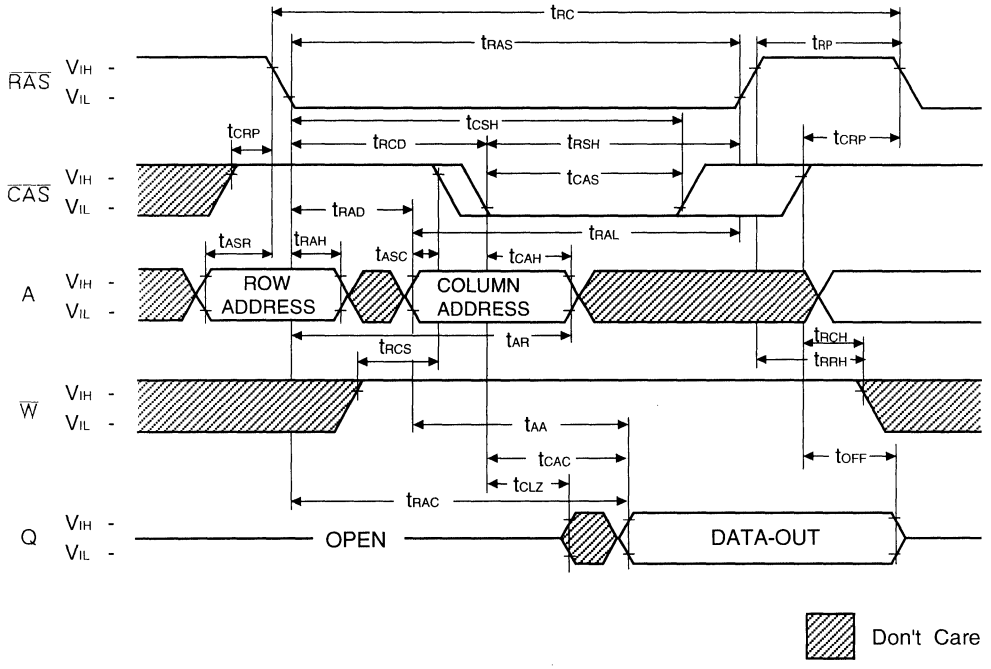
TIMING DIAGRAMS 3

- Fast Page Mode, x1 Device
- Fast Page Mode, x4 and x8 Device
- Fast Page Mode, x16(2$\overline{CAS}$) Device
- Fast Page Mode, x16(2$\overline{WE}$) Device
- Fast Page Mode, Quad $\overline{CAS}$ Device
- EDO Mode, x4 and x8 Device
- EDO Mode, x16(2$\overline{CAS}$) Device
- EDO Mode, x16(2$\overline{WE}$) Device
- EDO Mode, Quad $\overline{CAS}$ Device

Fast page Mode, x1 Device

TIMING DIAGRAM

READ CYCLE



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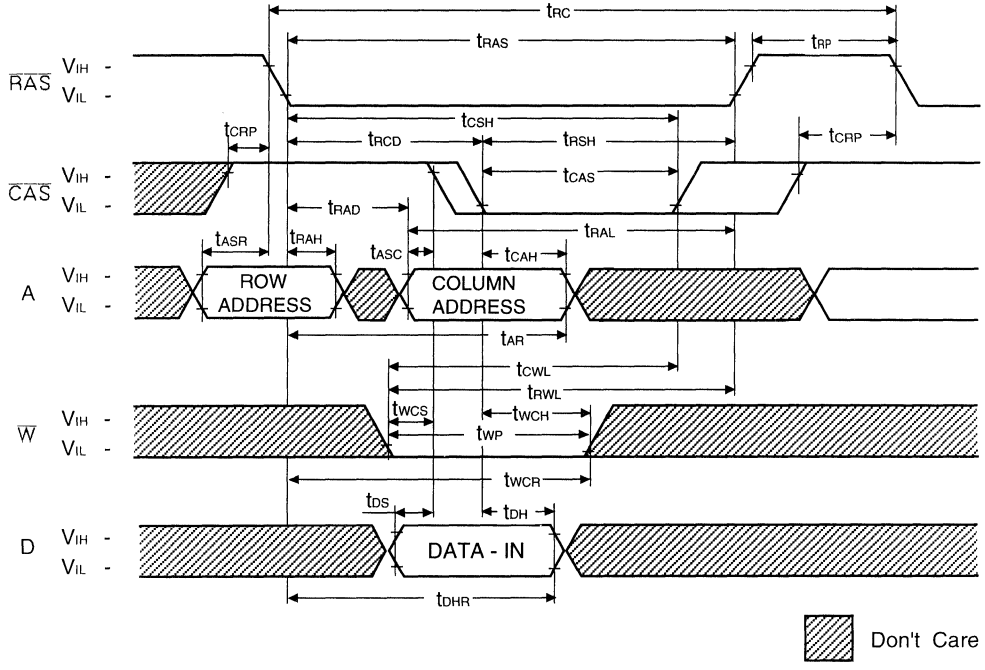
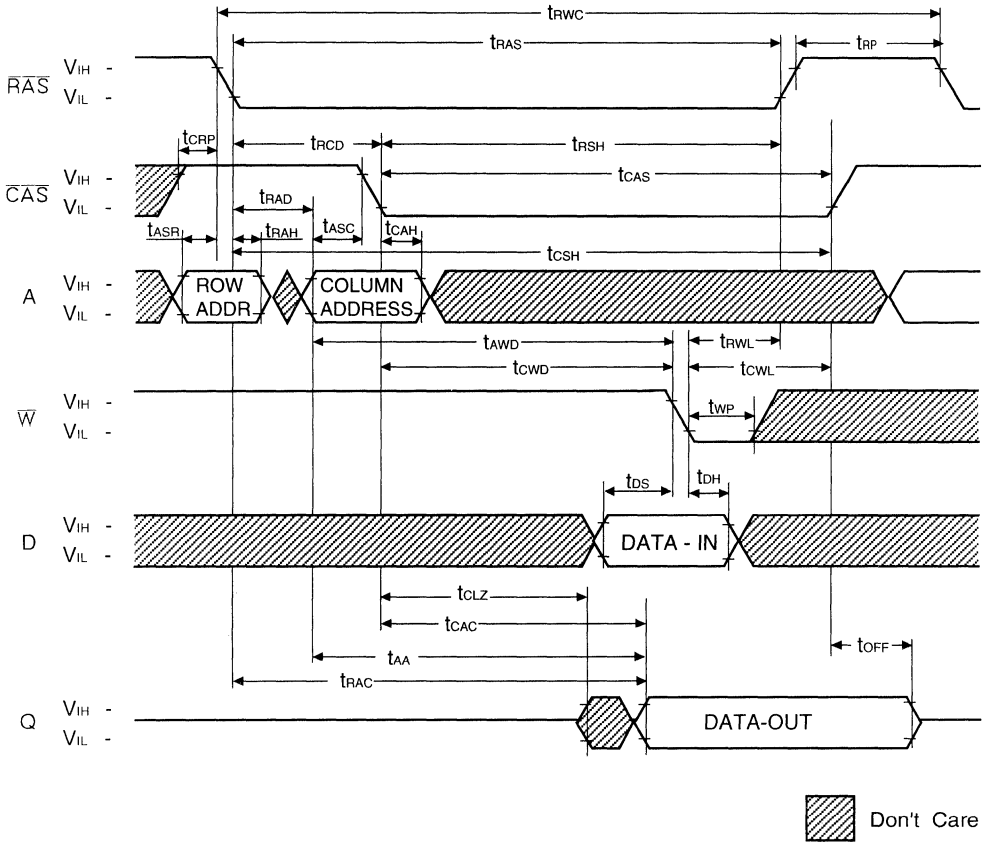
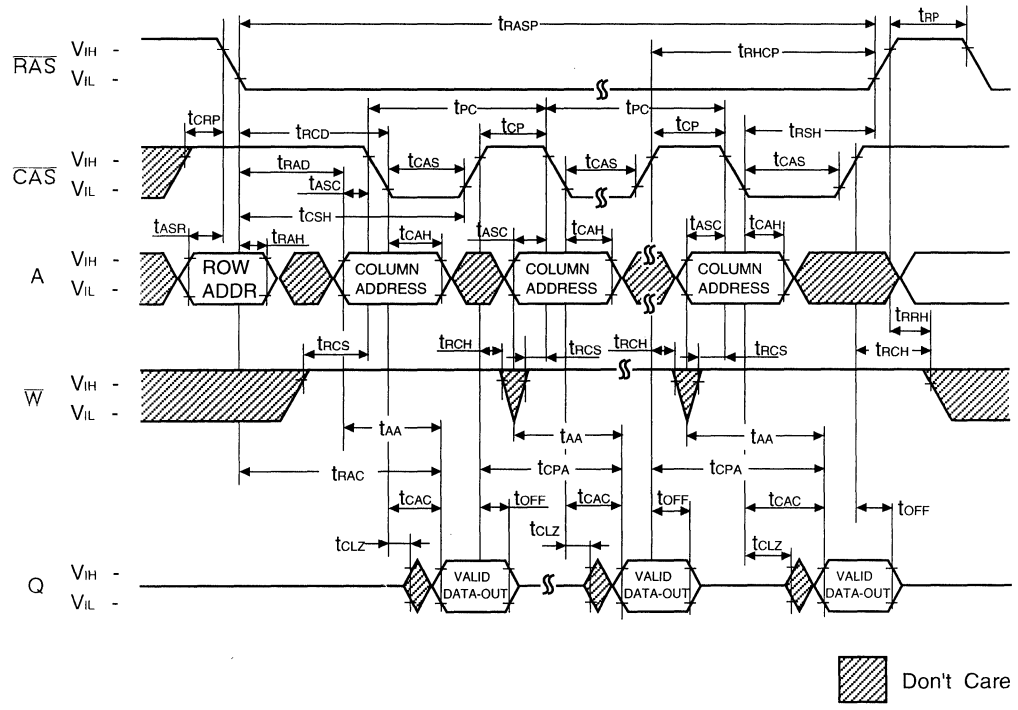
WRITE CYCLE (EARLY WRITE)



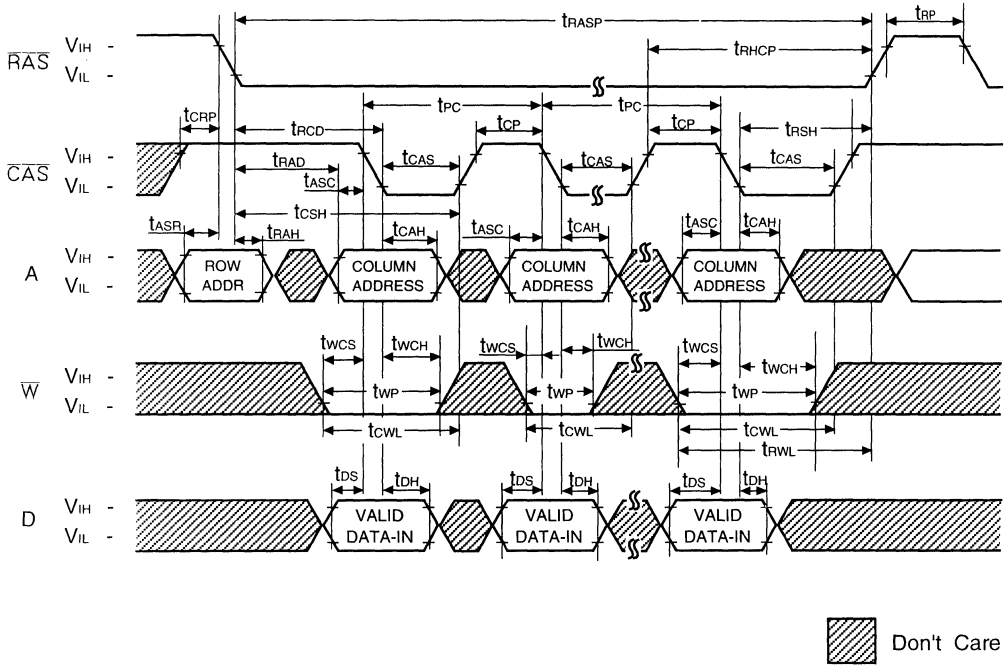
READ-WRITE / READ - MODIFY - WRITE CYCLE



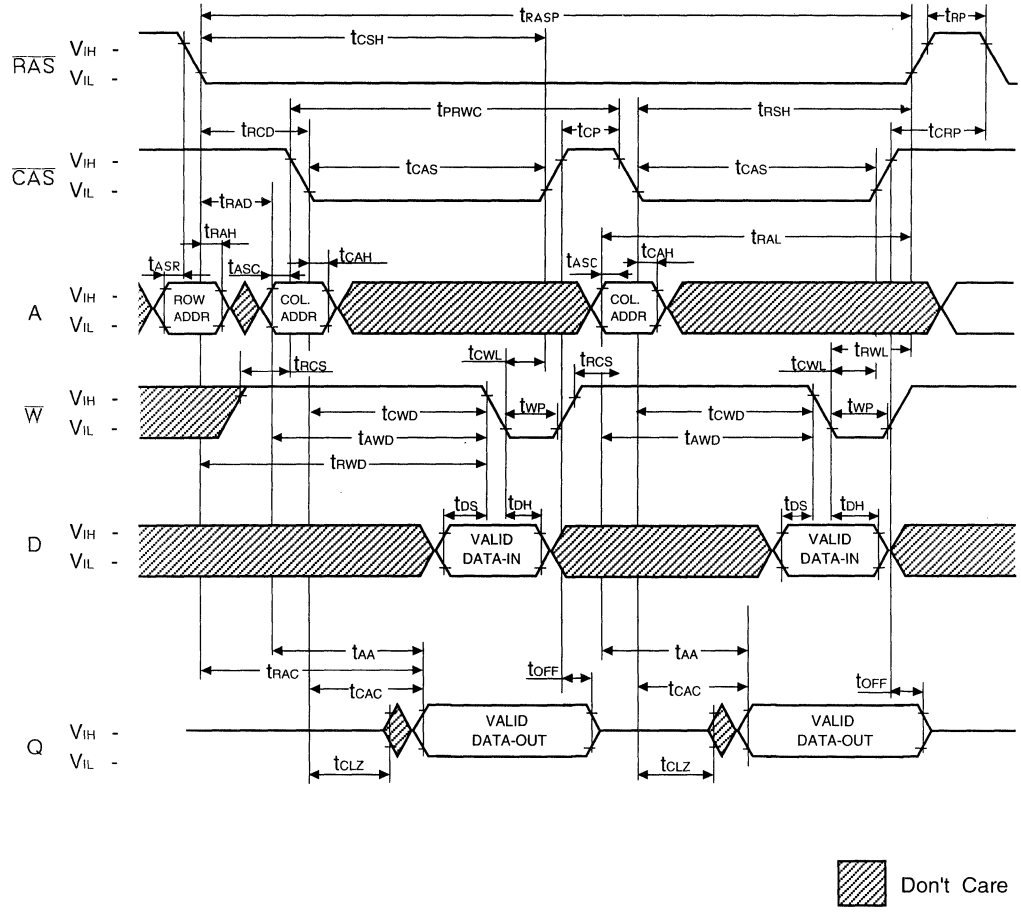
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

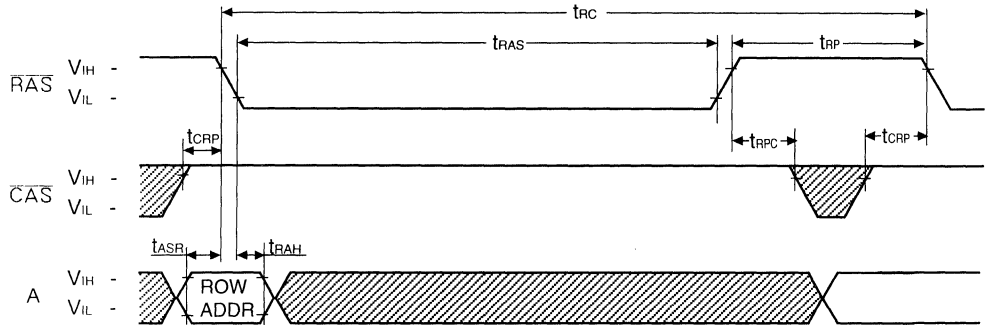


FAST PAGE MODE READ-MODIFY-WRITE CYCLE



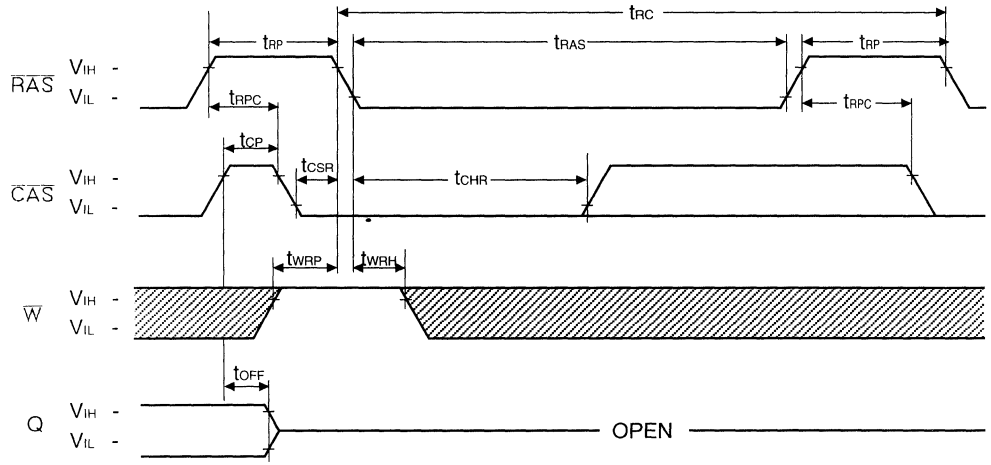
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, D_{IN} = Don't care
D_{OUT} = Open

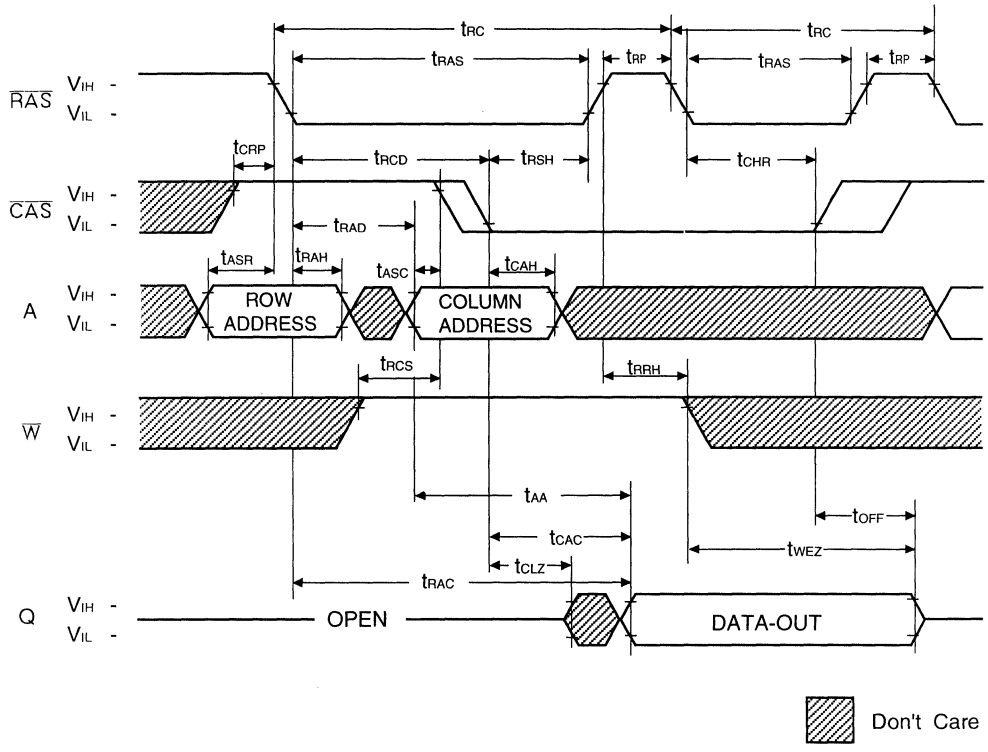


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : A = Don't Care

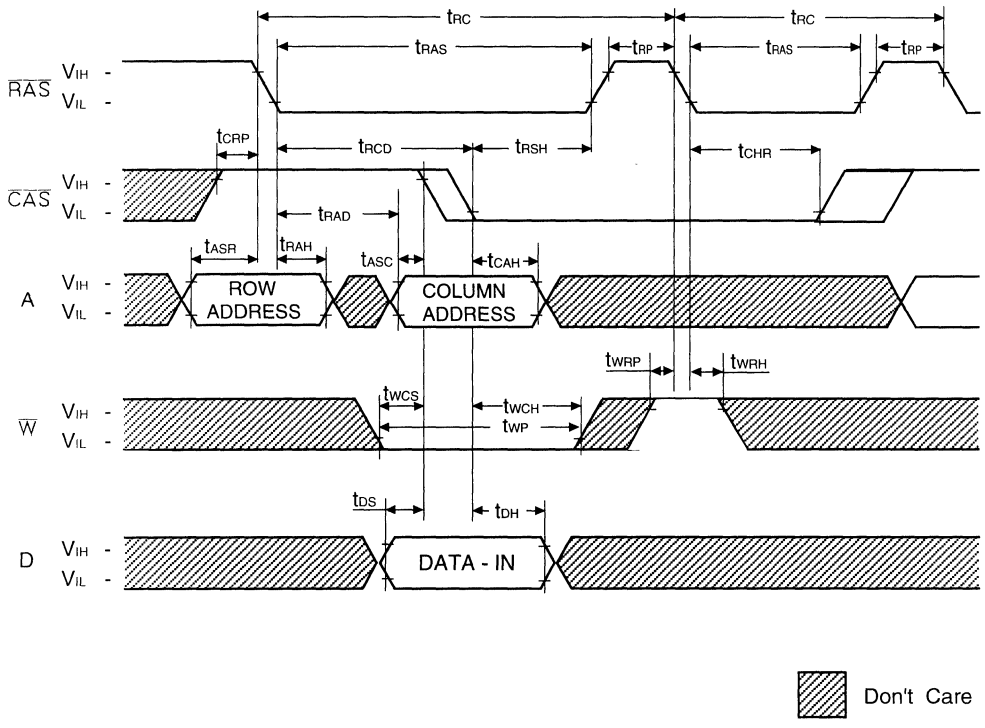


HIDDEN REFRESH CYCLE (READ)

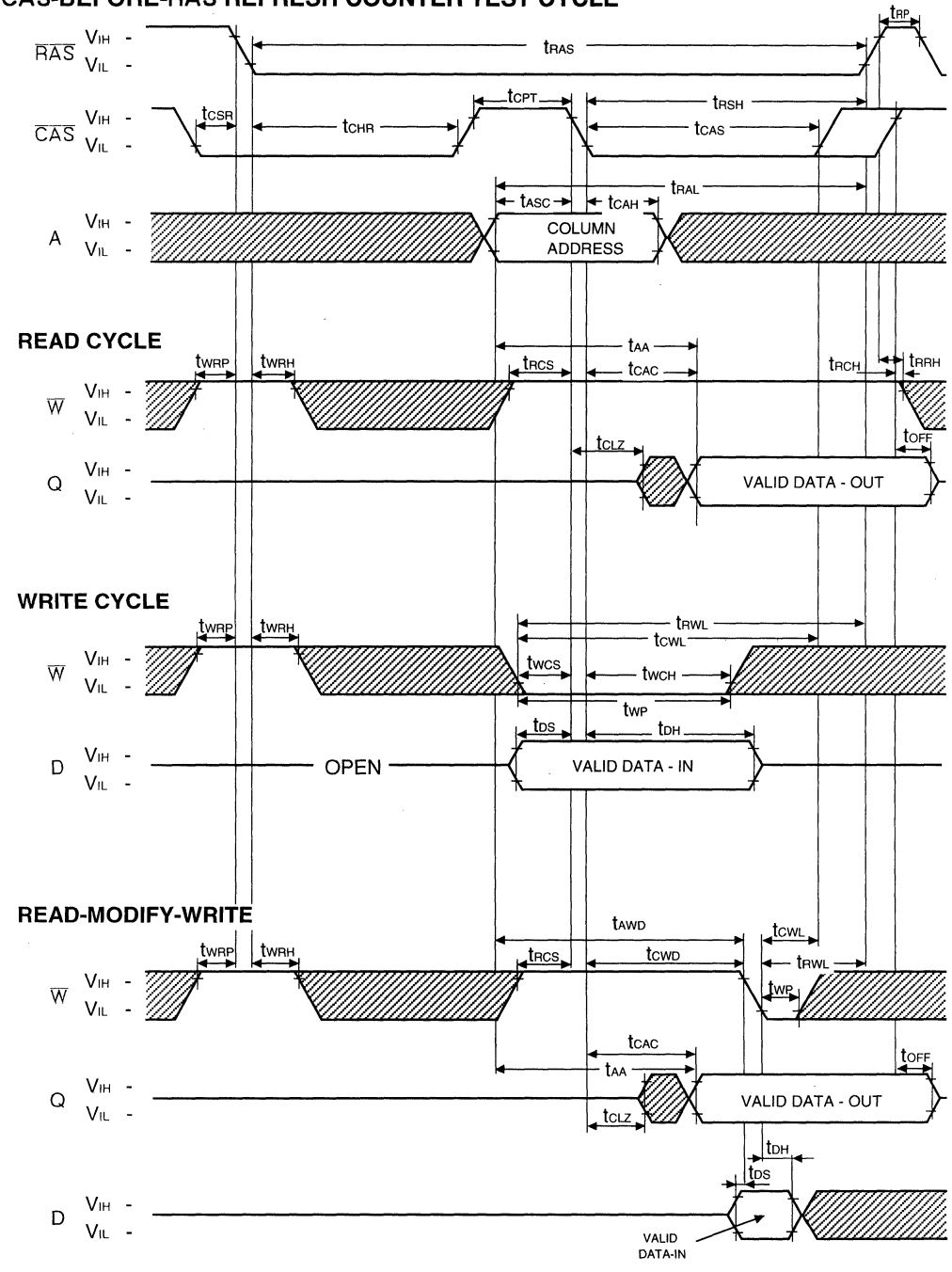


HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN

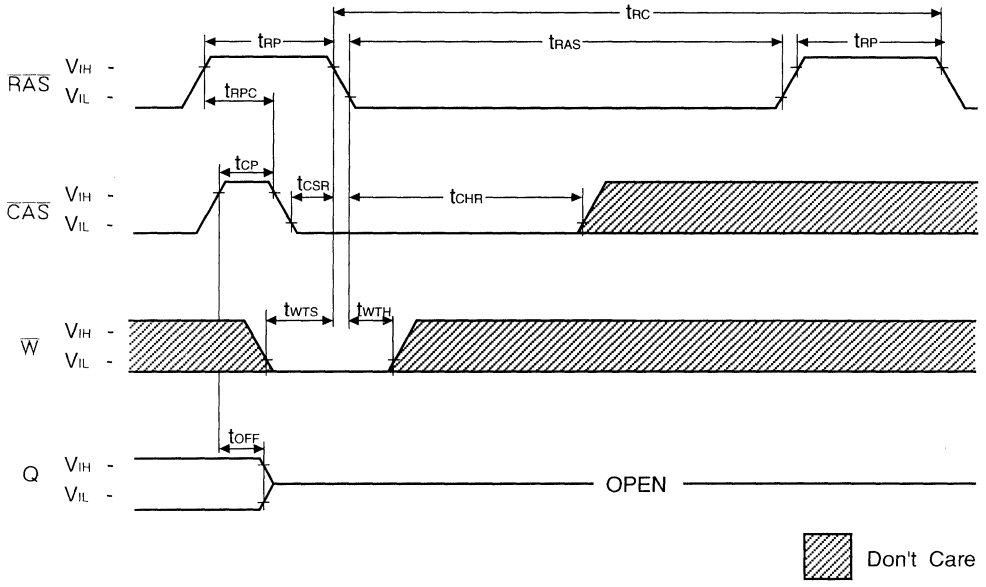


CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



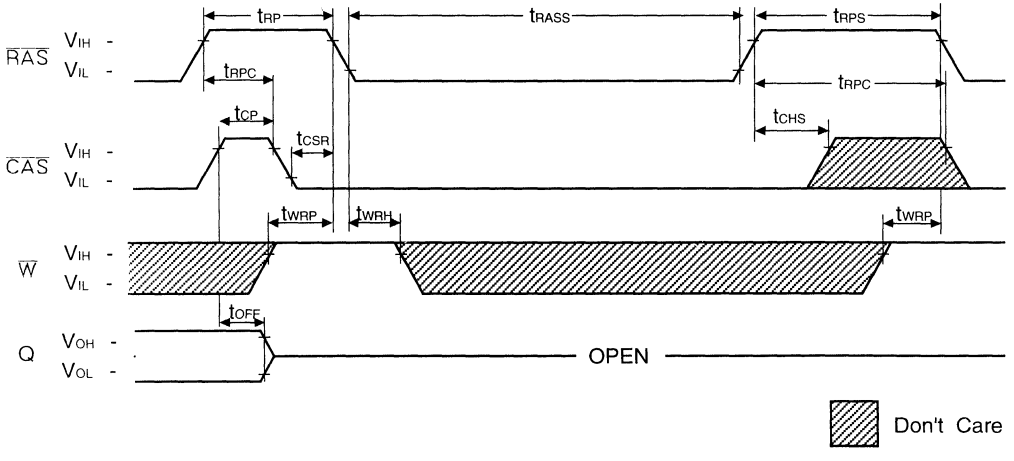
TEST MODE IN CYCLE

NOTE : D, A = Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE

NOTE : Address = Don't Care



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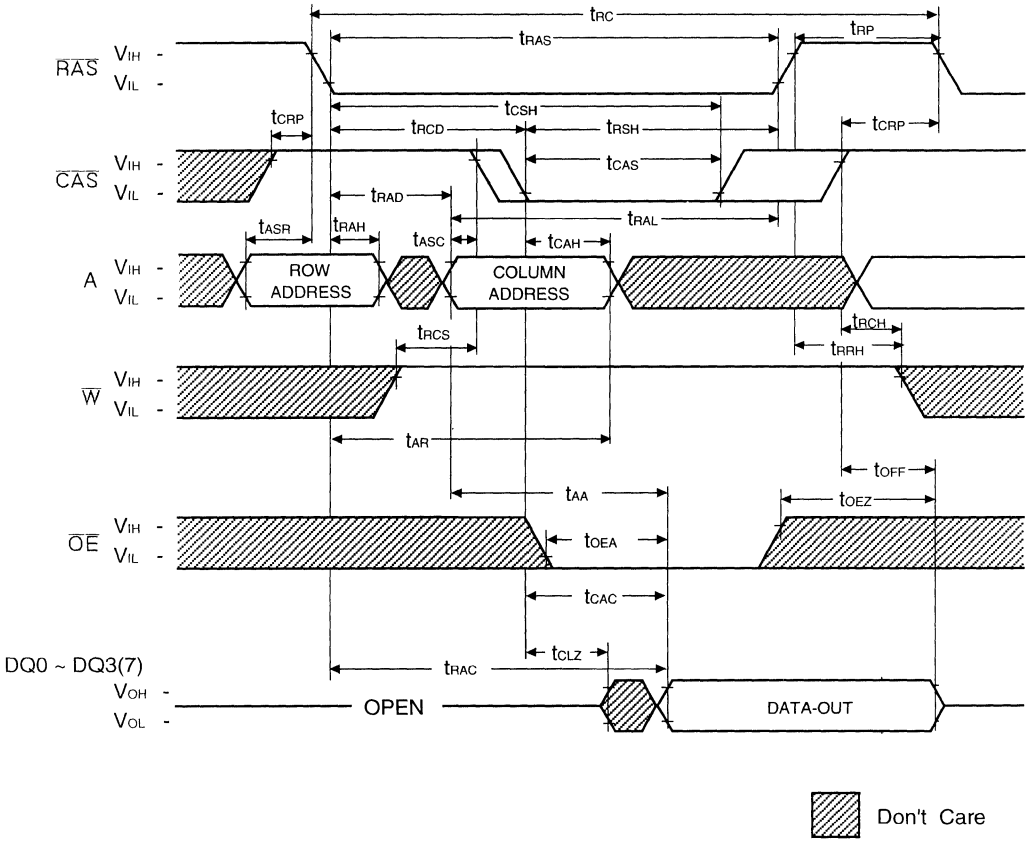
Fast page Mode, x4 and x8 Device

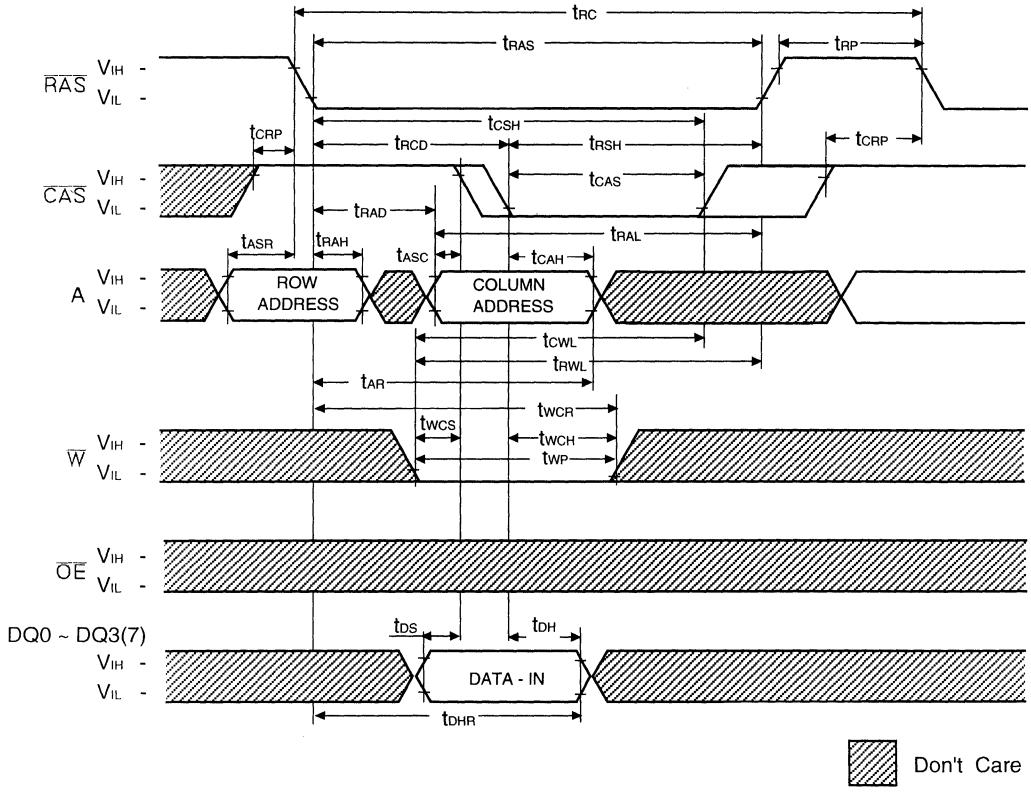
TIMING DIAGRAM

READ CYCLE



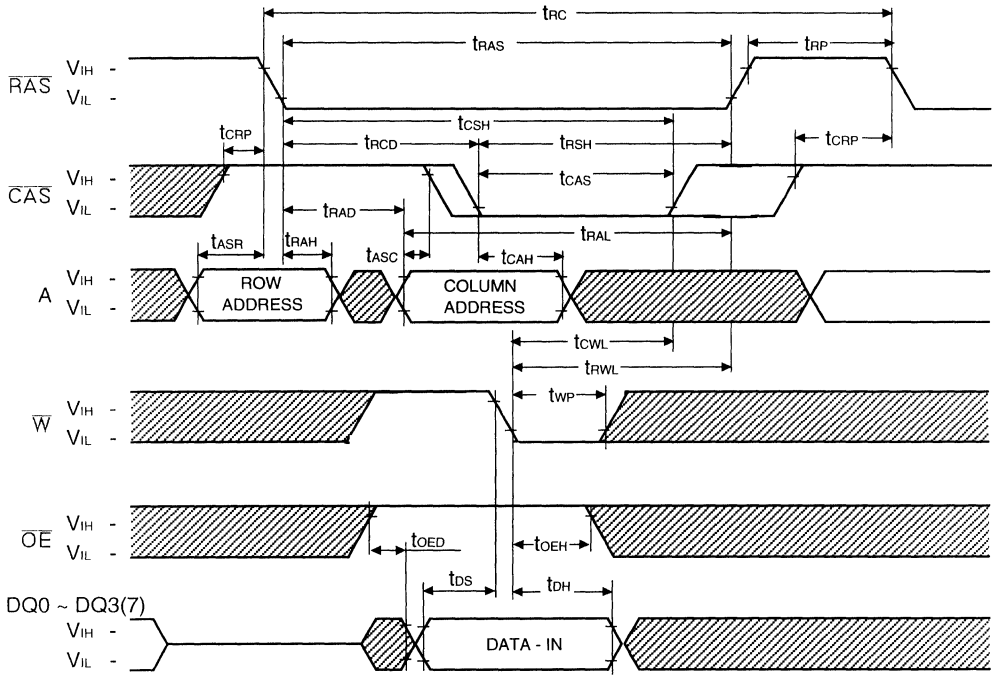
WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



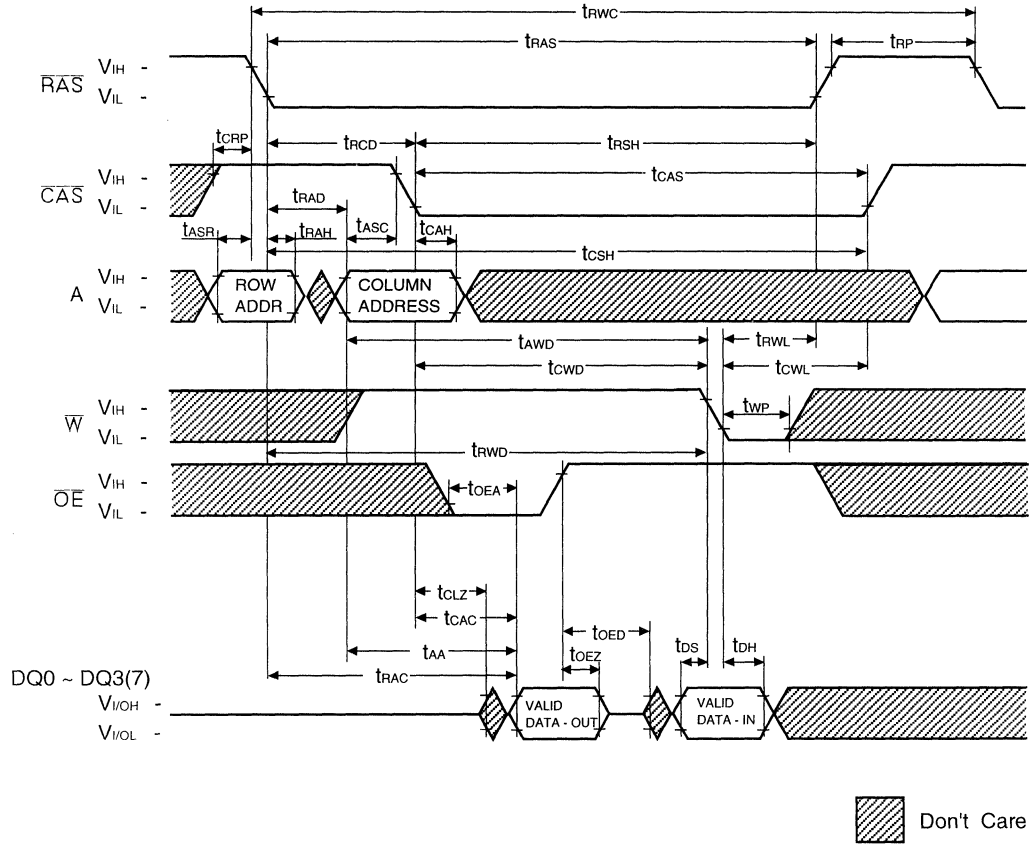
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



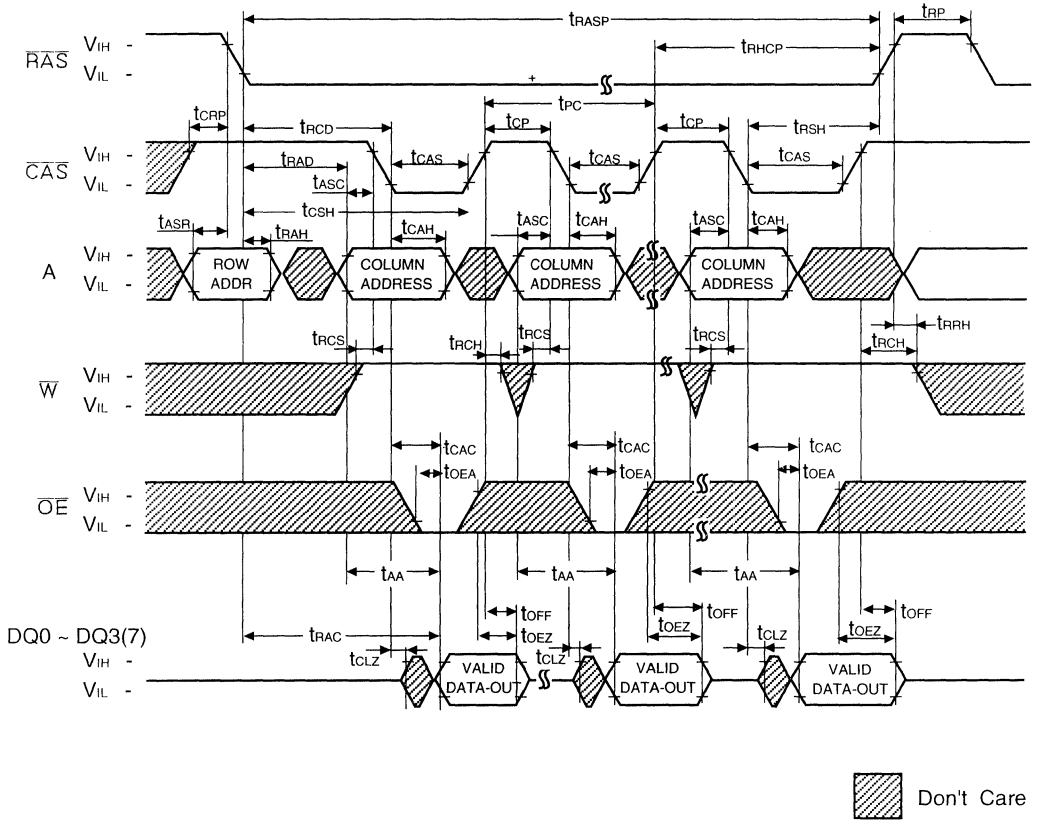
Don't Care

READ - MODIFY - WRITE CYCLE



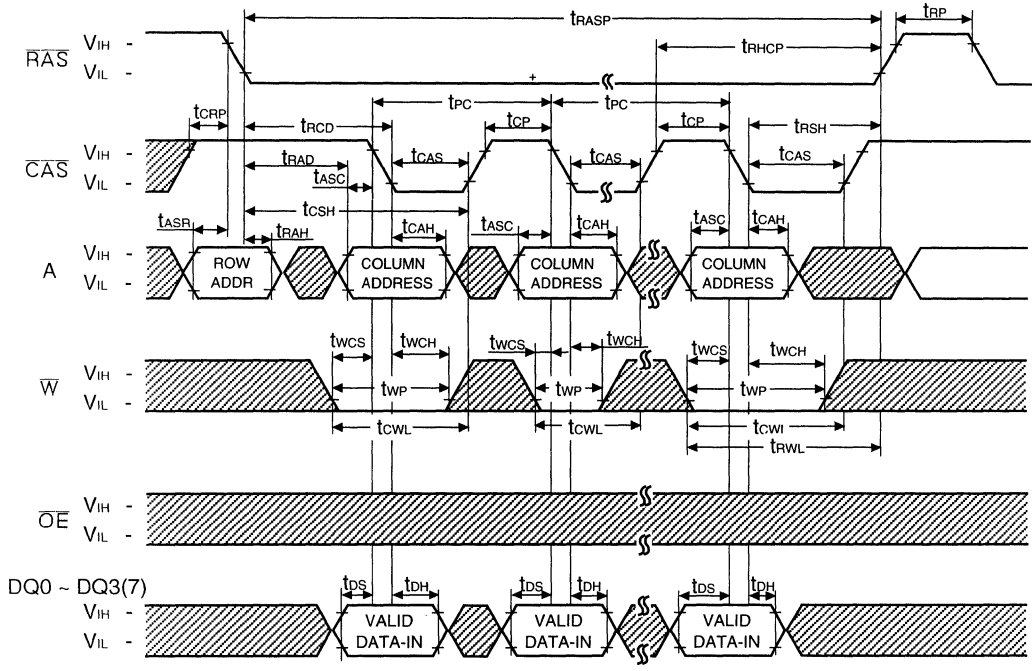
FAST PAGE READ CYCLE

NOTE : D_{OUT} = Open

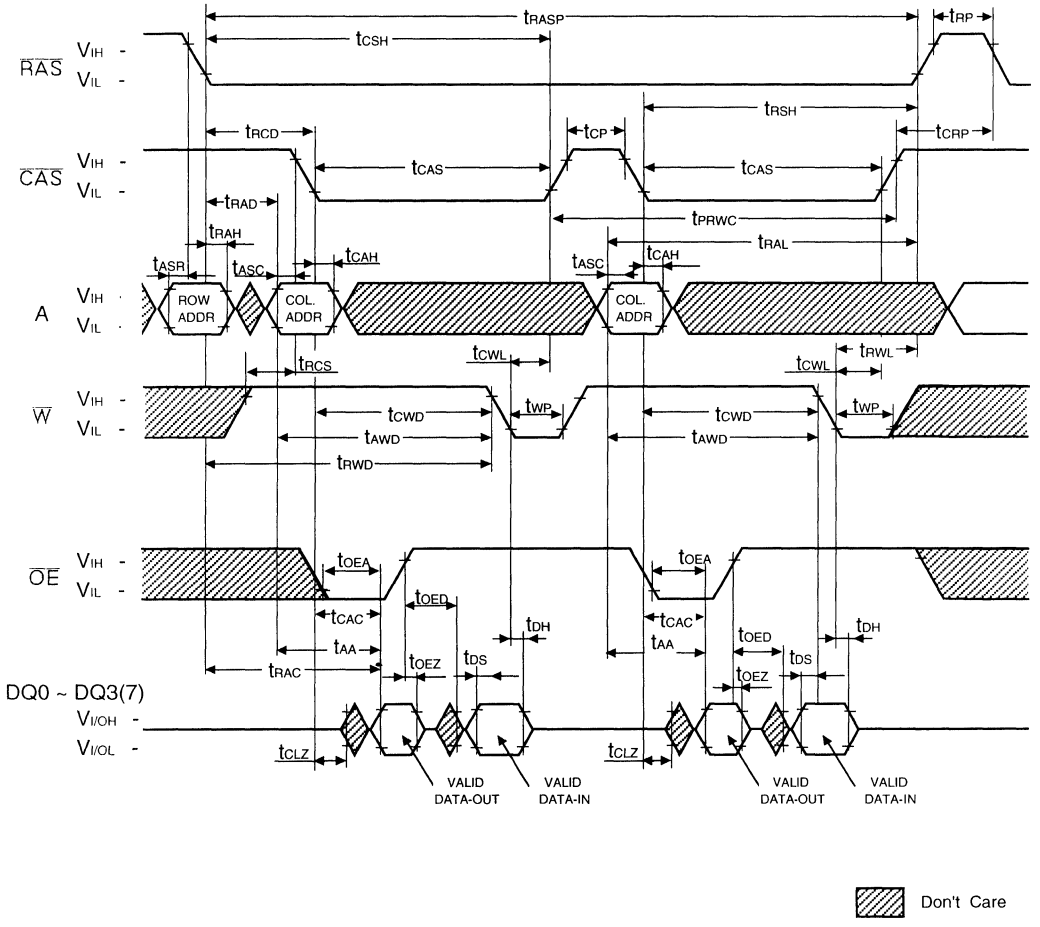


FAST PAGE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



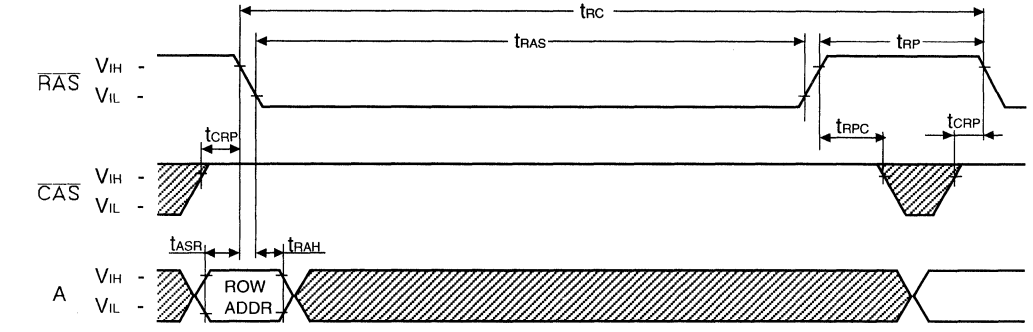
FAST PAGE READ-MODIFY-WRITE CYCLE



SAMSUNG ELECTRONICS

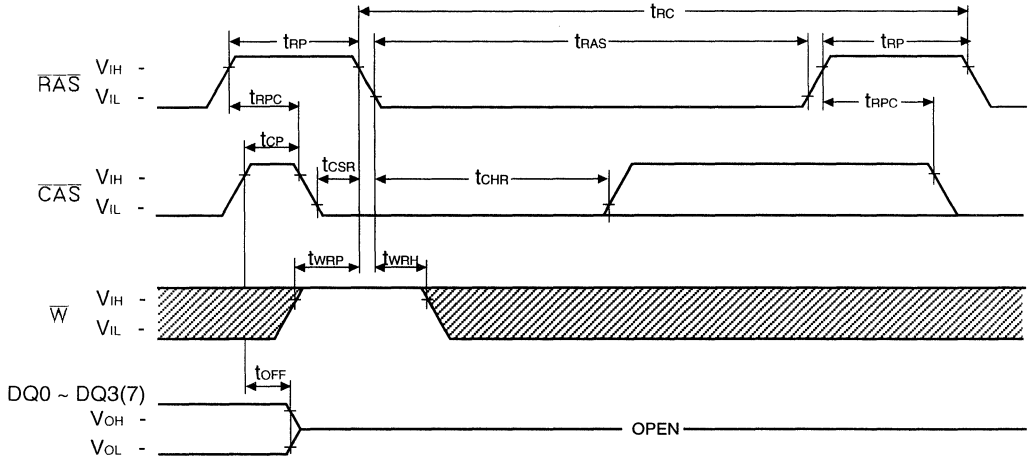
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open

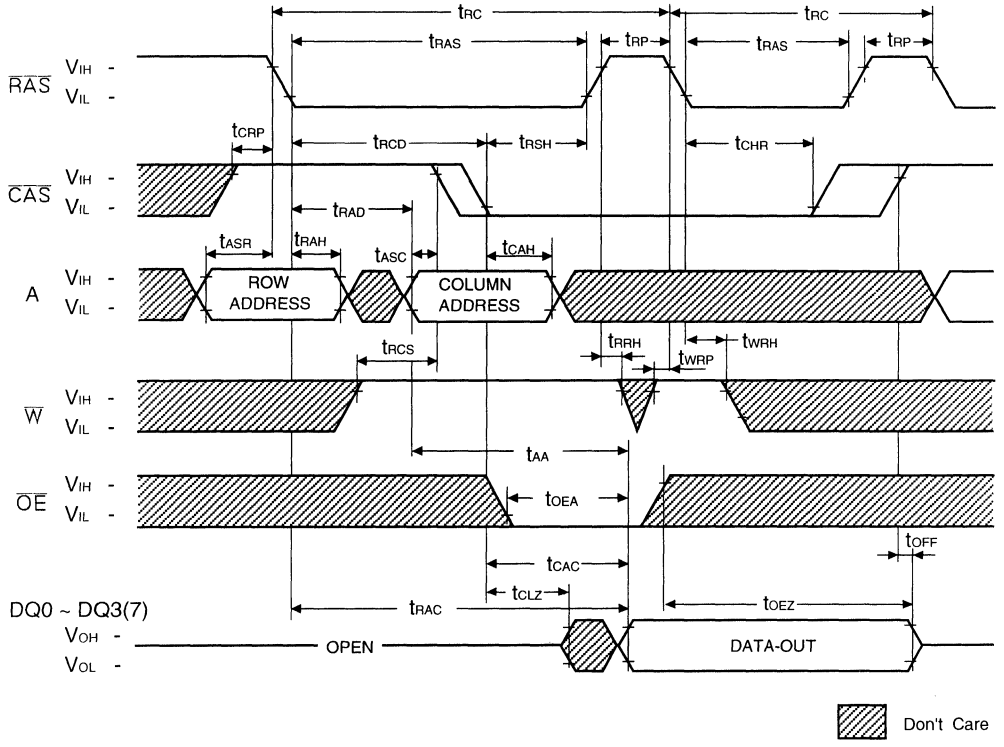


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't Care

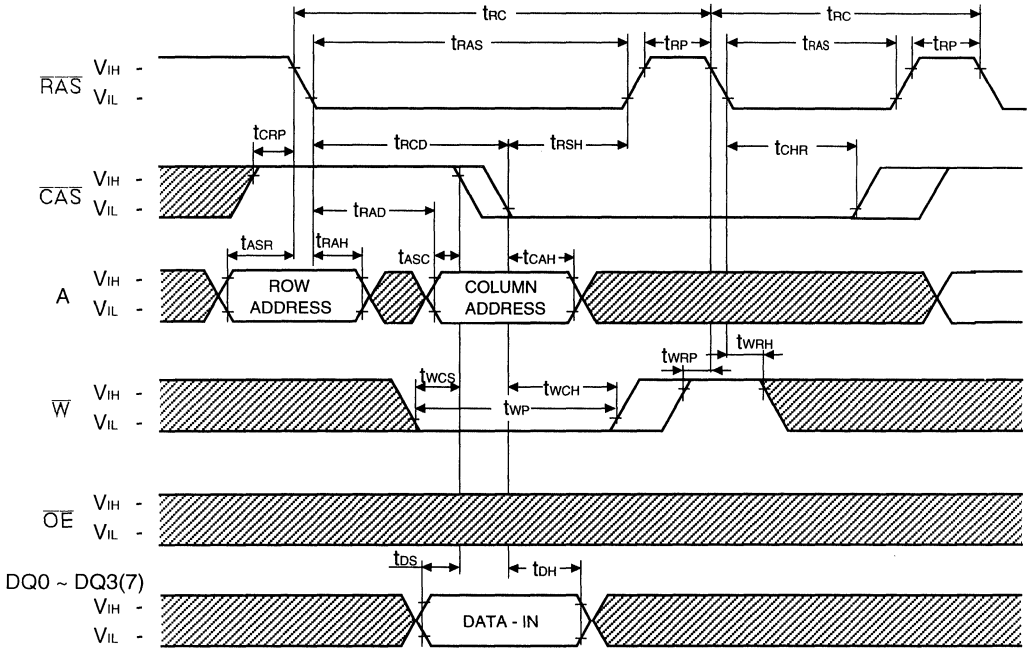


HIDDEN REFRESH CYCLE (READ)



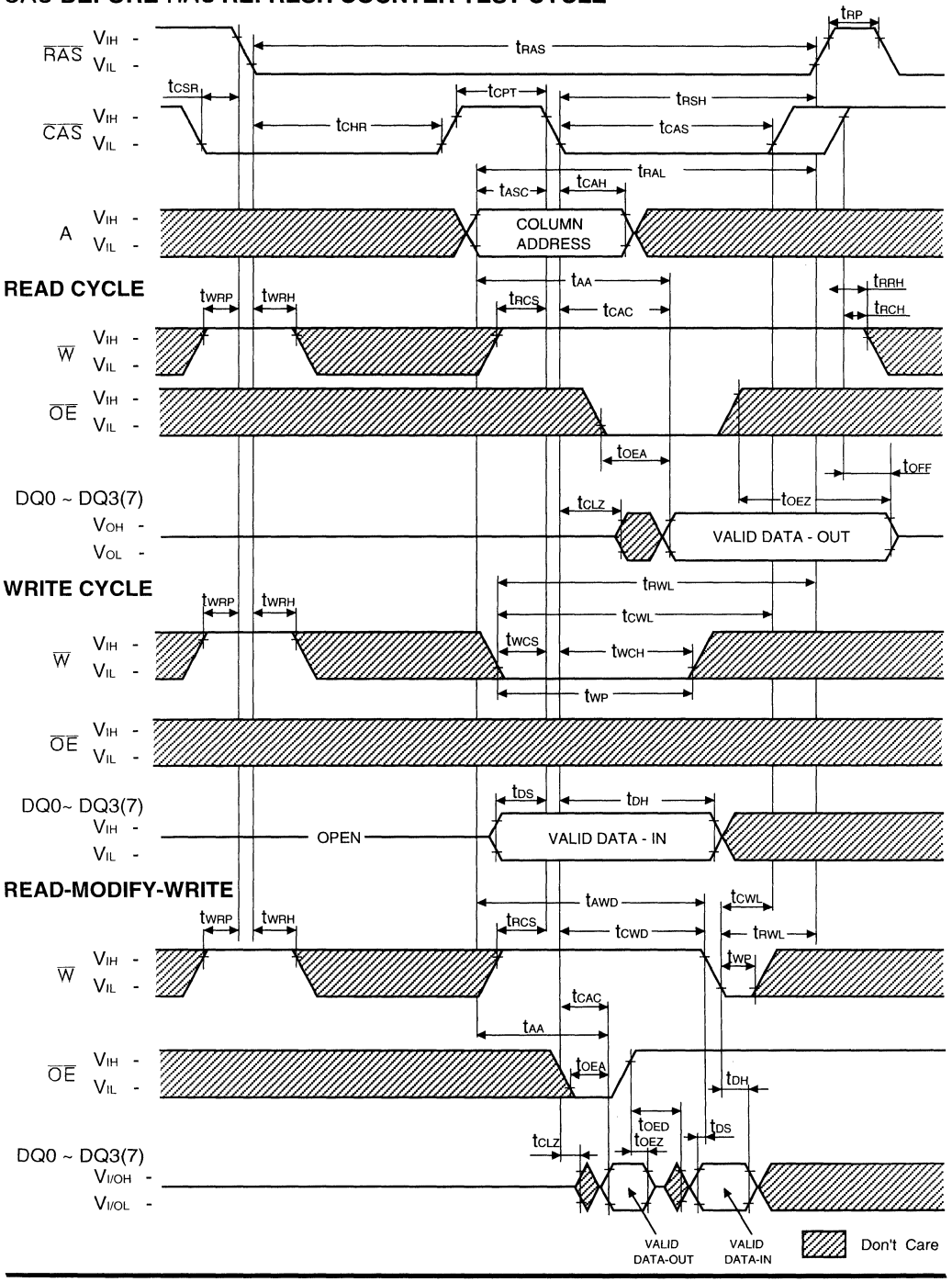
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



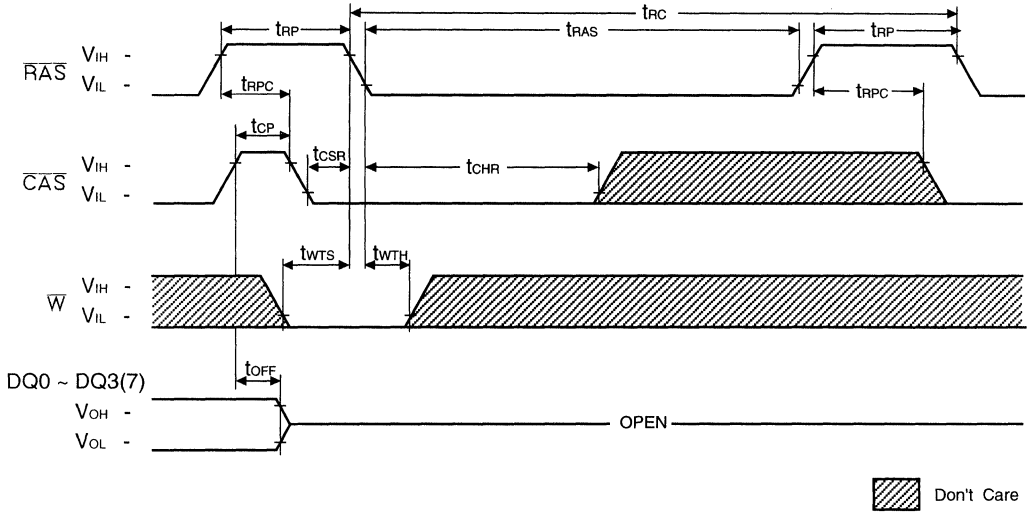
Don't Care

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



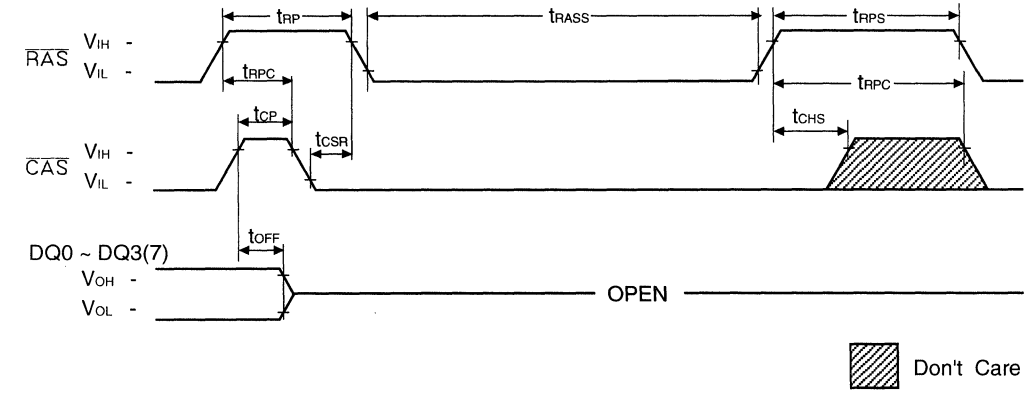
TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{W}$= VIH (1Mx4, 4Mx4, 16Mx4, 2Mx8, 8Mx8)
Don't Care (512Kx8)
$\overline{OE}$, A = Don't Care

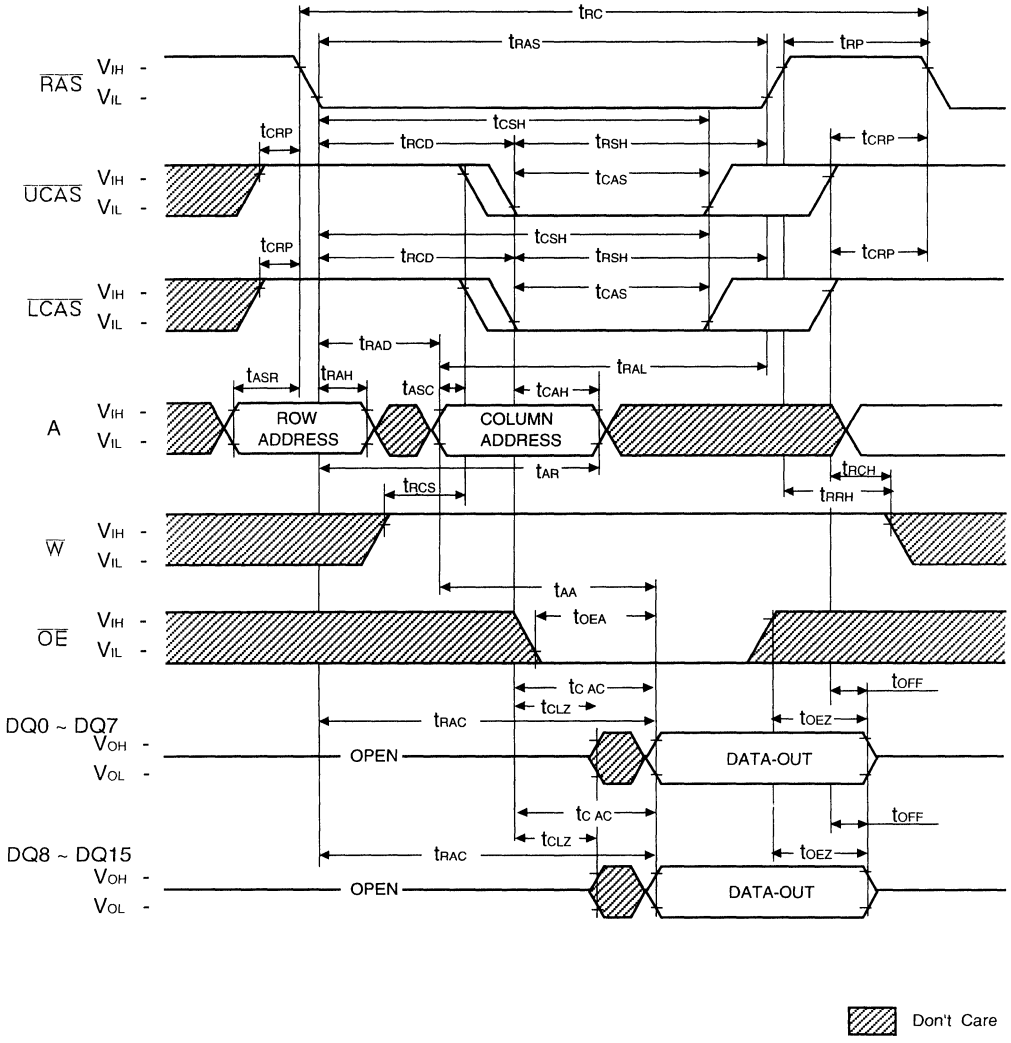


Fast page Mode, x16(2$\overline{CAS}$) Device

TIMING DIAGRAM

WORD READ CYCLE

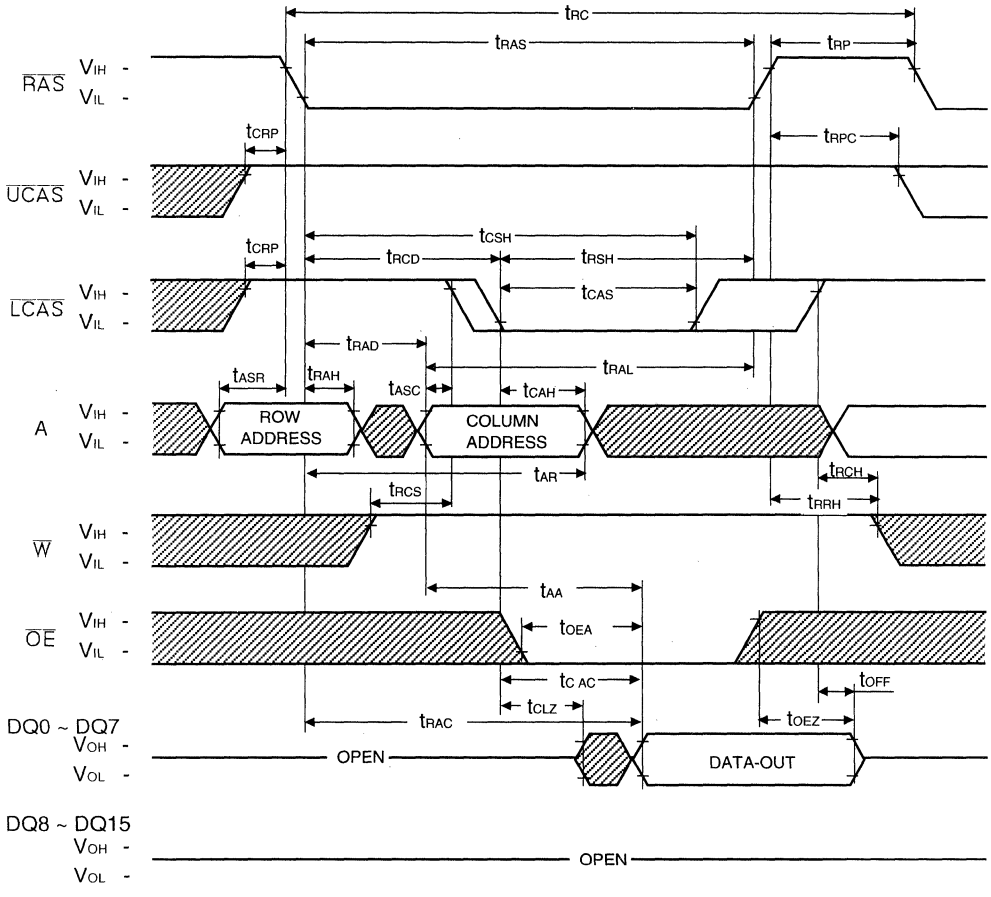
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

LOWER BYTE READ CYCLE

NOTE : D_{IN} = OPEN

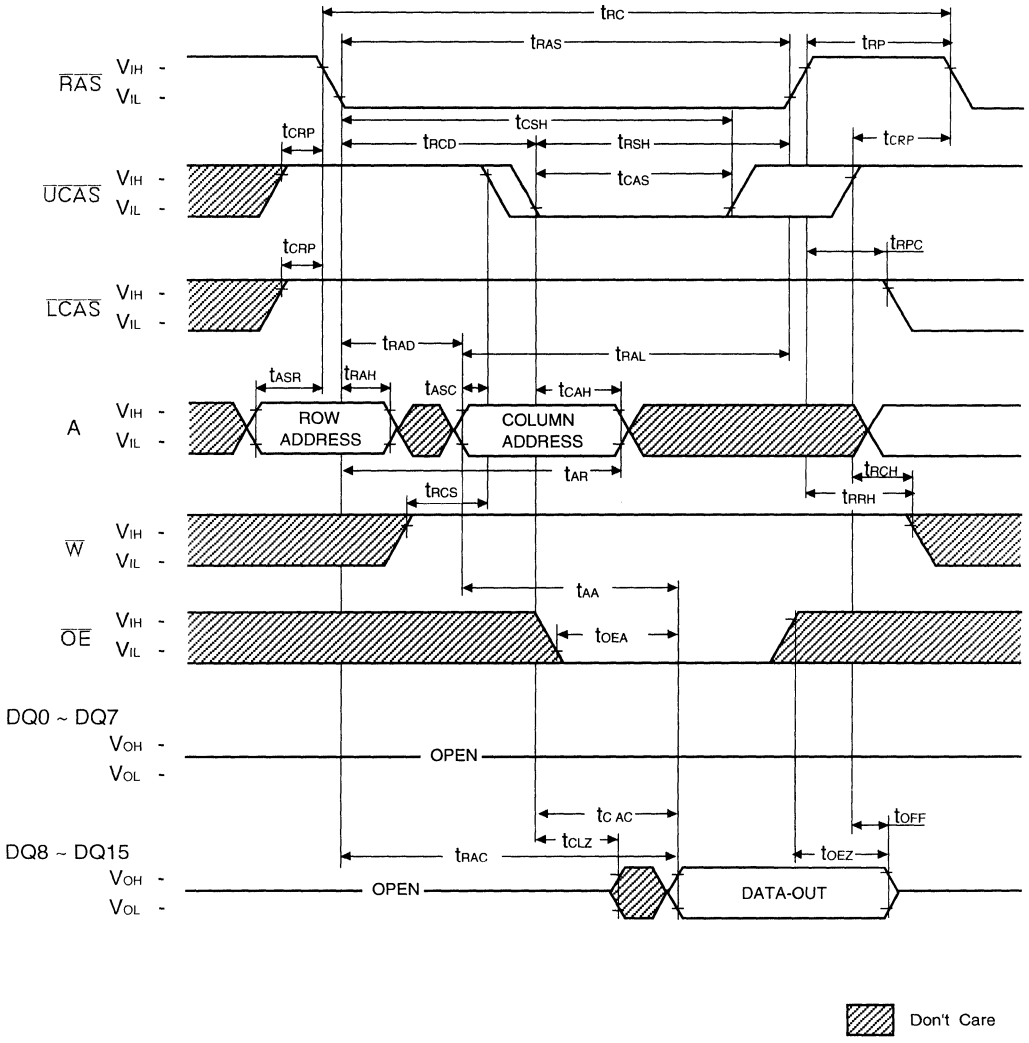


Don't Care

TIMING DIAGRAM

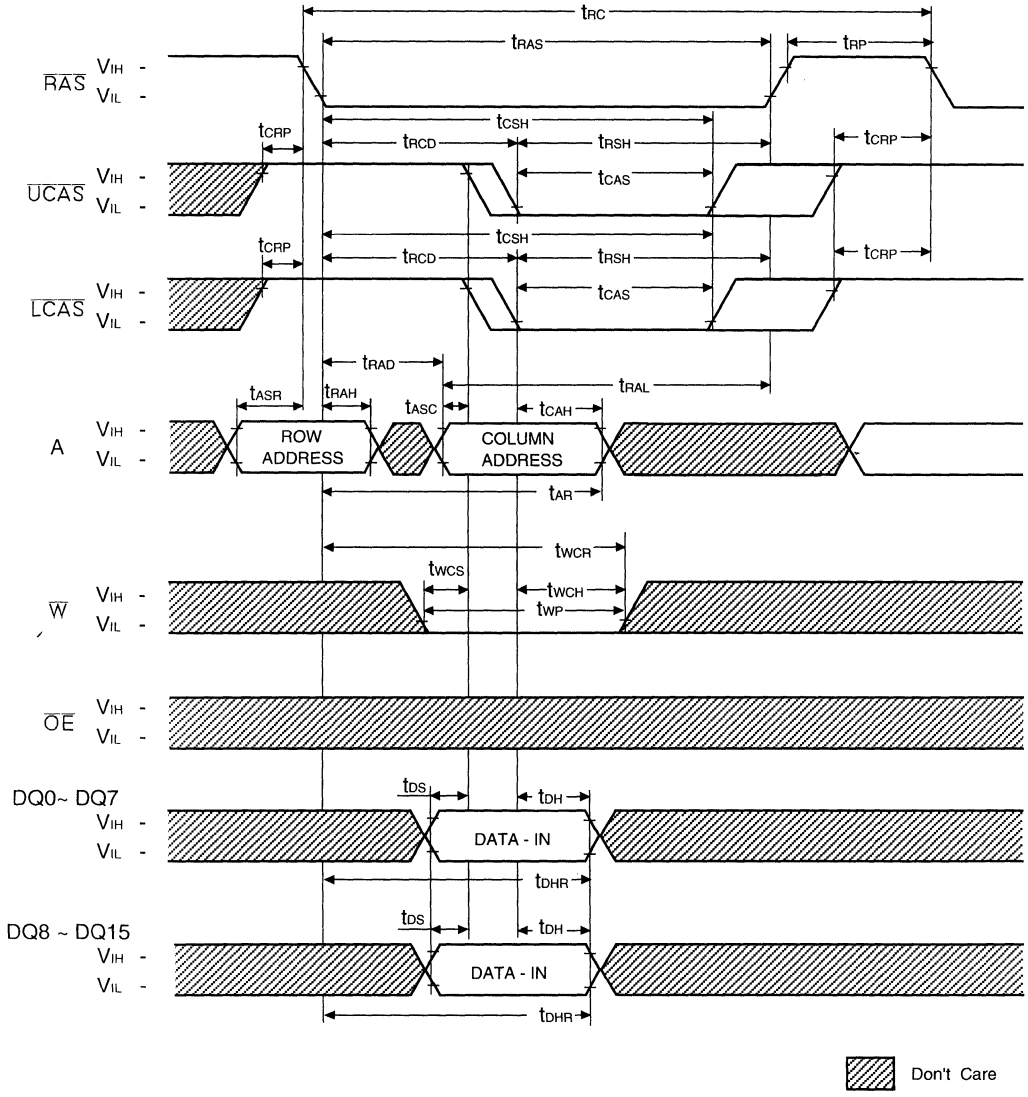
UPPER BYTE READ CYCLE

NOTE : D_{IN} = OPEN



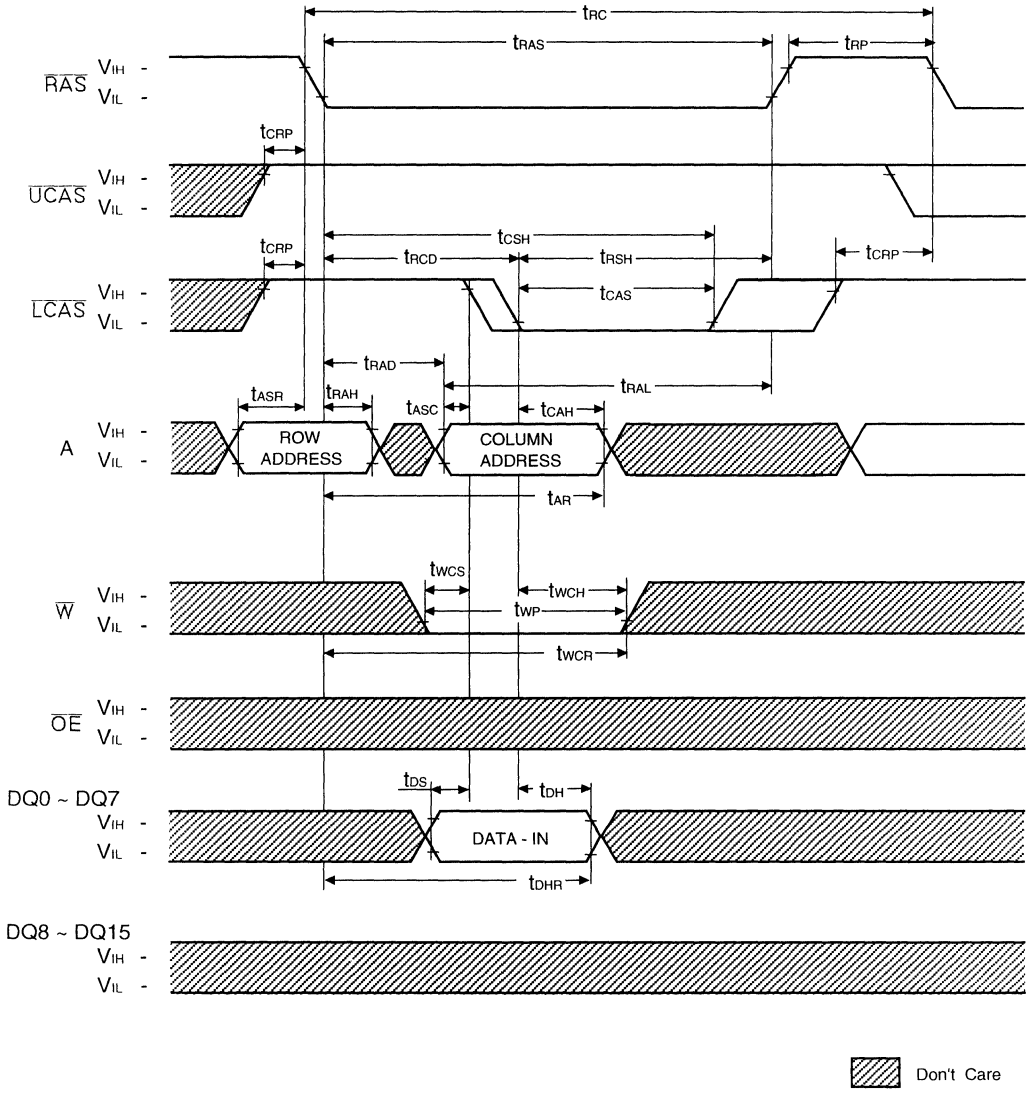
WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN

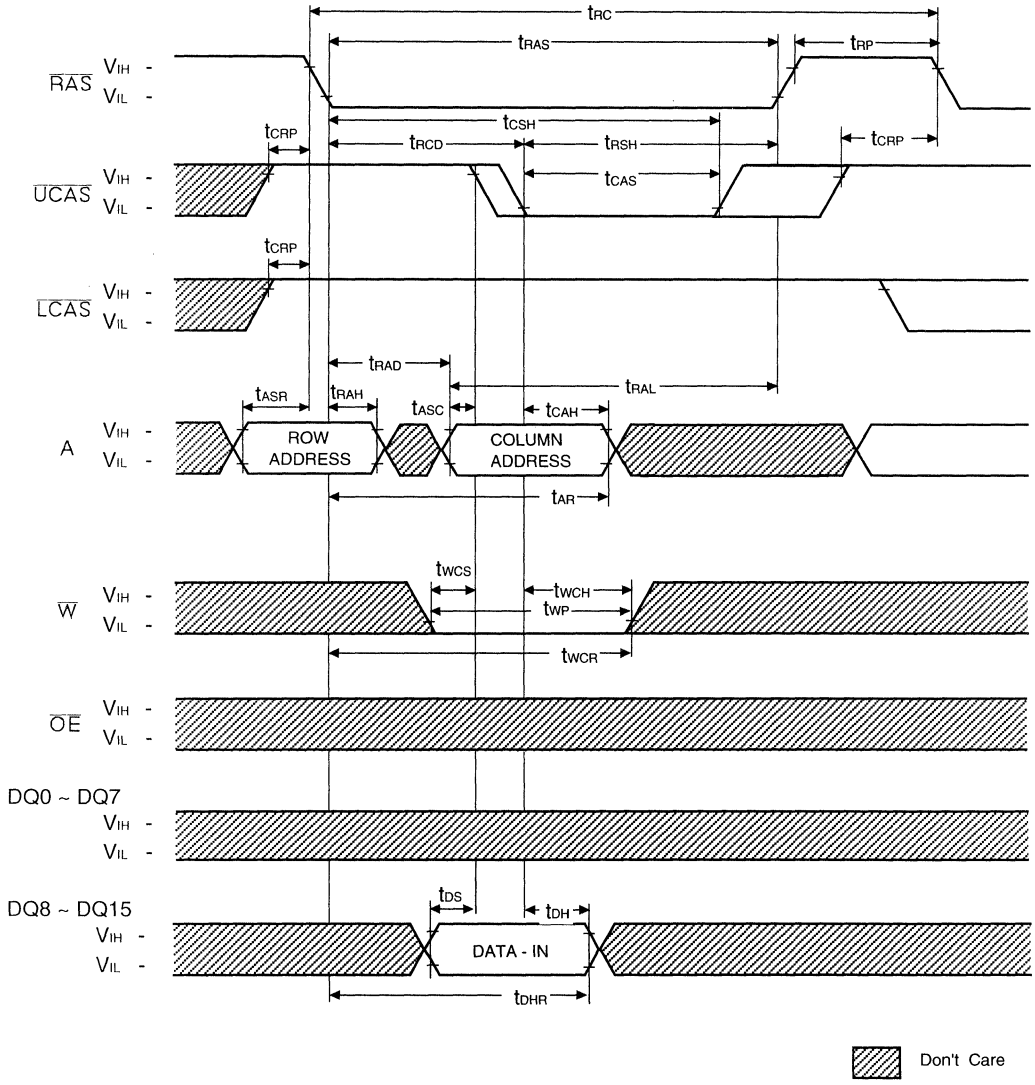


Don't Care

SAMSUNG ELECTRONICS

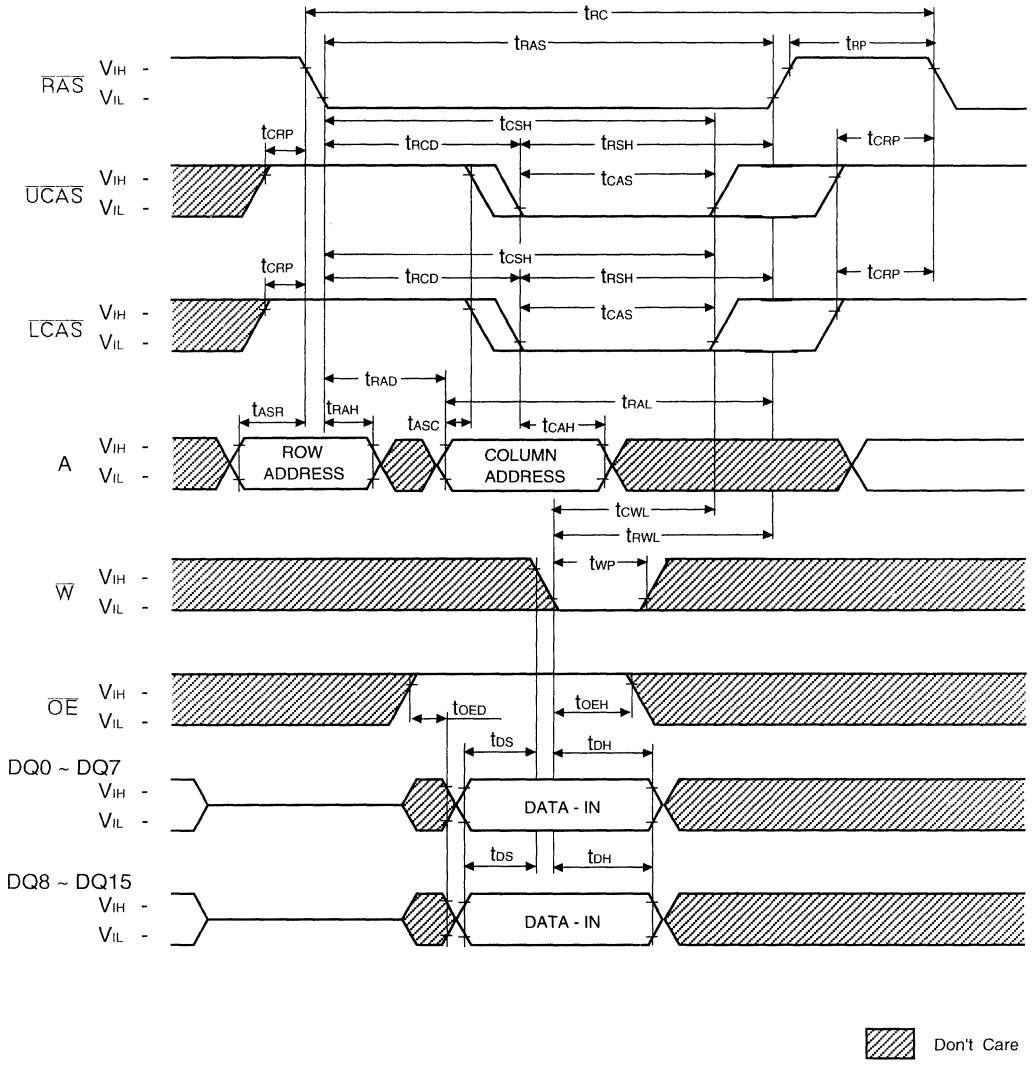
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



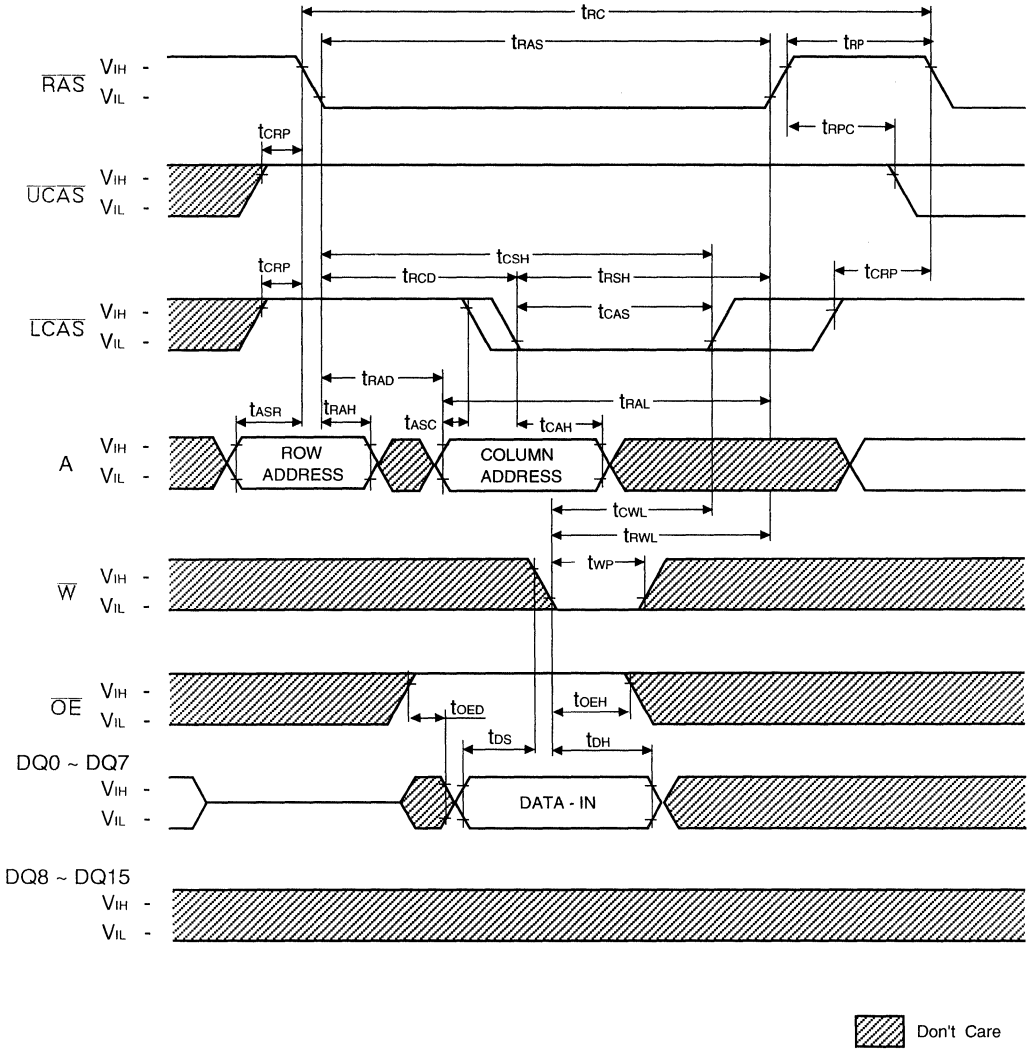
WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

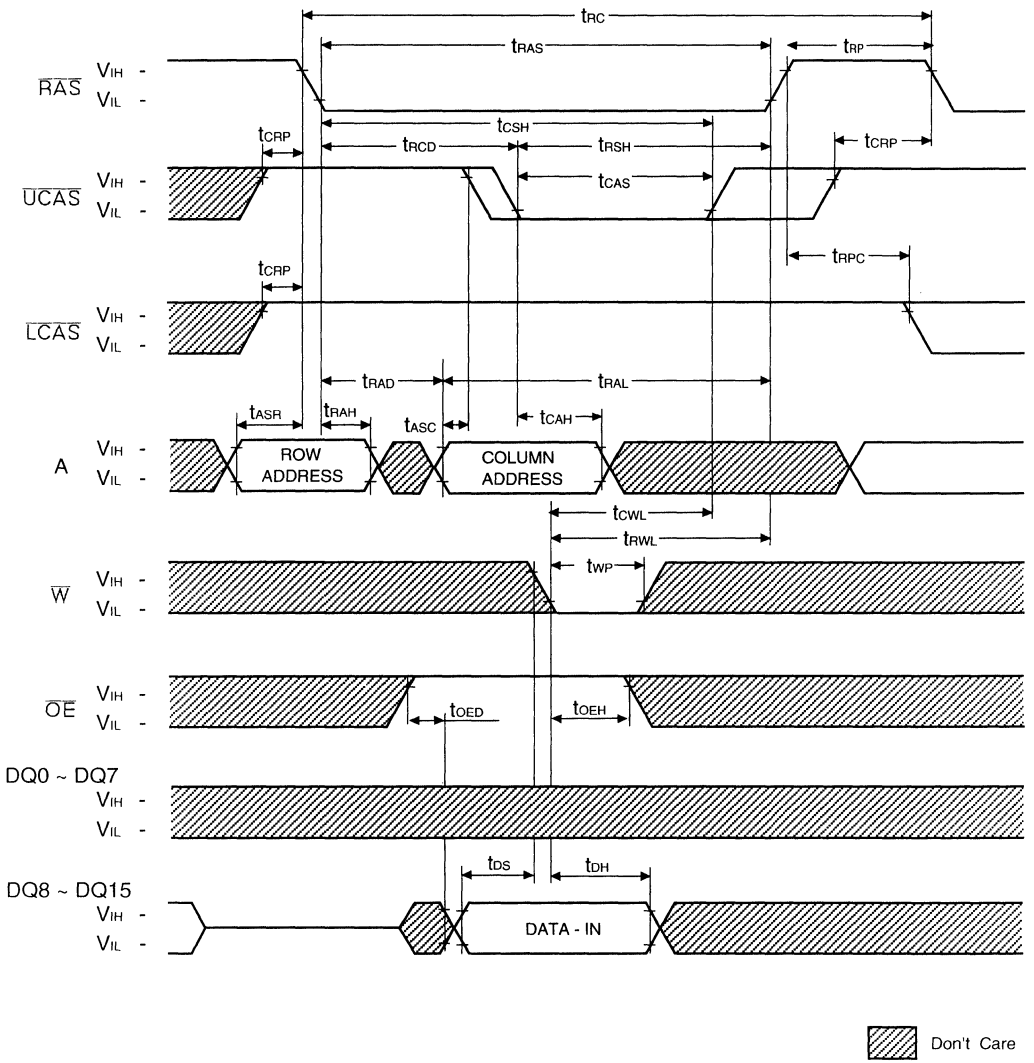
NOTE : D_{OUT} = OPEN



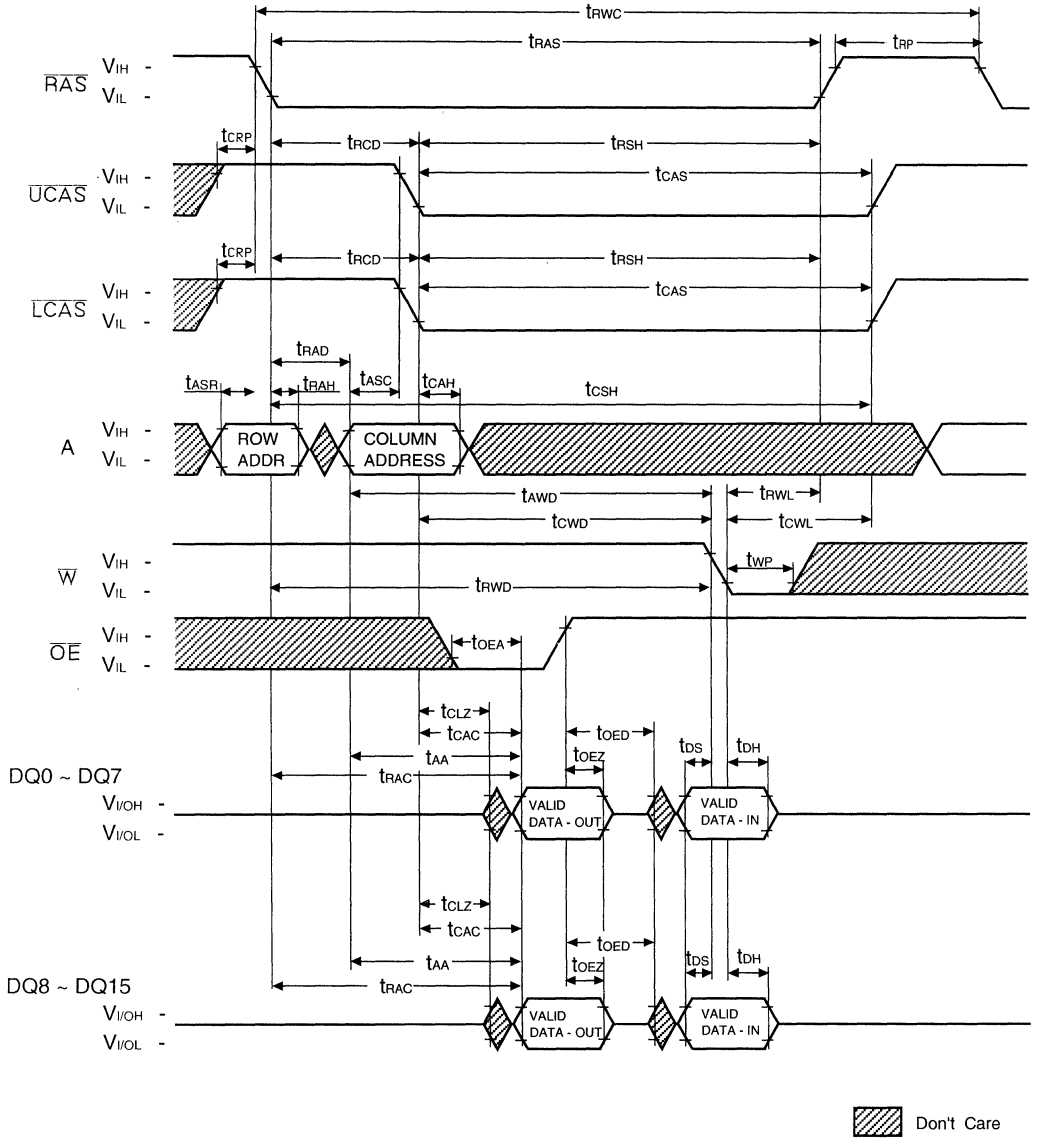
SAMSUNG ELECTRONICS

UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

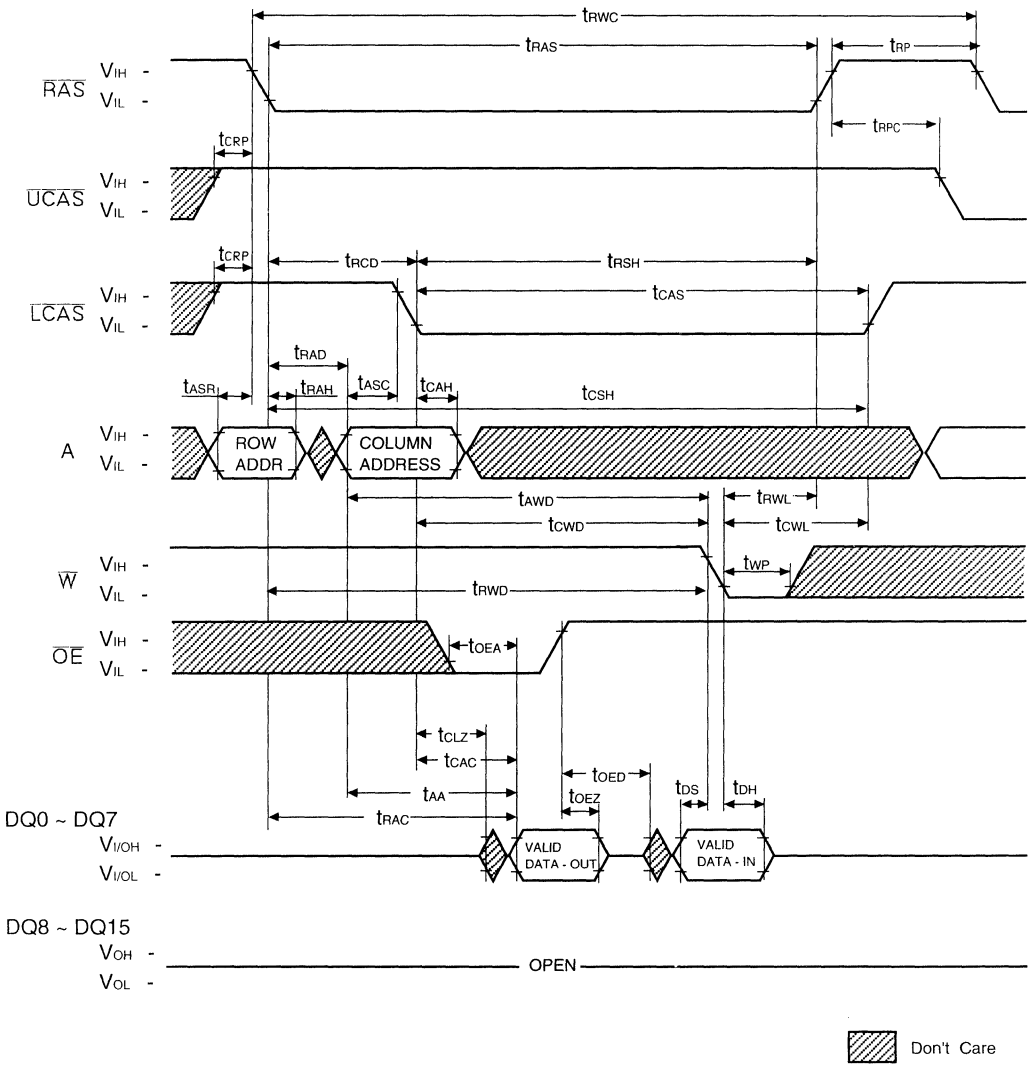
NOTE : D_{OUT} = OPEN



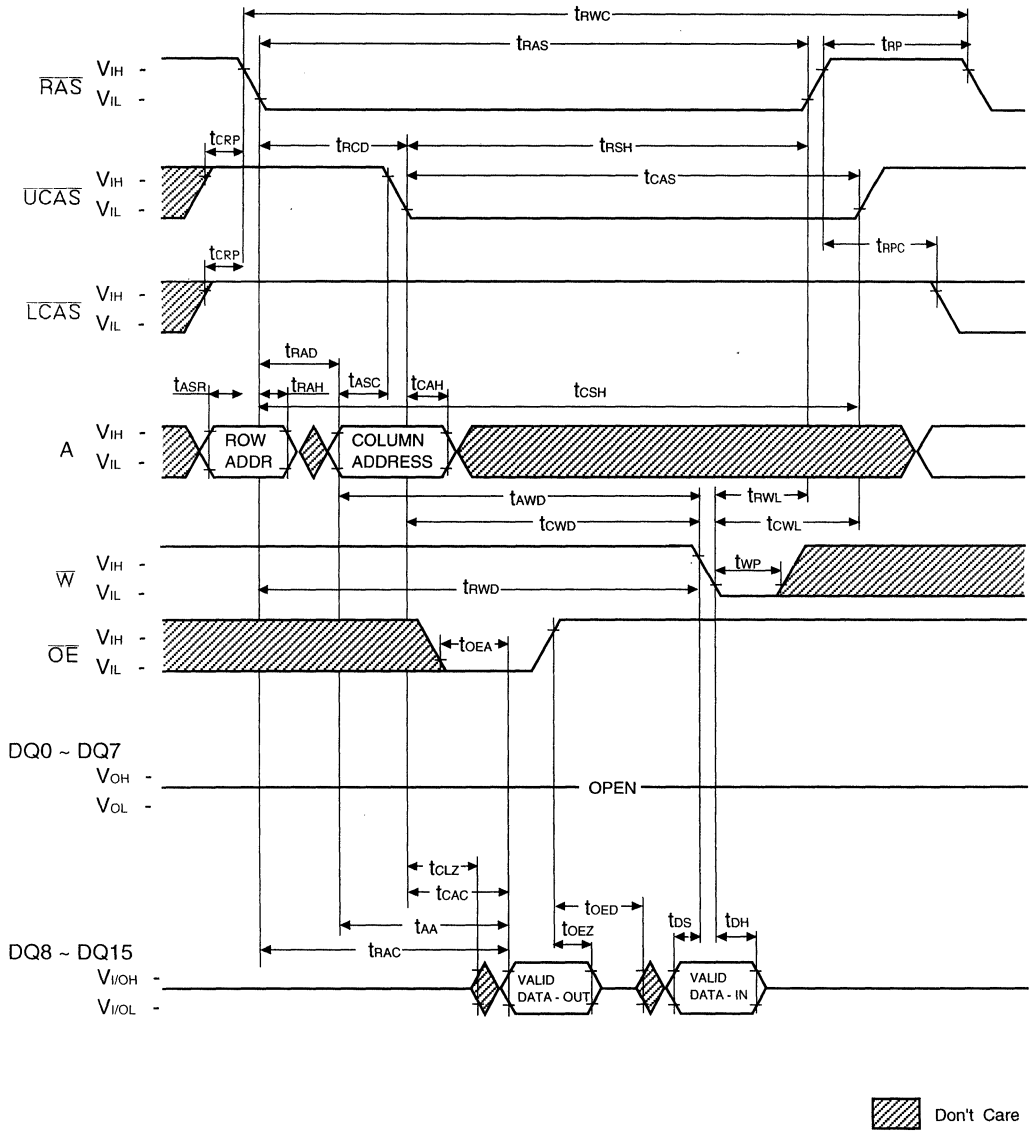
WORD READ - MODIFY - WRITE CYCLE



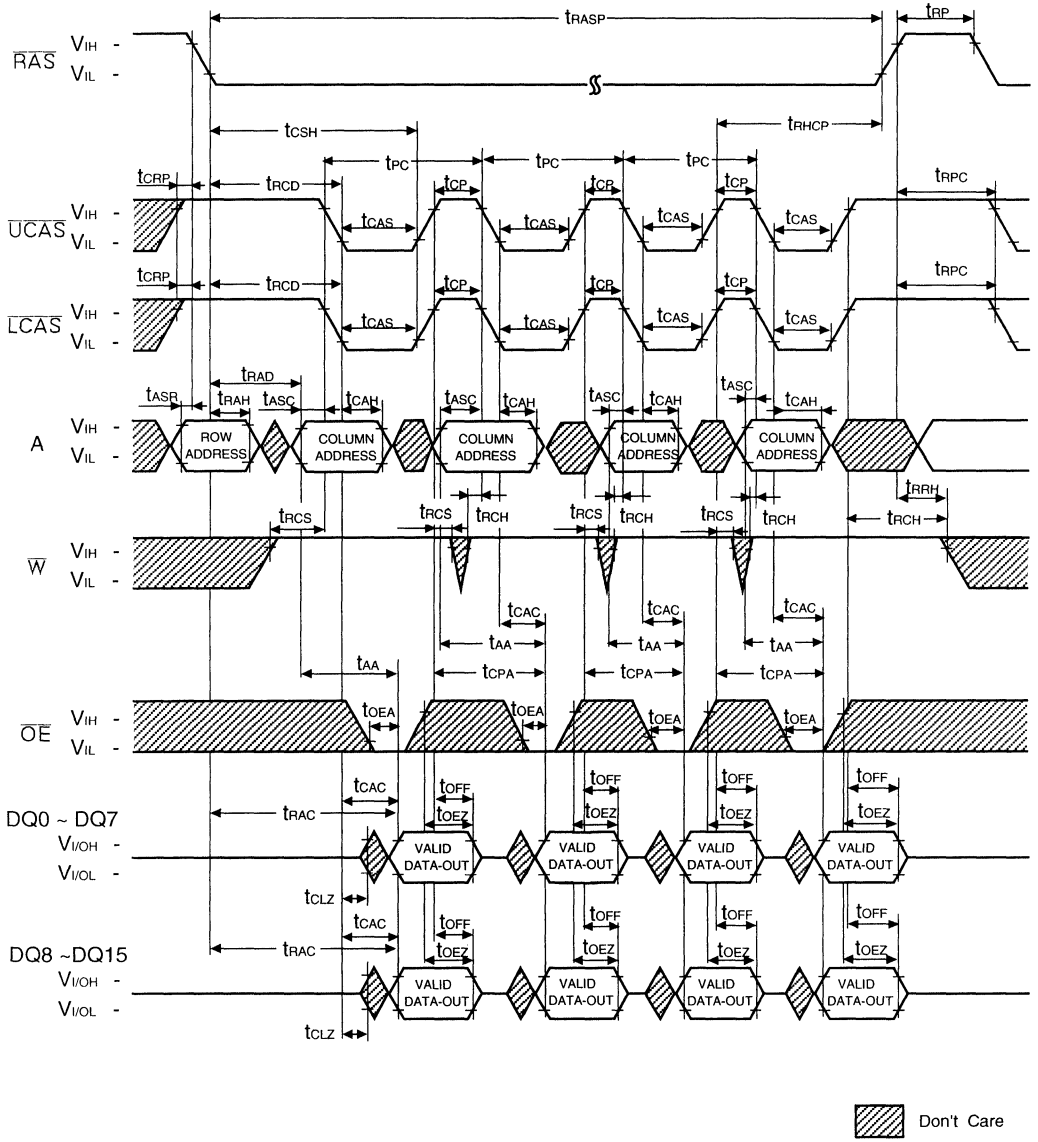
LOWER-BYTE READ - MODIFY - WRITE CYCLE



UPPER-BYTE READ - MODIFY - WRITE CYCLE

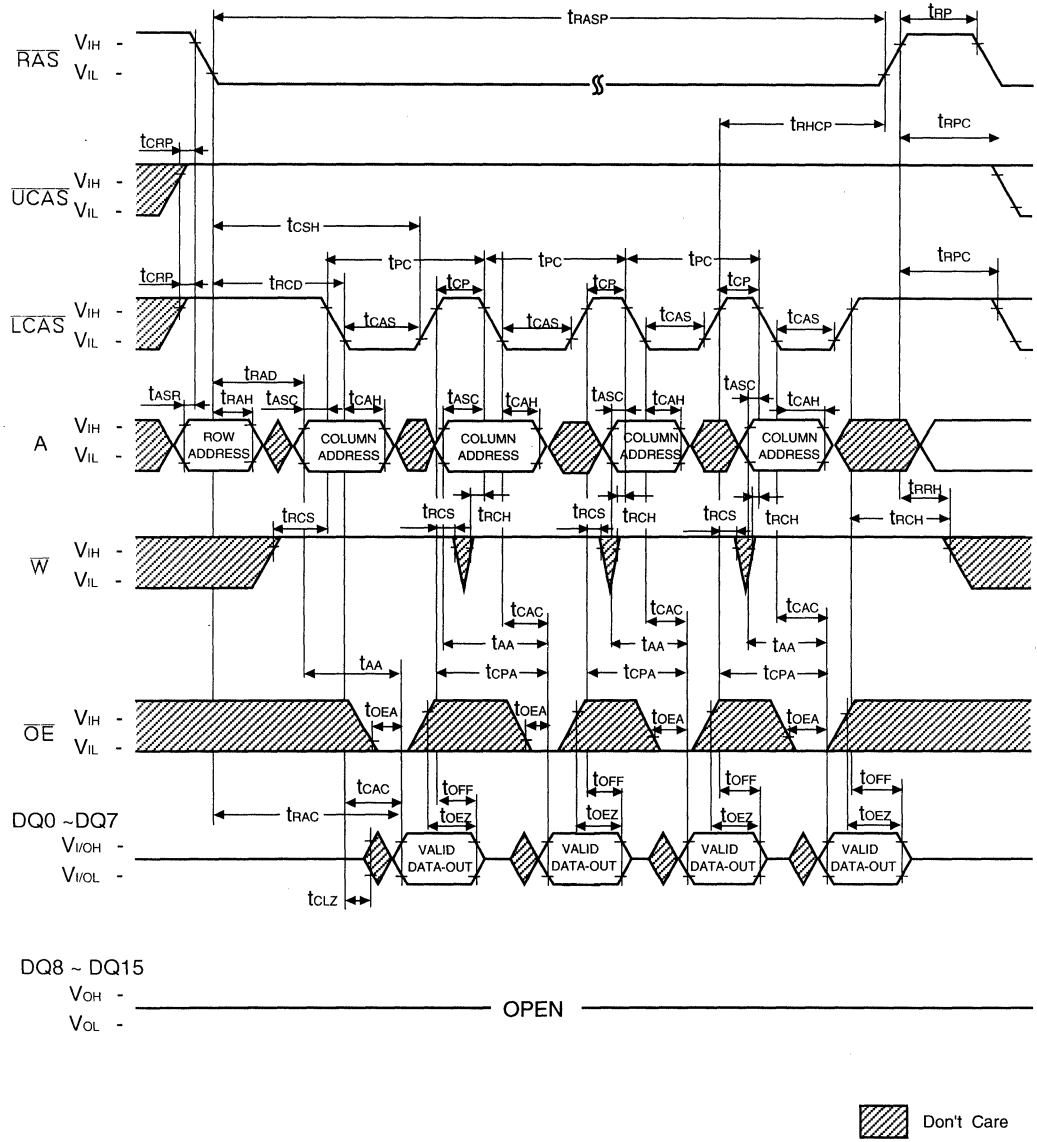


FAST PAGE MODE WORD READ CYCLE

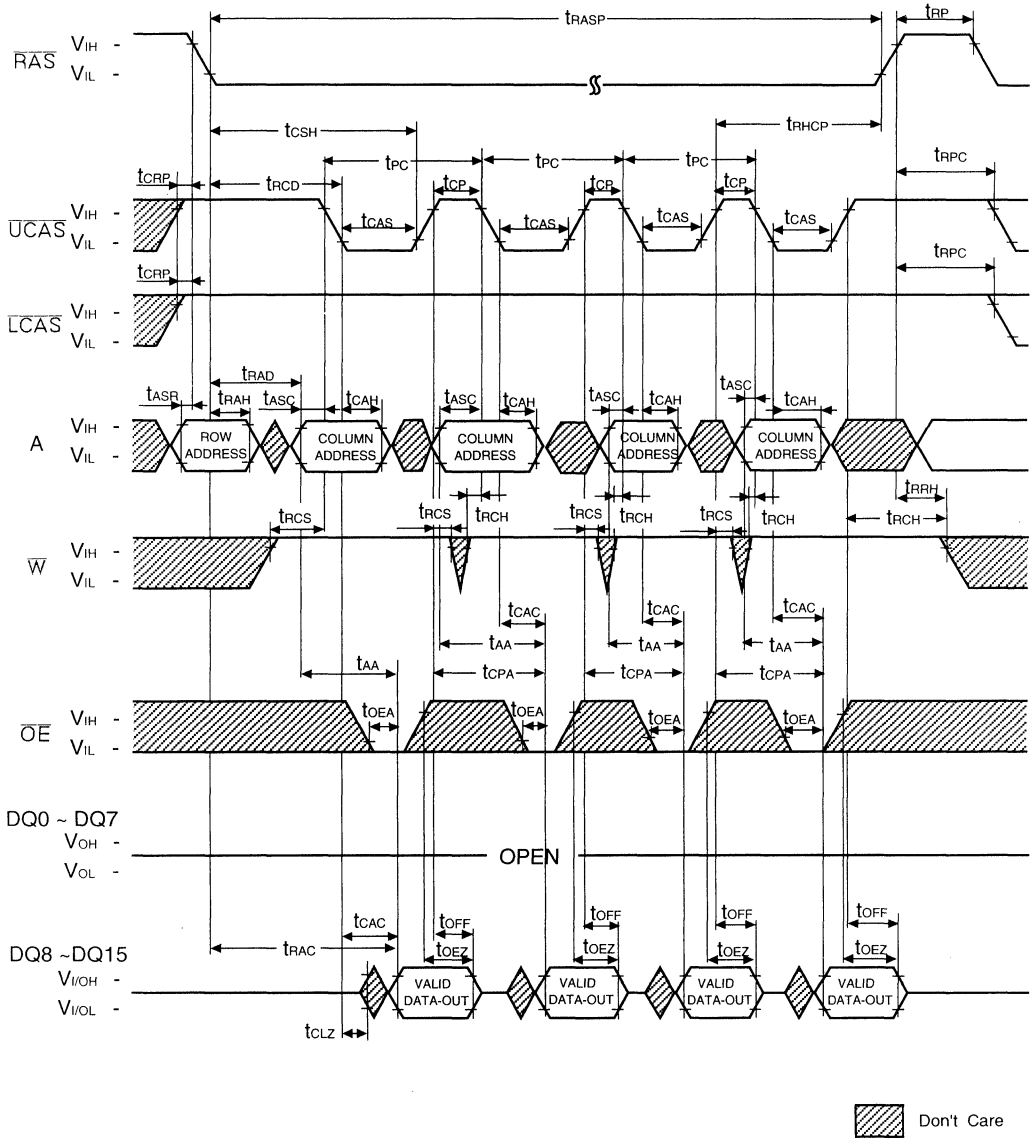


SAMSUNG ELECTRONICS

FAST PAGE MODE LOWER BYTE READ CYCLE

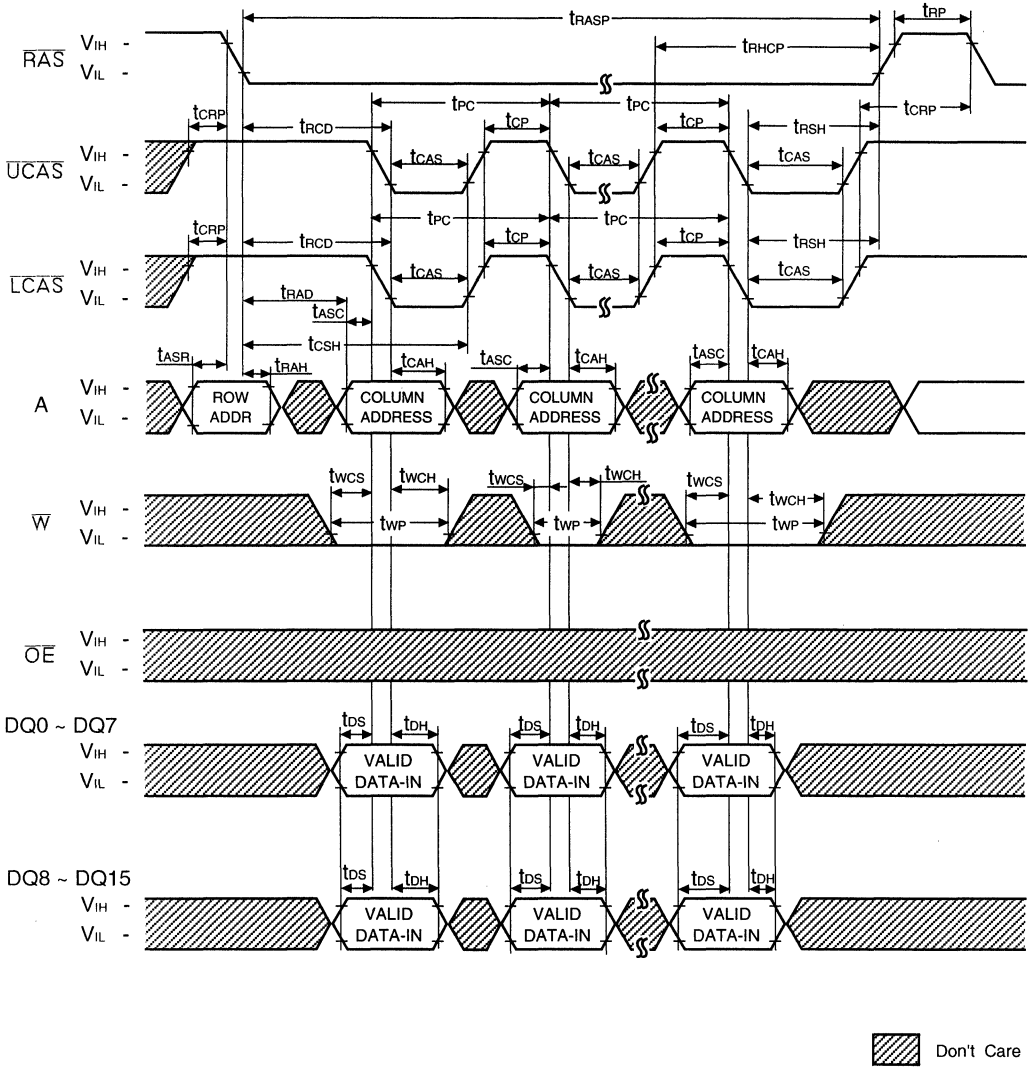


FAST PAGE MODE UPPER BYTE READ CYCLE



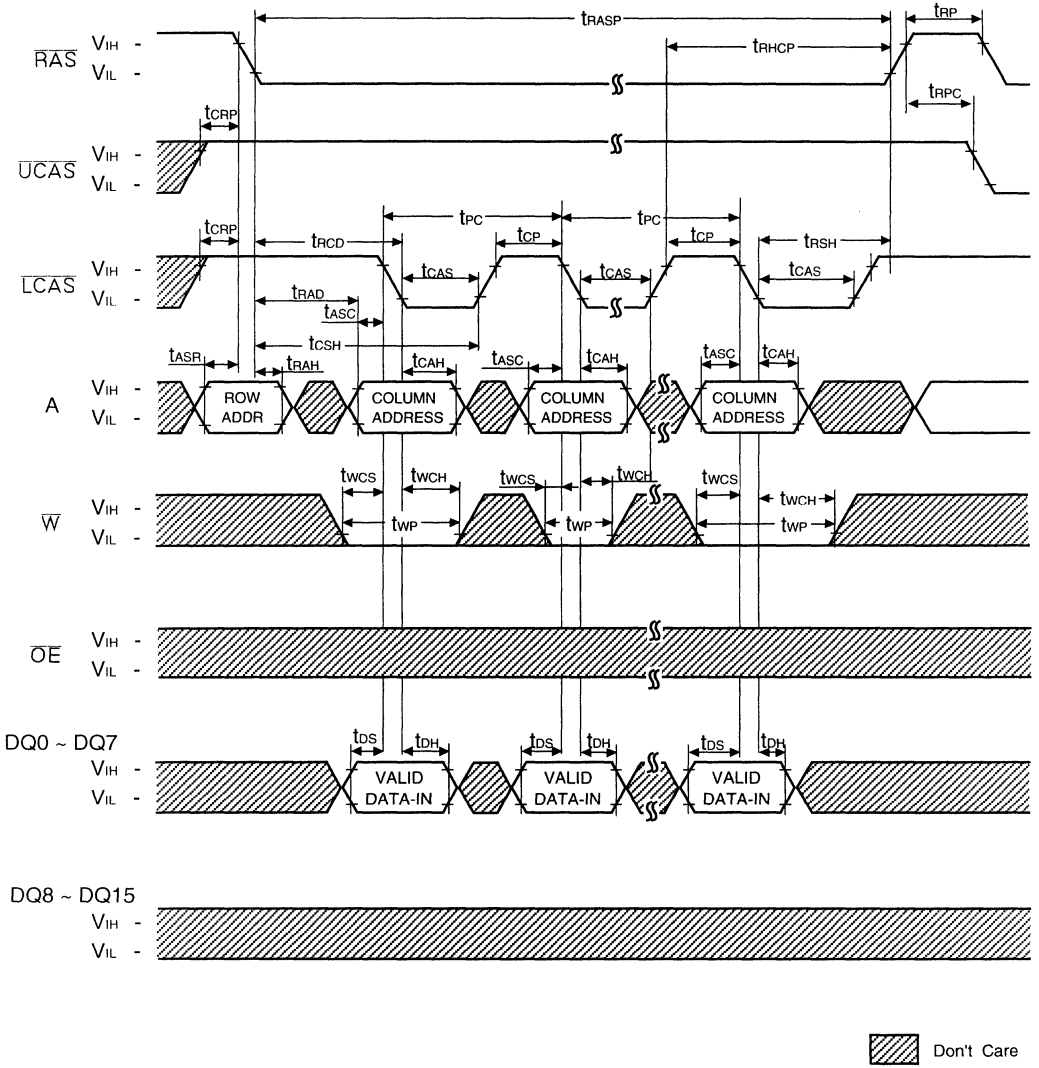
FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

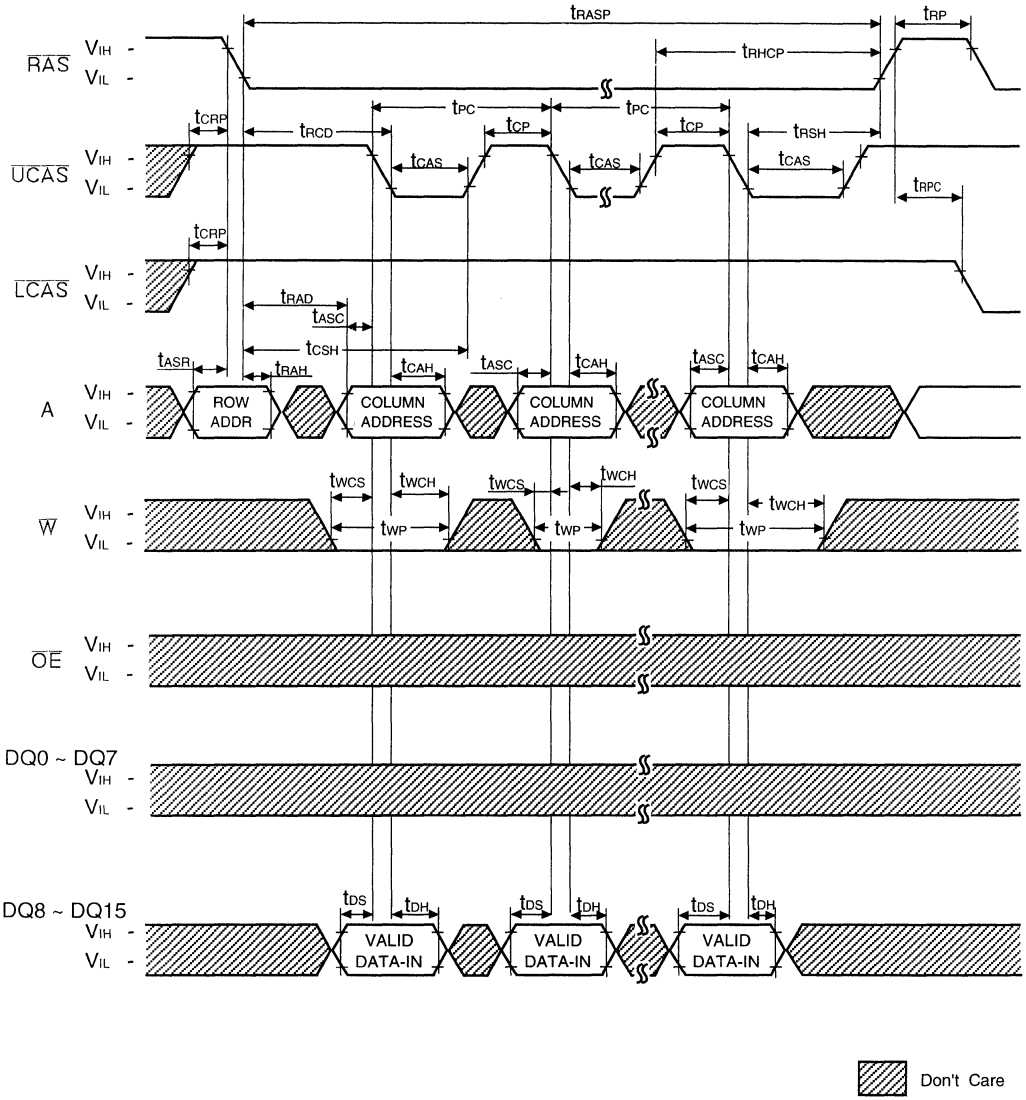
NOTE : D_{OUT} = Open



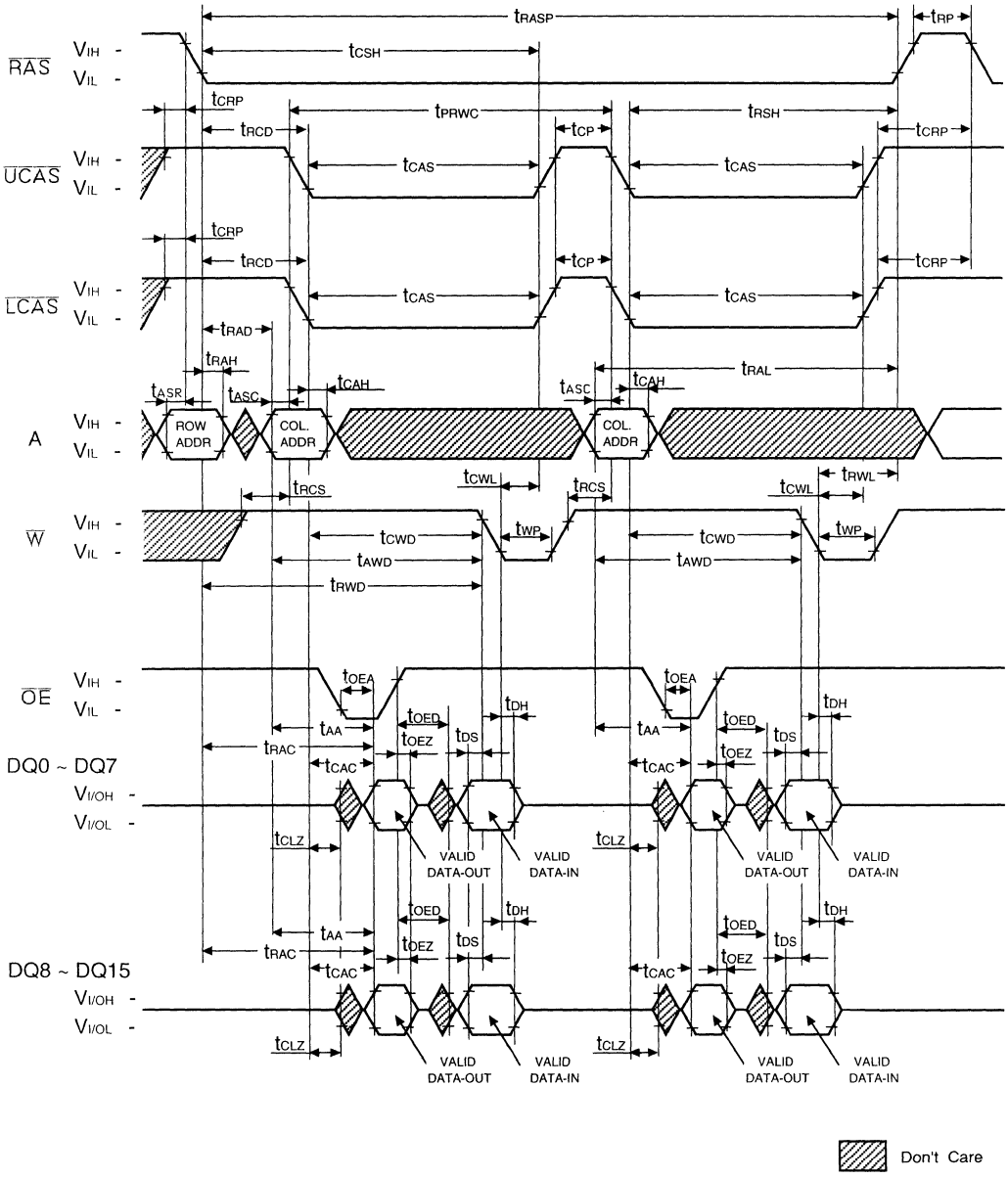
SAMSUNG ELECTRONICS

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open

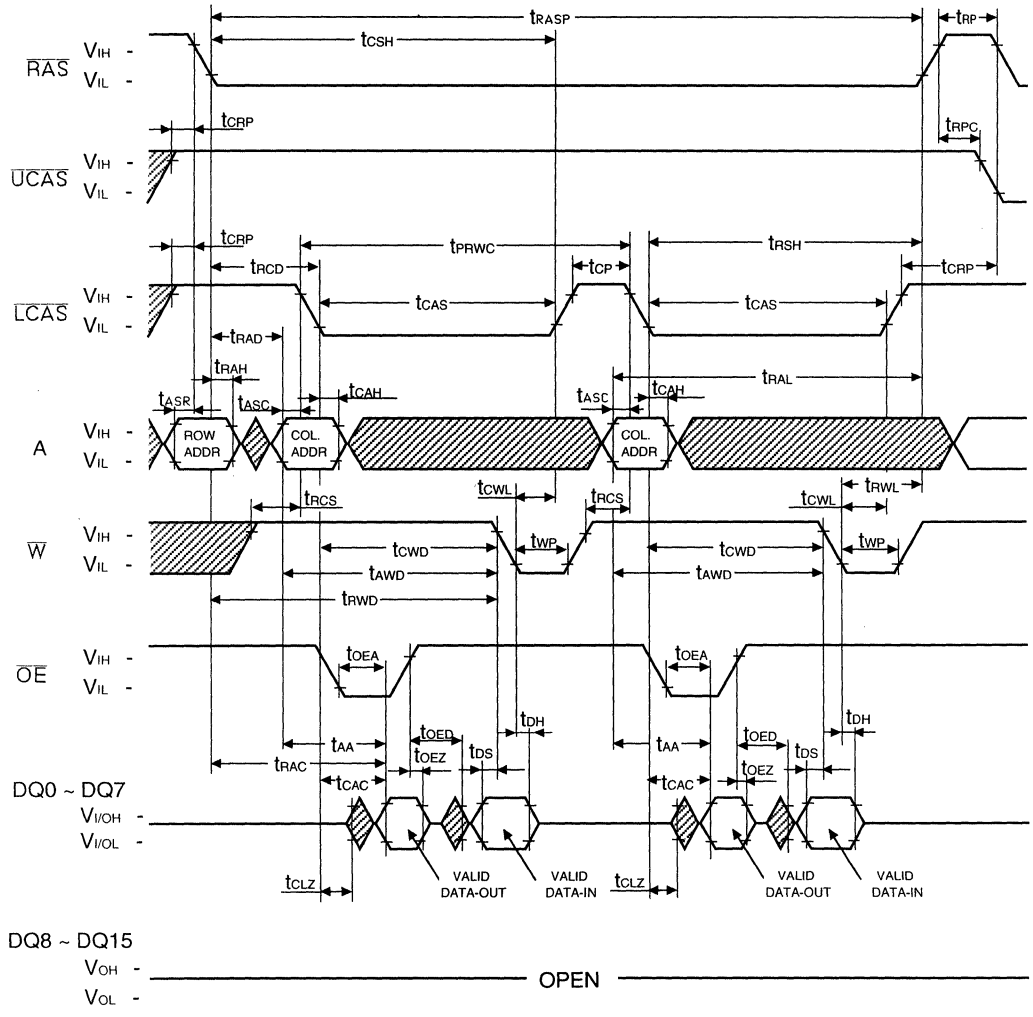


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

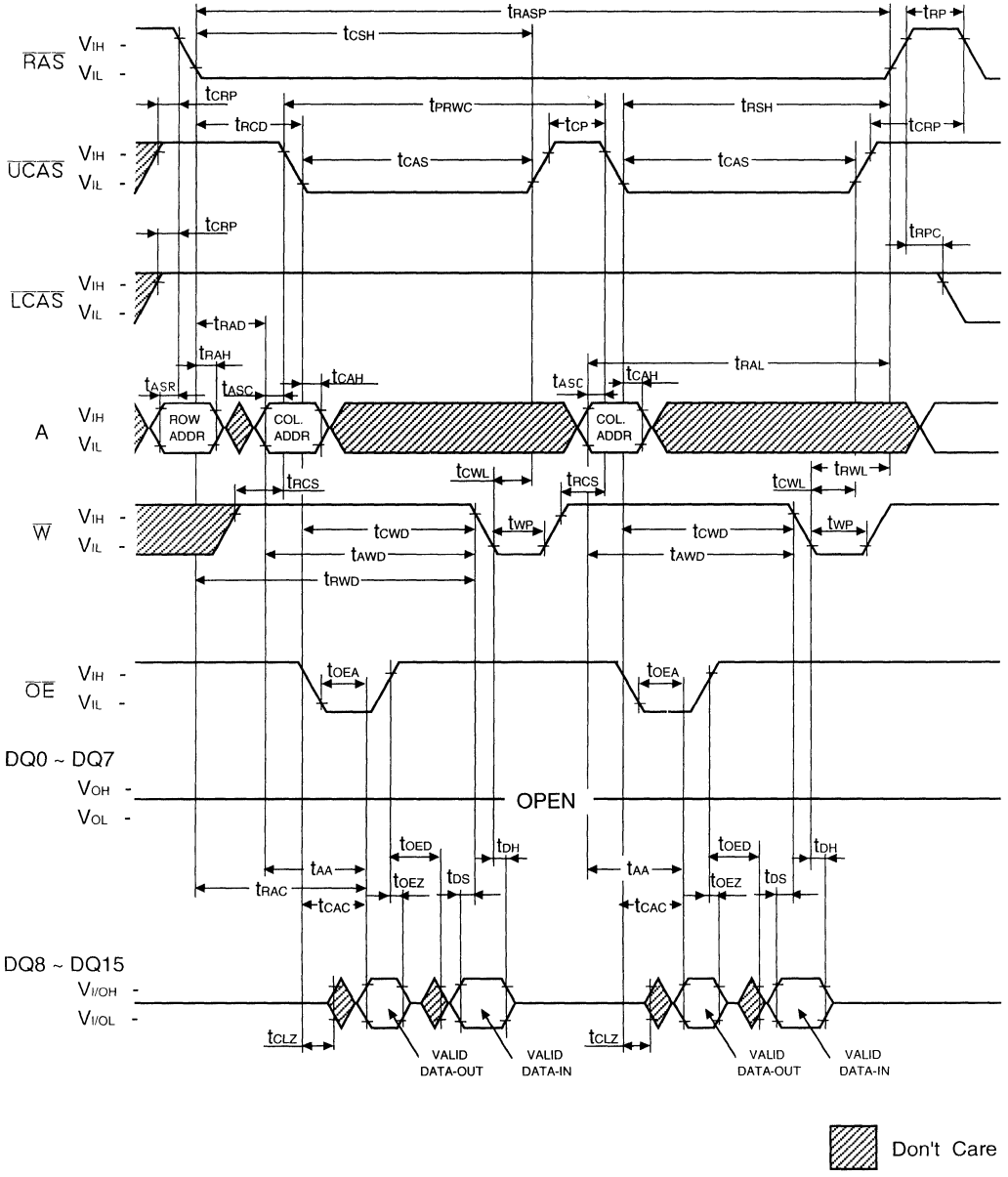


SAMSUNG ELECTRONICS

FAST PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE

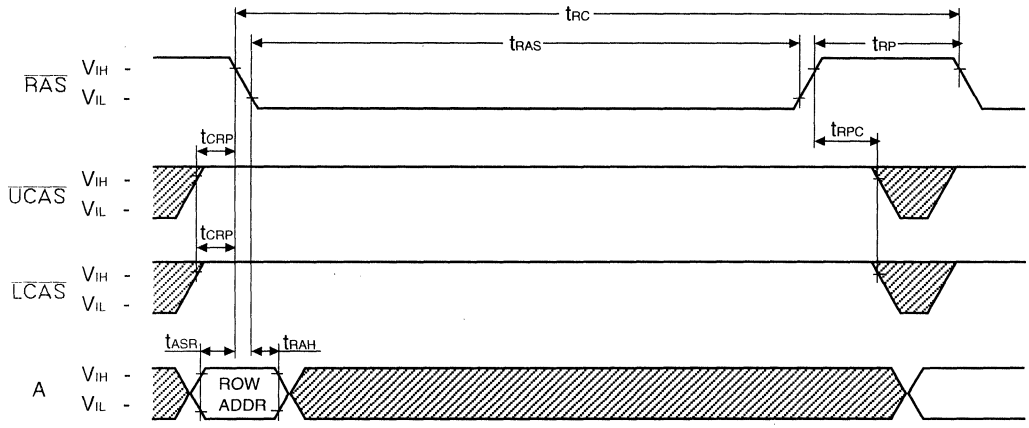


FAST PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



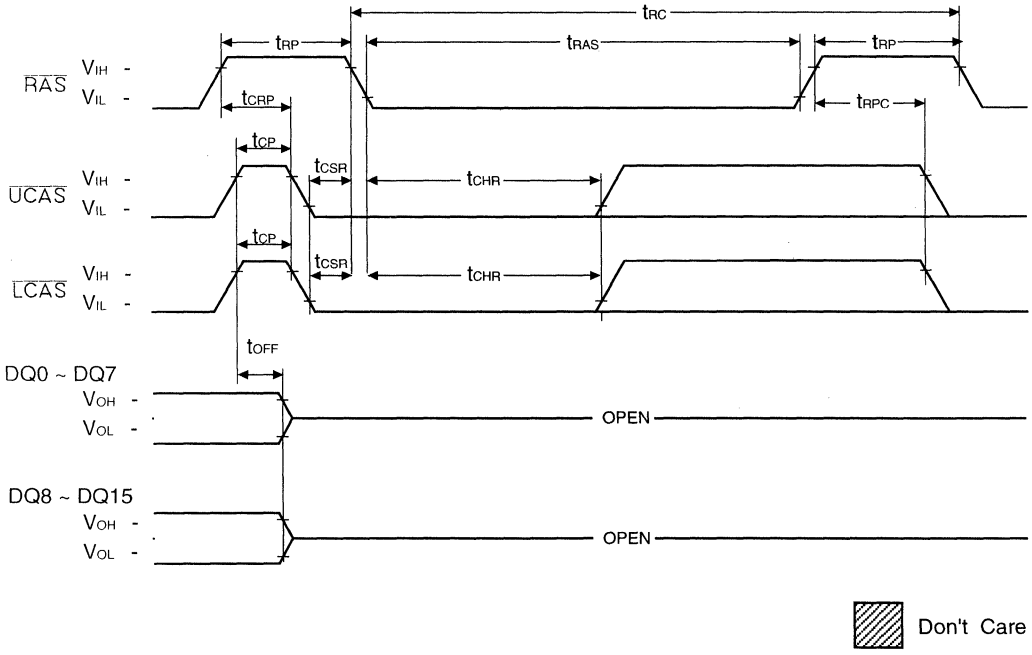
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



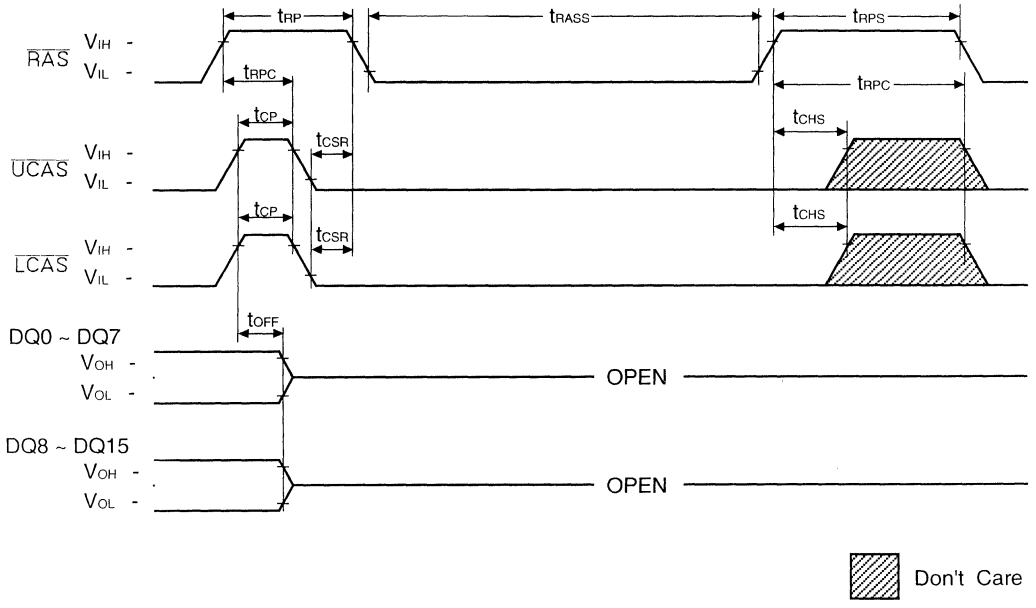
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

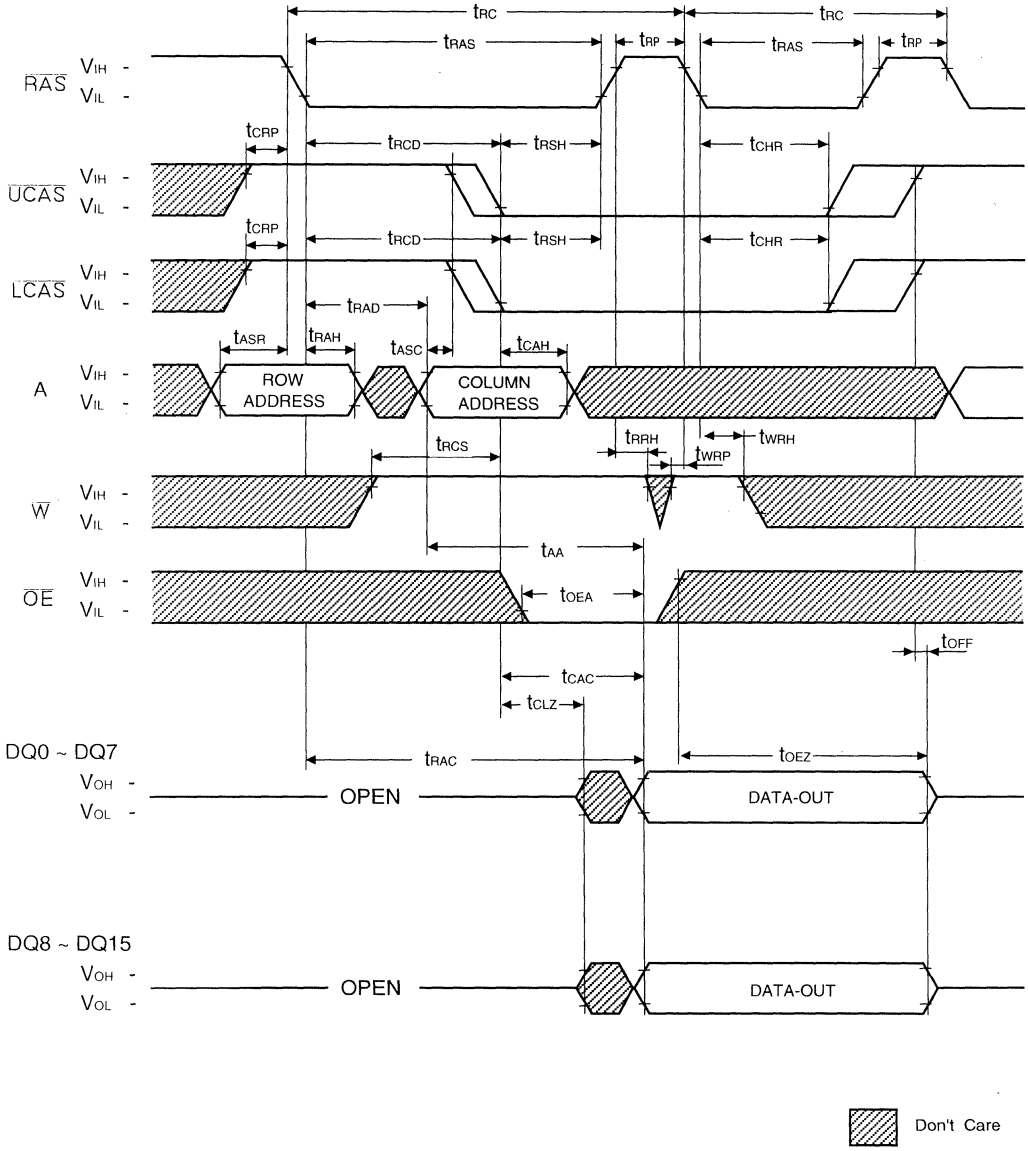


$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

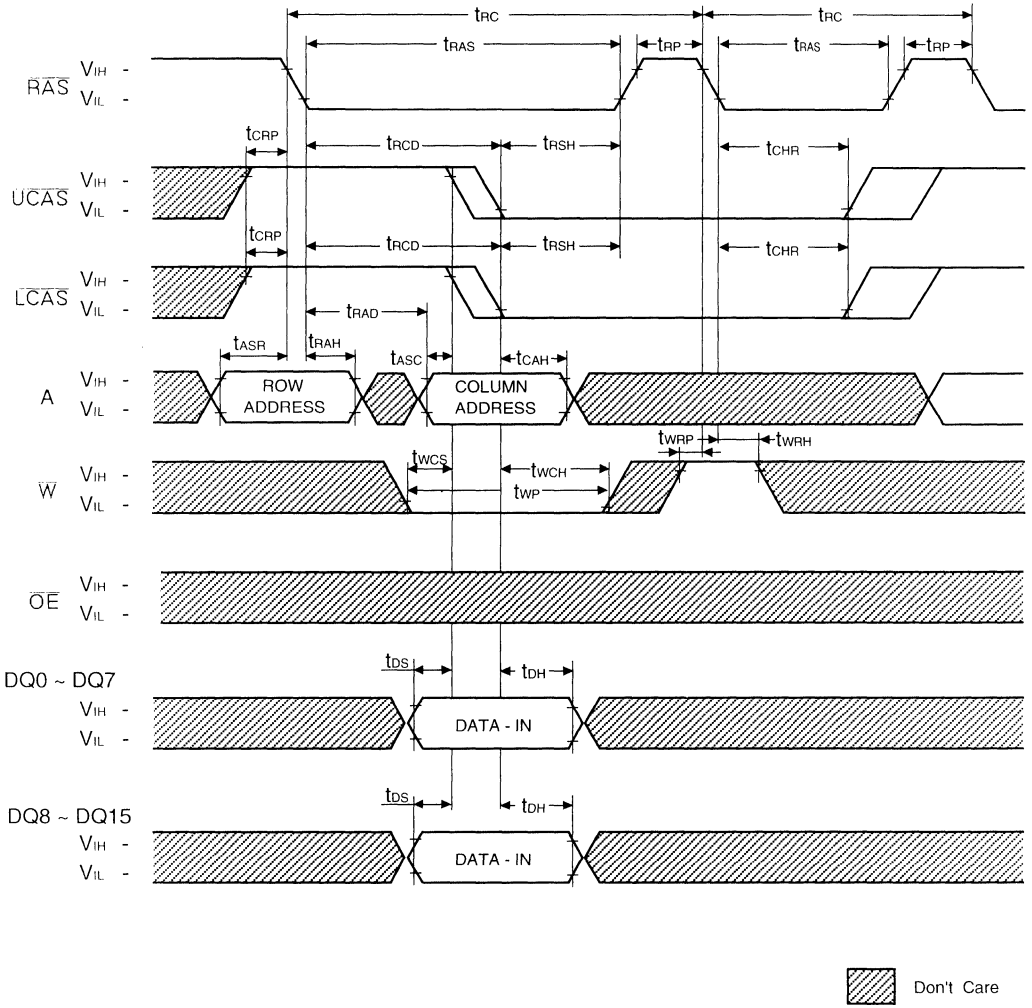


HIDDEN REFRESH CYCLE (READ)



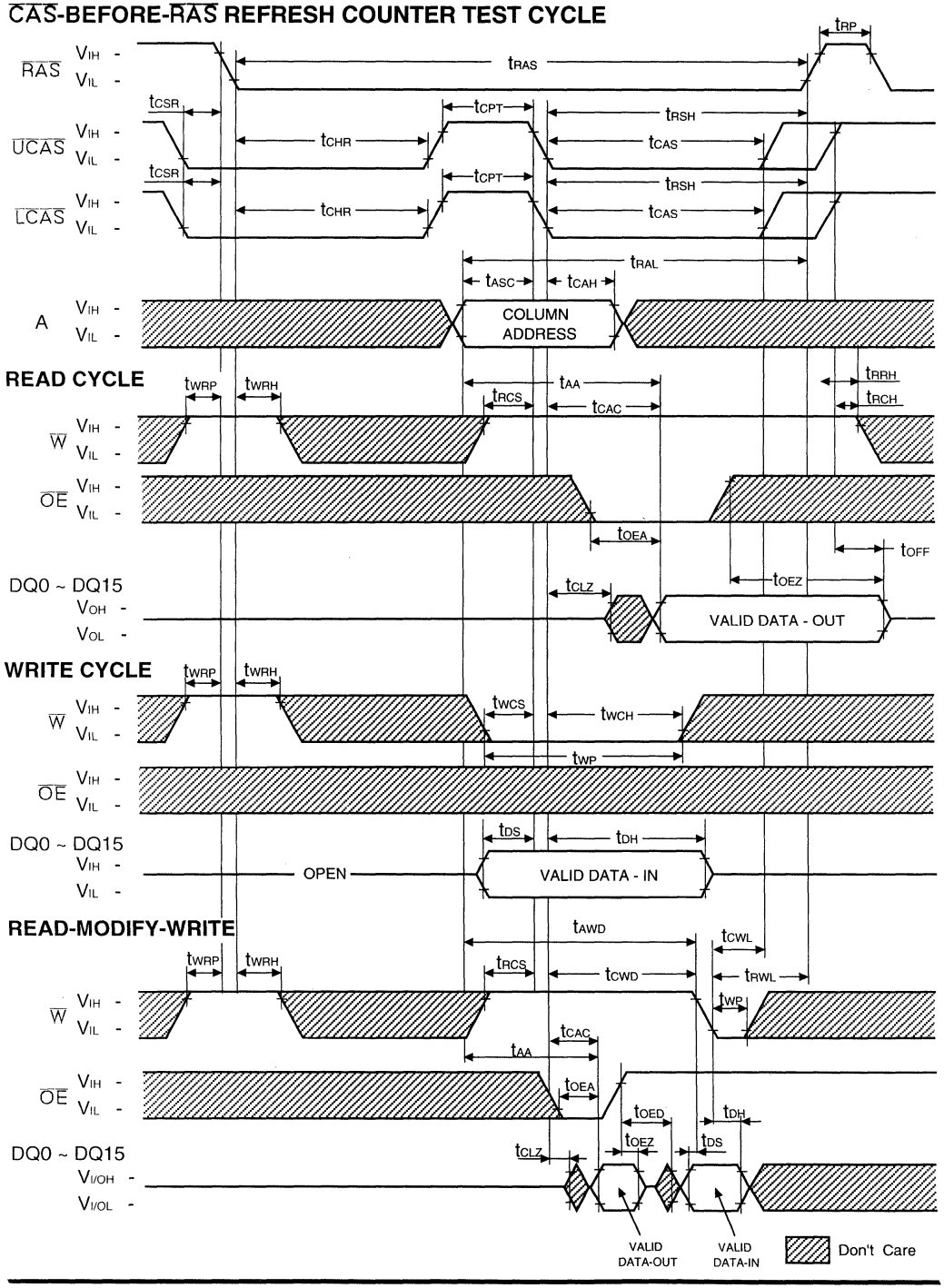
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



SAMSUNG ELECTRONICS

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

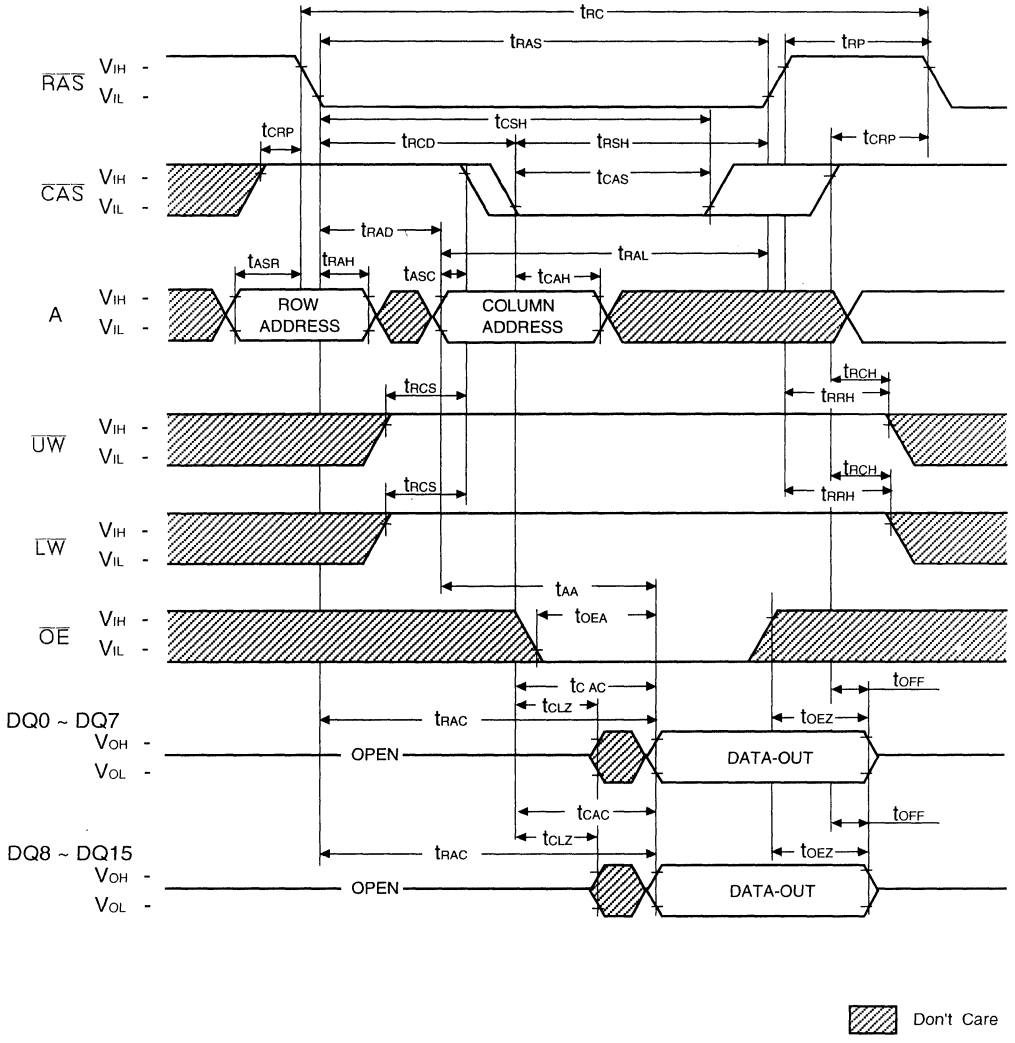


Fast page Mode, x16(2$\overline{WE}$) Device

TIMING DIAGRAM

READ CYCLE

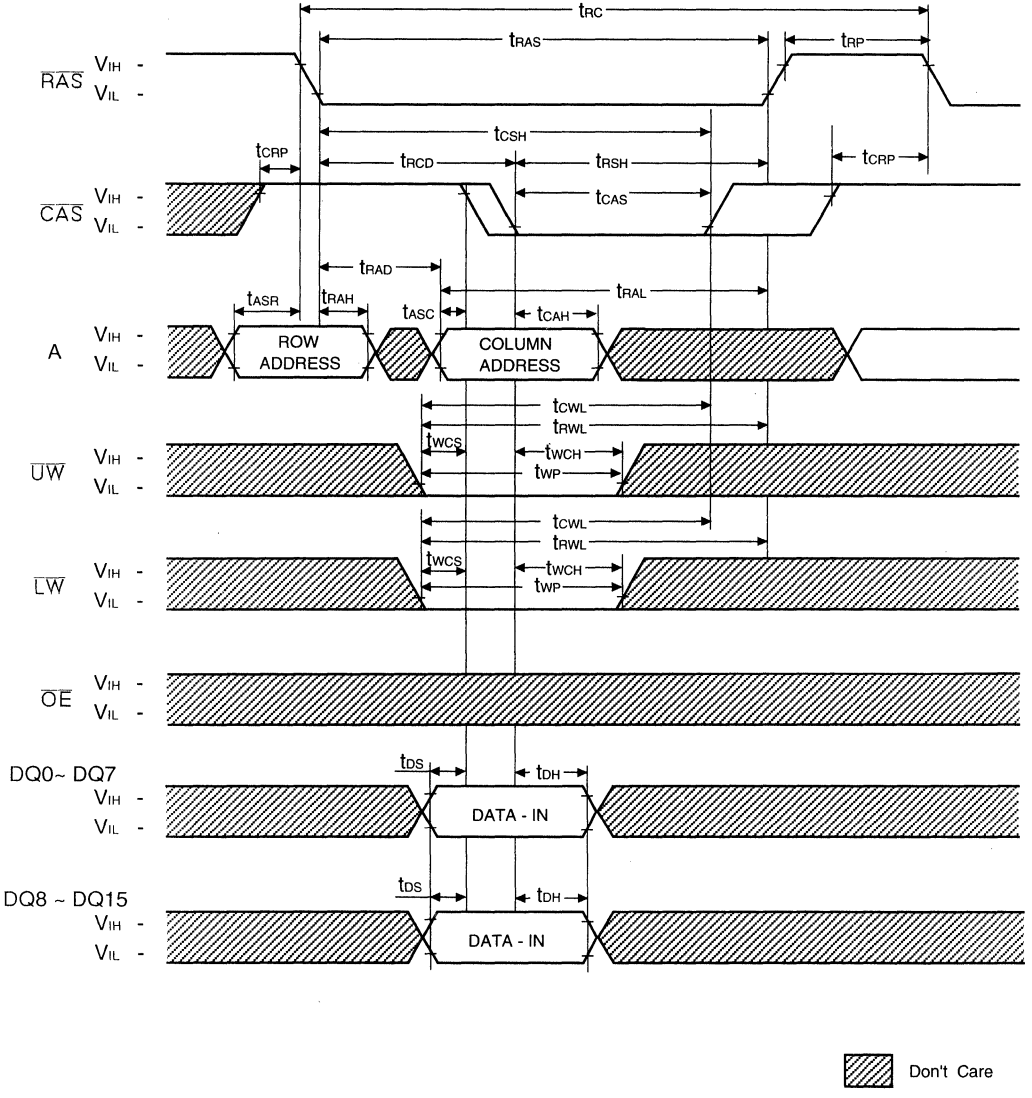
NOTE : D_{IN} = OPEN



SAMSUNG ELECTRONICS

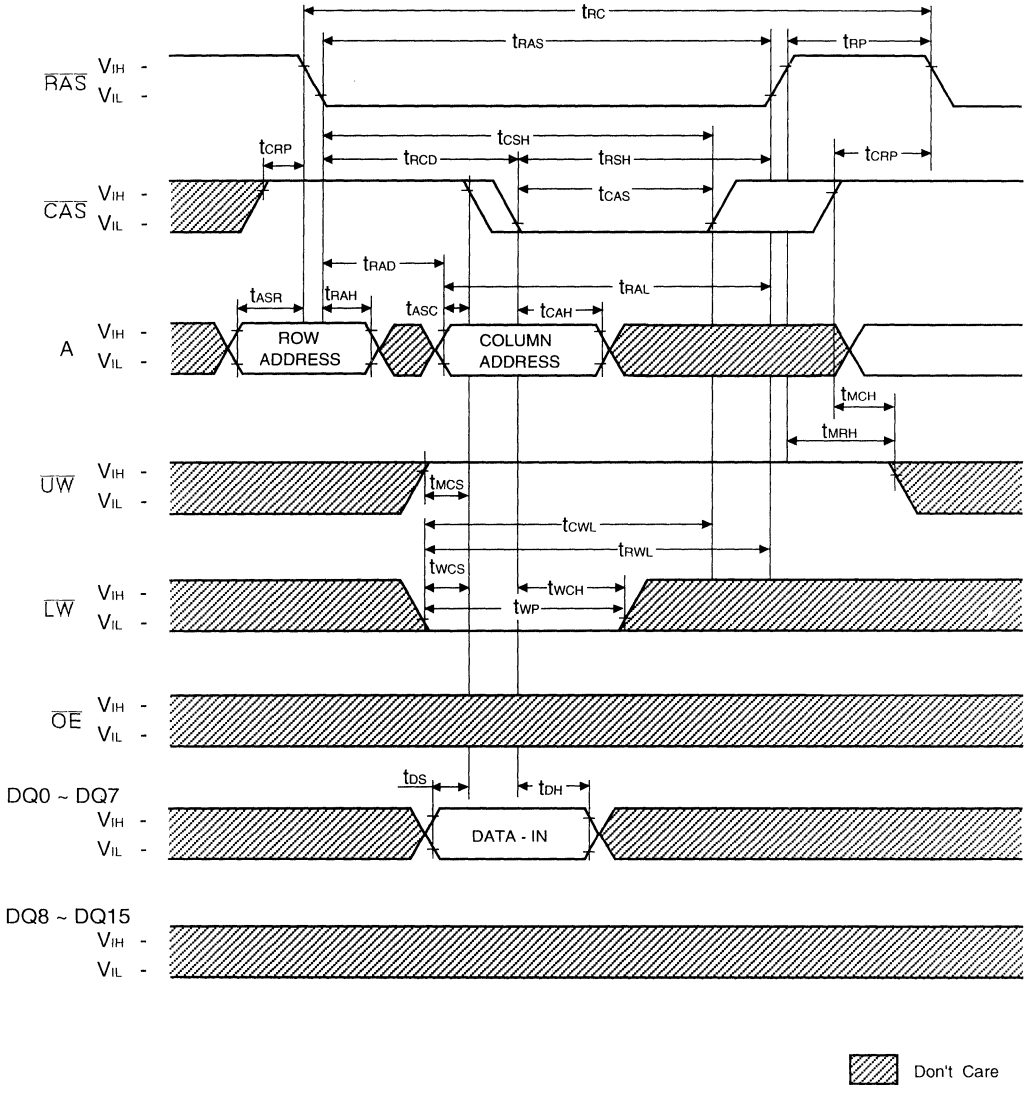
WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



LOWER BYTE WRITE CYCLE (EARLY WRITE)

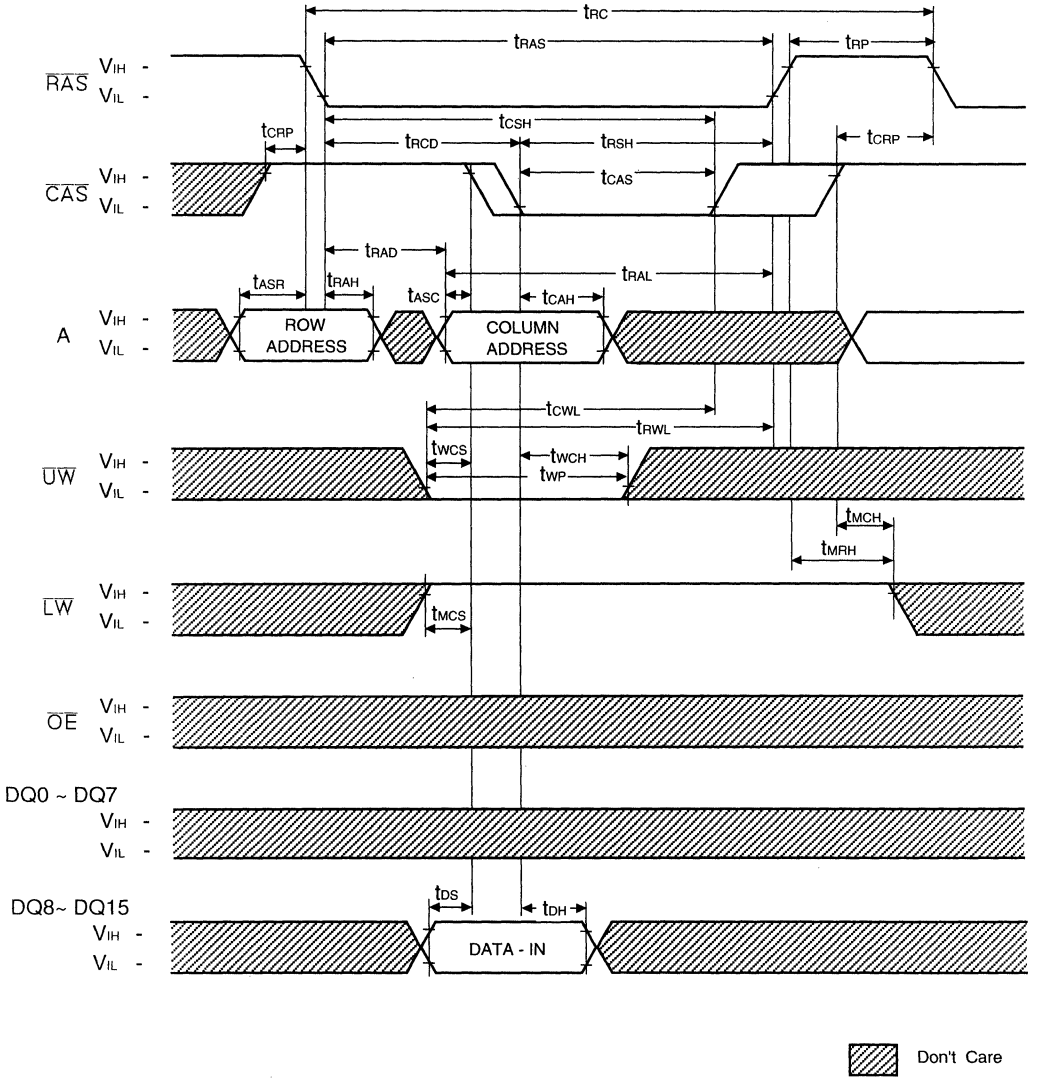
NOTE : D_{OUT} = OPEN



SAMSUNG ELECTRONICS

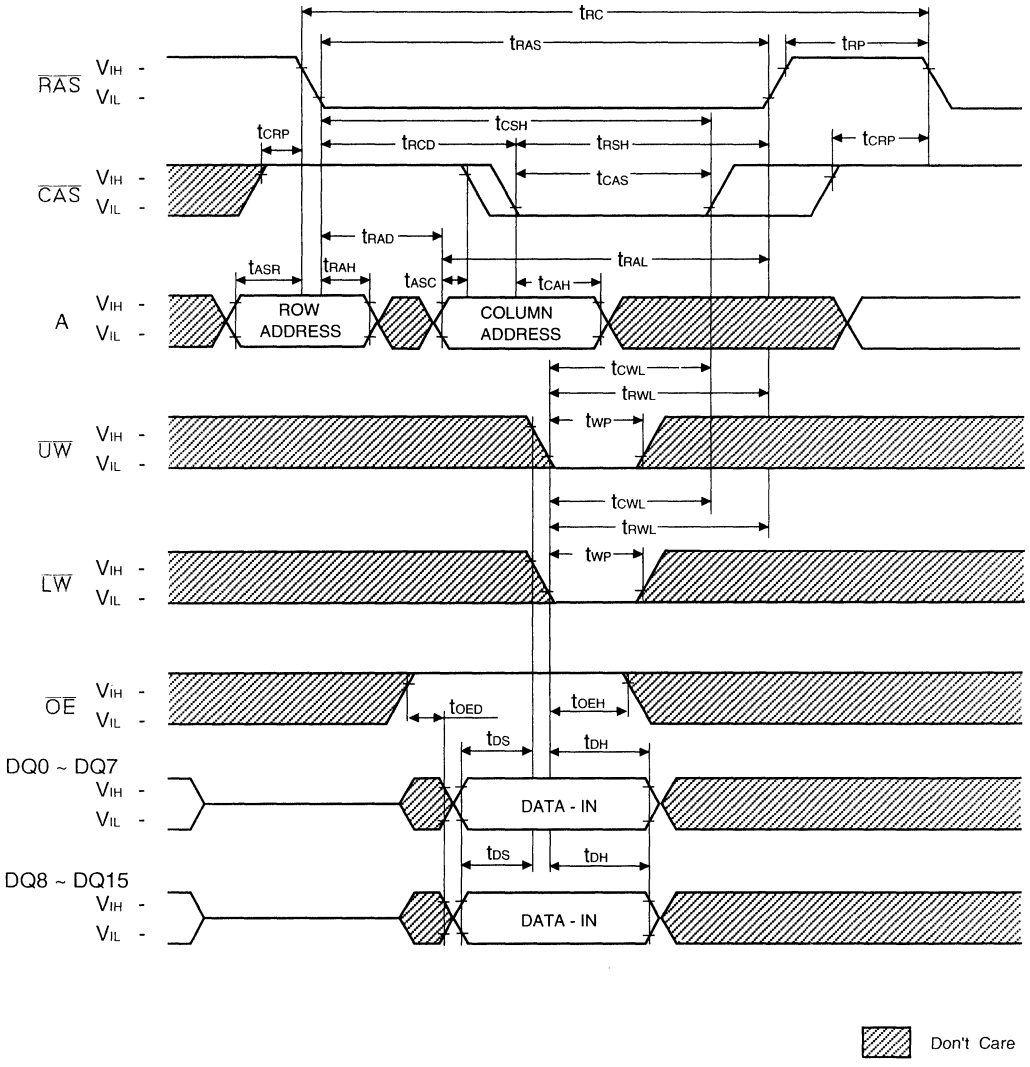
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



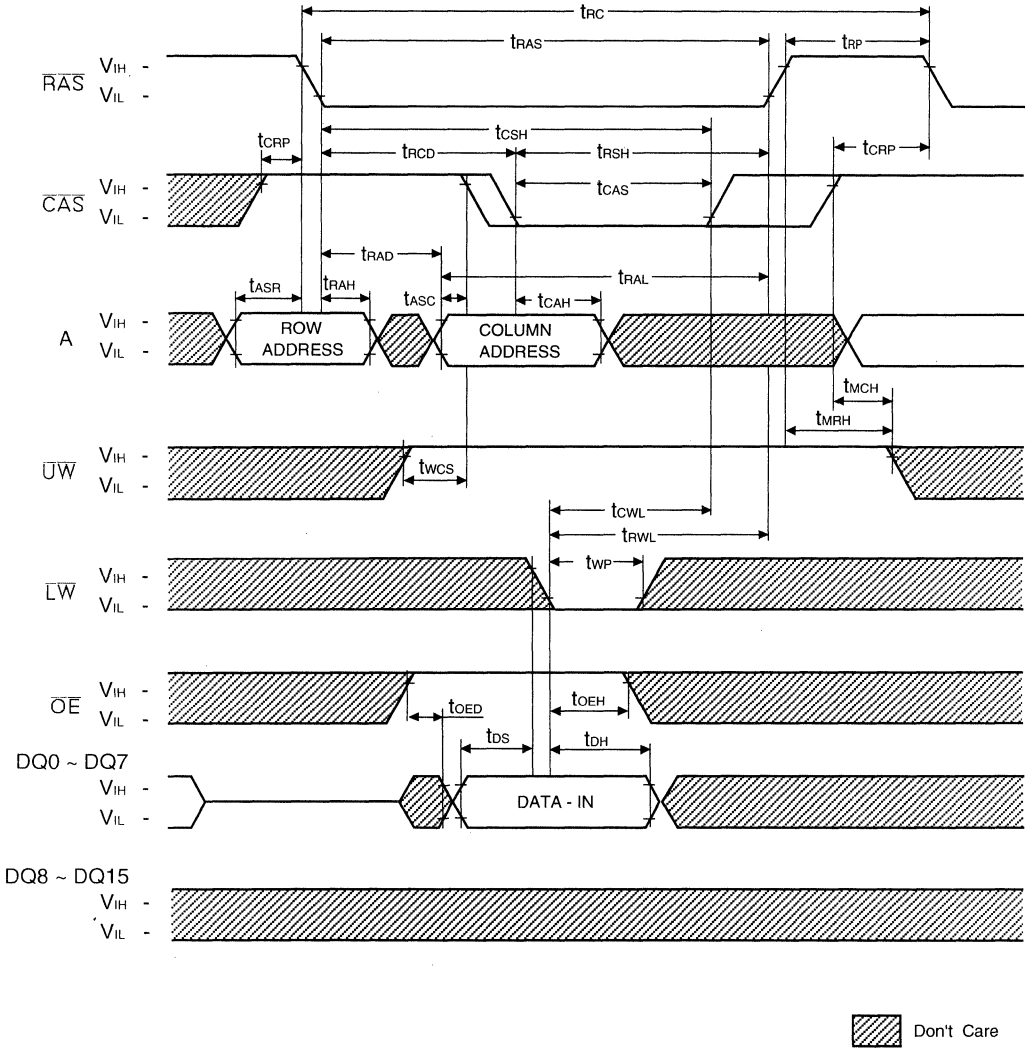
WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

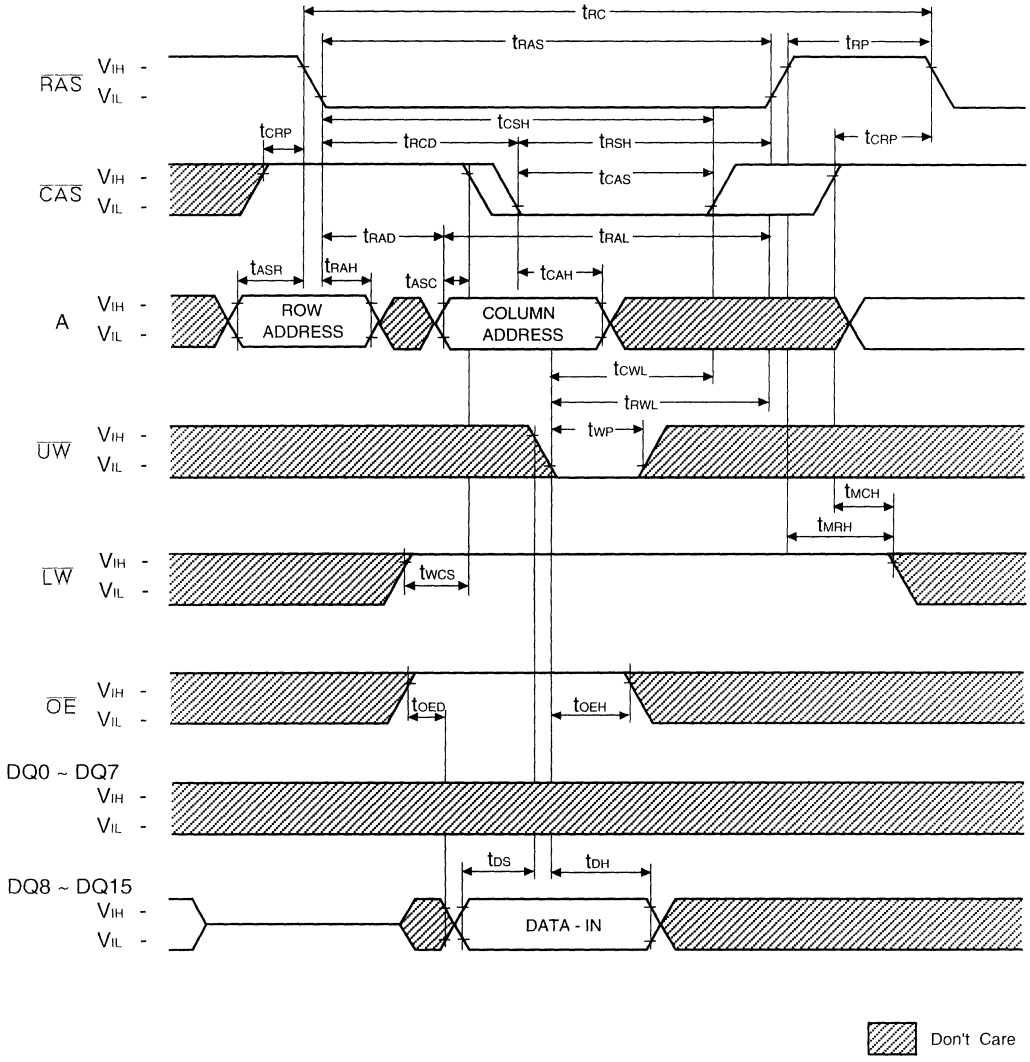
NOTE : D_{OUT} = OPEN



SAMSUNG ELECTRONICS

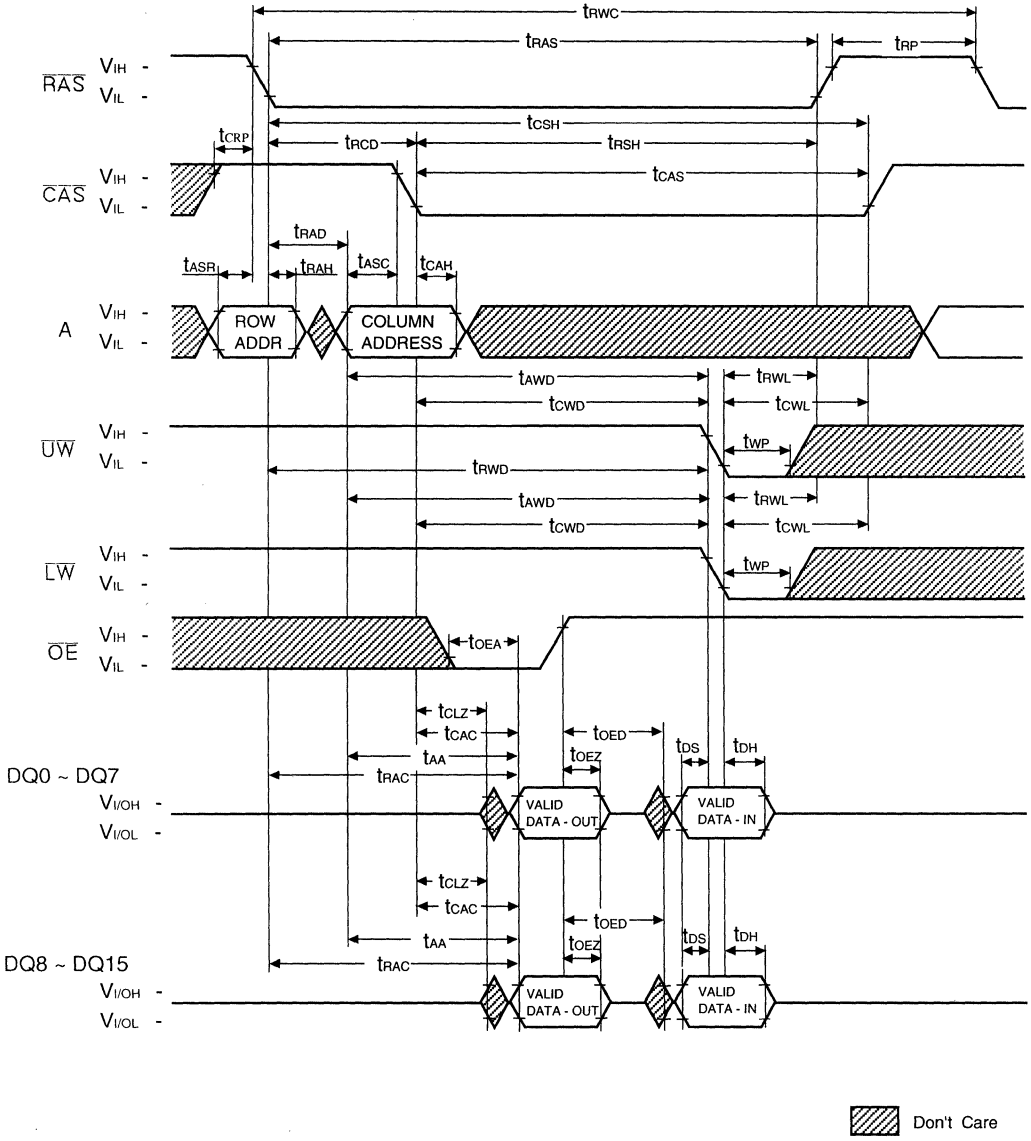
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

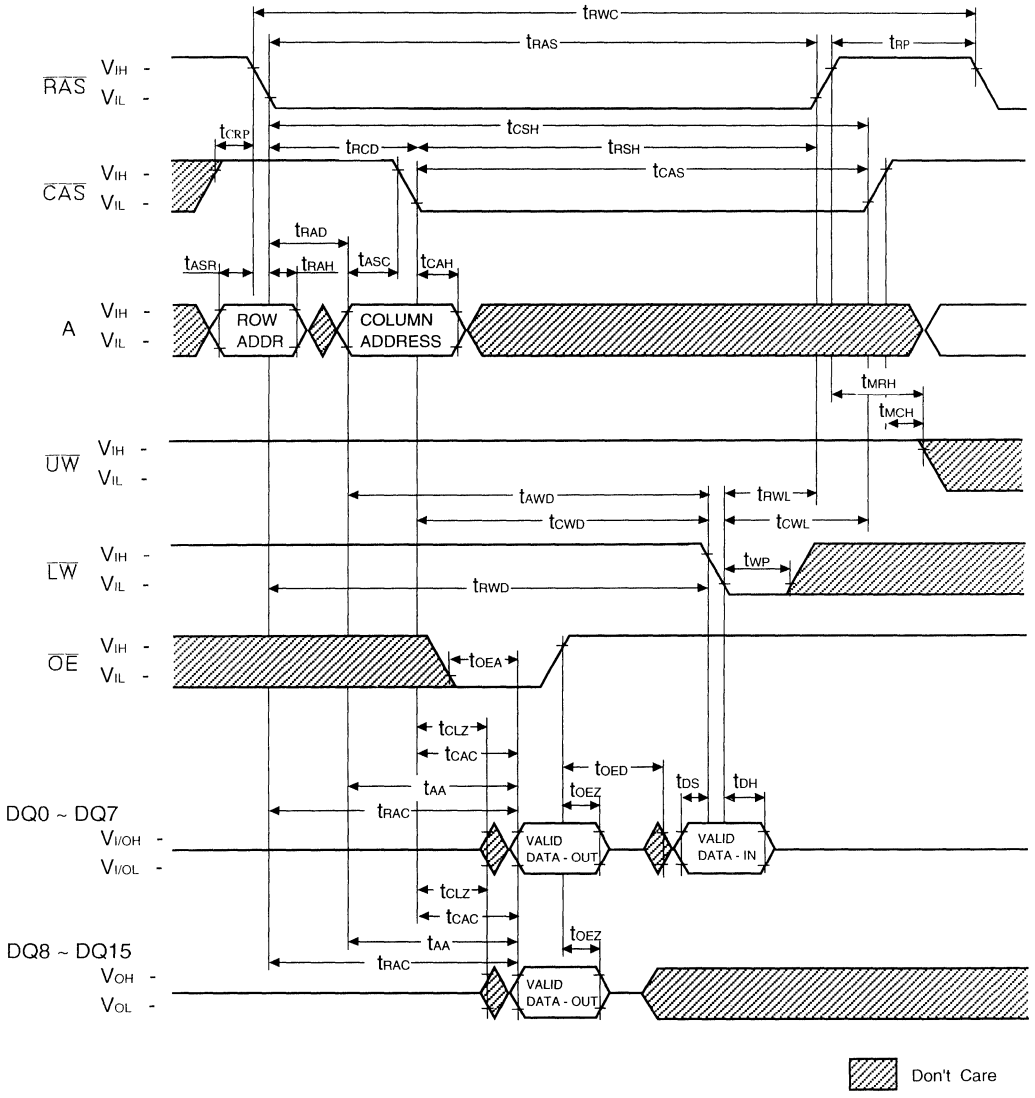


SAMSUNG ELECTRONICS

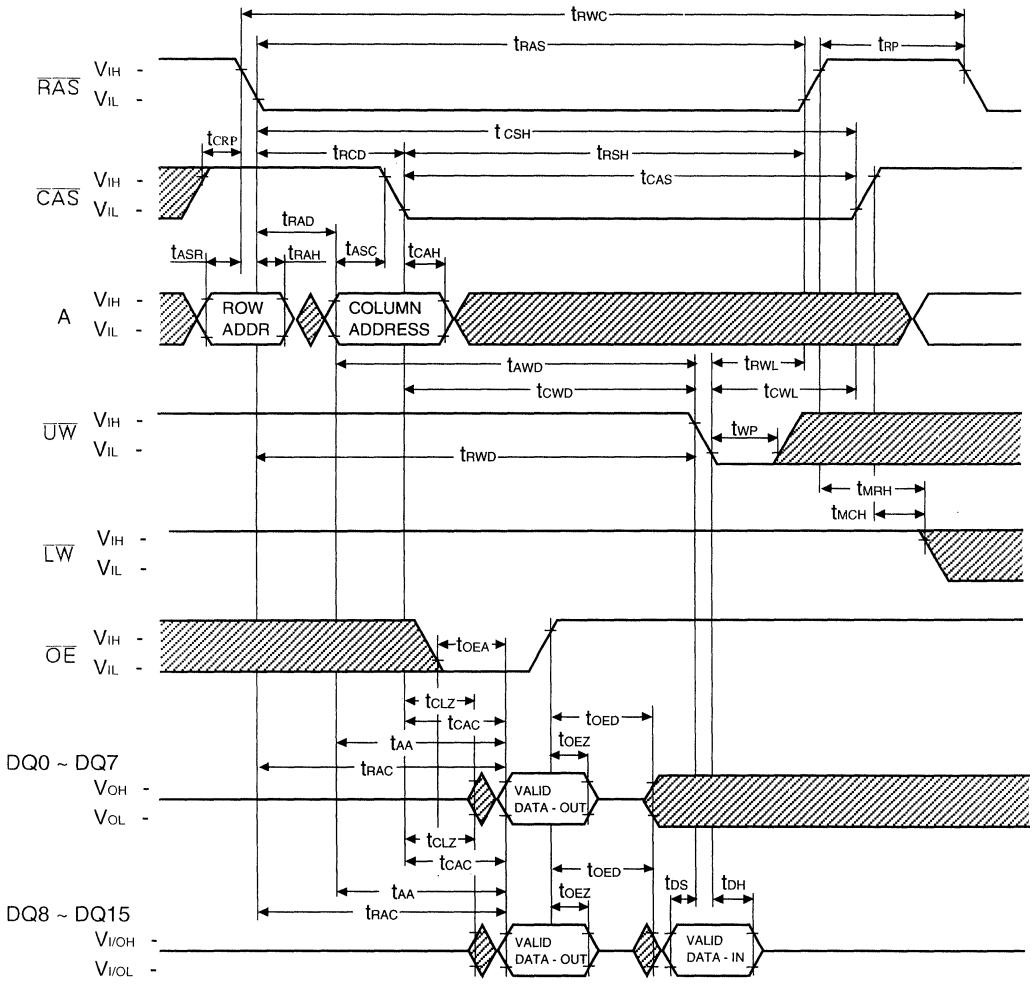
WORD READ - MODIFY - WRITE CYCLE



LOWER-BYTE READ - MODIFY - WRITE CYCLE

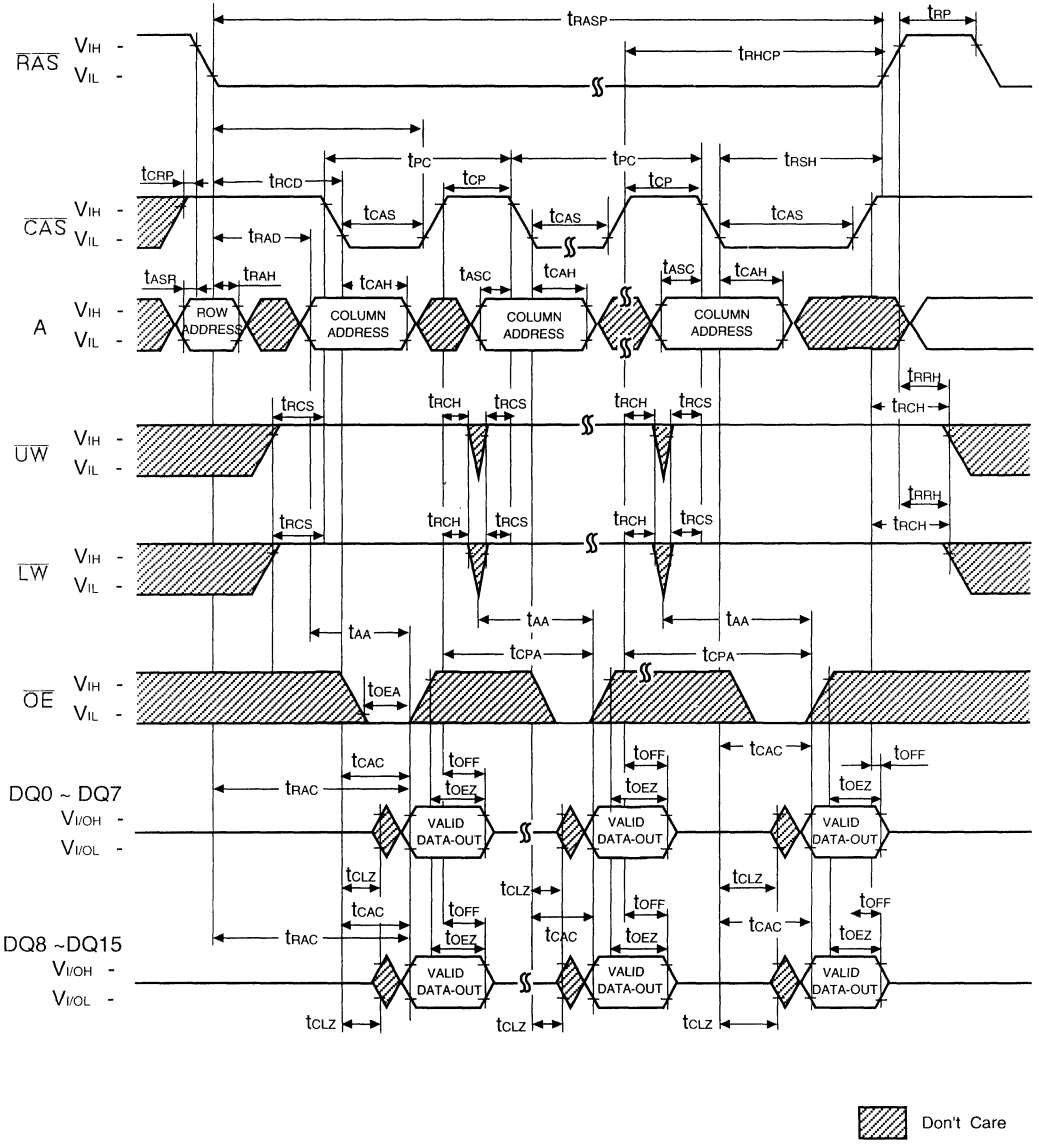


UPPER-BYTE READ - MODIFY - WRITE CYCLE



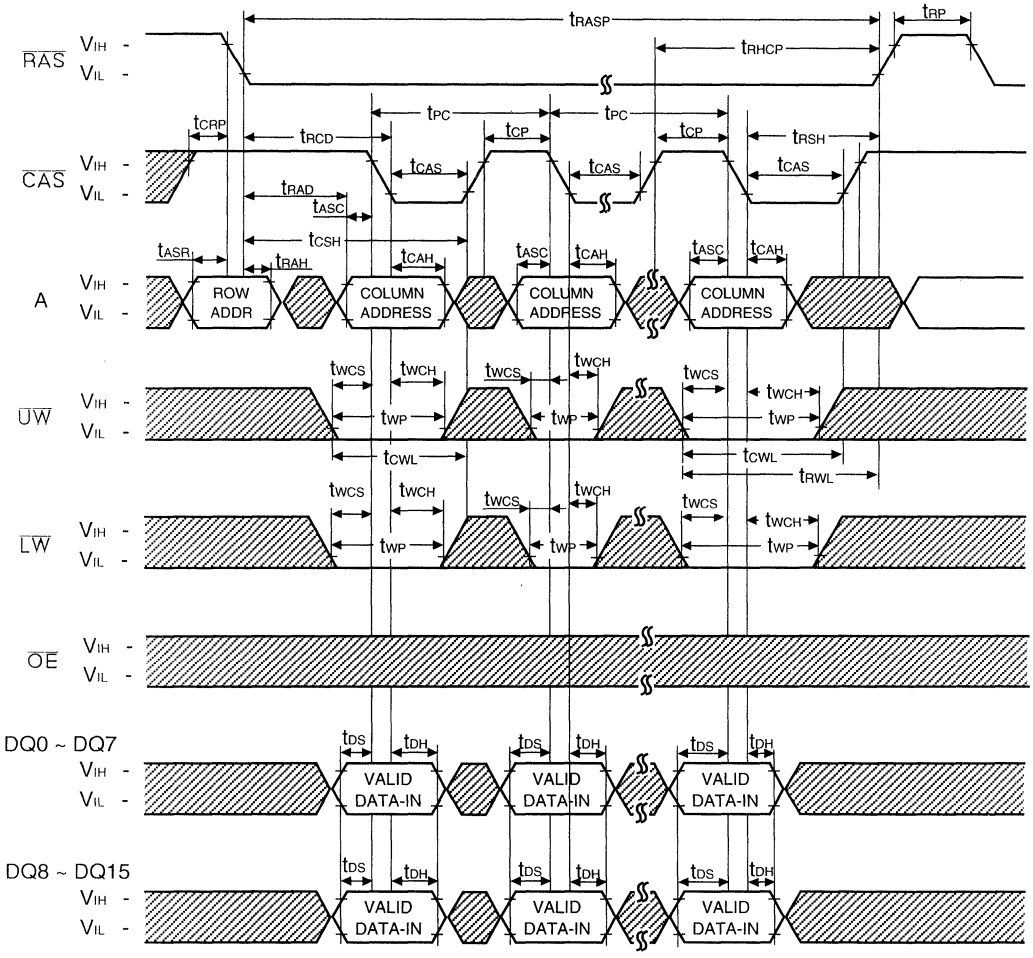
Don't Care

FAST PAGE MODE READ CYCLE



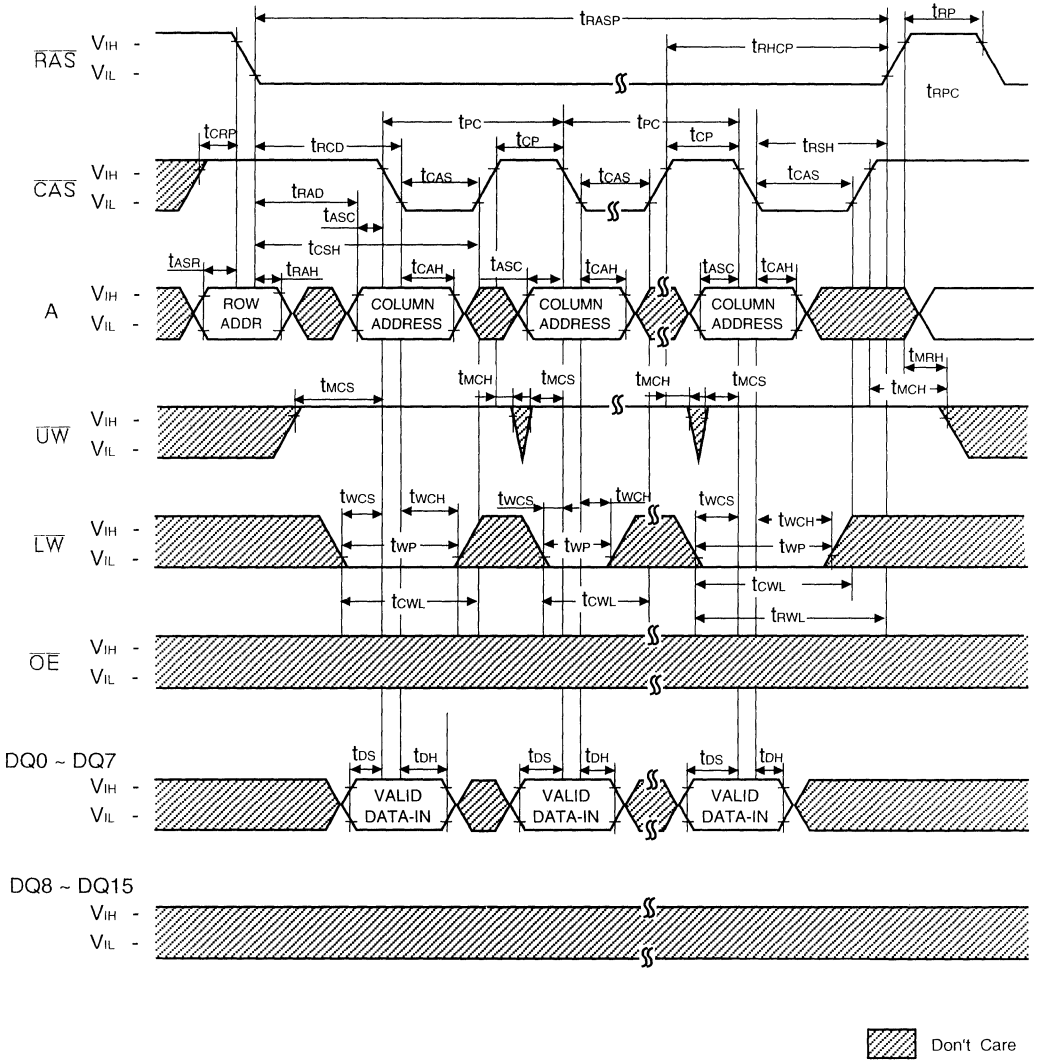
FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



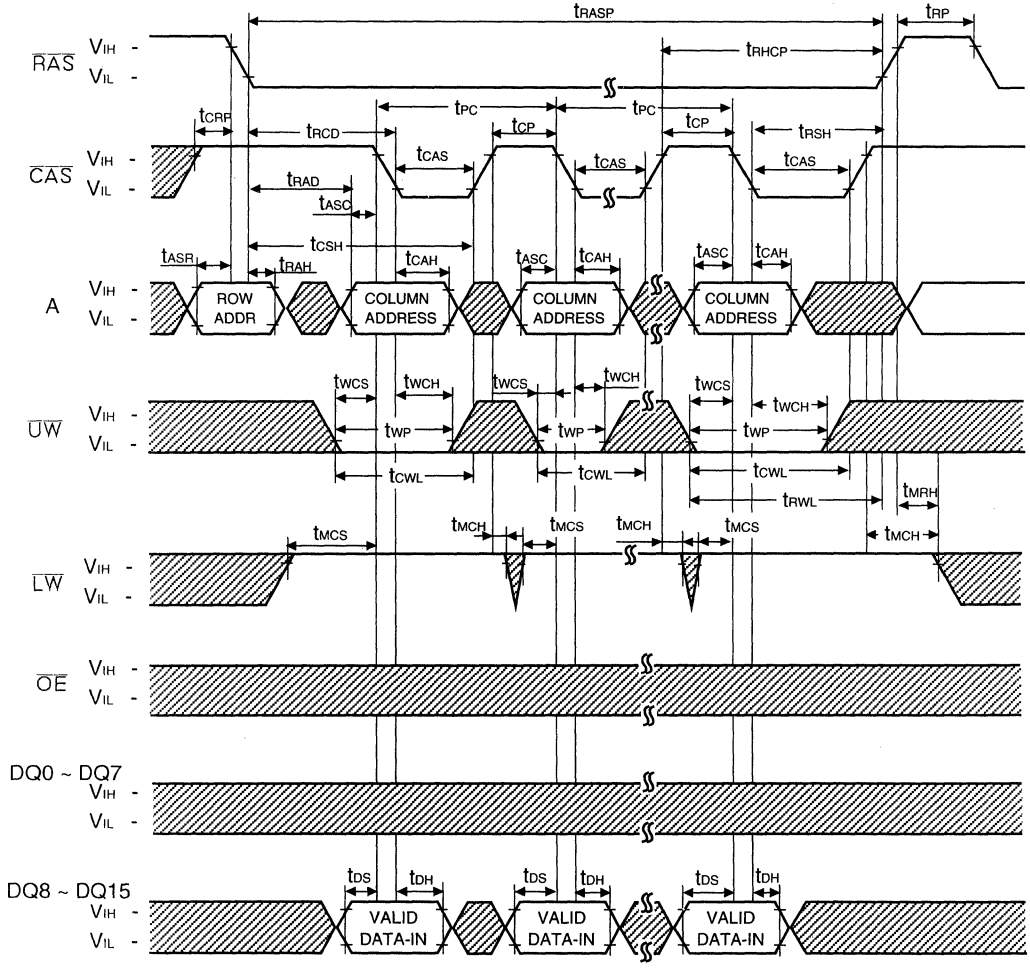
FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



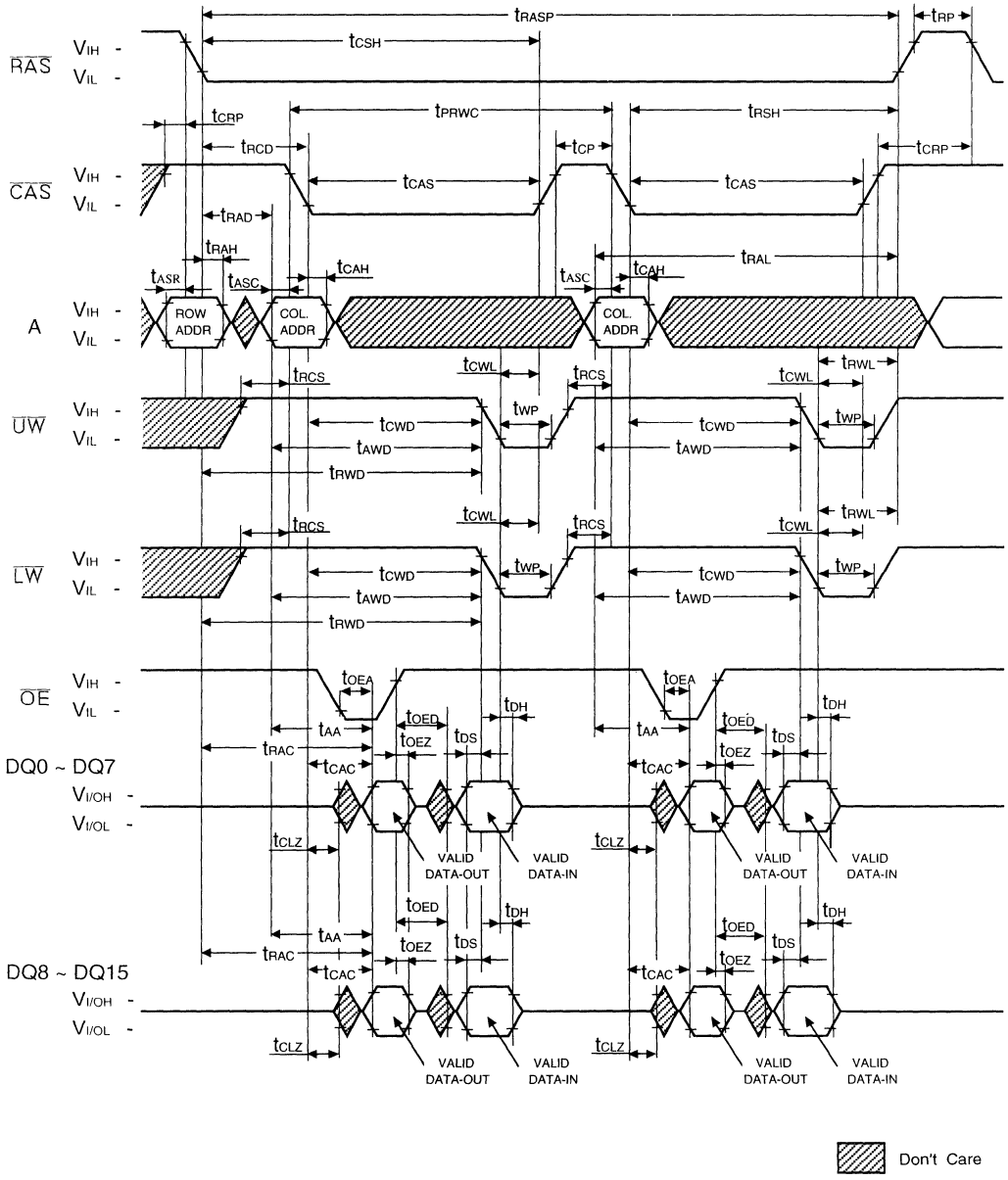
FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



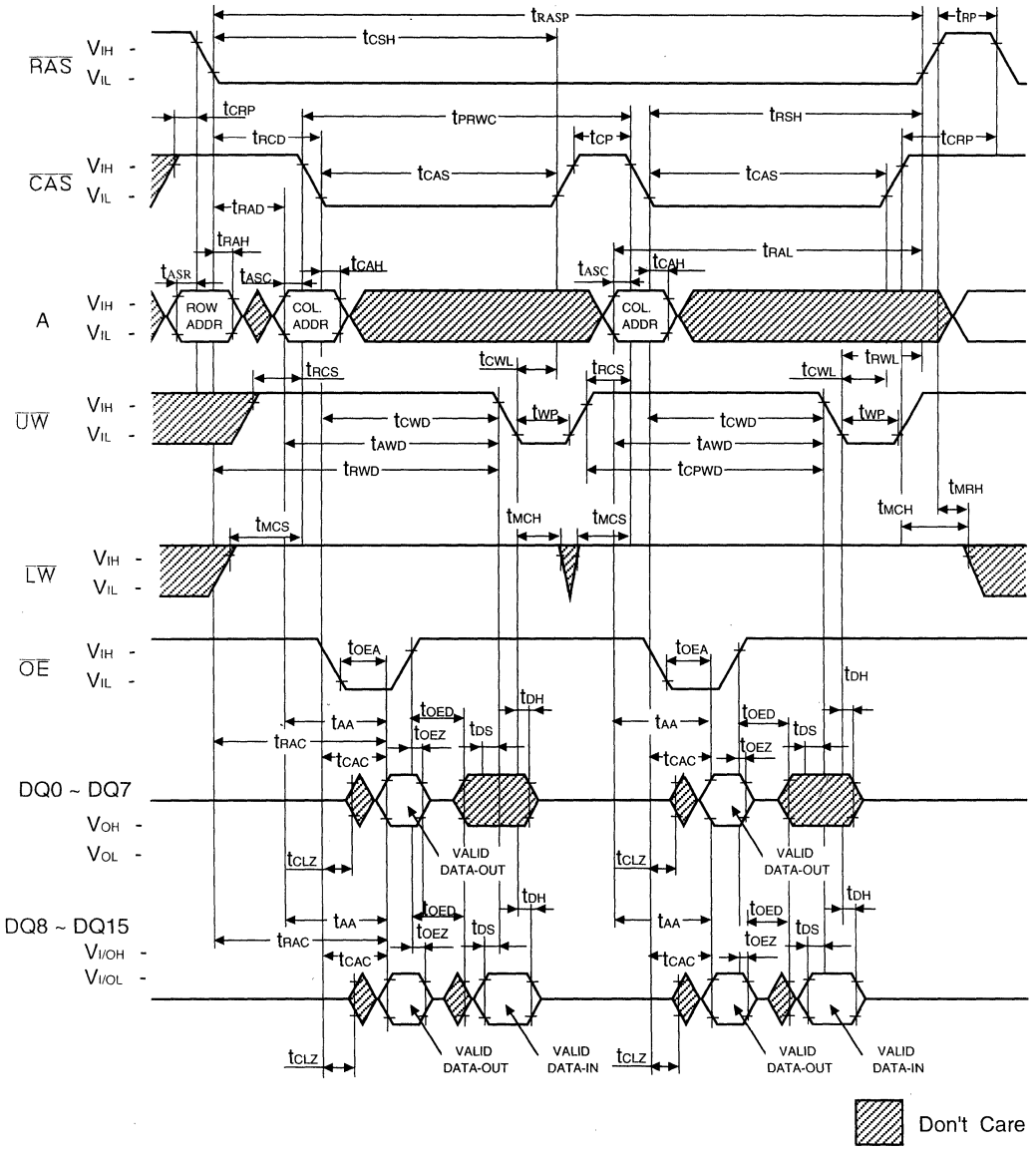
Don't Care

FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE



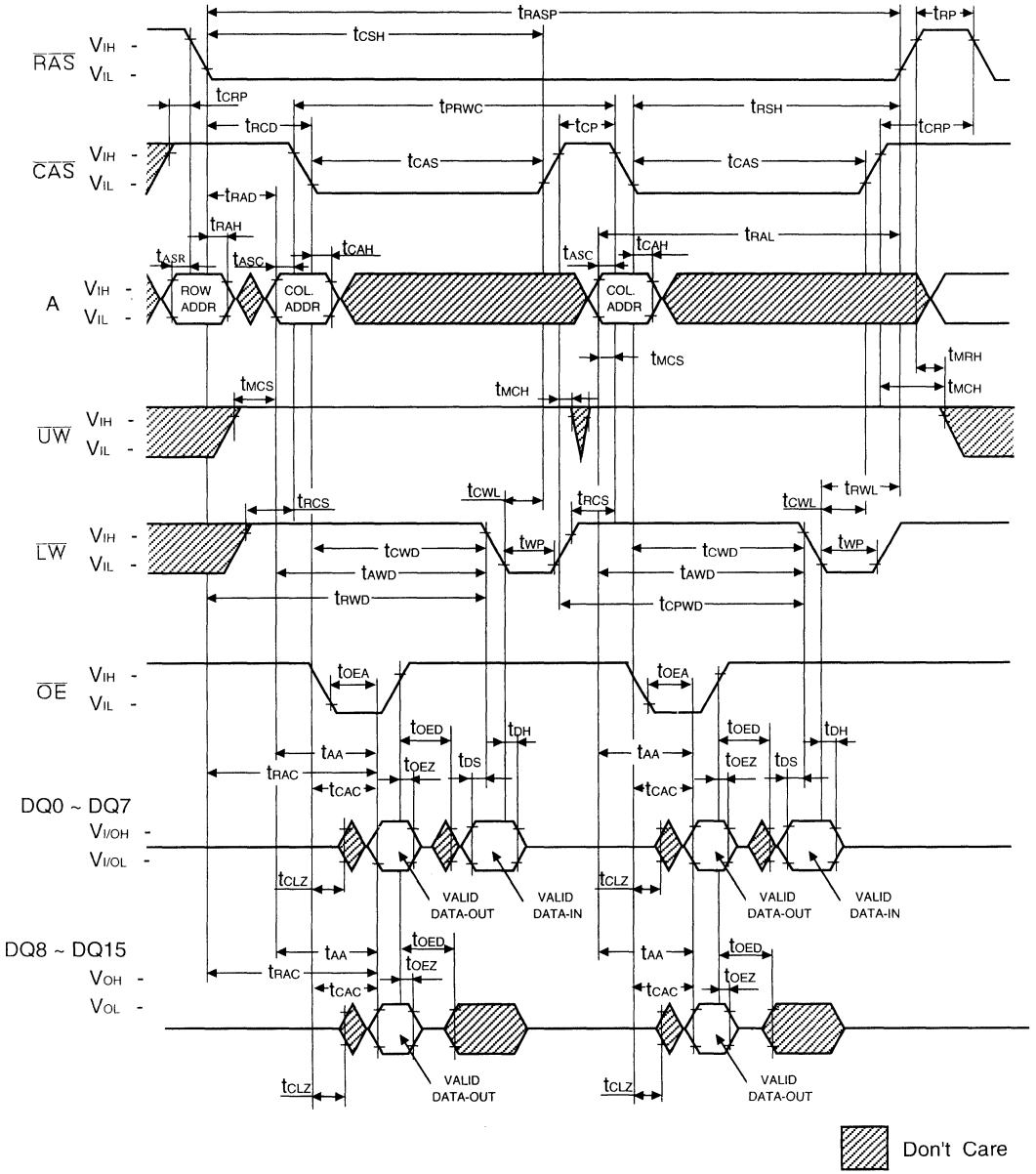
SAMSUNG ELECTRONICS

FAST PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



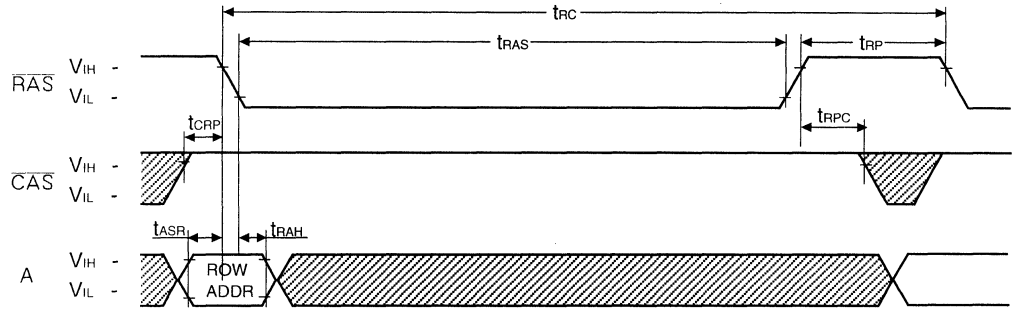
SAMSUNG ELECTRONICS

FAST PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



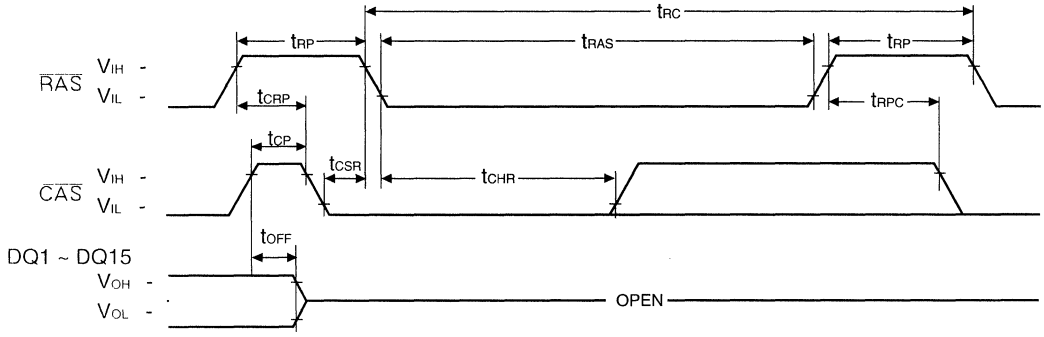
RAS-ONLY REFRESH CYCLE

NOTE : W, OE , DIN = Don't care
DOUT = Open



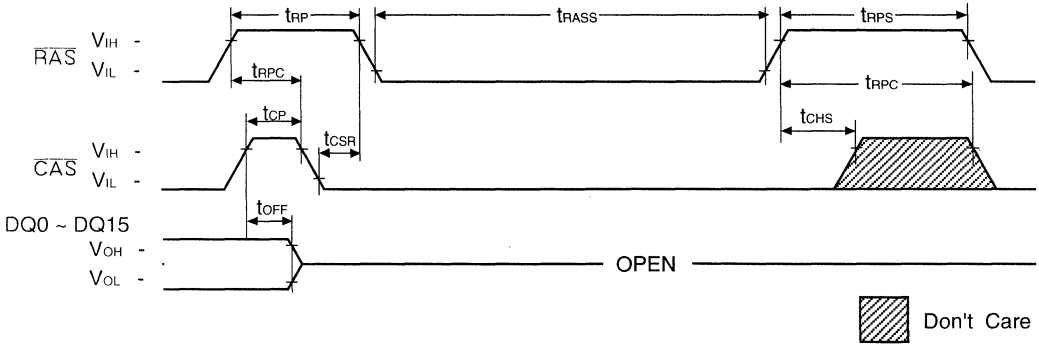
CAS-BEFORE-RAS REFRESH CYCLE

NOTE : W, OE, A = Don't Care

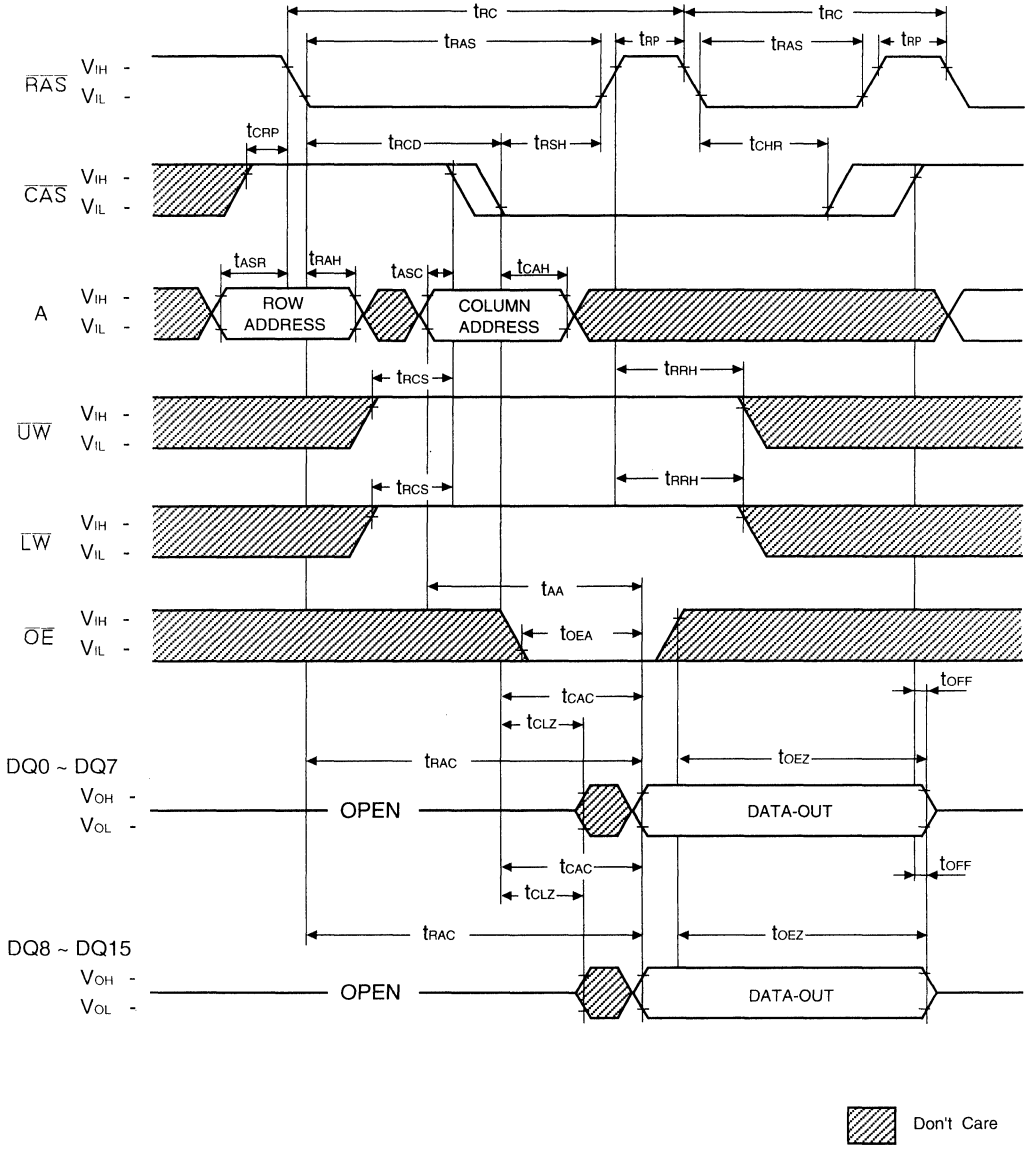


CAS-BEFORE-RAS SELF REFRESH CYCLE

NOTE : W, OE, A = Don't Care

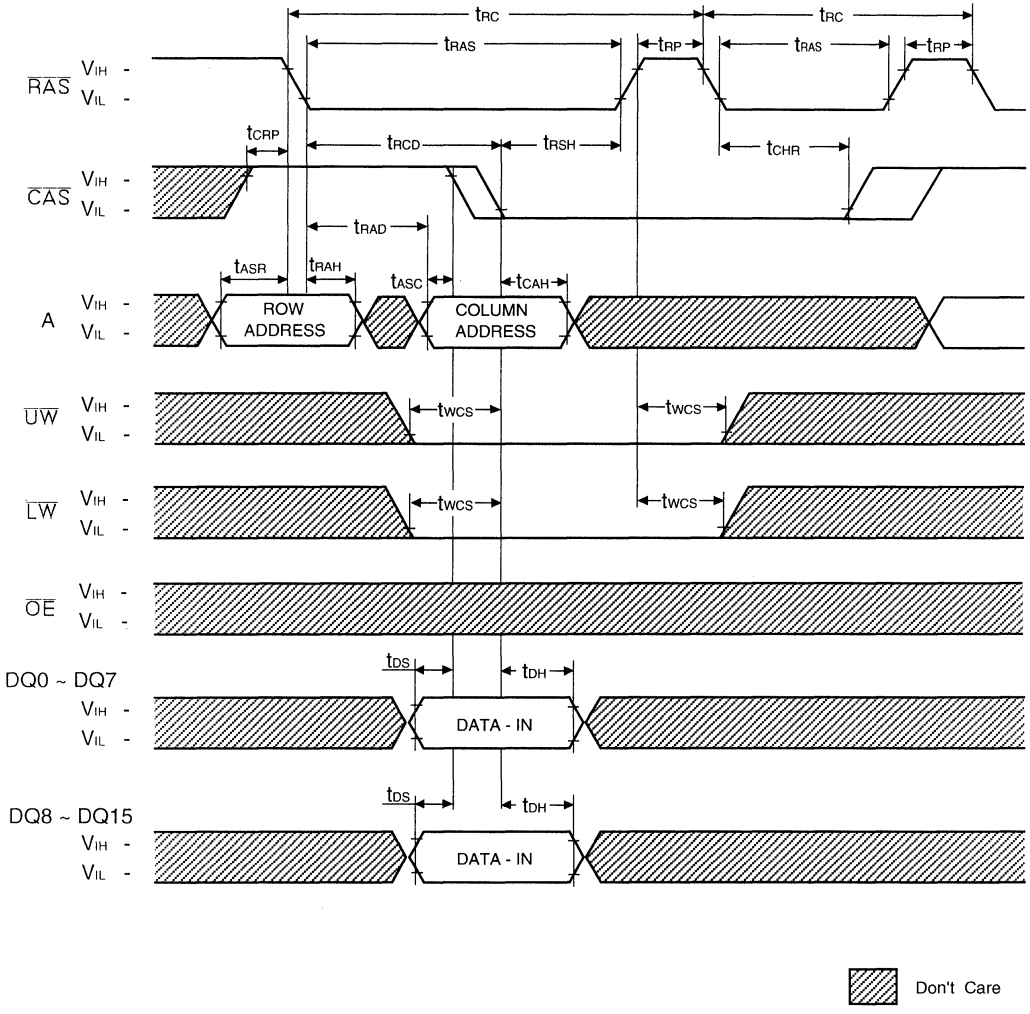


HIDDEN REFRESH CYCLE (READ)

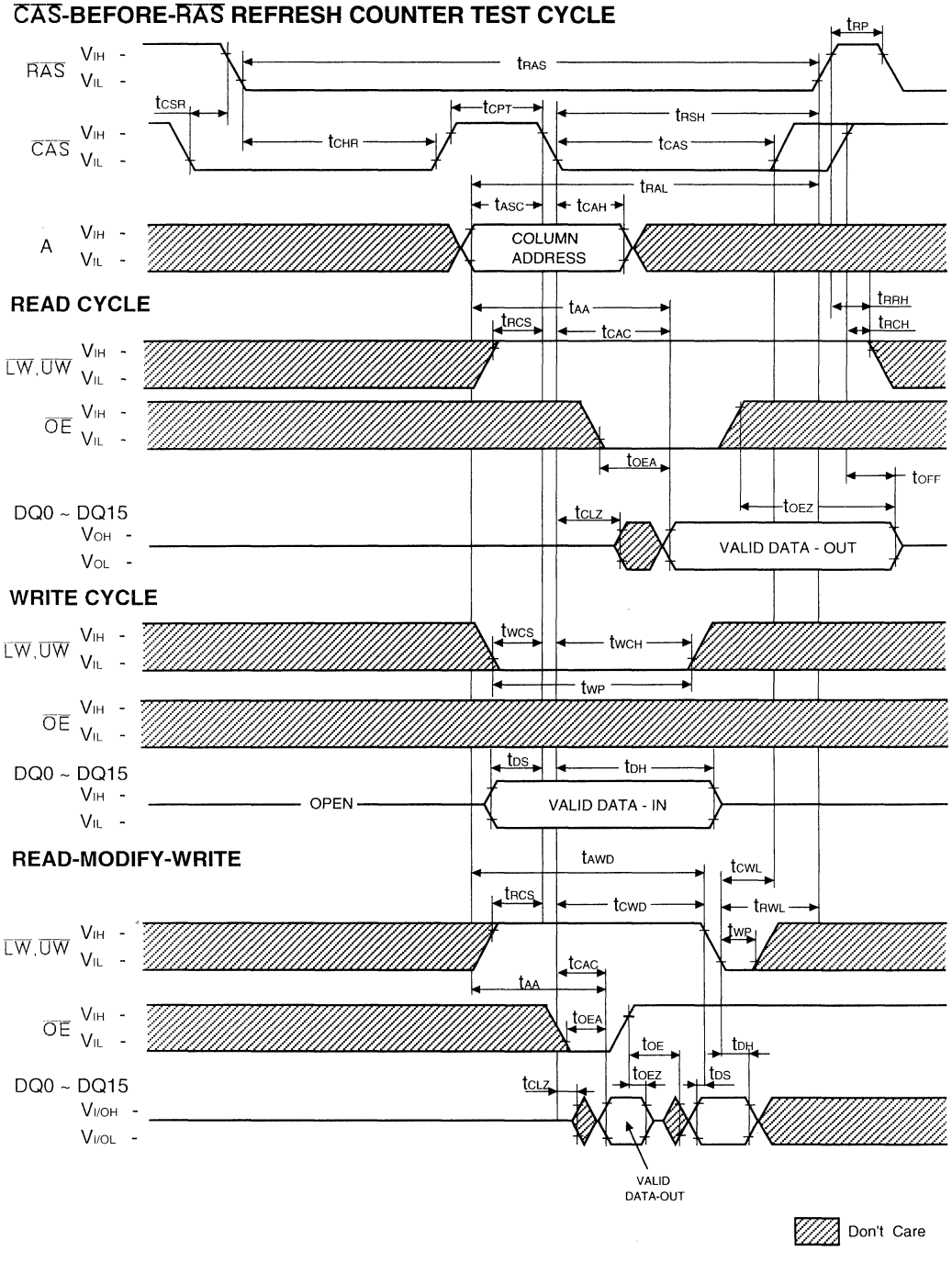


HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

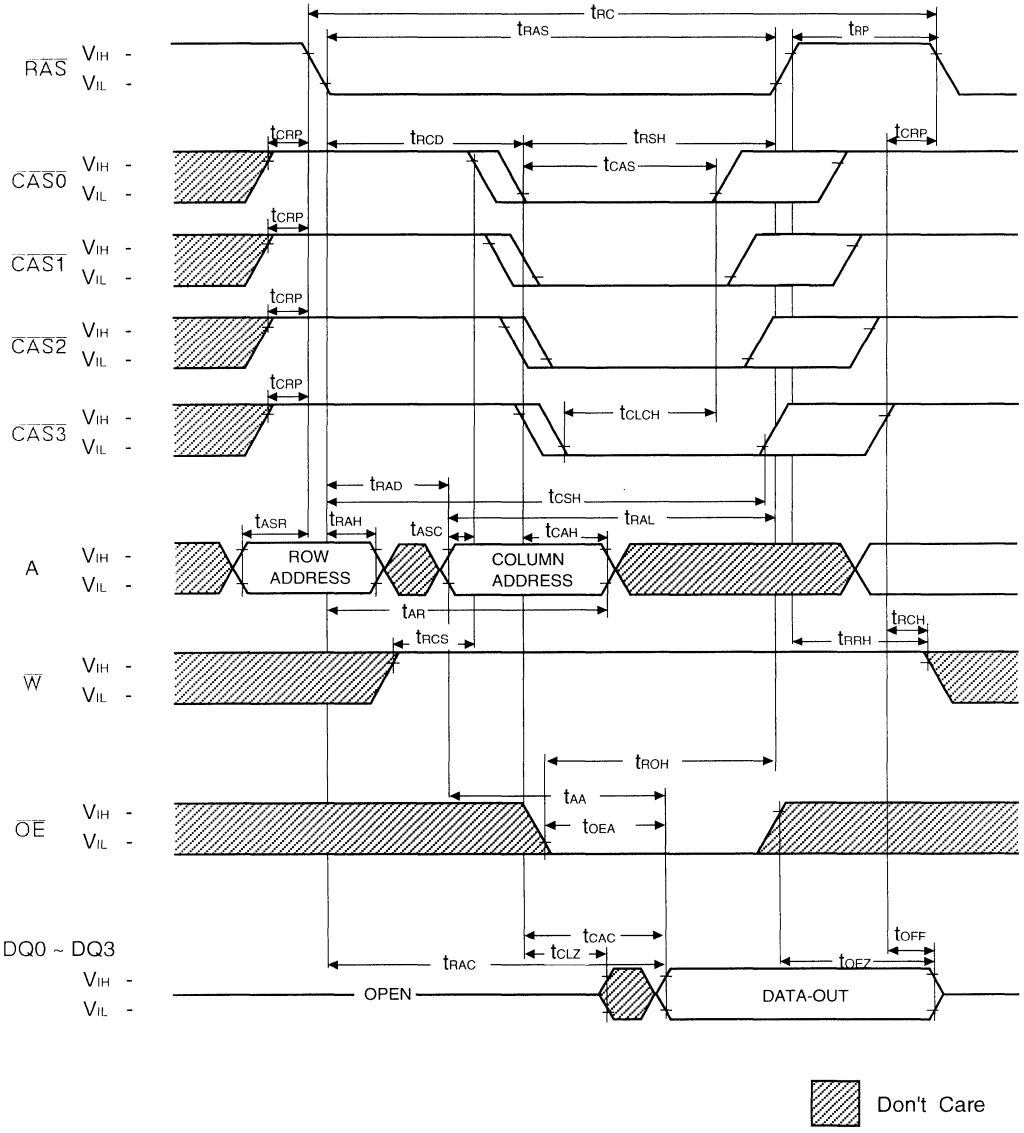


Fast page Mode, Quad $\overline{CAS}$ Device

TIMING DIAGRAM

READ CYCLE

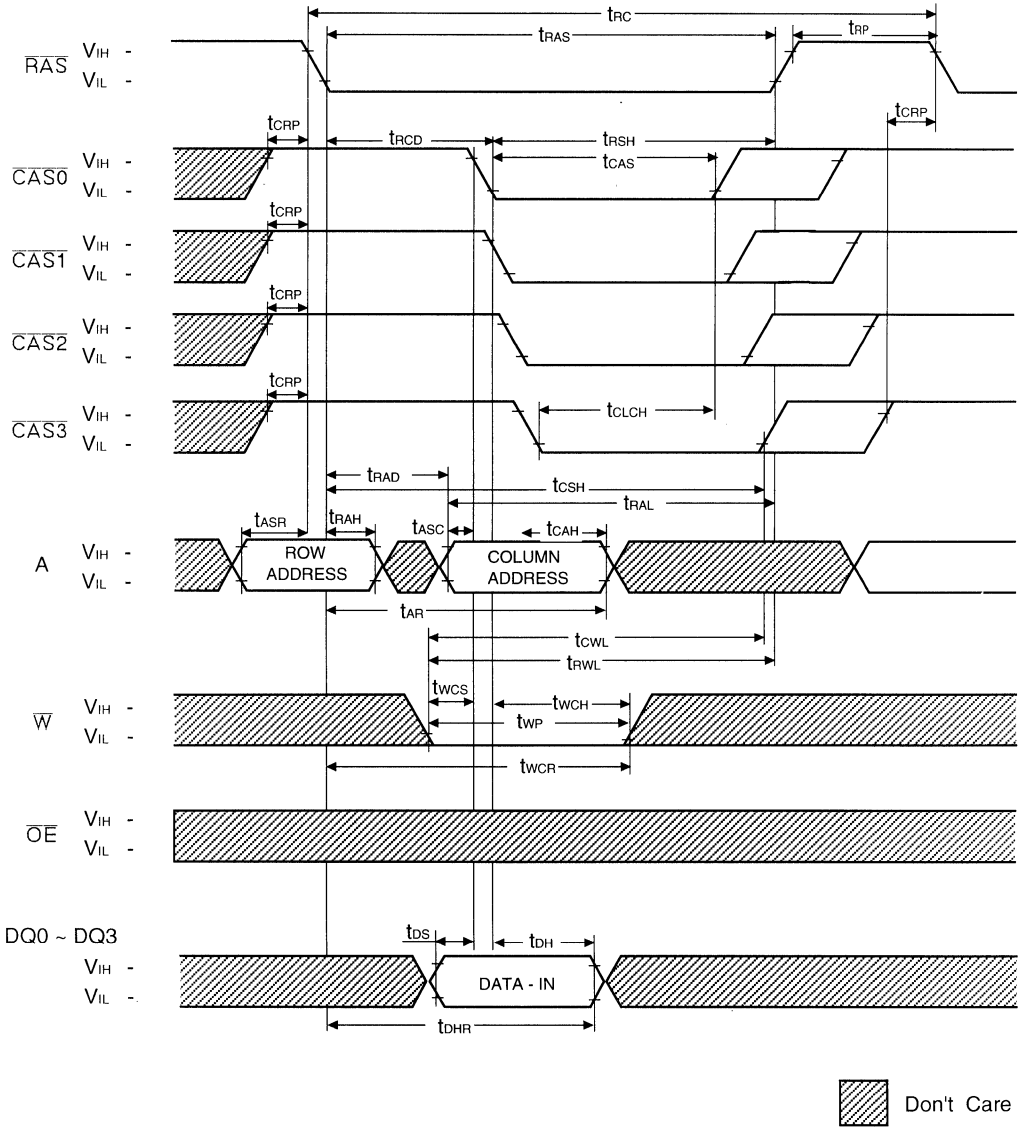
NOTE : D_{IN} = OPEN



SAMSUNG ELECTRONICS

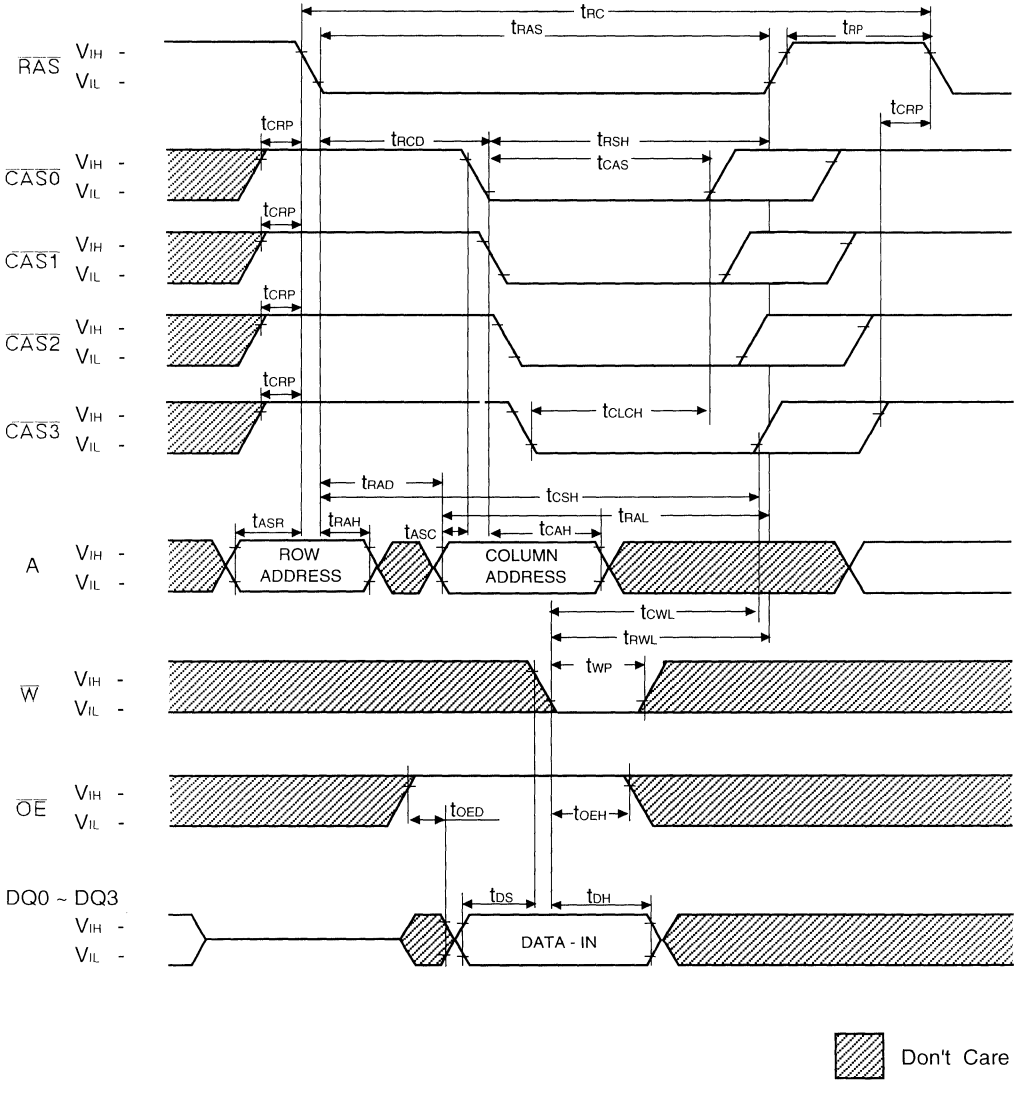
TIMING DIAGRAM

WRITE CYCLE (EARLY WRITE)



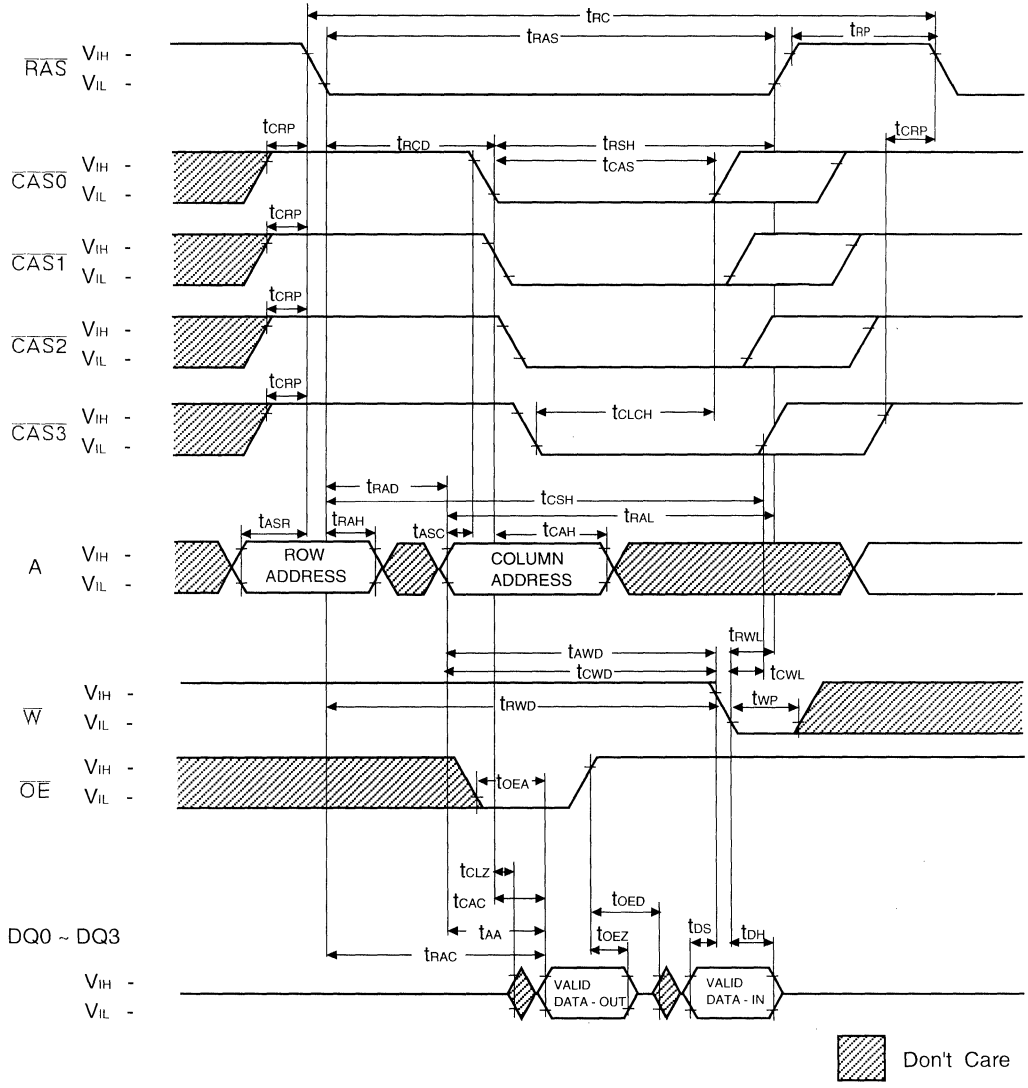
TIMING DIAGRAM

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

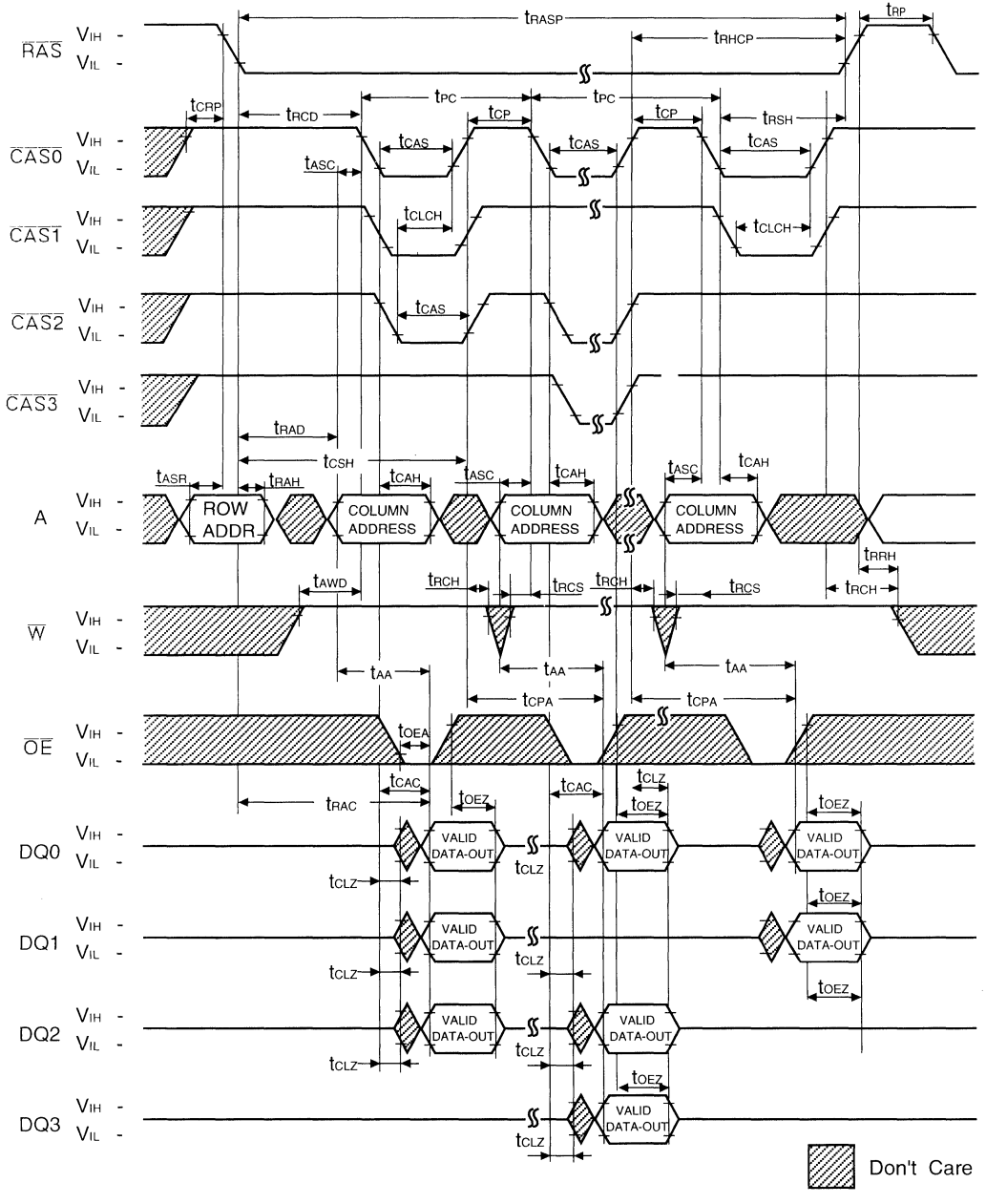


TIMING DIAGRAM

READ - MODIFY - WRITE CYCLE

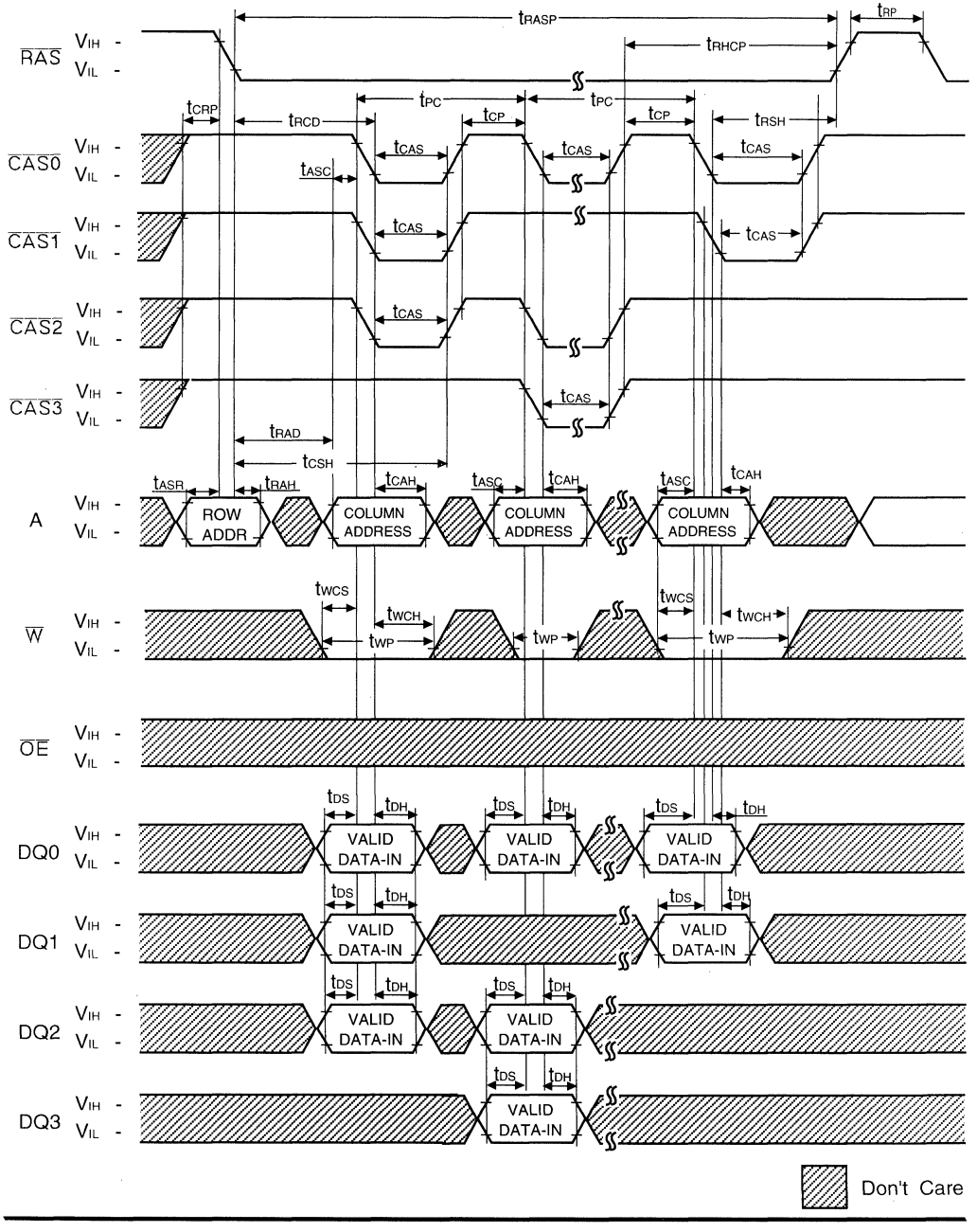


FAST PAGE MODE READ CYCLE

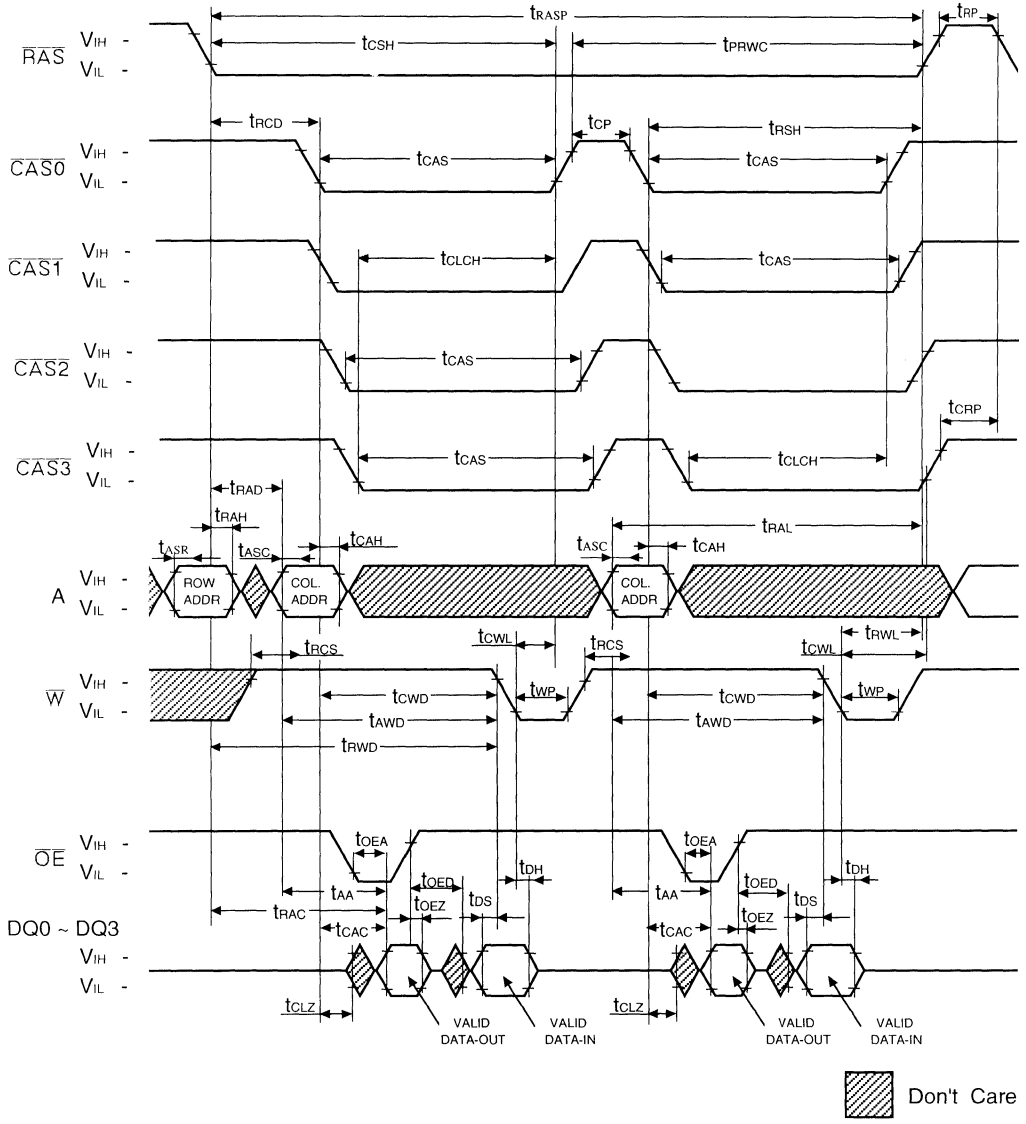


SAMSUNG ELECTRONICS

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

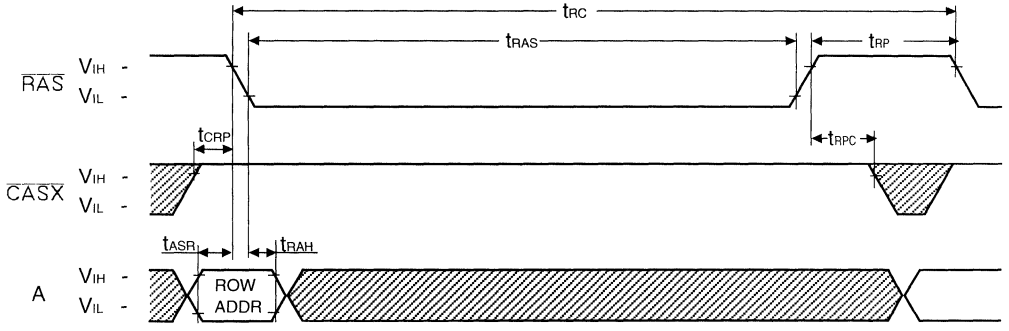


FAST PAGE MODE READ-MODIFY-WRITE CYCLE



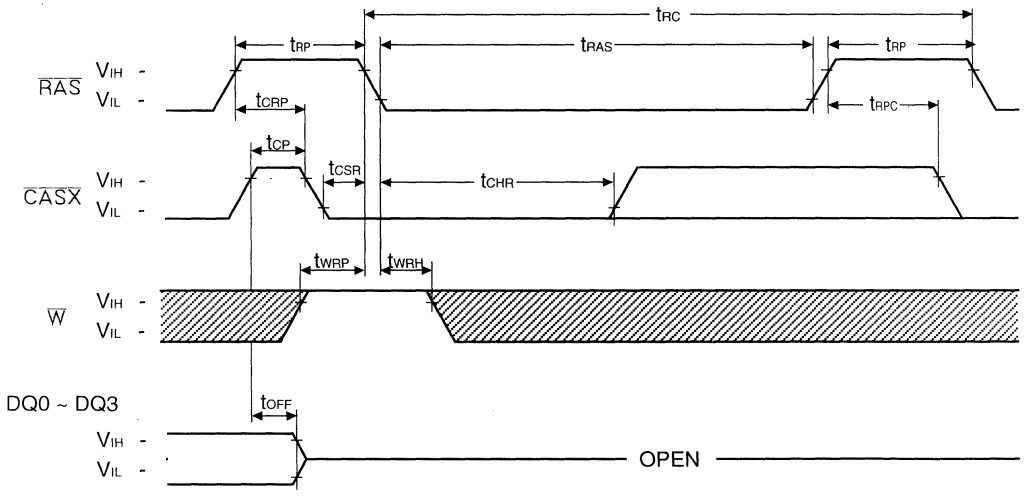
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

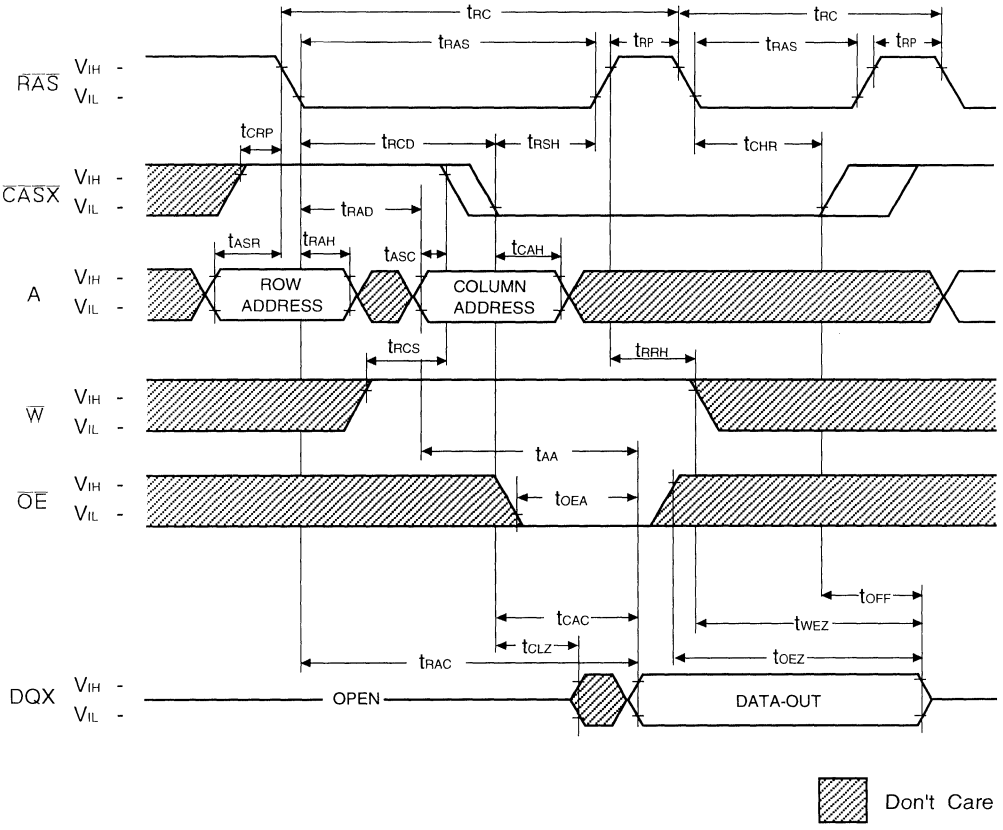
NOTE : $\overline{OE}$, A = Don't Care



Don't Care

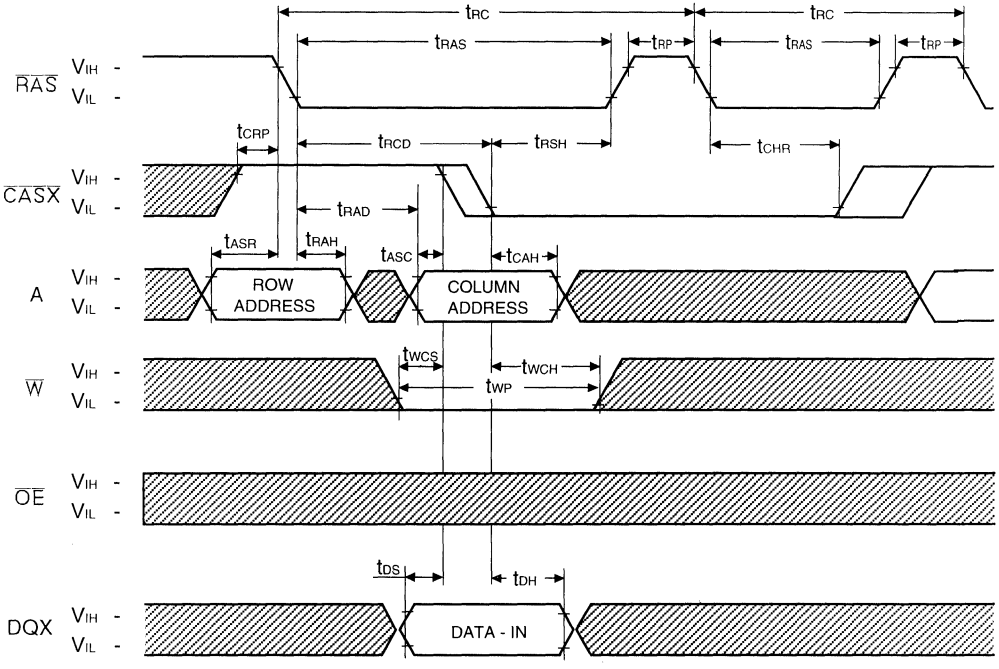
SAMSUNG ELECTRONICS

HIDDEN REFRESH CYCLE (READ)



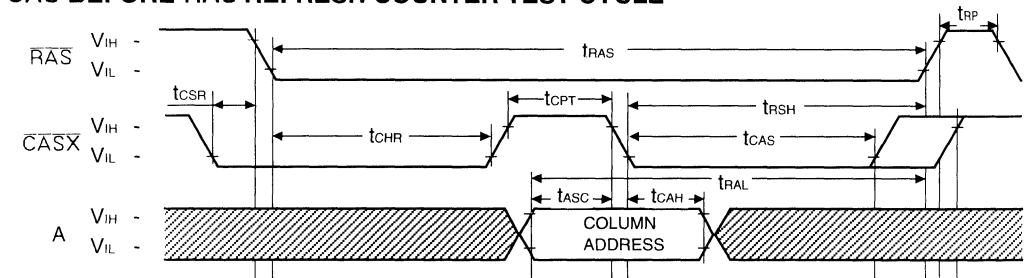
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN

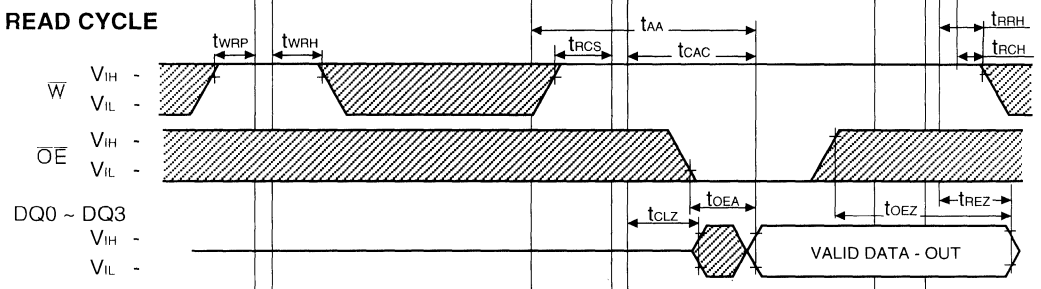


Don't Care

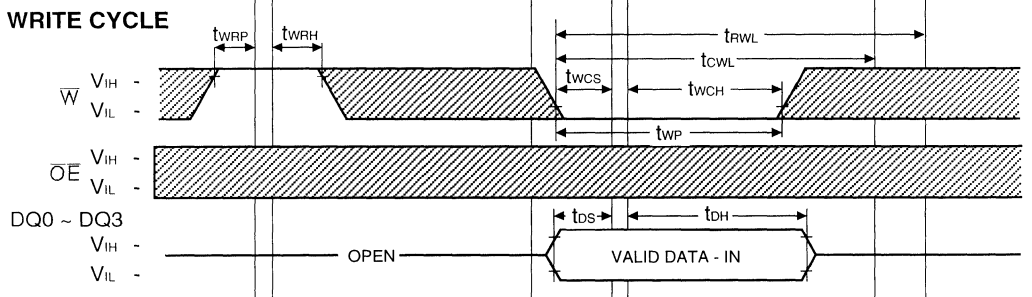
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



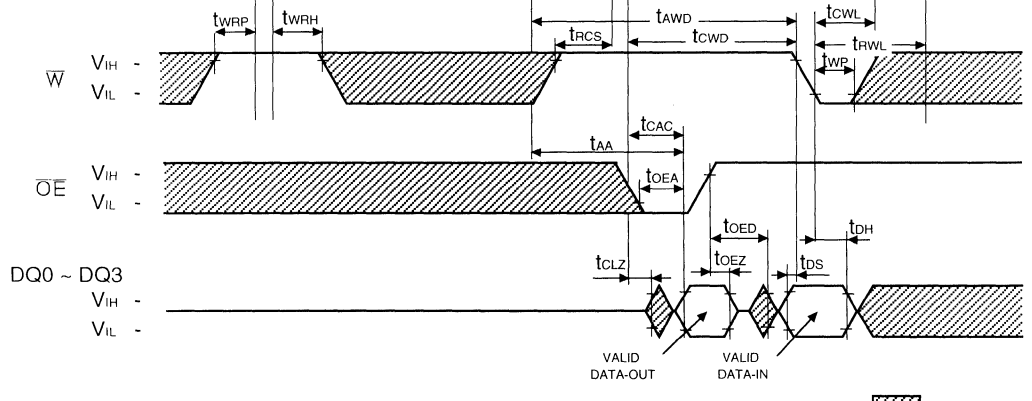
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE

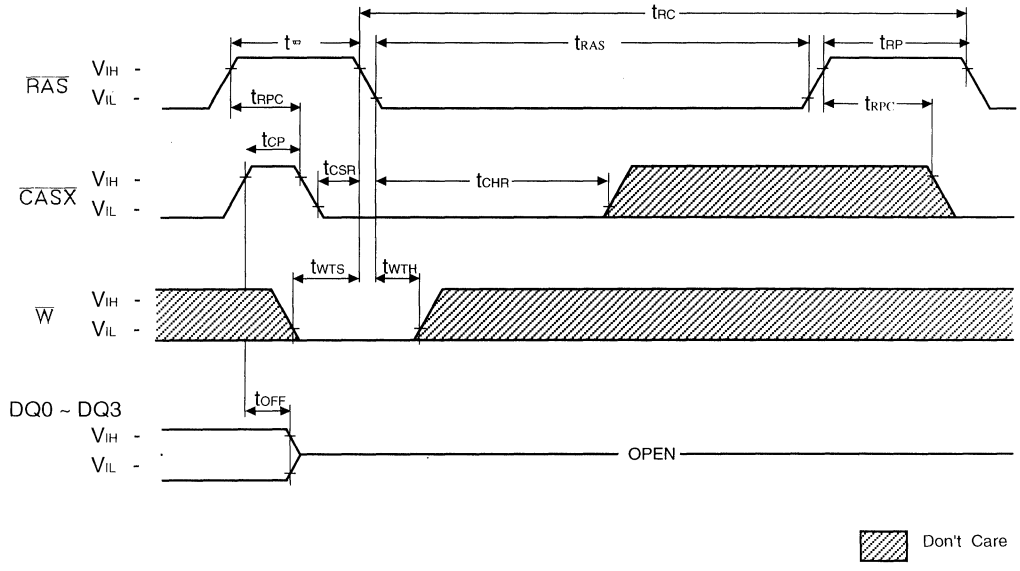


Don't Care

SAMSUNG ELECTRONICS

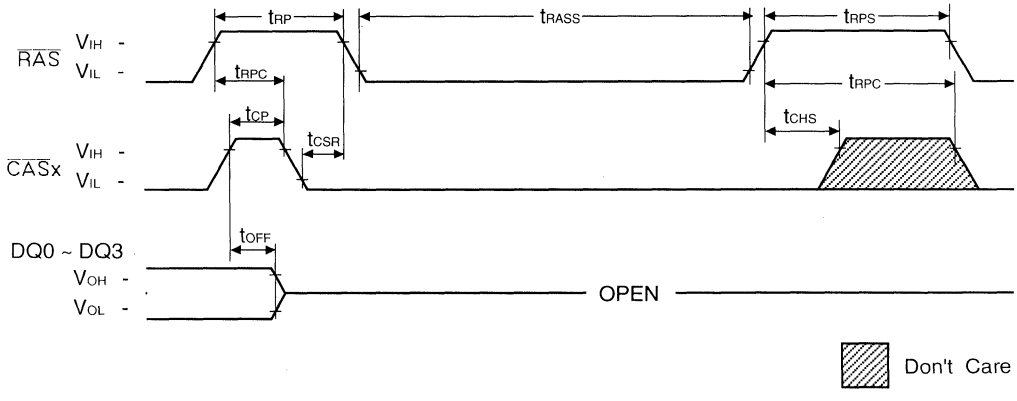
TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

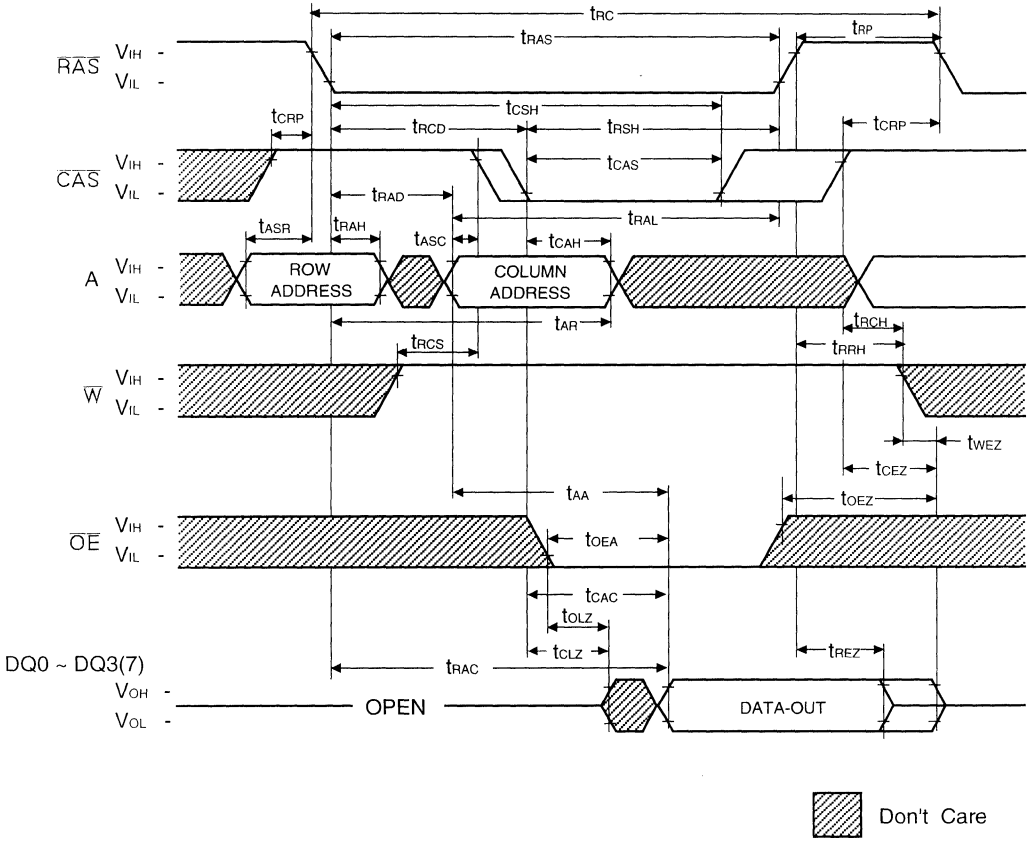


SAMSUNG ELECTRONICS

EDO Mode, x4 and x8 Device

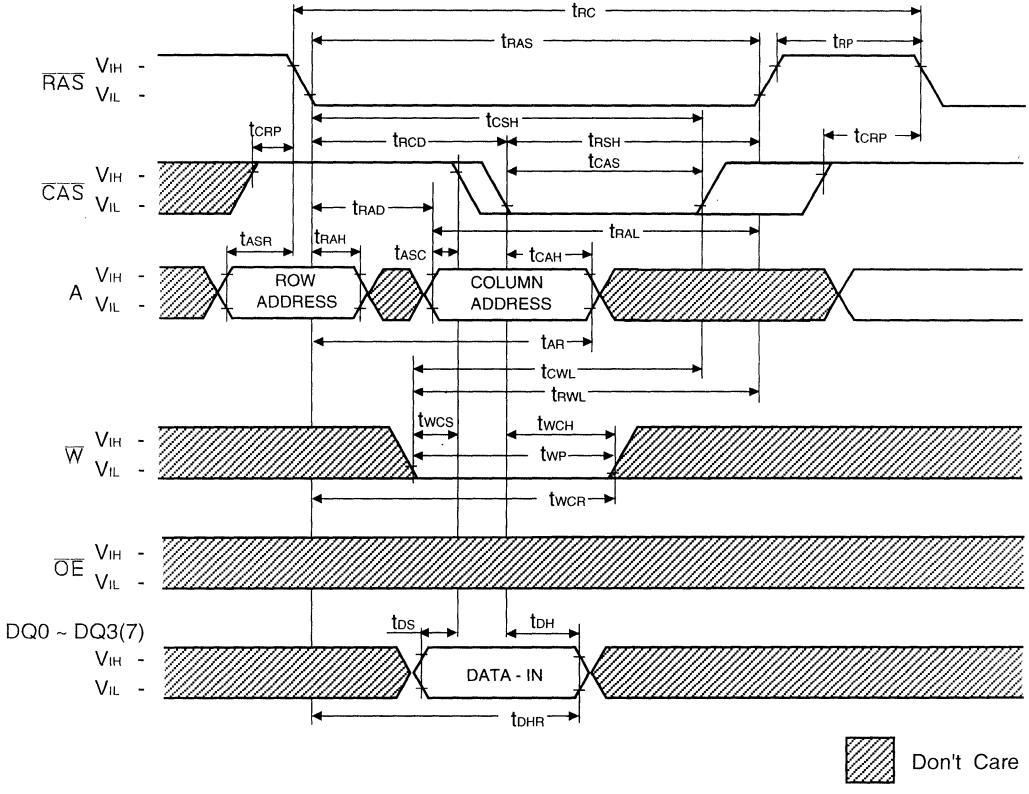
TIMING DIAGRAM

READ CYCLE



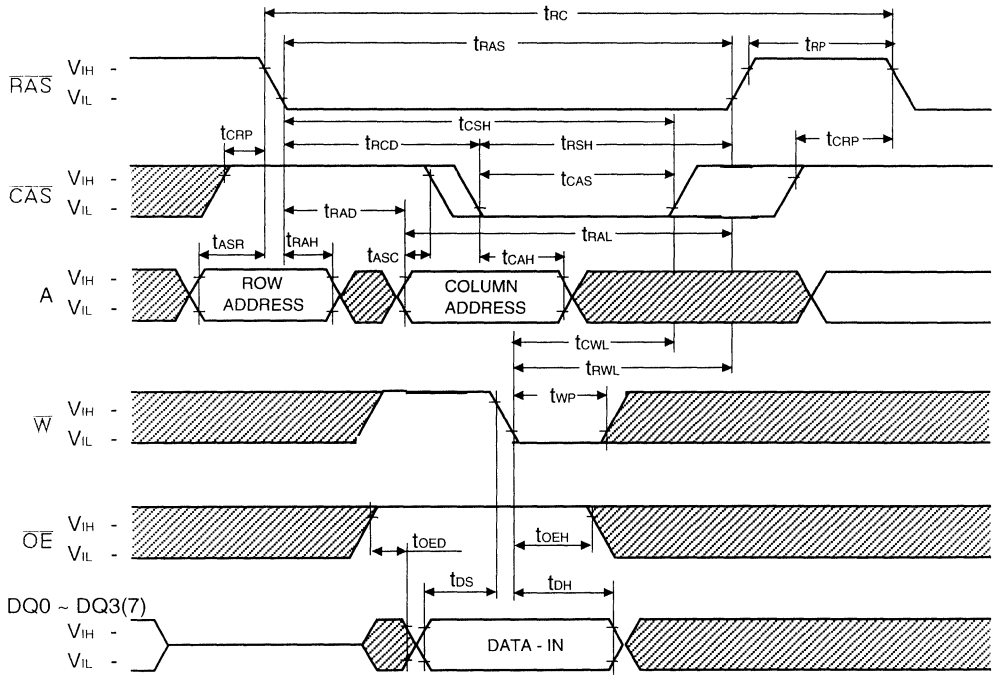
WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

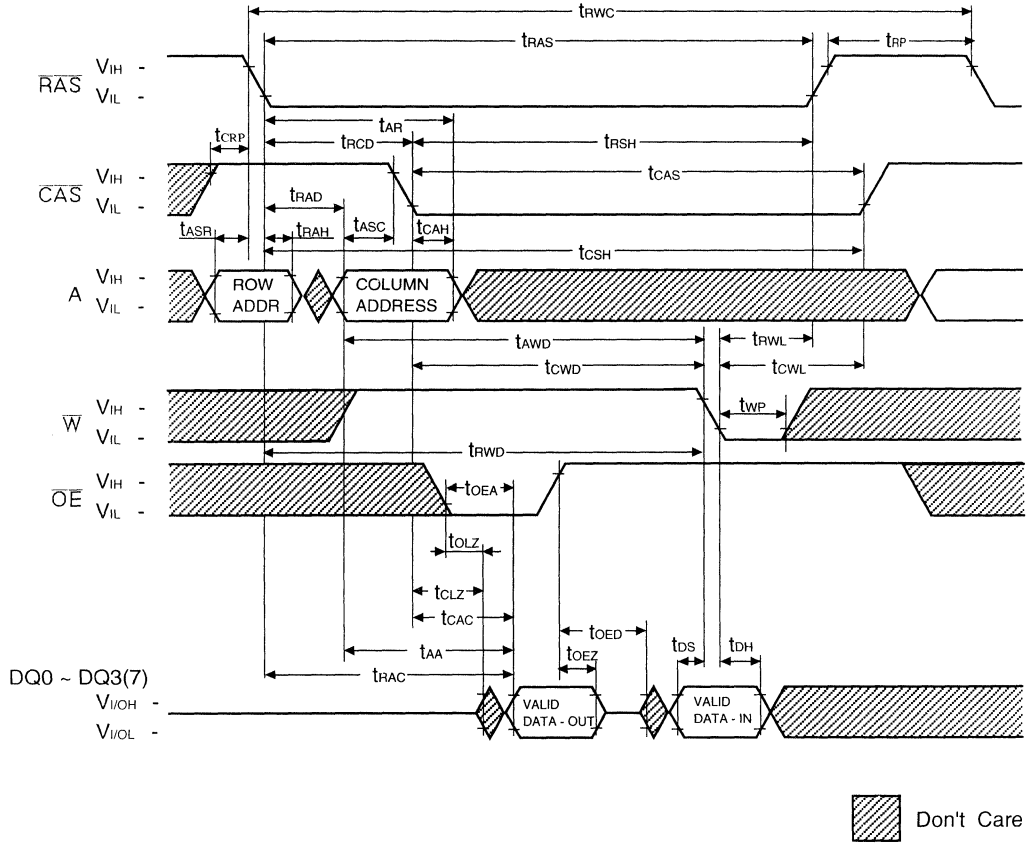
NOTE : D_{OUT} = OPEN



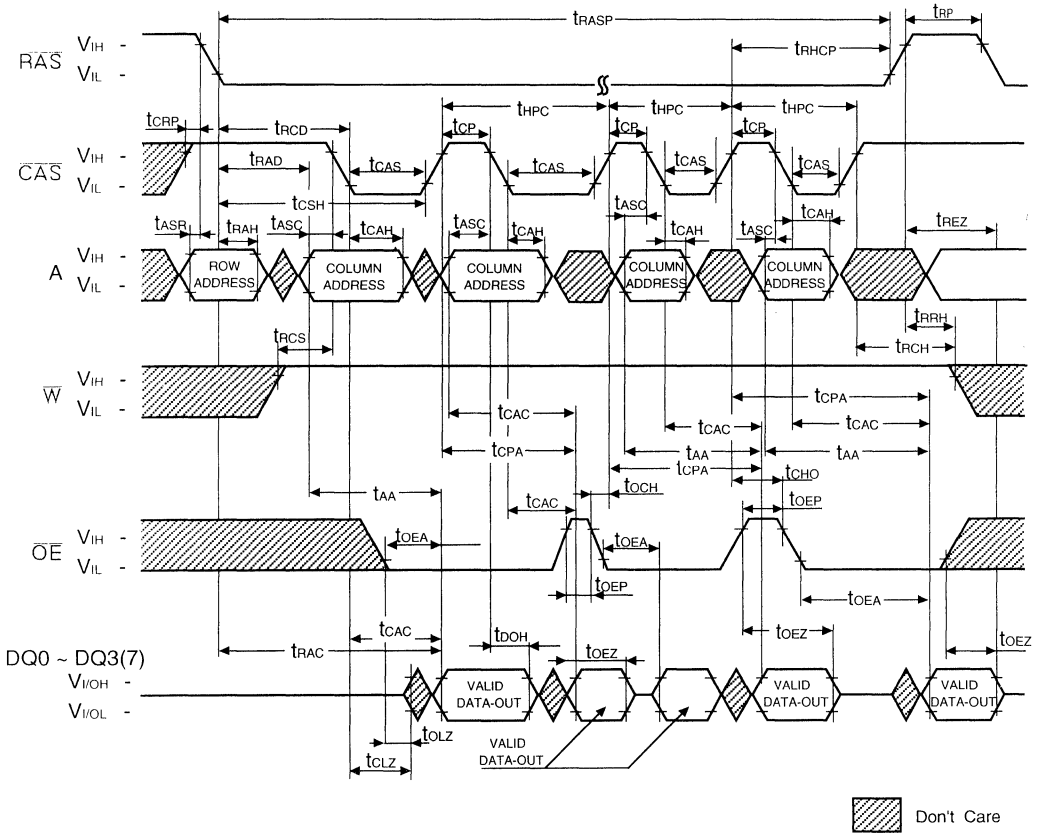
Don't Care

SAMSUNG ELECTRONICS

READ - MODIFY - WRITE CYCLE

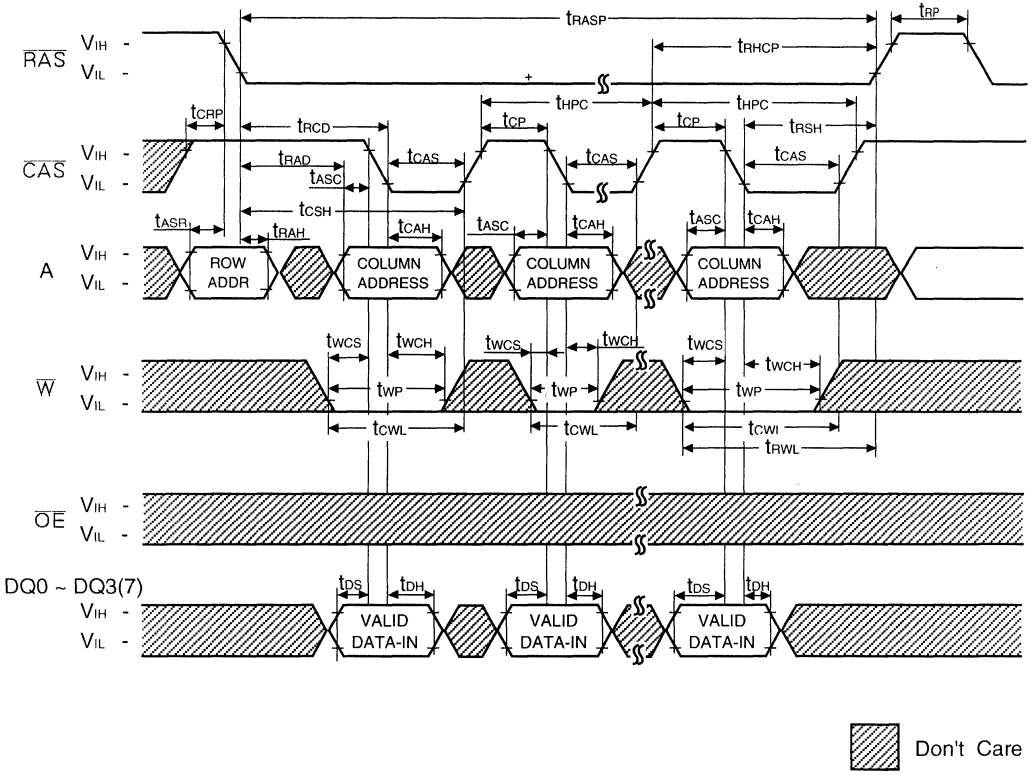


HYPER PAGE READ CYCLE

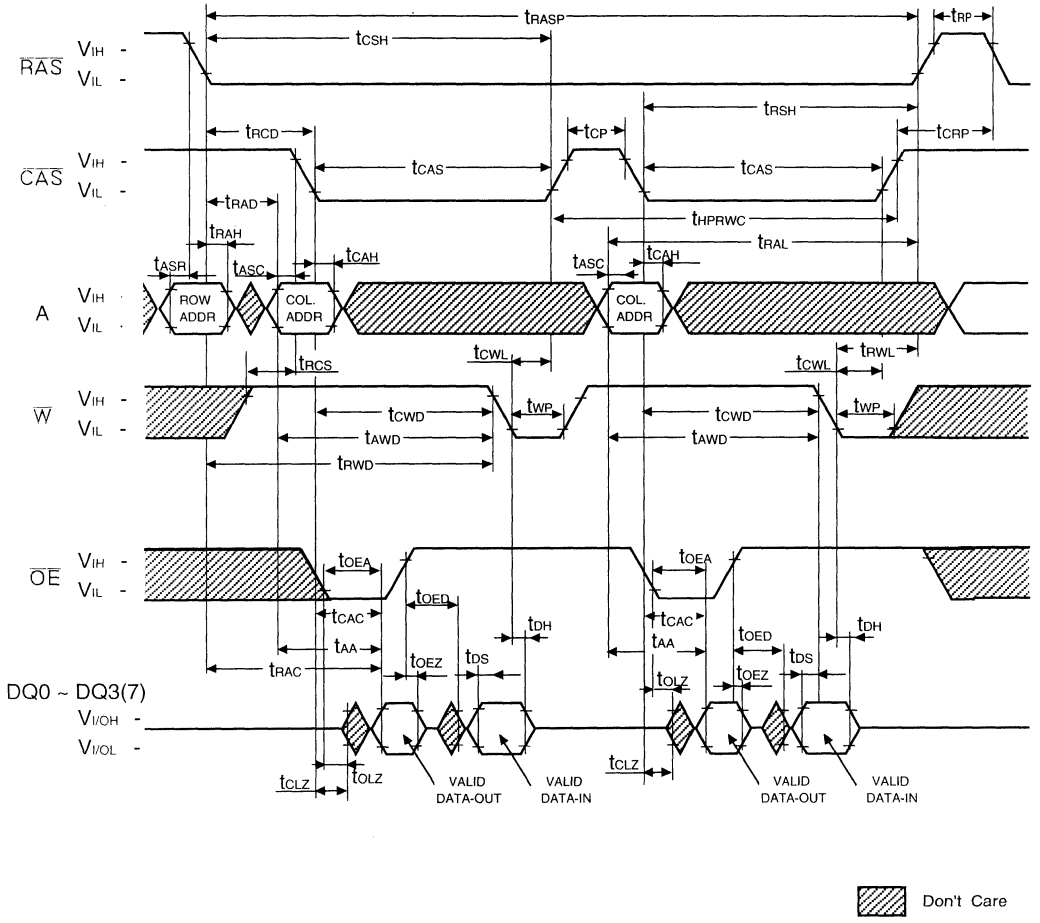


HYPER PAGE WRITE CYCLE (EARLY WRITE)

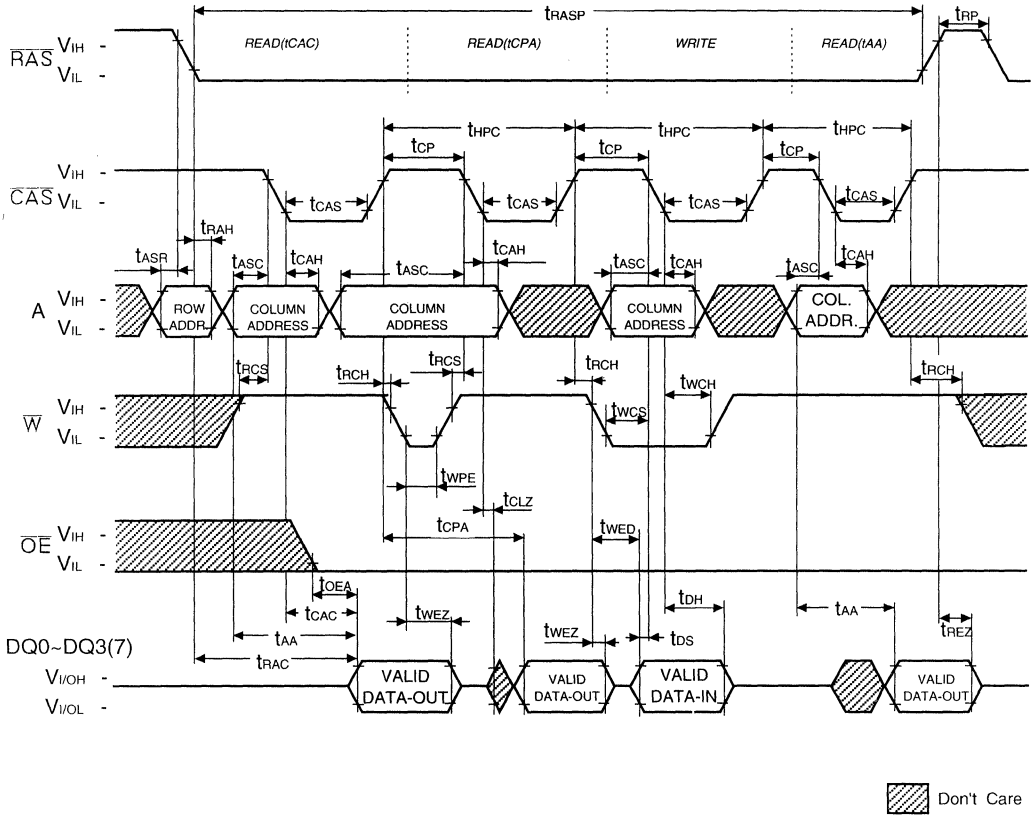
NOTE : D_{OUT} = Open



HYPER PAGE READ-MODIFY-WRITE CYCLE

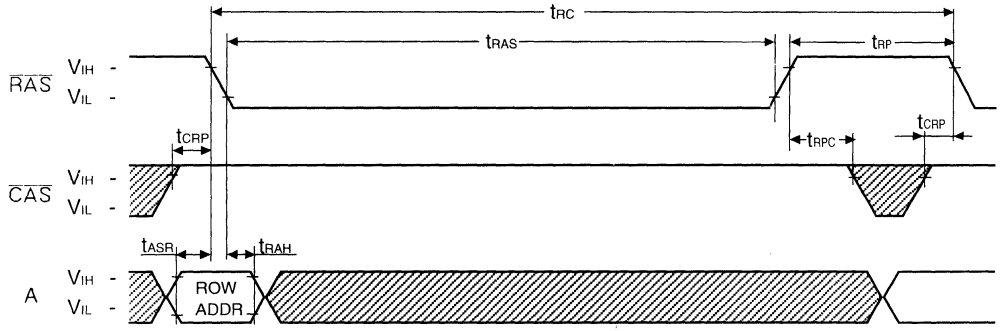


HYPER PAGE READ AND WRITE MIXED CYCLE



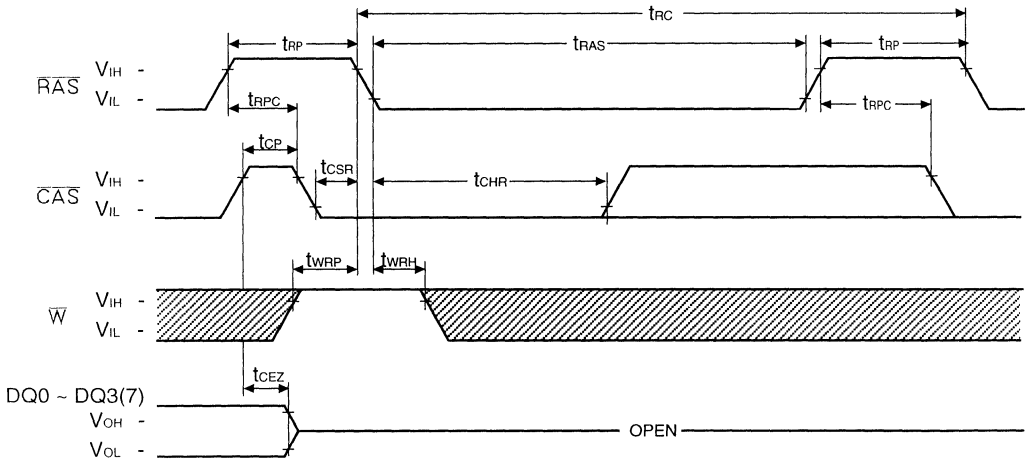
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

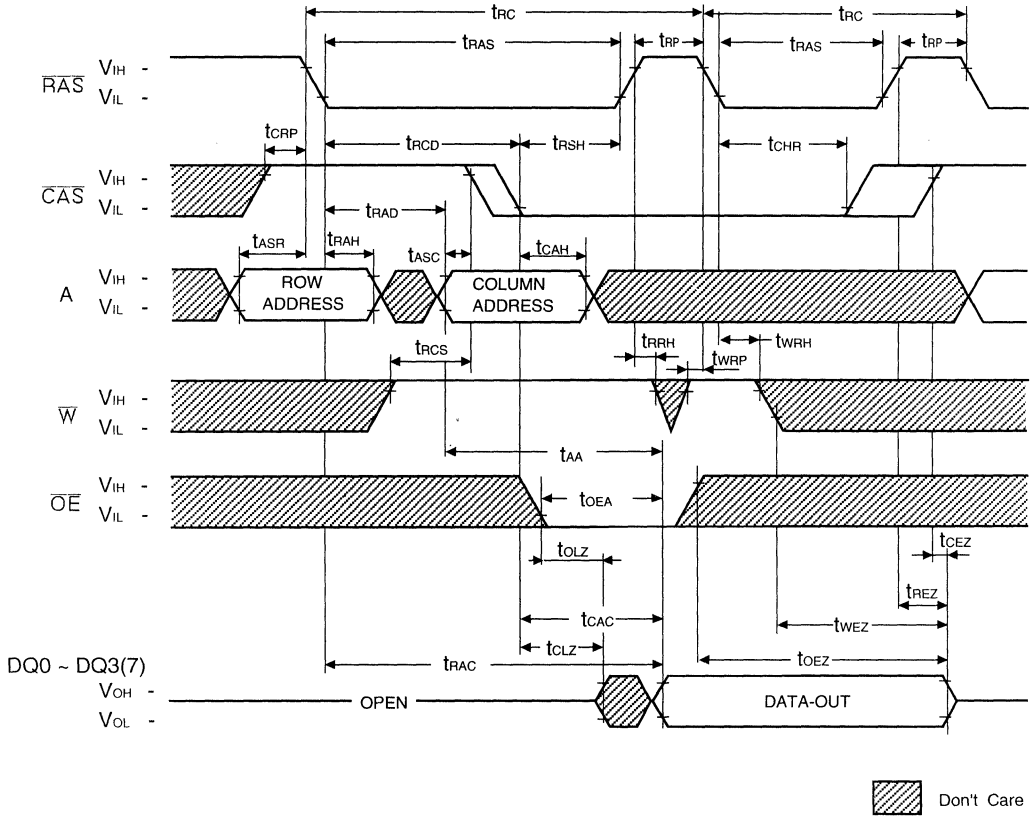
NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



Don't Care

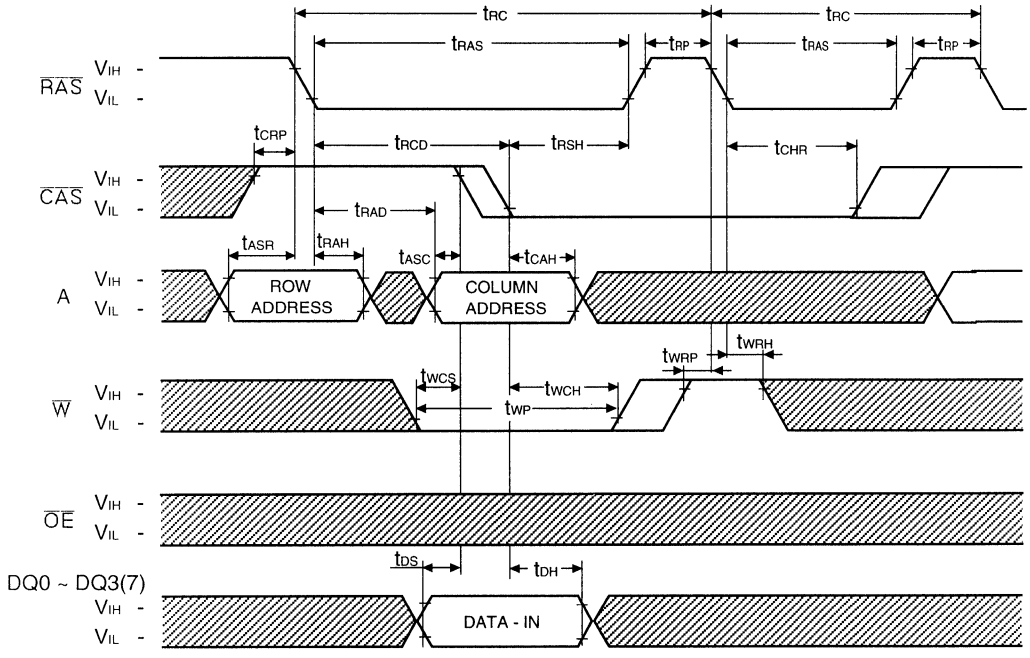
SAMSUNG ELECTRONICS

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

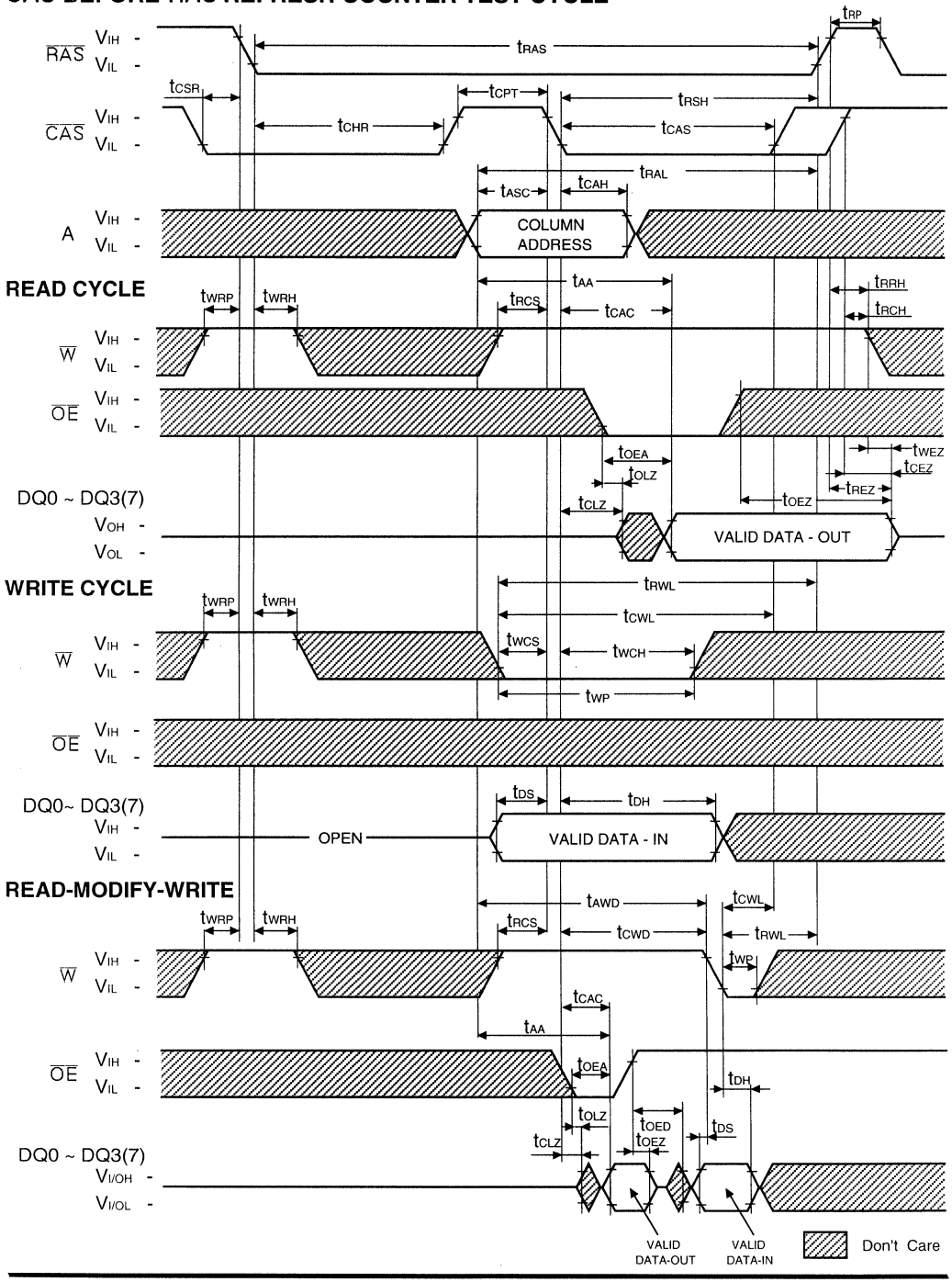
NOTE : D_{OUT} = OPEN



Don't Care

SAMSUNG ELECTRONICS

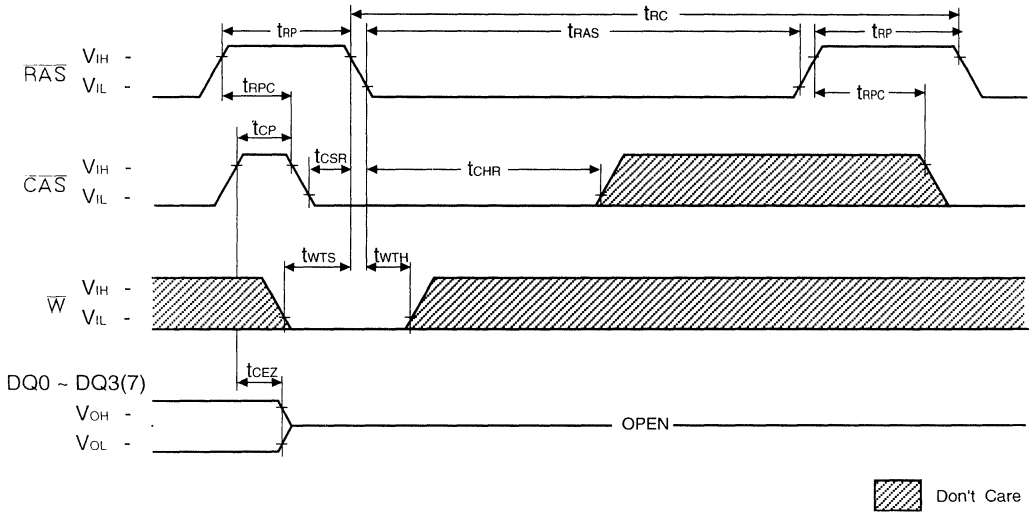
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



SAMSUNG ELECTRONICS

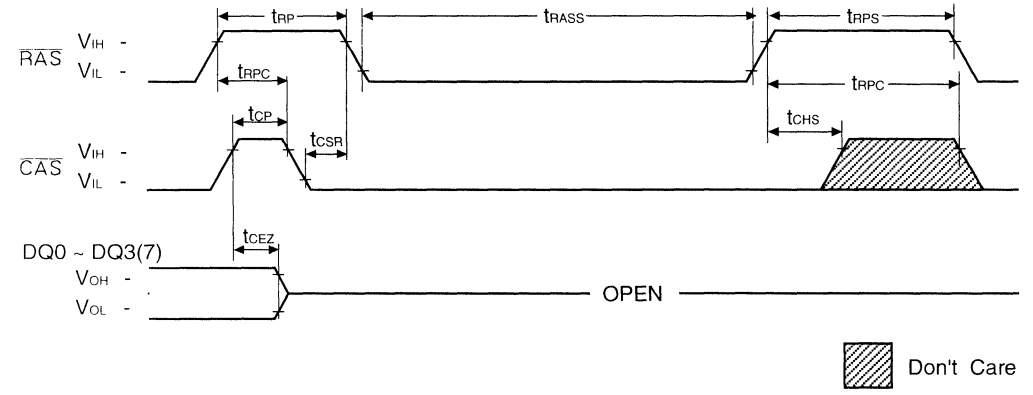
TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE

NOTE : $\overline{W}$=VIH (1Mx4, 4Mx4, 16Mx4, 2Mx8, 8Mx8)
Don't Care (512Kx8)
$\overline{OE}$, A = Don't Care

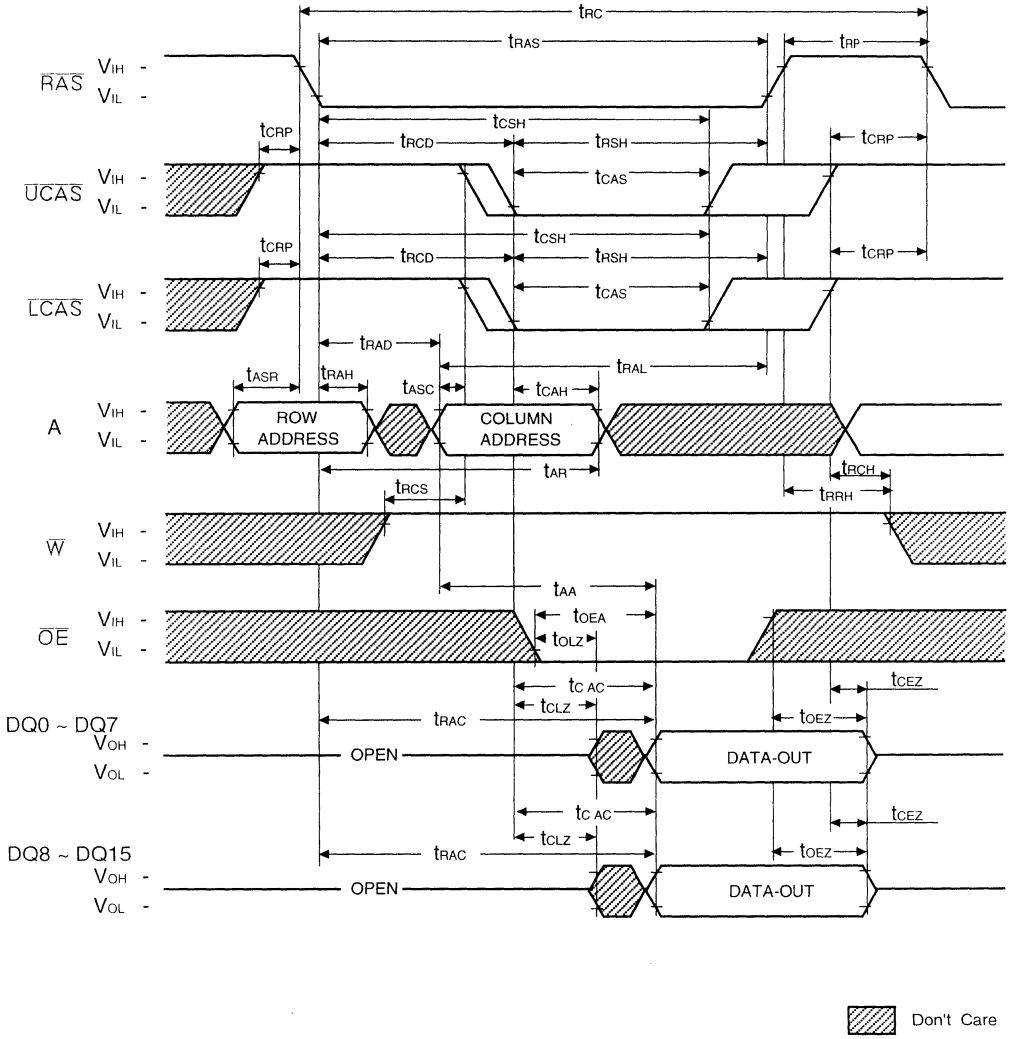


EDO Mode, x16(2CAS) Device

TIMING DIAGRAM

WORD READ CYCLE

NOTE : D_{IN} = OPEN

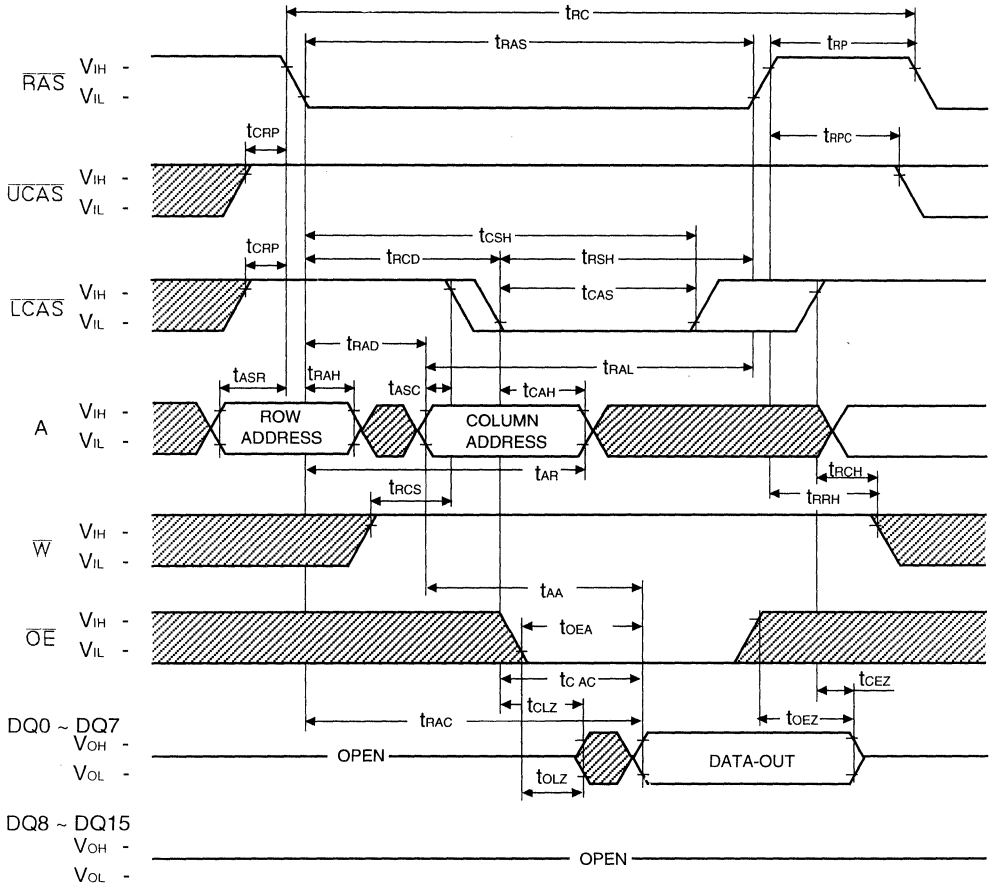


SAMSUNG ELECTRONICS

TIMING DIAGRAM

LOWER BYTE READ CYCLE

NOTE : D_{IN} = OPEN

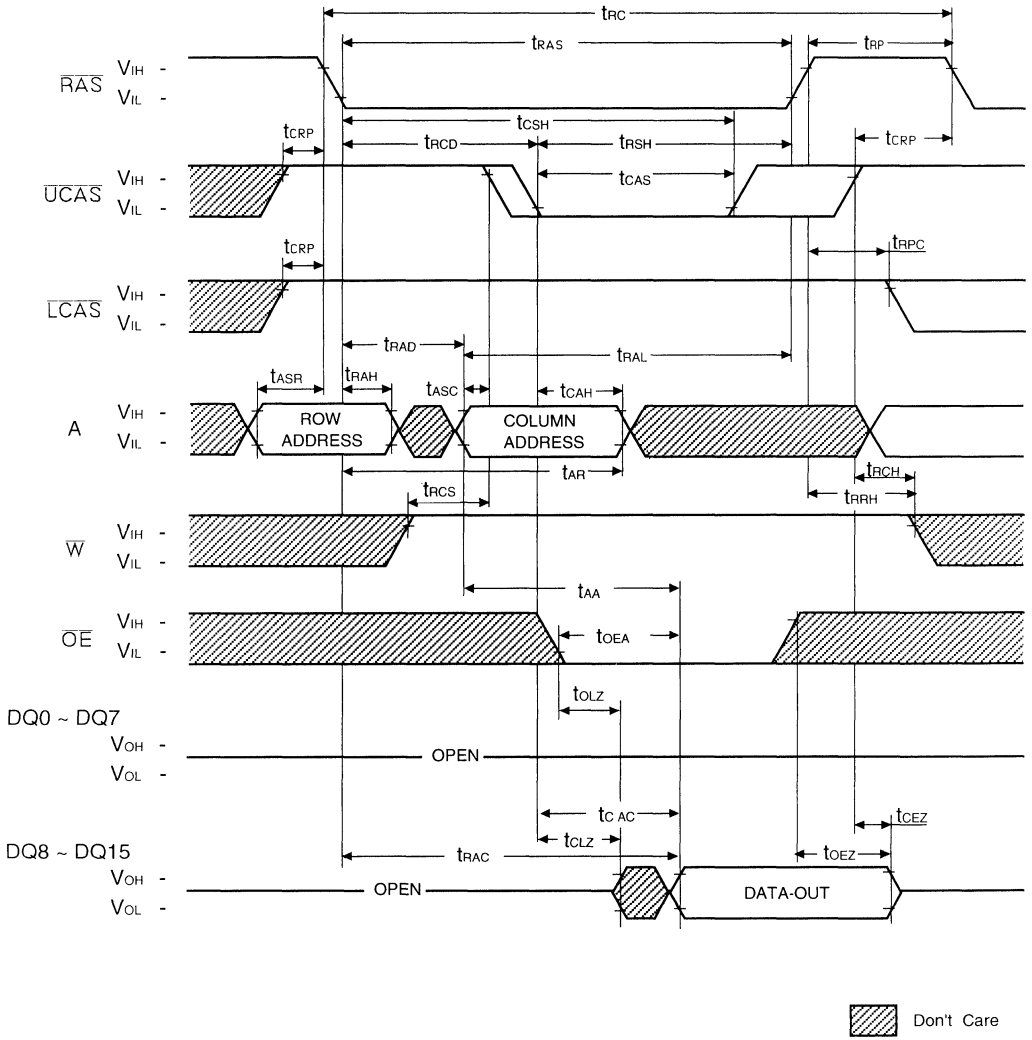


Don't Care

TIMING DIAGRAM

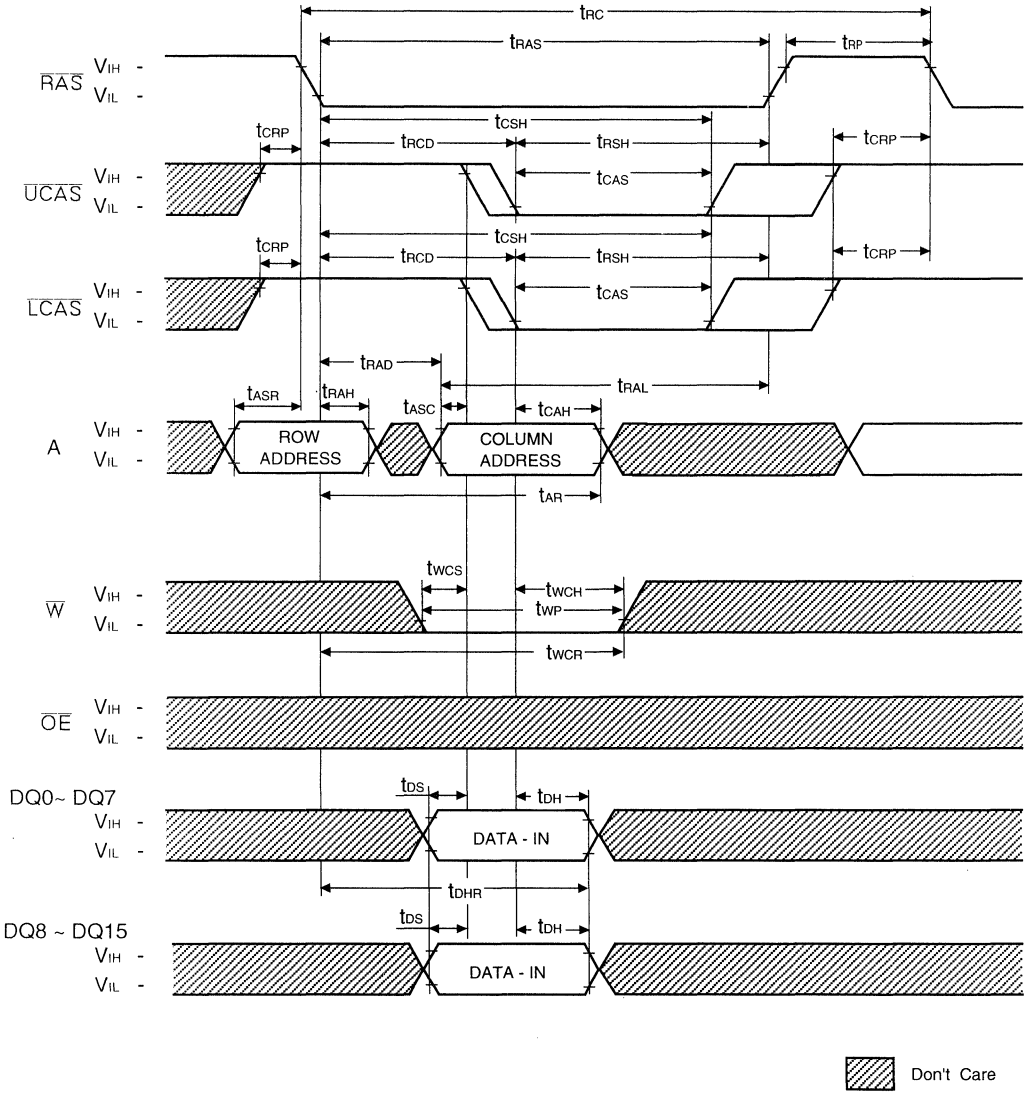
UPPER BYTE READ CYCLE

NOTE : D_{IN} = OPEN



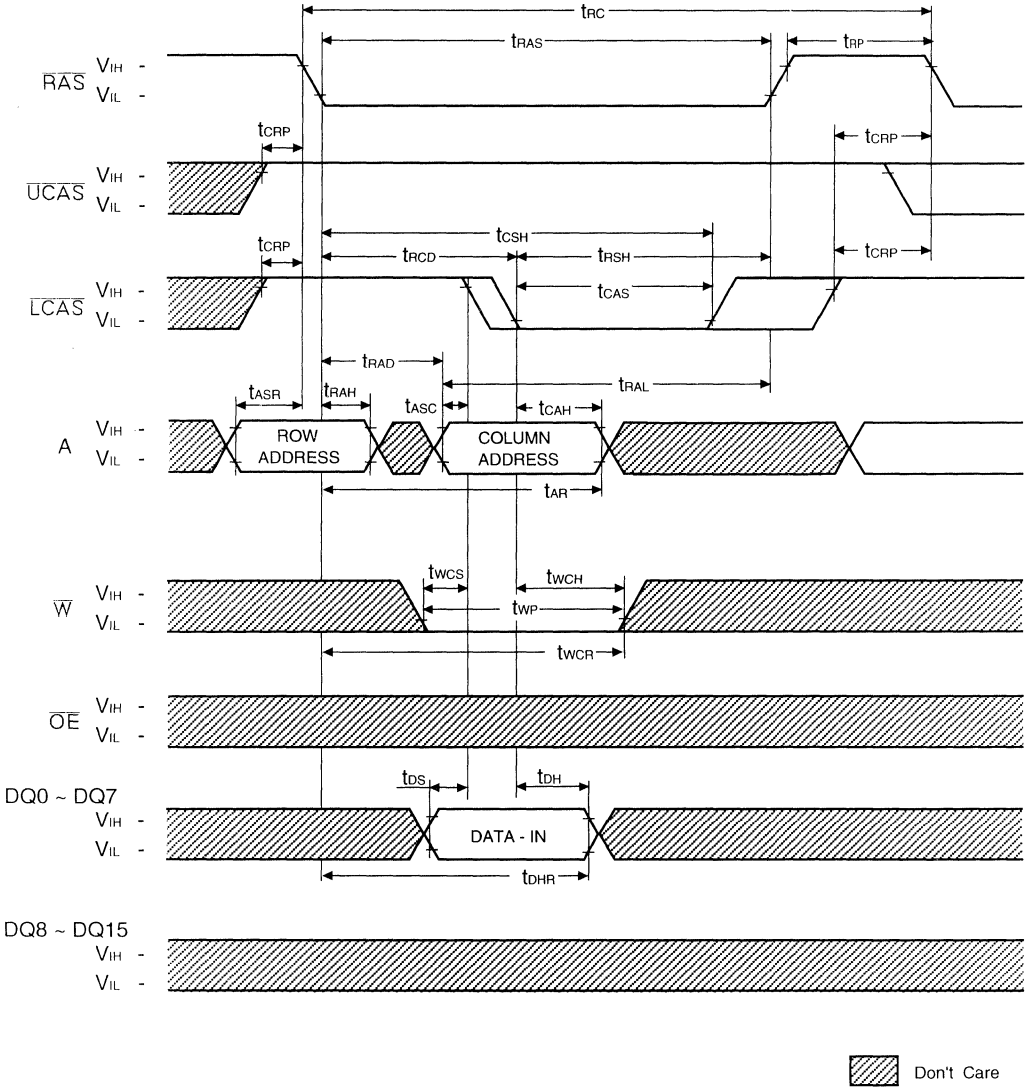
WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



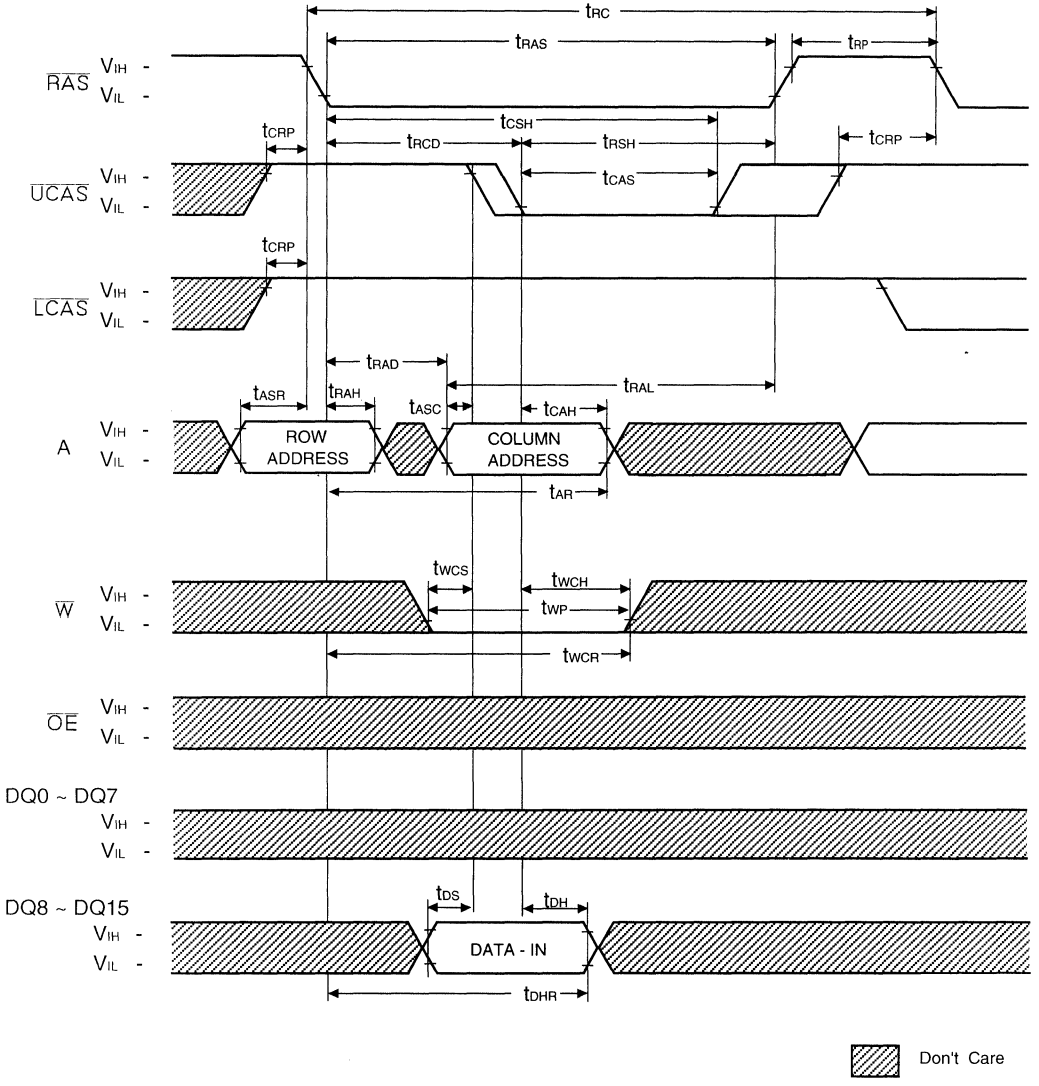
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



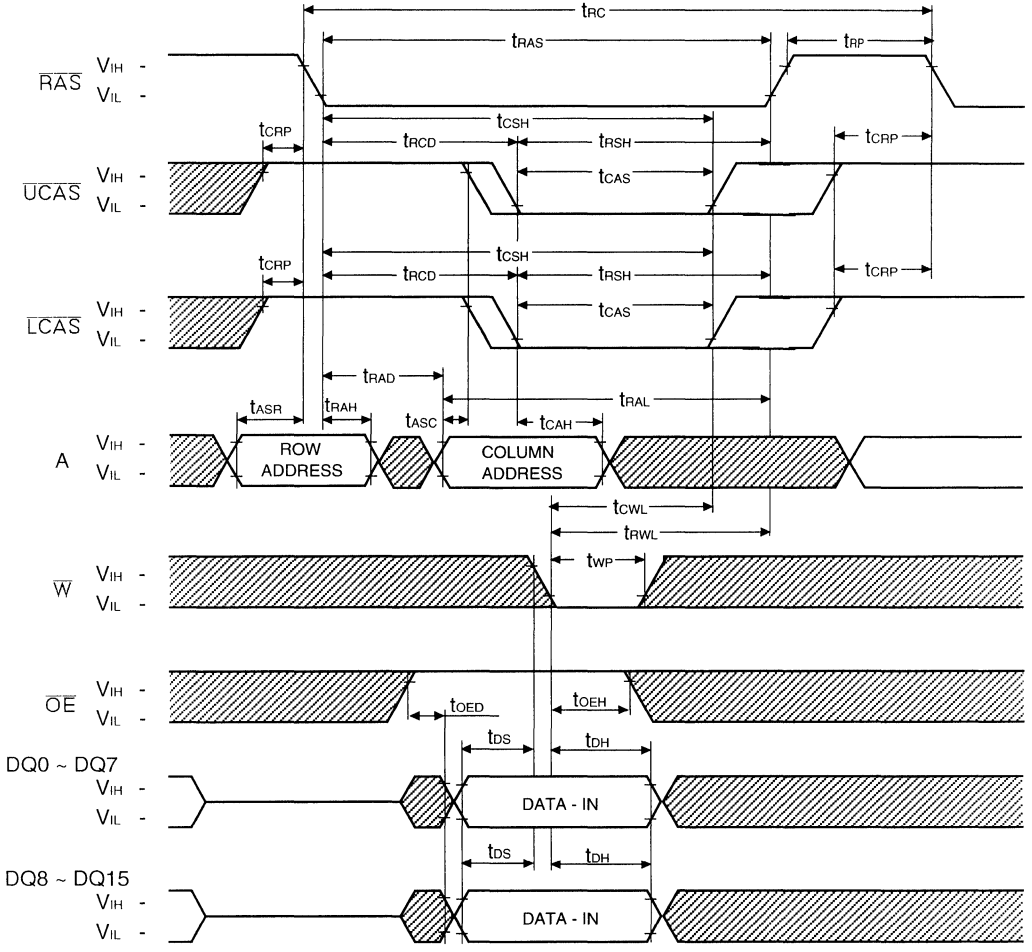
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

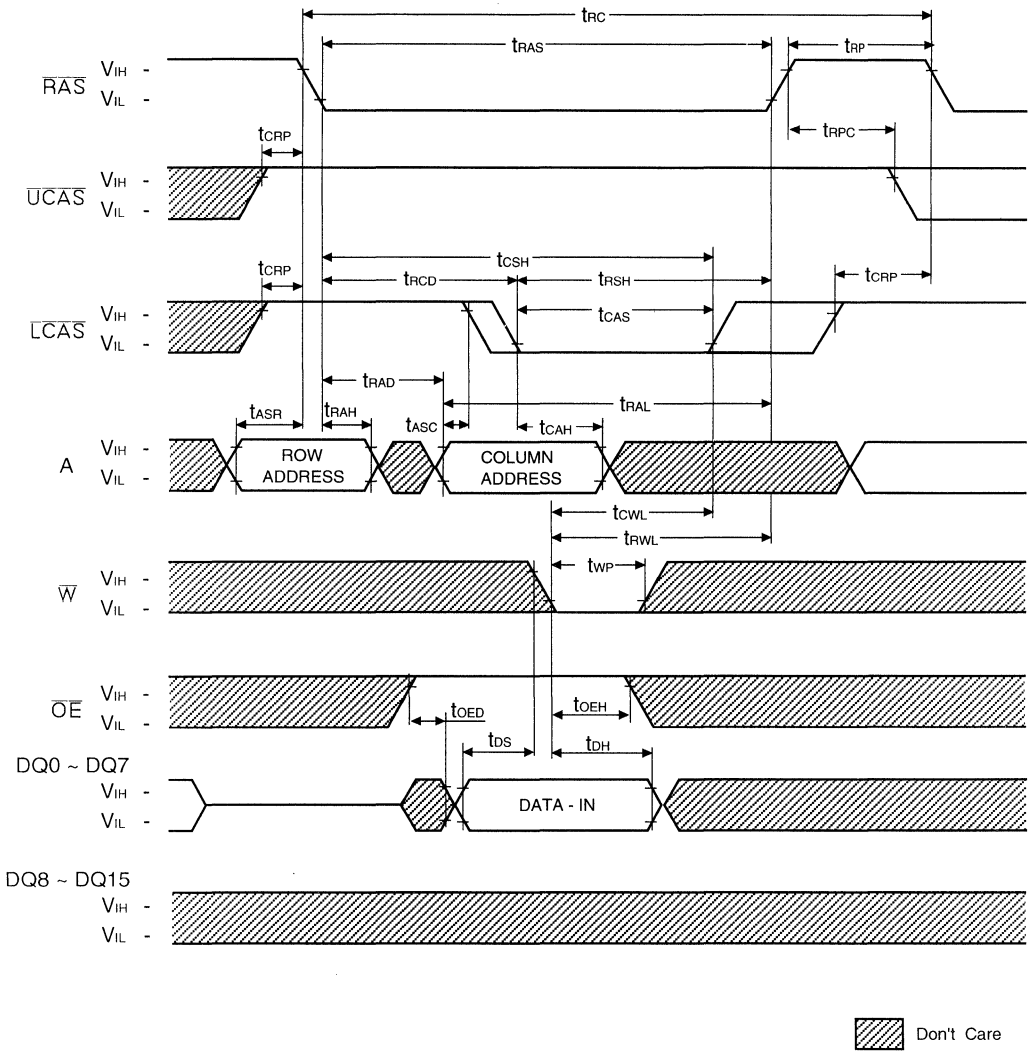
NOTE : D_{OUT} = OPEN



SAMSUNG ELECTRONICS

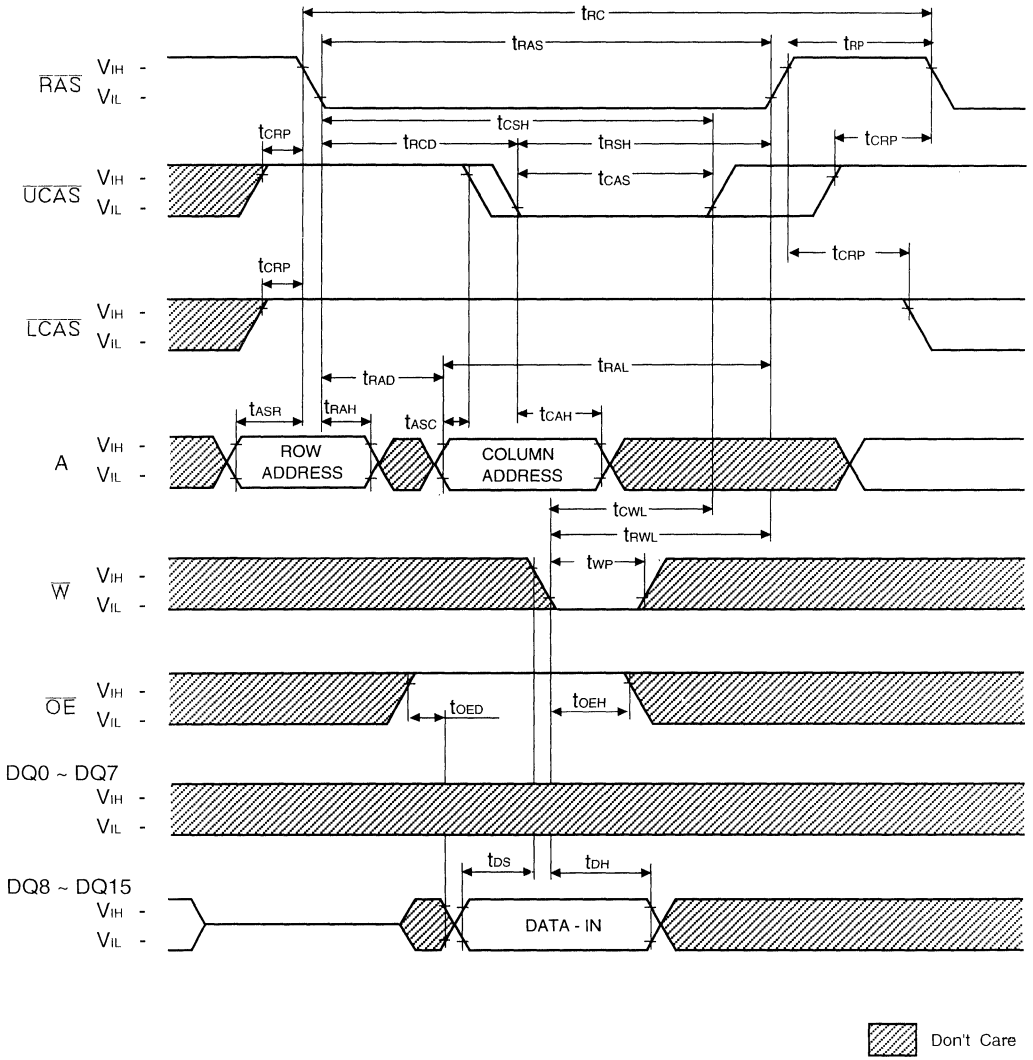
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

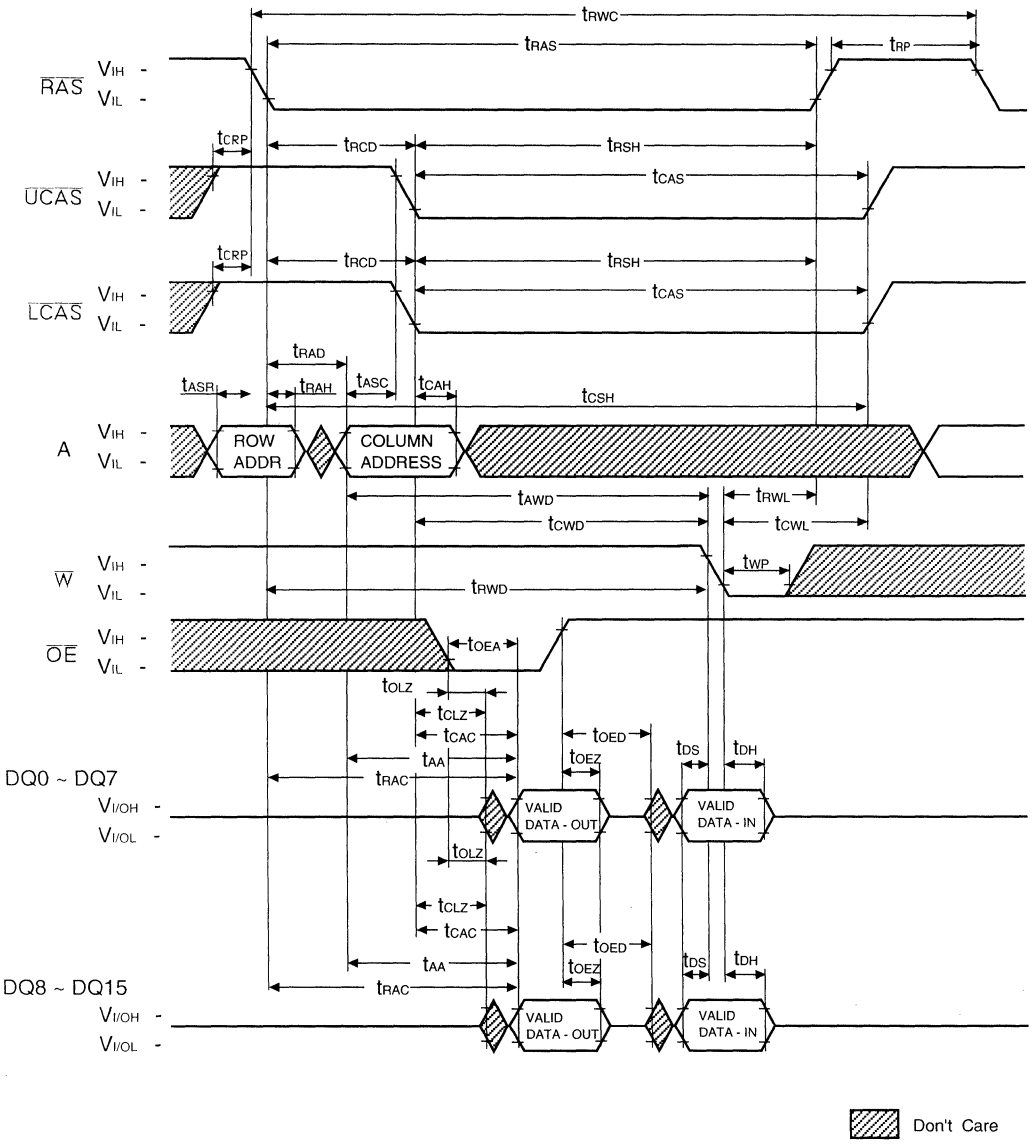


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

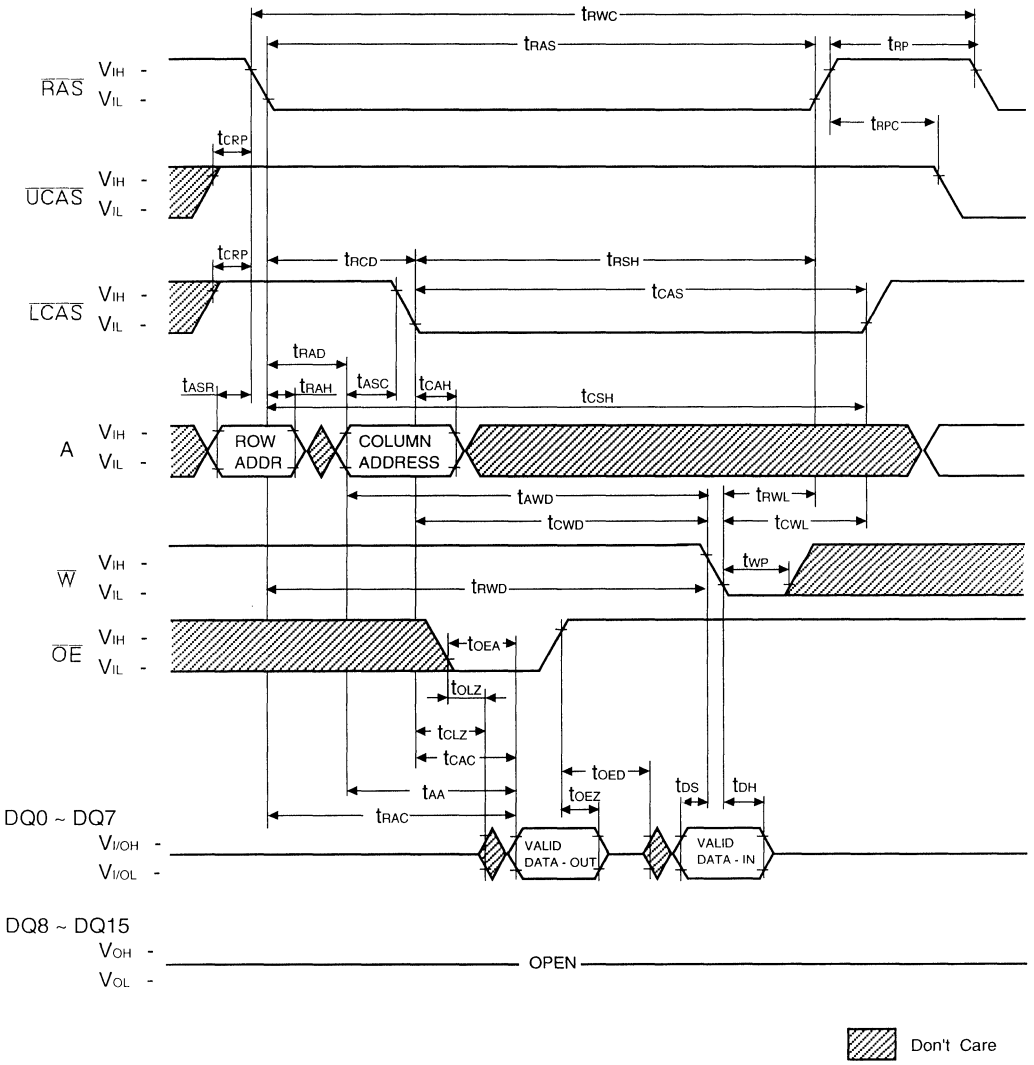
NOTE : D_{OUT} = OPEN



WORD READ - MODIFY - WRITE CYCLE

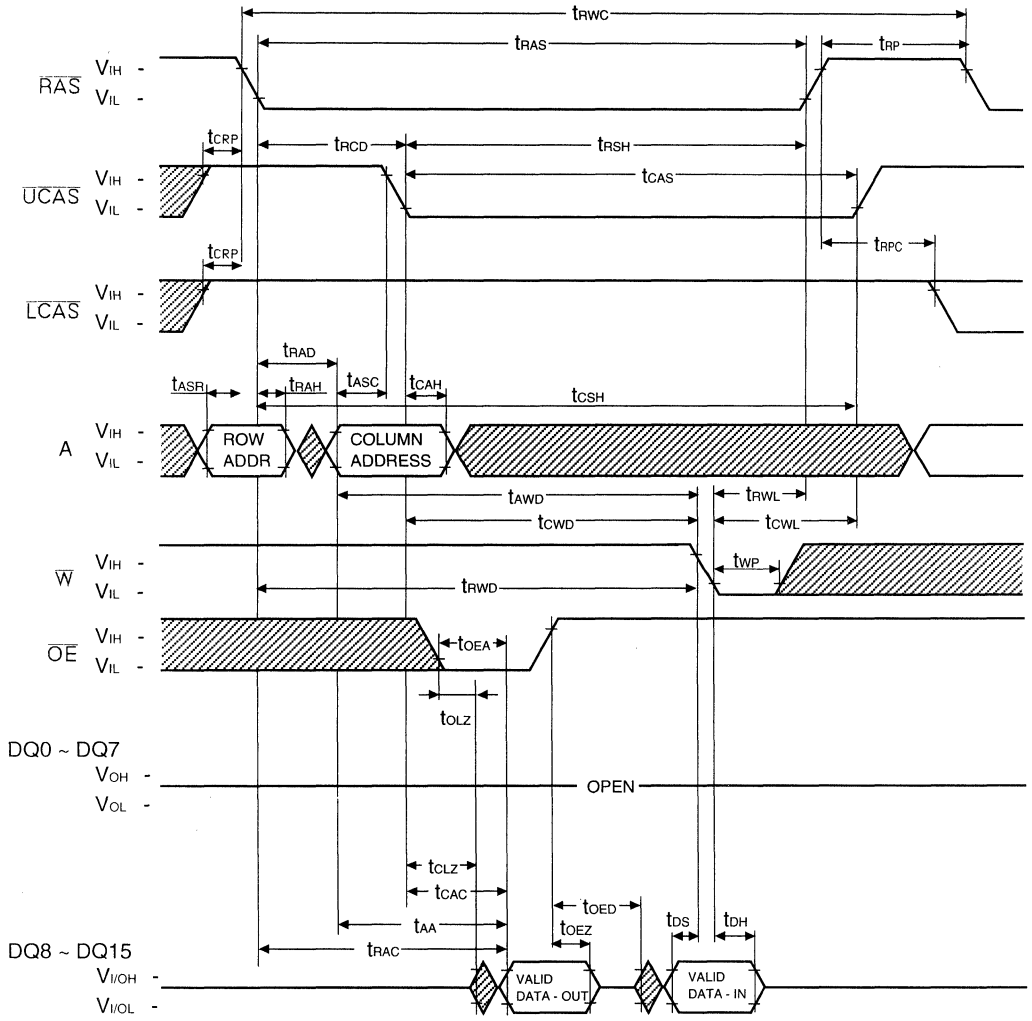


LOWER-BYTE READ - MODIFY - WRITE CYCLE

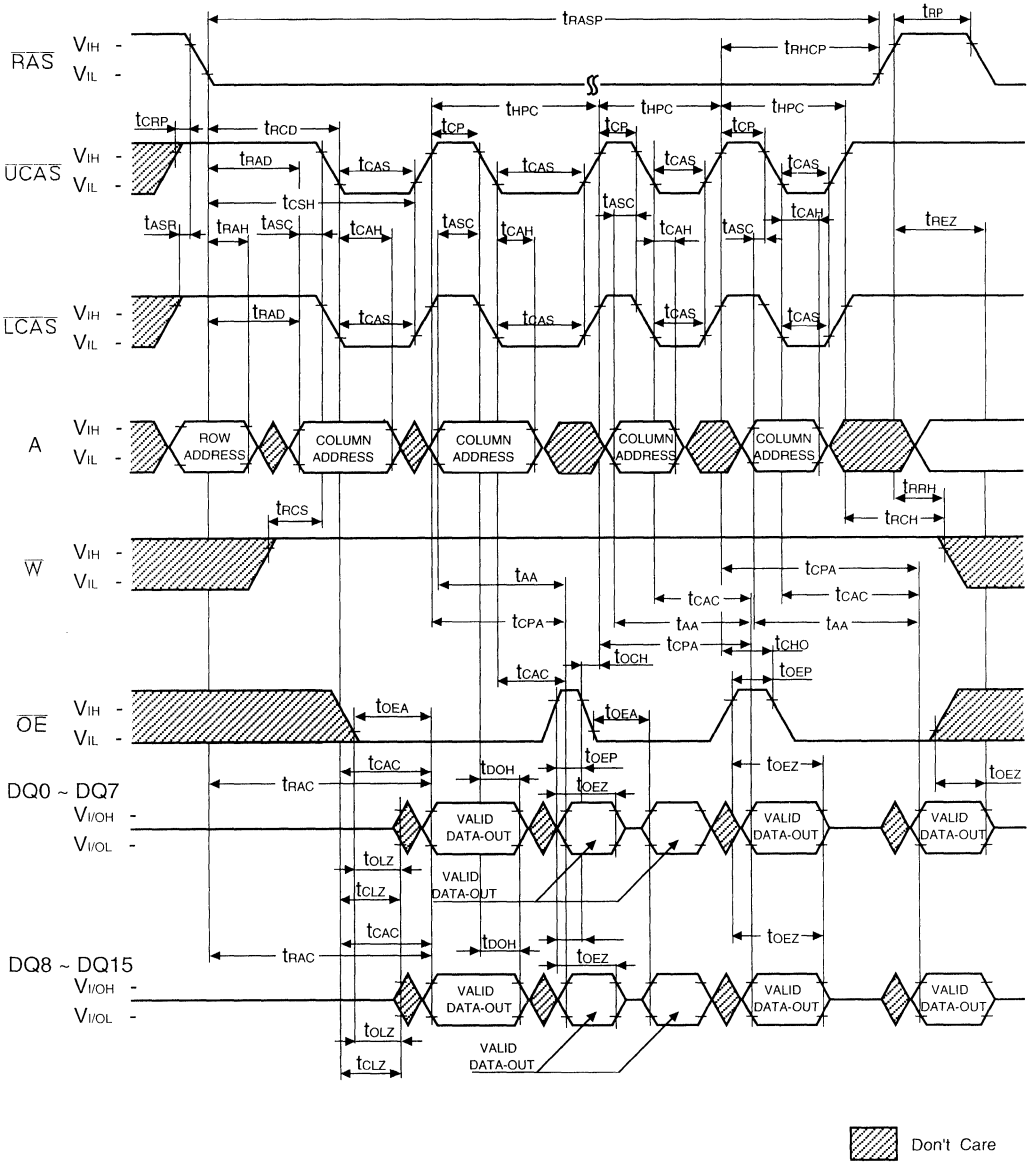


SAMSUNG ELECTRONICS

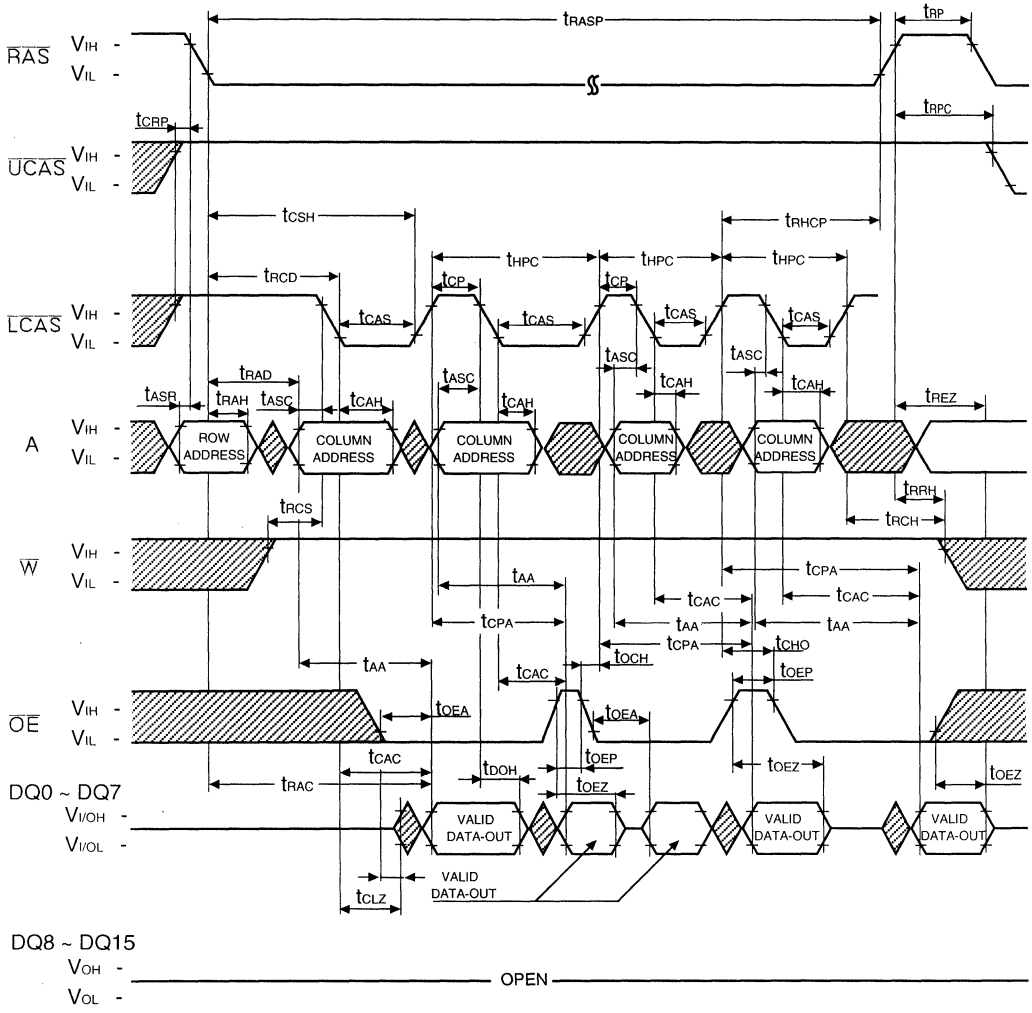
UPPER-BYTE READ - MODIFY - WRITE CYCLE



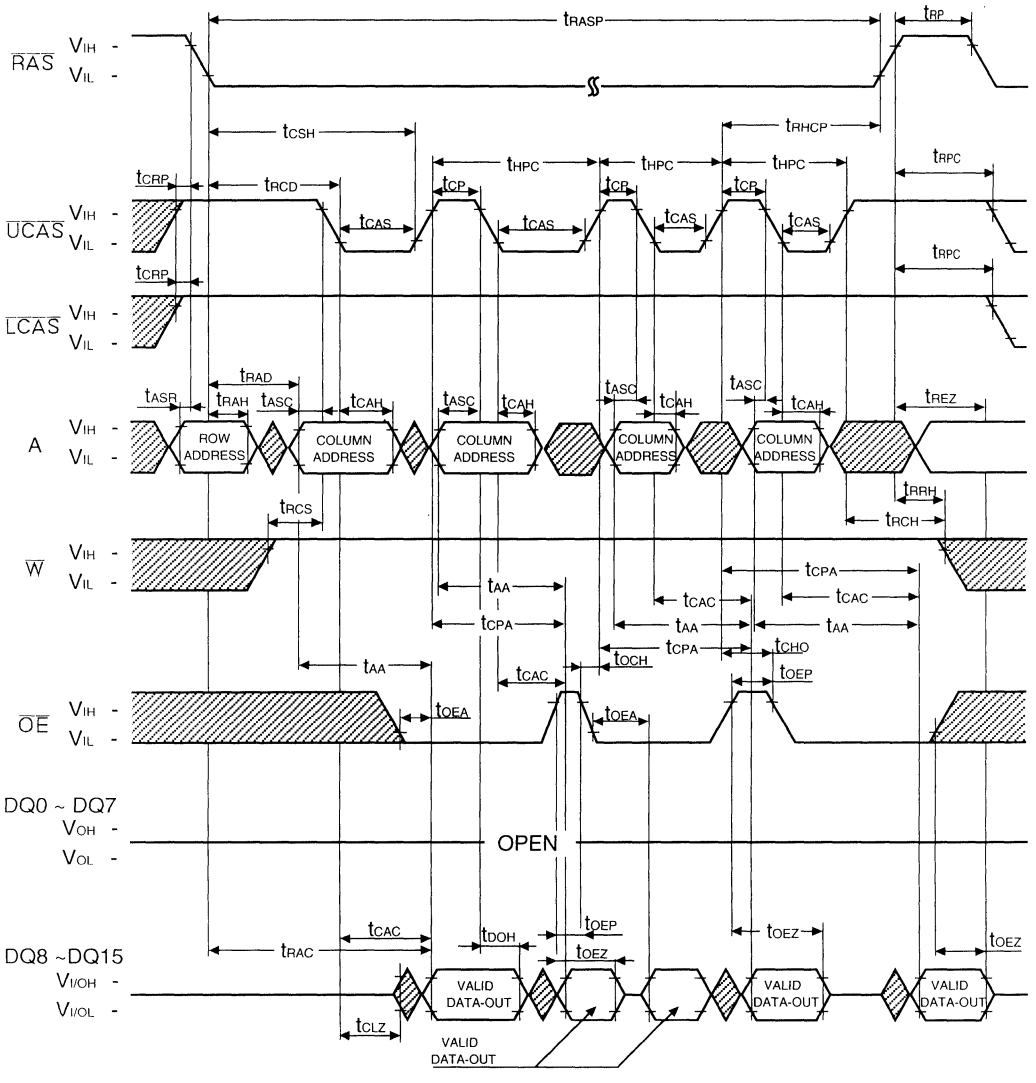
HYPER PAGE MODE WORD READ CYCLE



HYPER PAGE MODE LOWER BYTE READ CYCLE

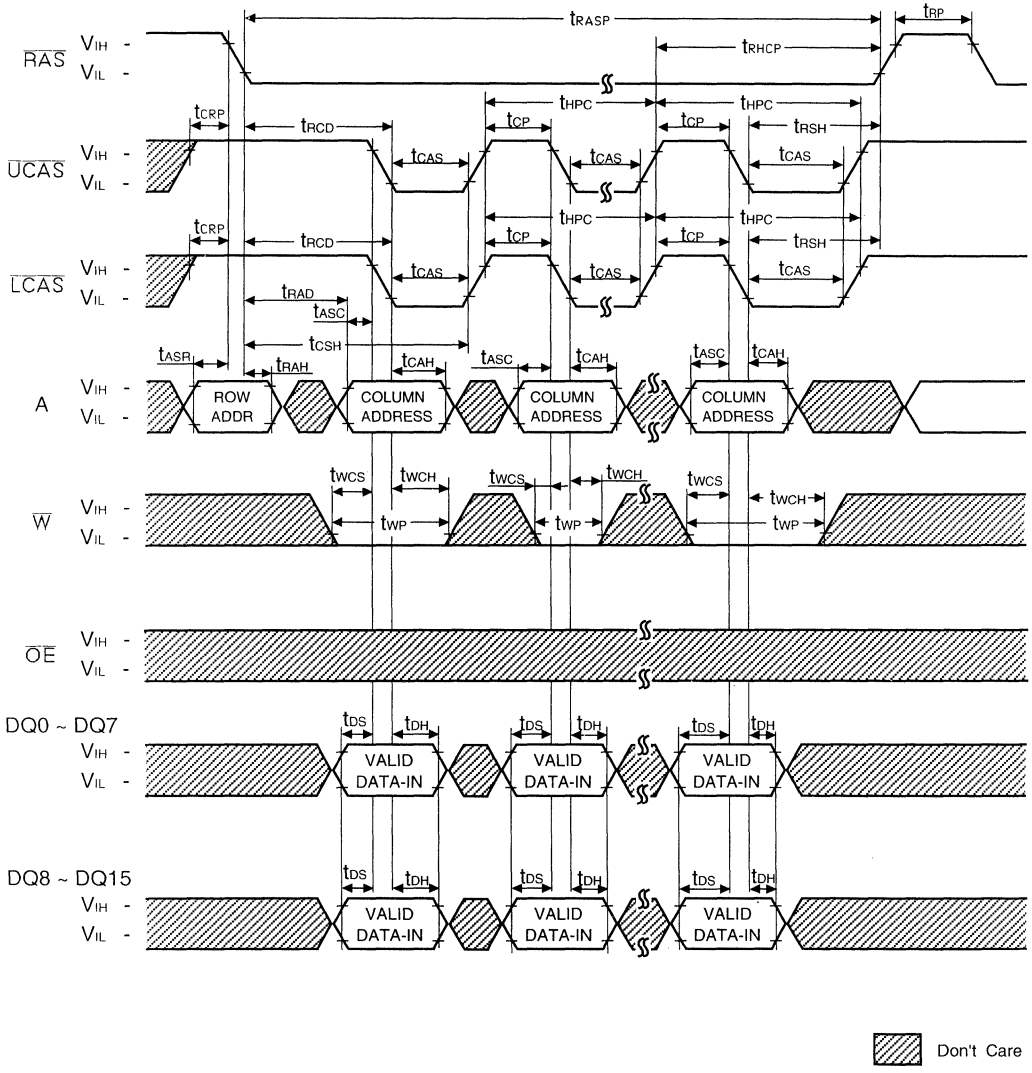


HYPER PAGE MODE UPPER BYTE READ CYCLE



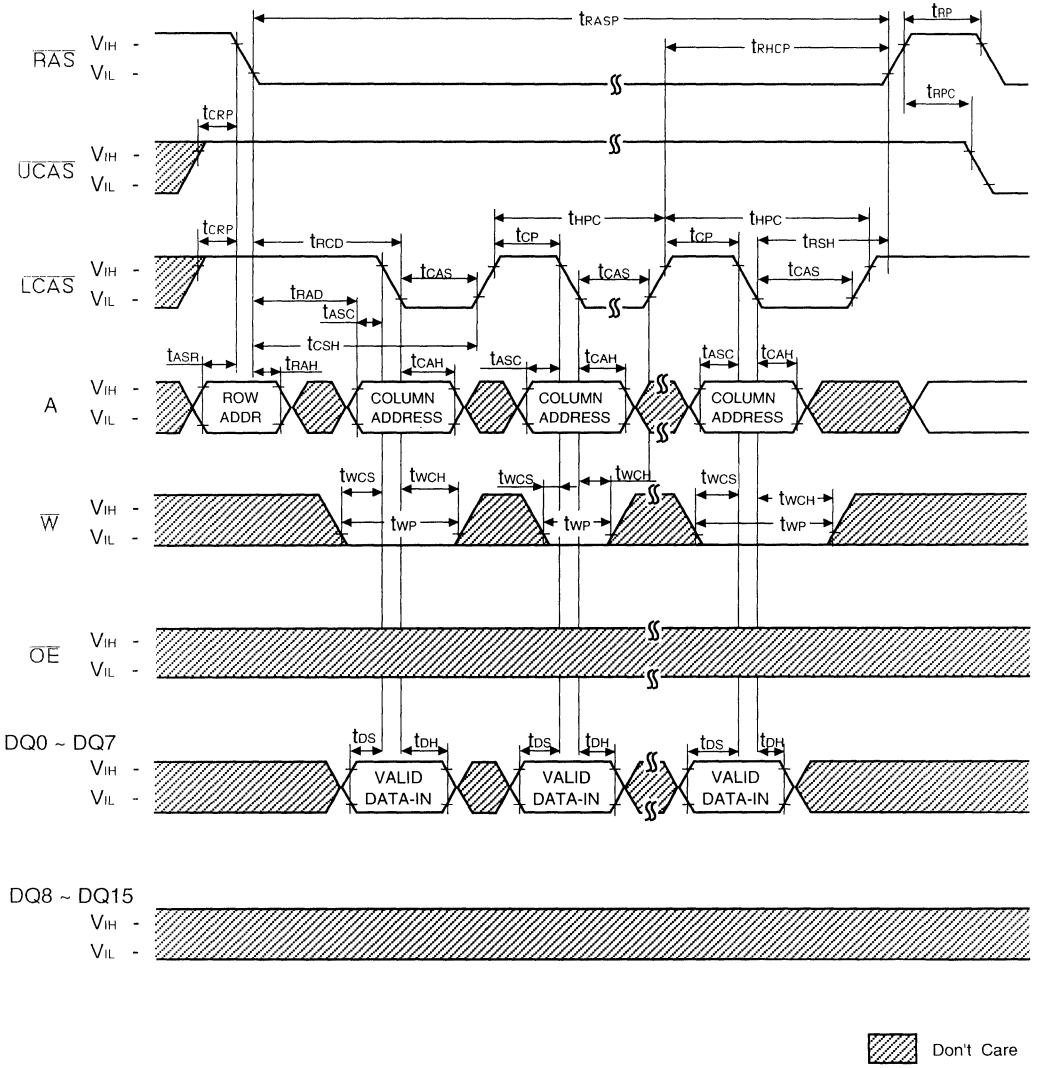
HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

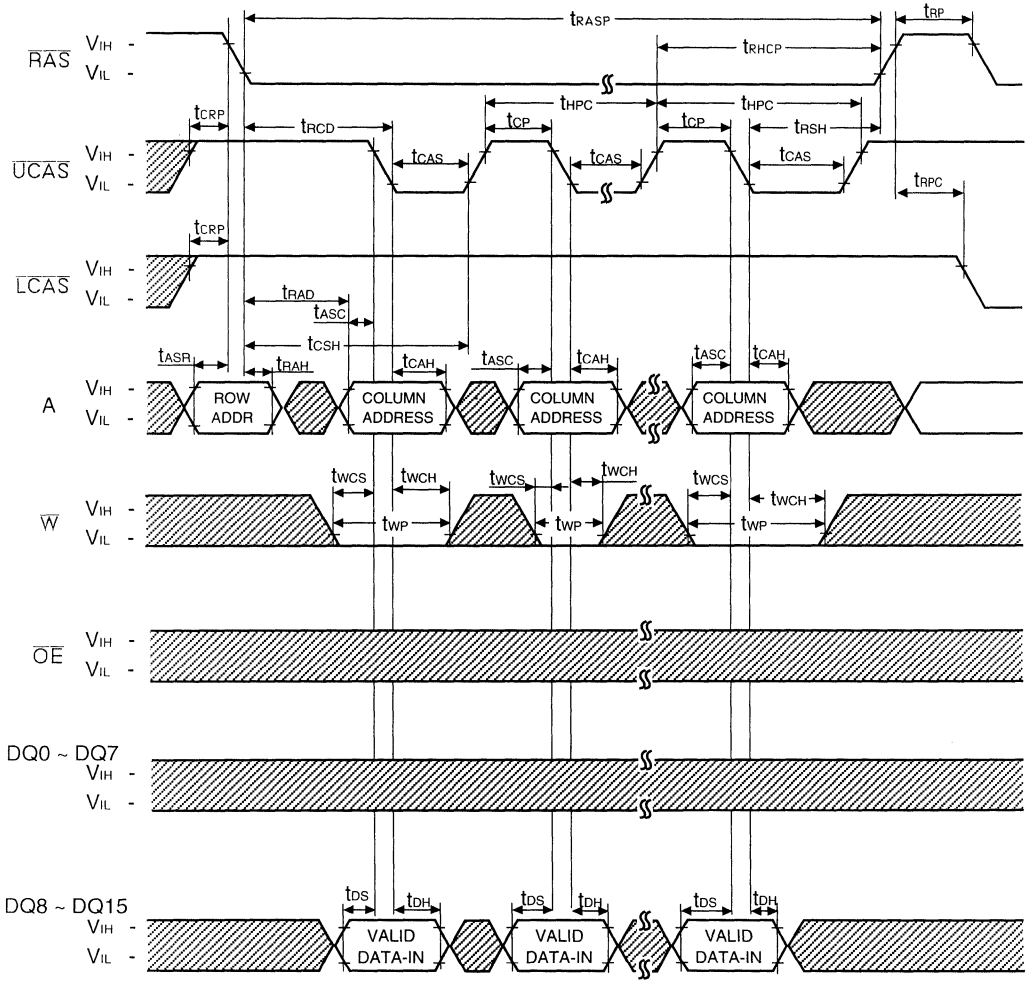
NOTE : D_{OUT} = Open



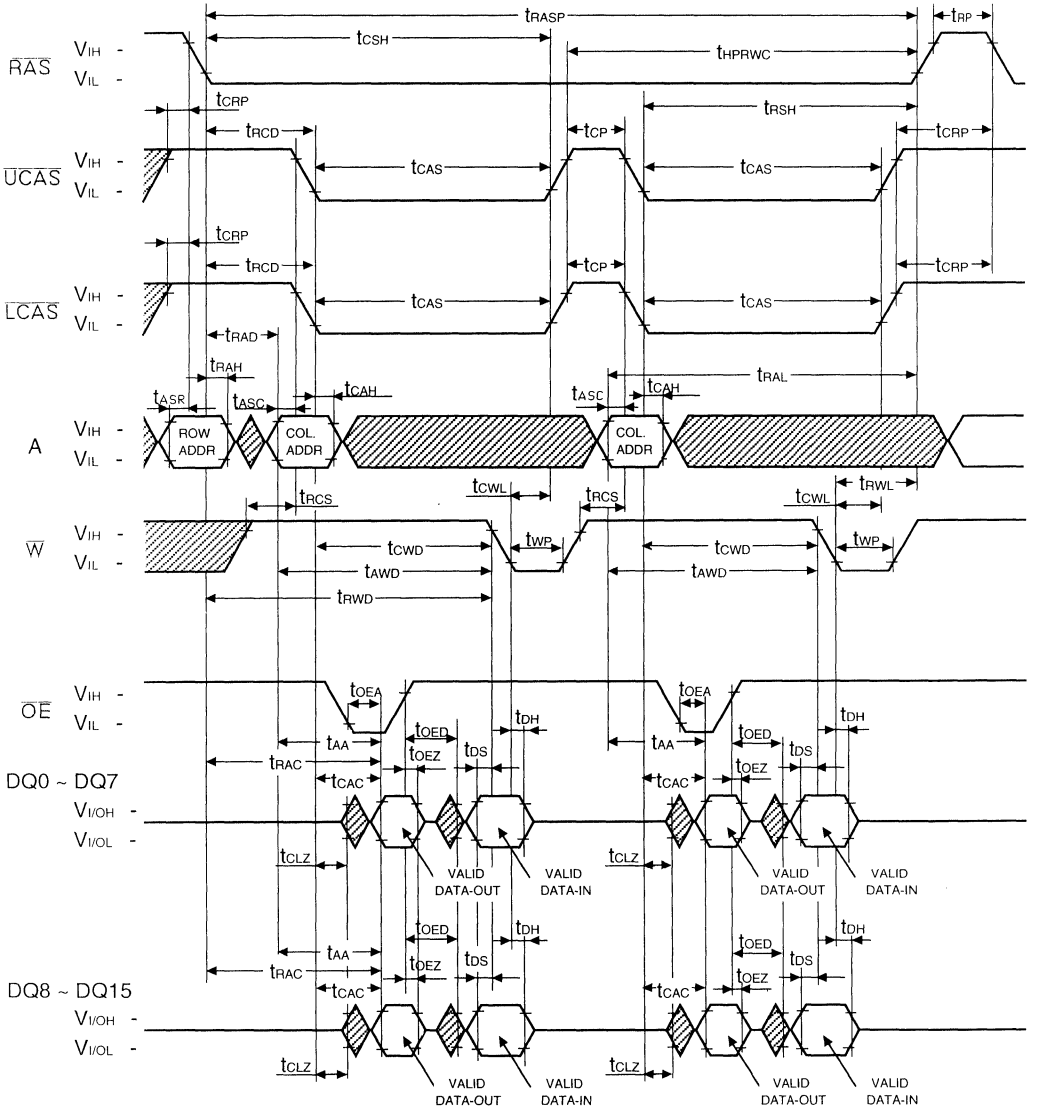
SAMSUNG ELECTRONICS

HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

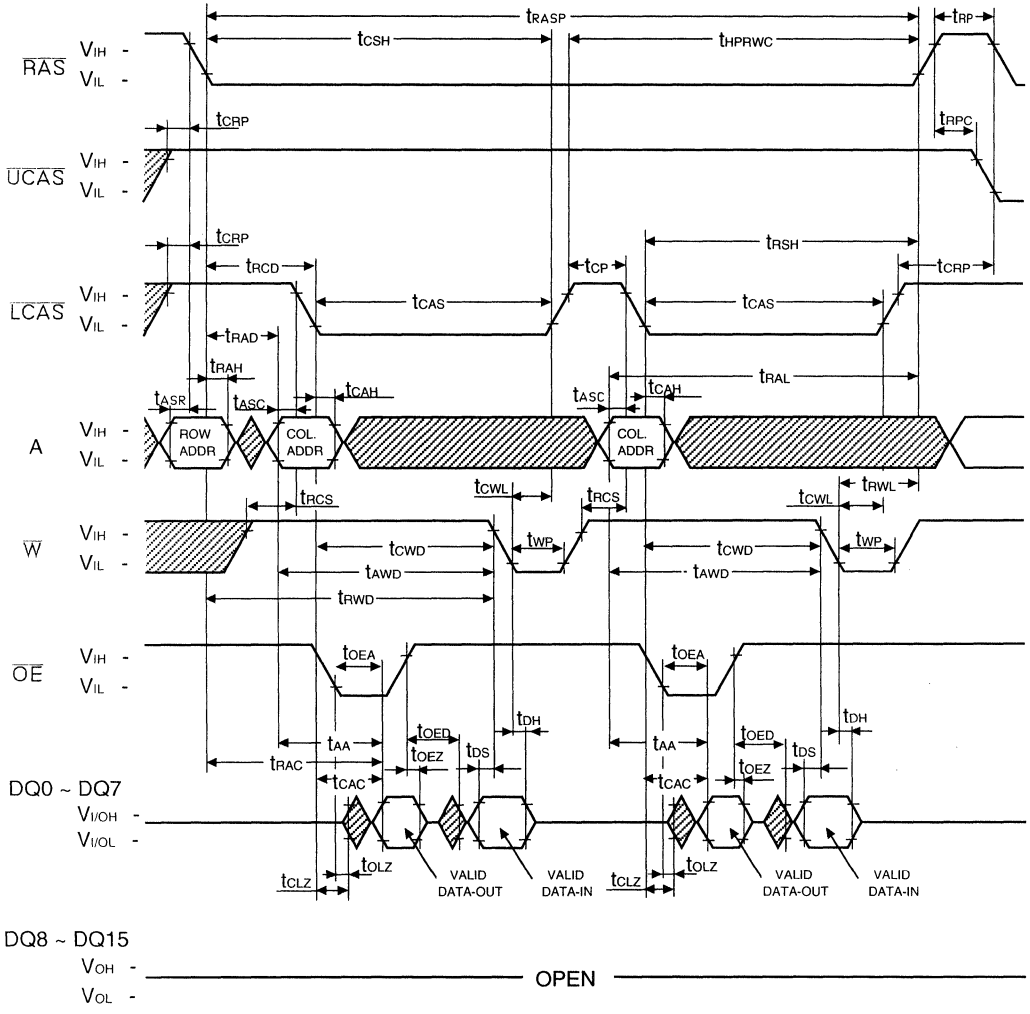
NOTE : D_{OUT} = Open



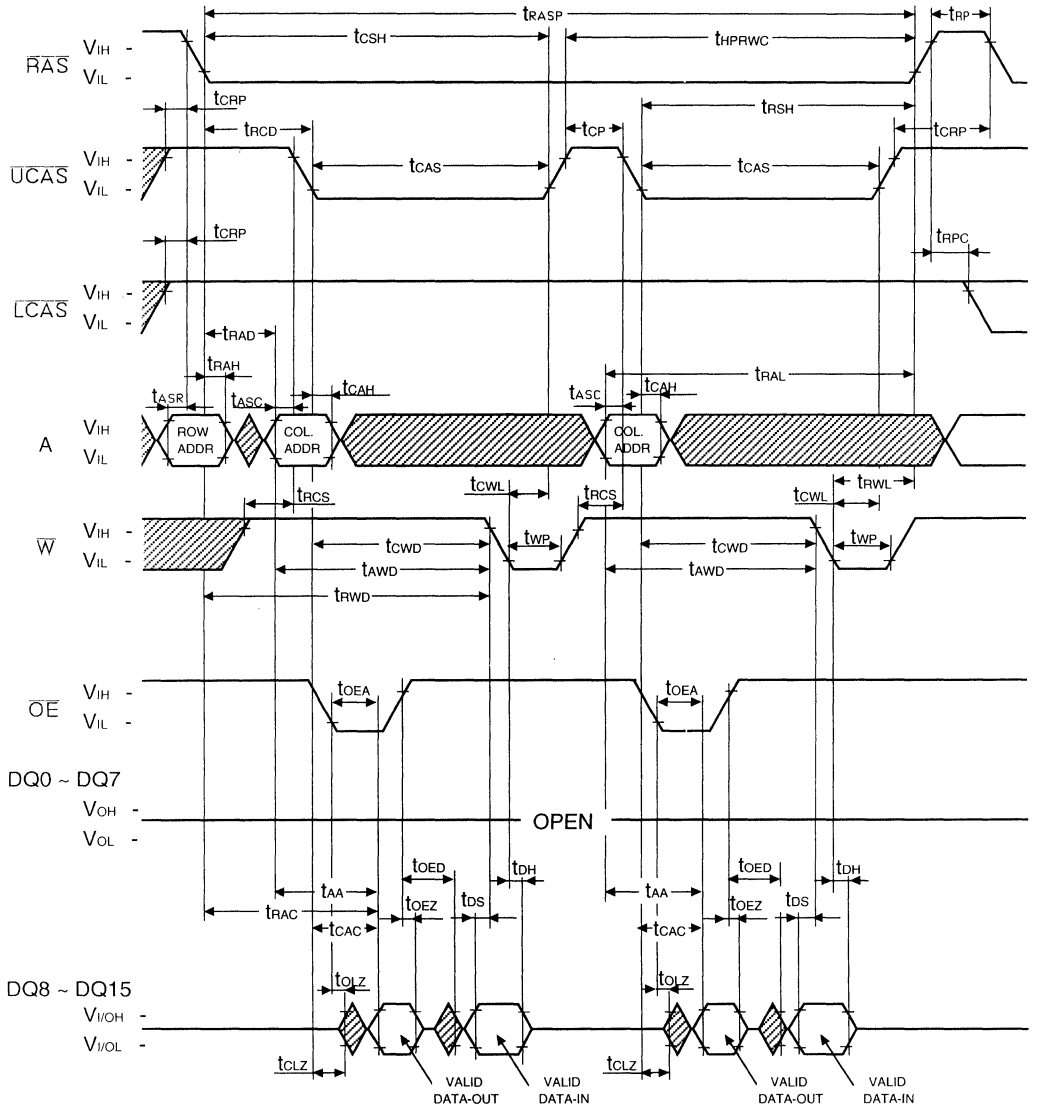
HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE



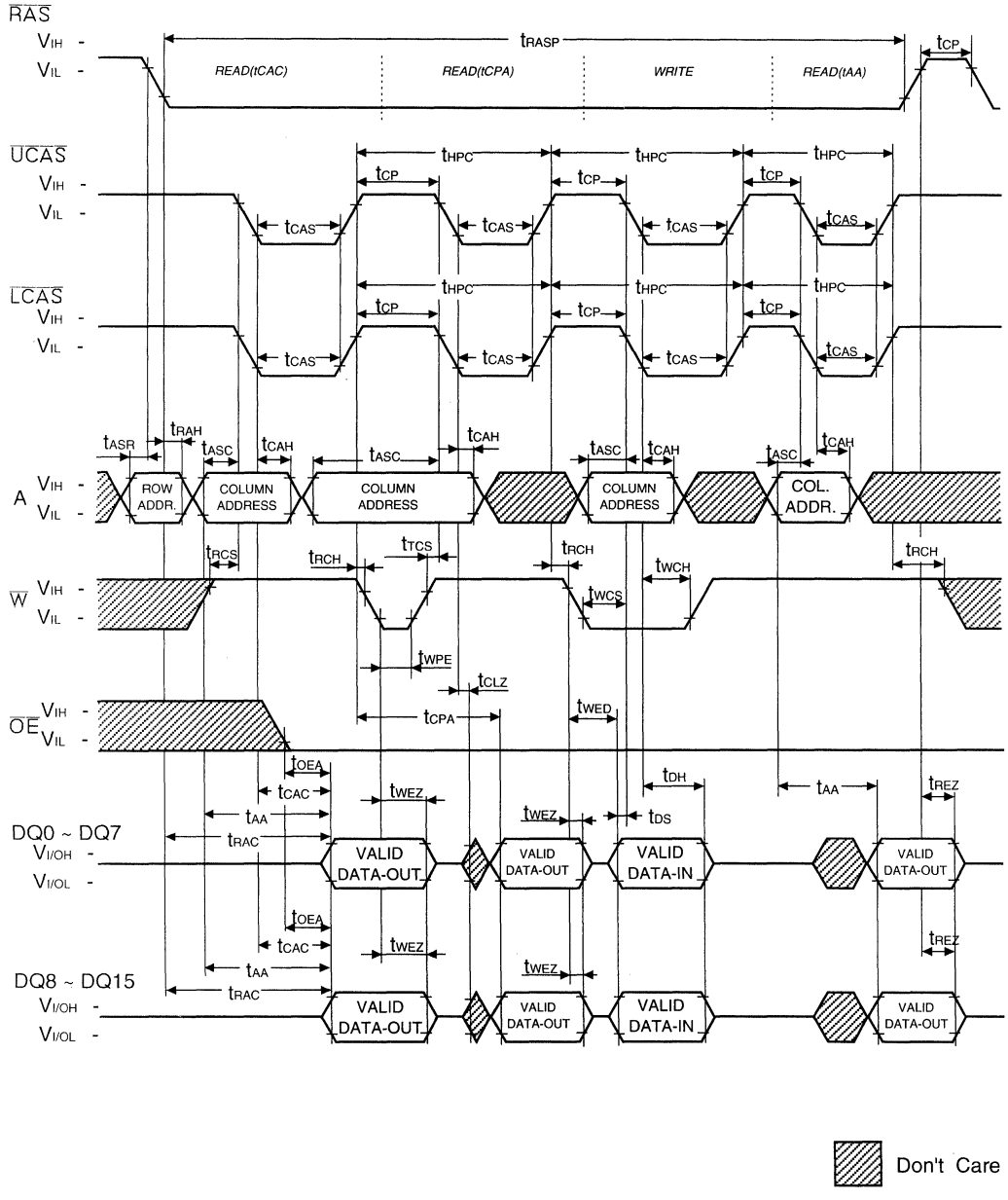
HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE

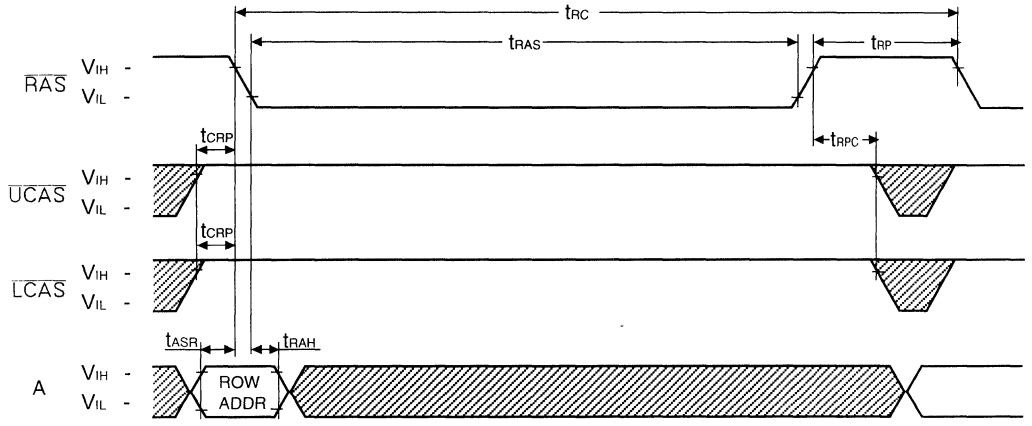


HYPER PAGE READ AND WRITE MIXED CYCLE



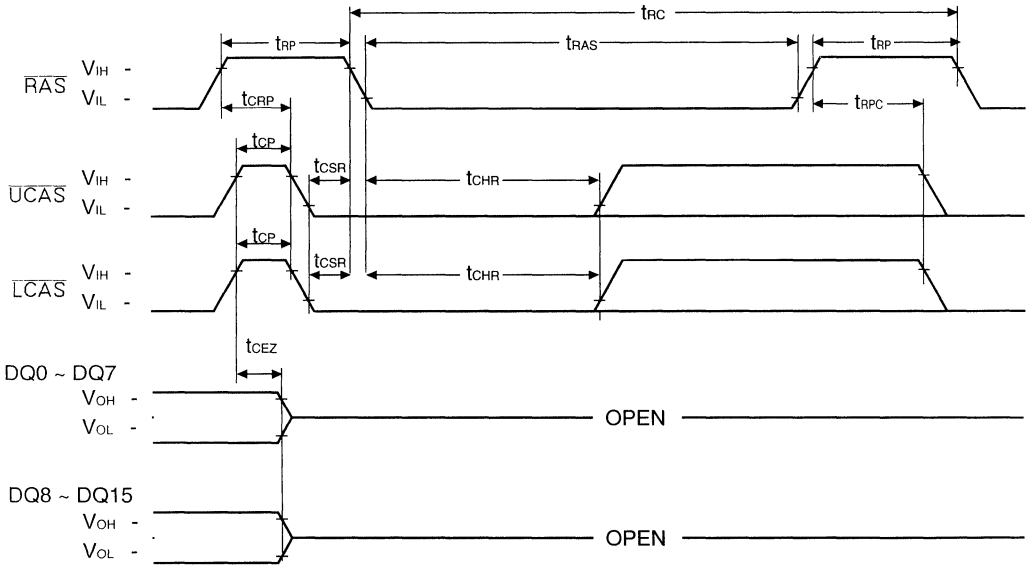
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

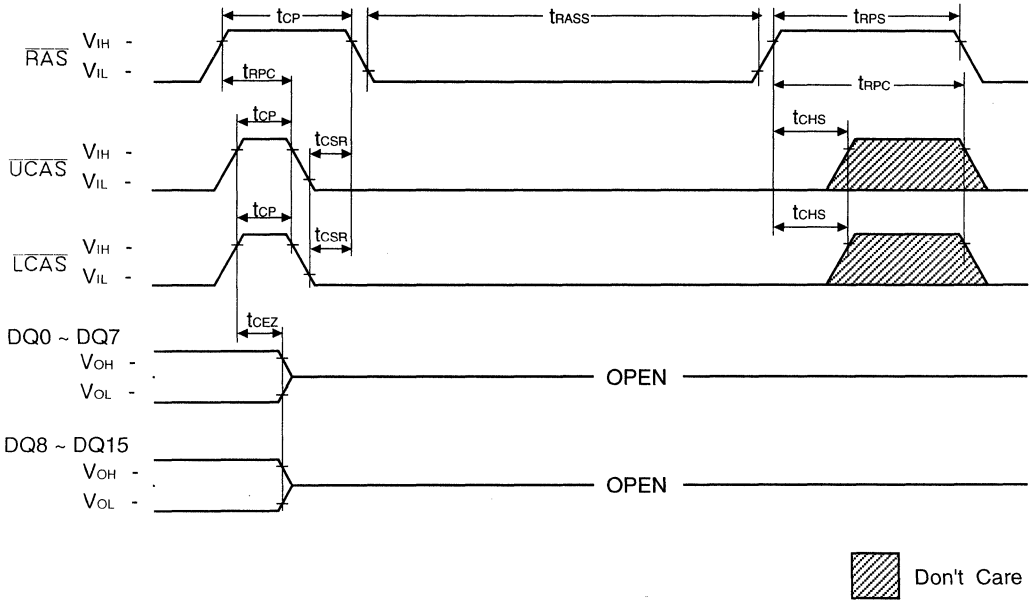


Don't Care

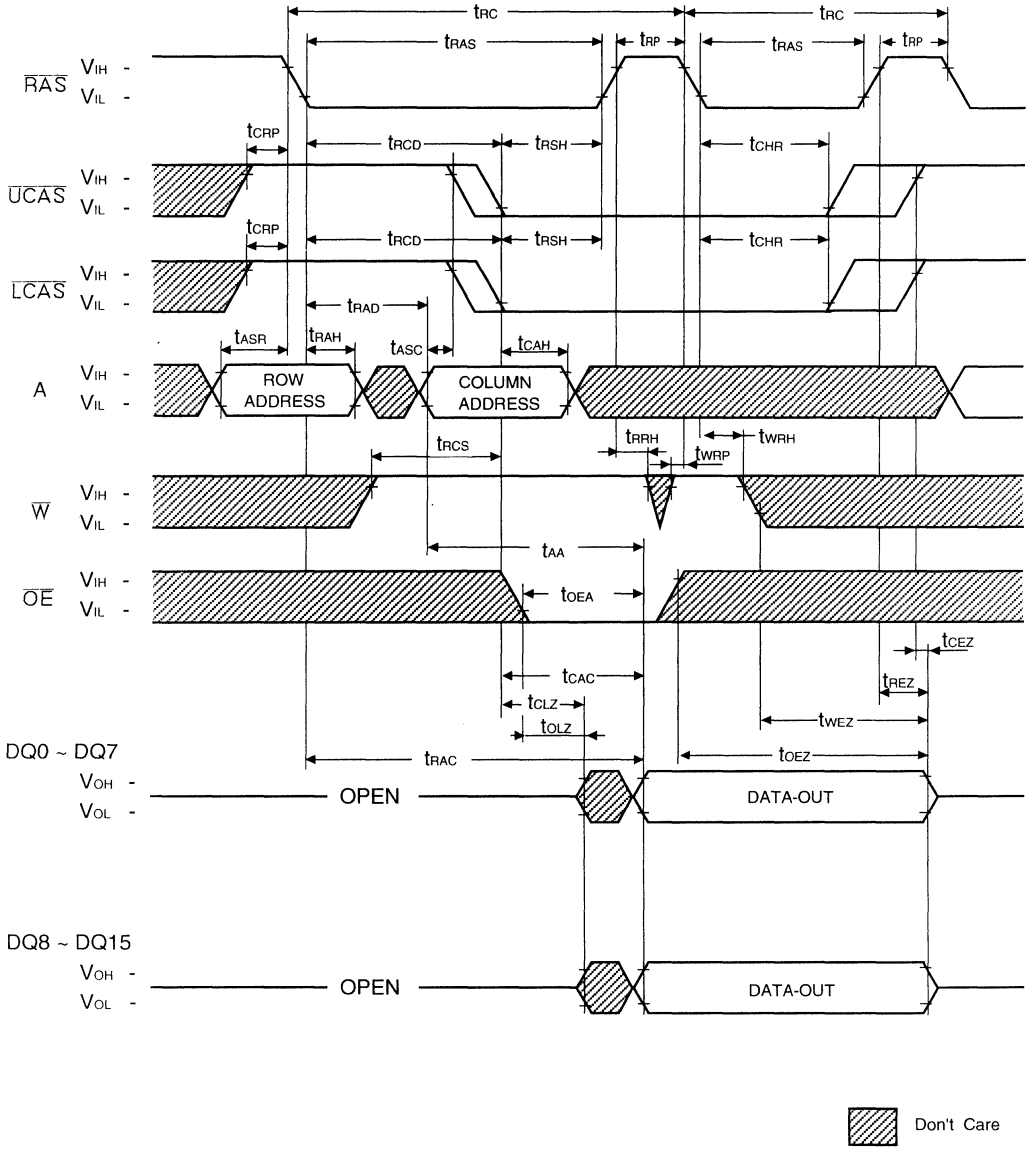
SAMSUNG ELECTRONICS

$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

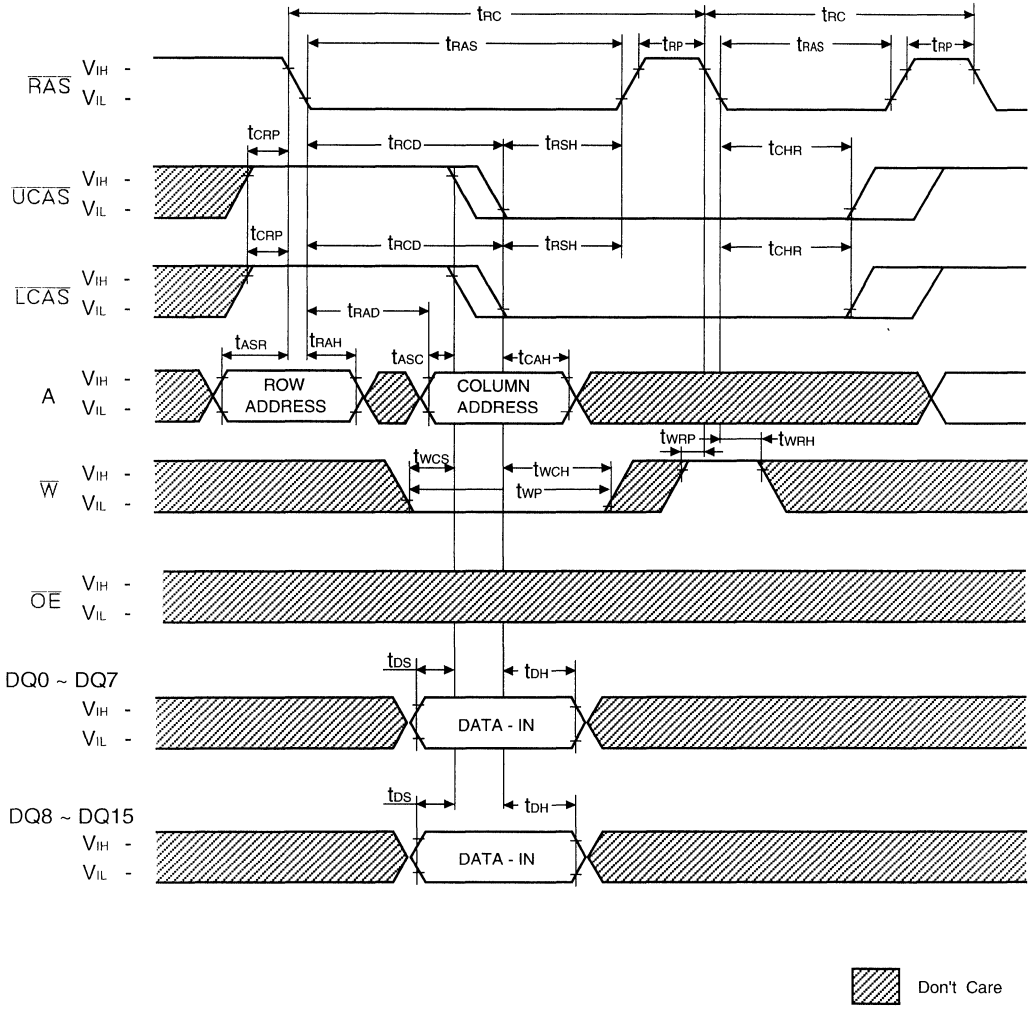


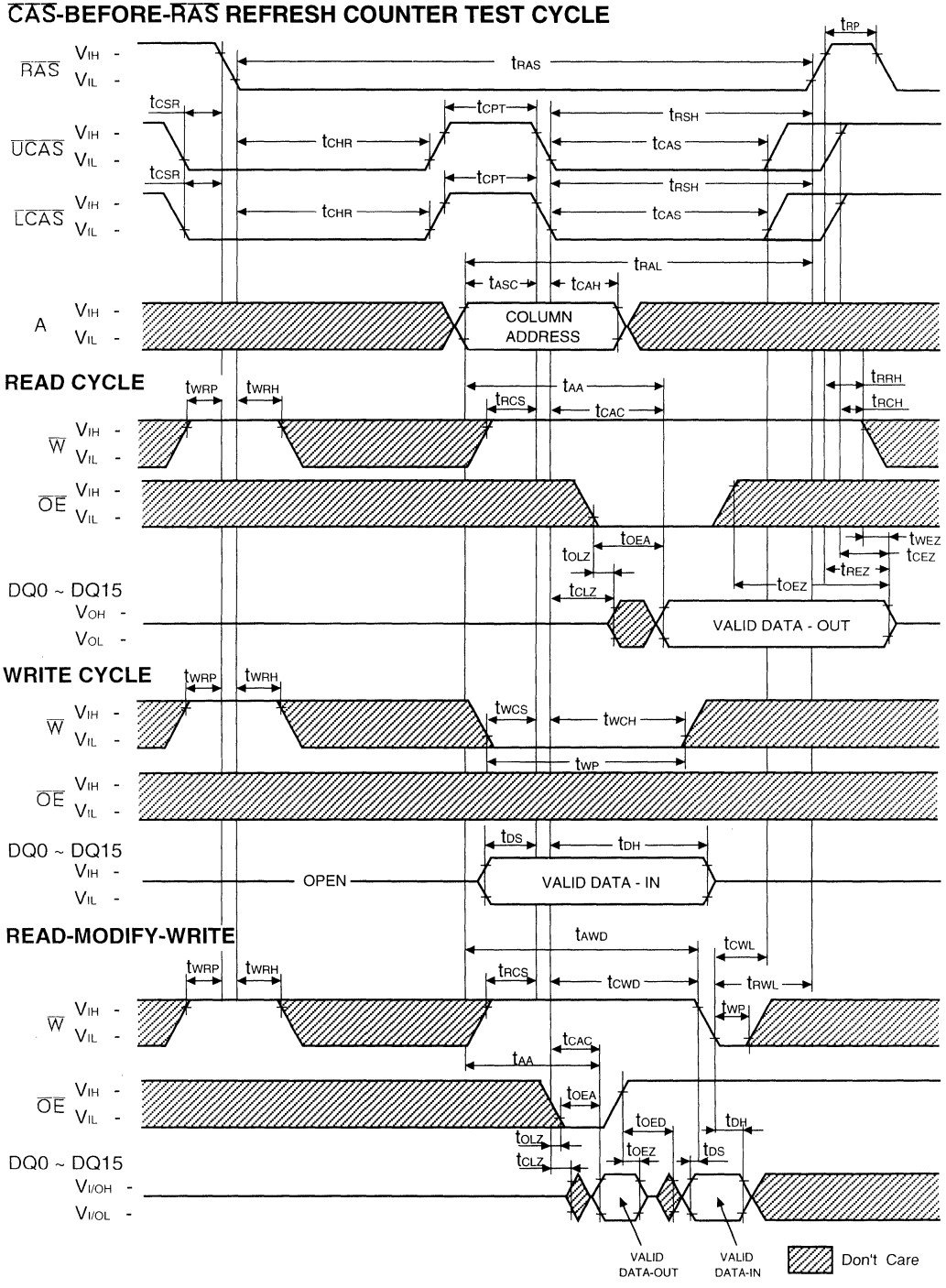
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



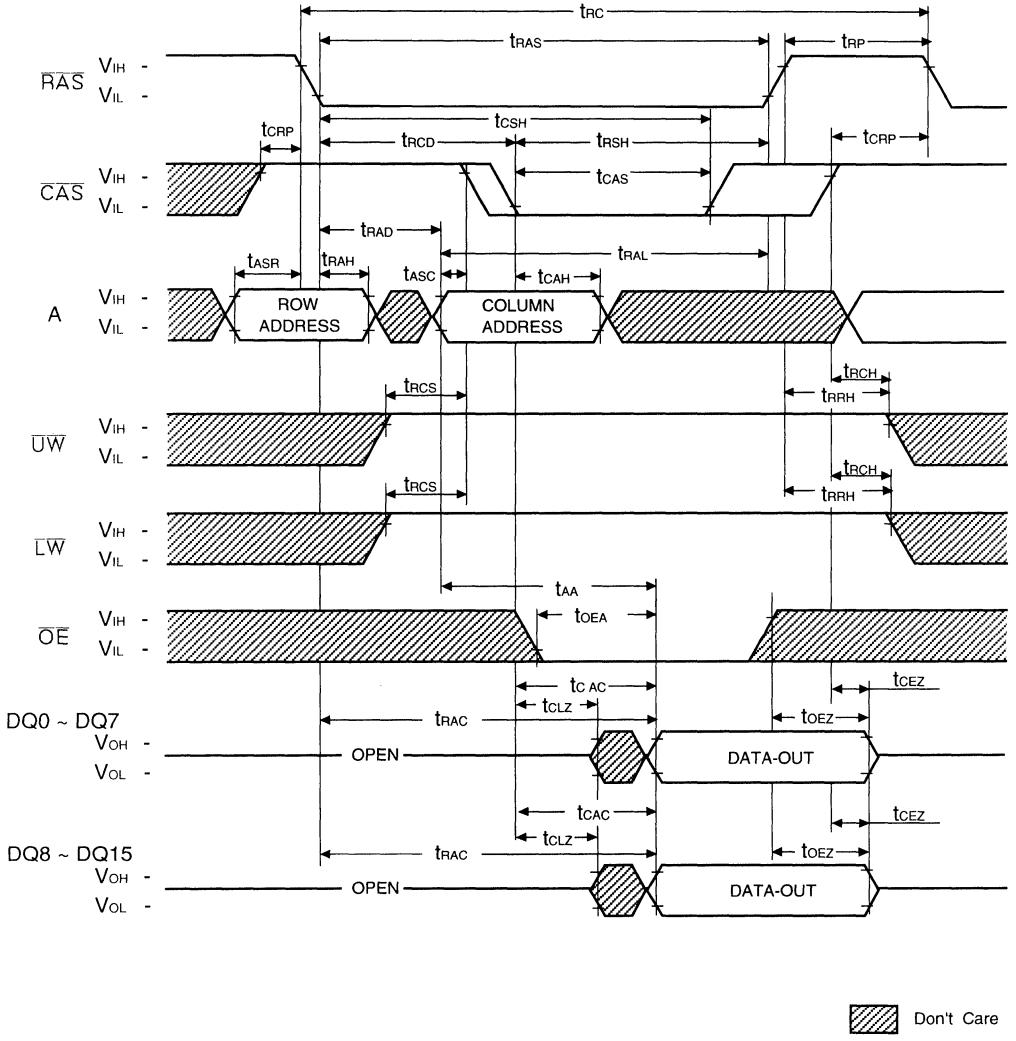

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE
RAS
UCAS
LCAS
A
VIH
VIL
tRP
tRAS
tCSR
tCPT
tRSH
tCHR
tCAS
tRAL
tASC
tCAH
COLUMN ADDRESS
READ CYCLE
tWRP
tWRH
tAA
tRCS
tCAC
tRRH
tRCH
W
OE
tOEA
tWEZ
tCEZ
tOLZ
tREZ
tCLZ
tOEZ
DQ0 ~ DQ15
VOH
VOL
VALID DATA - OUT
WRITE CYCLE
tWCS
tWCH
tWP
tDS
tDH
OPEN
VALID DATA - IN
READ-MODIFY-WRITE
tAWD
tCWL
tCWD
tRWL
VI/OH
VI/OL
VALID DATA-OUT
VALID DATA-IN
Don't Care

EDO Mode, x16(2$\overline{WE}$) Device

TIMING DIAGRAM

READ CYCLE

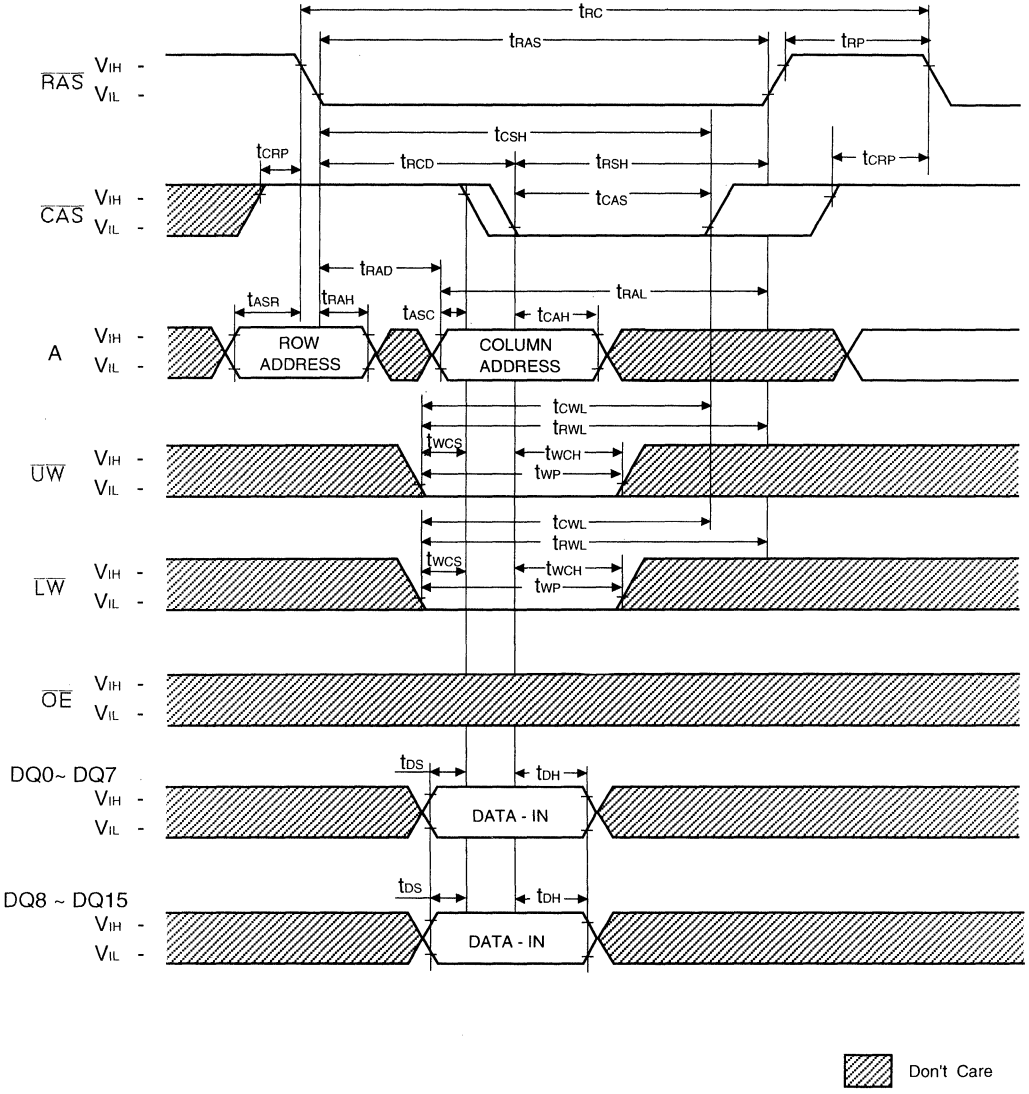
NOTE : D_{IN} = OPEN



SAMSUNG ELECTRONICS

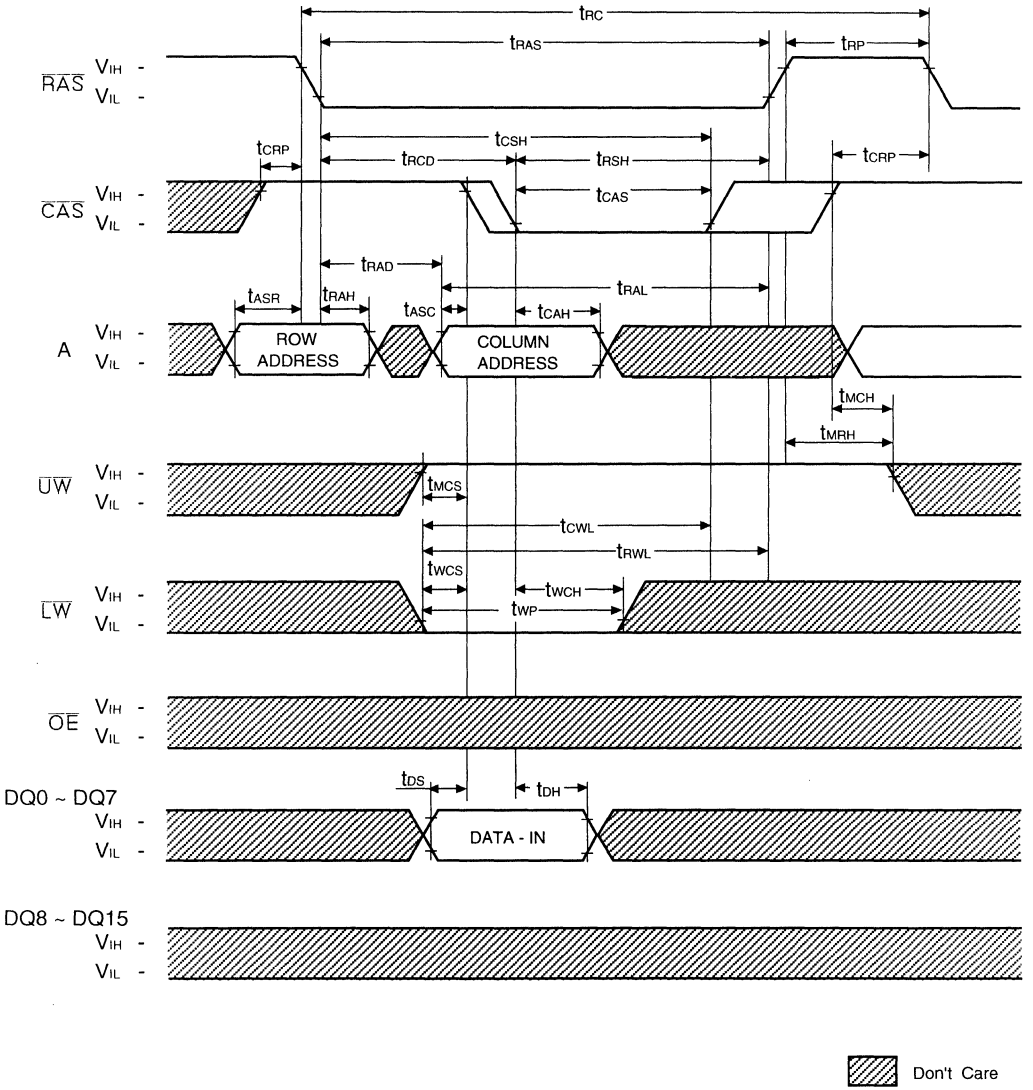
WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



LOWER BYTE WRITE CYCLE (EARLY WRITE)

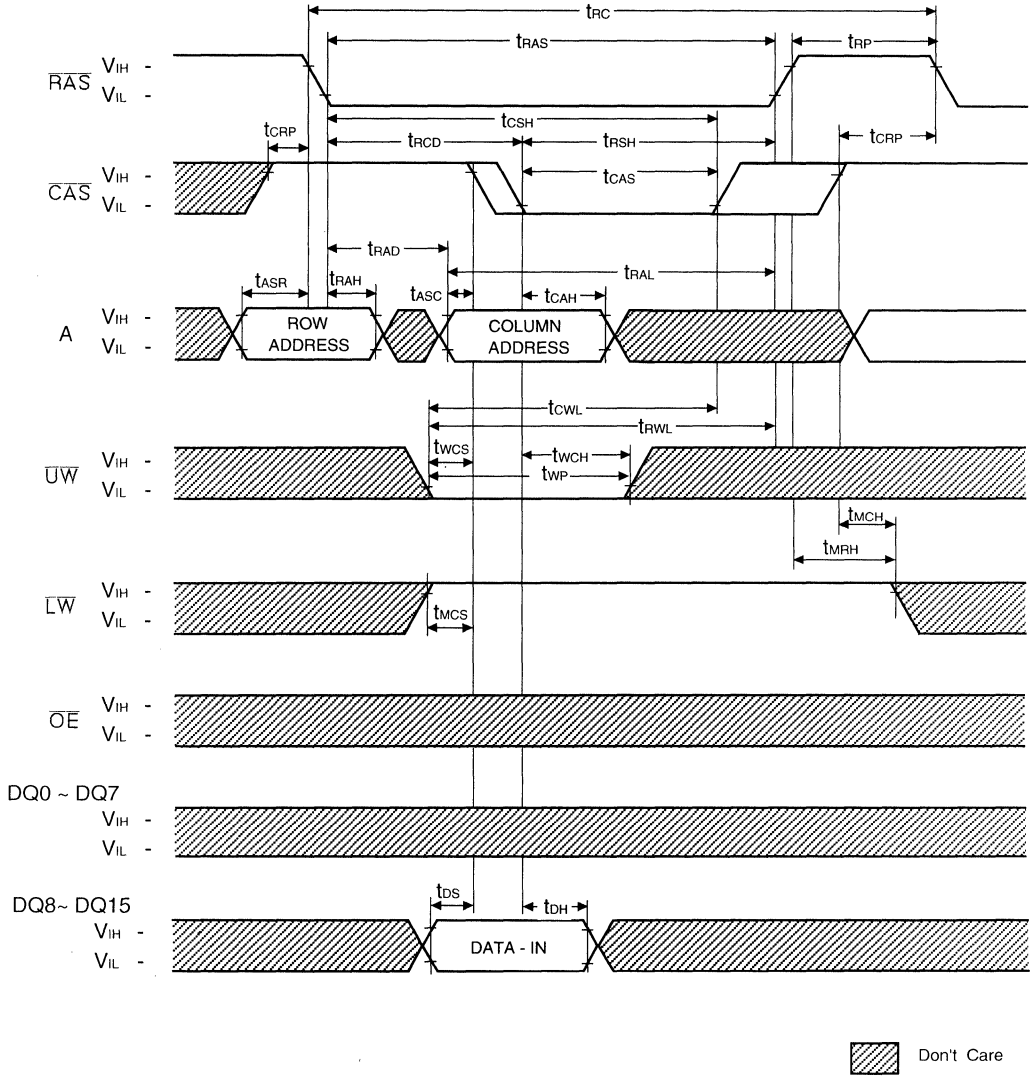
NOTE : D_{OUT} = OPEN



Don't Care

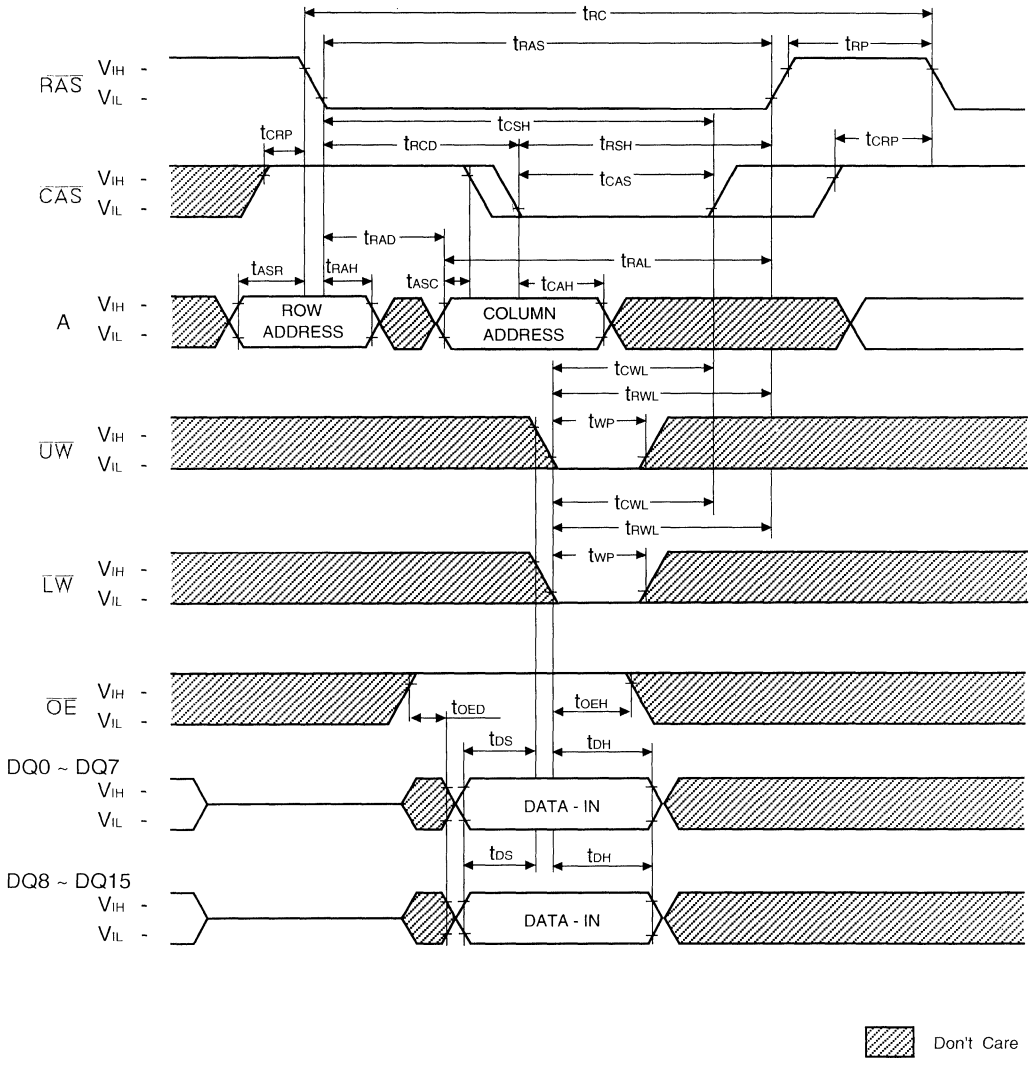
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



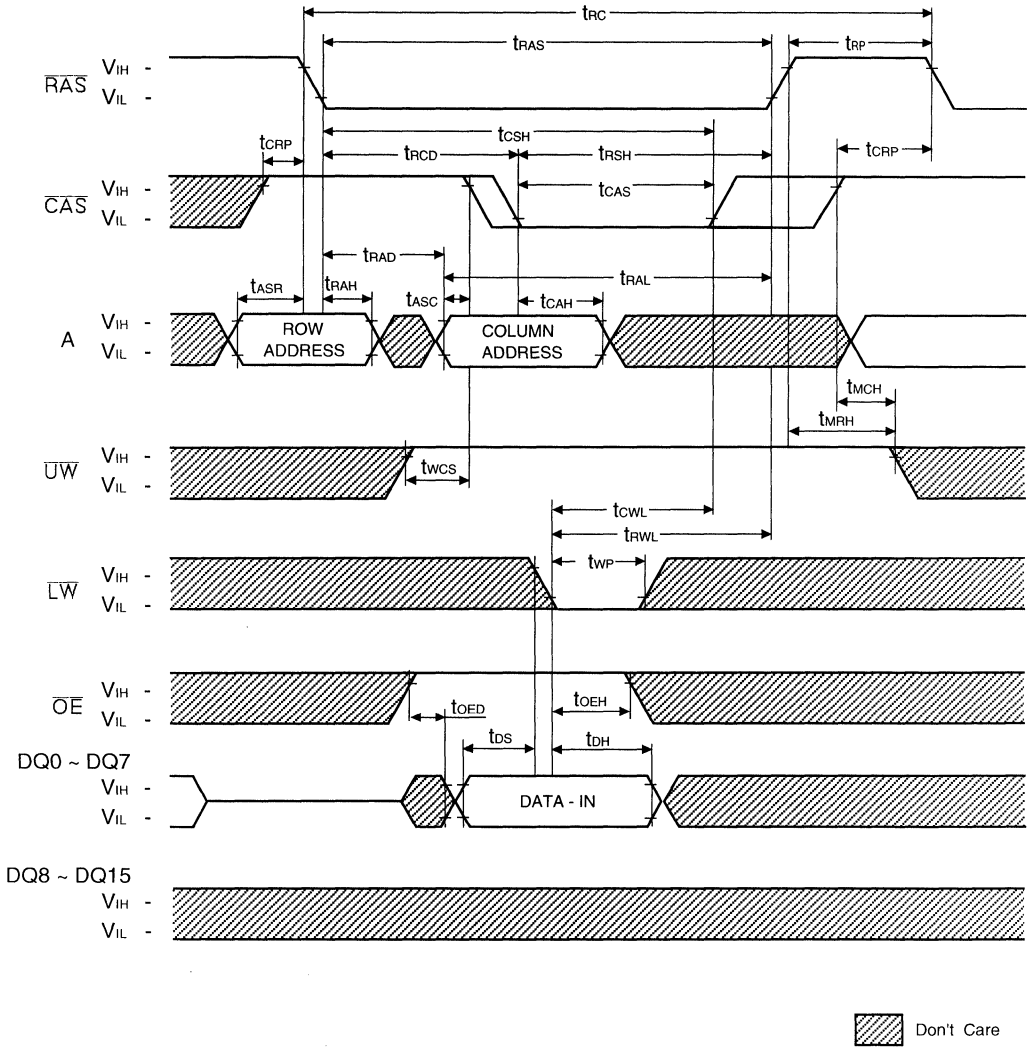
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



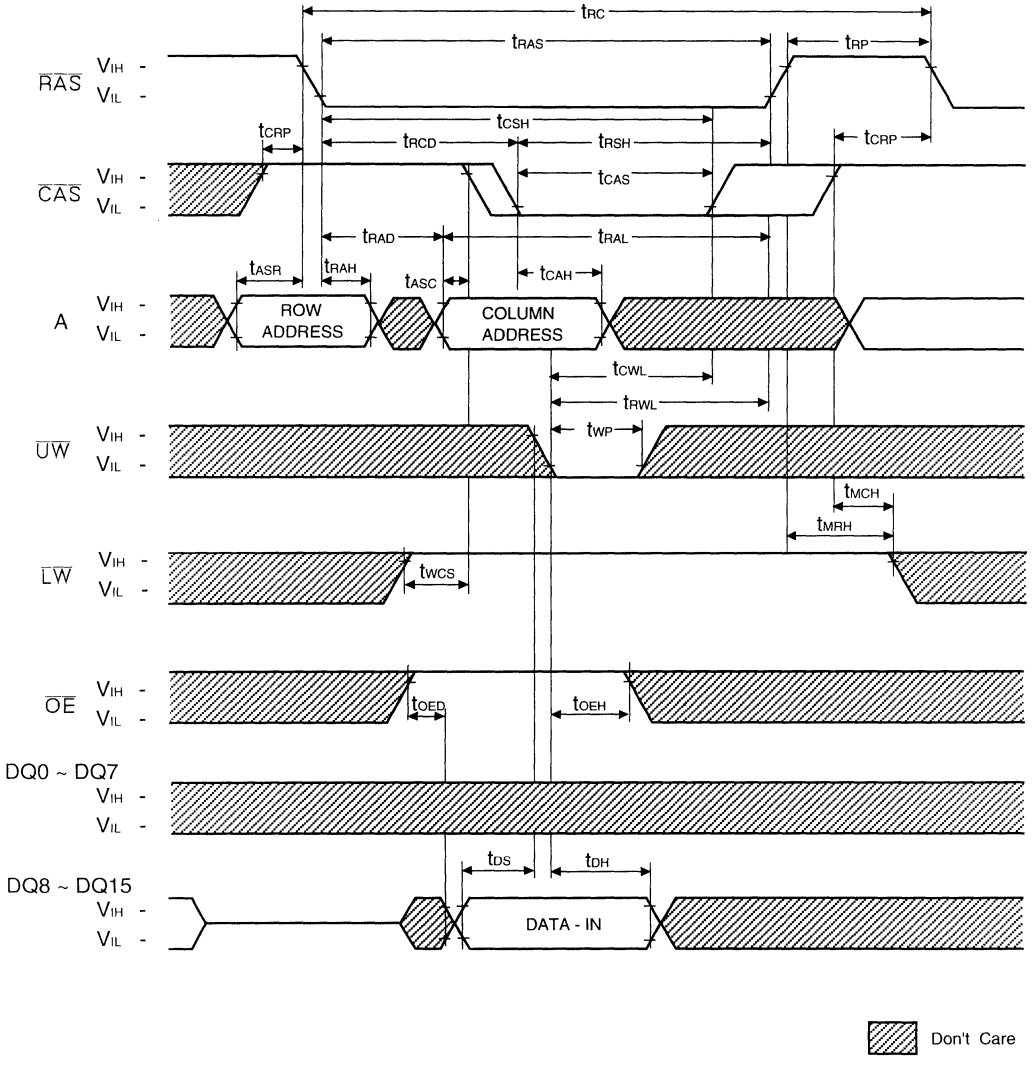
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



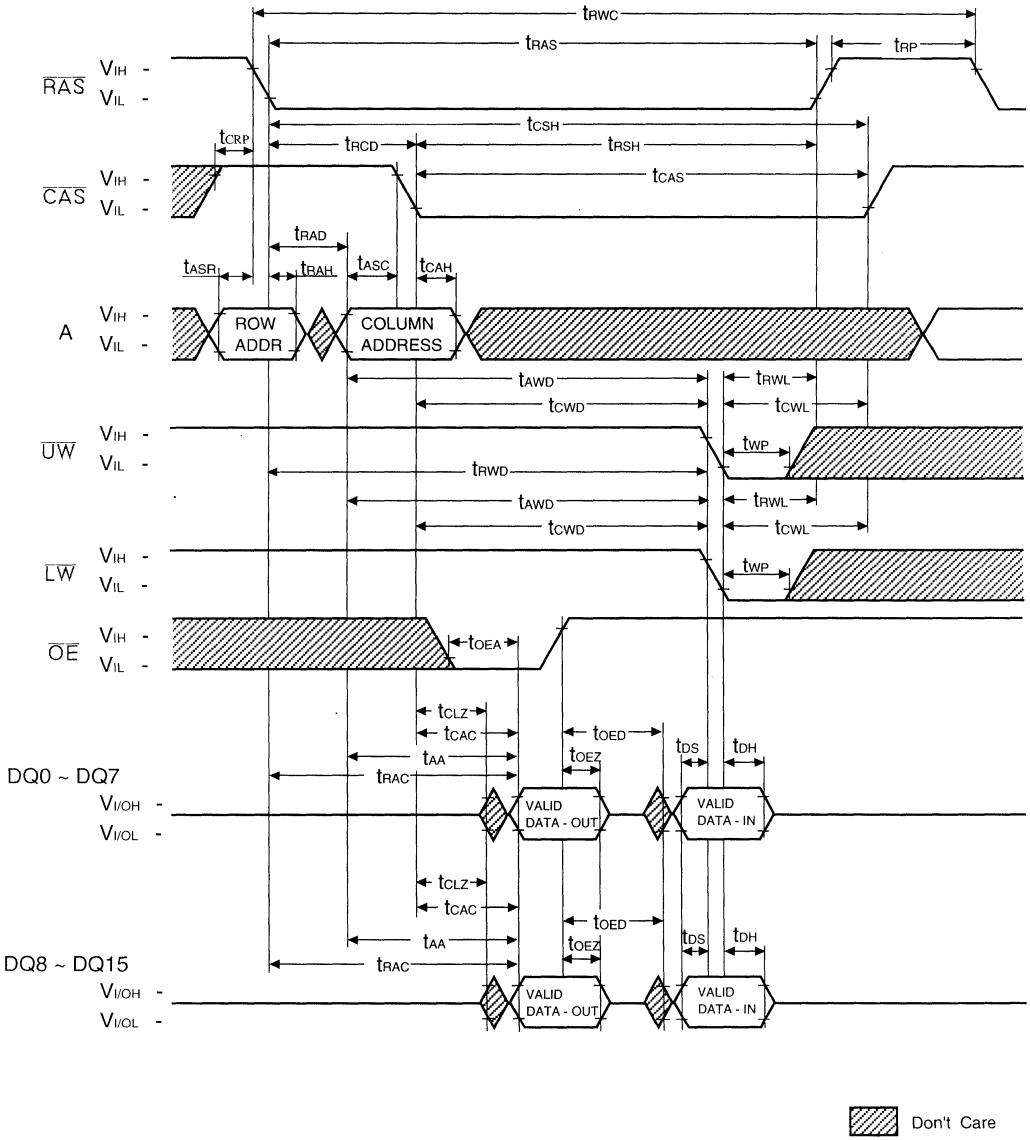
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

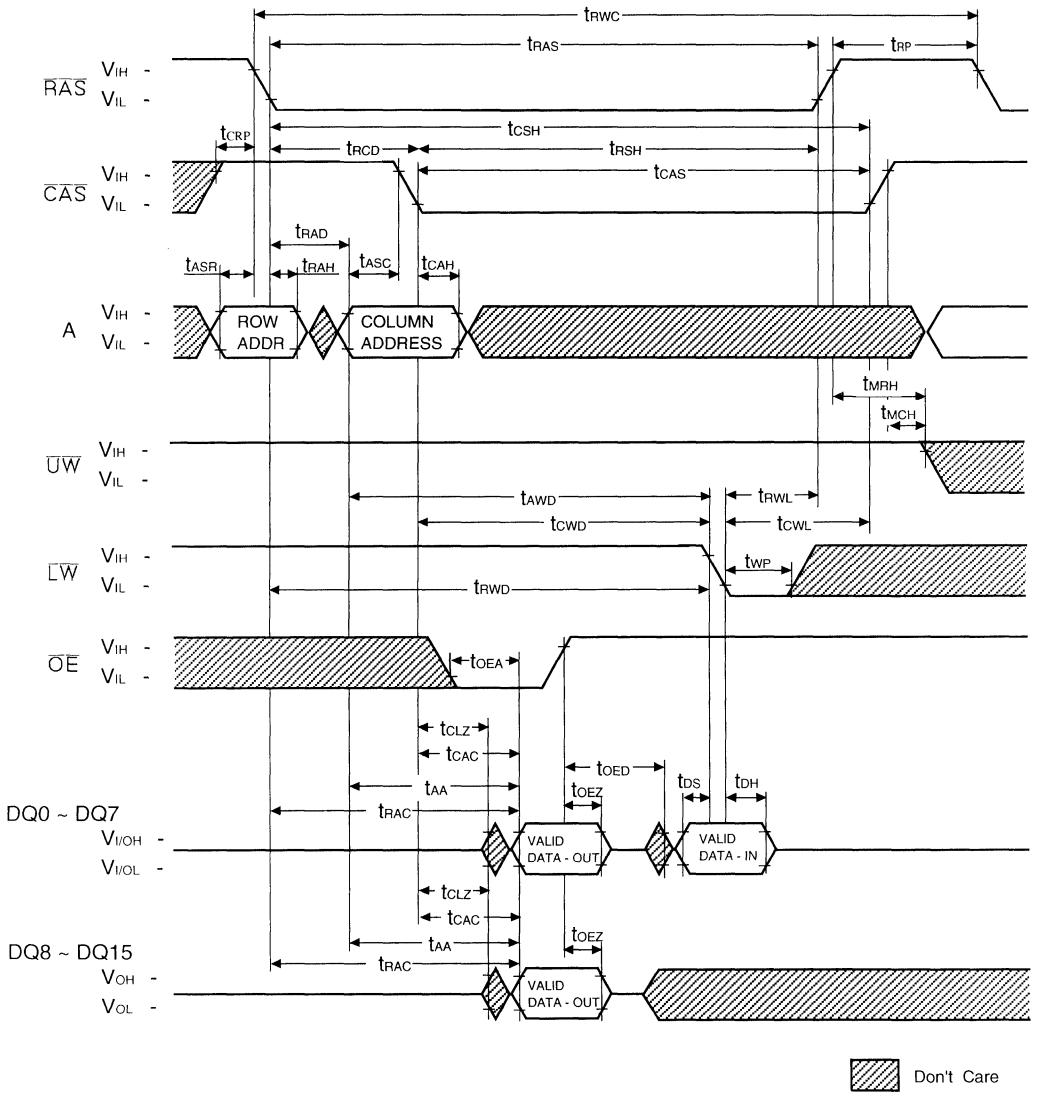


SAMSUNG ELECTRONICS

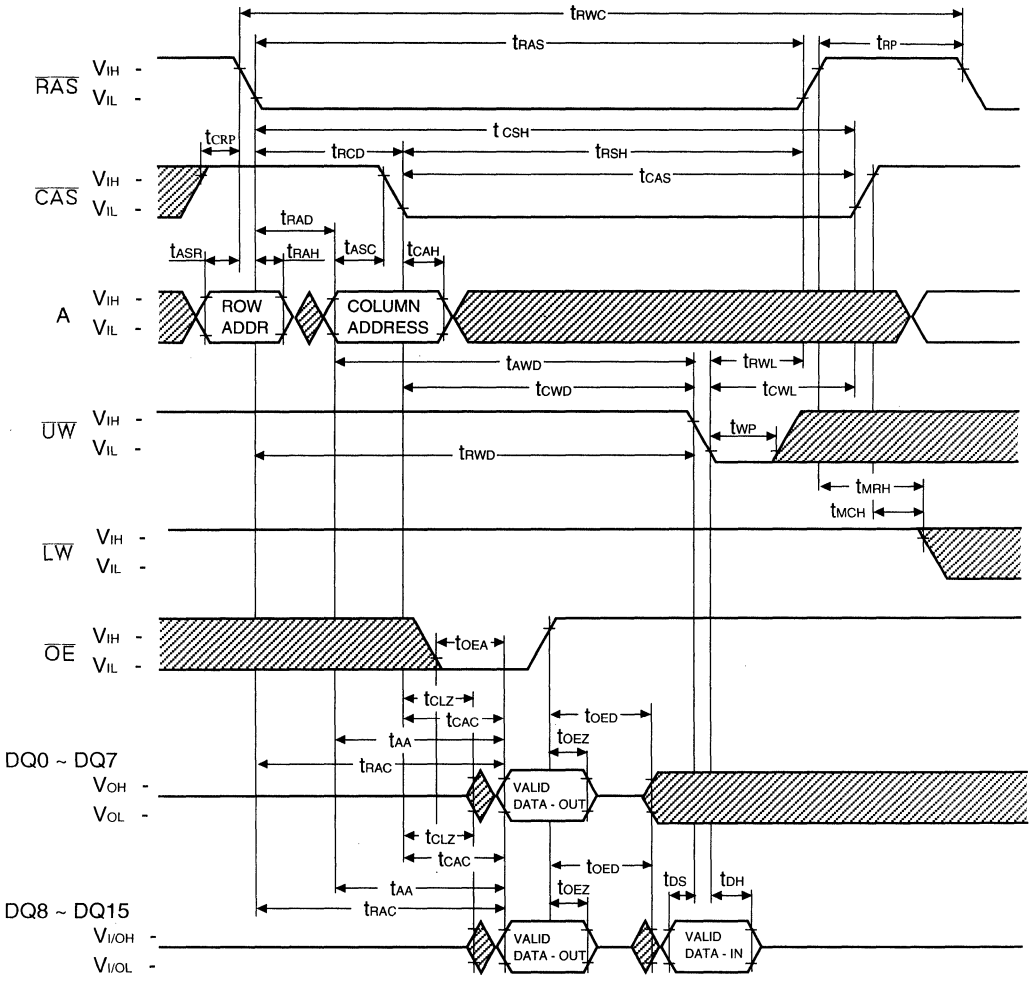
WORD READ - MODIFY - WRITE CYCLE



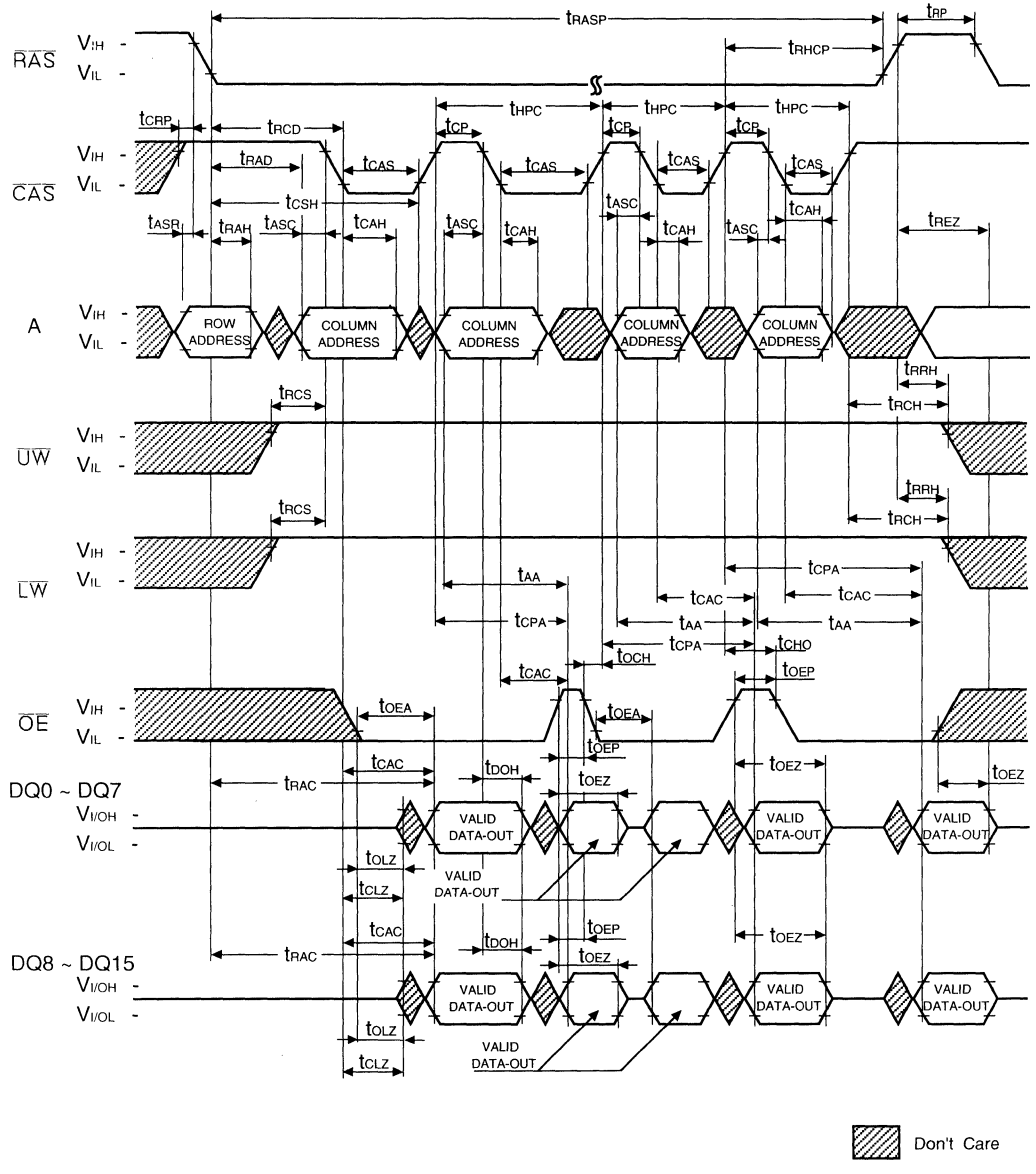
LOWER-BYTE READ - MODIFY - WRITE CYCLE



UPPER-BYTE READ - MODIFY - WRITE CYCLE

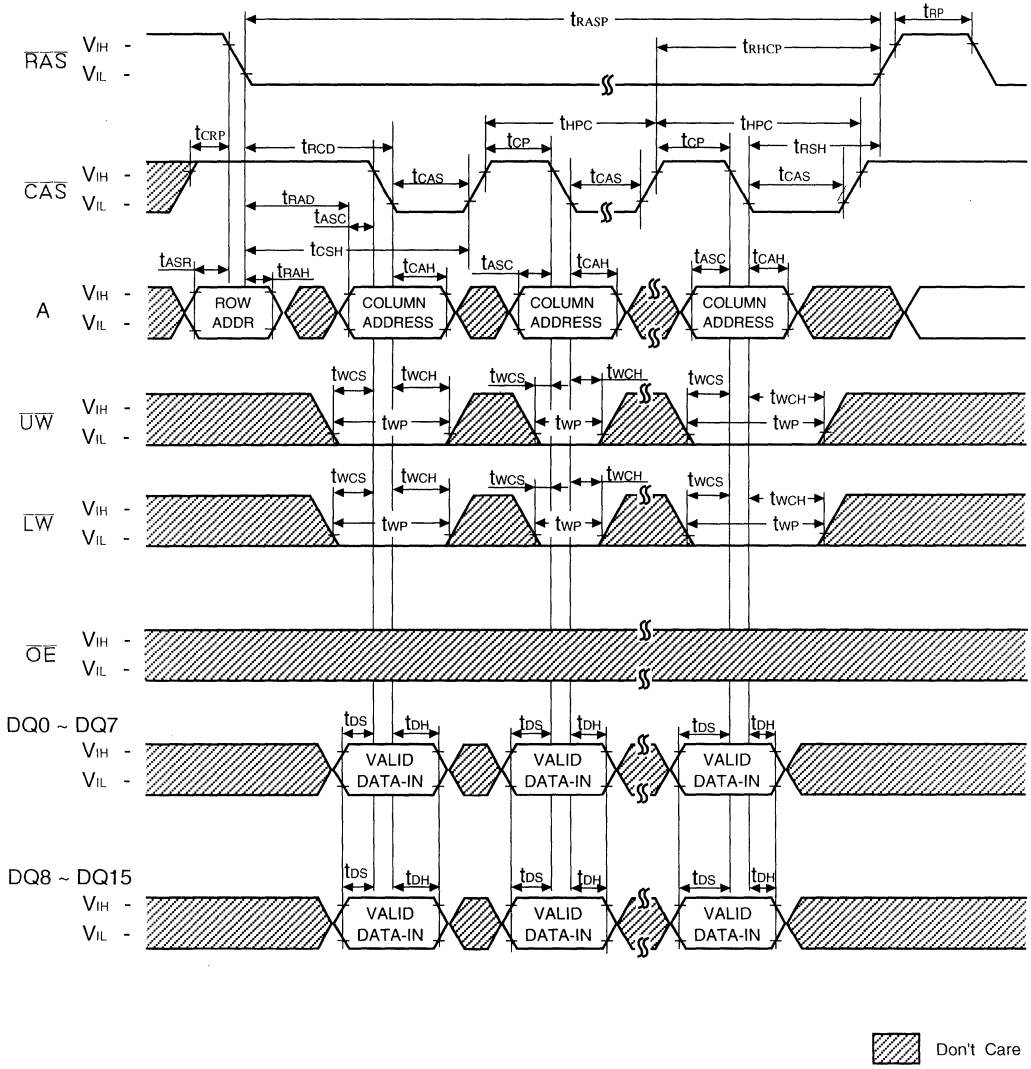


HYPER PAGE MODE WORD READ CYCLE



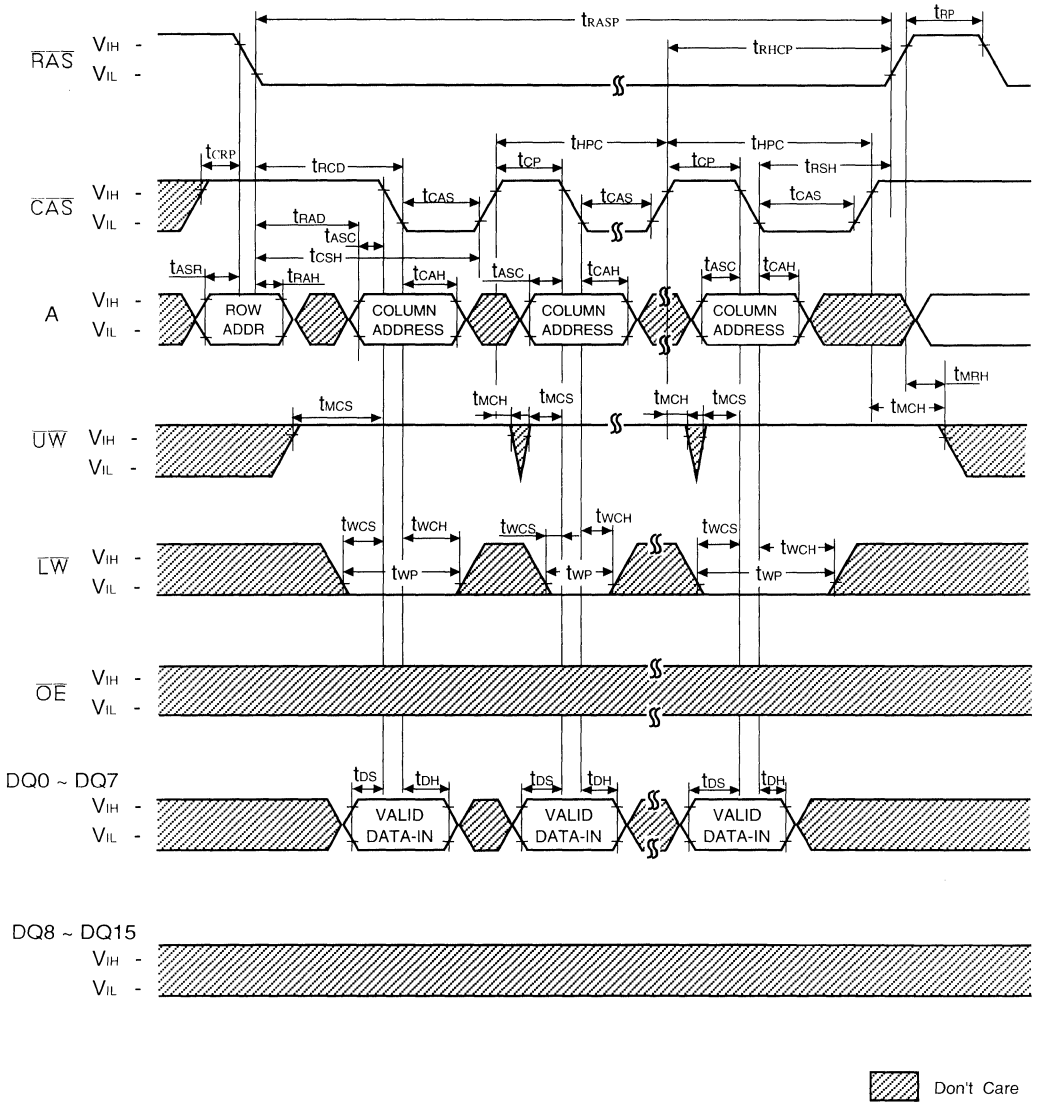
HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



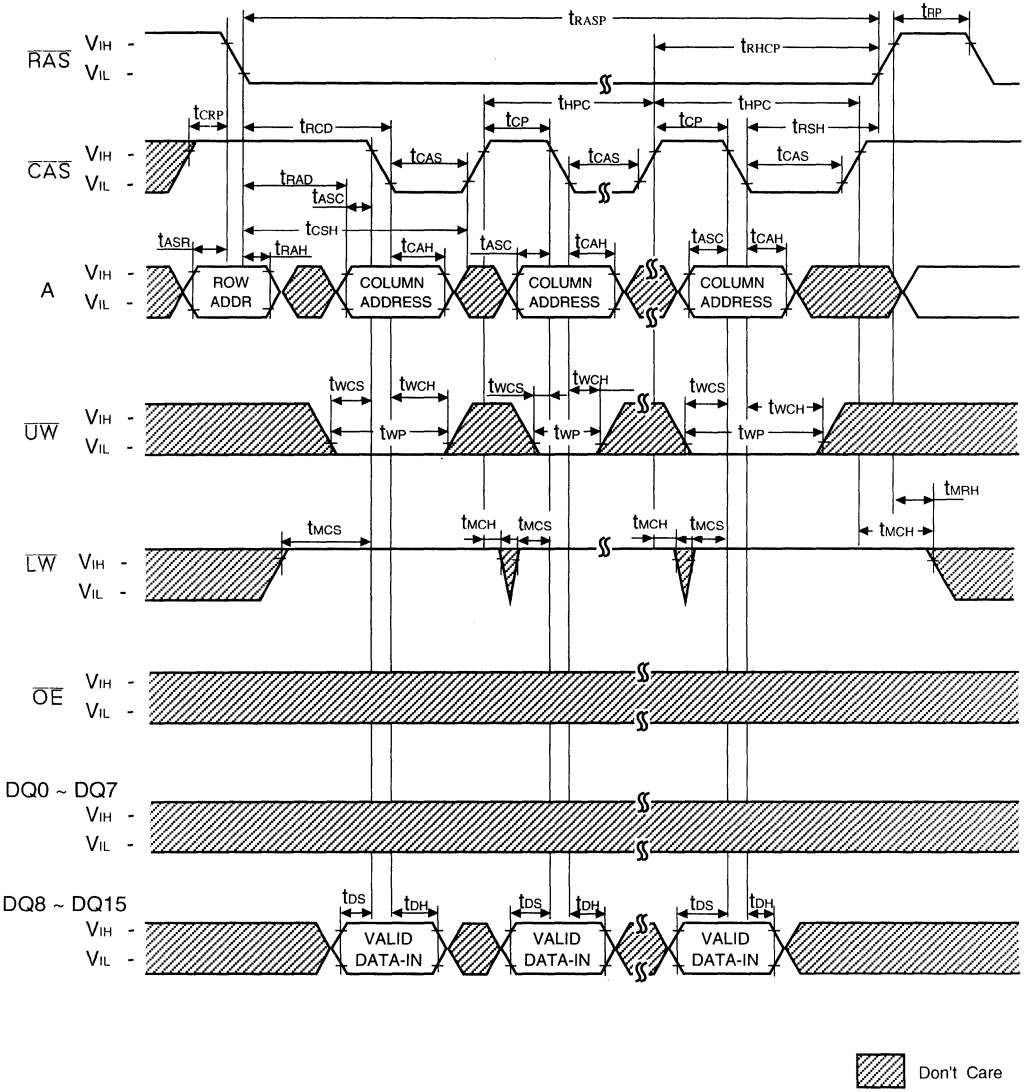
HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open

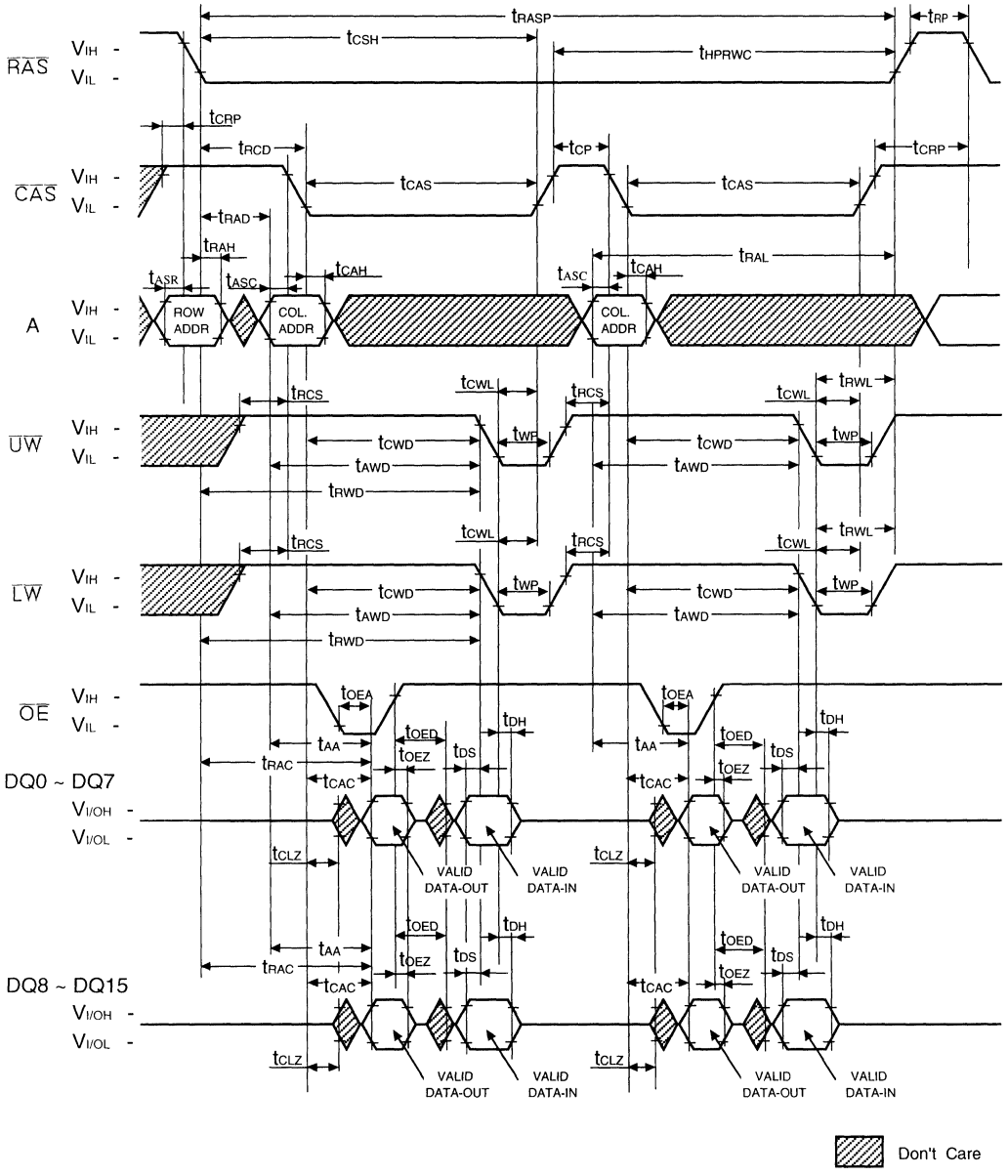


HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

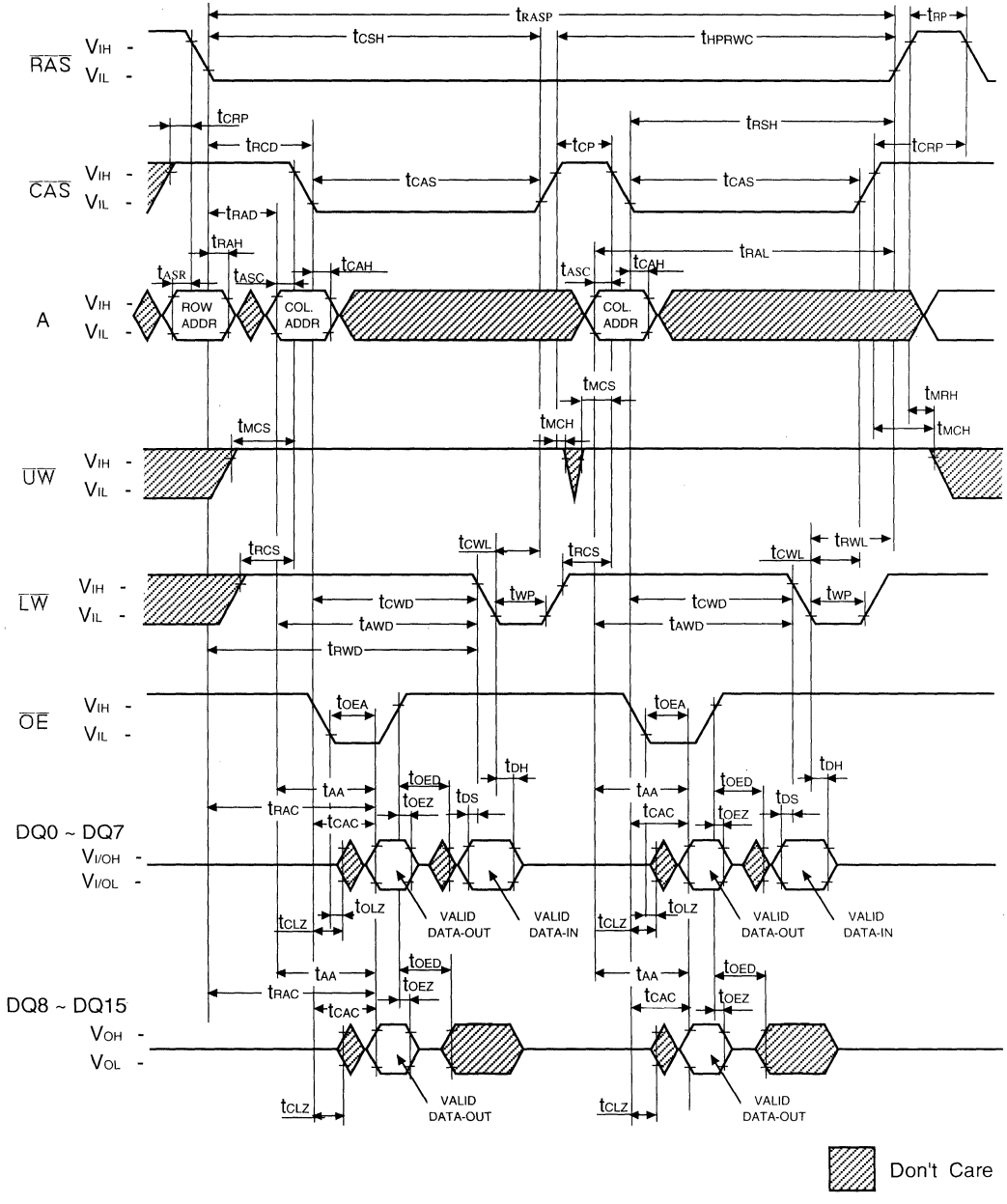
NOTE : D_{OUT} = Open



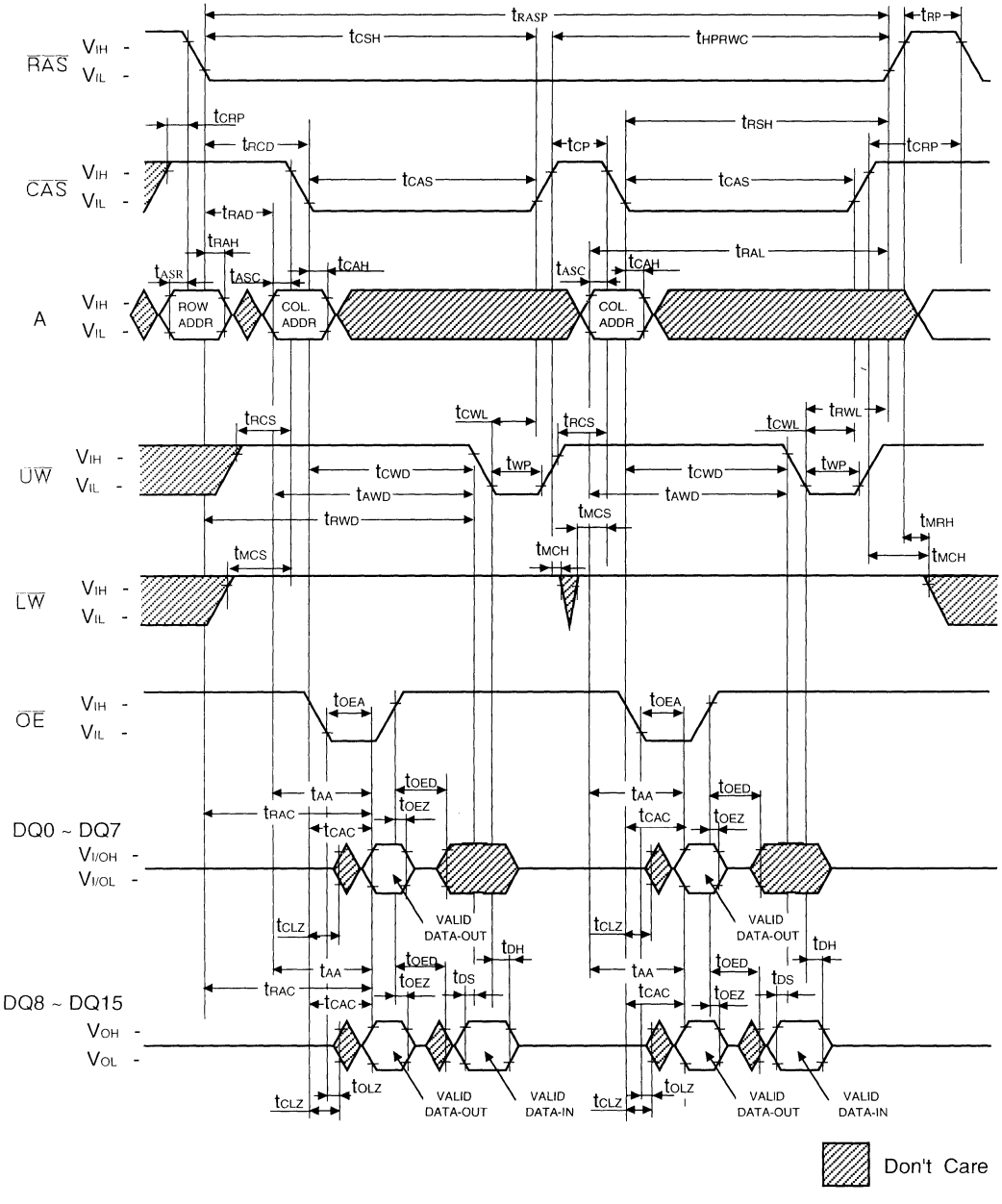
HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE



HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



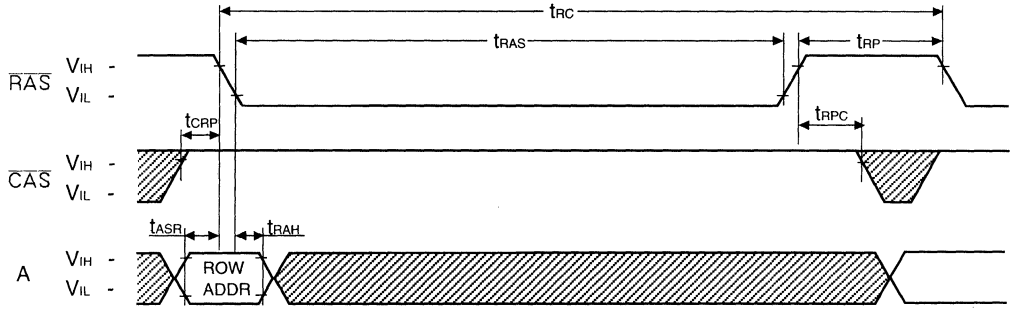
HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



SAMSUNG ELECTRONICS

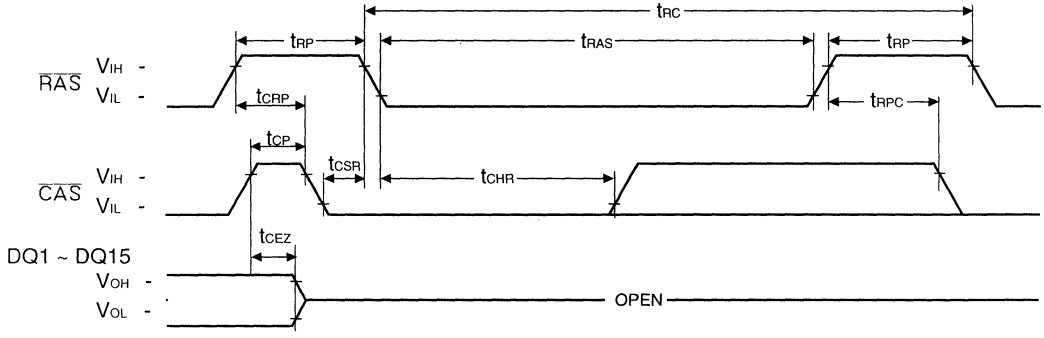
RAS-ONLY REFRESH CYCLE

NOTE : W, OE , DIN = Don't care
DOUT = Open



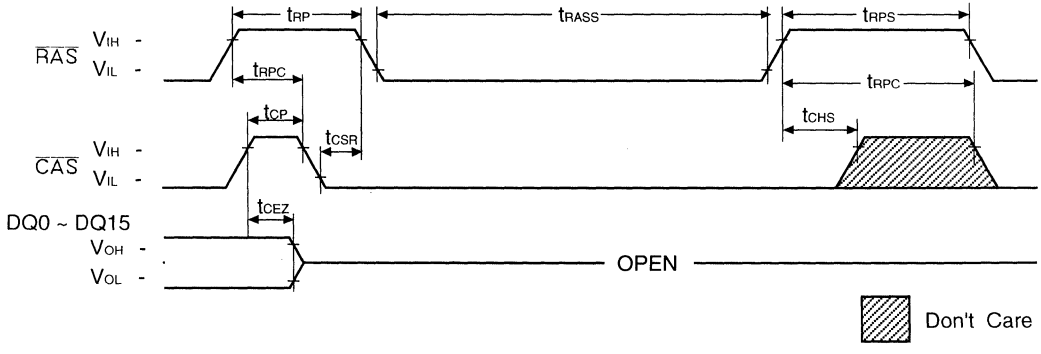
CAS-BEFORE-RAS REFRESH CYCLE

NOTE : W, OE, A = Don't Care

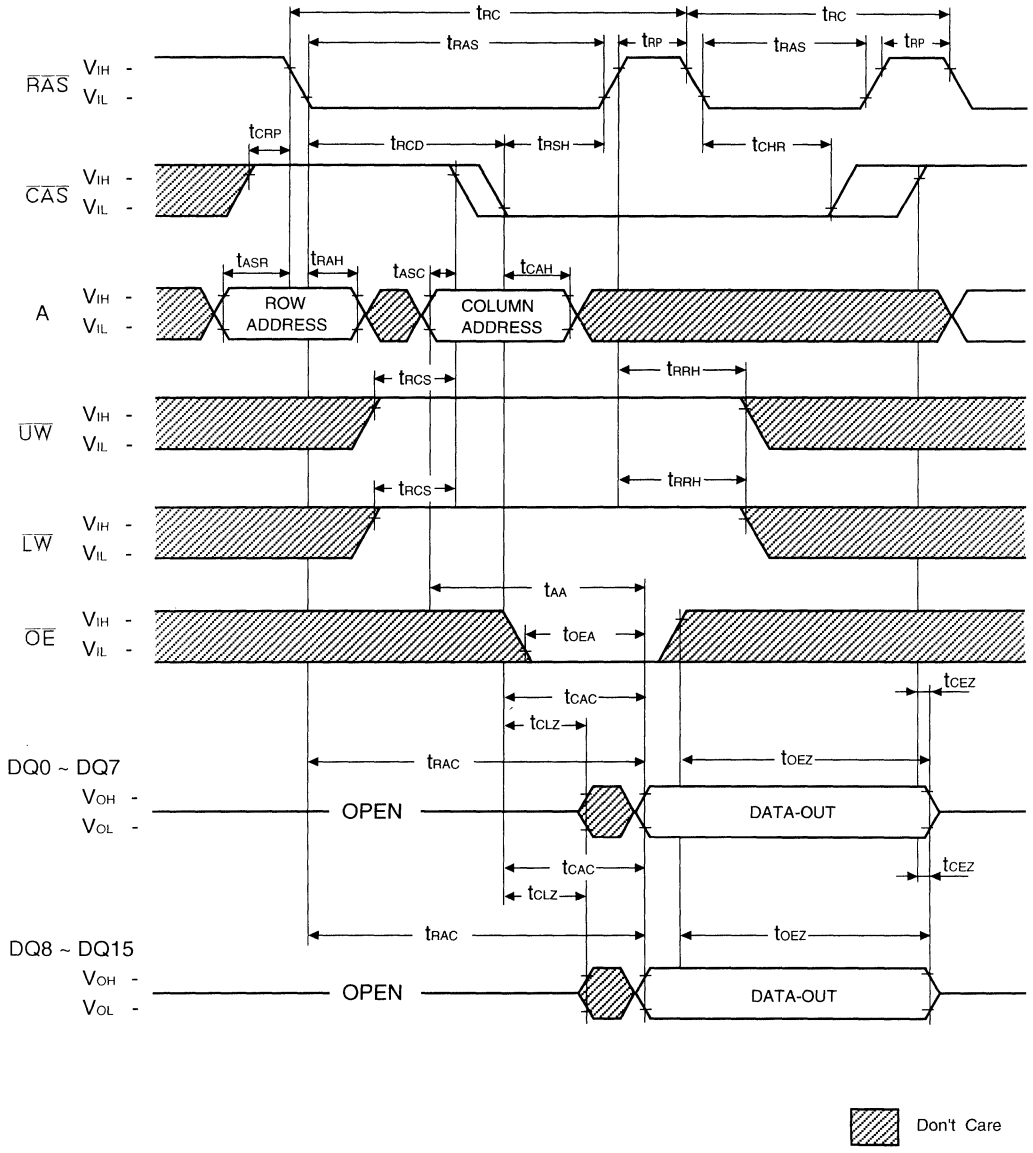


CAS-BEFORE-RAS SELF REFRESH CYCLE

NOTE : W, OE, A = Don't Care

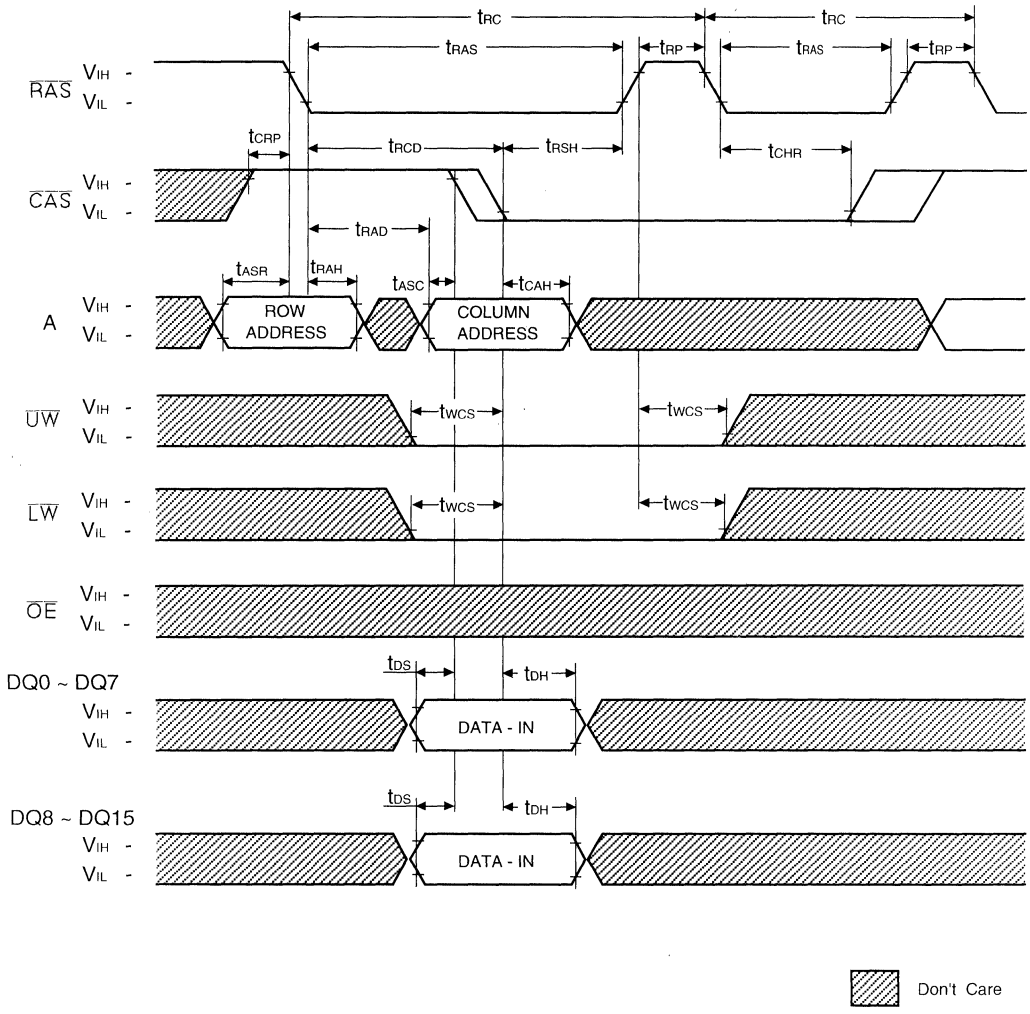


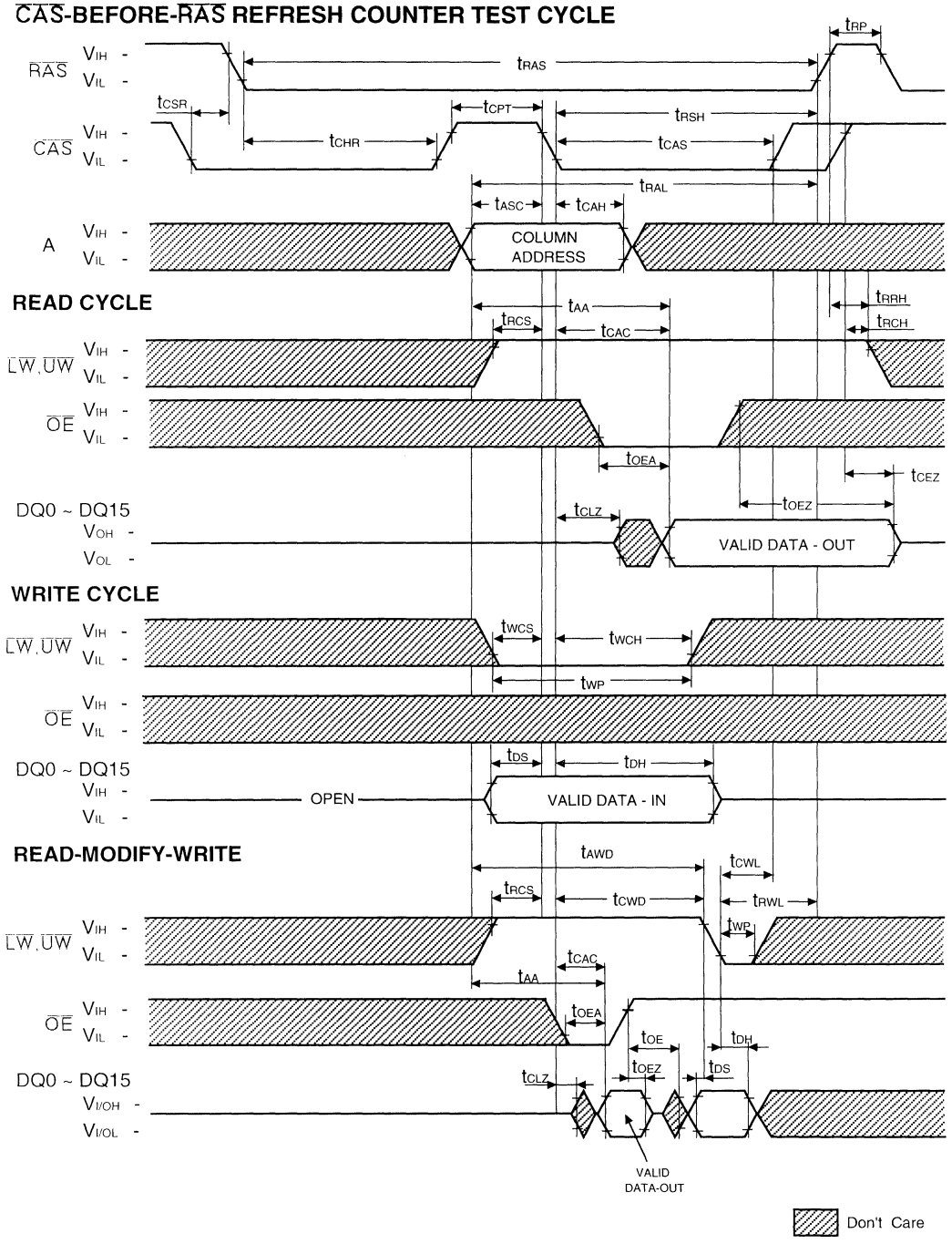
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN





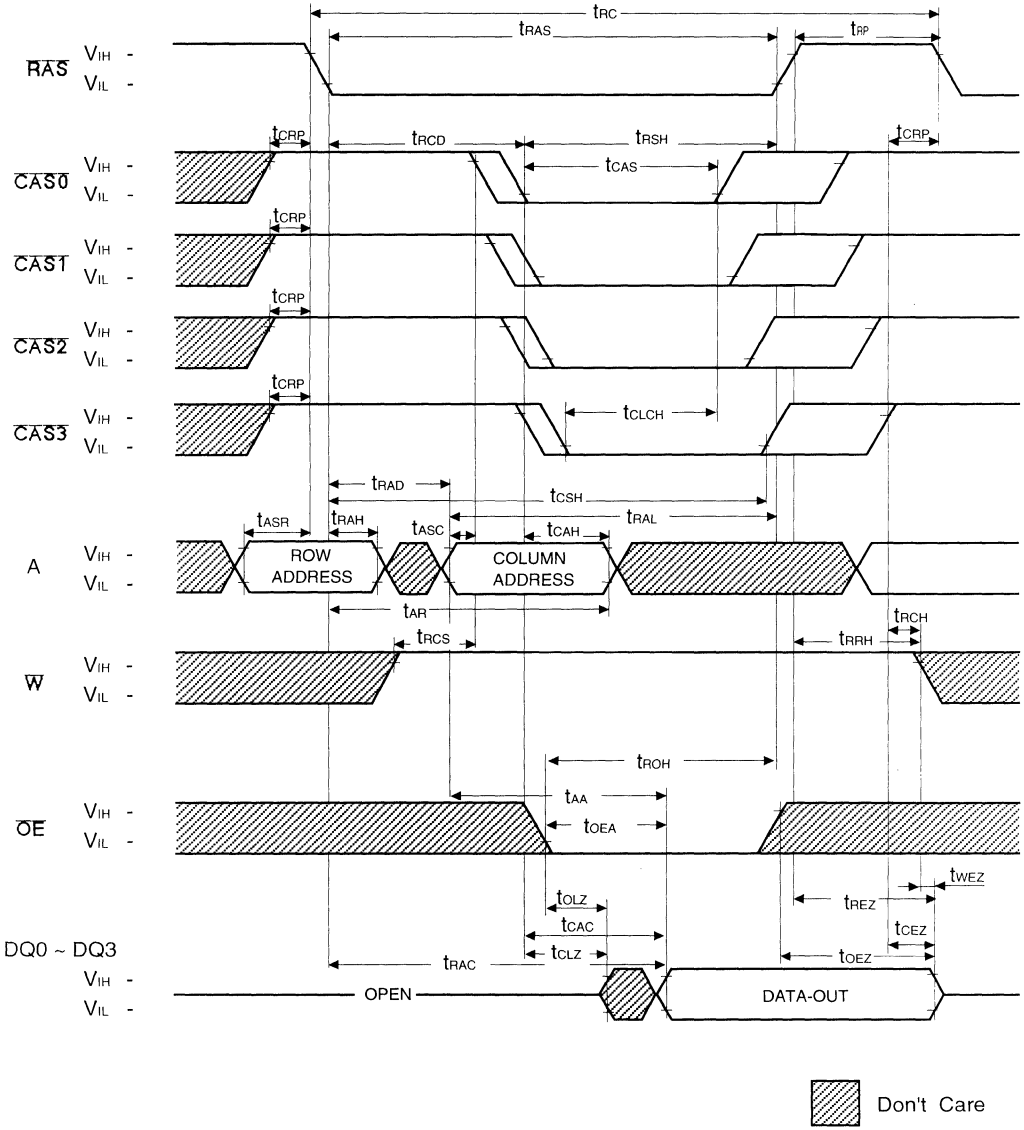
SAMSUNG ELECTRONICS

EDO Mode, Quad $\overline{CAS}$ Device

TIMING DIAGRAM

READ CYCLE

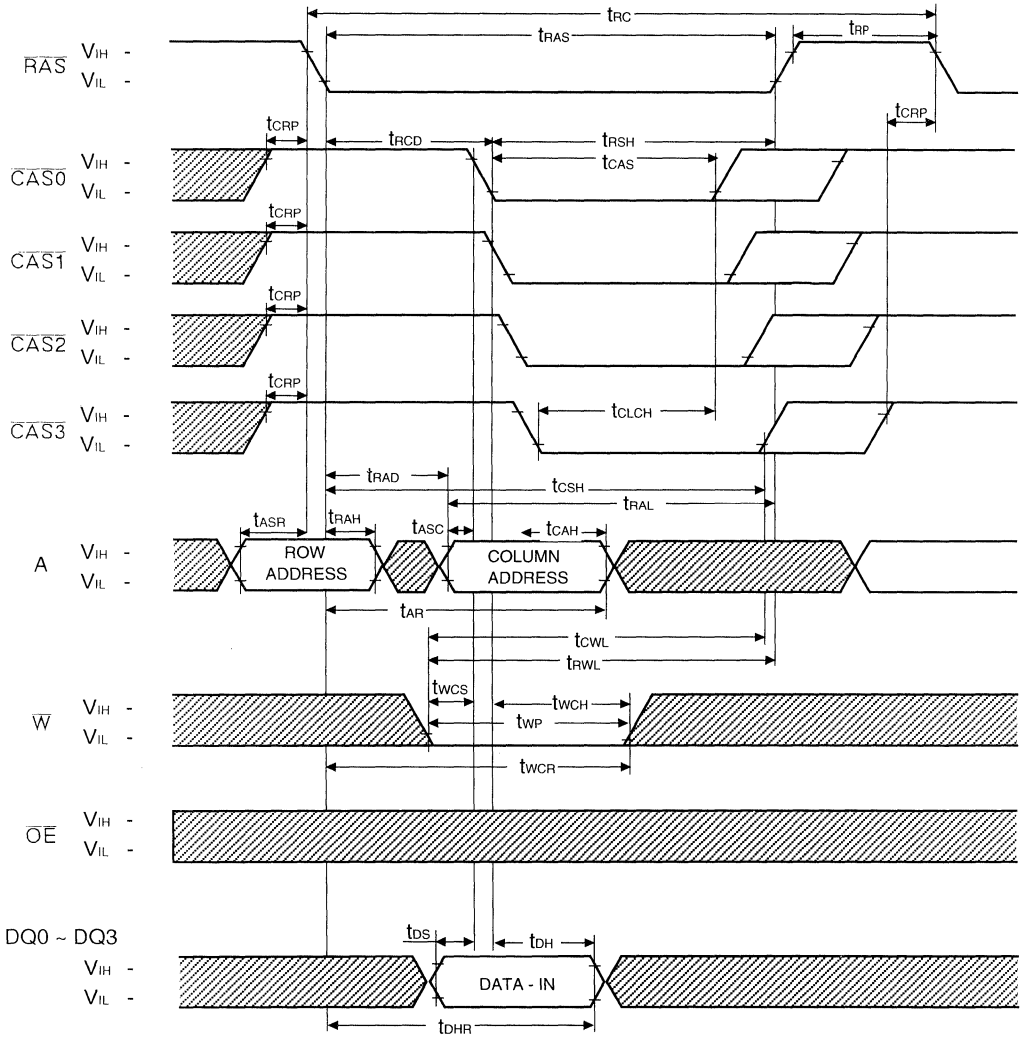
NOTE : D_{IN} = OPEN



SAMSUNG ELECTRONICS

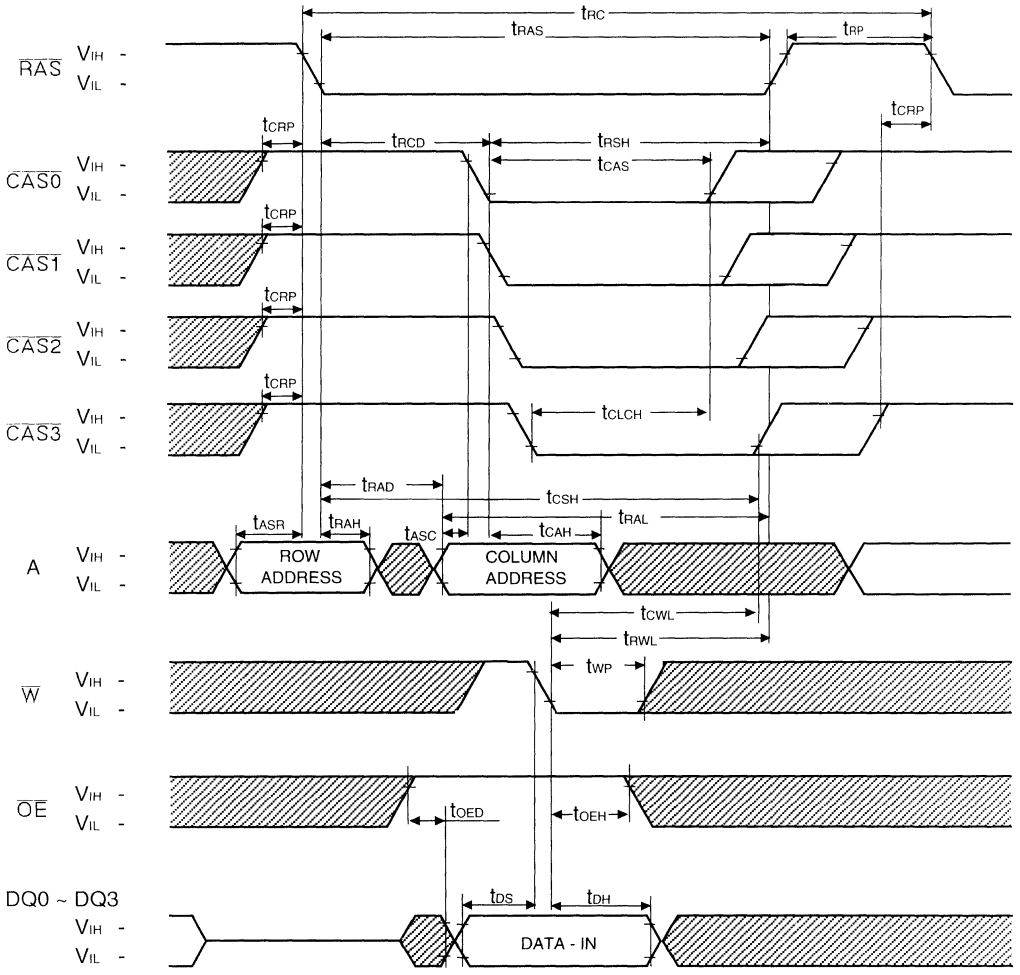
TIMING DIAGRAM

WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAM

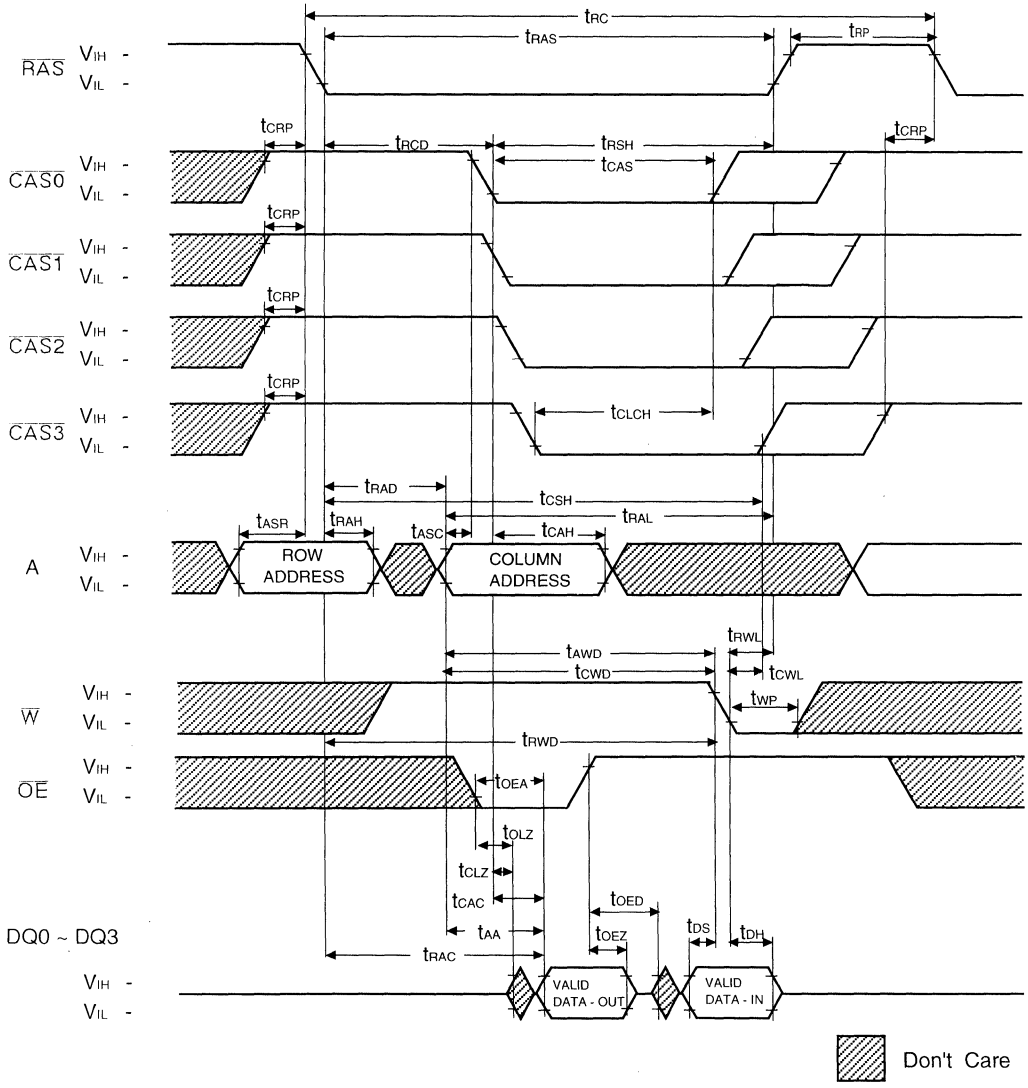
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



SAMSUNG ELECTRONICS

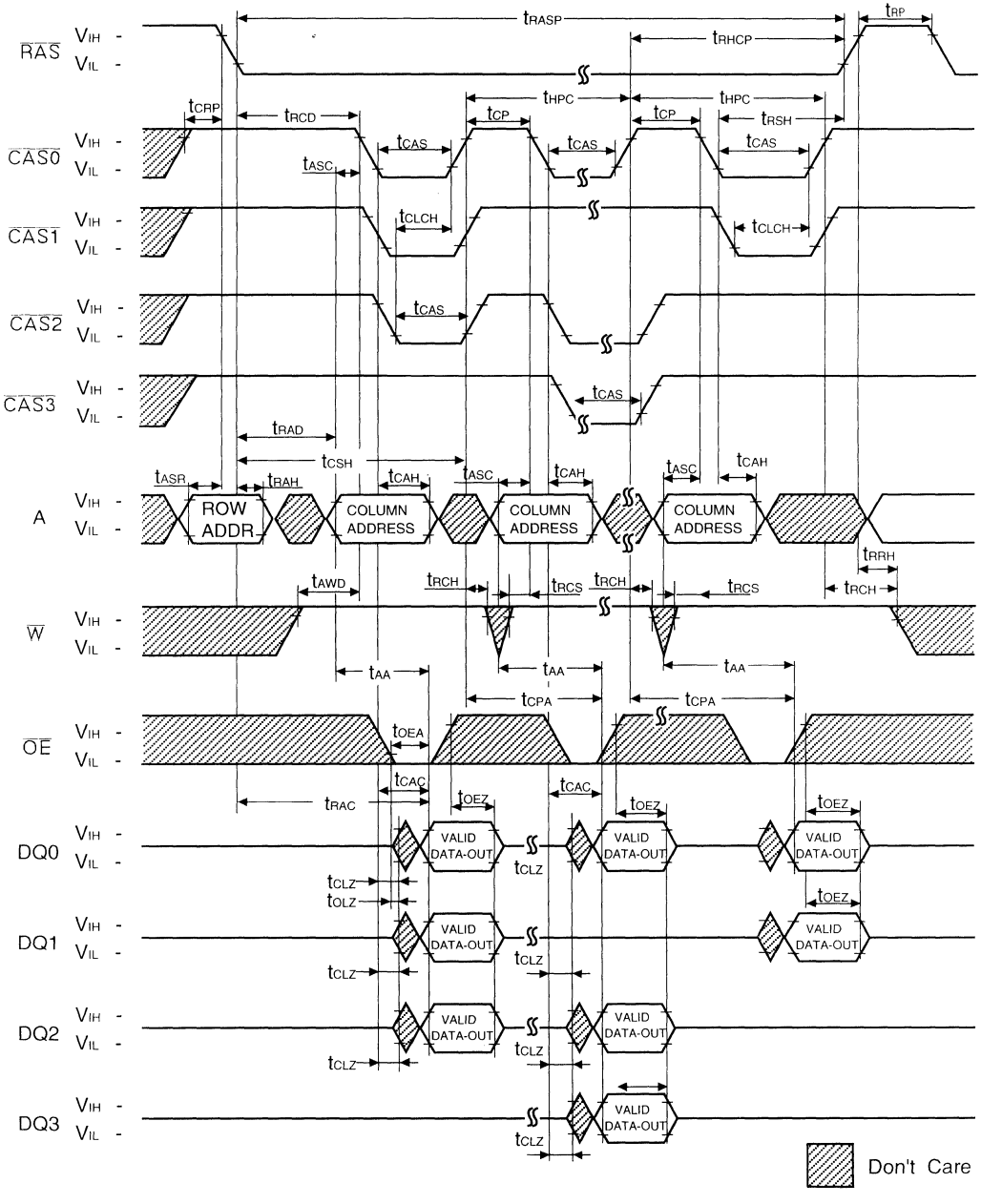
TIMING DIAGRAM

READ - MODIFY - WRITE CYCLE

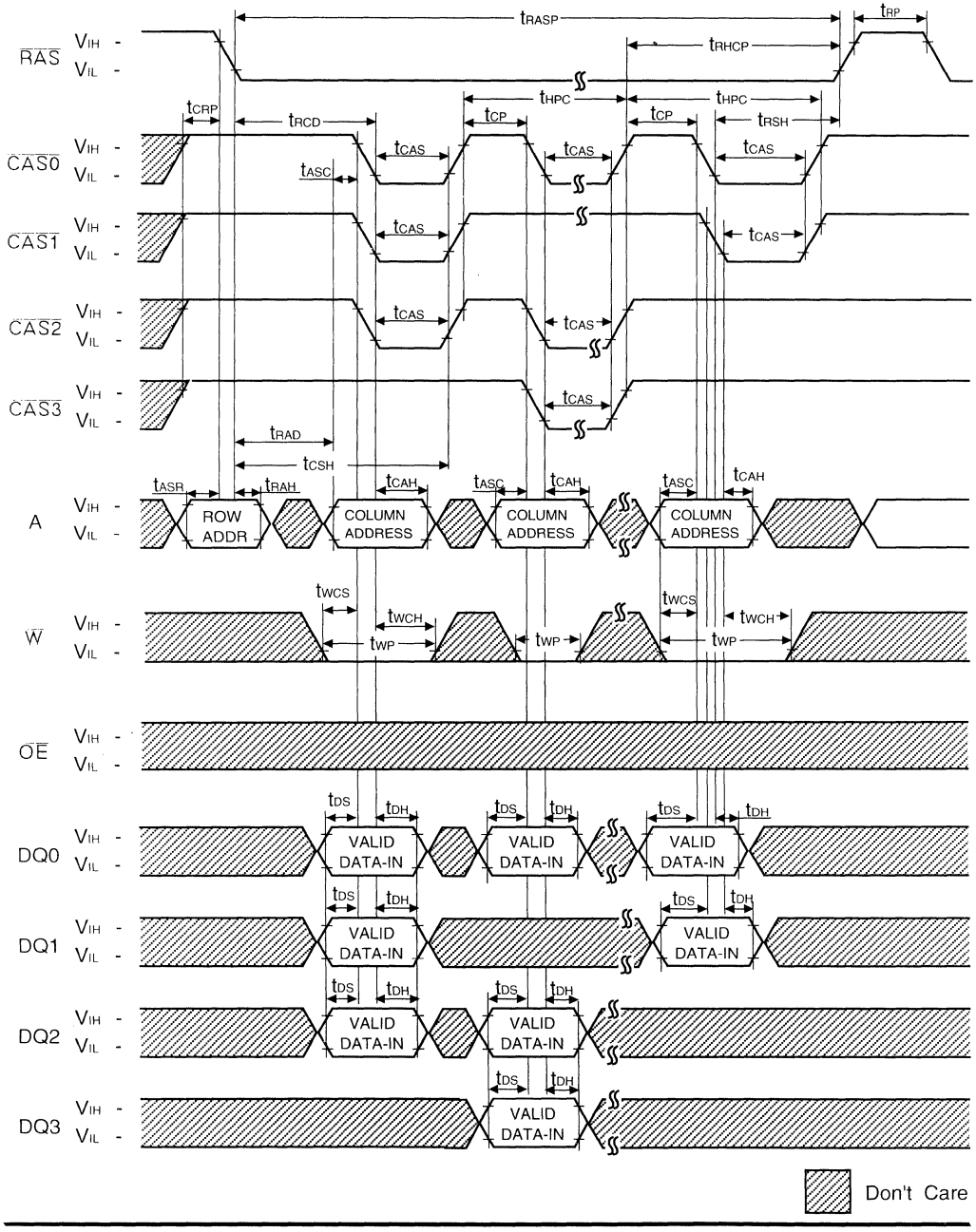


SAMSUNG ELECTRONICS

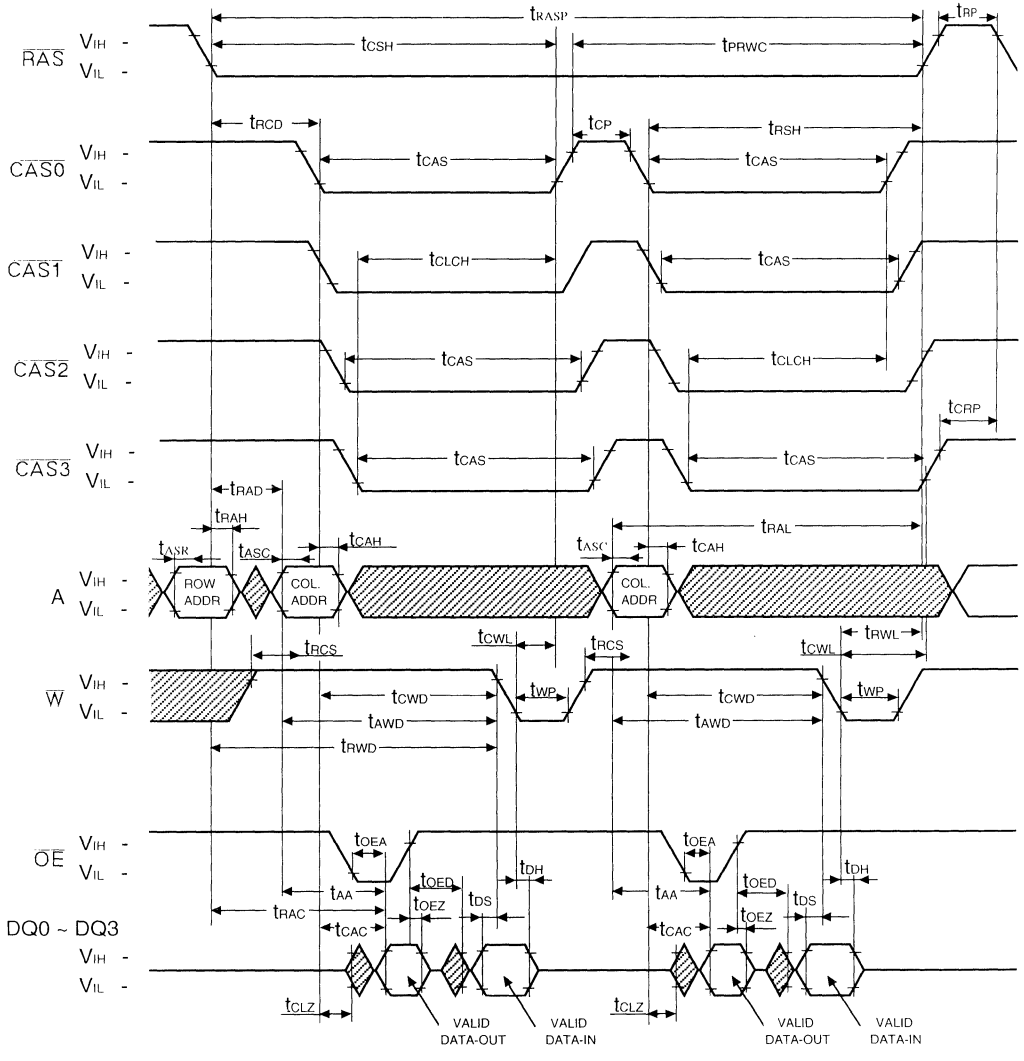
HYPER PAGE MODE READ CYCLE



HYPER PAGE MODE WRITE CYCLE (EARLY WRITE)



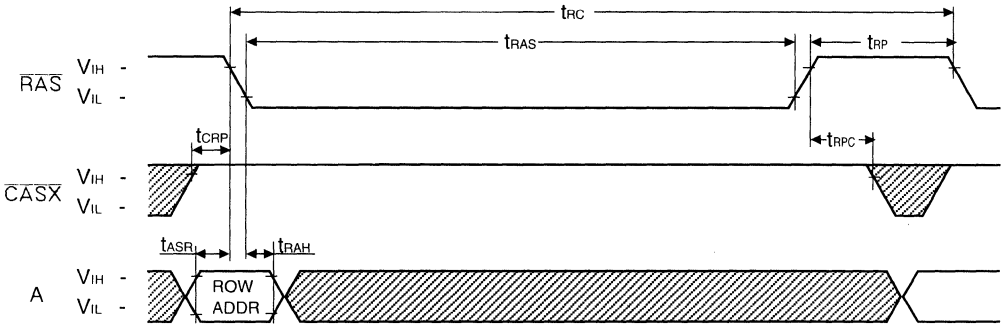
HYPER PAGE MODE READ-MODIFY-WRITE CYCLE



SAMSUNG ELECTRONICS

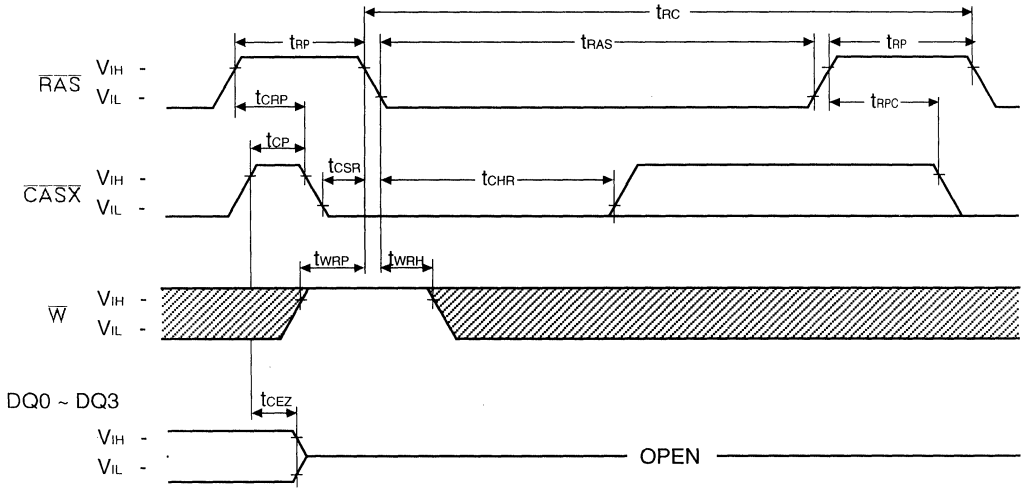
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open

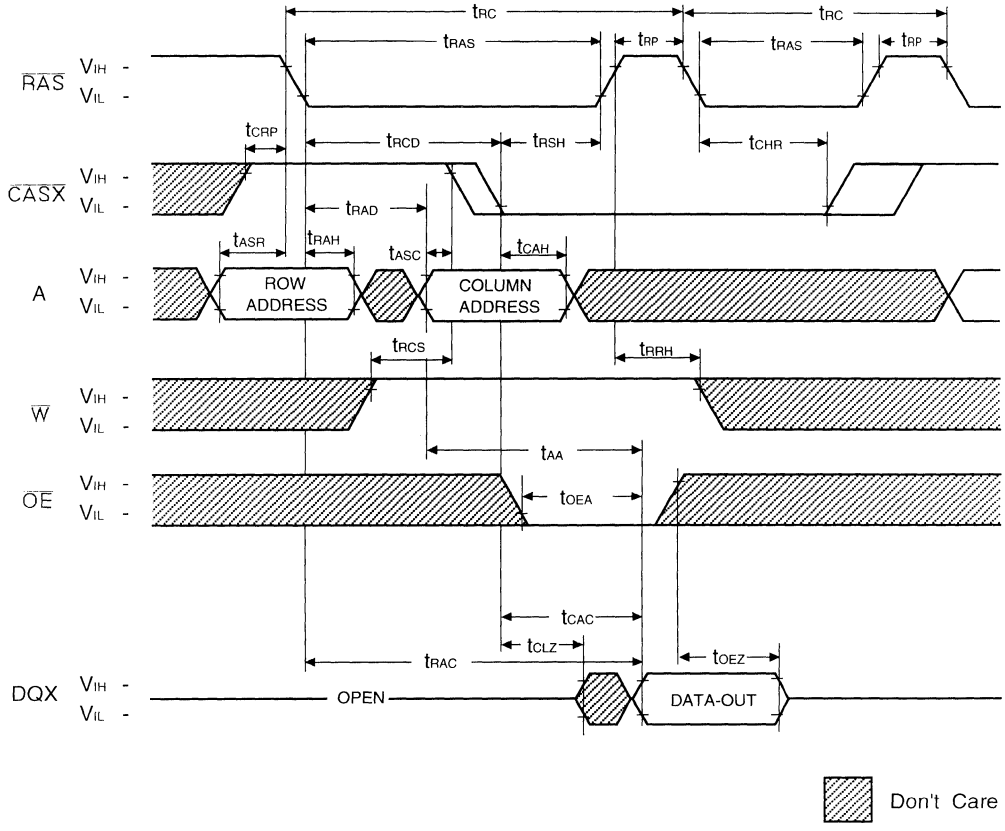


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

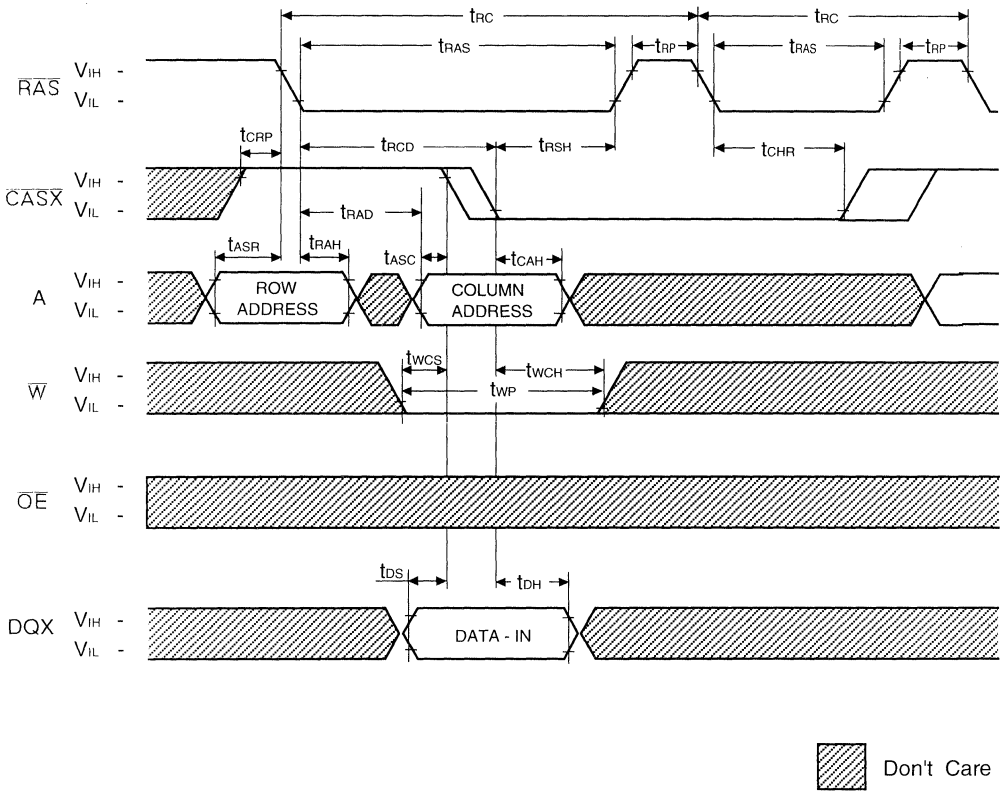


HIDDEN REFRESH CYCLE (READ)



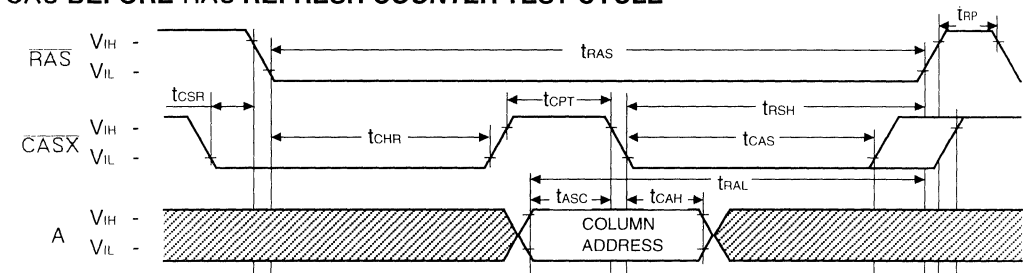
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN

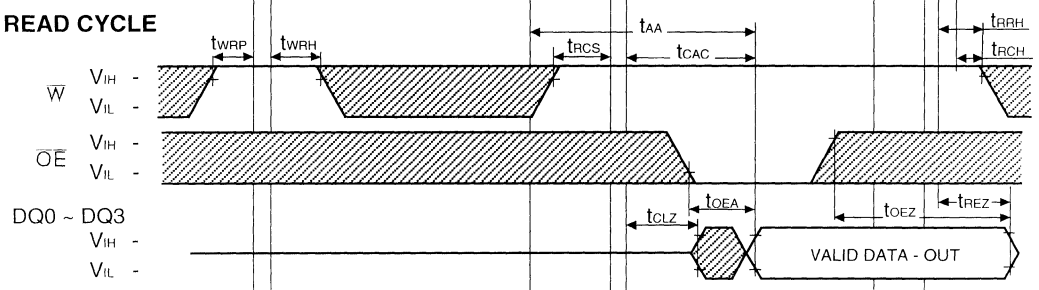


Don't Care

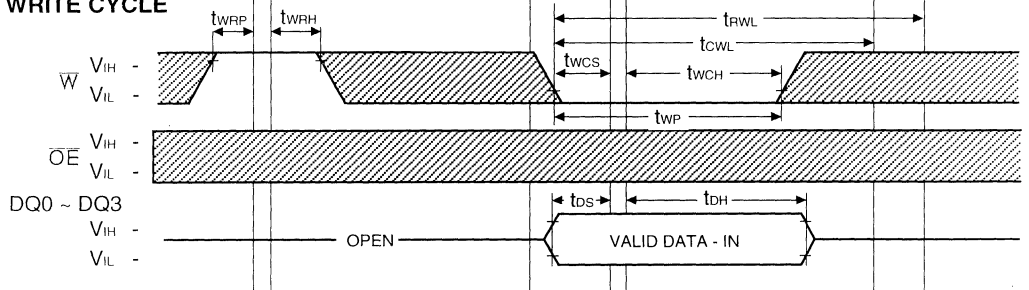
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



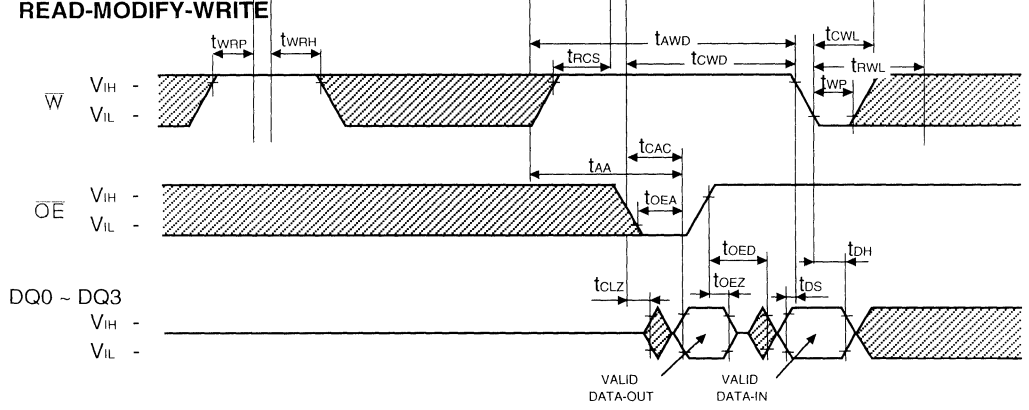
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE

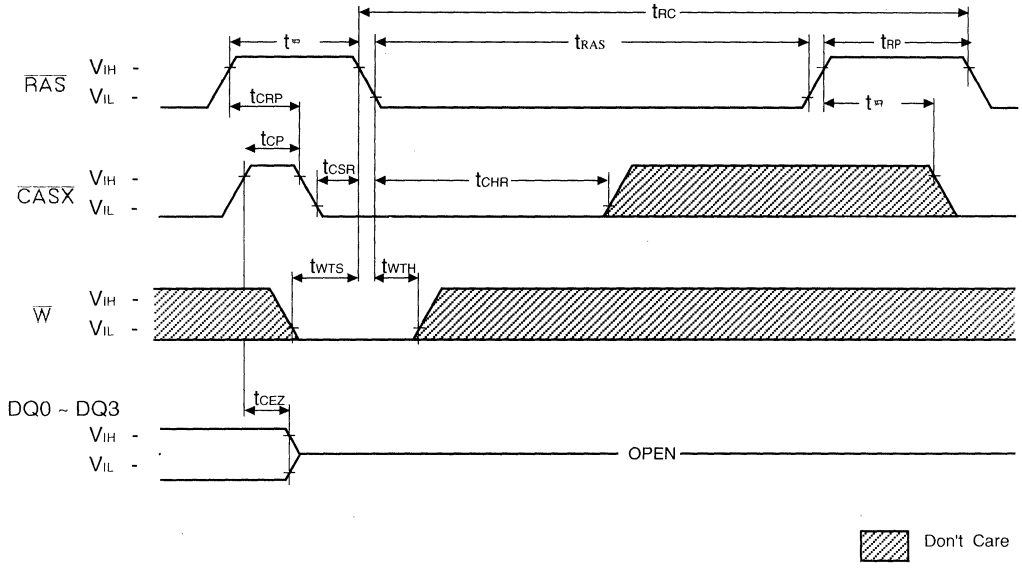


Don't Care

SAMSUNG ELECTRONICS

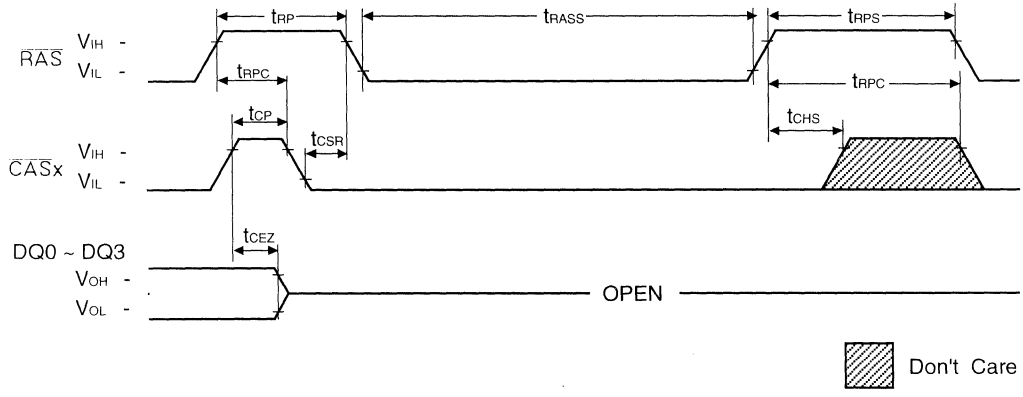
TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

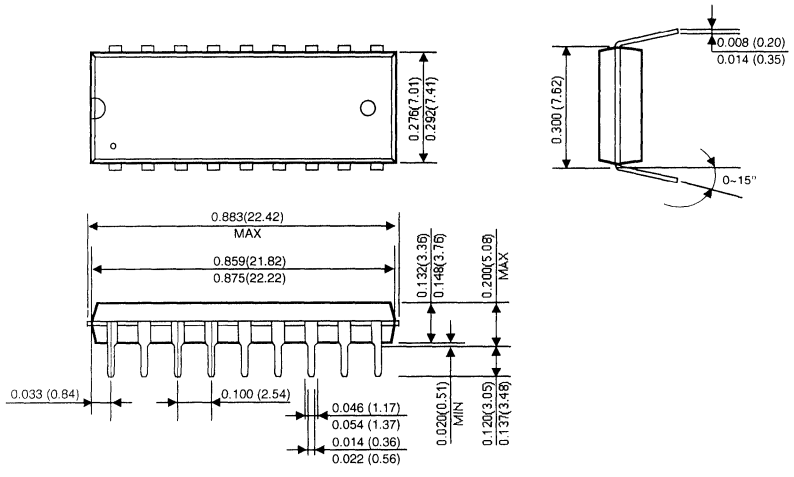


PACKAGE DIMENSIONS 4

PLASTIC DUAL IN-LINE PACKAGE

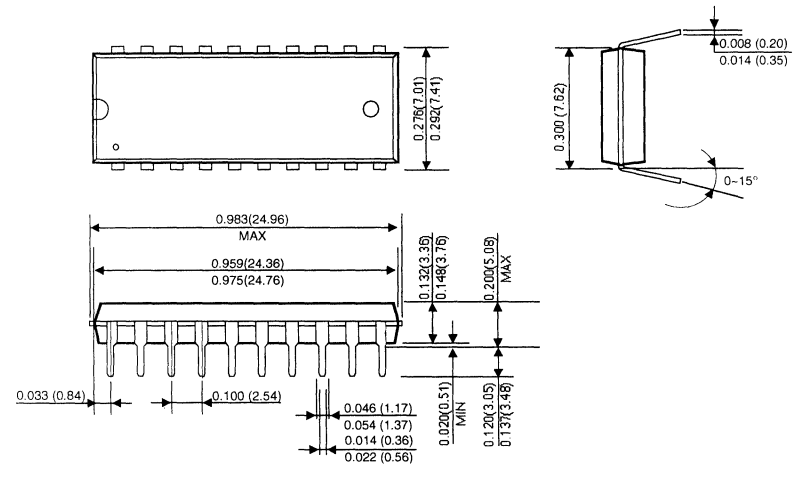
18 DIP 300 mil

Unit : Inches (millimeters)



20 DIP 300 mil

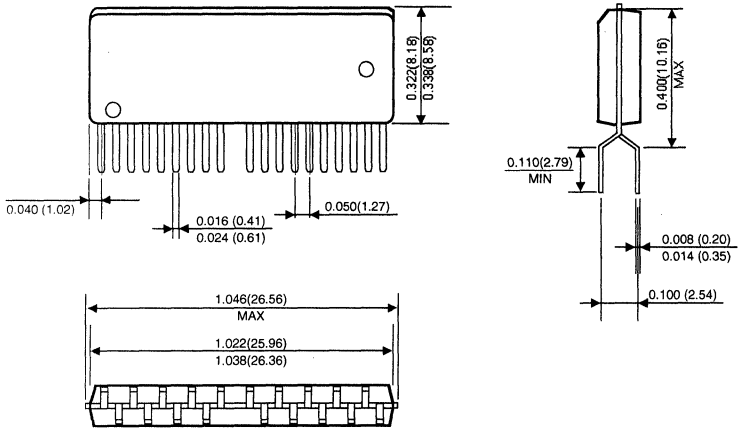
Unit : Inches (millimeters)



PLASTIC ZIGZAG IN-LINE PACKAGE

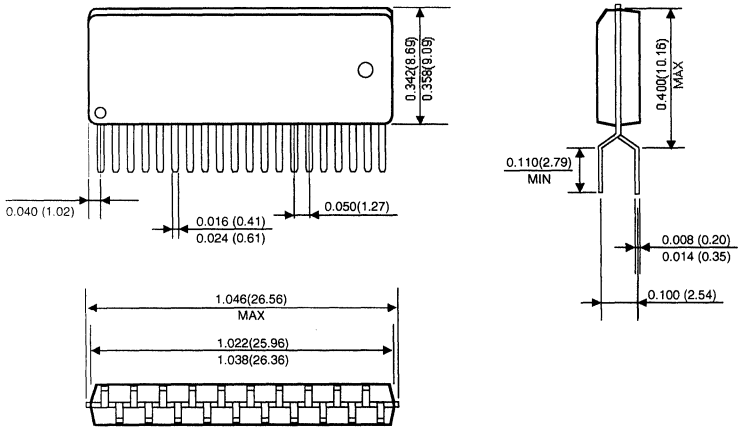
20(19) ZIP 400 mil

Unit : Inches (millimeters)



20 ZIP 400 mil

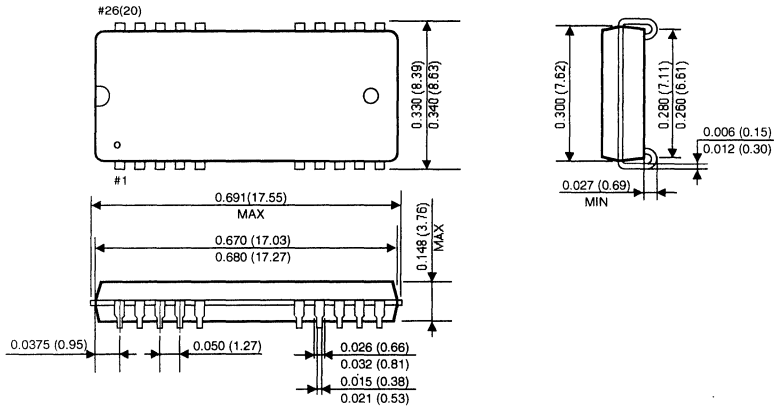
Unit : Inches (millimeters)



PLASTIC SMALL OUT-LINE J-LEAD

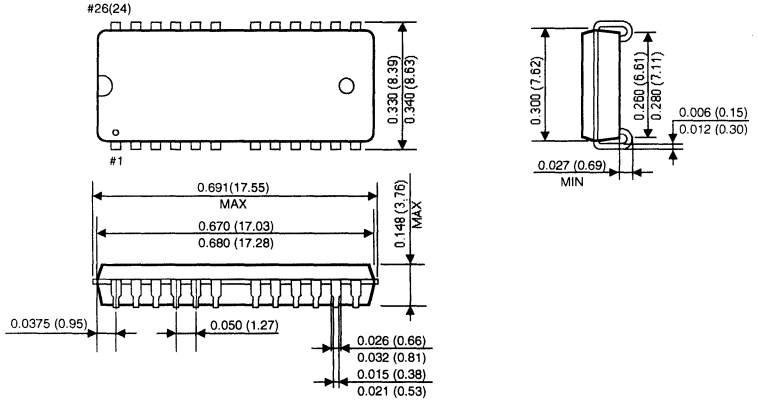
26(20) SOJ 300 mil

Unit : Inches (millimeters)



26(24) SOJ 300 mil

Unit : Inches (millimeters)

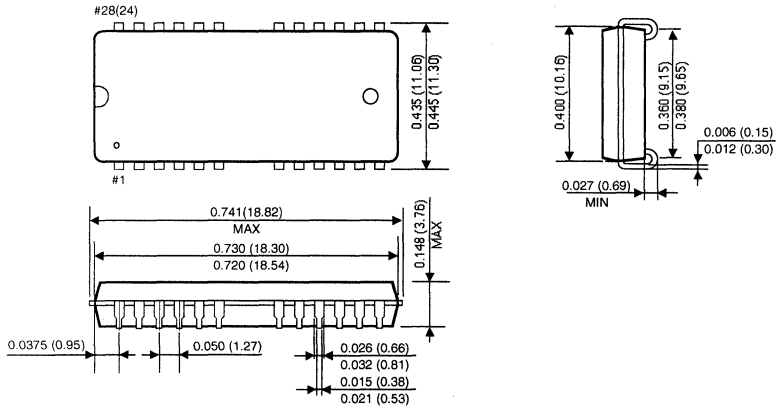


4

PLASTIC SMALL OUT-LINE J-LEAD

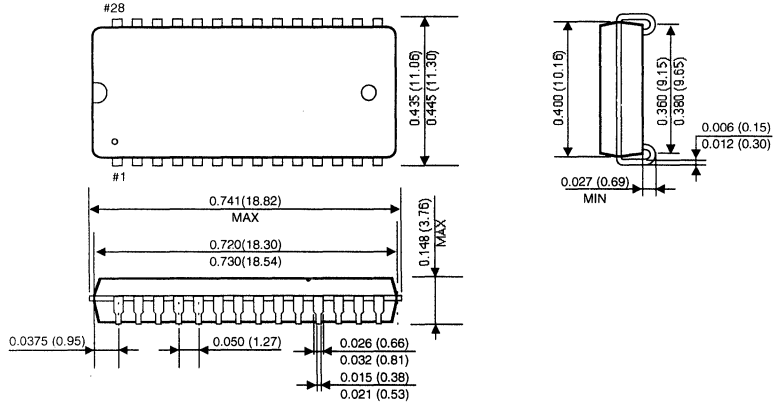
28(24) SOJ 400 mil

Unit : Inches (millimeters)



28 SOJ 400 mil

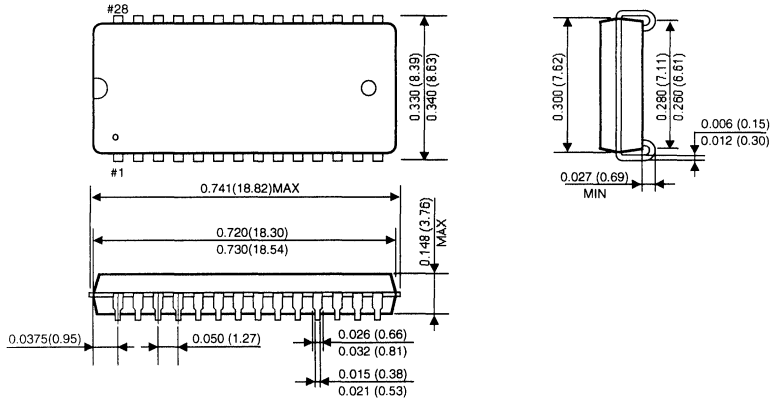
Unit : Inches (millimeters)



PLASTIC SMALL OUT-LINE J-LEAD

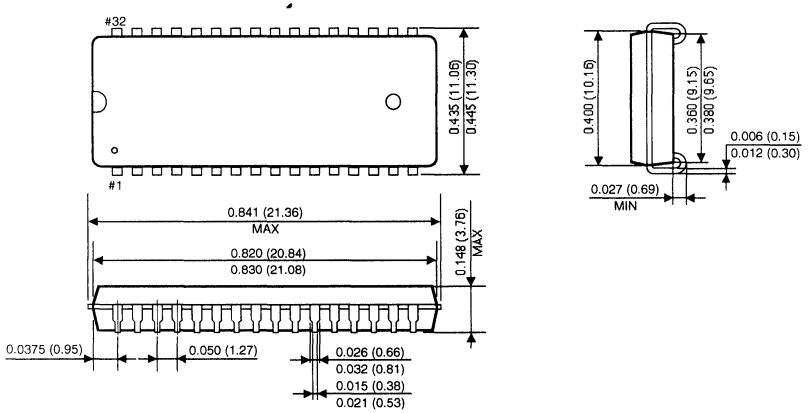
28 SOJ 300mil

Unit : Inches (millimeters)



32 SOJ 400 mil

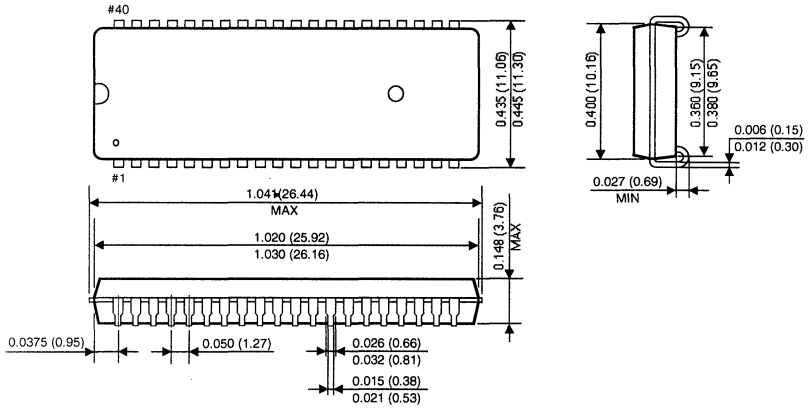
Unit : Inches (millimeters)



PLASTIC SMALL OUT-LINE J-LEAD

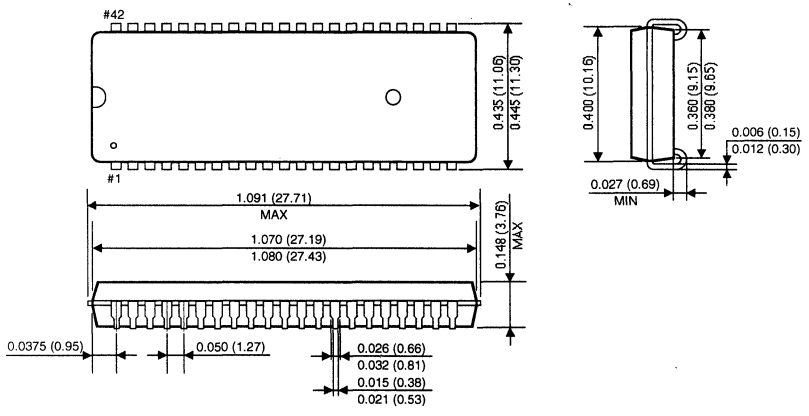
40SOJ 400 mil

Unit : Inches (millimeters)



42 SOJ 400 mil

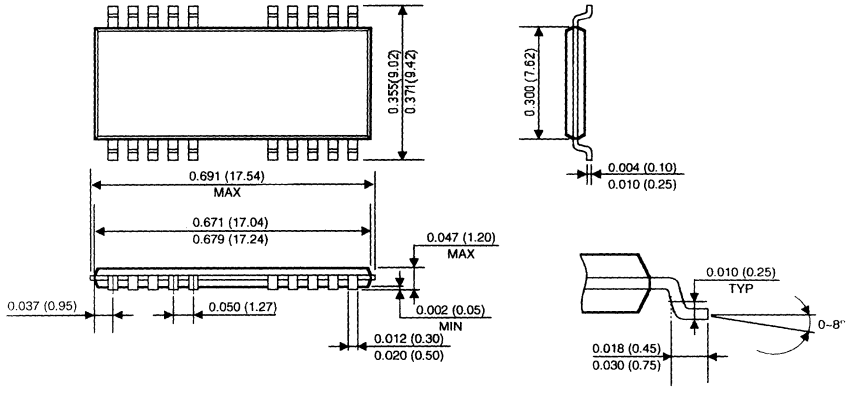
Unit : Inches (millimeters)



PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II)

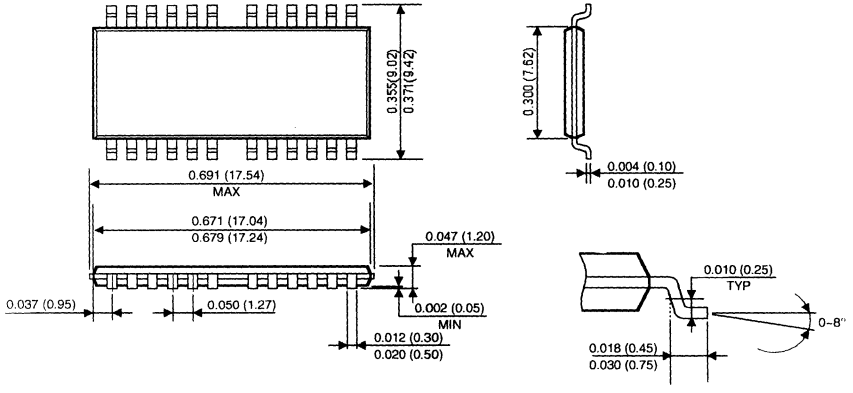
26(20) TSOP(II) 300 mil

Unit : Inches (millimeters)



26(24) TSOP(II) 300 mil

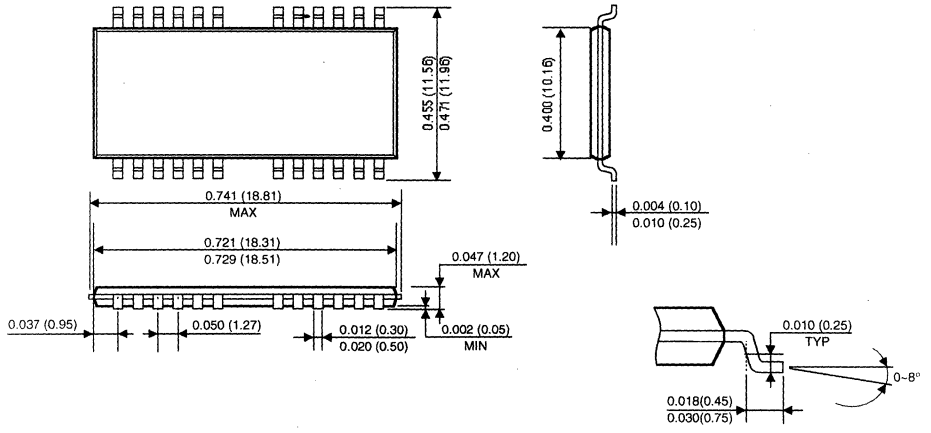
Unit : Inches (millimeters)



PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II)

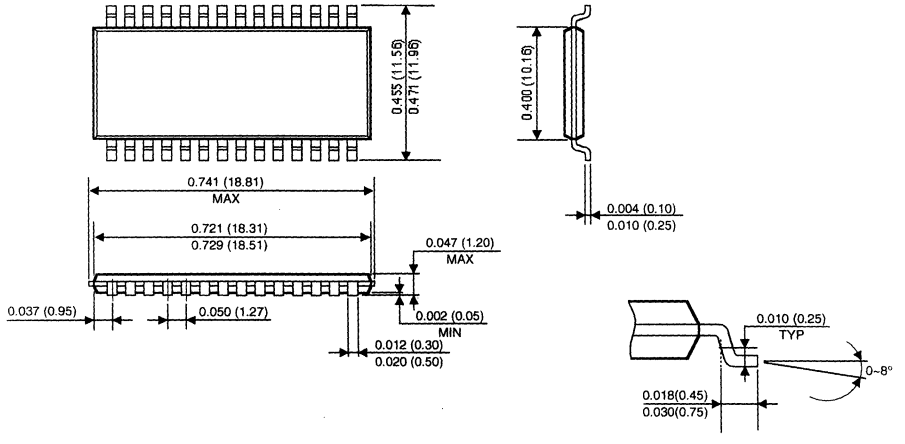
28(24) TSOP(II) 400 mil

Unit : Inches (millimeters)



28 TSOP(II) 400 mil

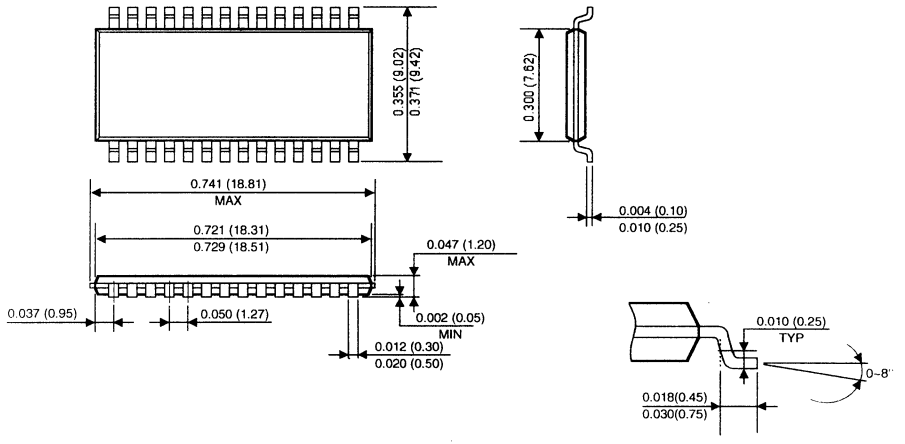
Unit : Inches (millimeters)



PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)

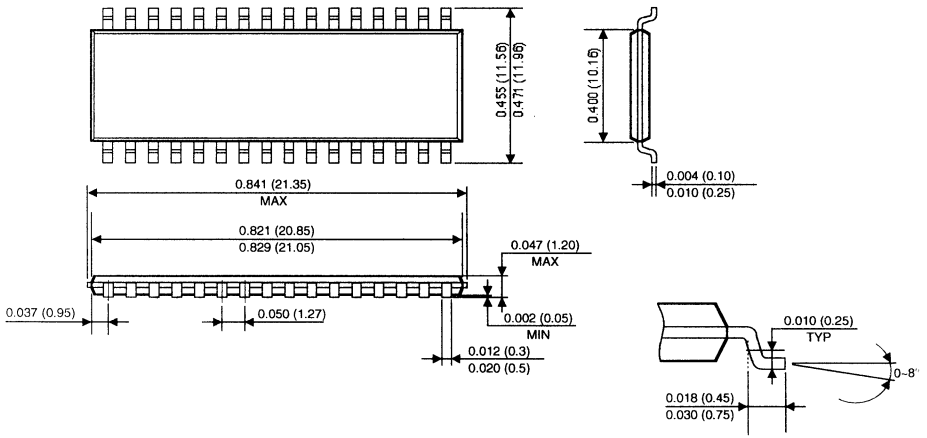
28 TSOP(II) 300mil

Unit : Inches (millimeters)



32 TSOP(II) 400 mil

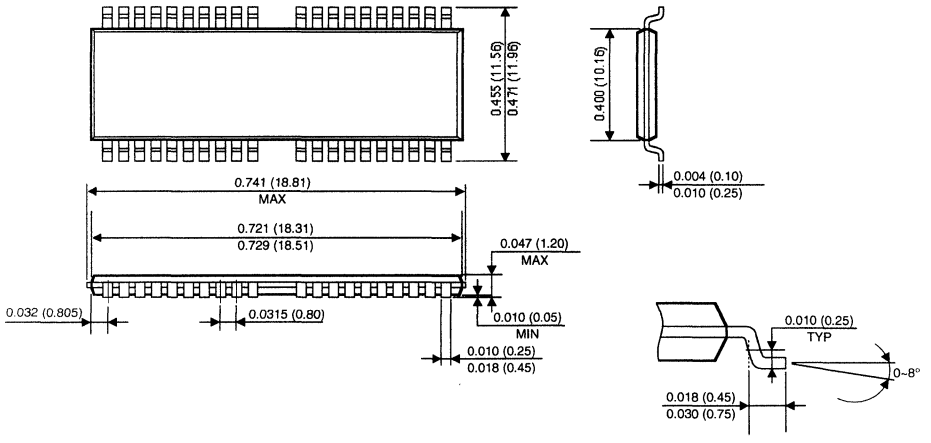
Unit : Inches (millimeters)



PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)

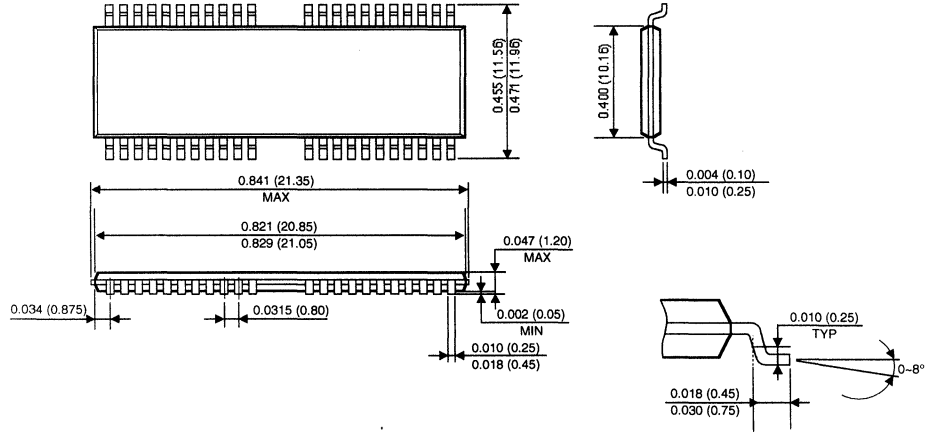
44(40) TSOP(II) 400 mil

Unit : Inches (millimeters)



50(44) TSOP(II) 400 mil

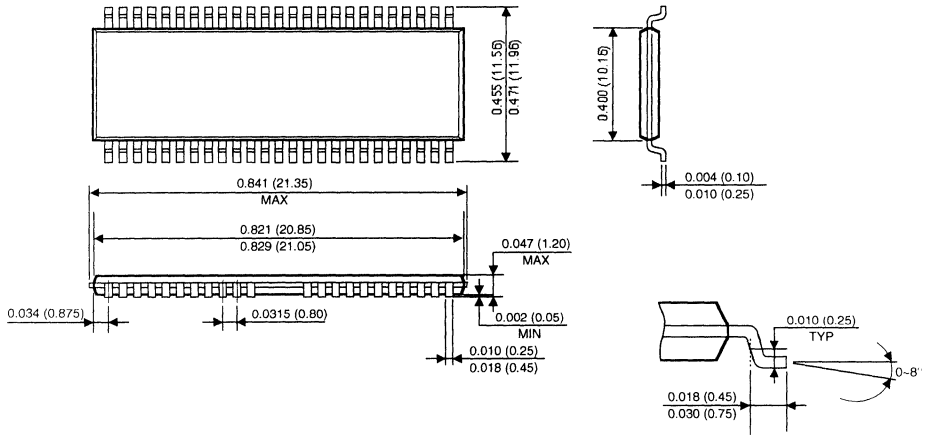
Unit : Inches (millimeters)



PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)

50 TSOP(II) 400 mil

Unit : Inches (millimeters)




5

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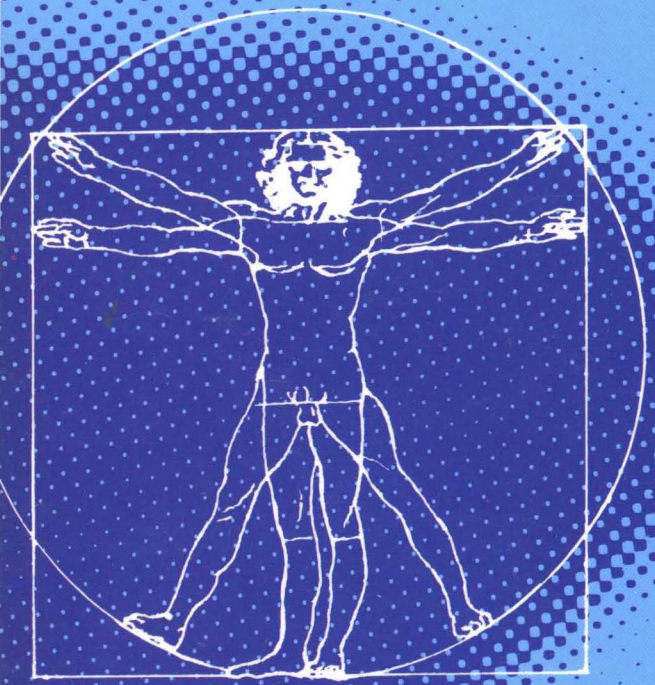

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