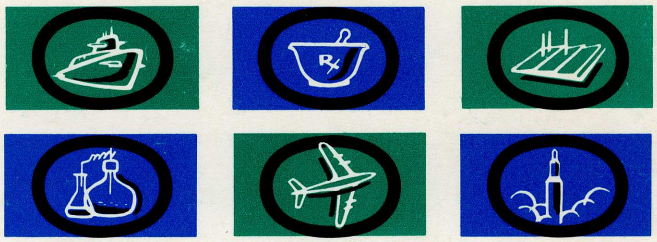
technical proposal

SEL 840
GENERAL PURPOSE
DIGITAL COMPUTER



SEL

systems engineering laboratories, incorporated

technical proposal

SEL Technical Proposal S-_____
Date _____

SEL 840
GENERAL PURPOSE
DIGITAL COMPUTER

REV 2-17-66

SEL SYSTEMS ENGINEERING LABORATORIES, INCORPORATED
P. O. BOX 9148 • FORT LAUDERDALE, FLA. 33310 • AREA CODE 305 587-2900

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1.0 INTRODUCTION

Systems Engineering Laboratories, Incorporated (SEL) is pleased to submit our Technical Proposal for an 840 Scientific Digital Computer.

SEL specializes in the design, development and fabrication of general-purpose digital data acquisition, processing and control systems and system components. Our firm has designed and fabricated numerous special-purpose wired program and stored program data processing systems. Application bulletins describing several of these are enclosed in the Appendix. Recently, SEL introduced a new series of high-speed integrated circuit general-purpose digital computers. These are designated as the SEL 810 and 840.

We propose the SEL 840 for your requirement, which is a high-speed general-purpose 24-bit binary computer. The single address instruction words utilize a 1.75 microsecond memory cycle time and parallel transfers to accomplish most of the 68 different instructions within 3.5 microseconds. This computer is well suited for use as a real time data processor, or as an off-line scientific or business computer. A FORTRAN IV compiler satisfying the latest ASA standards is available with the 840 provided the machine is ordered with 8K of memory (see Figure 1.0).

The SEL 840 is the most outstanding machine in its price range as shown by the following list of significant advantages:

1. All digital logic, silicon monolithic integrated circuits.

FIGURE 1.0

2. Hardware index register in basic system. No extra time required to index. (One index is standard in basic system; two additional index registers are available as options.)

3. All hardware required for two separate Input/Output channels in basic system.

4. Hardware multiply/divide is in the basic system.

5. Hardware instructions that allow Input/Output directly from core or via accumulator.

6. Six hundred nanosecond access time, 1.75 microseconds full cycle time.

7. Ninety instructions. (68 for Basic System, 22 for Extended Arithmetic Unit.)

8. Memory is expandable to 32,768 words, all directly addressable.

SEL is known throughout the industry as a true "systems" company. We produce all of the major components of any digital data system with the exception of the tape transports. SEL, however, produces the electronics for the transports. The following is a list of the system components manufactured by SEL. These are described in the Appendix of this proposal.

Analog-to-Digital Converters

Digital-to-Analog Converters

Low-Level Multiplexers

High Level Multiplexers

Magnetic Core Memories

Wide Band D. C. Instrumentation Amplifiers

Operational Amplifiers

Digital Logic Modules

Micrologic Modules

We have established Regional Sales Offices in Washington, D. C., Philadelphia, Boston and Los Angeles. The Area Managers in charge of these offices are qualified systems engineers who are always available to provide you with assistance. The names of these Area Managers, along with their addresses and telephone number are as follows:

Mr. George J. Burke
Area Manager
10400 Connecticut Avenue
Kensington, Maryland 27095
301-946-7100

Mr. James H Geers
Area Manager
885 N. San Antonio Road
Los Altos, California 94023
415-941-1185

Mr. Marvin L. Bunn
Area Manager
P. O. Box 1141
Huntsville, Alabama 35812
205-539-2181

Mr. William A. Gannon
Area Manager
P. O. Box 672
Framingham, Massachusetts 01701
617-879-0080

Mr. Karl R. Grice
Area Manager
637 North Park Avenue
Pomona, California 91767
714-623-5235

The performance and reliability of SEL systems may be verified by calling any of the contacts listed in the contracts completed and in the

progress document at the end of this section. This is a list of all SEL contracts, with the computer contracts listed on a separate page. We urge you to call these customers and verify the accuracy, performance and other characters of our products.

SEL CONTRACTS COMPLETED

Contract No.	Description	Customer	Technical Contact	Administrative Contact	Approximate Dollars
N62269-1453	Two Analog-to-Digital Converters	Naval Air Development Center, Johnsville, Pa.	H. Tremblay OS 5-7000	R. Harmon OS 5-7000	$ 15,000
DA44-177-TC-760	Two Digital Data Acquisition Systems	U.S. Army Transportation Research Command Fort Eustis, Virginia	W.M. Allen TR 7-1311	T. Domino TR 7-1131	80,000
BGP-458 (Now61-0647-U)	24-Channel Data Acquisition System	Hercules Powder Co. Magna, Utah	R. Wright OL 6-9811	R. Sawyer BY 7-5911	308,000
62-4-DESCS (AF40(600)800)	Data Translation System	ARO, Inc. Arnold Air Force Station, Tenn.	G. Sheraden GL 5-2611	J. Gary GL 5-2611	152,000
61-07970	Two Data Acquisition Systems	Thiokol Chemical Corp. Brigham City, Utah	D. Sherar AL 7-7111	C.R. Turner PA 3-3481	49,000
2-300067-7025	Three Digital Function Generators	Boeing Co., Aerospace Div., Seattle, Wash.	W. Munday CH 3-4222	R. Danell MA 3-7025	32,700
RS-79248	Digital Data Acquisition System	Thiokol Redstone Div. Huntsville, Alabama	J. Epps 876-9509	C. Duke 876-9475	65,000
Nonr3717(00)(X)	Digital Data Recording System & Card Tester	Naval Research Laboratory, Washington, D.C.	A.M. Knopp JO 3-6600	J. Somers (ONR) OX 6-2266	108,000
FSC 5820 (AF08(606)5229)	PCM Conversion System	USAF Missile Test Ctr. Patrick A.F.B., Fla.	E. Herrberger UL 7-2661	H.A. Brown UL 7-6920	56,000
N62306-1064	Airborne Data Recording System	Navy Oceanographic Office, Washington D.C.	W. Geddes RE 6-2700	Mrs. H. Bright RE 6-2700	35,000
LW-04073-1	Low Level Multiplexers for ROVER Program	Los Alamos Scientific Lab, Los Alamos, N.M.	D. Stephenson 7-5255	J.P. Harrison 7-4147	105,000
0216-0001-TK	Digital Data Acquisition System	Thiokol Chemical Co. Elkton, Maryland	D. Williamson EX 8-3000	T.A. King EX 8-3000	100,000
NAS 8-4609	High Speed Data Acquisition System	NASA Marshall SFC Huntsville, Alabama	J. Lucas 877-2152	W.L. Troupe 534-1678	94,500
NAS 3-2627	L-L Multiplexer & A/D Converter	NASA Lewis Res. Ctr. Cleveland, Ohio	R. Crowl 252-7700 Ext. 385	J. Cash 252-7700	27,000
97-6-X-78035	SEL Model ADC-1B A/D Converter	Westinghouse Elec. Corp. Pittsburgh, Penna.	James Belz CH 2-1500	R. Endean 391-2800	7,500
NAS 8-5032	Digital Data Acquisition System	NASA Marshall SFC Huntsville, Alabama	R. Brouns 876-1403	L. Wilkins 534-1678	80,000
NAS 5-2706	SEL A/D Converter & L-L Multiplexer	NASA Goddard SFC Hyattsville, Maryland	W. Stallings 474-9000 Ext. 4459	L. Purschwitz 982-4161	16,000
PO62-04973	High Level Data Acquisition System	Thiokol, Wasatch Div. Brigham City, Utah	D. Sherar AL 7-7111	C.R. Turner PA 3-3481	34,000
AM3-211528	One SEL Low-Level Multiplexer	Jet Propulsion Laboratory Pasadena, Calif.	R. Purves 790-6811	W.A. Frohn 790-6811	16,000
SC 168334	Digital Data Processor Set for POLARIS and Satellite Programs	Applied Physics Lab The John Hopkins Univ. Silver Spring, Maryland	A. Town 776-7100 Ext. 2243	C. H. Walters JU 9-7700 Ext. 785	340,000
NAS 1-1770	Analog-to-Digital Transcriber	NASA Langley Res. Ctr. Hampton, Virginia	L. Taylor 722-7961	J. Stowers 722-7961	216,000

SEL CONTRACTS COMPLETED (Continued)

Contract No.	Description	Customer	Technical Contact	Administrative Contact	Approximate Dollars
NAS 1-1900	High Speed Digital Data Recording System	NASA Langley Research Center, Langley Station Hampton, Virginia	C. Russell 722-7961 Ext. 4616	W. Simmons 722-7961 Ext. 3303	200,000
NAS 1-2088	H.S. Digital Data Recording System	NASA Langley Research Center, Langley Station Hampton, Virginia	C. Russell 722-7961 Ext. 4616	J. Munick 722-7961 Ext. 2024	140,000
NAS 8-7000	Direct Computer Entry System	NASA Marshall Space Flight Center Huntsville, Alabama	Frank Hay 877-2151	W.C. Vaughn 534-6404	60,000
PO 167191	Low Level Data Acquisition System	Pratt & Whitney Aircraft W. Palm Beach, Florida	Wm. Missimer VI 4-7311 Ext. 8383	F.D. Burk VI 4-7311 Ext. 2332	160,000
NAS 8-7018	150 Operational Amplifiers	NASA Marshall Space Flight Center Huntsville, Alabama	Gene Lee 877-2151	W.C. Vaughn 534-6404	57,000
PO 6-803590	300-Channel Low Level Data Acqsn. System	Allison Division, GMC Indianapolis, Indiana	Karl Wacker CH 4-1511	F.C. Cassell CH 4-1511	160,000
PO976X5102	5 Analog-to-Digital Converters	Westinghouse Electric Pittsburgh, Penna.	James Belz CH 2-1500	R.J. Endean 391-2800	30,700
PO 47511	Data Acquisition System	University of Florida Gainesville, Fla.	Dr. R. Uhrig FR 6-3261 Ext. 2271	T.N. Wells FR 6-3261	36,000
NAS 8-4496	Two Data Acquisition Systems	NASA Marshall SFC Huntsville, Alabama	W. Baker 876-3794	G.Troupe 534-1678	230,000
97-6-X-85555	One A/D Converter (less register)	Westinghouse Electric Pittsburgh, Penna.	James Belz CH 2-1500	R.J. Endean 391-2800	7,000
97-6-X-91415	Five A/D Converters	Westinghouse Electric Pittsburgh, Penna.	James Belz CH 2-1500	R.J. Endean 291-2800	31,000
NAS 8-5100	Telemetry Ground Station Digitzg. Sys.	NASA Marshall SFC Huntsville, Alabama	J. Eichelberger 876-7910	W.L. Troupe 534-7315	70,000
NAS 8-7062	High Density Tape Error Checker	NASA Marshall SFC Huntsville, Alabama	J. Lucas 877-2152	W. Troupe 534-7315	14,000
NAS 3-2977	Format Control Unit & Integration of Units	NASA Lewis Res. Ctr. Cleveland, Ohio	C. Mealey 216-252-7700 Ext. 353	P. Pirko 216-252-7700 Ext. 532	29,500
NAS 3-3151	One Multiplexer Three D/A Converters	NASA Lewis Res. Ctr. Cleveland, Ohio	C. Mealey 216-252-7700 Ext. 353	P. Pirko 216-252-7700 Ext. 532	23,000
PO 3X-14304	One Coder and One High Level Multiplexer	ARO, Inc. Tullahoma, Tenn.	W. R. Prater 615-GL 5-2611 Ext. 584	C. Solomon 615-GL 5-2611 Ext. 7113	16,000
NAS 8-8043	Digital Data Acqsn. System	NASA, Marshall Space Flight Center Huntsville, Alabama	J. Heaman 205-876-7227	W.L. Troupe 534-7315	58,300
PO 370391	48-Channel Digital Data Acqsn. System	Marquardt Corporation Van Nuys, California	G.B. Kubicek ST 1-2121 Ext. 1281	J. Nugent ST 1-2121 Ext. 1553	78,000
NAS 10-780	Analog High Level Multiplexer	NASA, Cape LOC Cocoa Beach, Florida	R. Bivans UL 3-3362	Mr. Mazzanoble 783-7709	12,000

SEL CONTRACTS COMPLETED (Continued)

Contract No.	Description	Customer	Technical Contact	Administrative Contact	Approximate Dollars
NAS 3-4653	Tape Search Unit	NASA, Lewis Res. Ctr. Cleveland, Ohio	R. Crowl 216-252-7700 Ext. 225	P. Pirko 216-252-7700 Ext. 532	$ 7,400
SC63-34-RTF-T	Low-Level Data Acquisition System	ARO, Inc. Tullahoma, Tenn.	J. D. Freeman 615-GL 5-2611	C. Solomon 615-GL 5-2611	111,000
NAS 8-7394	Data Acquisition System	NASA, Marshall Space Flight Center Huntsville, Alabama	B. Henson 877-2590	M. W. Moore	130,000
NAS 8-5461	Digital Tape Writing Station	NASA, Marshall Space Flight Center Huntsville, Alabama	R. Eichelberger 205-876-5275	J. Sanford 205-539-4233	45,000
PO 63-03987 (AF33(600)34468)	Tape to Tape Translator	Thiokol Chem. Corp. Wasatch Division Brigham City, Utah	Gene Davis 801-863-3511	L. B. Pyper 801-863-3511 Ext. 63287	112,000
NAS 9-1845	Two Low-Level Data Acquisition Systems	NASA, Manned Space-craft Center Houston, Texas	J. Lowery 713-928-2811 Ext. 2565	J. Stroup 713-928-2811 Ext. 3611	195,000
PON-691504D	Low-Level Data Acquisition System	Martin Company Orlando, Florida	B. Wigle 305-855-6100 Ext. 2396	J. T. Brady 305-855-6100 Ext. 2265	70,000
M3J7XA-700,007	800-Channel Data Acquisition and Processing System	North American Avia. Downey, California	D. E. Herbst 213-923-8141 Ext. 6161	S. Ramage 213-639-7870 Ext. 1635 (Montebello, Calif.)	800,000
PO SB 0387	100-Channel Data Acquisition System	Thiokol Chemical Corp. Space Booster Plant Brunswick, Georgia	E. L. Checketts 912-265-0180 Ext. 315	Douglas Bell 912-265-0180 Ext. 378	275,000
NAS 9-2189	Portable Low-Level Data Acquisition System	NASA Manned Space-craft Center Houston, Texas	R. J. Sachen 713-928-2811 Ext. 2475	R. P. Clyatt 713-928-2811 Ext. 7311	105,000
PO 72511	Compressor Data Acquisition System	Texas Gas Trans. Corp. Owensboro, Kentucky	C. McCulley 502-MU 3-2431	P. Fedde 502-MU 3-2421 Ext. 452	19,000
PO 470518	96-Channel Digital Data Recording System	Marquart Corporation Van Nuys, California	M. Feffer 781-2121 Ext. 1217	J. Nugent 781-2121 Ext. 1217	75,000
NAS 8-8864	150 Operational Amplifiers	NASA Marshall Space Flight Center, Huntsville, Alabama	Gene Lee 205-877-2151	W. L. Troupe 205-534-4586	57,000
PO 34X6853	10 Analog-to-Digital Converters with SEL Amplifiers Included	Westinghouse Electric Pittsburgh, Penna.	J. McCann 412-242-1500 Ext. 7628	R. J. Endean 412-391-2800 Ext. 7471	65,000
NAS 8-8179	Telemetry Data Analysis Equipment	NASA Marshall Space Flight Center, Huntsville, Alabama	R. Eichelberger 205-876-5275	W. L. Troupe 205-534-7315	330,000
NAS 1-4272	System Verifier	NASA Langley Research Center, Langley Station Hampton, Virginia	C. Russell 722-7961 Ext. 4616	W. E. Hutcheson 703-722-7961	19,000
PH 108-64-14 (P)	MOBIDAC 1	U.S. Public Health Ser. Bureau of State Services Washington, D.C.	Dr. B. H. Fox 202-962-8092	Miss M. Porter 202-962-8092	18,000

SEL CONTRACTS CONTRACTS COMPLETED
(Continued)

Contract No.	Description	Customer	Technical Contact	Administrative Contract	Approximate Dollars
NAS 3-5195	400 Channel and 200 Channel Facility Sub-Systems	NASA - Lewis Res. Ctr. Cleveland, Ohio	C. Mealey 216-252-7700 Ext. 353	M. Kapral 216-252-7700 Ext. 550	$280,000
N62306-1473	Modification & Expansion of Airborne Digital Data Recording System	U.S. Naval Oceanograph, Washington, D.C.	F. Dorsey RE 6-2700 Ext. 543	H. Crain RE 6-2700	20,000
NAS 8-12259	130 Operational Amplifiers	NASA - Marshall Space Flight Center, Huntsville Alabama	J. Lewis 205-876-7233	P. Clancy 205-876-7233	50,000
NAS 3-3735	Two Digital Data Logging Systems	NASA - Lewis Res. Ctr. Cleveland, Ohio	C. Mealey 216-252-7700 Ext. 353	M. Kapral 216-252-7700 Ext. 550	610,000
NAS 3-4514	Two Multiplexers	NASA - Lewis Res. Ctr. Cleveland, Ohio	R. Crowl 216-252-7700 Ext. 225	M. Kapral 216-252-7700 Ext. 550	23,000
NAS 1-3506	High Speed Digital Recording System	NASA - Langley Res. Ctr. Langley Station Hampton, Virginia	C. Russell 703-722-7961 Ext. 4616	J. Munick 703-722-7961 Ext. 2024	170,000
L-011298-7030	Four Telemetry Digitizing Systems	Boeing Aerospace Division, Huntsville Alabama	R. Anfield 205-536-4461	W.G. Dooley 205-536-4461	260,000
NAS 8-12645	1 Digital Tape Playback System	NASA - Marshall Space Flight Center Huntsville, Alabama	F. Hay 205-877-2151	W. L. Troupe 205-534-4586	15,000
NAS 3-6145-PB	5-Channels of Digital-to-Analog Converters	NASA - Plum Brook Station, Sandusky, Ohio	R. Reust 419-625-1123 Ext. 434	R. J. Koch 216-433-4000	10,000
PO 34-X-8676	5 Analog-to-Digital Converters	Westinghouse Electric Corporation Pittsburgh, Pa.	J. McCann 412-242-1500 Ext. 7628	R. J. Endean 412-391-2800 Ext. 7471	33,000
PO 504-477	3 14-Channel Consoles Hydrostatic Data Acquisition Systems	Sundstrand Hydrostatic Rockford, Illinois	C. J. Ricketts 815-962-4477	A. K. Nuckles 815-962-4477	45,000
PO 34-X-5782	2 Analog-to-Digital Converters without Amplifiers	Westinghouse Electric Corporation Pittsburgh, Pa.	J. McCann 412-242-1500 Ext. 7628	R. J. Endean 412-391-2800 Ext. 7471	12,000
NAS 8-12991	Digital-to-Analog Conversion System	NASA - Marshall Space Flight Center Huntsville, Alabama	B. Broad 205-876-6344	J. Grosser 205-539-2410	31,000
DA04353 ENG-9009	High Speed Digital Data Acquisition System	F & M Systems Company Dallas, Texas	W. T. Russell 214-428-1573	K. Bishop 214-428-1573	73,000
NAS 8-11702	Telemetry Digitizing System	Lockheed Aircraft Service Company Ontario, California	E. Young 714-984-1234	F. Tade 714-984-1234	55,000
PO L-24959-6010	2 SEL Model 2051-SIM Systems	The Boeing Company New Orleans, La.	Mr. Ushakoff 504-255-3311	H. Reardon 504-255-8134	1,700
NOw 61-0647-u	Auxillary Control Panel	Hercules Powder Co. Magna, Utah	D. Carroll 801-297-5911	R. W. Wright 801-297-5911	1,300

SEL CONTRACTS COMPLETED (Continued)

Contract No.	Description	Customer	Technical Contact	Administrative Contact	Approximate Dollars
PO 240674	MOBIDAC III	Pratt and Whitney West Palm Beach, Fla.	W. Missimer 844-7311 Ext. 8383	C. R. Brooks (144) 844-7311 Ext. 2426	$50,000
NAS 8-13906	Precision Oscillator	NASA Marshall Space Flight Center Huntsville, Alabama	G. Lee 205-877-2151	D. McCreless 205-534-6405	34,000
NAS 8-11654	Telemetry Digitizing System	NASA Marshall Space Flight Center Huntsville, Alabama	J. Rees 205-876-6445	D. D. Firestone 205-539-2795	80,000
AT(29-1)-1183	537-Channel Digital Data System	Edgerton, Germeshausen and Grier, Incorporated Boston 15, Massachusetts	K. Foster 617-271-5131 (Bedford, Mass.)	H. R. Silver 617-267-9700 Boston, Mass.	421,000
NAS 8-12646	Airborne Link Data Simulator	NASA - Marshall Space Flight Center Huntsville, Alabama	F. Hay 205-877-2151	W. L. Troupe 205-534-4586	50,000
NAS 9-3071	High Speed Analog-to-Digital Data Acquisition System	NASA Manned Spacecraft Center, Houston, Texas	M. Oberschmidt 713-483-7678	S. R. Nevin 713-928-2811	130,000
AF 04(611)-10221	3 Digital Data Recording Systems and 2 Patch-board Systems	Edwards Air Force Base California	W. Severin 714-762-5161 Ext. 82-7111	Mrs. G. M. Plock 805-258-2111 Ext. 3-3441 Mojave, California	365,000
NAS 3-6516-PB	Central Timing System and Remote Timing System	NASA Lewis Research Center; Cleveland, Ohio	J. Harrold 419-625-1123 Ext. 533	R. J. Koch 216-433-4000	49,000
PO NA 256396	1 Model 9029 Analog-to-Digital Converter	The Boeing Company Morton, Pennsylvania	F. Wilson 215-522-3950	C. B. Craskey 215-522-3950	20,000
PO 337050	SEL 700 Data Processor	Grumman Aircraft Engineering Corp., Bethpage, New York	R. LeCann 516-575-1896	F. Bolda 516-575-0574 Ext. 2115	113,000
NAS 8-13852	Modulated Digital-to-Analog Converter System	NASA Marshall Space Flight Center Huntsville, Alabama	P. D. Belton 205-877-2151	W. C. Vaughn 205-534-7315	58,000
PO L-024529-7030	One Telemetry Digitizing System	The Boeing Company Huntsville, Alabama	R. Anfield 205-536-4461	R. T. Meyer 205-842-2304	55,000
PO 17887965	High Level Multiplexer	Naval Weapons Laboratory Dahlgren, Virginia	T. H. Tharp 703-663-2511	J. J. Hanzel 703-663-2511	3,000
NAS9-3195	Two Low Level Analog-to-Digital Converters	NASA Manned Space-craft Center Houston, Texas	H. J. Lowery 713-928-2811 Ext. 2565	J. L. Vyner 713-483-5521	173,000
NAS8-13851	Digital Data Acquisition System	NASA Marshall Space Flight Center Huntsville, Alabama	J. C. Duffey 205-876-4132	W C. Vaughn 205-534-6404	122,000
NAS8-14436	PB Buffer	NASA Marshall Space Flight Center Huntsville, Alabama	P. D Belton 205-877-2151	D. McCreless 205-534-6405	30,000
C-530-62A-PB	Remote Display & Channel Selector	NASA Plum Brook Station Sandusky, Ohio	J Harrold 419-625-1123	A Grabach 419-625-1123 Ext. 331	3,000

SEL CONTRACTS COMPLETED (Continued)

Contract No.	Description	Customer	Technical Contact	Administrative Contact	Approximate Dollars
NAS 9-3626	200-Channel Digital Data Acquisition	NASA - Manned Spacecraft Center, Houston, Texas	R. Bozeman 713-483-4991	J. Vyner 713-483-5521	42,000
NAS 3-6941PB	200-Channel Sub-System	NASA - Lewis Research Center Cleveland, Ohio	J. Harrold 419-625-1123 Ext. 533	R. J. Koch 216-433-4000	85,000
AF 08(635)4825	Data Acquisition System	Eglin Air Force Base Florida	J. Himes 305-881-6668 Ext. 67-3314	Mrs. C. Hudgins 305-881-6668	82,000
NAS 8-13619	High Speed Data Acquisition System	NASA - MSFC Huntsville, Alabama	J. Heaman 205-876-7227	D. Hall 205-534-4586	110,000
SN PN 565 CTA 155	Eight Multiplexers	Pan American World Airways, Inc. Las Vegas, Nevada	D. Brindenstein 702-986-5357	J. G. McGuffin 702-735-9182	90,000
28X7563	Two Analog-to-Digital Converters with Amplifier	Westinghouse Corp. Pittsburgh, Pa.	R. Squires 412-391-2800	R. Endean 412-391-2800 Ext. 7471	18,000
LZ238051	MOBIDAC IV	Los Alamos Scientific Lab. Los Alamos, New Mexico	T. Springer 505-066-82526	J. N. Halliday 505-066-75084	40,000
16678	Digital Data Acquisition & Logging System	Brown University Providence, R. I.	B. W. Costerus 401-861-2900	R. L. Crowley 401-861-2900	28,200
NAS 8-11911	Modulated Digital to Analog Converter	NASA - MSFC Huntsville, Alabama	P. D. Belton 205-877-2151	W. L. Troupe 205-534-7315	60,000
NAS 8-11911	Data Link	NASA - MSFC Huntsville, Alabama	P. D. Belton 205-877-2151	W. L. Troupe 205-534-7315	40,000
NAS 8-11911	Real Time Entry	NASA - MSFC Huntsville, Alabama	F. Hay 205-877-2151	W. L. Troupe 205-534-7315	45,000
541-11418	Low Level 48-Channel Multiplexer	ARO, Inc. Arnold AFS Tennessee	W. N. Brock 615-GL 5-2611	C. Solomon 615-GL 5-2611 Ext. 7113	20,000
NAS 8-11584	Two Navigation System Test Stations	NASA - MSFC Huntsville, Alabama	J. Mitchell 205-876-4413	D. Marshall 205-539-0617	270 000
PO 60111	Digital Data Acquisition System	Brown Engineering Co. Huntsville, Alabama	B. Goldman 205-532-1221	G. Sharpe 205-532-1221	120.000
NAS 1-5151	Adding 20 Channels	NASA - Langley Research Center Hampton, Va.	L. E. Taylor 703-722-7961 Ext. 4851	W. T. Quinn 703-722-7961 Ext. 4410	20,000
NAS 3-6514	800-Channel Data Acquisition System	NASA Lewis Research Center; Cleveland, Ohio	C. Mealey 216-433-4000 Ext. 356	M. Kapral 216-433-4000 Ext. 356	545,000
J-30441, C-4	Sub-System # 2	Edgerton, Germeshausen and Grier, Incorporated Boston 15, Massachusetts	K. J. Foster 617-271-5131 (Bedford, Mass.)	H. R. Silver 617-267-9700	133,000
NAS 1-5404	Multiplexed Encoder	NASA Langley Research Center, Hampton, Virginia	J. Harrell 703-722-7961	J. Dorst 703-722-7961 Ext. 4414	25,000
NAS 1-5437	System Calibrator	NASA Langley Research Center, Hampton, Virginia	M. Limburg 703-722-7961	J. Leo 703-722-7961 Ext. 4683	10,000
230602	Count Down Timers	Applied Physics Lab Johns Hopkins Univ. Silver Spring, Md.	R. Mack 202-545-6700	C. Walters 301-589-7700 Ext. 330	35,000

SEL CONTRACTS COMPLETED (Continued)

Contract No.	Description	Customer	Technical Contact	Administrative Contact	Approximate Dollars
NAS 8-20021	Telemetry Measuring System (Rees #2)	NASA - MSFC Huntsville, Alabama	L. Etheredge 205-876-6143	J. McMurry 205-842-3597	$ 95,000
NAS 8-16371	Anelex Printer	NASA - MSFC Huntsville, Alabama	F. Hay 205-877-2151	J. Barker 205-842-3187	30,000
NAS 8-17451	Priority Interrupts	NASA - MSFC Huntsville, Alabama	F. Hay 205-877-2151	T. Johnson 205-842-3146	10,560
NAS 8-11841	High Speed Data Acquisition System	NASA - MSFC Huntsville, Alabama	F. Hay 205-877-2151	P. B. Higdon 205-539-2796	940,000
337050	SEL 700 Data Processor	Grumman Aircraft Engineering Corp. Bethpage, N. Y.	R. LeCann 516-575-1896	F. Bolda 516-575-0574 Ext. 2115	125,000
230582	SEL 840 Computer	Applied Physics Lab. Johns Hopkins Univ. Silver Spring, Md.	J. W. Jenkins 301-589-7700 Ext. 284	C. Walters 301-589-7700 Ext. 330	280,000
NAS 8-15388	2nd Plotter Interface	NASA - MSFC Huntsville, Alabama	F. Hay 205-877-2151	K. Harrell 205-842-2155	120,000
NAS 8-16365	Digital Data Acquisition System	NASA - MSFC Huntsville, Alabama	J. Heaman 205-876-7227	J. Barker 205-842-3187	75,000
NAS 3-8439-PB	Remote Display	NASA - Lewis Research Center - Plum Brook Sta. Sandusky, Ohio	J. Harrold 419-625-1123	A. Grabach 419-625-1123 Ext. 206	5,000
NAS 8-17034	Two Input Simulators	NASA - MSFC Huntsville, Alabama	B. Adair 205-876-2668	T. Johnson 205-842-3146	15,000

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SEL CONTRACTS IN PROGRESS

Contract No.	Description	Customer	Technical Contact	Administrative Contact	Approximate Dollars
NAS 8-13874	Vehicle Instrumentation Simulator	NASA - MSFC Huntsville, Alabama	W. W. Watts 205-876-0713	W. C. Vaughn 205-534-7315	$180,000
163730	SEL 810 Computer Controlled Locomotive Metering System	General Motors Corp. Electro-Motive Division La Grange, Illinois	G. E. Harper 312-485-7000	A. J. Purok 312-485-7000	100,000
167633	SEL 810 Computer Controlled High Voltage Cabinet Test System	General Motors Corp. La Grange, Illinois	H. E. Quinn 312-485-7000	D. J. Gothard 312-485-7000	260,000
DM75846	Data Acquisition System	General Motors Corp. Detroit Diesel Division Detroit, Michigan	R. Wellington 313-531-7100	W. Fogarty 313-539-5000	370,000
9802	Datatally Electronic Estimating Devices	Datatype Corporation Hialeah, Florida	M. Zappia 696-3832	W. Runnstrom 696-3832	25,000
NAS 8-15998	ASR-33 IBM Selectric	NASA - MSFC Huntsville, Alabama	F. Hay 205-877-2151	J. Barker 205-842-3187	5,000
NAS 8-14427	Telemetry Measuring System	NASA - MSFC Huntsville, Alabama	J. Toney 205-877-2444	D. McCreless 205-534-6405	140,000
NAS 8-11911	Plotter Interface System	NASA - MSFC Huntsville, Alabama	F. Hay 205-877-2151	W. Troupe 205-534-7315	80,000
NAS 8-16552	Digital Data Acquisition System	NASA - MSFC Huntsville, Alabama	J. Heaman 205-876-7227	T. Johnson 205-842-3146	50,000
DA-28-043-AMC-0-1606-	Stored Program Analog-to-Digital Tape Formatting System	U. S. Army White Sands Missile Range, New Mexico	S. Scott 915-678-1923	G. Tucker 201-535-2428 (New Jersey)	220,000
A2351S	Computer Simulation Systems	Melpar, Inc. Falls Church, Va.	F. E. Pappin 703-534-6000	D. Oglesby 703-534-6000	160,000
Withheld	SEL 810 Computer	Withheld by Request	Withheld	Withheld	95,000
NAS 9-5092	Data Acquisition System with SEL 840	NASA - MSC Houston, Texas	R. Sachen 713-928-2811	D. Humes 713-928-2811	155,000
L-036535-	Central Control System	Boeing Company Huntsville, Alabama	P. Thiel 205-539-8371	R. Meyer 205-842-2304	240,000
DA18-119-AMC 02765(X)	SEL 810 Computer	Procurement Division Fort George Meade Maryland	D. Albert	W. Clark	75,000
NAS 4-956	1200 Channel Digital Data Acquisition System	NASA - Edwards Air Force Base California	K. Anderson 805-258-3311	W. Taliaferro 805-258-3311 Ext. 301	520,000
NAS 8-16455	Digital Flow Converter	NASA - MSFC Huntsville, Alabama	J. Duffy 205-876-4132	R. Culbreth 205-842-2201	140,000
6-345424	16 Channel Multiplexer	Bell Telephone Labs. Burlington, N. C.	J. Hahn 919-228-7811	J. F. Cox 201-887-1000	45,000
6-601455	16 Channel D/A Converter	Bell Telephone Labs. Burlington, N. C.	J. Hahn 919-228-7811	A. Petersen 201-887-1000 Ext. 3374	8,000

SEL CONTRACTS IN PROGRESS (Continued)

Contract No.	Description	Customer	Technical Contact	Administrative Contact	Approximate Dollars
A36125S	SEL 810 Computers	Melpar, Inc. Falls Church, Va.	F. E. Pappin 703-534-6000	D. Oglesby 703-534-6000	225, 000
NAS 9-5562	Boundary Control Unit	NASA - MSC Houston, Texas	R. Bozeman 713-483-4991	T. McPhillips 713-483-4991	8, 000
NAS 1-5848	Real Time ID and Logging System	NASA - Langley Hampton, Virginia	C. Bryant 703-722-7961 Ext. 3483	W. Quinn 703-722-7961 Ext. 4410	70, 000
MD509180	Process Control Oriented DAS	General Motors Corp. Mfg. Develop. Center Warren, Michigan	D. Larson 313-539-5000 Ext. 5081	J. Burgin 313-539-5000	105, 000
E-21513	Digital Controller System	Hamilton Standard Windsor Locks, Conn.	J. Woloszynski 203-623-1621 Ext. 2291	R. Eckelman 203-623-1621	145, 000
FNP-49163	SEL 810	General Motors Corp. AC Electronics Div. Milwaukee, Wisconsin	R. Wagner 414-762-7000	A. Gray 414-762-7000	45, 000
N0016366 C0234	Digital Data Recording System	U. S. Naval Avionics Indianapolis, Indiana	J. Carr 317-357-8311	M. Dooley 317-357-8311 Ext. 549	30, 000

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SEL COMPUTER CONTRACTS

SEL 810

Customer	Contract No.	Description	Customer Engineer
NASA - QUAL Div Huntsville, Alabama	NAS 8-13874	Simulator	W. Watts
GM - Electro-Motive Div. LaGrange, Illinois	P.O. 163730	High Voltage Cabinet Test System	H. Quinn
NASA - ASTR Div. Huntsville, Alabama	NAS 8-11911	Plotting System	F. Hay
NASA - QUAL Div. Huntsville, Alabama	NAS 8-20021	Telemetry Digitizing System	J. Rees
GM - Electro-Motive Div. LaGrange, Illinois	P.O. 163733	Metering System	G. Harper
NASA - ASTR Div. Huntsville, Alabama	NAS 8-15388	Plotting System Number 2	F. Hay
GM - Detroit Diesel Detroit, Michigan	DM75846	Data Acquisition System	R. Wellington
White Sands Missile Range, New Mexico	DA-28-043-AMC 0-1606-CE	Stored Program A/D Tape Formatting System	S. Scott
Melpar, Inc. Falls Church, Va.	A24515	Two Computer Simulation Systems	F.E. Pappin
Withheld by Request	Withheld by Request	Direct Digital Control System	Withheld by Request
Boeing Company Huntsville, Alabama	L-036535-7022	Central Control System	P. Thiel
NASA, GSE Br. Huntsville, Alabama	NAS 8-16455	Digital Flow Converter	J.E. Duffy
NASA Edwards, California	NAS 4-956	1200 Ch. DAS	K. Anderson
Procurement Div. Ft. Geo. G. Mead, Md.	DA18-119-AMC- 02765(X)	810 Computer	D. Albert
Melpar, Inc. Falls Church, Va.	A36125S	3 810 Computers	F. E. Pappin
GM - Technical Center Warren, Michigan	MD509180	Process Control Oriented DAS	D. Larson
Hamilton Standard Windsor Locks, Conn.	E-21513	Digital Controlling System	J. Wołoszynski
GM - AC Electronics Milwaukee, Wisconsin	FNP-49163	SEL 810	R. Wagner
NASA - ASTR Div Huntsville, Alabama	NAS 8-14427	Telemetry Measuring System	J. Toney
Phillips Petroleum Bartlesville, Oklahoma	102709G	SEL 810	R.E. Garrison

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SEL COMPUTER CONTRACTS

SEL 840

Customer	Contract No.	Description	Customer Engineer
NASA - ASTR Division Huntsville, Alabama	NAS 8-11841	Fourier Processing System	F. Hay
Johns Hopkins University Silver Spring, Maryland	230582	Modification to Polaris Data Processor	J. Jenkins
NASA, MSC Houston, Texas	NAS 9-5092	Data Conversion System	R. Sachen
Mass. Inst. of Technology Lexington, Massachusetts	BB-242	SEL 840	F.E. Heart

2.0 SEL 840 COMPUTER

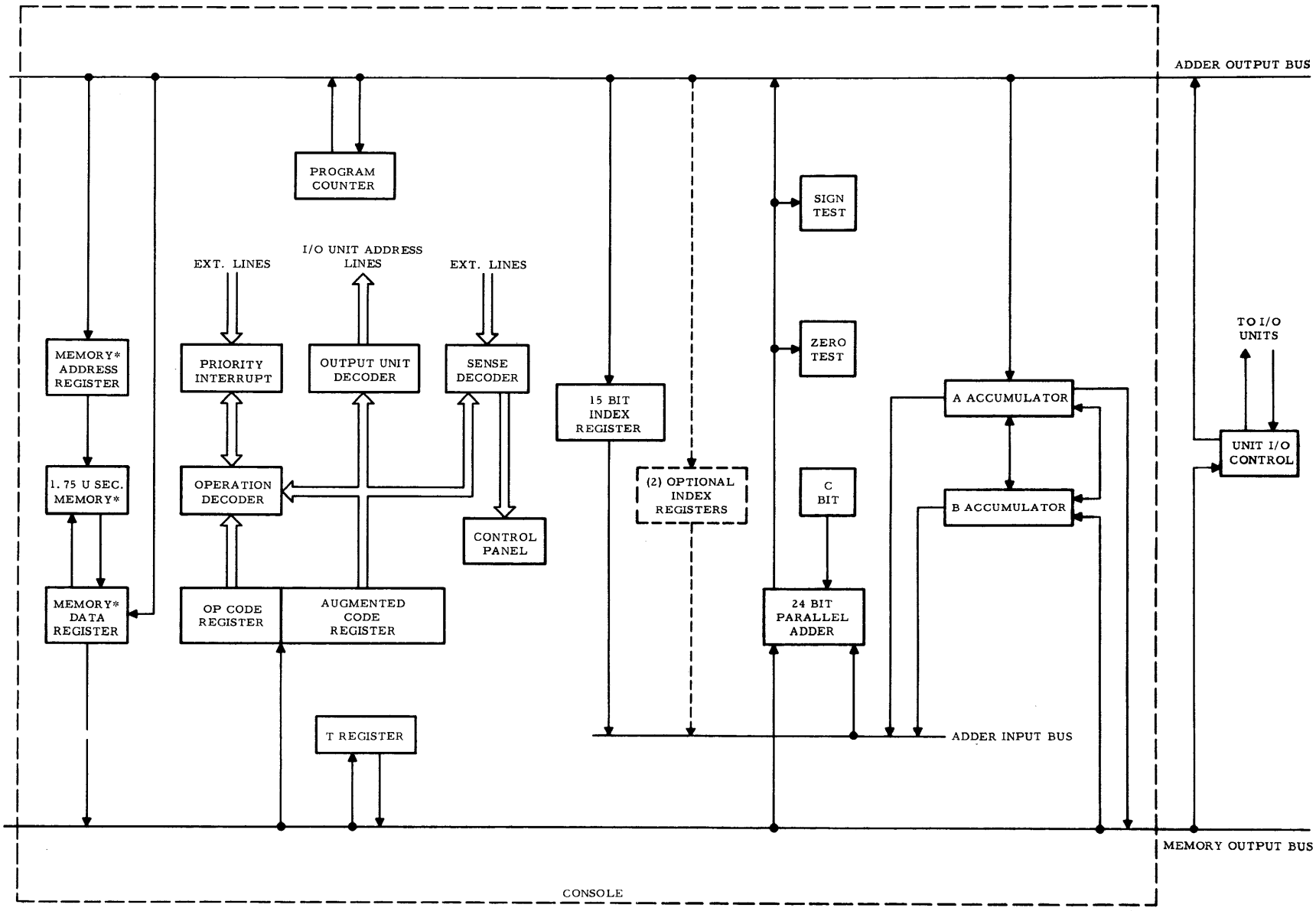
The SEL 840 general purpose computer is a fast (1.75 microseconds full cycle time) general purpose computer developed especially for real-time processing and process control as well as full scientific computation applications. The SEL 840 is offered in a standard configuration having 4096 memory locations, ASR 33 typewriter, paper tape punch and reader with the option of adding numerous standard, catalogue items to expand the basic configuration to meet any application. Section 2.1 defines the specifications of the SEL 840 basic configuration. The optional items available with your basic 840 are described individually following Section 2.1.

2.1 SEL 840 Computer - Basic Hardware Configuration

Figure 2.1 is a block diagram of the SEL 840 computer. The basic configuration is shown in solid lines.

The functional blocks shown have the following basic capabilities:

Memory	Up to eight 4096-address magnetic core modules used to store main programs, constants, subroutines and data awaiting output transfers or program manipulation. One 4096 word module is provided in the basic configuration.
"T" Register	The transfer register into which all words from memory are stored pending operation. Has complementing capability and holds the multiplicand, augend, subtrahend and divisor during arithmetic operations.



* UP TO EIGHT MEMORIES OPTIONAL

FIGURE 2.1 SEL 840 PROCESSOR BLOCK DIAGRAM

P806

A Accumulator	Main arithmetic register holds the addend, minuend, dividend, sum, difference, product and quotient of arithmetic operations.
B Accumulator	The extension of the A accumulator holds the least significant bits of double-precision words and the multiplier, least significant bits of product and remainder of arithmetic operations.
Index Register	Up to three 15-bit registers used in the modification of operand addresses to index files of data words. May be incremented or decremented by an instruction. One index register is provided in the basic configuration.
Adder	Full 24-bit parallel adder used in all arithmetic and logical operations and to add the index register to the operand address.
Memory Address Register	One 12-bit register is associated with each memory module to hold the instruction word and operand addresses. A master 3-bit address register is used to select the module to be accessed. The complete 15-bit address is included in each instruction word and operand address.
Program Counter	An incremental counter that provides the memory address from which the instruction words are taken. The counter is normally increased by one during each instruction cycle, but may be preset to any count by branch instructions.

2.1.1 SEL 840 Specifications

Classification	Parallel 24-bit binary, single address with index and indirect address modifiers.
Magnetic Core Memory	600 nanosecond access time, 1.75 microseconds full cycle time.
	The basic SEL 840 includes one 4096 word module, but is arranged to address up to 32,768 words of storage formed by the addition of 4096 word modules.

Arithmetic

Two's complement fully parallel adder with double-length accumulator. Full right and left, logical and arithmetic shift capabilities with single or double length accumulator.

Sample arithmetic process times are:

Add and Subtract	3.5 microseconds
Multiply	22.75 microseconds
Divide	24.5 microseconds
23-bit shift, right or left	12.25 microseconds

Control

A powerful instruction repertoire allows direct access of all memory locations and full arithmetic capabilities as well as a wide selection of input/output controls. A hardware program counter and a hardware index register allow instructions to be accessed and modified in the same cycle.

Input/Output

Systems I/O structure capable of handling 64 units.
Four armable multi-level priority interrupt lines.
Teletype ASR 33 typewriter, including paper tape punch and reader.

Control Console

Register and status indicators.
Priority interrupt inhibit.
Single step instruction execution.
Four sense switches.
Wired for all options - requires no field modification.

Packaging

Integrated micrologic modular construction operating ranges:

Input Voltage - 115 V60 cycle ±10%
Temperature - 10° to 35°C
Humidity - to 90%
System Weight - 1700 pounds
Space Requirement - Refer to Section 2.1.8
Maintenance Clearance - 36 inches front & rear

No special installation requirements.
Compatible with other equipment through supplied translators.

2.1.2 Input/Output Configurations

2.1.2.1 System Input/Output Control

The 840 computer uses an automatically synchronized time-shared I/O bus to communicate with up to 128 units. The six I/O instructions defined below perform all necessary data transfers and control functions.

DATA TRANSFER:

Mnemonic	Description
1) MOP (Memory Output)	24-bit word output from memory location. No registers affected.
2) AOP (Accumulator Output)	24-bit word output from the A accumulator.
3) MIP (Memory Input)	24-bit word input to specified memory location. No registers affected.
4) AIP (Accumulator Input)	24-bit word input to A accumulator
CONTROL:	
5) CEU (Command External Unit)	24-bit command output from instruction location. Interpreted by unit as a command to perform some function. No registers affected.
TEST:	
6) TEU (Test External Unit)	24-bit test code output from instruction location. Interpreted by unit as a test of some status. Reply from unit is on test return line.

All I/O instructions incorporate automatic hardware tests to insure synchronization with the unit, regardless of the speed capabilities of the unit. Instructions do not need to be changed if the same software is run with units of varying speed capabilities.

Several tests are performed by the computer to insure proper instruction execution.

Each I/O instruction addresses the unit desired, so no "Select"-"Deselect" operation is necessary. The I/O bus is used by the addressed unit only during the instruction time.

The 840 I/O connectors contain the logic signals shown in Figure 2.1.2-1. Each line is, in fact, a twisted pair and the two I/O cables are standard 51-pair cable.

The I/O instructions involve several operations. Unit addressing, test of unit response, test of ready for data transfer, and test of transfer complete, are performed on each instruction. A "Wait Flag" can be included in the data transfer and control instructions to cause the computer to "Wait" until the unit addressed is ready for data transfer. If a "Wait" occurs, it occurs as one or more "cycles" (1.75 microseconds).

Computer outputs appear as indicated in Figure 2.1.2-2. The cable driver (SEL #8614) will supply sufficient drive current to drive 16 cable terminators (SEL #8615), and a total of 100 feet of I/O cable. It should be noted that unnecessarily long cables may add cycles to the I/O instruction. The Basic 840 includes one set of drivers for the I/O channel. If more than 16 units are to be driven, additional drivers are available as an option. It should be noted

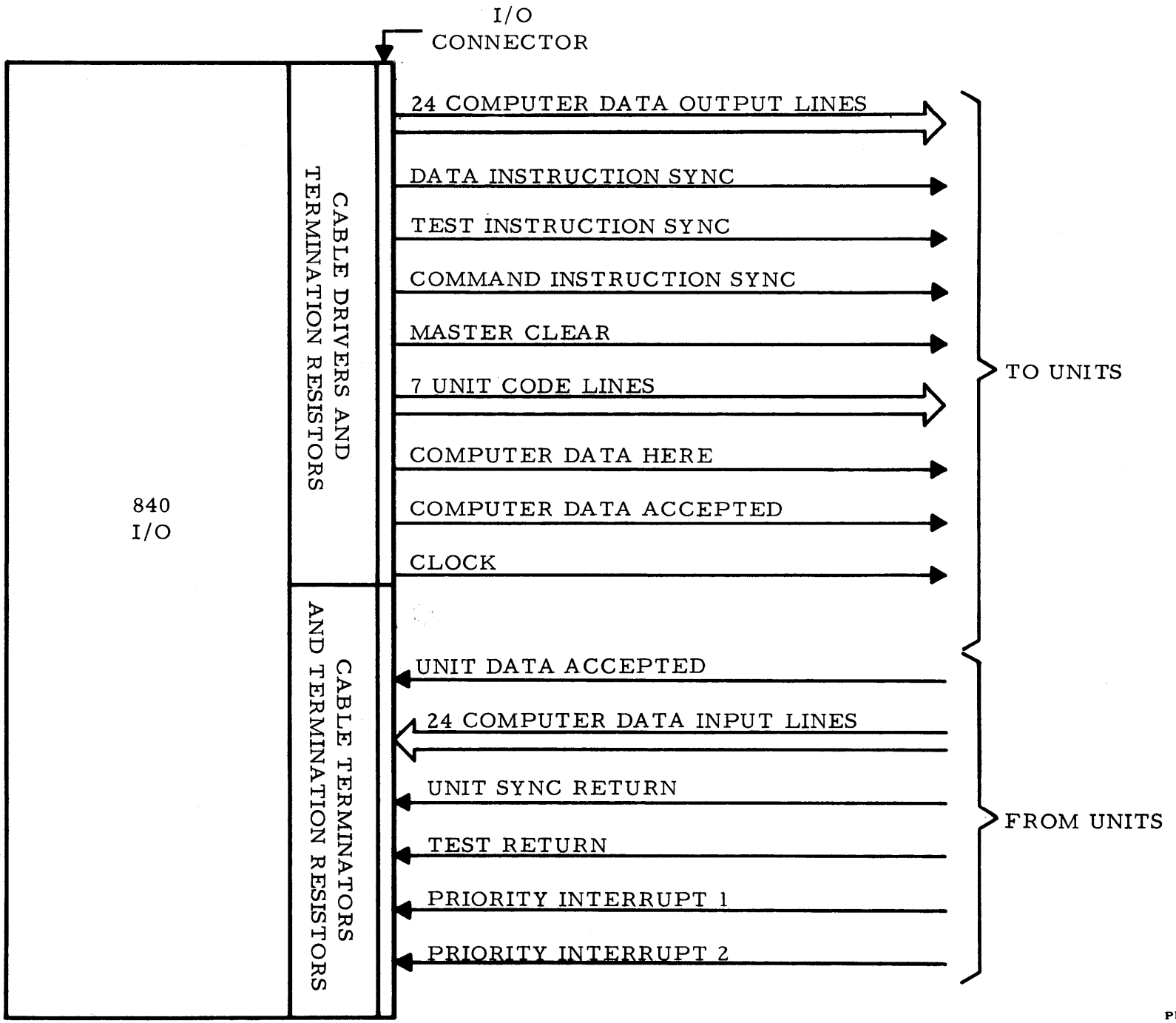


FIGURE 2.1.2-1 840 I/O INTERFACE

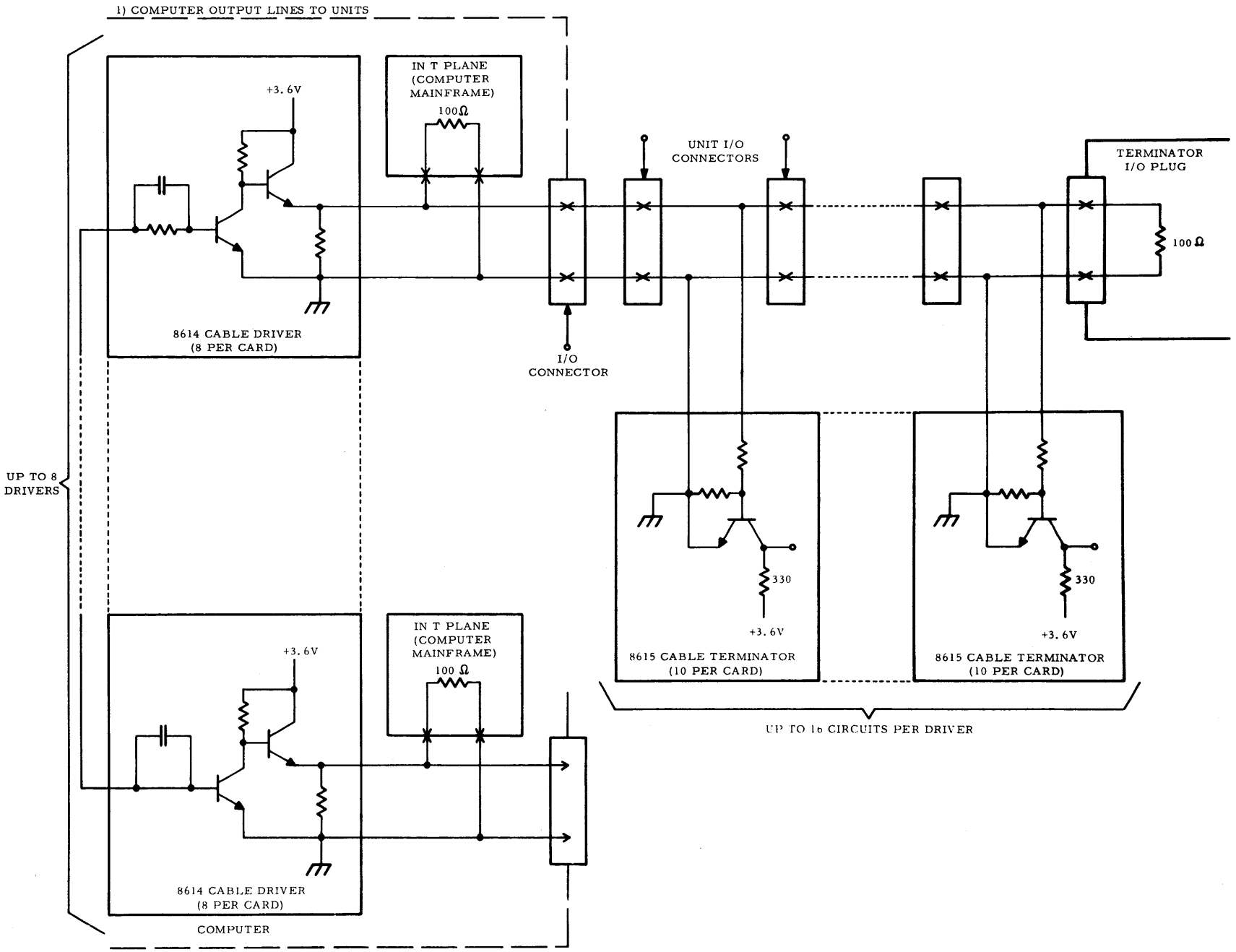


FIGURE 2.1.2-2 OUTPUT LINES FROM COMPUTER

P1361

that all data is presented to all units. Gating of data which pertains to the unit is done in the control logic for the unit.

Inputs to the computer appear as indicated in Figure 2.1.2-3. The emitter-follower configuration of the 8614 cable driver allows any unit to "lift" the line to the "true" level (+2V, +1.5V, -.5V). Gating to insure that only the unit addressed "on line" is done in the unit control logic. A total of 16 units can drive the input line. If additional units are required, additional terminators (and connectors) are available as an option. A total of 100 feet of cable can be used to connect the 16 units. Again, it should be noted that unnecessarily long cables should be avoided.

In Figure 2.1.2-4 the I/O cables are "daisy chained" from unit to unit, with a termination resistor plug on the end units output connector. Power is not supplied through the I/O cable.

Figures 2.1.2-5 and -6 illustrate the details of the timing of the I/O instructions, as seen from the main frame end. The symbology used is explained below the timing chart on Figure 2.1.2-5.

The timing shown assumes high-speed units with I/O cable of 50 feet or less. Delays of one or more cycles may take place with longer cable or lower speed logic.

The instructions operate as indicated in Figures 2.1.2-5 and -6. The unit code includes six bits of unit address and one bit which indicates input or output. This line is a 1 (+V on line) for output. In all I/O instructions, the unit code is placed on the unit code lines, then a sync line is raised. The

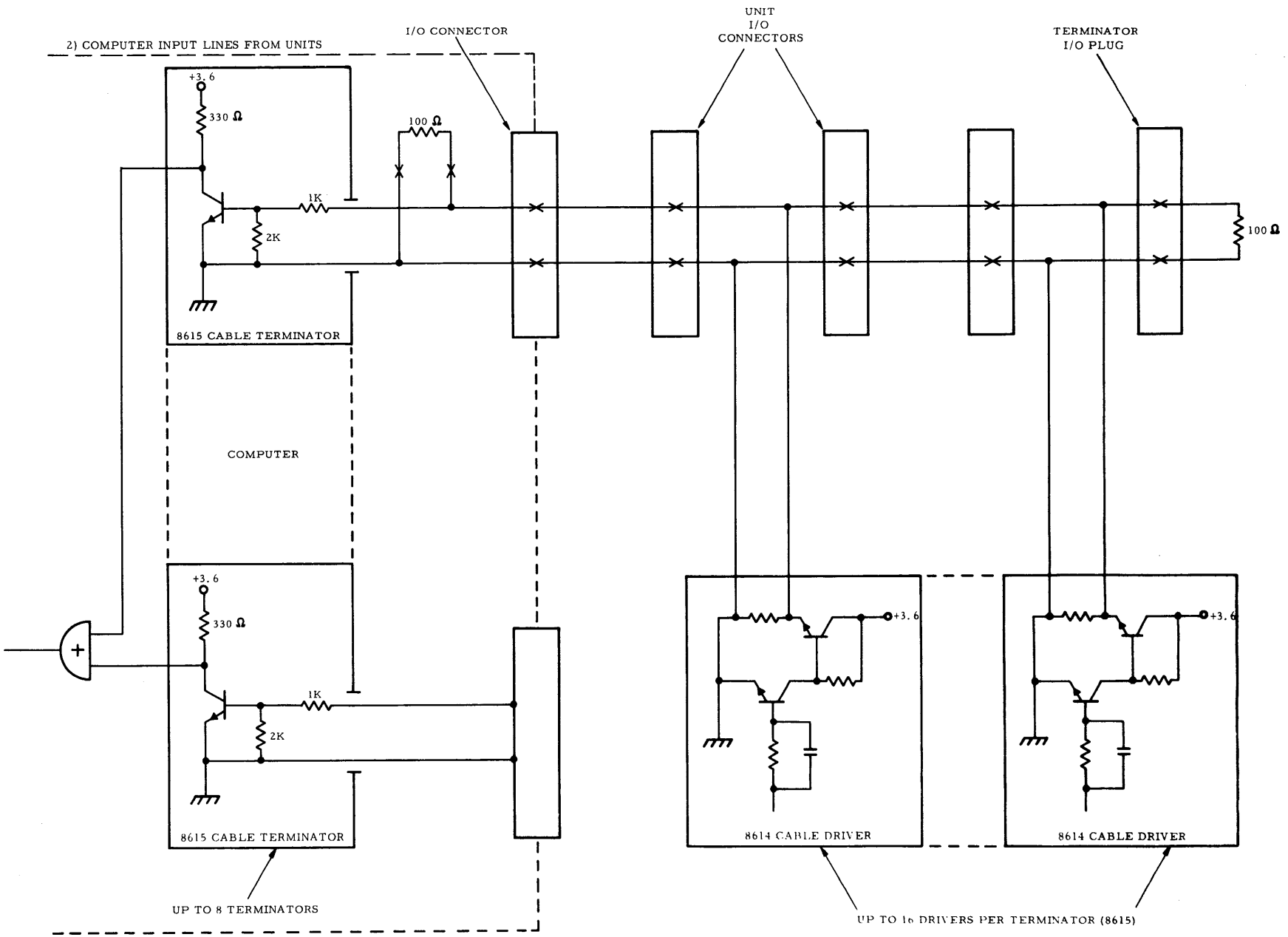


FIGURE 2.1.2-3 INPUT LINES TO COMPUTER

P1362

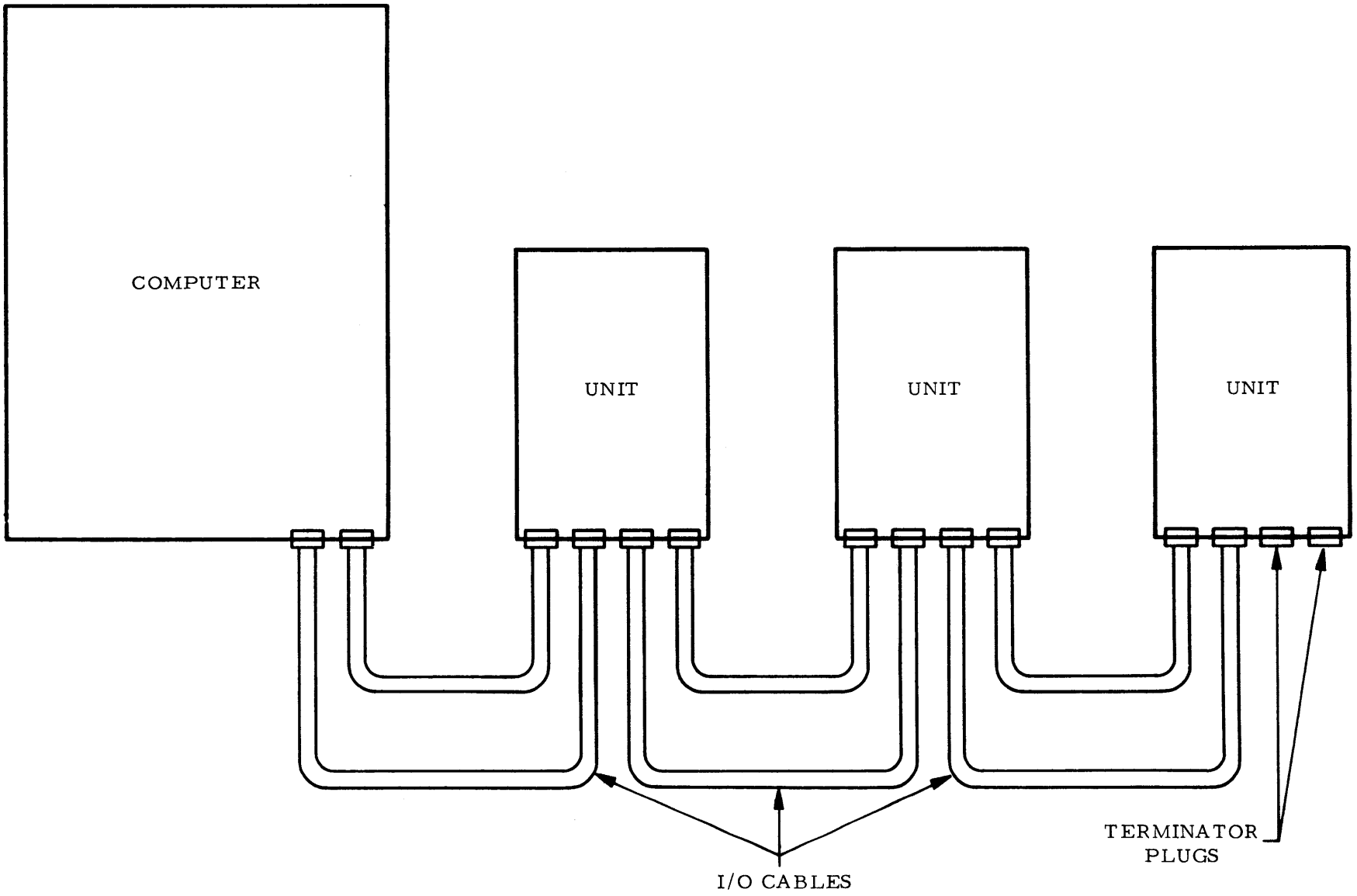
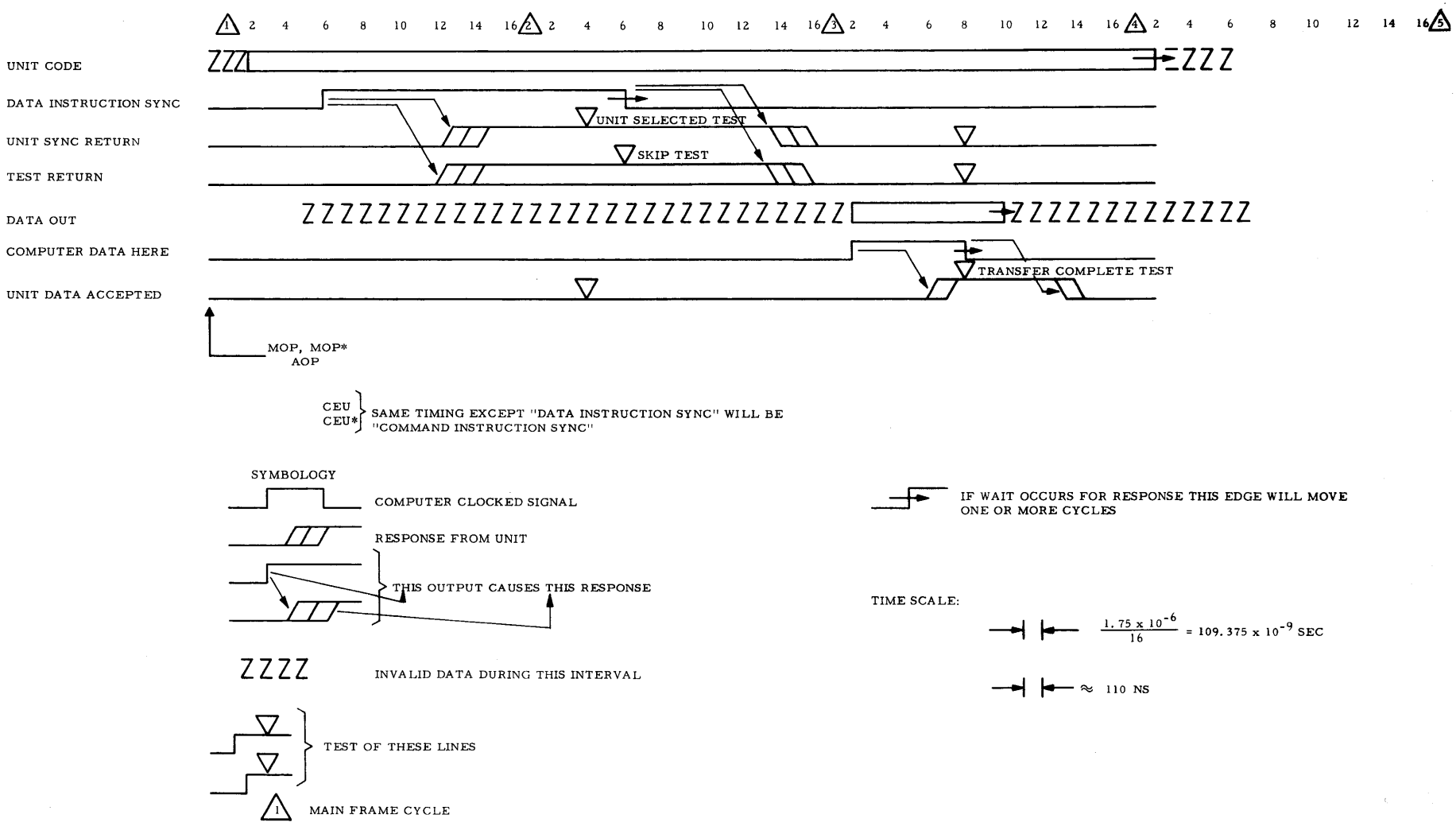


FIGURE 2.1.2-4 I/O CABLING

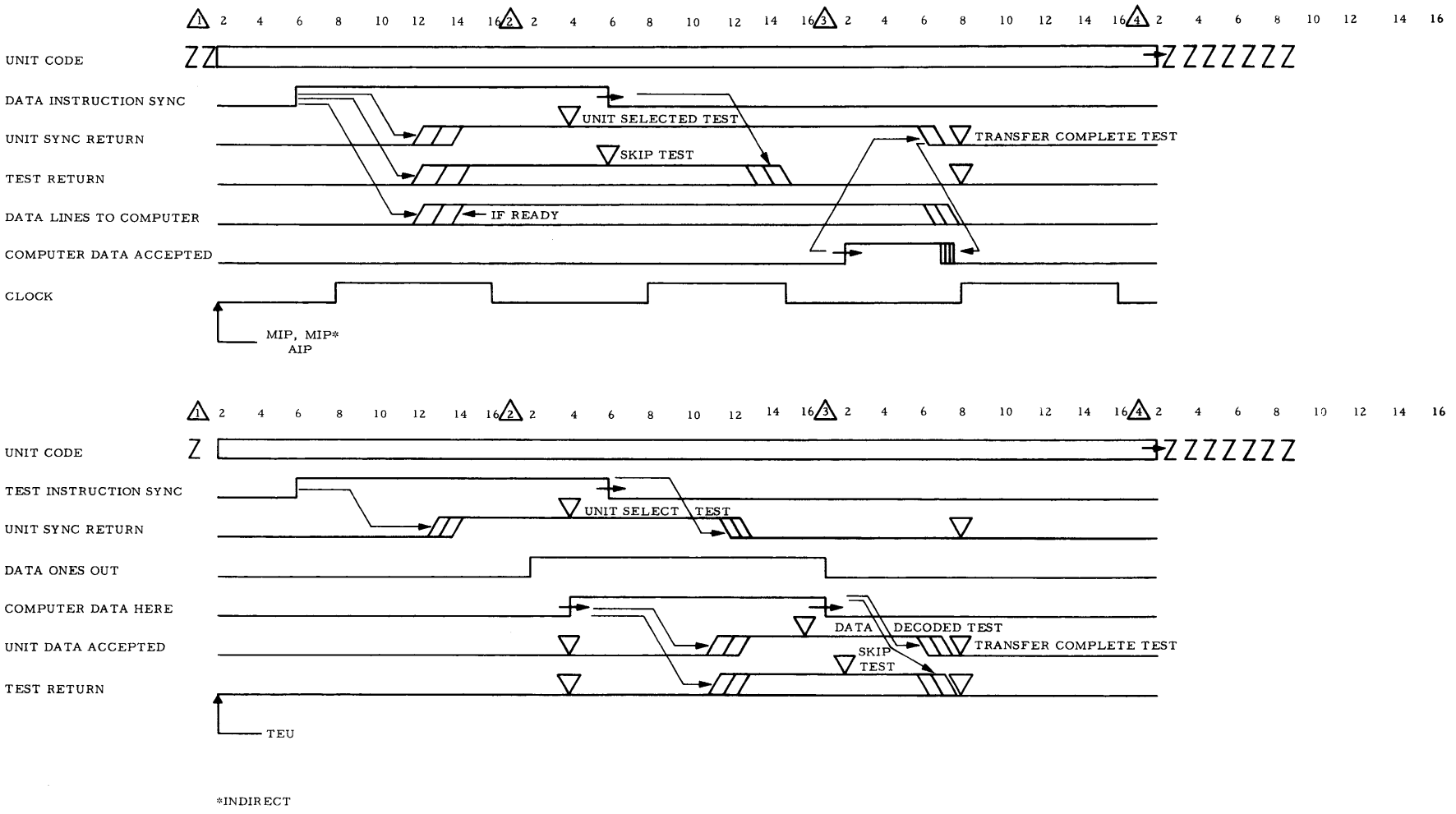
P1363



*INDIRECT

FIGURE 2.1.2-5 TIMING, OUTPUT COMMANDS

P1364



*INDIRECT

FIGURE 2.1.2-6 TIMING, INPUT AND TEST COMMANDS

P1365

specific line raised indicates what type of instruction follows. There are three sync lines: Data Instruction Sync (DIS), Command Instruction Sync (CIS), and Test Instruction Sync (TIS). The addressed unit is expected to reply on the sync return line as soon as it recognizes its unit code and which sync line is up. A unit-selected test is made at T_4. If this fails, a one-cycle wait will occur and then the test will be repeated. This continues until the addressed unit responds. The unit addressed gives a "status report" on the test return line to indicate if it can execute the indicated instruction (except for TEU, which will be discussed later). If the I/O instruction has a "Wait Flag", this test is repeated, adding a cycle each time, until the test return line goes "true", indicating the unit is ready to execute the instruction.

If the data or control I/O instruction does not have a "Wait Flag", the results of the skip test determine what action occurs. If the unit says "Ready To Execute", the data transfer takes place, then "skip" occurs in the program counter. If the unit says "Not Ready To Execute" during the skip test, no data transfer takes place and the instruction following the I/O instruction is accessed as the next instruction. This allows the programm to "branch out" when the unit is not ready. The final test on all I/O instructions involves a "Transfer Complete Test", which insures that slow units are "off line" before proceeding.

The lower part of 2. 1. 2-6, illustrates the timing of the Test External Unit (TEU) instruction. It is used specifically to test the status of a unit at the time it is executed; therefore, no "Wait Flag" is allowed.

"Wait" or "hold" may occur to allow unit response time but not to wait for a "ready" response to the skip test.

2.1.2.2 Block Transfer Control Unit

The SEL block transfer control (BTC) is an optional computer input/output control unit which enables fully buffered transfer of data between peripheral units and computer memory. The salient features of this unit are listed below.

Bits per Transfer	Full computer word
Maximum Words per Block	8,191
Maximum Transfer Rate	286,000 words per second
Memory Cycles Stolen per Transfer	1
Block Transfer Re-initialization	Automatic
Maximum Number of BTC's per Computer	8
Maximum Number of Peripheral Units per BTC	16

2.1.2.3 BTC Operation

The BTC contains two binary counters plus transfer initialization and synchronization logic. One of the counters stores the current word address (CWA) and the second stores the block length (BL). CWA defines the storage location for each word transferred to/from memory and BL defines the number of words to be transferred. The initial values for CWA and BL are obtained from two fixed locations in computer memory by the BTC each time a new block transfer is initiated. Each time a word is transferred between memory

and the selected peripheral unit, the hardware counters containing CWA and BL are incremented and decremented reseptively. The block transfer is completed and an interrupt is generated when BL = 0. After a block transfer is completed, the BTC automatically initaiates a new block transfer by obtaining a new initial set of CWA and BL values from the two dedicated memory locations. The block transfer sequence is terminated by placing a unique stop code in the BL word.

2.1.2.4 BTC Initialization and Data Flow

The BTC is initialized through the peripheral unit to/from which the block transfer is to be made. Figure 2.1.2.4 shows the data and control paths involved. The figure shows two peripheral units, each connected to a different BTC. Execution of a Command External Unit (CEU) instruction causes the unit specified by the instruction to send a transfer start signal to the BTC to which it is cabled. In many peripheral units this instruction also causes the unit to initiate action to produce/accept data. When the BTC receives the Transfer Start signal from the unit, it requests a memory cycle through the Unit I/O Control. It also generates the address of the CWA memory location assigned to it. When the memory cycle is granted, the CWA value is transferred from memory to the CWA counter in the BTC over the Unit I/O data lines connected to all peripheral units. A request for a second cycle is then made by the BTC, and the address of the memory location containing BL is placed on the address lines, again by the BTC. When the second cycle occurs, BL is transferred from memory to the BL counter in the BTC over the Unit I/O data output bus. A control code contained in the BL word is also decoded and a latch is set if the terminate code is detected, signifying that

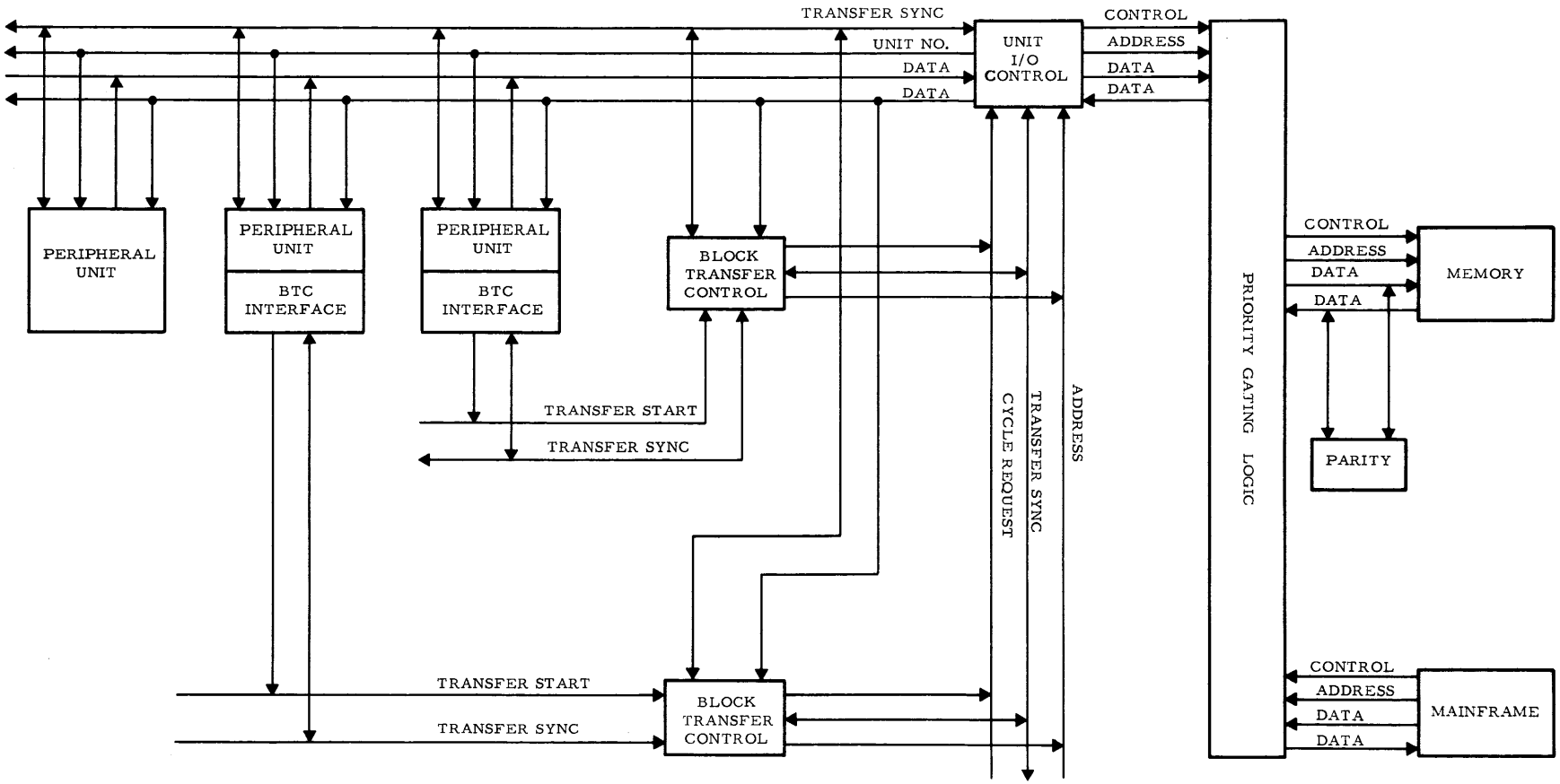


FIGURE 2.1.2.4 SEL COMPUTER DATA FLOW PATHS

P1471

no more block transfers are to be made after completion of the one being initialized. The maximum time for the entire initialization is three cycles for the CEU, 2 cycles for the CWA and BL transfers plus a maximum of three cycles for execution of a mainframe instruction between the CEU and CWA, BL transfers, resulting in a maximum time of 14 microseconds.

After BTC initialization, words are transferred between the selected peripheral unit and memory over the Unit I/O data lines under the joint control of the BTC and Unit I/O. A word transfer is initiated by the unit, which sends a Ready line to the BTC. The Ready signal causes the BTC to request a memory cycle through the Unit I/O Control. When the Unit I/O determines that the next cycle can be granted, memory available signal is sent to the BTC. The BTC, in turn, sends a signal to the peripheral unit which causes it to connect to the Unit I/O data lines, execute the data transfer, and then disconnect from the data lines. After completion of a word transfer, the CWA value is incremented and the BL value is decremented in the BTC counters. All words are transferred by repetition of this cycle, which is always initiated by the peripheral unit.

When the value of BL is decremented to zero, the block transfer is terminated. If the terminate latch in the BTC had not been set by the control code in the last BL word acquired from memory, a new block transfer is automatically initiated by the BTC. Re-initialization consists of acquiring new CWA and BL values from the memory locations assigned to the BTC. After re-initialization, an interrupt is generated which signifies that the transfer of the last block is completed and a new block transfer is initialized. The interrupt

processing routine may then store in the dedicated locations the CWA and BL values for the next block transfer anytime prior to the completion of the current block transfer. This re-initialization technique eliminates the problem of re-initializing block transfers under program control between the times of occurrence of two successive words in a continuous data stream.

If the terminate latch in the BTC had been set by the control code in the last BL word acquired from memory, an interrupt is generated when the value of BL is decremented to zero and no new transfer is initialized by the BTC. In addition, the Ready line from the peripheral unit is disconnected until a new Transfer Start signal is received. Hence, the BTC disconnects from the peripheral unit.

2.1.2.5 BTC Priority and Timing

BTC's are granted memory cycle requests on a priority basis. A unique priority is assigned to each BTC. The priority logic is structured similar to that of the interrupt priority logic, insuring that higher priority BTC's are always serviced before lower priority units. However, once a word transfer is initiated, it is not interrupted by a request from a higher priority BTC. In addition, BTC requests for memory cycles always take precedence over mainframe requests and can effectively "lock out" the mainframe if the peripheral transfer rate is high enough.

The maximum collective transfer rate for a BTC (or group of BTC's) is 572 KHz. Cycle stealing (or lockout) from the program is automatic and each BTC word transferred removes one cycle from the program. The BTC

can gain access to the memory after a delay of one cycle except for the following instructions:

Two Cycles		Three Cycles	
810	840	810	840
IMS	IMS	CEU	MOP
DIV	AAM	AOP	MIP
	IAM	AIP	TEU

When the listed instructions are executed, the main program will hold out the DMC transfer for the number of cycles indicated.

2.1.3 SEL 800 Series Peripheral Equipment

The SEL 840 processor line has a wide range of versatile input/output equipment. Each peripheral device has its own control unit which is compatible with each computer in the SEL 800 series. The peripheral equipment utilizes word or character buffering to relieve the computer of the need to provide a long time interface between the slower peripheral units and the processor.

A brief description of the optional I/O equipment is given below:

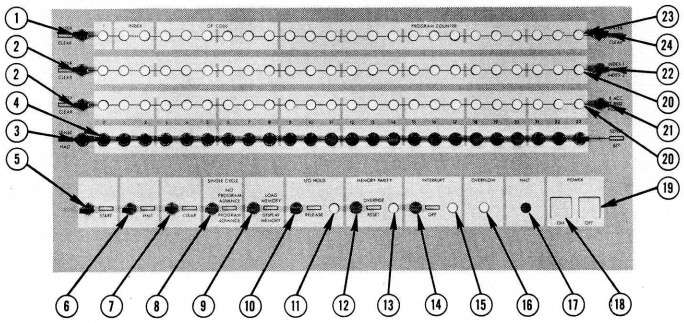
Paper Tape Reader	A photo-electric reader capable of reading 6, 7 8 level paper tapes at rates of 300 characters per second.
Paper Tape Punch	This unit punches 8 level paper tape at the rate of 110 characters per second.
Card Reader	Desk top type which reads 100 cards per minute (brush type). Desk top type which reads 400 cards per minute (photo-electric).
Magnetic Tape Systems	Includes tape control unit capable of handling up to eight tape transports with packing densities of 200 bpi, 556 bpi and 800 bpi at speeds to 112.5 inches per second. Tapes completely IBM 7-track compatible.
Line Printer	Models available with printing speeds of 300,600 or 1200 lines per minute, 120 characters per line and 64 printable characters.
CRT Displays	SEL standard products include a 21 inch and a 5 inch CRT display. These displays are capable of displaying alphanumeric characters, vector and points either simultaneously or individually.
Incremental Plotters	One or more Calcomp plotters may be connected to the computer through a standard coupler unit. This coupler enables the computer to control all pen and paper motions.
Disc File	The standard 840 disc unit stores up to 131,072 24-bit words. Data is stored on 128 tracks, each track containing 32 sectors of 32 words each. Average access time is 185 milliseconds. Up to eight disc units may be connected to the computer through a disc file control unit.

Converters	SEL standard lines of analog-to-digital and digital-to-analog converters providing binary words at a rate of up to 220 KC.
Multiplexer	SEL standard line of time-multiplexing units, sequential or random access, to 800 channels at rates up to 160 KC.

2.1.4 Control Console

The operator console is compactly arranged to provide maximum control and surveillance of the computer without the use of a distracting maze of controls. There are three rows of 24 indicators with the upper row showing the current instruction word. The second row displaying the contents of either the first or second index register or the A accumulator, depending on the position of a three-way switch. The third row, also switch controlled, displays the contents of either the B accumulator, T register or the third index register. A row of 24-three-position switches located below the indicators fulfills several functions: one, the switches may be used to enter data into the T register from which it can be transferred to any of the registers by means of enter/clear switches located beside each row of indicators; two, the switches may serve as console sense switches to modify the program, three, the switches may be used as programmed halt or "break point" controls. Another row of switches, including start, stop, master clear, program advance, memory load I/O hold, interrupt and power switches, provides the primary control. Also, included in this primary group are the program halt and arithmetic overflow indicators.

SEL 840 CONTROL PANEL



1. Raised to transfer bits 0 - 8 of the T register to the instruction register containing the operation code and address modifiers.
   Depressed to clear the instruction register.
2. Raised to transfer the contents of the T register to the selected register.
   Upper switch is depressed to clear the selected register.
   Lower switch depressed to clear T register.
3. Raised to connect switches 0 - 23 as console SENSE switches.
   Depressed to connect switches 9 - 23 as program HALT switches. (Computer halts when the program count equals selected value.)
4. Switches 0 - 23 are raised (lock) to function as SENSE or HALT switches and depressed to enter ONE bits into the T register.
5. Depressed to start computer operation.
6. Depressed to halt computer operation.
7. Depressed to clear all major registers and control latches.
8. Raised to repeat current instruction. Does not advance program counter.
   Depressed to execute single instruction in normal sequence and advances program counter.
9. Raised to enable SINGLE CYCLE switch to load contents of T register into memory.
   Depressed to enable SINGLE CYCLE switch to transfer contents of memory address to T register.
10. Depressed to release I/O wait and allow computer to resume.
11. Lights to indicate a wait for I/O function.
12. Raised to allow computer operation in the event of a memory parity error (lock).
    Centered to halt computer operation when memory parity error is detected.
    Depressed to reset the parity error latch.
13. Lights to indicate the detection of a memory parity error.
14. Depressed to inhibit operation of priority interrupts (lock).
15. Lights to indicate a priority interrupt.
16. Lights to indicate an arithmetic overflow condition.
17. Lights to indicate a program halt.
18. Pressed to apply power to computer.
    Lights when DC power is applied to computer.
19. Pressed to remove power from computer.
    Lights when AC power is connected to computer.
20. Indicators display the contents of the selected register.
21. Raised to gate the contents of the T register to the B accumulator and to display the contents of B accumulator register.
    Centered to display the contents of the T register.
    Depressed to gate the contents of the T register to Index Register 3 and to display the contents of index 3 register.
22. Raised to gate the contents of the T register and clear inputs to Index Register 1 and to display the contents of index 1 register.
    Centered to gate the contents of the T Register and clear inputs to the A accumulator and to display the contents of A accumulator register.
    Depressed to gate the contents of the T register and clear inputs to Index Register 2 and to display the contents of index 2 register.
23. Display the contents of the program counter.
24. Raised to enter bits 9 - 23 of the T register into the program counter.
    Depressed to clear the program counter.

Notes: 1. Only the SENSE, HALT and display selection switches are active while the computer is operating.
2. Switches 3 , 9 , 21 and 22 lock in all positions.

OPERATOR'S CONTROL PANEL

2.1.5 SEL 840 Programming Characteristics

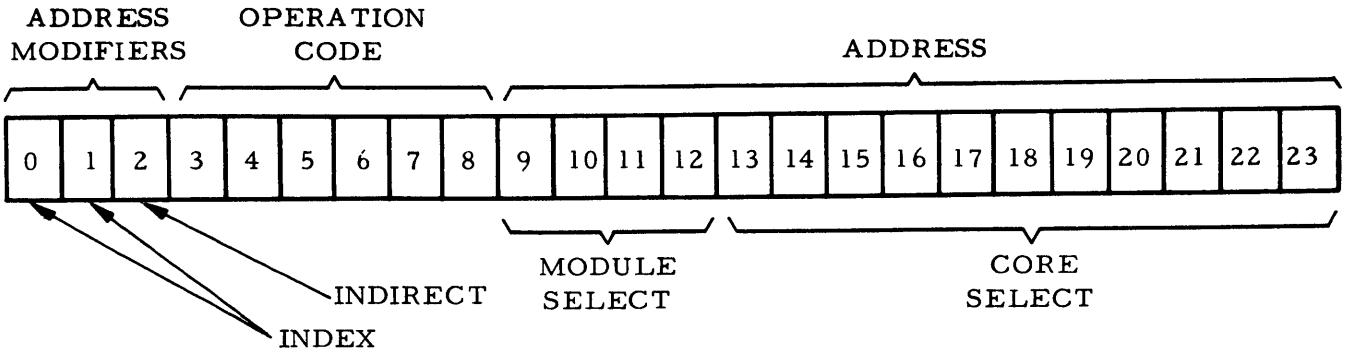
The SEL 840 is provided with two basic instruction word formats to achieve optimum program capability. The word format for those instructions requiring operands from memory contains a 6-bit operation code, a 15-bit address field and three address modifiers (see Figure 2.1.5). The 15-bit address field allows direct addressing of 32,768 possible memory locations. The two X modifiers (bits 0 and 1) are INDEX flags that may be coded to add the contents of one of the three index registers to the basic operand address. The I modifier (bit 2) is an INDIRECT flag that changes the function of the contents of the specified address from operand to address. This indirect addressing function provides additional programming flexibility to reduce total program time.

The word format for instructions other than the basic memory reference instruction (shifts, logical functions, control functions, input/output, etc.) contain an augmenting operation code in place of the operand address used in the memory reference word format.

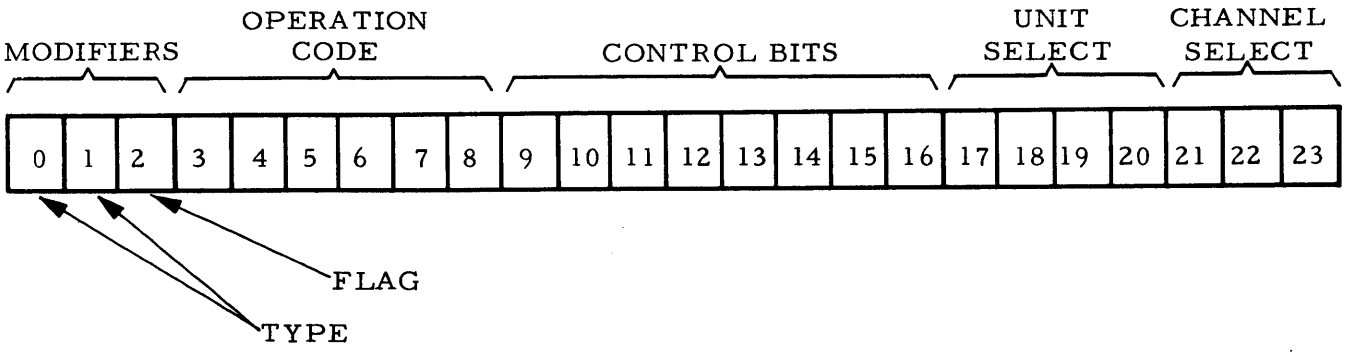
Also, shown in Figure 2.1.5 are some of the data formats used in the SEL 840 for single precision and double precision fixed point and floating point data.

PROGRAMMING

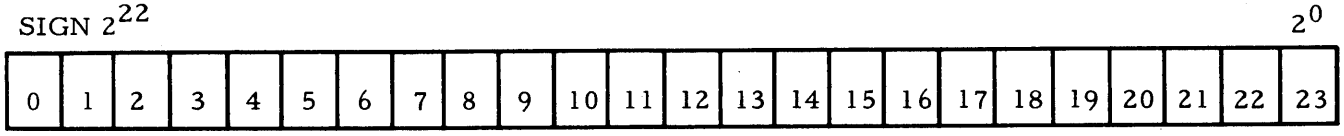
INSTRUCTION WORD FORMAT



I/O CONTROL WORD FORMAT



DATA WORD FORMAT (SINGLE PRECISION)



DATA WORD FORMAT (DOUBLE PRECISION)

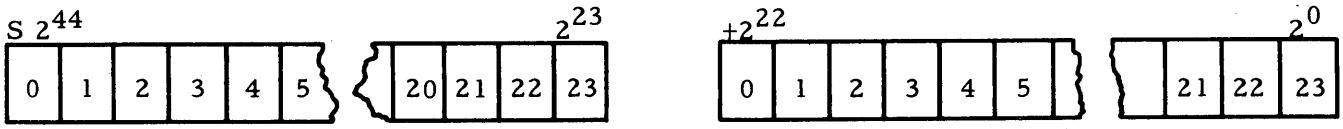


FIGURE 2.1.5 SEL 840 DATA FORMATS

P1376

Table 2.1.5 - SEL 840 Instruction List

Load/Store

Mnemonic	Description	Timing (1.75 microseconds cycles)
LAA	Load the A accumulator. The contents of the memory location determined by the effective address replace the contents of the A accumulator.	2
LBA	Load the B accumulator. The contents of the memory location determined by the effective address replace the contents of the B accumulator.	2
LIX	Load the index register. The contents of the memory location determined by the effective address replace the contents of the index register. The index bits indicate which register will be loaded.	2
STA	Store the A accumulator. The contents of the A accumulator are loaded into the memory location determined by the effective address.	2
STB	Store the B accumulator. The contents of the B accumulator are loaded into the memory location determined by the effective address.	2
STI	Store the index register. The contents of the index register are loaded into the memory location determined by the effective address. The index bit indicates which index register will be stored.	2
LCS	Load control switches. The contents of the console control switches replace the contents of the A accumulator.	1

Arithmetic

Mnemonic	Description	Timing (1.75 microsecond cycles)
AMA	Add memory to the A accumulator. The contents of the memory location determined by the effective address are added algebraically to the contents of the A accumulator and the result is stored in the A accumulator.	2
SMA	Subtract memory from the A accumulator. The contents of the memory location determined by the effective address are subtracted algebraically from the A accumulator and the result is stored in the A accumulator.	2
AAM	Add the A accumulator to memory. The contents of the A accumulator are added algebraically to the contents of the memory location determined by the effective address and the sum is stored in the same memory location.	3
AMX	Add memory to index register. The contents of the effective memory location are algebraically added to the contents of the designated index register The 15 least significant bits of the sum are stored in the designated index register.	2
MPY	Multiply. The contents of the B accumulator are multiplied by the contents of the memory location determined by the effective address. The most significant half of the product is placed in the A accumulator and the least significant half of the product is placed in the B accumulator. The signs of the A and B accumulator are set to the algebraic sign of the product.	13

Mnemonic	Description	Timing (1.75 microsecond cycles)
DIV	Divide. The contents of the memory location determined by the effective address are divided into the contents of the A and B registers. (When the dividend is a single precision number, it is necessary to clear the A accumulator prior to the divide instruction and load the dividend into the B accumulator). The quotient is stored in the A accumulator and the remainder is stored in the B accumulator. The sign of the A accumulator is set to the algebraic sign of the quotient. The sign of the remainder is the sign of the dividend.	14
RNA	Round the A accumulator. The contents of the A accumulator are increased by one if bit 2 in the B accumulator is a ONE and the sign of the A accumulator is positive. If the A accumulator sign is negative, the contents of the A accumulator are decreased by one if Bit 2 of the B accumulator is a ZERO.	1

Branch/Skip

Mnemonic	Description	Timing (1.75 microseconds cycles)
BRU	Unconditional branch. The effective address replaces the contents of the program counter.	1
SPB	Store place and branch. The contents of the program counter are stored in the memory location determined by the effective address. The effective address plus one is transferred to the program counter.	2
PIR	Priority interrupt return. The contents of the memory location determined by the effective address plus one are transferred to the program counter. This instruction also resets the highest set priority interrupt latch.	2
IIB	Increment index and branch. One is added to the contents of the addressed index register. If the index register contains a negative number, the effective address is transferred to the program counter.	1
BAZ	Branch accumulator zero. If the accumulator is zero, the effective address is transferred to the program counter.	1
BAP	Branch accumulator positive. If the A accumulator is equal to, or greater than, zero the effective address is transferred to the program counter.	1
BAN	Branch accumulator negative. If the contents of the accumulator are less than zero, the effective address is transferred to the program counter.	1

Branch/Skip (continued)

Mnemonic	Description	Timing (1.75 microseconds cycles)
CMA	Compare memory and A accumulator. The contents of the memory word at the effective address are compared to the contents of the A accumulator. If the contents of memory are greater than A, the next instruction is used; if the contents of memory equals A, the next instruction is skipped; if the memory is less than the A accumulator, the next two instructions are skipped.	2
SMP	Skip if memory is positive. If the contents of the memory location determined by the effective address are equal to, or greater than, zero, the next instruction is skipped.	2
BOF	Branch on overflow. The overflow indicator is reset. If it was set the effective address is transferred to the program counter.	1
SNS	Skip if external signal not set. If external signal is not present, the next sequential instruction is skipped.	1
IMS	Increment memory and skip. The memory location designated by the effective address is incremented by one. If the number becomes zero, the next instruction will be skipped.	3
SAS	Skip on A accumulator sign. If the sign of A is negative, the next instruction is executed; if the contents of A is zero, the next instruction is skipped; if the sign of A is positive, the next two instructions are skipped.	1

Logical

Mnemonic	Description	Timing (1.75 microseconds cycles)
MAA	AND memory and A accumulator. The contents of the memory location determined by the effective address form a logical product with the contents of the A accumulator.	2
MOA	OR memory and A accumulator. The contents of the memory location determined by the effective address form a logical sum with the contents of the A accumulator.	2
MEA	Exclusive OR memory and A accumulator. The contents of the memory location determined by the effective address form a logical exclusive OR with the contents of the A accumulator.	2
NEG	Negate the A accumulator. A 2's complement is formed with the contents of the A accumulator.	1
CSB	Copy sign from B accumulator. The carry latch is set to the sign of B accumulator and the sign of B is cleared to zero (plus).	1
ASC	Complement A accumulator sign. The sign of the A accumulator is complemented.	1
CNS	Convert number system. Converts sign magnitude numbers to two's complement and two's complement numbers to sign magnitude.	1

Shift

Mnemonic	Description	Timing (1.75 microseconds cycles)
RSA	Right shift the A accumulator. The contents of the A accumulator, bits 1-23, are shifted right as specified by the six shift bits of the instruction.	1 - 4 shifts - 2 cycles 5 - 8 shifts - 3 cycles 9 - 12 shifts - 4 cycles 13 - 16 shifts - 5 cycles 17 - 20 shifts - 6 cycles 21 - 23 shifts - 7 cycles
LSA	Left shift the A accumulator. The contents of the A accumulator, bits 1-23, are shifted left as specified by the six shift bits of the instruction.	
FRA	Full right shift arithmetic. The contents of the A accumulator, bits 1-23, and the B accumulator, bits 1-23, are shifted to the right as specified by the six shift bits of the instruction.	
FLA	Full left shift arithmetic. The contents of the A accumulator, bits 0-23, and the B accumulator, bits 1-23, are shifted to the left as specified by the six shift bits of the instruction.	
RSL	Right shift the A accumulator logically. The contents of the A accumulator, bits 0-23, are shifted to the right as specified by the six shift bits of the instruction.	
FRL	Full left rotate. The contents of the A accumulator, bits 0-23, and the B accumulator, bits 0-23, are shifted to the left as specified by the six shift bits of the instruction. The bits leaving the most significant position of B enter the least significant position A and the bits leaving the most significant position of A enter the least significant position of B.	
LSL	Left shift the A accumulator logically. The contents of the A accumulator, bits 0-23, are shifted to the left as specified by the six shift bits of the instruction.	

Shift (cont.)

Mnemonic	Description	Timing (1.75 microseconds cycles)
NOR	Normalize. The contents of A (bits 0-23) and B (bits 1-23) are shifted left until the sign bit of A (A_0) and the next bit (A_1) do not agree. If an index bit is present in the instruction, the index register is decremented by one for each shift. The instruction shift bits specify the maximum number of left shifts permitted.	1 - 4 shifts - 2 cycles 5 - 8 shifts - 3 cycles 9 - 12 shifts - 4 cycles 13 - 16 shifts - 5 cycles 17 - 20 shifts - 6 cycles 21 - 23 shifts - 7 cycles
FLL	Left shift the A and B accumulator logically. The contents of the A accumulator (including sign) and the B accumulator (including sign) are shifted to the left as specified by the shift bits of the instruction.	

Register Change

Mnemonic	Description	Timing (1.75 microseconds cycles)
CLA	Clear the A accumulator. The contents of the A accumulator are set to zero.	1
TAB	Transfer A accumulator to B accumulator. The contents of the A accumulator are placed in the B accumulator.	1
IAB	Interchange A and B accumulators. The contents of the A and B accumulators are interchanged.	1
TBI	Transfer the B accumulator to the index register. The contents of the A accumulator are transferred to the index register.	1
IAM	Interchange A accumulator and memory. The contents of the A accumulator are interchanged with the contents of the memory at the location determined by the effective address.	3
TBA	Transfer B accumulator to A accumulator. The contents of the B accumulator are transferred to the A accumulator.	1

Control

Mnemonic	Description	Timing (1.75 microseconds cycles)
EXU	Execute. The instruction in the memory location determined by the effective address is executed. The program counter is not affected.	1+I
HLT	Halt. The computer halts until the START switch is depressed. Execution begins at the next sequential instruction.	1
NOP	No operation. No operation is performed by this instruction. Any non-assigned opcode will also be executed as a NOP.	1
PIE	Priority Interrupt Enable. Enables a selected set of priority interrupt channels belonging to the same interrupt group. The enabled channels will sense any interrupts until disabled by a PID instruction.	1
PID	Priority Interrupt Disable. Disables a selected set of priority interrupt channels belonging to the same interrupt group. The disabled channels will not sense any interrupts until enabled by a PIE instruction.	1

Input/Output

Mnemonic	Description	Timing (1.75 microsecond cycles)
AOP	Accumulator output. The contents of the A accumulator are transferred to the specified unit.	3
AIP	Accumulator input. The contents of the specified unit are transferred to the A accumulator.	3
MOP	Memory output. The contents of the effective memory address are transferred to the specified unit.	3
MIP	Memory input. The contents of the specified unit are transferred to the effective memory address.	3
CEU	Command external unit. Commands a specified I/O unit to perform a designated operation.	3
TEU	Test external unit. Tests an I/O unit for the presence of a specific condition. If the abnormal condition is present, the next instruction is executed; if the normal condition is present, the next instruction is skipped.	3

2.1.6 SEL 840 Software System

A comprehensive, fully integrated, well documented and completely checked out program preparation, library, debugging and utility system is supplied with the SEL 840 computer system at no cost to the user.

Specific features of this standard package are listed below by item but a few words in regard to the philosophy behind the software system package design are appropriate here.

In determing the optimum software package for the type of equipment under consideration, the following factors were deemed to be of prime importance:

- The large variety of equipment configurations which will be delivered.
- The type of applications which will be programmed for the equipment.
- The amount of programming personnel time which will be involved in developing and debugging operational programs.
- The need to utilize programs and routines which may already exist on other equipment.
- The quality and completeness of the documentation supplied with the software and library routines.

In order to satisfy these objectives, two basic types of program preparation system are provided; a symbolic assembler (MNEMBLER) and a full FORTRAN IV compiling system. Depending upon the specific requirements of a specific portion of an operational package, these two programming systems

provide the user with an optimum capability where trade-offs between coding and checkout time and program running time are involved.

The fact that a specific portion of a program may be coded in either language is most significant to the user. Two methods of mixing are available a.) the FORTRAN IV processor will accept assembler coding 'in-line' or b.) the loader will accept both FORTRAN and assembler generated coding in any sequence.

This feature together with the very comprehensive debug package will significantly reduce the coding and checkout time required to produce operational programs.

The FORTRAN IV language specified for this system is the standard ACM published language which includes the IBM 7090/94 language as a sub-set, thus the SEL FORTRAN IV will provide direct compatibility with the majority of other manufacturers supplied FORTRAN IV systems.

In order to satisfy the requirement that all of the supplied software system will operate on a wide variety of computer configurations, especially in the area of peripheral equipment, all of the supplied packages are written in a modular form with a standard program interface specification. This will allow any combination of input/output equipments to be utilized without major revision of the program.

840 Assembly-Program - MNEMBLER

The MNEMBLER program operates in either a one-or two-pass mode. The one-pass mode offers a significant time advantage at assembly time, while the two-pass mode results in a shorter output tape and more complete error checking.

All computer instructions will be accepted by the assembler and addresses may be expressed in symbolic, decimal or octal formats.

The following special pseudo-ops are also processed:

BSS - Reserve block of storage; name at start.

BES - Reserve block of storage; name at end.

EQU - Define symbolic name.

ORG - Set next storage address.

ZZZ - Set instruction bits to zero.

REL - Set assembly mode to relative.

ABS - Set assembly mode to absolute.

CALL- Call library subroutine.

NAME- Define subroutine name.

DATA- Define octal, decimal (fixed or floating) or Alphanumeric data.

MOR - End of tape; more left in program.

END - End of program.

A symbolic side-by-side listing complete with error messages is output (operator optional) along with the object output tape.

SEL 840 Loader

The SEL 840 object program loader is designed to be compatible with the FORTRAN IV Compiler and the Assembly program.

The program provides for relocatable and absolute instructions. The capability of using pre-assembled subroutine libraries is included in a manner which guarantees that a given routine will only be loaded once, regardless of the ordering of the library.

Loading (and chaining if requested) is done using modular input/output driver subroutines, allowing maximum flexibility in choice of load device. The loader loads the main program and any subroutines called for. It completes linkage between the main program and the subroutines.

SEL 840 Debug

The debug program is a utility program designed to help a programmer debug a program while it is in memory. The following functions are provided:

a. Type the contents of specified memory in octal or command format.

b. Modify the specified memory. Input being in octal format.

c. Dump specified memory areas onto paper tape in a self-loading (non-relocatable) format.

d. Enter breakpoints in order to "leap-frog" trace a program.

e. Clear specified areas of memory to zero.

f. Search memory for references to specified areas.

g. Initiate branches (or HALT AND BRANCH) to any part of memory.

Each of these functions are initiated by typing a keyword through the console typewriter keyboard.

SEL 840 UPDATE

Correction of errors in card decks is a relatively easy procedure, consisting of pulling out the bad cards and inserting new cards. However, symbolic source programs on paper tapes are not so easily corrected or modified.

The UPDATE program is designed to allow the computer operator to easily correct or modify a symbolic source program tape by providing the following functions:

a. Deletion of a specified line or group of lines.

b. Insertion of a new or replacement line or lines.

c. List the source program (or portions of it) complete with line reference numbers.

All references to the symbolic source tape are made by referring to a sequence number. This number is present on all assembly listings and on all listings generated by the UPDATE program.

SEL Library Package

The SEL 840 library is a complete set of subroutines, including those needed for on-line data system operation. The ASA specified set of subroutines for the SEL FORTRAN IV are also included in the following categories:

1. Single precision floating point functions
2. Double precision floating point functions
3. Complex floating point functions
4. Integer functions
5. Input/output functions
6. Control functions

The following subroutines constitute the Library at the time of writing.

A. Single Precision Floating Point Functions

1) F$L ---- Load a single precision floating point value from memory into the pseudo accumulator.

2) F$H ---- Store a single precision floating point value from the pseudo accumulator into memory.

3) F$A ---- Add a single precision floating point value from memory to the pseudo accumulator.

4)	F$S ----	Subtract a single precision floating point value in memory from the pseudo accumulator.
5)	F$M----	Multiply a single precision floating point value in memory by the pseudo accumulator.
6)	F$D ----	Divide the single precision floating point value in the pseudo accumulator by an argument in memory.
7)	ALØG--	Compute LOG (base e) of argument.
8)	ALØGIO-	Compute LOG (base 10) or argument.
9)	SQRT---	Compute square root of argument.
10)	EXP ---	Compute e raised to the argument power.
11)	F$E2 --	Raise value in pseudo accumulator to the power specified by the interior argument.
12)	F$E3 --	Raise value in pseudo accumulator to the power specified by the single precision floating point argument.
13)	SIN ----	Compute SINE of argument
14)	CØS----	Compute COSINE of argument.
15)	ATAN --	Compute the ARCTANGENT of the argument.
16)	ATAN2 -	Divide argument 1 by argument 2 and compute the ARCTANGENT of the result.
17)	TANH --	Compute the Hyperbolic Tangent of the argument.
18)	AMAXO-	Find the maximum value in a list of fixed point arguments.
19)	AMAX1 -	Find the maximum value in a list of single precision floating point arguments.
20)	AMINO -	Find the minimum value in a list of fixed point arguments.
21)	AMIN1--	Find the minimum value in a list of floating point arguments.
22)	ABS----	Compute absolute value of argument.

23) AINT --- Truncate argument to its integer value.

24) AMØD --- Compute the remainder that results when dividing the first argument by the second argument.

25) DIM ---- Compute the difference between two arguments.

26) SIGN ---- Set the sign of the second argument onto the value of the first argument.

27) FLOAT-- Convert a fixed point argument to single precision floating point format.

28) SNGL --- Convert a double precision floating point argument to single precision floating point format.

29) REAL --- Compute the real part of a complex format argument.

30) AIMAG -- Compute the imaginary part of a complex format argument.

B. Double Precision Floating Point Functions

1) F$LD --- Load a double precision floating point value from memory into the pseudo accumulator.

2) F$HD --- Store a double precision floating point value from the pseudo accumulator into memory.

3) F$AD --- Add a double precision floating point value from memory to the pseudo accumulator.

4) F$SD --- Subtract a double precision floating point value in memory from the pseudo accumulator.

5) F$MD --- Multiply a double precision floating point value in memory by the pseudo accumulator.

6) F$DD --- Divide the double precision floating point value in the pseudo accumulator by an argument in memory.

7) DLØG --- Compute LOG (base e) of argument.

8) DLØGIO - Compute LOG (base 10) of argument.

9) DSQRT -- Compute square root of argument.

10) DEXP --- Compute e raised to the argument power.

11) F$E4 --- Raise single precision floating point value in pseudo accumulator to a double precision floating point argument value giving a double precision result.

12) F$E5 --- Raise a double precision value to an integer argument value giving a double precision floating point result.

13) F$E6 --- Raise a double precision value to a single precision argument value giving a double precision floating point result

14) F$E7 --- Raise a double precision value to a double precision argument value giving a double precision floating point result.

15) DSIN --- Compute SINE of argument.

16) DCØS --- Compute COSINE of argument.

17) DATAN - Compute the ARCTANGENT of the argument.

18) DATAN2- Divide argument 1 by argument 2 and compute the ARCTANGENT of the result.

19) DMAX1 - Find the maximum value in a list of double precision floating point arguments.

20) DMIN1 -- Find the minimum value in a list of double precision floating point arguments.

21) DABS --- Compute absolute value of argument.

22) DMOD--- Compute the remainder that results when dividing the first argument by the second argument.

23) DSIGN--- Set the sign of the second argument onto the value of the first argument.

24) DBLE--- Convert the single precision floating point argument to double precision floating point format.

C. Complex Floating Point Functions

1) F$LC --- Load a complex floating point value from memory into the pseudo accumulator.

2) F$HC --- Store a complex floating point value from the pseudo accumulator into memory.

3) F$AC --- Add a complex floating point value from memory to the pseudo accumulator.

4) F$SC --- Subtract a complex floating point value in memory from the pseudo accumulator.

5) F$MC--- Multiply a complex floating point value in memory by the pseudo accumulator.

6) F$DC --- Divide the complex floating point value in the pseudo accumulator by an argument in memory.

7) CLØG--- Compute LOG (base e) of the complex argument.

8) CSQRT-- Compute square root of the complex argument.

9) CEXP--- Compute e raised to the complex argument power

10) F$E8 --- Raise the complex value in the pseudo accumulator to the power specified by the integer argument. The result is a complex value.

11) CSIN --- Compute SINE of the complex argument.

12) CCØS --- Compute COSINE of the complex argument.

13) CABS --- Compute the positive vector generated by the real and imaginary parts of the complex format argument. The result is a single precision floating point value.

14) CMPLX - Combine two single precision floating point format arguments into one Complex format value.

15) CØNJG - Compute the conjugate of a Complex format argument.

D. Integer Functions

1) F$ID --- Divide the integer value in the accumulator register by the integer argument.

2) F$E1 --- Raise the integer value in the accumulator register to the value specified by the integer argument.

3) MAXO -- Find the maximum value in a list of fixed point arguments.

4) MAX1 --- Find the maximum value in a list of single precision floating point arguments.

5) MINO --- Find the minimum value in a list of fixed point arguments.

6) MINI --- Find the minimum value in a list of single precision floating point arguments.

7) IABS --- Compute absolute value of argument.

8) INT ---- Truncate the single precision floating point argument to an integer and convert result to integer mode.

9) IDINT --- Truncate the double precision floating point argument to an integer and convert result to integer mode.

10) MØD ---- Compute the remainder that results by dividing the first argument by the second argument.

11) IDIM ---- Compute the difference between two arguments.

12) ISIGN---- Set the sign of the second argument onto the value of the first argument.

13) IFIX ---- Convert the single precision floating point argument to integer format

E. Input/Output Functions

1) F$IØ ---- Format control and conversion of decimal, binary, logical or alphanumeric data for use by FORTRAN programs

2) F$AR --- Set up argument for input or output.

3) F$CB --- Close-out input/output buffer at end of an I/B argument list.

4) F$R1 --- Driver for typewriter input.

5) F$W1 --- Driver for typewriter output.

6) F$R2 --- Driver for paper tape input.

7) F$W2 --- Driver for paper tape output,

8) F$C2 --- Punch stop code on paper tape.

9) F$R3 --- Driver for card input.

10) F$W4 --- Driver for line printer output.

11) F$R5 --- Driver for mag. tape 1 input.

12) F$W5 --- Driver for mag. tape 1 output.

13) F$C5 --- Rewind, backspace or END file on mag. tape 1.

14) F$R6 --- Driver for mag. tape 2 input.

15) F$W6 --- Driver for mag. tape 2 output.

16) F$C6 --- Rewind, backspace or END file on mag tape 2.

17) F$R7 --- Driver for mag. tape 3 input.

18) F$W7 --- Driver for mag tape 3 output.

19) F$C7 --- Rewind, backspace or END file on mag. tape 3.

20) F$R8 --- Driver for mag. tape 4 input.

21) F$W8 --- Driver for mag. tape 4 output.

22) F$C8 --- Rewind, backspace or END file on mag. tape 4.

23) F$R9 --- Driver for mag. tape 5 input.

24) F$W9 --- Driver for mag. tape 5 output.

25) F$C9 --- Rewind, backspace or END file on mag. tape 5.

26) F$RN --- Driver for all input devices. Device used determined by argument value.

27) F$WN --- Driver for all output devices. Device used determined by argument value.

28) F$CN --- Driver for rewind, skip, or END file control of all devices. Device used determined by argument value.

F. Control Functions

1) SLITE --- Turn on the specified pseudo-sense-light, or turn off all pseudo-sense lights.

2) SLITET -- Test the specified pseudo-sense-light, set a variable to 1 or 2 depending on the sense light setting, and set the pseudo-sense-light off.

3) SSWITCH - Test the specified sense switch and set a variable to 1 or 2 depending on the sense switch setting

4) ØVERFL - Set a variable to 1 or 2 depending on the status of an error flag, then reset the error flag

5) F$ER ---- Set an error flag and halt if a sense switch is set. Then return to the calling program.

6) F$HT ---- Type a short message and halt. Then return to the calling program.

7) F$AT ---- Transfer argument addresses to a sub-program.

8) F$CL ---- Read in a segment of a chain program and initiate execution of that segment.

9) F$CD ---- Dump a section of memory in the format required for chaining.

10) F$T1 ---- Output trace information for an integer value.

11) F$T2 ---- Output trace information for a single precision floating point value.

12) F$T3 ---- Output trace information for a double precision floating point value.

13) F$T4 ---- Output trace information for a complex floating point value.

14) F$T5 ---- Output trace information for a logical value.

Diagnostic Routines

The SEL 840 Checkout Program is a complete package designed to give the operator the ability to exercise the memory, the main frame logic, the input/output channels and associated peripheral equipment.

The memory exerciser generates various types of worst case bit patterns and exercises the memory with these patterns while monitoring for errors. Provisions are made for automatic relocating of the exerciser program to allow the entire memory to be included in all tests. Also, included are certain branch/skip instructions which are sequenced and executed through each location in the memory.

The main frame exerciser executes the entire instruction repertoire individually in a large variety of sequences while monitoring the results for errors. Errors are indicated by halts. Pertinent information concerning the instruction that failed and the nature of the failure can be obtained from the A and B accumulator displays, the program counter and certain selected memory locations.

The programs for the I/O channels and associated peripheral equipment tests the ability of the various I/O units to generate or receive all acceptable characters. A selected input is used and visual monitoring of the control panel or output unit is required by the operator for verification of proper operation. Equipment tested includes standard teletypewriter output, input, punch and reader as well as optional card punch, card reader, line printer, high-speed paper tape equipment, magnetic tape units and other units as needed for a particular application.

2.1.7 System Logic

2.1.7.1 Circuit Module Form Factor

For ease of maintenance and reduced spare part complements, all electronic circuitry will be packaged on not more than two printed circuit board sizes and shall use the same connectors. All circuitry will be solid state. All digital logic in the computer will be silicon monolithic integrated circuits.

2.1.7.2 System Logic Detailed Description

2.1.7.2.1 All cards represent an advanced approach to implementing the logic design of digital systems. The circuit designs and packaging have been derived from extensive prior experience and reflect the latest thinking in the industry. These cards are not developmental items but do comply with current best practices. Circuit designs permit logic design to be implemented with a minimum number of rules. Military components and practices are used in all cases where applicable. In all cases, the electrical circuit design, card design, and card production reflect the most conservative and reliable approaches.

2.1.7.2.2 Logic levels in the computer will be nominal zero volts and +1.3 volts. The tolerances permitted on the zero volt levels are 0 ±0.6 volts. The tolerances permitted on the +1.3 volts levels shall be +2.3 volts or -0.5 volt. All circuits are able to perform their logic functions and maintain their load driving capabilities for a 10-percent variation of the power supply voltages.

2.1.7.3 All circuits in the computer will have a threshold of at least 0.5 volt which must be overcome by the applied signal before any response can occur. All logic circuits will consist of integrated circuits packaged in TO-5 cans operating with their emitters at ground and their collectors returned to +3.6 volts.

2.1.7.4 All circuits in the computer will use the same logic levels so that any output can be connected to any input. The prime consideration in making inter-connections is the maximum driving capability of each circuit.

2.1.7.5 Test points will be located on the front of all cards and will represent circuit outputs.

2.1.7.6 Elco miniature connectors will be used on all cards and will mate with 29-pin Elco miniature receptacle wire-wrap type #7001-29-5-1-19. Minimum card conductor spacing and conductor width will be 0.010 inch. Minimum land diameter will be 0.20 inches in addition to maximum component hold size diameter.

2.1.7.7 Transistors will be isolated from the printed circuit board material by use of Unipads.

2.1.7.8 Pin holes and other imperfections in the copper pattern following etching will not be larger than 0.010 inch.

2.1.7.9 All materials used in card packaging will be new, undamaged and the best grade for the purpose intended.

2.1.7.10 Decoupling

Each logic card will contain decoupling capacitors on the D.C. supply voltages.

2.1.8 System Construction

2.1.8.1 Logic Pages (Computer)

All system electronic pages will be mounted on hinges which can be locked in the open position.

2.1.8.2 Rear Access (Computer)

All electronic circuitry will be accessible from the rear of the system.

2.1.8.3 Metal Hardware

All aluminum parts used in the construction of the system will be black anodized in accordance with MIL-A-8625, Anodic Coating for Aluminum and Aluminum Alloys. All steel hardware (with the exception of that listed in paragraph 5.7.8) shall be stainless or cadmium plated. Sheet steel parts will be cadmium plated or zinc-chromate treated prior to painting.

2.1.8.4 Computer Cabinet

The computer will be housed in a cabinet whose dimensions are 70-1/4 inches in width, 51 inches in height and 43-1/4 inches in depth. The operator's table is 15-1/2 inches in depth and a maximum of 29-1/4 inches from the floor. The cabinet will house the entire computer including power supplies. The cabinet will be able to house all of the expansion capabilities of the basic processor system. Rear access doors will be fan-fold doors that provide complete access to the interior of the cabinet. The doors will not extend more than 7-3/4 inches when open.

3.0 FIELD MAINTENANCE PROVISIONS

SEL will submit, upon request, a list of recommended spare parts for your computer system. Delivery of those spare parts is made from stock and can be effected before your system is shipped if desired.

3.1 Service Policies

SEL offers several types of maintenance service policies. The three types of policies which would be applicable to your needs are described below.

TYPE I — Emergency or Demand Service: This includes all unscheduled maintenance at customer's request.

TYPE II — Scheduled Maintenance: This includes all operational checks, calibrations preventive maintenance etc. conducted in accordance with a prescribed schedule.

TYPE III — Resident Service: Under this policy, a resident engineer is assigned to the customer's facility to perform emergency service, trouble-shooting and preventive maintenance, as well as assist in programming, equipment application, engineering support, documentation, and training of customer personnel. The minimum contract period is one half year.

4.0 TRAINING

Systems Engineering Laboratories, Incorporated provides at no charge, training for your personnel in operation and maintenance of the computer and can provide programmer training. This training consists of classroom training and practical training.

Practical training for your personnel will be conducted at SEL's Fort Lauderdale facilities. Your engineers and technicians will participate in actual system testing and will be given simulated system malfunctions for corrective maintenance practice. The programmer training course will include instruction for the programming systems (MNEMBLER, LOADER, ETC.) and operating instructions for the 840 computer.

The classroom training will provide your operating and maintenance personnel with primary instruction in basic digital logic, SEL standard circuits, system logic, test equipment and maintenance procedures. Also, programmer training and instruction on the SEL 840 computer will be provided.

Once per quarter, SEL offers a two-week programming school in Fort Lauderdale, to which you can send your engineers and programmers for instruction in programming the 840 Computer.

Programming and maintenance courses for the 810 and 840 computers are held at SEL on a regularly scheduled basis. The following schedule covers the period from 10 January through 18 November 1966.

SEL 810 Programming Training

Jan. 10-21
Feb. 21 - Mar. 4
April 18-29
June 5-17
Aug. 8-19
Sept. 26 - Oct. 7
Nov. 28 - Dec. 9

SEL 840 Programming Training

March 7-18
June 20 - July 1
October 10-21

SEL 810 Maintenance Training

Jan. 24 - Feb. 18
May 2- 27
Aug. 22 - Sept. 2 & Sept. 12 - 23
(one week break in class)

SEL 840 Maintenance Trai ning

March 21 - April 15
July 11 - August 5
Oct. 24 - Nov. 18

The prerequisites for these courses are:

1. Programming course first week - no previous programming experience.

2. Programming course second week - first week of programming course or programming experience with other computers.

3. Maintenance course - programming course plus experience and/or training in the maintenance of electronic equipment.

Please advise SEL concerning your course preference thirty days prior to its date, the number of your personnel who will attend, and the programming and/or maintenance experience of each.

5.0 INSTALLATION

SEL will be responsible for the installation of the computer system at your facility. The assistance of your personnel will be requested to move the computer from your receiving dock to the site; however, all moving will be under the direct supervision of SEL personnel. The system Project Engineer will be responsible for this installation and checkout. He will remain with the system until its acceptance.

6.0 ACCEPTANCE TESTING

An acceptance test procedure will be submitted prior to the scheduled delivery of the system. You will have the right to recommend alternates in order to satisfy requirements of the specification.

The test procedure will be suitable for accurate and rapid operational testing. The tests will demonstrate the operation of the system in all functional modes and show compliance with the requirements of the contract specification.

Final acceptance tests will be performed at your facility. The SEL system project engineer will perform the tests and remain there until final acceptance.

7.0 DOCUMENTATION

7.1 Drawings

Systems Engineering Laboratories, Incorporated will supply drawings for your system. Drawing standards will be those of good commercial practice and in compliance with SEL drafting standards.

Drawings supplied under this contract will include:

1. Logic diagrams for the system and each subunit.
2. Schematic and assembly drawings for SEL standard printed circuit module boards with component parts labeled.
3. Cable terminations and interconnections.
4. Outline drawings showing locations of units in racks and dimensions.

SEL standard digital circuits are each represented by logic symbols. System logic diagrams are therefore simplified, and concise procedures set forth all capabilities of these modules in brief form.

7.2 Technical Manuals

Five copies of the instruction manual for operation and maintenance of your system will be supplied. Logic diagrams of each major sub-system and corresponding theory of operation discussions will enable new operators to familiarize themselves rapidly with the operation of the system. Step-by-step performance test procedures will be spelled out to permit complete functional checkouts of system operation at recommended intervals. The manual

will include detailed schematics, assembly drawings, wire lists and all other drawing information necessary for system maintenance.

Technical manuals will be delivered with the system.

All manuals will be illustrated, printed and bound in accordance with accepted standards of good commercial practice. Commercial manuals for any vendor-supplied unit in the system will be furnished separately.

In addition, five copies of the Software Reference Manual will be delivered prior to system delivery to coincide with the agreed-upon training periods as outlined in Section 4.0.

7.3 Reports

Systems Engineering Laboratories will submit letter-type progress reports on a calendar month basis. Reports will be in narrative form, brief in content, and shall include:

1. A bar chart to indicate program planning and work accomplished.
2. A quantitive description of overall progress.
3. An indication of any current problems which may impede performance and proposed corrective action.
4. A discussion of the work to be performed during the next reporting period.
5. Estimate of percentage completion.

8.0 MANAGEMENT

SEL was organized to design and develop specialized data acquisition and processing systems for government and industry. Definite considerations in establishing out management and engineering functions were the purchasing philosophies and practices of our potential customers. All customers desire the best equipment technically and they can be divided into these categories:

(1) Government - Defense

Procurement where money is generally available and in some cases is a secondary consideration.

(2) Government - Non Defense

Procurement where money is limited and is a basic, if not primary, consideration.

(3) Industry Capital Funds

Procurement where money is the primary consideration.

Therefore, to effectively sell out products and systems, the selling price must reflect both technical excellence and realistic costs.

We have estabilshed two basic management concepts to achieve this objective. They are:

(1) An advisory board comprised of representatives from all phases of Management meets on a weekly basis to review company progress, contract cost and schedule performances, discuss problem areas and plan future action.

(2) Each contract is assigned to a specific project engineer and contract administrator. These individuals are directly responsible for the technical and administrative requirements of the contract, and through their representatives on the Advisory Board, Management is aware of the status of all jobs.

The project engineer directs and supervises the design, development, fabrications and installation of the system and the preparation of all required documentation.

The contract administrator maintains contact with the customer through the customer's administrative designee. He transmits questions or information from the SEL project engineer to the customer or from the customer to the SEL Engineering Department. This insures that all requests for action or information conform to the requirements of the contract The administrator also insures that all required financial information is submitted to the customer in accordance with contract provisions.

SEL management procedures to implement this project are based on the Program Evaluation and Review Technique, (PERT). Because of SEL's comparatively small size, some particular PERT functions are deleted, e. g. high speed electronic computer processing of simulated program changes to determine network optimums by Paths of Criticality, Successor Predecessor Event Number and the like.

Within the basic PERT framework, however, SEL management for your project will achieve the following objectives:

a. Define and control the efforts necessary to accomplish program objectives on time.

b. Graphically illustrate the inter-relationships of events and activities required to complete the project.

c. Focus management attention on -

(1) danger signals that require remedial decisions to prevent problem materialization.

(2) areas of effort for which trade-offs in time and resources might improve capacity to meet major scheduled dates.

d. Maintain effective internal communications between the project group and support groups, and external communication with the customer.

9.0 FACILITIES

SEL has recently occupied a new 52,000 square-foot facility situated on twelve acres of land in Plantation, Florida, a western suburb of Fort Lauderdale. The approximate floor space allocation of the new facility is as follows:

Department	Square Footage
Engineering	10,000
Production and System Fabrication	20,000
Administration	10,000
Drafting, Graphic Arts, Publications and all other	12,000

Enclosed in this section are the floor plans and a photograph of our Fort Lauderdale facility.

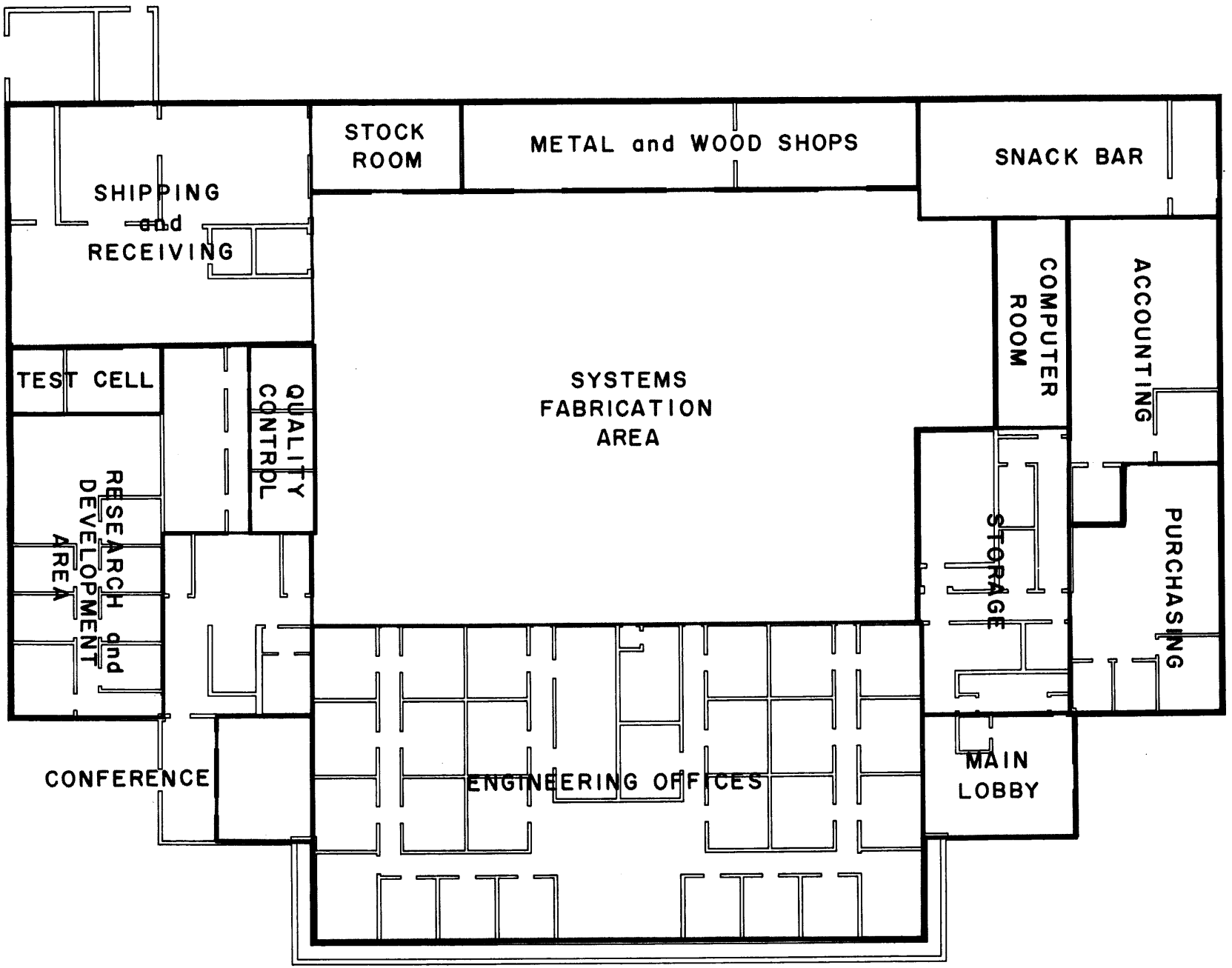
A 66,000 square-foot addition to our present building is in the planning stages, and ground breaking is scheduled for the spring of next year.

SEL currently employs 450 personnel, which includes field service engineers and field sales representatives. This compares to an employment figure of 12 at founding. Over one hundred of the 450 personnel are engineers with a minimum of a bachelor's degree.

Since incorporation in January of 1961, SEL's growth pattern has been steady, both in number of personnel and in dollar volume of sales. Our yearly sales (shipments) have been $1,016,225 for fiscal year 1962; $2,001,735

for fiscal year 1963; $3,069,289 for fiscal year 1964; and over $5,000,000 for fiscal year 1965. We are projecting sales in excess of $8,000,000 for the current fiscal year.

SEL extends to you a cordial invitation to visit us at your convenience.


SHIPPING
and
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METAL and WOOD SHOPS
SNACK BAR
COMPUTER
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ACCOUNTING
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CONTROL
SYSTEMS
FABRICATION
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DEVELOPMENT
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CONFERENCE
ENGINEERING OFFICES
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LOBBY

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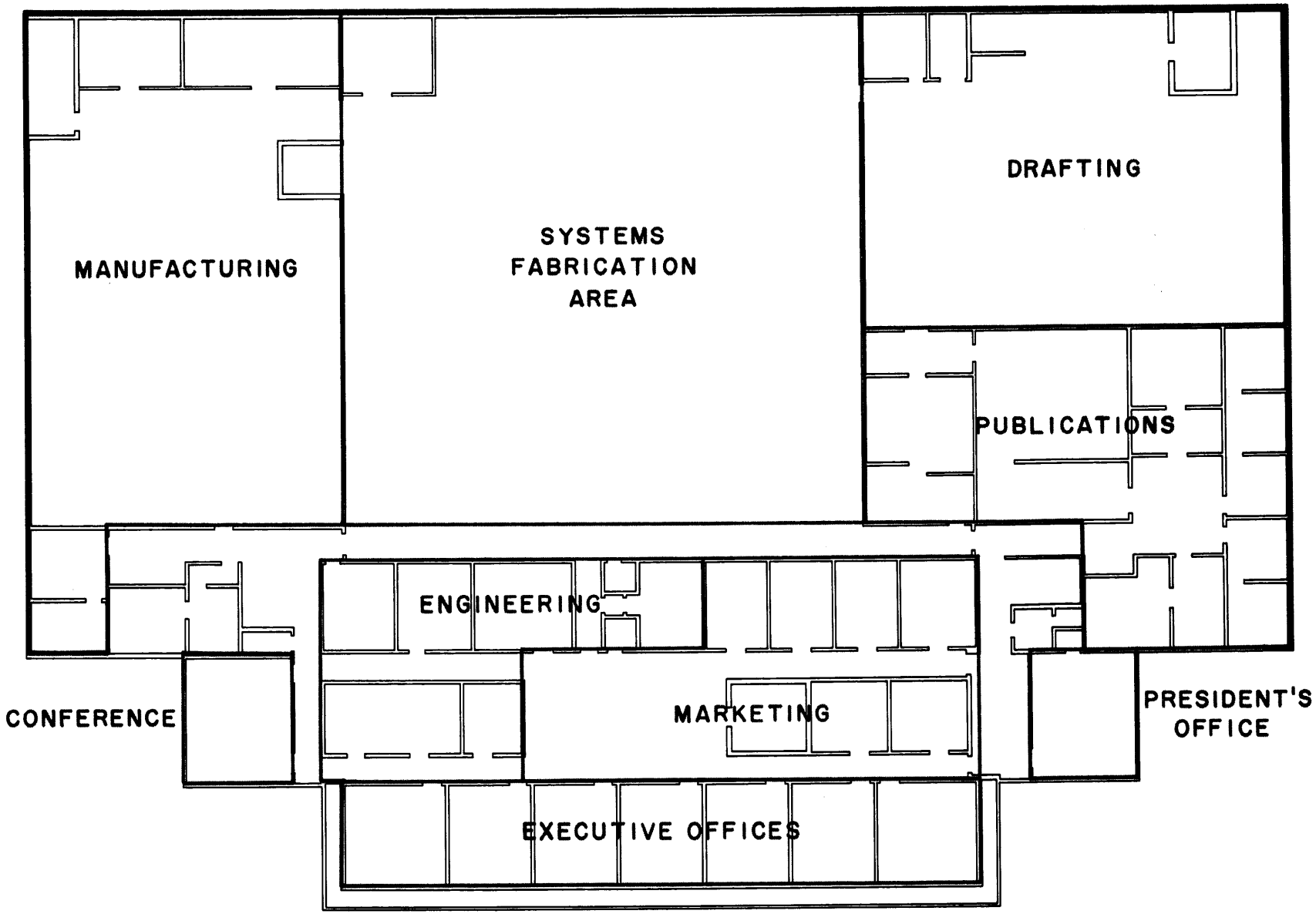
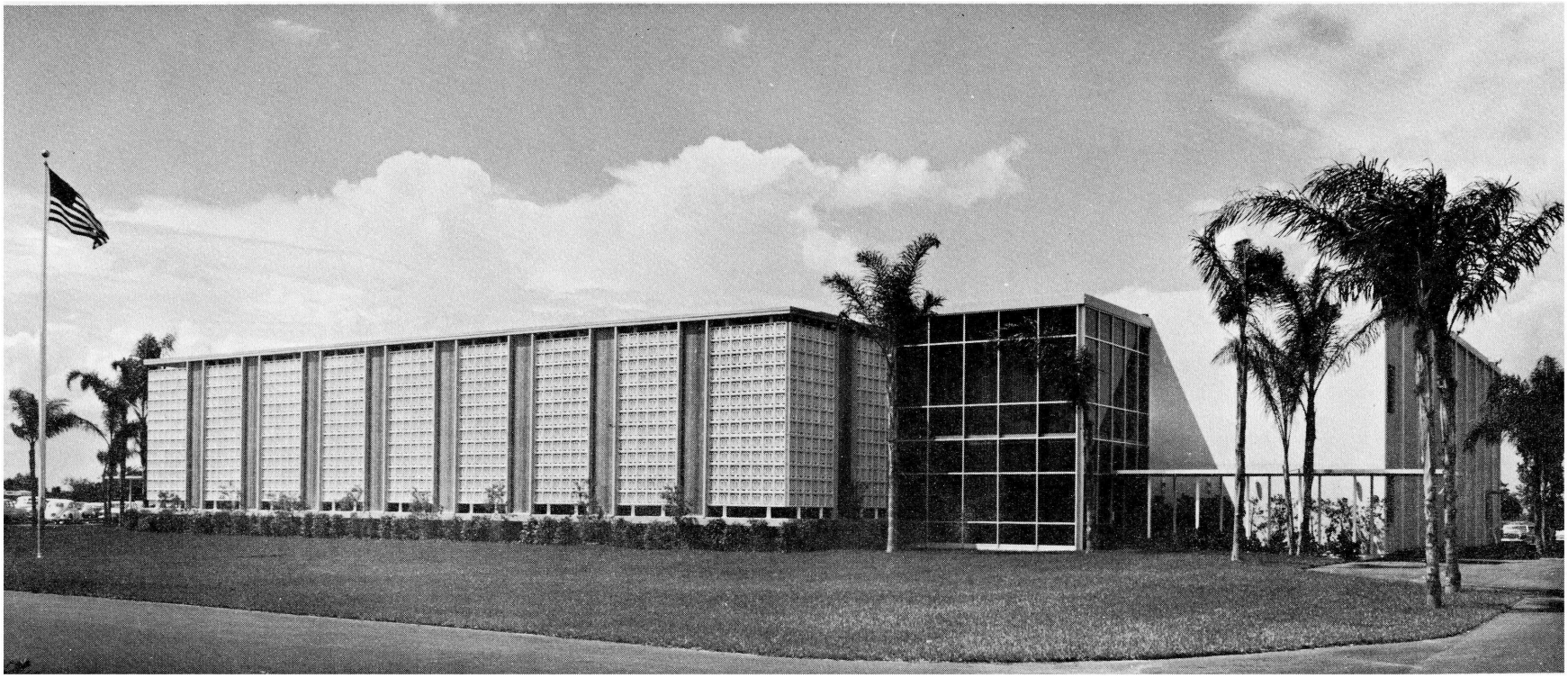
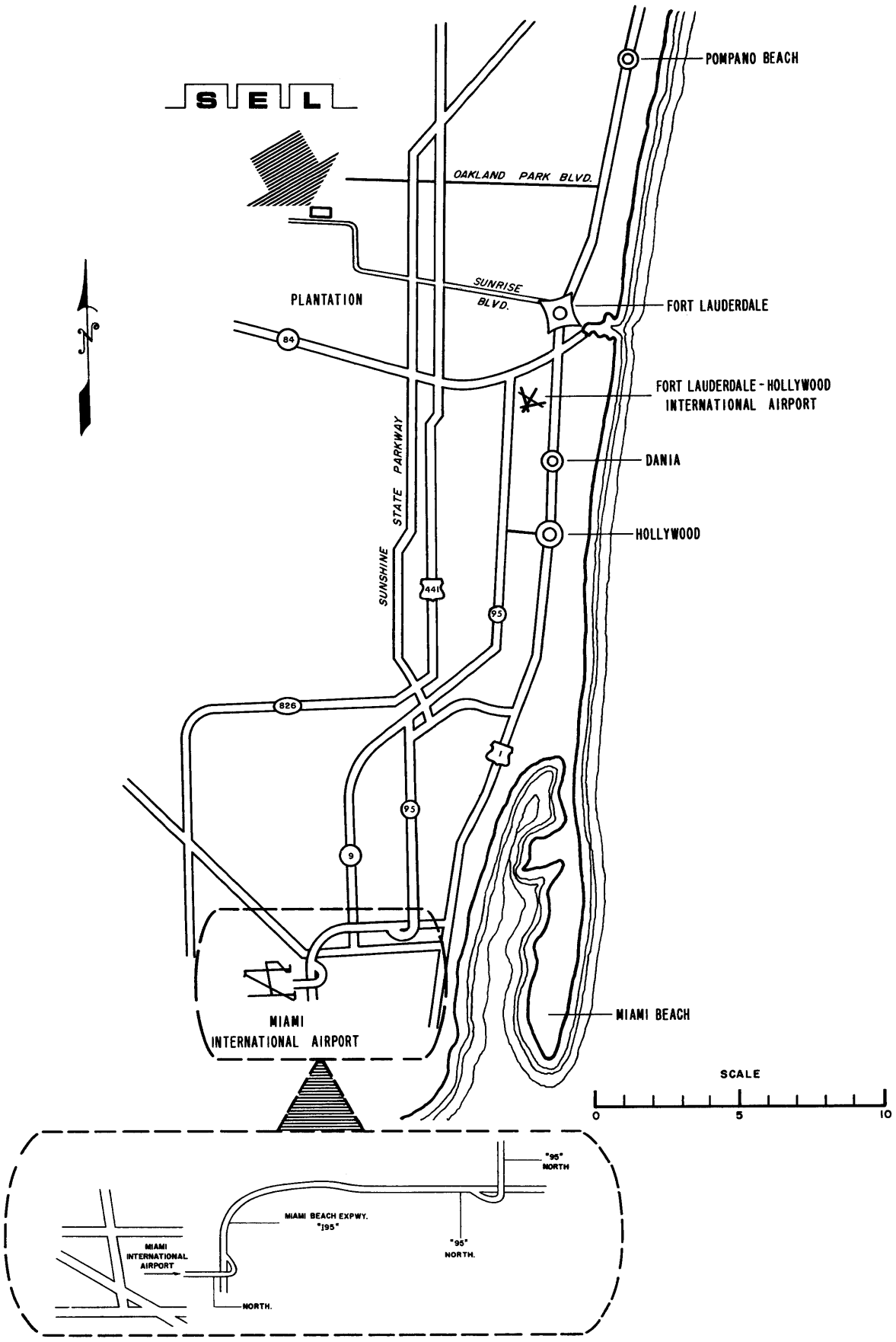


SECOND FLOOR





SEL® SYSTEMS ENGINEERING LABORATORIES, INCORPORATED
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APPENDIX