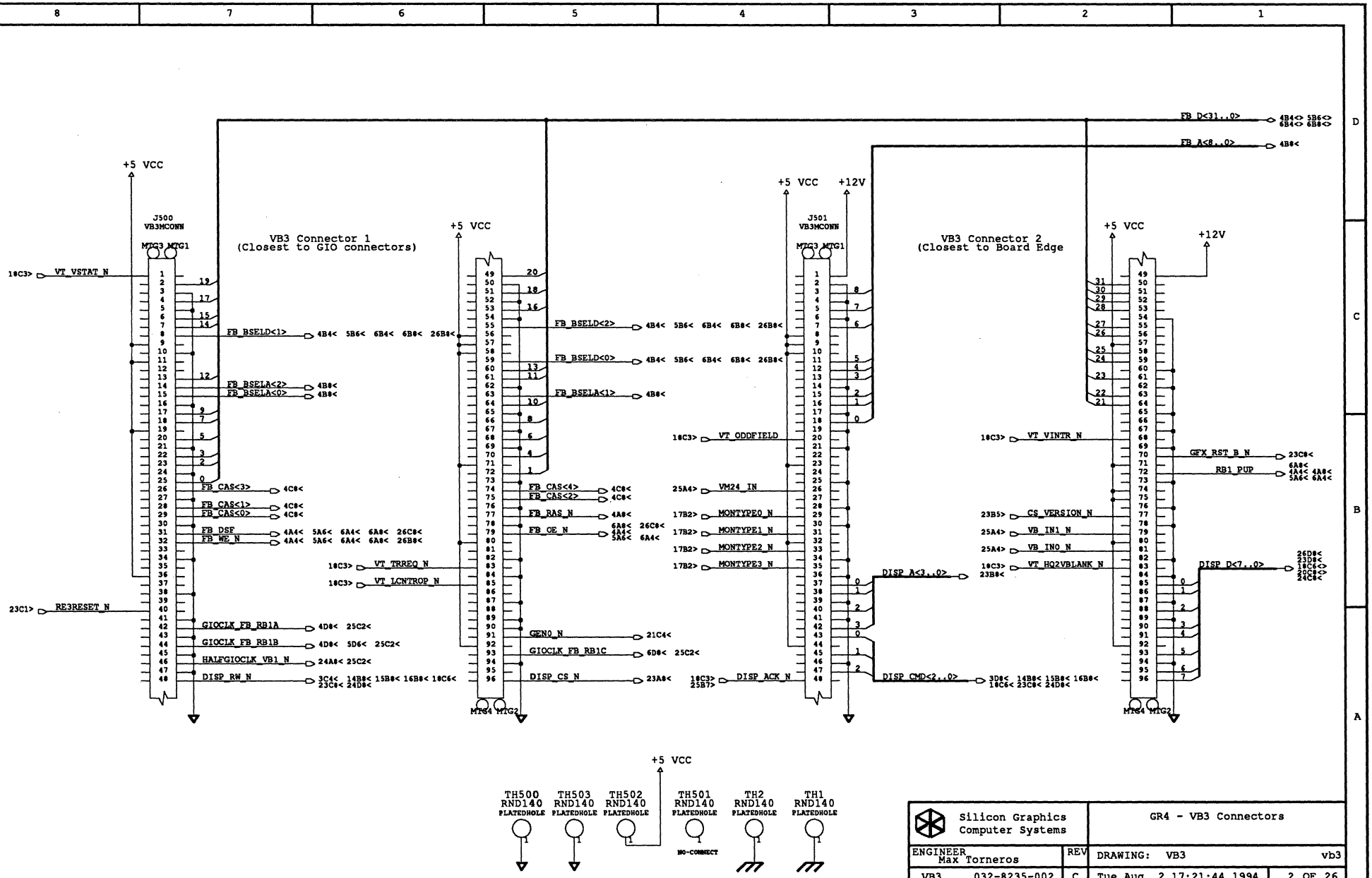
VB3 INDY XZ Graphics

Silicon Graphics Computer Systems - Digital Sight & Sound

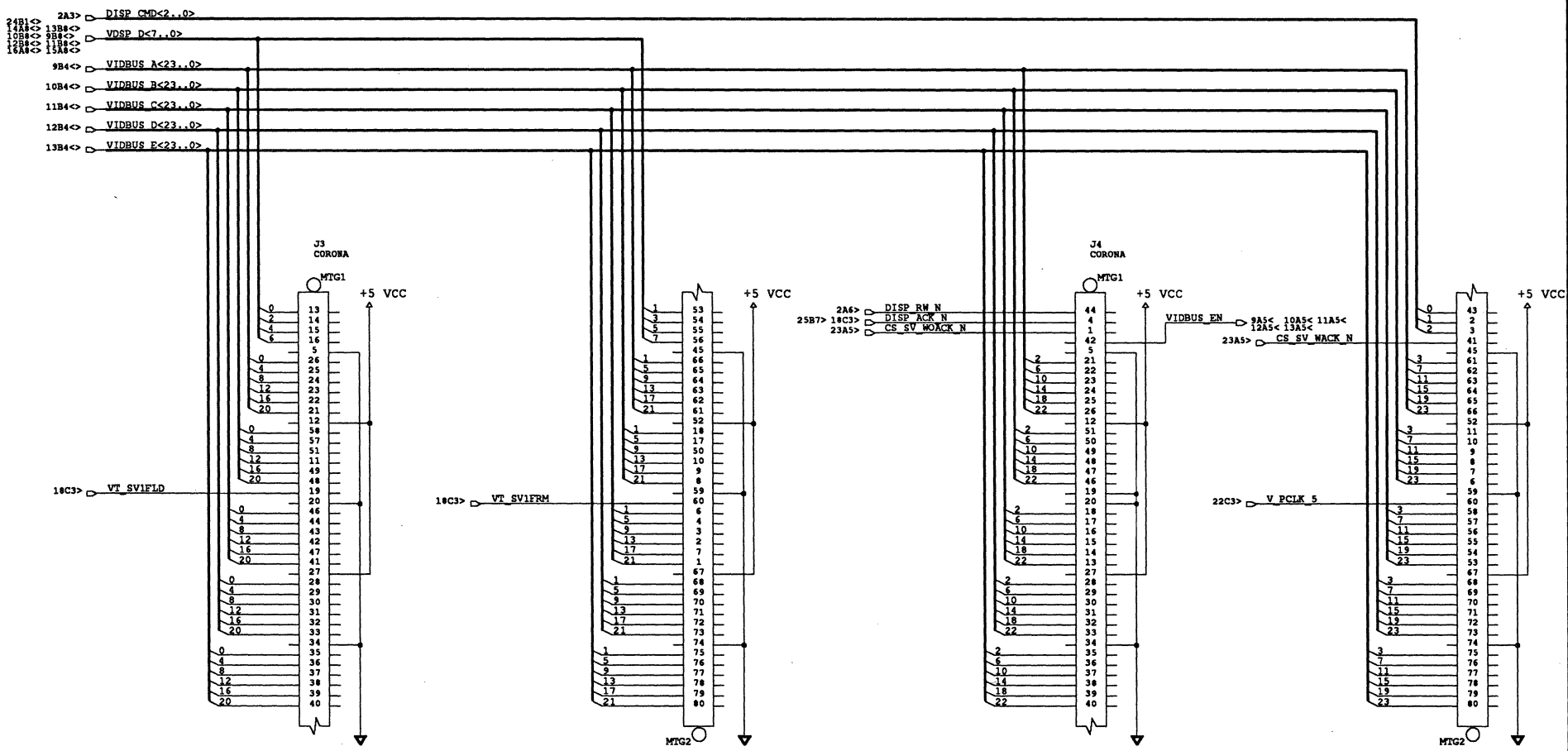
APPROVALS	DATE
DRW Max Torneros	09/23/93
CHK xxx	xxx
RLS xxx	xxx
RLS xxx	xxx

NP00 VB3 VB3 vb3

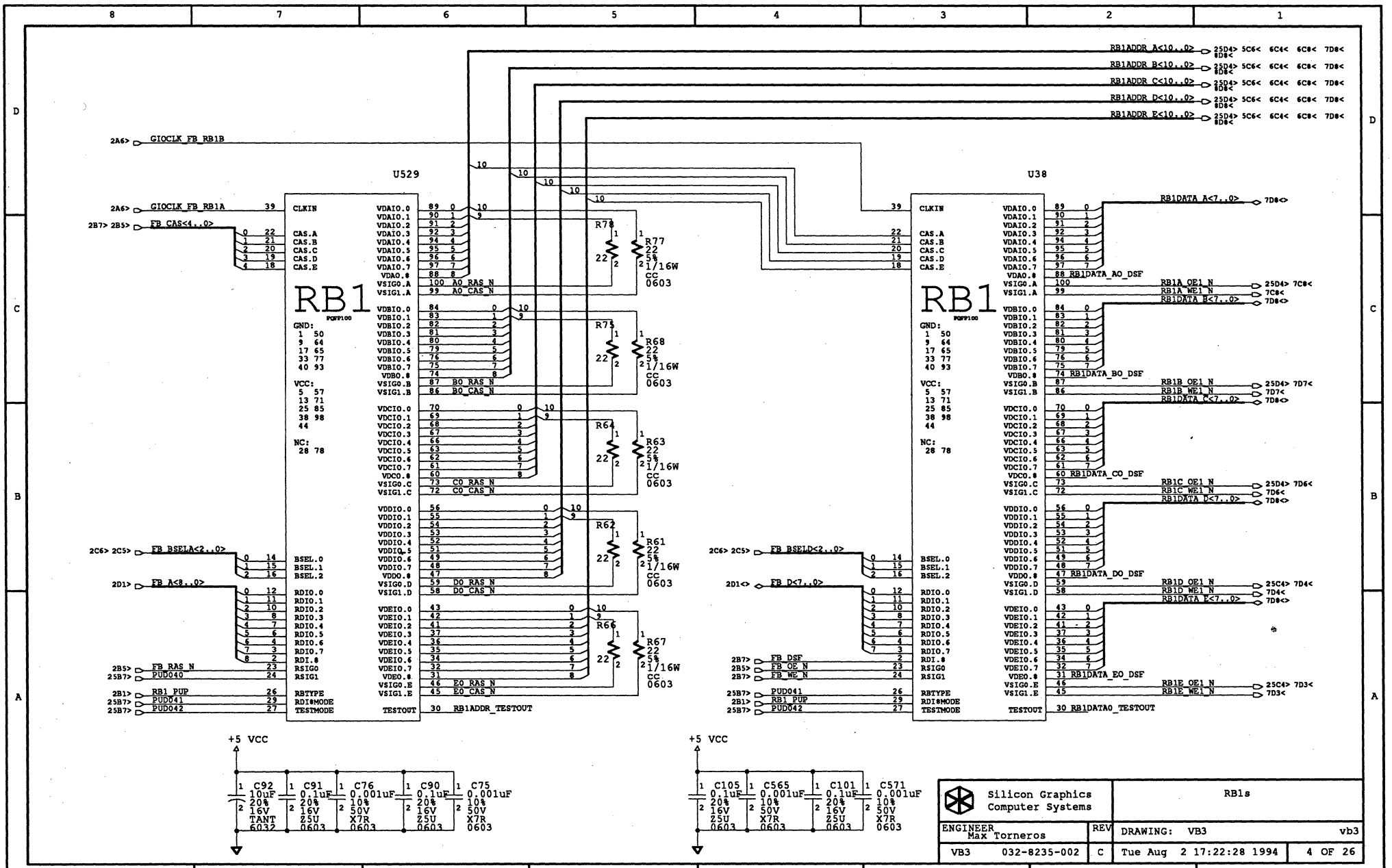
DRAWING	REV	DATE	SHEET
032-8235-002	C	Tue Aug 2 17:21:18 1994	1 OF 26



Silicon Graphics Computer Systems		GR4 - VB3 Connectors	
ENGINEER Max Torneros	REV	DRAWING: VB3	vb3
VB3 032-8235-002	C	Tue Aug 2 17:21:44 1994	2 OF 26



Silicon Graphics Computer Systems		CORONA Connectors	
ENGINEER Max Torneros	REV	DRAWING: VB3	vb3
VB3 032-8235-002	C	Tue Aug 2 17:22:04 1994	3 OF 26


RB1ADDR A<10..0>
RB1ADDR B<10..0>
RB1ADDR C<10..0>
RB1ADDR D<10..0>
RB1ADDR E<10..0>
GIOCLK_FB_RB1B
U529
U38
RB1
GIOCLK_FB_RB1A
FB_CAS<4..0>
FB_BSELA<2..0>
FB A<8..0>
FB_RAS_N
PUD040
RB1_PUP
PUD041
PUD042
A0_RAS_N
A0_CAS_N
B0_RAS_N
B0_CAS_N
C0_RAS_N
C0_CAS_N
D0_RAS_N
D0_CAS_N
E0_RAS_N
E0_CAS_N
RB1ADDR_TESTOUT
RB1DATA A<7..0>
RB1DATA B<7..0>
RB1DATA C<7..0>
RB1DATA D<7..0>
RB1DATA E<7..0>
RB1DATA_AO_DSF
RB1DATA_BO_DSF
RB1DATA_CO_DSF
RB1DATA_DO_DSF
RB1DATA_EO_DSF
RB1DATAO_TESTOUT
FB_BSELD<2..0>
FB_D<7..0>
FB_DSF
FB_OE_N
FB_WE_N
RB1A_OE1_N
RB1A_WE1_N
RB1B_OE1_N
RB1B_WE1_N
RB1C_OE1_N
RB1C_WE1_N
RB1D_OE1_N
RB1D_WE1_N
RB1E_OE1_N
RB1E_WE1_N
+5 VCC
C92 10uF 20% 16V TANT 6032
C91 0.1uF 20% 16V Z5U 0603
C76 0.001uF 10% 50V X7R 0603
C90 0.1uF 20% 16V Z5U 0603
C75 0.001uF 10% 50V X7R 0603
C105 0.1uF 20% 16V Z5U 0603
C565 0.001uF 10% 50V X7R 0603
C101 0.1uF 20% 16V Z5U 0603
C571 0.001uF 10% 50V X7R 0603
Silicon Graphics Computer Systems
RB1s
ENGINEER Max Torneros
REV
DRAWING: VB3
vb3
VB3 032-8235-002 C
Tue Aug 2 17:22:28 1994
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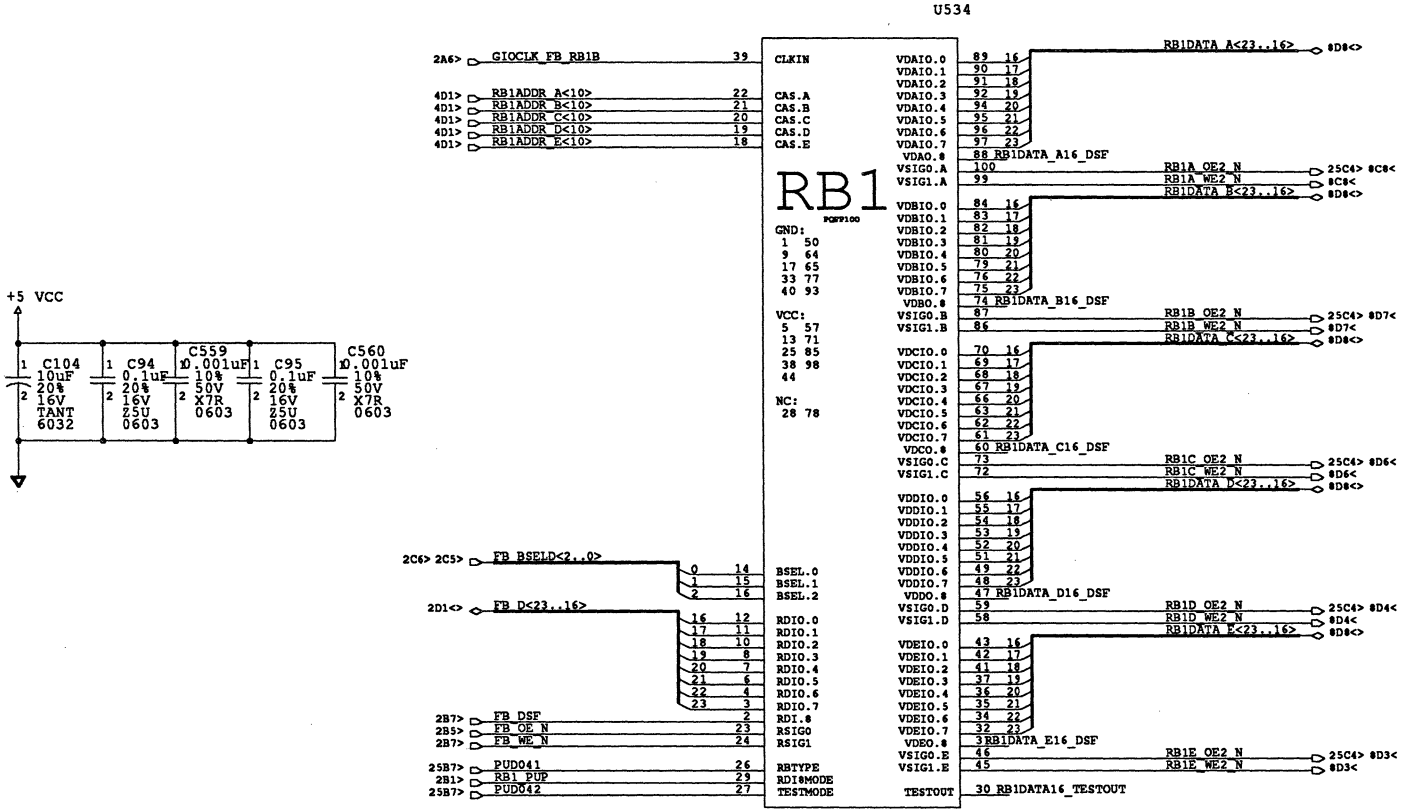

Silicon Graphics Computer Systems			RB1s, Cont.
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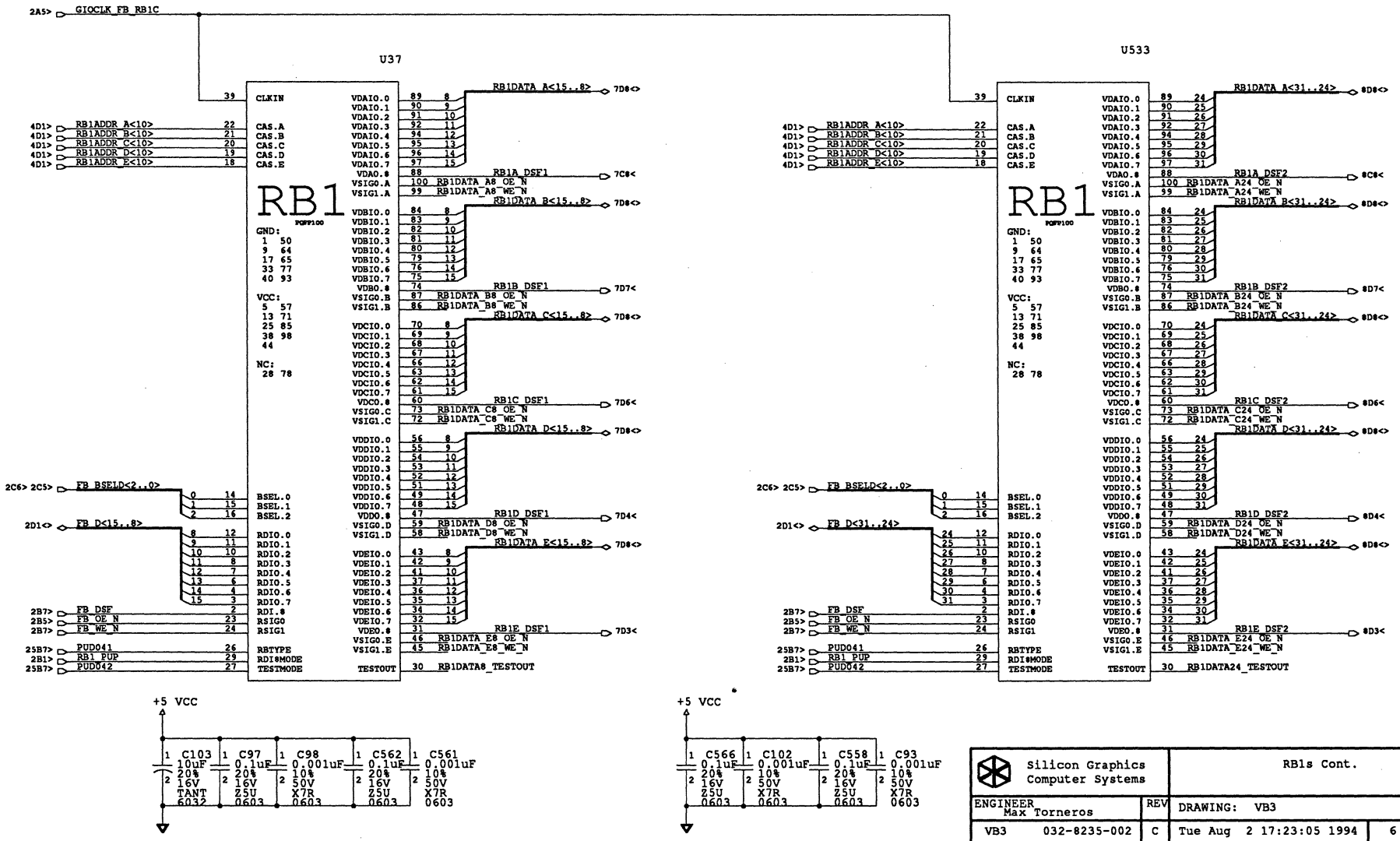
VB3 032-8235-002	C	Tue Aug 2 17:22:45 1994	5 OF 26



Silicon Graphics Computer Systems		RB1s Cont.	
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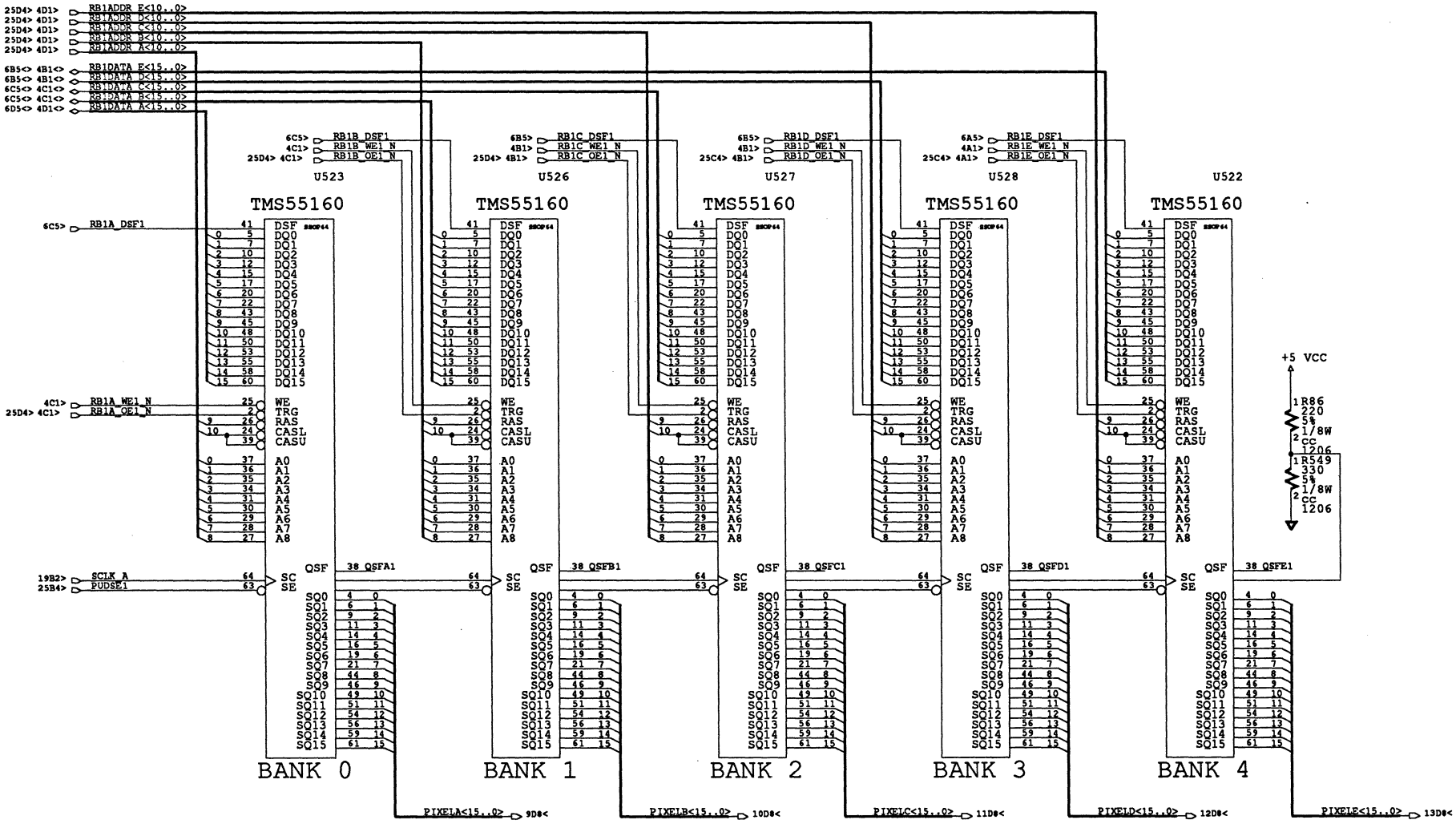
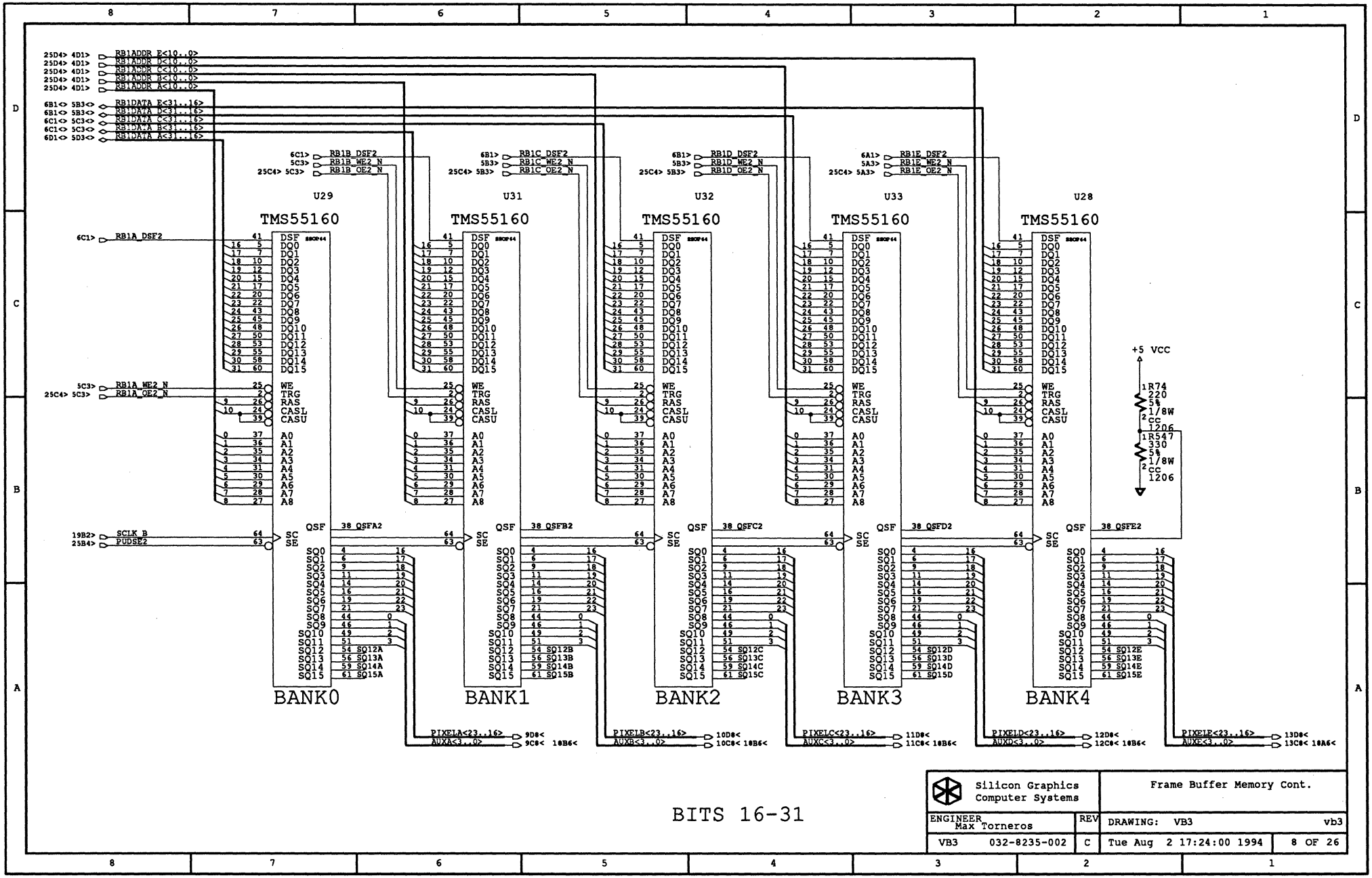
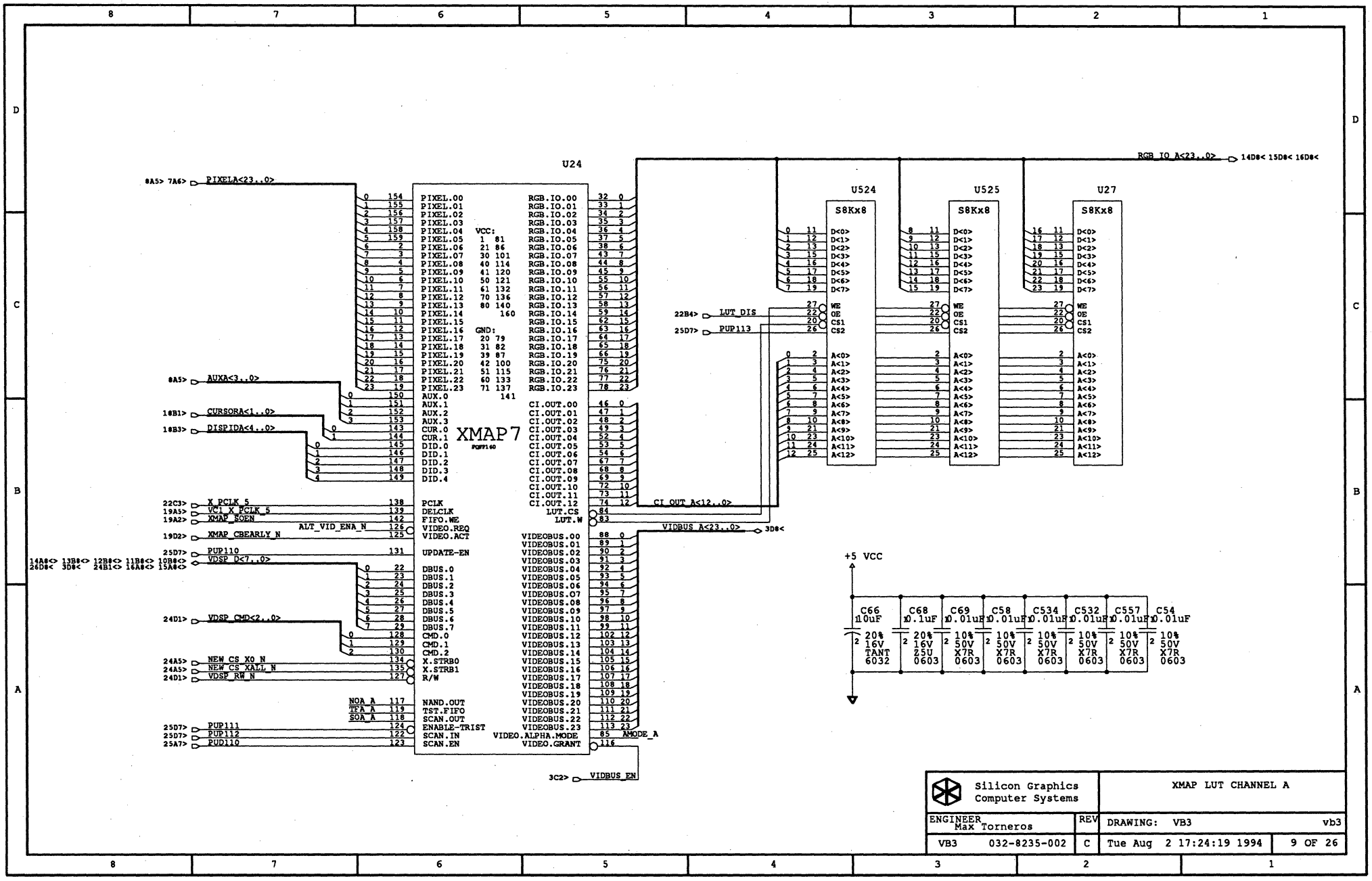
VB3 032-8235-002	C	Tue Aug 2 17:23:05 1994	6 OF 26



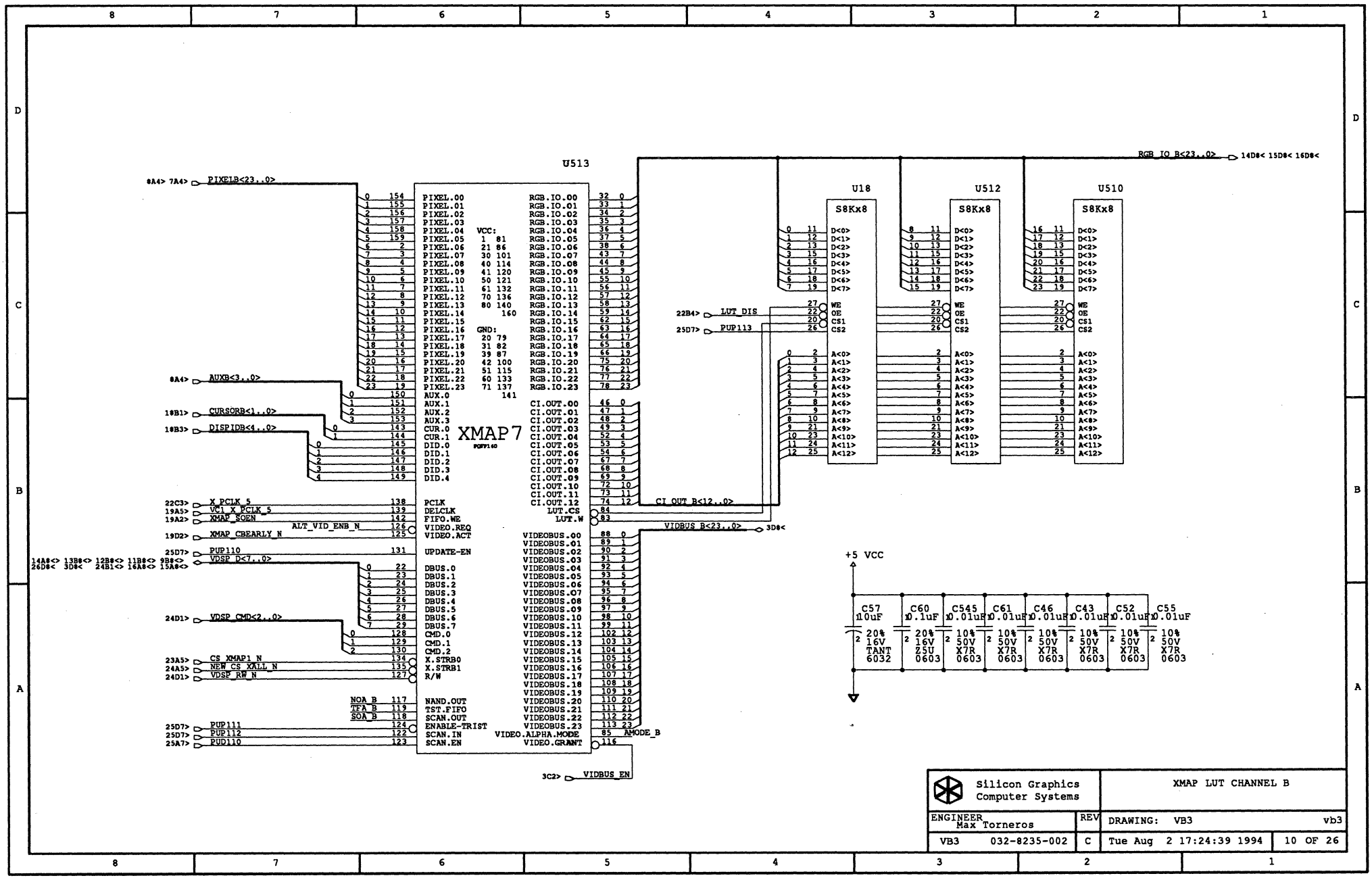
BITS 0-15

Silicon Graphics Computer Systems			Frame Buffer Memory
ENGINEER Max Torneros		REV	DRAWING: VB3 vb3
VB3	032-8235-002	C	Tue Aug 2 17:23:39 1994 7 OF 26


RB1ADDR E<10..0>
RB1ADDR D<10..0>
RB1ADDR C<10..0>
RB1ADDR B<10..0>
RB1ADDR A<10..0>
RB1DATA E<31..16>
RB1DATA D<31..16>
RB1DATA C<31..16>
RB1DATA B<31..16>
RB1DATA A<31..16>
RB1B_DSF2
RB1B_WE2_N
RB1B_OE2_N
RB1C_DSF2
RB1C_WE2_N
RB1C_OE2_N
RB1D_DSF2
RB1D_WE2_N
RB1D_OE2_N
RB1E_DSF2
RB1E_WE2_N
RB1E_OE2_N
RB1A_DSF2
RB1A_WE2_N
RB1A_OE2_N
SCLK_B
PUDSE2
U29
U31
U32
U33
U28
TMS55160
DSF
WE
TRG
RAS
CASL
CASU
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
A0
A1
A2
A3
A4
A5
A6
A7
A8
QSF
SC
SE
38 QSFA2
38 QSFB2
38 QSFC2
38 QSFD2
38 QSFE2
SQ0
SQ1
SQ2
SQ3
SQ4
SQ5
SQ6
SQ7
SQ8
SQ9
SQ10
SQ11
SQ12
SQ13
SQ14
SQ15
54 SQ12A
56 SQ13A
59 SQ14A
61 SQ15A
54 SQ12B
56 SQ13B
59 SQ14B
61 SQ15B
54 SQ12C
56 SQ13C
59 SQ14C
61 SQ15C
54 SQ12D
56 SQ13D
59 SQ14D
61 SQ15D
54 SQ12E
56 SQ13E
59 SQ14E
61 SQ15E
BANK0
BANK1
BANK2
BANK3
BANK4
+5 VCC
1R74
220
5%
1/8W
CC
1206
1R547
330
5%
1/8W
CC
1206
PIXELA<23..16>
AUXA<3..0>
PIXELB<23..16>
AUXB<3..0>
PIXELC<23..16>
AUXC<3..0>
PIXELD<23..16>
AUXD<3..0>
PIXELE<23..16>
AUXE<3..0>
BITS 16-31
Silicon Graphics
Computer Systems
Frame Buffer Memory Cont.
ENGINEER
Max Torneros
REV
DRAWING: VB3
vb3
VB3
032-8235-002
C
Tue Aug 2 17:24:00 1994
8 OF 26



Silicon Graphics Computer Systems		XMAP LUT CHANNEL A	
ENGINEER Max Torneros	REV	DRAWING: VB3	vb3
VB3 032-8235-002	C	Tue Aug 2 17:24:19 1994	9 OF 26


U513
XMAP7
PQFP160
PIXEL.00
PIXEL.01
PIXEL.02
PIXEL.03
PIXEL.04
PIXEL.05
PIXEL.06
PIXEL.07
PIXEL.08
PIXEL.09
PIXEL.10
PIXEL.11
PIXEL.12
PIXEL.13
PIXEL.14
PIXEL.15
PIXEL.16
PIXEL.17
PIXEL.18
PIXEL.19
PIXEL.20
PIXEL.21
PIXEL.22
PIXEL.23
AUX.0
AUX.1
AUX.2
AUX.3
CUR.0
CUR.1
DID.0
DID.1
DID.2
DID.3
DID.4
PCLK
DELCLK
FIFO.WE
VIDEO.REQ
VIDEO.ACT
UPDATE-EN
DBUS.0
DBUS.1
DBUS.2
DBUS.3
DBUS.4
DBUS.5
DBUS.6
DBUS.7
CMD.0
CMD.1
CMD.2
X.STRB0
X.STRB1
R/W
NAND.OUT
TST.FIFO
SCAN.OUT
ENABLE-TRIST
SCAN.IN
SCAN.EN
VCC:
GND:
RGB.IO.00
RGB.IO.01
RGB.IO.02
RGB.IO.03
RGB.IO.04
RGB.IO.05
RGB.IO.06
RGB.IO.07
RGB.IO.08
RGB.IO.09
RGB.IO.10
RGB.IO.11
RGB.IO.12
RGB.IO.13
RGB.IO.14
RGB.IO.15
RGB.IO.16
RGB.IO.17
RGB.IO.18
RGB.IO.19
RGB.IO.20
RGB.IO.21
RGB.IO.22
RGB.IO.23
CI.OUT.00
CI.OUT.01
CI.OUT.02
CI.OUT.03
CI.OUT.04
CI.OUT.05
CI.OUT.06
CI.OUT.07
CI.OUT.08
CI.OUT.09
CI.OUT.10
CI.OUT.11
CI.OUT.12
LUT.CS
LUT.W
VIDEOBUS.00
VIDEOBUS.01
VIDEOBUS.02
VIDEOBUS.03
VIDEOBUS.04
VIDEOBUS.05
VIDEOBUS.06
VIDEOBUS.07
VIDEOBUS.08
VIDEOBUS.09
VIDEOBUS.10
VIDEOBUS.11
VIDEOBUS.12
VIDEOBUS.13
VIDEOBUS.14
VIDEOBUS.15
VIDEOBUS.16
VIDEOBUS.17
VIDEOBUS.18
VIDEOBUS.19
VIDEOBUS.20
VIDEOBUS.21
VIDEOBUS.22
VIDEOBUS.23
VIDEO.ALPHA.MODE
VIDEO.GRANT
8A4> 7A4> PIXELB<23..0>
8A4> AUXB<3..0>
19B1> CURSORB<1..0>
19B3> DISPIDB<4..0>
22C3> X_PCLK_5
19A5> VC1_X_PCLK_5
19A2> XMAP_SOEN
ALT_VID_ENB_N
19D2> XMAP_CBEARLY_N
25D7> PUP110
14A8<> 13B8<> 12B8<> 11B8<> 9B8<>
26D8< 3D8< 24B1<> 16A8<> 15A8<>
VDSP_D<7..0>
24D1> VDSP_CMD<2..0>
23A5> CS_XMAP1_N
24A5> NEW_CS_XALL_N
24D1> VDSP_RW_N
NOA_B
TEA_B
SOA_B
25D7> PUP111
25D7> PUP112
25A7> PUD110
VIDBUS_B<23..0>
3D8<
3C2> VIDBUS_EN
AMODE_B
RGB_IO_B<23..0>
14D8< 15D8< 16D8<
CI_OUT_B<12..0>
22B4> LUT_DIS
25D7> PUP113
U18
U512
U510
S8Kx8
D<0>
D<1>
D<2>
D<3>
D<4>
D<5>
D<6>
D<7>
WE
OE
CS1
CS2
A<0>
A<1>
A<2>
A<3>
A<4>
A<5>
A<6>
A<7>
A<8>
A<9>
A<10>
A<11>
A<12>
+5 VCC
C57 10uF 20% 16V TANT 6032
C60 0.1uF 20% 16V Z5U 0603
C545 0.01uF 10% 50V X7R 0603
C61 0.01uF 10% 50V X7R 0603
C46 0.01uF 10% 50V X7R 0603
C43 0.01uF 10% 50V X7R 0603
C52 0.01uF 10% 50V X7R 0603
C55 0.01uF 10% 50V X7R 0603
Silicon Graphics
Computer Systems
XMAP LUT CHANNEL B
ENGINEER
Max Torneros
REV
DRAWING: VB3
vb3
VB3 032-8235-002
C
Tue Aug 2 17:24:39 1994
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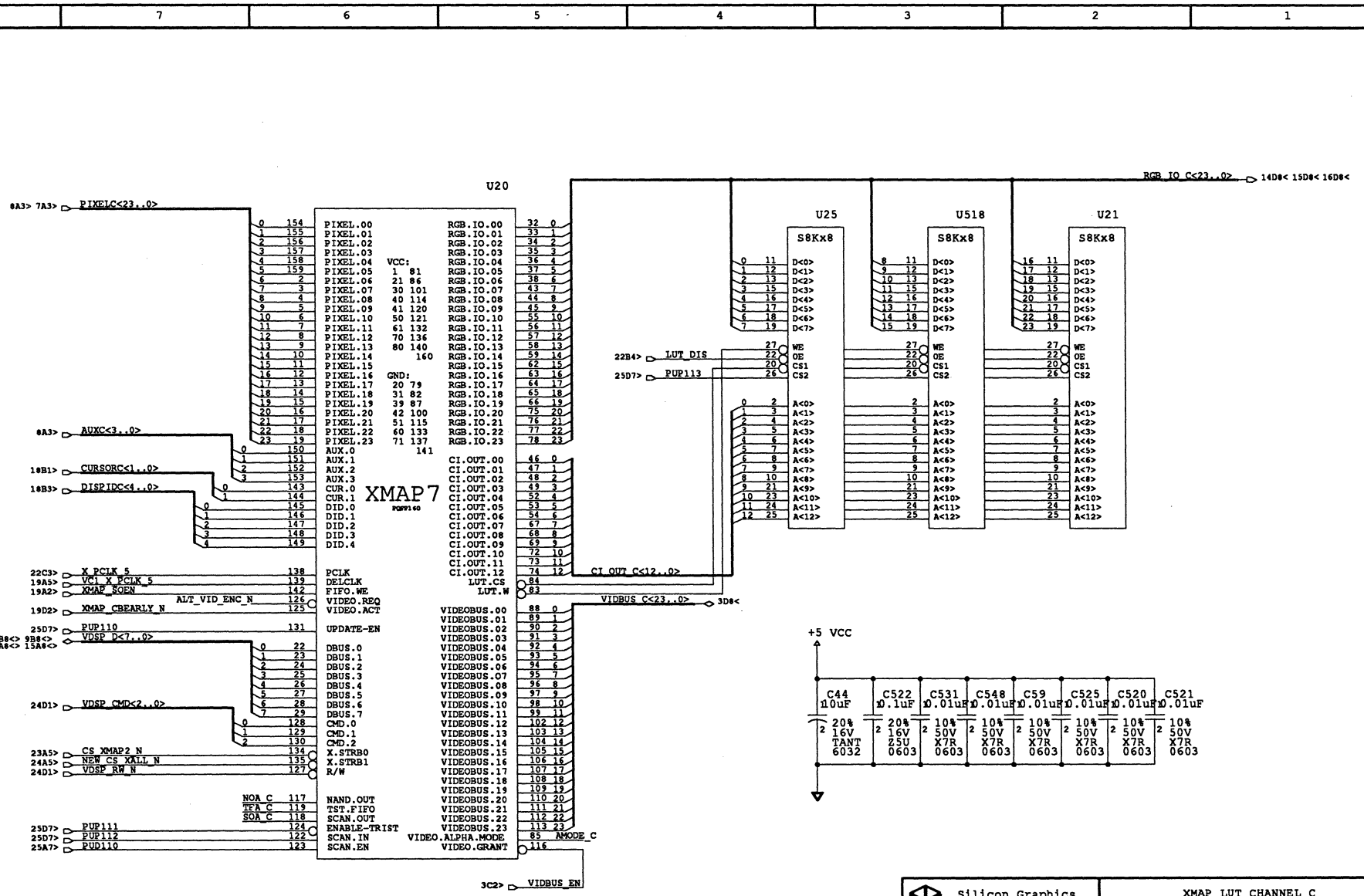
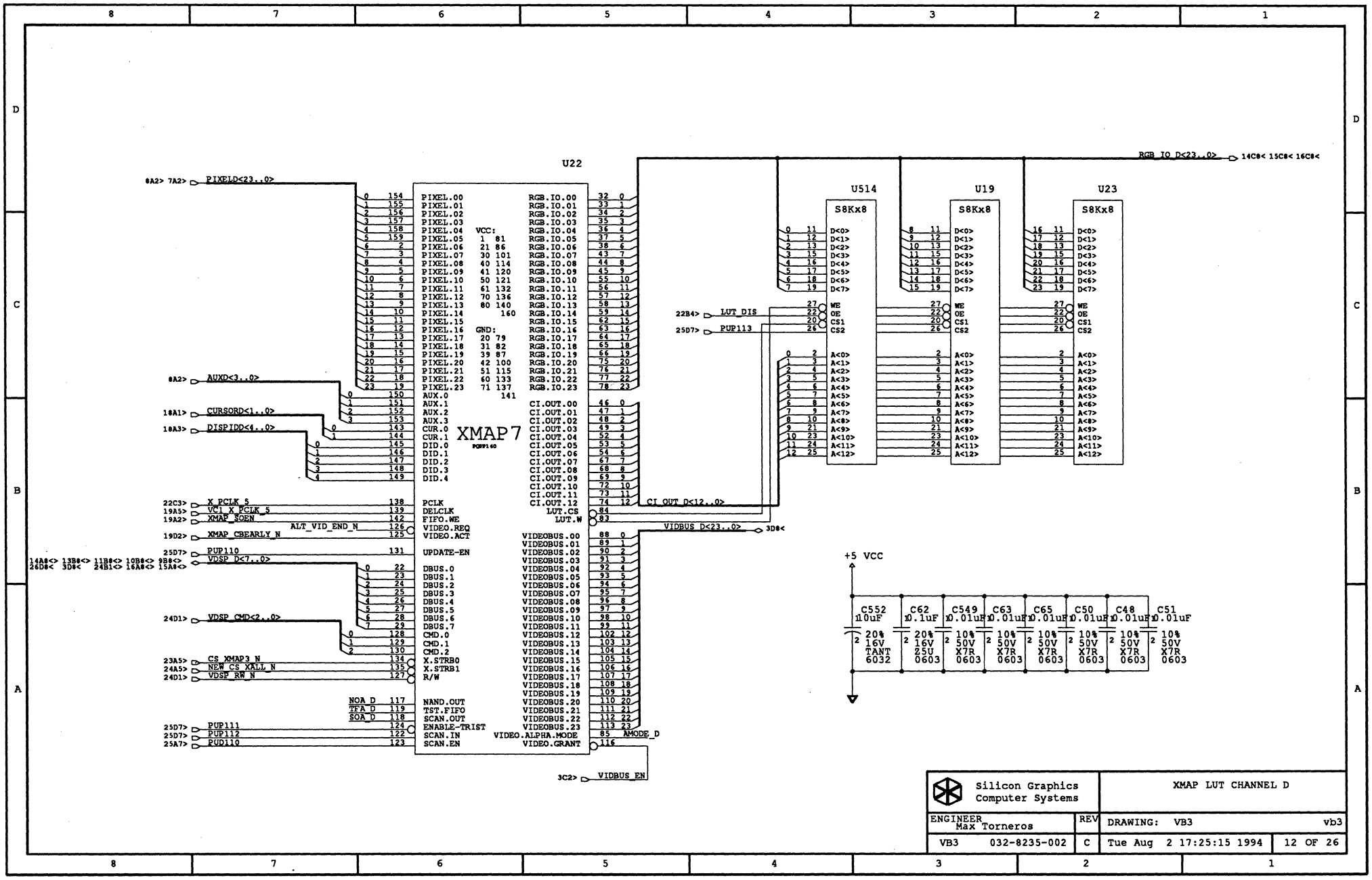


Silicon Graphics Computer Systems		XMAP LUT CHANNEL C	
ENGINEER Max Torneros	REV	DRAWING: VB3	vb3
VB3 032-8235-002	C	Tue Aug 2 17:24:57 1994	11 OF 26


U22
XMAP7
PGFP140
PIXELD<23..0>
AUXD<3..0>
CURSORD<1..0>
DISPIDD<4..0>
X_PCLK_5
VC1_X_PCLK_5
XMAP_SOEN
ALT_VID_END_N
XMAP_CBEARLY_N
PUP110
VDSP_D<7..0>
VDSP_CMD<2..0>
CS_XMAP3_N
NEW_CS_XALL_N
VDSP_RW_N
PUP111
PUP112
PUD110
PIXEL.00
PIXEL.01
PIXEL.02
PIXEL.03
PIXEL.04
PIXEL.05
PIXEL.06
PIXEL.07
PIXEL.08
PIXEL.09
PIXEL.10
PIXEL.11
PIXEL.12
PIXEL.13
PIXEL.14
PIXEL.15
PIXEL.16
PIXEL.17
PIXEL.18
PIXEL.19
PIXEL.20
PIXEL.21
PIXEL.22
PIXEL.23
AUX.0
AUX.1
AUX.2
AUX.3
CUR.0
CUR.1
DID.0
DID.1
DID.2
DID.3
DID.4
PCLK
DELCLK
FIFO.WE
VIDEO.REQ
VIDEO.ACT
UPDATE-EN
DBUS.0
DBUS.1
DBUS.2
DBUS.3
DBUS.4
DBUS.5
DBUS.6
DBUS.7
CMD.0
CMD.1
CMD.2
X.STRB0
X.STRB1
R/W
NAND.OUT
TST.FIFO
SCAN.OUT
ENABLE-TRIST
SCAN.IN
SCAN.EN
VCC:
GND:
RGB.IO.00
RGB.IO.01
RGB.IO.02
RGB.IO.03
RGB.IO.04
RGB.IO.05
RGB.IO.06
RGB.IO.07
RGB.IO.08
RGB.IO.09
RGB.IO.10
RGB.IO.11
RGB.IO.12
RGB.IO.13
RGB.IO.14
RGB.IO.15
RGB.IO.16
RGB.IO.17
RGB.IO.18
RGB.IO.19
RGB.IO.20
RGB.IO.21
RGB.IO.22
RGB.IO.23
CI.OUT.00
CI.OUT.01
CI.OUT.02
CI.OUT.03
CI.OUT.04
CI.OUT.05
CI.OUT.06
CI.OUT.07
CI.OUT.08
CI.OUT.09
CI.OUT.10
CI.OUT.11
CI.OUT.12
LUT.CS
LUT.W
VIDEOBUS.00
VIDEOBUS.01
VIDEOBUS.02
VIDEOBUS.03
VIDEOBUS.04
VIDEOBUS.05
VIDEOBUS.06
VIDEOBUS.07
VIDEOBUS.08
VIDEOBUS.09
VIDEOBUS.10
VIDEOBUS.11
VIDEOBUS.12
VIDEOBUS.13
VIDEOBUS.14
VIDEOBUS.15
VIDEOBUS.16
VIDEOBUS.17
VIDEOBUS.18
VIDEOBUS.19
VIDEOBUS.20
VIDEOBUS.21
VIDEOBUS.22
VIDEOBUS.23
VIDEO.ALPHA.MODE
VIDEO.GRANT
NOA_D
TFA_D
SOA_D
AMODE_D
VIDBUS_EN
RGB_IO_D<23..0>
CI_OUT_D<12..0>
VIDBUS_D<23..0>
LUT_DIS
PUP113
U514
U19
U23
S8Kx8
WE
OE
CS1
CS2
D<0>
D<1>
D<2>
D<3>
D<4>
D<5>
D<6>
D<7>
A<0>
A<1>
A<2>
A<3>
A<4>
A<5>
A<6>
A<7>
A<8>
A<9>
A<10>
A<11>
A<12>
+5 VCC
C552 10uF 20% 16V TANT 6032
C62 0.1uF 20% 16V 25U 0603
C549 0.01uF 10% 50V X7R 0603
C63 0.01uF 10% 50V X7R 0603
C65 0.01uF 10% 50V X7R 0603
C50 0.01uF 10% 50V X7R 0603
C48 0.01uF 10% 50V X7R 0603
C51 0.01uF 10% 50V X7R 0603
Silicon Graphics Computer Systems
XMAP LUT CHANNEL D
ENGINEER Max Torneros
REV C
DRAWING: VB3 vb3
VB3 032-8235-002
Tue Aug 2 17:25:15 1994
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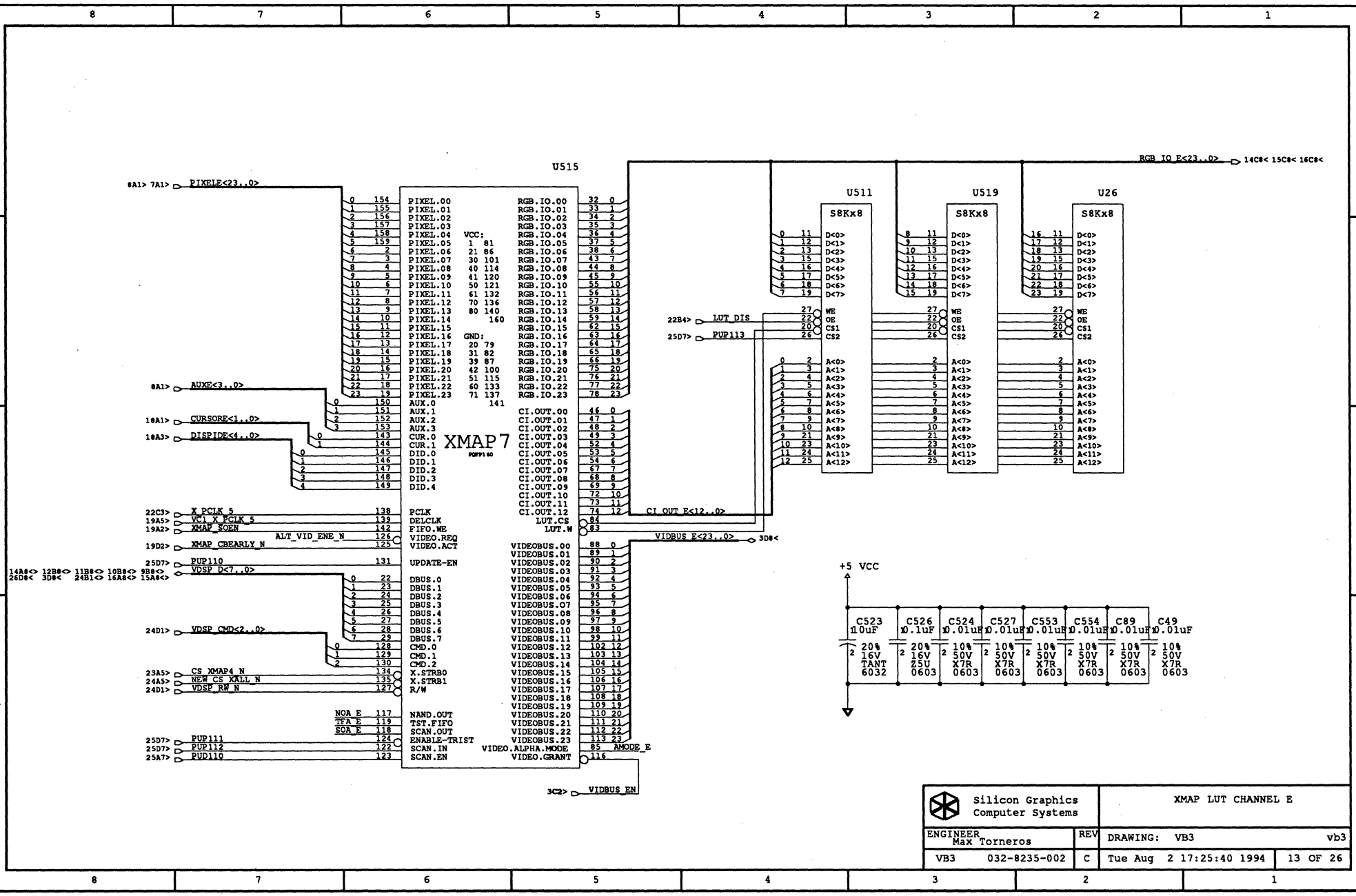
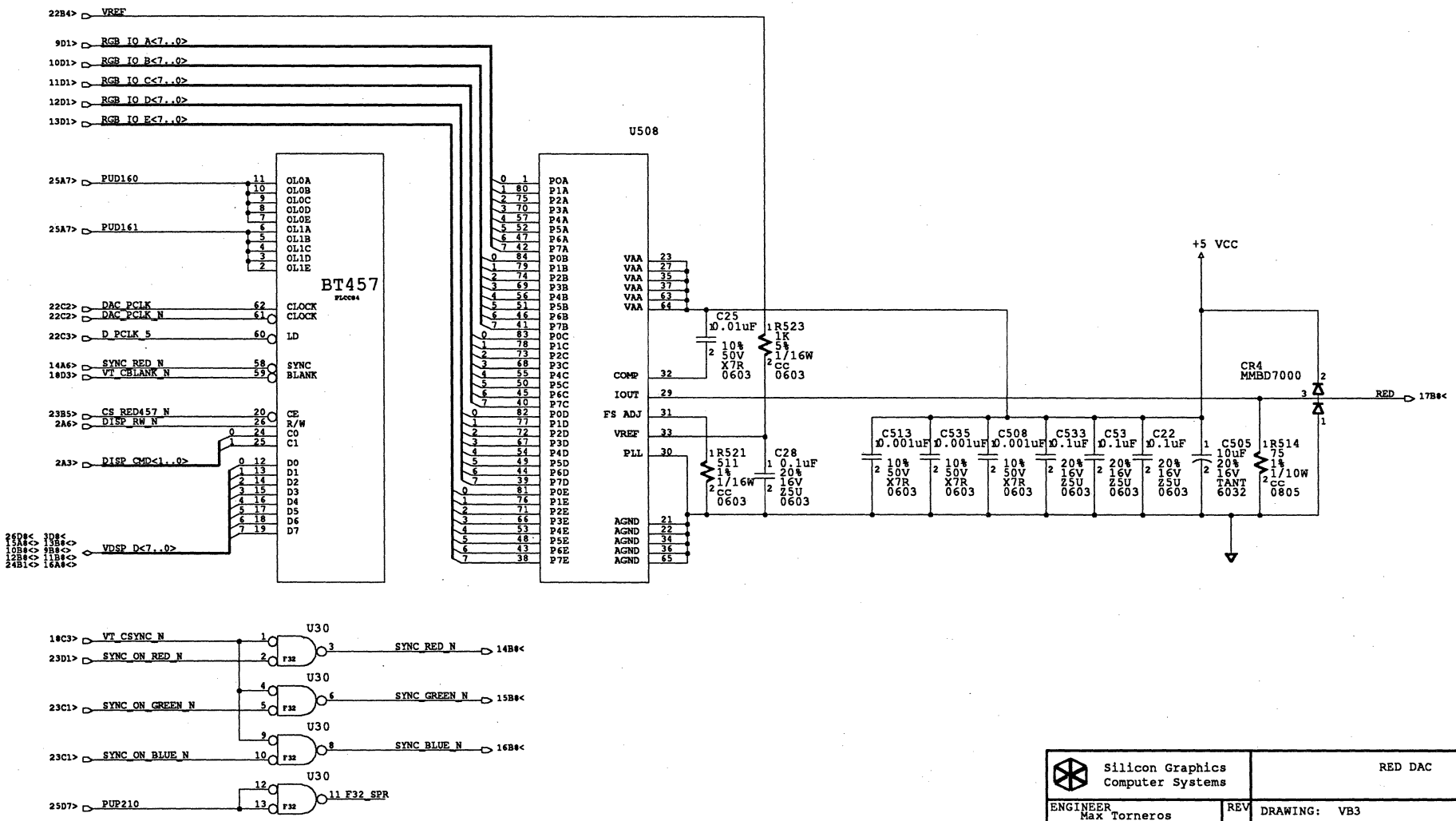
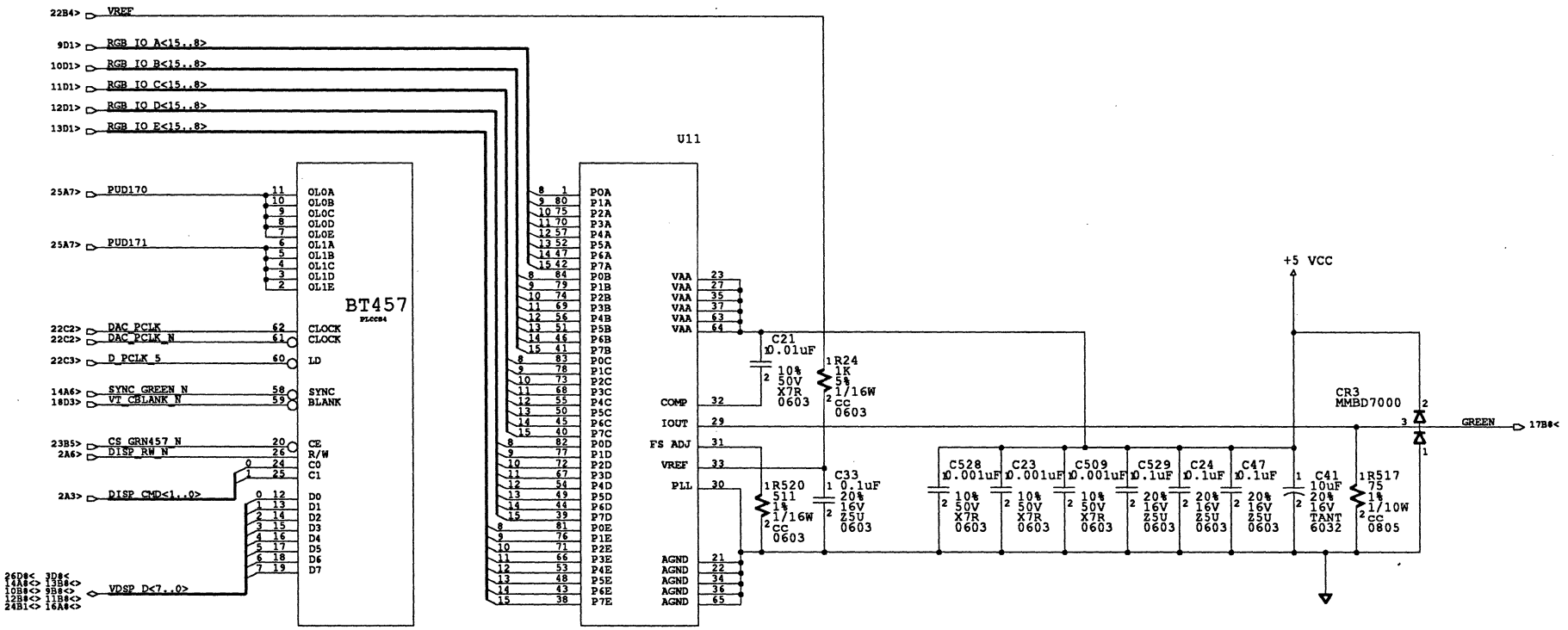


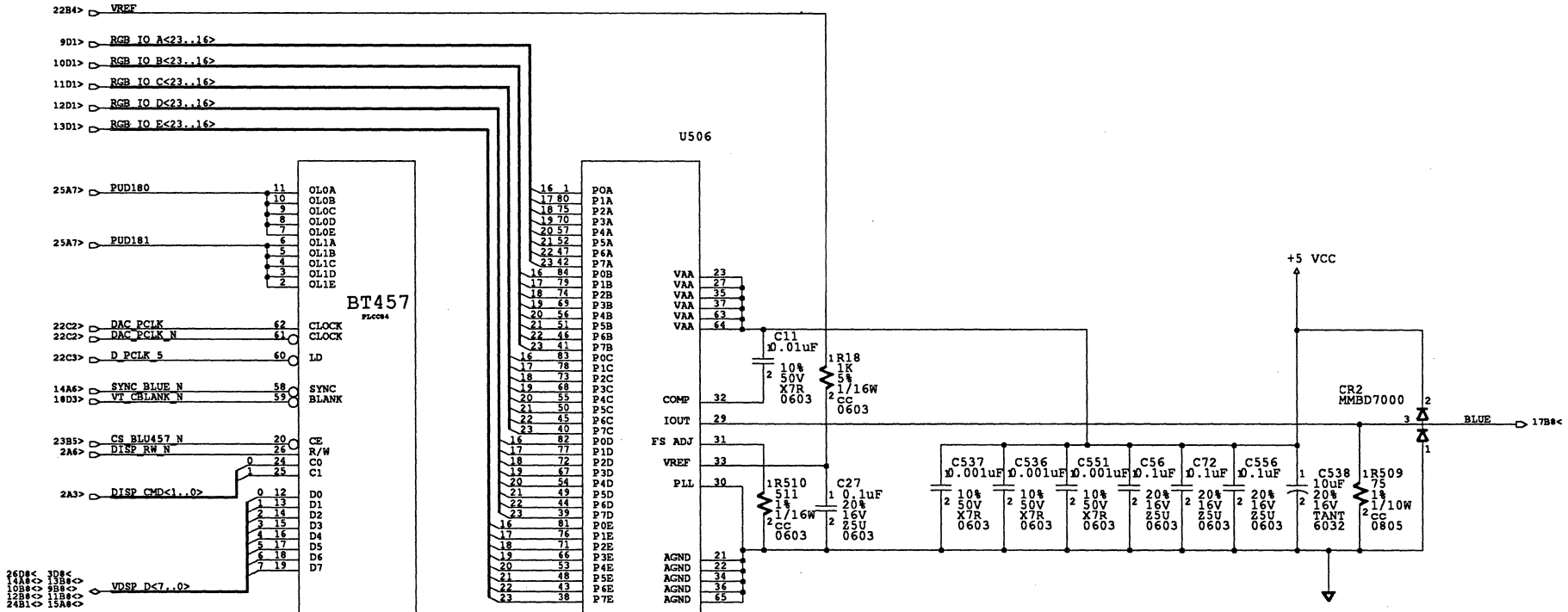
Silicon Graphics Computer Systems		XMAP LUT CHANNEL E	
ENGINEER Max Torneros	REV	DRAWING: VB3	vb3
VB3 032-8235-002	C	Tue Aug 2 17:25:40 1994	13 OF 26



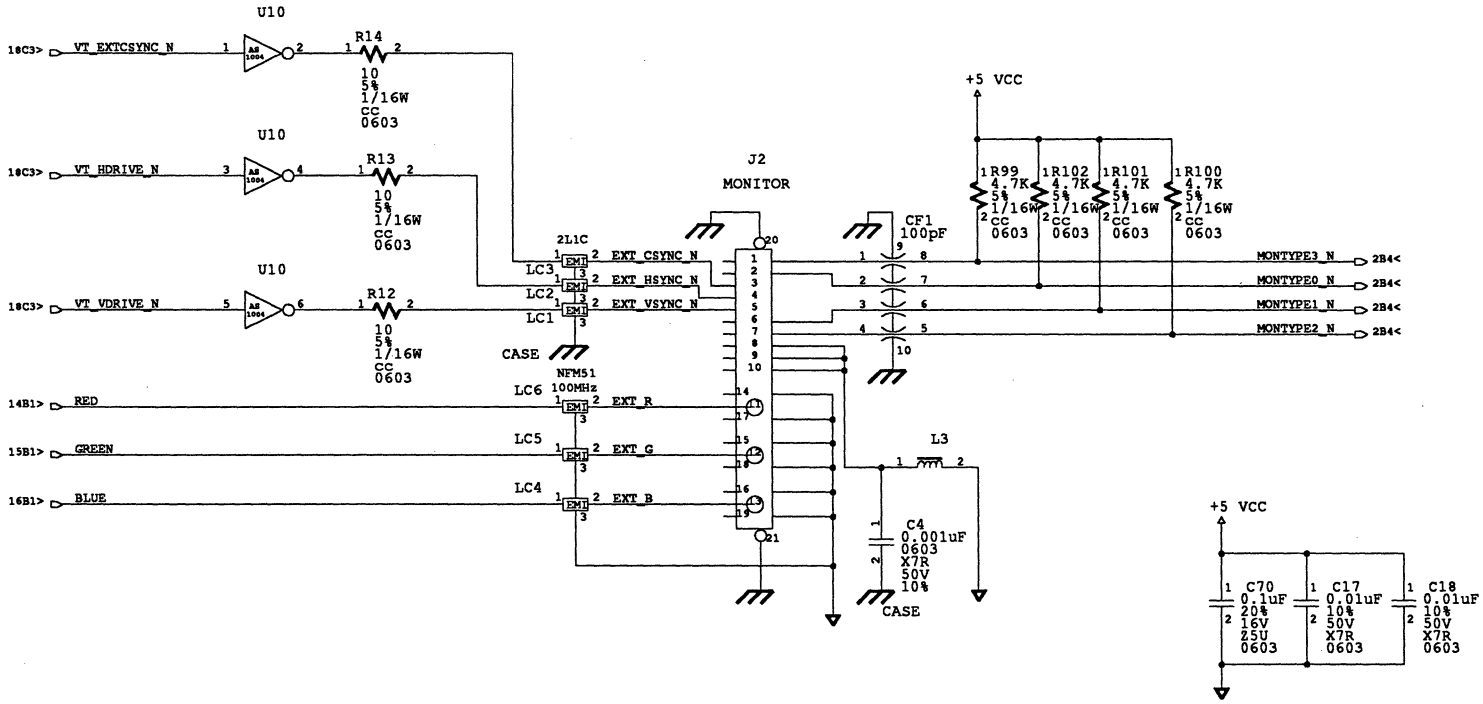
Silicon Graphics Computer Systems		RED DAC	
ENGINEER Max Torneros	REV	DRAWING: VB3	vb3
VB3 032-8235-002	C	Tue Aug 2 17:25:58 1994	14 OF 26



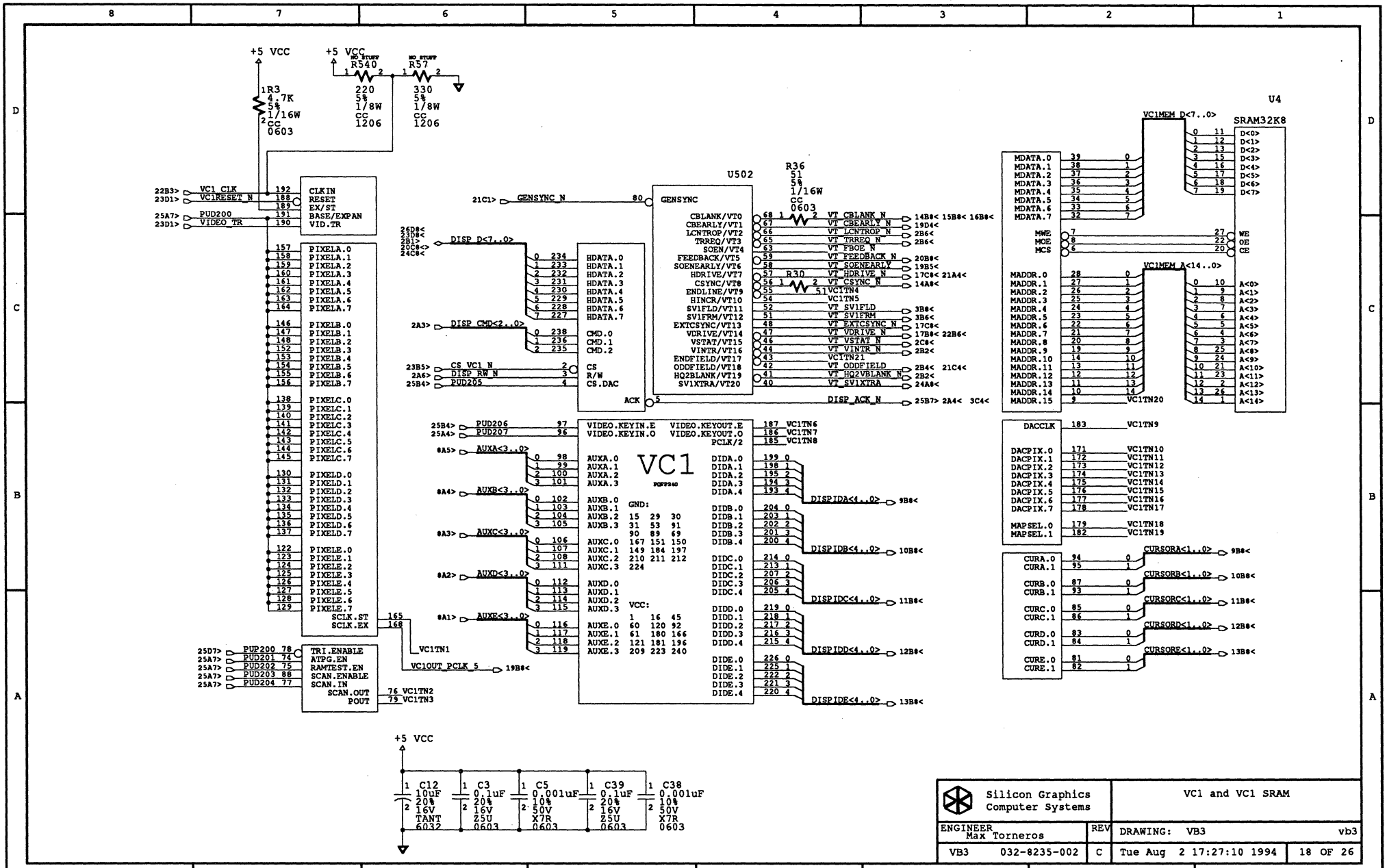
Silicon Graphics Computer Systems			GREEN DAC
ENGINEER Max Torneros	REV	DRAWING: VB3	vb3
VB3 032-8235-002	C	Tue Aug 2 17:26:16 1994	15 OF 26



Silicon Graphics Computer Systems		BLUE DAC	
ENGINEER Max Torneros	REV	DRAWING: VB3	vb3
VB3 032-8235-002	C	Tue Aug 2 17:26:32 1994	16 OF 26



Silicon Graphics Computer Systems		Video Output	
ENGINEER Max Torneros	REV	DRAWING: VB3	vb3
VB3 032-8235-002	C	Tue Aug 2 17:26:50 1994	17 OF 26


+5 VCC
1R3 4.7K 5% 1/16W CC 0603
+5 VCC
NO STUFF R540 220 5% 1/8W CC 1206
NO STUFF R57 330 5% 1/8W CC 1206
R36 51 5% 1/16W CC 0603
U502
VC1
SRAM32K8
U4
VC1MEM_D<7..0>
VC1MEM_A<14..0>
CLKIN
RESET
EX/ST
BASE/EXPAN
VID.TR
PIXELA.0
PIXELA.1
PIXELA.2
PIXELA.3
PIXELA.4
PIXELA.5
PIXELA.6
PIXELA.7
PIXELB.0
PIXELB.1
PIXELB.2
PIXELB.3
PIXELB.4
PIXELB.5
PIXELB.6
PIXELB.7
PIXELC.0
PIXELC.1
PIXELC.2
PIXELC.3
PIXELC.4
PIXELC.5
PIXELC.6
PIXELC.7
PIXELD.0
PIXELD.1
PIXELD.2
PIXELD.3
PIXELD.4
PIXELD.5
PIXELD.6
PIXELD.7
PIXELE.0
PIXELE.1
PIXELE.2
PIXELE.3
PIXELE.4
PIXELE.5
PIXELE.6
PIXELE.7
SCLK.ST
SCLK.EX
TRI.ENABLE
ATPG.EN
RAMTEST.EN
SCAN.ENABLE
SCAN.IN
SCAN.OUT
POUT
GENSYNC
CBLANK/VT0
CBEARLY/VT1
LCNTROP/VT2
TRREQ/VT3
SOEN/VT4
FEEDBACK/VT5
SOENEARLY/VT6
HDRIVE/VT7
CSYNC/VT8
ENDLINE/VT9
HINCR/VT10
SV1FLD/VT11
SV1FRM/VT12
EXTCSYNC/VT13
VDRIVE/VT14
VSTAT/VT15
VINTR/VT16
ENDFIELD/VT17
ODDFIELD/VT18
HQ2BLANK/VT19
SV1XTRA/VT20
HDATA.0
HDATA.1
HDATA.2
HDATA.3
HDATA.4
HDATA.5
HDATA.6
HDATA.7
CMD.0
CMD.1
CMD.2
CS
R/W
CS.DAC
ACK
VIDEO.KEYIN.E
VIDEO.KEYIN.O
VIDEO.KEYOUT.E
VIDEO.KEYOUT.O
PCLK/2
AUXA.0
AUXA.1
AUXA.2
AUXA.3
AUXB.0
AUXB.1
AUXB.2
AUXB.3
AUXC.0
AUXC.1
AUXC.2
AUXC.3
AUXD.0
AUXD.1
AUXD.2
AUXD.3
AUXE.0
AUXE.1
AUXE.2
AUXE.3
GND:
VCC:
DIDA.0
DIDA.1
DIDA.2
DIDA.3
DIDA.4
DIDB.0
DIDB.1
DIDB.2
DIDB.3
DIDB.4
DIDC.0
DIDC.1
DIDC.2
DIDC.3
DIDC.4
DIDD.0
DIDD.1
DIDD.2
DIDD.3
DIDD.4
DIDE.0
DIDE.1
DIDE.2
DIDE.3
DIDE.4
DISPIDA<4..0>
DISPIDB<4..0>
DISPIDC<4..0>
DISPIDD<4..0>
DISPIDE<4..0>
MDATA.0
MDATA.1
MDATA.2
MDATA.3
MDATA.4
MDATA.5
MDATA.6
MDATA.7
MADDR.0
MADDR.1
MADDR.2
MADDR.3
MADDR.4
MADDR.5
MADDR.6
MADDR.7
MADDR.8
MADDR.9
MADDR.10
MADDR.11
MADDR.12
MADDR.13
MADDR.14
MADDR.15
MWE
MOE
MCS
DACCLK
DACPIX.0
DACPIX.1
DACPIX.2
DACPIX.3
DACPIX.4
DACPIX.5
DACPIX.6
DACPIX.7
MAPSEL.0
MAPSEL.1
CURA.0
CURA.1
CURB.0
CURB.1
CURC.0
CURC.1
CURD.0
CURD.1
CURE.0
CURE.1
C12 10uF 20% 16V TANT 6032
C3 0.1uF 20% 16V Z5U 0603
C5 0.001uF 10% 50V X7R 0603
C39 0.1uF 20% 16V Z5U 0603
C38 0.001uF 10% 50V X7R 0603
Silicon Graphics Computer Systems
VC1 and VC1 SRAM
ENGINEER Max Torneros
REV
DRAWING: VB3
vb3
VB3 032-8235-002
C
Tue Aug 2 17:27:10 1994
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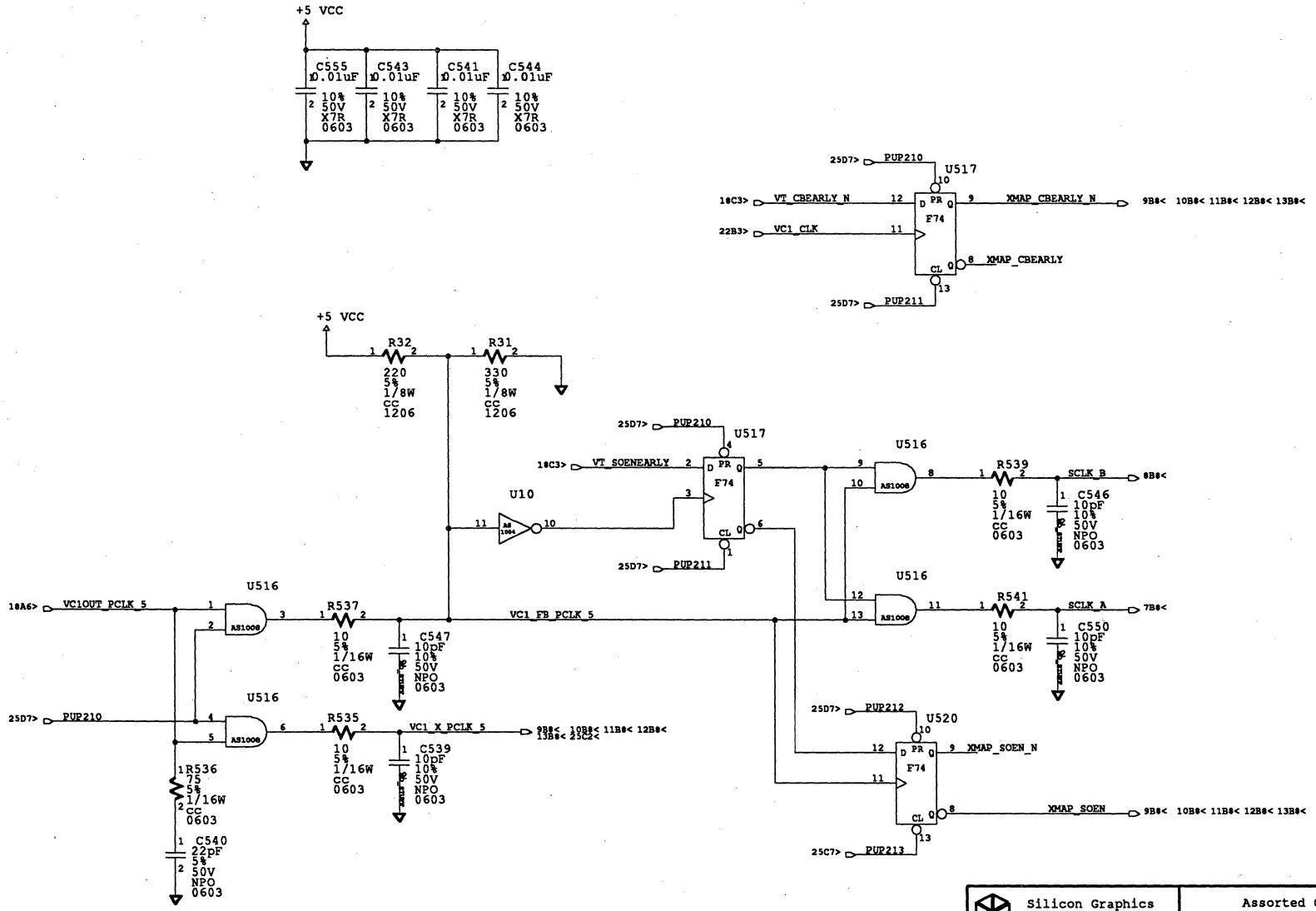
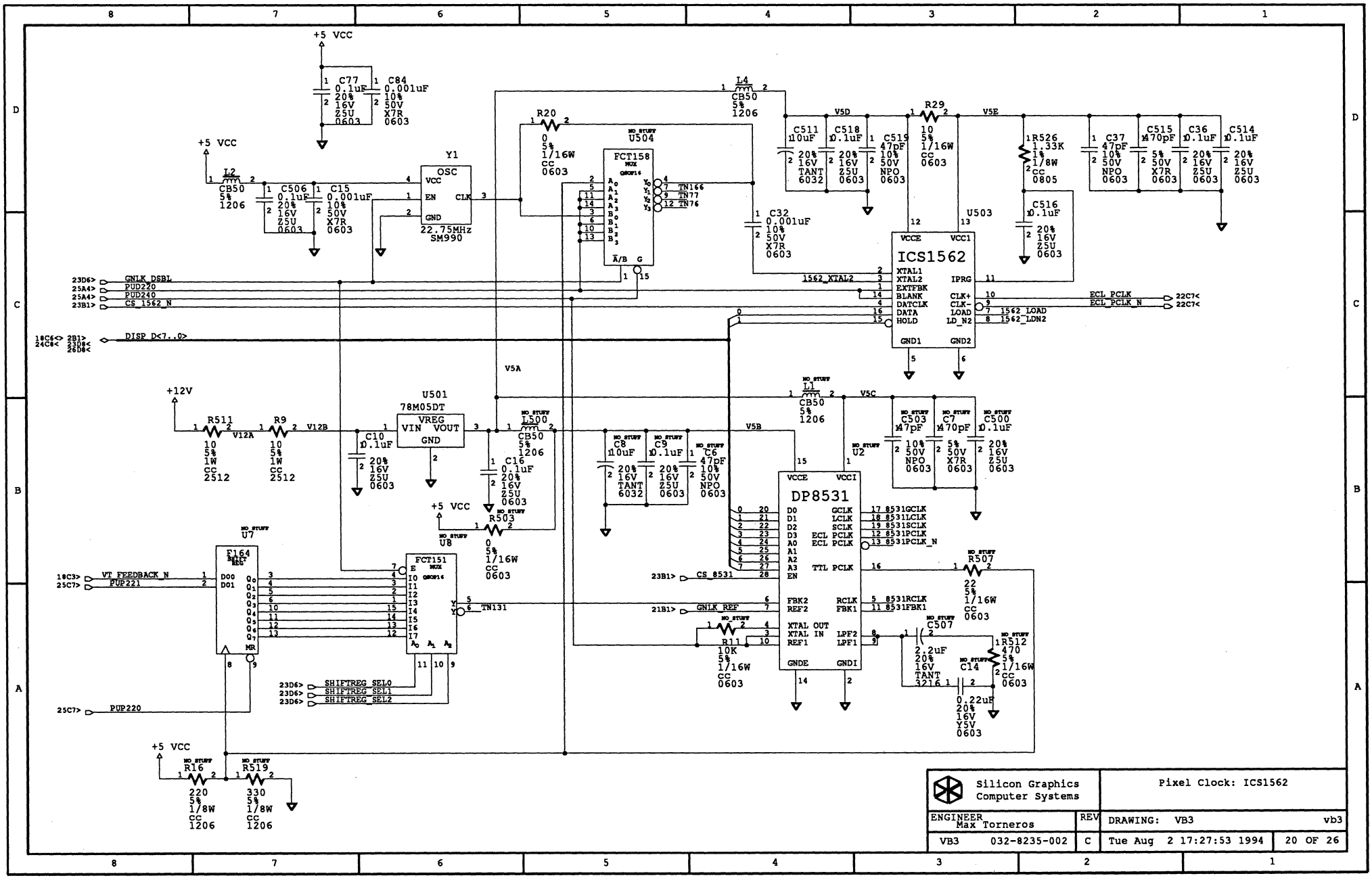

+5 VCC
C555 0.01uF 10% 50V X7R 0603
C543 0.01uF 10% 50V X7R 0603
C541 0.01uF 10% 50V X7R 0603
C544 0.01uF 10% 50V X7R 0603
25D7> PUP210
U517
18C3> VT_CBEARLY_N
XMAP_CBEARLY_N
9B8< 10B8< 11B8< 12B8< 13B8<
22B3> VC1_CLK
F74
XMAP_CBEARLY
25D7> PUP211
+5 VCC
R32 220 5% 1/8W CC 1206
R31 330 5% 1/8W CC 1206
25D7> PUP210
U517
18C3> VT_SOENEARLY
U516
R539 10 5% 1/16W CC 0603
SCLK_B
8B8<
C546 10pF 10% 50V NPO 0603
U10
25D7> PUP211
U516
R541 10 5% 1/16W CC 0603
SCLK_A
7B8<
C550 10pF 10% 50V NPO 0603
18A6> VC1OUT_PCLK_5
U516
R537 10 5% 1/16W CC 0603
VC1_FB_PCLK_5
C547 10pF 10% 50V NPO 0603
25D7> PUP210
U516
R535 10 5% 1/16W CC 0603
VC1_X_PCLK_5
9B8< 10B8< 11B8< 12B8< 13B8< 25C2<
C539 10pF 10% 50V NPO 0603
R536 75 5% 1/16W CC 0603
C540 22pF 5% 50V NPO 0603
25D7> PUP212
U520
XMAP_SOEN_N
XMAP_SOEN
9B8< 10B8< 11B8< 12B8< 13B8<
25C7> PUP213
Silicon Graphics Computer Systems
Assorted Clocks and Flops
ENGINEER Max Torneros
REV
DRAWING: VB3
vb3
VB3 032-8235-002
C
Tue Aug 2 17:28:49 1994
19 OF 26


+5 VCC
C77 0.1uF 20% 16V Z5U 0603
C84 0.001uF 10% 50V X7R 0603
L4 CB50 5% 1206
R20 0 5% 1/16W CC 0603
U504 FCT158
R29 10 5% 1/16W CC 0603
V5D
V5E
C511 10uF 20% 16V TANT 6032
C518 0.1uF 20% 16V Z5U 0603
C519 47pF 10% 50V NPO 0603
R526 1.33K 1% 1/8W CC 0805
C37 47pF 10% 50V NPO 0603
C515 470pF 5% 50V X7R 0603
C36 0.1uF 20% 16V Z5U 0603
C514 0.1uF 20% 16V Z5U 0603
Y1 OSC 22.75MHz SM990
L2 CB50 5% 1206
C506 0.1uF 20% 16V Z5U 0603
C15 0.001uF 10% 50V X7R 0603
C32 0.001uF 10% 50V X7R 0603
U503 ICS1562
C516 0.1uF 20% 16V Z5U 0603
GNLK_DSBL
PUD220
PUD240
CS_1562_N
DISP_D<7..0>
1562_XTAL2
ECL_PCLK
ECL_PCLK_N
1562_LOAD
1562_LDN2
V5A
V5B
V5C
+12V
R511 10 5% 1W CC 2512
R9 10 5% 1W CC 2512
V12A
V12B
U501 78M05DT VREG VIN VOUT GND
C10 0.1uF 20% 16V Z5U 0603
L500 CB50 5% 1206
C16 0.1uF 20% 16V Z5U 0603
L1 CB50 5% 1206
C503 47pF 10% 50V NPO 0603
C7 470pF 5% 50V X7R 0603
C500 0.1uF 20% 16V Z5U 0603
C8 10uF 20% 16V TANT 6032
C9 0.1uF 20% 16V Z5U 0603
C6 47pF 10% 50V NPO 0603
U2 DP8531
R503 0 5% 1/16W CC 0603
U8
U7 F164
FCT151
VT_FEEDBACK_N
PUP221
PUP220
SHIFTREG_SEL0
SHIFTREG_SEL1
SHIFTREG_SEL2
CS_8531
GNLK_REF
TN131
R507 22 5% 1/16W CC 0603
R11 10K 5% 1/16W CC 0603
C507 2.2uF 20% 16V TANT 3216
R512 470 5% 1/16W CC 0603
C14 0.22uF 20% 16V Y5V 0603
R16 220 5% 1/8W CC 1206
R519 330 5% 1/8W CC 1206
Silicon Graphics Computer Systems
Pixel Clock: ICS1562
ENGINEER Max Torneros
REV C
DRAWING: VB3 vb3
VB3 032-8235-002
Tue Aug 2 17:27:53 1994
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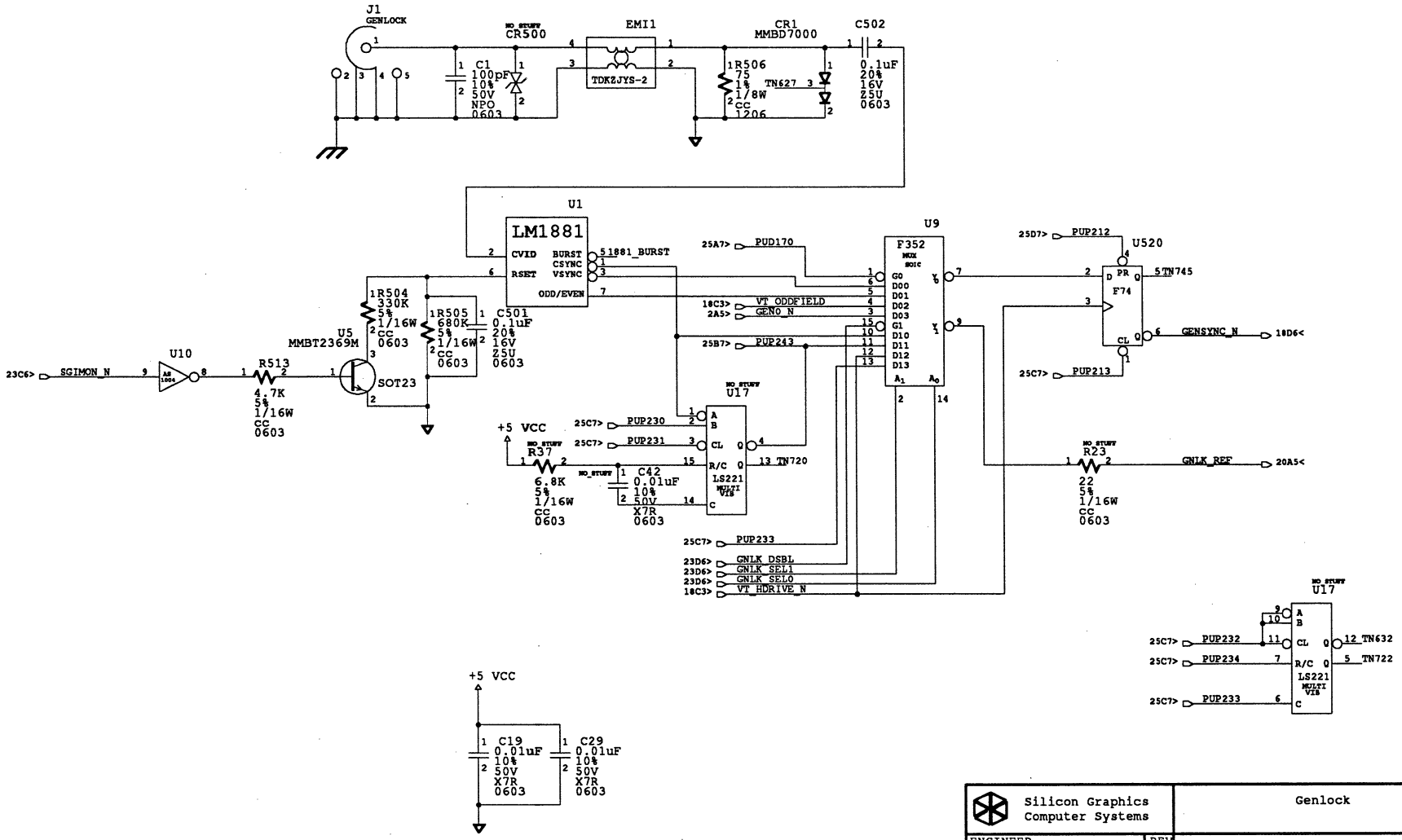
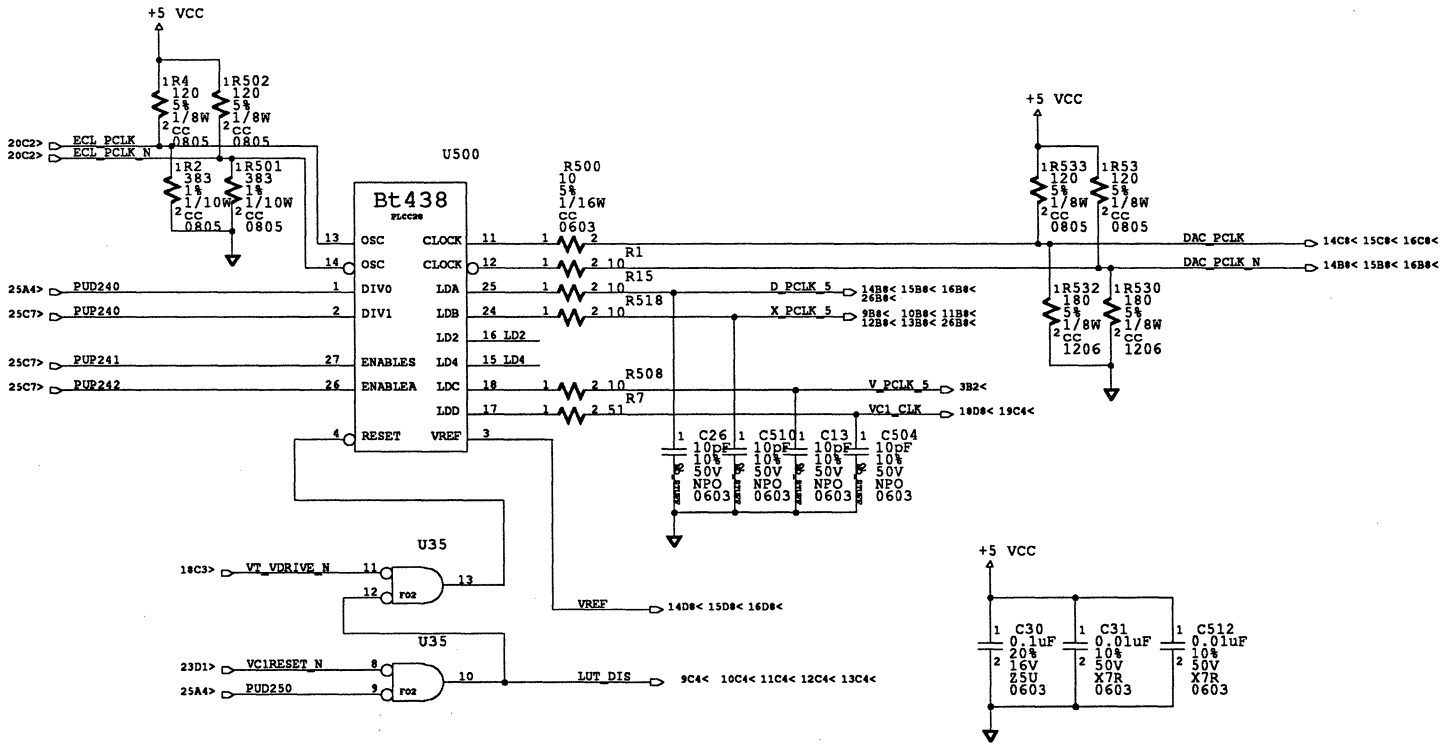
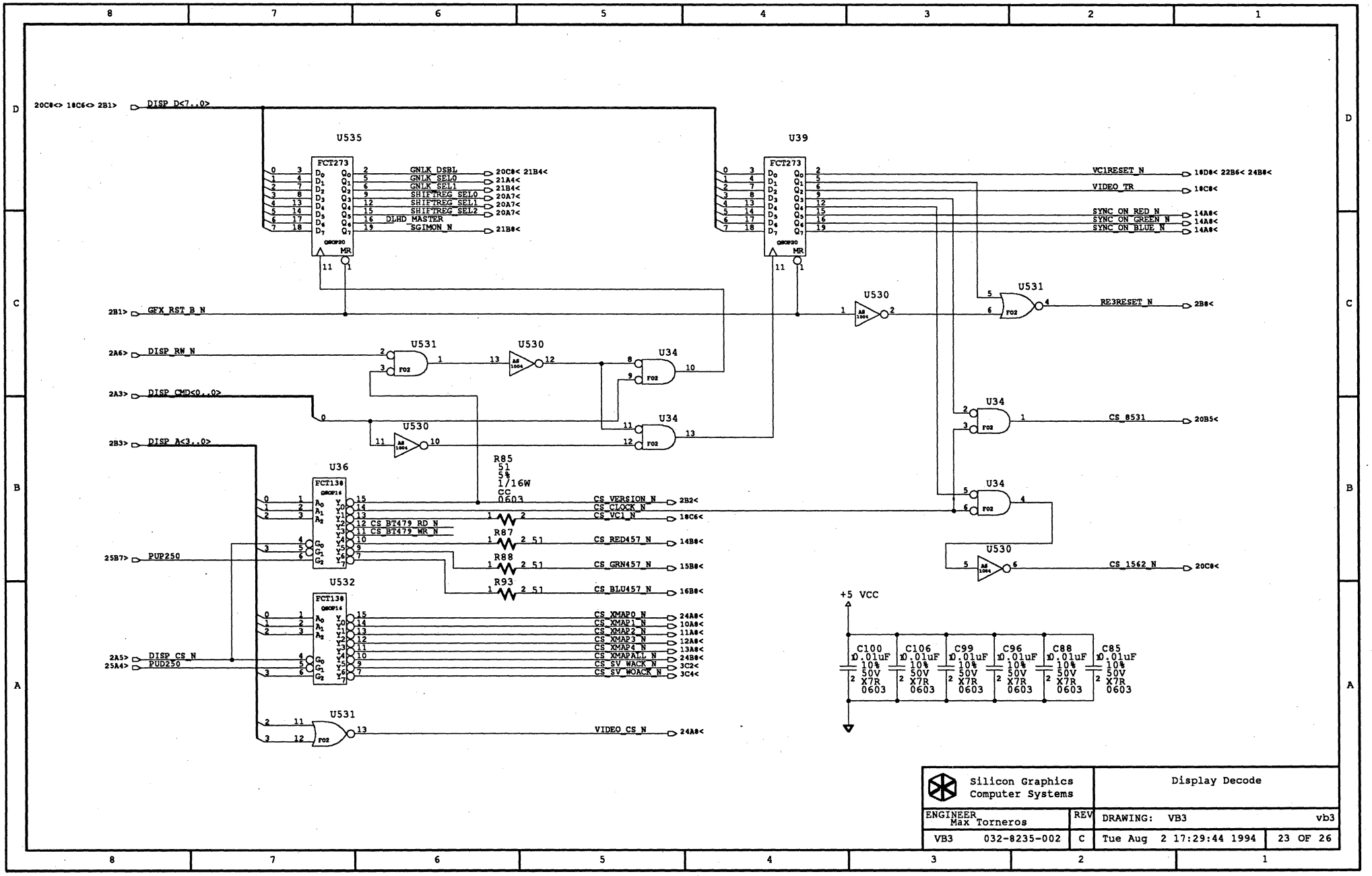


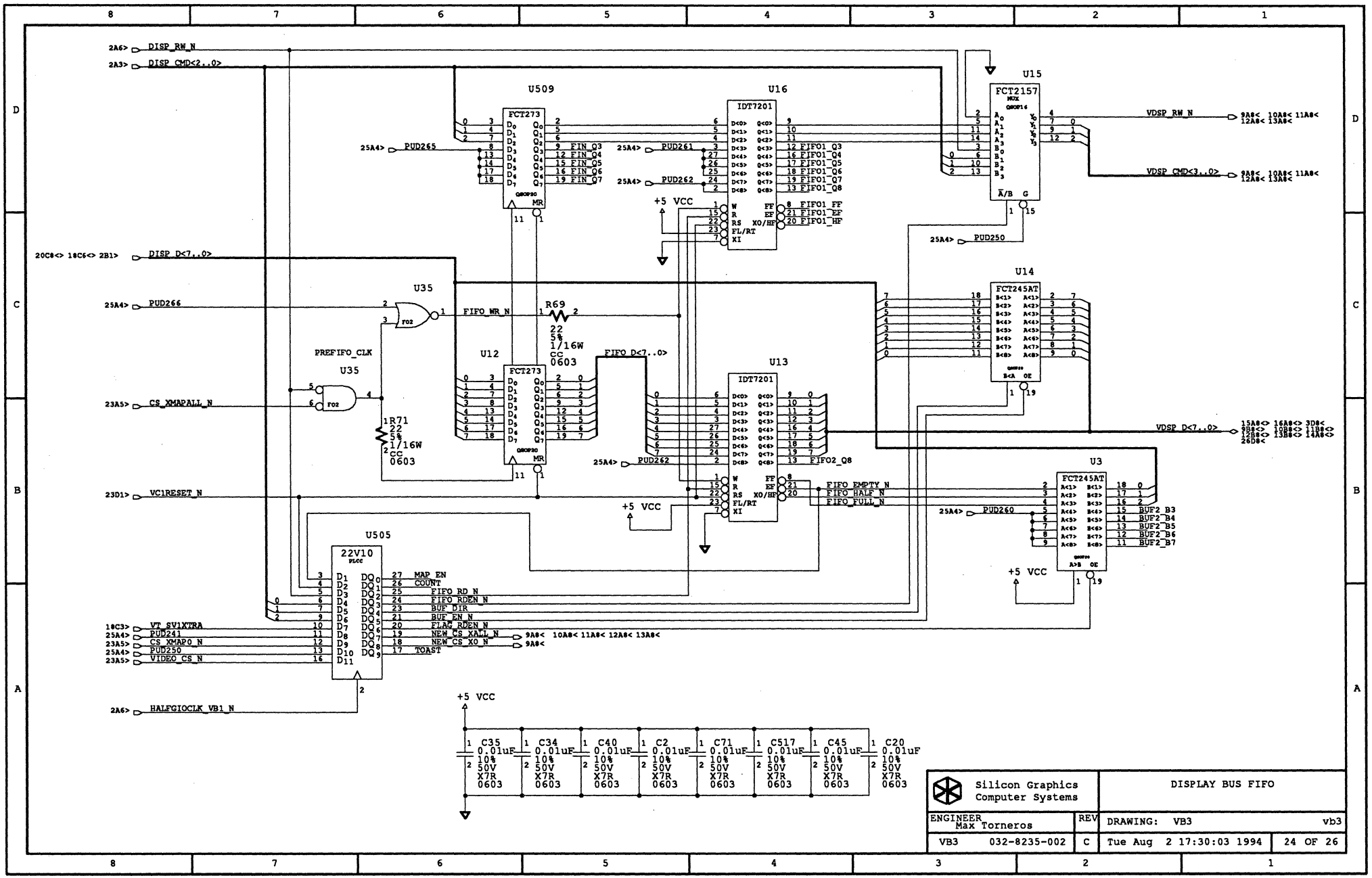
Silicon Graphics Computer Systems		Genlock	
ENGINEER Max Torneros	REV	DRAWING: VB3	vb3
VB3 032-8235-002	C	Tue Aug 2 17:29:08 1994	21 OF 26



Silicon Graphics Computer Systems		Pixel Clock: Bt438	
ENGINEER Max Torneros	REV	DRAWING: VB3	vb3
VB3 032-8235-002	C	Tue Aug 2 17:29:26 1994	22 OF 26



Silicon Graphics Computer Systems		Display Decode	
ENGINEER Max Torneros	REV	DRAWING: VB3	vb3
VB3 032-8235-002	C	Tue Aug 2 17:29:44 1994	23 OF 26


2A6> DISP_RW_N
2A3> DISP_CMD<2..0>
20C8<> 18C5<> 2B1> DISP_D<7..0>
U509
FCT273
25A4> PUD265
FIN_Q3
FIN_Q4
FIN_Q5
FIN_Q6
FIN_Q7
U16
IDT7201
25A4> PUD261
25A4> PUD262
FIFO1_Q3
FIFO1_Q4
FIFO1_Q5
FIFO1_Q6
FIFO1_Q7
FIFO1_Q8
FIFO1_FF
FIFO1_EF
FIFO1_HF
+5 VCC
U15
FCT2157
VDSP_RW_N
VDSP_CMD<3..0>
9A8< 10A8< 11A8< 12A8< 13A8<
25A4> PUD250
U35
25A4> PUD266
FIFO_WR_N
R69
22
5%
1/16W
CC
0603
PREFIFO_CLK
U12
FCT273
FIFO_D<7..0>
U13
IDT7201
25A4> PUD262
FIFO2_Q8
FIFO_EMPTY_N
FIFO_HALF_N
FIFO_FULL_N
U14
FCT245AT
VDSP_D<7..0>
15A8<> 16A8<> 3D8<
9B8<> 10B8<> 11B8<>
12B8<> 13B8<> 14A8<>
26D8<
23A5> CS_XMAPALL_N
1R71
22
5%
1/16W
CC
0603
23D1> VC1RESET_N
U3
FCT245AT
25A4> PUD260
BUF2_B3
BUF2_B4
BUF2_B5
BUF2_B6
BUF2_B7
U505
22V10
MAP_EN
COUNT
FIFO_RD_N
FIFO_RDEN_N
BUF_DIR
BUF_EN_N
FLAG_RDEN_N
NEW_CS_XALL_N
NEW_CS_XO_N
TOAST
18C3> VT_SV1XTRA
25A4> PUD241
23A5> CS_XMAP0_N
25A4> PUD250
23A5> VIDEO_CS_N
2A6> HALFGIOCLK_VB1_N
C35 0.01uF 10% 50V X7R 0603
C34 0.01uF 10% 50V X7R 0603
C40 0.01uF 10% 50V X7R 0603
C2 0.01uF 10% 50V X7R 0603
C71 0.01uF 10% 50V X7R 0603
C517 0.01uF 10% 50V X7R 0603
C45 0.01uF 10% 50V X7R 0603
C20 0.01uF 10% 50V X7R 0603
Silicon Graphics Computer Systems
DISPLAY BUS FIFO
ENGINEER Max Torneros
REV C
DRAWING: VB3 vb3
VB3 032-8235-002
Tue Aug 2 17:30:03 1994
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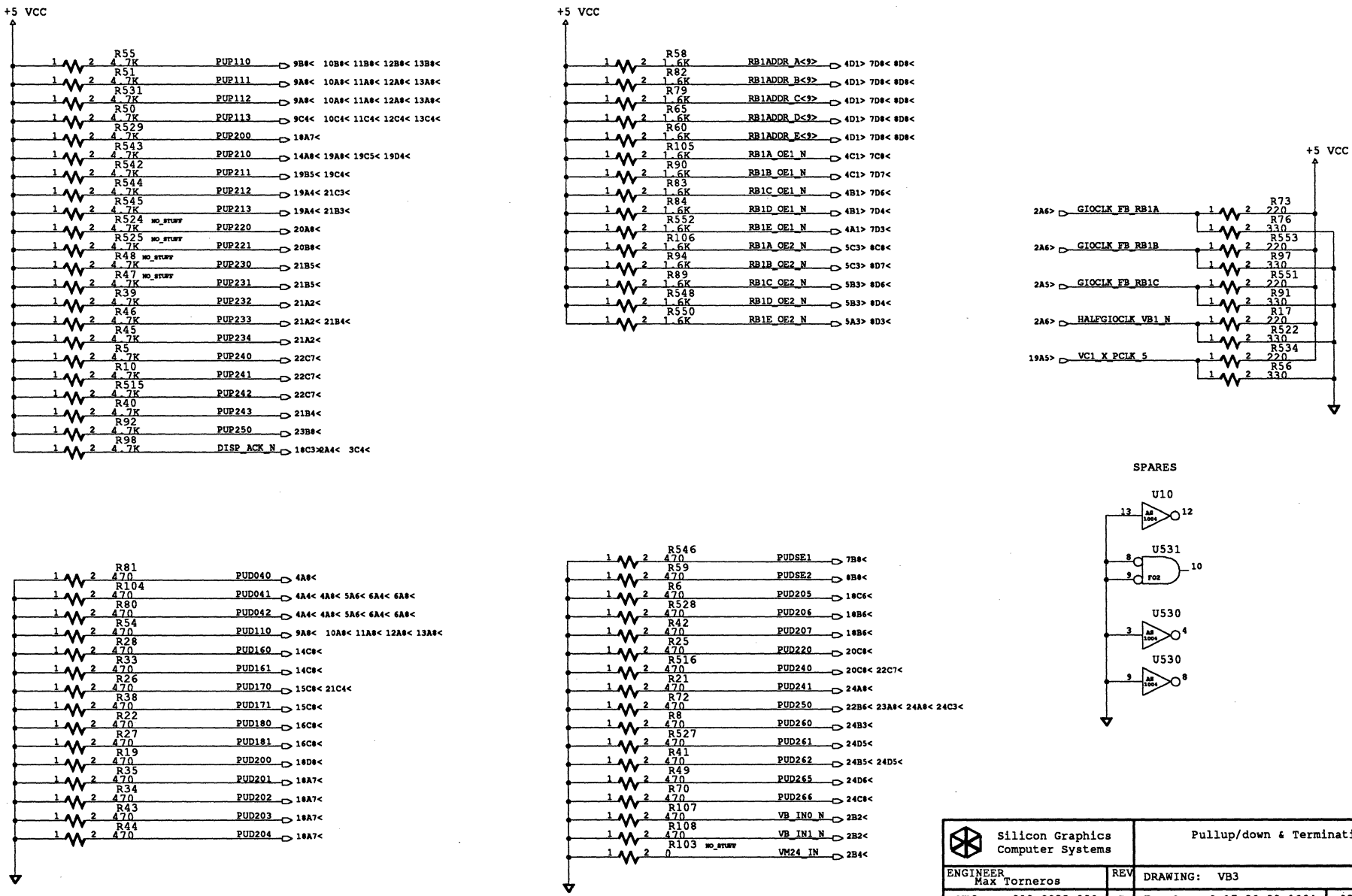
+5 VCC
R55 4.7K PUP110 9B8< 10B8< 11B8< 12B8< 13B8<
R51 4.7K PUP111 9A8< 10A8< 11A8< 12A8< 13A8<
R531 4.7K PUP112 9A8< 10A8< 11A8< 12A8< 13A8<
R50 4.7K PUP113 9C4< 10C4< 11C4< 12C4< 13C4<
R529 4.7K PUP200 18A7<
R543 4.7K PUP210 14A8< 19A8< 19C5< 19D4<
R542 4.7K PUP211 19B5< 19C4<
R544 4.7K PUP212 19A4< 21C3<
R545 4.7K PUP213 19A4< 21B3<
R524 4.7K NO_STUFF PUP220 20A8<
R525 4.7K NO_STUFF PUP221 20B8<
R48 4.7K NO_STUFF PUP230 21B5<
R47 4.7K NO_STUFF PUP231 21B5<
R39 4.7K PUP232 21A2<
R46 4.7K PUP233 21A2< 21B4<
R45 4.7K PUP234 21A2<
R5 4.7K PUP240 22C7<
R10 4.7K PUP241 22C7<
R515 4.7K PUP242 22C7<
R40 4.7K PUP243 21B4<
R92 4.7K PUP250 23B8<
R98 4.7K DISP_ACK_N 18C3> 2A4< 3C4<
+5 VCC
R58 1.6K RB1ADDR_A<9> 4D1> 7D8< 8D8<
R82 1.6K RB1ADDR_B<9> 4D1> 7D8< 8D8<
R79 1.6K RB1ADDR_C<9> 4D1> 7D8< 8D8<
R65 1.6K RB1ADDR_D<9> 4D1> 7D8< 8D8<
R60 1.6K RB1ADDR_E<9> 4D1> 7D8< 8D8<
R105 1.6K RB1A_OE1_N 4C1> 7C8<
R90 1.6K RB1B_OE1_N 4C1> 7D7<
R83 1.6K RB1C_OE1_N 4B1> 7D6<
R84 1.6K RB1D_OE1_N 4B1> 7D4<
R552 1.6K RB1E_OE1_N 4A1> 7D3<
R106 1.6K RB1A_OE2_N 5C3> 8C8<
R94 1.6K RB1B_OE2_N 5C3> 8D7<
R89 1.6K RB1C_OE2_N 5B3> 8D6<
R548 1.6K RB1D_OE2_N 5B3> 8D4<
R550 1.6K RB1E_OE2_N 5A3> 8D3<
+5 VCC
2A6> GIOCLK_FB_RB1A R73 220 R76 330
2A6> GIOCLK_FB_RB1B R553 220 R97 330
2A5> GIOCLK_FB_RB1C R551 220 R91 330
2A6> HALFGIOCLK_VB1_N R17 220 R522 330
19A5> VC1_X_PCLK_5 R534 220 R56 330
SPARES
U10
U531 FO2
U530
U530
R81 470 PUD040 4A8<
R104 470 PUD041 4A4< 4A8< 5A6< 6A4< 6A8<
R80 470 PUD042 4A4< 4A8< 5A6< 6A4< 6A8<
R54 470 PUD110 9A8< 10A8< 11A8< 12A8< 13A8<
R28 470 PUD160 14C8<
R33 470 PUD161 14C8<
R26 470 PUD170 15C8< 21C4<
R38 470 PUD171 15C8<
R22 470 PUD180 16C8<
R27 470 PUD181 16C8<
R19 470 PUD200 18D8<
R35 470 PUD201 18A7<
R34 470 PUD202 18A7<
R43 470 PUD203 18A7<
R44 470 PUD204 18A7<
R546 470 PUDSE1 7B8<
R59 470 PUDSE2 8B8<
R6 470 PUD205 18C6<
R528 470 PUD206 18B6<
R42 470 PUD207 18B6<
R25 470 PUD220 20C8<
R516 470 PUD240 20C8< 22C7<
R21 470 PUD241 24A8<
R72 470 PUD250 22B6< 23A8< 24A8< 24C3<
R8 470 PUD260 24B3<
R527 470 PUD261 24D5<
R41 470 PUD262 24B5< 24D5<
R49 470 PUD265 24D6<
R70 470 PUD266 24C8<
R107 470 VB_IN0_N 2B2<
R108 470 VB_IN1_N 2B2<
R103 0 NO_STUFF VM24_IN 2B4<
Silicon Graphics Computer Systems
Pullup/down & Termination
ENGINEER Max Torneros
REV
DRAWING: VB3
vb3
VB3 032-8235-002
C
Tue Aug 2 17:30:33 1994
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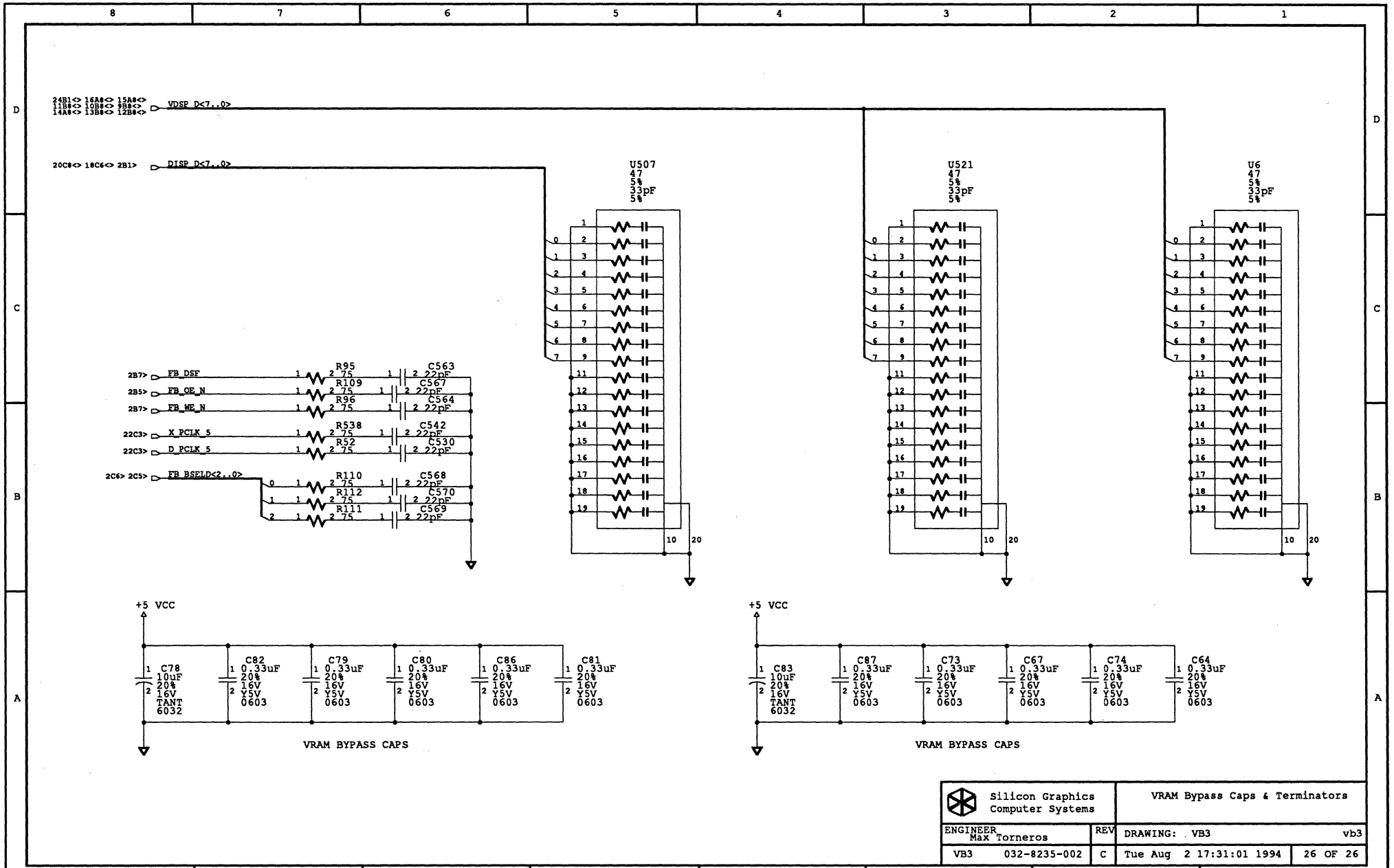

Silicon Graphics Computer Systems		VRAM Bypass Caps & Terminators	
ENGINEER Max Torneros	REV	DRAWING: VB3	vb3
VB3 032-8235-002	C	Tue Aug 2 17:31:01 1994	26 OF 26