STC-TSV11

Tape Transport Controller

Manual

Σ Sigma Information Systems

STC-TSV11

Tape Transport Controller

Manual

ANAHEIM, CALIFORNIA - AUGUST 1986

MA400250-1 REV B

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Section 1 - General Information

1.1 INTRODUCTION

This manual provides the necessary information to install and program the STC-TSV11 Tape Cartridge Transport Controller manufactured by Sigma Information Systems, Anaheim, California. The STC-TSV11 is designed for DEC* LSI-11 series computers and supports one or two Sentinal* tape transports.

The material in this manual is arranged into the following sections:

Section 1 - GENERAL INFORMATION. This section contains a brief general description of the STC-TSV11. Specifications are included.

Section 2 - INSTALLATION AND BOOTING. This section explains the procedures for equipment installation and booting the controller.

Section 3 - PROGRAMMING CONSIDERATIONS. This section contains register data bit functions and provides programming examples using register bit definitions.

REF: TSV11.WPS/DM4

*DEC and Q bus are registered trademarks of Digital Equipment Corporation. Sentinel is a registered trademark of Control Data Corporation.

1.2 GENERAL DESCRIPTION

The STC-TSV11 is a microprocessor based tape cartridge controller that supports one or two Control Data Corporation (CDC) Sentinel tape cartridge transports. The controller consists of a dual-wide TSV11 emulator module that plugs directly into the Q bus backplane, and a formatter module that mounts directly onto a CDC transport. A second formatter module is required if two tape transports are used.

The STC-TSV11 emulates the DEC* TSV05/TS11 and is software compatible with operating systems and application programs written for the TSV05/TS11 tape transport subsystems.

1.3 FEATURES

Compatible with TSV05/TS11 software.

Operates in streaming or start/stop modes while performing file-by-file operations.

Supports one or two streaming tape cartridge transports.

Includes on-board boot function.

LSI-11 compatibility supports 18-bit or 22-bit addressing, DMA transfers, and multilevel interrupt control.

1.4 EXAMPLE CONFIGURATION

Figure 1-1 is an example configuration using the STC-TSV11 and two CDC Sentinel tape transports. If a single tape transport is used only one formatter module is required.

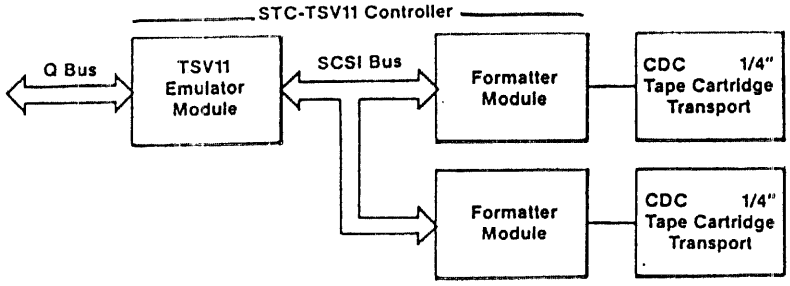


FIGURE 1-1: STC-TSV11 EXAMPLE CONFIGURATION

1.5 SPECIFICATIONS

Power Requirements:	+5VDC at 3.75A MAX (TSV11 emulator module) +5V @ 2.5A (formatter module)
Priority Level:	Selectable. Compatible with LSI-11/23
Device Address:	772520 standard with selectable alternate at 772530, or both 772520 and 772530
Vector Interrupt	224 (octal) standard with selectable alternate at 274, or both 224 and 274
Bus Load:	1
Bootstrap:	On-board. Initiated from ODT.
Tape Transport Compatibility:	CDC 92190 or 92192 steaming tape transports.
Media:	1/4" tape cartridge
Cabling:	Requires 34-conductor ribbon cable (not included) from formatter module to CDC tape transport. Also requires power cable with AMP 1-480698-0 mating connector and 350551-1 contacts to formatter module.
Dimensions:	Standard dual-wide Q bus TSV11 emulator module and 8.00" x 8.12" formatter module.
Installation:	TSV11 emulator module plugs directly into any dual Q bus slot. Formatter module with 6.75" x 7.50" mounting holes mounts on CDC tape transport.
Temperature	Operating: 5°C to 50°C Storage: -16°C to 60°C
Humidity:	10% to 95% (noncondensing)

Notes

Section 2 - Installation

2.1 UNPACKING AND INSPECTION

The STC-TSV11 is shipped in a special packing carton designed to keep the module from vibrating and to give it maximum protection during shipment. The packing carton should be retained in case the unit requires reshipment.

Unpack the STC-TSV11 and visually inspect for physical damage. If any damage has occurred, contact the factory immediately.

2.2 FACTORY-SET JUMPERS

The STC-TSV11 controller is shipped configured with DEC standard operating parameters as defined in Table 2-1. The location of the jumpers that determine these parameters are shown in Figure 2-1.

PARAMETER	SELECTION
Device Address	772520
Vector Address	224
Interrupt Request	Level 4 & 5

TABLE 2-1: FACTORY-SET JUMPERS

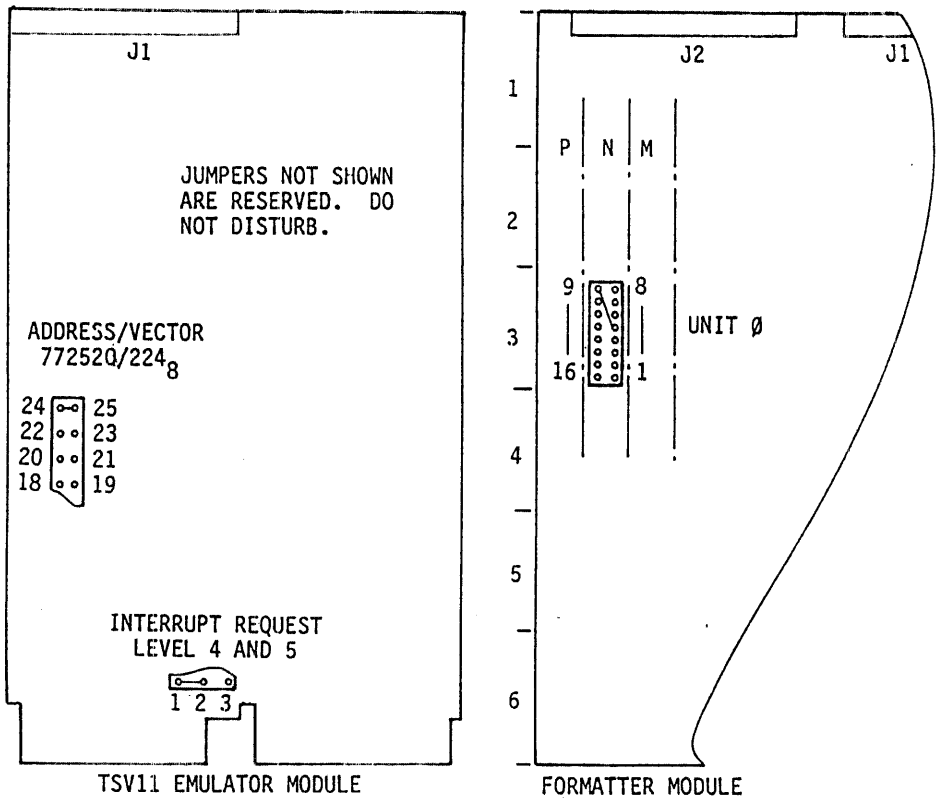


FIGURE 2-1: STC-TSV11 FACTORY-SET JUMPERS

Before installing modules, verify that these configurations are properly installed. The following sections describe the procedures to verify and/or reconfigure these operating parameters.

Most options are etched to the most often used operations. Etches must be cut before alternate jumpers are installed. Several of the options are selectable by using AMP 530153-2 pin jumpers or, alternately, No. 30 wire wrap.

NOTE

Certain jumpers are reserved or dedicated for factory test only. They must not be altered.

2.2.1 Device and Vector Address Selection

The controller is shipped with DEC standard device and vector addresses preset to 772520 and 224, respectively. These addresses are set on the TSV11 emulator module. Any change in these addresses requires a change in system software.

The alternate device and vector addresses are selectable at 772530 and 274, respectively. The standard or alternate addresses is used for TSV05 emulation where the tape transports are selected as unit 0 and unit 1 at the same address.

The STC-TSV11 can also be configured for both the standard and the alternate vector addresses; this configuration is typically used in systems with two tape transports that use DEC TS11 software, which selects only unit 0 or unit 1 at a singular address. To configure the controller for alternate address/vector assignments, or for simultaneous standard and alternate address/vector assignments, remove the jumper between W18 and W19; then jumper W22-W23 or W24-W25 as shown in Table 2-2.

OPTION	JUMPERS		
	W18-19	W22-23	W24-W25
Standard Address (772522)* Standard Vector (224)	OUT	OUT	IN
Alternate Address (772532) Alternate Vector (274)	OUT	IN	OUT
Standard (772522) and Alternate (772532) Address Standard (224) and Alternate (274) Vector	IN	OUT	OUT

TABLE 2-2: DEVICE/VECTOR ADDRESS JUMPERS

2.2.2 Unit Select

The unit select jumper is located on the formatter module (Figure 2-1). If a single tape transport is used, the controller is shipped with the formatter module configured as unit 0. If two tape transports are to be used, the controller is shipped with one formatter module configured as unit 0 and the other formatter module configured as unit 1. Check the jumpers in Table 2-3 to determine which formatter is unit 0 and which is unit 1.

UNIT SELECT	JUMPERS W5-W9	W6-W9
UNIT 0	IN	OUT
UNIT 1	OUT	IN

TABLE 2-3: UNIT SELECT JUMPERS

2.2.3 Interrupt Request Level

The STC-TSV11 interrupts are priority level 4 or 5 as shown in Table 2-4. Refer to Figure 2-1 for jumper locations.

INTERRUPT REQUEST LEVEL	W1-W2
4	OUT
4 AND 5	IN

TABLE 2-4: INTERRUPT REQUEST LEVEL SELECTION

2.3 MODULE INSTALLATION

The TSV11 emulator module plugs directly into any dual Q bus slot of an LSI-11 backplane. The formatter module, with 6.75" x 7.50" mounting holes, mounts on the CDC tape transport mounting posts, which must be tapped with a 6-32 thread. See Figure 2-2.

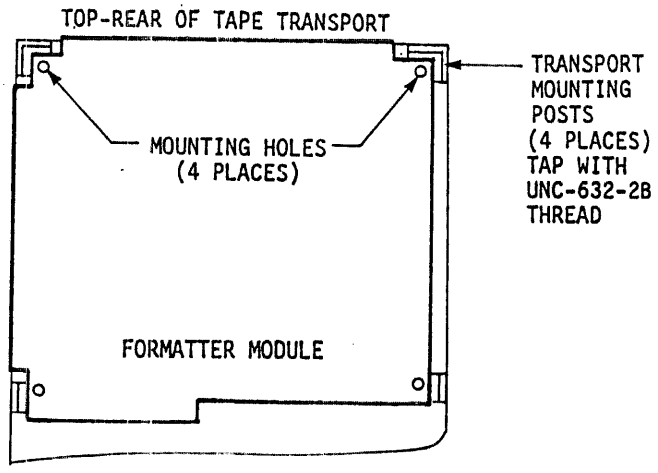


FIGURE 2-2: FORMATTER MODULE INSTALLATION

With Figure 2-3 as a guide, use the following procedure to cable the TSV11 emulator module and the formatter module to the tape transport.

1. There are two terminating resistors located under J1 on the formatter module. If two tape transports are to be installed, remove the terminating resistors from the formatter on unit 0. .

2. Connect the 50-conductor ribbon cable from J1 on the emulator module to J1 on the formatter module. If a second formatter module is used, the 50-conductor cable daisy chains from the first formatter module to J1 on the second module.

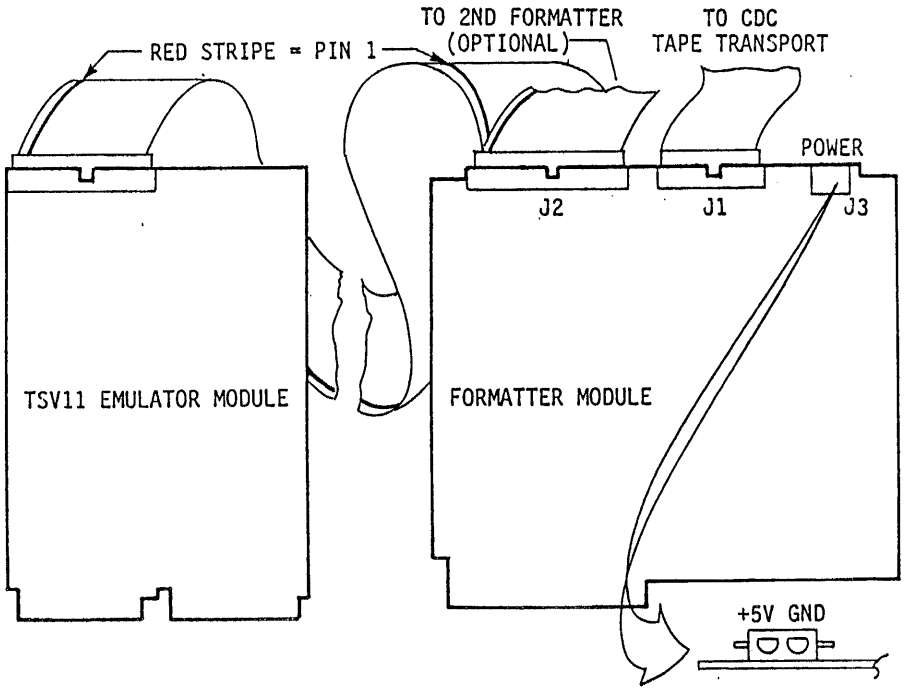


FIGURE 2-3: STC-TSV11 CABLING

3. Verify that the power source provides +5V @ 2.5A before attaching the power cable to J3 on the formatter module(s). The power cable requires an AMP 1-480698-0 mating connector with 350551-1 contacts.

4. Verify that the LSI-11 backplane provides +5V at 3.75A for the TSV11 emulator module before operating the system. Measure +5V on pin AA2, BA2, or BV1 of any backplane connector slot.

5. Refer to CDC specifications for attaching the 34-conductor ribbon cable from J2 on the formatter module to the Sentinel tape transport. The pin assignments on J2 are defined in Table 2-5.

*PIN	MNEMONIC	DESCRIPTION
1	FWD	FILE MARK DETECT
3	DER	DATA ERROR FLAG
5	BSY	DEVICE BUSY
7	RDATA	READ DATA
9	RDY	READY
10	LTS	LAST TRACK STATUS
11	INT	INTERRUPT
13	RGATE	READ GATE
15	DCLK	DATA CLOCK
17	CACK	COMMAND ACKNOWLEDGE
19	RST	RESET
21	WDATA	WRITE DATA
23	WGATE	WRITE GATE
25	CB0	COMMAND BUS 0
27	CGATE	COMMAND GATE
29	CB1	COMMAND BUS 1
31	CB3	COMMAND BUS 3
33	CB2	COMMAND BUS 2

*All even pins, except 10, are logic ground.

TABLE 2-5: 34-PIN CONNECTOR (J2) ASSIGNMENTS

2.4 BOOTING THE STC-TSV11

The STC-TSV11 can boot from ODT on LSI-11/2, LSI-11/23, or LSI-1/73 systems. Use the following procedures to boot the STC-TSV11.

2.4.1 Booting from an LSI-11/73 CPU

1. Place the CPU in HALT mode.
2. Power up and load the tape.
3. When the tape is ready, use ODT and enter the following:

	ENTER	RESPONSE
A.	**1000G**	Rewinds the tape.
B.	**1000/ 112737<LF>**	System responds with a series of numbers.
	1002/ 200<LF>	System responds with a series of numbers.
	1004/ 772523<LF>	System responds with a series of numbers.
	1006/ 5007<RET>	System responds with a series of numbers.
C.	**P**	Tape rewinds and loads bootstrap. Wait for Tape Ready.
D.	**Enable CPU**	
E.	**P**	Tape should continue booting; if not, return to step A.

2.4.2 Booting on LSI-11/2 or LSI-11/23 CPU

1. Place the CPU in HALT mode.
2. Power up and load the tape.
3. When the tape is ready, use ODT and enter the following:

	ENTER	RESPONSE
A.	**@G**	Rewinds the tape
B.	**772527/**	System responds with a series of numbers.
C.	**0<RET>**	Rewinds tape and loads bootstrap. Wait for @ prompt and Tape Ready.
D.	**Enable CPU**	
E.	**P**	Tape should continue booting, or return to step A.

Section 3 - Programming Considerations

3.1 INTRODUCTION

The functions listed below are compatible with the TSV05 and make up the STC-TSV11 Command Set. These commands utilize "command packets" stored in the computer system memory to operate the tape drive and transfer data. Some commands have various sub-commands, termed "modes." The interface device registers are used to initiate command packet processing and retrieve basic status. This section describes register manipulation and provides an overview of packet protocol (the format used to transfer commands and data).

3.2 REGISTERS

The STC-TSV11 uses the four TSV05 device registers which occupy only two LSI-11 bus word locations: a Data Buffer (TSDB), a Bus Address Register (TSBA), a Status Register (TSSR) and an Extended Data Buffer (TSDBX).

Data Buffer (TSDB)

The TSDB is an 18-bit register that is parallel loaded from the LSI-11 bus or from the STC-TSV11 controller itself. A 16-bit portion of this register is used as a word buffer register. It is written into by the CPU to initiate and operate, and it is written into by the controller logic itself to store data to be transmitted to LSI-11 bus memory during a DMA cycle.

Bus Address Register (TSBA)

The TSBA is an 18-bit register (22-bits when the high byte of the TSSR is written to) that is parallel loaded from the TSDB every time the TSDB is loaded. TSDB bits 15-02 load into TSBA bits 15-02, TSDB bits 1 and 0 load into TSBA bits 17 and 16, and zeroes are modulo-4 address. TSBA bits 17 and 16 are displayed in TSSR bits 09 and 08, respectively. TSDB can be extended to 22 bits by first loading TSDB bits 18-22 into the high byte of TSSR. The extended feature switch must be ON or else bits 18-22 are ignored. The TSBA register is incremented or decremented by two for DMA word transfers, or by one for DMA byte transfers.

Status Register (TSSR)

The TSSR is a 16 bit register that can only be updated from the STC-TSV11 internal logic.

Extended Data Buffer (TSDBX)

The TSDBX is a Write-Only hardware byte register located at the fourth byte address of the I/O register block. This address corresponds to the high-order byte of the TSSR register. The TSDBX is used to specify the most significant four bits of a 22-bit command pointer address, and also to allow an automatic tape boot sequence to be performed.

3.2.1 Bus Address Register (TSBA) - READ ONLY

The Bus Address Register (TSBA) is a Read-Only hardware register located at the first I/O register address. In normal operating mode, it displays the low-order 16 bits of the memory address used by the controller to access system main memory. In Maintenance Mode, it displays data from the Wraparound tests invoked by writing into TSDB.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00

Address Bits 15 through 00 normally reflect the low-order 16 bits of the 22-bit address used by the controller to access LSI-11 bus memory. They can be loaded by:

A. The CPU writing a word into TSDB to define the address of the Command Buffer for the next operation. TSDB 15:02 are copied into TSBA 15:02, and TSBA 01:00 are set to 0.

B. The CPU writing into the high byte (DATOB) of TSDB (for a maintenance function). TSDB bits 15-08 are copied into both bytes of TSBA. Data for bits 07-00 is TSDB 15:08. TSDB bits 08 and 09 are copied into TSSR bits 08 and 09 (A16,A17).

C. The CPU writing into the low byte (DATOB) of TSDB (for a maintenance function). TSDB bits 07-00 are copied to TSBA 07:00. TSBA 15:08 is then loaded from TSDB bits 07:00.

D. The CPU writing a word (DATO) into TSDB in Maintenance Mode. (Maintenance mode is achieved as a result of 2 or 3.)

E. The STC-TSV11 controller specifying bits 15-00 of a DMA address. TSBA is not modified by Initialize.

3.2.2 Data Buffer (TSDB) - WRITE ONLY

The TSDB is, externally, a 16-bit Write-Only register that is parallel loaded from the LSI-11 Bus. Internally, it is a 22-bit register. It can be loaded from the CPU by four different types of transfers. Two transfers are for maintenance purposes (DATOB to high byte and DATOB to low byte); these place the controller into Maintenance Mode, which can be cleared only by an Initialize, and causes the internal "Data Wraparound" functions. The third is for maintenance purposes (DATO word when in Maintenance Mode.) The fourth is for normal operation (DATO word when not in Maintenance Mode) to specify a Command Pointer. The 4-bit extension to TSDB is written at the high byte of the TSSR location.

The STC-TSV11 controller will respond whenever the TSDB location is written to, but will be loaded only when the SSR bit in the TSSR register is set; if SSR is clear, the RMR bit in TSSR will be set. Writing into TSDB clears SSR. After a DATO or DATOB to TSDB (for maintenance data "wraparound"), SSR momentarily clears then sets when the data "wraparound" has been performed. An Initialize should be performed (i.e., write into TSSR) in order to use the controller again for normal operation. Note that entering Maintenance Mode (by performing a DATOB to either byte of the TSDB) causes the NBA (Need Buffer Address) bit in TSSR to be set and automatic running of the ideal-time On-Line Microdiagnostics to be inhibited.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P17	P16

DATA BUFFER FORMAT (TSDB) - COMMAND POINTER

BIT	SIGNAL	DESCRIPTION
15-02 01-00	P15:P02 P17:P16	COMMAND POINTER BITS 17-02. When the TSDB is written as a word, and SSR = 1, and the controller is not in Maintenance Mode, the data is loaded into bits 17-02 of both the TSBA Output File register (for reading onto the LSI-11 bus) and into an internal TSBA register and command processing commences. TSBA bits 01-00 are cleared to 0 (modulo-4 address). In addition, the Extended TSDB Register (TSDBX) is loaded into TSBA bits 21-18; TSDBX must be loaded before TSDB.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00

DATA BUFFER FORMAT (TSDB) - MAINTENANCE MODE

BIT	SIGNAL	DESCRIPTION
15-08	M15:M08	MAINTENANCE DATA BITS 15-08. For wraparound to TSBA. If the wraparound is correct, M15:M08 appears in both bytes of TSBA. A DATOB to TSDB places the controller into maintenance mode. NOTE: DATOB to high byte.
07-00	M07:M00	MAINTENANCE DATA BITS 07-00. For wraparound to TSBA. If the wraparound is correct. M07:M00 appears in both TSBA 07:00 and in TSBA 15:08. A DATOB to TSDB places the controller into maintenance mode. NOTE: DATOB to Low Byte
15-00	M15:M00	MAINTENANCE DATA BIT 15:00. This function can be used for specifying the address used in the Low-Byte Data Wrap test. Bits 15-12 are reserved for future maintenance functions and should be written to 0. NOTE: DATO Word in Maintenance Mode.

3.2.3 Status Register (TSSR) - READ/WRITE

The TSSR is a 16-bit register. Although defined as a Read/Write register its contents cannot be modified by the LSI-11 bus. It can be read to examine status, but writing into it initializes the controller. A DATOB to the high byte of the TSSR, however, loads the extended TSDBX. The contents of the register are modified by the controller. If the initialize diagnostic fails, this register has alternate bit definitions.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	///		SCE	RMR	NXM	NBA	A17	A16	SSR	OFL	FC1	FC0	TC2	TC1	TC0	A00

BIT	NAME	DESCRIPTION
15	SC	SPECIAL CONDITION. When set, indicates that either an error was detected or an exception condition (Tape Mark on Read, Reverse Motion at BOT, etc.) occurred. Also set by error bits in TSSR (RMR and NXM). Indicates that the Termination Class bits are nonzero (unless RMR is the only error). Cleared by Initialize unless a self-test error is detected, in which case SC is set.
14	-	Not used.
13	SCE	SANITY CHECK ERROR. Set when the controller detects an internal failure, which is serious enough to inhibit transmission of a Message Buffer.
12	RMR	REGISTER MODIFICATION REFUSED. Set when the TSDB is written from the LSI-11 bus and Subsystem Ready (SSR) is not set. Causes the Special Condition (SC) bit to be set but no Termination Class because RMR can be set if TSDB is written while an ATTN message is being output. If ATTN is not enabled, RMR setting indicates a fatal controller problem or a software bug.
11	NXM	NONEXISTENT MEMORY. Set when trying a DMA transfer to/from a non-existant memory location (no response in 12 usec). May occur when fetching a Command Packet, fetching/storing data or storing a Message Packet. Can cause termination Class Codes 4 and 5 (bits 03-01).
10	NBA	NEED BUFFER ADDRESS. When set, indicates that a Message Buffer address is needed. Set by Initialize and by performing DATOB to TSDB (i.e., to enter Maintenance Mode). Cleared during Write Characteristics command with a valid address. If NBA=1 any command other than Write Characteristics terminates operation with Function Reject.

09-08 A17:A16 ADDRESS BITS 17-16. Displays bits 17 and 16 of the TSBA register that holds a Command Pointer or DMA address. Loaded from TSDB bits 01-00 when TSDB is written.

07 SSR SUB-SYSTEM READY. When set, indicates that the controller is not busy and is ready to accept new command pointer. Cleared by writing TSDB. Also cleared by Initialize, then set by the controller if the basic microdiagnostics are successfully passed.

06 OFL OFF-LINE. When set, indicates that the transport is off-line and unavailable for any tape motion commands. This bit does not indicate the current status of the Tape transport (updated on command completions). Can cause termination Class Codes 1 and 3 (bits 03-01).

05-04 FC1:FC0 FATAL TERMINATION CLASS CODE. Used to indicate the type of fatal error which has occurred. The code is valid only when the SC bit is set and the Termination Class Code (TC) bits are all set (111); they are clear otherwise. Can cause termination Class Code 7 (bits 03-01). The FC codes are:

0 Internal diagnostic failure.
See the Error Code byte (XST3) for the failed function. Initialize must be issued for the controller to accept further commands.
1 Reserved
2 Not used
3 Reserved

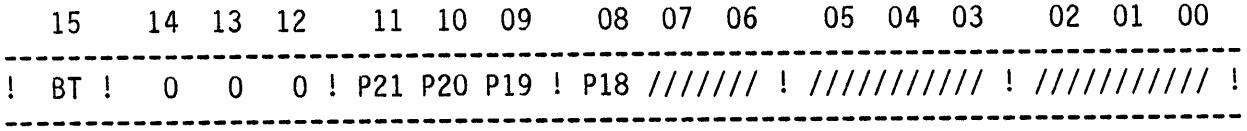
03-01 TC2:TC0 TERMINATION CLASS CODE. This 3-bit field acts as a word offset value whenever an error or exception condition occurs on a command. Each of the 8 possible values of this field represents a class of errors or exceptions. The conditions in each class have similar significance and recovery procedures (as applicable). The codes are:

0 Normal Termination
1 Attention Condition
2 Tape Status Alert
3 Function reject
4 Recoverable Error - tape position is one record down tape from start of function.
5 Recoverable Error - tape not moved
6 Unrecoverable Error - tape position lost
7 Fatal Controller Error - see Fatal Termination Class Codes (bits 05-04)
0 Not used

3.2.4 Extended Data Buffer (TSDBX) - WRITE ONLY

The Extended Data Buffer Register (TSDBX) is a Write-Only hardware byte register located at the fourth byte address of the STC-TSV11 1/O register block. This address corresponds to the high order byte of the TSSR register. The TSDBX is used to specify the most significant four bits of a 22-bit command pointer address, and also to allow an automatic tape boot sequence to be performed. TSDBX can be written only by a byte-access (DATOB) cycle addressed to the high byte of TSSR.

Once written, the contents of the least significant four bits of TSDBX are transferred to bits 18 through 21 of the internal TSBA (Bus Address) register for use as a command pointer. The low order 18 bits of the command pointer are specified by writing into the TSDB register, which starts operation and then clears TSDBX. Therefore, a subsequent load of the TSDB only will specify a 22-bit command pointer address with the high-order four bits equal to zero. For the TSDBX register to be properly written, the SSR (Subsystem Ready) bit in TSSR must be set. If it is not, the RMR (Register Modification Refused) bit will be set and no modification to TSDBX will occur. When the TSDBX is written, the SSR bit is not cleared. Therefore, RMR should be checked before TSDB is written. Writing the TSDB will begin processing on TSDBX. If the Boot bit is not set, the command pointer to the 22-bit TSDB will be retrieved, and command processing will begin. If the Boot bit is set, SSR will remain clear until the boot sequence is complete or until an error occurs.



BIT	NAME	DESCRIPTION
15	BT	BOOT COMMAND BIT. When written to 1, with SSR=1, causes the tape to be rewound to BOT, the first tape record to be skipped, and the second record (only the first 512 bytes of it) to be loaded into CPU memory space starting at location 0.
14-12	-	RESERVED. Should always be written as 0.
11-08	P21:P18	COMMAND POINTER BITS 21-18. When the TSDBX is written, and SSR=1, the data is loaded into bits 21-18 of the internal TSBA register. TSDBX is cleared after TSDB is written and is also cleared by Initialize.

3.2.5 Extended Status Register 0 (XST0)

The Extended Status Register 0(XST0) appears as the fourth word in the Message Buffer stored by the STC-TSV11 upon completion of a command or an Attention (ATTN).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TMK	RLS	LET	RLL	WLE	NEF	ILC	ILA	MOT	ONL	IE	VCK	PED	WLK	BOT	EOT

BIT	NAME	CODE DESCRIPTION
15	TMK	TAPE MARK DETECTED. Set whenever a Tape Mark is detected during a Read, Space, or Skip command, and also as a result of the Write Tape Mark or Write Tape Mark Retry commands. Can cause termination Class Code 2 (TSSR bits 03-01).
14	RLS	RECORD LENGTH SHORT. This bit indicates that either the record length was shorter than the byte count on Read operations, a Space Record operation encountered a tape mark or BOT before the position count was exhausted, or a Skip Tape Marks command was terminated by encountering BOT or a double tape mark (if that operational mode is enabled, see LET) prior to exhausting the position counter. Can cause termination Class Code 2 (TSSR bits 03-01).
13	LET	LOGICAL END OF TAPE. Set only on the Skip Tape Marks command when either two contiguous tape marks are detected, or when moving off of BOT and the first record encountered is a tape mark. The setting of this bit does not occur unless this mode of termination is enabled through use of the Write Characteristics command. Can cause termination Class Code 2 (TSSR bits 03-01).
12	RLL	RECORD LENGTH LONG. When set, indicates that the record read on a Read was longer than the byte count specified. Can cause termination Class Code 2 (TSSR bits 03-01).
11	WLE	WRITE LOCK ERROR. When set, indicates a write operation was issued but the tape does not contain a write enable ring. Can cause termination Class Codes 3 and 6 (TSSR bits 03-01).
10	NEF	NON-EXECUTABLE FUNCTION. When set, indicates that a command was not be executed for one of the following conditions: The command specified reverse tape direction but the tape was already at BOT. Any motion command when the Volume Check bit is set.

Any write command when the tape does not contain a write enable ring (also causes write Lock Status - WLE). Can cause termination Class Code 3 (TSSR bits 03-01).

09 ILC ILLEGAL COMMAND. Set when a command is issued and a Command field contains codes which are not supported. Can cause termination Class Code 3 (TSSR bits 03-01).

08 ILA ILLEGAL ADDRESS. Set when a command specifies an address more than 22 bits, or an odd address when an even one is required. Can cause termination Class Code 3 (TSSR bits 03-01).

07 MOT MOTION. Tape is moving. Indicates that the transport is asserting Formatter Busy or Rewinding status.

06 ONL ON LINE. When set, indicates that the transport is on-line and operable. A change in this bit can cause a Termination Class 1 if ATTENTIONS are enabled. If ONL is clear and a motion command is issued, it can cause a Termination Class 3. See TSSR bits 03-01.

05 IE INTERRUPT ENABLE. Reflects the state of Interrupt Enable bit supplied on the last command.

04 VCK VOLUME CHECK. When set, indicates that the transport has been either powered down or is off-line. Cleared by the Clear Volume Check (CVC) bit in the Command Headed word. This bit can cause a Termination Class of 3.

03 PED PHASE-ENCODED DRIVE. Always Set. Indicates that the transport is capable of reading and writing only phase encoded data.

02 WLK WRITE LOCKED. When set, indicates that the tape does not have a write enable ring installed (tape is write protected). Can cause termination Class Code 3 (TSSR bits 03-01).

01 BOT BEGINNING OF TAPE. When set, indicates that the tape is positioned at the load point as denoted by the BOT reflective strip on the tape. Can cause termination Class Code 3 (TSSR bits 03-01).

00 EOT END OF TAPE. This bit is set whenever the tape is positioned at or beyond the End of Tape reflective strip. Does not reset until the tape passes over the strip in the reverse direction under program control. If the controller is read buffering (pre-reading records from tape automatically) and the EOT strip is seen, this will not be sent until the program actually requests the record associated with the EOT. Can cause termination Class Code 2 (TSSR bits 03-01).

3.2.6 Extended Status Register 1 (XST1)

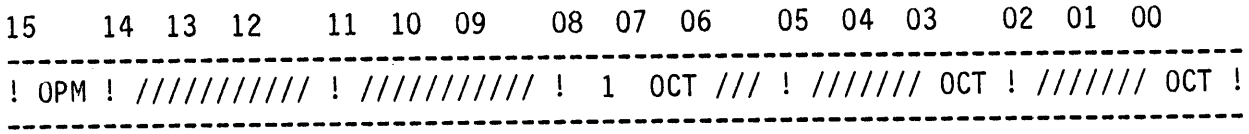
The Extended Status register 1 (XST1) appears as the fifth word in the Message Buffer stored by the STC-TSV11 upon completion of a command or on an Attention (ATTN).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	///		COR	///	///////////		////	0	0	0	0	0	0	UNC	///

BIT	NAME	DESCRIPTION
15	DLT	DATA LATE. Always zero. Can cause termination Class Code 4 (TSSR bits 03-01).
14	-	Not used.
13	COR	CORRECTED ERROR. Always zero. Can cause termination Class Code 4 (TSSR bits 03-01).
12-08	-	Not used.
07-02		Always set to 0
01	UNC	UNCORRECTABLE DATA OR HARD ERROR. Set in response to the transport asserting Hard Error, during a read or write to indicate that one of the following has occurred: False preamble detection False postamble detection Multichannel dropout Parity error without associated channel dropouts (could result from bad write Data Interface circuit in the controller) Loss of data envelope prior to postamble detection Excessive skew Can cause termination Class Code 4 (TSSR bits 03-01).
00	-	Not Used.

3.2.7 Extended Status Register 2 (XST2)

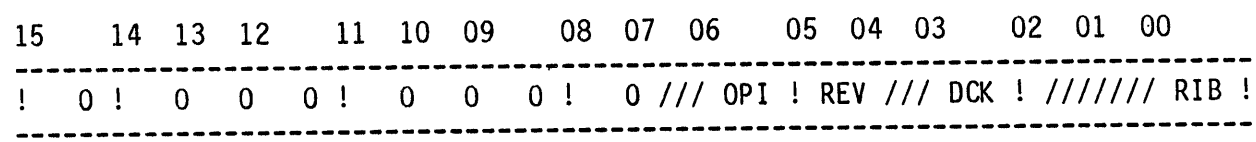
The Extended Status Register 2 (XST2) appears as the sixth word in the Message Buffer stored by the STC-TSV11 upon completion of a command or on an Attention (ATTN).



BIT	NAME	DESCRIPTION
15	OPM	OPERATION IN PROGRESS. Indicates tape has moved.
14-09	-	Not used.
08,03,00	OCT	OCTAL 211. Always set after Set Characteristics Command.
07,06-04 02,01	-	Not used.

3.2.8 Extended Status Register 3 (XST3)

Extended Status Register 3 appears as the seventh word in the Message Buffer upon completion of a command or on an Attention (ATTN).



BIT	CODE	DESCRIPTION
15-08	-	Not used. Always zeros.
07	-	Not used.
06	OPI	OPERATION INCOMPLETE. Set when Read, Space, or Skip operation has moved about 25 feet of tape without detecting any data of the tape.

05	REV	REVERSE. Set when the current operation caused reverse tape motion (includes the Retry commands as well as simple reverse Read, space, etc.). Cleared when operation is forward or rewind.
04	-	Not used.
03	DCK	DENSITY CHECK. Set when a PE identification Burst (IDB) is not detected while moving off of BOT. A Read, Space of Skip will complete (if no other errors occur) to allow tapes with the IDB wrong to be read.
02-01	-	Not used.
00	RIB	REVERSE INTO BOT. When set, indicates that a Read, Space, Skip or Retry command already in progress has encountered the BOT marker when moving tape in the reverse direction. Tape motion is halted at BOT.

3.2.9 Extended Status Register 4 (XST4)

Extended Status Register 4 (XST4) appears as the eighth word in the Message Buffer upon completion of a command or on Attention (ATTN).

The STC-TSV11 does not use the XST4. Bits 15-00 are always zeros.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

3.3 COMMAND PACKET DEFINITIONS

Table 3-1 lists the Command Set for the STC-TSV11.

COMMAND	DESCRIPTION
GET STATUS	Get Status (update the Extended Status registers in the message buffer in memory)
READ	Read Next (Forward)
WRITE	Write Next (Forward)
FORMAT	Write Tape Mark
CONTROL	Message Buffer Release Rewind and Unload Clean Tape (handle as a NO-OP) Rewind with Immediate Interrupt
INITIALIZE	Controller/Drive Initialize
SET CHARACTERISTICS	Load Message Buffer Address and Set Device Characteristics
POSITION	Space Records Forward Skip Tape Marks Forward Skip Tape Marks Reverse Rewind

TABLE 3-1: ASSIGNED COMMAND SET FOR STC-TSV11

The CPU issues a command to the STC-TSV11 by first building a Command Packet in CPU memory space (on a modulo-4 address boundary) then writing the address of the packet into the STC-TSV11 TSDB hardware register. The address written is the Command Pointer. If the STC-TSV11 is ready to accept a command, writing of the Command Pointer initiates command processing, in which the controller fetches the Command Packet and executes the command encoded within the packet.

Logically a Command Packet can be composed of one, two, three or four 16-Bit words, depending upon the type of command and the amount of information needed to proceed with execution. The following paragraphs describe each command in detail and its specific Command Packet format.

Certain bits of the Header Word and other words within the Command Packet are not defined for all commands. When building the Command Packet, the software should set these undefined bits to zero. If any bit is undefined or reserved with respect to a particular command and the bit is not zero, the command will not be executed and will be terminated with a Function Reject (See TSSR bits 03-01 - Termination Class 3).

The header (Word 1) of the command packet for the commands listed in Table 3-1 is shown below.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WORD 1	ACK	CVC	OPP	SWB	--COMMAND MODE--			IE	HDR TYPE		----COMMAND CODE----					

BIT	NAME	FUNCTION
15	ACK	ACKNOWLEDGE. This bit is set for issuing a command when the CPU owns the Message Buffer. Informs the STC-TSV11 that the Message Buffer is available for message packets. This passes ownership of the Message Buffer to the STC-TSV11. If the CPU has released ownership of the Message Buffer to the STC-TSV11 for Attentions and has not yet received an ATTN message, this bit should be 0.

Bits 14 through 12 are dependent on the command packets described in paragraphs 3.3.1 through 3.3.8.

BIT	NAME	DESCRIPTION
14	CVC	CLEAR VOLUME CHECK. When set, causes the Volume Check condition. Set when the transport is cleared to go from Off-Line to On-Line, allowing tape operations to be executed on the transport.
13	OPP	OPPOSITE. When set, reverses execution sequence of reread commands (e.g. Reread Next, Previous)
12	SWB	SWAP BYTES. When set, instructs the STC-TSV11 to alter the sequence of storing and retrieving tape data bytes from CPU memory. When SWB=0 (DEC protocol), the 1st byte in a word is the least significant byte (bits 7-0). When SWB=1 (industry standard protocol) the first byte of a word is to be bits 15 through 8.

11-08 COMMAND MODE Extension field to Command Code field. Allows further specification of device commands. (Table 3-2)

07 IE Interrupt Enable. 0 = Disable, 1 = Enable

06,05 HDR TYPE HEADER TYPE. Defines header type. Must be zero (1-word header).

04-00 COMMAND CODE Defines major command category. Used with Command Mode field to specify the command. See Table 3-2.

COMMAND CODE	COMMAND NAME	COMMAND MODE	MODE NAME
00001	READ	0000	Read Next (Forward)
00100	SET CHARACTERISTICS	0000	Load Message Buffer address and set device characteristics
00101	WRITE	0000	Write Data (Next)
00110	WRITE SUBSYSTEMS	0000	Enter Maintenance Mode and load test functions into memory (diagnostic use only - not for normal programming operations)
01000	POSITION	*0000	Space Records Forward
		*0001	Space Records Reverse
		*0010	Skip Tape Marks Forward
		*0011	Skip Tape Marks Reverse
		*0100	Rewind
01001	FORMAT	*0000	Write Tape Mark
		*0001	Erase
01010	CONTROL	*0000	Message Buffer Release
		*0001	Rewind and Unload
		*0010	Clean Tape function
		*0100	Rewind with Immediate interrupt
01011	INITIALIZE	*0000	Controller/Drive Initialize
01111	GET STATUS	*0000	Get Status (output END status message)

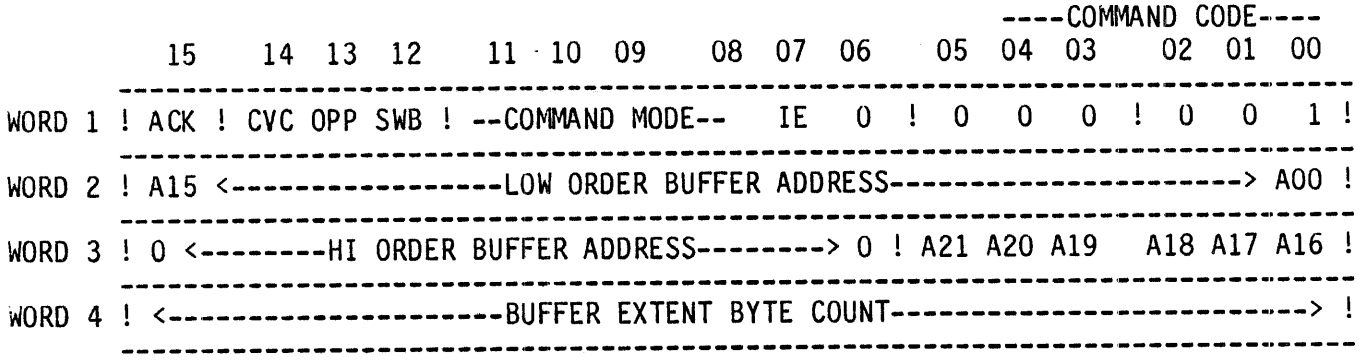
*1-word Command Packet

TABLE 3-2: COMMAND CODE AND MODE

3.3.1 Read Command Packet (Command Code 00001)

The command packet for a Read is shown below. The four normal modes of operation include two modes (Reread Previous and Next) that are further controlled by the OPP bit in the packet header word.

COMMAND MODE	DESCRIPTION
0000	Read Next (Forward)
0001	Read Previous (Reverse)
0010	Reread Previous
OPP = 0	Space Reverse, Read Forward
OPP = 1	Read Reverse, Space Forward
0011	Reread Next
OPP = 0	Space forward, Read Reverse
OPP = 1	Read Forward, Space Reverse



Word 1 is the Header Word (Section 3.3). Word 2 and Word 3 specify the address of the data buffer in CPU memory space where the data read from tape is to be deposited. Notice that Word 3 bits 15-06 must be zero; if not all zeros, the command is aborted with Function Reject termination with Illegal Address (ILA) error status. Word 3 specifies the number of bytes expected in the tape record to be read. A byte count of 0 specifies that 65,536 (64K) bytes are expected.

3.3.2 Set Characteristics Command Packet (Command Code 001000)

The Set Characteristics Command Packet defines the location and size of the message buffer in the CPU memory and some specific controls for executing other commands. When done, this command clears the Need Buffer Address (NBA) in TSSR. If the command is rejected because an illegal address was specified, NBA will be set.

		---COMMAND MODE---										----COMMAND CODE----					
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WORD 1	ACK	CVC	0	0	0	0	0	0	IE	0	0	0	0	1	0	0
WORD 2	A15 <---------- LOW-ORDER CHARACTERISTIC DATA ADDRESS ----------> A00															
WORD 3	0 <-HI ORDER CHARACTERISTICS DATA ADDRESS-> 0				A21	A20	A19		A18	A17	A16					
WORD 4	<----------BUFFER BYTE COUNT---------->															

Word 1 is the header word (section 3.3). Words 2 and 3 define the address of the characteristics data buffer, which must reside on an even address boundary in CPU memory. Notice that Word 3 bits 15-06 must be zeros. Word 4 specifies the number of bytes of the data buffer, which must be at least a count of 6 to allow the first three characteristic data words to be fetched. If byte count is less than 7, Word 1 will not be fetched, and the current values of the Characteristic Mode bits stored in the controller are retained.

The Set Characteristics Data format is shown below.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WORD 1	A15 <----------LOW ORDER MESSAGE BUFFER ADDRESS----------> A00															
WORD 2	0 <----HI ORDER MESSAGE BUFFER ADDRESS----> 0				A21	A20	A19		A18	A17	A16					
WORD 3	<---------LENGTH OF MESSAGE BUFFER (AT LEAST 16 BYTES LONG)---------->															
WORD 4	0	<-------MUST BE ZEROS-------->			0	ESS	ENB	EAI	ERI	0	0	0	0			

NAME	FUNCTION
ERI	ENABLE MESSAGE BUFFER RELEASE INTERRUPTS to the CPU. If this bit is 0, interrupts will not be generated when a Message Buffer Release command is received by the coupler; only Subsystem Ready (SSR) will be reasserted. If this bit is 1, an interrupt will be generated.

EAI ENABLE ATTENTION INTERRUPTS. When this bit is 0, attention conditions such as offline and online will not result in interrupt to the CPU. If this bit is 1, interrupts will be generated once the coupler owns the message buffer.

ENB ENABLE SKIP TAPE MARKS STOP AT BOT. This bit is meaningful only if the ESS bit is set. If the drive is at BOT when a Skip Tape Marks command is issued and the first record seen is a tape mark, then the transport will set LED (XSTAT0) and stop after the first tape mark. If ENB is clear, the drive will not set LET but just count the tape mark and continue.

ESS ENABLE SKIP TAPE MARKS STOP. When set, the transport stops during a Skip Tape Mark command when a double tape mark (two contiguous tape marks) is detected. If cleared, the Skip Tape Marks command will terminate only on Tape Mark Count Exhausted or if BOT is detected.

3.3.3 Write Command Packet (Command Code 00101)

The Write Command Packet is shown below.

		---COMMAND MODE---										----COMMAND CODE----						
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
WORD 1	! ACK	! CVC	0	SWB !	0	0	0	! 0	IE	0	! 0	0	0	! 1	0	1	!
WORD 2	! A15	<----------LOW ORDER BUFFER ADDRESS---------->														A00	!
WORD 3	! 0	<--------HI ORDER BUFFER ADDRESS-------->							0	! A21	A20	A19	A18	A17	A16		!
WORD 4	!	<----------BUFFER EXTENT BYTE COUNT---------->															!

Word 1 is the Command Packet Header (Section 3.3). Words 2 and 3 specify the address of the data buffer in the CPU memory space where the data to be written onto tape is stored. Notice that Word 3 bits 15-06 must be zero or the command will be aborted with Function Reject termination with Illegal Address (ILA) error status. Word 4 defines the number of bytes available in the data buffer and the number of bytes to be written onto tape. A byte count of 0 specifies that 65,536 (64K) bytes are to be written.

If a Write command is executed at or beyond the EOT marker, the data will be written by a Tape Status Alert (TSA) termination will occur. EOT will remain set until passed in the reverse direction.

3.3.4 Position Command Packet (Command Code 01000)

This command causes the tape to space records forward or reverse, skip tape marks forward or reverse, or to rewind to BOT. There are four Command Modes for the Position Command Packet shown below.

COMMAND MODE	FUNCTION
0000	Space Records Forward
0001	Space Records Reverse
0010	Skip Tape Marks Forward
0011	Skip Tape Marks Reverse
0100	Rewind (Record Count Ignored)

		---COMMAND MODE---								----COMMAND CODE----					
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WORD 1	ACK	CVC	0	0	--COMMAND MODE---				IE	0	0	0	1	0	0	0
WORD 2	<----------TAPE MARK/RECORD COUNT---------->															

Word 1 is the Command Packet Header (Section 3.3). Word 2 is a 16-bit positive integer that specifies the mark/record count. Word 2 must be exact for Skip Tape Mark and Space Record command modes.

A Space Records operation automatically terminates when a tape mark is traversed. Record Length Short (RLS) is also set if record count was not decremented to zero.

A Skip Tape Marks command terminates when it encounters a double tape mark and the Enable Skip Stop mode is specified (ESS bit set) in the Set Characteristics Data Buffer. Termination will also occur if a tape mark is the first record off BOT and ESS and ENB bits are set in the Set Characteristics Data Buffer. Record Length Short (RLS) is set if the record count is not decremented to zero.

A Space Records Reverse or Skip Tape Marks Reverse that runs into BOT set Reverse Into BOT (RIB) and causes a tape status alert termination. If the tape is positioned between BOT and the first record and a space reverse or skip reverse is done, RIB will set and the residual frame count will equal the specified count in the original command.

3.3.5 Format Command Packet (Command Code 01001)

This command writes/rewrites a tape mark or erases tape. There are three Command Modes for the Format Command Packet shown below.

COMMAND MODE	FUNCTION
0000	Write Tape Mark
0001	Erase
0010	Write Tape Mark Retry (Space Reverse, Erase, Write Tape Mark)

		---COMMAND MODE---								----COMMAND CODE----					
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WORD 1	ACK	CVC	0	0	--COMMAND MODE---				IE	0	0	0	1	0	0	1
WORD 2	<----------NOT USED---------->															

Word 1 is the Header Command Word (Section 3.3). Word 2 is present (fetched by the controller), but is not used in the command.

Executing a Format command at or beyond EOT will cause a Tape Status Alert Termination. The EOT bit will remain set until the EOT marker is passed in the reverse direction.

A Write Tape Mark or Erase command issued at BOT will cause the PE Identification Burst (IDB) to be written on the tape. If, during this operation, the IDB is not received from the transport, the Density Check (DCK) error will be set and Tape Position Lost termination will occur.

The Write Tape Mark Retry causes a space reverse (over the previous record), followed by an erase of 3.75" of tape and then by a Write Tape Mark (which erases 3.75" more of tape before writing the file mark). If the tape is positioned at BOT when the Write Tape Mark Retry command is issued, the operation will be aborted with Function Reject termination and the Nonexecutable Function (NEF) error bit will be set.

3.3.6 Control Command Packet (Command Code 01010)

There are four modes associated with the Control Command Packet shown below:

COMMAND MODE	FUNCTION
0000	Message Buffer Release
0001	Rewind and Unload
0010	NO-OP
0100	Rewind with Immediate Interrupt

		---COMMAND MODE---								----COMMAND CODE----					
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WORD 1	ACK	CVC	0	0	--COMMAND MODE---			IE	0		0	0	1	0	0	1
WORD 2	<----------NOT USED---------->															

The Message Buffer Release command (with ACK bit set) lets the controller own the Message Buffer so it can update the status in the message buffer area on an Attention (ATTN).

The Rewind and Unload command rewinds the tape completely onto the supply reel and places the transport offline. When this command is executed, termination (and an interrupt if IE is set) will occur immediately.

The NO-OP command causes immediate termination with no tape motion.

The Rewind with Immediate Interrupt command rewinds the tape to BOT. Termination response to the CPU occurs at the start of the rewind rather that when the tape reaches BOT, as in a normal Rewind command. This command is used in a multi-transport system to select another unit after issuing a rewind. If a transport is rewinding and another tape motion command is issued to it, the new controller will wait until the tape has been rewound to BOT before proceeding with the new command. During execution of a Rewind with Immediate Interrupt, the Motion (MOT) bit in XSTO is set if a Get Status command is performed.

3.3.7 Drive Initialize Command Packet (Command Code 01011)

The Drive Initialize Command Packet is shown below.

	---COMMAND MODE---												----COMMAND CODE----					
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WORD 1	ACK	CVC	0	0	0	0	0	0	IE	0	0	0	1	0	1	1
WORD 2	<----------NOT USED---------->															

If there are no microdiagnostic errors, this command is treated as a NO-OP. If error exist, the command is the same as a write into the TSSR register. In either case, IFEN to the Tape Transport is pulsed to stop runaway commands.

3.3.8 Get Status Command Packet (Command Code 01111)

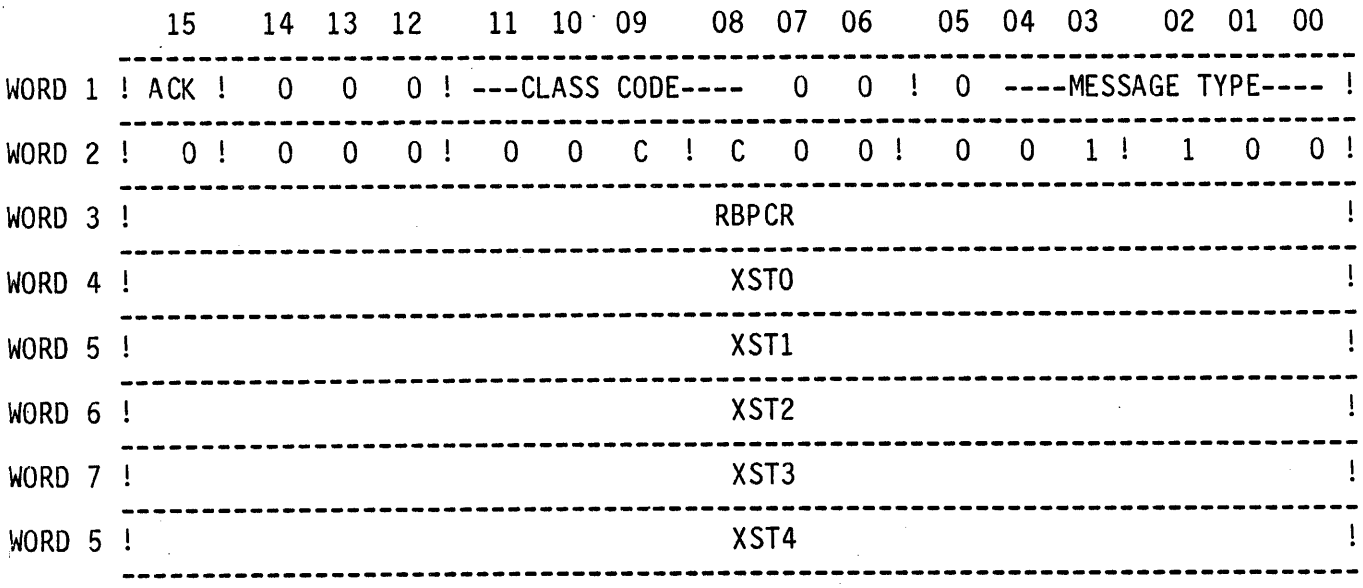
The Get Status Command Packet is shown below;

	---COMMAND MODE---												----COMMAND CODE----					
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WORD 1	ACK	CVC	0	0	0	0	0	0	IE	0	0	0	1	1	1	1
WORD 2	<----------NOT USED---------->															

This command deposits a message packet in the Message Buffer area to update the Extended Status registers. However, since the transport automatically updates the Extended Status registers after the end of any command (except Message Buffer Release), this command only needs to be used when the transport has been idle for some time, or when a status register update is desired without performing a tape motion command, or to read the unit number of the currently selected tape transport (deposited in bits 02-00 of the Extended Status Register 2).

3.4 MESSAGE PACKET FORMAT

The message packet format is shown below. This format is used for all messages, whether at the end of a command or for an Attention.



WORD 1

BIT	CODE	DESCRIPTION
15	ACK	ACKNOWLEDGE. This bit is set by the transport to tell the CPU that the Command Buffer is available for pending or subsequent command packets. An ATTN message will not set this bit since the controller does not own the Command Buffer.
14-12	RESERVED	Reserved for future expansion. Must be set as zeros.
11-08	C	CLASS CODE FIELD. These bits define the class of failure determined for the rest of the message buffer when the Message Type field is not indicating a normal END message. The codes are:

ATTN	0000	On or off line
ATTN	0001	Microdiagnostic failure
FAIL	0000	Not used.
FAIL	0001	Illegal Command (ILC), Illegal Address (ILA), or Need Buffer Address (NBA) on a tape motion command.

FAIL	0010	Write Lock error on Non-executable function.
Fail	0011	Microdiagnostic Error.

07-05 - PACKET FORMAT. Specifies a one-word message. Must be zeros.

04-00 - MESSAGE TYPE. Indicates the general type of message contained in the buffer. This field is related to the Termination Class Code in the TSSR register as follows:

MESSAGE TYPE	TERMINATION CLASS CODE	DEFINITION
10000	0,2	End
10001	3	Fail
10010	4,5,6,7	Error
10011	1.7	Attention

WORD 2

15-08 RESERVED Reserved for future expansion. Appears as zeros.

07-00 - DATA FIELD LENGTH. Specifies how many bytes of information (Word 3 through Word 8) follow this word in the message packet. Must be binary value of 00001100 (decimal 12), indicating the packet contains the RBPCR plus five extended status registers.

WORD 3

RESIDUAL BYTE/RECORD/FILE COUNT REGISTER. After a Read command, this word contains the difference between the number of bytes specified in the command and the number of bytes actually transferred from tape; i.e., how much the tape record fell short of the expected length. After a Space Records or Skip Tape Marks command, this register contains the difference between the number of records or tape marks specified in the Count word of the command and the number of records or files actually skipped. Note that spacing and skipping operations can terminate before the count is exhausted for many reasons (tape mark, BOT, etc.).

WORD 4 THROUGH WORD 8

See Paragraphs 3.2.5 through 3.2.9 for descriptions of Extended Status Registers 0 through 4 (XST0 through XST4).