REVISIONS					
EFFECTIVITY	AUTH	LTR	DESCRIPTION	DATE	APPROVED

DIAGRAM 202143

CHANGE ACTIVITY PENDING, YES ☐ NO ☐

TELEFILE PROPRIETARY

REV																											
SHEET	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
REV																											
SHEET	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52
REV STATUS	REV																										
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	

UNLESS OTHERWISE SPECIFIED	CONTRACT NO.		**Telefile**
DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH:	SIGNATURE	DATE	TITLE
.X = .1	DRAWN		IFX/7902 PRODUCT SPECIFICATION
.XX = .03	CHECK		
.XXX = .010	ENGR.		
ANGLES = 0° 30'	PROJ. ENGR.		
DO NOT SCALE DRAWING	QUAL. ASSURANCE		
MATERIAL:	RELIABILITY		SIZE: A — CODE IDENT NO.: 51360 — SPEC. NO.: SS-600-0058-1A
	PROD. DESIGN		
	OTHER APPROVALS		SCALE — REV — SHEET 1 OF

TF-600-0023-1A

DISTR NO.

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1.0 SCOPE

This document describes the functional characteristics of the IFX/7902 logic module contained in the TELEFILE T3281 Disk Controller. The module is designed to supply interface functions between the controller's internal processor and the 7902 modules which comprise the controller interface to the Xerox Sigma I/O processor.

1.1 DEFINITION OF TERMS

In the following description the terms "processor", "IOP" and "CPU" are used as follows:

processor - refers to the microprocessor function described in Reference 2.2

IOP - refers to the input/output processor function of the Xeros Sigma computer

CPU - refers to the Xerox Sigma computer

2.0 APPLICABLE REFERENCE DOCUMENTS

2.1	SS-600-0064-1A	Telefile Model T3281 Disk Controller Product Specification
2.2	SS-600-0050-1A	Microprocessor Control Board Product Specification
2.3	SS-600-0056-1A	Disk Drive Interface Product Specification
2.4	SS-600-0052-1A	Quad Port Data Buffer Product Specification
2.5	SS-600-0057-1A	T7902 Product Specification
2.6	XDS 900973D	XDS SIGMA Computer Systems Interface Design Manual
2.7	SS-600-0054-1A	Data Encoder/Decoder Product Specification

3.0 GENERAL

The IFX/7902 module interfaces to other components of the T3281 controller as shown in Figure 3-1. The module communicates with and is controlled by the processor function described in Reference 2.2. It provides an adapter function between the 7902 modules (Reference 2.5) and the processor and data buffer (Reference 2.4) functions. The IFX module and the two 7902 modules comprise the controller interface to the Xerox Sigma series I/O processor (IOP).

The IFX module provides the following functions:

a. control of data transmission between the 7902 and the data buffer;
b. registers to hold STH, TDV, AIO and operational status bytes required by the I/O processor;
c. device selection and status response on I/O instructions generated by the Xerox CPU;
d. monitoring of 7902 status by the processor;
e. monitoring by the processor of the order byte received from the IOP during order-out service connections;
f. control by the processor of interrupt and order-in calls sent to the IOP;
g. attention interrupt store;
h. device interrupt modifier bit store;
i. release interrupt mark store.

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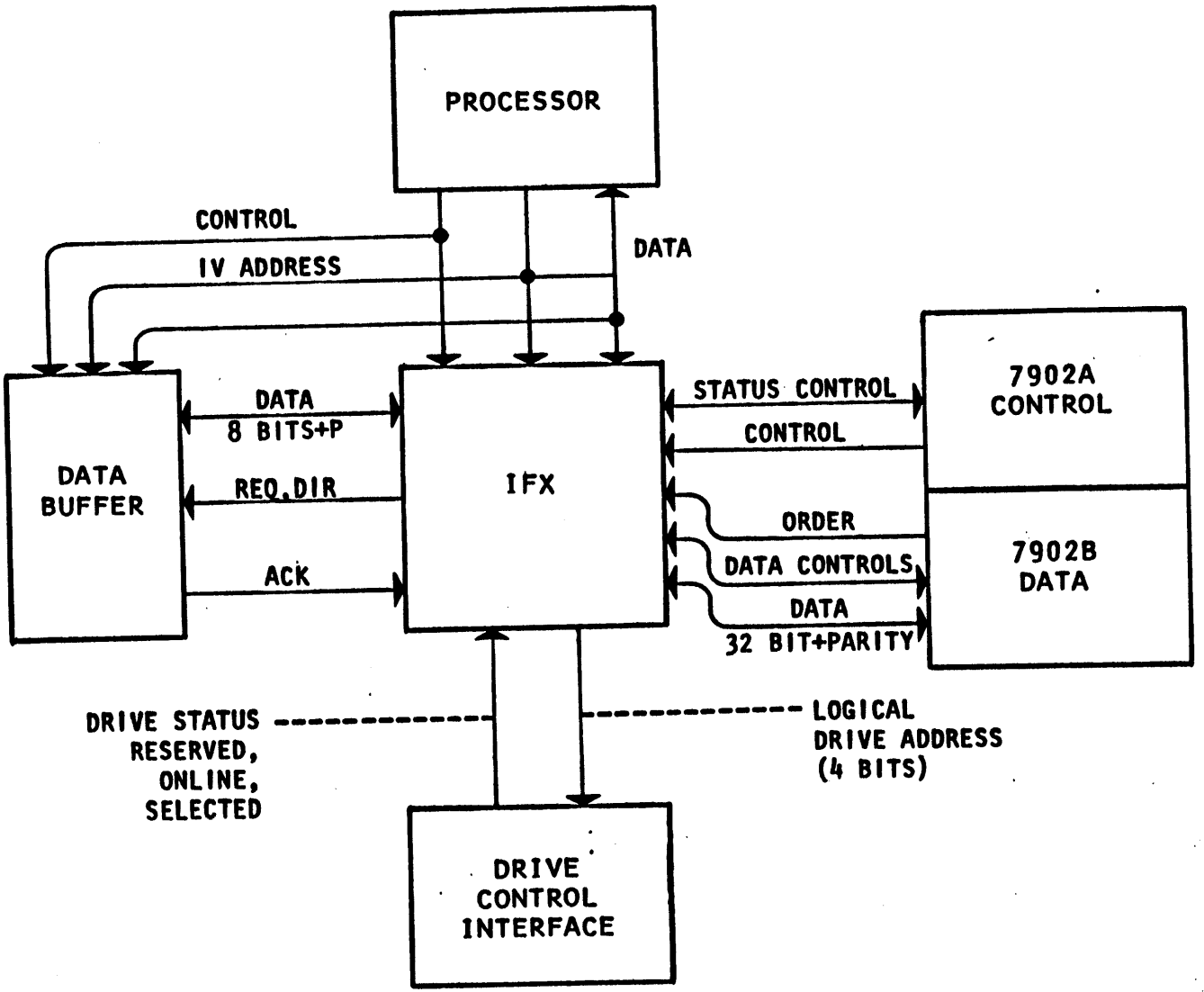

Figure 3-1. IFX System Interface

SIZE	CODE IDENT NO.	SPEC. NO.
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The processor micro code will set up most status and control functions at the 7902 interface. However, there are some functions required during the execution of I/O instructions generated by the CPU in which the timing requirements are too restrictive to allow any involvement of the processor in their execution. In these cases, the IFX hardware will handle these functions. The operation of the IFX for various I/O commands or functions is described briefly in the following.

3.1 DEVICE SELECTION--I/O INSTRUCTIONS

Input/Output instructions SIO, TIO, HIO and TDV all address discrete devices which must be selected in order to return status to provide proper condition code (see 3.8) and status response to the IOP. The selection function and response is accomplished by the IFX hardware in order to provide minimal IOP bandwidth usage by I/O instructions.

The controller processor, when the controller is not busy, may be selecting devices in order to obtain status, or for operational purposes in the case of in-line diagnostics, disk back up on tape, etc. The potential conflict of the processor and the IOP will be resolved in the following way:

a. the processor, if it is selecting devices for any purpose when the controller is not busy executing orders received from the IOP, will set one of two control bits indicating the device interface functions are busy in a "monitoring" or "operating" mode (see Reference 2.7, Section 3.14.5).

b. an I/O instruction received when the "monitoring" bit is set will cause the following events:

   1. a SUSPEND signal will be issued to the processors temporarily stopping its operation;
   2. any device tag function established by the processor will be inhibited;
   3. the device addressed by the I/O instruction will be selected, status returned to generate proper condition code bits (see 3.8) and status byte;
   4. the tag function inhibit will be removed;
   5. the SUSPEND signal will be removed from the processor allowing it to resume running.

c. an I/O instruction received when the "operating" bit is set will be rejected. The condition codes returned will indicate that "SIO may not be accepted" or "controller busy with other device" as applicable. The STH status (see 4.4) returned will indicate controller is "operationally" busy (bit 7 will be set).

3.2 START I/O--SIO

When an SIO is received from the IOP, the device will be selected as described in 3.1, its status monitored, and if proper, the SIO will be accepted. The 7902 will go busy and automatically execute an order-out service call. The 7902 "busy" status and "order received" status may be monitored by the processor as described in 4.2. The processor must, in executing its idle program, monitor this status frequently in order not to delay the start of order execution.

Once begun, execution of the order will continue until:

a. a COUNT DONE or UNUSUAL END (IOP HALT) is received from the IOP (see 4.2);
b. a HALT I/O instruction is received addressing the device on which the order is being executed;
c. an I/O RESET occurs, or
d. an error is detected in the order execution.

For cases 1 and 4, the processor will initiate an order-in service connection (see 9.7). As a result of the order-in connection, the 7902 will go not busy or another order will be chained. For the latter case, the order-out service connection will be accomplished automatically by the 7902 and the "order received" status (see 4.2) set.

Cases 2 and 3 are described in other paragraphs.

3.3 TEST I/O--TIO

The TIO instruction is used by the Xerox software to provide information necessary to determine the current status of the device, controller, and IOP. The device is selected as described in 3.1 and condition code bits CC1 and CC2 (see 3.8) and the STH status byte (4.4) are returned by the IFX. No operations are initiated or terminated by this instruction and no processor action is required.

3.4 HALT I/O--HIO

The HIO instruction is used to provide an unconditional halt to current operation and initialize the IFX/7902 interface. When the controller is busy, only an HIO addressing the device for which the order is being executed will be accepted. In this case, the operation will be aborted, the device released from reserve, any device interrupt enables (see 4.13) for the device will be cleared, the 7902 will go not busy and the processor will be interrupted.

If an HIO is accepted when the controller is not busy the addressed device will be released from reserve, and any device interrupt enables (see 4.13) will be cleared but the processor will not be interrupted.

3.5 TEST DEVICE--TDV

The TDV instruction will be used to return a status byte depicting the condition of the device and controller during or following the operation initiated by the most recent SIO. The device is selected as described in 3.1 and condition code bits and status returned (see 4.5). The TDV will not affect the state of the IFX, no operation is initiated or terminated by it and no processor action is required.

3.6 ACKNOWLEDGE I/O INTERRUPT--AIO

The AIO instruction is used to acknowledge an input/output interrupt and to identify the I/O subsystem causing the interrupt. No processor action is required on the AIO itself but the processor must set-up the AIO status (see 4.6) bit 0 prior to issuing an order in service call (see 4.7) or set-up AIO status and device address prior to issuing a device interrupt call (see 4.13). When an AIO is accepted, the AIO status byte, condition code bits, and device address are returned to the IOP and the enable flag for the specific (device) interrupt is cleared automatically by IFX hardware.

3.7 I/O RESET

When an I/O RESET function isreceived, all reserved devices are released from reserve, all interrupt enables are cleared and the 7902 and IFX are reset. The processor will be interrupted as described for an HIO.

3.8 CONDITION CODE BITS CC1, CC2

Condition code bits CC1 and CC2 are returned to the IOP on I/O instructions to describe the general status of the addressed I/O device and controller. The IFX and 7902 hardware generate these bits based on status signals from the addressed device, control state of the IFX and address recognition and control signals in the 7902. No action by the processor is required in generating these bits for any I/O instruction.

The condition code response for I/O instruction is shown in Table 3-1.

4.0 IFX BLOCK DIAGRAM

The block diagram for the IFX is shown in Figure 4-1. The characteristics of its functional blocks are described in the following.

4.1 PROCESSOR INTERFACE

Control of the IFX/7902 module is accomplished by the processor via its I/O interface which is described in Reference 2.2. It is assumed in the following description that the reader has a basic knowledge of the processor I/O.

4.1.1 Processor Data Bus

Data and commands will be transferred between the processor and IFX via the bilateral data bus BIVB0 through BIVB7. The module will present a maximum load to the bus of:

Current sink:	one TTL unit load maximum
Leakage:	one TTL driver leakage load maximum

I/O Instruction	CC1	CC2	Significance
SIO	0	0	I/O address recognized and SIO accepted.
	0	1	I/O address recognized, SIO not accepted.
	1	0	Not applicable.
	1	1	I/O address not recognized.
HIO	0	0	I/O address recognized and device not "busy" when halt occurred.
	0	1	I/O address recognized and device "busy" when halt occurred.
	1	0	HIO not accepted; controller "busy" with device other than one addressed.
	1	1	I/O address not recognized.
TIO	0	0	I/O address recognized and SIO can currently be accepted.
	0	1	I/O address recognized, but SIO cannot be currently accepted.
	1	0	Not applicable.
	1	1	I/O address not recognized.
TDV	0	0	I/O address recognized.
	0	1	Device controller in test mode.
	1	0	Controller busy with a device other than one addressed.
	1	1	I/O address not recognized.
AIO	0	0	Normal interrupt recognition.
	0	1	Unusual condition*, interrupt condition, or controller is switched to a test mode.
	1	0	Not applicable.
	1	1	No interrupt recognition.

*An unusual condition is one in which the Seek timeout error, unusual end, or transmission error storage elements were set in the previous operation.

Table 3-1. Condition Codes for I/O Instructions

SIZE	CODE IDENT NO.	SPEC. NO.
A	51360	SS-600-0058-1A
SCALE	REV.	SHEET 9 OF

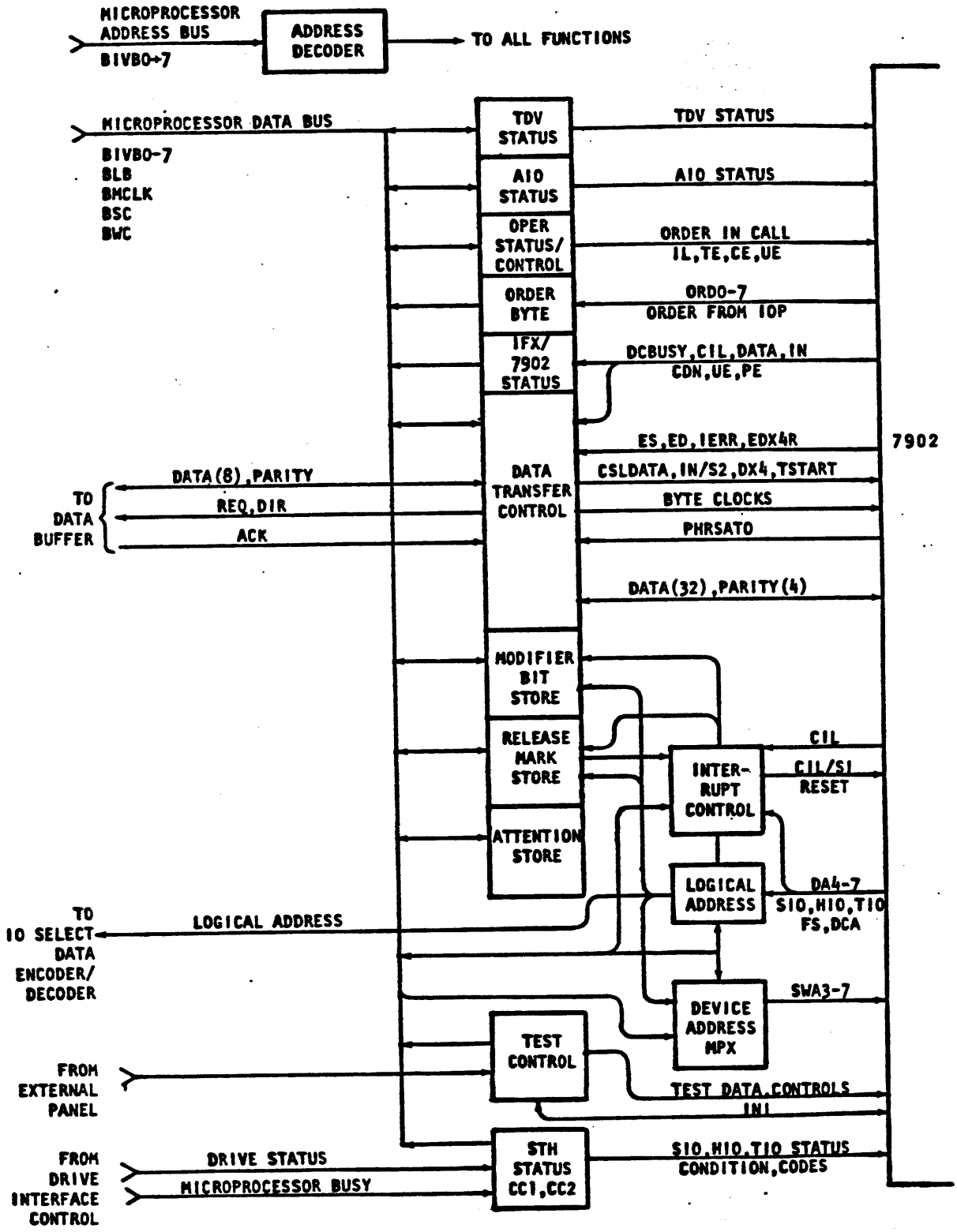

Figure 4-1. IFX/7902 Block Diagram

SIZE	CODE IDENT NO.	SPEC. NO.
A	51360	SS-600-0058-1A
SCALE	REV.	SHEET 10 OF

The IFX interface to the processor data bus is accomplished by transceiver circuits. The driver portion of the transceiver will be enabled only when the address block assigned to the module appears on the processor I/O address bus and an input operation is being executed.

Control signals BLB-1, BMCLK-0, BSC-0 and BWC-0 will be used by the IFX to enable and time commands and data transfer from/to the processor:

BLB-1 Interface vector left bank select. Enables module/processor I/O functions when high.

BMCLK-0 Processor master clock signal used to time data output and address changes.

BSC-0, BWC-0 Control signals which determine processor input or output as per:

BSC-0	BWC-0	
0	X	No IFX I/O Function
1	0	Data output on bus by processor
1	1	Data input on bus to processor

4.1.2 Address Decoder

The address decoder receives and stores inputs from the processor interface vector address bus BIVAD0 through BIVAD7. The contents of the bus are latched into the decoder on the trailing edge of the master clock BMCLK-0. The contents of the latches, in combination with control signals BLB-1, BMCLK-0, BSC-0 and BWC-0, are decoded to:

a. Enable the transceiver drivers for any data input function with interface vector address 120_8 through 157_8.

b. Produce register clocks or control functions for data output instructions with interface vector addresses of 120_8 through 157_8 (left bank). The clocks or control pulses will be produced during the low portion of the processor master clock BMCLK-0 duty cycle.

The address decoder will be implemented with high speed Schottky logic in order to maintain minimum propagation delays. A summary of interface vector address assignments for the IFX module is shown in Table 4-1.

ADDRESS	BANK	BIT FIELD	FUNCTION	COMMENT
120 (50)	L	0 1 2 3 4 5 6 7	DATA IN INTERRUPT PENDING COUNT DONE UNUSUAL END PARITY ERROR ORDER RECEIVED BUSY	IFX STATUS SEE 4.2 - READ ONLY
121 (51)	L	0→7	ORDER BYTE	READ ONLY SEE 4.3
122 (52)	L	0→7	SIO, TIO, HIO STATUS	READ ONLY SEE 4.4 (TABLE 4-2)
123 (53)	L	0→7	TDV STATUS	BIDIRECTIONAL SEE 4.5 (TABLE 4-3)
124 (54)	L	0→7	AIO STATUS	BIDIRECTIONAL SEE 4.6 (TABLE 4-4)
125 (55)	L	0→7	OPERATIONAL STATUS (ORDER IN)	BIDIRECTIONAL SEE 4.7
126 (56)	L	0→7	BYTE COUNTER - IOP LOWER BYTE	READ ONLY SEE 4.8.4
127 (57)	L	0→7	BYTE COUNTER - IOP UPPER BYTE	READ ONLY SEE 4.8.4
130 (58)	L	0→7	DATA CONTROL (IOP DATA TRANSFER)	BIDIRECTIONAL SEE 4.8.5
131 (59)	L	0→7	MODIFIER BITS DEVICES 0→7	READ ONLY SEE 4.9.1
132 (5A)	L	0→7	MODIFIER BITS DEVICES 8→E	READ ONLY SEE 4.9.1
133 (5B)	L	0→7	SET BIT STORE	BIDIRECTIONAL SEE 4.12.1
134 (5C)	L	0→7	RESET BIT STORE	BIDIRECTIONAL SEE 4.12.2
135 (5D)	L	0→7	BIT STORE CONTENTS (DEVICE INTERRUPT FLAGS)	READ ONLY SEE 4.13.1

Table 4-1. IFX Interface Vector Address Assignment 1/3

SIZE	CODE IDENT NO.	SPEC. NO.
A	51360	SS-600-0058-1A
SCALE	REV.	SHEET 12 OF

ADDRESS	BANK	BIT FIELD	FUNCTION	COMMENT
136 (5E)	L	0→7	INTERRUPT CALL (DEVICE INTERRUPT)	BIDIRECTIONAL SEE 4.13.2
137 (5F)	L	0→7	CONTROL (RELEASE INTERRUPT, DEVICE SELECT, ETC.)	BIDIRECTIONAL SEE 4.14
140 (60)	L	0 1 2 3 4→7	DUAL ADDRESS MODE DISK CONTROLLER LSB 0 CONTROLLER ADDRESS LSB DEVICE ADDRESS	READ ONLY DEVICE LOGICAL ADDRESS FROM IOP SEE 4.15
141 (61)	L	0→6 7	0 7902 ONLINE	BIDIRECTIONAL 7902 OFFLINE CONTROL SEE 4.17
142 (62)	L	0→7	IOP DATA A BYTE	BIDIRECTIONAL TEST DATA SEE 4.18.1
143 (63)	L	0→7	IOP DATA B BYTE	
144 (64)	L	0→7	IOP DATA C BYTE	
145 (65)	L	0→7	IOP DATA D BYTE	
146 (66)	L	0→7	IOP DATA ALL BYTES (A, B, C, D)	
147 (67)	L	0 1 2 3 4 5 6 7	SIO HIO AIO FS ASC TIO TDV IORST (I/O RESET)	BIDIRECTIONAL TEST CONTROL I/O FUNCTIONS SEE 4.18.2
150 (68)	L	0 1 2 3 4 5 6 7	EDX4 EDX2 STEP PHASE CLOCK IERR ES ED RSA	BIDIRECTIONAL TEST CONTROL IOP TIMING SEE 4.18.2

Table 4-1. IFX Interface Vector Address Assignment 2/3

SIZE	CODE IDENT NO.	SPEC. NO.
A	51360	SS-600-0058-1A
SCALE	REV.	SHEET 13 OF

ADDRESS	BANK	BIT FIELD	FUNCTION	COMMENT
151 (69)	L	0 1 2 3 4 5 6 7	FSL CC1 (DOR) CC2 (IOR) CCH CIL CSL DX4 RS	READ ONLY TEST CONTROL 7902/IOP CONTROL
152 (6A)	L	0→7	FUNCTION RESPONSE LINES FRX0→FRX7	READ ONLY SEE 4.18.2

Table 4-1. IFX Interface Vector Address Assignment 3/3

SIZE	CODE IDENT NO.	SPEC. NO.
A	51360	SS-600-0058-1A
SCALE	REV.	SHEET 14 OF

4.2 IFX STATUS BYTE--INTERFACE VECTOR 120_8

The processor may monitor status of the IFX/7902 interface to the IOP via input functions utilizing interface vector address 120 octal (left bank). The bit significance of the status byte returned to the processor is described in the following:

Bit	Function
0	DATA. When true, indicates that data transfers may be accomplished. See bit 1.
1	IN. Indicates direction of data transfers between the 7902 and IOP. Bits 0 and 1 define IFX/7902 operating modes per:

Bit 01	Mode
00	Order out
01	Order in
10	Data out
11	Data in

2	INTERRUPT PENDING. Set if an interrupt is pending (issued, but not acknowledged by an AIO instruction).
3	COUNT DONE. Set by the IOP via a terminal order when it has received or transmitted all data bytes for the current order. Bit also may be set by the processor (see 4.7).
4	UNUSUAL END. Set by the IOP via a terminal order if an abnormal condition has been detected in the operation for the current order. Bit is set by the processor (see 4.7) if any error condition is detected in execution of an order as described in Section 4.3.2 of Reference 2.1.
5	PARITY ERROR. Bit is set if parity error is detected in any data transmission between the IOP and IFX/7902.
6	ORDER RECEIVED. Bit is set when an order byte is received from the IOP during an order out service connection. The bit may be reset by the processor (see 4.8.5).
7	BUSY. Bit is set when an SIO has been accepted and indicates that the controller may process orders. Bit will be reset by a terminal order appended to an order-in service connection in which unusual end is set or order chaining is not required, by an HIO or I/O RESET.

4.3 ORDER BYTE--INTERFACE VECTOR 121_8

The order byte acquired automatically by the 7902 as a result of acceptance of an SIO or command chaining may be monitored by the processor via input functions utilizing interface vector address 121 octal (left bank). The order codes represented by this byte are described in Section 4.2 of Reference 2.1.

4.4 SIO, TIO, HIO STATUS--INTERFACE VECTOR 122_8

The status byte returned to the IOP or SIO, TIO, or HIO instructions is described in Table 4-2. The byte is not controlled directly by the processor but may be monitored by input functions utilizing interface vector address 122 octal (left bank). The bits of the byte are generated by condition signals returned from the selected device during the execution of the instruction by the IOP and by state signals from the 7902 (i.e., bits 0, 4, 5, 6) and IFX.

4.5 TDV STATUS BYTE--INTERFACE VECTOR 123_8

The TDV status byte function consists of a register which may be loaded and monitored by the processor via input/output functions utilizing interface vector address 123 octal (left bank). The register outputs supply the TDV status byte described in Section 4.4.2 of Reference 2.1. Bit significance of the status byte for the T3281 controller is shown in Table 4-3. The TDV byte will reflect controller status that was a result of the last order executed by the controller. The byte is cleared on acceptance of an SIO, by an HIO or I/O RESET.

4.6 AIO STATUS BYTE--INTERFACE VECTOR 124_8

The AIO status byte function consists of a register which may be loaded and monitored by the processor via input/output functions utilizing interface vector address 124 octal (left bank). AIO status will be posted by the processor prior to issuing a device interrupt call CIL (see 4.13). Bit 0 reflects conditions that were a result of the last order and will be set up prior to issuing an order-in call (see 4.7) at the termination of the order. Bit significance of the AIO status byte is shown in Table 4-4. The byte is cleared on acceptance of an SIO, by an HIO, AIO or I/O RESET.

The various interrupts initiated by either the IOP or the controller (device interrupts) are described in Section 4.5.2 of Reference 2.1.

4.7 OPERATIONAL STATUS BYTE--INTERFACE VECTOR 125_8

The IFX will issue an order-in service call and generate an operational status byte which is returned to the IOP during an order-in service connection to depict the conditions at the termination of the order operation. The processor will set four bits of this status via an output function with interface vector address 125 octal (left bank). The bit significance of this data is:

BIT POSITION	FUNCTION	VALUE	MEANING
0	Interrupt Pending	1	Set if interrupt is pending (issued, but not acknowledged by an AIO instruction.
1,2	Device Condition		Describes the current device condition as follows:
		00	Device "ready".
		01	Device "not operational".
		10	Device "unavailable" (reserved by other controller).
		11	Device "busy".
3	Mode	1	Always set to automatic mode.
4	Unusual End	1	Set if previous controller operation terminated with "unusual end".
5,6	Controller Condition		Describes the current controller condition as follows:
		00	Controller "ready".
		01	Controller "not operational".
		10	Not applicable.
		11	Controller "busy".
7	Processor Busy	1	Processor is busy with device interface executing some function not initiated by the CPU i.e., in-like diagnostic, disk backup on tape, etc.

Table 4-2. Device Status Byte for SIO, TIO and HIO Instructions

SIZE	CODE IDENT NO.	SPEC. NO.
A	51360	SS-600-0058-1A
SCALE	REV.	SHEET 17 OF

Bit Position	Function	Value	Meaning
0	Error Corrected	1	Error Correction was successfully applied to data read from disk during block transmission. Data in core is valid.
1	Flaw detection	1	Flaw byte detected during Header Read, Write, Read, or Check-write.
2	Programming error	1	Invalid order detected; illegal address (address X'F' used for orders other than Select Test Mode or Conditional Release Interrupt); invalid Seek address; address incremented out of limits while attempting a Read or Write order; invalid test mode; Seek order received while arm was in motion; first six bits of Seek order were not zero; or incorrect length detected for Seek, Sense, Header Read, or Header Write order.
3	Write protection	1	Write-protect violation.
4	Parity error (IOP)	1	Order parity error detected; Seek address parity error detected; even parity received on a terminal order; or IOP detected on address parity error (channel address parity error).
5	Operational Error	1	Device interface error detected; missing an on-sector signal from device during a multisector Read or Write; missing Read or Write clock, command strobe, or status request acknowledgment from the device; detection of Seek address transfer verification comparison error during Seek, Read, or Write; device unavailable error or "not operational" signal detected from device by the controller; or a Seek error during a Read or Write.
6	Verification	1	Head address verification error detected; sector address verification error detected; or cylinder address verification error detected while reading a header.
7	Header check byte	1	Header check byte error.

Table 4-3. Device Status Byte for TDV Instruction

Bit Position	Function	Value	Meaning
0	Data overrun	1	Data overrun (rate error) has occurred during execution of the previous order.
1	Attention interrupt	1	Attention interrupt acknowledged.
2	Release interrupt	1	Release interrupt acknowledged.
3	Reserved	0	This bit is currently zero; however, it may be used in future enhancements.
4	On-sector interrupt	1	On-sector interrupt acknowledged. Note that either bit 4 or bit 6 can be set; both cannot be set.
5	Reserved	0	This bit is currently zero; however, it may be used in future enhancements.
6	Seek timeout error interrupt	1	Seek timeout error interrupt acknowledged. See note for bit 4. If bit 6 is set, program must issue a Restore Carriage order and retry the previous operation.
7	Power down interrupt	1	Power down interrupt acknowledged.

Table 4-4. Device and Controller Status Byte for AIO Instruction

Bit	Function
0	ORDER-IN CALL. When set, causes the 7902 to issue an order-in service call.
1-2	Unassigned and always zero.
3	COUNT DONE. Sets count done latch in 7902 to enable an order-in service call. Bit will be used to terminate orders in which COUNT DONE is not received from the IOP.
4	INCORRECT LENGTH. An incorrect length condition as described in Section 4.3.4 of Reference 2.1 occurred during the order operation.
5	TRANSMISSION DATA ERROR. A transmission error condition as described in Section 4.3.3 of Reference 2.1 occurred during the order operation. Parity errors detected by the IFX or 7902 during data transmission will cause the bit to be set without processor action.
6	CHANNEL END. Bit will be set on any order-in call in which any of the conditions listed in Section 4.3.1 of Reference 2.1 apply.
7	UNUSUAL END. Bit must be set for any of the conditions listed in Section 4.3.2 of Refenence 2.1. Bit defines an abnormal end to an order operation.

The bits set up by the processor will be combined with other status maintained by the IOP to produce the operational status byte shown in Tables 4-5 and 4-6 of Reference 2.1.

Bit 0, when set by the processor, will cause the 7902 to issue an order-in service call (CSLOI) if the 7902 is not in DATA state (see 4.2). The 7902 will go automatically to order-in state if COUNT DONE or UNUSUAL END (see 4.2) is received on any terminal order from the IOP. Bit 0 will be reset when an order-in service call is issued by the 7902.

4.8 DATA TRANSFER CONTROL

The data transfer control function shown in Figure 4-2 will, once enabled by the processor, provide control of data transfer between the controller DATA BUFFER (Reference 2.4) and the IOP via the 7902 without further involvement of the processor. The function and its control are described in the following paragraphs.

4.8.1 Interface to Data Buffer

The interface between the IFX and the DATA BUFFER consists of a simple handshake system composed of the following signals:

DATA/PARITY--nine bilateral tri-state lines provide transmission of data between the IFX and the DATA BUFFER. Data is gated from the IFX onto these lines only if signal DIR is low at ACK time.

REQ--a signal generated by the data buffer control to request transmission of a data byte. The signal will be enabled only if the ENABLE DATA TRANSFER control bit (4.8.5) has been set by the processor and:

a. the data register is full if data transfer is into the DATA BUFFER;
b. the data register is empty if transfer direction is from the DATA BUFFER.

ACK--a signal generated by the DATA BUFFER to acknowledge the request for data transfer and to:

a. clock data into the register if DIR is true (high);
b. gate the register onto the data lines if DIR is false (low).

DIR--a signal generated by the IFX to indicate direction of data transfer between the IFX and DATA BUFFER. The signal is controlled by the processor and determines the direction of data transfer per:

DIR = 1: data is transferred from the DATA BUFFER to the IFX;
DIR = 0: data is transferred from the IFX to the DATA BUFFER.

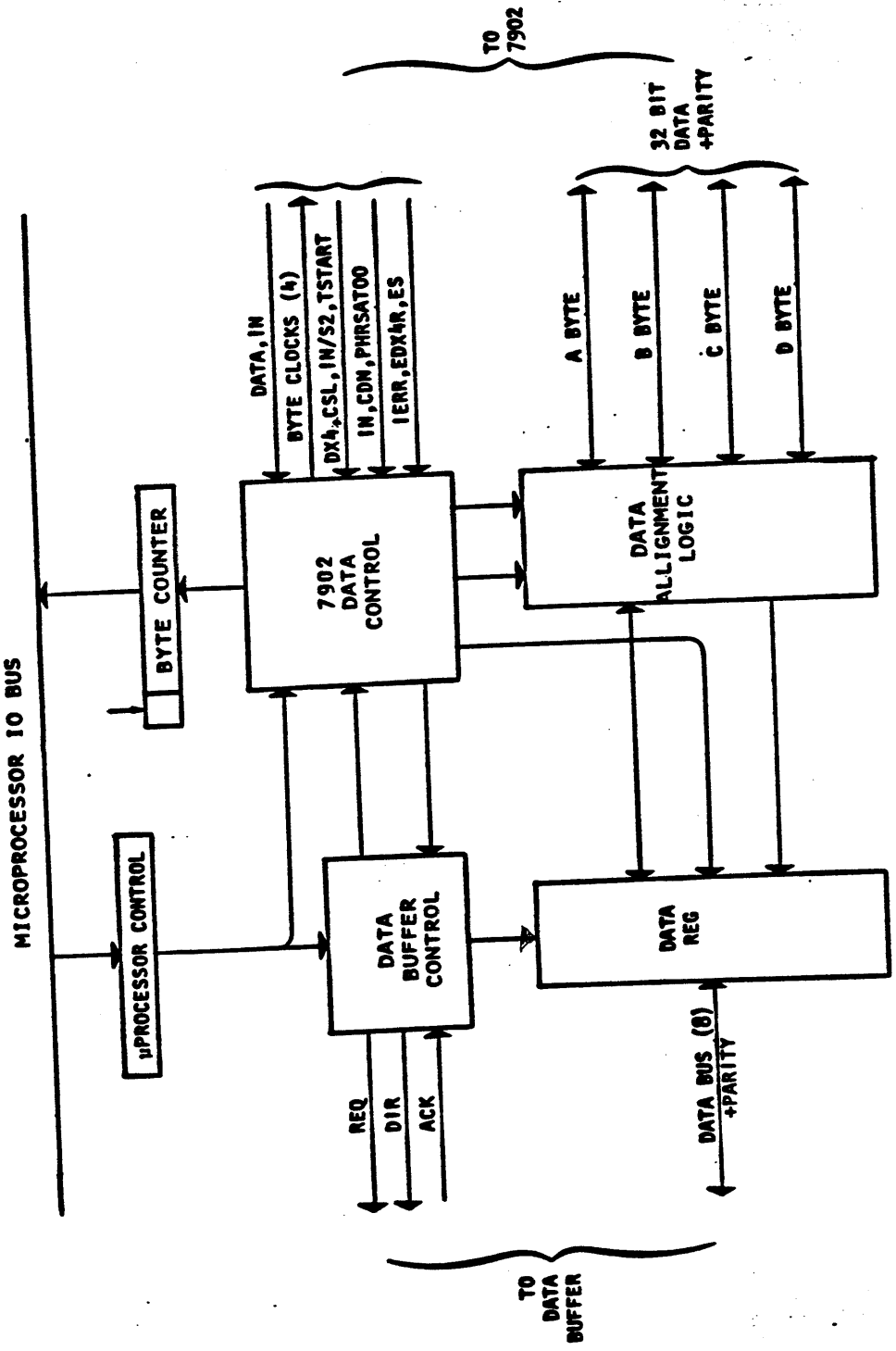

Figure 4-2. Data Transfer Control

SIZE	CODE IDENT NO.	SPEC. NO.
A	51360	SS-600-0058-1A
SCALE	REV.	SHEET 22 OF

Parity generation and checking will be provided on the data transmitted between the IFX and DATA BUFFER. Any parity error will set a latch which may be monitored by the processor (see 4.2) and will be reported to the IOP as a transmission data error (see 4.7).

4.8.2 Data Alignment Logic

The data alignment logic provides alignment control of the data transmitted between the data register in the IFX and the four byte register in the 7902. Control of the logic is based on width of the service connection (one byte/four byte) and content of the IFX data register at start of set up or processing of data for a service connection.

For single byte wide service connections, all data will be transmitted between the IFX and 7902 on the A byte data path.

Four four-byte wide service connections data will be assembled in the IFX data register for transmission to the 7902 or will be held in the register for disassembly and transmission to the DATA BUFFER. This permits overlapping of word assembly/disassembly and IOP service connections.

4.8.3 7902 Data Control

The 7902 DATA CONTROL function provides control for:

a. initiation of data service calls;
b. set-up of data in the 7902 registers prior to the service call or during a service connection if the direction is in to the IOP;
c. processing of the data received during a service connection if the direction is from the IOP.

The function monitors signals IERR and EDX4R from the IOP on any service connection to determine if the next data service connection may be one byte or four bytes wide (IERR=0, EDX4R=1). It drives signal CSLDATA to the 7902 to request a data service connection and DX4D to request a four byte wide service connection. The data control function monitors signals:

a. ED to determine end of data on any service connection;
b. ES to determine end of service connection;
c. CDN (count done) to determine end of transmission for the present order.

It provides control of the data alignment logic (see 4.8.2), four clocks to strobe the data register contents into the proper byte(s) of the 7902 register when transmission is into the IOP, and two clocks to strobe data into the proper byte of the data register when transmission is from the IOP.

Processor control of this function is described in Section 4.8.5.

4.8.4 Byte Counter--Interface Vector 126_8 and 127_8

The byte counter consists of an eleven (11) bit counter which may be cleared by the processor (see 4.8.5) and is incremented on each byte transfer between the 7902 and IFX. The counter may be read by the processor via input functions utilizing interface vector addresses 126 and 127 octal (left bank). The counter contents will be used in determining the INCORRECT LENGTH status returned to the IOP during an order-in service connection (see 4.7). Format of the counter contents is:

IV 112_8: least significant eight bits of the counter

IV 113_8: Bit 0 - NO DATA TRANSMITTED. This bit is set when the counter is cleared (see 4.8.5) and is reset if any byte transmission occurs.

Bit 1 - MORE THAN 1024. This bit, when set, indicates that the data transferred between the 7902 and IFX has exceeded 1024 bytes. The bit will remain set until cleared by the processor (4.8.5).

Bit 2→5 - Zero

Bit 6,7 - Most significant two bits of the counter.

4.8.5 Processor Data Control--Interface Vector 130_8

This function provides processor control for enabling and establishing the mode of data transfer. It consists of a register which may be loaded and read by the processor utilizing input/output functions with interface vector address 130 octal (left bank). The bit significance of the register content is:

Bit	Meaning
0	INHIBIT FOUR BYTE TRANSFERS. When bit is set, all data transfers between the IOP and controller will occur on the one byte data path.
1	SELECT PROCESSOR INPUT. When bit is set, the interface between the data register and DATA BUFFER (see 4.8.1) is inhibited and input to the data register from the processor data bus is enabled.
2	IN (DIR). Controls the direction of data transfer between the IOP and controller. Supplies signal DIR to the DATA BUFFER and signal DIR to the DATA BUFFER and signal IN/S2 to the 7902. Bit is true for transfer to the IOP (in), false for transfer from the IOP (out).

1 = IN
0 = OUT

Bit	Meaning
3	RESET BYTE COUNTER. The bit, when true, produces a single pulse which resets the byte counter (see 4.8.4).
4	ENABLE DATA TRANSFER. When the bit is set, data transfer may occur between the controller and the IOP (see 4.8.1 and 4.8.3).
5	RESET ORDER RECEIVED. When true, the bit produces a single pulse which resets the ORDER RECEIVED status flat (see 4.2).
6	FORCE IOP INPUT PARITY ERROR. When the bit is set, a zero is forced on the parity line to the IOP. Used only when executing test mode orders (Reference 2.1, Section 4.2.1.13).
7	FORCE IOP OUTPUT PARITY ERROR. When the bit is set, a one is forced on the parity line from the IOP. Used only when executing test mode orders (Reference 2.1, Section 4.2.1.13).

4.9 MODIFIER BIT STORE

The MODIFIER BIT STORE provides a storage function for the device interrupt enabling bits contained in SEEK or RESTORE CARRIAGE orders. These bits are the most significant bits of the order byte (M) as described in Section 4.2.1 of Reference 2.1.

The store contains sixteen locations, one for each of the devices which may be attached to the controller. The contents of the store will be set during the execution of the SEEK or RESTORE CARRIAGE order by the processor. The location in the store is determined by the device logical address that is latched into the IFX by the SIO that initiated the order or order chain (see 4.15). The processor will set the device bit via the SET MODIFIER BIT command (see 4.12.1).

The modifier bit is utilized by the processor in initiating an on-sector or seek timeout error interrupt (see 4.6 and Table 4-4). These interrupts may only be initiated by the processor if the modifier bit for the device is set. The modifier bit is reset by:

a. an HIO instruction. Only the specific bit for the addressed device is reset.

b. an HIO instruction in response to a device on-sector or seek timeout error interrupt (see 4.6). Only the bit corresponding to the device for which the interrupt was issued will be reset.

c. an I/O RESET. All modifier bits will be reset.

d. a RESET MODIFIER BIT or RESET ALL MODIFIER BITS command issued by the processor (see 4.12.2). These commands will not normally be utilized and are included only for hardware diagnostic purposes.

4.9.1 Modifier Bit Store Data--IV Addresses 131_8 and 132_8

The contents of the MODIFIER BIT STORE may be monitored by the processor via input functions utilizing interface vector addresses 131 and 132 octal (left bank). The processor will utilize the data for bytes 10 and 11 of the data returned to the IOP during execution of a SENSE order (see Section 4.2.1.12 of Reference 2.1). Device address/bit position correspondence will be:

DEVICE ADDRESS (HEX)

Bit	IV-131	IV-132
0	0	8
1	1	9
2	2	A
3	3	B
4	4	C
5	5	D
6	6	E
7	7	N/A

4.10 RELEASE MARK STORE

The RELEASE MARK STORE provides storage on a device basis for a bit which enables the device "release interrupt" to occur. This interrupt is pertinent only to multiple access systems and is described in Section 4.5.2.3 of Reference 2.1. Release interrupts are enabled only when the release interrupt mark control is set. This control is set by a SET RELEASE INTERRUPT CONTROL command (see 4.13.2) issued by the processor during the execution of a CONDITION RELEASE INTERRUPT order. The order is described in Section 4.2.1 of Reference 2.1. The release mark control will be set if the M bit of the order code = 1. If M = 0, the processor will issue a RESET RELEASE INTERRUPT CONTROL command (see 4.13.2) to clear the release mark control and disable any release interrupts.

The processor will scan the devices and if a device has a "release" signal set will:

a. set the device bit in the RELEASE MARK STORE via a SET RELEASE MARK command (see 4.12.1). The device bit is addressed by the logical address established by the processor (see 4.12.1) during the scan.

b. reset the release signal from the device.

c. set bit 2 of AIO status (see 4.6) the logical address of the device in the interrupt control (see 4.13) and issue an interrupt call CIL if no interrupt call is set and controller is not busy.

If a TIO, TDV, HIO or SIO instruction is issued to a device other than the one causing the release interrupt, the interrupt will be removed but will be raised later by the processor in scanning the devices and RELEASE MARK STORE contents.

4.11 ATTENTION STORE

The ATTENTION STORE provides storage on a device basis for the ATTENTION bit from the device. This bit indicates that:

a. a head movement has completed or timed out, or

b. some manual operation has occurred at the device i.e., power up, pack change, etc.

The processor will scan the devices and when it finds an ATTENTION signal will:

a. set the corresponding device bit in the ATTENTION STORE by issuing a SET ATTENTION command as described in 4.12 and,

b. reset the ATTENTION signal from the device.

When the controller is not busy, the processor will scan the MODIFIER, RELEASE MARK and ATTENTION stores in order to determine the necessity of a device interrupt call as described in 4.13.

The bits of the ATTENTION STORE, when set, will indicate that either an attention interrupt or an on-sector interrupt is required. An attention interrupt is indicated if the corresponding bit of the MODIFIER BIT STORE (see 4.9) is not set.

The bits of the ATTENTION STORE may be set or reset by the processor as described in 4.12, and may be reset by an HIO, AIO in response to an attention or on-sector device interrupt, or by an IO RESET. The AIO or HIO clear only a single bit; IO RESET clears all bits.

4.12 BIT STORE CONTROL

The processor may set or reset the bits in the MODIFIER, RELEASE MARK, and ATTENTION bit stores by utilizing the interface vector functions described below.

4.12.1 Set Bit--IV Address 133_8

An output function utilizing interface vector address 133 octal (left bank) will be utilized to set bits in the stores. Bit significance of the byte is described in the following:

Bit	Function
0	Unassigned and always zero.
1	SET RELEASE MARK. This bit, when true, will cause the bit in the RELEASE MARK STORE (see 4.10) specified by bits 4 through 7 to be set.
2	SET ATTENTION. This bit, when true, will cause the bit in the ATTENTION STORE (see 4.11) specified by bits 4 through 7 to be set.
3	SET MODIFIER BIT. This bit, when true, will cause the bit in the MODIFIER BIT STORE (see 4.9) specified by bits 4 through 7 to be set.
4→7	DEVICE ADDRESS. These bits define the logical device addresses, 0 through E, hexadecimal, used by the IOP to address the disk drives. Each store contains one location for each device.

4.12.2 Reset Bit--IV Address 134_8

An output function utilizing interface vector address 134 octal (left bank) will be used to reset bits in the stores. Bit significance of the byte is described in the following:

Bit	Function
0	RESET ALL BITS. This bit, if true, enables resetting of all bits of any bit store having its control bit 1 through 3 set.
1	RESET RELEASE MARK. Enables resetting of the bit in the RELEASE MARK STORE (see 4.10) specified by bits 4 through 7. If bit 0 is true, bit 1 will cause all bits to be reset.
2	RESET ATTENTION. Enables resetting of the bit in the ATTENTION STORE (see 4.11) defined by bits 4 through 7. If bit 0 is true, bit 2 will cause all bits of the ATTENTION STORE to be reset.
3	RESET MODIFIER BIT. Enables resetting of the bit in the MODIFIER BIT STORE (see 4.9) specified by bits 4 through 7. If bit 0 is true, bit 3 will cause all bits of the MODIFIER BIT STORE to be reset.
4→7	DEVICE ADDRESS. These bits define device logical address and bit store location as defined in 4.12.1.

The bit stores are also reset by HIO or AIO instructions or by IO RESET as described in 4.9 through 4.11.

4.13 INTERRUPT CONTROL

The T3281 controller may, when not busy, raise device interrupts if conditions require. These interrupts are described in Section 4.5.2 of Reference 2.1, and depicted in the AIO status byte described in Section 4.6 of this document. The processor will:

a. scan the contents of the bit stores described in Sections 4.9 through 4.11 to determine if a device interrupt is required;

b. select the device and monitor other status if necessary to determine the interrupt type;

c. set up the proper AIO status bit as described in 4.6, Table 4-4;

d. set up the device interrupt address and issue the interrupt call.

4.13.1 Bit Store Scan

The processor will scan the contents of the bit stores described in Section 4.9 through 4.11 by:

a. establishing the bit store device address via an output IV-133_8 or 134_8 as described in 4.12 with bits 0 through 3 set to zero;

b. monitoring the bit store contents via an input function utilizing interface vector address 135 octal (left bank). The format of the data returned is:

Bit	Function
0→4	Zero
5	RELEASE MARK
6	ATTENTION
7	MODIFIER

Bits 5 through 7 define the type of device interrupt to be posted by the processor as per:

5	6	7	Interrupt Type
X	1	0	Attention
X	1	1	On sector or seek time-out error. The device must be interrogated to determine if a seek time-out has occurred. If not, the rotational position counter for the device (Reference 2.3) must be interrogated prior to raising the interrupt.
1	0	X	Release Interrupt.

4.13.2 Interrupt Call--IV Address 136_8

The processor, after determining the type of device interrupt as described in 4.13.1 must set-up the appropriate AIO status (see 4.6), set up the device address for the interrupt and issue an interrupt call. The interrupt call and device address are established via an output function utilizing interface vector address 136 octal (left bank). The bit format of the byte is:

Bit	Function
0	INTERRUPT CALL. This bit, when true, will set the interrupt call latch CIL in the 7902. This bit will be reset when CIL is set.
1	ON-SECTOR RESET ENABLE. This bit, when true, will enable the trailing edge of the on-sector window to reset the on-sector interrupt call if bit 4 of AIO status (see 4.6) is set. Device is defined by bits 3 through 7.
2	Zero
3	CONTROLLER ADDRESS LSB. Defines the least significant bit of the controller address if the 7902 is operating in dual address mode (see 4.15). Bit will be zero otherwise.
4→7	DEVICE ADDRESS. These bits define the logical address of the device for which the device interrupt was initiated. The address will be returned to the IOP by an AIO if bits 1, 2, 4 or 6 of the AIO status (see 4.6) is set.

An SIO, TIO, HIO or TDV instruction addressing a device other than that defined by bits 4 through 7 will cause the device interrupt to be reset. The interrupt will be raised again by the processor if the bit stores are not reset.

4.14 INTERRUPT AND OTHER CONTROL--IV ADDRESS 137_8

The processor will utilize interface address vector 137 octal (left bank) to provide setting and resetting of the RELEASE INTERRUPT CONTROL and other control functions. The format of the byte is described in the following.

Bit	Meaning
0-5	Unassigned
6	SET RELEASE INTERRUPT CONTROL This bit will be used during execution of a CONDITION RELEASE INTERRUPT order to enable release interrupts and the RELEASE MARK STORE described in 4.10.
7	RESET RELEASE INTERRUPT CONTROL. This bit will be used during the execution of a CONDITION RELEASE INTERRUPT order to inhibit release interrupts and clear the RELEASE MARK STORE described in 4.10. The control is also reset by an HIO instruction with device address X'F' or an IO RESET.

4.15 DEVICE LOGICAL ADDRESS--IV ADDRESS 140_8

The DEVICE LOGICAL ADDRESS function shown in Figure 4-1 stores the device address contained in SIO, HIO, TIO and TDV instructions. The address is used to determine device selection by supplying inputs to the address translator (Reference 2.3) which selects the physical drive corresponding to the logical device address. The device address established by the I/O commands may be monitored by the processor via input functions utilizing interface vector address 140 octal (left bank). The format of the byte returned is:

Bit	Function
0	DUAL ADDRESS MODE. Set by a switch on the IFX to indicate 7902 can recognize two controller addresses.
1	DISK CONTROLLER LSB. Set by a switch on the IFX to indicate the state of bit 3 which applies to the disk controller. Determines which address selects the disk drives on I/O commands.
2	Zero
3	CONTROLLER ADDRESS LSB. The least significant bit of the controller address received in the I/O command.
4-7	DEVICE ADDRESS. The logical device address received in the I/O command.

The 7902 can be operated in a mode that allows acceptance of two controller addresses differing only in the least significant bit (3).

4.16 DEVICE ADDRESS MPX

The DEVICE ADDRESS MPX provides the device address returned to the IOP during service connections or AIO commands. The outputs of the multiplexer will reflect the DEVICE LOGICAL ADDRESS (see 4.15) for service connections or AIO commands for channel end interrupts initiated by the IOP. It will reflect the device address established by the processor (see 4.13.2) for AIO commands in response to a device interrupt (see 4.13).

4.17 7902 OFFLINE CONTROL--IV ADDRESS 141_8

The processor will have the capability of switching the 7902 interface on-line or off-line from the IOP. Interface vector address 141 octal (left bank) will supply this function. Bit 7 of the byte will cause the 7902 to be on-line if true, off-line if false. At power turn on, the 7902 will be off-line. The processor will set the 7902 on-line only after the initial program load is completed and initial device scans are completed for establishing device address and status.

4.18 TEST CONTROL

The TEST CONTROL function of the IFX/7902 module, when the 7902 modules are off-line from the IOP, provides:

a. control of the 7902 modules by the processor for simulation of IOP signals. This function can be used in stand alone hardware diagnostics in order to verify the basic functionality of the IOP interface without involving any disk drives or the IOP.

b. provide a control path for a test panel or device to simulate function of the IOP in order to test or troubleshoot the controller and devices functionally.

The test control functions are described in the following.

4.18.1 Test Data--IV Address 142_8 through 152_8

The processor will simulate data from the IOP via an output function utilizing interface vector addresses 142 through 152 octal (left bank) to load a register which supplies the test data byte TD0 through TD7 to the 7902. The register will simulate:

a. device address for I/O instructions (SIO, HIO, etc.);
b. data from the IOP during data-out service connections;
c. order byte from the IOP during order-out service connections;
d. terminal order from the IOP. For this function, the bit significance of the byte is:

Bit	Meaning
0	INTERRUPT
1	COUNT DONE
2	COMMAND CHAIN
3	UNUSUAL END (IOP HALT)
4→7	Zeros

The interface vector addresses represent the four byte wide IOP data interface as follows:

IV 142_8 -- A byte
IV 143_8 -- B byte
IV 144_8 -- C byte
IV 145_8 -- D byte
IV 146_8 -- All bytes (A,B,C,D)

Device addresses for I/O instructions, order codes, and terminal orders will always be transmitted on the A byte. All data bytes for one byte wide data-out service connections will be transmitted via the A byte. The other IV addresses will be used only in setting up data for simulation of four byte wide data-out service connections.

4.18.2 Test Control--IV Addresses 147_8 through 152_8

The TEST CONTROL function consists of registers which may be loaded or read by the processor via interface vector addresses 147 through 152 octal (left bank). These registers provide the processor with the capability of simulating IOP control functions. The bit significance of the registers are described in the following:

4.18.2.1 I/O Function--IV Address 147_8

Interface vector address 147 octal (left bank) will be used by the processor to simulate IOP functions. Bit significance of the byte is:

Bit	Function
0	SIO. Start I/O instruction indicator
1	HIO. Halt I/O instruction indicator
2	AIO. Acknowledge interrupt
3	FS. Function Strobe
4	ASC. Acknowledge Service Call
5	TIO. Test IO instruction indicator
6	TDV. Test Device instruction indicator
7	IORST. IO RESET

Functions and timing of these signals are defined in Reference 2,6.

4.18.2.2 IOP Timing--IV Address 150_8

Interface vector address 150 octal (left bank) will provide processor simulation of IOP signals for service connections and single phase step control of the 7902. Bit significance of the byte is:

Bit	Function
0	EDX4. IOP has four byte wide data interface.
1	EDX2. IOP has two byte wide data interface.
2	STEP. Allows 7902 to operate in single phase step mode.
3	PHASE CLOCK. If bit 2 is true, produces single pulse which will advance 7902 timing by one phase.
4	IERR. Inhibit extended interface.
5	ES. End Service.
6	ED. End Data.
7	RSA. Request Strobe Acknowledge

Function and timing of these signals, except bits 2 and 3, are described in Reference 2.6.

4.18.2.3 7902/IOP Control--IV Address 151_8

Interface vector address 151 octal (left bank) will be used by the processor during testing to monitor signals that are transmitted from the 7902 to the IOP to call for service connections or interrupts, request data handshakes or respond to I/O commands. The bit significance of the byte is:

Bit	Function
0	FSL. Function Strobe Acknowledge
1	CC1 (DOR). Condition Code bit 1
2	CC2 (IOR). Condition code bit 2
3	CCH. Command Chain
4	CIL. Interrupt Call
5	CSL. Service Call
6	DX4. Four byte wide service request
7	RS. Request Strobe.

Function and timing of these signals are defined in Reference 2.6.

4.18.2.4 Function Response Lines--IV Address 152_8

Interface vector address 152 octal (left bank) will be used by the processor to monitor the function response lines FR0 through FR7. These lines represent:

a. status byte shown in Table 4-2 for SIO, HIO or TIO instructions (see 4.4);

b. status byte shown in Table 4-3 for TDV instructions (see 4.5);

c. controller and device address during time a service call is acknowledged or in response to an AIO instruction. Byte format is:

Bits 0↔3: controller address
Bits 4↔7: device address

4.18.3 Test Panel Interface

The TEST CONTROL function provides an interface for an external control panel which can be used to simulate the IOP to a certain extent and will allow controller functional programs to run i.e., the controller will function as described in Reference 2.1. The panel will be used to input chains of orders and control data in order to check the functional microcode off-line from the IOP. When the 7902 is off-line, the panel interface is enabled by setting a switch on the back edge of the IFX card. This will disable the processor test interface described in 4.18.1 and 4.18.2.

The panel interface, shown in Figure 4-3, is composed of an eight bit data bus, three function code lines, a strobe line, and eight status lines returned from the IFX. The interface will function much as the processor interface described in 4.18.1 and 4.18.2. The contents of the eight data lines will be routed to the registers described in 4.18.1 and 4.18.2 determined by the state of the function code lines. The strobe will provide a clock function to strobe the data lines into the registers. The function code to register correspondence is:

Function

4	2	1	Register
0	0	0	A byte
0	0	1	B byte
0	1	0	C byte
0	1	1	D byte
1	0	0	All bytes (A,B,C,D)
1	0	1	IO FUNCTION as described in 4.18.2.1
1	1	0	IOP TIMING as described in 4.18.2.2
1	1	1	-

The eight status lines monitored by the control panel consist of the 7902/IOP CONTROL byte described in 4.18.2.3. These lines will allow the panel to respond to service and interrupt calls and accomplish data handshakes.

5.0 TEST FEATURES

LED's on the back edge of the IFX/7902 module will provide display of order and status bytes and 7902 control and timing functions. Display will include:

a. IFX status byte (4.2)
b. Order byte (4.3)
c. SIO, TIO, HIO status (4.4)
d. TDV status (4.5)
e. AIO status (4.6)
f. Operational status (4.7)
g. Device interrupt address (4.13.2)
h. Device logical address (4.15)
i. 7902/IOP functions described in 4.18
j. Parity error indicator

6.0 CIRCUIT REQUIREMENTS

The IFX/7902 module will be implemented with readily available TTL SSI, MSI and CSI commercial temperature range dual in-line integrated circuits. High speed Schottky logic will be used where required by system timing.

7.0 PHYSICAL

The IFX/7902 is packaged on a single circuit card whose dimensions are 11.75 by 15.4 inches. The rear edge of the card will contain LED displays and control switches.

8.0 POWER REQUIREMENTS

The IFX/7902 requires only +5VDC provided by the card will be 4 amps maximum.

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