TEXAS INSTRUMENTS

Improving Man's Effectiveness Through Electronics

Model 960/980 Computers

Direct Memory Access Channel Manual

MANUAL NO. 966312-9701
ORIGINAL ISSUE 15 AUGUST 1972
REVISED AND REISSUED 15 JULY 1974
INCLUDES
CHANGE 1 . . . . . 1 AUGUST 1977

Digital Systems Division

LIST OF EFFECTIVE PAGES

INSERT LATEST CHANGED PAGES DESTROY SUPERSEDED PAGES

Note: The portion of the text affected by the changes is indicated by a vertical bar in the outer margins of the page.

Model 960/980 Computers Direct Memory Access Channel Manual (966312-9701)

Original Issue	15 August 1972
Revised	15 February 1973
Revised and Reissued	15 July 1974 (ECN 393104)
Change 1	1 August 1977 (ECN 419558)

Total number of pages in this publication is 60 consisting of the following:

PAGE NO.	CHANGE NO.	PAGE NO.	CHANGE NO.	PAGE NO.	CHANGE NO.
Cover	1	2-11 - 2-13	0		
Eff. Pages	1	2-14 blank	0		
iii - v	0	3-1 - 3-9	0		
vi blank	0	3-10 blank	0		
1-1 - 1-6	0	4-1 - 4-14	0		
2-1 - 2-2	0	5-1 - 5-4	0		
2-3	1	User's Resp	1		
2-4 blank	0	Bus. Reply	0		
2-5 - 2-9	1	Cover Blank	0		
2-10 blank	0	Cover	0		

TABLE OF CONTENTS

Paragraph	Title	Page
	SECTION I. INTRODUCTION	
1.1	Scope of Manual	1-1
1.2	Functional Description	1-1
1.2.1	Controller Operation	1-1
1.2.2	Logic Signal Levels	1-2
1.3	Software Interface	1-2
1.3.1	Activate Word 1	1-2
1.3.2	Activate Word 2	1-3
1.3.3	List Words 1 Through 4	1-3
1.4	Interrupts and Status	1-4
1.4.1	General	1-4
1.4.2	Interrupt and Status Storage Sequence	1-4
	SECTION II. INTERFACE	
2.1	General	2-1
2.2	Interface Signals	2-1
2.2.1	Interface Signal Loading and Termination	2-1
	SECTION III. SIGNALS	
3.1	General	3-1
3.1.1	Timing	3-1
3.1.2	Logic Levels	3-1
3.2	Master Reset	3-1
3.3	Memory Power Reset	3-1
3.4	System Clock	3-3
3.5	Parity Error	3-3
3.6	Active Word Strobes	3-5
3.7	Memory Read Data Available	3-5
3.8	Memory Fetch and Store Initiate	3-5
3.9	Memory Access Request	3-6
3.10	Memory Access Granted	3-7
3.11	Memory Address	3-7
3.12	Memory Write Data	3-8
3.13	Memory Read Data	3-8
3.14	Interrupt Request	3-8
3.15	Interrupt Recognized	3-9

TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
	SECTION IV. HARDWARE	
4.1	General	4-1
4.2	Expansion Kits	4-1
4.2.1	Internal	4-1
4.2.2	External	4-4
4.3	Expansion Chassis	4-5
4.4	Custom Logic Boards	4-7
4.5	Expansion Kit Interface Requirements	4-11
	SECTION V. DOCUMENTATION	
5.1	Manuals	5-1
5.2	Computer Generated Documentation	5-1
5.2.1	Load List	5-1
5.2.2	Pin List	5-4
5.2.3	LIMP or Documentation List	5-4

LIST OF ILLUSTRATIONS

Figure	Title	Page
2-1	Direct Memory Access Interface Card Assembly Drawing	2-3
2-2	Direct Memory Access Interface Card Logic Drawing	2-9
2-3	Twisted Pair Interface Connections	2-12
2-4	Coax Output Interface Connection	2-13
2-5	Coax Input Interface Connections	2-13
3-1	Direct Memory Access Signal Timing Relationships	3-2
3-2	Master Reset Logic	3-3
3-3	Computer Clock Cycle Variations	3-4
3-4	Memory Read Data Available Logic	3-6
4-1	Internal DMA Expansion Backplane	4-2
4-2	Moving Head Disc Controller CPU Mounting Configuration	4-3
4-3	Fixed Head Disc Controller CPU Mounting Configuration	4-3
4-4	Model 979 Magnetic Tape Controller CPU Mounting Configuration	4-4

LIST OF ILLUSTRATIONS (Continued)

Figure	Title	Page
4-5	External Single Controller Mounting Kit	4-5
4-6	DMA External Expansion Backplane Connectors and Pin Configurations	4-6
4-7	Rack Mounted Input/Output Expansion Chassis	4-8
4-8	Input/Output Power Supply Functional Diagram	4-10
4-9	Single Connector Type 1PC Board Physical Configuration	4-11
4-10	Double Connector Type 1 PC Board, Physical Configuration	4-12
4-11	Double Connector Type 2 PC Board, Physical Configuration	4-13
4-12	Type 2 Top Edge Connector Pin Assignment	4-14
5-1	Direct Memory Access PC Card Locations, Expansion Kit 966555-0002	5-2
5-2	Direct Memory Access PC Card Locations Expansion Kit 966555-0001	5-3

LIST OF TABLES

Table	Title	Page
1-1	Pre-Assigned DMA Status Storage Addresses	1-6
2-1	Direct Memory Access Interface Signals and Locations	2-11
4-1	DMA Internal Expansion Kit Part Numbers	4-2
4-2	Three Basic Types of External DMA Expansion	4-7
4-3	External Expansion Chassis Characteristics	4-9
4-4	Power Supply Characteristics	4-9
4-5	Controller Card Current Loads	4-10
5-1	Direct Access Documentation List	5-1

SECTION I

INTRODUCTION

1.1 SCOPE OF MANUAL

This manual familiarizes the user with the functional operation and interface requirements of the Direct Memory Access Channel (DMAC) of the Texas Instruments (TI) Model 960 and Model 980 series computer systems. The Direct Memory Access (DMA) channel of both computers is identical, and all further reference to computers will pertain to both the 960 and 980 series. This manual describes the following topics:

a. CPU DMA interface

b. Expanded DMA Bus

c. DMA Signals and Interface

d. DMA Hardware

e. DMA Documentation

Information concerning the standard device controllers that are available for both the Model 960 and 980 series computers is included in the "Direct Memory Access Channel Controller" manual for the Model 960/980 series computers (TI Part No. 966312-9702).

1.2 FUNCTIONAL DESCRIPTION

The DMA channel consists of a single bus at the DMA interface card (TI Part No. 966390) of the CPU and an expanded bus at the DMA expander interface. The single bus at the CPU interface has one line each for the memory access and interrupt signals; the expanded bus has eight (8) lines for each of these signals. The expanded DMA bus can handle eight completely autonomous controllers on a priority memory access basis. The DMA bus has a combined maximum memory transfer speed of 1,000,000 words-per-second. This speed can be achieved by one continuous user. When the DMA bus is expanded and access to the DMA bus is switched between controllers, the speed is reduced by 20 percent to 800,000 words-per-second.

1.2.1 CONTROLLER OPERATION

A controller, attached to either section of the DMA bus (single or expanded), acts as a completely autonomous user of the computer memory after being activated. Thus, the following information must be furnished from the controller logic:

a. Memory Access Request

b. Memory Address

c. Memory Write Data

d. Memory Store/Fetch Pulses

The controller must accept the following signals for control and data transfer:

a. Memory Read Data

b. Activate Control

c. Memory Access Granted

After the specified activate command has been issued (ADAC or ATI), the controller can communicate with the CPU by use of interrupt requests acknowledge signals, and/or by storing status into a pre-assigned memory address.

Signal descriptions, signal signatures, and signal usage are discussed in a subsequent section of this manual. Standard and optional hardware can be used to implement a DMA system. This hardware is described in Section V.

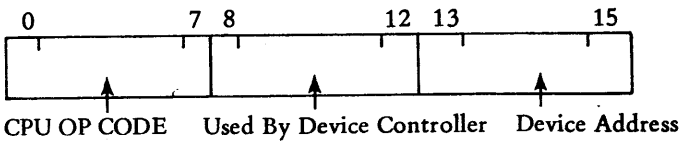
1.2.2 LOGIC SIGNAL LEVELS

All signals at the DMA channel interface are compatible with Texas Instruments Series 54/74 transistor-transistor logic (TTL) circuits. The logic ZERO (low) level is 0.0 to +0.4 Vdc. The logic ONE (high) level is +2.4 to +5.0 Vdc.

1.3 SOFTWARE INTERFACE

An Automatic Transfer Instruction (ATI) in the Model 980 series computers and the Activate Direct Access Channel (ADAC) command in the Model 960 series computers is the software instruction required to activate a DMA device controller. When this instruction is executed by the CPU, the CPU generates two distinct pulses. One pulse strobes each of two instruction words from the memory read data lines to the device controller interface. General use of the two instruction words and additional controller acquired instruction (LIST) words are described in following subparagraphs. When the customer does not use any of the standard device controllers, use of available bits in the activate words is arbitrary. This also applies to those bits assigned to the device address field, because these bits are not used for expander operation.

1.3.1 ACTIVATE WORD 1



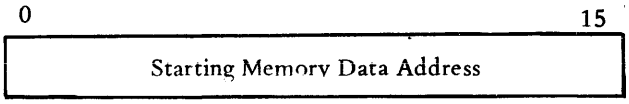
The first activate word is strobed with the DEVATI1 signal on the expander bus or ATISTB1 on the CPU DMA interface. The standard controllers use available bits to indicate the functions noted. Bits 8 through 12 are used by device controllers to indicate such items as device unit number encoded commands for independent functions; i.e., functions which do not acquire additional list words. Bits 13 through 15 are generally assigned as device controller address bits. The device controllers are assigned a distinct binary address of 0 through 7. A device controller accepts an activate word if the assigned address matches the three bit address in the activate word. All standard device controllers have selectable decode logic to permit the controllers to accept one of the eight addresses and automatically select all DMA functions associated with that address including the pre-assigned status address. The implementation of this address selection scheme is described in the "Direct Memory Access Channel Controller Equipment Manual for the Model 960/980 Computer" (TI Part No. 966312-9702).

1.3.2 ACTIVATE WORD 2

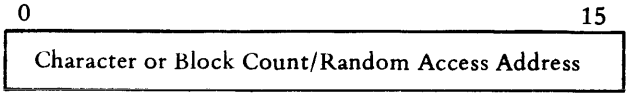
The second word of the DMA activate instruction is strobed by a signal with a like signature, only the suffix of this signature is 2. The second word is used by the standard controllers as a pointer to a memory location where additional instruction or LIST words are stored for the controller. The controller performs the function of extracting these list words from memory. Although the standard controllers utilize the 16 bits of this word for this function, the user may desire to use them as an extension of the control bits in activate word 1. This gives the user a total of 24 bits from the activate command for arbitrary use in system design.

1.3.3 LIST WORDS 1 THROUGH 4.

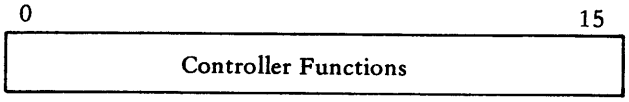
LIST WORD 1.



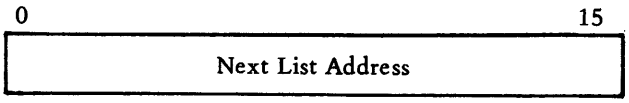
LIST WORD 2.



LIST WORD 3.



LIST WORD 4.



List Words are device controller acquired instruction words that are described in the preceding subparagraph. These additional instruction words are required for the standard DMA device controllers because the 24 bits of the activate words are insufficient for complete control information. Standard device controllers use List Words 1 and 2 as noted.

List Word 3 is generally used to indicate the following:

a. 1 bit for masking interrupts

b. 1 bit to indicate a chaining command

c. Bits to indicate type of command to be performed

d. Additional address bits for random access storage

List Word 4 is normally used for chaining. This word defines the address of the next list to be executed.

1.4 INTERRUPTS AND STATUS

1.4.1 GENERAL

After a device controller is activated, the controller communicates a response to the software via an interrupt and/or a status storage into a preassigned memory location. A response from the device controller may occur at intermediate points in an operation and should always occur when the device controller activity is terminated. Termination may be abnormal or a normal completion.

1.4.2 INTERRUPT AND STATUS STORAGE SEQUENCE

The device controller issues an interrupt request to indicate the controller status needs to be processed by the CPU. The interrupt request from the device controller is registered by the expander and an interrupt request is forwarded to the CPU. The interrupt request to the CPU is the logical sum of the interrupt requests from all device controllers. The expander and each device controller must wait for an interrupt recognition signal before taking further action on an interrupt cycle. However, data transfer may continue until the interrupt is recognized.

In order that interrupt recognition may be received by the DMAC device controller(s), the DMAC interrupt bit in the CPU status register must be armed, and a Store Status Block (SSB) command must be executed. An interrupt request remains active until interrupt recognition is received. When interrupt recognition is received by the expander, a memory access request is generated that has priority over all channel data transfer requests. The expander has the next memory cycle available and uses this memory cycle to store the interrupt word in memory (location 0096_{16}). This interrupt word indicates which device controller(s) have interrupted, by containing a logic ONE in each bit position that corresponds to a channel whose interrupt request has been registered . That is, bit 0 indicates that Channel 0 has interrupted, bit 7 indicates that Channel 7 has interrupted, etc. Bits 8 through 15 are always ZERO.

As the expander stores the interrupt word in memory, the expander also issues an interrupt recognition signal to each device controller whose interrupt request bit was present in the interrupt word. Once a device controller receives interrupt recognition, it issues a normal memory access request and stores the status when memory access is granted through the channel priority scheme.

There is no priority among interrupt request. The expander registers all requests until interrupt recognition is received. However, storage of the interrupt (request) word does have priority over data transfer (memory access) requests.

If interrupts are disabled during list acquisition, a device controller stores status through a normal memory (access request) cycle without issuing an interrupt. Status is stored when a specified operation is completed or when the controller terminates.

Table 1-1 lists the memory locations in both the Model 960 series and Model 980 series computers that are reserved for interrupt and status information storage. Device status is always stored in the even (lower) location of each pair. The odd location of each pair may be used for information pertinent to a device controller at the time of status storage.

Table 1-1. Pre-Assigned DMA Status Storage Addresses

Hexadecimal Location	Use
96	DMAC interrupt word Bits 0 through 7 indicate that the corresponding channel has interrupted. Bits 8 through 15 are always zero.
98, 99	Status, Channel 0
9A, 9B	Status, Channel 1
9C, 9D	Status, Channel 2
9E, 9F	Status, Channel 3
A0, A1	Status, Channel 4
A2, A3	Status, Channel 5
A4, A5	Status, Channel 6
A6, A7	Status, Channel 7

SECTION II
INTERFACE

2.1 GENERAL

The Direct Memory Access (DMA) interface to the Central Processor Unit (CPU) consists of a single DMA channel bus. Logic for the interface is located on a single three-layer printed circuit card (figure 2-1). The logic on this card performs the following functions:

1. Accepts a memory address from the user on the single bus and holds both for use by the memory controller of the CPU.
2. Accepts control signals from the bus, synchronizes same, and passes these signals on to the memory controller of the CPU.
3. Terminates all input lines and drives all memory read data lines with a reverse termination.

A diagram of the logic on the interface card is illustrated in figure 2-2. A table of the interface signals with corresponding pin numbers on the top edge connector of the printed circuit (PC) card are listed in table 2-1. A detailed description of the signals is included in Section IV of this manual.

2.2 INTERFACE SIGNALS

The following interface information is only pertinent to the single DMA bus. Interface information which is common to this bus and the expander DMA bus is included in Section IV of this manual. The signal descriptions are listed by signature as printed on the logic diagram and top edge connector of the PC card. Signals in the attached controller or expander do not necessarily use the same exact nomenclature.

2.2.1 INTERFACE SIGNAL LOADING AND TERMINATION

Memory Read Data signals are reverse terminated with an 82 ohm resistor before being applied to the connector. (See figure 2-3). The receiver of these signals is limited to a maximum of two TTL input loads. Only one load is recommended at the receiver end. This type termination reduces the cross coupling effect of switching currents on the connected cable. A standard TTL input load is defined as a load which requires a maximum of 1.2 ma sink current.

The following signals have the same loading restrictions as the memory read data signals:

DMRESET-

DMPERROR-

ACCGRANT-

INTREC-

Several input signals are terminated through a 470 ohm resistor to Vcc. This termination permits the signal source to be compatible with the expanded DMA bus which is a wire-OR'ed bus. The signatures of these signals are as follows:

DMADR(00-15)

DMD(00-15)

DMAPWRFAIL-

INTREQ-

DMACCR-

The following signals are terminated as illustrated in figure 2-4. These signals must be driven with a gate capable of sinking 30 ma minimum. A type 7438 network is recommended for use as a driver. The open collector driver is compatible with the expanded DMA bus when the following signals are applied to a wired-OR configuration:

DMSTORE-

DMFETCH-

The following signals are driven with a type 7440 power gate and should be terminated as illustrated in figure 2-5.

CK3D1-

ATISTB1-

ATISTB2-

DATAV-

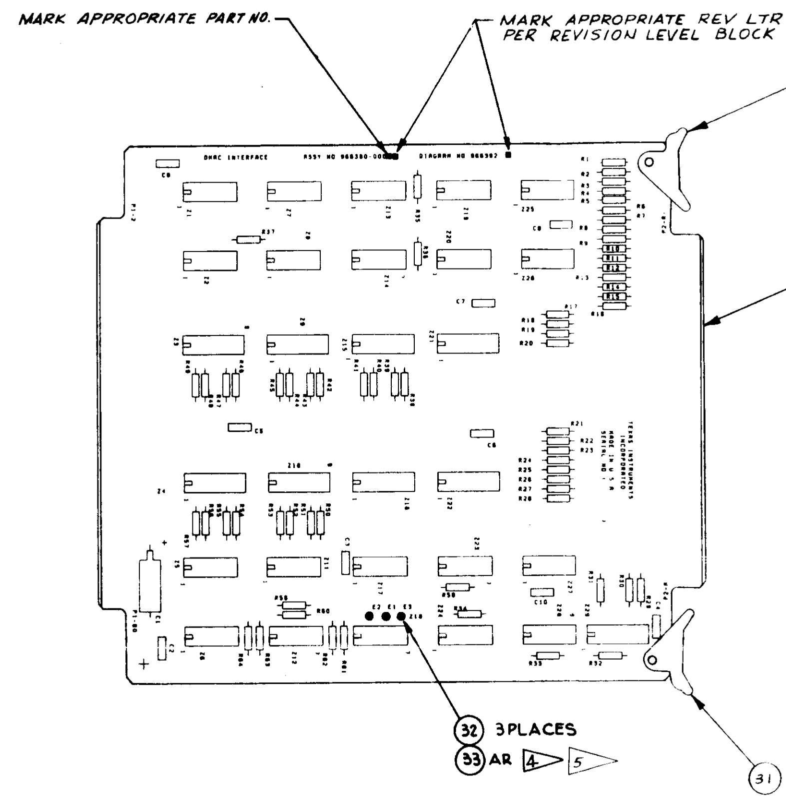
NOTES:

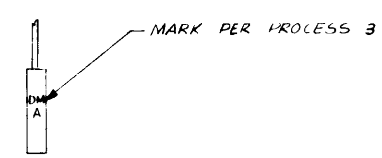
1. MAXIMUM COMPONENT HEIGHT FROM COMPONENT SIDE OF BOARD IS .31
2. MAXIMUM LEAD LENGTH FROM CONDUCTOR SIDE OF BOARD IS .075
3. TO PREVENT SOLDER FROM WICKING DOWN CONNECTOR FINGERS, WHEN SOLDERING, MASK ALL CONNECTOR FINGERS ON BOTH SIDES OF BOARD.

4 INSTALL JUMPER WIRE (ITEM 33) FOR DASH 1 ASSEMBLY

5 JUMPER WIRE (ITEM 33) FOR DASH 2 ASSEMBLY TO BE INSTALLED AT UNIT TEST

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	C	372432 (E) G James 11/10/72 REDRAWN WITH CHG'S SUPERCEDES EXISTING DWG REV B ADDED -0002 & ITEMS 32 & 33	16 Nov 72	
	D	384766 (C) D. Parr (1) NOTE 4 WAS "...(ITEM 33) PER PART NO SCHEDULE" (2) ADDED NOTE 5 AND FLAG 5 TO F/D (3) UPDATED REV LEVEL BLOCK		
	E	392774 (C) R. Garner (1) ADDED 960B & 980B TO -0002 IN TABLE (2) LM: ADDED 960B & 980B TO TITLE OF -0002 (3) UPDATED REV LEVEL BLOCK		
	F	CN 397443 (D) R. De Leon (1) N/A 943851 WAS 943852 (2) N/A 943651 WAS 943652 (3) REVISED REV BLOCK		
	G	CN 383189 (D) T Bailey (1) UPDATED REV LEVEL BLOCK	11/6/75	
	H	CN 411725 (D) (1) IN ALL LIMS ITEM 32 WAS 235789-0005 (2) UPDATED REV LEVEL BLOCK & ADDED TEST PROCEDURE	10-12-76	
	J	CN 417150 (E) R. Pazzini (1) UPDATED REV. LEVEL CONTROL BLOCK	11-24-76	





PART NO.	DESCRIPTION	JUMPER		
966390-0002	DMAC INTERFACE, 980A, 960B, 980B	E1	TO	E3
966390-0001	DMAC INTERFACE, 960A	E1	TO	E2

PROCESSES:

1. RUBBER STAMP F100, HEIGHT .09, COLOR BLK
2. SOLDER PER F124 AND/OR F127
3. HOT STAMP F100, HEIGHT .12, COLOR BLK

REVISION LEVEL									
TEST PROCEDURE 966393-[illegible]									
PRINTED WIRING BOARD FOR -0001, 0002 ASSY 966391-0001	*	A	A	A	A	B	C	D	
LOGIC DIAGRAM FOR -0001, -0002 ASSY 966392-9901	*	A	A	B	B	B	B	B	
ASSEMBLY	B	C	D	E	F	G	H	J	

-2	-1	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION
QTY REQD						

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIR
- DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
- IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
- INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100

HOLE TOLERANCE

.013 THRU .125 +.004 -.001	.126 THRU .250 +.005 -.001	.251 THRU .500 +.006 -.001
.501 THRU .750 +.008 -.001	.751 THRU 1.000 +.010 -.001	1.001 THRU 2.000 +.012 -.001

NEXT ASSY	USED ON
943870	7503
943851	7503
943651	7502
960700	[illegible]
[illegible]	1502
960700	810
226700	8100

APPLICATION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES
  ANGLES ±1°
  3 PLACE DECIMALS ±.010
  2 PLACE DECIMALS ±.02

MATERIAL

DWN [illegible] DATE 9/7/72
CHK [illegible]
ENGR [illegible]
QA [illegible]
APVD [illegible] 11/15/72
CONTR NO
DESIGN ACTIVITY RELEASE [illegible]

TEXAS INSTRUMENTS INCORPORATED Equipment Group Dallas, Texas

DMAC INTERFACE

SIZE D | CODE IDENT NO 96214 | DRAWING NO 966390

SCALE 1/1 | REV F | SHEET 1

32

LM

TI-7914E P3

FILMED

Figure 2-1. Direct Memory Access Interface Card Assembly Drawing

TEXAS INSTRUMENTS
INCORPORATED

DATE 10/05/76

LIST OF MATERIAL

PAGE 1 of

PART NUMBER LM 966390 -0001 REV J

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		966391 -0001	PWB,CMAC INTERFACE	
C002	00001.000	EA		222222 -7400	NETWORK SN7400N	-SN7400N
C002A					Z7	
0003	00001.000	EA		222222 -7401	NETWORK SN7401N	
C003A					Z12	
C004	00001.000	EA		222222 -7404	NETWORK SN7404N	
C004A					Z8	
C005	00004.000	EA		222222 -7408	NETWORK-SN7408N	
C005A					Z19 Z20 Z25 Z26	
C006	00001.000	EA		222222 -7410	NETWORK SN7410N	-SN7410N
C006A					Z28	
C007	00005.000	EA		222222 -7440	NETWORK SN7440N	-SN7440N
C007A					Z2 Z5 Z13 Z14 Z27	
C008	00001.000	EA		222222 -7474	NETWORK SN7474N	-SN7474N
C008A					Z1	
C009	00009.000	EA		222222 -7475	NETWORK-SN7475N	
C009A					Z3 Z4 Z9 Z10 Z15 Z16 Z21	
C009B					Z22 Z29	
C010	00001.000	EA		222222 -7486	NETWORK-SN7486N	
C010A					Z23	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
		J. Robb	10-5-76			DMAC INTERFACE,960A
APPD. MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						8100

PART NUMBER LM 966390 -0001 REV J

T.I. 13849

1/6 FM

TEXAS INSTRUMENTS INCORPORATED

DATE 10/05/7 **LIST OF MATERIAL** PAGE 2 of

PART NUMBER LM 966390 -0001 REV J

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0011	00001.000	EA		240000 -7404	NETWORK SN74H04N	
0011A					Z24	
0012	00001.000	EA		240000 -7410	NETWORK-SN74H10N	
0012A					Z6	
0013	00001.000	EA		240000 -7103	NETWORK SN74H103N	
0013A					Z18	
0014	00002.000	EA		222222 -7180	NETWORK SN74180N	
C014A					Z11 Z17	
C017	00020.000	EA		972946 -0039	RES FIX 82.0 OHMS 5 % .25 W CARBON FILM	ROH- R-25
C017A					R1 THRU R16 R29 R35 R36 R58	
C018	00002.000	EA		972946 -0047	RES FIX 180 OHM 5 % .25 W CARBON FILM	ROH- R-25
C018A					R61 R63	
0019	00002.000	EA		972946 -0051	RES FIX 270 OHM 5 % .25 W CARBON FILM	ROH- R-25
C019A					R62 R64	
0020	00034.000	EA		972946 -0057	RES FIX 470 OHM 5 % .25 W CARBON FILM	ROH- R-25
C020A					R17 THRU R28,R30,R32	
C020B					R38 THRU R57	
C021	00003.000	EA		972946 -0065	RES FIX 1.0K OHM 5 % .25 W CARBON FILM	ROH- R-25
0021A					R33 R59 R60	
C022	00003.000	EA		972946 -0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	ROH- R-25

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						CMAC INTERFACE,960A
APPD.-MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.

PART NUMBER LM 966390 -0001 REV J

T.I. 13849

TEXAS INSTRUMENTS
INCORPORATED

DATE 10/05/7

LIST OF MATERIAL

PART NUMBER LM 966390 -0001 REV J

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0022A					R31 R34 R37	
0025	00008.000	EA		230590 -9000	CAP .05 MF 12 V 20. % CER TRANSCAP	ERI-5635-000-Y5F0503M
C025A					C2 THRU C5	
0026	00001.000	EA		972924 -0011	CAP FIX TANT SOLID 68 MFD 10 % 15 VOLT	QPL-M39003/1-2274
C026A					C1	
0027	00001.000	EA		972929 -0394	CAP FIX CERAMIC 680 PF 10 % 200 V	QPL-M39014/01-1394
C027A					C10	
C028	REF	EA		966392 -9901	DIAGRAM,LOGIC,DET-DMAC INTERFACE	
C029	REF	EA		966393 -9901	TEST PROCEDURE,DMAC INTERFACE	
0030	00001.000	EA		533887 -0001	EJECTOR,PCB,NON-LOCKING,WHITE	SCA-S-202 WHITE
0031	00001.000	EA		533887 -0009	EJECTOR,PCB,NON-LOCKING,GREEN	SCA-S-202 GREEN
0032	00003.000			532258 -0003	TERMINAL,STUD-SINGLE TURRET	CAB- 2100-3
C032A					E1 E2 E3	
0033	AR	FT		411400 -0024	WIRE, 24AWG ELECTRO TIN PLATED COPPER	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						DMAC INTERFACE,960A
APPD.-MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.

PART NUMBER LM 966390 -0001 REV J

T.I. 13849

TEXAS INSTRUMENTS
INCORPORATED

DATE 10/05/7

LIST OF MATERIAL

PAGE 2 of

PART NUMBER LM 966390 -0002 REV J

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
C011	00001.000	EA		240000 -7404	NETWORK SN74H04N	
C011A					Z24	
C012	00001.000	EA		240000 -7410	NETWORK-SN74H10N	
0012A					Z6	
0013	00001.000	EA		240000 -7103	NETWORK SN74H103N	
C013A					Z18	
0014	00002.000	EA		222222 -7180	NETWORK SN74180N	
C014A					Z11 Z17	
0017	00020.000	EA		972946 -0039	RES FIX 82.0 OHMS 5 % .25 W CARBON FILM	ROH- R-25
0017A					R1 THRU R16 R29 R35 R36 R58	
0018	00002.000	EA		972946 -0047	RES FIX 180 OHM 5 % .25 W CARBON FILM	ROH- R-25
C018A					R61 R63	
0019	00002.000	EA		972946 -0051	RES FIX 270 OHM 5 % .25 W CARBON FILM	ROH- R-25
C019A					R62 R64	
0020	00034.000	EA		972946 -0057	RES FIX 470 OHM 5 % .25 W CARBON FILM	ROH- R-25
C020A					R17 THRU R28,R30,R32	
0020B					R38 THRU R57	
0021	00003.000	EA		972946 -0065	RES FIX 1.0K OHM 5 % .25 W CARBON FILM	ROH- R-25
0021A					R33 R59 R60	
0022	00003.000	EA		972946 -0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	ROH- R-25

DRAFTSMAN / DATE	CKD. DRAFTSMAN / DATE	DESIGN ENGINEER / DATE	TITLE
			DMAC INTERFACE 980A 960B 980B
APPD.-MFG. / DATE	APPD. PROJECT ENGINEER / DATE	RELEASED / DATE	PROJECT NO.
			PART NUMBER LM 966390 -0002 REV J

T.I. 13849

TEXAS INSTRUMENTS INCORPORATED

DATE 10/05/7 **LIST OF MATERIAL** PAGE 3 of

PART NUMBER LM 966390 -0002 REV J

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
C022A					R31 R34 R37	
0025	00008.000	EA		23059C -9000	CAP .05 MF 12 V 20. % CER TRANSCAP	ERI-5635-000-Y5F0503M
C025A					C2 THRU C5	.
0026	00001.000	EA		972924 -0011	CAP FIX TANT SOLID 68 MFD 10 % 15 VOLT	QPL-M39003/1-2274
C026A					C1	
0027	00001.000	EA		972925 -0394	CAP FIX CERAMIC 680 PF 10 % 200 V	QPL-M39014/01-1394
C027A					C10	
0028	REF	EA		966392 -9501	DIAGRAM,LOGIC,DET-DMAC INTERFACE	
0029	REF	EA		966393 -9501	TEST PROCEDURE,DMAC INTERFACE	
0030	00001.000	EA		533887 -0001	EJECTOR,PCB,NON-LOCKING,WHITE	SCA-S-202 WHITE
0031	00001.000	EA		533887 -0009	EJECTOR,PCB,NON-LOCKING,GREEN	SCA-S-202 GREEN
0032	00003.000			532258 -0003	TERMINAL,STUD-SINGLE TURRET	CAB- 2100-3
C032A					E1 E2 E3	
0033	AR	FT		411400 -0024	WIRE, 24AWG ELECTRO TIN PLATED COPPER	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						CMAC INTERFACE 980A 960B 980B
APPD.-MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER LM 966390 -0002 REV J

T.I. 13849

TEXAS INSTRUMENTS
INCORPORATED

DATE 10/05/7

LIST OF MATERIAL

PAGE 1 of

PART NUMBER LM 966390 -0002 REV J

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
C001	CC0C1.000	EA		966391 -0001	PWB,CMAC INTERFACE	
C002	000C1.000	EA		222222 -74C0	NETWCRK SN7400N	-SN7400N
C002A					Z7	
C003	CC0C1.CCC	EA		222222 -7401	NETWCRK SN7401N	
C003A					Z12	
C004	000C1.0CC	EA		222222 -7404	NETWCRK SN7404N	
C0C4A					Z8	
C0C5	000C4.000	EA		222222 -7408	NETWORK-SN7408N	
CCC5A					Z19,Z2C,Z25,Z26	
C0C6	00001.000	EA		222222 -7410	NETWCRK SN7410N	-SN7410N
C0C6A					Z28	
0CC7	00005.00C	EA		222222 -7440	NETWCRK SN7440N	-SN7440N
CCC7A					Z2,Z5,Z13,Z14,Z27	
C0C8	00001.000	EA		222222 -7474	NETWCRK SN7474N	-SN7474N
CCC8A					Z1	
C009	C0009.0C0	EA		222222 -7475	NETWCRK-SN7475N	
C0C9A					Z3,Z4,Z9,Z10,Z15,Z16,Z21,	
C0C9B					Z22,Z29	
C010	0C0C1.0C0	EA		222222 -7486	NETWCRK-SN7486N	
C010A					Z23	

DRAFTSMAN DATE	CKD. DRAFTSMAN DATE	DESIGN ENGINEER DATE	TITLE
			CMAC INTERFACE 980A 960B 980B
APPD.-MFG. DATE	APPD. PROJECT ENGINEER DATE	RELEASED DATE	PROJECT NO.
			LM 966390 -0002 J

T.I. 13849

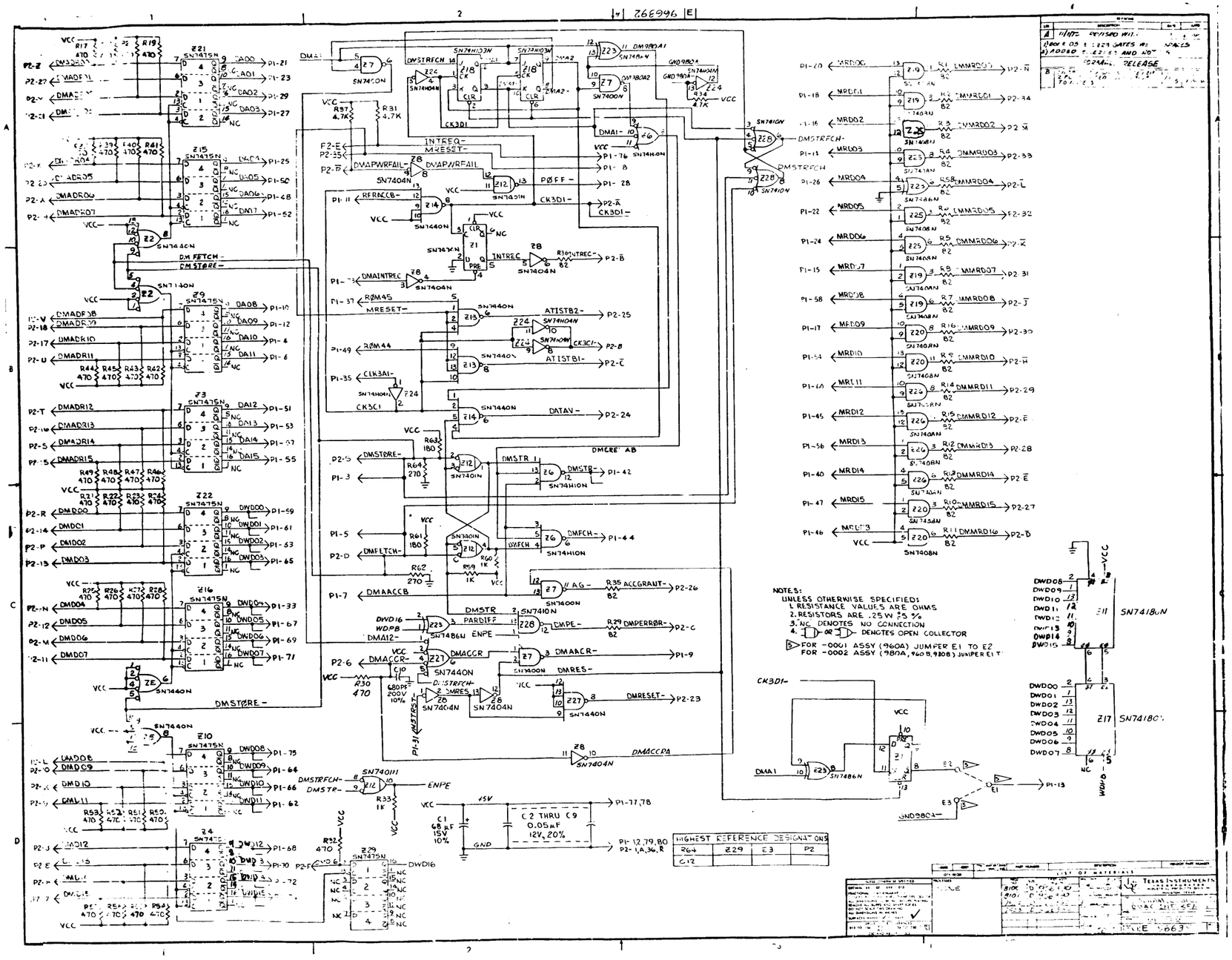


Figure 2-2. Direct Memory Access Interface Card Logic Diagram

Table 2-1. Direct Memory Access Interface Signals and Locations

Signature	P2 Pin No.	Description	Paragraph Reference	Transmission Line Figure Reference
DMADR00	Z	Memory Address Bit (0), Most Significant	2-2.3, 4-11	2-3
DMADR01	22	Memory Address Bit 1	2-2.3, 4-11	2-3
DMADR02	Y	Memory Address Bit 2	2-2.3, 4-11	2-3
DMADR03	21	Memory Address Bit 3	2-2.3, 4-11	2-3
DMADR04	X	Memory Address Bit 4	2-2.3, 4-11	2-3
DMADR05	20	Memory Address Bit 5	2-2.3, 4-11	2-3
DMADR06	W	Memory Address Bit 6	2-2.3, 4-11	2-3
DMADR07	19	Memory Address Bit 7	2-2.3, 4-11	2-3
DMADR08	V	Memory Address Bit 8	2-2.3, 4-11	2-3
DMADR09	18	Memory Address Bit 9	2-2.3, 4-11	2-3
DMADR10	17	Memory Address Bit 10	2-2.3, 4-11	2-3
DMADR11	U	Memory Address Bit 11	2-2.3, 4-11	2-3
DMADR12	T	Memory Address Bit 12	2-2.3, 4-11	2-3
DMADR13	16	Memory Address Bit 13	2-2.3, 4-11	2-3
DMADR14	S	Memory Address Bit 14	2-2.3, 4-11	2-3
DMADR15	15	Memory Address Bit (15), Least Significant	2-2.3, 4-11	2-3
DMD00	R	Memory Write Data Bit (0), Most Significant	2-2.3, 4-12	2-3
DMD01	14	Memory Write Data Bit 1	2-2,3, 4-12	
DMD02	P	Memory Write Data Bit 2	2-2.3, 4-12	
DMD03	13	Memory Write Data Bit 3	2-2.3, 4-12	
DMD04	N	Memory Write Data Bit 4	2-2.3, 4-12	
DMD05	12	Memory Write Data Bit 5	2-2.3, 4-12	
DMD06	M	Memory Write Data Bit 6	2-2.3, 4-12	
DMD07	11	Memory Write Data Bit 7	2-2.3, 4-12	
DMD08	L	Memory Write Data Bit 8	2-2.3, 4-12	
DMD09	10	Memory Write Data Bit 9	2-2.3, 4-12	
DMD10	K	Memory Write Data Bit 10	2-2.3, 4-12	
DMD11	9	Memory Write Data Bit 11	2-2.3, 4-12	
DMD12	J	Memory Write Data Bit 12	2-2.3, 4-12	
DMD13	8	Memory Write Data Bit 13	2-2.3, 4-12	
DMD14	H	Memory Write Data Bit 14	2-2.3, 4-12	
DMD15	7	Memory Write Data Bit (15), Least Significant Bit	2-2.3, 4-12	
DMD16	F	Memory Write Data Bit 16, Parity Bit	2-2.3, 4-12	
DMMRD00	$\overline{N}$	Memory Read Data Bit 0, Most Significant Bit	2-2.1, 4-13	2-3
DMMRD01	34	Memory Read Data Bit 1	2-2.1, 4-13	2-3
DMMRD02	$\overline{M}$	Memory Read Data Bit 2	2-2.1, 4-13	2-3
DMMRD03	33	Memory Read Data Bit 3	2-2.1, 4-13	2-3
DMMRD04	$\overline{L}$	Memory Read Data Bit 4	2-2.1, 4-13	2-3
DMMRD05	32	Memory Read Data Bit 5	2-2.1, 4-13	2-3
DMMRD06	$\overline{K}$	Memory Read Data Bit 6	2-2.1, 4-13	2-3
DMMRD07	31	Memory Read Data Bit 7	2-2.1, 4-13	2-3
DMMRD08	$\overline{J}$	Memory Read Data Bit 8	2-2.1. 4-13	2-3
DMMRD09	30	Memory Read Data Bit 9	2-2.1, 4-13	2-3
DMMRD10	$\overline{H}$	Memory Read Data Bit 10	2-2.1, 4-13	2-3
DMMRD11	29	Memory Read Data Bit 11	2-2.1, 4-13	2-3
DMMRD12	$\overline{F}$	Memory Read Data Bit 12	2-2.1, 4-13	2-3
DMMRD13	28	Memory Read Data Bit 13	2-2.1, 4-13	2-3

Table 2-1. Direct Memory Access Interface Signals and Locations (Continued)

Signature	P2 Pin No.	Description	Paragraph Reference	Transmission Line Figure Reference
DMMRD14	$\overline{E}$	Memory Read Data Bit 14	2-2.1, 4-13	2-3
DMMRD15	27	Memory Read Data Bit 15, Least Significant Bit	2-2.1, 4-13	2-3
DMMRD16	$\overline{D}$	Memory Read Data Bit 16, Parity Bit	2-2.1, 4-13	2-3
DMRESET-	23	Master Reset from CPU	2-2.2, 4-2	2-3
DMPERROR-	C	Memory Write Data Parity Error from CPU	2-2.2, 4-5	2-4
ACCGRANT-	26	Access Granted from CPU	2-2.2, 4-10	2-3
INTREC-	$\overline{B}$	Interrupt Recognized	2-2.1, 4-15	2-3
DATAV-	24	Memory Read Data Available	2-2.2, 4-7	2-4
ATISTB1-	$\overline{C}$	Activate Word No. 1 Strobe	2-2.2, 4-6	2-4
ATISTB2-	25	Activate Word No. 2 Strobe	2-2.2, 4-6	2-4
INTREQ-	$\overline{E}$	Interrupt Request from Controller	2-2.4, 4-14	2-4
DMSTORE-	5	Memory Store Cycle Initiate from Controller	2-2.4, 4-8	2-5
DMFETCH-	$\overline{D}$	Memory Fetch Cycle Initiate from Controller	2-2.4, 4-8	2-5
DMACCR-	6	Access Request from Controller	2-2.3, 4-9	2-5
CK3D1-	$\overline{A}$	System Clock	2-2.3, 4-4	2-4

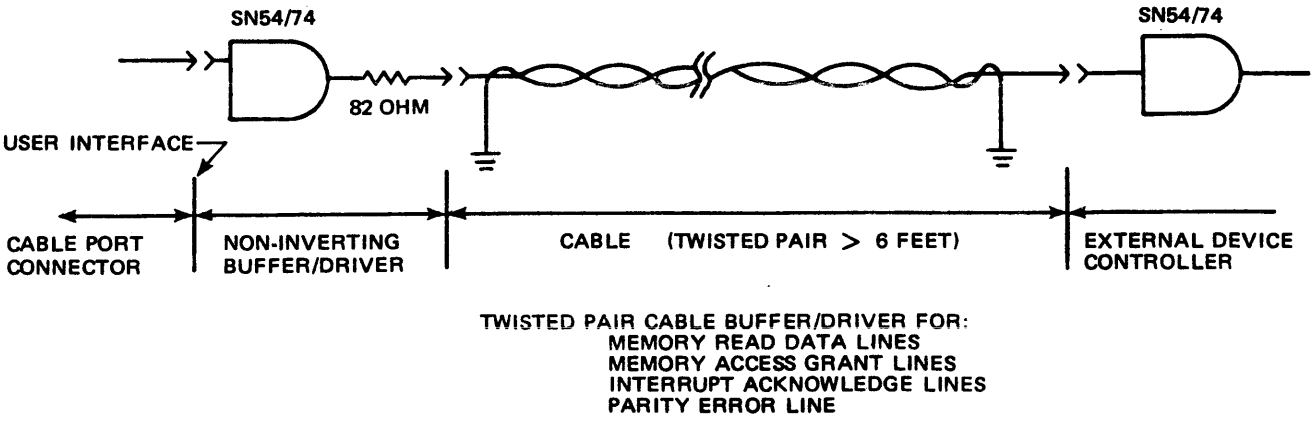


Figure 2-3. Twisted Pair Interface Connections

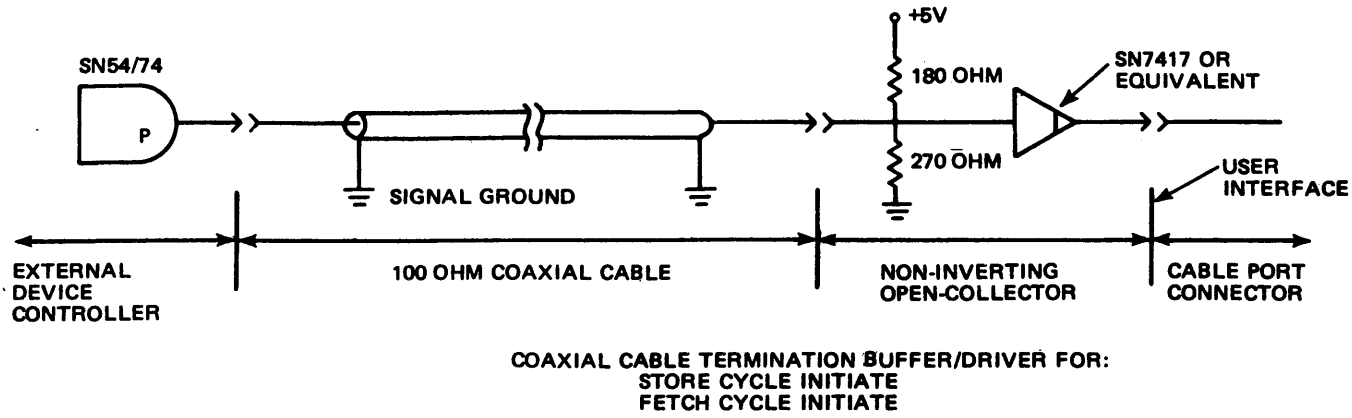


Figure 2-4. Coax Output Interface Connection

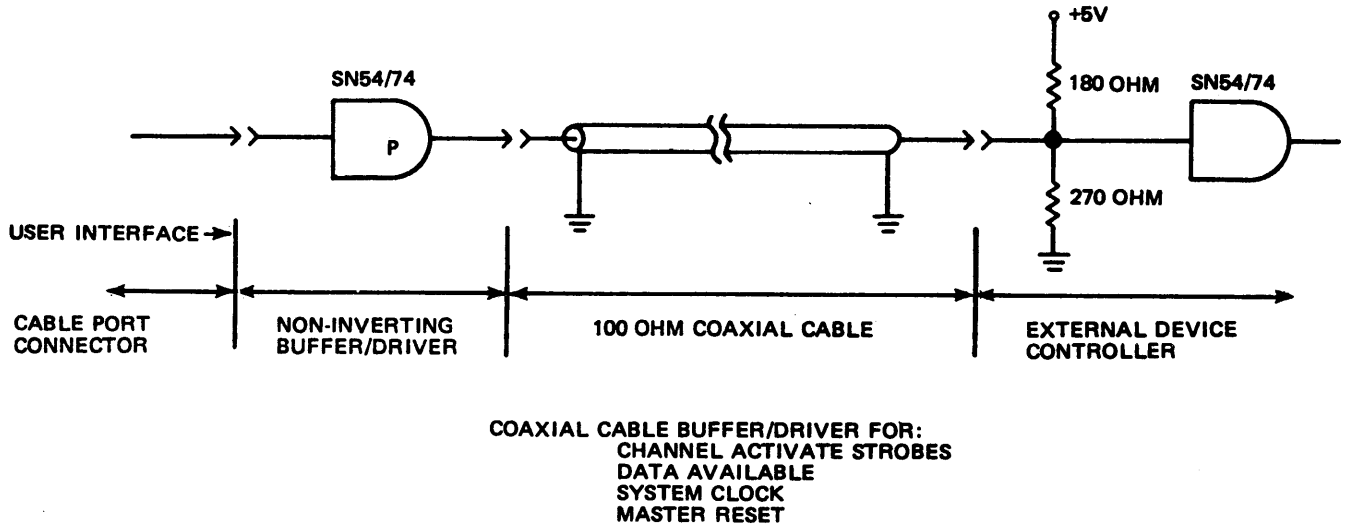


Figure 2-5. Coax Input Interface Connections

SECTION III
SIGNALS

3.1 GENERAL

The following paragraphs contain detailed descriptions of signals on the DMA bus (single or expanded bus) and the related timing requirements.

3.1.1 TIMING

Figure 3-1 illustrates the timing relationship of DMA signals that apply to the single or expanded bus.

3.1.2 LOGIC LEVELS

The logic level that defines a True signal is indicated by the suffix of the signature. A bar (–) following the signature indicates that the signal is True when it is in a logic ZERO state (0.0 Vdc). The absence of the bar (–) indicates that the signal is True when it is in a logic ONE state (+Vcc). For example, "RESET-" is in a low logic state when the master RESET switch is depressed.

3.2 MASTER RESET

Master reset signal signatures for the Central Processor Unit (CPU) and Expander are as follows:

CPU = DMRESET-

Expander = RESET-

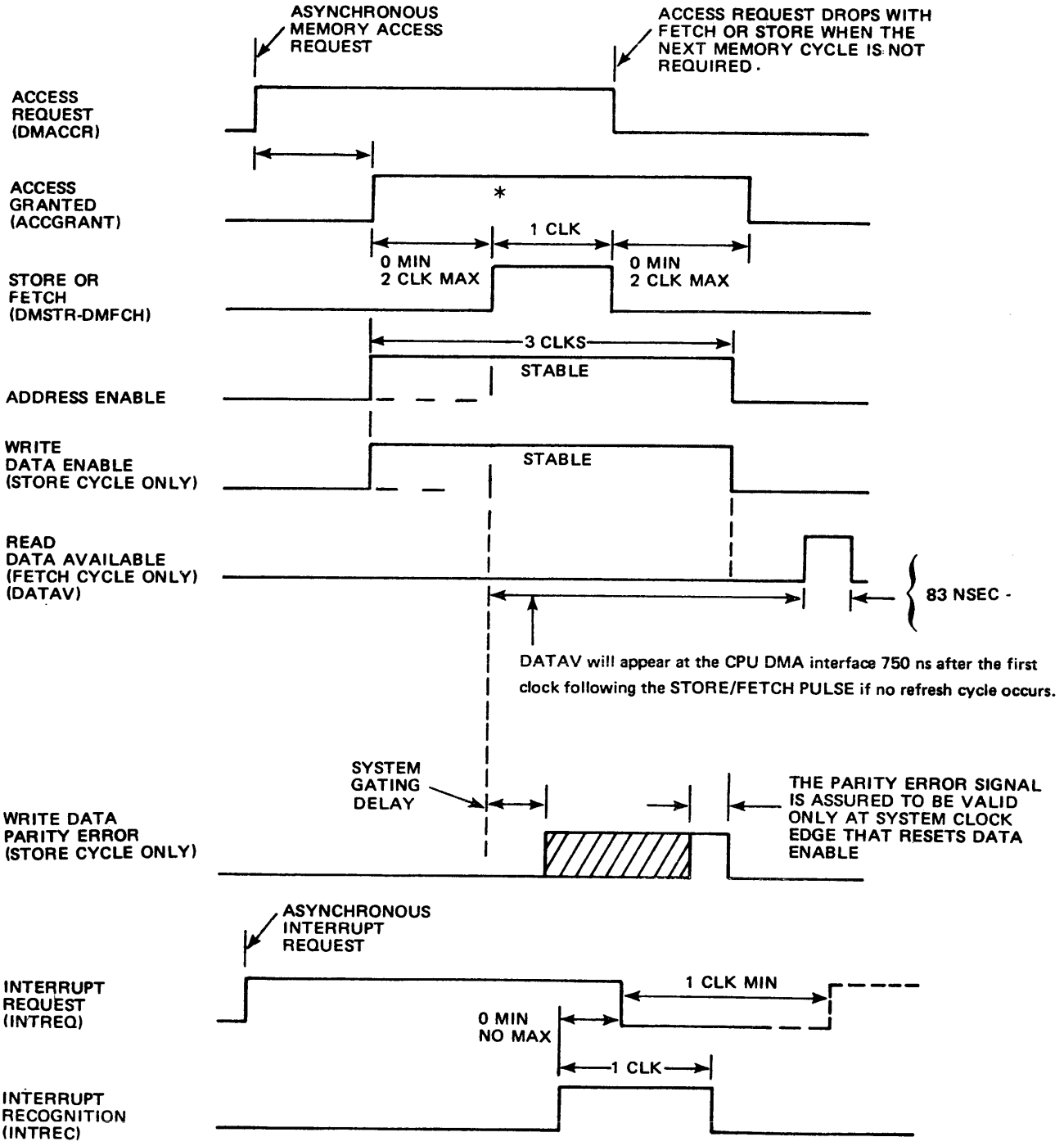
The master reset signal originates at the front panel of the CPU where a master RESET switch is used to generate the signal. The RESET switch signal is ORed with a power clear signal from the CPU power supply. The resultant signal is applied to the DMA interface of the CPU. In the expander, this signal is ORed with a power clear signal from the I/O chassis power supply. The resultant signal is applied to the controllers. A logic illustration of this signal generation is illustrated in figure 3-2.

3.3 MEMORY POWER RESET

Memory power reset signal signatures for the CPU and Expander are as follows:

CPU = MPRESET-

Expander = MPRESET-



NOTES:
1. SIGNALS ARE SHOWN IN THE TRUE SENSE.
* MAY DROP DURING REFRESH.

Figure 3-1. Direct Memory Access Signal Timing Relationships

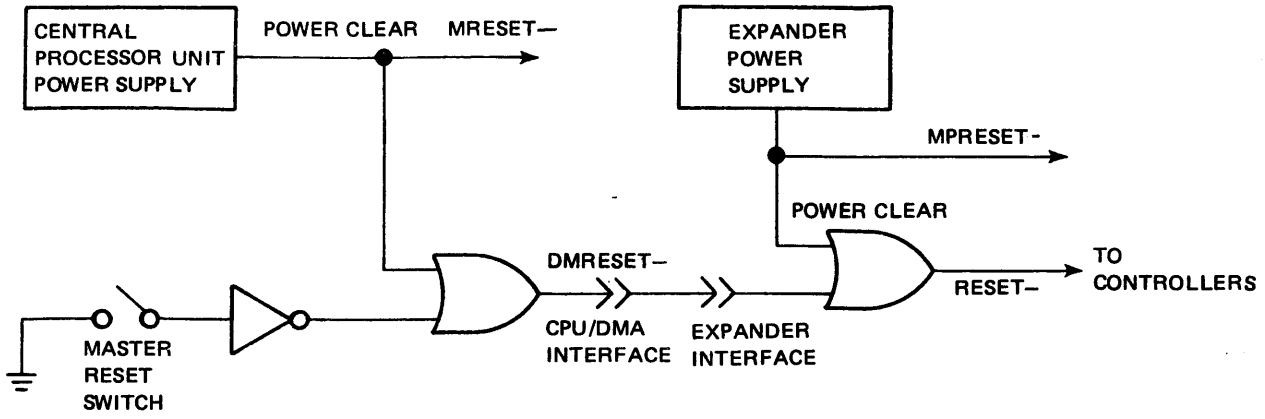


Figure 3-2. Master Reset Logic

The power supply reset signal is generated by a relay contact that is located within the power supply. This relay signal is used by the controllers to inhibit the generation of critical signals during power cycling. For instance, the disc controller would use MPRESET- at the point where a critical signal such as "Write Enable" is applied to the disc memory. MPRESET- should be used to inhibit a NAND gate driver at the interface. Only at this point is the signal effective for preventing False signal generation during power cycling.

3.4 SYSTEM CLOCK

System clock signal signatures for the CPU and Expander are as follows:

CPU = CK3D1-

Expander = CLOCK-

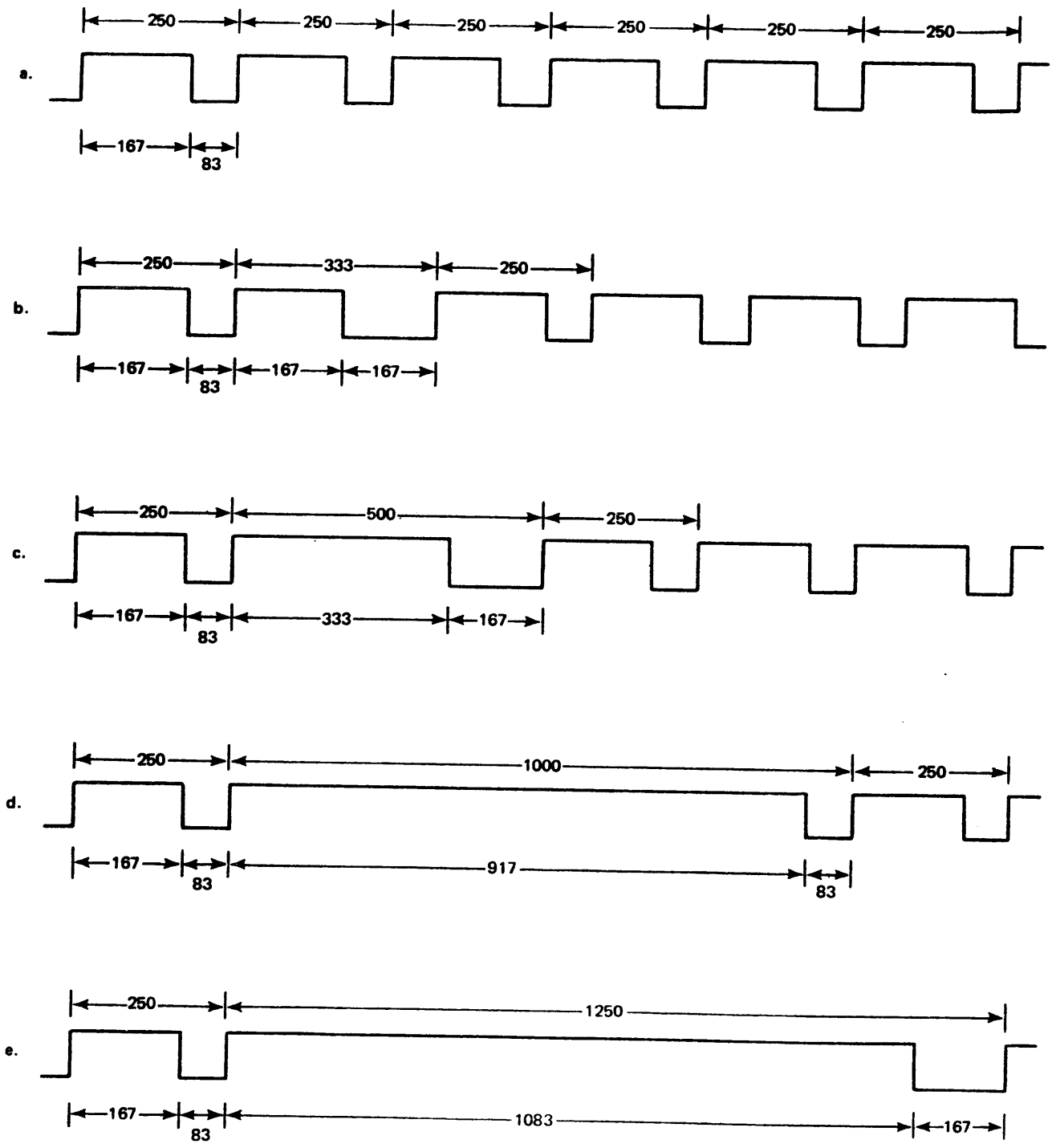
The basic system clock from the CPU originates from a 2.5 mHz crystal oscillator. This clock is a one-third duty cycle clock that remains True for 83 nanoseconds and False for 167 nanoseconds. The clock is modified by certain CPU operations before it appears at the interface. Variations in the clock are illustrated in figure 3-3. The clock is modified for a memory refresh cycle. The logic which interfaces to the DMAC must be of a synchronous design with the system clock, and must adhere to the timing diagram in figure 3-1 for implementation.

3.5 PARITY ERROR

The DMA bus parity error signatures for the CPU and Expander are as follows:

CPU = DMPERROR-

Expander = PARERR-



NOTE: ALL TIMES ARE IN NSEC UNLESS OTHERWISE SPECIFIED.
SIGNAL LEVEL IS CLOCK–

Figure 3-3. Computer Clock Cycle Variations

The presence of a logic ZERO indicates that memory write data sent to the CPU on a store cycle has even parity. A controller that is generating write data must generate a write parity bit (DEVMWD, 16) for the DMPERROR signal to be valid. Use of this signal is optional to the controller. No action is initiated by the CPU or the expander when this signal is True.

3.6 ACTIVE WORD STROBES

Activate word strobe one and two signatures for the CPU and Expander are as follows:

CPU = ATISTB1- and ATISTB2-

Expander = DEVATI1- and DEVATI2-

Channel activate word 1 and word 2 strobes have a logic ZERO duration of one clock pulse (83 nanoseconds). These strobes indicate the presence of word 1 of the ADAC (Model 960) or ATI (Model 980) command on the memory read data lines. These signals coincide with DATAV- for these special words on the memory read data lines. Use of the data word is described in Section I of this manual.

3.7 MEMORY READ DATA AVAILABLE

Memory read data available signatures for the CPU and Expander are as follows:

CPU = DATAV-

Expander = DATAV-

The memory read data available signal is a logic ZERO for the duration of one clock pulse (83 nsec) to indicate that the memory read data is stable on the bus. The controller uses this signal to strobe memory read data and conclude a memory read cycle. This strobe appears on the bus for all memory read cycles. The controller must keep track of selecting the DATAV for his memory fetch cycle. A new memory access can be initiated prior to receiving DATAV from the previous cycle. Sample logic for performing this tracking is illustrated in figure 3-4.

3.8 MEMORY FETCH AND STORE INITIATE

The memory fetch and store initiate signal signatures for the CPU and Expander are as follows:

CPU = DMFETCH- and DMSTORE-

Expander = DEVFETCH- and DEVSTORE-

The memory store and fetch lines are activated by the device controller. The signals on these lines will remain a logic ZERO for one clock time to permit a memory read cycle to be initiated with DEVFETCH- or DMFCH-;

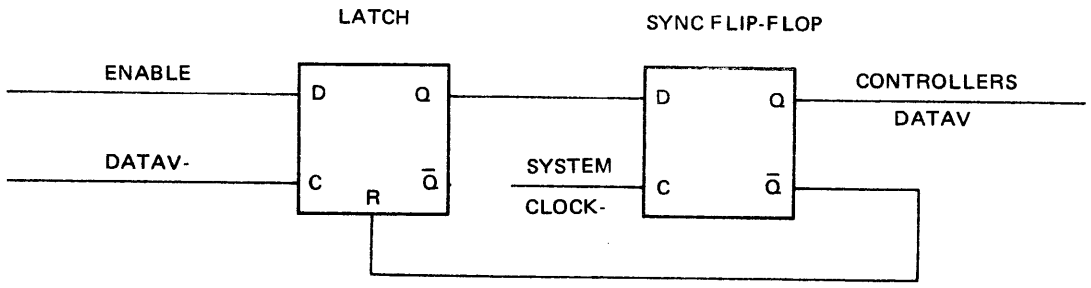


Figure 3-4. Memory Read Data Available Logic

or a memory store cycle with DEVSTORE- or DMSTR-. The trailing edge of the True signal is used by the CPU interface to retain the memory write data and/or the memory address. The controller must guarantee that addresses and data lines are stable at this time. This is assured if access granted is used to gate these lines to the DMA bus.

3.9 MEMORY ACCESS REQUEST

The memory access request signal signatures for the CPU and Expander are as follows:

CPU = DMAACCR-

Expander = ARDEV, (n)-
(n = 0 through 7)

A logic ZERO on the memory access request line indicates a memory cycle is being requested by a device controller. The expander receives eight request signals (ARDEV, (n)) from the expanded bus and services each request on a priority basis; i.e. device zero (N=0) has the highest priority and device seven (N=7) has the lowest priority. The CPU interface receives one request signal which may be from the expander or a device controller. The CPU signal is passed on to the CPU memory controller where access to memory is switched between the CPU and the DMA bus. The CPU will receive all cycles not used by the DMA. If a device requires continuous memory access, or the expander has a request pending from several users, the access request lines may be kept on. Continuous memory cycles are then granted to the DMA bus. The system clock is altered as shown in figure 3-3, line d, when a memory refresh cycle is required.

3.10 MEMORY ACCESS GRANTED

The memory access granted signatures for the CPU and Expander are as follows:

CPU = ACCGRANT-

Expander = AG, (N)-
(N = 0 through 7)

A logic ZERO on the memory access granted line indicates a response from the CPU or Expander to a memory access request. At the CPU DMA interface, a response to a request occurs in 3 clock periods or less depending upon the time in a CPU memory cycle that the request was issued. At the expander DMA interface, the maximum time for a response depends upon the priority level of the user and the activity level of higher priority users. The latched access granted signal should be used by the controller to gate the memory write data and memory address lines to the bus. The memory store/fetch pulses should then be generated within three clock periods of the granted time. If additional memory cycles are not requested, the request lines should be reset with the same clock that resets the store/fetch pulses. Since the trailing edge of the store/fetch signal is used to sample the memory address and write data lines, the designer must establish the interval (time setting) required from the time data is gated until the time it is sampled. Granted must be latched to maintain proper timing during memory refresh.

3.11 MEMORY ADDRESS

The memory address signal signatures for the CPU and Expander are as follows:

CPU = DMADR, (N)
(N = 00 through 15)

Expander = DEVADD, (N)
(N = 00 through 15)

The memory address signals are generated by the device controller. These signals are implemented on an open collector bus, which is shared by all controllers. The address lines are normally held at a logic ONE level and are only defined when the controller has been granted memory access. The controller will enable its memory address and maintain these lines on the bus in a stable state concurrent with memory access. Signal stability is required at the CPU at the trailing edge of the store or fetch pulse. This timing is accomplished by using the access granted signal to enable the address lines.

3.12 MEMORY WRITE DATA

The memory write data signal signatures for the CPU and Expander are as follows:

CPU = DMD (N)

Expander = DEVMWD, (N)
(N = 00 through 16)

Memory write data signals are generated by the device controller. These signals are generated and gated by the same method used for the memory address lines during a memory store cycle. Timing requirements are the same. Bit 00 is the most significant bit, and bit 15 is the LSB. The seventeenth bit on the bus (DEVMWD 16) is used to generate odd parity on the write data lines. The memory controller performs a parity check on this bus, and returns the parity indication to the device controller. This bit does not have to be used. However, it must be correct if the DMPERROR signal is used by the controller.

3.13 MEMORY READ DATA

The memory read data signal signatures for the CPU and Expander are as follows:

CPU = DMMRD (N)

Expander = DEVMRD (N)
(N = 00 through 16)

All controllers monitor the memory read data lines. These signal lines should not be loaded with more than two gate inputs on each line. The data available signal defines the interval that these signals represent True data for the previous memory fetch cycle. Bit 00 is the MSB and bit 15 is the LSB. The seventeenth bit is the parity bit that is used to generate odd parity on the read data lines. This signal is True for the Model 980 series computers only.

3.14 INTERRUPT REQUEST

The interrupt request signatures for the CPU and Expander are as follows:

CPU = INREQ-

Expander = INTDEV, (N)-
(N = 0 through 7)

The interrupt request, from the device controller to the CPU is a logic ZERO when the device controller requests an interrupt cycle with the CPU. The controller holds the signal at a logic ZERO until the interrupt is recognized by the CPU. (See the signal timing relationships in figure 3-1.) The controller removes the request signal and stores status when the interrupt recognition signal is received. There is one signal for each controller.

3.15 INTERRUPT RECOGNIZED

The interrupt recognized signal signatures for the CPU and Expander are as follows:

CPU = INTREC-

Expander = IRECOG, (N)-
(N = 0 through 7)

The interrupt recognized signal from the CPU to the controller is a logic ZERO when the CPU has received a DMA interrupt and is acquiring the instruction in the DMA trap location. The Model 960 CPU will only recognize a DMA interrupt when bit 8 of the CPU status register is a logic ZERO and no higher priority interrupt is pending in the CPU. The Model 980 will recognize a DMA interrupt when bit 12 of the CPU status register is a logical ONE and no higher priority interrupt is pending.

SECTION IV
HARDWARE

4.1 GENERAL

This section of the manual describes the standard hardware that is available to implement a computer system with Direct Memory Access (DMA) device controllers. The hardware required to install and interconnect DMA subsystems (controllers) are described in this section of the manual. Information for the DMA controllers and associated peripherals is included in the "Direct Memory Access Channel Controller" equipment manual (TI Part No. 966312-9702).

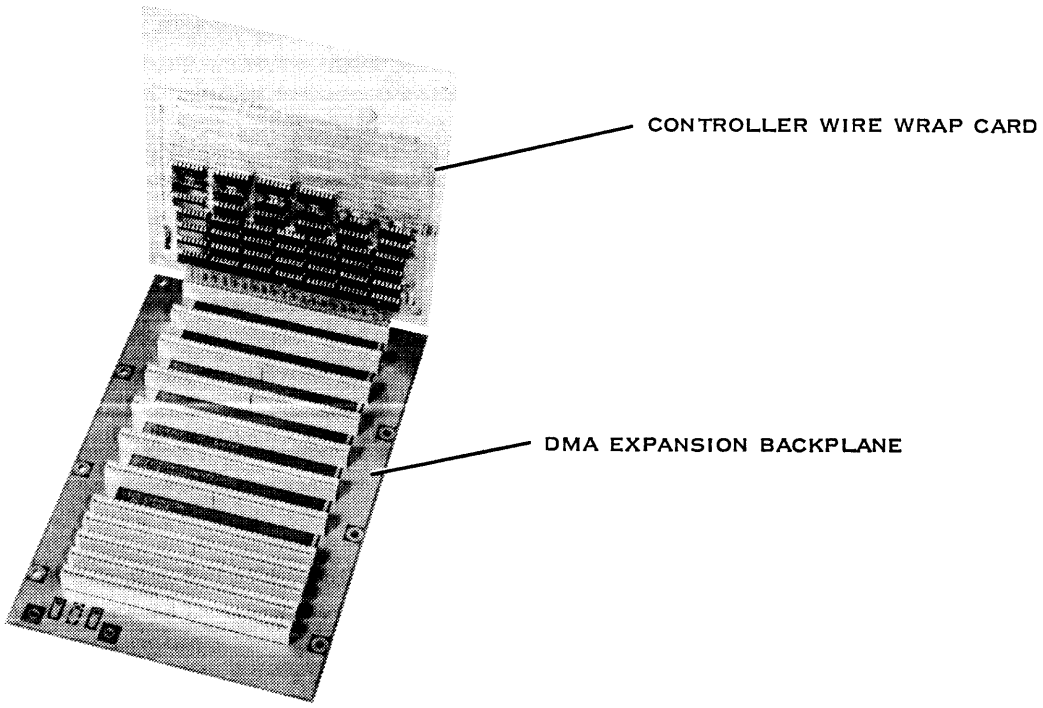
4.2 EXPANSION KITS

A variety of standard expansion kits are available for mounting standard DMA device controllers or for mounting interface equipment that is designed by the user. A DMA expansion kit completes the wired interface connection between the DMA bus wiring and controller wiring. A DMA expansion kit includes a cable, backplane, and printed circuit (PC) card(s). One end of the cable is connected to the DMA interface card of the CPU. The other end of the cable is connected to the DMA expander cards or to a paddle board. The backplane is a chassis with a number of 80 pin edge connectors which are wired for the DMA bus signals (single or expanded) and controller card(s) for which the kit is designed. The card(s) in the kit include a paddle board for internal expansion or four expander cards for external expansion.

4.2.1 INTERNAL

The standard internal DMA expansion kit is used to install a DMA controller in the CPU chassis. The expansion backplane connector plate is illustrated in figure 4-1. The DMA backplane connector plate occupies the space which is also used for the Input/Output (I/O) expansion backplane on the Model 980 series computers or the Communications Register Unit (CRU) expansion backplane on the Model 960 series computers. The basic Texas Instruments part number for the DMA expansion kit is 957482. This kit is made available to the customer to complete the interface for various configurations as listed in table 4-1. Figures 4-2 through 4-4 provide views of the various configurations.

The internal DMA expansion kit is made available in two configurations to satisfy special or customer designed interface requirements. One configuration includes the DMA expander cards and wiring for three sets of DMA ports. The customer can complete the interface to these connectors from device controllers that are located in the customer designed hardware. This configuration also permits fan-out of the DMA bus to at least three separate expansion chassis.



128998 (389-27)

Figure 4-1. Internal DMA Expansion Backplane

Table 4-1. DMA Internal Expansion Kit Part Numbers

TI Part No. Kit	Description
957482-0001	Wired for moving head disc controller with escutcheon for Model 960 computer. All connectors utilized.
957482-0002	Wired for fixed head disc controller with escutcheon for Model 960 computer. Three blank connectors.
954482-0003	Wired for Model 979 magnetic tape controller with escutcheon for Model 960 computer. All connectors utilized.
973599-0001	Unwired for customer applications for 960.
957482-0004	Same as -0001, except Model 980 escutcheon.
957482-0005	Same as -0002, except Model 980 escutcheon.
957482-0006	Same as -0003, except Model 980 escutcheon.
973599-0002	Same as -0001, except for 980.

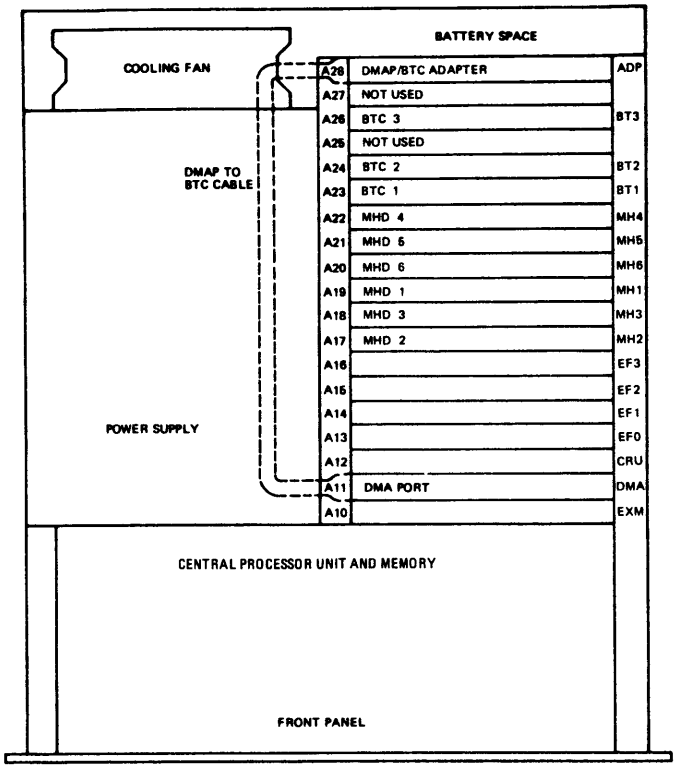


Figure 4-2. Moving Head Disc Controller CPU Mounting Configuration

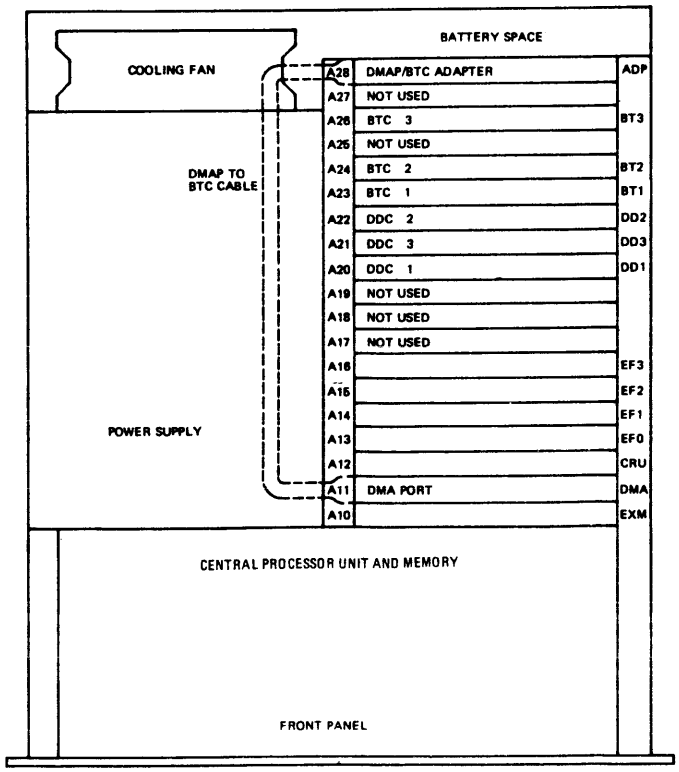


Figure 4-3. Fixed Head Disc Controller CPU Mounting Configuration

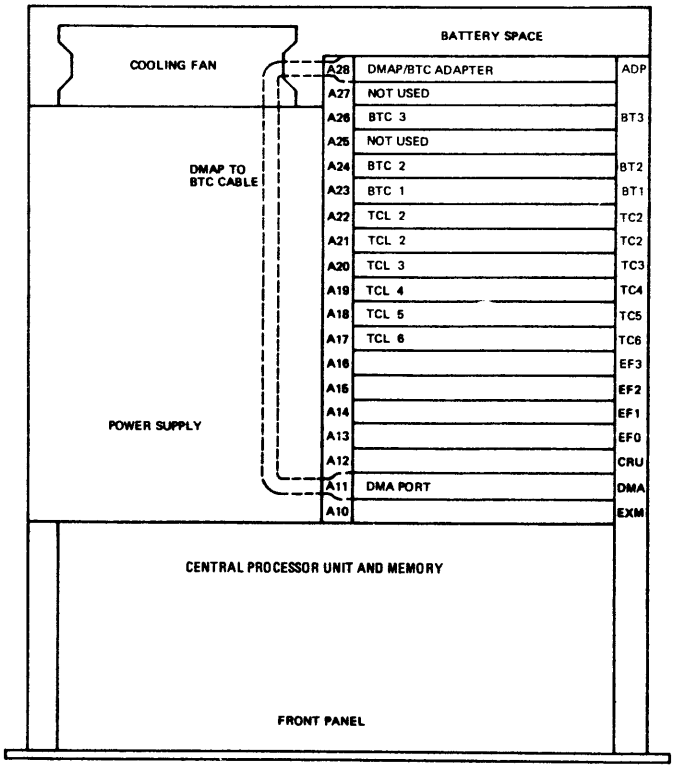


Figure 4-4. Model 979 Magnetic Tape Controller CPU Mounting Configuration

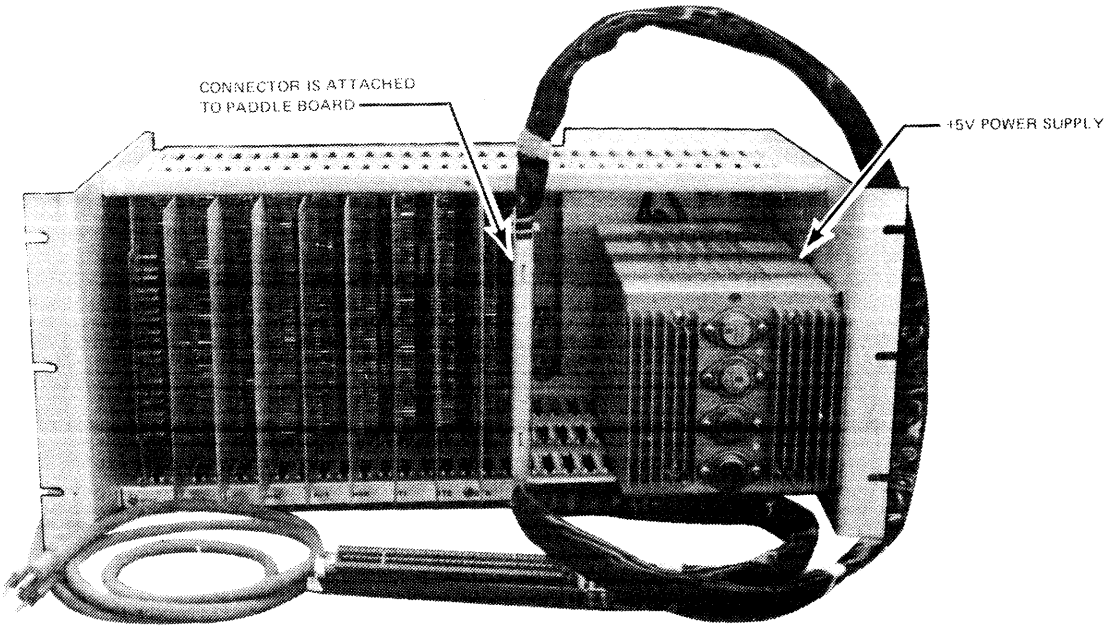
The second configuration contains the same hardware that is used in kits having TI Part Nos. 957482-0001 through -0006; however, all wiring has been excluded on the expander backplane. This kit is designed for the customer that elects to design, package, and implement a custom controller similar to the 957482-0001 through -0006 kits.

If only one DMA controller needs to be interfaced, and the internal expansion has been allocated for I/O or CRU, then the External Signal Controller Mounting Kit (TI Part No. 966340) may be used to house the controller (see figure 4-5).

4.2.2 EXTERNAL

When a system requires more than one DMA device controller or when the internal CPU mounting space is in use for I/O or CRU expansion, the device controllers must be installed in a separate equipment chassis external to the standard computer mainframe. This is accomplished by use of an external DMA expansion kit. An external DMA expansion kit consists of:

- a 10-foot cable that connects the DMA interface card in the CPU to the DMA expander cards



128999

Figure 4-5. External Single Controller Mounting Kit

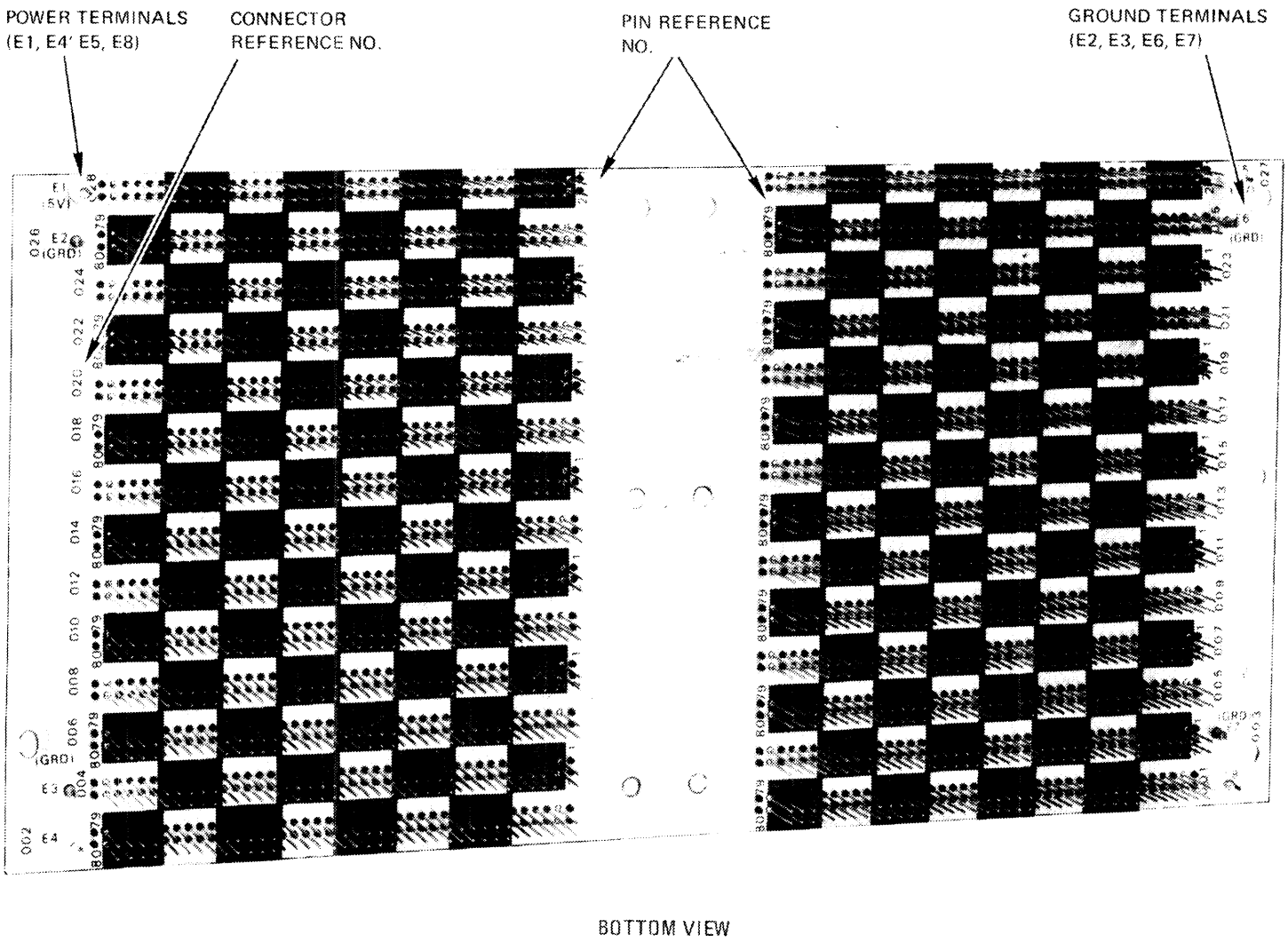
- a backplane expander board (figure 4-6) that is wired for various configurations
- 4 PCB cards which make up the DMA expander.

There are three basic types of external DMA expansion kits. Each kit has a different basic part number. These three kit types are identified in table 4-2. (See figures 5-1 through 5-3.)

4.3 EXPANSION CHASSIS

The DMA external expansion kits are mounted in an optional Input/Output (I/O) Expansion chassis. The I/O Expansion chassis includes a frame, power supply, card cage, and front panel. (A pictorial illustration is provided in figure 4-7. Slides are included for a rack mounting installation. The overall physical dimensions of the I/O Expansion chassis are listed in table 4-3.

The power supply is located at the rear of the unit and can be easily removed from the chassis for servicing. The power supply specifications are listed in table 4-4. The supply is functionally illustrated in figure 4-8.



129000 (17592-7)

Figure 4-6. DMA External Expansion Backplane Connectors and Pin Configurations

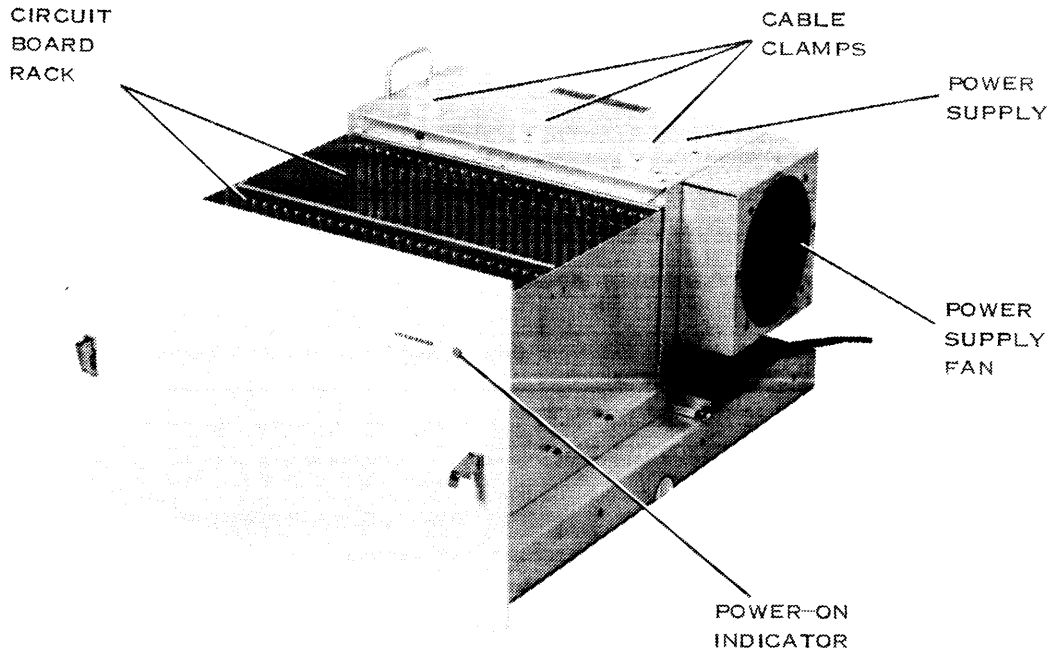
Table 4-2. Three Basic Types of External DMA Expansion

Part Number	Description	
1.	DMA Expansion with 28 connectors wired as follows, this kit uses one half of the space available in the Expansion chassis:	
	966555-2	Wired for the expander cards(4) only. Remaining 24 connectors are blank for custom wiring.
2.	DMA Expansion with 56 connectors wired as follows, this kit uses all of the space available in the Expansion chassis.	
	966555-0001	Wired for the expander cards, the moving head disc controller, the fixed head disc controller, the 2310 line printer controller, and the Model 979 Tape Transport Controller.
3.	DMA Expansion with 10 connectors wired as follows:	
	966340-0001	Wired for moving head disc controller.
	966340-0002	Wired for fixed head disc controller.
	966340-0003	Wired for 979 magnetic tape controller.

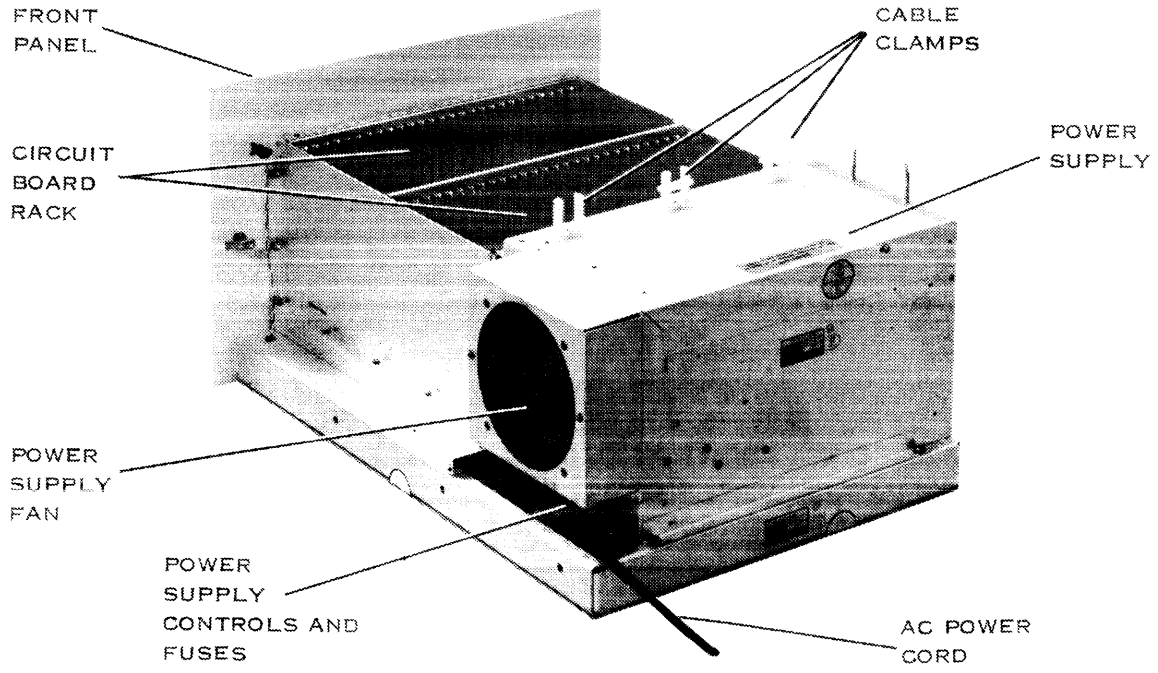
The I/O expansion unit card cage has a capacity of 56 half-inch spaced logic cards. The unit can house two expansion kits (TI Part No. 966555-2) or one of the larger kits (TI Part Nos. 966555-1). Controller cards that are implemented on wire-wrap boards require one-inch center-to-center card spacing. The power supply fan circulates cooling air throughout the chassis. The +5V power supplies current to the controller cards installed in the chassis. Typical power consumption for this voltage source is listed in table 4-5.

4.4 CUSTOM LOGIC BOARDS

When a user elects to complete the interface to the DMA bus with custom designed logic and an internal or external expansion kit has been selected which satisfies the expansion and/or implementation requirements, the user can select custom circuit boards to implement the custom designed logic. Two types of boards (Type 1 and Type 2) are available. Both types of boards have the same outside dimensions. These boards contain 80 pin bottom edge connectors with preassigned Vcc and ground connections. These boards are also available with 72 pin top edge connectors.



129027 (980-1173-15-2)



129026 (980-1173-15-4)

Figure 4-7. Rack Mounted Input/Output Expansion Chassis

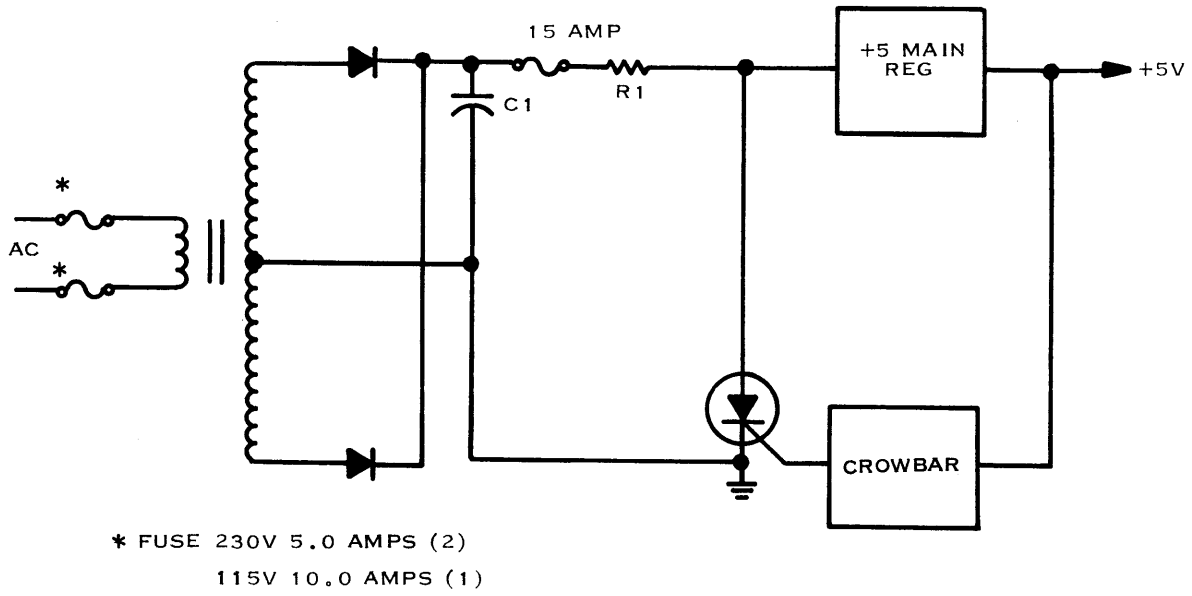
Table 4-3. External Expansion Chassis Characteristics

Characteristic	Specifications
Height	10.5 inches, 26.67 centimeters
Width	19 inches, 48.26 centimeters
Depth	24 inches, 60.96 centimeters
Weight	*66 lbs., 145.5 kilograms
NOTE	
*Unit only – Expansion kit and controllers excluded.	

Table 4-4. Power Supply Characteristics

Characteristic	Specification
Environmental Characteristics	
Temperature:	
Operating	0° to 60° Centigrade
Non-operating	–40° to +100° Centigrade
Humidity:	
Operating	10 to 85 percent
Non-operating	0 to 95 percent
Barometric Pressure	25 to 30 millimeters of mercury
Power Characteristics	
Input Voltage	105 to 125 Vac
Frequency	47 to 63 Hz
Power Consumption	350 Watts maximum

The Type 1 board is illustrated in figures 4-9 and 4-10. This board may be purchased in a single ended version (TI Part No. 214082-0001), or in a double ended version (TI Part No. 214084-0001). The Type 1 board is configured for point-to-point soldering connections. This board is designed for use with half-inch spaced connectors on the backplane, provided the build up of wiring on the solder side of the PC board is minimized. The board is designed for the wiring to be installed on the component side of the board. Special features of this board include: pre-bussed ground and Vcc connections, three holes for each network, two holes for from/to wiring, and one hole for the integrated circuit (IC) pin. The Type 1 board can accept 14 or 16 pin standard dual-in-line packages.



(A)129002

Figure 4-8. Input/Output Power Supply Functional Diagram

Table 4-5. Controller Card Current Loads

Load	Current
Expander cards (4)	1.3 Amperes
Line printer controller cards	1.0 Ampere
Model 979 Tape Controller	8.6 Amperes
Fixed head disc controller	5.8 Amperes
Moving head disc controller	7.5 Amperes

The Type 2 custom logic board is illustrated in figure 4-11 and 4-12. This board may be purchased in the single ended configuration (TI Part No. 217862-0001) or the double ended configuration (TI Part No. 217863). These boards are designed for use in a wire-wrap configuration. Pin location accuracy is compatible for use on automatic wire wrap machines. Due to wire wrap pin length, these boards require one inch center spacing for the backplane connectors. Therefore, two connectors on the backplane, with one-half inch spacing, must be allocated for one wire-wrap board.

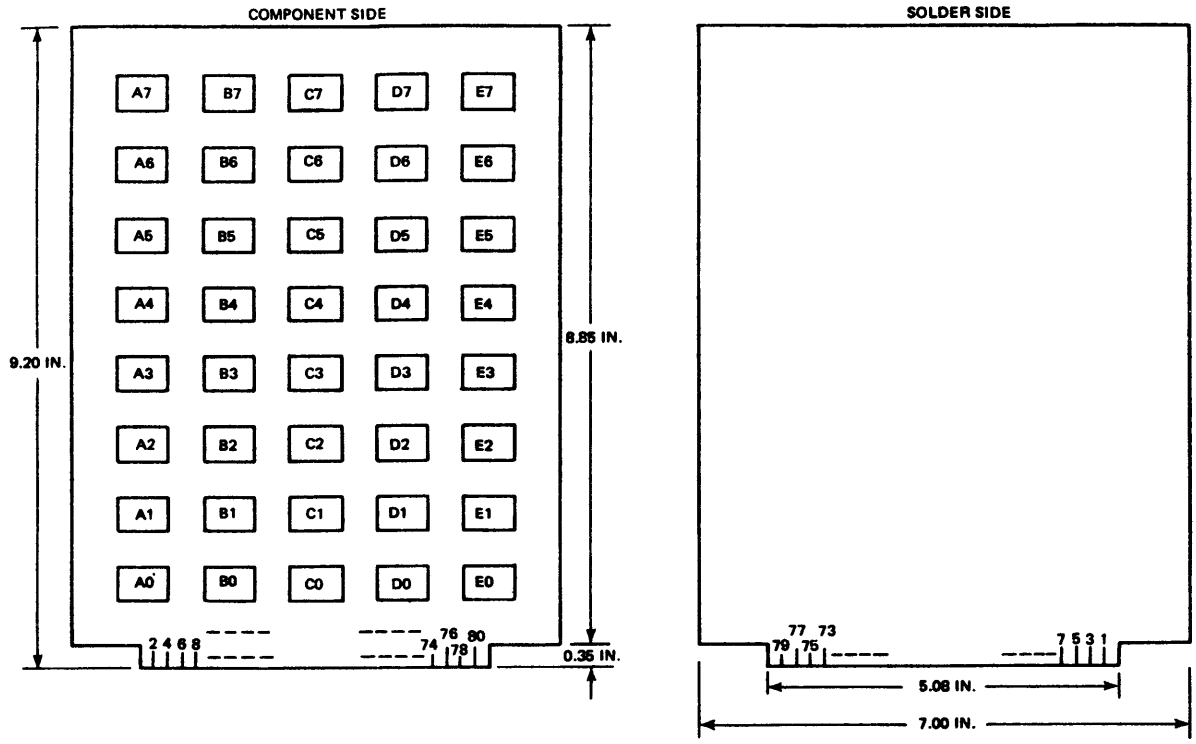


Figure 4-9. Single Connector Type 1 PC Board Physical Configuration

4.5 EXPANSION KIT INTERFACE REQUIREMENTS

When the customer selects a suitable DMA expansion kit and has installed a special device controller, the interface connection from the DMA bus termination on the backplane must be completed to the DMA interface of the controller. The point-to-point information is included in an appendix to the DMAC expansion manual (TI Part No. 216759-9701 and 216759-9711 or 216759-9712). In this appendix the customer can establish and compare individual signals and related pin locations as listed in the "Load List" and "Pin List". See the following section for documentation details.

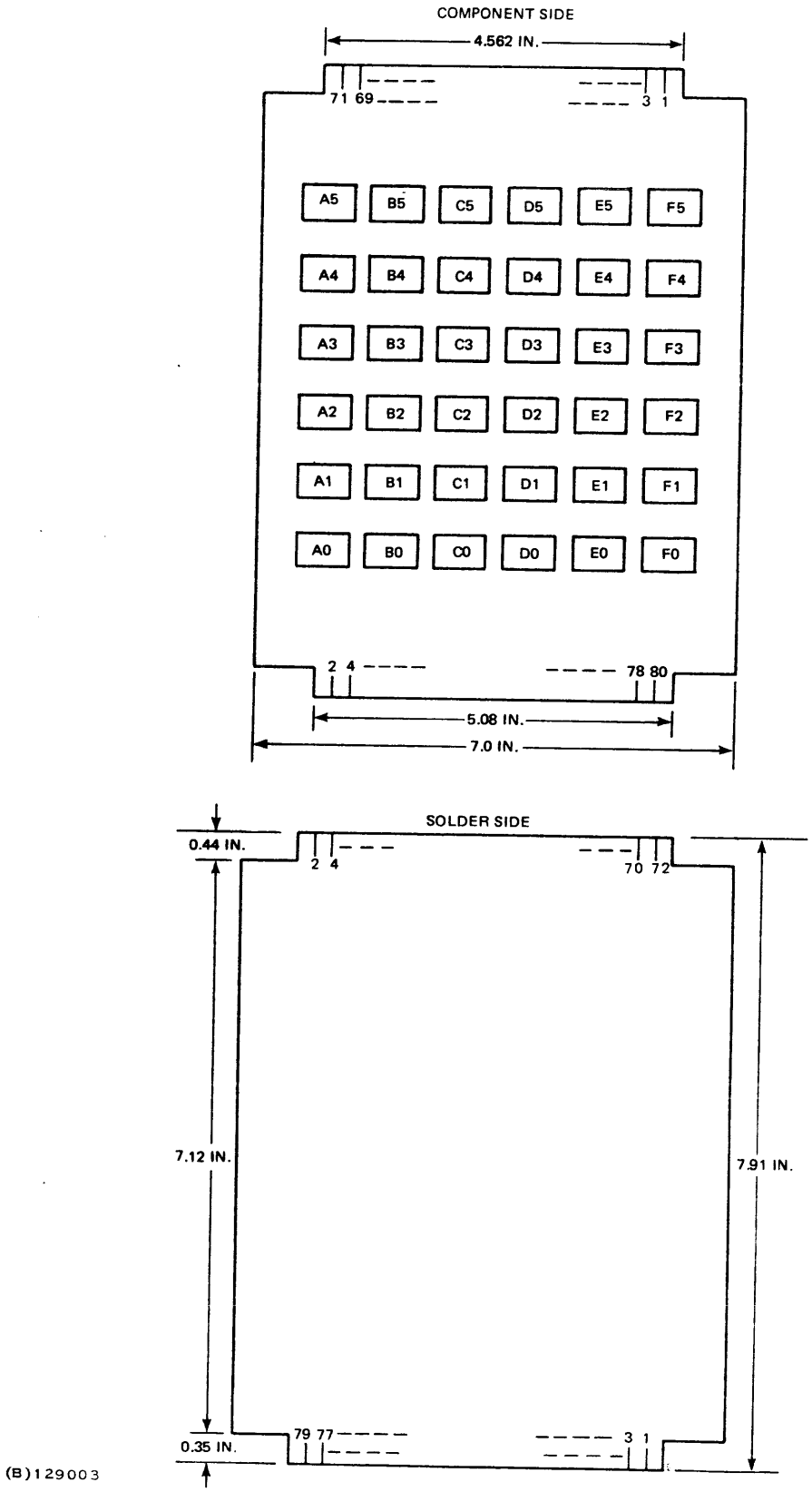


Figure 4-10. Double Connector Type 1 PC Board, Physical Configuration

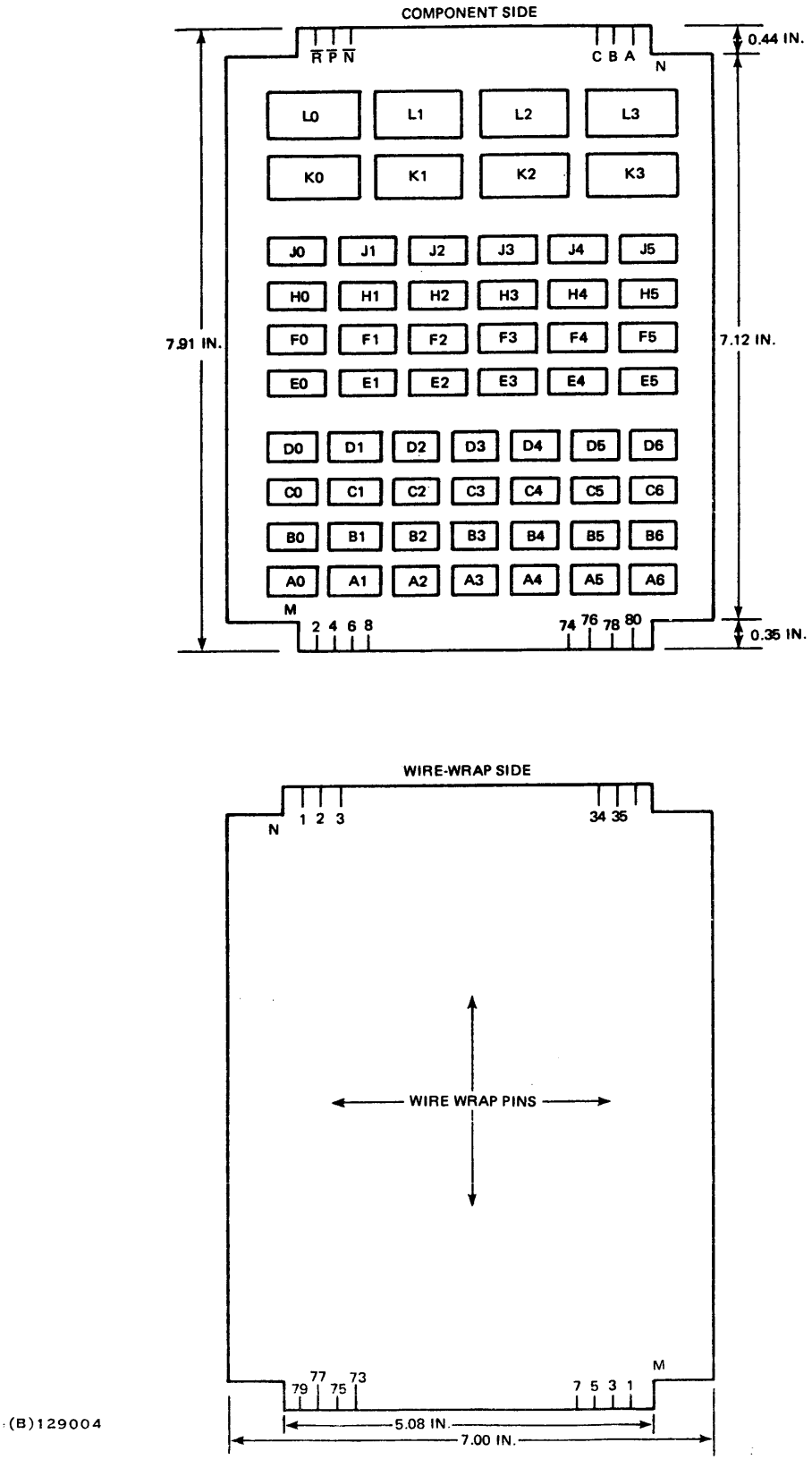
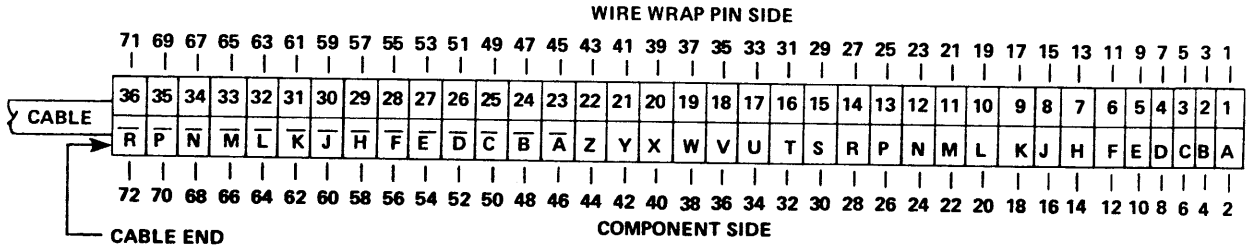


Figure 4-11. Double Connector Type 2 PC Board, Physical Configuration



(B)129005

Figure 4-12. Type 2 Top Edge Connector Pin Assignment

SECTION V
DOCUMENTATION

5.1 MANUALS

All components of the computer DMA subsystem are adequately documented. This information is supplied in the form of maintenance manuals to facilitate the installation and maintenance requirements. The manuals listed in table 5-1 can be purchased for the DMA hardware that is noted in the table.

Table 5-1. Direct Access Documentation List

KIT	KIT NO.	REFERENCE ILLUSTRATION	MANUAL NO.
DMA Expansion Kits, All			216759-9701
DMA Expansion Kit,	966555-0002	Figure 6-1	216759-9703
	966555-0001	Figure 6-2	216759-9708
DMA CPU Mounting Kit	957482 – All		961741-9701
Fixed Head Disc Controller Kit			961700-9701
Moving Head Disc Controller Kit			961693-9701
979 Tape Controller Kit			240801-9701
Line Printer Controller Kit			217704-9701
Block Transfer Controller	All Controller Kits		240802-9701

5.2 COMPUTER GENERATED DOCUMENTATION

All manuals are supported by computer generated documentation in the form of a load list, pin list, wire list and Logic Implementation List (LIMP). The same data base for this documentation is used for the automated wiring data.

5.2.1 LOAD LIST

A load list is supplied with every controller manual and DMA expansion manual. The function of the "Load List" is to provide quick identification of all pins in any wired chain and includes locations, pin numbers, and semiconductor network types or connector types. All pin signatures are sorted into alpha-numeric order.

The load list is a combined interconnection list of all signals in the controller regardless of the number of boards on which the logic is implemented. All signals that are routed from board to board appear on the bottom edge connector (Type CB) of the boards. The wire which interconnects the signal from board to board is documented in the load list for the expansion kit in which the controller is wired. The load list for the expansion kit is a list of all wires on the backplane where all circuit types in the Load List are Type CB.

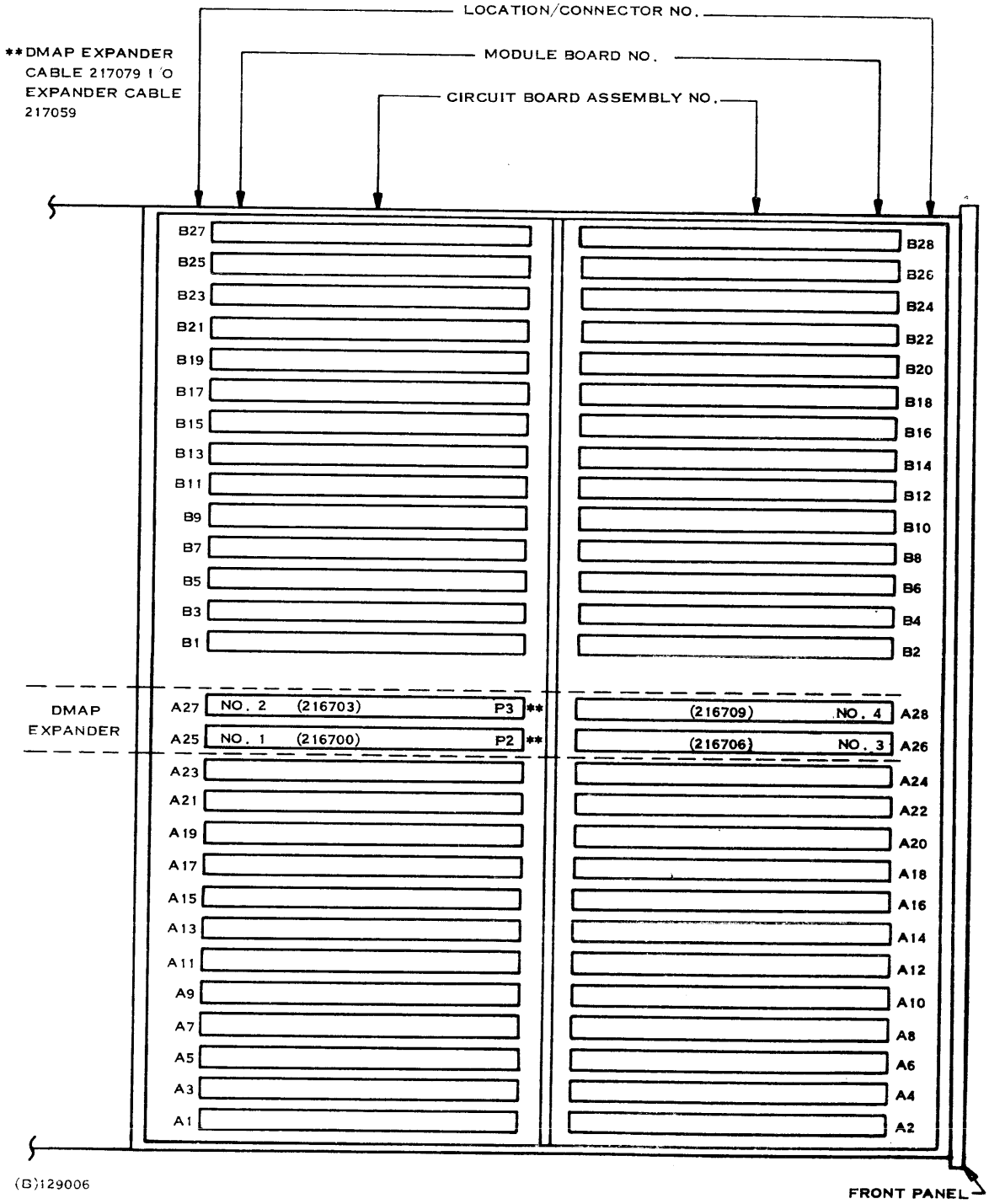


Figure 5-1. Direct Memory Access PC Card Locations, Expansion Kit 966555-0002

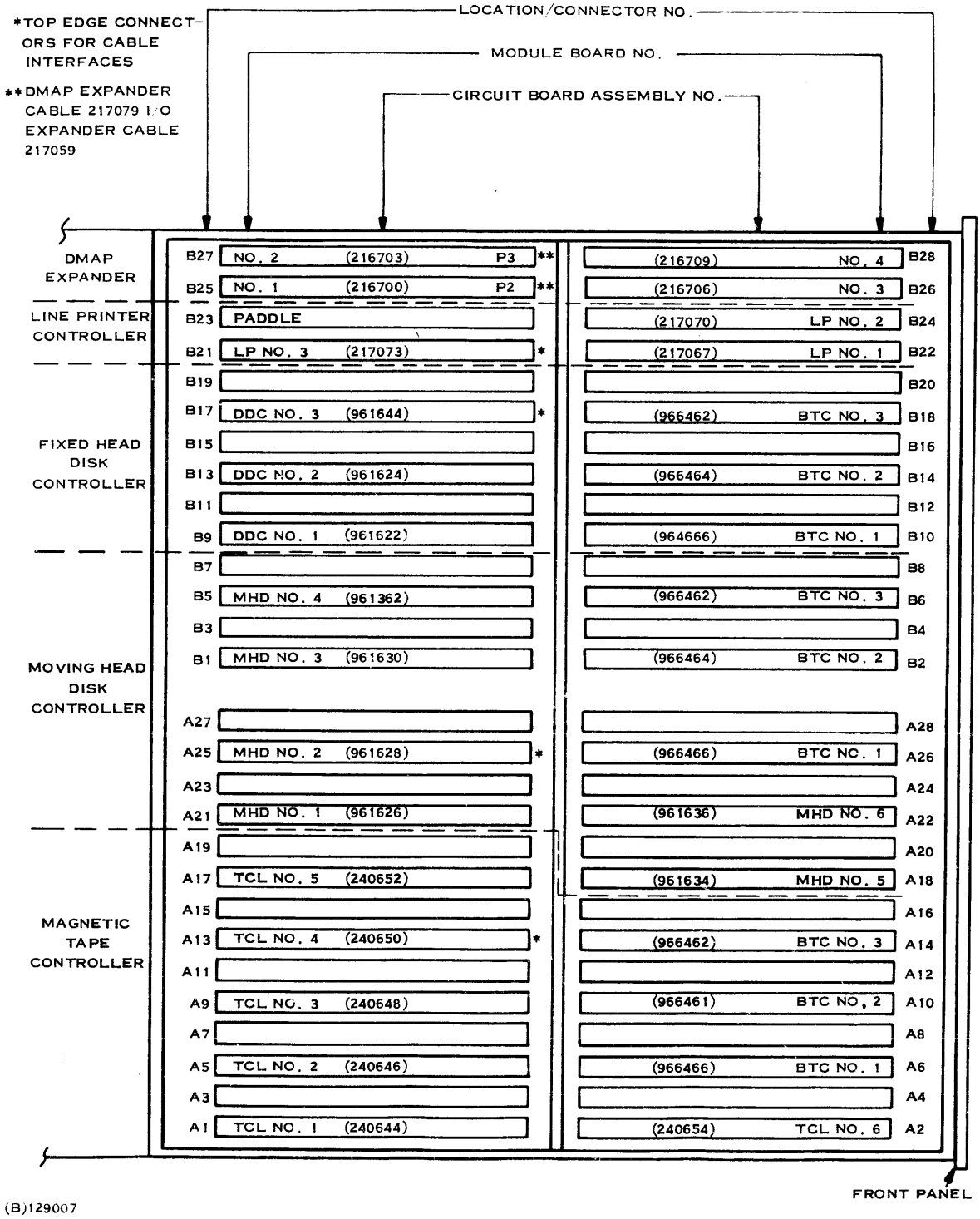


Figure 5-2. Direct Memory Access PC Card Locations
Expansion Kit 966555-0001

5.2.2 PIN LIST

Every load list is accompanied by a pin list. The pin list is a list of all devices and connectors in order by location sequence. This list makes it possible to identify signals appearing on all pins of any given circuit device, network, and connectors.

5.2.3 LIMP OR DOCUMENTATION LIST

All logic is supported by a computer generated Logic Implementation List (LIMP). This computer list is the equivalent of the logic drawings. The LIMP is a list of the logic implementation from the gate output to the input. The implementation is continued for any number of fan-outs to the level which defines the generated signal. Signals are defined by glossary statements, comments, and Boolean equations.

USER'S RESPONSE SHEET

Manual Title: Model 960/980 Computers Direct Memory Access Channel Manual (966312-9701)

Manual Date: 1 August 1977 **Date of This Letter:** _____

User's Name: _____ **Telephone:** _____

Company: _____ **Office/Department:** _____

Street Address: _____

City/State/Zip Code: _____

Please list any discrepancy found in this manual by page, paragraph, figure, or table number in the following space. If there are any other suggestions that you wish to make, feel free to include them. Thank you.

Location in Manual	Comment/Suggestion
_____	_____
	_____
	_____
	_____
_____	_____
	_____
	_____
	_____
_____	_____
	_____
	_____
	_____

CUT ALONG LINE

NO POSTAGE NECESSARY IF MAILED IN U.S.A.
FOLD ON TWO LINES (LOCATED ON REVERSE SIDE), TAPE AND MAIL

FOLD

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

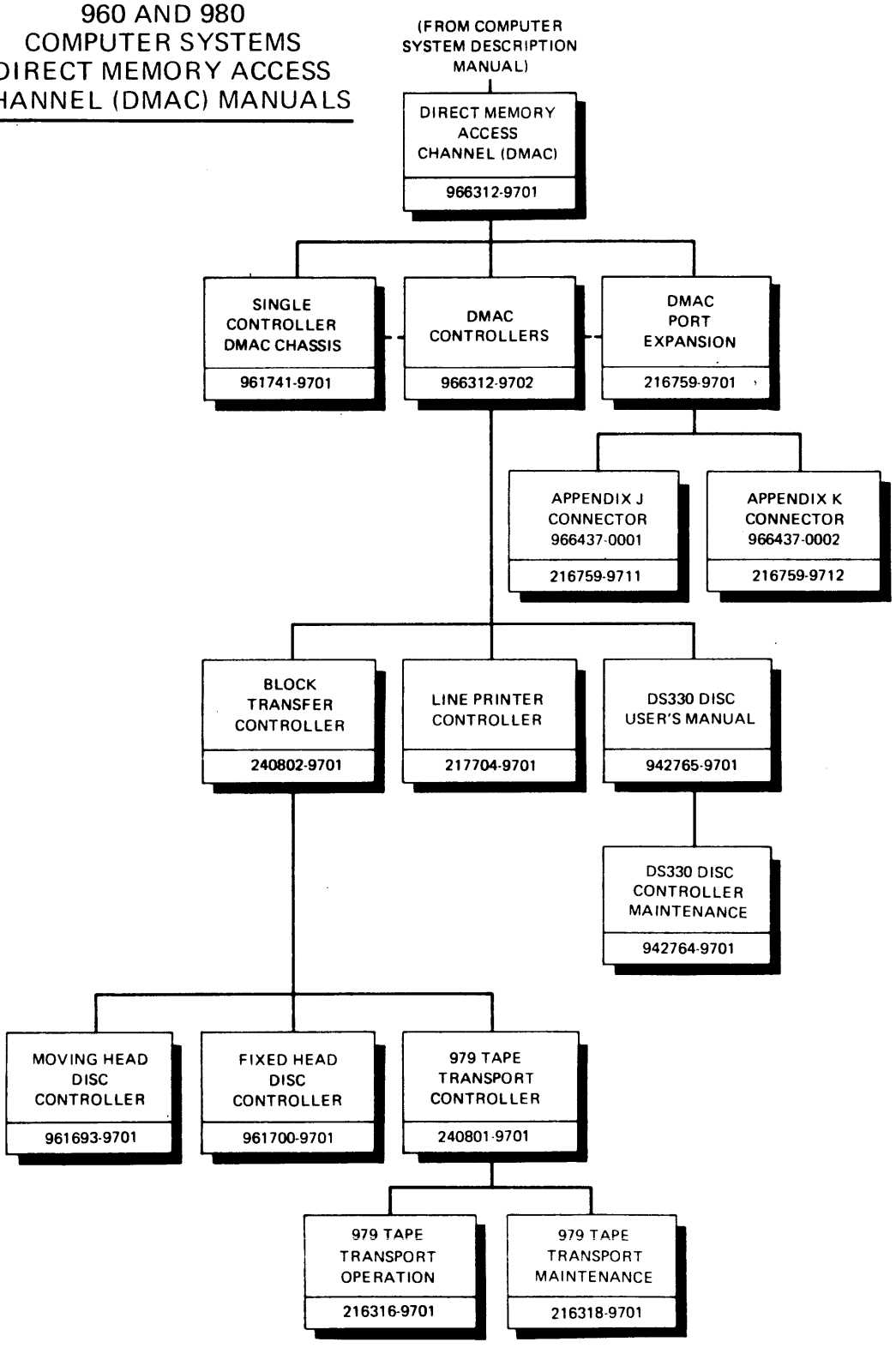
FIRST CLASS PERMIT NO. 7284 DALLAS, TX

POSTAGE WILL BE PAID BY ADDRESSEE

TEXAS INSTRUMENTS INCORPORATED
DIGITAL SYSTEMS GROUP
ATTN: TECHNICAL PUBLICATIONS
P.O. Box 2909 M/S 2146
Austin, Texas 78769

FOLD

960 AND 980 COMPUTER SYSTEMS DIRECT MEMORY ACCESS CHANNEL (DMAC) MANUALS



TEXAS INSTRUMENTS
INCORPORATED
DIGITAL SYSTEMS DIVISION
POST OFFICE BOX 2909 AUSTIN, TEXAS 78769