Data Manual

TGC100 Series
1-μm CMOS Gate Arrays

1989

TEXAS INSTRUMENTS

TGC100 Series

1-μm CMOS Gate Arrays

Data Manual

1989 Application Specific Integrated Circuits

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INSTRUMENTS

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Specifications contained in this data book supersede all data for these products published by TI in the United States before October 1987.

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Contents

1 Introduction

INTRODUCTION

Texas Instruments presents the TGC100 Series 1-μm CMOS Gate Array Data Manual, a comprehensive reference document providing detailed specifications for each macro included in TI's TGC100 Series engineering workstation software, release 2.0.

how to use this manual

This manual provides sufficient detail for a system designer to evaluate the availability, performance, and suitability of macros to employ in the design of custom gate-array ASICs. For the macro evaluation process, the macro data sheets contain the following detailed information:

- Macro identification including a description supported with logic symbol and truth table or typical functional sequences
- Electrical and switching time parametric specifications
- Detailed logic diagram showing the hardwired macros used in the creation of the software macros
- Indexes and notes cross referencing the gate array macro to similar CMOS and TTL functions

Other sections of the manual contain data for matching the design evaluation with the base arrays and packages offered in the TGC100 Series gate array family. As examples:

- The family data includes data pertinent to the array sizes and packages available.
- The alphanumeric index and library cell summary include a basic cell count for each macro which can be used to determine the base array needed.

Beyond use as a design evaluation tool, this manual can be used as a supplement to the TI library software and the TI CMOS Gate Array Design Manual.

As a supplement to the software library, individual data sheets show the extent of worst-case ranges for the specifications, whereas the functional and simulation models contained in the TI library software include fully expanded, node-by-node specifications. With respect to the completed design, the TI-supplied library software will be used to determine the final design specifications.

As a supplement to the CMOS Gate Array Design Manual, techniques presented in the design manual include explanations of CMOS technology and TGC100 macro characteristics that can simplify the evaluation, selection, and application of macros required for the execution of a custom gate array design.

organization of this manual

SECTION 1 — Introduction. Presents a brief description of the contents of each data manual chapter. Also provides an alphanumeric listing of the TGC100 Series macros, including a cross reference for similar CMOS and TTL functions.

SECTION 2 — Series Data. Provides a brief technology discussion, base arrays offered, packaging options, and family-related specifications.

SECTION 3 — Mechanical Data. Provides drawings with dimensions and descriptive material for the packages offered in the TGC100 family.

SECTION 4 — Definitions and Ratings. Details the methodologies used in the characterization of functional and parametric ratings. Also defines abbreviations and terms.

SECTION 5 — Library Summary. Contains a complete listing of the macros available in the software library and summarizes key specifications portraying the performance of the functions offered. Also provides basic cell requirements for each of the macros.

SECTION 6 through 19 — Macro Data Sheets. Contain the description, electrical, and switching characteristics for each individual macro available in the library. The data sheets are grouped under the following tabs:

6. SPECIAL FUNCTIONS
7. BUFFERS/DRIVERS (Internal)
8. GATES
9. FLIP-FLOPS/LATCHES
10. CLOCK DRIVERS/GENERATORS/OSCILLATORS
11. INPUT BUFFERS
12. BIDIRECTIONAL (I/O) BUFFERS
13. OUTPUT BUFFERS
14. ARITHMETIC FUNCTIONS
15. COUNTERS
16. DEMULTIPLEXERS
17. MULTIPLEXERS
18. REGISTERS
19. REGISTER FILES

Each tabbed section is preceded by a functional selection guide or general information related to that group of data sheets.

ALPHANUMERIC CROSS-REFERENCE INDEX

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IOs and IPs do not occupy basic-cell locations.

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MACRO NAME	SIMILAR TO	CELLS USED	PAGE
IPI01LJ		–	11-4
IPI04LJ		–	11-5
IPI06LJ		–	11-6
IPI09LJ		–	11-8
IPL01LJ		–	11-9
IPL04LJ		–	11-10
IPU01LJ		–	11-11
IPU04LJ		–	11-12
IV110LJ	'7404	1	7-5
IV120LJ	'7404	1	7-6
IV140LJ	'7404	2	7-7
IV211LJ		2	7-8
IV221LJ		4	7-10
IV241LJ		5	7-12
JKB20LJ	'74109	12	9-29
JKB21LJ		12	9-31
LAB20LJ	'74279	4	9-33
LAH12LJ		5	9-35
LAH13LJ		5	9-37
LAH14LJ		7	9-39
LAH20LJ		5	9-41
LAH22LJ	'74116	4	9-43
LH110LJ		4	9-45
LH400LJ	'7475	11	9-46
MU111LJ	'74157	3	17-3
MU220LJ	'74153	7	17-4
MU311LJ	'75151	13	17-6
NA210LJ	'7400	1	8-28
NA220LJ	'7400	2	8-29
NA310LJ	'7410	2	8-30
NA311LJ		2	8-31
NA320LJ	'7410	3	8-32
NA410LJ	'7420	2	8-33
NA420LJ	'7420	4	8-34
NA510LJ		3	8-35
NA520LJ		5	8-36
NA810LJ	'7430	6	8-37
NA820LJ	'7430	6	8-38
NO210LJ	'7402	1	8-39
NO220LJ	'7402	2	8-40
NO310LJ	'7427	2	8-41
NO320LJ	'7427	3	8-42
NO410LJ	'4002	4	8-43
NO420LJ	'4002	4	8-44
NO510LJ	'74260	4	8-45
NO520LJ	'74260	5	8-46
NO810LJ	'4078	6	8-47
NO820LJ	'4078	6	8-49
OA220LJ		3	8-51
OA231LJ		3	8-52
OA241LJ		4	8-53
OPIA0LJ		–	13-3
OPIH0LJ		–	13-5
OPIJ0LJ		–	13-7
OPI20LJ		–	13-9
OPI21LJ		–	13-11
OPI23LJ		–	13-13
OPI24LJ		–	13-16
OPI40LJ		–	13-18
OPI41LJ		–	13-20
OPI43LJ		–	13-22
OPI44LJ		–	13-25
OPI80LJ		–	13-27
OPI81LJ		–	13-29
OPI83LJ		–	13-31
OPI84LJ		–	13-34
OPKA0LJ		–	13-36
OPKH0LJ		–	13-38
OPKJ0LJ		–	13-40
OPK20LJ		–	13-42
OPK21LJ		–	13-44
OPK23LJ		–	13-46
OPK24LJ		–	13-49
OPK40LJ		–	13-51
OPK41LJ		–	13-53
OPK43LJ		–	13-55
OPK44LJ		–	13-58
OPK80LJ		–	13-60
OPK81LJ		–	13-62
OPK83LJ		–	13-64
OPK84LJ		–	13-67
OR210LJ	'7432	2	8-54
OR220LJ	'7432	2	8-55
OR310LJ	'4075	2	8-56
OR320LJ	'4075	3	8-57
OR410LJ	'4072	3	8-58

IOs and IPs do not occupy basic-cell locations.
OPs and OSs do not occupy basic-cell locations.

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MACRO NAME	SIMILAR TO	CELLS USED	PAGE
OR420LJ	'4072	3	8-59
OR510LJ		4	8-60
OR810LJ		5	8-61
OSI11LJ		–	10-15
OSI12LJ		–	10-17
OSI13LJ		–	10-19
OSI14LJ		–	10-21
RF400LJ		418	19-5
RF402LJ		462	19-8
R2401LJ		26	18-3
R2402LJ		27	18-5
R2403LJ		27	18-7
R2404LJ		31	18-9
R2405LJ		26	18-11
R2406LJ		28	18-13
S085LJ	'7485	58	14-5
S138LJ	'74138	25	16-4
S139LJ	'74139	26	16-7
S150LJ	'74150	123	17-8
S151LJ	'74151	40	17-12
S153LJ	'74153	26	17-16
S157LJ	'74157	18	17-19
S161ALJ	'74161A	79	15-3
S163ALJ	'74163A	81	15-8
S164LJ	74164	88	18-15
S165ALJ	'74165A	124	18-19
S173LJ	'74173	53	9-90
S175LJ	'74175	31	9-94
S180XLJ	'74180	21	14-9
S181LJ	'74181	125	14-11
S182LJ	'74182	35	14-18
S191LJ	'74191	98	15-13
S193LJ	'74193	87	15-19
S194ALJ	'74194A	73	18-23
S244LJ	'74244	28	7-14
S273LJ	'74273	55	9-97
S283LJ	'74283	69	14-22
S373LJ	'74373	47	9-103
S374LJ	'74374	76	9-100
S375LJ	'74375	16	9-107
S686LJ	'74686	104	14-26
S688LJ	'74688	32	14-30
TAB20LJ		9	9-48
TDB10LJ		10	9-50
TDC11LJ		10	9-56
TDN11LJ		8	9-63
TDN12LJ		9	9-69
TDN13LJ		12	9-76
TDN22LJ		11	9-83
TO010LJ		2	6-5

OPs and OSs do not occupy basic-cell locations.

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This cross-reference index lists TTL/CMOS device types and shows the equivalent and/or similar TGC100 Series macro type for each. The functions shown are intended for internal macros utilized as the core-logic of a 5-V CMOS ASIC custom design. As such, the bus-driver functions referenced are for driving on-chip buses. A subset macro may require multiple macros of that type or other macro types to achieve a replacement function. A superset macro contains either multiples of or additional circuitry when compared to the referenced TTL/CMOS type.

TTL/CMOS TYPE	SEE NOTE	MACRO TYPE
4000	(1)	NO310LJ
4000	(1)	NO320LJ
4001	(1)	NO210LJ
4001	(1)	NO220LJ
4002	(1)	NO410LJ
4002	(1)	NO420LJ
4011	(1)	NA210LJ
4011	(1)	NA220LJ
4012	(1)	NA410LJ
4012	(1)	NA420LJ
4013	(1)	DFB20LJ
4013	(1)	DTB10LJ
4015	(2)	R2401LJ
4023	(1)	NA310LJ
4023	(1)	NA320LJ
4023	(1)	NA340LJ
4027	(2)	JKB20LJ
4030	(1)	EX210LJ
4030	(1)	EX220LJ
4044	(1)	LAB20LJ
4063		S085LJ
4068	(1)	NA810LJ
4068	(1)	NA820LJ
4069	(1)	IV140LJ
4070	(1)	EX210LJ
4070	(1)	EX220LJ
4071	(1)	OR210LJ
4071	(1)	OR220LJ
4072	(1)	OR410LJ
4072	(1)	OR420LJ
4073	(1)	AN310LJ
4073	(1)	AN320LJ
4075	(1)	OR310LJ
4075	(1)	OR320LJ
4076		S173LJ
4077	(1)	EN210LJ
4078		NO810LJ
4078		NO820LJ
4081	(1)	AN210LJ
4081	(1)	AN220LJ
4082	(1)	AN410LJ
4082	(1)	AN420LJ
4085	(1)	AO221LJ
4095	(1)	JKB20LJ
4512	(2)	MU311LJ
4520		S161ALJ
4520	(2)	S163ALJ
4539	(1)	MU220LJ
4585		S085LJ
7266	(1)	EN210LJ
40104	(2)	S194ALJ
40181		S181LJ
40193		S193LJ
'00	(1)	NA210LJ
'00	(1)	NA220LJ
'02	(1)	NO210LJ
'02	(1)	NO220LJ
'04	(1)	IV110LJ
'04	(1)	IV120LJ
'04	(1)	IV140LJ
'08	(1)	AN210LJ
'08	(1)	AN220LJ
'10	(1)	NA310LJ
'10	(1)	NA320LJ
'11	(1)	AN310LJ
'11	(1)	AN320LJ
'14	(2)	IPI09LJ
'20	(1)	NA410LJ
'20	(1)	NA420LJ
'21	(1)	AN410LJ

NOTES: 1. Macro is a subset of the referenced function.
2. Macro is similar to a subset of the referenced function.

CMOS/TTL-TO-GATE ARRAY MACRO CROSS-REFERENCE INDEX

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TTL/CMOS TYPE	SEE NOTE	MACRO TYPE
'21	(1)	AN420LJ
'27	(1)	NO310LJ
'27	(1)	NO320LJ
'30		AN810LJ
'30	(1)	NA810LJ
'30	(1)	NA820LJ
'32	(1)	OR210LJ
'32	(1)	OR220LJ
'40	(1)	NA420LJ
'50	(2)	AO220LJ
'51	(3)	AO421LJ
'S51	(1)	AO221LJ
'58	(3)	AO320LJ
'74	(1)	DFB20LJ
'74	(1)	DTB10LJ
'75	(1)	LAH20LJ
'85		S085LJ
'86	(1)	EX210LJ
'86	(1)	EX220LJ
'94	(1)	R2403LJ
'94	(1)	R2404LJ
'109	(1)	JKB20LJ
'138		S138LJ
'139		S139LJ
'139	(1)	DE210LJ
'150		S150LJ
'151		S151LJ
'153		S153LJ
'155	(1)	DE210LJ
'157		S157LJ
'157	(1)	MU111LJ
'161A		S161ALJ
'163A		S163ALJ
'164		S164LJ
'165A		S165ALJ
'173		S173LJ
'174	(1)	R2405LJ
'175		R2406LJ
'175		S175LJ
'181		S181LJ
'182		S182LJ
'191		S191LJ
'193		S193LJ
'194A		S194ALJ
'244		S244LJ
'266	(1)	EN210LJ
'273		S273LJ
'373		S373LJ
'374		S374LJ
'375		S375LJ
'468	(1)	IV211LJ
'468	(1)	IV221LJ
'468	(1)	IV241LJ
'670	(4)	RF400LJ
'670	(4)	RF402LJ
'686		S686LJ
'688		S688LJ

NOTES: 1. Macro is a subset of the referenced function.
2. Macro is similar to a subset of the referenced function.
3. Macro is a subset of the referenced function but may contain additional inputs.
4. Macro is a superset to the referenced function.

2

TGC100 Series Data

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- **Six Arrays with Up to 16,758 Useable Gates**
- **Fast Prototype Turn-Around Time**
- **Extensive Design Support, Including:**
  - **Design Libraries Compatible with Daisy and Mentor CAE Systems**
  - **TI Regional ASIC Design Centers**
  - **TI ASIC Distributor Design Centers**
- **222 Macros in Library, Including:**
  - **Register Files, Oscillators**
  - **Scan Flip-Flops/Latches**
  - **Clock Distribution Macros**
- **TGC100 1-μm CMOS EPIC™ Process Features:**
  - **Double-Level Metal, Silicided-Poly**
  - **Typical Gate Delay 500 ps (FO = 3)**
  - **Flip-Flop Toggle Rates Up to 208 MHz**
  - **ESD and Latch-Up Protected I/Os**
  - **Outputs with Up to 20-mA Sink Current**
  - **di/dt Controlled or Full-Speed Outputs**

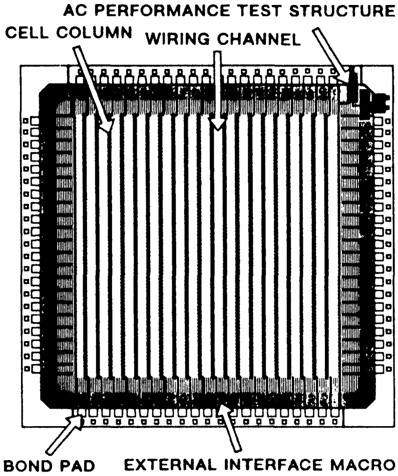

FIGURE 2-1. TGC103 CMOS GATE ARRAY

description

The Texas Instruments TGC100 Series comprises six gate arrays, each fabricated using TI's 1-μm advanced silicon-gate CMOS EPIC™ process. The process features two levels of copper-doped-aluminum metallization for interconnect. Silicided polysilicon gate, source, and drain elements further reduce internal resistance and enhance performance. N-channel and P-channel gate lengths are patterned at 1 μm. The six gate array types, with their basic-cell and bond-pad configurations and production packages, are shown below in Table 2-1 and Table 2-2:

TABLE 2-1. TGC100 GATE ARRAY SUMMARY

GATE ARRAY TYPE	BASIC CELLS 2-INPUT GATES		BOND PADS
	TOTAL AVAILABLE	MAXIMUM USABLE	
TGC103	3200	2880	84
TGC105	5376	4838	118
TGC108	8896	8006	142
TGC112	12654	11389	196
TGC115	15580	14022	216
TGC118	18620	16758	216

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TABLE 2-2. TGC100 GATE CONFIGURATION DESCRIPTIONS

GATE ARRAY TYPE	PRODUCTION PACKAGES															
	PLASTIC DIP		PLASTIC LEADED CHIP CARRIER				PLASTIC QUAD FLAT (QFP) (see Note 1)				PLASTIC OR CERAMIC PIN-GRID ARRAY					
	28	40	28	44	68	84	100	120	132	160	100	120	132	144	180	208
TGC103	✓	✓	✓	✓	✓	✓					✓					
TGC105	✓	✓		✓	✓	✓	✓ ●	●			✓	✓				
TGC108	✓	✓		✓	✓	✓	✓ ●	●	✓		✓	✓	✓	✓		
TGC112					✓	✓		●	✓	●	✓	✓	✓	✓	✓	
TGC115								●	✓	●			✓	✓	✓	✓
TGC118								●	✓	●			✓	✓	✓	✓

NOTE 1: For the quad-flat packages (QFP), ✓ = JEDEC and ● = EIAJ

The basic structure of the TGC100 Series 1-μm CMOS gate arrays consists of basic-cell columns separated by wiring channels and a perimeter of external interface macros that are configurable as inputs, outputs, bidirectional I/Os, oscillators, or power pins. Each 4-transistor internal basic cell is equivalent to a 2-input NAND gate.

Each base array in the TGC100 Series incorporates an ac-performance test structure embedded in an otherwise unused corner of the array. Although not user accessible from the I/O bond pads, this test structure is activated by TI during the wafer-probe stage of device fabrication. Measurements are made to verify that the ac performance of the finished gate array falls within the normal production range. For most applications, this ac performance verification, in conjunction with the standard 1-MHz functional testing and dc parametric testing, is sufficient to ensure correct device operation and performance.

library functions

The TGC100 Series gate array library includes basic gates, buffers, flip-flops, latches, registers, and MSI macros. Of the 222 macros offered, 195 are hardwired and 27 are software macros. The hardwired macros provide a broad selection of predesigned, fully characterized functions. The software macros provide popular TTL/CMOS-type MSI functions which can be used as supplied or modified at the workstation to suit design requirements. Additional user-defined software macros can be created using the TGC100 library macros. Library release 2.0 contains the following classes of macros:

— 2 Hardwired MegaModule™ Register Files and 27 MSI Software Macros
— 39 Registers, Scan Flip-Flops/Latches, Delay Elements, and Oscillators
— 75 Gate, Bus Buffer, and Macro Building Blocks
— 79 External Input, Output, and Bidirectional Buffer Macros

A workstation library summary, showing essential performance data and basic-cell utilization, is included in Section 5. A complete TGC100 Series Design Kit, supplied for the Daisy or Mentor CAE Systems, includes the following:

- TGC100 Series Data Manual
- CMOS Gate Array Design Manual
- Design Support Software User's Manual
- TGC100 Series Design Library.

The Design Kit is arranged to accommodate new material as it is issued.

design flow

User-defined semicustom integrated circuits, designed using TI's TGC100 Series Macro Function Library in conjunction with Daisy or Mentor CAE Systems, can be simulated and verified prior to creating the design database files. The database files generated are used to create the photomask tooling for fabrication. These files are also used by the test programs required for acceptance of the user-defined gate array prototypes. Figure 2-2 provides an overview of the design flow. Gate array designs can be migrated easily to TI standard cell designs, if desired.

prototype and production

The standard TGC100 Series nonrecurring engineering (NRE) charge and prototype cycle time quotation includes the following products and services:

- Initial Design Review
- Generation of Design Specification
- Preparation of Development Contract
- Design Layout (macro placement and routing)
- Post-Layout QC
- Delivery of Post-Layout Delay Files (back annotation)
- Photomask Tooling
- Fabrication, Assembly, and Test of Prototypes
- Delivery of Five (5) Prototypes (see Notes 2 and 3)

NOTES: 2. Prototypes are assembled in packages that are socket- and footprint-compatible with the package chosen for production units.
3. Prototypes are tested for functionality using customer-supplied test patterns at $f = 1$ MHz, $V_{CC} = 5$ V, and $T_A = 25°C$.

prototype and production testing

Table 2-3 enumerates the standard testing that is performed on TGC100 Series products. The wafer probe tests use the 1-MHz test description language (TDL) pattern set and include testing the ac performance of the die by exercising the ac-performance test structure. Specified logic-level thresholds are utilized to test output voltage (V_{OH}, V_{OL}), off-state output current (I_{OZ}), quiescent supply current (I_{CC}), and input current (I_{IL}, I_{IH}).

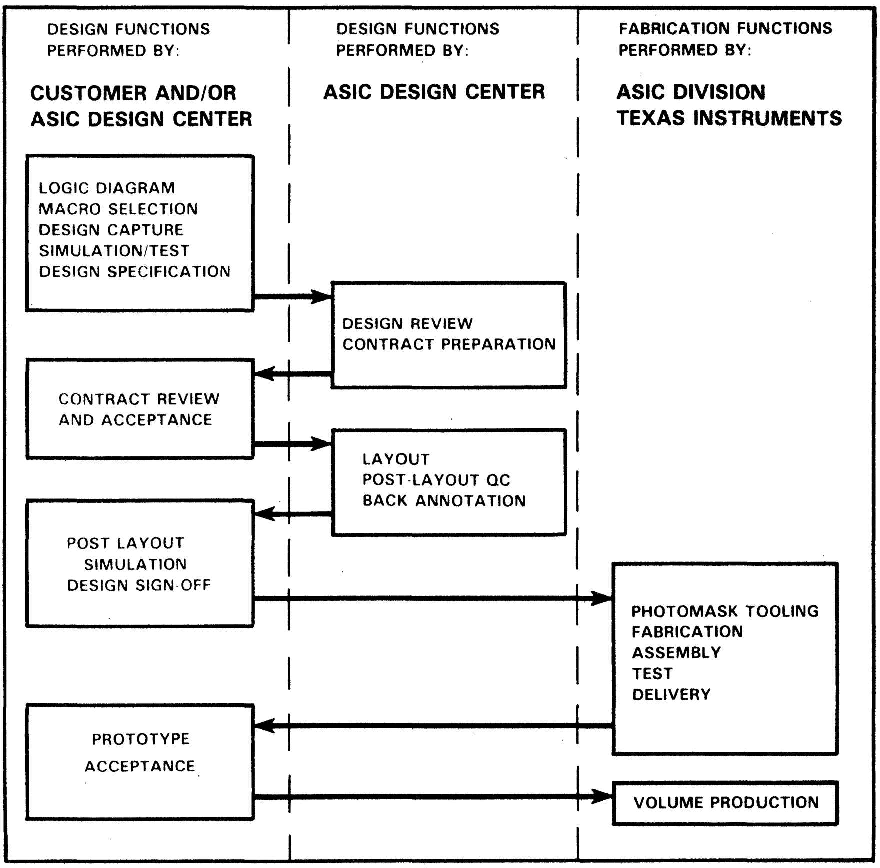

FIGURE 2-2. TGC100 SERIES DESIGN FLOW OVERVIEW

TABLE 2-3. TGC100 SERIES STANDARD TESTING REQUIREMENTS

1-MHz TEST DESCRIPTION LANGUAGE (TDL) PATTERN SET	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE		DC PARAMETRICS TESTED	AC TEST STRUCTURE PROBE
	4.5 V	5 V	5.5 V	25°C	70°C		
Prototype unit tests		✓		✓			
Production wafer probe tests	✓	✓	✓	✓		✓	✓
Production unit tests	✓	✓	✓		✓	✓	

options for prototype and production units

In addition to the standard TGC100 Series product and services previously outlined, the following options may be selected (at additional cost and cycle time):

- Additional Prototypes
- Additional 1-MHz Test Vectors
- Prototype Devices Tested Over Temperature and V_{CC} Range Plus DC Parametrics
- Critical-Path Delay Measurements (pin-to-pin)
- ''At-Speed'' Test Vectors
- Nonstandard V_{CC} and Ground Pin Locations
- Operating Temperature Range Other Than 0°C to 70°C

For a quotation or further details of available options, please contact your local TI Sales Office or TI Authorized ASIC Distributor.

macro function names

The logic function implemented by each of the TGC100 Series gate array macro functions is indicated by the macro name prefix. An index to the macro name prefixes is shown in Table 2-4. Each standard cell is further specified, as shown in the example, using the data in Table 2-5.

EXAMPLE ⟶ AN 2 1 0 LJ

FUNCTION PREFIX (AN = AND gate, see Table 2-4)

NUMBER OF INPUTS (2) (Except AOs,BFs,BU2s,Ds,Gs,IOs,IV2s,JKs, LAs,MUs,OPs,PDs,PRs,Rs,Ss, and Ts. See Table 2-4)

DRIVE LEVEL (1X) Except IOs,IPs, and OPs)

NUMERICAL SEQUENCE (Except IOs, IPs, and OPs)

TECHNOLOGY: LJ = 1-μm CMOS

TABLE 2-4. INDEX TO MACRO FUNCTION PREFIXES

AD	Adder	LA	D-Type and S-R Latches
AN	AND Gates	LH	Latches
AO	AND-OR Gates	MU	Multiplexers
BF	Multi-stage AND, NAND, NOR, OR Gates	NA	NAND Gates
BU	Buffers	NO	NOR Gates
CK	Clock Generator/Drivers	OA	AND/OR Gates
DE	Decoders/Demultiplexers	OP	Output Buffers
DF/DT	D-Type Flip-Flops	OR	OR Gates
DL	Delay Line Elements	OS	Oscillators
EN	Exclusive-NOR Gates	R	Registers
EX	Exclusive-OR Gates	RF	Register Files
IO	Bidirectional I/O Buffers	S	Software Macros
IP	Input Buffers	TA	Toggle Type, Flip-Flops
IV	Inverters	TD	Scan Flip-Flops
JK	J-K Type Flip-Flops	TO	Hi- and Lo-Level Tie-Off Gate

TABLE 2-5. CODING DEFINITIONS FOR FUNCTION PREFIXES

AOs (3rd and 4th characters):
22 = 2-wide, 2-inputs
23 = 3-wide, 2-inputs
24 = 4-wide, 2-inputs
BFs,Gs, and TOs (3rd,4th,5th characters):
Three digit numerical sequence
BUs, and IVs (3rd character):
2 = 3-State output
Ds,JKs,LAs, and TAs (3rd character):
B = Both preset and clear inputs
C = Clear input
P = Preset input
N = Neither preset nor clear input
DEs and MUs (3rd character):
1 = 1 select line (2-wide)
2 = 2 select lines (4-wide)
3 = 3 select lines (8-wide)
IOs,OPs (3rd character):
I = IO or OP without di/dt control
K = IO or OP with di/dt control
L = IO without di/dt and 70-μA pull-up
N = IO with di/dt and 70-μA pull-up

IOs, and OPs (4th character):
A = 16/12-mA sink/source current
H = 12/12-mA sink/source current
J = 20/12-mA sink/source current
2 = 2/2-mA sink/source current
4 = 4/4-mA sink/source current
8 = 8/8-mA sink/source current
IOs, IPs (5th character):
1 = CMOS input
4 = TTL input
6 = CMOS input with hysteresis
9 = TTL input with hysteresis
LA (3rd character):
H = high enable
L = low enable
OPs (5th character):
0 = Totem-pole
1 = N-channel open drain
3 = 3-State
4 = P-channel open drain
Rs and Ss (2nd,3rd,4th,5th characters):
Three or four digit numerical sequence

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I	−0.5 V to V_{CC}
Output voltage range, V_O	−0.5 V to V_{CC}
Input clamp current‡, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current§, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current§, ($V_O = 0$ to V_{CC})	±25 mA
Storage temperature range	−65 °C to 150 °C
Operating free-air temperature range	0 °C to 70 °C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other condition(s) beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
‡ Applies to external input and bidirectional buffers.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage¶	CMOS-compatible inputs	0.7V_{CC}			V
		TTL-compatible inputs	2			
V_{IL}	Low-level input voltage¶	CMOS-compatible inputs			0.2V_{CC}	V
		TTL-compatible inputs			0.8	
V_I	Input voltage¶ #		0		V_{CC}	V
V_{T+}	Positive-going threshold voltage #	CMOS-compatible inputs	0.7V_{CC}			V
		TTL-compatible inputs	2			
V_{T-}	Negative-going threshold voltage #	CMOS-compatible inputs			0.2V_{CC}	V
		TTL-compatible inputs			0.8	
V_{hys}	Hysteresis # ($V_{T+} - V_{T-}$)	CMOS-compatible inputs		1.7		V
		TTL-compatible inputs		0.4		
V_O	Output voltage§		0		V_{CC}	V
I_{OH}	High-level output current§			As specified on data sheets		mA
I_{OL}	Low-level output current§					
t_t	Input transition (rise and fall) times¶		0		25	ns
T_A	Operating temperature range		0		70	°C

§ Applies to external bidirectional and output buffers.
¶ Applies to external input and bidirectional buffers without hysteresis.
# Applies to external input buffers with hysteresis.

TEXAS INSTRUMENTS

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage†	CMOS threshold	I_{OH} = ≤ Rated	3.7			V
		TTL threshold		2.4			
		Outputs without pull-up or -down	$I_{OH} = -20\ \mu A$, See Note 4	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage‡	CMOS threshold	I_{OL} = ≤ Rated			0.5	V
		TTL threshold				0.5	
		Outputs without pull-up or -down	$I_{OL} = 20\ \mu A$, See Note 4			0.1	
I_{CC}	Supply current	TGC103	$V_I = V_{CC}$ or 0, See Note 5			325	µA
		TGC105				450	
		TGC108				550	
		TGC112				750	
		TGC115				850	
		TGC118				900	

† Not applicable for N-channel open-drain output buffers.
‡ Not applicable for P-channel open-drain output buffers.

NOTES: 4. These limits apply when all other outputs are open.
5. For external inputs and bidirectional I/O buffers with pull-up source $V_I = V_{CC}$ and for external inputs and bidirectional I/O buffers with pull-down source $V_I = 0$.

input, output, and bidirectional buffers

The TGC100 Series library contains a wide selection of input, output, and bidirectional buffers that facilitate design optimization. The buffers include versions having active pull-up or pull-down terminators, and N-channel and P-channel open-drain buffers.

input buffers

Input buffers are available with CMOS- or TTL-level thresholds that feature inverting and noninverting versions with and without hysteresis. A guide to input buffer selection is shown below.

INPUT BUFFER SELECTION GUIDE

INPUT THRESHOLD	INVERTING/ NONINVERTING	LOGIC TYPE AND OPTIONS	MACRO NAME
CMOS	NONINVERTING	STANDARD	IPI01LJ
		70-μA PULL-UP	IPL01LJ
		70-μA PULL-DOWN	IPU01LJ
	INVERTING	HYSTERESIS	IPI06LJ
		STANDARD	IPI00LJ
TTL	NONINVERTING	STANDARD	IPI04LJ
		70-μA PULL-UP	IPL04LJ
		70-μA PULL-DOWN	IPU04LJ
		HYSTERESIS	IPI09LJ

Additionally, another class of input buffers features 2-pin crystal-controlled oscillator circuits embedded in an input design. A guide to oscillator selection is shown below:

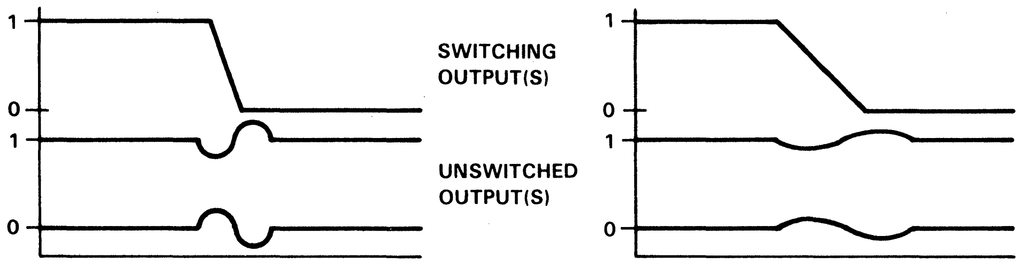
CRYSTAL-CONTROLLED OSCILLATOR SELECTION GUIDE

FREQUENCY	MACRO NAME
55 to 75 MHz	OSI11LJ
35 to 55 MHz	OSI12LJ
20 to 35 MHz	OSI13LJ
1 to 20 MHz	OSI14LJ

Performance specifications are contained in the workstation library summary section of this data sheet and also in Section 10.

di/dt control

The rapid rate of change of current (di/dt) developed during high-speed logic-level transitions of output and bidirectional buffers creates unwanted voltage transients if the gate array is installed in a system having high V_{CC} and/or ground impedances (see Figure 2-3A). To minimize unwanted voltage transients, the TGC100 Series Gate Array library includes output and bidirectional buffers having integral di/dt control (see Figure 2-3B). Full-speed, non-di/dt-controlled versions are also offered for critical paths.



A. WITHOUT di/dt CONTROL   B. WITH di/dt CONTROL

FIGURE 2-3. TYPICAL EFFECTS OF di/dt

When using non-di/dt-controlled output buffers, the following steps minimize the di/dt-related transients and reduce V_{CC} and ground trace impedances.

- Locate non-di/dt-controlled output and bidirectional buffers on low-inductance pins and adjacent to V_{CC} and ground pins.
- Minimize the number of simultaneously switching outputs.
- Increase the number of V_{CC} and ground pins.
- Increase the width of printed-circuit board's V_{CC} and ground traces, or use dedicated V_{CC} and ground planes.

The following selection guide provides data for choosing the correct buffer based on the type of load driven, along with potential V_{CC} and ground pin requirements reduction:

BIDIRECTIONAL AND OUTPUT BUFFER SELECTION GUIDE

APPLICATION (TYPE OF LOAD DRIVEN)				CONSIDER USING BUFFER TYPE		POTENTIAL V_{CC}/GND PIN REDUCTION
CMOS/MOS LS	AC/ACT ALS/S/AS/F	TERMINATED LINES	CRITICAL PATHS	I/Os	OUTPUTS	
●	●	●		IO(K,N,W)XXLJ	OPKXXLJ	45%
	●	●	●	IO(I,L,U)XXLJ	OPIXXLJ	0

Detailed design guidelines on the selection of output and bidirectional buffers and V_{CC} and ground pin requirements are contained in the *CMOS Gate Array Design Manual.*

output and bidirectional I/O characteristics

The high-level and low-level output voltage characteristics of external outputs and bidirectional I/Os are common for all types of macros. Parametric values for the V_{OH} and V_{OL} output voltage levels are included in the electrical characteristics table (page 2-8).

output buffers

Output buffers are available in totem-pole, 3-state, n-channel or p-channel open-drain output configurations with drive current ratings from 2 to 20 mA. Performance specifications are contained in Sections 5 and 13. A guide to output buffer selection is shown below:

OUTPUT BUFFER SELECTION GUIDE
(Each macro is designed for CMOS and TTL loads)

OUTPUT CONFIGURATION (See Note 6)	OUTPUT CURRENT (Source/Sink) (mA)	MACRO NAME (and performance class)	
		WITH di/dt	WITHOUT di/dt
TOTEM-POLE	2/2	OPK20LJ	OPI20LJ
	4/4	OPK40LJ	OPI40LJ
	8/8	OPK80LJ	OPI80LJ
	12/12	OPKH0LJ	OPIH0LJ
	12/16	OPKA0LJ	OPIA0LJ
	12/20	OPKJ0LJ	OPIJ0LJ
OPEN-DRAIN (N-Channel) (See Note 7)	2	OPK21LJ	OPI21LJ
	4	OPK41LJ	OPI41LJ
	8	OPK81LJ	OPI81LJ
OPEN-DRAIN (P-Channel) (See Note 8)	2	OPK24LJ	OPI24LJ
	4	OPK44LJ	OPI44LJ
	8	OPK84LJ	OPI84LJ
3-STATE	2/2	OPK23LJ	OPI23LJ
	4/4	OPK43LJ	OPI43LJ
	8/8	OPK83LJ	OPI83LJ

NOTES: 6. All output buffers are noninverting.
7. N-channel open-drain outputs are for sink current.
8. P-channel open-drain outputs are for source current.

3

Mechanical Data

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mechanical data summary

Electrical characteristics presented in this data manual, unless otherwise noted, apply to gate array macros prior to interconnect routing and packaging. Characteristics and effects of macro layout, routing, and interconnection of a completed ASIC design are covered in the post-layout simulation software. The capacitive loading effects of the package bond wire(s) and terminal(s) are assumed to be a portion of the 15-pF or 50-pF switching-characteristics load shown for the output and I/O cells. Typically, the packaging bond wire and terminal capacitance values range from 1 to 2 pF. Consult TI's design-center personnel and the *CMOS Gate Array Design Manual* for further assistance in choosing and specifying ASIC packaging options.

package selection

The following classes of conventional through-hole and surface-mount packages are recommended for ASIC designs:

- Dual-in-line (DIP) and plastic (N)
- Leaded chip carrier (PLCC), plastic (FN)
- Pin-grid-array (PGA), low-cost (GP)
- Quad flatpack, JEDEC plastic (PQ), EIAJ plastic (PB,PC,PJ).

TI will review and consider supplying package requirements other than those listed.

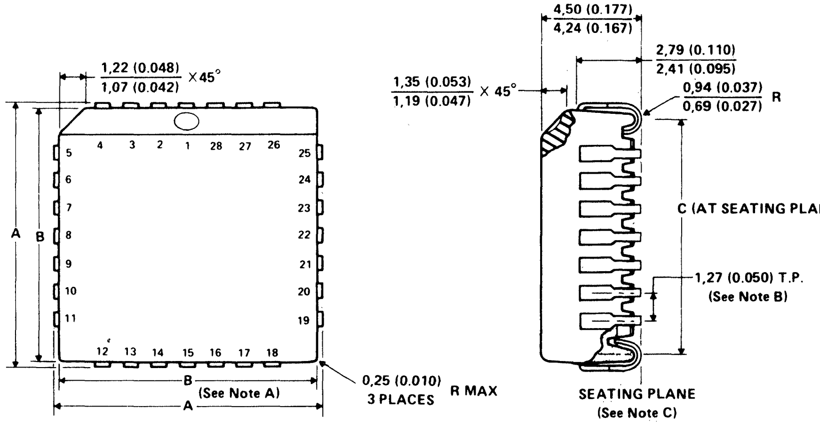
ordering instructions

Implementing semiconductor solutions using TGC100 components normally results in an application-specific integrated circuit. Total specifications, including packaging and ordering instructions, are developed as a part of the Design Specification. Contact your TI representative for further information on getting started with an ASIC design.

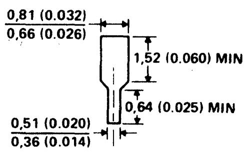
FN plastic chip carrier package

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN PLASTIC CHIP CARRIER
(28-terminal package used for illustration)



JEDEC OUTLINE	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
MO-047AB	28	12,32 (0.485)	12,57 (0.495)	11.43 (0.450)	11,58 (0.456)	10,41 (0.410)	10,92 (0.430)
MO-047AC	44	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,49 (0.610)	16,00 (0.630)
MO-047AE	68	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.956)	23,11 (0.910)	23.62 (0.930)
MO-047AF	84	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)



LEAD DETAIL

All dimensions and notes for the specified JEDEC outline apply.

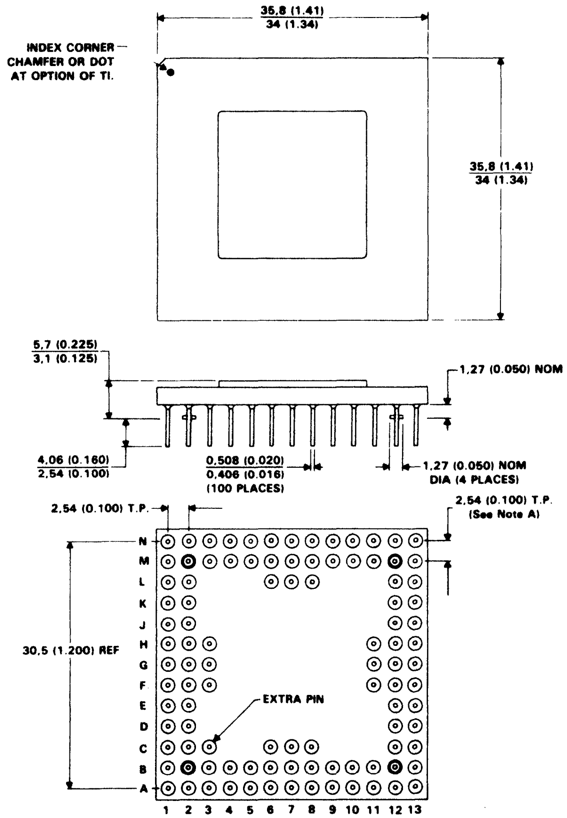
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. The centerline of the center pin on each side is within 0,10 (0.004) of the package centerline as determined by dimension B.
B. The location of each pin is within 0,127 (0.005) of its true position with respect to the center pin on each side.
C. The lead contact points are planar within 0,10 (0.004).

GP pin-grid-array plastic package

This plastic pin-grid-array package consists of a high-temperature epoxy circuit board that positions and supports the package terminals, interconnections, bond pads, and metallized cavity. The conductively mounted die, bonding wires, and pads are enclosed within a moisture-resistant envelope. The anodized aluminum cover is secured with an epoxy preform. The solder-dipped terminals require no additional cleaning or processing when used in soldered assembly.

100-PIN GP



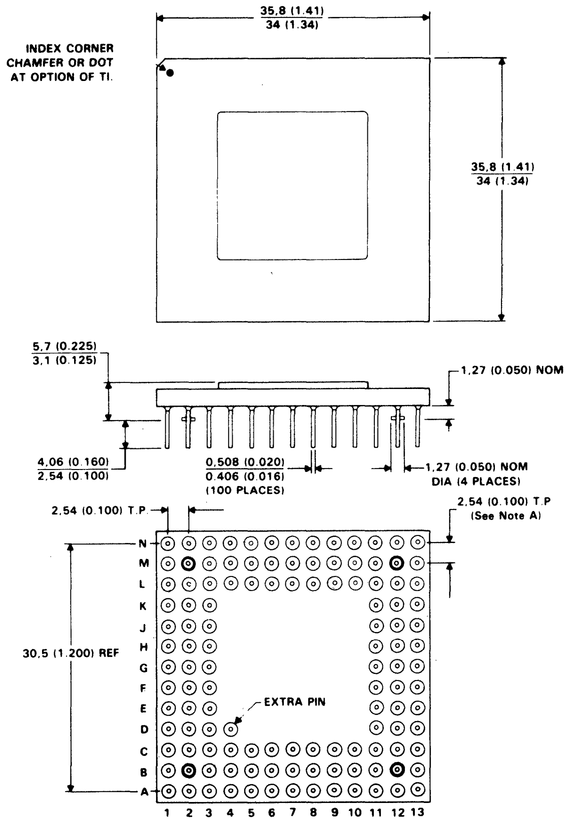
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the plastic.

GP pin-grid-array plastic package

This plastic pin-grid-array package consists of a high-temperature epoxy circuit board that positions and supports the package terminals, interconnections, bond pads, and metallized cavity. The conductively mounted die, bonding wires, and pads are enclosed within a moisture-resistant envelope. The anodized aluminum cover is secured with an epoxy preform. The solder-dipped terminals require no additional cleaning or processing when used in soldered assembly.

120-PIN GP



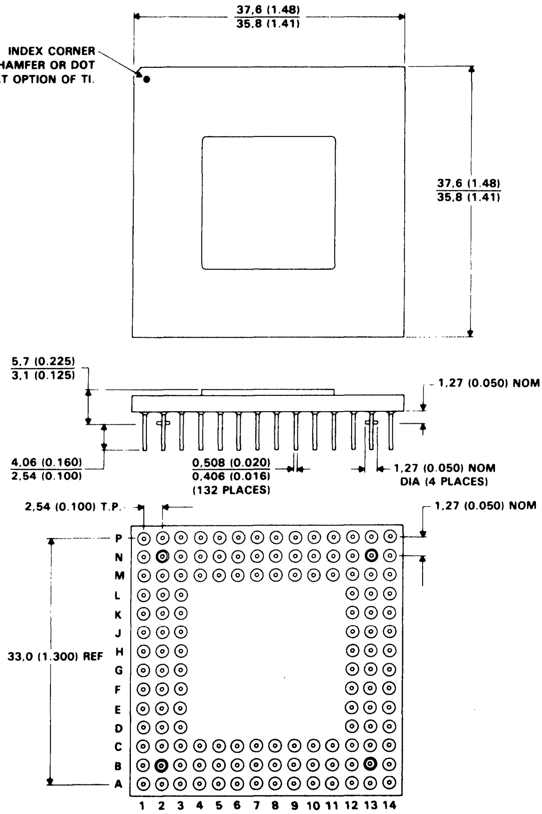
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the plastic.

GP pin-grid-array plastic package

This plastic pin-grid-array package consists of a high-temperature epoxy circuit board that positions and supports the package terminals, interconnections, bond pads, and metallized cavity. The conductively mounted die, bonding wires, and pads are enclosed within a moisture-resistant envelope. The anodized aluminum cover is secured with an epoxy preform. The solder-dipped terminals require no additional cleaning or processing when used in soldered assembly.

132-PIN GP



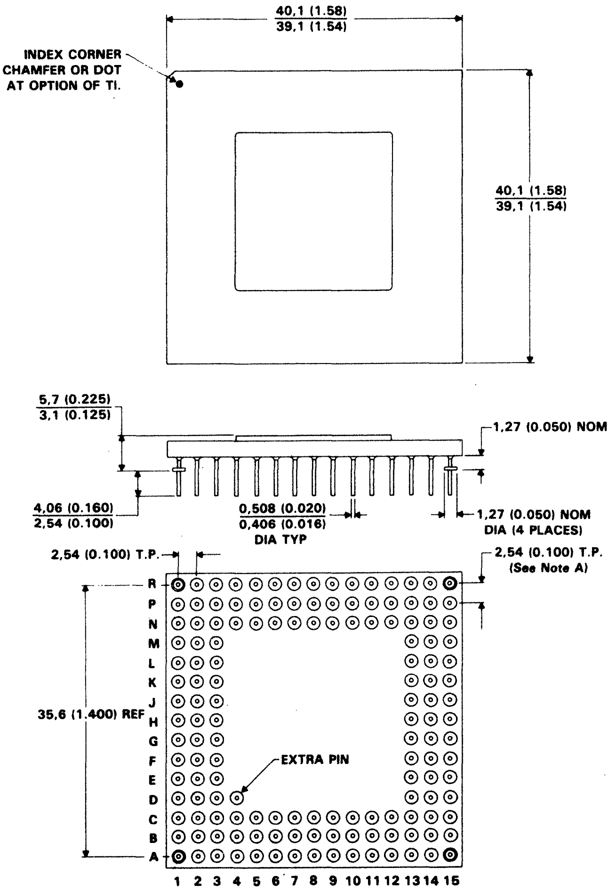
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the plastic.

GP pin-grid-array plastic package

This plastic pin-grid-array package consists of a high-temperature epoxy circuit board that positions and supports the package terminals, interconnections, bond pads, and metallized cavity. The conductively mounted die, bonding wires, and pads are enclosed within a moisture-resistant envelope. The anodized aluminum cover is secured with an epoxy preform. The solder-dipped terminals require no additional cleaning or processing when used in soldered assembly.

144-PIN GP



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the plastic.

GP pin-grid-array plastic package

This plastic pin-grid-array package consists of a high-temperature epoxy circuit board that positions and supports the package terminals, interconnections, bond pads, and metallized cavity. The conductively mounted die, bonding wires, and pads are enclosed within a moisture-resistant envelope. The anodized aluminum cover is secured with an epoxy preform. The solder-dipped terminals require no additional cleaning or processing when used in soldered assembly.

180-PIN GP

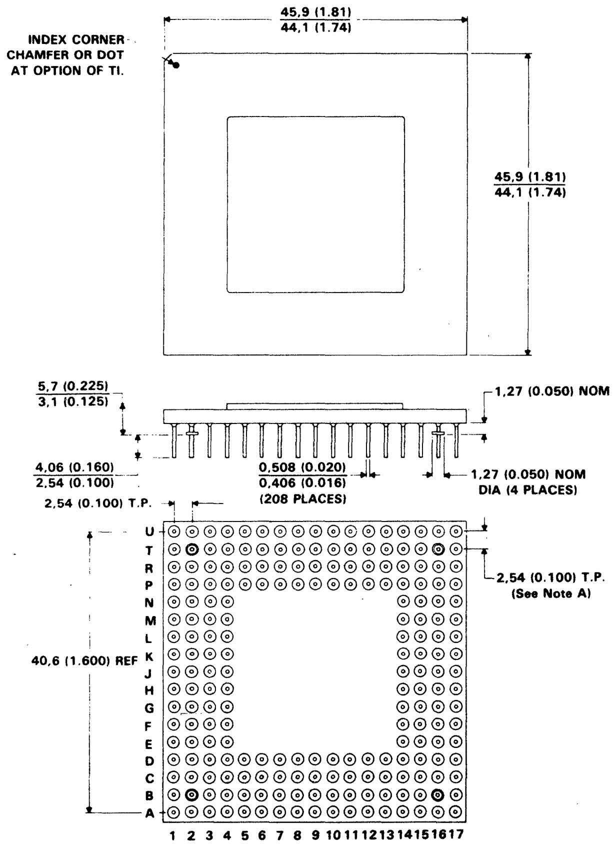
CONTACT ASIC FIELD SALES SPECIALIST
OR
REGIONAL TECHNOLOGY CENTER

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

GP pin-grid-array plastic package

This plastic pin-grid-array package consists of a high-temperature epoxy circuit board that positions and supports the package terminals, interconnections, bond pads, and metallized cavity. The conductively mounted die, bonding wires, and pads are enclosed within a moisture-resistant envelope. The anodized aluminum cover is secured with an epoxy preform. The solder-dipped terminals require no additional cleaning or processing when used in soldered assembly.

208-PIN GP



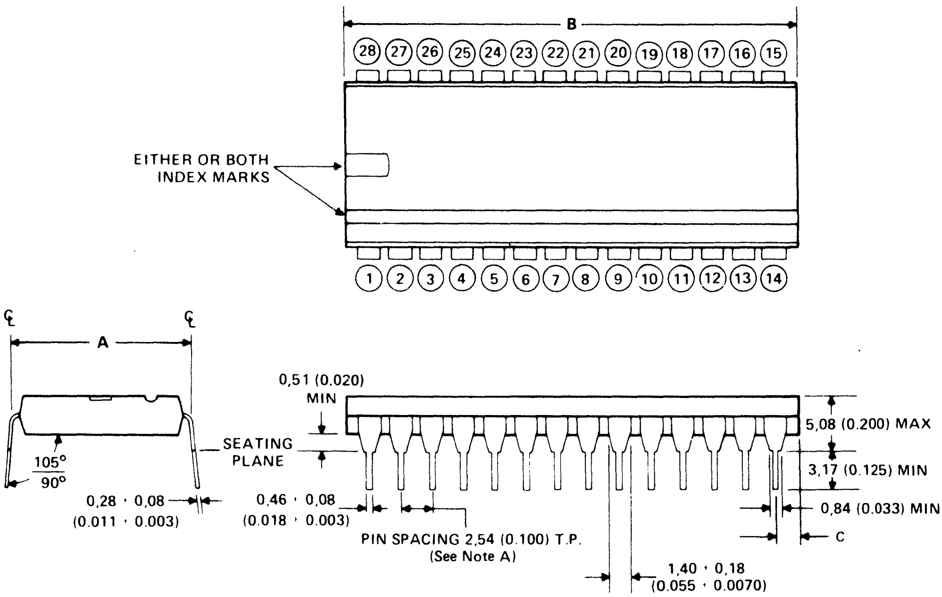
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the plastic.

NW dual-in-line packages

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remaining stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NW PLASTIC
(28-PIN PACKAGE SHOWN)



DIM \ PINS (N)	28	40
A ±0,25 (0.600)	15,24 (0.600)	15,24 (0.600)
B (MAX)	36,6 (1.440)	53,1 (2.090)
C ±0,51 (0.020)	1,27 (0.050)	1,91 (0.075)

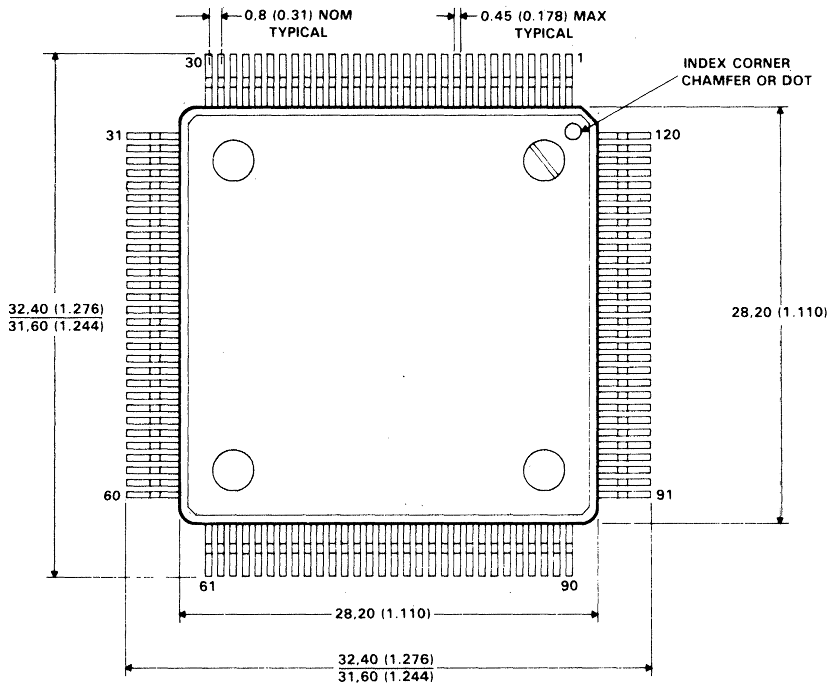
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

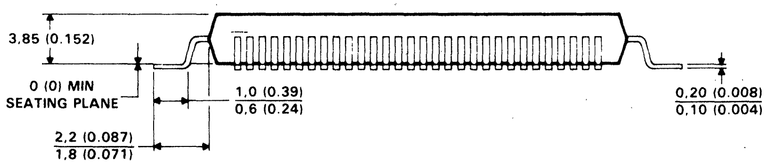
NOTE A: Each pin centerline is located with 0,25 (0.010) of its true longitudinal position.

PB plastic quad flat packages (EIAJ)

This quad flat package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperature with no deformation, and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for surface-mount assembly. The solder-dipped leads require no additional cleaning or processing when used in soldered assembly.

120-PIN PB PLASTIC PACKAGE†





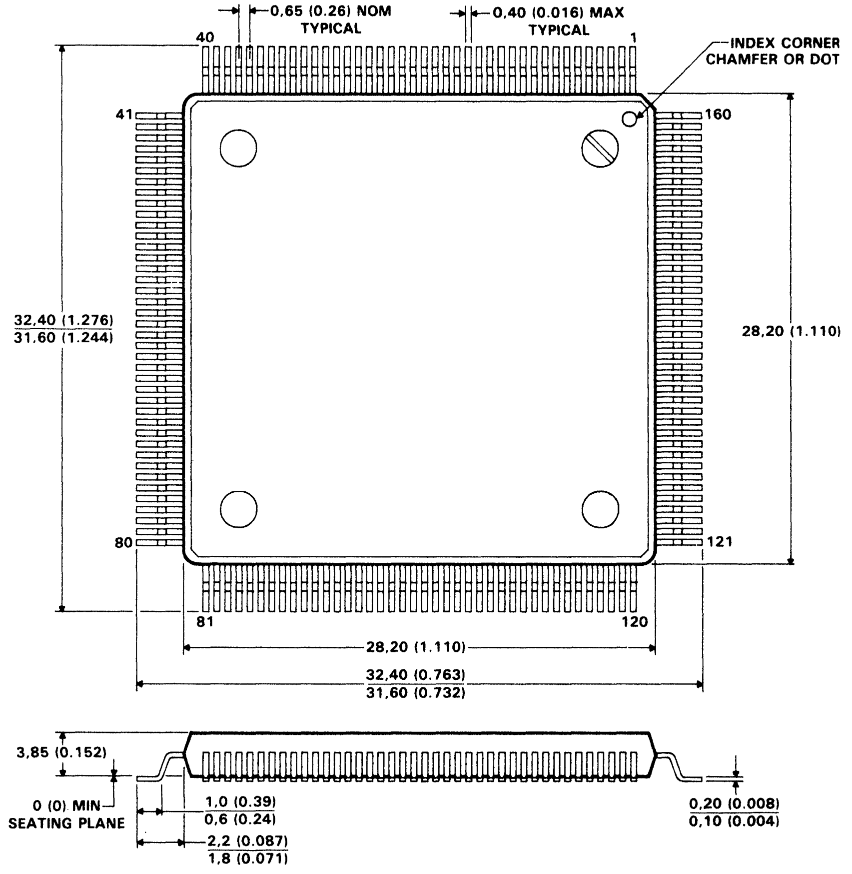
†All dimensions and notes for EIAJ QFP mechanical outline apply.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

PC plastic quad flat packages (EIAJ)

This quad flat package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperature with no deformation, and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for surface-mount assembly. The solder-dipped leads require no additional cleaning or processing when used in soldered assembly.

160-PIN PC PLASTIC PACKAGE†



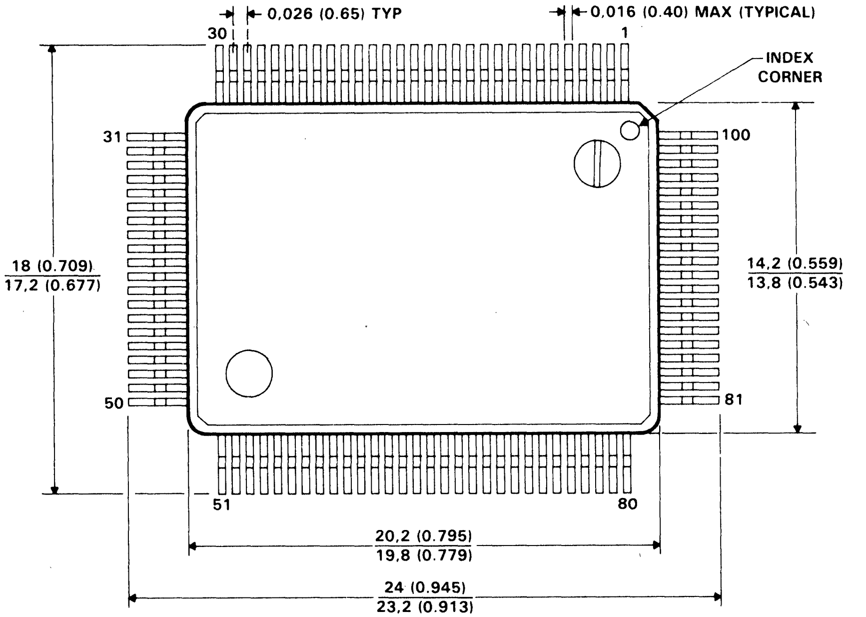
†All dimensions and notes for EIAJ QFP mechanical outline apply.

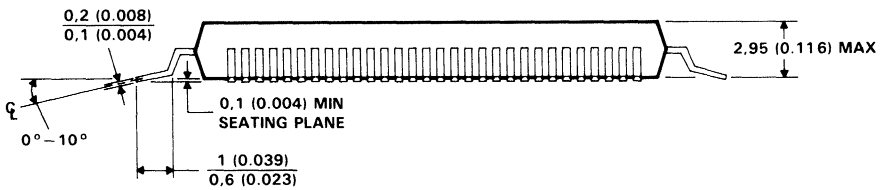
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

PJ plastic quad flat package (EIAJ)

This quad flat package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperature with no deformation, and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for surface-mount assembly. The solder-dipped leads require no additional cleaning or processing when used in soldered assembly.

100-PIN PJ





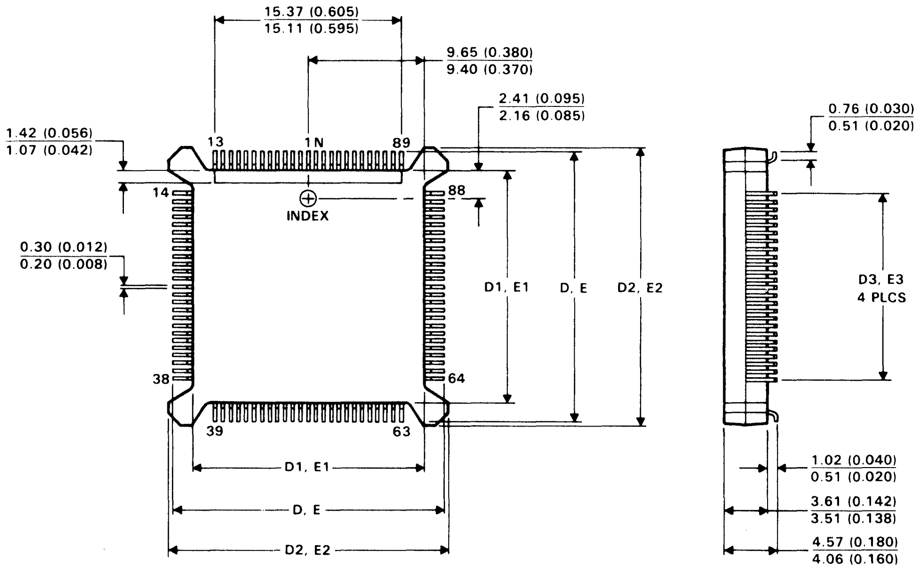
†All dimensions and notes for EIAJ QFP mechanical outline apply.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

PQ plastic quad flat package

This quad flat package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperature with no deformation, and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for surface-mount assembly. The solder-dipped leads require no additional cleaning or processing when used in soldered assembly.

PQ QUAD FLAT PACKAGE
(100-lead package used for illustration)



JEDEC OUTLINE DESIGNATION†

DIMENSION	MO-069AD		MO-069AE	
	MIN	MAX	MIN	MAX
D, E	22,23 (0.875)	22,48 (0.885)	27.31 (1.075)	27,56 (1.085)
D1, E1	18,97 (0.747)	19,13 (0.753)	24,05 (0.947)	24,21 (0.953)
D2, E2	22,78 (0.897)	22,94 (0.903)	27,86 (1.097)	28,02 (1.103)
D3, E3	15,24 (0.6) REF		20,32 (0.8) REF	
N	100		132	

†All dimensions and notes for the specified JEDEC outline apply.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

4

Definitions and Ratings

D3015, OCTOBER 1987—REVISED OCTOBER 1988

This section provides an explanation of function tables, parameter measurement information, and a glossary.

explanation of function tables

Function tables used in this data manual employ symbols to describe the states of input stimuli and the resultant output response. Definitions of the symbols are provided followed by an explanation of how the symbols are used ~~to~~ construct an actual function table. The function table example is a sequential storage macro which includes a description of the relationships between the application of static conditions versus the dynamic inputs. Sufficient detail is included to provide for interpretation of truth tables used in this manual.

parameter measurement information

Test conditions used for measurement of electrical characteristics are provided in the family data sheet or on each individual data sheet. Conditions used for measurement of switching characteristics are shown in this section in the form of load circuits and voltage waveforms. Test points are illustrated schematically on the load circuits and reference points are plotted on the voltage waveforms.

glossary

A glossary in this section defines the symbols, terms, and definitions used in this manual.

The following symbols are now being used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . h	=	the level of steady-state inputs at inputs A through H, respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↑ or ↓
$\sqcap$	=	one high-level pulse
$\sqcup$	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↑ or ↓
?	=	unknown

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains, H, L, and/or X together with ↑ and/or ↓, the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, $\sqcap$ or $\sqcup$, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., S194LJ.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		SLSER	SRSER	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

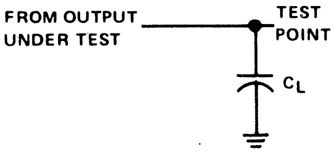
The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of the high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

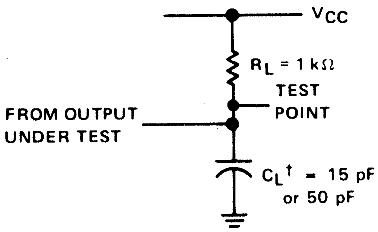


LOAD CIRCUIT

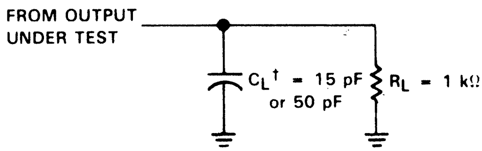
PARAMETER	CELLS	C_L†
t_{pd}	INTERNAL and INPUT	0
t_{pd}	OUTPUTS	15 pF or 50 pF

†C_L includes probe and test fixture capacitance.

FIGURE 1. TOTEM-POLE OUTPUTS



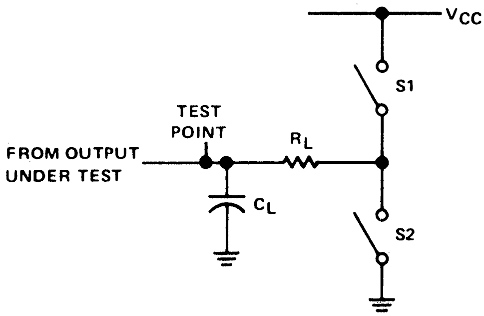
N-CHANNEL LOAD CIRCUIT



P-CHANNEL LOAD CIRCUIT

†C_L includes probe and test fixture capacitance.

FIGURE 2. OPEN-DRAIN OUTPUTS



LOAD CIRCUIT

PARAMETER		INTERNAL BUFFER R_L	INTERNAL BUFFER C_L†	OUTPUT OR I/O R_L	OUTPUT OR I/O C_L†	S1	S2
t_{en}	t_{PZH}	40 kΩ	0 pF	1 kΩ	15 pF or 50 pF	OPEN	CLOSED
	t_{PZL}	20 kΩ				CLOSED	OPEN
t_{dis}	t_{PHZ}	40 kΩ	0 pF	1 kΩ	50 pF	OPEN	CLOSED
	t_{PLZ}	20 kΩ				CLOSED	OPEN
t_{pd}	t_{PLH}	—	0 pF	—	15 pF or 50 pF	OPEN	OPEN
	t_{PHL}						

† C_L includes probe and test fixture capacitance.

FIGURE 3. 3-STATE OUTPUTS

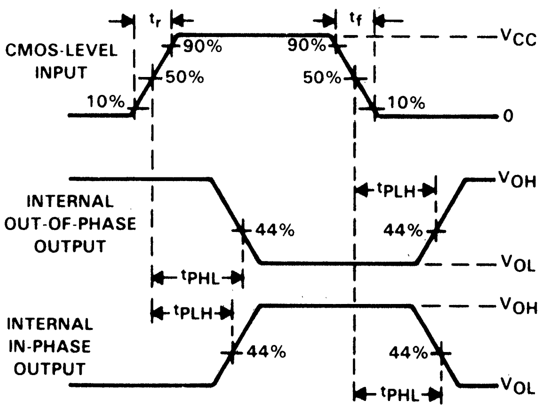


FIGURE 4. CMOS INPUT CELL AND CMOS 3-STATE BIDIRECTIONAL INPUT PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

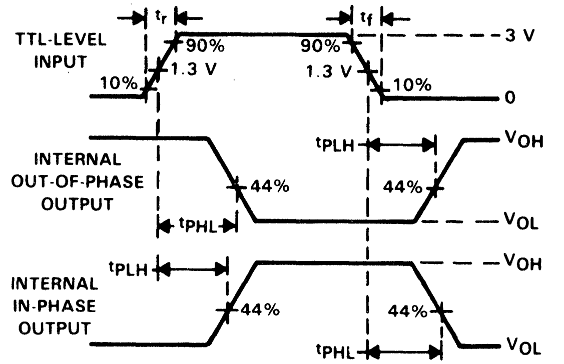


FIGURE 5. TTL INPUT CELL AND TTL 3-STATE BIDIRECTIONAL INPUT PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

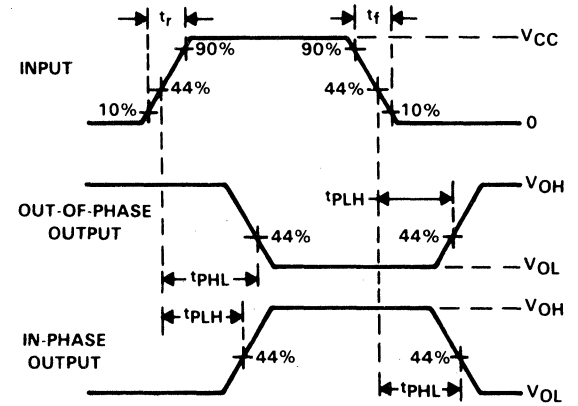


FIGURE 6. INTERNAL TOTEM-POLE OUTPUT PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

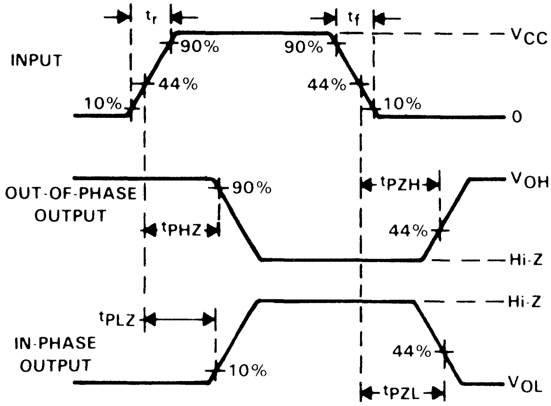


FIGURE 7. INTERNAL 3-STATE OUTPUT BUFFER DISABLE AND ENABLE VOLTAGE WAVEFORMS

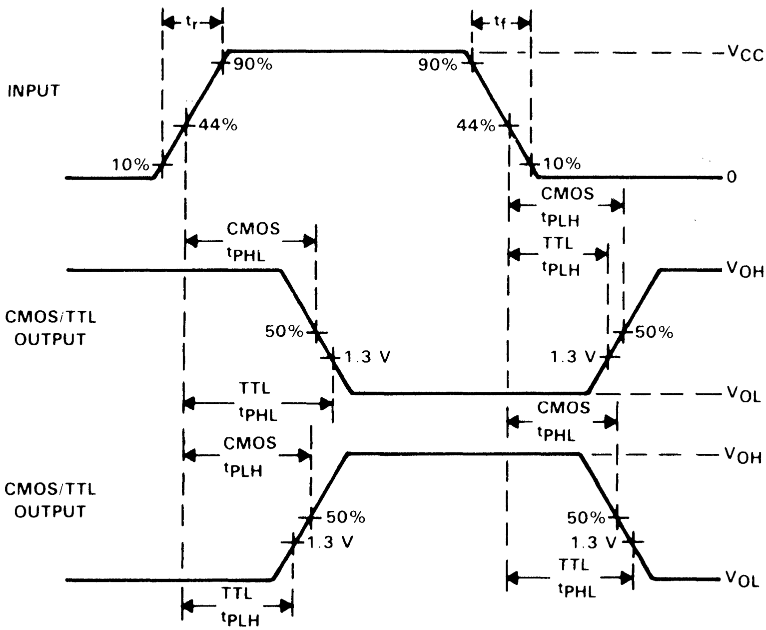


FIGURE 8. CMOS/TTL OUTPUT AND 3-STATE BIDIRECTIONAL INPUT/OUTPUT PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

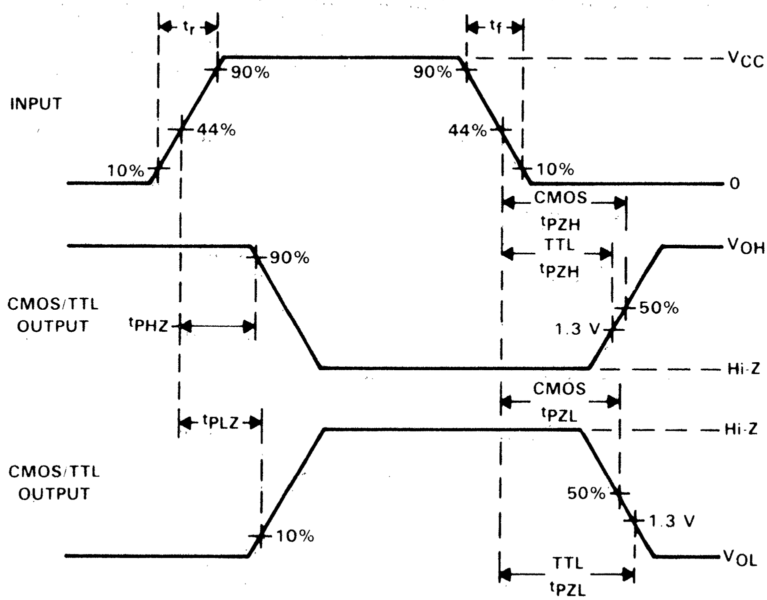


FIGURE 9. CMOS/TTL 3-STATE BIDIRECTIONAL INPUT/OUTPUT DISABLE AND ENABLE VOLTAGE WAVEFORMS

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_{pd} **Power dissipation capacitance**
Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

f_{clock} **Clock frequency**
The rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of the output logic level in accordance with the specification.

f_{opr} **Operating frequency**
The rate at which the inputs of a circuit can be driven through its required sequences while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of the output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OZ} **Off-state (high-impedance-state) output current (of a 3-state output)**
The current flowing into* an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output.

*Current out of a terminal is given as a negative value.

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

V_{T+} **Positive-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} **Negative-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

t_a **Access time**
The time interval between the application of a specified input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a 3-state output)**
The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. $t_{dis} = \frac{t_{PHZ} + t_{PLZ}}{2}$.

t_{en} **Enable time (of a 3-state output)**
The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). $t_{en} = \frac{t_{PZH} + t_{PZL}}{2}$.

t_f **Fall time**
The time interval between two reference points (90% and 10% unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level.

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. $t_{pd} = \frac{t_{PHL} + t_{PLH}}{2}$.

t_{PHL} **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a 3-state output) from high level**
The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a 3-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a 3-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a 3-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to the defined low level.

t_r **Rise time**
The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level.

t_{sr} **Sense recovery time**
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES:
1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_t **Transition time (general)**
The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

Δt_{PHL} **Delta propagation delay time, high-to-low level output**
The change in propagation delay time (t_{PHL}) with load capacitance.

Δt_{PHZ} **Delta disable time (of a 3-state output) from high level**
The change in disable time (t_{PHZ}) with load capacitance.

Δt_{PLH} **Delta propagation delay time, low-to-high level output**
The change in propagation delay time (t_{PLH}) with load capacitance.

Δt_{PLZ} **Delta disable time (of a 3-state output) from low level**
The change in disable time (t_{PLZ}) with load capacitance.

Δt_{PZH} **Delta enable time (of a 3-state output) to high level**
The change in enable time (t_{PZH}) with load capacitance.

Δt_{PZL} **Delta enable time (of a 3-state output) to low level**
The change in enable time (t_{PZL}) with load capacitance.

5

Library Summary

WORKSTATION LIBRARY SUMMARY
1-μm CMOS GATE ARRAYS

D3015, OCTOBER 1987 – REVISED OCTOBER 1988

This section provides summary tables of functionally similar macros from which the designers can select specific functions having the performance criteria that best meet their design requirements. Grouped into functional categories, the summary provides:

- Macro identification (name)
- General description, such as number of inputs, width, size, or scope of the macro
- Output drive of internal macros and output current ratings of outputs and bidirectional I/Os
- The number of basic array cells used by internal macros
- Typical and maximum delay and delta delay times for the primary or data path. Delay times for internal and inut macros are at $C_L = 0$. Delay times for I/Os and outputs are at $C_L = 15$ pF.
- Setup and hold times for the data path input to hardwired sequential functions.

Maximum delay times are the worst-case path or input. The worst-case propagation times for the low-to-high and high-to-low transition may occur in different paths or inputs.

For complete specifications, consult the macro data sheets in the following sections.

D3015, OCTOBER 1987 – REVISED OCTOBER 1988

AND, AND-OR, AND-NOR GATES

FUNCTION HARDWIRED	MACRO NAME	NO. OF INPUTS	OUTPUT DRIVE	CELLS USED		SWITCHING CHARACTERISTICS $C_L = 0$ DELAY TIME t_{PLH} (ns)	t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
AND GATES	AN210LJ	2	1X	2	TYP	0.48	0.54	0.88	0.49
					MAX	0.89	1.07	1.72	0.88
	AN220LJ	2	2X	2	TYP	0.55	0.6	0.44	0.3
					MAX	1.02	1.19	0.88	0.56
	AN310LJ	3	1X	2	TYP	0.65	0.65	0.89	0.5
					MAX	1.33	1.36	1.72	0.94
	AN320LJ	3	2X	3	TYP	0.71	0.67	0.46	0.31
					MAX	1.42	1.43	0.92	0.59
	AN410LJ	4	1X	3	TYP	0.77	0.67	0.9	0.52
					MAX	1.66	1.46	1.76	0.98
	AN420LJ	4	2X	3	TYP	0.87	0.7	0.48	0.33
					MAX	1.86	1.54	0.97	0.65
	AN510LJ	5	1X	3	TYP	0.99	0.74	0.92	0.54
					MAX	2.27	1.67	1.83	1.03
	AN810LJ	8	1X	5	TYP	0.88	0.7	1.69	0.52
					MAX	1.89	1.54	3.41	0.98
AN-OR GATES	AO220LJ	4	2X	3	TYP	0.62	0.97	0.46	0.38
					MAX	1.28	2.35	0.9	0.74
	AO320LJ	6	1X	4	TYP	0.8	1.06	0.89	0.63
					MAX	1.82	2.84	1.78	1.22
AND-NOR GATES	AO221LJ	4	1X	2	TYP	0.5	0.38	1.68	0.75
					MAX	1.25	0.7	3.42	1.5
	AO241LJ	4	2X	6	TYP	1.23	0.92	0.44	0.3
					MAX	3.15	1.95	0.88	0.59
	AO421LJ	8	1X	4	TYP	0.72	0.62	1.67	1.3
					MAX	2.13	1.63	3.43	2.79

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ARITHMETIC FUNCTIONS

FUNCTION ARITHMETIC OPERATORS (SOFTWARE)	MACRO NAME	WIDTH OR SIZE	OUTPUT DRIVE	CELLS USED	SWITCHING CHARACTERISTICS $C_L = 0$	DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
1-BIT FULL	AD100LJ	1-BIT	1X	9	TYP	1.2	1.51	0.89	0.51
ADDER					MAX	2.44	3.27	1.71	0.91
MAGNITUDE	S085LJ	4-BITS	2X	58	TYP	4.6	5.5	0.44	0.32
COMPARATOR					MAX	8.9	10.8	0.84	0.44
PARITY	S180XLJ	8-BITS	1X	21	TYP	3.2	3.1	0.89	0.5
TREE					MAX	6.1	5.9	1.72	0.9
ALU WITH	S181LJ	4-BITS	1X	125	TYP	7.4	6.7	0.88	1.27
LOOK-AHEAD					MAX	13.1	11.7	1.74	2.66
LOOK-AHEAD	S182LJ	4	2X	35	TYP	2.5	2.3	1.68	0.75
CARRY GEN.		STAGES			MAX	4.3	4.1	3.42	1.5
RIPPLE	S283LJ	4-BITS	2X	69	TYP	3.8	3.4	0.44	0.32
ADDER					MAX	6.9	6.5	0.84	0.44
MAGNITUDE	S686LJ	8-BITS	2X	104	TYP	3.2	4.2	0.44	0.64
COMPARATOR					MAX	5.7	7.9	0.9	1.34
IDENTITY	S688LJ	8-BITS	2X	32	TYP	2.5	3.2	0.44	0.32
COMPARATOR					MAX	4.4	6.3	0.84	0.44

D3015, OCTOBER 1987 – REVISED OCTOBER 1988

BOOLEANS, BUFFERS

FUNCTION	MACRO NAME	NO. OF INPUTS	OUTPUT DRIVE	CELLS USED	SWITCHING CHARACTERISTICS $C_L = 0$	DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
HARDWIRED MULTI-STAGE GATES	BF001LJ	3	1X	2	TYP	0.46	0.37	1.67	0.67
					MAX	1.12	0.59	3.4	1.46
	BF006LJ	4	1X	2	TYP	0.6	0.36	2.49	0.64
					MAX	1.77	0.63	5.1	1.53
	BF011LJ	6	1X	3	TYP	0.8	0.42	2.5	0.76
					MAX	2.39	0.77	5.12	1.58
	BF022LJ	6	1X	3	TYP	1.19	0.53	2.49	1.05
					MAX	2.69	1.07	5.1	2.2
	BF051LJ	3	1X	2	TYP	0.49	0.33	1.41	0.73
					MAX	1.07	0.58	3.4	1.48
	BF053LJ	4	1X	2	TYP	0.52	0.38	1.69	0.74
					MAX	1.32	0.69	3.42	1.46
	BF056LJ	4	1X	2	TYP	0.48	0.41	1.28	1
					MAX	1.39	0.86	3.4	2.06
HARDWIRED BUFFER GATES	BU130LJ	1	3X	2	TYP	0.49	0.69	0.28	0.3
					MAX	0.82	1.27	0.58	0.56
	BU150LJ	1	5X	3	TYP	0.57	0.85	0.2	0.26
					MAX	0.99	1.66	0.38	0.47
SOFTWARE W/3-STATE OUTPUTS	S244LJ	1 X 8 BITS 2 EN	1X	28	TYP	1.9	2.5	0.96	0.62
					MAX	2.6	3.2	1.9	1.26

D3015, OCTOBER 1988

CLOCK GENERATOR/DRIVERS

FUNCTION CLOCK GENERATOR DRIVERS HARDWIRED	MACRO NAME	NO. OF INPUTS	OUTPUT DRIVE	CELLS USED	SWITCHING CHARACTERISTICS $C_L = 0$				
						DELAY TIME		DELTA DELAY	
						t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
2-PHASE CLOCK GENERATOR	CK120LJ	1	1X	10	TYP	5.84	1.54	0.55	0.33
					MAX	12.69	3.82	1.14	0.62
USE ON TGC103	CKD03LJ	1	25 pF	40	TYP	1.94	1.95	0.02	0.03
					MAX	3.05	3.12	0.04	0.04
USE ON TGC105	CKD05LJ	1	25 pF	48	TYP	2.18	2.21	0.02	0.02
					MAX	3.44	3.55	0.03	0.03
USE ON TGC108	CKD08LJ	1	25 pF	64	TYP	2.3	2.29	0.01	0.02
					MAX	3.64	3.7	0.02	0.03
USE ON TGC112	CKD12LJ	1	35 pF	74	TYP	2.36	2.41	0.01	0.01
					MAX	3.75	3.87	0.02	0.02
USE ON TGC115	CKD15LJ	1	35 pF	82	TYP	2.45	2.5	0.01	0.01
					MAX	3.88	4.03	0.02	0.02
USE ON TGC118	CKD18LJ	1	35 pF	98	TYP	2.45	2.5	0.01	0.01
					MAX	3.88	4.03	0.02	0.02

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COUNTERS, DECODERS/DEMULTIPLEXERS

FUNCTION COUNTERS (SOFTWARE)	MACRO NAME	TYPE OF CLEAR	OUTPUT DRIVE	CELLS USED	SWITCHING CHARACTERISTICS $C_L = 0$ (See Note 1)	DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
4-BIT BINARY	S161ALJ	ASYNCH	1X	79	TYP	3.9	3.5	0.9	0.52
					MAX	7.1	7.1	1.73	0.96
4-BIT BINARY	S163ALJ	SYNCH	1X	81	TYP	3.9	3.5	0.9	0.52
					MAX	7.1	7.1	1.73	0.96
4-BIT UP/DOWN BINARY	S191LJ	NONE	1X	98	TYP	4.7	3.9	0.88	0.99
					MAX	9	7.5	1.72	2.04
4-BIT UP/DOWN BINARY	S193LJ	ASYNCH	1X	87	TYP	3.8	3.7	0.88	1.56
					MAX	7.4	7.2	1.76	3.3

NOTE 1: Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked functions embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation, produce workstation output used to identify and resolve each specific timing need.

FUNCTION DECODER/ DEMULTI-PLEXERS	MACRO NAME	SIZE	OUTPUT DRIVE	CELLS USED	SWITCHING CHARACTERISTICS $C_L = 0$	DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
HARDWIRED	DE210LJ	2-TO-4	1X	3	TYP	0.39	0.47	0.87	0.73
					MAX	0.97	1.18	1.7	1.46
3-ENABLES (SOFTWARE)	S138LJ	3-TO-8	1X	25	TYP	1.6	2.7	0.88	1.27
					MAX	2.5	5.3	1.74	2.66
1-ENABLE (SOFTWARE)	S139LJ	DUAL 2-TO-4	1X	26	TYP	1.3	1.4	0.88	0.99
					MAX	2.1	2.4	1.72	2.04

D-TYPE FLIP-FLOPS

FUNCTION D-TYPE FLIP-FLOPS HARDWIRED (f_{clock})	MACRO NAME	OUTPUT DRIVE	CELLS USED		SWITCHING CHARACTERISTICS C_L = 0 (CLK to Q) DELAY TIME t_{PLH} (ns)	t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)	TIMING RQMTS SETUP t_{su} (ns)	HOLD t_h (ns)
115 MHz W/CLRZ AND PREZ	DFB20LJ	2X	12	TYP	2	1.37	0.46	0.35	3	1
				MAX	4.21	2.9	0.92	0.64		
100 MHz W/CLRZ AND PREZ	DTB00LJ	0.5X	8	TYP	1.38	1.39	1.96	1.98	2	0
				MAX	2.83	2.9	3.88	3.86		
170 MHz W/CLRZ AND PREZ	DTB10LJ	1X	9	TYP	1.46	1.53	0.88	0.52	1.9	0
				MAX	3.11	3.2	1.7	0.96		
193 MHz W/CLRZ AND PREZ	DTB20LJ	2X	10	TYP	1.68	1.65	0.42	0.32	2.1	0.6
				MAX	3.64	3.53	0.84	0.6		
100 MHz W/CLRZ	DTC00LJ	0.5X	7	TYP	1.29	1.33	1.92	1.86	2	0
				MAX	2.57	2.76	3.82	3.58		
185 MHz W/CLRZ	DTC10LJ	1X	8	TYP	1.44	1.54	0.9	0.52	1.5	0.7
				MAX	3.02	3.21	1.72	0.96		
208 MHz W/CLRZ	DTC20LJ	2X	9	TYP	1.[illegible]3	1.64	0.44	0.32	1.6	0.7
				MAX	3.46	3.45	0.86	0.62		
100 MHz	DTN00LJ	0.5X	6	TYP	1.23	1.26	1.6	1.84	2	0
				MAX	2.48	2.55	3.06	3.6		
179 MHz	DTN10LJ	1X	7	TYP	1.32	2.43	0.88	0.52	0.7	0.6
				MAX	2.75	2.99	1.68	0.92		
208 MHz	DTN20LJ	2X	8	TYP	1.49	1.56	0.44	0.3	0.7	0.6
				MAX	3.19	3.24	0.82	0.6		
95 MHz W/PREZ	DTP00LJ	0.5X	7	TYP	1.35	1.44	1.58	1.96	2	0
				MAX	2.65	2.91	3.06	3.84		
167 MHz W/PREZ	DTP10LJ	1X	8	TYP	1.34	1.55	0.88	0.52	1.6	0
				MAX	2.75	3.19	1.7	0.92		
200 MHz W/PREZ	DTP20LJ	2X	9	TYP	1.53	1.69	0.42	0.3	1.6	0
				MAX	3.18	3.5	0.82	0.6		

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D-TYPE FLIP-FLOPS, DELAY ELEMENTS

FUNCTION D-TYPE FLIP-FLOPS SOFTWARE	MACRO NAME	OUTPUT DRIVE	CELLS USED		SWITCHING CHARACTERISTICS $C_L = 0$ (See Note 1) DELAY TIME t_{PLH} (ns)	t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
4-BIT 3-STATE WITH CLR	S173LJ	1X	53	TYP	2.3	2.5	0.96	0.64
				MAX	4.5	5.1	1.9	1.26
4-BIT COMP. OUTPUTS WITH CLRZ	S175LJ	1X	31	TYP	1.8	1.7	0.9	0.52
				MAX	3.9	3.5	1.73	0.96
8-BIT WITH CLRZ	S273LJ	1X	55	TYP	1.4	1.6	0.89	0.51
				MAX	2.8	3.4	1.72	0.95
8-BIT WITH 3-STATE	S374LJ	1X	76	TYP	2.3	2.5	0.96	0.64
				MAX	4.5	5.1	1.9	1.26

NOTE 1: Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked functions embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation, produce workstation output used to identify and resolve each specific timing need.

FUNCTION DELAY ELEMENTS HARDWIRED	MACRO NAME	FUNC-TION	OUTPUT DRIVE	CELLS USED		SWITCHING CHARACTERISTICS $C_L = 0$ DELAY TIME t_{PLH} (ns)	t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
LEVEL RESTORER	DLD00LJ	LOGIC DRIVER	1X	2	TYP	0.59	0.42	0.44	0.49
					MAX	1.26	0.92	0.86	0.87
DELAY ELEMENT	DLE00LJ	2 ns TYP DELAY	DRIVES DLD00LJ DLE00LJ	3	TYP	1.58	1.92	2.55	1.24
					MAX	3.73	4.45	5.19	2.57

EX-NOR, EX-OR GATES, INPUT BUFFERS

FUNCTION HARDWIRED	MACRO NAME	NO. OF INPUTS	OUTPUT DRIVE	CELLS USED		SWITCHING CHARACTERISTICS $C_L = 0$ DELAY TIME t_{PLH} (ns)	t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
EX-NOR GATE	EN210LJ	2	1X	3	TYP	0.57	0.85	0.89	0.57
					MAX	1.09	2.02	1.72	1.06
EX-OR GATES	EX210LJ	2	1X	3	TYP	0.81	0.75	0.89	0.5
					MAX	1.6	1.48	1.72	0.9
	EX220LJ	2	2X	4	TYP	0.86	0.81	0.45	0.3
					MAX	1.75	1.61	0.88	0.56

FUNCTION INPUT BUFFERS HARDWIRED	MACRO NAME	INPUT THRESHOLD VOLTAGE		SWITCHING CHARACTERISTICS $C_L = 0$ DELAY TIME t_{PLH} (ns)	t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
INVERTING	IPI00LJ	2.5	TYP	0.95	1.13	0.18	0.16
		(CMOS)	MAX	1.64	1.87	0.38	0.25
NON-INVERTING	IPI01LJ	2.5	TYP	1.1	0.77	0.2	0.17
		(CMOS)	MAX	1.63	1.36	0.39	0.27
	IPI04LJ	1.3	TYP	1.62	1.22	0.2	0.26
		(TTL)	MAX	2.39	2.82	0.39	0.62
INV. WITH HYSTERESIS	IPI06LJ	0.9/3.85	TYP	2.22	2.31	0.81	0.92
		(CMOS)	MAX	2.8	3.05	1.48	1.7
NONINVERTING WITH HYSTERESIS	IPI09LJ	0.8/2	TYP	1.74	2.71	0.24	0.44
		(TTL)	MAX	2.59	5.27	0.45	0.83
WITH 70-μA PULL-UP CURRENT SOURCE	IPL01LJ	2.5	TYP	1.15	0.82	0.19	0.18
		(CMOS)	MAX	1.71	1.45	0.36	0.24
	IPL04LJ	1.3	TYP	1.66	1.23	0.19	0.26
		(TTL)	MAX	2.44	2.84	0.39	0.62
WITH 70-μA PULL-DOWN CURRENT SOURCE	IPU01LJ	2.5	TYP	1.16	0.8	0.19	0.14
		(CMOS)	MAX	1.7	1.4	0.36	0.25
	IPU04LJ	1.3	TYP	1.68	1.29	0.19	0.26
		(TTL)	MAX	2.47	3.01	0.37	0.64

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BIDIRECTIONAL INPUT/OUTPUT BUFFERS

FUNCTION I/O 3-STATE BIDIRECTIONAL HARDWIRED	MACRO NAME	OUTPUT CURRENT (mA)	INPUT THRESHOLD VOLTAGE		OUTPUT SWITCHING CHARACTERISTICS† C_L = 15 pF DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
	IOI21LJ	2	2.5	TYP	4.29	5.04	0.16	0.14
			(CMOS)	MAX	8.31	9.66	0.3	0.25
	IOI24LJ	2	1.3	TYP	4.31	5.03	0.16	0.14
			(TTL)	MAX	8.33	9.63	0.3	0.25
	IOI41LJ	4	2.5	TYP	2.88	3.84	0.08	0.07
			(CMOS)	MAX	5.72	7.7	0.15	0.13
	IOI44LJ	4	1.3	TYP	2.88	3.84	0.08	0.07
			(TTL)	MAX	5.72	7.69	0.15	0.13
	IOI81LJ	8	2.5	TYP	2.56	3.58	0.04	0.05
			(CMOS)	MAX	5.29	7.53	0.08	0.09
	IOI84LJ	8	1.3	TYP	2.56	3.58	0.04	0.05
			(TTL)	MAX	5.29	7.53	0.08	0.09
WITH di/dt CONTROL	IOK21LJ	2	2.5	TYP	5.21	7.88	0.16	0.15
			(CMOS)	MAX	10.27	15.14	0.3	0.27
	IOK24LJ	2	1.3	TYP	5.22	7.86	0.16	0.15
			(TTL)	MAX	10.3	15.11	0.3	0.27
	IOK41LJ	4	2.5	TYP	4.12	6.75	0.08	0.09
			(CMOS)	MAX	8.38	13.41	0.16	0.17
	IOK44LJ	4	1.3	TYP	4.12	6.74	0.03	0.09
			(TTL)	MAX	8.39	13.4	0.16	0.17
	IOK81LJ	8	2.5	TYP	4.17	6.82	0.05	0.07
			(CMOS)	MAX	8.8	14.06	0.1	0.13
	IOK84LJ	8	1.3	TYP	4.18	6.81	0.05	0.07
			(TTL)	MAX	8.8	14.05	0.1	0.13

† CMOS shown.

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BIDIRECTIONAL INPUT/OUTPUT BUFFERS

FUNCTION I/O 3-STATE BIDIRECTIONAL HARDWIRED	MACRO NAME	OUTPUT CURRENT (mA)	INPUT THRESHOLD VOLTAGE		OUTPUT SWITCHING CHARACTERISTICS† C_L = 15 pF			
					DELAY TIME		DELTA DELAY	
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
WITH 70-μA PULL-UP	IOL21LJ	2	2.5	TYP	4.28	5.08	0.16	0.14
			(CMOS)	MAX	8.27	9.74	0.3	0.25
	IOL24LJ	2	1.3	TYP	4.29	5.07	0.16	0.14
			(TTL)	MAX	8.29	9.72	0.3	0.25
	IOL41LJ	4	2.5	TYP	2.88	3.87	0.08	0.07
			(CMOS)	MAX	5.71	7.75	0.15	0.13
	IOL44LJ	4	1.3	TYP	2.88	3.86	0.08	0.07
			(TTL)	MAX	5.71	7.74	0.15	0.13
	IOL81LJ	8	2.5	TYP	2.56	3.6	0.04	0.05
			(CMOS)	MAX	5.28	7.56	0.08	0.09
	IOL84LJ	8	1.3	TYP	2.56	3.59	0.04	0.05
			(TTL)	MAX	5.28	7.56	0.08	0.09
WITH di/dt CONTROL AND 70-μA PULL-UP	ION21LJ	2	2.5	TYP	5.19	7.93	0.16	0.15
			(CMOS)	MAX	10.22	15.24	0.3	0.27
	ION24LJ	2	1.3	TYP	5.2	7.92	0.16	0.15
			(TTL)	MAX	10.25	15.21	0.3	0.27
	ION41LJ	4	2.5	TYP	4.11	6.78	0.08	0.09
			(CMOS)	MAX	8.36	13.47	0.16	0.17
	ION44LJ	4	1.3	TYP	4.11	6.78	0.08	0.09
			(TTL)	MAX	8.37	13.46	0.16	0.17
	ION81LJ	8	2.5	TYP	4.17	6.84	0.05	0.07
			(CMOS)	MAX	8.79	14.11	0.1	0.13
	ION84LJ	8	1.3	TYP	4.17	6.84	0.05	0.07
			(TTL)	MAX	8.79	14.09	0.1	0.13

† CMOS shown.

BIDIRECTIONAL INPUT/OUTPUT BUFFERS

FUNCTION I/O 3-STATE BIDIRECTIONAL HARDWIRED	MACRO NAME	OUTPUT CURRENT (mA)	INPUT THRESHOLD VOLTAGE	OUTPUT SWITCHING CHARACTERISTICS† C_L = 15 pF	DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
WITH 70-μA PULL-DOWN	IOU21LJ	2	2.5	TYP	4.33	5.02	0.16	0.14
			(CMOS)	MAX	8.37	9.61	0.3	0.25
	IOU24LJ	2	1.3	TYP	4.34	5	0.16	0.14
			(TTL)	MAX	8.4	9.59	0.3	0.25
	IOU41LJ	4	2.5	TYP	2.89	3.84	0.08	0.07
			(CMOS)	MAX	5.75	7.69	0.15	0.13
	IOU44LJ	4	1.3	TYP	2.89	3.83	0.08	0.07
			(TTL)	MAX	5.75	7.68	0.15	0.13
	IOU81LJ	8	2.5	TYP	2.57	3.58	0.04	0.05
			(CMOS)	MAX	5.3	7.53	0.08	0.09
	IOU84LJ	8	1.3	TYP	2.57	3.58	0.04	0.05
			(TTL)	MAX	5.3	7.52	0.08	0.09
WITH di/dt CONTROL AND 70-μA PULL-DOWN	IOW21LJ	2	2.5	TYP	5.24	7.84	0.16	0.15
			(CMOS)	MAX	10.33	15.06	0.3	0.27
	IOW24LJ	2	1.3	TYP	5.25	7.82	0.16	0.15
			(TTL)	MAX	10.36	15.03	0.3	0.27
	IOW41LJ	4	2.5	TYP	4.13	6.73	0.08	0.09
			(CMOS)	MAX	8.4	13.37	0.16	0.17
	IOW44LJ	4	1.3	TYP	4.13	6.73	0.08	0.09
			(TTL)	MAX	8.41	13.36	0.16	0.17
	IOW81LJ	8	2.5	TYP	4.18	6.81	0.05	0.07
			(CMOS)	MAX	8.82	14.04	0.1	0.13
	IOW84LJ	8	1.3	TYP	4.18	6.8	0.05	0.07
			(TTL)	MAX	8.81	14.02	0.1	0.13

† CMOS shown.

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INVERTERS, 3-STATE INVERTERS, J-K FLIP-FLOPS

FUNCTION HARDWIRED	MACRO NAME	NO. OF INPUTS	OUTPUT DRIVE	CELLS USED		SWITCHING CHARACTERISTICS $C_L = 0$ DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
INVERTERS	IV110LJ	1	1X	1	TYP	0.26	0.28	0.86	0.5
					MAX	0.36	0.41	1.68	0.82
	IV120LJ	1	2X	1	TYP	0.24	0.19	0.44	0.32
					MAX	0.32	0.36	0.84	0.44
	IV140LJ	1	4X	2	TYP	0.2	0.13	0.26	0.22
					MAX	0.34	0.28	0.4	0.3
3-STATE INVERTERS	IV211LJ A to Y	2	1X	2	TYP	0.45	0.43	0.96	0.64
					MAX	0.77	0.66	1.9	1.26
	IV221LJ A to Y	2	2X	4	TYP	0.38	0.33	0.45	0.31
					MAX	0.62	0.58	0.88	0.61
	IV241LJ A to Y	2	4X	5	TYP	0.33	0.29	0.26	0.25
					MAX	0.52	0.58	0.52	0.48

FUNCTION J-$\overline{K}$ FLIP-FLOPS HARDWIRED (f_{clock})	MACRO NAME	OUTPUT DRIVE	CELLS USED		SWITCHING CHARACTERISTICS $C_L = 0$ (CLK to Q) DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)	TIMING RQMTS SETUP (min) t_{su} (ns)	TIMING RQMTS HOLD (min) t_h (ns)
135 MHz W/CLRZ AND PREZ	JKB20LJ	2X	12	TYP	2.13	2.07	0.44	0.34	4	0
				MAX	4.45	4.34	0.86	0.64		
135 MHz W/CLRZ AND PREZ	JKB21LJ (NEG. EDGE CLOCK)	2X	12	TYP	2.08	2.28	0.44	0.34	3	0
				MAX	4.33	4.81	0.88	0.66		

LATCHES, MULTIPLEXERS

FUNCTION					SWITCHING CHARACTERISTICS C_L = 0 (See Note 1)				
						DELAY TIME		DELTA DELAY	
LATCHES	MACRO NAME	WIDTH OR SIZE	OUTPUT DRIVE	CELLS USED		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
HARDWIRED	LAB20LJ	1-BIT	2X	4	TYP	1.1	0.68	0.44	0.3
					MAX	2.24	1.28	0.86	0.6
	LAH12LJ	1-BIT	1X	5	TYP	1.27	1.43	0.97	0.64
					MAX	2.5	2.85	1.88	1.27
	LAH13LJ	1-BIT	1X	5	TYP	1.26	1.16	0.96	0.63
					MAX	2.53	2.23	1.89	1.27
	LAH14LJ	1-BIT	1X	7	TYP	1.43	1.55	0.96	0.64
					MAX	2.81	3.11	1.89	1.26
	LAH20LJ	1-BIT	2X	5	TYP	1.31	1.48	0.44	0.3
					MAX	2.64	3.05	0.86	0.6
	LAH22LJ	1-BIT	2X	4	TYP	0.89	0.99	0.48	0.38
					MAX	1.73	1.99	0.96	0.73
	LH110LJ	1-BIT	1X	4	TYP			(0.56 pF)	(0.56 pF)
	LH400LJ	4-BITS	1X	11	TYP	1.35	1.51	1.59	1.89
					MAX	2.73	3.07	3.09	3.61
SOFTWARE	S373LJ	8-BITS	1X	47	TYP	1.8	2.3	0.96	0.64
					MAX	3.4	4.4	1.9	1.26
	S375LJ	4-BITS	2X	16	TYP	2	1.9	0.44	0.32
					MAX	4.2	3.2	0.84	0.44

NOTE 1: Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked functions embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation, produce workstation output used to identify and resolve each specific timing need.

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MULTIPLEXERS

FUNCTION MULTIPLEXERS	MACRO NAME	SIZE	OUTPUT DRIVE	CELLS USED	SWITCHING CHARACTERISTICS $C_L = 0$	DELAY TIME t_{PLH} (ns)	t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
HARDWIRED	MU111LJ	2-TO-1	1X	3	TYP	0.62	0.81	0.89	0.57
					MAX	1.36	1.87	1.72	1.1
	MU220LJ	4-TO-1	1X	7	TYP	0.95	1.11	0.47	0.49
					MAX	1.87	2.33	0.94	1
	MU311LJ	8-TO-1	1X	13	TYP	1.28	1.5	0.91	0.88
					MAX	2.61	3.27	1.81	1.8
SOFTWARE	S150LJ	16-TO-1	2X	123	TYP	4.3	4.5	0.44	0.32
					MAX	8.2	9	0.84	0.44
	S151LJ	8-TO-1	2X	40	TYP	3.5	3.5	0.44	0.32
					MAX	6.6	6.8	0.84	0.44
	S153LJ	DUAL 4-TO-1	1X	26	TYP	2.4	2.2	0.88	1.27
					MAX	4.1	3.9	1.74	2.66
	S157LJ	QUAD 2-TO-1	1X	18	TYP	2.5	2.4	0.87	0.72
					MAX	4.1	3.9	1.7	1.44

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NAND GATES

FUNCTION	MACRO NAME	NO. OF INPUTS	OUTPUT DRIVE	CELLS USED		SWITCHING CHARACTERISTICS $C_L = 0$ DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
NAND GATES	NA210LJ	2	1X	1	TYP	0.3	0.33	0.87	0.72
					MAX	0.52	0.47	1.7	1.44
	NA220LJ	2	2X	2	TYP	0.29	0.28	0.43	0.39
					MAX	0.5	0.46	0.84	0.72
	NA310LJ	3	1X	2	TYP	0.36	0.4	0.88	0.99
					MAX	0.73	0.72	1.72	2.04
	NA311LJ	3	1X	2	TYP	0.38	0.46	0.88	0.99
					MAX	0.78	1.09	1.72	2.05
	NA320LJ	3	2X	3	TYP	0.34	0.36	0.44	0.5
					MAX	0.65	0.61	0.86	1.04
	NA410LJ	4	1X	2	TYP	0.4	0.46	0.88	1.27
					MAX	0.82	0.95	1.74	2.66
	NA420LJ	4	2X	4	TYP	0.38	0.44	0.44	0.64
					MAX	0.77	0.92	0.9	1.34
	NA510LJ	5	1X	3	TYP	0.46	0.61	0.88	1.56
					MAX	1.01	1.43	1.76	3.3
	NA520LJ	5	2X	5	TYP	0.42	0.56	0.45	0.78
					MAX	0.89	1.26	0.92	1.66
	NA810LJ	8	1X	6	TYP	0.85	1.26	0.88	0.55
					MAX	1.86	2.75	1.72	1.02
	NA820LJ	8	2X	6	TYP	0.9	1.36	0.44	0.37
					MAX	1.97	3.04	0.86	0.7

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NOR, OR-AND, OR-NAND GATES

FUNCTION	MACRO NAME	NO. OF INPUTS	OUTPUT DRIVE	CELLS USED	SWITCHING CHARACTERISTICS $C_L = 0$	DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
NOR GATES	NO210LJ	2	1X	1	TYP	0.35	0.31	1.67	0.5
					MAX	0.67	0.49	3.4	0.82
	NO220LJ	2	2X	2	TYP	0.35	0.23	0.82	0.32
					MAX	0.62	0.43	1.72	0.45
	NO310LJ	3	1X	2	TYP	0.57	0.34	2.48	0.49
					MAX	1.45	0.51	5.1	0.88
	NO320LJ	3	2X	3	TYP	0.49	0.25	1.23	0.31
					MAX	1.22	0.47	2.58	0.45
	NO410LJ	4	1X	4	TYP	0.95	0.68	0.88	0.49
					MAX	1.95	1.47	1.71	0.88
	NO420LJ	4	2X	4	TYP	1.02	0.74	0.45	0.3
					MAX	2.15	1.61	0.87	0.59
	NO510LJ	5	1X	4	TYP	1.19	0.71	0.88	0.5
					MAX	3.12	1.5	1.7	0.9
	NO520LJ	5	2X	5	TYP	1.22	0.77	0.45	0.3
					MAX	3.08	1.66	0.88	0.58
	NO810LJ	8	1X	6	TYP	1.63	0.75	0.89	0.49
					MAX	4.23	1.56	1.72	0.9
	NO820LJ	8	2X	6	TYP	1.72	0.81	0.45	0.3
					MAX	4.49	1.7	0.9	0.56
OR-AND	OA220LJ	4	2X	3	TYP	0.63	0.99	0.45	0.39
					MAX	1.25	2.38	0.88	0.78
OR-NAND	OA231LJ	6	1X	3	TYP	0.64	0.48	1.69	1
					MAX	1.78	1.03	3.42	2.07
	OA241LJ	8	1X	4	TYP	0.88	0.97	1.72	1.29
					MAX	2.47	2.35	3.43	2.7

WORKSTATION LIBRARY SUMMARY 1-μm CMOS GATE ARRAYS

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TOTEM-POLE OUTPUTS

FUNCTION OUTPUT TOTEM-POLE HARDWIRED	MACRO NAME	OUTPUT CURRENT SOURCE/ SINK (mA)	SWITCHING CHARACTERISTICS† C_L = 15 pF	DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ps/pF)	DELTA DELAY Δt_{PHL} (ps/pF)
	OPIA0LJ	12/16	TYP	1.56	1.76	30	20
			MAX	2.92	3.45	50	40
	OPIH0LJ	12/12	TYP	1.56	1.78	30	30
			MAX	2.91	3.42	50	50
	OPIJ0LJ	12/20	TYP	1.57	1.8	30	10
			MAX	2.92	3.6	50	30
	OPI20LJ	2/2	TYP	3.91	4.01	160	140
			MAX	7.36	7.28	300	250
	OPI40LJ	4/4	TYP	2.24	2.36	80	70
			MAX	4.17	4.28	150	120
	OPI80LJ	8/8	TYP	1.63	1.86	40	40
			MAX	3.02	3.5	70	70
di/dt CONTROL	OPKA0LJ	12/16	TYP	3.73	5.66	40	50
			MAX	7.7	11.6	80	90
	OPKH0LJ	12/12	TYP	3.72	5.24	40	50
			MAX	7.68	10.6	80	100
	OPKJ0LJ	12/20	TYP	3.73	6.24	40	40
			MAX	7.71	12.9	80	80
	OPK20LJ	2/2	TYP	4.63	6.53	160	150
			MAX	8.98	12.19	300	260
	OPK40LJ	4/4	TYP	3.47	5.3	80	80
			MAX	6.81	10.04	150	150
	OPK80LJ	8/8	TYP	3.38	5.23	50	60
			MAX	6.87	10.28	90	110

† CMOS shown.

3-STATE OUTPUTS

FUNCTION OUTPUT 3-STATE HARDWIRED	MACRO NAME	OUTPUT CURRENT SOURCE/ SINK (mA)	SWITCHING CHARACTERISTICS† C_L = 15 pF	DELAY TIME		DELTA DELAY	
				t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
	OPI23LJ	2/2	TYP	4.14	4.91	160	140
			MAX	8	9.41	300	250
	OPI43LJ	4/4	TYP	2.81	3.77	80	70
			MAX	5.57	7.56	150	140
	OPI83LJ	8/8	TYP	2.52	3.53	40	50
			MAX	5.2	7.43	80	90
di/dt CONTROL	OPK23LJ	2/2	TYP	5.06	7.74	160	150
			MAX	9.98	14.88	300	270
	OPK43LJ	4/4	TYP	4.04	6.66	80	90
			MAX	8.23	13.24	160	170
	OPK83LJ	8/8	TYP	4.12	6.75	50	70
			MAX	8.69	13.92	100	130

† CMOS shown.

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OPEN-DRAIN OUTPUTS

FUNCTION OUTPUT OPEN-DRAIN HARDWIRED	MACRO NAME	OUTPUT CURRENT (mA)		SWITCHING CHARACTERISTICS† C_L = 15 pF DELAY TIME t_{PZL} (ns)	DELAY TIME t_{PZH} (ns)	DELTA DELAY Δt_{PZL} (ps/pF)	DELTA DELAY Δt_{PZH} (ps/pF)
N-CHANNEL (SINK CURRENT)	OPI21LJ	2	TYP	3.95		150	
			MAX	7.51		290	
	OPI41LJ	4	TYP	2.26		70	
			MAX	4.17		130	
	OPI81LJ	8	TYP	1.77		40	
			MAX	3.35		70	
N-CHANNEL WITH di/dt CONTROL (SINK CURRENT)	OPK21LJ	2	TYP	6.59		160	
			MAX	12.8		290	
	OPK41LJ	4	TYP	5.26		90	
			MAX	10.17		160	
	OPK81LJ	8	TYP	5.19		60	
			MAX	10.34		110	
P-CHANNEL (SOURCE CURRENT)	OPI24LJ	2	TYP		4.1		170
			MAX		8.26		340
	OPI44LJ	4	TYP		2.25		80
			MAX		4.26		160
	OPI84LJ	8	TYP		1.61		40
			MAX		3.01		80
P-CHANNEL WITH di/dt CONTROL (SOURCE CURRENT)	OPK24LJ	2	TYP		4.85		170
			MAX		9.94		340
	OPK44LJ	4	TYP		3.5		80
			MAX		7.03		160
	OPK84LJ	8	TYP		3.4		50
			MAX		6.95		90

† CMOS shown.

OR GATES

FUNCTION	MACRO NAME	NO. OF INPUTS	OUTPUT DRIVE	CELLS USED		SWITCHING CHARACTERISTICS $C_L = 0$ DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
OR GATES	OR210LJ	2	1X	2	TYP	0.39	0.71	0.88	0.55
					MAX	0.78	1.47	1.7	1
	OR220LJ	2	2X	2	TYP	0.46	0.82	0.44	0.36
					MAX	0.83	1.72	0.86	0.7
	OR310LJ	3	1X	2	TYP	0.43	1.04	0.88	0.64
					MAX	0.84	2.44	1.73	1.21
	OR320LJ	3	2X	3	TYP	0.52	1.2	0.44	0.42
					MAX	0.93	2.88	0.87	0.83
	OR410LJ	4	1X	3	TYP	0.46	1.34	0.89	0.72
					MAX	0.85	3.43	1.75	1.39
	OR420LJ	4	2X	3	TYP	0.51	1.53	0.45	0.49
					MAX	0.91	3.98	0.89	0.97
	OR510LJ	5	1X	4	TYP	0.46	0.97	0.89	0.79
					MAX	0.97	2.49	1.73	1.6
	OR810LJ	8	1X	5	TYP	0.5	1.43	0.89	0.9
					MAX	0.98	3.83	1.76	1.92

OSCILLATORS

FUNCTION				SWITCHING CHARACTERISTICS† $C_L = 0$				
		FREQUENCY	INTERNAL		DELAY TIME		DELTA DELAY	
OSCILLATORS HARDWIRED	MACRO NAME	RANGE (MHz)	OUTPUT DRIVE		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
THIRD OVERTONE	OSI11LJ	55 TO 75	1X	TYP	2.52	2.33	160	160
				MAX	4.2	4.04	350	340
THIRD OVERTONE	OSI12LJ	35 TO 55	1X	TYP	2.37	2.19	170	180
				MAX	3.99	3.87	370	350
THIRD OVERTONE	OSI13LJ	20 TO 35	1X	TYP	2.29	2.13	180	180
				MAX	3.89	3.78	370	350
FUNDAMENTAL	OSI14LJ	1 TO 20	1X	TYP	2.27	2.11	190	190
				MAX	3.88	3.76	370	350

† CMOS output delay times are shown.

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REGISTERS

FUNCTION REGISTER/ FLIP-FLOPS HARDWIRED	MACRO NAME	f_{clock}	OUTPUT DRIVE	CELLS USED		SWITCHING CHARACTERISTICS (CLK to Q OUT) DELAY TIME t_{PLH} (ns)	t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)	TIMING RQMTS SETUP (min) t_{su} (ns)	HOLD (min) t_h (ns)
4-BIT, SER IN, CLRZ	R2401LJ	135 MHz	1X	26	TYP	1.38	1.59	0.89	0.51	2	0
					MAX	2.77	3.21	1.73	0.95		
4-BIT, SER IN, CLRZ, COMP. OUT.	R2402LJ	135 MHz	1X	27	TYP	1.49	1.66	0.89	0.55	2	0
					MAX	3.07	3.43	1.74	1.01		
4-BIT, PARALLEL IN	R2403LJ	135 MHz	1X	27	TYP	1.25	1.58	0.89	0.51	2	0
					MAX	2.46	3.19	1.71	0.93		
4-BIT, PARALLEL IN COMP. OUT.	R2404LJ	135 MHz	1X	31	TYP	1.26	1.58	0.89	0.51	2	0
					MAX	2.48	3.22	1.72	0.94		
4-BIT WITH CLRZ	R2405LJ	135 MHz	1X	26	TYP	1.42	1.63	0.89	0.51	2	0
					MAX	2.85	3.33	1.72	0.95		
4-BIT WITH CLRZ AND COMP. OUT.	R2406LJ	135 MHz	1X	28	TYP	1.36	1.68	0.9	0.52	2	0
					MAX	2.73	3.49	1.73	0.96		

REGISTER FILES†

FUNCTION 3-PORT REGISTER FILES HARD-WIRED	MACRO NAME	ORGANI-ZATION (W X 8)	OUT-PUT DRIVE	CELLS USED		ACCESS/CYCLE TIME CHARACTERISTICS (CLK to Q OUT) WRITE CYCLE $t_{c(W)}$ (min)	ADDR. ACCESS $t_{a(A)}$ (ns)	ENABLE ACCESS $t_{en(G)}$ (ns)	DELTA DELAY Δt_a (ns/pF)	TIMING RQMTS WRITE SETUP (min) t_{su} (ns)	WRITE HOLD (min) t_h (ns)
1-WRITE, 2-READ	RF400LJ	16 X 8	2X	418	TYP		5.2	1.3	0.3		
					MAX	10	10.89	3.23	1.02	5	2
	RF402LJ	16 X 9	2X	462	TYP		5.3	1.4	0.3		
					MAX	10	11.03	3.4	1.07	5	2

† RF400LJ and RF402LJ are for use on TGC112, TGC115, or TGC118 gate arrays only.

SCAN FLIP-FLOPS/LATCHES

FUNCTION SCAN FLIP-FLOPS LATCHES HARDWIRED	MACRO NAME	OPERATING FREQ. f_{opr}	OUTPUT DRIVE	CELLS USED	SWITCHING CHARACTERISTICS (CLK to Q OUT)	DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)	TIMING RQMTS† SETUP (min) t_{su} (ns)	TIMING RQMTS† HOLD (min) t_h (ns)
D-FF, WITH CLRZ	TDB10LJ	90 MHz	1X	10	TYP	1.83	2.57	0.9	0.58	4	0
					MAX	3.69	5.69	1.77	1.06		
M-S D-LTCH WITH CLR, COMP. OUT.	TDC11LJ	100 MHz	1X	10	TYP	2.18	2.23	0.9	0.68	3	0
					MAX	4.49	4.98	1.76	1.31		
M-S D-LTCH	TDN11LJ	100 MHz	1X	8	TYP	1.67	1.95	0.89	0.51	3	0
					MAX	3.69	4.3	1.76	0.94		
M-S D-LTCH WITH COMP. OUT.	TDN12LJ	100 MHz	1X	9	TYP	1.89	2.17	0.91	0.54	3	0
					MAX	4.23	4.84	1.77	0.95		
M-S D-LTCH W/SLAVE D, COMP. OUT.	TDN13LJ	100 MHz	1X	12	TYP	1.99	2.31	0.91	0.54	3	0
					MAX	4.41	5.07	1.77	0.98		
M-S D-LTCH	TDN22LJ	83 MHz	2X	11	TYP	2.18	2.57	0.44	0.32	3	0
					MAX	4.91	5.73	0.87	0.62		

† Use CK120LJ.

SHIFT REGISTERS, TOGGLE FLIP-FLOP, TIE-OFF

FUNCTION SHIFT REGISTERS SOFTWARE	MACRO NAME	LENGTH	OUTPUT DRIVE	CELLS USED		SWITCHING CHARACTERISTICS (See Note 1) DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
SIPO WITH CLRZ	S164LJ	8-BITS	2X	88	TYP	2.5	2.5	0.44	0.32
					MAX	4.7	4.7	0.84	0.44
PISO WITH CLKINH	S165ALJ	8-BITS	1X	124	TYP	3	2.4	0.46	0.34
					MAX	6.4	4.9	0.92	0.65
PIPO BIDIRECT. WITH CLRZ	S194ALJ	4-BITS	1X	73	TYP	1.8	1.9	0.89	0.51
					MAX	3.7	3.8	1.72	0.95

NOTE 1: Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked functions embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation, produce workstation output used to identify and resolve each specific timing need.

FUNCTION TOGGLE FLIP-FLOP (f_{clock}) HARDWIRED	MACRO NAME	OUTPUT DRIVE	CELLS USED		SWITCHING CHARACTERISTICS (CLK TO Q OUT) DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
131 MHz WITH CLRZ AND PREZ	TAB20LJ	2X	9	TYP	1.2	1.08	0.48	0.44
				MAX	2.48	2.3	0.98	0.84

FUNCTION TIEOFF FOR UNUSED INPUTS HARDWIRED	MACRO NAME	OUTPUT DRIVE	CELLS USED		SWITCHING CHARACTERISTICS DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
HI/LO WITH ESD PROTECTION	TO010LJ	1X	2	TYP				
				MAX	N/A	N/A	N/A	N/A

SPECIAL FUNCTIONS FUNCTIONAL INDEX

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SPECIAL FUNCTIONS

DESCRIPTION	MACRO NAME	OUTPUT DRIVE	COMMENTS	CELLS USED	PAGE
Delay Driver	DLD00LJ	2X	Level restorer	2	6-3
Delay Element	DLE00LJ	1X	2-ns delay	3	6-4
Tie-Off Gate	TO010LJ	1X	HI and LO outputs	2	6-5

DLD00LJ
DELAY DRIVER

D3015, OCTOBER 1988

INTERNAL DELAY DRIVER MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

POSITIVE LOGIC EQUATION: Y = A

description

The DLD00LJ is a noninverting internal delay driver that interfaces DLE00LJ delay elements with other CMOS functions. When DLE00LJ delay elements are used, the last element in cascade must be a DLD00LJ delay driver/level restorer. When the driver is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DLD00LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2		V
C_i	Input capacitance		0.17		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.64		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	0.2	0.59	1.26	ns
t_{PHL}			0.15	0.42	0.92	
Δt_{PLH}	A	Y	0.2	0.44	0.86	ns/pF
Δt_{PHL}			0.25	0.49	0.87	

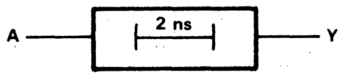
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

INTERNAL DELAY MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

POSITIVE LOGIC EQUATION: Y = A

description

The DLE00LJ is a noninverting delay element that provides 2 ns of delay from input to output. Delay elements may be cascaded to provide the desired total delay. When DLE00LJ delay elements are used, the last element in cascade must be a DLD00LJ delay driver/level restorer. When the delay element is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DLE00LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2		V
C_i	Input capacitance		0.23		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.6		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	0.4	1.58	3.73	ns
t_{PHL}			0.51	1.92	4.45	
Δt_{PLH}	A	Y	0.94	2.55	5.19	ns/pF
Δt_{PHL}			0.46	1.24	2.57	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TGC100 SERIES

T0010LJ ESD-PROTECTED TIE-OFF GATE WITH COMPLEMENTARY OUTPUTS

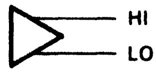
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

OUTPUTS	
HI	**LO**
H	L

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

WITH V_{CC} APPLIED: HI = H, LO = L

description

The T0010LJ internal tie-off gate is offered for managing unused inputs. The tie-off gate features complementary high-logic-level HI and low-logic-level LO outputs, each capable of handling all unused inputs encountered in the gate-array design. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: T0010LJ LO,HI;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	Nil		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

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Buffers/Drivers

BUFFERS/DRIVERS FUNCTIONAL INDEX

D3015, OCTOBER 1987 – REVISED OCTOBER 1988

BUFFERS

DESCRIPTION	MACRO NAME	OUTPUT DRIVE	COMMENTS	CELLS USED	PAGE
Buffers	BU130LJ	3X	Noninverting	2	7-3
	BU150LJ	5X		3	7-4
8-Bit 3-State Buffers	S244LJ	1X	Active-Low Enable	28	7-14

INVERTERS

DESCRIPTION	MACRO NAME	OUTPUT DRIVE	COMMENTS	CELLS USED	PAGE
Inverters	IV110LJ	1X		1	7-5
	IV120LJ	2X		1	7-6
	IV140LJ	4X		2	7-7
Inverting 3-State Buffers	IV211LJ	1X	Active-Low Enable	2	7-8
	IV221LJ	2X		4	7-10
	IV241LJ	4X		5	7-12

BU130LJ NONINVERTING BUFFER WITH 3X OUTPUT

D3015, OCTOBER 1987—REVISED OCTOBER 1988

INTERNAL BUFFER MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

POSITIVE LOGIC EQUATION: Y = A

description

The BU130LJ is a CMOS function featuring a 3X output to enhance its capacitive-drive capability and fanout. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BU130LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.96		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	0.21	0.28	0.82	ns
t_{PHL}			0.32	0.38	1.26	
Δt_{PLH}	A	Y	0.14	0.28	0.58	ns/pF
Δt_{PHL}			0.16	0.3	0.56	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BU150LJ
NONINVERTING BUFFER
WITH 5X OUTPUT

D3015, OCTOBER 1987 – REVISED OCTOBER 1988

INTERNAL BUFFER MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The BU150LJ is a CMOS function featuring a 5X output to enhance its capacitive-drive capability and fanout. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BU150LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	1.36		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	0.25	0.5	0.99	ns
t_{PHL}			0.41	0.85	1.66	
Δt_{PLH}	A	Y	0.1	0.2	0.38	ns/pF
Δt_{PHL}			0.1	0.26	0.47	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
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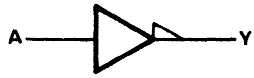
INTERNAL INVERTER MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



Equivalent to 1/4 7404

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$

description

The IV110LJ is a minimum-power inverter CMOS gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV110LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.21		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	0.21	0.26	0.36	ns
t_{PHL}			0.1	0.28	0.41	
Δt_{PLH}	A	Y	0.34	0.86	1.68	ns/pF
Δt_{PHL}			0.36	0.5	0.82	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

IV120LJ
INVERTER
WITH 2X OUTPUT

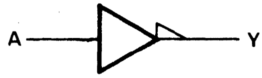
D3015, OCTOBER 1987

INTERNAL INVERTER MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



Equivalent to 1/4 7404

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$

description

The IV120LJ is an inverter CMOS gate featuring twice the capacitive-drive capability when compared to the IV110LJ inverter. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV120LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2		V
C_i	Input capacitance		0.15		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.39		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	0.16	0.24	0.32	ns
t_{PHL}			0.05	0.19	0.36	
Δt_{PLH}	A	Y	0.22	0.44	0.84	ns/pF
Δt_{PHL}			0.22	0.32	0.44	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

IV140LJ INVERTER WITH 4X OUTPUT

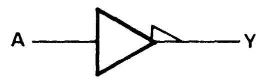
D3015, OCTOBER 1987

INTERNAL INVERTER MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



Equivalent to 1/4 7404

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$

description

The IV140LJ is an inverter CMOS gate featuring four times the capacitive-drive capability when compared to the IV110LJ inverter. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV140LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2		V
C_i	Input capacitance		0.31		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.8		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	0.15	0.2	0.34	ns
t_{PHL}			0.02	0.13	0.28	
Δt_{PLH}	A	Y	0.12	0.26	0.4	ns/pF
Δt_{PHL}			0.14	0.22	0.3	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

IV211LJ INVERTING 3-STATE BUFFER WITH ACTIVE-LOW ENABLE

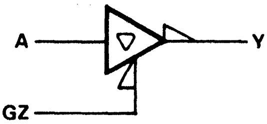
D3015, OCTOBER 1987

INTERNAL 3-STATE BUFFER

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$

description

The IV211LJ is an internal 3-state buffer that interfaces CMOS internal gates with internal 3-state bus lines. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV211LJ A,GZ,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A		0.08		pF
		GZ		0.16		
C_o	Output capacitance			0.08		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	0.38		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	0.27	0.45	0.77	ns
t_{PHL}				0.23	0.43	0.66	
t_{PZH}	GZ	Y	$R_L = 40\ k\Omega$ to GND	0.18	0.32	0.54	ns/pF
t_{PZL}			$R_L = 20\ k\Omega$ to V_{CC}	0.22	0.40	0.69	
t_{PHZ}	GZ	Y	$R_L = 40\ k\Omega$ to GND		3.81		ns
t_{PLZ}			$R_L = 20\ k\Omega$ to V_{CC}		2.19		
Δt_{PLH}	A	Y		0.38	0.96	1.9	ps/pF
Δt_{PHL}				0.32	0.64	1.26	
Δt_{PZH}	GZ	Y		0.18	0.86	1.76	ps/pF
Δt_{PZL}				0.24	0.62	1.26	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

IV221LJ
INVERTING 3-STATE BUFFER WITH ACTIVE-LOW ENABLE AND 2X OUTPUT

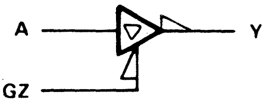
D3015, OCTOBER 1988

INTERNAL 3-STATE BUFFER

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The IV221LJ is an internal 3-state buffer that interfaces CMOS internal gates with internal 3-state bus lines. The inverter features two times the capability of inverter IV211LJ to drive capacitive loads. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV221LJ A,GZ,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	A		0.23		pF
		GZ		0.23		
C_o	Output capacitance			0.17		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.96		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

IV221LJ INVERTING 3-STATE BUFFER WITH ACTIVE-LOW ENABLE AND 2X OUTPUT

D3015, OCTOBER 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	0.22	0.38	0.62	ns
t_{PHL}				0.14	0.33	0.58	
t_{PZH}	GZ	Y	R_L = 40 kΩ to GND	0	0.3	0.56	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.17	0.43	0.77	
t_{PHZ}	GZ	Y	R_L = 40 kΩ to GND		4.48		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		2.44		
Δt_{PLH}	A	Y		0.16	0.36	0.69	ps/pF
Δt_{PHL}				0.17	0.31	0.55	
Δt_{PZH}	GZ	Y		0.33	0.45	0.88	ps/pF
Δt_{PZL}				0.19	0.31	0.61	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

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IV241LJ
INVERTING 3-STATE BUFFER WITH ACTIVE-LOW ENABLE AND 4X OUTPUT

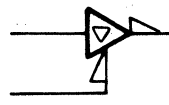
D3015, OCTOBER 1988

INTERNAL 3-STATE BUFFER

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The IV241LJ is an internal 3-state inverter that interfaces CMOS internal gates with internal 3-state bus lines. The inverter features four times the capability of inverter IV211LJ to drive capacitive loads. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV241LJ A,GZ,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	A		0.38		pF
		GZ		0.23		pF
C_o	Output capacitance			0.17		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	1.36		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	0.2	0.33	0.52	ns
t_{PHL}				0.08	0.29	0.58	
t_{PZH}	GZ	Y	R_L = 40 kΩ to GND	0	0.24	0.46	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.16	0.43	0.77	
t_{PHZ}	GZ	Y	R_L = 40 kΩ to GND		3.86		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		2.14		
Δt_{PLH}	A	Y		0.12	0.26	0.52	ps/pF
Δt_{PHL}				0.16	0.25	0.48	
Δt_{PZH}	GZ	Y		0.34	0.46	0.86	ps/pF
Δt_{PZL}				0.19	0.29	0.56	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

S244LJ
OCTAL INTERNAL BUS BUFFER WITH 3-STATE OUTPUTS

D3015, OCTOBER 1987—REVISED FEBRUARY 1989

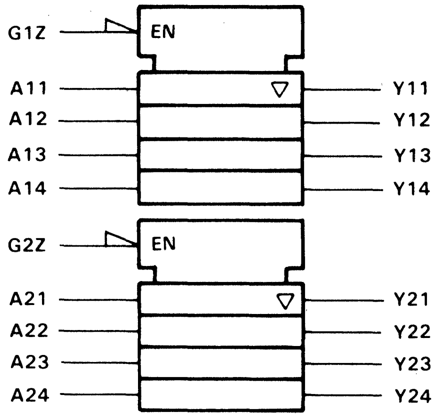
SOFTWARE MACRO

- **3-State Outputs Interface Internal Data Buses Directly**
- **Active-Low Enables for Expandability**
- **Use Bus Interfaces in Parallel for Wide Words**

description

The S244LJ gate-array software macro implements an octal internal 3-state bus buffer. The macro is organized as dual 4-bit drivers with individual enables, G1Z and G2Z, that enable and disable the 3-state outputs to permit interfacing the internal bus directly in either a parallel or word mode. The Y outputs are in a high-impedance state when GZ is high. When GZ is low, the outputs drive the bus lines. The S244LJ is implemented with the macro functions indicated.

logic symbol†



Equivalent to 74244

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
BU130LJ	2	2	4	1.84
IV110LJ	1	8	8	1.68
IV211LJ	2	8	16	3.04
TOTALS		18	28	6.56

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S244LJ A11,A12,A13,A14,G1Z,A21,A22,A23,A24,G2Z,
Y11,Y12,Y13,Y14,Y21,Y22,Y23,Y24;

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S244LJ
OCTAL INTERNAL BUS BUFFER WITH 3-STATE OUTPUTS

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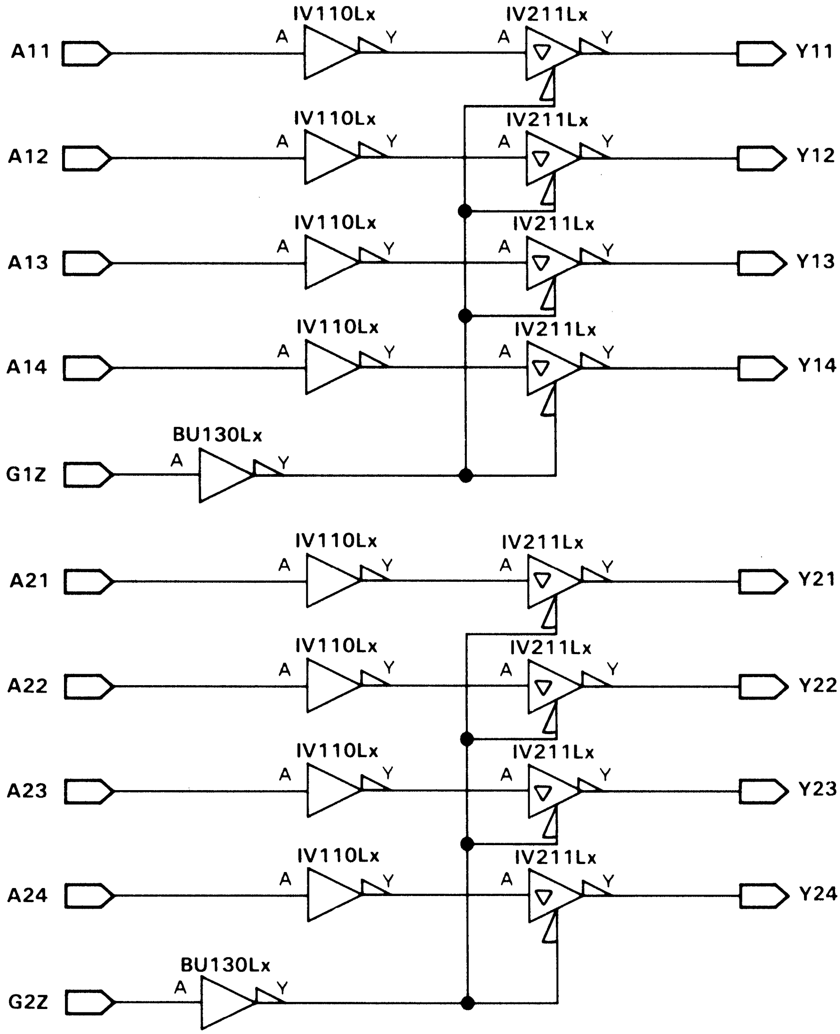
logic diagram



Lx = LJ for 1-μm gate arrays

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	G1Z,G2Z		0.15		pF
		All others		0.07		
C_o	Output capacitance			0.08		pF
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	6.56		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Notes 1 and 2), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y		0.9	1.5	ns
t_{PHL}				1	1.6	
t_{PZH}	GZ	Y		1.1	2.1	ns
t_{PZL}				1.2	2.3	
t_{PHZ}	GZ	Y		2.5	3.2	ns
t_{PLZ}				1.9	2.6	
Δt_{PLH}	Any	Y	0.38	0.96	1.9	ns/pF
Δt_{PHL}			0.32	0.64	1.26	
Δt_{PZH}	Any	Y	0.18	0.86	1.76	ns/pF
Δt_{PZL}			0.24	0.62	1.26	

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.
2. Enable and delta-enable times are measured using the conditions specified for the IV211LJ.

GATES
FUNCTIONAL INDEX

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AND GATES

DESCRIPTION	CELL NAME	CELLS USED	OUTPUT DRIVE	PAGE
2-Input AND	AN210LJ	2	1X	8-3
	AN220LJ	2	2X	8-4
3-Input AND	AN310LJ	2	1X	8-5
	AN320LJ	3	2X	8-6
4-Input AND	AN410LJ	3	1X	8-7
	AN420LJ	3	2X	8-8
5-Input AND	AN510LJ	3	1X	8-9
8-Input AND	AN810LJ	5	1X	8-10

AND-OR/AND-NOR GATES

DESCRIPTION	CELL NAME	CELLS USED	OUTPUT DRIVE	PAGE
AND-OR	AO220LJ	3	2X	8-11
AND-NOR	AO221LJ	2	1X	8-12
AND-NOR	AO241LJ	4	1X	8-13
AND-OR	AO320LJ	4	1X	8-14
AND-NOR	AO421LJ	4	1X	8-15

HARDWIRED MULTI-STAGE GATES

DESCRIPTION	CELL NAME	CELLS USED	OUTPUT DRIVE	PAGE
AND-NOR	BF001LJ	2	1X	8-16
	BF006LJ	2	1X	8-17
	BF011LJ	3	1X	8-19
OR-AND-NOR	BF022LJ	3	1X	8-20
OR-NAND	BF051LJ	2	1X	8-22
	BF053LJ	2	1X	8-23
	BF056LJ	2	1X	8-24
OR-AND/OR-NAND	OA220LJ	3	1X	8-51
	OA231LJ	3	1X	8-52
	OA241LJ	4	1X	8-53

EX-NOR/EX-OR GATES

DESCRIPTION	CELL NAME	CELLS USED	OUTPUT DRIVE	PAGE
EX-NOR/EX-OR	EN210LJ	3	1X	8-25
	EX210LJ	3	1X	8-26
	EX220LJ	4	2X	8-27

TEXAS INSTRUMENTS

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NAND GATES

DESCRIPTION	CELL NAME	CELLS USED	OUTPUT DRIVE	PAGE
2-Input NAND	NA210LJ	1	1X	8-28
	NA220LJ	2	2X	8-29
3-Input NAND	NA310LJ	2	1X	8-30
	NA311LJ	2	1X	8-31
	NA320LJ	3	2X	8-32
4-Input NAND	NA410LJ	2	1X	8-33
	NA420LJ	4	2X	8-34
5-Input NAND	NA510LJ	3	1X	8-35
	NA520LJ	5	2X	8-36
8-Input NAND	NA810LJ	6	1X	8-37
	NA820LJ	6	2X	8-38

NOR GATES

DESCRIPTION	CELL NAME	CELLS USED	OUTPUT DRIVE	PAGE
2-Input NOR	NO210LJ	1	1X	8-39
	NO220LJ	2	2X	8-40
3-Input NOR	NO310LJ	2	1X	8-41
	NO320LJ	3	2X	8-42
4-Input NOR	NO410LJ	4	1X	8-43
	NO420LJ	4	2X	8-44
5-Input NOR	NO510LJ	4	1X	8-45
	NO520LJ	5	2X	8-46
8-Input NOR	NO810LJ	6	1X	8-47
	NO820LJ	6	2X	8-49

OR GATES

DESCRIPTION	CELL NAME	CELLS USED	OUTPUT DRIVE	PAGE
2-Input OR	OR210LJ	2	1X	8-54
	OR220LJ	2	2X	8-55
3-Input OR	OR310LJ	2	1X	8-56
	OR320LJ	3	2X	8-57
4-Input OR	OR410LJ	3	1X	8-58
	OR420LJ	3	2X	8-59
5-Input OR	OR510LJ	4	1X	8-60
8-Input OR	OR810LJ	5	1X	8-61

TEXAS INSTRUMENTS
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TGC100 SERIES

AN210LJ 2-INPUT POSITIVE-AND GATE

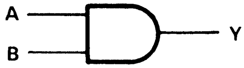
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS		OUTPUT
A	**B**	**Y**
H	H	H
L	X	L
X	L	L

logic symbol†



Equivalent to 1/4 7408

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \bullet B = \overline{A + B}$

description

The AN210LJ is a minimum-power, 2-input positive-AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN210LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.1		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.44		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B	Y	0.22	0.48	0.89	ns
t_{PHL}			0.26	0.54	1.07	
Δt_{PLH}	A,B	Y	0.34	0.88	1.72	ns/pF
Δt_{PHL}			0.24	0.49	0.88	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
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AN220LJ 2-INPUT POSITIVE-AND GATE WITH 2X OUTPUT

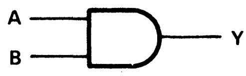
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS		OUTPUT
A	**B**	**Y**
H	H	H
L	X	L
X	L	L

logic symbol†



Equivalent to 1/4 7408

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \bullet B = \overline{A + B}$

description

The AN220LJ is a 2-input positive-AND gate featuring twice the capacitive-drive capability when compared to the AN210LJ AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN220LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.1		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.6		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B	Y	0.25	0.55	1.02	ns
t_{PHL}			0.26	0.6	1.19	
Δt_{PLH}	A,B	Y	0.16	0.44	0.88	ns/pF
Δt_{PHL}			0.12	0.3	0.56	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

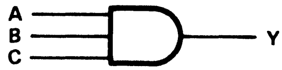
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol†



Equivalent to 1/3 7411

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \bullet B \bullet C = \overline{\overline{A}+\overline{B}+\overline{C}}$

description

The AN310LJ is a minimum-size, 3-input positive-AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN310LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.3		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.56		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C	Y	0.26	0.65	1.33	ns
t_{PHL}			0.27	0.65	1.36	
Δt_{PLH}	A,B,C	Y	0.36	0.89	1.72	ns/pF
Δt_{PHL}			0.24	0.5	0.94	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS

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AN320LJ
3-INPUT POSITIVE-AND GATE WITH 2X OUTPUT

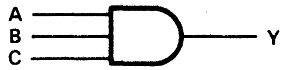
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol†



Equivalent to 1/3 7411

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \bullet B \bullet C = \overline{\overline{A} + \overline{B} + \overline{C}}$

description

The AN320LJ is a 3-input positive-AND gate featuring twice the capacitive-drive capability when compared to the AN310LJ AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN320LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.3		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.73		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C	Y	0.28	0.71	1.42	ns
t_{PHL}			0.28	0.67	1.43	
Δt_{PLH}	A,B,C	Y	0.19	0.46	0.92	ns/pF
Δt_{PHL}			0.13	0.31	0.59	

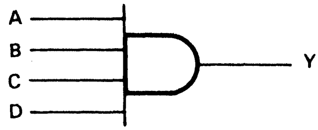
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

logic symbol†



Equivalent to 1/2 7421

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \bullet B \bullet C \bullet D = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}}$

description

The AN410LJ is a minimum-power, 4-input positive-AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN410LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.4		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.57		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C,D	Y	0.31	0.77	1.66	ns
t_{PHL}			0.25	0.67	1.46	
Δt_{PLH}	A,B,C,D	Y	0.35	0.9	1.76	ns/pF
Δt_{PHL}			0.25	0.52	0.98	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AN420LJ
4-INPUT POSITIVE-AND GATE WITH 2X OUTPUT

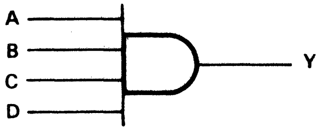
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

logic symbol†



Equivalent to 1/2 7421

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \bullet B \bullet C \bullet D = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}}$

description

The AN420LJ is a 4-input positive-AND gate featuring twice the capacitive-drive capability when compared to the AN410LJ AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN420LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.4		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.83		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C,D	Y	0.34	0.87	1.86	ns
t_{PHL}			0.27	0.7	1.54	
Δt_{PLH}	A,B,C,D	Y	0.18	0.48	0.97	ns/pF
Δt_{PHL}			0.13	0.33	0.65	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

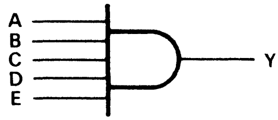
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
H	H	H	H	H	H
L	X	X	X	X	L
X	L	X	X	X	L
X	X	L	X	X	L
X	X	X	L	X	L
X	X	X	X	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \bullet B \bullet C \bullet D \bullet E = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}+\overline{E}}$

description

The AN510LJ is a minimum-size, 5-input positive-AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN510LJ A,B,C,D,E,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.5		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.65		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C,D,E	Y	0.36	0.99	2.27	ns
t_{PHL}			0.25	0.74	1.67	
Δt_{PLH}	A,B,C,D,E	Y	0.36	0.92	1.83	ns/pF
Δt_{PHL}			0.26	0.54	1.03	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
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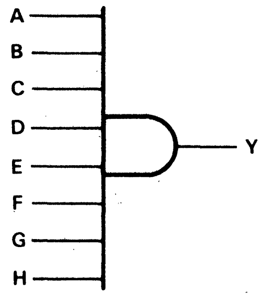
INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS								OUTPUT
A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**Y**
H	H	H	H	H	H	H	H	H
L	X	X	X	X	X	X	X	L
X	L	X	X	X	X	X	X	L
X	X	L	X	X	X	X	X	L
X	X	X	L	X	X	X	X	L
X	X	X	X	L	X	X	X	L
X	X	X	X	X	L	X	X	L
X	X	X	X	X	X	L	X	L
X	X	X	X	X	X	X	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A{\bullet}B{\bullet}C{\bullet}D{\bullet}E{\bullet}F{\bullet}G{\bullet}H = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}+\overline{E}+\overline{F}+\overline{G}+\overline{H}}$

description

The AN810LJ is a minimum-size, 8-input positive-AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN810LJ A,B,C,D,E,F,G,H,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.4		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.94		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A thru H	Y	0.34	0.88	1.89	ns
t_{PHL}			0.25	0.7	1.54	
Δt_{PLH}	A thru H	Y	0.62	1.69	3.41	ns/pF
Δt_{PHL}			0.26	0.52	0.98	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS

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AO220LJ AND-OR GATE WITH 2X OUTPUT $Y = (A \bullet B) + (C \bullet D)$

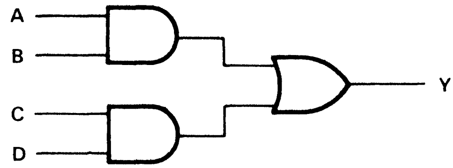
D3015, OCTOBER 1987

INTERNAL MACRO

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	X	X	H
X	X	H	H	H
Any other combination				L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = (A \bullet B) + (C \bullet D)$

description

The AO220LJ is a 2-wide, 2-input AND-OR gate CMOS macro featuring a 2X output-drive capability to enhance its performance. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AO220LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.76		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C,D	Y	0.24	0.62	1.28	ns
t_{PHL}			0.35	0.97	2.35	
Δt_{PLH}	A,B,C,D	Y	0.16	0.46	0.9	ns/pF
Δt_{PHL}			0.16	0.38	0.74	

§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

AO221LJ AND-NOR GATE WITH 1X OUTPUT

$Y = \overline{(A \bullet B) + (C \bullet D)}$

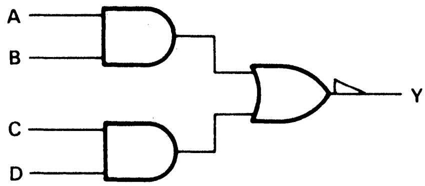
D3015, OCTOBER 1987

INTERNAL MACRO

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	X	X	L
X	X	H	H	L
Any other combination				H

logic symbol†



Similar to 1/2 7451

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A \bullet B) + (C \bullet D)}$

description

The AO221LJ is a 2-wide, 2-input AND-NOR gate CMOS macro with a 1X output. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AO221LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.28		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C,D	Y	0.25	0.5	1.25	ns
t_{PHL}			0.17	0.38	0.7	
Δt_{PLH}	A,B,C,D	Y	0.58	1.68	3.42	ns/pF
Δt_{PHL}			0.34	0.75	1.5	

§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

AO241LJ
AND-NOR GATE WITH 1X OUTPUT
$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2) + (D1 \cdot D2)}$

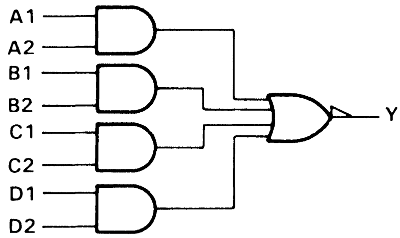
D3015, OCTOBER 1987 – REVISED OCTOBER 1988

INTERNAL MACRO

FUNCTION TABLE

INPUTS								OUTPUT
A1	A2	B1	B2	C1	C2	D1	D2	Y
H	H	X	X	X	X	X	X	L
X	X	H	H	X	X	X	X	L
X	X	X	X	H	H	X	X	L
X	X	X	X	X	X	H	H	L
Any other combination								H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2) + (D1 \cdot D2)}$

description

The AO241LJ is a 4-wide, 2-input AND-NOR gate CMOS macro with a 1X output. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AO241LJ A1,A2,B1,B2,C1,C2,D1,D2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	1.36		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	Any	Y	0.46	1.23	3.15	ns
t_{PHL}			0.3	0.92	1.95	
Δt_{PLH}	Any	Y	0.16	0.44	0.88	ns/pF
Δt_{PHL}			0.12	0.3	0.59	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AO320LJ
2-WIDE, 3-INPUT AND-OR GATE WITH 1X OUTPUT
Y = (A1•A2•A3) + (B1•B2•B3)

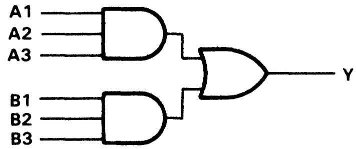
D3015, OCTOBER 1988

INTERNAL MACRO

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	A3	B1	B2	B3	Y
H	H	H	X	X	X	H
X	X	X	H	H	H	H
Any other combination						L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = (A1•A2•A3) + (B1•B2•B3)

description

The AO320LJ is a 2-wide, 3-input AND-OR gate with a 1X output. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AO320LJ A1,A2,A3,B1,B2,B3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.6		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	Any	Y	0.26	0.8	1.82	ns
t_{PHL}			0.38	1.06	2.84	
Δt_{PLH}	Any	Y	0.36	0.89	1.78	ns/pF
Δt_{PHL}			0.28	0.63	1.22	

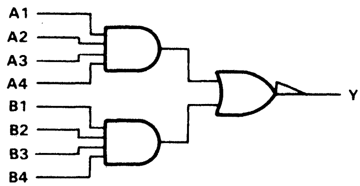
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AO421LJ
2-WIDE, 4-INPUT AND-NOR GATE WITH 1X OUTPUT
$Y = \overline{(A1 \cdot A2 \cdot A3 \cdot A4) + (B1 \cdot B2 \cdot B3 \cdot B4)}$

D3015, OCTOBER 1988

INTERNAL MACRO

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

FUNCTION TABLE

INPUTS								OUTPUT
A1	A2	A3	A4	B1	B2	B3	B4	Y
H	H	H	H	X	X	X	X	L
X	X	X	X	H	H	H	H	L
Any other combination								H

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2 \cdot A3 \cdot A4) + (B1 \cdot B2 \cdot B3 \cdot B4)}$

description

The AO421LJ is a 2-wide, 4-input AND-NOR gate with a 1X output. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AO421LJ A1,A2,A3,A4,B1,B2,B3,B4,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.9		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.38		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	Any	Y	0.23	0.72	2.13	ns
t_{PHL}			0.24	0.62	1.63	
Δt_{PLH}	Any	Y	0.6	1.67	3.43	ns/pF
Δt_{PHL}			0.45	1.3	1.63	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TGC100 SERIES

BF001LJ AND-NOR GATE

$Y = \overline{A1 + (B1 \bullet B2)}$

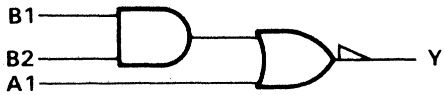
D3015, OCTOBER 1987

INTERNAL MACRO

FUNCTION TABLE

INPUTS			OUTPUT
A1	B1	B2	Y
H	X	X	L
X	H	H	L
L	L	X	H
L	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 + (B1 \bullet B2)}$

description

The BF001LJ is an expandable 1-2-input AND-NOR CMOS macro. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF001LJ A1,B1,B2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.19		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A1	Y	0.25	0.31	0.46	ns
t_{PHL}			0.09	0.28	0.42	
t_{PLH}	B1,B2	Y	0.2	0.46	1.12	ns
t_{PHL}			0.19	0.37	0.59	
Δt_{PLH}	Any	Y	0.6	1.67	3.4	ns/pF
Δt_{PHL}			0.34	0.67	1.46	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF006LJ AND-NOR GATE $Y = \overline{A1 + A2 + (B1 \cdot B2)}$

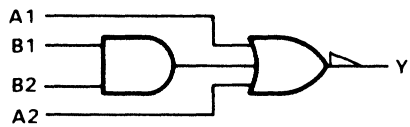
D3015, OCTOBER 1988

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS				OUTPUT
A1	A2	B1	B2	Y
H	X	X	X	L
X	H	X	X	L
X	X	H	H	L
L	L	L	X	H
L	L	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 + A2 + (B1 \cdot B2)}$

description

The BF006LJ is a 1-1-2-input AND-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF006LJ A1,A2,B1,B2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.18		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	Any A	Y	0.29	0.48	1.05	ns
t_{PHL}			0.08	0.32	0.5	
t_{PLH}	Any B	Y	0.25	0.72	1.77	ns
t_{PHL}			0.19	0.39	0.63	
Δt_{PLH}	Any A	Y	0.85	2.47	5.1	ns/pF
Δt_{PHL}			0.34	0.5	0.84	
Δt_{PLH}	Any B	Y	0.89	2.51	5.08	ns/pF
Δt_{PHL}			0.35	0.78	1.53	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

BF011LJ
AND-NOR GATE
$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2)}$

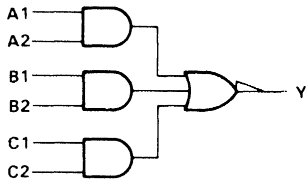
D3015, OCTOBER 1987

INTERNAL MACRO

FUNCTION TABLE

INPUTS						OUTPUT
A1	**A2**	**B1**	**B2**	**C1**	**C2**	**Y**
H	H	X	X	X	X	L
X	X	H	H	X	X	L
X	X	X	X	H	H	L
Any other combination						H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2)}$

description

The BF011LJ is a 3-wide, 2-input AND-NOR CMOS macro. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF011LJ A1,A2,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.7		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.34		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	Any	Y	0.31	0.8	2.39	ns
t_{PHL}			0.18	0.42	0.77	
Δt_{PLH}	Any	Y	0.84	2.5	5.12	ns/pF
Δt_{PHL}			0.34	0.76	1.58	

§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

BF022LJ
OR-AND-NOR GATE
$Y = \overline{A1 \cdot A2 + [B1 \cdot B2 \cdot (C1 + C2)]}$

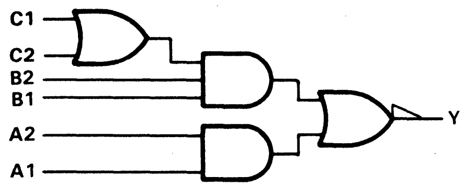
D3015, OCTOBER 1987 – REVISED FEBRUARY 1989

INTERNAL MACRO

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	B1	B2	C1	C2	Y
H	H	X	X	X	X	L
X	X	H	H	H	X	L
X	X	H	H	X	H	L
Any other combination						H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot A2 + [B1 \cdot B2 \cdot (C1 + C2)]}$

description

The BF022LJ is a 2-wide, 2-3-input sum-of-products AND-NOR CMOS macro. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF022LJ A1,A2,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.31		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	Any A	Y	0.35	0.8	1.8	ns
t_{PHL}			0.19	0.38	0.55	
t_{PLH}	Any B	Y	0.24	0.61	1.39	ns
t_{PHL}			0.26	0.52	0.97	
t_{PLH}	Any C	Y	0.38	1.19	2.69	ns
t_{PHL}			0.22	0.53	1.07	
Δt_{PLH}	Any A	Y	0.86	2.49	5.1	ns/pF
Δt_{PHL}			0.34	0.74	1.48	
Δt_{PLH}	Any B	Y	0.62	1.7	3.38	ns/pF
Δt_{PHL}			0.38	1.04	2.12	
Δt_{PLH}	Any C	Y	0.9	2.51	5.02	ns/pF
Δt_{PHL}			0.4	1.05	2.2	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

BF051LJ
OR-NAND GATE
$Y = \overline{A1 \cdot (B1 + B2)}$

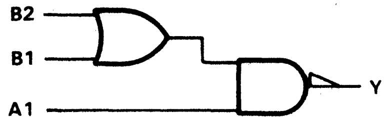
D3015, OCTOBER 1987 – REVISED FEBRUARY 1989

INTERNAL MACRO

FUNCTION TABLE

INPUTS			OUTPUT
A1	B1	B2	Y
H	H	X	L
H	X	H	L
L	X	X	H
X	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot (B1+B2)}$

description

The BF051LJ is a 2-wide, 1-2-input OR-NAND CMOS macro. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF051LJ A1,B1,B2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.27		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A1	Y	0.2	0.27	0.38	ns
t_{PHL}			0.19	0.33	0.44	
t_{PLH}	Any B	Y	0.24	0.49	1.07	ns
t_{PHL}			0.16	0.33	0.58	
Δt_{PLH}	A1	Y	0.34	0.86	1.7	ns/pF
Δt_{PHL}			0.36	0.72	1.44	
Δt_{tPLH}	Any B	Y	0.58	1.68	3.4	ns/pF
Δt_{PHL}			0.34	0.74	1.48	

§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

BF053LJ
OR-NAND GATE
$Y = \overline{(A1 + A2) \cdot (B1 + B2)}$

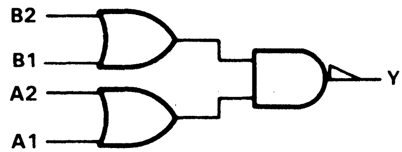
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

INTERNAL MACRO

FUNCTION TABLE

INPUTS				OUTPUT
A1	A2	B1	B2	Y
H	X	H	X	L
H	X	X	H	L
X	H	H	X	L
X	H	X	H	L
L	L	X	X	H
X	X	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1+A2) \cdot (B1+B2)}$

description

The BF053LJ is a 2-wide, 2-input OR-NAND gate CMOS macro. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF053LJ A1,A2,B1,B2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.3		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	Any	Y	0.21	0.52	1.32	ns
t_{PHL}			0.19	0.38	0.69	
Δt_{PLH}	Any	Y	0.6	1.69	3.42	ns/pF
Δt_{PHL}			0.34	0.74	1.46	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

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BF056LJ
OR-NAND GATE
$Y = \overline{A1 \cdot A2 \cdot (B1 + B2)}$

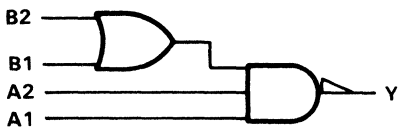
D3015, OCTOBER 1988

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS				OUTPUT
A1	A2	B1	B2	Y
H	H	H	X	L
H	H	X	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot A2 \cdot (B1 + B2)}$

description

The BF056LJ is an expandable 3-wide, 1-1-2-input OR-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF056LJ A1,A2,B1,B2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.26		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	Any A	Y	0.19	0.33	0.57	ns
t_{PHL}			0.23	0.39	0.62	
t_{PLH}	Any B	Y	0.27	0.63	1.39	ns
t_{PHL}			0.19	0.42	0.86	
Δt_{PLH}	Any A	Y	0.34	0.87	1.71	ns/pF
Δt_{PHL}			0.38	0.99	2.05	
$\Delta_t t_{PLH}$	Any B	Y	0.59	1.68	3.4	ns/pF
Δt_{PHL}			0.38	1	2.06	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

EN210LJ
2-INPUT EXCLUSIVE-NOR GATE

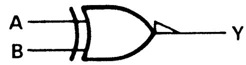
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS		OUTPUT
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	H

logic symbol†



Similar to 1/4 74266

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \oplus B} = A \cdot B + \overline{A} \cdot \overline{B}$

description

The EN210LJ is a minimum-size, 2-input exclusive-NOR gate CMOS function. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: EN210LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.17		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.52		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A or B	Y	0.23	0.57	1.09	ns
t_{PHL}			0.32	0.85	2.02	
Δt_{PLH}	A or B	Y	0.34	0.89	1.72	ns/pF
Δt_{PHL}			0.26	0.57	1.06	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

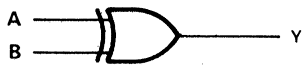
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†



Equivalent to 1/4 7486

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \oplus B = \overline{A} \cdot B + A \cdot \overline{B}$

description

The EX210LJ is a minimum-size, 2-input exclusive-OR gate CMOS function. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: EX210LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.17		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.76		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A or B	Y	0.35	0.81	1.6	ns
t_{PHL}			0.29	0.75	1.48	
Δt_{PLH}	A or B	Y	0.36	0.89	1.72	ns/pF
Δt_{PHL}			0.24	0.5	0.9	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TGC100 SERIES

EX220LJ 2-INPUT EXCLUSIVE-OR GATE WITH 2X OUTPUT

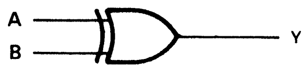
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†



Equivalent to 1/4 7486

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \oplus B = \overline{A} \cdot B + A \cdot \overline{B}$

description

The EX220LJ is a 2-input exclusive-OR gate CMOS function featuring twice the capacitive-drive capability when compared to the EX210LJ exclusive-OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: EX220LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.16		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	1.1		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A or B	Y	0.37	0.86	1.75	ns
t_{PHL}			0.29	0.81	1.61	
Δt_{PLH}	A or B	Y	0.18	0.45	0.88	ns/pF
Δt_{PHL}			0.16	0.3	0.56	

§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NA210LJ
2-INPUT POSITIVE-NAND GATE

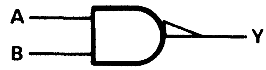
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



Equivalent to 1/4 7400

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \bullet B} = \overline{A} + \overline{B}$

description

The NA210LJ is a minimum-power, 2-input positive-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA210LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.1		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.27		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A or B	Y	0.19	0.3	0.52	ns
t_{PHL}			0.17	0.33	0.47	
Δt_{PLH}	A or B	Y	0.34	0.87	1.7	ns/pF
Δt_{PHL}			0.34	0.72	1.44	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA220LJ
2-INPUT POSITIVE-NAND GATE WITH 2X OUTPUT

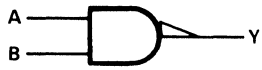
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



Equivalent to 1/4 7400

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \cdot B} = \overline{A} + \overline{B}$

description

The NA220LJ is a 2-input positive-NAND gate featuring twice the capacitive-drive capability when compared to the NA210LJ NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA220LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.1		V
C_i	Input capacitance		0.15		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.52		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A or B	Y	0.15	0.29	0.5	ns
t_{PHL}			0.1	0.28	0.46	
Δt_{PLH}	A or B	Y	0.2	0.43	0.84	ns/pF
Δt_{PHL}			0.24	0.39	0.72	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA310LJ 3-INPUT POSITIVE-NAND GATE

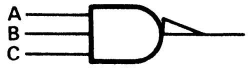
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol†



Equivalent to 1/3 7410

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \bullet B \bullet C} = \overline{A} + \overline{B} + \overline{C}$

description

The NA310LJ is a minimum-power, 3-input positive-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA310LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.3		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.28		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C	Y	0.21	0.36	0.73	ns
t_{PHL}			0.2	0.4	0.72	
Δt_{PLH}	A,B,C	Y	0.34	0.88	1.72	ns/pF
Δt_{PHL}			0.38	0.99	2.04	

§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NA311LJ
3-INPUT NAND GATE
WITH ACTIVE-LOW INPUT

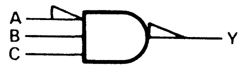
D3015, OCTOBER 1988

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	H	H	L
H	X	X	H
X	L	X	H
X	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{\overline{A} \cdot B \cdot C} = A + \overline{B} + \overline{C}$

description

The NA311LJ is a 3-input NAND gate with active-low A input. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA311LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.6		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C	Y	0.17	0.38	0.78	ns
t_{PHL}			0.2	0.46	1.09	
Δt_{PLH}	A,B,C	Y	0.34	0.88	1.72	ns/pF
Δt_{PHL}			0.37	0.99	2.05	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
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NA320LJ
3-INPUT POSITIVE-NAND GATE WITH 2X OUTPUT

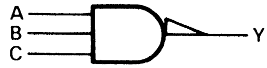
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol†



Equivalent to 1/3 7410

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \cdot B \cdot C} = \overline{A} + \overline{B} + \overline{C}$

description

The NA320LJ is 3-input positive-NAND gate featuring twice the capacitive-drive capability when compared to the NA310LJ NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA320LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.3		V
C_i	Input capacitance		0.15		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.52		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C	Y	0.14	0.34	0.65	ns
t_{PHL}			0.16	0.36	0.61	
Δt_{PLH}	A,B,C	Y	0.2	0.44	0.86	ns/pF
Δt_{PHL}			0.22	0.5	1.04	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
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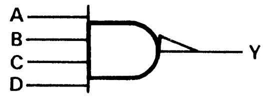
INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol†



Equivalent to 1/2 7420

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \bullet B \bullet C \bullet D} = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

description

The NA410LJ is a minimum-size, 4-input positive-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA410LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.4		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.29		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C,D	Y	0.19	0.4	0.82	ns
t_{PHL}			0.21	0.46	0.95	
Δt_{PLH}	A,B,C,D	Y	0.34	0.88	1.74	ns/pF
Δt_{PHL}			0.44	1.27	2.66	

§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NA420LJ
4-INPUT POSITIVE-NAND GATE WITH 2X OUTPUT

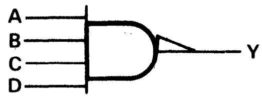
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol†



Equivalent to 1/2 7420

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \bullet B \bullet C \bullet D} = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

description

The NA420LJ is a 4-input positive-NAND gate featuring twice the capacitive-drive capability when compared to the NA410LJ NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA420LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.4		V
C_i	Input capacitance		0.15		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.56		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C,D	Y	0.14	0.38	0.77	ns/pF
t_{PHL}			0.2	0.44	0.92	
Δt_{PLH}	A,B,C,D	Y	0.18	0.44	0.9	ns/pF
Δt_{PHL}			0.22	0.64	1.34	

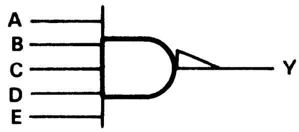
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
H	H	H	H	H	L
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \bullet B \bullet C \bullet D \bullet E} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E}$

description

The NA510LJ is a minimum-size, 5-input positive-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA510LJ A,B,C,D,E,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.5		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.34		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A thru E	Y	0.2	0.46	1.01	ns
t_{PHL}			0.26	0.61	1.43	
Δt_{PLH}	A thru E	Y	0.34	0.88	1.76	ns/pF
Δt_{PHL}			0.5	1.56	3.3	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA520LJ
5-INPUT POSITIVE-NAND GATE WITH 2X OUTPUT

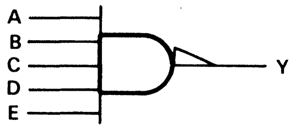
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
H	H	H	H	H	L
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \bullet B \bullet C \bullet D \bullet E} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E}$

description

The NA520LJ is a 5-input positive-NAND gate featuring twice the capacitive-drive capability when compared to the NA510LJ NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA520LJ A,B,C,D,E,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5\ V$, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.5		V
C_i	Input capacitance		0.15		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.6		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A thru E	Y	0.14	0.42	0.89	ns
t_{PHL}			0.24	0.56	1.26	
Δt_{PLH}	A thru E	Y	0.18	0.45	0.92	ns/pF
Δt_{PHL}			0.25	0.78	1.66	

§ Typical values are at $V_{CC} = 5\ V$, $T_A = 25°C$.

TEXAS INSTRUMENTS
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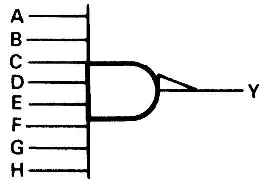
INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H

logic symbol†



Equivalent to 7430

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$

description

The NA810LJ is a minimum-power, 8-input positive-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA810LJ A,B,C,D,E,F,G,H,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.4		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	1.2		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A thru H	Y	0.27	0.85	1.86	ns
t_{PHL}			0.46	1.26	2.75	
Δt_{PLH}	A thru H	Y	0.34	0.88	1.72	ns/pF
Δt_{PHL}			0.24	0.55	1.02	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA820LJ
8-INPUT POSITIVE-NAND GATE WITH 2X OUTPUT

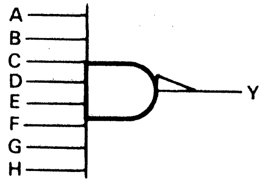
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H

logic symbol†



Equivalent to 7430

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$

description

The NA820LJ is an 8-input positive-NAND gate featuring twice the capacitive-drive capability when compared to the NA810LJ NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA820LJ A,B,C,D,E,F,G,H,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.4		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	1.7		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A thru H	Y	0.31	0.9	1.97	ns
t_{PHL}			0.48	1.36	3.04	
Δt_{PLH}	A thru H	Y	0.16	0.44	0.86	ns/pF
Δt_{PHL}			0.16	0.37	0.7	

§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NO210LJ 2-INPUT POSITIVE-NOR GATE

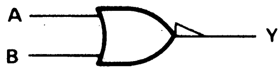
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†



Equivalent to 1/4 7402

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A+B} = \overline{A} \cdot \overline{B}$

description

The NO210LJ is a minimum-size, 2-input positive-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO210LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.18		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A or B	Y	0.21	0.35	0.67	ns
t_{PHL}			0.09	0.31	0.49	
Δt_{PLH}	A or B	Y	0.58	1.67	3.4	ns/pF
Δt_{PHL}			0.34	0.5	0.82	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

NO220LJ 2-INPUT POSITIVE-NOR GATE WITH 2X OUTPUT

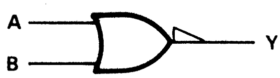
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†



Equivalent to 1/4 7402

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A+B} = \overline{A} \bullet \overline{B}$

description

The NO220LJ is a 2-input positive-NOR gate featuring twice the capacitive-drive capability when compared to the NO210LJ NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO220LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.15		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.3		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A or B	Y	0.22	0.35	0.62	ns
t_{PHL}			0.02	0.23	0.43	
Δt_{PLH}	A or B	Y	0.29	0.82	1.72	ns/pF
Δt_{PHL}			0.22	0.32	0.45	

§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

TEXAS INSTRUMENTS
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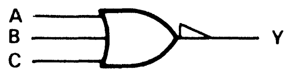
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

logic symbol†



Equivalent to 1/3 7427

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A+B+C} = \overline{A} \bullet \overline{B} \bullet \overline{C}$

description

The NO310LJ is a minimum-size, 3-input positive-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO310LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.7		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.21		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C	Y	0.27	0.57	1.45	ns
t_{PHL}			0.1	0.34	0.51	
Δt_{PLH}	A,B,C	Y	0.84	2.48	5.1	ns/pF
Δt_{PHL}			0.34	0.49	0.88	

§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NO320LJ
3-INPUT POSITIVE-NOR GATE WITH 2X OUTPUT

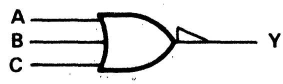
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

logic symbol†



Equivalent to 1/3 7427

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A+B+C} = \overline{A} \bullet \overline{B} \bullet \overline{C}$

description

The NO320LJ is a 3-input positive-NOR gate featuring twice the capacitive-drive capability when compared to the NO310LJ NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO320LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.7		V
C_i	Input capacitance		0.15		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.34		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C	Y	0.25	0.49	1.22	ns
t_{PHL}			0.03	0.25	0.47	
Δt_{PLH}	A,B,C	Y	0.41	1.23	2.58	ns/pF
Δt_{PHL}			0.23	0.31	0.45	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

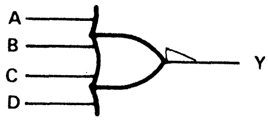
D3015, OCTOBER 1987 – REVISED OCTOBER 1988

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L
L	L	L	L	H

logic symbol†



Equivalent to 1/2 4002

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A+B+C+D} = \overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}$

description

The NO410LJ is a minimum-size, 4-input positive-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO410LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.96		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C,D	Y	0.4	0.95	1.95	ns
t_{PHL}			0.22	0.68	1.47	
Δt_{PLH}	A,B,C,D	Y	0.36	0.88	1.71	ns/pF
Δt_{PHL}			0.22	0.49	0.88	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TGC100 SERIES

NO420LJ 4-INPUT POSITIVE-NOR GATE WITH 2X OUTPUT

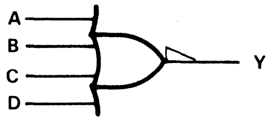
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L
L	L	L	L	H

logic symbol†



Equivalent to 1/2 4002

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A+B+C+D} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$

description

The NO420LJ is a 4-input positive-NOR gate featuring twice the capacitive-drive capability when compared to the NO410LJ NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO420LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	1.2		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C,D	Y	0.39	1.02	2.15	ns
t_{PHL}			0.22	0.74	1.61	
Δt_{PLH}	A,B,C,D	Y	0.17	0.45	0.87	ns/pF
Δt_{PHL}			0.11	0.3	0.59	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

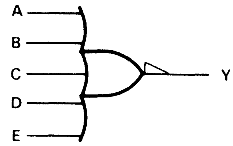
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
L	L	L	L	L	H

logic symbol†



Equivalent to 1/2 74260

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A+B+C+D+E} = \overline{A}\bullet\overline{B}\bullet\overline{C}\bullet\overline{D}\bullet\overline{E}$

description

The NO510LJ is a minimum-size, 5-input positive-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO510LJ A,B,C,D,E,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.7		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.96		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C,D,E	Y	0.41	1.19	3.12	ns
t_{PHL}			0.23	0.71	1.5	
Δt_{PLH}	A,B,C,D,E	Y	0.36	0.88	1.7	ns/pF
Δt_{PHL}			0.22	0.5	0.9	

§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NO520LJ
5-INPUT POSITIVE-NOR GATE WITH 2X OUTPUT

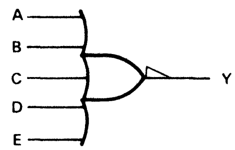
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
L	L	L	L	L	H

logic symbol†



Equivalent to 1/2 74260

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A+B+C+D+E} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E}$

description

The NO520LJ is a 5-input positive-NOR gate featuring twice the capacitive-drive capability when compared to the NO510LJ NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO520LJ A,B,C,D,E,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.7		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	1.25		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C,D,E	Y	0.41	1.22	3.08	ns
t_{PHL}			0.24	0.77	1.66	
Δt_{PLH}	A,B,C,D,E	Y	0.17	0.45	0.88	ns/pF
Δt_{PHL}			0.11	0.3	0.58	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NO810LJ
8-INPUT POSITIVE-NOR GATE

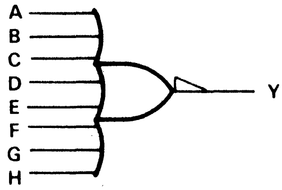
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
H	X	X	X	X	X	X	X	L
X	H	X	X	X	X	X	X	L
X	X	H	X	X	X	X	X	L
X	X	X	H	X	X	X	X	L
X	X	X	X	H	X	X	X	L
X	X	X	X	X	H	X	X	L
X	X	X	X	X	X	H	X	L
X	X	X	X	X	X	X	H	L
L	L	L	L	L	L	L	L	H

logic symbol†



Equivalent to 4078

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A+B+C+D+E+F+G+H} = \overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}\cdot\overline{E}\cdot\overline{F}\cdot\overline{G}\cdot\overline{H}$

description

The NO810LJ is a minimum-power, 8-input positive-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO810LJ A,B,C,D,E,F,G,H,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.6		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	1.3		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	A thru H	Y	0.55	1.63	4.23	ns
t_{PHL}			0.21	0.75	1.56	
Δt_{PLH}	A thru H	Y	0.36	0.89	1.72	ns/pF
Δt_{PHL}			0.24	0.49	0.9	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NO820LJ
8-INPUT POSITIVE-NOR GATE
WITH 2X OUTPUT

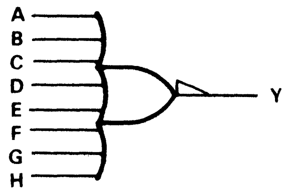
D3015, OCTOBER 1987

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
H	X	X	X	X	X	X	X	L
X	H	X	X	X	X	X	X	L
X	X	H	X	X	X	X	X	L
X	X	X	H	X	X	X	X	L
X	X	X	X	H	X	X	X	L
X	X	X	X	X	H	X	X	L
X	X	X	X	X	X	H	X	L
X	X	X	X	X	X	X	H	L
L	L	L	L	L	L	L	L	H

logic symbol†



Equivalent to 4078

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A+B+C+D+E+F+G+H} = \overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}\cdot\overline{E}\cdot\overline{F}\cdot\overline{G}\cdot\overline{H}$

description

The NO820LJ is an 8-input positive-NOR gate featuring twice the capacitive-drive capability when compared to the NO810LJ NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO820LJ A,B,C,D,E,F,G,H,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.6		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	1.4		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	A thru H	Y	0.58	1.72	4.49	ns
t_{PHL}			0.23	0.81	1.7	
Δt_{PLH}	A thru H	Y	0.18	0.45	0.9	ns/pF
Δt_{PHL}			0.12	0.3	0.56	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

OA220LJ
2-WIDE, 2-INPUT OR-AND GATE WITH 2X OUTPUT
$Y = (A+B)\cdot(C+D)$

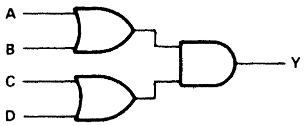
D3015, OCTOBER 1988

INTERNAL MACRO

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	L	X	X	L
X	X	L	L	L
Any H		Any H		H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = (A+B)\bullet(C+D)$

description

The OA220LJ is a 2-wide, 2-input OR-NAND gate with a 2X output. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OA220LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.6		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	Any	Y	0.25	0.63	1.25	ns
t_{PHL}			0.34	0.99	2.38	
Δt_{PLH}	Any	Y	0.18	0.45	0.88	ns/pF
Δt_{PHL}			0.15	0.39	0.78	

§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

TEXAS INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OA231LJ
3-WIDE, 2-INPUT OR-NAND GATE WITH 1X OUTPUT
$Y = \overline{(A1+A2)\cdot(B1+B2)\cdot(C1+C2)}$

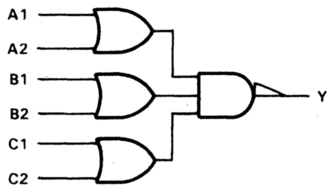
D3015. OCTOBER 1988

INTERNAL MACRO

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	B1	B2	C1	C2	Y
L	L	X	X	X	X	H
X	X	L	L	X	X	H
X	X	X	X	L	L	H
Any H		Any H		Any H		L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1+A2)\bullet(B1+B2)\bullet(C1+C2)}$

description

The OA231LJ is a 3-wide, 2-input OR-NAND gate with a 1X output. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OA231LJ A1,A2,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.9		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.38		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	Any	Y	0.21	0.64	1.78	ns
t_{PHL}			0.22	0.48	1.03	
Δt_{PLH}	Any	Y	0.6	1.69	3.42	ns/pF
Δt_{PHL}			0.38	1	2.07	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
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OA241LJ
OR-NAND GATE WITH 4X OUTPUT
$Y = \overline{(A1 + A2) \cdot (B1 + B2) \cdot (C1 + C2) \cdot (D1 + D2)}$

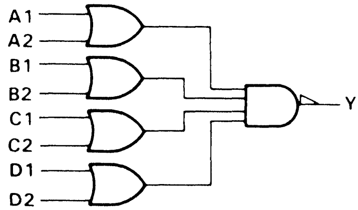
D3015, OCTOBER 1987 – REVISED OCTOBER 1988

INTERNAL MACRO

FUNCTION TABLE

INPUTS								OUTPUT
A1	A2	B1	B2	C1	C2	D1	D2	Y
L	L	X	X	X	X	X	X	H
X	X	L	L	X	X	X	X	H
X	X	X	X	L	L	X	X	H
X	X	X	X	X	X	L	L	H
Any H		Any H		Any H		Any H		L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1+A2) \bullet (B1+B2) \bullet (C1+C2) \bullet (D1+D2)}$

description

The OA241LJ is a 4-wide, 2-input OR-NAND gate CMOS macro with a 4X output. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OA241LJ A1,A2,B1,B2,C1,C2,D1,D2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.9		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.4		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	Any	Y	0.27	0.88	2.46	ns
t_{PHL}			0.35	0.97	2.35	
Δt_{PLH}	Any	Y	0.63	1.72	3.43	ns/pF
Δt_{PHL}			0.46	1.29	2.7	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OR210LJ
2-INPUT POSITIVE-OR GATE

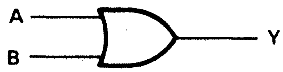
D3015, OCTOBER 1987 – REVISED FEBRUARY 1989

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS		OUTPUT
A	**B**	**Y**
H	X	H
X	H	H
L	L	L

logic symbol†



Equivalent to 1/4 7432

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A+B = \overline{\overline{A}\cdot\overline{B}}$

description

The OR210LJ is a minimum-power, 2-input positive-OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR210LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.48		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B	Y	0.1	0.39	0.78	ns
t_{PHL}			0.32	0.71	1.47	
Δt_{PLH}	A,B	Y	0.38	0.88	1.7	ns/pF
Δt_{PHL}			0.26	0.55	1	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OR220LJ
2-INPUT POSITIVE-OR GATE
WITH 2X OUTPUT

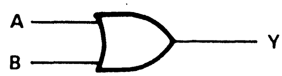
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†



Equivalent to 1/4 7432

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

POSITIVE LOGIC EQUATION: $Y = A+B = \overline{\overline{A}\bullet\overline{B}}$

description

The OR220LJ is a 2-input positive-OR gate featuring twice the capacitive-drive capability when compared to the OR210LJ OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR220LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.8		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.8		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B	Y	0.17	0.46	0.83	ns
t_{PHL}			0.35	0.82	1.72	
Δt_{PLH}	A,B	Y	0.16	0.44	0.86	ns/pF
Δt_{PHL}			0.14	0.36	0.7	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TGC100 SERIES

OR310LJ 3-INPUT POSITIVE-OR GATE

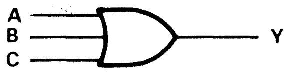
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	H
X	H	X	H
X	X	H	H
L	L	L	L

logic symbol†



Equivalent to 1/3 4075

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A+B+C = \overline{\overline{A} \cdot \overline{B} \cdot \overline{C}}$

description

The OR310LJ is a minimum-power, 3-input positive-OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR310LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.7		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.45		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C	Y	0.12	0.43	0.84	ns
t_{PHL}			0.41	1.04	2.44	
Δt_{PLH}	A,B,C	Y	0.34	0.88	1.73	ns/pF
Δt_{PHL}			0.29	0.64	1.21	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OR320LJ
3-INPUT POSITIVE-OR GATE WITH 2X OUTPUT

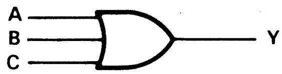
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	H
X	H	X	H
X	X	H	H
L	L	L	L

logic symbol†



Equivalent to 1/4 4075

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A+B+C = \overline{\overline{A}\cdot\overline{B}\cdot\overline{C}}$

description

The OR320LJ is a 3-input positive-OR gate featuring twice the capacitive-drive capability when compared to the OR310LJ OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR320LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.7		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.89		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C	Y	0.2	0.52	0.93	ns
t_{PHL}			0.43	1.2	2.88	
Δt_{PLH}	A,B,C	Y	0.16	0.44	0.87	ns/pF
Δt_{PHL}			0.18	0.42	0.83	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OR410LJ
4-INPUT POSITIVE-OR GATE

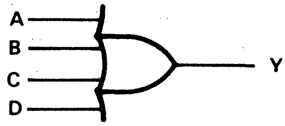
D3015, OCTOBER 1987 – REVISED FEBRUARY 1989

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H
L	L	L	L	L

logic symbol†



Equivalent to 1/2 4072

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A+B+C+D = \overline{\overline{A} \bullet \overline{B} \bullet \overline{C} \bullet \overline{D}}$

description

The OR410LJ is a minimum-power, 4-input positive-OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR410LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.6		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.55		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C,D	Y	0.12	0.46	0.85	ns
t_{PHL}			0.49	1.34	3.43	
Δt_{PLH}	A,B,C,D	Y	0.34	0.89	1.75	ns/pF
Δt_{PHL}			0.31	0.72	1.39	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
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OR420LJ 4-INPUT POSITIVE-OR GATE WITH 2X OUTPUT

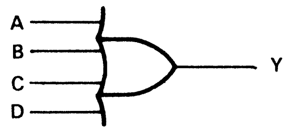
D3015, OCTOBER 1987 – REVISED FEBRUARY 1989

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H
L	L	L	L	L

logic symbol†



Equivalent to 1/4 4072

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A+B+C+D = \overline{\overline{A} \bullet \overline{B} \bullet \overline{C} \bullet \overline{D}}$

description

The OR420LJ is a 4-input positive-OR gate featuring twice the capacitive-drive capability when compared to the OR410LJ OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR420LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.6		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	1.16		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C,D	Y	0.2	0.51	0.91	ns
t_{PHL}			0.51	1.53	3.98	
Δt_{PLH}	A,B,C,D	Y	0.16	0.45	0.89	ns/pF
Δt_{PHL}			0.19	0.49	0.97	

§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

TEXAS INSTRUMENTS
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OR510LJ 5-INPUT POSITIVE-OR GATE

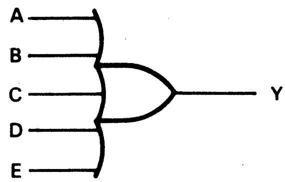
D3015, OCTOBER 1987 – REVISED FEBRUARY 1989

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
H	X	X	X	X	H
X	H	X	X	X	H
X	X	H	X	X	H
X	X	X	H	X	H
X	X	X	X	H	H
L	L	L	L	L	L

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A+B+C+D+E = \overline{\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E}}$

description

The OR510LJ is a minimum-size, 5-input positive-OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR510LJ A,B,C,D,E,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.7		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.74		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C,D,E	Y	0.12	0.46	0.97	ns
t_{PHL}			0.35	0.97	2.49	
Δt_{PLH}	A,B,C,D,E	Y	0.35	0.89	1.73	ns/pF
Δt_{PHL}			0.32	0.79	1.6	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TGC100 SERIES

OR810LJ 8-INPUT POSITIVE-OR GATE

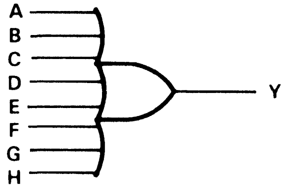
D3015, OCTOBER 1987 – REVISED FEBRUARY 1989

INTERNAL GATE MACRO

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
H	X	X	X	X	X	X	X	H
X	H	X	X	X	X	X	X	H
X	X	H	X	X	X	X	X	H
X	X	X	H	X	X	X	X	H
X	X	X	X	H	X	X	X	H
X	X	X	X	X	H	X	X	H
X	X	X	X	X	X	H	X	H
X	X	X	X	X	X	X	H	H
L	L	L	L	L	L	L	L	L

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A+B+C+D+E+F+G+H = \overline{\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}\cdot\overline{E}\cdot\overline{F}\cdot\overline{G}\cdot\overline{H}}$

description

The OR810LJ is a minimum-size, 8-input positive-OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR810LJ A,B,C,D,E,F,G,H,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		1.6		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.97		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	A thru H	Y	0.13	0.5	0.98	ns
t_{PHL}			0.53	1.43	3.83	
Δt_{PLH}	A thru H	Y	0.34	0.89	1.76	ns/pF
Δt_{PHL}			0.34	0.9	1.92	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

TEXAS INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS TEXAS 75265

9 Flip-Flops/Latches

FLIP-FLOPS AND LATCHES FUNCTIONAL INDEX

D3015, OCTOBER 1987 – REVISED OCTOBER 1988

D-TYPE FLIP-FLOPS

DESCRIPTION	f_{max} (MHz)	MACRO NAME	OUTPUT DRIVE	CELLS USED	PAGE
With Clear and Preset	115	DFB20LJ	2X	12	9-3
With Clear and Preset	100	DTB00LJ	0.5X	8	9-5
With Clear and Preset	170	DTB10LJ	1X	9	9-7
With Clear and Preset	193	DTB20LJ	2X	10	9-9
Clear Only	100	DTC00LJ	0.5X	7	9-11
Clear Only	185	DTC10LJ	1X	8	9-13
Clear Only	208	DTC20LJ	2X	9	9-15
Neither Preset nor Clear	100	DTN00LJ	0.5X	6	9-17
Neither Preset nor Clear	179	DTN10LJ	1X	7	9-19
Neither Preset nor Clear	208	DTN20LJ	2X	8	9-21
Preset Only	95	DTP00LJ	0.5X	7	9-23
Preset Only	167	DTP10LJ	1X	8	9-25
Preset Only	200	DTP20LJ	2X	9	9-27

D-TYPE FLIP-FLOPS (SOFTWARE)

DESCRIPTION	CELL NAME	OUTPUT DRIVE	EQUIVALENT NA210s	PAGE
4-Bit, 3-State Outputs, Active H Clear	S173LJ	1X	53	9-90
4-Bit, Complementary Outputs, Active L Clear	S175LJ	1X	31	9-94
8-Bit, Active L Clear	S273LJ	1X	55	9-97
8-Bit, 3-State Outputs	S374LJ	1X	76	9-100

J-K FLIP-FLOPS

DESCRIPTION	f_{max} (MHz)	MACRO NAME	OUTPUT DRIVE	CELLS USED	PAGE
With Clear and Preset	135	JKB20LJ	2X	12	9-29
With Clear and Preset	135	JKB21LJ	2X	12	9-31

D3015, OCTOBER 1987—REVISED OCTOBER 1988

LATCHES

DESCRIPTION	MACRO NAME	OUTPUT DRIVE	COMMENTS	CELLS USED	PAGE
Set-Reset	LAB20LJ	2X		4	9-33
D-Type	LAH12LJ	1X	3-state Q output	5	9-35
	LAH13LJ	1X	3-state QZ output	5	9-37
	LAH14LJ	1X	3-state Q and QZ outputs	5	9-39
	LAH20LJ	2X	Active-high enable	5	9-41
	LAH22LJ	2X	Active-high enable	4	9-43
Bus Holder	LH110LJ	1X	Latches 3-state bus	4	9-45
4-Bit D-Type	LH400LJ	1X	Active-high enable	11	9-46

LATCHES (SOFTWARE)

DESCRIPTION	MACRO NAME	OUTPUT DRIVE	EQUIVALENT NA210s	PAGE
8-Bit D-Type, 3-State Output	S373LJ	1X	47	9-103
4-Bit Bistable	S375LJ	2X	16	9-107

SCAN LATCHES

DESCRIPTION	MACRO NAME	OUTPUT DRIVE	COMMENTS	CELLS USED	PAGE
Master-Slave Scan-Input D-Type Latches	TDB10LJ	1X	Clear only	10	9-50
	TDC11LJ	1X	Clear, master and slave outputs	10	9-56
	TDN11LJ	1X		8	9-63
	TDN12LJ	1X	Master and slave outputs	10	9-69
	TDN13LJ	1X	Slave D input, master and slave outputs	12	9-76
	TDN22LJ	2X	Master and slave outputs	10	9-83

TOGGLE FLIP-FLOP

DESCRIPTION	f_{max} (MHz)	MACRO NAME	OUTPUT DRIVE	CELLS USED	PAGE
With Clear and Preset	131	TAB20LJ	2X	9	9-48

DFB20LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET AND CLEAR

D3015, OCTOBER 1987

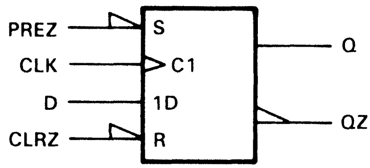
INTERNAL FLIP-FLOP HARDWIRED MACRO

FUNCTION TABLE

INPUTS				OUTPUTS	
PREZ	**CLRZ**	**CLK**	**D**	**Q**	**QZ**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	L*	L*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

* This configuration is nonstable; that is, it will not persist when PREZ or CLRZ returns to its inactive (high) level.

logic symbol†



Similar to 1/2 7474

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DFB20LJ hardwired gate-array macro implements a D-type flip-flop. The flip-flop incorporates direct inputs for both preset and clear providing the IC designer a full-function storage element to embed in ASICs in its most efficient form. It can be used as a stand-alone, bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DFB20LJ CLRZ,PREZ,D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	115	MHz
t_w	Pulse duration	CLRZ low	3		ns
		PREZ low	3		
		CLK high or low	4.3		
t_{su}	Setup time	CLRZ inactive	3		ns
		PREZ inactive	1		
		D high or low	3		
t_h	Hold time	D high or low	1		ns

D3015, OCTOBER 1987

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.4		V
C_i	Input capacitance	CLRZ		0.21		pF
		PREZ		0.22		
		D		0.07		
		CLK		0.12		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	2.06		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
t_{PLH}	CLK	Q	0.71	2	4.21	ns
t_{PHL}			0.5	1.37	2.9	
t_{PLH}	CLK	QZ	0.72	2.04	4.36	ns
t_{PHL}			0.5	1.33	2.73	
t_{PLH}	CLRZ	QZ	0.58	1.53	3.22	ns
t_{PHL}		Q	0.32	0.76	1.47	
t_{PLH}	PREZ	Q	0.57	1.49	3.11	ns
t_{PHL}		QZ	0.3	0.77	1.49	
Δt_{PLH}	CLK	Q	0.18	0.46	0.92	ns/pF
Δt_{PHL}			0.16	0.35	0.64	
Δt_{PLH}	CLK	QZ	0.19	0.46	0.92	ns/pF
Δt_{PHL}			0.16	0.34	0.65	
Δt_{PLH}	CLRZ	QZ	0.17	0.47	0.93	ns/pF
Δt_{PHL}		Q	0.16	0.34	0.65	
Δt_{PLH}	PREZ	Q	0.17	0.47	0.93	ns/pF
Δt_{PHL}		QZ	0.16	0.31	0.59	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DTB00LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET, CLEAR, AND UNBUFFERED OUTPUTS

D3015, OCTOBER 1987

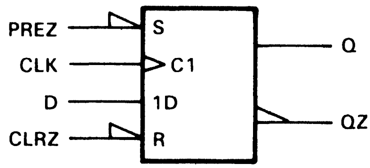
INTERNAL FLIP-FLOP HARDWIRED MACRO

FUNCTION TABLE

INPUTS				OUTPUTS	
PREZ	CLRZ	CLK	D	Q	QZ
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	L*	L*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

* This configuration is nonstable; that is, it will not persist when PREZ or CLRZ returns to its inactive (high) level.

logic symbol†



Similar to 1/2 7474

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DTB00LJ hardwired gate-array macro implements a D-type flip-flop at minimum gate size. The flip-flop incorporates direct inputs for both preset and clear providing the IC designer a full-function storage element to embed in ASICs in its most efficient form. It can be used as a stand-alone, bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DTB00LJ CLRZ,PREZ,D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	100	MHz
t_w	Pulse duration	CLRZ low	6		ns
		PREZ low	7		
		CLK high or low	5		
t_{su}	Setup time	CLRZ inactive	0		ns
		PREZ inactive	1		
		D high or low	2		
t_h	Hold time	D high or low	0		ns

TEXAS INSTRUMENTS
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electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLRZ		0.19		pF
		PREZ		0.18		
		D		0.07		
		CLK		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	1.9		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
t_{PLH}	CLK	Q	0.49	1.38	2.83	ns
t_{PHL}			0.48	1.39	2.9	
t_{PLH}	CLK	QZ	0.4	1.15	2.37	ns
t_{PHL}			0.39	1.09	2.21	
t_{PLH}	CLRZ	QZ	0.29	0.42	0.64	ns
t_{PHL}		Q	0.41	0.8	1.45	
t_{PLH}	PREZ	Q	0.23	0.33	0.55	ns
t_{PHL}		QZ	0.48	1.18	2.45	
Δt_{PLH}	CLK	Q	0.78	1.96	3.88	ns/pF
Δt_{PHL}			0.82	1.98	3.86	
Δt_{PLH}	CLK	QZ	0.38	0.9	1.74	ns/pF
Δt_{PHL}			0.34	0.8	1.56	
Δt_{PLH}	CLRZ	QZ	0.26	0.84	1.76	ns/pF
Δt_{PHL}		Q	0.58	1.62	3.34	
Δt_{PLH}	PREZ	Q	0.34	0.88	1.68	ns/pF
Δt_{PHL}		QZ	0.32	0.8	1.56	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DTB10LJ D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET AND CLEAR

D3015, OCTOBER 1987

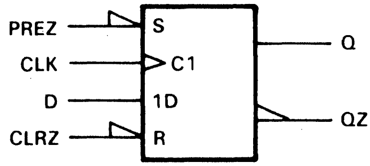
INTERNAL FLIP-FLOP HARDWIRED MACRO

FUNCTION TABLE

INPUTS				OUTPUTS	
PREZ	CLRZ	CLK	D	Q	QZ
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	L*	L*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

* This configuration is nonstable; that is, it will not persist when PREZ or CLRZ returns to its inactive (high) level.

logic symbol†



Similar to 1/2 7474

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DTB10LJ hardwired gate-array macro implements a D-type flip-flop with 1X drive outputs. The flip-flop incorporates direct inputs for both preset and clear providing the IC designer a full-function storage element to embed in ASICs in its most efficient form. It can be used as a stand-alone, bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DTB10LJ CLRZ,PREZ,D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	170	MHz
t_w	Pulse duration	CLRZ low	1.8		ns
		PREZ low	2.4		
		CLK high or low	2.9		
t_{su}	Setup time	CLRZ inactive	0		ns
		PREZ inactive	0.4		
		D high or low	1.9		
t_h	Hold time	D high or low	0		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLRZ		0.19		pF
		PREZ		0.18		
		D		0.07		
		CLK		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	2.1		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
t_{PLH}	CLK	Q	0.47	1.46	3.11	ns
t_{PHL}			0.52	1.53	3.2	
t_{PLH}	CLK	QZ	0.39	1.16	2.39	ns
t_{PHL}			0.37	1.07	2.24	
t_{PLH}	CLRZ	QZ	0.61	1.65	3.52	ns
t_{PHL}		Q	0.33	0.71	1.35	
t_{PLH}	PREZ	Q	0.56	1.51	3.23	ns
t_{PHL}		QZ	0.44	1.12	2.31	
Δt_{PLH}	CLK	Q	0.36	0.88	1.7	ns/pF
Δt_{PHL}			0.24	0.52	0.96	
Δt_{PLH}	CLK	QZ	0.38	0.9	1.76	ns/pF
Δt_{PHL}			0.28	0.66	1.22	
Δt_{PLH}	CLRZ	QZ	0.36	0.9	1.74	ns/pF
Δt_{PHL}		Q	0.26	0.52	0.96	
Δt_{PLH}	PREZ	Q	0.36	0.88	1.68	ns/pF
Δt_{PHL}		QZ	0.3	0.66	1.26	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET, CLEAR, AND 2X OUTPUTS

D3015, OCTOBER 1987

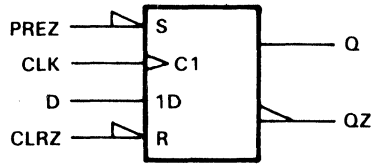
INTERNAL FLIP-FLOP HARDWIRED MACRO

FUNCTION TABLE

INPUTS				OUTPUTS	
PREZ	CLRZ	CLK	D	Q	QZ
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	L*	L*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

* This configuration is nonstable; that is, it will not persist when PREZ or CLRZ returns to its inactive (high) level.

logic symbol†



Similar to 1/2 7474

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DTB20LJ hardwired gate-array macro implements a D-type flip-flop featuring twice the capacitive-drive capability when compared to the DFB10LJ flip-flop. The flip-flop incorporates direct inputs for both preset and clear providing the IC designer a full-function storage element to embed in ASICs in its most efficient form. It can be used as a stand-alone, bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DTB20LJ CLRZ,PREZ,D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	193	MHz
t_w	Pulse duration	CLRZ low	2.2		ns
		PREZ low	2.8		
		CLK high or low	2.6		
t_{su}	Setup time	CLRZ inactive	0		ns
		PREZ inactive	0.8		
		D high or low	2.1		
t_h	Hold time	D high or low	0.6		ns

TEXAS INSTRUMENTS

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electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLRZ		0.19		pF
		PREZ		0.18		
		D		0.07		
		CLK		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	2.6		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
t_{PLH}	CLK	Q	0.51	1.68	3.64	ns
t_{PHL}			0.54	1.65	3.53	
t_{PLH}	CLK	QZ	0.41	1.18	2.46	ns
t_{PHL}			0.36	1.08	2.26	
t_{PLH}	CLRZ	QZ	0.62	1.7	3.62	ns
t_{PHL}		Q	0.33	0.74	1.4	
t_{PLH}	PREZ	Q	0.6	1.74	3.77	ns
t_{PHL}		QZ	0.43	1.11	2.28	
Δt_{PLH}	CLK	Q	0.18	0.42	0.84	ns/pF
Δt_{PHL}			0.14	0.32	0.6	
Δt_{PLH}	CLK	QZ	0.18	0.48	0.96	ns/pF
Δt_{PHL}			0.16	0.42	0.84	
Δt_{PLH}	CLRZ	QZ	0.18	0.48	0.96	ns/pF
Δt_{PHL}		Q	0.16	0.32	0.64	
Δt_{PLH}	PREZ	Q	0.18	0.42	0.8	ns/pF
Δt_{PHL}		QZ	0.18	0.44	0.9	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DTC00LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH CLEAR AND UNBUFFERED OUTPUTS

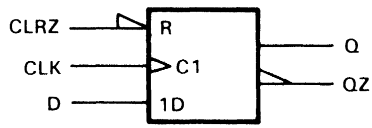
D3015, OCTOBER 1987–REVISED FEBRUARY 1989

INTERNAL FLIP-FLOP HARDWIRED MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
CLRZ	CLK	D	Q	QZ
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

logic symbol†



Equivalent to 1/4 74175

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DTC00LJ hardwired gate-array macro implements a D-type flip-flop at minimum gate size. The flip-flop incorporates a direct clear input providing the IC designer a custom storage element to embed in ASICs in its most efficient form. It can be used as a stand-alone, bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DTC00LJ CLRZ,D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	100	MHz
t_w	Pulse duration	CLRZ low	6		ns
		CLK high or low	5		
t_{su}	Setup time	CLRZ inactive	0		ns
		D high or low	2		
t_h	Hold time	D high or low	0		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLRZ		0.19		pF
		CLK		0.07		
		D		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	1.8		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	CLK	Q	0.47	1.29	2.57	ns
t_{PHL}			0.48	1.33	2.76	
t_{PLH}	CLK	QZ	0.4	1.15	2.34	ns
t_{PHL}			0.4	1.06	2.11	
t_{PLH}	CLRZ	QZ	0.28	0.41	0.59	ns
t_{PHL}		Q	0.36	0.71	1.31	
Δt_{PLH}	CLK	Q	0.78	1.92	3.82	ns/pF
Δt_{PHL}			0.76	1.86	3.58	
Δt_{PLH}	CLK	QZ	0.38	0.88	1.7	ns/pF
Δt_{PHL}			0.32	0.76	1.5	
Δt_{PLH}	CLRZ	QZ	0.24	0.76	1.66	ns/pF
Δt_{PHL}		Q	0.54	1.4	2.8	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

DTC10LJ D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH CLEAR

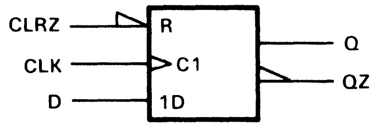
D3015, OCTOBER 1987 – REVISED FEBRUARY 1989

INTERNAL FLIP-FLOP HARDWIRED MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
CLRZ	**CLK**	**D**	**Q**	**QZ**
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

logic symbol†



Equivalent to 1/4 74175

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DTC10LJ hardwired gate-array macro implements a D-type flip-flop with 1X drive outputs. The flip-flop incorporates a direct clear input providing the IC designer a custom storage element to embed in ASICs in its most efficient form. It can be used as a stand-alone, bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DTC10LJ CLRZ,D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	185	MHz
t_w	Pulse duration	CLRZ low	2.6		ns
		CLK high or low	2.7		
t_{su}	Setup time	CLRZ inactive	0.6		ns
		D high or low	1.5		
t_h	Hold time	D high or low	0.7		ns

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLRZ		0.19		pF
		CLK		0.07		
		D		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	2.1		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
t_{PLH}	CLK	Q	0.47	1.44	3.02	ns
t_{PHL}			0.52	1.54	3.21	
t_{PLH}	CLK	QZ	0.39	1.07	2.19	ns
t_{PHL}			0.38	1.11	2.29	
t_{PLH}	CLRZ	QZ	0.55	1.4	2.92	ns
t_{PHL}		Q	0.3	0.65	1.22	
Δt_{PLH}	CLK	Q	0.38	0.9	1.72	ns/pF
Δt_{PHL}			0.26	0.52	0.96	
Δt_{PLH}	CLK	QZ	0.36	0.9	1.72	ns/pF
Δt_{PHL}			0.28	0.64	1.2	
Δt_{PLH}	CLRZ	QZ	0.36	0.9	1.72	ns/pF
Δt_{PHL}		Q	0.26	0.52	0.96	

‡ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

DTC20LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH CLEAR AND 2X OUTPUTS

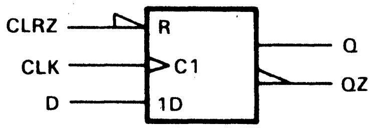
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

INTERNAL FLIP-FLOP HARDWIRED MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
CLRZ	CLK	D	Q	QZ
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

logic symbol†



Equivalent to 1/4 74175

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DTC20LJ hardwired gate-array macro implements a D-type flip-flop featuring twice the capacitive-drive capability when compared to the DTC10LJ. The flip-flop incorporates a direct clear input providing the IC designer a custom storage element to embed in ASICs in its most efficient form. It can be used as a stand-alone, bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DTC20LJ CLRZ,D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	208	MHz
t_w	Pulse duration	CLRZ low	2.1		ns
		CLK high or low	2.4		
t_{su}	Setup time	CLRZ inactive	0.6		ns
		D high or low	1.6		
t_h	Hold time	D high or low	0.7		ns

DTC20LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH CLEAR AND 2X OUTPUTS

D3015, OCTOBER 1987

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER[†]			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLRZ		0.19		pF
		CLK		0.07		
		D		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	2.6		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP[‡]	MAX	UNIT
t_{PLH}	CLK	Q	0.52	1.63	3.46	ns
t_{PHL}			0.55	1.64	3.45	
t_{PLH}	CLK	QZ	0.39	1.12	2.26	ns
t_{PHL}			0.35	1.09	2.28	
t_{PLH}	CLRZ	QZ	0.56	1.45	3.01	ns
t_{PHL}		Q	0.32	0.67	1.3	
Δt_{PLH}	CLK	Q	0.18	0.44	0.86	ns/pF
Δt_{PHL}			0.14	0.32	0.62	
Δt_{PLH}	CLK	QZ	0.18	0.44	0.9	ns/pF
Δt_{PHL}			0.18	0.44	0.86	
Δt_{PLH}	CLRZ	QZ	0.18	0.46	0.9	ns/pF
Δt_{PHL}		Q	0.14	0.34	0.62	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DTN00LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH UNBUFFERED OUTPUTS

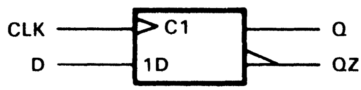
D3015, OCTOBER 1987

INTERNAL FLIP-FLOP HARDWIRED MACRO

FUNCTION TABLE

INPUTS		OUTPUTS	
CLK	D	Q	QZ
↑	H	H	L
↑	L	L	H
L	X	Q_0	$\overline{Q}_0$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DTN00LJ hardwired gate-array macro implements a D-type flip-flop at minimum gate size. The flip-flop provides the IC designer a custom storage element to embed in ASICs in its most efficient form. It can be used as a stand-alone, bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DTN00LJ D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	100	MHz
t_w	Pulse duration	CLK high or low	5		ns
t_{su}	Setup time	D high or low	2		ns
t_h	Hold time	D high or low	0		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLK		0.07		pF
		D		0.07		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	1.7		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	CLK	Q	0.45	1.23	2.48	ns
t_{PHL}			0.44	1.26	2.55	
t_{PLH}	CLK	QZ	0.38	1.07	2.18	ns
t_{PHL}			0.38	1.03	2.05	
Δt_{PLH}	CLK	Q	0.7	1.6	3.06	ns/pF
Δt_{PHL}			0.78	1.84	3.6	
Δt_{PLH}	CLK	QZ	0.38	0.9	1.72	ns/pF
Δt_{PHL}			0.28	0.56	1.04	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

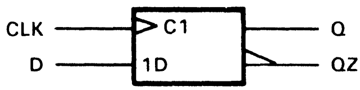
D3015, OCTOBER 1987

INTERNAL FLIP-FLOP HARDWIRED MACRO

FUNCTION TABLE

INPUTS		OUTPUTS	
CLK	D	Q	QZ
↑	H	H	L
↑	L	L	H
L	X	Q_0	$\overline{Q}_0$

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DTN10LJ hardwired gate-array macro implements a D-type flip-flop with 1X drive outputs. The flip-flop provides the IC designer a custom storage element to embed in ASICs in its most efficient form. It can be used as a stand-alone, bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DTN10LJ D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	179	MHz
t_w	Pulse duration	CLK high or low	2.8		ns
t_{su}	Setup time	D high or low	0.7		ns
t_h	Hold time	D high or low	0.6		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLK		0.07		pF
		D		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	2		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

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D3015, OCTOBER 1987

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	CLK	Q	0.43	1.32	2.75	ns
t_{PHL}			0.5	1.43	2.99	
t_{PLH}	CLK	QZ	0.39	1.07	2.19	ns
t_{PHL}			0.38	1.12	2.28	
Δt_{PLH}	CLK	Q	0.38	0.88	1.68	ns/pF
Δt_{PHL}			0.24	0.52	0.92	
Δt_{PLH}	CLK	QZ	0.36	0.9	1.72	ns/pF
Δt_{PHL}			0.28	0.62	1.2	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

DTN20LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH 2X OUTPUTS

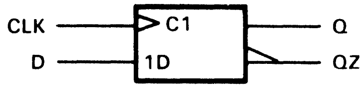
D3015, OCTOBER 1987

INTERNAL FLIP-FLOP HARDWIRED MACRO

FUNCTION TABLE

INPUTS		OUTPUTS	
CLK	D	Q	QZ
↑	H	H	L
↑	L	L	H
L	X	Q_0	$\overline{Q}_0$

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DTN20LJ hardwired gate-array macro implements a D-type flip-flop featuring twice the capacitive-drive capability when compared to the DTN10LJ. The flip-flop provides the IC designer a custom storage element to embed in ASICs in its most efficient form. It can be used as a stand-alone, bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DTN20LJ D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	208	MHz
t_w	Pulse duration	CLK high or low	2.4		ns
t_{su}	Setup time	D high or low	0.7		ns
t_h	Hold time	D high or low	0.6		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLK		0.07		pF
		D		0.07		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	2.4		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	CLK	Q	0.47	1.49	3.19	ns
t_{PHL}			0.52	1.56	3.24	
t_{PLH}	CLK	QZ	0.39	1.1	2.25	ns
t_{PHL}			0.35	1.1	2.3	
Δt_{PLH}	CLK	Q	0.18	0.44	0.82	ns/pF
Δt_{PHL}			0.14	0.3	0.6	
Δt_{PLH}	CLK	QZ	0.18	0.46	0.9	ns/pF
Δt_{PHL}			0.18	0.42	0.84	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

DTP00LJ D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET AND UNBUFFERED OUTPUTS

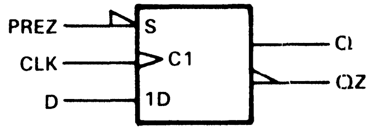
D3015, OCTOBER 1987

INTERNAL FLIP-FLOP HARDWIRED MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
PREZ	CLK	D	Q	QZ
L	X	X	H	L
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DTP00LJ hardwired gate-array macro implements a D-type flip-flop at minimum gate size. The flip-flop incorporates a direct preset input providing the IC designer a custom storage element to embed in ASICs in its most efficient form. It can be used as a stand-alone, bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DTP00LJ PREZ,D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	95	MHz
t_w	Pulse duration	PREZ low	6		ns
		CLK high or low	5.3		
t_{su}	Setup time	PREZ inactive	0		ns
		D high or low	2		
t_h	Hold time	D high or low	0		ns

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	PREZ		0.18		pF
		CLK		0.07		
		D		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	1.9		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	CLK	Q	0.52	1.35	2.65	ns
t_{PHL}			0.54	1.44	2.91	
t_{PLH}	CLK	QZ	0.44	1.18	2.36	ns
t_{PHL}			0.41	1.04	2.03	
t_{PLH}	PREZ	Q	0.58	1.47	3.13	ns
t_{PHL}		QZ	0.44	1.05	2.19	
Δt_{PLH}	CLK	Q	0.68	1.58	3.06	ns/pF
Δt_{PHL}			0.8	1.96	3.84	
Δt_{PLH}	CLK	QZ	0.38	0.9	1.74	ns/pF
Δt_{PHL}			0.28	0.58	1.06	
Δt_{PLH}	PREZ	Q	0.16	0.42	0.8	ns/pF
Δt_{PHL}		QZ	0.14	0.44	0.86	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

DTP10LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET

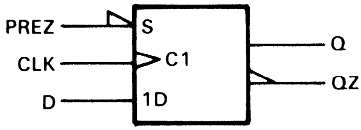
D3015, OCTOBER 1987

INTERNAL FLIP-FLOP HARDWIRED MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
PREZ	CLK	D	Q	QZ
L	X	X	H	L
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DTP10LJ hardwired gate-array macro implements a D-type flip-flop with 1X drive outputs. The flip-flop incorporates a direct preset input providing the IC designer a custom storage element to embed in ASICs in its most efficient form. It can be used as a stand-alone, bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DTP10LJ PREZ,D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	167	MHz
t_w	Pulse duration	PREZ low	2.6		ns
		CLK high or low	3		
t_{su}	Setup time	PREZ inactive	0.2		ns
		D high or low	1.6		
t_h	Hold time	D high or low	0		ns

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	PREZ		0.18		pF
		CLK		0.07		
		D		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	2.2		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	CLK	Q	0.51	1.34	2.75	ns
t_{PHL}			0.57	1.55	3.19	
t_{PLH}	CLK	QZ	0.45	1.19	2.4	ns
t_{PHL}			0.41	1.13	2.29	
t_{PLH}	PREZ	Q	0.5	1.28	2.68	ns
t_{PHL}		QZ	0.43	1.07	2.23	
Δt_{PLH}	CLK	Q	0.34	0.88	1.7	ns/pF
Δt_{PHL}			0.24	0.52	0.92	
Δt_{PLH}	CLK	QZ	0.36	0.9	1.76	ns/pF
Δt_{PHL}			0.28	0.64	1.22	
Δt_{PLH}	PREZ	Q	0.36	0.88	1.68	ns/pF
Δt_{PHL}		QZ	0.28	0.64	1.2	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

DTP20LJ D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET AND 2X OUTPUTS

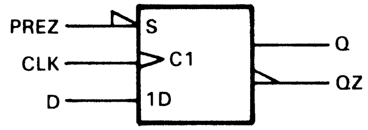
D3015, OCTOBER 1987

INTERNAL FLIP-FLOP HARDWIRED MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
PREZ	CLK	D	Q	QZ
L	X	X	H	L
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DTP20LJ hardwired gate-array macro implements a D-type flip-flop featuring twice the capacitive-drive capability when compared to the DTP10LJ. The flip-flop incorporates a direct preset input providing the IC designer a custom storage element to embed in ASICs in its most efficient form. It can be used as a stand-alone, bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DTP20LJ PREZ,D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	200	MHz
t_w	Pulse duration	PREZ low	2.6		ns
		CLK high or low	2.5		
t_{su}	Setup time	PREZ inactive	0.2		ns
		D high or low	1.6		
t_h	Hold time	D high or low	0		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	PREZ		0.18		pF
		CLK		0.07		
		D		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	2.5		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	CLK	Q	0.53	1.53	3.18	ns
t_{PHL}			0.59	1.69	3.5	
t_{PLH}	CLK	QZ	0.46	1.22	2.46	ns
t_{PHL}			0.39	1.1	2.3	
t_{PLH}	PREZ	Q	0.58	1.47	3.13	ns
t_{PHL}		QZ	0.44	1.05	2.19	
Δt_{PLH}	CLK	Q	0.16	0.42	0.82	ns/pF
Δt_{PHL}			0.14	0.3	0.6	
Δt_{PLH}	CLK	QZ	0.18	0.48	0.98	ns/pF
Δt_{PHL}			0.18	0.44	0.84	
Δt_{PLH}	PREZ	Q	0.16	0.42	0.8	ns/pF
Δt_{PHL}		QZ	0.14	0.44	0.86	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

JKB20LJ
J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET, CLEAR, AND 2X OUTPUTS

D3015, OCTOBER 1987 – REVISED FEBRUARY 1989

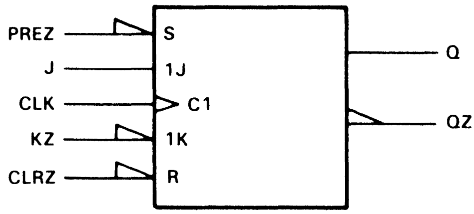
INTERNAL FLIP-FLOP HARDWIRED MACRO

FUNCTION TABLE

INPUTS					OUTPUTS	
PREZ	CLRZ	CLK	J	KZ	Q	QZ
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

* This configuration is nonstable; that is, it will not persist when PREZ or CLRZ returns to its inactive (high) level.

logic symbol†



Equivalent to 1/2 74109

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The JKB20LJ hardwired gate-array macro implements a positive-edge-triggered J-$\overline{K}$ flip-flop featuring the capacitive-drive capability of a 2X output. The flip-flop incorporates direct inputs for both preset and clear providing the IC designer a full-function decision-making storage element to embed in ASICs in its most efficient form. It can be used as a stand-alone, bit-resolution device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: JKB20LJ CLRZ,PREZ,KZ,J,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	135	MHz
t_w	Pulse duration	CLRZ low	4		ns
		PREZ low	4		
		CLK high or low	3.7		
t_{su}	Setup time	CLRZ inactive	1		ns
		PREZ inactive	0		
		J or KZ high or low	4		
t_h	Hold time	J or KZ high or low	0		ns

JKB20LJ
J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET, CLEAR, AND 2X OUPUTS

D3015, OCTOBER 1987

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			1.8		V
C_i	Input capacitance	CLRZ		0.17		pF
		PREZ		0.18		
		J,KZ		0.07		
		CLK		0.08		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	3		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
t_{PLH}	CLK	Q	0.74	2.13	4.45	ns
t_{PHL}			0.72	2.07	4.34	
t_{PLH}	CLK	QZ	0.53	1.47	2.99	ns
t_{PHL}			0.59	1.58	3.28	
t_{PLH}	CLRZ	QZ	0.59	1.69	3.61	ns
t_{PHL}		Q	0.38	0.91	1.78	
t_{PLH}	PREZ	Q	0.62	1.58	3.26	ns
t_{PHL}		QZ	0.37	0.81	1.6	
Δt_{PLH}	CLK	Q	0.2	0.44	0.86	ns/pF
Δt_{PHL}			0.14	0.34	0.64	
Δt_{PLH}	CLK	QZ	0.18	0.46	0.92	ns/pF
Δt_{PHL}			0.12	0.36	0.68	
Δt_{PLH}	CLRZ	QZ	0.2	0.44	0.86	ns/pF
Δt_{PHL}		Q	0.18	0.38	0.74	
Δt_{PLH}	PREZ	Q	0.18	0.48	0.94	ns/pF
Δt_{PHL}		QZ	0.14	0.36	0.68	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

JKB21LJ J-$\overline{K}$ NEGATIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET, CLEAR, AND 2X OUTPUTS

D3015, OCTOBER 1987 – REVISED FEBRUARY 1989

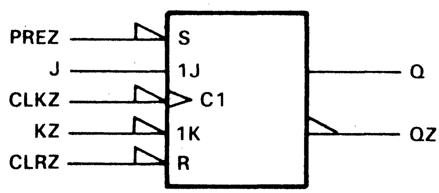
INTERNAL FLIP-FLOP HARDWIRED MACRO

FUNCTION TABLE

INPUTS					OUTPUTS	
PREZ	CLRZ	CLKZ	J	KZ	Q	QZ
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	L	H
H	H	↓	H	L	TOGGLE	
H	H	↓	L	H	Q_0	$\overline{Q_0}$
H	H	↓	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q_0}$

* This configuration is nonstable; that is, it will not persist when PREZ or CLRZ returns to its inactive (high) level.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The JKB21LJ hardwired gate-array macro implements a negative-edge-triggered J-$\overline{K}$ flip-flop featuring the capacitive-drive capability of a 2X output. The flip-flop incorporates direct inputs for both preset and clear providing the IC designer a full-function decision-making storage element to embed in ASICs in its most efficient form. It can be used as a stand-alone, bit-resolution device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: JKB21LJ CLRZ,PREZ,KZ,J,CLKZ,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	135	MHz
t_w	Pulse duration	CLRZ low	4		ns
		PREZ low	3		
		CLKZ high	3.7		
t_{su}	Setup time	CLRZ inactive	0		ns
		PREZ inactive	0		
		J or KZ high or low	3		
t_h	Hold time	J or KZ high or low	0		ns

JKB21LJ
J-$\overline{K}$ NEGATIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET, CLEAR, AND 2X OUTPUTS

D3015, OCTOBER 1987—REVISED FEBRUARY 1989

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			1.8		V
C_i	Input capacitance	CLRZ		0.16		pF
		PREZ		0.18		
		J,KZ		0.07		
		CLKZ		0.08		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	3.2		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
t_{PLH}	CLKZ	Q	0.77	2.08	4.33	ns
t_{PHL}			0.8	2.28	4.81	
t_{PLH}	CLKZ	QZ	0.63	1.69	3.49	ns
t_{PHL}			0.59	1.55	3.19	
t_{PLH}	CLRZ	QZ	0.59	1.69	3.61	ns
t_{PHL}		Q	0.38	0.91	1.78	
t_{PLH}	PREZ	Q	0.61	1.58	3.26	ns
t_{PHL}		QZ	0.37	0.81	1.6	
Δt_{PLH}	CLKZ	Q	0.18	0.44	0.88	ns/pF
Δt_{PHL}			0.18	0.34	0.66	
Δt_{PLH}	CLKZ	QZ	0.2	0.46	0.9	ns/pF
Δt_{PHL}			0.14	0.34	0.66	
Δt_{PLH}	CLRZ	QZ	0.2	0.44	0.86	ns/pF
Δt_{PHL}		Q	0.18	0.38	0.74	
Δt_{PLH}	PREZ	Q	0.2	0.48	0.94	ns/pF
Δt_{PHL}		QZ	0.14	0.36	0.68	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

LAB20LJ
$\overline{S}$-$\overline{R}$ LATCHES WITH 2X OUTPUTS

D3015, OCTOBER 1987

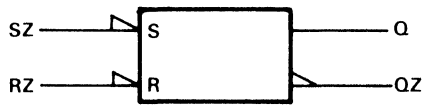
INTERNAL LATCH HARDWIRED MACRO

FUNCTION TABLE

INPUTS		OUTPUTS	
SZ	**RZ**	**Q**	**QZ**
H	H	Q_0	$\overline{Q}_0$
L	H	H	L
H	L	L	H
L	L	L*	L*

* This configuration is nonstable; that is, it will not persist when either SZ or RZ returns to its inactive (H) level.

logic symbol†



Similar to 1/4 74279

† This symbol is in accordance with ANSI/IEEE Std 19-1984.

description

The LAB20LJ hardwired function implements an $\overline{S}$-$\overline{R}$ latch element. The latch incorporates direct inputs for both set (SZ) and reset (RZ) providing the custom IC designer a latch element to embed in ASICs in its most efficient form: as stand-alone bit-storage devices or as additions to larger latched functions. When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: LAB20LJ SZ,RZ,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER;			MIN	MAX	UNIT
t_w	Pulse duration	RZ low	1.8		ns
		SZ low	1.8		
		RZ inactive	1.8		
		SZ inactive	1.8		

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.1		V
C_i	Input capacitance	RZ		0.07		pF
		SZ		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	1.6		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	SZ	Q	0.44	1.1	2.24	ns
t_{PHL}	RZ		0.31	0.68	1.28	
t_{PLH}	RZ	QZ	0.44	1.1	2.24	ns
t_{PHL}	SZ		0.31	0.68	1.28	
Δt_{PLH}	RZ,SZ	Q,QZ	0.18	0.44	0.86	ns/pF
Δt_{PHL}			0.14	0.3	0.6	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

LAH12LJ D-TYPE LATCH WITH 3-STATE Q OUTPUT

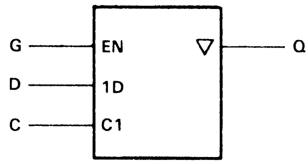
D3015, OCTOBER 1988

INTERNAL LATCH MACRO

FUNCTION TABLE

INPUTS			OUTPUT
G	C	D	Q
H	H	H	H
H	H	L	L
H	L	X	Q_0
L	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The LAH12LJ hardwired function implements a D-type latch element with a 3-state Q output. Information present at the data input is transferred to the Q output when the C input is high and output enable G is high. The output follows the data input as long as C is high and G is high. When enable G is high and C goes low, the data present at the data input when the transistion occurs is retained at the outputs until C is taken high. The outputs are placed in a high-impedance state, Z, by a low logic level at G. When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: LAH12LJ D,C,G,Q;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
t_w	Pulse duration	C high	2		ns
t_{su}	Setup time	D high or low	2		ns
t_h	Hold time	D high or low	0		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	C		0.15		pF
		D		0.07		
		G		0.15		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	1.48		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	C	Q	$R_L = \infty$	0.42	1.12	2.29	ns
t_{PHL}				0.49	1.33	2.57	
t_{PZH}	D	Q	$R_L = \infty$	0.49	1.27	2.5	ns
t_{PZL}				0.64	1.43	2.85	
t_{PHZ}	G	Q	R_L = 40 kΩ to GND	0.19	0.28	0.31	ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}	0.07	0.29	0.42	
t_{PHZ}	G	Q	R_L = 40 kΩ to GND		3.14		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		1.43		
Δt_{PLH}	C	Q		0.39	0.97	1.88	ns/pF
Δt_{PHL}				0.27	0.64	1.26	
Δt_{PLH}	D	Q		0.4	0.97	1.88	ns/pF
Δt_{PHL}				0.25	0.64	1.27	
Δt_{PZH}	G	Q		0.28	0.81	1.79	ns/pF
Δt_{PZH}				0.35	0.64	1.29	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

LAH13LJ D-TYPE LATCH WITH 3-STATE QZ OUTPUT

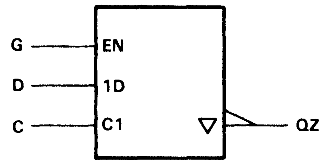
D3015, OCTOBER 1988

INTERNAL LATCH MACRO

FUNCTION TABLE

INPUTS			OUTPUT
G	C	D	QZ
H	H	H	L
H	H	L	H
H	L	X	QZ_0
L	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The LAH13LJ hardwired function implements a D-type latch element with a 3-state QZ output. Information present at the data input is transferred to the QZ output when the C input is high and output enable G is high. The output follows the data input as long as C is high and G is high. When enable G is high and C goes low, the data present at the data input when the transition occurs is retained at the outputs until C is taken high. The outputs are placed in a high-impedance state, Z, by a low logic level at G. When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: LAH13LJ D,C,G,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
t_w	Pulse duration	C high	2		ns
t_{su}	Setup time	D high or low	2		ns
t_h	Hold time	D high or low	0		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	C		0.15		pF
		D		0.07		pF
		G		0.15		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	1.48		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	C	QZ	$R_L = \infty$	0.4	1.14	2.21	ns
t_{PHL}				0.37	1	1.99	
t_{PZH}	D	QZ	$R_L = \infty$	0.51	1.26	2.53	ns
t_{PZL}				0.47	1.16	2.53	
t_{PZH}	G	QZ	R_L = 40 kΩ to GND	0.19	0.28	0.31	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.09	0.29	0.43	
t_{PHZ}	G	QZ	R_L = 40 kΩ to GND		3.12		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		1.44		
Δt_{PLH}	C	QZ		0.4	0.97	1.89	ns/pF
Δt_{PHL}				0.27	0.64	1.27	
Δt_{PLH}	D	QZ		0.39	0.96	1.89	ns/pF
Δt_{PHL}				0.27	0.63	1.24	
Δt_{PZH}	G	QZ		0.28	0.81	1.79	ns/pF
Δt_{PZH}				0.34	0.64	1.29	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

LAH14LJ D-TYPE LATCH WITH 3-STATE COMPLEMENTARY OUTPUTS

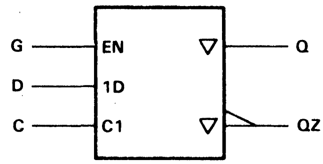
D3015, OCTOBER 1988

INTERNAL LATCH HARDWIRED MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
G	C	D	Q	QZ
H	H	H	H	L
H	H	L	L	H
H	L	X	Q_0	QZ_0
L	X	X	Z	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The LAH14LJ hardwired macro implements a D-type latch element with complementary 3-state Q and QZ outputs. Information present at the data input is transferred to the outputs when the C input is high and output enable G is high. The outputs follow the data input as long as C is high and G is high. When enable G is high and C goes low, the data present at the data inputs when the transition occurs is retained at the outputs until C is taken high. The outputs are placed in a high-impedance state, Z, by a low logic level at G. When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: LAH14LJ D,C,G,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
t_w	Pulse duration	C high	2		ns
t_{su}	Setup time	D high or low	2		ns
t_h	Hold time	D high or low	0		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	C		0.15		pF
		D		0.07		
		G		0.23		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	1.8		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	C	Q	$R_L = \infty$	0.46	1.27	2.57	ns
t_{PHL}				0.56	1.45	2.8	
t_{PLH}	C	QZ	$R_L = \infty$	0.41	1.13	2.18	ns
t_{PHL}				0.37	1	1.99	
t_{PLH}	D	Q	$R_L = \infty$	0.55	1.43	2.81	ns
t_{PHL}				0.64	1.55	3.11	
t_{PLH}	D	QZ	$R_L = \infty$	0.5	1.24	2.5	ns
t_{PHL}				0.47	1.15	2.22	
t_{PZH}	G	Q	R_L = 40 kΩ to GND	0.23	0.29	0.35	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.1	0.3	0.44	
t_{PHZ}	G	Q	R_L = 40 kΩ to GND		3.27		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		1.41		
t_{PZH}	G	QZ	R_L = 40 kΩ to GND	0.22	0.29	0.33	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.1	0.3	0.43	
t_{PHZ}	G	QZ	R_L = 40 kΩ to GND		3.16		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		1.42		
Δt_{PLH}	C	Q		0.39	0.96	1.89	ns/pF
Δt_{PHL}				0.25	0.64	2.8	
Δt_{PLH}	C	QZ		0.39	0.97	1.89	ns/pF
Δt_{PHL}				0.27	0.64	1.27	
Δt_{PZH}	D	Q		0.38	0.96	1.89	ns/pF
Δt_{PZH}				0.27	0.64	1.26	
Δt_{PLH}	D	QZ		0.37	0.96	1.89	ns/pF
Δt_{PHL}				0.27	0.64	1.25	
Δt_{PZH}	G	Q		0.26	0.82	1.77	ns/pF
Δt_{PZL}				0.34	0.64	1.3	
Δt_{PZH}	G	QZ		0.27	0.81	1.77	ns/pF
Δt_{PZL}				0.34	0.64	1.3	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

LAH20LJ
D-TYPE LATCH
WITH ACTIVE-HIGH ENABLE AND 2X OUTPUTS

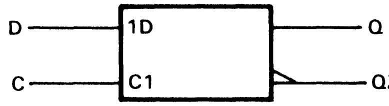
D3015, OCTOBER 1987 – REVISED FEBRUARY 1989

INTERNAL LATCH HARDWIRED MACRO

FUNCTION TABLE

INPUTS		OUTPUTS	
D	C	Q	QZ
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

logic symbol†



Similar to 1/4 7475

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

description

The LAH20LJ hardwired function implements a D-type latch element. Information present at the data input is transferred in true form to the Q output and in inverted form to the QZ output when the enable input is high, and the outputs will follow the data input as long as enable C remains high. When enable goes low, the data that was present at the data input when the transition occurred is retained at the outputs until enable is taken high. When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: LAH20LJ D,C,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
t_w	Pulse duration, C high	1.6		ns
t_{su}	Setup time, D high or low	2		ns
t_h	Hold time, D high or low	0		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	D		0.07		pF
		C		0.17		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	2.2		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	C	Q	0.39	1.16	2.4	ns
t_{PHL}			0.47	1.34	2.72	
t_{PLH}	C	QZ	0.35	0.94	1.84	ns
t_{PHL}			0.28	0.87	1.76	
t_{PLH}	D	Q	0.5	1.31	2.64	ns
t_{PHL}			0.57	1.48	3.05	
t_{PLH}	D	QZ	0.44	1.08	2.19	ns
t_{PHL}			0.41	1.02	2.01	
Δt_{PLH}	Any	Q,QZ	0.16	0.44	0.86	ns/pF
Δt_{PHL}			0.14	0.3	0.6	

†Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

TGC100 SERIES

LAH22LJ D-TYPE LATCH WITH ACTIVE-HIGH ENABLE, CLEAR, AND 2X OUTPUTS

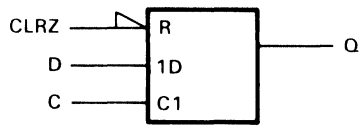
D3015, OCTOBER 1988

INTERNAL LATCH HARDWIRED MACRO

FUNCTION TABLE

INPUTS			OUTPUT
CLRZ	D	C	Q
H	L	H	L
H	H	H	H
H	X	L	Q_0
L	X	X	L

logic symbol†



Similar to 1/8 74116

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The LAH22LJ hardwired function implements a D-type latch element with a direct clear input. Information present at the data input is transferred to the Q output when the enable input is high, and the output will follow the data input as long as enable C remains high. When enable goes low, the data that was present at the data input when the transition occurred is retained at the outputs until enable is taken high. When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: LAH22LJ D,C,CLRZ,Q;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
t_w	Pulse duration	C high	2		ns
		CLRZ low	3		
t_{su}	Setup time	D high or low	2		ns
		CLRZ inactive	2		
t_h	Hold time	D high or low	0		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	D		0.07		pF
		C		0.15		
		CLRZ		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	0.8		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

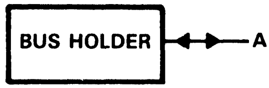
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	C	Q	0.37	0.89	1.8	ns
t_{PHL}			0.37	1.16	2.49	
t_{PHL}	CLRZ	Q	0.4	0.91	1.82	ns
t_{PLH}	D	Q	0.37	0.89	1.73	ns
t_{PHL}			0.42	0.98	1.99	
Δt_{PHL}	CLRZ	Q	0.15	0.34	0.63	ns/pF
Δt_{PLH}	Any other	Q	0.18	0.48	0.96	ns/pF
Δt_{PHL}			0.16	0.38	0.73	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

D3015, OCTOBER 1987

INTERNAL LATCH HARDWIRED MACRO

logic symbol



description

The LH110LJ hardwired function implements a bus-holder latch element for 3-state internal buses. When driven to either a high- or low-logic level, the output of the holder latch reinforces the bus state. The holder is particularly useful in providing stable bus levels during a system period when all 3-state bus drivers transition through the high-impedance state prior to the next driven level. When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: LH110LJ A;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2		V
$C_{i/o}$	Input/output capacitance		0.56		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.76		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

LH400LJ
4-BIT D-TYPE LATCH WITH ACTIVE-HIGH ENABLE

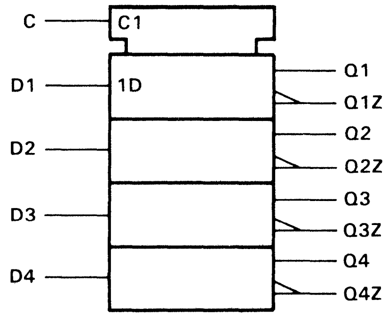
D3015, OCTOBER 1987

INTERNAL LATCH HARDWIRED MACRO

FUNCTION TABLE
(EACH LATCH)

INPUTS		OUTPUTS	
D_n	C	Q_n	QZ_n
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

logic symbol†



Similar to 7475

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The LH400LJ hardwired function implements a 4-bit D-type latch element. Information present at the data input is transferred in true form to the Q output and in inverted form to the QZ output when the enable input is high, and the outputs will follow the data input as long as enable C remains high. When enable goes low, the data that was present at the data input at the time the transition occurred is retained at the outputs until enable is taken high. When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: LH400LJ D1,D2,D3,D4,C,Q1,Q1Z,Q2,Q2Z,Q3,Q3Z,Q4,Q4Z;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
t_w	Pulse duration	C high	5		ns
		C low	5		
t_{su}	Setup time, D high or low		4		ns
t_h	Hold time, D high or low		1		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	D_n		0.08		pF
		C		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	3.92		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
t_{PLH}	C	Q_n	0.51	1.35	2.73	ns
t_{PHL}			0.47	1.17	2.27	
t_{PLH}	C	QZ_n	0.57	1.36	2.67	ns
t_{PHL}			0.58	1.51	3.07	
t_{PLH}	D_n	Q_n	0.3	0.71	1.33	ns
t_{PHL}			0.38	0.85	1.66	
t_{PLH}	D_n	QZ_n	0.49	1.06	2.07	ns
t_{PHL}			0.35	0.88	1.68	
Δt_{PLH}	Any	Q_n	0.36	0.89	1.72	ns/pF
Δt_{PHL}			0.26	0.57	1.07	
Δt_{PLH}	Any	QZ_n	0.66	1.59	3.09	ns/pF
Δt_{PHL}			0.73	1.85	3.61	

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

TAB20LJ
TOGGLE FLIP-FLOP
WITH CLEAR AND PRESET

D3015, OCTOBER 1987

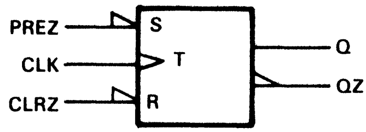
INTERNAL FLIP-FLOP HARDWIRED MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
PREZ	**CLRZ**	**CLK**	**Q**	**QZ**
L	H	X	H	L
H	L	X	L	H
L	L	X	L*	L*
H	H	L	$\overline{Q}_0$	Q_0
H	H	L	Q_0	$\overline{Q}_0$

* This configuration is nonstable; that is, it will not persist when PREZ or CLRZ returns to its inactive (high) level.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TAB20LJ hardwired gate-array macro implements a toggle flip-flop. The flip-flop incorporates direct inputs for both preset and clear providing the IC designer a full-function storage element to embed in ASICs in its most efficient form. It can be used as a stand-alone, bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TAB20LJ CLRZ,PREZ,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	131	MHz
t_w	Pulse duration	CLRZ low	4.1		ns
		PREZ low	2.7		
		CLK high or low	3.8		
t_{su}	Setup time	CLRZ inactive	0.3		ns
		PREZ inactive	0		

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TAB20LJ TOGGLE FLIP-FLOP WITH CLEAR AND PRESET

D3015, OCTOBER 1987

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLRZ		0.2		pF
		PREZ		0.2		
		CLK		0.2		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	3		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
t_{PLH}	CLK	Q	0.41	1.2	2.48	ns
t_{PHL}			0.37	1.08	2.3	
t_{PLH}	CLK	QZ	0.53	1.68	3.68	ns
t_{PHL}			0.55	1.67	3.55	
t_{PLH}	CLRZ	QZ	0.6	1.75	3.76	ns
t_{PHL}		Q	0.45	1.11	2.28	
t_{PLH}	PREZ	Q	0.62	1.71	3.63	ns
t_{PHL}		QZ	0.33	0.72	1.39	
Δt_{PLH}	CLK	Q	0.2	0.48	0.98	ns/pF
Δt_{PHL}			0.18	0.44	0.84	
Δt_{PLH}	CLK	QZ	0.18	0.44	0.82	ns/pF
Δt_{PHL}			0.14	0.32	0.6	
Δt_{PLH}	CLRZ	QZ	0.18	0.42	0.82	ns/pF
Δt_{PHL}		Q	0.16	0.44	0.9	
Δt_{PLH}	PREZ	Q	0.18	0.48	0.96	ns/pF
Δt_{PHL}		QZ	0.16	0.34	0.64	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TDB10LJ MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH CLEAR AND 1X OUTPUTS

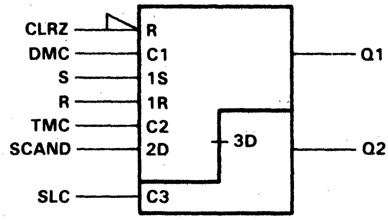
D3015, OCTOBER 1988

INTERNAL MACRO

FUNCTION TABLE

INPUTS							OUTPUTS	
DATA PATH			SCAN PATH		MASTER SLAVE		MASTER SLAVE	
S	R	DMC	SCAND	TMC	CLRZ	SLC	Q1	Q2
X	X	X	X	X	L	L	L	$Q2_0$
X	X	X	X	X	L	H	L	L
X	X	L	X	L	H	L	$Q1_0$	$Q2_0$
L	L	H	X	L	H	L	$Q1_0$	$Q2_0$
H	X	H	X	L	H	L	H	$Q2_0$
L	H	H	X	L	H	L	L	$Q2_0$
X	X	L	d1	H	H	L	d1	$Q2_0$
X	X	H	X	H	H	L	?	$Q2_0$
X	X	L	X	L	H	H	$Q1_0$	$Q1_0$
L	L	H	X	L	H	H	$Q1_0$	$Q1_0$
H	X	H	X	L	H	H	H	H
L	H	H	X	L	H	H	L	L
X	X	L	d1	H	H	H	d1	d1
X	X	H	X	H	H	H	?	?

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TDB10LJ macro implements a scan-input R-S/D-type latch with 1X drive master and slave outputs. The macro consists of an R-S/D-type master input-data and scan-data latch with active-low clear and single slave latch. In the data- or scan-path mode, either DMC or TMC can be used to select the entry and storage of data. When TMC is low and DMC is high, the Q1 output follows the R-S inputs. When DMC is subsequently taken low, the Q1 output is latched. When DMC is low and TMC is high, the Q1 output follows the SCAND input. When TMC is subsequently taken low, the Q1 output is latched. Data entered is available to the slave output latch, which follows the selected master input latch while SLC is high. Data at the Q2 output is latched by taking SLC low. The clock generator, CK120LJ provides nonoverlapping clock signals timed specifically for driving the DMC, TMC, and SLC clocks. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TDB10LJ DMC,TMC,SLC,S,R,SCAND,CLRZ,Q1,Q2;

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TDB10LJ MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH CLEAR AND 1X OUTPUTS

D3015, OCTOBER 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

			MIN	MAX	UNIT
f_{opr}	Operating frequency		0	76	MHz
t_w	Pulse duration	CLRZ low	3		ns
		DMC or TMC high	3		
		SLC high	2		
		R-S high	3		
t_{su}	Setup time	S high or low before DMC↓	4		ns
		R high or low before DMC↓	4		
		SCAND high or low before TMC↓	3		
		DMC or TMC low before SLC↑ (non-overlap)	3.5		
		SLC low before DMC or TMC↑ (non-overlap)	3.5		
t_h	Hold time	R-S high or low after DMC↓	0		
		SCAND high or low after TMC↓	0		
		DMC or TMC low after SLC↓ (non-overlap)	3.5		

NOTE 1: Additional data regarding pulse-duration, setup-time, and hold-time are incorporated in the engineering workstation library.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage				2	V
C_i	Input capacitance	CLRZ		0.07		pF
		DMC		0.15		
		R		0.07		
		S		0.07		
		SCAND		0.07		
		SLC		0.15		
		TMC		0.15		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	4.6		pF

† For supply current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	CLRZ	Q1	0.38	0.79	1.5	ns
t_{PHL}			0.61	1.52	3.1	
t_{PLH}	CLRZ	Q2	0.54	1.24	2.45	ns
t_{PHL}			0.61	1.52	3.1	
t_{PLH}	DMC	Q1	0.52	1.38	2.74	ns
t_{PHL}			0.67	1.6	3.15	
t_{PLH}	DMC	Q2	0.68	1.83	3.69	ns
t_{PHL}			0.83	2.1	4.27	
t_{PLH}	R	Q1	0.63	2.08	4.57	ns
t_{PHL}		Q2	0.78	2.57	5.69	
t_{PLH}	S	Q1	0.51	1.27	2.54	ns
t_{PHL}			0.72	1.92	4.04	
t_{PLH}	S	Q2	0.64	1.73	3.47	ns
t_{PHL}			0.88	2.39	5.16	
t_{PLH}	SCAND	Q1	0.52	1.26	2.5	ns
t_{PHL}			0.59	1.6	3.35	
t_{PLH}	SLC	Q2	0.35	0.92	1.84	ns
t_{PHL}			0.52	1.17	2.21	
t_{PLH}	TMC	Q1	0.51	1.39	2.75	ns
t_{PHL}			0.67	1.6	3.14	
t_{PLH}	TMC	Q2	0.68	1.83	3.7	ns
t_{PHL}			0.82	2.09	4.26	
Δt_{PLH}	CLRZ	Q1	0.35	0.9	1.77	ns/pF
Δt_{PHL}			0.3	0.73	1.41	
Δt_{PLH}	CLRZ	Q2	0.36	0.89	1.7	ns/pF
Δt_{PHL}			0.24	0.49	0.9	
Δt_{PLH}	DMC	Q1	0.35	0.9	1.76	ns/pF
Δt_{PHL}			0.26	0.58	1.06	
Δt_{PLH}	DMC	Q2	0.36	0.89	1.7	ns/pF
Δt_{PHL}			0.21	0.49	0.89	
Δt_{PHL}	R	Q1	0.27	0.58	1.06	ns/pF
Δt_{PHL}		Q2	0.22	0.49	0.9	ns/pF
Δt_{PLH}	S	Q1	0.36	0.91	1.76	ns/pF
Δt_{PHL}			0.28	0.58	1.06	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
Δt_{PLH}	S	Q2	0.36	0.88	1.7	ns/pF
Δt_{PHL}			0.23	0.5	0.9	
Δt_{PLH}	SCAND	Q1	0.36	0.91	1.76	ns/pF
Δt_{PHL}			0.29	0.57	1.07	
Δt_{PLH}	SLC	Q2	0.37	0.89	1.7	ns/pF
Δt_{PHL}			0.24	0.5	0.9	
Δt_{PLH}	TMC	Q1	0.36	0.9	1.76	ns/pF
Δt_{PHL}			0.26	0.58	1.06	
Δt_{PLH}	TMC	Q2	0.37	0.89	1.7	ns/pF
Δt_{PHL}			0.22	0.49	0.89	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

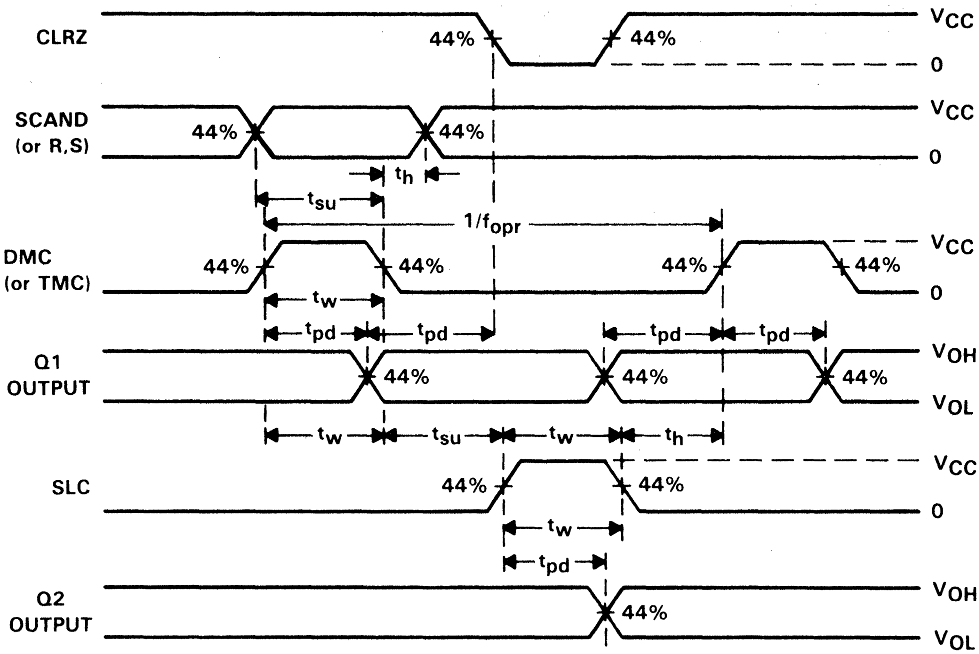
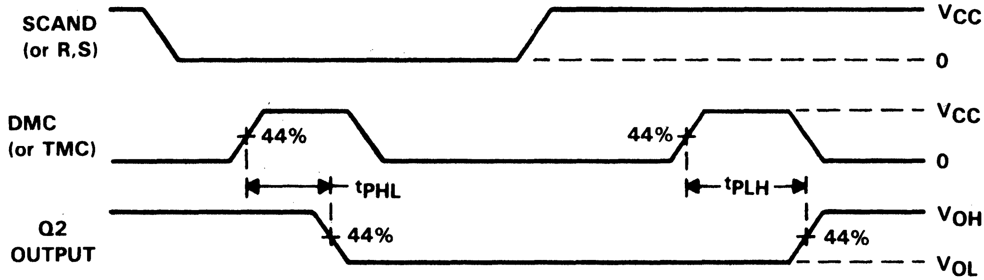
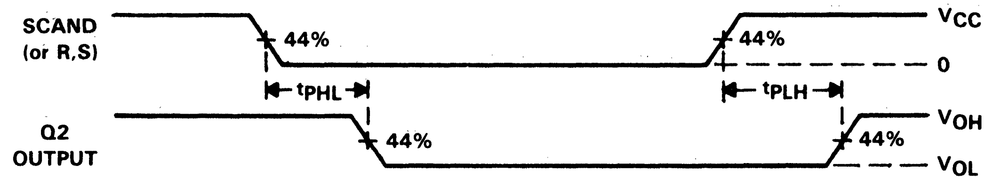


FIGURE 1. TIMING DIAGRAM



NOTE: SLC is high.

FIGURE 2. DMC OR TMC TO Q2 TIMING DIAGRAM



NOTE: DMC, TMC, SLC are high.

FIGURE 3. SCAND (OR R-S) TO Q2 OR QZ2 TIMING DIAGRAM

TDC11LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH MASTER CLEAR AND MASTER AND SLAVE 1X OUTPUTS

D3015, OCTOBER 1988

INTERNAL LATCH MACRO

FUNCTION TABLE

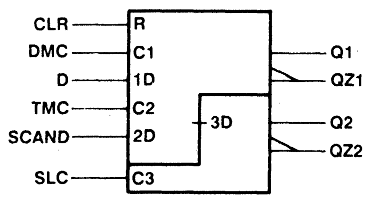
INPUTS						OUTPUTS			
DATA PATH		SCAN PATH		MASTER SLAVE		MASTER SLAVE			
D	DMC	SCAND	TMC	CLR	SLC	Q1	QZ1	Q2	QZ2
X	X	X	X	H	H	L	H	L	H
X	L	X	L	L	L	$Q1_0$	$QZ1_0$	$Q2_0$	$QZ2_0$
d1	H	X	L	L	L	d1	d1Z	$Q2_0$	$QZ2_0$
X	L	d2	H	L	L	d2	d2Z	$Q2_0$	$QZ2_0$
d1	H	d2	H	L	L	?	?Z	$Q2_0$	$QZ2_0$
X	L	X	L	L	H	$Q1_0$	$QZ1_0$	$Q1_0$	$QZ1_0$
d1	H	X	L	L	H	d1	d1Z	d1	d1Z
X	L	d2	H	L	H	d2	d2Z	d2	d2Z
d1	H	d2	H	L	H	?	?Z	?	?Z

description

The TDC11LJ macro implements a scan-input D-type latch with 1X-drive master and slave outputs. The macro consists of a dual D-type master input-data and scan-data latch with active-high clear and complementary outputs and a single slave latch with complementary outputs. In the data- or scan-path mode, either DMC or TMC can select the entry and storage of data. When TMC is low and DMC is high, the Q1 output follows the R-S inputs when DMC is subsequently taken low, the Q1 output is latched. When DMC is low and TMC is high, the Q1 output follows the SCAND input. When TMC is subsequently taken low, the Q1 output is latched. Data entered is available to the slave output latch, which follows the selected master input latch while SLC is high. Data at the Q2 and QZ2 outputs is latched by taking SLC low. The clock generator, CK120LJ, provides nonoverlapping clock signals timed specifically for the DMC, TMC, and SLC clocks. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TDC11LJ D,SCAND,CLR,DMC,TMC,SLC,Q1,QZ1,Q2,QZ2;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

			MIN	MAX	UNIT
f_{opr}	Operating frequency		0	100	MHz
t_w	Pulse duration	CLR high	3		ns
		DMC or TMC high	2.5		
		SLC high	2.5		
t_{su}	Setup time	D high or low before DMC↓	3		ns
		SCAND high or low before TMC↓	3		
		DMC or TMC low before SLC↑ (non-overlap)	2		
		SLC low before DMC or TMC↑ (non-overlap)	2		
t_h	Hold time	D high or low after DMC↓	0		ns
		SCAND high or low after TMC↓	0		
		DMC or TMC low after SLC↓ (non-overlap)	2		

NOTE 1: Additional data regarding pulse-duration, setup-time, and hold-time are incorporated in the engineering workstation library.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLR		0.07		pF
		D		0.07		
		DMC		0.15		
		SCAND		0.07		
		SLC		0.15		
		TMC		0.15		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	3.99		pF

† For supply current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	CLR	QZ1	0.19	0.46	0.84	ns
t_{PHL}		Q1	0.39	1.01	1.96	
t_{PLH}	CLR	QZ2	0.47	1.36	2.87	ns
t_{PHL}		Q2	0.56	1.67	3.48	
t_{PLH}	D	Q1	0.56	1.47	2.96	ns
t_{PHL}			0.57	1.59	3.45	
t_{PLH}	D	QZ1	0.41	1.08	2.35	ns
t_{PHL}			0.46	1.19	2.4	
t_{PLH}	D	Q2	0.77	2.07	4.21	ns
t_{PHL}			0.77	2.23	4.98	
t_{PLH}	D	QZ2	0.66	1.95	4.37	ns
t_{PHL}			0.73	1.91	3.89	
t_{PLH}	DMC	Q1	0.56	1.58	3.21	ns
t_{PHL}			0.68	1.61	3.22	
t_{PLH}	DMC	QZ1	0.49	1.09	2.13	ns
t_{PHL}			0.45	1.3	2.66	
t_{PLH}	DMC	Q2	0.75	2.17	4.48	ns
t_{PHL}			0.84	2.25	4.73	
t_{PLH}	DMC	QZ2	0.74	1.95	4.13	ns
t_{PHL}			0.71	2.01	4.15	
t_{PLH}	SCAND	Q1	0.57	1.47	2.96	ns
t_{PHL}			0.58	1.6	3.45	
t_{PLH}	SCAND	QZ1	0.41	1.08	2.36	ns
t_{PHL}			0.46	1.19	2.4	
t_{PLH}	SCAND	Q2	0.77	2.07	4.21	ns
t_{PHL}			0.77	2.23	4.98	
t_{PLH}	SCAND	QZ2	0.66	1.95	4.37	ns
t_{PHL}			0.73	1.91	3.89	
t_{PLH}	SLC	Q2	0.36	0.99	2.01	ns
t_{PHL}			0.6	1.3	2.5	
t_{PLH}	SLC	QZ2	0.5	1	1.89	ns
t_{PHL}			0.3	0.83	1.68	
t_{PLH}	TMC	Q1	0.57	1.59	3.22	ns
t_{PHL}			0.68	1.61	3.22	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TDC11LJ MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH MASTER CLEAR AND MASTER AND SLAVE 1X OUTPUTS

D3015, OCTOBER 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	TMC	QZ1	0.49	1.09	2.13	ns
t_{PHL}			0.46	1.31	2.67	
t_{PLH}	TMC	Q2	0.79	2.18	4.49	ns
t_{PHL}			0.84	2.25	4.73	
t_{PLH}	TMC	QZ2	0.74	1.95	4.13	ns
t_{PHL}			0.71	2.02	4.16	
Δt_{PLH}	CLR	QZ1	0.35	0.88	1.71	ns/pF
Δt_{PHL}		Q1	0.3	0.68	1.31	
Δt_{PLH}	CLR	QZ2	0.35	0.89	1.75	ns/pF
Δt_{PHL}		Q2	0.25	0.48	0.9	
Δt_{PLH}	D	Q1	0.36	0.88	1.69	ns/pF
Δt_{PHL}			0.27	0.53	0.96	
Δt_{PLH}	D	QZ1	0.36	0.9	1.75	ns/pF
Δt_{PHL}			0.27	0.62	1.16	
Δt_{PLH}	D	Q2	0.36	0.87	1.67	ns/pF
Δt_{PHL}			0.24	0.49	0.88	
Δt_{PLH}	D	QZ2	0.36	0.89	1.74	ns/pF
Δt_{PHL}			0.24	0.51	0.92	
Δt_{PLH}	DMC	Q1	0.35	0.87	1.69	ns/pF
Δt_{PHL}			0.24	0.52	0.96	
Δt_{PLH}	DMC	QZ1	0.35	0.89	1.75	ns/pF
Δt_{PHL}			0.27	0.61	1.16	
Δt_{PLH}	DMC	Q2	0.36	0.87	1.66	ns/pF
Δt_{PHL}			0.24	0.48	0.9	
Δt_{PLH}	DMC	QZ1	0.35	0.89	1.75	ns/pF
Δt_{PHL}			0.27	0.61	1.16	
Δt_{PLH}	SCAND	Q1	0.35	0.88	1.69	ns/pF
Δt_{PHL}			0.26	0.53	0.96	
Δt_{PLH}	SCAND	QZ1	0.36	0.9	1.75	ns/pF
Δt_{PHL}			0.27	0.62	1.16	
Δt_{PLH}	SCAND	Q2	0.36	0.87	1.67	ns/pF
Δt_{PHL}			0.24	0.49	0.88	
Δt_{PLH}	SCAND	QZ2	0.36	0.89	1.74	ns/pF
Δt_{PHL}			0.24	0.51	0.92	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
Δt_{PLH}	SLC	Q2	0.37	0.89	1.7	ns/pF
Δt_{PHL}			0.23	0.49	0.9	
Δt_{PLH}	SLC	QZ2	0.35	0.9	1.76	ns/pF
Δt_{PHL}			0.24	0.51	0.93	
Δt_{PLH}	TMC	Q1	0.36	0.87	1.69	ns/pF
Δt_{PHL}			0.24	0.52	0.96	
Δt_{PLH}	TMC	QZ1	0.35	0.89	1.75	ns/pF
Δt_{PHL}			0.27	0.61	1.16	
Δt_{PLH}	TMC	Q2	0.34	0.87	1.67	ns/pF
Δt_{PHL}			0.24	0.48	0.9	
Δt_{PLH}	TMC	QZ1	0.35	0.89	1.75	ns/pF
Δt_{PHL}			0.27	0.61	1.16	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TDC11LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH MASTER CLEAR AND MASTER AND SLAVE 1X OUTPUTS

D3015, OCTOBER 1988

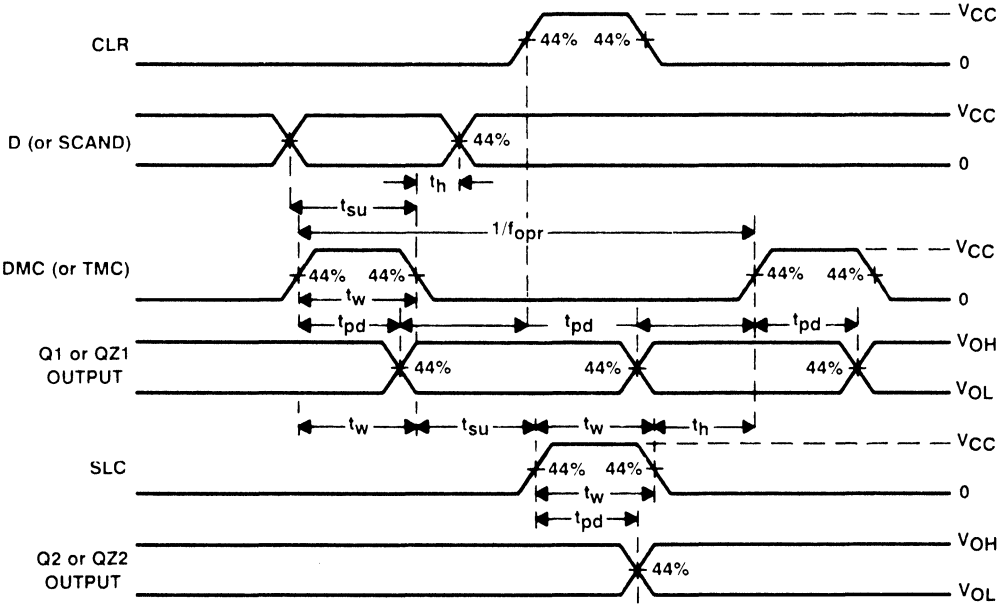
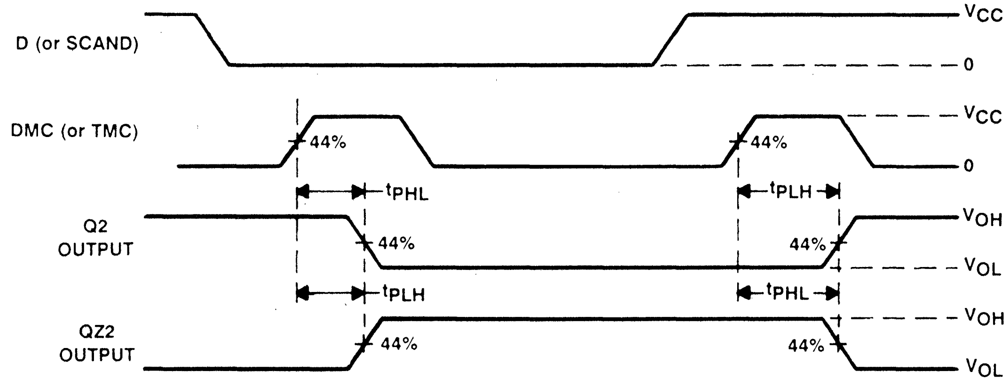
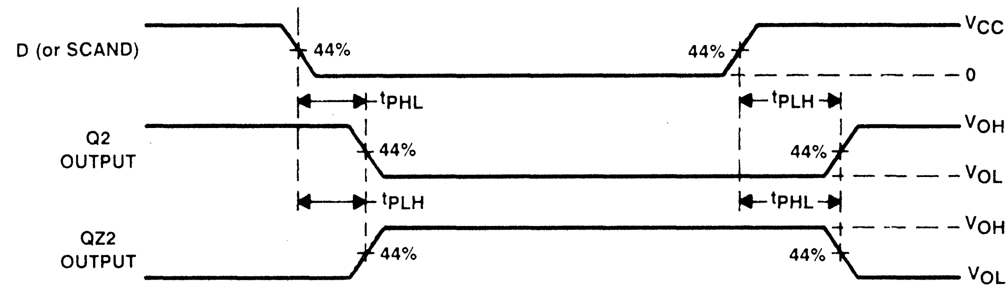


FIGURE 1. TIMING DIAGRAM



NOTE: SLC is high.

FIGURE 2. DMC OR TMC TO Q2 OR QZ2 TIMING DIAGRAM



NOTE: DMC, TMC, SLC are high.

FIGURE 3. D OR SCAND TO Q2 OR QZ2 TIMING DIAGRAM

TDN11LJ MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH 1X OUTPUTS

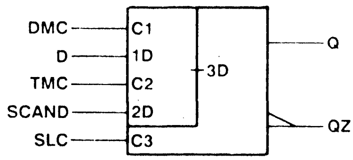
D3015, OCTOBER 1988

INTERNAL LATCH MACRO

FUNCTION TABLE

INPUTS					OUTPUTS	
DATA PATH		SCAN PATH		SLAVE		
D	DMC	SCAND	TMC	SLC	Q	QZ
X	L	X	L	L	Q_0	QZ_0
d1	H	X	L	L	Q_0	QZ_0
X	L	d2	H	L	Q_0	QZ_0
d1	H	d2	H	L	Q_0	QZ_0
X	L	X	L	H	Q_0	QZ_0
d1	H	X	L	H	d1	d1Z
X	L	d2	H	H	d2	d2Z
d1	H	d2	H	H	?	?Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TDN11LJ macro implements a scan-input D-type latch with 1X-drive outputs. The macro consists of a dual D-type input master latch for data and scan-data and a single slave latch with complementary outputs. In the data- or scan-path mode, either DMC or TMC can select the entry and storage of data. When TMC is low and DMC is high, the Q1 output follows the R-S inputs. When DMC is subsequently taken low, the Q1 output is latched. When DMC is low and TMC is high, the Q1 output follows the SCAND input. When TMC is subsequently taken low, the Q1 output is latched. Data entered is available to the slave output latch, which follows the selected master input latch while SLC is high. Data at the Q and QZ outputs is latched by taking SLC low. The clock generator, CK120LJ, provides nonoverlapping clock signals timed specifically for driving the DMC, TMC, and SLC clocks. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TDN11LJ D,SCAND,DMC,TMC,SLC,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

			MIN	MAX	UNIT
f_{opr}	Operating frequency			100	MHz
t_w	Pulse duration	DMC or TMC high	2.5		ns
		SLC high			
t_{su}	Setup time	D high or low before DMC↓	3		ns
		SCAND high or low before TMC↓	3		
		DMC or TMC low before SLC↑ (non-overlap)	2		
		SLC low before DMC or TMC↑ (non-overlap)	2		
t_h	Hold time	D high or low after DMC↓	0		ns
		SCAND high or low after TMC↓	0		
		DMC or TMC low after SLC↓ (non-overlap)	2		

NOTE 1: Additional data regarding pulse-duration, setup-time, and hold-time are incorporated in the engineering workstation library.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	D		0.07		pF
		DMC		0.15		
		SCAND		0.07		
		TMC		0.15		
		SLC		0.15		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	2.2		pF

† For supply current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	D	Q	0.6	1.52	2.98	ns
t_{PHL}			0.71	1.95	4.3	
t_{PLH}	D	QZ	0.59	1.67	3.69	ns
t_{PHL}			0.57	1.36	2.68	
t_{PLH}	DMC	Q	0.59	1.62	3.17	ns
t_{PHL}			0.78	1.97	4.07	
t_{PLH}	DMC	QZ	0.68	1.68	3.46	ns
t_{PHL}			0.56	1.47	2.85	
t_{PLH}	SCAND	Q	0.61	1.52	2.98	ns
t_{PHL}			0.71	1.95	4.3	
t_{PLH}	SCAND	QZ	0.59	1.67	3.69	ns
t_{PHL}			0.57	1.36	2.67	
t_{PLH}	SLC	Q	0.36	0.99	2.01	ns
t_{PHL}			0.6	1.3	2.5	
t_{PLH}	SLC	QZ	0.5	1	1.89	ns
t_{PHL}			0.3	0.83	1.69	
t_{PLH}	TMC	Q	0.62	1.63	3.19	ns
t_{PHL}			0.78	1.97	4.07	
t_{PLH}	TMC	QZ	0.68	1.68	3.45	ns
t_{PHL}			0.57	1.48	2.88	
Δt_{PLH}	D	Q	0.37	0.8	1.7	ns/pF
Δt_{PHL}			0.22	0.5	0.9	
Δt_{PLH}	D	QZ	0.37	0.9	1.75	ns/pF
Δt_{PHL}			0.23	0.51	0.93	
Δt_{PLH}	DMC	Q	0.37	0.89	1.7	ns/pF
Δt_{PHL}			0.24	0.5	0.9	
Δt_{PLH}	DMC	QZ	0.36	0.9	1.75	ns/pF
Δt_{PHL}			0.23	0.51	0.94	
Δt_{PLH}	SCAND	Q	0.36	0.88	1.7	ns/pF
Δt_{PHL}			0.22	0.5	0.9	
Δt_{PLH}	SCAND	QZ	0.37	0.9	1.75	ns/pF
Δt_{PHL}			0.23	0.51	0.93	
Δt_{PLH}	SLC	Q	0.37	0.89	1.7	ns/pF
Δt_{PHL}			0.23	0.49	0.9	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
Δt_{PLH}	SLC	QZ	0.35	0.9	1.76	ns/pF
Δt_{PHL}			0.24	0.51	0.93	
Δt_{PLH}	TMC	Q	0.36	0.89	1.7	ns/pF
Δt_{PHL}			0.24	0.5	0.9	
Δt_{PLH}	TMC	QZ	0.36	0.9	1.76	ns/pF
Δt_{PHL}			0.23	0.51	0.93	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TDN11LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH 1X OUTPUTS

D3015, OCTOBER 1988

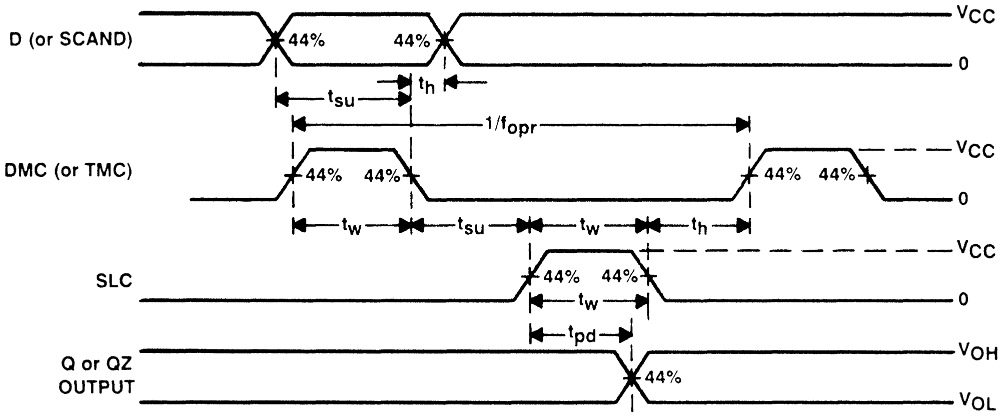
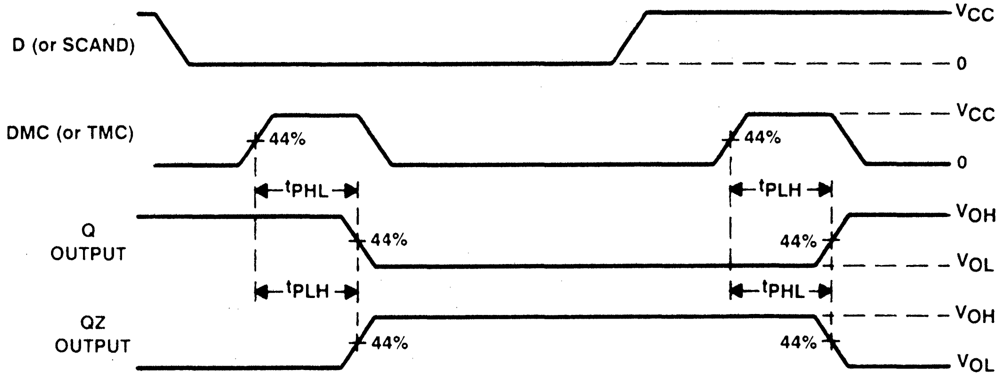
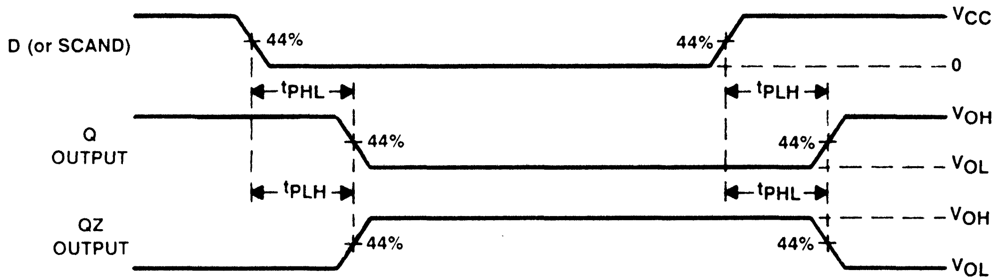


FIGURE 1. TIMING DIAGRAM



NOTE: SLC is high.

FIGURE 2. DMC OR TMC TO Q OR QZ TIMING DIAGRAM



NOTE: DMC, TMC, and SLC are high.

FIGURE 3. D OR SCAND TO Q OR QZ TIMING DIAGRAM

TDN12LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH MASTER AND SLAVE 1X OUTPUTS

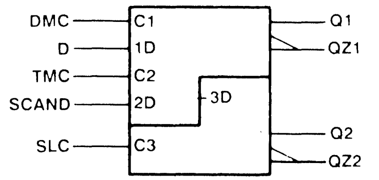
D3015, OCTOBER 1988

INTERNAL LATCH MACRO

FUNCTION TABLE

INPUTS					OUTPUTS			
DATA PATH		SCAN PATH		SLAVE	MASTER		SLAVE	
D	DMC	SCAND	TMC	SLC	Q1	QZ1	Q2	QZ2
X	L	X	L	L	$Q1_0$	$QZ1_0$	$Q2_0$	$QZ2_0$
d1	H	X	L	L	d1	d1Z	$Q2_0$	$QZ2_0$
X	L	d2	H	L	d2	d2Z	$Q2_0$	$QZ2_0$
d1	H	d2	H	L	?	?Z	$Q2_0$	$QZ2_0$
X	L	X	L	H	$Q1_0$	$QZ1_0$	$Q1_0$	$QZ1_0$
d1	H	X	L	H	d1	d1Z	d1	d1Z
X	L	d2	H	H	d2	d2Z	d2	d2Z
d1	H	d2	H	H	?	?Z	?	?Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TDN12LJ macro implements a scan-input D-type latch with 1X-drive master and slave outputs. The macro consists of a dual D-type master input-data and scan-data latch with complementary outputs and a single slave latch with complementary outputs. In the data- or scan-path mode, either DMC or TMC can select the entry and storage of data. When TMC is low and DMC is high, the Q1 output follows the R-S inputs. When DMC is subsequently taken low, the Q1 output is latched. When DMC is low and TMC is high, the Q1 output follows the SCAND input. When TMC is subsequently taken low, the Q1 output is latched. Data entered is available to the slave output latch, which follows the selected master input latch while SLC is high. Data at the Q2 and QZ2 outputs is latched by taking SLC low. The clock generator, CK120LJ, provides nonoverlapping clock signals timed specifically for driving the DMC, TMC, and SLC clocks. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TDN12LJ D,SCAND,DMC,TMC,SLC,Q1,QZ1,Q2,QZ2;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

			MIN	MAX	UNIT
f_{opr}	Operating frequency		0	100	MHz
t_w	Pulse duration	DMC or TMC high			ns
		SLC high	2.5		
t_{su}	Setup time	D high or low before DMC↓	3		ns
		SCAND high or low before TMC↓	3		
		DMC or TMC low before SLC↑ (non-overlap)	2		
		SLC low before DMC or TMC↑ (non-overlap)	2		
t_h	Hold time	D high or low after DMC↓	0		ns
		SCAND high or low after TMC↓	0		
		DMC or TMC low after SLC↓ (non-overlap)	2		

NOTE 1: Additional data regarding pulse-duration, setup-time, and hold-time are incorporated in the engineering workstation library.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	D		0.07		pF
		DMC		0.15		
		SCAND		0.07		
		SLC		0.15		
		TMC		0.15		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	3.69		pF

† For supply current, I_{CC}, see the TGC100 Series Data.

TEXAS INSTRUMENTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	D	Q1	0.49	1.13	2.16	ns
t_{PHL}			0.56	1.54	3.32	
t_{PLH}	D	QZ1	0.39	1.03	2.21	ns
t_{PHL}			0.39	0.87	1.66	
t_{PLH}	D	Q2	0.72	1.72	3.42	ns
t_{PHL}			0.76	1.17	4.83	
t_{PLH}	D	QZ2	0.66	1.89	4.23	ns
t_{PHL}			0.61	1.56	3.09	
t_{PLH}	DMC	Q1	0.48	1.22	2.38	ns
t_{PHL}			0.69	1.54	3.06	
t_{PLH}	DMC	QZ1	0.51	1.02	1.96	ns
t_{PHL}			0.37	0.97	1.88	
t_{PLH}	DMC	Q2	0.71	1.81	3.61	ns
t_{PHL}			0.85	2.17	4.58	
t_{PLH}	DMC	QZ2	0.75	1.89	3.96	ns
t_{PHL}			0.61	1.66	3.29	
t_{PLH}	SCAND	Q1	0.49	1.13	2.15	ns
t_{PHL}			0.56	1.54	3.32	
t_{PLH}	SCAND	QZ1	0.39	1.03	2.21	ns
t_{PHL}			0.39	0.87	1.66	
t_{PLH}	SCAND	Q2	0.72	1.72	3.42	ns
t_{PHL}			0.76	2.17	4.84	
t_{PLH}	SCAND	QZ2	0.66	1.89	4.23	ns
t_{PHL}			0.61	1.56	3.09	
t_{PLH}	SLC	Q2	0.36	0.99	2.01	ns
t_{PHL}			0.6	1.3	2.5	
t_{PLH}	SLC	QZ2	0.5	1	1.89	ns
t_{PHL}			0.3	0.83	1.68	
t_{PLH}	TMC	Q1	0.37	0.97	1.88	ns
t_{PHL}			0.49	1.23	2.4	
t_{PLH}	TMC	QZ1	0.51	1.02	1.96	ns
t_{PHL}			0.37	0.99	1.9	
t_{PLH}	TMC	Q2	0.72	1.82	3.63	ns
t_{PHL}			0.85	2.17	4.59	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	TMC	QZ2	0.75	1.89	3.96	ns
t_{PHL}			0.62	1.67	3.3	
Δt_{PLH}	D	Q1	0.35	0.88	1.7	ns/pF
Δt_{PHL}			0.26	0.54	0.95	
Δt_{PLH}	D	QZ1	0.37	0.91	1.76	ns/pF
Δt_{PHL}			0.24	0.52	0.95	
Δt_{PLH}	D	Q2	0.36	0.87	1.68	ns/pF
Δt_{PHL}			0.24	0.5	0.89	
Δt_{PLH}	D	QZ2	0.35	0.9	1.74	ns/pF
Δt_{PHL}			0.26	0.51	0.92	
Δt_{PLH}	DMC	Q1	0.35	0.88	1.7	ns/pF
Δt_{PHL}			0.24	0.53	0.95	
Δt_{PLH}	DMC	QZ1	0.35	0.91	1.77	ns/pF
Δt_{PHL}			0.24	0.52	0.95	
Δt_{PLH}	DMC	Q2	0.36	0.88	1.69	ns/pF
Δt_{PHL}			0.24	0.49	0.88	
Δt_{PLH}	DMC	QZ2	0.36	0.89	1.75	ns/pF
Δt_{PHL}			0.26	0.5	0.93	
Δt_{PLH}	SCAND	Q1	0.35	0.88	1.71	ns/pF
Δt_{PHL}			0.26	0.54	0.95	
Δt_{PLH}	SCAND	QZ1	0.37	0.91	1.76	ns/pF
Δt_{PHL}			0.24	0.52	0.95	
Δt_{PLH}	SCAND	Q2	0.36	0.87	1.68	ns/pF
Δt_{PHL}			0.24	0.5	0.89	
Δt_{PLH}	SCAND	QZ2	0.35	0.9	1.74	ns/pF
Δt_{PHL}			0.26	0.51	0.92	
Δt_{PLH}	SLC	Q2	0.37	0.89	1.7	ns/pF
Δt_{PHL}			0.23	0.49	0.9	
Δt_{PLH}	SLC	QZ2	0.35	0.9	1.76	ns/pF
Δt_{PHL}			0.24	0.51	0.93	
Δt_{PLH}	TMC	Q1	0.35	0.88	1.7	ns/pF
Δt_{PHL}			0.24	0.53	0.95	
Δt_{PLH}	TMC	QZ1	0.35	0.91	1.77	ns/pF
Δt_{PHL}			0.25	0.51	0.95	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$ (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
Δt_{PLH}	TMC	Q2	0.36	0.88	1.69	ns/pF
Δt_{PHL}			0.24	0.49	0.87	
Δt_{PLH}	TMC	QZ2	0.36	0.89	1.75	ns/pF
Δt_{PHL}			0.26	0.5	0.94	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

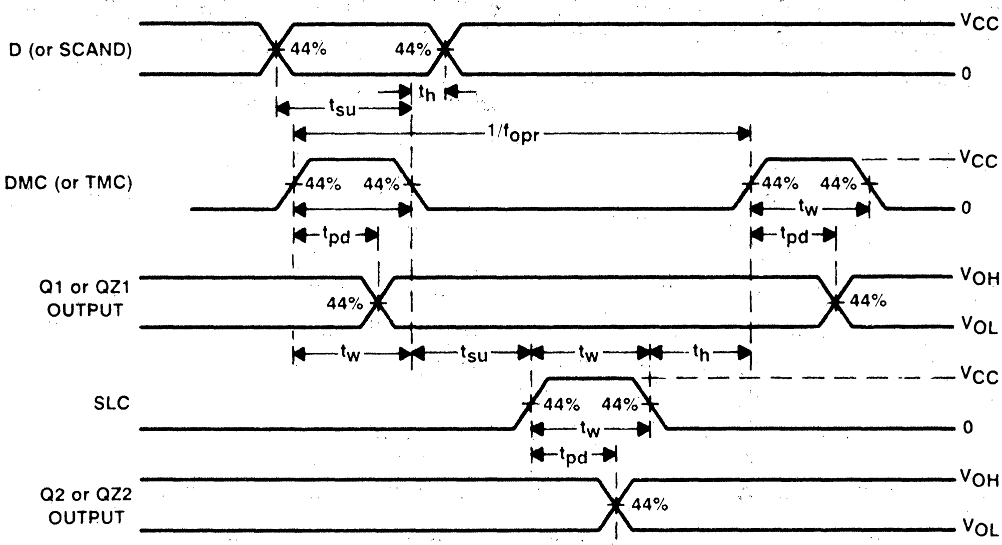
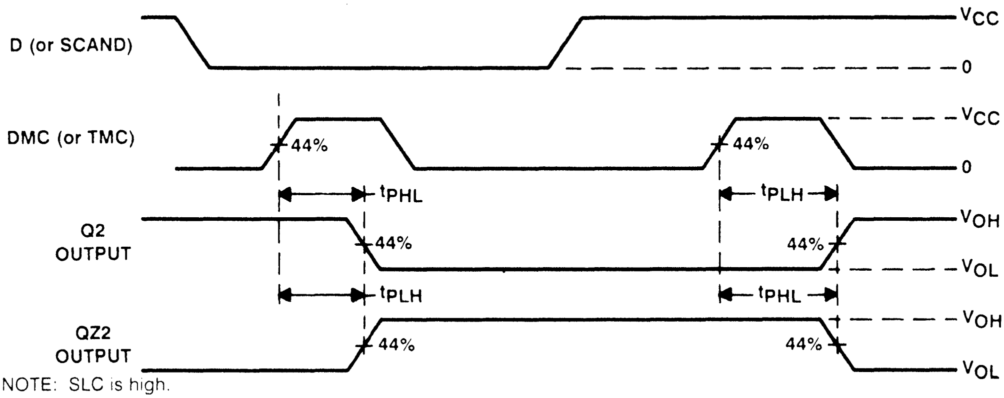


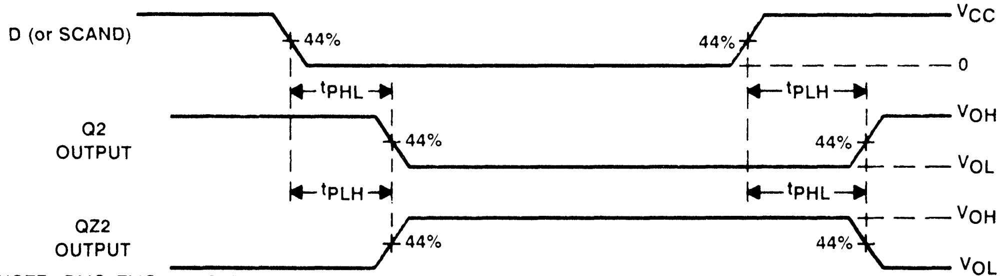
FIGURE 1. TIMING DIAGRAM

D3015, OCTOBER 1988



NOTE: SLC is high.

FIGURE 2. DMC OR TMC TO Q2 OR QZ2 TIMING DIAGRAM



NOTE: DMC, TMC, and SLC are high.

FIGURE 3. D OR SCAND TO Q2 OR QZ2 TIMING DIAGRAM

TDN13LJ MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH SLAVE D-INPUT, MASTER AND SLAVE 1X OUTPUTS

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INTERNAL LATCH MACRO

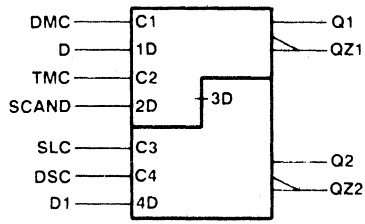
FUNCTION TABLE

MASTER INPUTS				SLAVE INPUTS			OUTPUTS			
DATA PATH		SCAN PATH		SLAVE	SLAVE DATA		MASTER		SLAVE	
D	DMC	SCAND	TMC	SLC	D1	DSC	Q1	QZ1	Q2	QZ2
X	L	X	L	L	X	L	$Q1_0$	$\overline{Q}Z1_0$	$Q2_0$	$\overline{Q}Z2_0$
d1	H	X	L	L	X	L	d1	$\overline{d}1Z$	$Q2_0$	$\overline{Q}Z2_0$
X	L	d2	H	L	X	L	d2	$\overline{d}2Z$	$Q2_0$	$\overline{Q}Z2_0$
d1	H	d2	H	L	X	L	?	?Z	$Q2_0$	$\overline{Q}Z2_0$
X	L	X	L	H	X	L	$Q1_0$	$\overline{Q}Z1_0$	$Q1_0$	$\overline{Q}Z1_0$
d1	H	X	L	H	X	L	d1	$\overline{d}1Z$	d1	$\overline{d}1Z$
X	L	d2	H	H	X	L	d2	$\overline{d}2Z$	d2	$\overline{d}2Z$
d1	H	d2	H	H	X	L	?	?Z	?	?Z
X	L	X	L	L	d3	H	$Q1_0$	$\overline{Q}Z1_0$	d3	$\overline{d}3Z$
d1	H	X	L	L	d3	H	d1	$\overline{d}1Z$	d3	$\overline{d}3Z$
X	L	d2	H	L	d3	H	d2	$\overline{d}2Z$	d3	$\overline{d}3Z$
d1	H	d2	H	L	d3	H	?	?Z	d3	$\overline{d}3Z$
X	L	X	L	H	d3	H	$Q1_0$	$\overline{Q}Z1_0$	?	?Z
d1	H	X	L	H	d3	H	d1	$\overline{d}1Z$	?	?Z
X	L	d2	H	H	d3	H	d2	$\overline{d}2Z$	?	?Z
d1	H	d2	H	H	d3	H	?	?Z	?	?Z

description

The TDN13LJ macro implements a scan-input D-type latch with 1X-drive master and slave outputs. The macro consists of a dual D-type master input-data and scan-data latch with complementary outputs and a single slave latch with a data input and complementary outputs. In the data- or scan-path mode, either DMC or TMC can select the entry and storage of data. When TMC is low and DMC is high, the Q1 output follows the R-S inputs. When DMC is subsequently taken low, the Q1 output is latched. When DMC is low and TMC is high, the Q1 output follows the SCAND input. When TMC is subsequently taken low, the Q1 output is latched. Data entered is available to the slave output latch,

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

which follows the selected master input latch while SLC is high and DSC is low. Data at the Q2 and QZ2 outputs is latched by taking SLC low. When SLC is low and while DSC is high, the Q2 output follows the D1 input. When DSC is subsequently taken low, the Q2 output is latched. The clock generator, CK120LJ, provides nonoverlapping clock signals timed specifically for driving the DMC, TMC, and SLC clocks. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TDN13LJ D,D1,SCAND,DMC,DSC,TMC,SLC,Q1,QZ1,Q2,QZ2;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

			MIN	MAX	UNIT
f_{opr}	Operating frequency			100	MHz
t_w	Pulse duration	DMC or TMC high	2.5		ns
		SLC or DSC high			
t_{su}	Setup time	D high or low before DMC↓	3		ns
		SCAND high or low before TMC↓	3		
		D1 high or low before DSC↓	3		
		DMC or TMC low before SLC↑ (non-overlap)	2		
		SLC low before DMC or TMC↑ (non-overlap)	2		
t_h	Hold time	D high or low After DMC↓	0		ns
		SCAND high or low after TMC↓	0		
		D1 high or low After DSC↓	0		
		DMC or TMC low after SLC↓ (non-overlap)	2		

NOTE 1: Additional data regarding pulse-duration, setup-time, and hold-time are incorporated in the engineering workstation library.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	D		0.07		pF
		D1		0.07		
		DMC		0.15		
		DSC		0.15		
		SCAND		0.07		
		SLC		0.15		
		TMC		0.15		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	4		pF

† For supply current, I_{CC} see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	D	Q1	0.51	1.16	2.21	ns
t_{PHL}			0.58	1.62	3.45	
t_{PLH}	D	QZ1	0.39	1.04	2.21	ns
t_{PHL}			0.39	0.87	1.66	
t_{PLH}	D	Q2	0.74	1.76	3.5	ns
t_{PHL}			0.8	2.31	5.07	
t_{PLH}	D	QZ2	0.67	1.99	4.4	ns
t_{PHL}			0.63	1.6	3.15	
t_{PLH}	DMC	Q1	0.5	1.25	2.43	ns
t_{PLH}			0.71	1.61	3.2	
t_{PHL}	DMC	QZ1	0.51	1.02	1.95	ns
t_{PLH}			0.37	0.97	1.88	
t_{PHL}	DMC	Q2	0.72	1.87	3.71	ns
t_{PHL}			0.91	2.29	4.81	
t_{PLH}	DMC	QZ2	0.8	1.96	4.15	ns
t_{PHL}			0.62	1.69	3.35	
t_{PLH}	DSC	Q2	0.43	1.19	2.3	ns
t_{PHL}			0.61	1.33	2.61	
t_{PLH}	DSC	QZ2	0.51	1.02	1.97	ns
t_{PHL}			0.38	1.02	1.95	
t_{PLH}	D1	Q2	0.42	1.04	1.98	ns
t_{PHL}			0.5	1.35	2.9	
t_{PLH}	D1	QZ2	0.39	1.05	2.23	ns
t_{PHL}			0.39	0.86	1.64	
t_{PLH}	SCAND	Q1	0.51	1.16	2.2	ns
t_{PHL}			0.58	1.62	3.45	
t_{PLH}	SCAND	QZ1	0.39	1.04	2.21	ns
t_{PHL}			0.39	0.87	1.65	
t_{PLH}	SCAND	Q2	0.74	1.76	3.5	ns
t_{PHL}			0.8	2.31	5.08	
t_{PLH}	SCAND	QZ2	0.67	1.99	4.41	ns
t_{PHL}			0.63	1.59	3.15	
t_{PLH}	SLC	Q2	0.42	1.18	2.27	ns
t_{PHL}			0.61	1.33	2.61	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$ (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	SLC	QZ2	0.51	1.02	1.96	ns
t_{PHL}			0.38	1	1.96	
t_{PLH}	TMC	Q1	0.51	1.26	2.45	ns
t_{PHL}			0.71	1.61	3.2	
t_{PLH}	TMC	QZ1	0.51	1.02	1.96	ns
t_{PHL}			0.37	0.99	1.9	
t_{PLH}	TMC	Q2	0.73	1.88	3.74	ns
t_{PHL}			0.9	2.29	4.81	
t_{PLH}	TMC	QZ2	0.8	1.97	4.15	ns
t_{PHL}			0.63	1.7	3.38	
Δt_{PLH}	D	Q1	0.35	0.88	1.71	ns/pF
Δt_{PHL}			0.28	0.54	0.98	
Δt_{PLH}	D	QZ1	0.37	0.9	1.76	ns/pF
Δt_{PHL}			0.24	0.52	0.95	
Δt_{PLH}	D	Q2	0.36	0.88	1.69	ns/pF
Δt_{PHL}			0.22	0.49	0.89	
Δt_{PLH}	D	QZ2	0.36	0.89	1.74	ns/pF
Δt_{PHL}			0.26	0.5	0.92	
Δt_{PLH}	DMC	Q1	0.35	0.88	1.71	ns/pF
Δt_{PHL}			0.26	0.54	0.98	
Δt_{PLH}	DMC	QZ1	0.35	0.91	1.77	ns/pF
Δt_{PHL}			0.24	0.52	0.95	
Δt_{PLH}	DMC	Q2	0.37	0.88	1.69	ns/pF
Δt_{PHL}			0.24	0.5	0.9	
Δt_{PLH}	DMC	QZ2	0.35	0.9	1.74	ns/pF
Δt_{PHL}			0.26	0.51	0.94	
Δt_{PLH}	DSC	Q2	0.37	0.88	1.7	ns/pF
Δt_{PHL}			0.25	0.51	0.92	
Δt_{PLH}	DSC	QZ2	0.35	0.91	1.76	ns/pF
Δt_{PHL}			0.25	0.51	0.94	
Δt_{PLH}	D1	Q2	0.38	0.89	1.7	ns/pF
Δt_{PHL}			0.25	0.51	0.91	
Δt_{PLH}	D1	QZ2	0.37	0.9	1.75	ns/pF
Δt_{PHL}			0.24	0.51	0.93	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$ (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
Δt_{PLH}	SCAND	Q1	0.35	0.88	1.71	ns/pF
Δt_{PHL}			0.28	0.54	0.98	
Δt_{PLH}	SCAND	QZ1	0.37	0.9	1.76	ns/pF
Δt_{PHL}			0.24	0.52	0.95	
Δt_{PLH}	SCAND	Q2	0.36	0.88	1.69	ns/pF
Δt_{PHL}			0.22	0.49	0.89	
Δt_{PLH}	SCAND	QZ2	0.36	0.89	1.74	ns/pF
Δt_{PHL}			0.26	0.5	0.92	
Δt_{PLH}	SLC	Q2	0.37	0.88	1.7	ns/pF
Δt_{PHL}			0.25	0.51	0.92	
Δt_{PLH}	SLC	QZ2	0.35	0.91	1.76	ns/pF
Δt_{PHL}			0.24	0.51	0.94	
Δt_{PLH}	TMC	Q1	0.35	0.88	1.71	ns/pF
Δt_{PHL}			0.26	0.54	0.98	
Δt_{PLH}	TMC	QZ1	0.35	0.91	1.77	ns/pF
Δt_{PHL}			0.25	0.51	0.95	
Δt_{PLH}	TMC	Q2	0.37	0.88	1.68	ns/pF
Δt_{PHL}			0.25	0.5	0.9	
Δt_{PLH}	TMC	QZ2	0.35	0.9	1.74	ns/pF
Δt_{PHL}			0.25	0.51	0.93	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH SLAVE D-INPUT, MASTER AND SLAVE 1X OUTPUTS

D3015, OCTOBER 1988

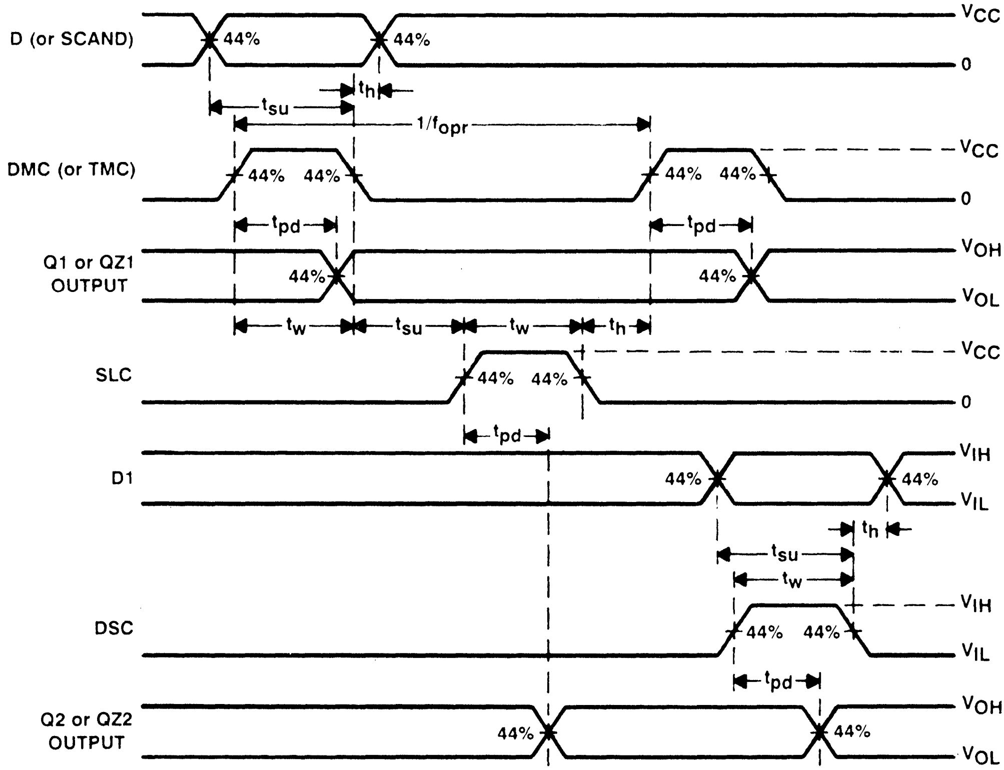
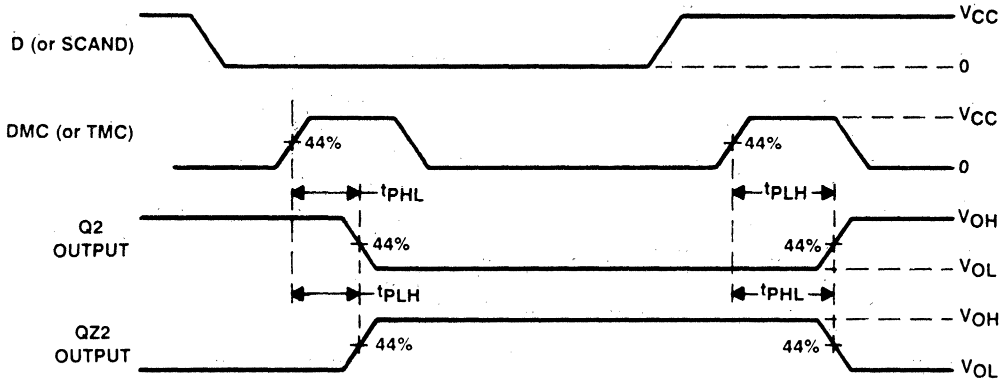
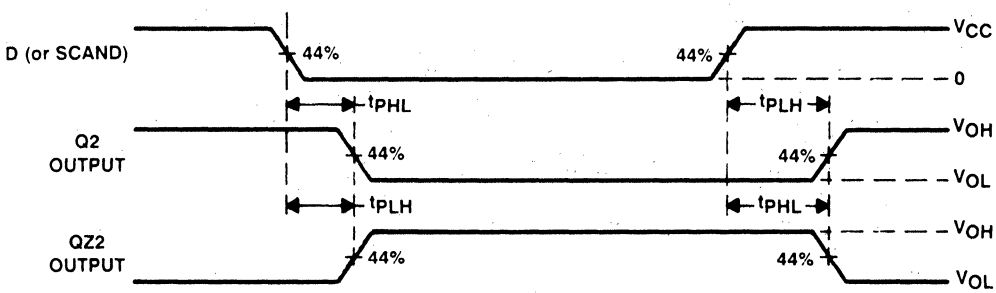


FIGURE 1. TIMING DIAGRAM



NOTE: SLC is high.

FIGURE 2. DMC OR TMC TO Q2 OR QZ2 TIMING DIAGRAM



NOTE: DMC, TMC, SLC are high.

FIGURE 3. D OR SCAND TO Q2 OR QZ2 TIMING DIAGRAM

TDN22LJ MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH MASTER AND SLAVE 2X OUTPUTS

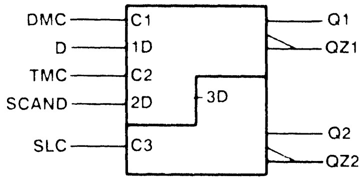
D3015, OCTOBER 1988

INTERNAL LATCH MACRO

FUNCTION TABLE

INPUTS					OUTPUTS			
DATA PATH		SCAN PATH		SLAVE	MASTER SLAVE			
D	DMC	SCAND	TMC	SLC	Q1	QZ1	Q2	QZ2
X	L	X	L	L	$Q1_0$	$QZ1_0$	$Q2_0$	$QZ2_0$
d1	H	X	L	L	d1	d1Z	$Q2_0$	$QZ2_0$
X	L	d2	H	L	d2	d2Z	$Q2_0$	$QZ2_0$
d1	H	d2	H	L	?	?Z	$Q2_0$	$QZ2_0$
X	L	X	L	H	$Q1_0$	$QZ1_0$	$Q1_0$	$QZ1_0$
d1	H	X	L	H	d1	d1Z	d1	d1Z
X	L	d2	H	H	d2	d2Z	d2	d2Z
d1	H	d2	H	H	?	?Z	?	?Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TDN22LJ macro implements a scan-input D-type latch with 2X-drive master and slave outputs. The macro consists of a dual D-type master input-data and scan-data latch with complementary outputs and a single slave latch with complementary outputs. In the data- or scan-path mode, either DMC or TMC can select the entry and storage of data. When TMC is low and DMC is high, the Q1 output follows the R-S inputs. When DMC is subsequently taken low, the Q1 output is latched. When DMC is low and TMC is high, the Q1 output follows the SCAND input. When TMC is subsequently taken low, the Q1 output is latched. Data entered is available to the slave output latch, which follows the selected master input latch while SLC is high. Data at the Q2 and QZ2 outputs is latched by taking SLC low. The clock generator, CK120LJ, provides nonoverlapping clock signals timed specifically for driving the DMC, TMC, and SLC clocks. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TDN22LJ D,SCAND,DMC,TMC,SLC,Q1,QZ1,Q2,QZ2;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

TDN22LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH MASTER AND SLAVE 2X OUTPUTS

D3015, OCTOBER 1988

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

			MIN	MAX	UNIT
f_{opr}	Operating frequency			83	MHz
t_w	Pulse duration	DMC or TMC high	2.5		ns
		SLC high			
t_{su}	Setup time	D high or low before DMC↓	3		ns
		SCAND high or low before TMC↓	3		
		DMC or TMC low before SLC↑ (non-overlap)	2		
		SLC low before DMC or TMC↑ (non-overlap)	2		
t_h	Hold time	D high or low After DMC↓	0		ns
		SCAND high or low after TMC↓	0		
		DMC or TMC low after SLC↓ (non-overlap)	2		

NOTE 1: Additional data regarding pulse-duration, setup-time, and hold-time are incorporated in the engineering workstation library.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	D		0.07		pF
		DMC		0.15		
		SCAND		0.07		
		SLC		0.15		
		TMC		0.15		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	5.8		pF

† For supply current, I_{CC}, see the TGC100 Series Data.

TDN22LJ MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH MASTER AND SLAVE 2X OUTPUTS

D3015, OCTOBER 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	D	Q1	0.53	1.28	2.48	ns
t_{PHL}			0.59	1.67	3.67	
t_{PLH}	D	QZ1	0.43	1.11	2.4	ns
t_{PHL}			0.4	0.92	1.74	
t_{PLH}	D	Q2	0.77	2.07	4.19	ns
t_{PHL}			0.85	2.57	5.73	
t_{PLH}	D	QZ2	0.69	2.18	4.9	ns
t_{PHL}			0.65	1.76	3.55	
t_{PLH}	DMC	Q1	0.5	1.37	2.71	ns
t_{PHL}			0.68	1.68	3.43	
t_{PLH}	DMC	QZ1	0.49	1.12	2.18	ns
t_{PHL}			0.39	0.99	1.95	
t_{PLH}	DMC	Q2	0.74	2.17	4.41	ns
t_{PHL}			0.89	2.55	5.48	
t_{PLH}	DMC	QZ2	0.81	2.17	4.65	ns
t_{PHL}			0.61	1.88	3.8	
t_{PLH}	SCAND	Q1	0.53	1.28	2.48	ns
t_{PHL}			0.59	1.67	3.67	
t_{PLH}	SCAND	QZ1	0.43	1.11	2.41	ns
t_{PHL}			0.4	0.92	1.74	
t_{PLH}	SCAND	Q2	0.77	2.07	4.19	ns
t_{PHL}			0.85	2.57	5.73	
t_{PLH}	SCAND	QZ2	0.69	2.18	4.91	ns
t_{PHL}			0.65	1.76	3.55	
t_{PLH}	SLC	Q2	0.38	1.16	2.36	ns
t_{PHL}			0.64	1.46	2.92	
t_{PLH}	SLC	QZ2	0.49	1.09	2.12	ns
t_{PHL}			0.28	0.88	1.77	
t_{PLH}	TMC	Q1	0.51	1.37	2.73	ns
t_{PHL}			0.68	1.68	3.43	
t_{PLH}	TMC	QZ1	0.49	1.12	2.18	ns
t_{PHL}			0.4	1.01	1.99	
t_{PLH}	TMC	Q2	0.78	2.17	4.43	ns
t_{PHL}			0.89	2.54	5.48	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	TMC	QZ2	0.81	2.17	4.65	ns
t_{PHL}			0.63	1.9	3.82	
Δt_{PLH}	D	Q1	0.18	0.43	0.85	ns/pF
Δt_{PHL}			0.14	0.33	0.6	
Δt_{PLH}	D	QZ1	0.16	0.45	0.89	ns/pF
Δt_{PHL}			0.13	0.31	0.6	
Δt_{PLH}	D	Q2	0.18	0.4	0.76	ns/pF
Δt_{PHL}			0.09	0.26	0.51	
Δt_{PLH}	D	QZ2	0.18	0.43	0.85	ns/pF
Δt_{PHL}			0.18	0.32	0.59	
Δt_{PLH}	DMC	Q1	0.19	0.43	0.84	ns/pF
Δt_{PHL}			0.15	0.32	0.61	
Δt_{PLH}	DMC	QZ1	0.19	0.44	0.89	ns/pF
Δt_{PHL}			0.12	0.33	0.62	
Δt_{PLH}	DMC	Q2	0.18	0.39	0.77	ns/pF
Δt_{PHL}			0.17	0.27	0.52	
Δt_{PLH}	DMC	QZ2	0.16	0.43	0.86	ns/pF
Δt_{PHL}			0.19	0.28	0.57	
Δt_{PLH}	SCAND	Q1	0.18	0.43	0.85	ns/pF
Δt_{PHL}			0.14	0.33	0.6	
Δt_{PLH}	SCAND	QZ1	0.16	0.45	0.89	ns/pF
Δt_{PHL}			0.13	0.31	0.6	
Δt_{PLH}	SCAND	Q2	0.18	0.4	0.76	ns/pF
Δt_{PHL}			0.09	0.26	0.51	
Δt_{PLH}	SCAND	QZ2	0.18	0.43	0.85	ns/pF
Δt_{PHL}			0.18	0.32	0.59	
Δt_{PLH}	SLC	Q2	0.18	0.42	0.82	ns/pF
Δt_{PHL}			0.11	0.29	0.56	
Δt_{PLH}	SLC	QZ2	0.19	0.44	0.89	ns/pF
Δt_{PHL}			0.17	0.3	0.6	
Δt_{PLH}	TMC	Q1	0.19	0.44	0.84	ns/pF
Δt_{PHL}			0.15	0.32	0.61	
Δt_{PLH}	TMC	QZ1	0.19	0.44	0.89	ns/pF
Δt_{PHL}			0.12	0.33	0.61	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
Δt_{PLH}	TMc	Q2	0.16	0.4	0.77	ns/pF
Δt_{PHL}			0.17	0.28	0.52	
Δt_{PLH}	TMC	QZ2	0.16	0.43	0.86	ns/pF
Δt_{PHL}			0.18	0.28	0.57	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

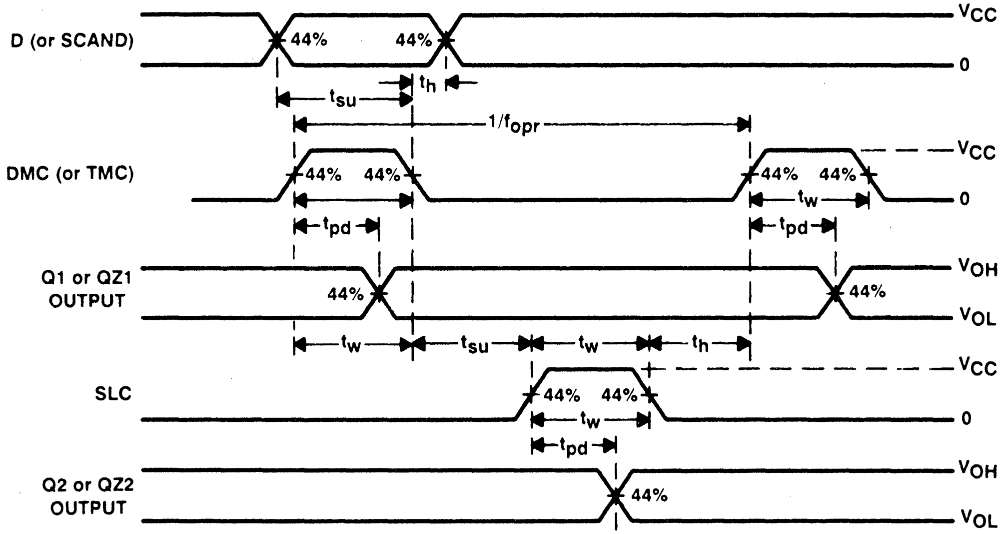
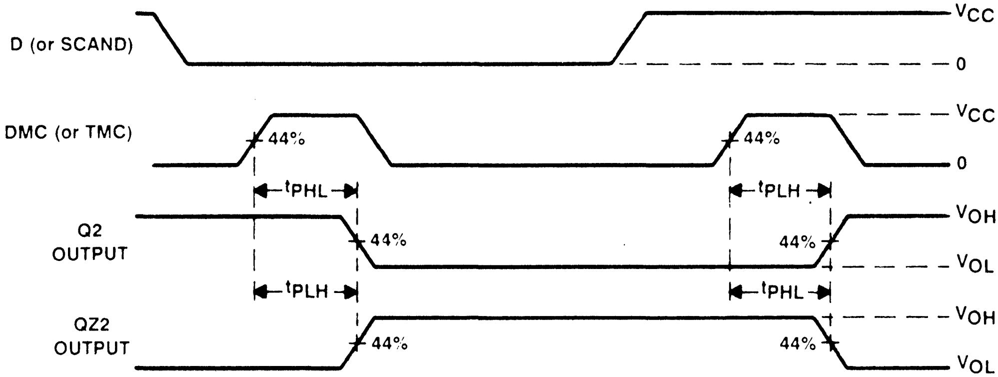
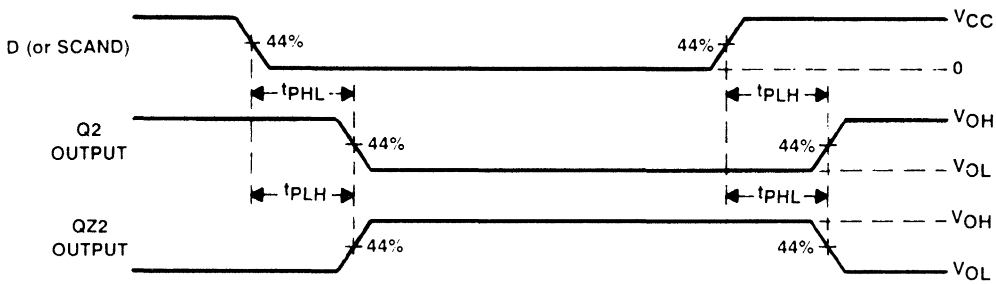


FIGURE 1. TIMING DIAGRAM



NOTE: SLC is high.

FIGURE 2. DMC OR TMC TO Q2 OR QZ2 TIMING DIAGRAM



NOTE: DMC, TMC, SLC are high.

FIGURE 3. D OR SCAND TO Q2 OR QZ2 TIMING DIAGRAM

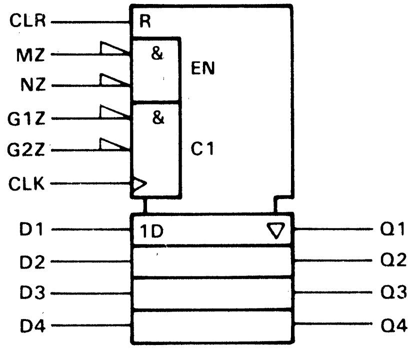
S173LJ 4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

D3015, OCTOBER 1987

SOFTWARE MACRO

- 3-State Outputs Interface Internal Data Buses Directly
- Direct Clear Input Simplifies Initialization or Pattern Length
- Embedded Clock Driver Provides Symmetrical Performance Across Long Registers
- Use Registers in Parallel for 8-Bit, 16-Bit, 32-Bit Word Widths

logic symbol†



Equivalent to 74173

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S173LJ gate-array software macro implements a 4-bit D-type register. The 4-bit length means that testability is simplified when constructing large registers. Gated enable inputs are provided on these macros for controlling the entry of data into the register. When both data enable inputs, GZ, are low, data at the D inputs are loaded on the next positive transition of the clock input. Buffer output enable inputs, MZ and NZ, are also provided. When both are low, the normal logic states (high or low levels) of the four outputs are impressed on the data bus. The outputs are disabled by a high logic level at either output control input. The outputs then present a high impedance to the internal bus. When the outputs are disabled, sequential operation of the flip-flops is not affected. The S173LJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
IV120LJ	1	2	2	0.78
IV211LJ	2	4	8	1.52
NA210LJ	1	12	12	3.24
NO210LJ	1	1	1	0.18
OR210LJ	2	1	2	0.48
R2406LJ	28	1	28	8.17
TOTALS		21	53	14.37

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

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S173LJ
4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

D3015, OCTOBER 1987

When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S173LJ D1,D2,D3,D4,CLK,CLR,G1Z,G2Z,MZ,NZ,Q1,Q2,Q3,Q4;

FUNCTION TABLE
(EACH FLIP-FLOP) (see Note 1)

INPUTS					OUTPUT
CLR	CLK	G1Z	G2Z	D	Q
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

Q_0 = level of Q before the indicated steady-state input conditions were established.

NOTE 1: When either MZ or NZ (or both) is (are) high, the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

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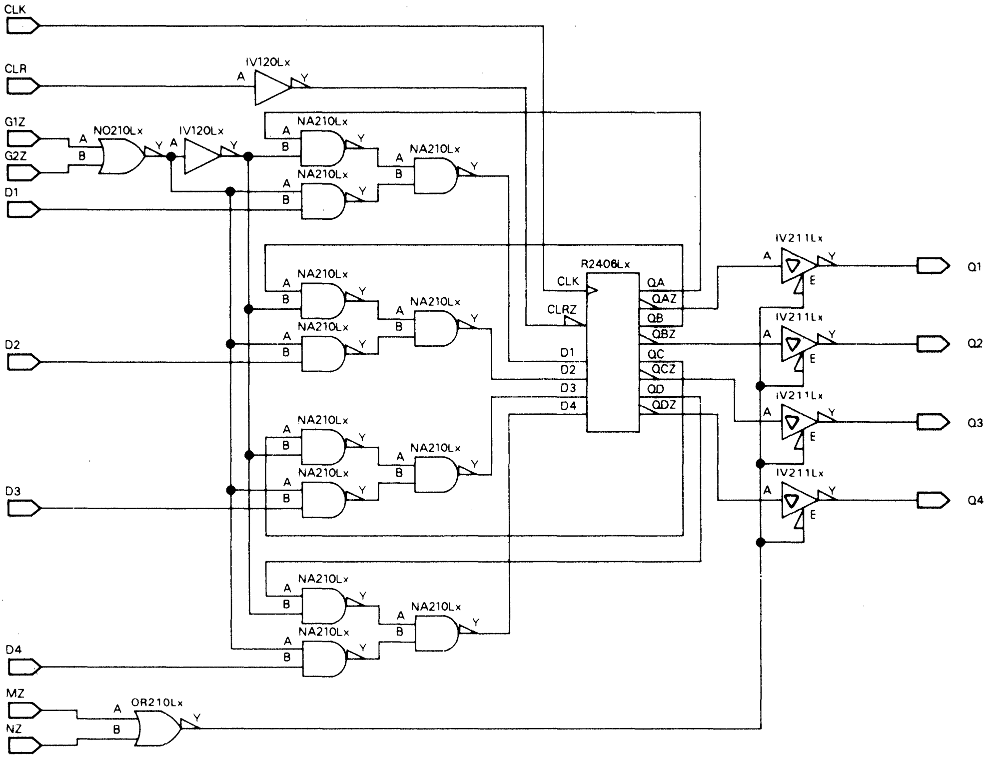
S173LJ
4-BIT D-TYPE REGISTER
WITH 3-STATE OUTPUTS

D3015, OCTOBER 1987

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

S173LJ 4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

D3015, OCTOBER 1987

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	CLK,CLR		0.15		pF
		All others		0.07		
C_o	Output capacitance			0.08		pF
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	14.37		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Notes 2 and 3), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	CLK	Q		2.3	4.5	ns
t_{PHL}				2.5	5.1	
t_{PHL}	CLR	Q		2.1	4.3	ns
t_{PZH}	GZ	Q		1.6	2.9	ns
t_{PHZ}				2.5	4.4	
t_{PZL}	GZ	Q		1.7	3	ns
t_{PLZ}				2.1	3.7	
Δt_{PZH}	Any	Q	0.38	0.96	1.9	ns/pF
Δt_{PZL}			0.32	0.64	1.26	

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 2. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

3. Enable and delta-enable times are measured using the conditions specified for the IV211LJ.

S175LJ QUADRUPLE D-TYPE FLIP-FLOP WITH COMPLEMENTARY OUTPUTS

D3015, OCTOBER 1987

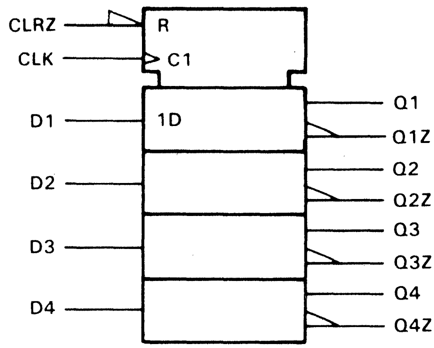
SOFTWARE MACRO

- **Four-Bit Register with Complementary Outputs**
- **Direct Clear Input Simplifies Initialization or Pattern Length**
- **Embedded Clock Driver Provides Clock Buffering**
- **Use Latches in Parallel for 8-Bit, 16-Bit, 32-Bit Word Widths**

description

The S175LJ gate-array software macro implements a 4-bit register. The 4-bit length simplifies construction of large registers. This software macro reduces the input loading for implementation of larger registers, as standard library cells are used to buffer the clear input, and the R2406LJ register clock input is internally buffered. The S175LJ is implemented with the macro functions indicated.

logic symbol†



Equivalent to 74175

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
IV110LJ	1	1	1	0.21
IV140LJ	2	1	2	0.8
R2406LJ	28	1	28	8.17
TOTALS		3	31	9.18

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S175LJ D1,D2,D3,D4,CLK,CLRZ,Q1,Q1Z,Q2,Q2Z,Q3,Q3Z,Q4,Q4Z;

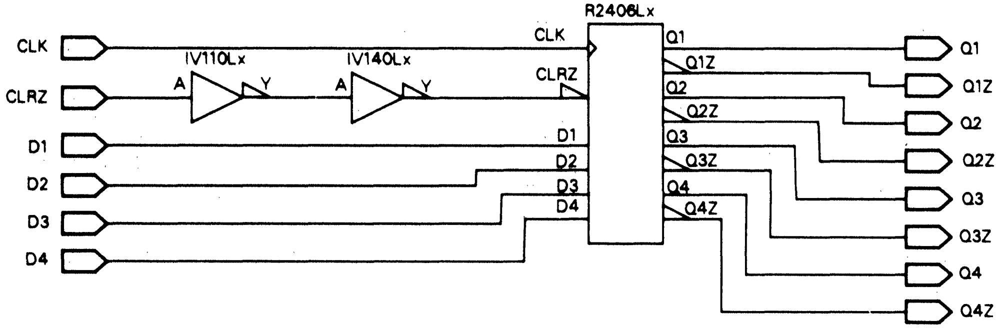
S175LJ
QUADRUPLE D-TYPE FLIP-FLOP WITH COMPLEMENTARY OUTPUTS

D3015, OCTOBER 1987

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLRZ	CLK	D	Q	QZ
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TCG100 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	CLRZ		0.07		pF
		CLK		0.15		
		All others		0.08		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	9.18		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	CLK	Q		1.4	2.7	ns
t_{PHL}				1.7	3.5	
t_{PLH}	CLK	QZ		1.8	3.9	ns
t_{PHL}				1.7	3.4	
t_{PLH}	CLRZ	QZ		2	3.8	ns
t_{PHL}		Q		1.7	3.1	
Δt_{PLH}	Any	Q,QZ	0.37	0.9	1.73	ns/pF
Δt_{PHL}			0.25	0.52	0.96	

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

S273LJ OCTAL D-TYPE FLIP-FLOP

D3015, OCTOBER 1987

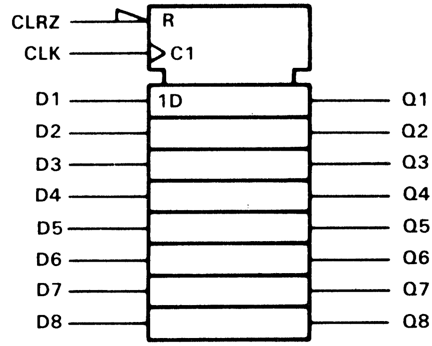
SOFTWARE MACRO CELL

- 8-Bit Software Register
- Direct Clear Input Simplifies Initialization or Pattern Length
- Buffered Clear Simplifies System Design
- Use Registers in Parallel for Wide Words

description

The S273LJ gate-array software macro implements an 8-bit register. The 8-bit length simplifies construction of large registers. The software macro reduces the input loading for implementation of larger registers, as standard library cells are used to buffer the clear input. The S273LJ is implemented with the macro functions indicated.

logic symbol†



Equivalent to 74273

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
IV110LJ	1	1	1	0.21
IV140LJ	2	1	2	0.8
R2405LJ	26	2	52	7.02
TOTALS		4	55	8.03

‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

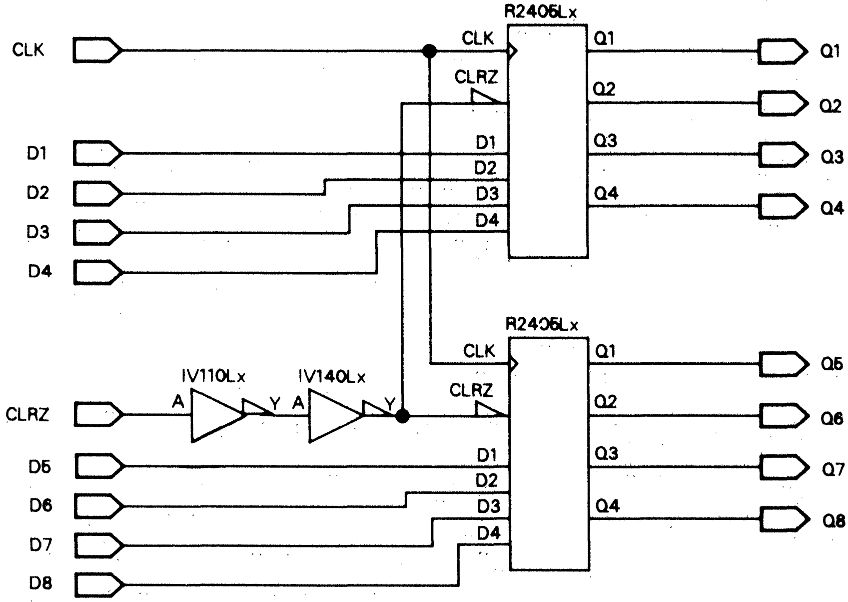
Label: S273LJ D1,D2,D3,D4,D5,D6,D7,D8,CLK,CLRZ,Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8;

D3015, OCTOBER 1987

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLRZ	CLK	Dn	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	CLRZ		0.07		pF
		CLK		0.32		
		All others		0.08		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	8.03		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	CLK	Q		1.4	2.8	ns
t_{PHL}				1.6	3.3	
t_{PHL}	CLRZ	Q		2	3.4	ns
Δt_{PLH}	Any	Q	0.36	0.89	1.72	ns/pF
Δt_{PHL}			0.26	0.51	0.95	

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

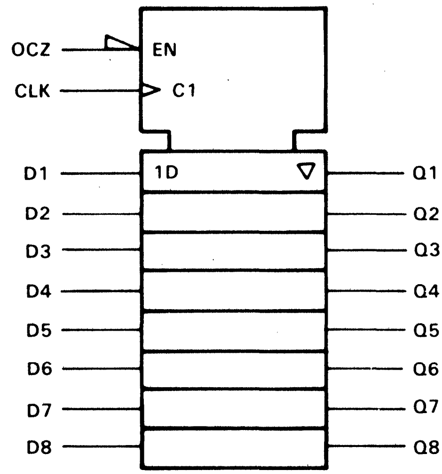
S374LJ
8-BIT D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

D3015, OCTOBER 1987

SOFTWARE MACRO

- **3-State Outputs Interface with Internal Data Buses Directly**
- **Buffered Output Control Simplifies System Design**
- **Embedded Clock Drivers Provide Symmetrical Performance Across Long Registers**
- **Use Latches in Parallel for 16-Bit, 32-Bit, 64-Bit Word Widths**

logic symbol†



Equivalent to 74374

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S374LJ gate-array software macro implements an 8-bit D-type register. The macro is designed specifically for interfacing internal bus lines. The 8-bit length simplifies construction of large registers. The Output-Control input, OCZ, can be used to place the eight outputs in either a normal logic state (high- or low-logic levels) or a high-impedance state. When the outputs are enabled with OCZ low, the logic level at each of the eight outputs is impressed on the data bus. The outputs are disabled by a high logic level at OCZ. The outputs then present a high impedance to the internal bus. When the outputs are disabled, sequential operation of the flip-flops is not affected. The S374LJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
BU130LJ	2	1	2	0.92
IV211LJ	2	8	16	3.04
R2406LJ	28	2	56	16.34
TO010LJ	2	1	2	—
TOTALS		12	76	20.3

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

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S374LJ
8-BIT D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

D3015, OCTOBER 1987—REVISED FEBRUARY 1989

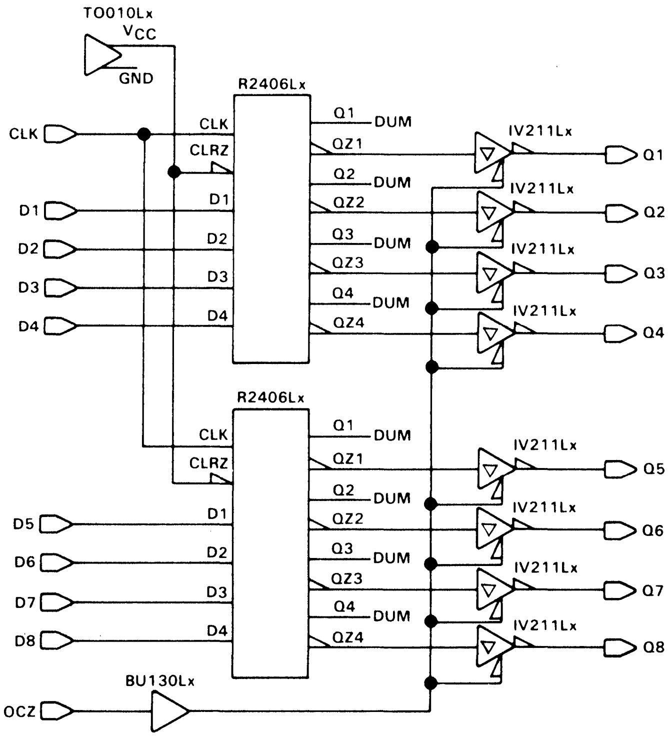
When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S374LJ D1,D2,D3,D4,D5,D6,D7,D8,CLK,OCZ,Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8;

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
OCZ	CLK	Dn	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram



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absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	OCZ		0.07		pF
		CLK		0.30		
		All others		0.08		
C_o	Output capacitance			0.08		pF
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	20.3		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Notes 1 and 2), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	CLK	Q		2.3	4.5	ns
t_{PHL}				2.5	5.1	
t_{PZH}	OCZ	Q		1.3	2.4	ns
t_{PHZ}				2.3	4	
t_{PZL}	OCZ	Q		1.4	2.6	ns
t_{PLZ}				1.8	3.2	
Δt_{PLH}	Any	Q	0.38	0.96	1.9	ns/pF
Δt_{PHL}			0.32	0.64	1.26	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.
2. Enable and delta-enable times are measured using the conditions specified for the IV211LJ.

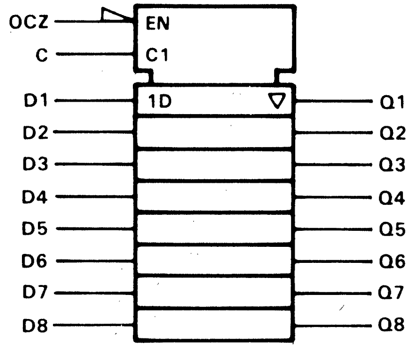
S373LJ 8-BIT D-TYPE LATCH WITH 3-STATE OUTPUTS

D3015, OCTOBER 1987

SOFTWARE MACRO

- **3-State Outputs Interface with Internal Data Buses Directly**
- **Buffered Output Enable Simplifies System Design**
- **Full Parallel Access for Loading**
- **Use Latches in Parallel for 16-Bit, 32-Bit, 64-Bit Word Widths**

logic symbol†



Equivalent to 74373

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S373LJ gate-array software macro implements an 8-bit D-type latch. The macro is designed specifically for interfacing with internal bus lines. The 8-bit length means that testability is simplified when constructing large latches. The eight latches of the S373LJ are transparent D-type latches. While the enable (C) is high, the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs. The output-control input (OCZ) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. When the outputs are enabled with OCZ low, the logic level at each of the eight outputs is impressed on the data bus. The outputs are disabled by a high logic level at OCZ. The outputs then present a high impedance to the internal bus. The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off. The S373LJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
AO221LJ	2	8	16	2.24
BU150LJ	3	1	3	1.5
IV110LJ	1	8	8	1.68
IV140LJ	2	2	4	1.6
IV211LJ	2	8	16	3.04
TOTALS		27	47	10.06

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S373LJ D1,D2,D3,D4,D5,D6,D7,D8,C,OCZ,Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8;

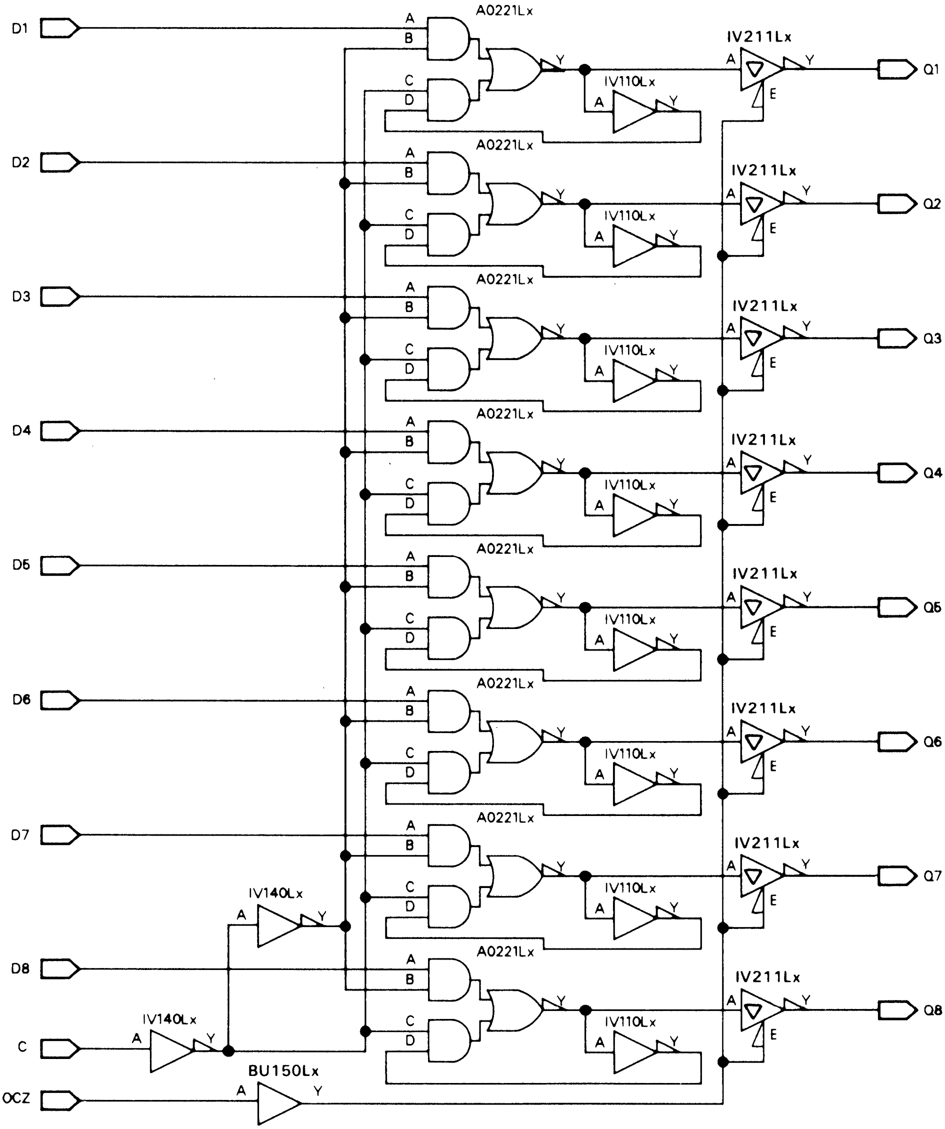
FUNCTION TABLE
(EACH LATCH)

INPUTS			OUTPUT
OCZ	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

S373LJ
8-BIT D-TYPE LATCH WITH 3-STATE OUTPUTS

D3015, OCTOBER 1987

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	C		0.31		pF
		All others		0.07		
C_o	Output capacitance			0.08		pF
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f$ = 1 ns	10.06		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Notes 1 and 2), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	C	Q		1.8	3.4	ns
t_{PHL}				2.3	4.4	
t_{PLH}	D	Q		1.1	2.1	ns
t_{PHL}				1.6	3.1	
t_{PZH}	OCZ	Q		1.4	2.6	ns
t_{PZL}				1.5	2.8	
t_{PHZ}	OCZ	Q		3.2	4.2	ns
t_{PHL}				2.4	3.4	
Δt_{PLH}	Any	Q	0.38	0.96	1.9	ns/pF
Δt_{PHL}			0.32	0.64	1.26	
Δt_{PZH}	D	Q	0.18	0.86	1.76	ns/pF
Δt_{PZL}			0.24	0.62	1.26	

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Acutal performance can be evaluated at post-layout simulation.

2. Enable and delta-enable times are measured using the conditions specified for the IV211LJ.

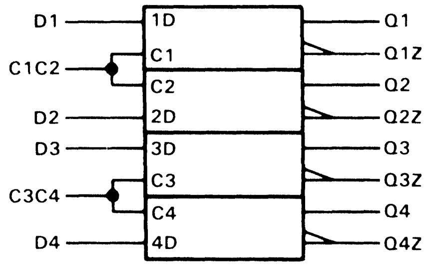
S375LJ
4-BIT BISTABLE LATCH

D3015, OCTOBER 1987

SOFTWARE MACRO

- **Four-Bit Software Latches with Complementary Outputs**
- **Eliminates Skew and Mismatch of Long Versus Short Data Paths**
- **Use Latches in Parallel for 8-Bit, 16-Bit, 32-Bit Word Widths**

logic symbol†



Equivalent to 74375

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S375LJ gate-array software macro implements a 4-bit bistable latch. The 4-bit length simplifies construction of large registers. Information present at a Dn input is transferred to the Qn output when the CnCm input is high, and the Qn output will follow the data input as long as CnCm remains high. When CnCm goes low, the data (that was present at the Dn input at the time the transition occurred) is retained at the Qn output until CnCm is taken high. The S375LJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
AO221LJ	2	4	8	1.12
IV110LJ	1	4	4	0.84
IV120LJ	1	4	4	1.56
TOTALS		12	16	3.52

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

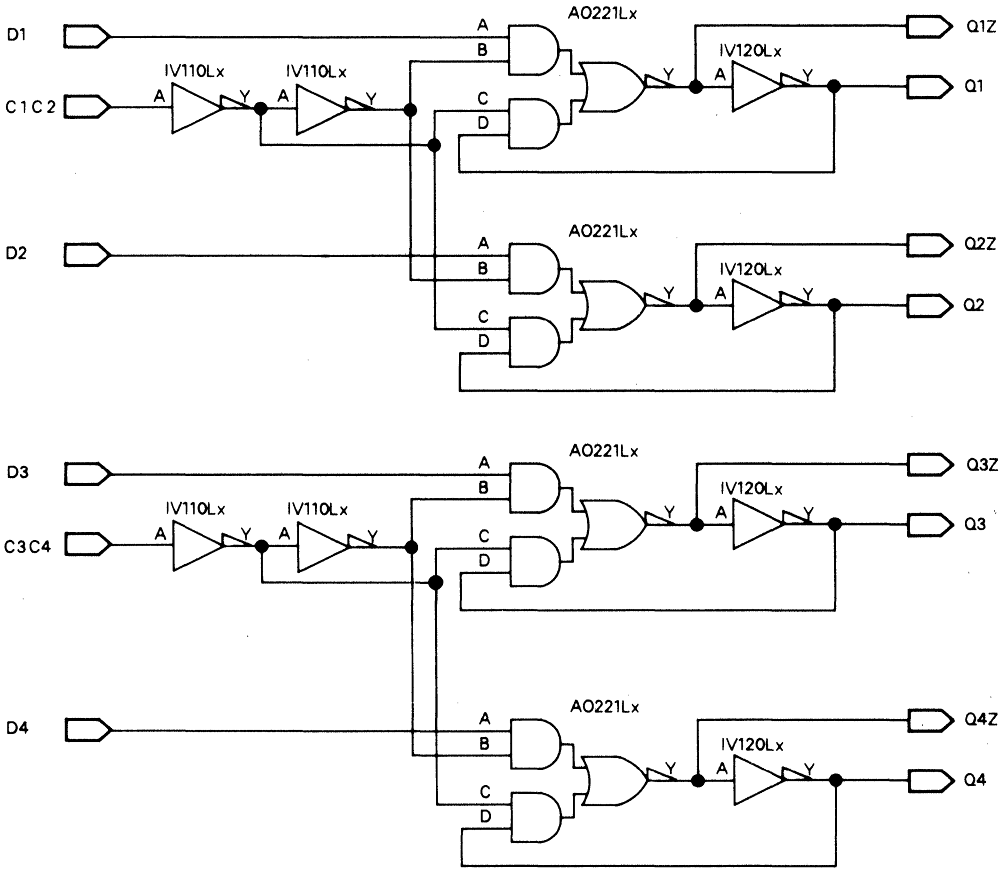
Label: S375LJ D1,D2,D3,D4,C1C2,C3C4,Q1,Q1Z,Q2,Q2Z,Q3,Q3Z,Q4,Q4Z;

D3015, OCTOBER 1987

FUNCTION TABLE
(EACH LATCH)

INPUTS		OUTPUTS	
Dn	CnCm	Qn	QnZ
L	H	L	H
H	H	H	L
X	L	Qn_0	$\overline{Qn_0}$

logic diagram



D3015, OCTOBER 1987

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation, produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†		TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance‡	$t_r = t_f = 1$ ns	3.52		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	D	Q		1	1.9	ns
t_{PHL}				1.4	2.8	
t_{PLH}	D	QZ		1.1	2.3	ns
t_{PHL}				0.7	1.3	
t_{PLH}	CnCm	Q		2	4.2	ns
t_{PHL}				1.9	3.2	
t_{PLH}	CnCm	QZ		1.6	2.7	ns
t_{PHL}				1.9	3.2	
Δt_{PLH}	Any	Q	0.22	0.44	0.84	ns/pF
Δt_{PHL}			0.22	0.32	0.44	
Δt_{PLH}	Any	QZ	0.58	1.68	3.42	ns/pF
Δt_{PHL}			0.34	0.75	1.5	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

10

Clock Drivers/Generator/Oscillators

CLOCK GENERATOR AND OSCILLATORS FUNCTIONAL INDEX

D3015, OCTOBER 1988

CLOCK DISTRIBUTORS

DESCRIPTION	MACRO NAME	OUTPUT DRIVE	COMMENTS	CELLS USED	PAGE
25-pF Clock Drivers	CKD03LJ	X	For use on TGC103	40	10-3
	CKD05LJ	X	For use on TGC105	48	10-4
	CKD08LJ	X	For use on TGC108	64	10-5
35-pF Clock Drivers	CKD12LJ	X	For use on TGC112	74	10-6
	CKD15LJ	X	For use on TGC115	82	10-7
	CKD18LJ	X	For use on TGC118	98	10-8

CLOCK GENERATOR

DESCRIPTION	MACRO NAME	OUTPUT DRIVE	COMMENTS	CELLS USED	PAGE
Two-Phase Clock Generator	CK120LJ	1X	Non-overlapping for use with scan latches	10	10-9

OSCILLATORS

DESCRIPTION	MACRO NAME	COMMENTS	CELLS USED†	PAGE
Two-Pin Crystal Oscillators	OSI11LJ	55 to 75 MHz	0	10-15
	OSI12LJ	35 to 55 MHz	0	10-17
	OSI13LJ	20 to 35 MHz	0	10-19
	OSI14LJ	1 to to 20 MHz	0	10-21

† Two bond pads

INTERNAL CLOCK DISTRIBUTION MACROS

description

The six CKDnnLJs are clock-driver macros designed to drive large numbers of synchronous clock inputs with a minimum amount of skew. Utilizing pre-routed, high-current-density metallization, a unique layout is patterned for each of the six arrays offered in the TGC100 Series.

The CKD03LJ through CKD08LJ can drive up to 25 pF of load capacitance each and the CKD12LJ through CKD18LJ can drive up to 35 pF of load capacitance each in addition to the pre-routed metallization. Assuming a C_{in} of 0.07 pF, up to 350 D-type flip-flop clock inputs can be driven by the CKD03LJ, CKD05LJ, and CKD08LJ clock distribution macros, and up to 500 clock inputs can be driven by the CKD12LJ, CKD15LJ, and CKD18LJ macros. At full loading, clock speeds up to 50 MHz can be achieved.

The CKDxxLJ macro can be driven by an input buffer or a 2-pin oscillator for use as a master clock for the entire chip, or the CKDnnLJ may be driven by a 2X-output internal macro. Up to six CKDnnLJ macros can be used on each gate-array design for implementing functions such as multiple and/or two-phase, nonoverlapping clocks.

When clock distribution macros are used to drive over 150 simultaneously switching flip-flops, and especially at frequencies above 20 MHz, secondary V_{CC} and GND pins are necessary to handle the large currents. When driving 150 or more clock inputs, it is recommended that a secondary GND pin be added. When driving 300 or more clock inputs, it is recommended that 2 secondary GND pins and 1 secondary V_{CC} pin be added. When the CKD12LJ, CKD15LJ, and CKD18LJ are loaded with 450 clock inputs, a third secondary ground pin is recommended. The added secondary power pins reduce the effects of di/dt and IR drop on the IC.

CKD03LJ
NONINVERTING CLOCK DISTRIBUTOR

D3015, OCTOBER 1988

INTERNAL CLOCK DISTRIBUTION MACROS

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The CKD03LJ clock distributor provides high-fanout clock drivers with attendant current-handling metal interconnects that can be called as a macro into a design using the TGC103 gate array. When the clock distributor is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: CKD03LJ A,CLK;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2		V
C_i	Input capacitance		0.32		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	18.1		pF

‡ For supply current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	1.21	1.94	3.05	ns
t_{PHL}			1.19	1.95	3.12	
Δt_{PLH}	A	Y	13	23	37	ps/pF
Δt_{PHL}			14	25	42	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

D3015, OCTOBER 1988

INTERNAL CLOCK DISTRIBUTION MACROS

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The CKD05LJ clock distributor provides high-fanout clock drivers with attendant current-handling metal interconnects that can be called as a macro into a design using the TGC105 gate array. When the clock distributor is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: CKD05LJ A,CLK;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.3		V
C_i	Input capacitance		0.32		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	24.1		pF

‡ For supply current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	1.32	2.18	3.44	ns
t_{PHL}			1.33	2.21	3.55	
Δt_{PLH}	A	Y	11	18	30	ps/pF
Δt_{PHL}			12	21	35	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

CKD08LJ NONINVERTING CLOCK DISTRIBUTOR

D3015, OCTOBER 1988

INTERNAL CLOCK DISTRIBUTION MACROS

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The CKD08LJ clock distributor provides high-fanout clock drivers with attendant current-handling metal interconnects that can be called as a macro into a design using the TGC108 gate array. When the clock distributor is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: CKD08LJ A,CLK;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.3		V
C_i	Input capacitance		0.32		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	31.6		pF

‡ For supply current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	1.41	2.3	3.64	ns
t_{PHL}			1.35	2.29	3.7	
Δt_{PLH}	A	Y	8	14	23	ps/pF
Δt_{PHL}			9	16	26	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS

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CKD12LJ
NONINVERTING CLOCK DISTRIBUTOR

D3015, OCTOBER 1988

INTERNAL CLOCK DISTRIBUTION MACROS

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The CKD12LJ clock distributor provides high-fanout clock drivers with attendant current-handling metal interconnects that can be called as a macro into a design using the TGC112 gate array. When the clock distributor is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: CKD12LJ A,CLK;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.3		V
C_i	Input capacitance		0.32		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	36.6		pF

‡ For supply current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	1.45	2.36	3.75	ns
t_{PHL}			1.45	2.41	3.87	
Δt_{PLH}	A	Y	7	13	21	ps/pF
Δt_{PHL}			8	14	24	

§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

D3015, OCTOBER 1988

INTERNAL CLOCK DISTRIBUTION MACROS

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The CKD15LJ clock distributor provides high-fanout clock drivers with attendant current-handling metal interconnects that can be called as a macro into a design using the TGC115 gate array. When the clock distributor is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: CKD15LJ A,CLK;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.3		V
C_i	Input capacitance		0.32		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	40.8		pF

‡ For supply current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	1.48	2.45	3.88	ns
t_{PHL}			1.48	2.5	4.03	
Δt_{PLH}	A	Y	7	11	19	ps/pF
Δt_{PHL}			7	13	21	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS

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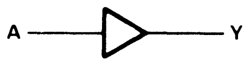
D3015, OCTOBER 1988

INTERNAL CLOCK DISTRIBUTION MACROS

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The CKD18LJ clock distributor provides high-fanout clock drivers with attendant current-handling metal interconnects that can be called as a macro into a design using the TGC118 gate array. When the clock distributor is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: CKD18LJ A,CLK;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.3		V
C_i	Input capacitance		0.32		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	40.8		pF

‡ For supply current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	1.48	2.45	3.88	ns
t_{PHL}			1.48	2.5	4.03	
Δt_{PLH}	A	Y	7	11	19	ps/pF
Δt_{PHL}			7	13	21	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

CK120LJ
CLOCK GENERATOR
WITH NONOVERLAPPING TWO-PHASE OUTPUTS

D3015, OCTOBER 1988

INTERNAL CLOCK DISTRIBUTION MACRO

FUNCTION TABLE

INPUT	OUTPUTS	
A	CLK	CLKZ
L	L	H
H	H	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The CK120LJ clock generator provides two-phase nonoverlapping clock inputs from a single clock input. The generator can be used with the dual clocks needed to strobe the TDXXXLJ scan latches. When the clock generator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: CK120LJ A,CLK,CLKZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2		V
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	4.8		pF

‡ For supply current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	CLK	1.94	5.64	11.65	ns
t_{PHL}			0.71	1.83	3.82	
t_{PLH}	A	CLKZ	2.09	6.05	12.69	ns
t_{PHL}			0.5	1.23	2.39	
Δt_{PLH}	A	CLK	0.19	0.55	1.12	ps/pF
Δt_{PHL}			0.15	0.33	0.62	
Δt_{PLH}	A	CLKZ	0.19	0.55	1.14	ns/pF
Δt_{PHL}			0.14	0.31	0.61	

§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

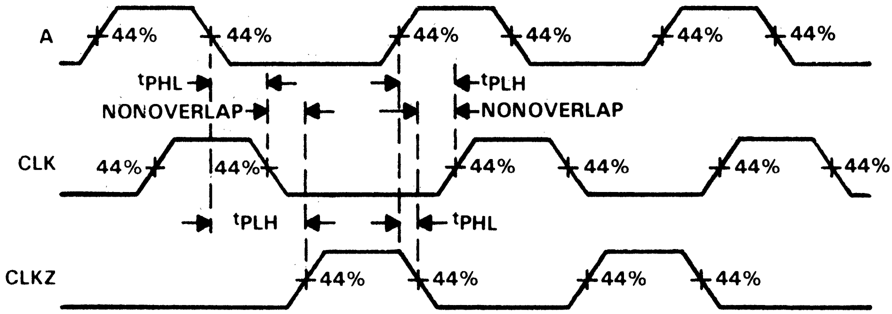


FIGURE 1. A TO CLK OR CLKZ TIMING DIAGRAM

D3015, OCTOBER 1988

OSCILLATOR INPUT MACRO CELLS

- **Crystal-Controlled Oscillator for Generating On-Chip Clock Signals**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Dependable Texas Instruments Quality and Reliability**

OSCILLATOR FUNCTIONAL INDEX

MACRO NAME	FREQUENCY RANGE (MHz)	CRYSTAL TYPE	PAGE
OSI11LJ	55 to 75	3rd Overtone	10-15
OSI12LJ	35 to 55	3rd Overtone	10-17
OSI13LJ	20 to 35	3rd Overtone	10-19
OSI14LJ	1 to 20	Fundamental	10-21

description

These four input macros are two-pin crystal oscillators designed for use with an external series- or parallel-resonant crystal and feedback resistor. On-chip frequencies from 1 to 75 MHz can be generated.

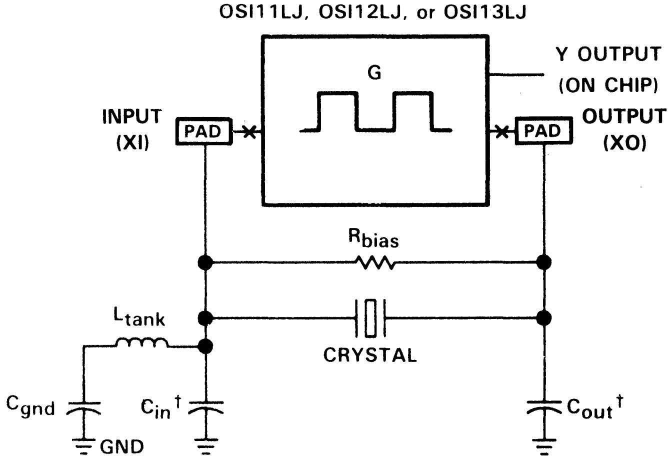
DESIGN CONSIDERATIONS

series- or parallel-mode crystal operation

A series- or parallel-mode crystal can be used, but a parallel-mode crystal should be used if frequency accuracy is important. Series- and parallel-mode crystals are identical except that the frequency of a series-mode crystal is set at the series-resonant, low-impedance frequency of operation. Parallel-mode crystals are tuned with a load capacitor in series that causes them to be tuned for operation between the series resonant frequency and the antiresonant, high- impedance frequency. The value of the load capacitor is specified to be typically 12 pF to 32 pF. This load capacitance value should be equal to the equivalent capacitance between the pins of the oscillator to which the crystal is connected. If accurate frequency of operation is desired, either the input or output capacitance can be set to produce the correct frequency with a given crystal or the crystal manufacturer can make a crystal that will operate at the correct frequency with the existing capacitance.

third-overtone frequency operation

The capacitance loading the input and output should be larger at lower frequencies and smaller at higher frequencies to provide gain sufficient for third-overtone oscillation yet insufficient for oscillation at unwanted frequencies. Third-overtone-frequency operation is achieved by adding an external LC circuit consisting of an inductor to ground through a capacitor. (See Figure 1.) The output pin capacitance and the inductor-capacitor combination form a tank circuit. The tank values are chosen so that its resonant frequency is at the second overtone frequency of the third-overtone crystal. This produces a phase shift that prevents oscillation at the fundamental frequency. Smaller values of output capacitance are used at higher frequencies to provide sufficient gain for oscillation.



† C_{in} and C_{out} are the total capacitance of the circuit board and components, excluding the integrated circuit.

FIGURE 1. OVERTONE FREQUENCY OPERATION OF OSI11LJ, OSI12LJ, OR OSI13LJ

Insufficient capacitance may produce oscillation at the fifth overtone. It is important to operate with as little capacitance as practical by loading the crystal at third-overtone frequencies to keep the crystal drive level low. Operation at 15 pF or less equivalent load capacitance allows the crystal to behave more as an inductor. High drive level can cause excessive frequency drift and possible crystal failure.

Good design practices include:

- Placing the oscillator pins in the least "noisy" area of the package pins.
- Placing the oscillator on two adjacent pin locations.
- Placing the oscillator between a V_{CC} and ground pin utilizing primary or secondary power pin locations.
- Placing large outputs, especially those operating at data rates near the oscillator frequency, away from the oscillator pins.

trial values recommended for third-overtone operation

OSI11LJ (See Figure 1)

3rd-overtone frequency	L_{tank}	C_{gnd}	C_{in}†	C_{out}†	R_{bias}
75 MHz	0.47 µH	1000 pF	10 pF	10 pF	90 kΩ
64 MHz	0.68 µH	1000 pF	10 pF	10 pF	90 kΩ
55 MHz	1 µH	1000 pF	10 pF	10 pF	90 kΩ

OSI2LJ (See Figure 1)

3rd-overtone frequency	L_{tank}	C_{gnd}	C_{in}†	C_{out}†	R_{bias}
55 MHz	1 µH	1000 pF	10 pF	10 pF	90 kΩ
48 MHz	1.5 µH	1000 pF	10 pF	10 pF	90 kΩ
35 MHz	2.2 µH	1000 pF	10 pF	10 pF	90 kΩ

OSI3LJ (See Figure 1)

3rd-overtone frequency	L_{tank}	C_{gnd}	C_{in}†	C_{out}†	R_{bias}
35 MHz	2.2 µH	1000 pF	10 pF	10 pF	90 kΩ
28 MHz	3.3 µH	1000 pF	10 pF	10 pF	90 kΩ
20 MHz	N/A	N/A	27 pF	27 pF	90 kΩ

† C_{in} and C_{out} are the total capacitance of the circuit board and components, excluding the integrated circuit.

D3015, OCTOBER 1988

trial values recommended for fundamental operation

OSI14LJ (See Figure 2)

FUNDAMENTAL FREQUENCY	R_{EXT} (C_{in}† = C_{out}† = 30 pF)	R_{ext} C_{in}† = C_{out}† = 64 pF)
20 MHz	0	0
16 MHz	220 Ω	0
12 MHz	470 Ω	220 Ω
8 MHz	1 kΩ	470 Ω
4 MHz	3.3 kΩ	1.5 kΩ
3 MHz	6.8 kΩ	3.3 kΩ
2 MHz	10 kΩ	4.7 kΩ
1 MHz	33 kΩ	15 kΩ

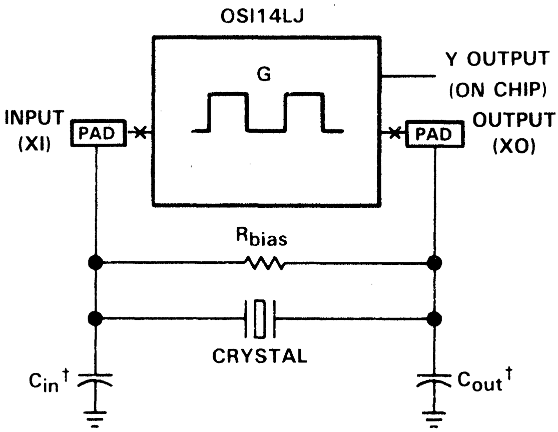


FIGURE 2. FUNDAMENTAL FREQUENCY OPERATION OF OSI14LJ

† C_{in} and C_{out} are the total capacitance of the circuit board and components, excluding the integrated circuit. Typical values range from 10 pF to 64 pF. For operation at lower frequencies, increase the size of C_{out} and/or add a series resistor between XO and C_{out}.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

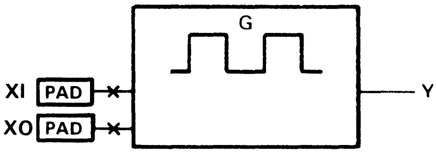
OSI11LJ
55- TO 75-MHz CRYSTAL-CONTROLLED OSCILLATOR WITH 8X DRIVE

D3015, OCTOBER 1988

OSCILLATOR INPUT MACRO

- **Crystal-Controlled Oscillator for Generating On-Chip Clock Signals from 55 to 75 MHz**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The OSI11LJ is a two-pin crystal oscillator designed for use with an external series- or parallel-resonant crystal and feedback resistor. As a third-harmonic, crystal-controlled oscillator, on-chip frequencies from 55 to 75 MHz can be generated. When the oscillator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OSI11LJ XI,XO,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, $V_{CC} = 5$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.5		V
I_{CC}	Supply current		$f_{osc} = 64$ MHz	12		mA
C_i	Input capacitance	XI		3.79		pF
C_o	Output capacitance	XO		6.92		pF
C_{pd}	Equivalent power dissipation capacitance		$f_{osc} = 1$ MHz, $t_r = t_f = 1$ ns	10.9		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	XI	Y		1.42	2.52	4.2	ns
t_{PHL}				1.14	2.33	4.04	
Δt_{PLH}	XI	Y		40	160	350	ps/pF
Δt_{PHL}				60	160	340	

TEXAS INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

DESIGN CONSIDERATIONS

series- or parallel-mode crystal operation

A series- or parallel-mode crystal can be used. See oscillators general information for more detailed information on the selection of crystals.

third-overtone frequency operation

For detailed design considerations, including a schematic of the external component hookup, see the oscillators general information.

trial values recommended for third-overtone operation

OSI11LJ

3rd-overtone frequency	L_{tank}	C_{gnd}	C_{in}†	C_{out}†	R_{bias}
55 MHz	1 μH	1000 pF	10 pF	10 pF	90 kΩ
64 MHz	0.68 μH	1000 pF	10 pF	10 pF	90 kΩ
75 MHz	0.47 μH	1000 pF	10 pF	10 pF	90 kΩ

† C_{in} and C_{out} are the total capacitance of the circuit board and components, excluding the integrated circuit.

Good design practices include:
- Placing the oscillator pins in the least "noisy" area of the package pins.
- Placing the oscillator on two adjacent pin locations.
- Placing the oscillator between a V_{CC} and ground pin utilizing primary or secondary power pin locations.
- Placing large outputs, especially those operating at data rates near the oscillator frequency, away from the oscillator pins.

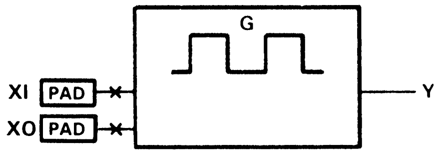
OSI12LJ
35- TO 55-MHz CRYSTAL-CONTROLLED OSCILLATOR WITH 4X DRIVE

D3015, OCTOBER 1988

OSCILLATOR INPUT MACRO

- Crystal-Controlled Oscillator for Generating On-Chip Clock Signals from 35 to 55 MHz
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Dependable Texas Instruments Quality and Reliability

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The OSI12LJ is a two-pin crystal oscillator designed for use with an external series- or parallel-resonant crystal and feedback resistor. As a third-harmonic, crystal-controlled oscillator, on-chip frequencies from 35 to 55 MHz can be generated. When the oscillator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OSI12LJ XI,XO,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.5		V
I_{CC}	Supply current		f_{osc} = 48 MHz	6.77		mA
C_i	Input capacitance	XI		3.79		pF
C_o	Output capacitance	XO		6.89		pF
C_{pd}	Equivalent power dissipation capacitance		f_{osc} = 1 MHz, $t_r = t_f$ = 1 ns	10.3		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	XI	Y		1.3	2.37	3.99	ns
t_{PHL}				1.05	2.19	3.87	
Δt_{PLH}	XI	Y		60	170	370	ps/pF
Δt_{PHL}				70	180	350	

DESIGN CONSIDERATIONS

series- or parallel-mode crystal operation

A series- or parallel-mode crystal can be used. See oscillators general information for more detailed information on the selection of crystals.

third-overtone frequency operation

For detailed design considerations, including a schematic of the external component hookup, see the oscillators general information.

trial values recommended for third-overtone operation

OSI12LJ

3rd-overtone frequency	L_{tank}	C_{gnd}	C_{in}†	C_{out}†	R_{bias}
35 MHz	2.2 μH	1000 pF	10 pF	10 pF	90 kΩ
48 MHz	1.5 μH	1000 pF	10 pF	10 pF	90 kΩ
55 MHz	1 μH	1000 pF	10 pF	10 pF	90 kΩ

† C_{in} and C_{out} are the total capacitance of the circuit board and components, excluding the integrated circuit.

Good design practices include:

- Placing the oscillator pins in the least "noisy" area of the package pins.
- Placing the oscillator on two adjacent pin locations.
- Placing the oscillator between a V_{CC} and ground pin utilizing primary or secondary power pin locations.
- Placing large outputs, especially those operating at data rates near the oscillator frequency, away from the oscillator pins.

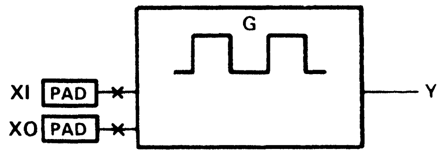
OSI13LJ
20- TO 35-MHz CRYSTAL-CONTROLLED OSCILLATOR WITH 2X DRIVE

D3015, OCTOBER 1988

OSCILLATOR INPUT MACRO

- Crystal-Controlled Oscillator for Generating On-Chip Clock Signals from 20 to 35 MHz
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Dependable Texas Instruments Quality and Reliability

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The OSI13LJ is a two-pin crystal oscillator designed for use with an external series- or parallel-resonant crystal and feedback resistor. As a third-harmonic, crystal-controlled oscillator, on-chip frequencies from 20 to 35 MHz can be generated. When the oscillator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OSI13LJ XI,XO,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.5		V
I_{CC}	Supply voltage		f_{osc} = 32 MHz	3.28		mA
C_i	Input capacitance	XI		3.79		pF
C_o	Output capacitance	XO		6.98		pF
C_{pd}	Equivalent power dissipation capacitance		f_{osc} = 1 MHz, $t_r = t_f$ = 1 ns	10.2		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	XI	Y		1.25	2.29	3.89	ns
t_{PHL}				1	2.13	3.78	
Δt_{PLH}	XI	Y		70	180	370	ps/pF
Δt_{PHL}				80	180	350	

DESIGN CONSIDERATIONS

series- or parallel-mode crystal operation

A series- or parallel-mode crystal can be used. See oscillators general information for more detailed information on the selection of crystals.

third-overtone frequency operation

For detailed design considerations, including a schematic of the external component hookup, see the oscillators general information.

trial values recommended for third-overtone operation

3rd-overtone frequency	L_{tank}	C_{gnd}	C_{in}†	C_{out}†	R_{bias}
20 MHz	N/A	N/A	27 pF	27 pF	90 kΩ
28 MHz	3.3 µH	1000 pF	10 pF	10 pF	90 kΩ
35 MHz	2.2 µH	1000 pF	10 pF	10 pF	90 kΩ

† C_{in} and C_{out} are the total capacitance of the circuit board and components, excluding the integrated circuit.

Good design practices include:

- Placing the oscillator pins in the least "noisy" area of the package pins.
- Placing the oscillator on two adjacent pin locations.
- Placing the oscillator between a V_{CC} and ground pin utilizing primary or secondary power pin locations.
- Placing large outputs, especially those operating at data rates near the oscillator frequency, away from the oscillator pins.

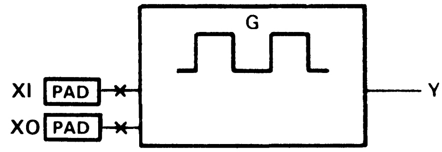
OSI14LJ 1- TO 20- MHz CRYSTAL-CONTROLLED OSCILLATOR

D3015, AUGUST 1988

OSCILLATOR INPUT MACRO

- Crystal-Controlled Oscillator for On-Chip Clock Signals of 1 to 20 MHz
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Dependable Texas Instruments Quality and Reliability

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The OSI14LJ is a two-pin crystal oscillator designed for use with an external series- or parallel-resonant fundamental crystal and feedback resistor. On-chip frequencies from 1 to 20 MHz can be generated. When the oscillator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OSI14LJ XI,XO,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.5		V
I_{CC}	Supply voltage		f_{osc} = 16 MHz	2.18		mA
C_i	Input capacitance	XI		3.79		pF
C_o	Output capacitance	XO		6.9		pF
C_{pd}	Equivalent power dissipation capacitance		f_{osc} = 1 MHz, $t_r = t_f$ = 1 ns	10.1		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	XI	Y	$C_L = 0$	1.24	2.27	3.88	ns
t_{PHL}				0.99	2.11	3.76	
Δt_{PLH}	XI	Y		0.07	0.19	0.37	ps/pF
Δt_{PHL}				0.08	0.19	0.35	

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

DESIGN CONSIDERATIONS

series- or parallel-mode crystal operation

A series- or parallel-mode crystal can be used. See oscillators general information for more detailed information on the selection of crystals.

fundamental frequency operation

For detailed design considerations, including a schematic of the external component hookup, see the oscillators general information.

trial values recommended for fundamental operation

Fundamental frequency	C_{in}†	C_{out}†	R_{bias}
16 MHz	32 pF	32 pF	90 kΩ

† C_{in} and C_{out} are the total capacitance of the circuit board and components, excluding the integrated circuit. Typical values range from 10 pF to 64 pF. For operation at lower frequencies, increase the size of C_{out} and/or add a series resistor between XO and C_{out}.

Good design practices include:

- Placing the oscillator pins in the least "noisy" area of the package pins.
- Placing the oscillator on two adjacent pin locations.
- Placing the oscillator between a V_{CC} and ground pin utilizing primary or secondary power pin locations.
- Placing large outputs, especially those operating at data rates near the oscillator frequency, away from the oscillator pins.

D3015, OCTOBER 1987—REVISED OCTOBER 1988

EXTERNAL INPUT MACRO

Input buffers incorporate circuit elements that are designed to actively bypass electrostatic discharges. Guard-ring structures are employed to provide current-management techniques that allow the buffer to recover from exposure to high currents of up to 400 mA, thereby negating most common sources that can produce a latch-up condition.

The following input functions are available in the TGC100 Series Data.

NAME	DESCRIPTION	PAGE
IPI00LJ	CMOS-COMPATIBLE INVERTING INPUT BUFFER	11-3
IPI01LJ	CMOS-COMPATIBLE INPUT BUFFER	11-4
IPI04LJ	TTL-COMPATIBLE INPUT BUFFER	11-5
IPI06LJ	CMOS-COMPATIBLE INVERTING SCHMITT-TRIGGER INPUT BUFFER	11-6
IPI09LJ	TTL-COMPATIBLE INPUT BUFFER WITH HYSTERESIS	11-8
IPL01LJ	CMOS-COMPATIBLE INPUT BUFFER WITH 70-μA PULL-UP SOURCE	11-9
IPL04LJ	TTL-COMPATIBLE INPUT BUFFER WITH 70-μA PULL-UP SOURCE	11-10
IPU01LJ	CMOS-COMPATIBLE INPUT BUFFER WITH 70-μA PULL-DOWN SOURCE	11-11
IPU04LJ	TTL-COMPATIBLE INPUT BUFFER WITH 70-μA PULL-DOWN SOURCE	11-12

IPI00LJ CMOS-COMPATIBLE INVERTING INPUT BUFFER

D3015, OCTOBER 1987 – REVISED FEBRUARY 1989

EXTERNAL INPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
L	H
H	L

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$

description

The IPI00LJ is an inverting input buffer that interfaces CMOS input voltage levels to CMOS internal-gate voltage levels. When the input buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IPI00LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡		TEST CONDITIONS	TYP§	MAX	UNIT
V_T	Input threshold voltage		2.5		V
I_I	Input current	$V_I = V_{CC}$ or 0		±1	μA
C_i	Intrinsic input capacitance¶		3.79		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	2.63		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	0.37	0.95	1.64	ns
t_{PHL}			0.64	1.13	1.87	
Δt_{PLH}	A	Y	0.11	0.18	0.38	ns/pF
Δt_{PHL}			0.08	0.16	0.25	

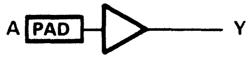
‡For Supply Current, I_{CC}, see the TGC100 Series Data.
§Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
¶Total input capacitance is dependent on the package and is equal to the sum of package capacitance and intrinsic input capacitance.

EXTERNAL INPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The IPI01LJ is an input buffer that interfaces CMOS input voltage levels to CMOS internal-gate voltage levels. When the input buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IPI01LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡		TEST CONDITIONS	TYP§	MAX	UNIT
V_T	Input threshold voltage		2.5		V
I_I	Input current	$V_I = V_{CC}$ or 0		±1	μA
C_i	Intrinsic input capacitance¶		3.79		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	1.8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	0.74	1.1	1.63	ns
t_{PHL}			0.29	0.77	1.36	
Δt_{PLH}	A	Y	0.09	0.2	0.39	ns/pF
Δt_{PHL}			0.11	0.17	0.27	

‡For Supply Current, I_{CC}, see the TGC100 Series Data.

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

¶Total input capacitance is dependent on the package and is equal to the sum of package capacitance and intrinsic input capacitance.

D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL INPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The IPI04LJ is an input buffer that interfaces TTL input voltage levels to CMOS internal-gate voltage levels. When the input buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IPI04LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡		TEST CONDITIONS	TYP§	MAX	UNIT
V_T	Input threshold voltage		1.3		V
I_I	Input current	$V_I = V_{CC}$ or 0		±1	μA
C_i	Intrinsic input capacitance¶		3.79		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	2.18		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	0.95	1.62	2.39	ns
t_{PHL}			0.14	1.22	2.82	
Δt_{PLH}	A	Y	0.1	0.2	0.39	ns/pF
Δt_{PHL}			0.08	0.26	0.62	

‡For Supply Current, I_{CC}, see the TGC100 Series Data.
§Typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Total input capacitance is dependent on the package and is equal to the sum of package capacitance and intrinsic input capacitance.

IPI06LJ CMOS-COMPATIBLE INVERTING SCHMITT-TRIGGER INPUT BUFFER

D3015, OCTOBER 1987 – REVISED FEBRUARY 1989

EXTERNAL INPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
L	H
H	L

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$

description

The IPI06LJ is an inverting input buffer that interfaces CMOS Schmitt-trigger input voltage levels to CMOS internal-gate voltage levels. When the input buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IPI06LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_{T+}	Positive-going threshold level			3.35	3.85	V
V_{T-}	Negative-going threshold level		0.9	1.65		V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)			1.7		V
I_I	Input current	$V_I = V_{CC}$ or 0			±1	μA
C_i	Intrinsic input capacitance¶			3.79		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		2.04		pF

‡For Supply Current, I_{CC}, see the TGC100 Series Data.
§Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
¶Total input capacitance is dependent on the package and is equal to the sum of package capacitance and intrinsic input capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	1.67	2.22	2.8	ns
t_{PHL}			1.73	2.31	3.05	
Δt_{PLH}	A	Y	0.49	0.81	1.48	ns/pF
Δt_{PHL}			0.55	0.92	1.7	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL-COMPATIBLE INPUT BUFFER WITH HYSTERESIS

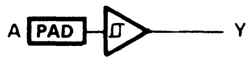
D3015, OCTOBER 1988

INPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The IPI09LJ is an input buffer with hysteresis that interfaces TTL input levels to CMOS internal voltage levels. When the input buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IPI09LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_{T+}	Positive-going threshold level			1.67	2	V
V_{T-}	Negative-going threshold level		0.8	1.23		V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)			0.44		V
I_I	Input current	$V_I = V_{CC}$ or 0			±1	µA
C_i	Intrinsic input capacitance¶			3.79		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		2.15		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.
¶ Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	1.04	1.74	2.59	ns
t_{PHL}			1.24	2.71	5.27	
Δt_{PLH}	A	Y	0.13	0.24	0.45	ns/pF
Δt_{PHL}			0.19	0.44	0.83	

§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

IPL01LJ
CMOS-COMPATIBLE INPUT BUFFER WITH 70-μA PULL-UP SOURCE

D3015, OCTOBER 1987 – REVISED FEBRUARY 1989

EXTERNAL INPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The IPL01LJ is an input buffer that interfaces CMOS input voltage levels to CMOS internal-gate voltage levels. A 70-μA pull-up current source terminates the input pad to V_{CC}. When the input buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IP01LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡		TEST CONDITIONS	TYP§	MAX	UNIT
V_T	Input threshold voltage		2.5		V
I_I	Input current	$V_I = V_{CC}$		±1	μA
		$V_I = 0$	−70		
C_i	Intrinsic input capacitance¶		3.79		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	1.82		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	0.75	1.15	1.71	ns
t_{PHL}			0.35	0.82	1.45	
Δt_{PLH}	A	Y	0.1	0.19	0.36	ns/pF
Δt_{PHL}			0.09	0.18	0.24	

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Total input capacitance is dependent on the package and is equal to the sum of package capacitance and intrinsic input capacitance.

IPL04LJ
TTL-COMPATIBLE INPUT BUFFER WITH 70-μA PULL-UP SOURCE

D3015, OCTOBER 1987 – REVISED FEBRUARY 1989

EXTERNAL INPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The IPL04LJ is an input buffer that interfaces TTL input voltage levels to CMOS internal-gate voltage levels. A 70-μA pull-up current source terminates the input pad to V_{CC}. When the input buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IPL04LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡		TEST CONDITIONS	TYP§	MAX	UNIT
V_T	Input threshold voltage		1.3		V
I_I	Input current	$V_I = V_{CC}$		±1	μA
		$V_I = 0$	−70		
C_i	Intrinsic input capacitance¶		3.79		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	2.31		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	0.93	1.66	2.44	ns
t_{PHL}			0.13	1.23	2.84	
Δt_{PLH}	A	Y	0.1	0.19	0.39	ns/pF
Δt_{PHL}			0.12	0.26	0.62	

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.
§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
¶ Total input capacitance is dependent on the package and is equal to the sum of package capacitance and intrinsic input capacitance.

IPU01LJ
CMOS-COMPATIBLE INPUT BUFFER WITH 70-μA PULL-DOWN SOURCE

D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL INPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The IPU01LJ is an input buffer that interfaces CMOS input voltage levels to CMOS internal-gate voltage levels. A 70-μA pull-down current source terminates the input pad to GND. When the input buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IPU01LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended operating ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡		TEST CONDITIONS	TYP§	MAX	UNIT
V_T	Input threshold voltage		2.5		V
I_I	Input current	$V_I = V_{CC}$	70		μA
		$V_I = 0$		±1	
C_i	Intrinsic input capacitance¶		3.79		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	1.82		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	0.76	1.16	1.7	ns
t_{PHL}			0.31	0.8	1.4	
Δt_{PLH}	A	Y	0.1	0.19	0.36	ns/pF
Δt_{PHL}			0.08	0.14	0.25	

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.
§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
¶ Total input capacitance is dependent on the package and is equal to the sum of package capacitance and intrinsic input capacitance.

IPU04LJ
TTL-COMPATIBLE INPUT BUFFER WITH 70-μA PULL-DOWN SOURCE

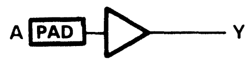
D3015, OCTOBER 1987 – REVISED FEBRUARY 1989

EXTERNAL INPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The IPU04LJ is an input buffer that interfaces TTL input voltage levels to CMOS internal-gate voltage levels. A 70-μA pull-down current source terminates the input pad to V_{CC}. When the input buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IPU04LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡		TEST CONDITIONS	TYP§	MAX	UNIT
V_T	Input threshold voltage		1.3		V
I_I	Input current	$V_I = V_{CC}$	70		μA
		$V_I = 0$		±1	
C_i	Intrinsic input capacitance¶		3.79		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	2.31		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Y	0.99	1.68	2.47	ns
t_{PHL}			0.13	1.29	3.01	
Δt_{PLH}	A	Y	0.09	0.19	0.37	ns/pF
Δt_{PHL}			0.11	0.26	0.64	

‡ For Suppply Current, I_{CC}, see the TGC100 Series Data.
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Total input capacitance is dependent on the package and is equal to the sum of package capacitance and intrinsic input capacitance.

D3015, OCTOBER 1987

EXTERNAL BIDIRECTIONAL I/O MACROS

The TGC100 Series 1-μm CMOS Gate Arrays provide the custom IC designer with a wide selection of bidirectional I/Os featuring both CMOS- and TTL-compatible outputs. Each output is characterized for driving either CMOS loads or TTL loads. For each output offered, both a CMOS and a TTL threshold input buffer version are available with the additional choice of either an active pull-up or pull-down terminator. Additionally, for each output offered, the designer can select from I/Os minimizing delay time or from I/Os incorporating di/dt circuitry designed to reduce the effects of impedance mismatch.

TGC100 Series I/Os are designed to actively bypass electrostatic discharges. Guard-ring structures are employed that provide current management techniques for the buffer to recover from exposure to high currents of up to 400 mA thereby negating most common sources that can produce a latch-up condition.

These bidirectional I/Os are designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation; therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

The dynamic-drive capability of the outputs is specified by the change in propagation delay time parameters included with the switching characteristics. The change in propagation delay times provides a means for making direct comparisons of the various output responses to changes in capacitive loading.

MACRO SELECTION TABLE

MACRO NAME	OUTPUT CURRENT (SINK AND SOURCE) (mA)	di/dt CIRCUITRY	I/O TERMINATION	INPUT THRESHOLD	PAGE NUMBERS
IOI21LJ	2	NO	NONE	CMOS	12-3
IOI24LJ	2	NO	NONE	TTL	12-6
IOI41LJ	4	NO	NONE	CMOS	12-9
IOI44LJ	4	NO	NONE	TTL	12-12
IOI81LJ	8	NO	NONE	CMOS	12-15
IOI84LJ	8	NO	NONE	TTL	12-18
IOK21LJ	2	YES	NONE	CMOS	12-21
IOK24LJ	2	YES	NONE	TTL	12-24
IOK41LJ	4	YES	NONE	CMOS	12-27
IOK44LJ	4	YES	NONE	TTL	12-30
IOK81LJ	8	YES	NONE	CMOS	12-33
IOK84LJ	8	YES	NONE	TTL	12-36

D3015, OCTOBER 1987

MACRO SELECTION TABLE (Continued)

MACRO NAME	OUTPUT CURRENT (SINK AND SOURCE) (mA)	di/dt CIRCUITRY	I/O TERMINATION	INPUT THRESHOLD	PAGE NUMBERS
IOL21LJ	2	NO	PULLUP	CMOS	12-39
IOL24LJ	2	NO	PULLUP	TTL	12-42
IOL41LJ	4	NO	PULLUP	CMOS	12-45
IOL44LJ	4	NO	PULLUP	TTL	12-48
IOL81LJ	8	NO	PULLUP	CMOS	12-51
IOL84LJ	8	NO	PULLUP	TTL	12-54
ION21LJ	2	YES	PULLUP	CMOS	12-57
ION24LJ	2	YES	PULLUP	TTL	12-60
ION41LJ	4	YES	PULLUP	CMOS	12-63
ION44LJ	4	YES	PULLUP	TTL	12-66
ION81LJ	8	YES	PULLUP	CMOS	12-69
ION84LJ	8	YES	PULLUP	TTL	12-72
IOU21LJ	2	NO	PULLDOWN	CMOS	12-75
IOU24LJ	2	NO	PULLDOWN	TTL	12-78
IOU41LJ	4	NO	PULLDOWN	CMOS	12-81
IOU44LJ	4	NO	PULLDOWN	TTL	12-84
IOU81LJ	8	NO	PULLDOWN	CMOS	12-87
IOU84LJ	8	NO	PULLDOWN	TTL	12-90
IOW21LJ	2	YES	PULLDOWN	CMOS	12-93
IOW24LJ	2	YES	PULLDOWN	TTL	12-96
IOW41LJ	4	YES	PULLDOWN	CMOS	12-99
IOW44LJ	4	YES	PULLDOWN	TTL	12-102
IOW81LJ	8	YES	PULLDOWN	CMOS	12-105
IOW84LJ	8	YES	PULLDOWN	TTL	12-108

notes

The following notes apply to the electrical characteristics tables of all TGC100 Series Input/Output Macros:

‡For Supply Current, I_{CC}, see the TGC100 Series Data.

§Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

¶Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

NOTE 1: These limits apply when all other external outputs are open.

IO121LJ
2-mA 3-STATE I/O BUFFER
WITH CMOS INPUT AND CMOS/TTL OUTPUT

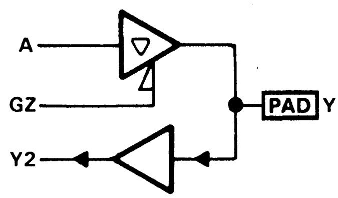
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IO121LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IO121LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		$I_{OH} = -2$ mA	3.7			V
			$I_{OH} = -20\ \mu A$, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 2$ mA			0.5	V
			$I_{OL} = 20\ \mu A$, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		11.5		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.03	2.56	5.33	ns
t_{PHL}				3.15	6.72	12.41	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.02	3	6.55	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.31	7.40	14.55	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.99	5.31	11.18	ns
t_{PHL}				7.02	14.19	25.23	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.98	5.86	12.91	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	7.37	15.84	30.53	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.47	1.17	2.28	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.27	0.52	0.81	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.17	ns/pF
Δt_{PHL}				0.11	0.21	0.37	
Δt_{PZH}	GZ	Y1		0.03	0.08	0.18	ns/pF
Δt_{PZL}				0.12	0.24	0.46	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.82	4.29	8.31	ns
t_{PHL}				2.29	5.04	9.66	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.95	4.98	10.3	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.37	5.31	10.48	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	4.13	9.77	18.75	ns
t_{PHL}				4.75	9.96	18.42	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.29	10.96	22.65	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.9	10.6	20.45	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.07	0.16	0.3	ns/pF
Δt_{PHL}				0.07	0.14	0.25	
Δt_{PZH}	GZ	Y1		0.07	0.17	0.35	ns/pF
Δt_{PZL}				0.07	0.15	0.28	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.72	1.09	1.65	ns
t_{PHL}				0.31	0.79	1.35	
Δt_{PLH}	Y1	Y2		0.1	0.22	0.37	ns/pF
Δt_{PHL}				0.08	0.14	0.27	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

IO124LJ 2-mA 3-STATE I/O BUFFER WITH TTL INPUT AND CMOS/TTL OUTPUT

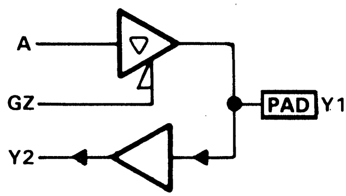
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IO124LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IO124LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		I_{OH} = −2 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		I_{OL} = 2 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		11.4		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.03	2.56	5.32	ns
t_{PHL}				3.14	6.69	12.34	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.02	3	6.54	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.3	7.36	14.44	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.99	5.31	11.18	ns
t_{PHL}				7.01	14.15	25.15	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.98	5.86	12.91	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	7.36	15.8	30.43	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.47	1.17	2.28	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.27	0.52	0.81	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.17	ns/pF
Δt_{PHL}				0.11	0.21	0.37	
Δt_{PZH}	GZ	Y1		0.03	0.08	0.18	ns/pF
Δt_{PZL}				0.12	0.24	0.46	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.95	1.63	2.38	ns
t_{PHL}				0.13	1.32	3.14	
Δt_{PLH}	Y1	Y2		0.09	0.2	0.4	ns/pF
Δt_{PHL}				0.1	0.29	0.67	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.83	4.31	8.33	ns
t_{PHL}				2.28	5.03	9.63	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.96	5	10.35	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.37	5.3	10.45	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	4.14	9.8	18.8	ns
t_{PHL}				4.74	9.94	18.4	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.3	10.99	22.72	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.89	10.58	20.42	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.07	0.16	0.3	ns/pF
Δt_{PHL}				0.07	0.14	0.25	
Δt_{PZH}	GZ	Y1		0.07	0.17	0.35	ns/pF
Δt_{PZL}				0.07	0.15	0.28	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

IO141LJ 4-mA 3-STATE I/O BUFFER WITH CMOS INPUT AND CMOS/TTL OUTPUT

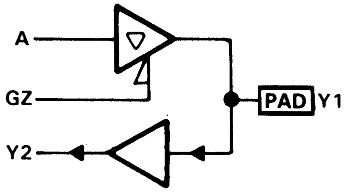
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IO141LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IO141LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		I_{OH} = −4 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		10.9		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.8	1.98	4.14	ns
t_{PHL}				2.06	4.79	9.3	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.81	2.37	5.13	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.13	4.99	9.83	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.29	3.38	7.12	ns
t_{PHL}				4.02	8.62	15.95	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.29	3.79	8.21	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.13	9.02	17.06	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.61	1.63	3.29	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.3	0.62	0.97	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.04	0.09	ns/pF
Δt_{PHL}				0.06	0.11	0.19	
Δt_{PZH}	GZ	Y1		0.01	0.04	0.09	ns/pF
Δt_{PZL}				0.06	0.12	0.21	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.19	2.88	5.72	ns
t_{PHL}				1.61	3.84	7.7	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.31	3.33	6.8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.66	3.94	7.91	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.34	5.63	10.97	ns
t_{PHL}				2.88	6.45	12.42	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.47	6.19	12.45	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.95	6.62	12.86	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.15	ns/pF
Δt_{PHL}				0.04	0.07	0.13	
Δt_{PZH}	GZ	Y1		0.03	0.08	0.16	ns/pF
Δt_{PZL}				0.04	0.08	0.14	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.72	1.09	1.65	ns
t_{PHL}				0.31	0.79	1.35	
Δt_{PLH}	Y1	Y2		0.1	0.22	0.37	ns/pF
Δt_{PHL}				0.08	0.14	0.27	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

IO144LJ 4-mA 3-STATE I/O BUFFER WITH TTL INPUT AND CMOS/TTL OUTPUT

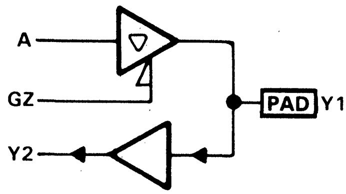
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IO144LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IO144LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		I_{OH} = −4 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		11.7		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

$C_L = 15$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.8	1.98	4.14	ns
t_{PHL}				2.06	4.78	9.27	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.81	2.37	5.12	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.12	4.98	9.79	

$C_L = 50$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.29	3.38	7.12	ns
t_{PHL}				4.01	8.6	15.91	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.29	3.79	8.21	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.12	9	17.01	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.61	1.63	3.29	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.3	0.62	0.97	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.04	0.09	ns/pF
Δt_{PHL}				0.06	0.11	0.19	
Δt_{PZH}	GZ	Y1		0.01	0.04	0.09	ns/pF
Δt_{PZL}				0.06	0.11	0.21	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.94	1.63	2.38	ns
t_{PHL}				0.13	1.31	3.09	
Δt_{PLH}	Y1	Y2		0.09	0.2	0.4	ns/pF
Δt_{PHL}				0.1	0.28	0.66	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.19	2.88	5.72	ns
t_{PHL}				1.61	3.84	7.69	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.31	3.33	6.8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.66	3.93	7.9	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.35	5.64	10.98	ns
t_{PHL}				2.88	6.45	12.41	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.48	6.2	12.47	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.95	6.61	12.85	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.15	ns/pF
Δt_{PHL}				0.04	0.07	0.13	
Δt_{PZH}	GZ	Y1		0.03	0.08	0.16	ns/pF
Δt_{PZL}				0.04	0.08	0.14	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOI81LJ
8-mA 3-STATE I/O BUFFER WITH CMOS INPUT AND CMOS/TTL OUTPUT

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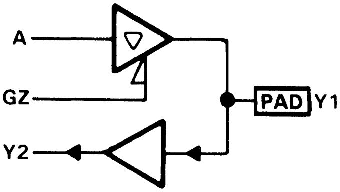
EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOI81LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOI81LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		$I_{OH} = -8$ mA	3.7			V
			$I_{OH} = -20$ μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 8$ mA			0.5	V
			$I_{OL} = 20$ μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		12.6		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

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TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

$C_L = 15$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.75	1.97	4.22	ns
t_{PHL}				1.64	4.26	8.73	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.75	2.34	5.16	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.68	4.34	8.92	

$C_L = 50$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.05	2.83	6.06	ns
t_{PHL}				2.71	6.52	12.81	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.05	3.21	7.03	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.77	6.65	13.1	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.9	2.6	5.42	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.42	0.76	1.31	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.02	0.05	ns/pF
Δt_{PHL}				0.03	0.06	0.12	
Δt_{PZH}	GZ	Y1		0.01	0.02	0.05	ns/pF
Δt_{PZL}				0.03	0.07	0.12	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.98	2.56	5.29	ns
t_{PHL}				1.34	3.58	7.53	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.1	2.96	6.2	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.37	3.61	7.58	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.58	4.04	8.17	ns
t_{PHL}				2.1	5.25	10.68	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.7	4.46	9.16	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.14	5.3	10.77	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.04	0.08	ns/pF
Δt_{PHL}				0.02	0.05	0.09	
Δt_{PZH}	GZ	Y1		0.02	0.04	0.08	ns/pF
Δt_{PZL}				0.02	0.05	0.09	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.72	1.09	1.65	ns
t_{PHL}				0.31	0.79	1.35	
Δt_{PLH}	Y1	Y2		0.1	0.22	0.37	ns/pF
Δt_{PHL}				0.08	0.14	0.27	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

IO184LJ
8-mA 3-STATE I/O BUFFER WITH TTL INPUT AND CMOS/TTL OUTPUT

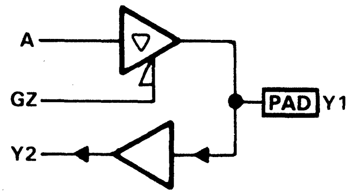
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IO184LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IO184LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		$I_{OH} = -8$ mA	3.7			V
			$I_{OH} = -20\ \mu A$, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 8$ mA			0.5	V
			$I_{OL} = 20\ \mu A$, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		13.4		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

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TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.75	1.97	4.22	ns
t_{PHL}				1.64	4.25	8.71	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.75	2.34	5.16	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.67	4.33	8.9	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.05	2.83	6.06	ns
t_{PHL}				2.71	6.51	12.79	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.05	3.21	7.03	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.77	6.64	13.08	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.9	2.6	5.42	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.42	0.76	1.31	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.02	0.05	ns/pF
Δt_{PHL}				0.03	0.06	0.12	
Δt_{PZH}	GZ	Y1		0.01	0.02	0.05	ns/pF
Δt_{PZL}				0.03	0.07	0.12	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.94	1.63	2.38	ns
t_{PHL}				0.12	1.29	2.99	
Δt_{PLH}	Y1	Y2		0.09	0.2	0.4	ns/pF
Δt_{PHL}				0.11	0.26	0.64	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

$C_L = 15$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.98	2.56	5.29	ns
t_{PHL}				1.34	3.58	7.53	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.1	2.96	6.19	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.37	3.6	7.57	

$C_L = 50$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.58	4.04	8.18	ns
t_{PHL}				2.1	5.25	10.67	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.7	4.46	9.16	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.14	5.3	10.77	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.04	0.08	ns/pF
Δt_{PHL}				0.02	0.05	0.09	
Δt_{PZH}	GZ	Y1		0.02	0.04	0.08	ns/pF
Δt_{PZL}				0.02	0.05	0.09	

†Typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.

2-mA 3-STATE I/O BUFFER WITH CMOS INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

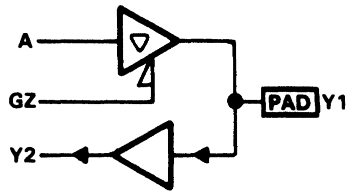
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L),Y2 = Y1

description

The IOK21LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOK21LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		$I_{OH} = -2$ mA	3.7			V
			$I_{OH} = -20\ \mu A$, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 2$ mA			0.5	V
			$I_{OL} = 20\ \mu A$, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		10.4		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.33	3.43	7.23	ns
t_{PHL}				4.5	9.78	18.23	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.38	3.89	8.42	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.69	10.66	21.07	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.31	6.2	13.12	ns
t_{PHL}				8.44	17.45	31.48	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.35	6.76	14.8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	8.8	19.21	37.15	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.52	1.29	2.49	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.27	0.55	0.87	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.17	ns/pF
Δt_{PHL}				0.11	0.22	0.38	
Δt_{PZH}	GZ	Y1		0.03	0.08	0.18	ns/pF
Δt_{PZL}				0.12	0.24	0.46	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.15	5.21	10.27	ns
t_{PHL}				3.51	7.88	15.14	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.33	5.91	12.25	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.61	8.29	16.47	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	4.46	10.69	20.72	ns
t_{PHL}				6.12	13.13	24.53	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.67	11.89	24.59	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	6.28	13.85	26.87	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.07	0.16	0.3	ns/pF
Δt_{PHL}				0.07	0.15	0.27	
Δt_{PZH}	GZ	Y1		0.07	0.17	0.35	ns/pF
Δt_{PZL}				0.08	0.16	0.3	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.72	1.1	1.65	ns
t_{PHL}				0.31	0.79	1.37	
Δt_{PLH}	Y1	Y2		0.1	0.21	0.37	ns/pF
Δt_{PHL}				0.08	0.14	0.26	

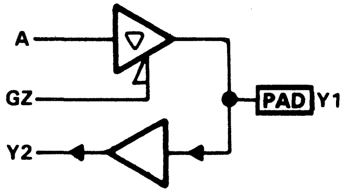
†Typical values are at V_{CC} = 5 V, T_A = 25°C.

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOK24LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOK24LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		I_{OH} = −2 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		I_{OL} = 2 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		12.6		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.33	3.43	7.23	ns
t_{PHL}				4.48	9.74	18.15	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.38	3.88	8.41	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.67	10.61	20.95	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.31	6.21	13.12	ns
t_{PHL}				8.43	17.41	31.4	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.35	6.77	14.8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	8.79	19.16	37.03	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.52	1.29	2.49	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.27	0.55	0.87	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.17	ns/pF
Δt_{PHL}				0.11	0.22	0.38	
Δt_{PZH}	GZ	Y1		0.03	0.08	0.18	ns/pF
Δt_{PZL}				0.12	0.24	0.46	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.95	1.64	2.39	ns
t_{PHL}				0.14	1.33	3.15	
Δt_{PLH}	Y1	Y2		0.09	0.2	0.4	ns/pF
Δt_{PHL}				0.1	0.29	0.67	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.16	5.22	10.3	ns
t_{PHL}				3.5	7.86	15.11	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.34	5.93	12.3	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.6	8.28	16.44	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	4.47	10.72	20.77	ns
t_{PHL}				6.11	13.11	24.50	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.68	11.92	24.66	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	6.27	13.84	26.84	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.07	0.16	0.3	ns/pF
Δt_{PHL}				0.07	0.15	0.27	
Δt_{PZH}	GZ	Y1		0.07	0.17	0.35	ns/pF
Δt_{PZL}				0.08	0.16	0.3	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

4-mA 3-STATE I/O BUFFER WITH CMOS INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

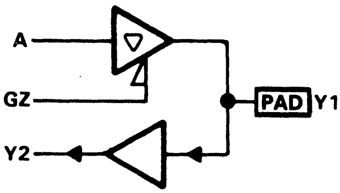
D3015, OCTOBER 1987–REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOK41LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOK41LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		V
V_{OH}	High-level output voltage		I_{OH} = −4 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	$V_{CC}-0.1$			V
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	V
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		pF
		Y1¶			7.13		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		11.8		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.14	3.05	6.55	ns
t_{PHL}				3.46	8.04	15.51	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.2	3.46	7.5	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.57	8.41	16.6	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.72	4.64	9.88	ns
t_{PHL}				5.7	12.45	23.21	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.79	5.07	10.93	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.83	12.97	24.76	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.65	1.75	3.53	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.32	0.64	1	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.05	0.1	ns/pF
Δt_{PHL}				0.06	0.13	0.22	
Δt_{PZH}	GZ	Y1		0.02	0.05	0.1	ns/pF
Δt_{PZL}				0.06	0.13	0.23	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.62	4.12	8.38	ns
t_{PHL}				2.81	6.75	13.41	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.81	4.6	9.48	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.87	6.95	14.01	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.83	6.97	13.86	ns
t_{PHL}				4.4	10	19.25	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.01	7.56	15.31	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.48	10.26	20.02	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.16	ns/pF
Δt_{PHL}				0.05	0.09	0.17	
Δt_{PZH}	GZ	Y1		0.03	0.08	0.17	ns/pF
Δt_{PZL}				0.05	0.09	0.17	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.72	1.1	1.65	ns
t_{PHL}				0.31	0.79	1.37	
Δt_{PLH}	Y1	Y2		0.1	0.21	0.37	ns/pF
Δt_{PHL}				0.08	0.14	0.26	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOK44LJ
4-mA 3-STATE I/O BUFFER WITH TTL INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

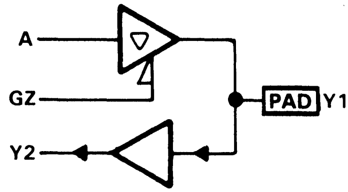
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOK44LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOK44LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		$I_{OH} = -4$ mA	3.7			V
			$I_{OH} = -20$ μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 4$ mA			0.5	V
			$I_{OL} = 20$ μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		12.1		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.14	3.05	6.55	ns
t_{PHL}				3.45	8.02	15.47	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.2	3.46	7.5	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.56	8.38	16.54	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.72	4.64	9.88	ns
t_{PHL}				5.69	12.43	23.17	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.79	5.07	10.93	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.82	12.95	24.71	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.65	1.75	3.53	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.32	0.64	1	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.05	0.1	ns/pF
Δt_{PHL}				0.06	0.13	0.22	
Δt_{PZH}	GZ	Y1		0.02	0.05	1	ns/pF
Δt_{PZL}				0.06	0.13	0.23	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.95	1.64	2.39	ns
t_{PHL}				0.13	1.32	3	
Δt_{PLH}	Y1	Y2		0.09	0.2	0.4	ns/pF
Δt_{PHL}				0.1	0.28	0.66	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.63	4.12	8.39	ns
t_{PHL}				2.8	6.74	13.4	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.81	4.61	9.48	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.87	6.94	14	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.83	6.98	13.87	ns
t_{PHL}				4.4	9.99	19.24	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.02	7.57	15.33	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.48	10.25	20.01	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.16	ns/pF
Δt_{PHL}				0.05	0.09	0.17	
Δt_{PZH}	GZ	Y1		0.03	0.08	0.17	ns/pF
Δt_{PZL}				0.05	0.09	0.17	

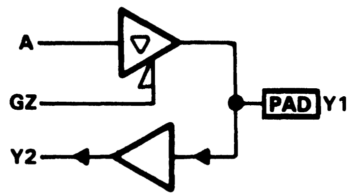
†Typical values are at V_{CC} = 5 V, T_A = 25°C.

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOK81LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOK81LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		$I_{OH} = -8$ mA	3.7			V
			$I_{OH} = -20\ \mu A$, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 8$ mA			0.5	V
			$I_{OL} = 20\ \mu A$, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		13.2		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

$C_L = 15$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.12	3.3	7.28	ns
t_{PHL}				3.16	7.94	15.91	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.2	3.7	8.19	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.24	8.19	16.64	

$C_L = 50$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.58	4.51	9.8	ns
t_{PHL}				4.69	11.05	21.46	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.66	4.91	10.72	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.78	11.3	22.16	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.94	2.72	5.65	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.42	0.79	1.38	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.03	0.07	ns/pF
Δt_{PHL}				0.04	0.09	0.16	
Δt_{PZH}	GZ	Y1		0.01	0.03	0.07	ns/pF
Δt_{PZL}				0.04	0.09	0.16	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

$C_L = 15$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.52	4.17	8.8	ns
t_{PHL}				2.59	6.82	14.06	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.72	4.62	9.73	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.65	6.97	14.51	

$C_L = 50$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.29	6.02	12.38	ns
t_{PHL}				3.76	9.28	18.58	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.49	6.49	13.37	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.83	9.41	18.97	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.05	0.1	ns/pF
Δt_{PHL}				0.03	0.07	0.13	
Δt_{PZH}	GZ	Y1		0.02	0.05	0.1	ns/pF
Δt_{PZL}				0.03	0.07	0.13	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.72	1.1	1.65	ns
t_{PHL}				0.31	0.79	1.37	
Δt_{PLH}	Y1	Y2		0.1	0.21	0.37	ns/pF
Δt_{PHL}				0.08	0.14	0.26	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOK84LJ
8-mA 3-STATE I/O BUFFER WITH TTL INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

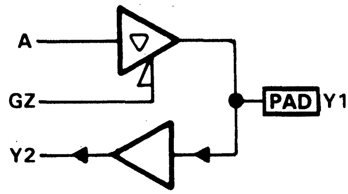
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOK84LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOK84LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		$I_{OH} = -8$ mA	3.7			V
			$I_{OH} = -20$ μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 8$ mA			0.5	V
			$I_{OL} = 20$ μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		13.4		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.12	3.3	7.28	ns
t_{PHL}				3.15	7.92	15.88	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.2	3.7	8.18	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.24	8.18	16.61	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.58	4.51	9.8	ns
t_{PHL}				4.68	11.04	21.43	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.66	4.91	10.72	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.77	11.29	22.13	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.94	2.72	5.64	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.43	0.79	1.38	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.03	0.07	ns/pF
Δt_{PHL}				0.04	0.09	0.16	
Δt_{PZH}	GZ	Y1		0.01	0.03	0.07	ns/pF
Δt_{PZL}				0.04	0.09	0.16	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.95	1.64	2.39	ns
t_{PHL}				0.12	1.29	3	
Δt_{PLH}	Y1	Y2		0.09	0.2	0.4	ns/pF
Δt_{PHL}				0.11	0.26	0.64	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.52	4.18	8.8	ns
t_{PHL}				2.59	6.81	14.05	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.72	4.62	9.73	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.65	6.96	14.49	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.3	6.03	12.39	ns
t_{PHL}				3.76	9.27	18.56	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.49	6.49	13.37	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.82	9.41	18.95	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.05	0.1	ns/pF
Δt_{PHL}				0.03	0.07	0.13	
Δt_{PZH}	GZ	Y1		0.02	0.05	0.1	ns/pF
Δt_{PZL}				0.03	0.07	0.13	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

2-mA 3-STATE I/O BUFFER WITH 70-μA PULL-UP, CMOS INPUT, AND CMOS/TTL OUTPUT

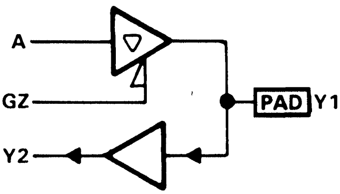
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOL21LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. A 70-μA pull-up current source terminates the output pad to V_{CC}. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOL21LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		I_{OH} = −2 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	V_{CC} − 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 2 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$			±10	μA
			V_O = 0		−70		
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		19.3		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.02	2.55	5.3	ns
t_{PHL}				3.18	6.79	12.52	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.22	6.78	12.39	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.22	6.78	12.39	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.98	5.27	11.09	ns
t_{PHL}				7.06	14.28	25.39	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	7.1	14.27	25.24	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	7.1	14.27	25.24	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.47	1.19	2.38	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.27	0.52	0.82	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.17	ns/pF
Δt_{PHL}				0.11	0.21	0.37	
Δt_{PZH}	GZ	Y1		0.11	0.21	0.37	ns/pF
Δt_{PZL}				0.11	0.21	0.37	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

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CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.82	4.28	8.27	ns
t_{PHL}				2.31	5.08	9.74	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.35	5.08	9.61	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.35	5.08	9.61	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	4.12	9.72	18.63	ns
t_{PHL}				4.78	10.02	18.53	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.81	10.01	18.38	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.81	10.01	18.38	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.07	0.16	0.3	ns/pF
Δt_{PHL}				0.07	0.14	0.25	
Δt_{PZH}	GZ	Y1		0.07	0.14	0.25	ns/pF
Δt_{PZL}				0.07	0.14	0.25	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.74	1.15	1.7	ns
t_{PHL}				0.35	0.83	1.44	
Δt_{PLH}	Y1	Y2		0.1	0.19	0.36	ns/pF
Δt_{PHL}				0.09	0.17	0.24	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOL24LJ
2-mA 3-STATE I/O BUFFER WITH 70-μA PULL-UP, TTL INPUT, AND CMOS/TTL OUTPUT

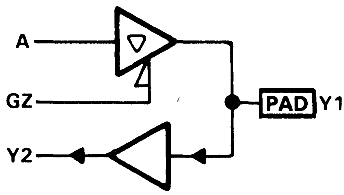
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOL24LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. A 70-μA pull-up current source terminates the output pad to V_{CC}. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOL24LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		I_{OH} = −2 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	V_{CC} − 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 2 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$			±10	μA
			V_O = 0		−70		
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		19.3		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.02	2.55	5.29	ns
t_{PHL}				3.17	6.75	12.45	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.21	6.75	12.33	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.21	6.75	12.33	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.98	5.27	11.09	ns
t_{PHL}				7.05	14.24	25.31	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	7.08	14.24	25.16	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	7.08	14.24	25.16	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.47	1.19	2.38	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.27	0.52	0.82	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.17	ns/pF
Δt_{PHL}				0.11	0.21	0.37	
Δt_{PZH}	GZ	Y1		0.11	0.21	0.37	ns/pF
Δt_{PZL}				0.11	0.21	0.37	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.93	1.64	2.43	ns
t_{PHL}				0.18	1.34	3.17	
Δt_{PLH}	Y1	Y2		0.1	0.2	0.39	ns/pF
Δt_{PHL}				0.08	0.29	0.66	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.83	4.29	8.29	ns
t_{PHL}				2.31	5.07	9.72	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.34	5.07	9.59	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.34	5.07	9.59	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	4.13	9.75	18.68	ns
t_{PHL}				4.77	10	18.51	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.81	10	18.36	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.81	10	18.36	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.07	0.16	0.3	ns/pF
Δt_{PHL}				0.07	0.14	0.25	
Δt_{PZH}	GZ	Y1		0.07	0.14	0.25	ns/pF
Δt_{PZL}				0.07	0.14	0.25	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

4-mA 3-STATE I/O BUFFER WITH 70-µA PULL-UP, CMOS INPUT, AND CMOS/TTL OUTPUT

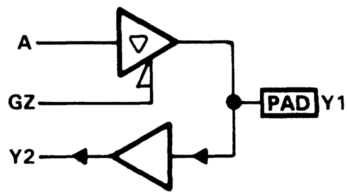
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOL41LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. A 70-µA pull-up current source terminates the output pad to V_{CC}. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOL41LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER[‡]			TEST CONDITIONS	MIN	TYP[§]	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		$I_{OH} = -4$ mA	3.7			V
			$I_{OH} = -20$ µA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 4$ mA			0.5	V
			$I_{OL} = 20$ µA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$			±10	µA
			$V_O = 0$		−70		
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1[¶]			7.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		18.8		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.8	1.98	4.13	ns
t_{PHL}				2.08	4.82	9.36	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.11	4.82	9.23	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.11	4.82	9.23	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.29	3.37	7.1	ns
t_{PHL}				4.03	8.66	16.01	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.07	8.65	15.87	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.07	8.65	15.87	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.62	1.66	3.39	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.3	0.62	0.98	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.04	0.08	ns/pF
Δt_{PHL}				0.06	0.11	0.19	
Δt_{PZH}	GZ	Y1		0.06	0.11	0.19	ns/pF
Δt_{PZL}				0.06	0.11	0.19	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.18	2.88	5.71	ns
t_{PHL}				1.62	3.87	7.75	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.66	3.86	7.61	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.66	3.86	7.61	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.34	5.62	10.94	ns
t_{PHL}				2.89	6.48	12.47	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.93	6.47	12.33	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.93	6.47	12.33	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.15	ns/pF
Δt_{PHL}				0.04	0.07	0.13	
Δt_{PZH}	GZ	Y1		0.04	0.07	0.13	ns/pF
Δt_{PZL}				0.04	0.07	0.13	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.74	1.15	1.7	ns
t_{PHL}				0.35	0.83	1.44	
Δt_{PLH}	Y1	Y2		0.1	0.19	0.36	ns/pF
Δt_{PHL}				0.09	0.17	0.24	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOL44LJ
4-mA 3-STATE I/O BUFFER WITH 70-μA PULL-UP, TTL INPUT, AND CMOS/TTL OUTPUT

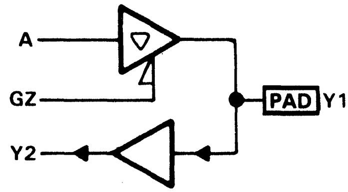
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOL44LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. A 70-μA pull-up current source terminates the output pad to V_{CC}. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOL44LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		I_{OH} = −4 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		V_O = V_{CC}			±10	μA
			V_O = 0		−70		
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		19.3		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.8	1.98	4.13	ns
t_{PHL}				2.07	4.81	9.33	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.11	4.81	9.2	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.11	4.81	9.2	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.29	3.37	7.09	ns
t_{PHL}				4.03	8.64	15.97	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.06	8.63	15.83	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.06	8.63	15.83	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.62	1.66	3.39	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.3	0.62	0.98	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.04	0.08	ns/pF
Δt_{PHL}				0.06	0.11	0.19	
Δt_{PZH}	GZ	Y1		0.06	0.11	0.19	ns/pF
Δt_{PZL}				0.06	0.11	0.19	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.93	1.64	2.43	ns
t_{PHL}				0.17	1.32	3.12	
Δt_{PLH}	Y1	Y2		0.1	0.2	0.39	ns/pF
Δt_{PHL}				0.09	0.29	0.66	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.19	2.88	5.71	ns
t_{PHL}				1.62	3.86	7.74	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.66	3.86	7.6	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.66	3.86	7.6	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.35	5.63	10.95	ns
t_{PHL}				2.89	6.47	12.46	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.93	6.47	12.32	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.93	6.47	12.32	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.15	ns/pF
Δt_{PHL}				0.04	0.07	0.13	
Δt_{PZH}	GZ	Y1		0.04	0.07	0.13	ns/pF
Δt_{PZL}				0.04	0.07	0.13	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

8-mA 3-STATE I/O BUFFER WITH 70-μA PULL-UP, CMOS INPUT, AND CMOS/TTL OUTPUT

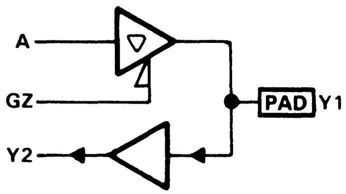
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOL81LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. A 70-μA pull-up current source terminates the output pad to V_{CC}. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOL81LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		$I_{OH} = -8$ mA	3.7			V
			$I_{OH} = -20$ μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 8$ mA			0.5	V
			$I_{OL} = 20$ μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$			±10	μA
			$V_O = 0$		−70		
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		20.4		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.75	1.97	4.22	ns
t_{PHL}				1.64	4.28	8.76	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.67	4.26	8.62	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.67	4.26	8.62	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.05	2.83	6.05	ns
t_{PHL}				2.72	6.54	12.84	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.75	6.53	12.7	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.75	6.53	12.7	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.9	2.63	5.53	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.42	0.76	1.32	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.02	0.05	ns/pF
Δt_{PHL}				0.03	0.06	0.12	
Δt_{PZH}	GZ	Y1		0.03	0.06	0.12	ns/pF
Δt_{PZL}				0.03	0.06	0.12	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.98	2.56	5.28	ns
t_{PHL}				1.35	3.6	7.56	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.37	3.57	7.4	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.37	3.57	7.4	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.58	4.04	8.16	ns
t_{PHL}				2.1	5.26	10.7	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.14	5.25	10.55	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.14	5.25	10.55	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.04	0.08	ns/pF
Δt_{PHL}				0.02	0.05	0.09	
Δt_{PZH}	GZ	Y1		0.02	0.05	0.09	ns/pF
Δt_{PZL}				0.02	0.05	0.09	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.74	1.15	1.7	ns
t_{PHL}				0.35	0.83	1.44	
Δt_{PLH}	Y1	Y2		0.1	0.19	0.36	ns/pF
Δt_{PHL}				0.09	0.17	0.24	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOL84LJ
8-mA 3-STATE I/O BUFFER WITH 70-μA PULL-UP, TTL INPUT, AND CMOS/TTL OUTPUT

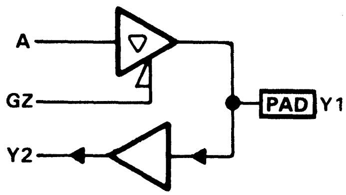
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOL84LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. A 70-μA pull-up current source terminates the output pad to V_{CC}. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOL84LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		I_{OH} = −8 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			
V_{OL}	Low-level output voltage		I_{OL} = 8 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$			±10	μA
			V_O = 0		−70		
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		21.3		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TEXAS INSTRUMENTS
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TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.75	1.97	4.21	ns
t_{PHL}				1.64	4.27	8.75	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.67	4.25	8.6	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.67	4.25	8.6	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.05	2.83	6.05	ns
t_{PHL}				2.72	6.53	12.82	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.75	6.52	12.68	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.75	6.52	12.68	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.9	2.63	5.53	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.42	0.76	1.32	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.02	0.05	ns/pF
Δt_{PHL}				0.03	0.06	0.12	
Δt_{PZH}	GZ	Y1		0.03	0.06	0.12	ns/pF
Δt_{PZL}				0.03	0.06	0.12	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.93	1.64	2.43	ns
t_{PHL}				0.15	1.3	3.01	
Δt_{PLH}	Y1	Y2		0.1	0.2	0.39	ns/pF
Δt_{PHL}				0.1	0.27	0.64	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.98	2.56	5.28	ns
t_{PHL}				1.35	3.59	7.56	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.37	3.56	7.4	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.37	3.56	7.4	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.58	4.04	8.17	ns
t_{PHL}				2.1	5.26	10.7	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.14	5.25	10.55	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.14	5.25	10.55	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.04	0.08	ns/pF
Δt_{PHL}				0.02	0.05	0.09	
Δt_{PZH}	GZ	Y1		0.02	0.05	0.09	ns/pF
Δt_{PZL}				0.02	0.05	0.09	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

2-mA 3-STATE I/O BUFFER WITH 70-μA PULL-UP, CMOS INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

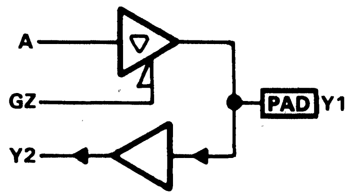
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The ION21LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. A 70-μA pull-up source terminates the output pad to V_{CC}. The input buffer responds to CMOS threshold levels on the I/O bus regardless of the state of the internal output enable GZ. When called, the following label format is developed and captured in the design netlist:

Label: ION21LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		I_{OH} = −2 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		I_{OL} = 2 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$			±10	μA
			V_O = 0		−70		
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		18		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.33	3.42	7.19	ns
t_{PHL}				4.54	9.85	18.36	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.56	9.85	18.28	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.56	9.85	18.28	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.3	6.17	13.02	ns
t_{PHL}				8.48	17.54	31.63	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	8.51	17.53	31.54	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	8.51	17.53	31.54	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.52	1.32	2.6	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.27	0.55	0.88	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.17	ns/pF
Δt_{PHL}				0.11	0.22	0.38	
Δt_{PZH}	GZ	Y1		0.11	0.22	0.38	ns/pF
Δt_{PZL}				0.11	0.22	0.38	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.15	5.19	10.22	ns
t_{PHL}				3.53	7.93	15.24	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.56	7.93	15.16	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.56	7.93	15.16	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	4.45	10.64	20.6	ns
t_{PHL}				6.15	13.19	24.64	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	6.18	13.19	24.55	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	6.18	13.19	24.55	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.07	0.16	0.3	ns/pF
Δt_{PHL}				0.07	0.15	0.27	
Δt_{PZH}	GZ	Y1		0.07	0.15	0.27	ns/pF
Δt_{PZL}				0.07	0.15	0.27	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.75	1.15	1.71	ns
t_{PHL}				0.35	0.82	1.45	
Δt_{PLH}	Y1	Y2		0.1	0.19	0.36	ns/pF
Δt_{PHL}				0.09	0.18	0.24	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

2-mA 3-STATE I/O BUFFER WITH 70-μA PULL-UP, TTL INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

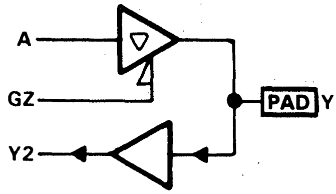
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The ION24LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. A 70-μA pull-up source terminates the output pad to V_{CC}. The input buffer responds to TTL threshold levels on the I/O bus regardless of the state of the internal output enable GZ. When called, the following label format is developed and captured in the design netlist:

Label: ION24LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		I_{OH} = −2 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		I_{OL} = 2 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$			±10	μA
			V_O = 0		−70		
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		20		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.33	3.41	7.18	ns
t_{PHL}				4.52	9.81	18.28	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.55	9.81	18.21	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.55	9.81	18.21	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.3	6.17	13.02	ns
t_{PHL}				8.47	17.5	31.55	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	8.5	17.5	31.47	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	8.5	17.5	31.47	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.52	1.32	2.6	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.27	0.55	0.88	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.17	ns/pF
Δt_{PHL}				0.11	0.22	0.38	
Δt_{PZH}	GZ	Y1		0.11	0.22	0.38	ns/pF
Δt_{PZL}				0.11	0.22	0.38	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.94	1.66	2.44	ns
t_{PHL}				0.18	1.35	3.19	
Δt_{PLH}	Y1	Y2		0.09	0.19	0.39	ns/pF
Δt_{PHL}				0.08	0.29	0.66	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

$C_L = 15$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.16	5.2	10.25	ns
t_{PHL}				3.53	7.92	15.21	
t_{PZH}	GZ	Y1	$R_L = 1\ k\Omega$ to GND	3.55	7.91	15.13	ns
t_{PZL}			$R_L = 1\ k\Omega$ to V_{CC}	3.55	7.91	15.13	

$C_L = 50$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	4.46	10.66	20.64	ns
t_{PHL}				6.14	13.18	24.61	
t_{PZH}	GZ	Y1	$R_L = 1\ k\Omega$ to GND	6.17	13.17	24.52	ns
t_{PZL}			$R_L = 1\ k\Omega$ to V_{CC}	6.17	13.17	24.52	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.07	0.16	0.3	ns/pF
Δt_{PHL}				0.07	0.15	0.27	
Δt_{PZH}	GZ	Y1		0.07	0.15	0.27	ns/pF
Δt_{PZL}				0.07	0.15	0.27	

†Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

ION41LJ
4-mA 3-STATE I/O BUFFER WITH 70-μA PULL-UP, CMOS INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

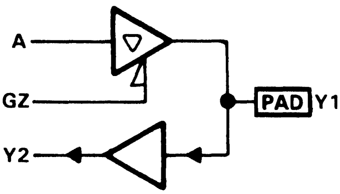
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The ION41LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. A 70-μA pull-up source terminates the output pad to V_{CC}. The input buffer responds to CMOS threshold levels on the I/O bus regardless of the state of the internal output enable GZ. When called, the following label format is developed and captured in the design netlist:

Label: ION41LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		$I_{OH} = -4$ mA	3.7			V
			$I_{OH} = -20$ μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 4$ mA			0.5	V
			$I_{OL} = 20$ μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$			±10	μA
			$V_O = 0$		−70		
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		19.6		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TEXAS INSTRUMENTS
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TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.14	3.04	6.53	ns
t_{PHL}				3.48	8.08	15.58	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.52	8.08	15.51	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.52	8.08	15.51	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.72	4.63	9.85	ns
t_{PHL}				5.71	12.49	23.27	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	5.75	12.49	23.21	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.75	12.49	23.21	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.65	1.77	3.63	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.32	0.64	1	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.05	0.1	ns/pF
Δt_{PHL}				0.06	0.13	0.22	
Δt_{PZH}	GZ	Y1		0.06	0.13	0.22	ns/pF
Δt_{PZL}				0.06	0.13	0.22	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.62	4.11	8.36	ns
t_{PHL}				2.82	6.78	13.47	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.85	6.78	13.39	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.85	6.78	13.39	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.82	6.96	13.82	ns
t_{PHL}				4.41	10.03	19.3	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.45	10.03	19.23	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.45	10.03	19.23	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.16	ns/pF
Δt_{PHL}				0.05	0.09	0.17	
Δt_{PZH}	GZ	Y1		0.05	0.09	0.17	ns/pF
Δt_{PZL}				0.05	0.09	0.17	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.75	1.15	1.71	ns
t_{PHL}				0.35	0.82	1.45	
Δt_{PLH}	Y1	Y2		0.1	0.19	0.36	ns/pF
Δt_{PHL}				0.09	0.18	0.24	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

ION44LJ
4-mA 3-STATE I/O BUFFER WITH 70-μA PULL-UP, TTL INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

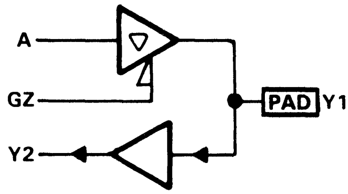
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The ION44LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. A 70-μA pull-up source terminates the output pad to V_{CC}. The input buffer responds to TTL threshold levels on the I/O bus regardless of the state of the internal output enable GZ. When called, the following label format is developed and captured in the design netlist:

Label: ION44LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		I_{OH} = −4 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$			±10	μA
			V_O = 0		−70		
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		19.7		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.14	3.04	6.52	ns
t_{PHL}				3.47	8.06	15.54	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.51	8.05	15.47	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.51	8.05	15.47	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.72	4.63	9.85	ns
t_{PHL}				5.71	12.47	23.23	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	5.74	12.47	23.17	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.74	12.47	23.17	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.65	1.77	3.63	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.32	0.64	1	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.05	0.1	ns/pF
Δt_{PHL}				0.06	0.13	0.22	
Δt_{PZH}	GZ	Y1		0.06	0.13	0.22	ns/pF
Δt_{PZL}				0.06	0.13	0.22	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.93	1.66	2.44	ns
t_{PHL}				0.17	1.33	3.13	
Δt_{PLH}	Y1	Y2		0.1	0.19	0.39	ns/pF
Δt_{PHL}				0.09	0.29	0.66	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.62	4.11	8.37	ns
t_{PHL}				2.82	6.78	13.46	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.85	6.77	13.37	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.85	6.77	13.37	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.83	6.97	13.84	ns
t_{PHL}				4.41	10.02	19.28	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.44	10.02	19.21	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.44	10.02	19.21	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.16	ns/pF
Δt_{PHL}				0.05	0.09	0.17	
Δt_{PZH}	GZ	Y1		0.05	0.09	0.17	ns/pF
Δt_{PZL}				0.05	0.09	0.17	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

8-mA 3-STATE I/O BUFFER WITH 70-μA PULL-UP, CMOS INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

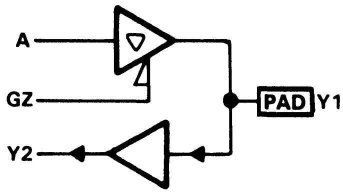
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The ION81LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. A 70-μA pull-up source terminates the output pad to V_{CC}. The input buffer responds to CMOS threshold levels on the I/O bus regardless of the state of the internal output enable GZ. When called, the following label format is developed and captured in the design netlist:

Label: ION81LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		I_{OH} = −8 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			
V_{OL}	Low-level output voltage		I_{OL} = 8 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$			±10	μA
			V_O = 0		−70		
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		21.6		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.12	3.29	7.27	ns
t_{PHL}				3.17	7.96	15.95	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.21	7.97	15.9	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.21	7.97	15.9	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.58	4.5	9.78	ns
t_{PHL}				4.7	11.07	21.47	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.74	11.06	21.41	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.74	11.06	21.41	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.94	2.75	5.75	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.42	0.79	1.38	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.03	0.07	ns/pF
Δt_{PHL}				0.04	0.09	0.16	
Δt_{PZH}	GZ	Y1		0.04	0.09	0.16	ns/pF
Δt_{PZL}				0.04	0.09	0.16	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

$C_L = 15$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.52	4.17	8.79	ns
t_{PHL}				2.61	6.84	14.11	
t_{PZH}	GZ	Y1	$R_L = 1\ k\Omega$ to GND	2.64	6.84	14.03	ns
t_{PZL}			$R_L = 1\ k\Omega$ to V_{CC}	2.64	6.84	14.03	

$C_L = 50$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.29	6.02	12.37	ns
t_{PHL}				3.77	9.29	18.59	
t_{PZH}	GZ	Y1	$R_L = 1\ k\Omega$ to GND	3.81	9.28	18.51	ns
t_{PZL}			$R_L = 1\ k\Omega$ to V_{CC}	3.81	9.28	18.51	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.05	0.1	ns/pF
Δt_{PHL}				0.03	0.07	0.13	
Δt_{PZH}	GZ	Y1		0.03	0.07	0.13	ns/pF
Δt_{PZL}				0.03	0.07	0.13	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.75	1.15	1.71	ns
t_{PHL}				0.35	0.82	1.45	
Δt_{PLH}	Y1	Y2		0.1	0.19	0.36	ns/pF
Δt_{PHL}				0.09	0.18	0.24	

†Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

ION84LJ
8-mA 3-STATE I/O BUFFER WITH 70-μA PULL-UP, TTL INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

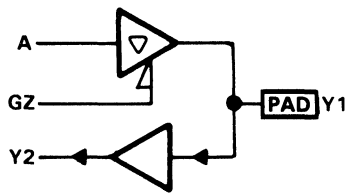
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The ION84LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. A 70-μA pull-up source terminates the output pad to V_{CC}. The input buffer responds to TTL threshold levels on the I/O bus regardless of the state of the internal output enable GZ. When called, the following label format is developed and captured in the design netlist:

Label: ION84LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		I_{OH} = −8 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	V_{CC} − 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 8 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$			±10	μA
			V_O = 0		−70		
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		21		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

8-mA 3-STATE I/O BUFFER WITH 70-μA PULL-UP, TTL INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

D3015, OCTOBER 1987

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.12	3.29	7.26	ns
t_{PHL}				3.16	7.95	15.92	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.2	7.95	15.87	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.2	7.95	15.87	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.58	4.5	9.78	ns
t_{PHL}				4.69	11.05	21.47	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.73	11.05	21.39	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.73	11.05	21.39	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.94	2.75	5.75	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.42	0.79	1.38	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.03	0.07	ns/pF
Δt_{PHL}				0.04	0.09	0.16	
Δt_{PZH}	GZ	Y1		0.04	0.09	0.16	ns/pF
Δt_{PZL}				0.04	0.09	0.16	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.93	1.66	2.44	ns
t_{PHL}				0.16	1.3	3.03	
Δt_{PLH}	Y1	Y2		0.1	0.19	0.39	ns/pF
Δt_{PHL}				0.1	0.27	0.64	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.52	4.17	8.79	ns
t_{PHL}				2.6	6.84	14.09	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.64	6.83	14.02	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.64	6.83	14.02	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.3	6.02	12.37	ns
t_{PHL}				3.77	9.29	18.6	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.81	9.28	18.51	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.81	9.28	18.51	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.05	0.1	ns/pF
Δt_{PHL}				0.03	0.07	0.13	
Δt_{PZH}	GZ	Y1		0.03	0.07	0.13	ns/pF
Δt_{PZL}				0.03	0.07	0.13	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOU21LJ 2-mA 3-STATE I/O BUFFER WITH 70-μA PULL-DOWN, CMOS INPUT, AND CMOS/TTL OUTPUT

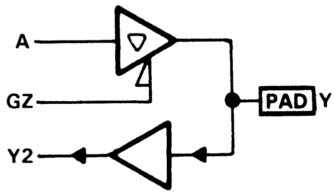
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOU21LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. A 70-μA pull-down current source terminates the output pad to GND. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOU21LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		$I_{OH} = -2$ mA	3.7			V
			$I_{OH} = -20$ μA, See Note 1	$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 2$ mA			0.5	V
			$I_{OL} = 20$ μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$		70		μA
			$V_O = 0$			±10	
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		16.8		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

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TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.03	2.58	5.36	ns
t_{PHL}				3.15	6.7	12.36	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.03	2.94	6.23	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.03	2.94	6.23	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.99	5.33	11.23	ns
t_{PHL}				7	14.13	25.1	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2	5.69	12.09	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2	5.69	12.09	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.47	1.19	2.38	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.27	0.52	0.82	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.17	ns/pF
Δt_{PHL}				0.11	0.21	0.36	
Δt_{PZH}	GZ	Y1		0.03	0.08	0.17	ns/pF
Δt_{PZL}				0.03	0.08	0.17	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

$C_L = 15$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.83	4.33	8.37	ns
t_{PHL}				2.28	5.02	9.61	
t_{PZH}	GZ	Y1	$R_L = 1$ kΩ to GND	1.94	4.68	9.12	ns
t_{PZL}			$R_L = 1$ kΩ to V_{CC}	1.94	4.68	9.12	

$C_L = 50$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	4.15	9.82	18.85	ns
t_{PHL}				4.73	9.9	18.31	
t_{PZH}	GZ	Y1	$R_L = 1$ kΩ to GND	4.26	10.18	19.6	ns
t_{PZL}			$R_L = 1$ kΩ to V_{CC}	4.26	10.18	19.6	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.07	0.16	0.3	ns/pF
Δt_{PHL}				0.07	0.14	0.25	
Δt_{PZH}	GZ	Y1		0.07	0.16	0.3	ns/pF
Δt_{PZL}				0.07	0.16	0.3	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.96	1.16	1.7	ns
t_{PHL}				0.31	0.8	1.39	
Δt_{PLH}	Y1	Y2		0.1	0.19	0.36	ns/pF
Δt_{PHL}				0.08	0.14	0.25	

†Typical values are at $V_{CC} = 5$ V, $T_A = 25\,°C$.

IOU24LJ
2-mA 3-STATE I/O BUFFER WITH 70-μA PULL-DOWN, TTL INPUT, AND CMOS/TTL OUTPUT

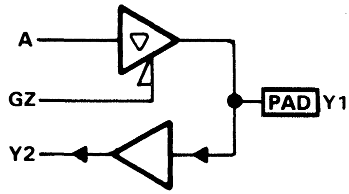
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOU24LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. A 70-μA pull-down current source terminates the output pad to GND. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOU24LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		$I_{OH} = -2$ mA	3.7			V
			$I_{OH} = -20$ μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 2$ mA			0.5	V
			$I_{OL} = 20$ μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$		70		μA
			$V_O = 0$			±10	
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		17.2		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.03	2.57	5.35	ns
t_{PHL}				3.13	6.67	12.29	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.03	2.93	6.22	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.03	2.93	6.22	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.99	5.33	11.22	ns
t_{PHL}				6.98	14.09	25.03	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2	5.68	12.09	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2	5.68	12.09	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.47	1.19	2.38	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.27	0.52	0.82	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.17	ns/pF
Δt_{PHL}				0.11	0.21	0.36	
Δt_{PZH}	GZ	Y1		0.03	0.08	0.17	ns/pF
Δt_{PZL}				0.03	0.08	0.17	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.99	1.68	2.45	ns
t_{PHL}				0.16	1.37	3.3	
Δt_{PLH}	Y1	Y2		0.09	0.19	0.38	ns/pF
Δt_{PHL}				0.08	0.29	0.67	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.84	4.34	8.4	ns
t_{PHL}				2.28	5	9.59	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.95	4.7	9.15	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.95	4.7	9.15	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	4.16	9.85	18.9	ns
t_{PHL}				4.72	9.89	18.29	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.27	10.21	19.65	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.27	10.21	19.65	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.07	0.16	0.3	ns/pF
Δt_{PHL}				0.07	0.14	0.25	
Δt_{PZH}	GZ	Y1		0.07	0.16	0.3	ns/pF
Δt_{PZL}				0.07	0.16	0.3	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOU41LJ
4-mA 3-STATE I/O BUFFER WITH 70-μA PULL-DOWN, CMOS INPUT, AND CMOS/TTL OUTPUT

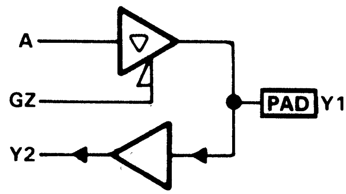
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOU41LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. A 70-μA pull-down current source terminates the output pad to GND. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOU41LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		I_{OH} = −4 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$		70		μA
			$V_O = 0$			±10	
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		16.5		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.8	1.99	4.15	ns
t_{PHL}				2.06	4.79	9.29	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.81	2.35	5.03	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.81	2.35	5.03	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.29	3.38	7.14	ns
t_{PHL}				4.01	8.61	15.92	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.3	3.75	8.02	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.3	3.75	8.02	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.62	1.66	3.39	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.3	0.62	0.98	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.04	0.09	ns/pF
Δt_{PHL}				0.06	0.11	0.19	
Δt_{PZH}	GZ	Y1		0.01	0.04	0.09	ns/pF
Δt_{PZL}				0.01	0.04	0.09	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.19	2.89	5.75	ns
t_{PHL}				1.61	3.84	7.69	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.3	3.25	6.52	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.3	3.25	6.52	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.35	5.65	11.01	ns
t_{PHL}				2.88	6.44	12.39	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.47	6.01	11.77	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.47	6.01	11.77	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.15	ns/pF
Δt_{PHL}				0.04	0.07	0.13	
Δt_{PZH}	GZ	Y1		0.03	0.08	0.15	ns/pF
Δt_{PZL}				0.03	0.08	0.15	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.76	1.15	1.7	ns
t_{PHL}				0.31	0.8	1.39	
Δt_{PLH}	Y1	Y2		0.1	0.19	0.36	ns/pF
Δt_{PHL}				0.08	0.14	0.25	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

4-mA 3-STATE I/O BUFFER WITH 70-μA PULL-DOWN, TTL INPUT, AND CMOS/TTL OUTPUT

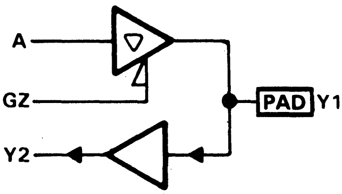
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOU44LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. A 70-μA pull-down current source terminates the output pad to GND. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOU44LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		I_{OH} = −4 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$		70		μA
			V_O = 0			±10	
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		17.3		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.8	1.99	4.15	ns
t_{PHL}				2.05	4.77	9.26	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.81	2.35	5.03	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.81	2.35	5.03	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.29	3.38	7.14	ns
t_{PHL}				4	8.59	15.88	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.3	3.74	8.01	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.3	3.74	8.01	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.62	1.66	3.39	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.3	0.62	0.98	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.04	0.09	ns/pF
Δt_{PHL}				0.06	0.11	0.19	
Δt_{PZH}	GZ	Y1		0.01	0.04	0.09	ns/pF
Δt_{PZL}				0.01	0.04	0.09	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.99	1.68	2.45	ns
t_{PHL}				0.15	1.36	3.25	
Δt_{PLH}	Y1	Y2		0.09	0.19	0.38	ns/pF
Δt_{PHL}				0.09	0.26	0.67	

†Typical values are at V_{CC} = 5 V, T_A = 25 °C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.19	2.89	5.75	ns
t_{PHL}				1.61	3.83	7.68	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.3	3.25	6.52	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.3	3.25	6.52	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.35	5.66	11.02	ns
t_{PHL}				2.87	6.43	12.38	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.47	6.02	11.78	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.47	6.02	11.78	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.15	ns/pF
Δt_{PHL}				0.04	0.07	0.13	
Δt_{PZH}	GZ	Y1		0.03	0.08	0.15	ns/pF
Δt_{PZL}				0.03	0.08	0.15	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOU81LJ
8-mA 3-STATE I/O BUFFER WITH 70-μA PULL-DOWN, CMOS INPUT, AND CMOS/TTL OUTPUT

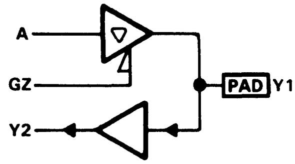
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOU81LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. A 70-μA pull-down current source terminates the output pad to GND. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOU81LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		I_{OH} = −8 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	V_{CC} − 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 8 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		V_O = V_{CC}		70		μA
			V_O = 0			±10	
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		18.2		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.75	1.97	4.23	ns
t_{PHL}				1.64	4.26	8.72	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.75	2.33	5.11	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.75	2.33	5.11	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.05	2.83	6.07	ns
t_{PHL}				2.71	6.52	12.8	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.05	3.2	6.96	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.05	3.2	6.96	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.9	2.63	5.53	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.42	0.76	1.32	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.02	0.05	ns/pF
Δt_{PHL}				0.03	0.06	0.12	
Δt_{PZH}	GZ	Y1		0.01	0.02	0.05	ns/pF
Δt_{PZL}				0.01	0.02	0.05	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.99	2.57	5.3	ns
t_{PHL}				1.34	3.58	7.53	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.1	2.93	6.08	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.1	2.93	6.08	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.58	4.05	8.19	ns
t_{PHL}				2.1	5.25	10.67	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.7	4.41	8.97	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.7	4.41	8.97	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.04	0.08	ns/pF
Δt_{PHL}				0.02	0.05	0.09	
Δt_{PZH}	GZ	Y1		0.02	0.04	0.08	ns/pF
Δt_{PZL}				0.02	0.04	0.08	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.76	1.15	1.7	ns
t_{PHL}				0.31	0.8	1.39	
Δt_{PLH}	Y1	Y2		0.1	0.19	0.36	ns/pF
Δt_{PHL}				0.08	0.14	0.25	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

8-mA 3-STATE I/O BUFFER WITH 70-μA PULL-DOWN, TTL INPUT, AND CMOS/TTL OUTPUT

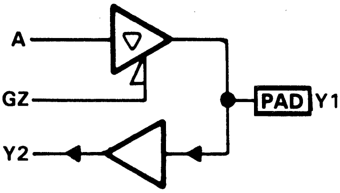
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOU84LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. A 70-μA pull-down current source terminates the output pad to GND. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the internal output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOU84LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		$I_{OH} = -8$ mA	3.7			V
			$I_{OH} = -20$ μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 8$ mA			0.5	V
			$I_{OL} = 20$ μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$		70		μA
			$V_O = 0$			±10	
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		19.1		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.75	1.97	4.23	ns
t_{PHL}				1.64	4.25	8.71	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.75	2.33	5.11	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.75	2.33	5.11	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.05	2.83	6.07	ns
t_{PHL}				2.71	6.51	12.78	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.05	3.19	6.96	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.05	3.19	6.96	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.9	2.63	5.53	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.42	0.76	1.32	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.02	0.05	ns/pF
Δt_{PHL}				0.03	0.06	0.12	
Δt_{PZH}	GZ	Y1		0.01	0.02	0.05	ns/pF
Δt_{PZL}				0.01	0.02	0.05	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.99	1.68	2.45	ns
t_{PHL}				0.15	1.33	3.15	
Δt_{PLH}	Y1	Y2		0.09	0.19	0.38	ns/pF
Δt_{PHL}				0.09	0.29	0.67	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.99	2.57	5.3	ns
t_{PHL}				1.34	3.58	7.52	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.1	2.93	6.08	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.1	2.93	6.08	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.59	4.05	8.19	ns
t_{PHL}				2.09	5.24	10.66	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.7	4.41	8.97	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.7	4.41	8.97	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.04	0.08	ns/pF
Δt_{PHL}				0.02	0.05	0.09	
Δt_{PZH}	GZ	Y1		0.02	0.04	0.08	ns/pF
Δt_{PZL}				0.02	0.04	0.08	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

2-mA 3-STATE I/O BUFFER WITH 70-μA PULL-DOWN, CMOS INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

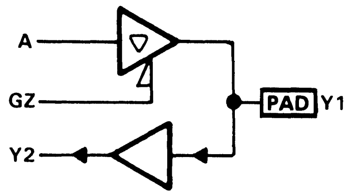
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOW21LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. A 70-μA pull-down current source terminates the output pad to GND. The input buffer responds to CMOS threshold levels on the I/O bus regardless of the state of the internal output enable GZ. When called, the following label format is developed and captured in the design netlist:

Label: IOW21LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		$I_{OH} = -2$ mA	3.7			V
			$I_{OH} = -20$ μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 2$ mA			0.5	V
			$I_{OL} = 20$ μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$		70		μA
			$V_O = 0$			±10	
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		16		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.33	3.44	7.26	ns
t_{PHL}				4.49	9.75	18.16	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.39	3.81	8.05	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.39	3.81	8.05	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.31	6.23	13.16	ns
t_{PHL}				8.41	17.37	31.32	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.37	6.59	13.96	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.37	6.59	13.96	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.52	1.32	2.59	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.27	0.55	0.88	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.17	ns/pF
Δt_{PHL}				0.11	0.22	0.38	
Δt_{PZH}	GZ	Y1		0.03	0.08	0.17	ns/pF
Δt_{PZL}				0.03	0.08	0.17	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.16	5.24	10.33	ns
t_{PHL}				3.49	7.84	15.06	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.32	5.6	11.01	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.32	5.6	11.01	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	4.48	10.74	20.82	ns
t_{PHL}				6.09	13.06	24.38	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.64	11.1	21.5	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.64	11.1	21.5	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.07	0.16	0.3	ns/pF
Δt_{PHL}				0.07	0.15	0.27	
Δt_{PZH}	GZ	Y1		0.07	0.16	0.3	ns/pF
Δt_{PZL}				0.07	0.16	0.3	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.77	1.16	1.71	ns
t_{PHL}				0.31	0.8	1.39	
Δt_{PLH}	Y1	Y2		0.1	0.19	0.36	ns/pF
Δt_{PHL}				0.08	0.14	0.25	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

TGC100 SERIES

IOW24LJ
2-mA 3-STATE I/O BUFFER WITH 70-μA PULL-DOWN, TTL INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

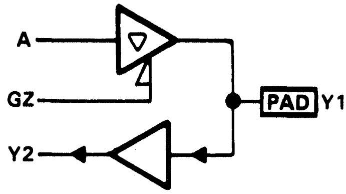
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOW24LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. A 70-μA pull-down current source terminates the output pad to GND. The input buffer responds to TTL threshold levels on the I/O bus regardless of the state of the internal output enable GZ. When called, the following label format is developed and captured in the design netlist:

Label: IOW24LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		$I_{OH} = -2$ mA	3.7			V
			$I_{OH} = -20$ μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 2$ mA			0.5	V
			$I_{OL} = 20$ μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$		70		μA
			$V_O = 0$			±10	
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		17.8		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.33	3.44	7.25	ns
t_{PHL}				4.47	9.71	18.08	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.39	3.81	8.04	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.39	3.81	8.04	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.31	6.22	13.16	ns
t_{PHL}				8.4	17.34	31.24	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.37	6.59	13.96	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.37	6.59	13.96	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.52	1.32	2.59	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.27	0.55	0.88	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.17	ns/pF
Δt_{PHL}				0.11	0.22	0.38	
Δt_{PZH}	GZ	Y1		0.03	0.08	0.17	ns/pF
Δt_{PZL}				0.03	0.08	0.17	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.99	1.68	2.47	ns
t_{PHL}				0.16	1.38	3.32	
Δt_{PLH}	Y1	Y2		0.09	0.19	0.37	ns/pF
Δt_{PHL}				0.08	0.29	0.67	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.17	5.25	10.36	ns
t_{PHL}				3.48	7.82	15.03	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.33	5.61	11.04	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.33	5.61	11.04	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	4.49	10.77	20.87	ns
t_{PHL}				6.09	13.04	24.35	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.65	11.13	21.55	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.65	11.13	21.55	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.07	0.16	0.3	ns/pF
Δt_{PHL}				0.07	0.15	0.27	
Δt_{PZH}	GZ	Y1		0.07	0.16	0.3	ns/pF
Δt_{PZL}				0.07	0.16	0.3	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOW41LJ
4-mA 3-STATE I/O BUFFER WITH 70-μA PULL-DOWN, CMOS INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

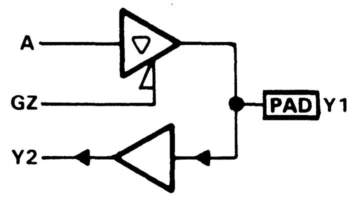
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOW41LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. A 70-μA pull-down current source terminates the output pad to GND. The input buffer responds to CMOS threshold levels on the I/O bus regardless of the state of the internal output enable GZ. When called, the following label format is developed and captured in the design netlist:

Label: IOW41LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		$I_{OH} = -4$ mA	3.7			V
			$I_{OH} = -20$ μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 4$ mA			0.5	V
			$I_{OL} = 20$ μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$		70		μA
			$V_O = 0$			±10	
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		17.4		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

$C_L = 15$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.14	3.06	6.56	ns
t_{PHL}				3.46	8.03	15.48	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.2	3.43	7.34	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.2	3.43	7.34	

$C_L = 50$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.72	4.65	9.90	ns
t_{PHL}				5.69	12.43	23.16	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.79	5.02	10.69	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.79	5.02	10.69	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.65	1.77	3.63	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.32	0.64	1	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.05	0.1	ns/pF
Δt_{PHL}				0.06	0.13	0.22	
Δt_{PZH}	GZ	Y1		0.02	0.05	0.1	ns/pF
Δt_{PZL}				0.02	0.05	0.1	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

D3015, OCTOBER 1987

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.63	4.13	8.40	ns
t_{PHL}				2.80	6.73	13.37	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.8	4.5	9.09	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.8	4.5	9.09	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.83	6.99	13.89	ns
t_{PHL}				4.39	9.98	19.2	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3	7.36	14.57	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3	7.36	14.57	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.16	ns/pF
Δt_{PHL}				0.05	0.09	0.17	
Δt_{PZH}	GZ	Y1		0.03	0.08	0.16	ns/pF
Δt_{PZL}				0.03	0.08	0.16	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.77	1.16	1.71	ns
t_{PHL}				0.39	0.8	1.39	
Δt_{PLH}	Y1	Y2		0.1	0.19	0.36	ns/pF
Δt_{PHL}				0.08	0.14	0.25	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

4-mA 3-STATE I/O BUFFER WITH 70-μA PULL-DOWN, TTL INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

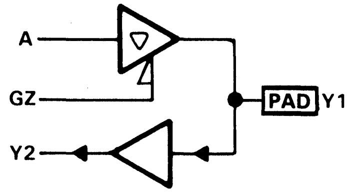
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOW44LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. A 70-μA pull-down current source terminates the output pad to GND. The input buffer responds to TTL threshold levels on the I/O bus regardless of the state of the internal output enable GZ. When called, the following label format is developed and captured in the design netlist:

Label: IOW44LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		I_{OH} = −4 mA	3.7			V
			I_{OH} = −20 μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.5	V
			I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$		70		μA
			$V_O = 0$			±10	
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		17.7		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TEXAS INSTRUMENTS

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.14	3.05	6.55	ns
t_{PHL}				3.45	8.01	15.44	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.2	3.43	7.34	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.2	3.43	7.34	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.72	4.64	9.89	ns
t_{PHL}				5.68	12.41	23.12	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.79	5.02	10.69	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.79	5.02	10.69	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.65	1.77	3.63	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.32	0.64	1	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.05	0.1	ns/pF
Δt_{PHL}				0.06	0.13	0.22	
Δt_{PZH}	GZ	Y1		0.02	0.05	0.1	ns/pF
Δt_{PZL}				0.02	0.05	0.1	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.99	1.68	2.47	ns
t_{PHL}				0.15	1.37	3.28	
Δt_{PLH}	Y1	Y2		0.09	0.19	0.37	ns/pF
Δt_{PHL}				0.09	0.29	0.66	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.63	4.13	8.41	ns
t_{PHL}				2.8	6.73	13.36	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.8	4.5	9.09	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.8	4.5	9.09	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.84	7	13.9	ns
t_{PHL}				4.39	9.97	19.19	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.01	7.37	14.58	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.01	1.37	14.58	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.03	0.08	0.16	ns/pF
Δt_{PHL}				0.05	0.09	0.17	
Δt_{PZH}	GZ	Y1		0.03	0.08	0.16	ns/pF
Δt_{PZL}				0.03	0.08	0.16	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

8-mA 3-STATE I/O BUFFER WITH 70-μA PULL-DOWN, CMOS INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

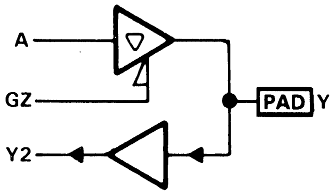
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOW81LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. A 70-μA pull-down current source terminates the output pad to GND. The input buffer responds to CMOS threshold levels on the I/O bus regardless of the state of the internal output enable GZ. When called, the following label format is developed and captured in the design netlist:

Label: IOW81LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			2.5		
V_{OH}	High-level output voltage		$I_{OH} = -8$ mA	3.7			V
			$I_{OH} = -20$ μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 8$ mA			0.5	V
			$I_{OL} = 20$ μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$		70		μA
			$V_O = 0$			±10	
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		19.8		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.12	3.3	7.29	ns
t_{PHL}				3.16	7.93	15.89	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.2	3.67	8.06	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.2	3.67	8.06	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.58	4.51	9.8	ns
t_{PHL}				4.69	11.04	21.43	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.66	4.89	10.59	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.66	4.89	10.59	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.94	2.75	5.75	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.42	0.79	1.38	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.03	0.07	ns/pF
Δt_{PHL}				0.04	0.09	0.16	
Δt_{PZH}	GZ	Y1		0.01	0.03	0.07	ns/pF
Δt_{PZL}				0.01	0.03	0.07	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.52	4.18	8.82	ns
t_{PHL}				2.59	6.81	14.04	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.71	4.56	9.49	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.71	4.56	9.49	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.3	6.03	12.39	ns
t_{PHL}				3.76	9.26	18.54	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.49	6.41	13.07	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.49	6.41	13.07	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.05	0.1	ns/pF
Δt_{PHL}				0.03	0.07	0.13	
Δt_{PZH}	GZ	Y1		0.02	0.05	0.1	ns/pF
Δt_{PZL}				0.02	0.05	0.1	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.86	1.16	1.71	ns
t_{PHL}				0.39	0.8	1.39	
Δt_{PLH}	Y1	Y2		0.1	0.19	0.36	ns/pF
Δt_{PHL}				0.08	0.14	0.25	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOW84LJ
8-mA 3-STATE I/O BUFFER WITH 70-μA PULL-DOWN, TTL INPUT, CMOS/TTL OUTPUT, AND di/dt CONTROL

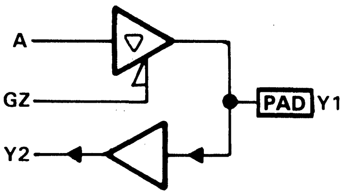
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL BIDIRECTIONAL I/O MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L), Y2 = Y1

description

The IOW84LJ is a 3-state input/output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. A 70-μA pull-down current source terminates the output pad to GND. The input buffer responds to TTL threshold levels on the I/O bus regardless of the state of the internal output enable GZ. When called, the following label format is developed and captured in the design netlist:

Label: IOW84LJ A,GZ,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage	A,GZ			2.2		V
		Y1			1.3		
V_{OH}	High-level output voltage		$I_{OH} = -8$ mA	3.7			V
			$I_{OH} = -20$ μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 8$ mA			0.5	V
			$I_{OL} = 20$ μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$		70		μA
			$V_O = 0$			±10	
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
		Y1¶			7.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		19		pF

‡, §, ¶, and NOTE 1: For notes in this section, see "Bidirectional Input/Output Buffers General Information".

TEXAS INSTRUMENTS

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.13	3.3	7.29	ns
t_{PHL}				3.15	7.92	15.86	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.2	3.67	8.06	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.2	3.67	8.06	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.58	4.51	9.8	ns
t_{PHL}				4.68	11.03	21.41	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.66	4.88	10.59	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.66	4.88	10.59	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND	0.94	2.75	5.75	ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}	0.42	0.79	1.39	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.01	0.03	0.07	ns/pF
Δt_{PHL}				0.04	0.09	0.16	
Δt_{PZH}	GZ	Y1		0.01	0.03	0.07	ns/pF
Δt_{PZL}				0.01	0.03	0.07	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Y1	Y2		0.99	1.68	2.47	ns
t_{PHL}				0.24	1.33	3.17	
Δt_{PLH}	Y1	Y2		0.09	0.19	0.37	ns/pF
Δt_{PHL}				0.09	0.29	0.67	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.52	4.18	8.81	ns
t_{PHL}				2.59	6.8	14.02	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.71	4.56	9.49	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.71	4.56	9.49	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.3	6.03	12.39	ns
t_{PHL}				3.76	9.26	18.54	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.49	6.41	13.08	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.49	6.41	13.08	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y1		0.02	0.05	0.1	ns/pF
Δt_{PHL}				0.03	0.07	0.13	
Δt_{PZH}	GZ	Y1		0.02	0.05	0.1	ns/pF
Δt_{PZL}				0.02	0.05	0.1	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

D3015, OCTOBER 1987

EXTERNAL OUTPUT MACRO

The TGC100 Series CMOS gate array library provides the custom IC designer a wide selection of output buffers featuring CMOS-/TTL-compatible outputs. Each output is characterized for driving either CMOS loads or TTL loads. Additionally, for each output offered, the designer can select from outputs minimizing delay time or from outputs incorporating di/dt circuitry designed to reduce the effects of impedance mismatch.

TGC100 Series output buffers are designed to actively bypass electrostatic discharges. Guard-ring structures are employed that provide current-management techniques for the output to recover from exposure to high currents of up to 400 mA, thereby negating most common sources that can produce a latch-up condition.

These output buffers are designed to provide low-impedance drive levels for both the high- and low-logic level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

The dynamic-drive capability of the outputs is specified by the change in propagation delay time parameters included with the switching characteristics. The change in propagation delay times provides a means for making direct comparisons of the various output responses to changes in capacitive loading.

D3015, OCTOBER 1987—REVISED OCTOBER 1988

MACRO SELECTION TABLE

TYPE OF OUTPUT	OUTPUT CURRENT (SINK AND SOURCE) (mA)	di/dt CIRCUITRY	MACRO NAME	PAGE NUMBERS
TOTEM-POLE	2/2	NO	OPI20LJ	13-9
TOTEM-POLE	4/4	NO	OPI40LJ	13-18
TOTEM-POLE	8/8	NO	OPI80LJ	13-27
TOTEM-POLE	12/12	NO	OPIH0LJ	13-5
TOTEM-POLE	16/12	NO	OPIA0LJ	13-3
TOTEM-POLE	20/12	NO	OPIJ0LJ	13-7
TOTEM-POLE	2/2	YES	OPK20LJ	13-42
TOTEM-POLE	4/4	YES	OPK40LJ	13-51
TOTEM-POLE	8/8	YES	OPK80LJ	13-60
TOTEM-POLE	12/12	YES	OPKH0LJ	13-38
TOTEM-POLE	16/12	YES	OPKA0LJ	13-36
TOTEM-POLE	20/12	YES	OPKJ0LJ	13-40
N-CHANNEL OPEN-DRAIN	2 (SINK)	NO	OPI21LJ	13-11
N-CHANNEL OPEN-DRAIN	4 (SINK)	NO	OPI41LJ	13-20
N-CHANNEL OPEN-DRAIN	8 (SINK)	NO	OPI81LJ	13-29
N-CHANNEL OPEN-DRAIN	2 (SINK)	YES	OPK21LJ	13-44
N-CHANNEL OPEN-DRAIN	4 (SINK)	YES	OPK41LJ	13-53
N-CHANNEL OPEN-DRAIN	8 (SINK)	YES	OPK81LJ	13-62
3-STATE	2/2	NO	OPI23LJ	13-13
3-STATE	4/4	NO	OPI43LJ	13-22
3-STATE	8/8	NO	OPI83LJ	13-31
3-STATE	2/2	YES	OPK23LJ	13-46
3-STATE	4/4	YES	OPK43LJ	13-55
3-STATE	8/8	YES	OPK83LJ	13-64
P-CHANNEL OPEN-DRAIN	2 (SOURCE)	NO	OPI24LJ	13-16
P-CHANNEL OPEN-DRAIN	4 (SOURCE)	NO	OPI44LJ	13-25
P-CHANNEL OPEN-DRAIN	8 (SOURCE)	NO	OPI84LJ	13-34
P-CHANNEL OPEN-DRAIN	2 (SOURCE)	YES	OPK24LJ	13-49
P-CHANNEL OPEN-DRAIN	4 (SOURCE)	YES	OPK44LJ	13-58
P-CHANNEL OPEN-DRAIN	8 (SOURCE)	YES	OPK84LJ	13-67

OPIA0LJ
16-mA CMOS/TTL OUTPUT BUFFER

D3015, OCTOBER 1988

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPIA0LJ is a totem-pole output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPIA0LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	$I_{OH} = -12$ mA	3.7			V
		$I_{OH} = -20$ µA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage	$I_{OL} = 16$ mA			0.5	V
		$I_{OL} = 20$ µA, See Note 1			0.1	
C_i	Input capacitance			0.41		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		13		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.
§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
NOTE 1: These limits apply when all other external outputs are open.

TEXAS INSTRUMENTS
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, R_L = ∞	0.61	1.23	2.3	ns
t_{PHL}				0.87	2.07	4	
t_{PLH}	A	Y	C_L = 50 pF, R_L = ∞	0.8	1.74	3.39	ns
t_{PHL}				1.38	3.12	5.9	
Δt_{PLH}	A	Y		10	10	30	ps/pF
Δt_{PHL}				10	30	50	

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, R_L = ∞	0.73	1.56	2.92	ns
t_{PHL}				0.77	1.76	3.45	
t_{PLH}	A	Y	C_L = 50 pF, R_L = ∞	1.12	2.5	4.73	ns
t_{PHL}				1.12	2.52	4.87	
Δt_{PLH}	A	Y		10	30	50	ps/pF
Δt_{PHL}				10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

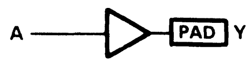
D3015, OCTOBER 1988

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPIH0LJ is a totem-pole output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPIH0LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	$I_{OH} = -12$ mA	3.7			V
		$I_{OH} = -20$ µA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage	$I_{OL} = 12$ mA			0.5	V
		$I_{OL} = 20$ µA, See Note 1			0.1	
C_i	Input capacitance			0.41		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		12.9		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.
§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
NOTE 1: These limits apply when all other external outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$C_L = 15$ pF, $R_L = \infty$	0.61	1.23	2.3	ns
t_{PHL}				0.93	2.12	4.02	
t_{PLH}	A	Y	$C_L = 50$ pF, $R_L = \infty$	0.8	1.74	3.38	ns
t_{PHL}				1.57	3.4	6.27	
Δt_{PLH}	A	Y		10	10	30	ps/pF
Δt_{PHL}				20	40	60	

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$C_L = 15$ pF, $R_L = \infty$	0.73	1.56	2.91	ns
t_{PHL}				0.81	1.78	3.42	
t_{PLH}	A	Y	$C_L = 50$ pF, $R_L = \infty$	1.12	2.5	4.72	ns
t_{PHL}				1.23	2.67	5.05	
Δt_{PLH}	A	Y		10	30	50	ps/pF
Δt_{PHL}				10	30	50	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

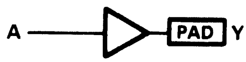
D3015, OCTOBER 1988

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPIJ0LJ is a totem-pole output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPIJ0LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	$I_{OH} = -12$ mA	3.7			V
		$I_{OH} = -20\ \mu A$, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage	$I_{OL} = 20$ mA			0.5	V
		$I_{OL} = 20\ \mu A$, See Note 1			0.1	
C_i	Input capacitance			0.41		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		13.2		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.
§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
NOTE 1: These limits apply when all other external outputs are open.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, $R_L = \infty$	0.62	1.23	2.31	ns
t_{PHL}				0.86	2.1	4.13	
t_{PLH}	A	Y	C_L = 50 pF, $R_L = \infty$	0.8	1.75	3.4	ns
t_{PHL}				1.3	2.97	5.7	
Δt_{PLH}	A	Y		10	10	30	ps/pF
Δt_{PHL}				10	20	40	

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, $R_L = \infty$	0.73	1.57	2.92	ns
t_{PHL}				0.76	1.8	3.6	
t_{PLH}	A	Y	C_L = 50 pF, $R_L = \infty$	1.12	2.51	4.73	ns
t_{PHL}				1.08	2.32	4.8	
Δt_{PLH}	A	Y		10	30	50	ps/pF
Δt_{PHL}				10	10	30	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI20LJ
2-mA CMOS/TTL OUTPUT BUFFER

D3015, OCTOBER 1987–REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI20LJ is a totem-pole output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI20LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −2 mA	3.7			V
		I_{OH} = −20 μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.5	V
		I_{OL} = 20 μA, See Note 1			0.1	
C_i	Input capacitance			0.23		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		7.36		pF

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These limits apply when all other external outputs are open.

TEXAS INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, R_L = ∞	0.95	2.27	4.55	ns
t_{PHL}				2.77	5.55	9.8	
t_{PLH}	A	Y	C_L = 50 pF, R_L = ∞	1.91	5.01	10.39	ns
t_{PHL}				6.63	13.01	22.52	
Δt_{PLH}	A	Y		30	80	170	ps/pF
Δt_{PHL}				110	210	360	

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, R_L = ∞	1.71	3.91	7.38	ns
t_{PHL}				1.97	4.01	7.28	
t_{PLH}	A	Y	C_L = 50 pF, R_L = ∞	4.01	9.38	17.8	ns
t_{PHL}				4.42	8.9	15.93	
Δt_{PLH}	A	Y		70	160	300	ps/pF
Δt_{PHL}				70	140	250	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI21LJ
2-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER

D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	Z
L	L

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI21LJ is an N-channel open-drain output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI21LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.5	V
		I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			10	μA
C_i	Input capacitance			0.14		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		0.5		pF

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These limits apply when all other external outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}	2.69	5.74	10.99	ns
t_{PZL}			C_L = 50 pF, R_L = 1 kΩ to V_{CC}	6.74	14.19	27.02	
t_{PLZ}	A	Y	R_L = 1 kΩ to V_{CC}		0.5		
Δt_{PZL}				120	240	460	ps/pF

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}	1.88	3.95	7.51	ns
t_{PZL}			C_L = 50 pF, R_L = 1 kΩ to V_{CC}	4.4	9.22	17.49	
Δt_{PZL}	A	Y		70	150	290	ps/pF

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI23LJ
2-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

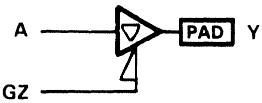
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPI23LJ is a 3-state output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI23LJ A,GZ,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage				2.2		V
V_{OH}	High-level output voltage		$I_{OH} = -2$ mA	3.7			V
			$I_{OH} = -20$ μA, See Note 1	$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 2$ mA			0.5	V
			$I_{OL} = 20$ μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		7.34		pF

‡Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NOTE 1: These limits apply when all other external outputs are open.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	1.01	2.49	5.16	ns
t_{PHL}				3.03	6.51	12.02	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1	2.92	6.37	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.19	7.15	14.05	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	1.96	5.23	11.01	ns
t_{PHL}				6.9	13.97	24.84	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.95	5.78	12.73	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	7.25	15.59	30.03	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		1.15		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		0.48		

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y		30	80	170	ps/pF
Δt_{PHL}				110	210	370	
Δt_{PZH}	GZ	Y		30	80	180	ps/pF
Δt_{PZL}				120	240	460	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

$C_L = 15$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	1.76	4.14	8	ns
t_{PHL}				2.22	4.91	9.41	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.89	4.81	9.93	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.3	5.17	10.2	

$C_L = 50$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	4.07	9.61	18.43	ns
t_{PHL}				4.67	9.83	18.18	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	4.22	10.79	22.27	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.82	10.46	20.17	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y		70	160	300	ps/pF
Δt_{PHL}				70	140	250	
Δt_{PZH}	GZ	Y		70	170	350	ps/pF
Δt_{PZL}				70	150	280	

†Typical values are at V_{CC} = 5 V, TA = 25°C.

TEXAS INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPI24LJ
2-mA P-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER

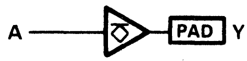
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI24LJ is a P-channel open-drain output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI24LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	$I_{OH} = -2$ mA	3.7			V
		$I_{OH} = -20$ μA, See Note 1	$V_{CC}-0.1$			
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			−10	μA
C_i	Input capacitance			0.14		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		0.62		pF

‡Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NOTE 1: These limits apply when all other external outputs are open.

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZH}	A	Y	C_L = 15 pF, R_L = 1 kΩ to GND	0.93	2.27	4.7	ns
t_{PZH}			C_L = 50 pF, R_L = 1 kΩ to GND	1.81	4.96	10.78	
t_{PHZ}	A	Y	R_L = 1 kΩ to GND		0.9		
Δt_{PZH}				30	80	170	ps/pF

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZH}	A	Y	C_L = 15 pF, R_L = 1 kΩ to GND	1.69	4.1	8.26	ns
t_{PZH}			C_L = 50 pF, R_L = 1 kΩ to GND	3.95	9.91	20.32	
Δt_{PZH}	A	Y		60	170	340	ps/pF

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI40LJ
4-mA CMOS/TTL OUTPUT BUFFER

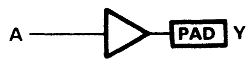
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI40LJ is a totem-pole output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI40LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA	3.7			V
		$I_{OH} = -20\ \mu A$, See Note 1	$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA			0.5	V
		$I_{OL} = 20\ \mu A$, See Note 1			0.1	
C_i	Input capacitance			0.41		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		8.51		pF

‡Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NOTE 1: These limits apply when all other external outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$C_L = 15$ pF, $R_L = \infty$	0.65	1.42	2.73	ns
t_{PHL}				1.56	3.14	5.58	
t_{PLH}	A	Y	$C_L = 50$ pF, $R_L = \infty$	1.13	2.79	5.65	ns
t_{PHL}				3.49	6.87	11.98	
Δt_{PLH}	A	Y		10	40	80	ps/pF
Δt_{PHL}				60	110	180	

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$C_L = 15$ pF, $R_L = \infty$	1	2.24	4.17	ns
t_{PHL}				1.18	2.36	4.28	
t_{PLH}	A	Y	$C_L = 50$ pF, $R_L = \infty$	2.16	4.98	9.39	ns
t_{PHL}				2.41	4.81	8.64	
Δt_{PLH}	A	Y		30	80	150	ps/pF
Δt_{PHL}				40	70	120	

†Typical values are at $V_{CC} = 5$ V, $T_A = 25\,°C$.

OPI41LJ
4-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER

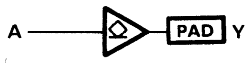
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	Z
L	L

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI41LJ is an N-channel open-drain output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI41LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.5	V
		I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			10	μA
C_i	Input capacitance			0.22		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		0.82		pF

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These limits apply when all other external outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}	1.48	3.07	5.62	ns
t_{PZL}			C_L = 50 pF, R_L = 1 kΩ to V_{CC}	3.45	7.02	12.69	
t_{PLZ}	A	Y	R_L = 1 kΩ to V_{CC}		0.39		
Δt_{PZL}				60	110	200	ps/pF

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}	1.11	2.26	4.17	ns
t_{PZL}			C_L = 50 pF, R_L = 1 kΩ to V_{CC}	2.36	4.8	8.81	
Δt_{PZL}	A	Y		40	70	130	ps/pF

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI43LJ 4-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

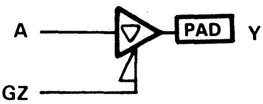
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPI43LJ is a 3-state output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI43LJ A,GZ,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage				2.2		V
V_{OH}	High-level output voltage		$I_{OH} = -4$ mA	3.7			V
			$I_{OH} = -20\ \mu A$, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 4$ mA			0.5	V
			$I_{OL} = 20\ \mu A$, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		7.95		pF

‡Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NOTE 1: These limits apply when all other external outputs are open.

TEXAS INSTRUMENTS

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	0.79	1.95	4.06	ns
t_{PHL}				2	4.68	9.1	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	0.79	2.33	5.04	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.07	4.87	9.6	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	1.28	3.34	7.03	ns
t_{PHL}				3.95	8.51	15.75	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.27	3.75	8.13	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.07	8.9	16.83	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		1.63		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		0.58		

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y		10	40	80	ps/pF
Δt_{PHL}				60	110	190	
Δt_{PZH}	GZ	Y		10	40	90	ps/pF
Δt_{PZL}				60	120	210	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

$C_L = 15$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	1.16	2.81	5.57	ns
t_{PHL}				1.57	3.77	7.56	
t_{PZH}	GZ	Y	$R_L = 1\ k\Omega$ to GND	1.27	3.25	6.63	ns
t_{PZL}			$R_L = 1\ k\Omega$ to V_{CC}	1.62	3.86	7.76	

$C_L = 50$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	2.32	5.55	10.8	ns
t_{PHL}				2.84	6.39	12.3	
t_{PZH}	GZ	Y	$R_L = 1\ k\Omega$ to GND	2.43	6.11	12.27	ns
t_{PZL}			$R_L = 1\ k\Omega$ to V_{CC}	2.91	6.55	12.73	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y		30	80	150	ps/pF
Δt_{PHL}				40	70	140	
Δt_{PZH}	GZ	Y		30	80	160	ps/pF
Δt_{PZL}				40	80	140	

†Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

OPI44LJ
4-mA P-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER

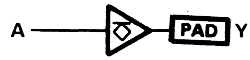
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI44LJ is a P-channel open-drain output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI44LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA	3.7			V
		$I_{OH} = -20$ μA, See Note 1	$V_{CC}-0.1$			
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			−10	μA
C_i	Input capacitance			0.24		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		1.16		pF

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These limits apply when all other external outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZH}	A	Y	C_L = 15 pF, R_L = 1 kΩ to GND	0.64	1.39	2.71	ns
t_{PZH}			C_L = 50 pF, R_L = 1 kΩ to GND	1.08	2.7	5.59	
t_{PHZ}	A	Y	R_L = 1 kΩ to GND		0.86		
Δt_{PZH}				10	40	80	ps/pF

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZH}	A	Y	C_L = 15 pF, R_L = 1 kΩ to GND	0.99	2.25	4.29	ns
t_{PZH}			C_L = 50 pF, R_L = 1 kΩ to GND	2.11	5.02	9.78	
Δt_{PZH}	A	Y		30	80	160	ps/pF

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI80LJ is a totem-pole output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI80LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −8 mA	3.7			V
		I_{OH} = −20 μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.5	V
		I_{OL} = 20 μA, See Note 1			0.1	
C_i	Input capacitance			0.41		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		10.5		pF

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These limits apply when all other external outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$C_L = 15$ pF, $R_L = \infty$	0.59	1.2	2.24	ns
t_{PHL}				1.06	2.3	4.26	
t_{PLH}	A	Y	$C_L = 50$ pF, $R_L = \infty$	0.84	1.89	3.72	ns
t_{PHL}				2.03	4.18	7.52	
Δt_{PLH}	A	Y		10	20	40	ps/pF
Δt_{PHL}				30	50	90	

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$C_L = 15$ pF, $R_L = \infty$	0.75	1.63	3.02	ns
t_{PHL}				0.88	1.86	3.5	
t_{PLH}	A	Y	$C_L = 50$ pF, $R_L = \infty$	1.33	3	5.64	ns
t_{PHL}				1.51	3.13	5.78	
Δt_{PLH}	A	Y		20	40	70	ps/pF
Δt_{PHL}				20	40	70	

†Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

OPI81LJ
8-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER

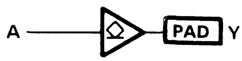
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	Z
L	L

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI81LJ is an N-channel open-drain output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI81LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.5	V
		I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			10	μA
C_i	Input capacitance			0.22		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		1.09		pF

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These limits apply when all other external outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZL}	A	Y	$C_L = 15$ pF, $R_L = 1$ kΩ to V_{CC}	1.02	2.21	4.14	ns
t_{PZL}			$C_L = 50$ pF, $R_L = 1$ kΩ to V_{CC}	2	4.15	7.56	
t_{PLZ}	A	Y	$R_L = 1$ kΩ to V_{CC}		0.53		
Δt_{PZL}				30	60	100	ps/pF

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZL}	A	Y	$C_L = 15$ pF, $R_L = 1$ kΩ to V_{CC}	0.84	1.77	3.35	ns
t_{PZL}			$C_L = 50$ pF, $R_L = 1$ kΩ to V_{CC}	1.47	3.07	5.72	
Δt_{PZL}	A	Y		20	40	70	ps/pF

†Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

OPI83LJ
8-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

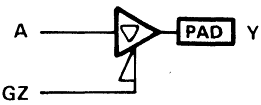
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPI83LJ is a 3-state output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI83LJ A,GZ,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage				2.2		V
V_{OH}	High-level output voltage		$I_{OH} = -8$ mA	3.7			V
			$I_{OH} = -20\ \mu A$, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 8$ mA			0.5	V
			$I_{OL} = 20\ \mu A$, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		10.1		pF

‡Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NOTE 1: These limits apply when all other external outputs are open.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

$C_L = 15$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	0.75	1.95	4.16	ns
t_{PHL}				1.6	4.19	8.59	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	0.74	2.32	5.1	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.64	4.27	8.78	

$C_L = 50$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	1.05	2.81	6.02	ns
t_{PHL}				2.67	6.46	12.7	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.04	3.19	6.98	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.73	6.59	12.98	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		2.6		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		0.75		

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y		10	20	50	ps/pF
Δt_{PHL}				30	60	120	
Δt_{PZH}	GZ	Y		10	20	50	ps/pF
Δt_{PZL}				30	70	120	

†Typical values are at V_{CC} = 5 V, T_A = 25 °C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	0.97	2.52	5.2	ns
t_{PHL}				1.31	3.53	7.43	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.08	2.92	6.1	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.34	3.56	7.47	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	1.57	4	8.09	ns
t_{PHL}				2.07	5.21	10.6	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.68	4.42	9.07	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.11	5.26	10.69	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y		20	40	80	ps/pF
Δt_{PHL}				20	50	90	
Δt_{PZH}	GZ	Y		20	40	80	ps/pF
Δt_{PZL}				20	50	90	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI84LJ
8-mA P-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER

D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	Z

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI84LJ is a P-channel open-drain output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI84LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	$I_{OH} = -8$ mA	3.7			V
		$I_{OH} = -20\ \mu A$, See Note 1	$V_{CC} - 0.1$			
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			−10	μA
C_i	Input capacitance			0.24		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		1.74		pF

‡Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
NOTE 1: These limits apply when all other external outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZH}	A	Y	C_L = 15 pF, R_L = 1 kΩ to GND	0.58	1.18	2.2	ns
t_{PZH}			C_L = 50 pF, R_L = 1 kΩ to GND	0.81	1.83	3.62	
t_{PHZ}	A	Y	R_L = 1 kΩ to GND		1.35		
Δt_{PZH}				10	20	40	ps/pF

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZH}	A	Y	C_L = 15 pF, R_L = 1 kΩ to GND	0.75	1.61	3.01	ns
t_{PZH}			C_L = 50 pF, R_L = 1 kΩ to GND	1.3	2.96	5.64	
Δt_{PZH}	A	Y		20	40	80	ps/pF

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKA0LJ
16-mA CMOS/TTL OUTPUT BUFFER WITH di/dt CONTROL

D3015, OCTOBER 1988

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPKA0LJ is a totem-pole output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. The buffer incorporates di/dt circuity designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPKA0LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	$I_{OH} = -12$ mA	3.7			V
		$I_{OH} = -20$ µA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage	$I_{OL} = 16$ mA			0.5	V
		$I_{OL} = 20$ µA, See Note 1			0.1	
C_i	Input capacitance			0.41		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		10.6		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.
§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
NOTE 1: These limits apply when all other external outputs are open.

TEXAS INSTRUMENTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, R_L = ∞	1.11	2.99	6.47	ns
t_{PHL}				2.74	6.57	13.06	
t_{PLH}	A	Y	C_L = 50 pF, R_L = ∞	1.51	4	8.5	ns
t_{PHL}				3.81	8.77	16.98	
Δt_{PLH}	A	Y		10	30	60	ps/pF
Δt_{PHL}				30	60	110	

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, R_L = ∞	1.45	3.73	7.7	ns
t_{PHL}				2.26	5.66	11.6	
t_{PLH}	A	Y	C_L = 50 pF, R_L = ∞	2.1	5.2	10.5	ns
t_{PHL}				3.11	7.46	14.88	
Δt_{PLH}	A	Y		20	40	80	ps/pF
Δt_{PHL}				20	50	90	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKH0LJ
12-mA CMOS/TTL OUTPUT BUFFER WITH di/dt CONTROL

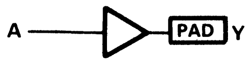
D3015, OCTOBER 1988

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPHA0LJ is a totem-pole output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. The buffer incorporates di/dt circuity designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPKHA0LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	$I_{OH} = -12$ mA	3.7			V
		$I_{OH} = -20$ µA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage	$I_{OL} = 12$ mA			0.5	V
		$I_{OL} = 20$ µA, See Note 1			0.1	
C_i	Input capacitance			0.41		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		10.3		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.
§ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
NOTE 1: These limits apply when all other external outputs are open.

OPKHOLJ
12-mA CMOS/TTL OUTPUT BUFFER WITH di/dt CONTROL

D3015, OCTOBER 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, $R_L = \infty$	1.11	2.99	6.44	ns
t_{PHL}				2.62	6.1	11.98	
t_{PLH}	A	Y	C_L = 50 pF, $R_L = \infty$	1.52	3.99	8.49	ns
t_{PHL}				3.79	8.43	16.09	
Δt_{PLH}	A	Y		10	30	60	ps/pF
Δt_{PHL}				30	70	120	

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, $R_L = \infty$	1.46	3.72	7.68	ns
t_{PHL}				2.18	5.24	10.6	
t_{PLH}	A	Y	C_L = 50 pF, $R_L = \infty$	2.1	5.19	10.49	ns
t_{PHL}				3.09	7.11	13.98	
Δt_{PLH}	A	Y		20	40	80	ps/pF
Δt_{PHL}				30	50	100	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKJ0LJ
20-mA CMOS/TTL OUTPUT BUFFER WITH di/dt CONTROL

D3015, OCTOBER 1988

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPKJ0LJ is a totem-pole output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. The buffer incorporates di/dt circuity designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPKJ0LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −12 mA	3.7			V
		I_{OH} = −20 μA, See Note 1	V_{CC}−0.1			
V_{OL}	Low-level output voltage	I_{OL} = 20 mA			0.5	V
		I_{OL} = 20 μA, See Note 1			0.1	
C_i	Input capacitance			0.41		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		10.9		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These limits apply when all other external outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, $R_L = \infty$	1.11	2.99	6.47	ns
t_{PHL}				2.96	7.24	14.5	
t_{PLH}	A	Y	C_L = 50 pF, $R_L = \infty$	1.52	4	8.52	ns
t_{PHL}				3.99	9.16	18.16	
Δt_{PLH}	A	Y		10	30	60	ps/pF
Δt_{PHL}				30	50	100	

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, $R_L = \infty$	1.46	3.73	7.71	ns
t_{PHL}				2.42	6.24	12.9	
t_{PLH}	A	Y	C_L = 50 pF, $R_L = \infty$	2.1	5.2	10.51	ns
t_{PHL}				3.25	7.8	15.86	
Δt_{PLH}	A	Y		20	40	80	ps/pF
Δt_{PHL}				20	40	80	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK20LJ
2-mA CMOS/TTL OUTPUT BUFFER WITH di/dt CONTROL

D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK20LJ is a totem-pole output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. The gates incorporate di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK20LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	$I_{OH} = -2$ mA	3.7			V
		$I_{OH} = -20\ \mu A$, See Note 1	$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage	$I_{OL} = 2$ mA			0.5	V
		$I_{OL} = 20\ \mu A$, See Note 1			0.1	
C_i	Input capacitance			0.23		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		7.44		pF

‡Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
NOTE 1: These limits apply when all other external outputs are open.

OPK20LJ
2-mA CMOS/TTL OUTPUT BUFFER WITH di/dt CONTROL

D3015, OCTOBER 1987

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, R_L = ∞	1.21	2.96	6.11	ns
t_{PHL}				3.99	8.24	14.95	
t_{PLH}	A	Y	C_L = 50 pF, R_L = ∞	2.18	5.71	11.98	ns
t_{PHL}				7.89	15.79	27.87	
Δt_{PLH}	A	Y		30	80	170	ps/pF
Δt_{PHL}				110	220	370	

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, R_L = ∞	1.98	4.63	8.98	ns
t_{PHL}				3.1	6.53	12.19	
t_{PLH}	A	Y	C_L = 50 pF, R_L = ∞	4.29	10.11	19.43	ns
t_{PHL}				5.64	11.62	21.18	
Δt_{PLH}	A	Y		70	160	300	ps/pF
Δt_{PHL}				70	150	260	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK21LJ
2-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH di/dt CONTROL

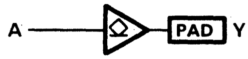
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	Z
L	L

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK21LJ is an N-channel open-drain output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. The gates incorporate di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK21LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.5	V
		I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current	V_O = V_{CC} or 0			10	μA
C_i	Input capacitance			0.14		pF
C_{pd}	Equivalent power dissipation capacitance	t_r = t_f = 1 ns		0.53		pF

‡Typical values are at V_{CC} = 5 V, T_A = 25 °C.

NOTE 1: These limits apply when all other external outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}	3.94	8.60	16.65	ns
t_{PZL}			C_L = 50 pF, R_L = 1 kΩ to V_{CC}	8.02	17.08	32.65	
t_{PLZ}	A	Y	R_L = 1 kΩ to V_{CC}		0.53		
Δt_{PZL}				120	240	460	ps/pF

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}	3.02	6.59	12.8	ns
t_{PZL}			C_L = 50 pF, R_L = 1 kΩ to V_{CC}	5.64	12.03	22.98	
Δt_{PZL}	A	Y		70	160	290	ps/pF

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK23LJ
2-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE AND di/dt CONTROL

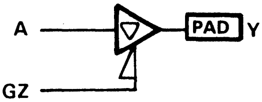
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPK23LJ is a 3-state output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. The gates incorporate di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK23LJ A,GZ,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage				2.2		V
V_{OH}	High-level output voltage		$I_{OH} = -2$ mA	3.7			V
			$I_{OH} = -20$ μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 2$ mA			0.5	V
			$I_{OL} = 20$ μA, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			± 10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		7.56		pF

‡Typical values are at $V_{CC} = 5$ V, $T_A = 25$ °C.
NOTE 1: These limits apply when all other external outputs are open.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	1.31	3.37	7.08	ns
t_{PHL}				4.38	9.56	17.84	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.35	3.81	8.28	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.57	10.42	20.58	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	2.29	6.14	12.96	ns
t_{PHL}				8.33	17.25	31.11	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.32	6.69	14.63	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	8.68	18.97	36.67	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		1.27		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		0.52		

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y		30	80	170	ps/pF
Δt_{PHL}				110	220	380	
Δt_{PZH}	GZ	Y		30	80	180	ps/pF
Δt_{PZL}				120	240	460	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	2.1	5.06	9.98	ns
t_{PHL}				3.43	7.74	14.88	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.27	5.75	11.91	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.53	8.15	16.19	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	4.41	10.54	20.42	ns
t_{PHL}				6.05	13.01	24.3	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	4.61	11.73	24.23	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	6.21	13.72	26.61	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y		70	160	300	ps/pF
Δt_{PHL}				70	150	270	
Δt_{PZH}	GZ	Y		70	170	350	ps/pF
Δt_{PZL}				80	160	300	

†Typical values are at V_{CC} = 5 V, T_A = 25 °C.

OPK24LJ
2-mA P-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH di/dt CONTROL

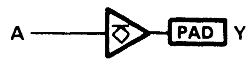
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK24LJ is a P-channel open-drain output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. The gates incorporate di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK24LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	$I_{OH} = -2$ mA	3.7			V
		$I_{OH} = -20\ \mu A$, See Note 1	$V_{CC} - 0.1$			
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			−10	μA
C_i	Input capacitance			0.14		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		0.61		pF

‡Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NOTE 1: These limits apply when all other external outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZH}	A	Y	C_L = 15 pF, R_L = 1 kΩ to GND	1.19	2.99	6.32	ns
t_{PZH}			C_L = 50 pF, R_L = 1 kΩ to GND	2.08	5.68	12.4	
t_{PHZ}	A	Y	R_L = 1 kΩ to GND		1		
Δt_{PZH}				30	80	170	ps/pF

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZH}	A	Y	C_L = 15 pF, R_L = 1 kΩ to GND	1.96	4.85	9.94	ns
t_{PZH}			C_L = 50 pF, R_L = 1 kΩ to GND	4.23	10.66	22	
Δt_{PZH}	A	Y		60	170	340	ps/pF

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

TGC100 SERIES

OPK40LJ 4-mA CMOS/TTL OUTPUT BUFFER WITH di/dt CONTROL

D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK40LJ is a totem-pole output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. The gates incorporate di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK40LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −4 mA	3.7			V
		I_{OH} = −20 μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.5	V
		I_{OL} = 20 μA, See Note 1			0.1	
C_i	Input capacitance			0.41		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		8.28		pF

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These limits apply when all other external outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, R_L = ∞	1.09	2.53	5.19	ns
t_{PHL}				3.06	6.38	11.78	
t_{PLH}	A	Y	C_L = 50 pF, R_L = ∞	1.64	4.02	8.31	ns
t_{PHL}				5.18	10.49	18.86	
Δt_{PLH}	A	Y		20	40	90	ps/pF
Δt_{PHL}				60	120	200	

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, R_L = ∞	1.52	3.47	6.81	ns
t_{PHL}				2.5	5.3	10.04	
t_{PLH}	A	Y	C_L = 50 pF, R_L = ∞	2.7	6.26	12.12	ns
t_{PHL}				3.99	8.25	15.25	
Δt_{PLH}	A	Y		30	80	150	ps/pF
Δt_{PHL}				40	80	150	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK41LJ
4-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH di/dt CONTROL

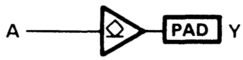
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	Z
L	L

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK41LJ is an N-channel open-drain output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. The gates incorporate di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK41LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.5	V
		I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			10	μA
C_i	Input capacitance			0.23		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		0.76		pF

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These limits apply when all other external outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}	3	6.42	12.19	ns
t_{PZL}	A	Y	C_L = 50 pF, R_L = 1 kΩ to V_{CC}	5.17	10.75	19.86	ns
t_{PLZ}	A	Y	R_L = 1 kΩ to V_{CC}		0.38		ns
Δt_{PZL}	A	Y	R_L = 1 kΩ to V_{CC}	60	120	220	ps/pF

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}	2.43	5.26	10.17	ns
t_{PZL}	A	Y	C_L = 50 pF, R_L = 1 kΩ to V_{CC}	3.95	8.32	15.67	ns
Δt_{PZL}	A	Y		40	90	160	ps/pF

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK43LJ
4-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE AND di/dt CONTROL

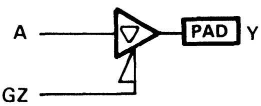
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPK43LJ is a 3-state output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. The gates incorporate di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK43LJ A,GZ,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage				2.2		V
V_{OH}	High-level output voltage		$I_{OH} = -4$ mA	3.7			V
			$I_{OH} = -20\ \mu A$, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 4$ mA			0.5	V
			$I_{OL} = 20\ \mu A$, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		8.16		pF

‡Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NOTE 1: These limits apply when all other external outputs are open.

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TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	1.12	3.01	6.45	ns
t_{PHL}				3.39	7.91	15.27	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.18	3.42	7.41	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.49	8.27	16.34	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	1.71	4.61	9.76	ns
t_{PHL}				5.64	12.35	23.02	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.76	5.04	10.86	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.77	12.86	24.54	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		1.74		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		0.62		

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y		20	50	90	ps/pF
Δt_{PHL}				60	130	220	
Δt_{PZH}	GZ	Y		20	50	100	ps/pF
Δt_{PZL}				60	1.30	230	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	1.59	4.04	8.23	ns
t_{PHL}				2.76	6.66	13.24	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.76	4.52	9.31	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.82	6.86	13.84	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	2.8	6.9	13.67	ns
t_{PHL}				4.36	9.93	19.12	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.97	7.48	15.15	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.43	10.19	19.89	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y		30	80	160	ps/pF
Δt_{PHL}				50	90	170	
Δt_{PZH}	GZ	Y		30	80	170	ps/pF
Δt_{PZL}				50	100	170	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK44LJ
4-mA P-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH di/dt CONTROL

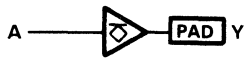
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK44LJ is a P-channel open-drain output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. The gates incorporate di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK44LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA	3.7			V
		$I_{OH} = -20$ μA, See Note 1	$V_{CC} - 0.1$			
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			−10	μA
C_i	Input capacitance			0.23		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		1.04		pF

‡Typical values are at $V_{CC} = 5$ V, $T_A = 25\,°C$.

NOTE 1: These limits apply when all other external outputs are open.

OPK44LJ 4-mA P-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH di/dt CONTROL

D3015, OCTOBER 1987

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZH}	A	Y	C_L = 15 pF, R_L = 1 kΩ to GND	1.07	2.51	5.24	ns
t_{PZH}			C_L = 50 pF, R_L = 1 kΩ to GND	1.58	3.94	8.31	
t_{PHZ}	A	Y	R_L = 1 kΩ to GND		0.88		
Δt_{PZH}				10	40	90	ps/pF

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZH}	A	Y	C_L = 15 pF, R_L = 1 kΩ to GND	1.5	3.5	7.03	ns
t_{PZH}			C_L = 50 pF, R_L = 1 kΩ to GND	2.65	6.31	12.58	
Δt_{PZH}	A	Y		30	80	160	ps/pF

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK80LJ
8-mA CMOS/TTL OUTPUT BUFFER WITH di/dt CONTROL

D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK80LJ is a totem-pole output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. The gates incorporate di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK80LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	$I_{OH} = -8$ mA	3.7			V
		$I_{OH} = -20$ μA, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA			0.5	V
		$I_{OL} = 20$ μA, See Note 1			0.1	
C_i	Input capacitance			0.41		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		9.36		pF

‡Typical values are at $V_{CC} = 5$ V, $T_A = 25$ °C.

NOTE 1: These limits apply when all other external outputs are open.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, R_L = ∞	1.05	2.65	5.64	ns
t_{PHL}				2.74	6.11	11.71	
t_{PLH}	A	Y	C_L = 50 pF, R_L = ∞	1.47	3.71	7.8	ns
t_{PHL}				4.13	8.87	16.48	
Δt_{PLH}	A	Y		10	30	60	ps/pF
Δt_{PHL}				40	80	140	

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF, R_L = ∞	1.39	3.38	6.87	ns
t_{PHL}				2.28	5.23	10.28	
t_{PLH}	A	Y	C_L = 50 pF, R_L = ∞	2.12	5.06	10.08	ns
t_{PHL}				3.33	7.36	14.07	
Δt_{PLH}	A	Y		20	50	90	ps/pF
Δt_{PHL}				30	60	110	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK81LJ
8-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH di/dt CONTROL

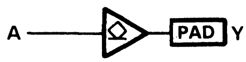
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	Z
L	L

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK81LJ is an N-channel open-drain output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. The gates incorporate di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK81LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.5	V
		I_{OL} = 20 μA, See Note 1			0.1	
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			10	μA
C_i	Input capacitance			0.23		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		1.04		pF

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These limits apply when all other external outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}	2.7	6.13	11.94	ns
t_{PZL}			C_L = 50 pF, R_L = 1 kΩ to V_{CC}	4.13	8.95	16.85	
t_{PLZ}	A	Y	R_L = 1 kΩ to V_{CC}		0.52		
Δt_{PZL}				40	80	140	ps/pF

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZL}	A	Y	C_L = 15 pF, R_L = 1 kΩ to V_{CC}	2.23	5.19	10.34	ns
t_{PZL}			C_L = 50 pF, R_L = 1 kΩ to V_{CC}	3.32	7.38	14.24	
Δt_{PZL}	A	Y		30	60	110	ps/pF

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK83LJ
8-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE AND di/dt CONTROL

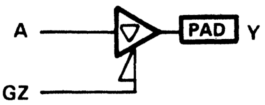
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPK83LJ is a 3-state output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. The gates incorporate di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK83LJ A,GZ,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage				2.2		V
V_{OH}	High-level output voltage		$I_{OH} = -8$ mA	3.7			V
			$I_{OH} = -20\ \mu A$, See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 8$ mA			0.5	V
			$I_{OL} = 20\ \mu A$, See Note 1			0.1	
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			± 10	μA
C_i	Input capacitance	A			0.23		pF
		GZ			0.18		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns		9.04		pF

‡Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NOTE 1: These limits apply when all other external outputs are open.

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TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	1.12	3.26	7.21	ns
t_{PHL}				3.11	7.84	15.73	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.18	3.67	8.11	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.19	8.1	16.46	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	1.57	4.49	9.75	ns
t_{PHL}				4.65	10.98	21.33	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.64	4.89	10.67	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.73	11.24	22.06	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		2.72		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		0.78		

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y		10	30	70	ps/pF
Δt_{PHL}				40	90	160	
Δt_{PZH}	GZ	Y		10	40	70	ps/pF
Δt_{PZL}				40	90	160	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

$C_L = 15$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	1.5	4.12	8.69	ns
t_{PHL}				2.56	6.75	13.92	
t_{PZH}	GZ	Y	$R_L = 1\ k\Omega$ to GND	1.68	4.57	9.62	ns
t_{PZL}			$R_L = 1\ k\Omega$ to V_{CC}	2.62	6.9	14.37	

$C_L = 50$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	A	Y	$R_L = \infty$	2.28	5.99	12.3	ns
t_{PHL}				3.74	9.23	18.49	
t_{PZH}	GZ	Y	$R_L = 1\ k\Omega$ to GND	2.46	6.45	13.28	ns
t_{PZL}			$R_L = 1\ k\Omega$ to V_{CC}	3.79	9.37	18.9	

change in propagation delay time with load capacitance over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Δt_{PLH}	A	Y		20	50	100	ps/pF
Δt_{PHL}				30	70	130	
Δt_{PZH}	GZ	Y		20	50	100	ps/pF
Δt_{PZL}				30	70	130	

†Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

TGC100 SERIES

OPK84LJ
8-mA P-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH di/dt CONTROL

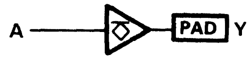
D3015, OCTOBER 1987–REVISED FEBRUARY 1989

EXTERNAL OUTPUT MACRO

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK84LJ is a P-channel open-drain output buffer that interfaces CMOS internal gates with TTL or CMOS external buses. The gates incorporate di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK84LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_T	Input threshold voltage			2.2		V
V_{OH}	High-level output voltage	$I_{OH} = -8$ mA	3.7			V
		$I_{OH} = -20\ \mu A$, See Note 1	$V_{CC}-0.1$			
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			−10	μA
C_i	Input capacitance			0.23		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns		1.64		pF

‡Typical values are at $V_{CC} = 5$ V, $T_A = 25\,°C$.

NOTE 1: These limits apply when all other external outputs are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZH}	A	Y	C_L = 15 pF, R_L = 1 kΩ to GND	1.05	2.65	5.64	ns
t_{PZH}			C_L = 50 pF, R_L = 1 kΩ to GND	1.45	3.66	7.73	
t_{PHZ}	A	Y	R_L = 1 kΩ to GND		1.37		
Δt_{PZH}				10	30	60	ps/pF

CMOS loads

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZH}	A	Y	C_L = 15 pF, R_L = 1 kΩ to GND	1.39	3.4	6.95	ns
t_{PZH}			C_L = 50 pF, R_L = 1 kΩ to GND	2.1	5.06	10.15	
Δt_{PZH}	A	Y		20	50	90	ps/pF

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

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Arithmetic Functions and Comparators

ARITHMETIC FUNCTIONS FUNCTIONAL INDEX

D3015, OCTOBER 1987—REVISED OCTOBER 1988

MAGNITUDE COMPARATORS AND ARITHMETIC FUNCTIONS

DESCRIPTION	MACRO NAME	OUTPUT DRIVE	COMMENTS	CELLS USED	PAGE
1-Bit Binary Full Adder	AD100LJ	1X	With Carry	9	14-3
Magnitude Comparator	S085LJ	2X	P=Q, P<Q, P>Q	58	14-5
	S686LJ	2X	P=Q, P>Q	104	14-26
Identity Comparator	S688LJ	2X	P=Q	32	14-30
Parity Tree	S180XLJ	1X	Odd/Even Parity	21	14-9
4-Bit ALU	S181LJ	1X	16 Arithmetic, 16 Logic Functions	125	14-11
Look Ahead Carry Gen.	S182LJ	2X	Use with S181LJ	35	14-18
4-Bit Binary Full Adder	S283LJ	2X	Internal Look Ahead	69	14-22

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AD100LJ
1-BIT FULL ADDER WITH 1X OUTPUT

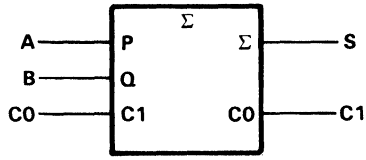
D3015, OCTOBER 1988

INTERNAL ADDER MACRO

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C0	S	C1
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The AD100LJ is a 1-bit full adder that adds two one-bit binary numbers. When the sum exceeds a single binary bit, carry (C1) is generated. The macro can be paralleled to create adders of n-bit width. When the adder is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AD100LJ A,B,C0,S,C1;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			1.7		V
C_i	Input capacitance	C0		0.34		pF
		All others		0.29		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	1.72		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

D3030, OCTOBER 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	C0	SUM	0.26	0.61	1.17	ns
t_{PHL}			0.41	1.04	2.7	
t_{PLH}	A,B	SUM	0.44	1.2	2.44	ns
t_{PHL}			0.63	1.51	3.27	
t_{PLH}	C0	C1	0.32	0.73	1.41	ns
t_{PHL}			0.54	1.51	3.29	
t_{PLH}	A,B	C1	0.34	0.8	1.51	ns
t_{PHL}			0.52	1.64	3.82	
Δt_{PLH}	C0	SUM	0.36	0.89	1.72	ns/pF
Δt_{PHL}			0.28	0.61	1.12	
Δt_{PLH}	A,B	SUM	0.36	0.89	1.71	ns/pF
Δt_{PHL}			0.23	0.51	0.91	
Δt_{PLH}	C0	C1	0.36	0.89	1.74	ns/pF
Δt_{PHL}			0.33	0.74	1.4	
Δt_{PLH}	A,B	C1	0.36	0.92	1.81	ns/pF
Δt_{PHL}			0.31	0.7	1.42	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

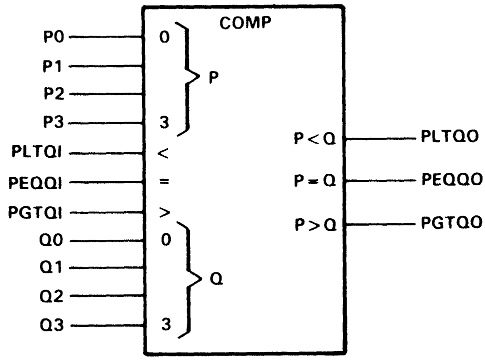
S085LJ 4-BIT MAGNITUDE COMPARATOR

D3015, OCTOBER 1987

SOFTWARE MACRO

- **Performs Magnitude Comparison of Binary, BCD, and Monotonic Codes**
- **Weighted Cascading Inputs Accomodate Both Serial and Parallel Expansion**

logic symbol†



Equivalent to 7485

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S085LJ gate-array software macro implements a 4-bit expandable magnitude comparator that evaluates binary and BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (P and Q) are made and are available at three outputs. These macros are fully expandable to any number of bits without additional gates. Words of greater length may be compared by connecting comparators in cascade.

The PGTQO, PLTQO, and PEQQO outputs of a stage handling less significant bits are connected to the corresponding PGTQI, PLTQI, and PEQQI inputs of the next stage handling more significant bits. The stage handling the least significant bits must have a high-level voltage applied to the PEQQI input. The cascading path of the S085LJ is implemented with only a two-gate-level delay to reduce overall comparison times for long words. The S085LJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
AO221LJ	2	4	8	1.12
IV120LJ	1	3	3	1.17
NA210LJ	1	6	6	1.62
NA310LJ	2	2	4	0.56
NA410LJ	2	2	4	0.58
NA510LJ	3	7	21	2.38
NA810LJ	6	2	12	2.4
TOTALS		26	58	9.83

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

D3015, OCTOBER 1987

When the comparator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

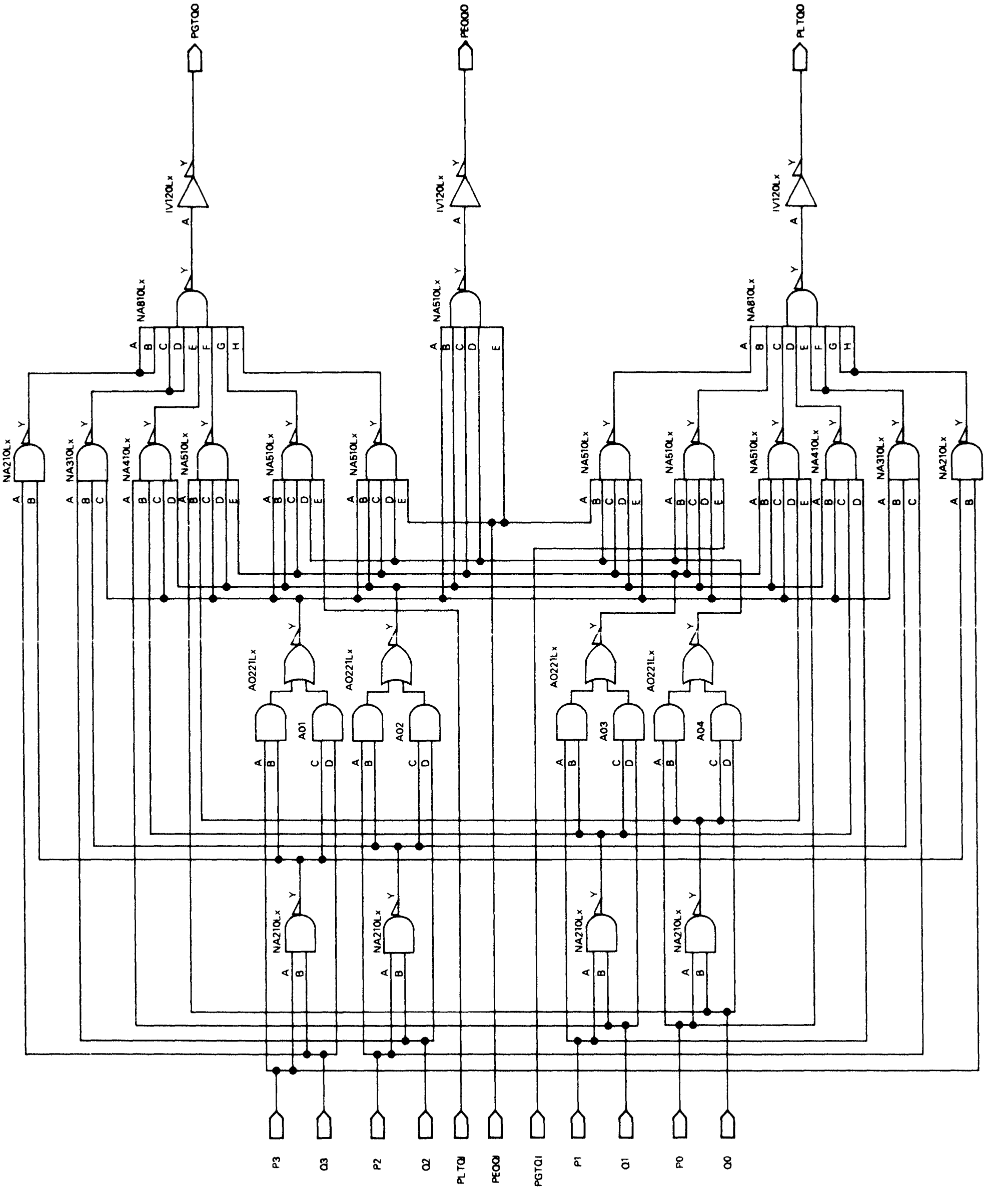
Label: S085LJ P3,P2,P1,P0,Q3,Q2,Q1,Q0,PGTQI,PLTQI,PEQQI,
PGTQO,PLTQO,PEQQO;

FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
P3, Q3	**P2, Q2**	**P1, Q1**	**P0, Q0**	**PGTQI**	**PLTQI**	**PEQQI**	**PGTQO**	**PLTQO**	**PEQQO**
P3 > Q3	X	X	X	X	X	X	H	L	L
P3 < Q3	X	X	X	X	X	X	L	H	L
P3 = Q3	P2 > Q2	X	X	X	X	X	H	L	L
P3 = Q3	P2 < Q2	X	X	X	X	X	L	H	L
P3 = Q3	P2 = Q2	P1 > Q1	X	X	X	X	H	L	L
P3 = Q3	P2 = Q2	P1 < Q1	X	X	X	X	L	H	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 > Q0	X	X	X	H	L	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 < Q0	X	X	X	L	H	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	H	L	L	H	L	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	L	H	L	L	H	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	X	X	H	L	L	H
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	H	H	L	L	L	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	L	L	L	H	H	L

D3015, OCTOBER 1987

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	PGTQI,PLTQI		0.07		pF
		All others		0.21		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	9.83		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	P,Q	PGTQO,PLTQO		4.6	8.6	ns
t_{PHL}				5.5	10.8	
t_{PLH}	P,Q	PEQQO		4.6	8.9	ns
t_{PHL}				2.3	4.4	
t_{PLH}	PLTQI,PEQQI	PGTQO		3	5.9	ns
t_{PHL}				2.6	5.3	
t_{PLH}	PGTQI,PEQQI	PLTQO		3.1	5.8	ns
t_{PHL}				2.6	5.3	
t_{PLH}	PEQQI	PEQQO		1.5	2.9	ns
t_{PHL}				1	2.1	
Δt_{PLH}	Any	Any	0.22	0.44	0.84	ns/pF
Δt_{PHL}			0.22	0.32	0.44	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

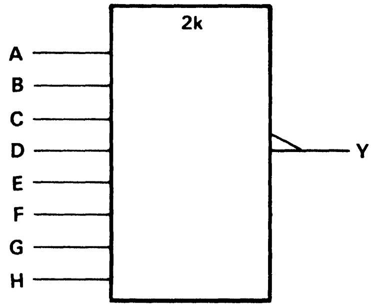
S180XLJ
8-BIT ODD/EVEN PARITY TREE

D3015, OCTOBER 1987

SOFTWARE MACRO

- **Generates Either Odd or Even Parity for Eight Data Lines on Single Output**
- **Cascadable for n Bits**

logic symbol†



Similar to parity tree of 74180

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S180XLJ gate-array software macro implements an 8-bit odd- or even-parity tree. The 8-bit length simplifies construction of large parity trees. This universal 8-bit parity tree features a single output that operates in either odd- or even-parity applications. The word-length capability is easily expanded by cascading. The S180XLJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
EX210LJ	3	7	21	5.32

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

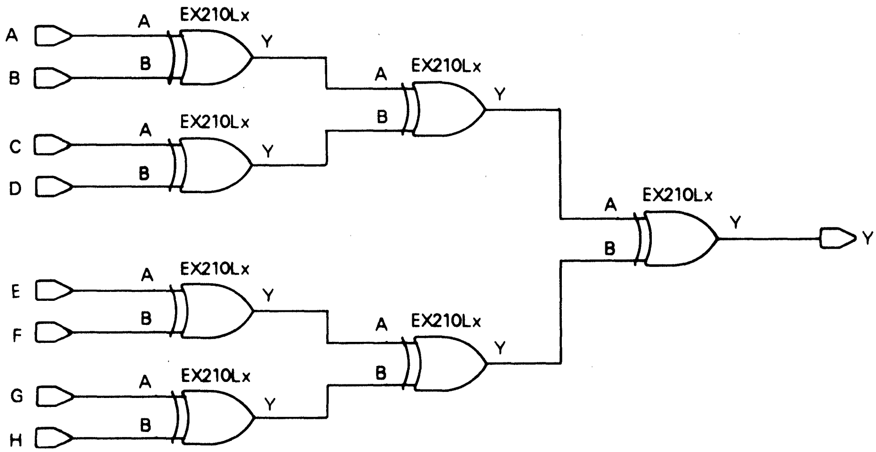
When the parity tree is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S180XLJ A,B,C,D,E,F,G,H,Y

FUNCTION TABLE

PARITY	NUMBER OF INPUTS A THRU H THAT ARE HIGH	OUTPUT
EVEN	0,2,4,6,8	L
ODD	1,3,5,7,9	H

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†		TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance		0.17		pF
C_{pd}	Equivalent power dissipation capacitance‡	$t_r = t_f = 1$ ns	5.32		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	Any	Y		3.2	6.1	ns
t_{PHL}				3.1	5.9	
Δt_{PLH}	Any	Y	0.36	0.89	1.72	ns/pF
Δt_{PHL}			0.24	0.50	0.9	

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

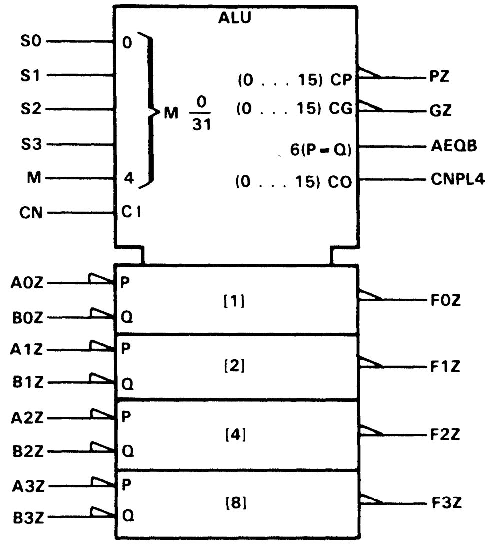
NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

D3015, OCTOBER 1987

SOFTWARE MACRO

- Performs Full 16-Function Arithmetic or Boolean Combinations of Two Variables
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus Ten Other Logic Operations

logic symbol†



Equivalent to 74181

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S181LJ gate-array software macro implements a 4-bit arithmetic logic unit. The S181LJ performs 16 arithmetic or Boolean operations on two 4-bit binary words as shown in Tables 1 and 2. Choice between the two operating modes is established by the mode control M, and selection of one-of-sixteen operations is accomplished at the select inputs S3, S2, S1, and S0. The S181LJ is implemented with the standard cell functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
EX210LJ	3	8	24	6.08
IV110LJ	1	27	27	5.67
IV120LJ	1	1	1	0.39
NA210LJ	1	14	14	3.78
NA310LJ	2	13	26	3.64
NA410LJ	2	7	14	2.03
NA510LJ	3	2	6	0.68
NO210LJ	1	5	5	0.9
NO310LJ	2	4	8	0.84
TOTALS		81	125	24.01

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the ALU is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S181LJ A3Z,A2Z,A1Z,A0Z,B3Z,B2Z,B1Z,B0Z,CN,M,S3,S2,S1,S0,
F3Z,F2Z,F1Z,F0Z,AEQB, GZ,PZ,CNPL4;

When the mode control input is low, the 16 arithmetic operations are accessible via the four select inputs. The 4-bit full adder incorporates both ripple and look-ahead carry circuitry, providing the capability to extend either technique across expanded word widths when multiple S181LJs are used in parallel.

The S181LJ accommodates both active-high and active-low data simply by redefining the designations used to describe the data inputs and outputs. For use with active-low data, use Table 1 and the input/output designations provided for the label developed above. For use with active-high data, use Table 2.

Note that only the relationship of A, B, and F data with respect to the carry and look-ahead circuitry are affected.

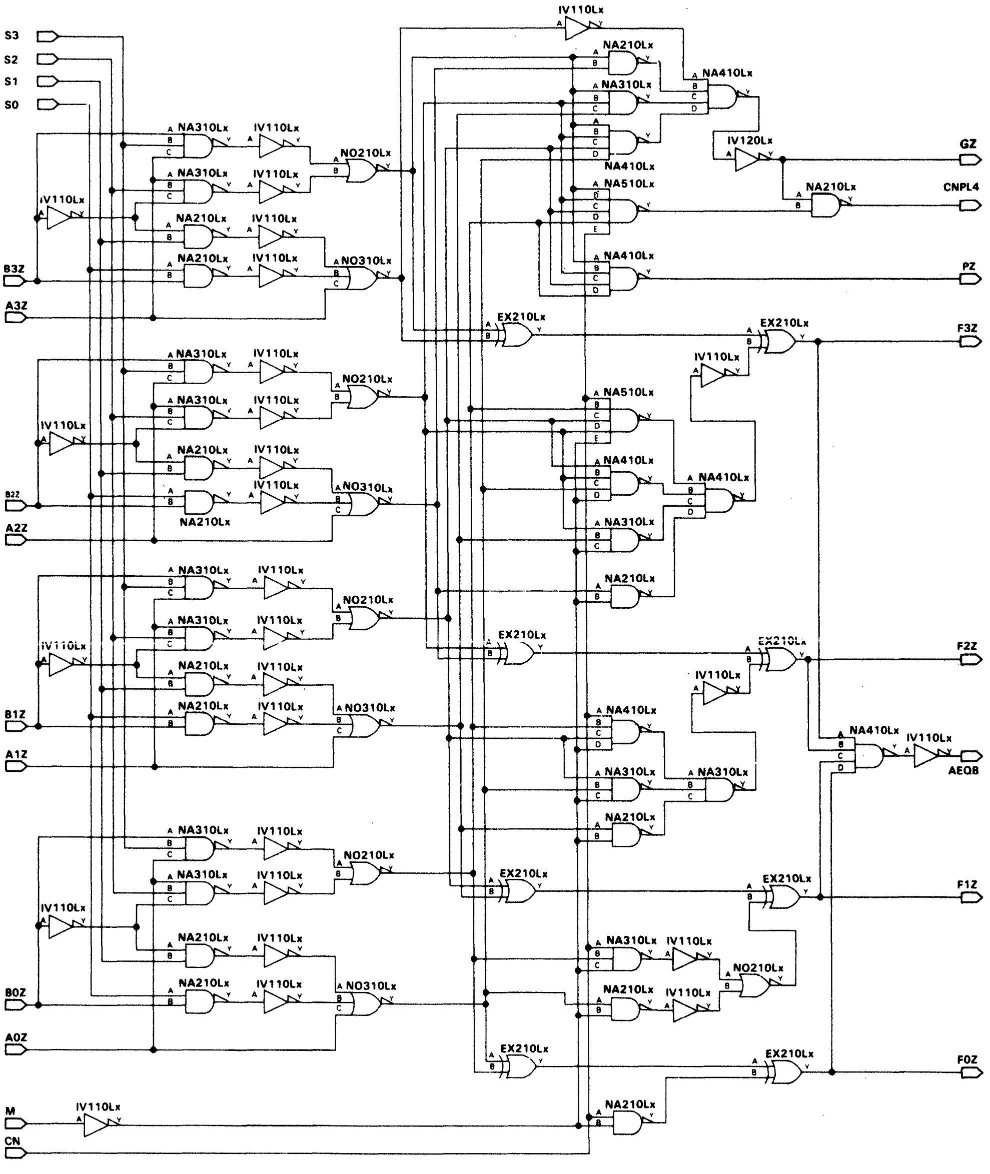
Subtraction is accomplished by 1's complement addition in which the 1's complement of the subtrahend is generated internally. The resultant output is A − B − 1, which requires an end-around or forced carry to provide A − B. Arithmetic operations with and without carry are shown in Tables 1 and 2.

The S181LJ also performs a comparison of the A and B operands. The AEQB output is decoded from the function outputs (F3, F2, F1, and F0) so that, when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with CN = H when performing this comparison. The AEQB output can be AND- or NAND-gated to perform comparisons over expanded ALUs. The CNPL4 carry output can also be used to supply relative magnitude information. Again, the ALU must be in the subtract mode by having the select inputs S3, S2, S1, and S0 at L, H, H, L, respectively.

INPUT CN	OUTPUT CNPL4	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	$A \geq B$	$A \leq B$
H	L	$A < B$	$A > B$
L	H	$A > B$	$A < B$
L	L	$A \leq B$	$A \geq B$

D3015, OCTOBER 1987—REVISED FEBRUARY 1989

logic diagram



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signal designations

The polarity indicators (open arrowheads) in both Figures 1 and 2 indicate that the associated input or output is active-low with respect to the function shown inside the symbol, and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations used in Figure 2 accommodate the logic functions and arithmetic operations for the active-high data given in Table 2.

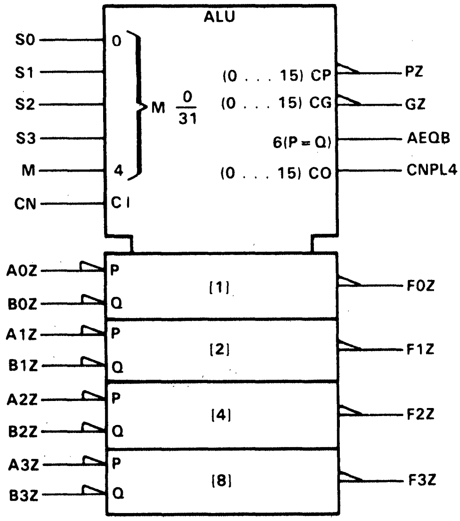

FIGURE 1

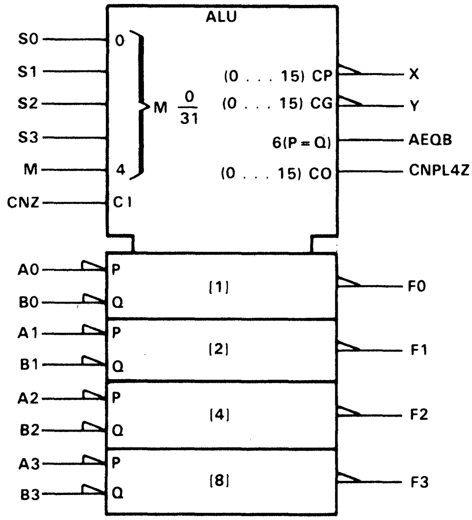

FIGURE 2

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TABLE 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	CN = L (no carry)	CN = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A} + B$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

†Each bit is shifted to the next more significant position.

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TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	CNZ = H (no carry)	CNZ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

†Each bit is shifted to the next more significant position.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	M		0.07		pF
		S0,S1,S2,S3		0.28		
		CN		0.35		
		All others		0.21		
C_{pd}	Equivalent power dissipation capacitance§		t_r = t_f = 1 ns	24.01		pF

‡For Supply Current, I_{CC}, see the TGC100 Series Data.
§The equivalent power dissipation capacitance does not include interconnect capacitance.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	CN	CNPL4	SUM or DIFF		1.6	2.9	ns
t_{PHL}					1.1	2	
t_{PLH}	AZ,BZ	CNPL4			5.4	9.9	ns
t_{PHL}					4.5	7.9	
t_{PLH}	CN	FZ			3.2	6.1	ns
t_{PHL}					3	6	
t_{PLH}	AZ,BZ	GZ			4.2	7.4	ns
t_{PHL}					5.1	9.5	
t_{PLH}	AZ,BZ	PZ			3.2	5.3	ns
t_{PHL}					4.5	7.9	
t_{PLH}	AZ,BZ	FZ			6.4	11.6	ns
t_{PHL}					6.2	11.2	
t_{PLH}	AZ,BZ	AEQB	DIFF		7.4	13.1	ns
t_{PHL}					6.7	11.7	
Δt_{PLH}	Any	CNPL4		0.34	0.87	1.7	ns/pF
Δt_{PHL}				0.34	0.72	1.44	
Δt_{PLH}	AZ,BZ	GZ		0.22	0.86	1.68	ns/pF
Δt_{PHL}				0.22	0.5	0.82	
Δt_{PLH}	AZ,BZ	PZ		0.34	0.88	1.74	ns/pF
Δt_{PHL}				0.44	1.27	2.66	
Δt_{PLH}	Any	FZ		0.36	0.89	1.72	ns/pF
Δt_{PHL}				0.24	0.5	0.9	
Δt_{PLH}	Any	AEQB		0.34	0.86	1.68	ns/pF
Δt_{PHL}				0.36	0.5	0.82	

†Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

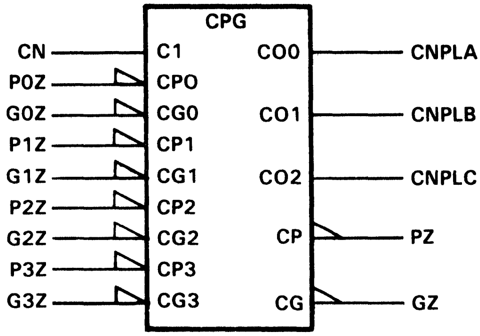
S182LJ
4-BIT LOOK-AHEAD CARRY GENERATOR

D3015, OCTOBER 1987

SOFTWARE MACRO

- **Offers Carry Functions in a Compatible Form for Direct Combinations to the ALU**
- **Cascadable to Provide Anticipated Carries Across Four Groups of Binary ALUs**
- **Designed to Accept Up to Four Pairs of Carry-Propagate and Carry-Generate Inputs, and a Carry Input**

logic symbol†



Equivalent to 74182

†This symbol is in accordancae with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S182LJ gate-array software macro implements a 4-bit look-ahead carry generator. The macro is capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. This generator, when used with the S181LJ Arithmetic Logic Unit, provides high-speed carry look-ahead capability for any word length. This macro generates the look-ahead (anticipated carry) across a group of four ALUs. In addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n bits. The carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connections to the ALU. The S182LJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
AO221LJ	2	1	2	0.28
IV110LJ	1	1	1	0.21
IV120LJ	1	5	5	1.95
NA210LJ	1	3	3	0.81
NA310LJ	2	5	10	1.4
NA410LJ	2	6	12	1.74
NO410LJ	2	1	2	0.23
TOTALS		22	35	6.62

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

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When the generator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S182LJ P3Z,G3Z,P2Z,G2Z,P1Z,G1Z,P0Z,G0Z,CN,PZ,GZ,CNPLC,CNPLB,CNPLA;

FUNCTION TABLE FOR GZ OUTPUT

INPUTS							OUPUT
G3Z	G2Z	G1Z	G0Z	P3Z	P2Z	P1Z	GZ
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR PZ OUTPUT

INPUTS				OUTPUT
P3Z	P2Z	P1Z	P0Z	PZ
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR CNPLA OUTPUT

INPUTS			OUTPUT
G0Z	P0Z	CN	CNPLA
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE FOR CNPLB OUTPUT

INPUTS					OUTPUT
G1Z	G0Z	P1Z	P0Z	CN	CNPLB
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

FUNCTION TABLE FOR CNPLC OUTPUT

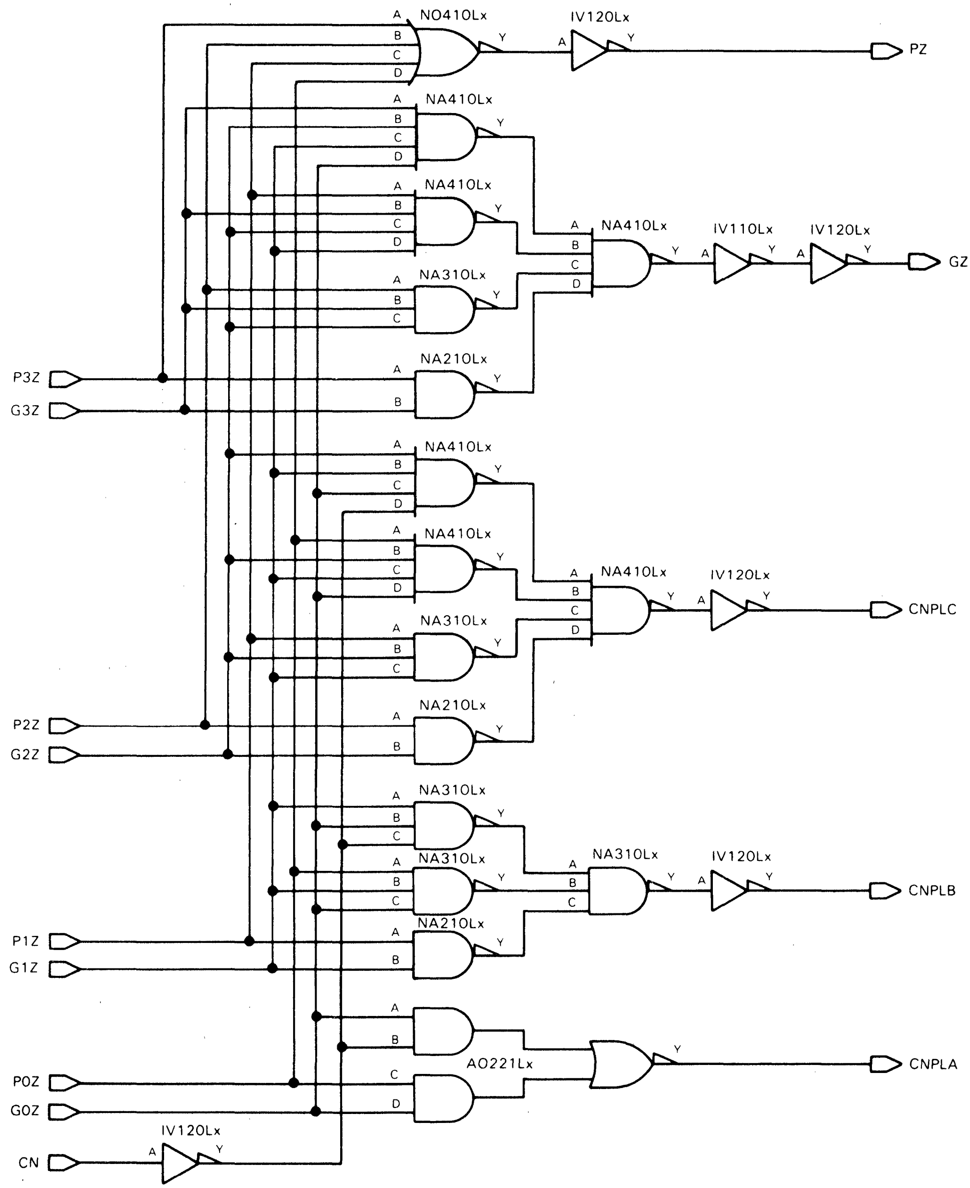
INPUTS							OUPUT
G2Z	G1Z	G0Z	P2Z	P1Z	P0Z	CN	CNPLC
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = High level, L = Low level, X = Irrelevant
Any inputs not shown in a given table are irrelevant with regard to that output.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

logic diagram



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electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	P3Z		0.14		pF
		CN		0.15		
		P2Z		0.21		
		G3Z,P0Z,P1Z		0.28		
		G0Z,G2Z		0.49		
		G1Z		0.56		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	6.62		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	Any	PZ		0.7	1.1	ns
t_{PHL}				1.9	3.7	
t_{PLH}	Any	GZ		2	3.2	ns
t_{PHL}				2.3	4.1	
t_{PLH}	Any	CNPLA		0.5	0.9	ns
t_{PHL}				0.8	1.4	
t_{PLH}	Any	CNPLB or CNPC		1.8	3.2	ns
t_{PHL}				1.7	3.5	
t_{PLH}	C	CNPLA		0.7	1.3	ns
t_{PHL}				0.8	1.4	
t_{PLH}	C	CNPLB		2.1	3.7	ns
t_{PHL}				1.9	3.5	
t_{PLH}	C	CNPLC		2.5	4.3	ns
t_{PHL}				1.7	3.3	
Δt_{PLH}	C,G0Z,P0Z	CNPLA		1.68	3.42	ns/pF
Δt_{PHL}				0.75	1.5	
Δt_{PLH}	Any other	Any other	0.22	0.44	0.84	ns/pF
Δt_{PHL}			0.22	0.32	0.44	

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

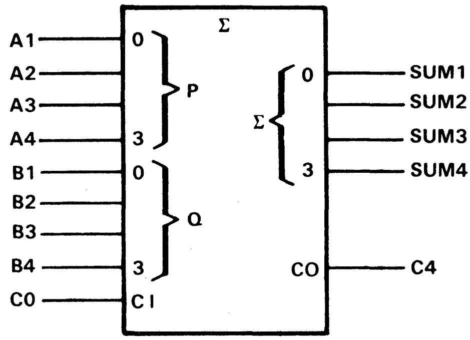
S283LJ 4-BIT BINARY FULL ADDER WITH FAST CARRY

D3015, OCTOBER 1987—REVISED FEBRUARY 1989

SOFTWARE MACRO CELL

- **Full-Carry Look-Ahead Across the Four Bits**
- **Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry**

logic symbol†



Equivalent to 74283

†This symbol is in accordancae with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S283LJ gate-array software macro implements a parallel 4-bit binary full adder. The 4-bit configuration provides the custom IC designer a fully designed, fast-carry adder and simplifies construction of large adders. These full adders perform the addition of two 4-bit binary words. The sum outputs are provided for each bit and the resultant carry (C4) is generated in parallel from the four bits. These adders feature full carry look-ahead across all four bits, providing the system designer with built-in partial look-ahead. The adder logic, including the carry, is implemented in its true form. End-around carry can be accomplished without the need for logic or level inversion. The S283LJ is implemented with the macro functions indicated:

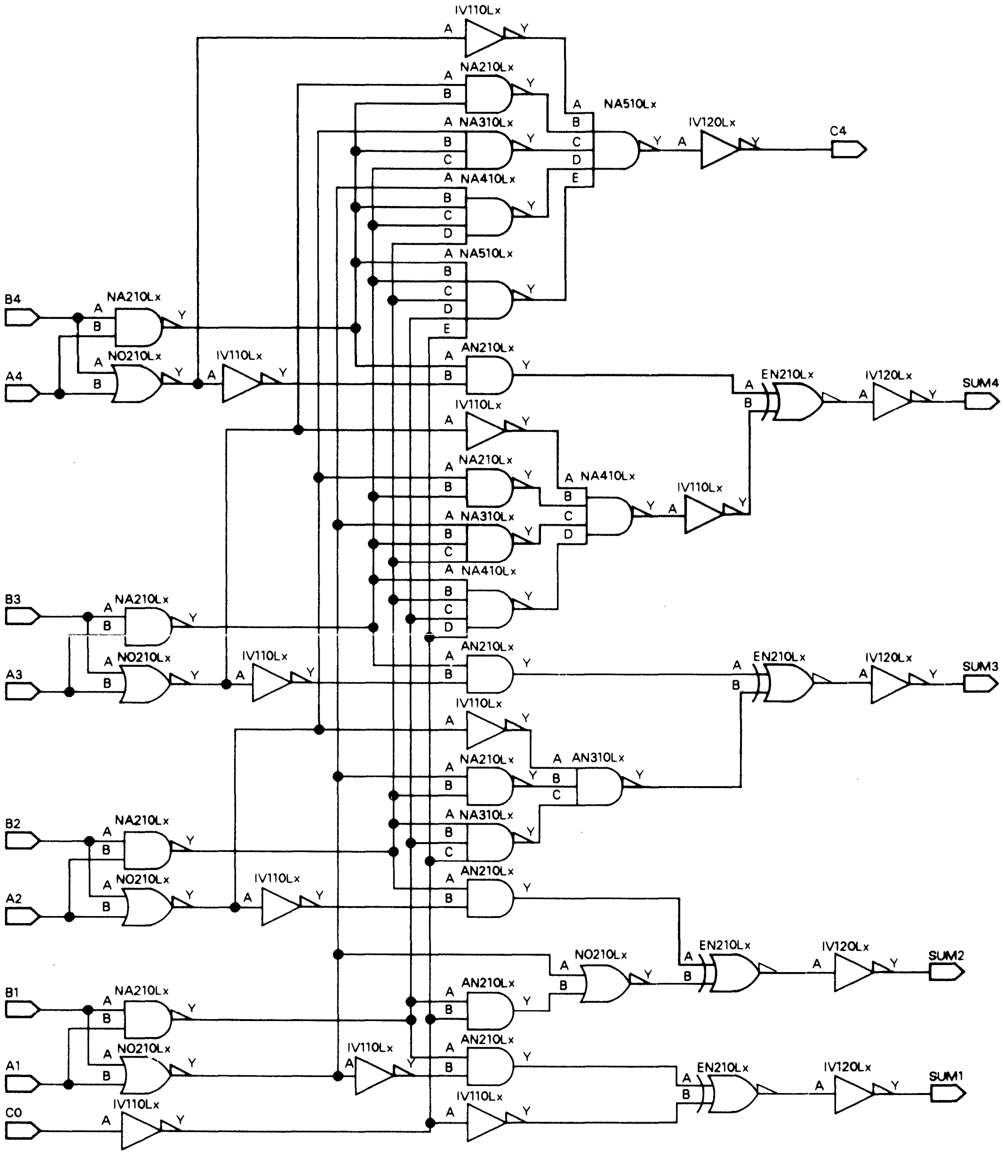
MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
AN210LJ	2	5	10	2.2
AN310LJ	2	1	2	0.56
EN210LJ	3	4	12	2.08
IV110LJ	1	10	10	2.1
IV120LJ	1	5	5	1.95
NA210LJ	1	7	7	1.89
NA310LJ	2	3	6	0.84
NA410LJ	2	3	6	0.87
NA510LJ	3	2	6	0.68
NO210LJ	1	5	5	0.18
TOTALS		45	69	13.35

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

S283LJ 4-BIT BINARY FULL ADDER WITH FAST CARRY

D3015, OCTOBER 1987

logic diagram



When the adder is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S283LJ A4,A3,A2,A1,B4,B3,B2,B1,C0,SUM4,SUM3,SUM2,SUM1,C4;

FUNCTION TABLE

INPUTS				OUTPUTS					
				WHEN C0 = L / WHEN C2 = L			WHEN C0 = H / WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	SUM1 / SUM3	SUM2 / SUM4	C2 / C4	SUM1 / SUM3	SUM2 / SUM4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs SUM1 and SUM2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs SUM3, SUM4, and C4.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	C0		0.07		pF
		All others		0.3		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	13.35		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	C0	SUM		3.5	6.4	ns
t_{PHL}				3.5	6.3	
t_{PLH}	A,B	SUM		3.4	6.1	ns
t_{PHL}				3.3	6	
t_{PLH}	C0	C4		2.3	4.1	ns
t_{PHL}				2.3	4.5	
t_{PLH}	A,B	C4		3.8	6.9	ns
t_{PHL}				3.4	6.5	
Δt_{PLH}	Any	Any	0.22	0.44	0.84	ns/pF
Δt_{PHL}			0.22	0.32	0.44	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

S686LJ
8-BIT MAGNITUDE COMPARATOR

D3015, OCTOBER 1987

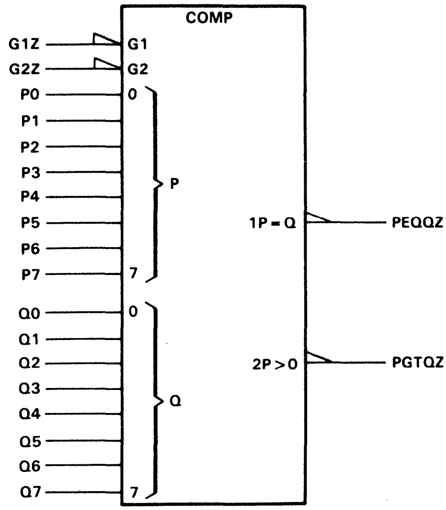
SOFTWARE MACRO

- **Performs Magnitude Comparison of Binary, BCD, and Monotonic Codes**
- **Weighted Cascaded Inputs Accomodate Both Serial and Parallel Expansion**

description

The S686LJ gate-array software macro implements an 8-bit expandable magnitude comparator. The 8-bit configuration provides the custom IC designer a magnitude comparator to embed in ASICs in its most efficient form, and the 8-bit width simplifies construction of wider comparators. These 8-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Two fully decoded decisions, (P>Q?) or (P = Q?), about two eight-bit words (P and Q) are made and are externally available at two outputs that can be decoded with a NAND gate to provide the P<Q decision. These devices are fully expandable to any number of bits. Words of greater length may be compared by connecting comparators in cascade. The PEQQZ and PGTQZ outputs of a stage handling less significant bits are connected to the corresponding G1Z and G2Z inputs of the next stage handling more significant bits. The S686LJ is implemented with the macro functions indicated.

logic symbol†



Equivalent to 74686

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}† (pF)
AN210LJ	2	4	8	1.76
AN310LJ	2	7	14	3.92
AN410LJ	3	6	18	3.42
EX210LJ	3	8	24	6.08
IV110LJ	1	13	13	2.73
IV120LJ	1	5	5	1.95
NA210LJ	1	4	4	1.08
NA310LJ	2	3	6	0.84
NA410LJ	2	3	6	0.87
NA420LJ	4	1	4	0.56
NO220LJ	2	1	2	0.3
TOTALS		55	104	23.51

†The equivalent power dissipation capacitance does not include interconnect capacitance.

When the comparator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S686LJ P0,P1,P2,P3,P4,P5,P6,P7,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7,
G1Z,G2Z,PEQQZ,PGTQZ;

FUNCTION TABLE

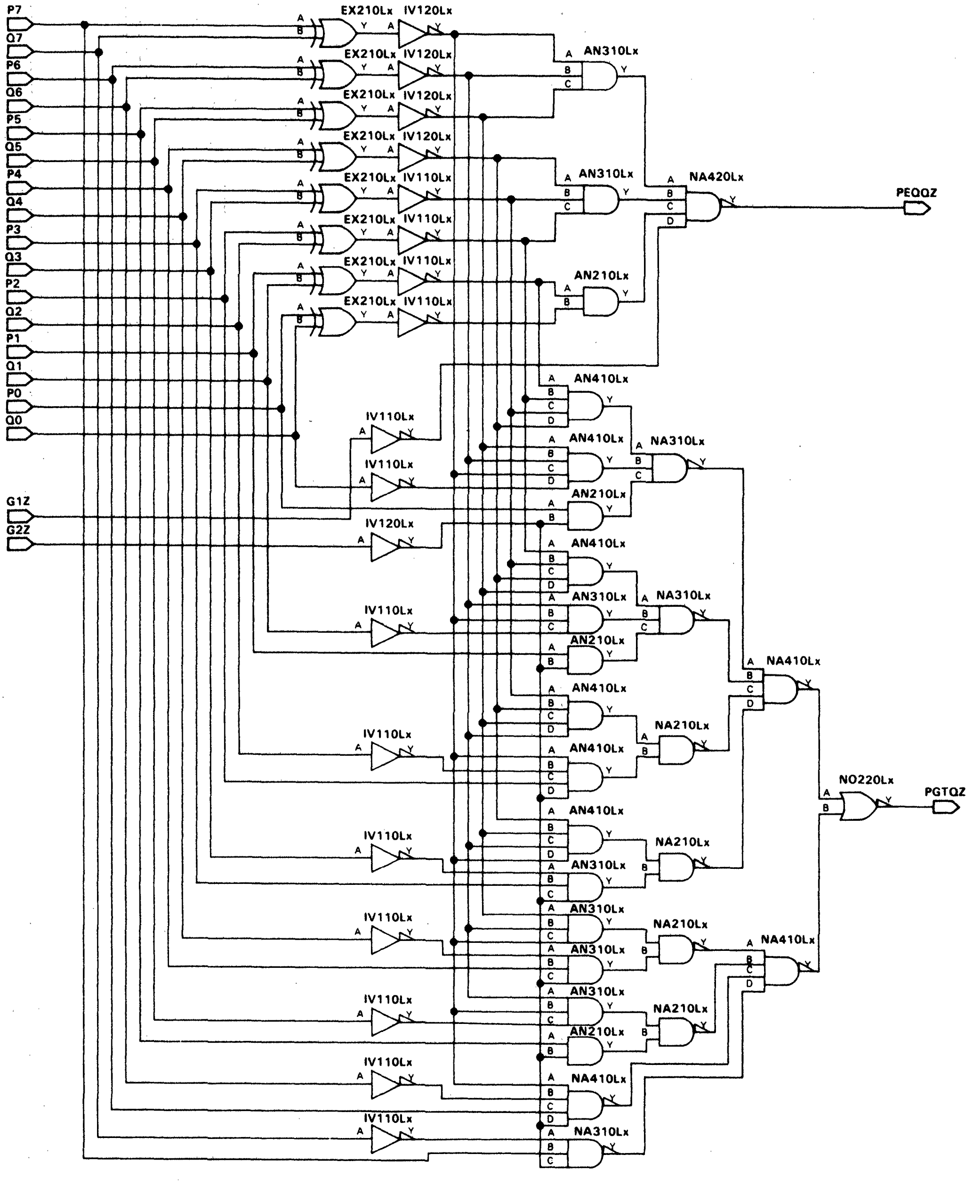
INPUTS			OUTPUTS‡	
DATA	ENABLES§		PEQQZ	PGTQZ
P,Q	G1Z	G2Z		
P=Q	L	X	L	H
P>Q	X	L	H	L
P<Q	X	X	H	H
P=Q	H	X	H	H
P>Q	X	H	H	H
X	H	H	H	H

‡The P<Q function can be generated by applying the PEQQZ and PGTQZ outputs to a 2-input NAND gate.

§G1Z enables PEQQZ, and G2Z enables PGTQZ.

D3015, OCTOBER 1987

logic diagram



D3015, OCTOBER 1987

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25 °C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	G1Z		0.07		pF
		G2Z		0.15		
		All others		0.24		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	23.51		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	P,Q	PEQQZ		2.8	4.7	ns
t_{PHL}				2.8	5.3	
t_{PLH}		PGTQZ		3.3	5.6	ns
t_{PHL}				4.2	7.9	
t_{PLH}	G1Z	PEQQZ		0.9	1.5	ns
t_{PHL}				1	1.9	
t_{PLH}	G2Z	PGTQZ		3.2	5.7	ns
t_{PHL}				4.2	7.9	
Δt_{PLH}	Any	Any	0.18	0.44	0.9	ns/pF
Δt_{PHL}			0.22	0.64	1.34	

§Typical values are at V_{CC} = 5 V, T_A = 25 °C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

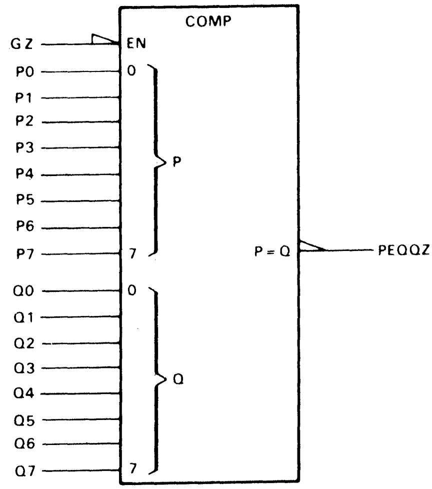
S688LJ
8-BIT IDENTITY COMPARATOR

D3015, OCTOBER 1987—REVISED OCTOBER 1988

SOFTWARE MACRO

- **Performs Identity Comparison of Binary, BCD, and Monotonic Codes**
- **Cascading Input Accomodates Expansion**

logic symbol†



Equivalent to 74688

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S688LJ gate-array software macro implements an 8-bit expandable identity comparator. The 8-bit configuration provides the custom IC designer an identity comparator to embed in ASICs in its most efficient form, and the 8-bit width simplifies construction of wider comparators. These 8-bit identity comparators perform bit-by-bit comparison of binary, straight BCD (8-4-2-1), or random codes. The fully decoded equality decision (P = Q?) on 8-bit words (P and Q) is made. These devices are expandable to any number of bits. Words of greater length may be compared by connecting comparators in cascade. The PEQQZ output of a stage handling less significant bits is connected to the corresponding GZ input of the next stage handling more significant bits. The S688LJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
EN210LJ	3	8	24	4.16
IV110LJ	1	1	1	0.21
IV120LJ	1	1	1	0.39
NA410LJ	2	1	2	0.29
NA510LJ	3	1	3	0.34
NO210LJ	1	1	1	0.18
TOTALS		13	32	5.57

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

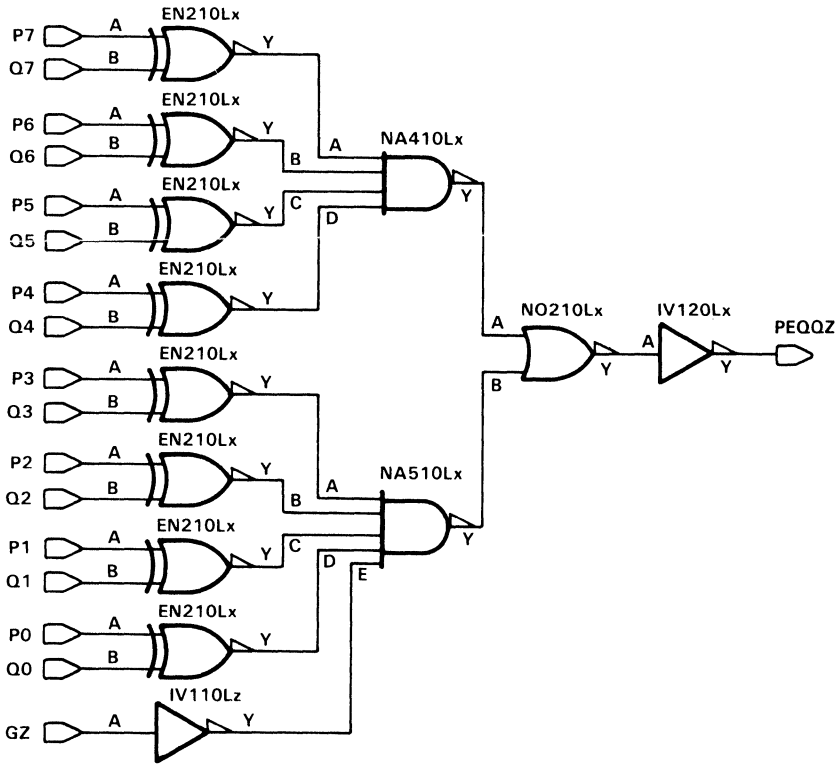
When the comparator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S688LJ P0,P1,P2,P3,P4,P5,P6,P7,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7,GZ,PEQQZ;

FUNCTION TABLE

INPUTS		OUTPUT
DATA	ENABLE	PEQQZ
Pn,Qn	GZ	
P=Q	L	L
P>Q	X	H
P<Q	X	H
X	H	H

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	GZ		0.07		pF
		All others		0.17		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	5.57		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	P	PEQQZ		2.5	4.4	ns
t_{PHL}				3.2	6.3	
t_{PLH}	Q			2.4	4.3	ns
t_{PHL}				3.2	6.3	
t_{PLH}	GZ			2	3.2	ns
t_{PHL}				3	5.7	
Δt_{PLH}	Any	PEQQZ	0.22	0.44	0.84	ns/pF
Δt_{PHL}			0.22	0.32	0.44	

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

COUNTERS FUNCTIONAL INDEX

D3015, OCTOBER 1987—REVISED OCTOBER 1988

SYNCHRONOUS COUNTERS — POSITIVE-EDGE-TRIGGERED

DESCRIPTION	MACRO NAME	LOAD	OUTPUT DRIVE	COMMENTS	CELLS USED	PAGE
4-Bit Binary	S161ALJ	Sync	1X	Async Clear	79	15-3
	S163ALJ	Sync	1X	Sync Clear	81	15-8
4-Bit Up/Down	S191LJ	Async	1X	With Mode Control	98	15-13
	S193LJ	Async	1X	Dual Clock	87	15-19

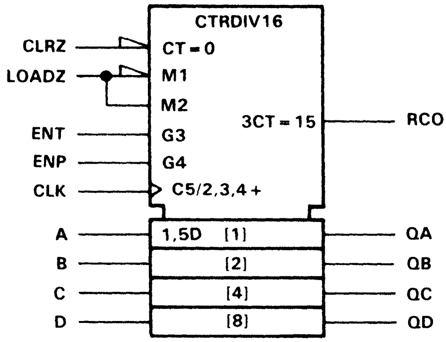
S161ALJ
SYNCHRONOUS 4-BIT BINARY COUNTER WITH DIRECT CLEAR

D3015, OCTOBER 1987

SOFTWARE MACRO

- Internal Look-Ahead Enhances Performance of Cascaded Counters
- Asynchronous Clear Initializes Sequence Regardless of Mode
- Parallel Synchronously Presettable for Full-Cycle Modulo-N Sequences
- Gated Enables and RCO Implement Local and Global Carry Status

logic symbol†



Equivalent to 74161A

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S161ALJ gate-array software macro implements a synchronous 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change coincidentally with each other when so instructed by the count-enable inputs and other gating. This mode of operation eliminates output counting spikes associated with asynchronous (ripple) counters. The clear and load inputs are buffered to enhance performance. Clocking of the register occurs on the rising (positive-going) edge of the clock waveform. The S161ALJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
AN320LJ	3	1	3	0.73
IV110LJ	1	4	4	0.84
IV120LJ	1	4	4	1.56
IV140LJ	2	2	4	1.6
NA210LJ	1	6	6	1.62
NA310LJ	2	10	20	2.8
NA410LJ	2	2	4	0.58
NA510LJ	3	2	6	0.68
R2406LJ	28	1	28	8.17
TOTALS		32	79	18.58

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the counter is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S161ALJ D,C,B,A,CLK,CLRZ,ENP,ENT,LOADZ,QD,QC,QB,QA,RCO;

These counters are fully programmable; that is, they may be preset to any number between 0 and 15. Since presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

Clearing is asychronous. A low level at the clear input sets all outputs low regardless of the levels of the clock, load, or enable.

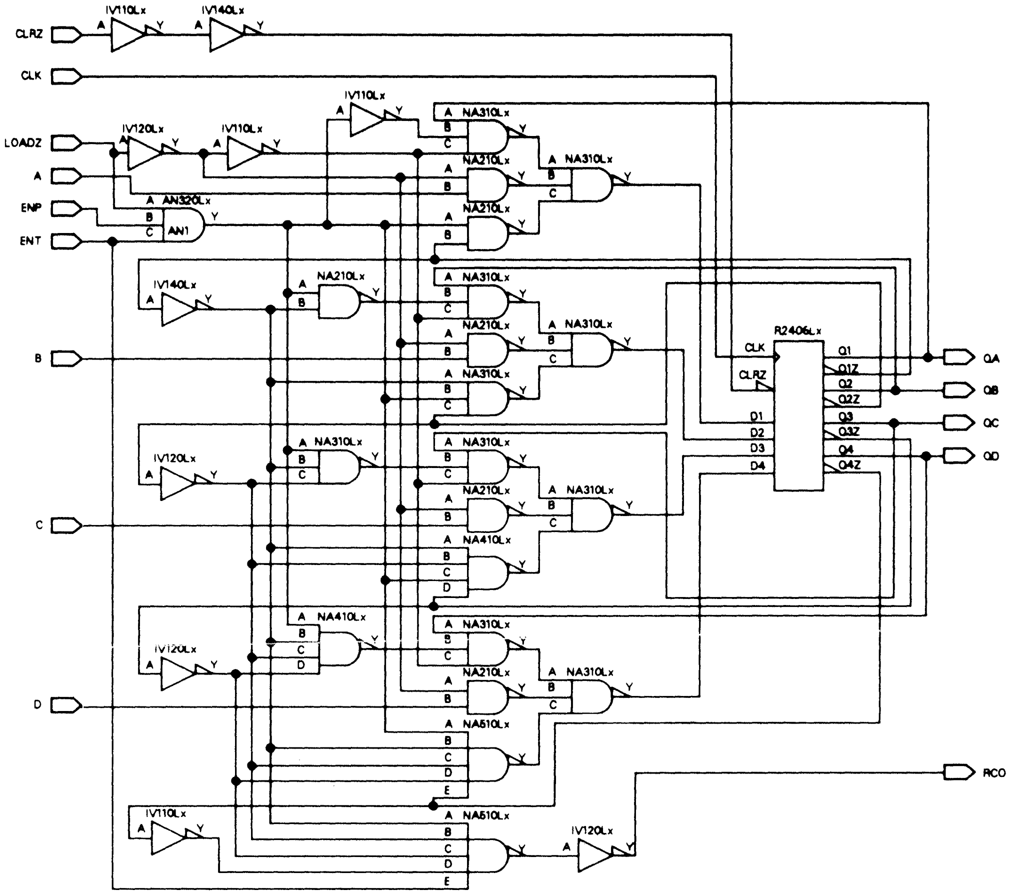
The carry look-ahead circuitry provides for cascading counters in n-bit synchronous applications without additional gating. Instrumental in achieving this are two count-enable inputs and a ripple-carry output. Both count-enable inputs (ENP and ENT) must be high to count. ENP enables the local 4-bits and the ENT is fed forward to globally extend the enable/disable of previous/next 4-bit cascaded counters. The ripple-carry out (RCO), when locally and globally enabled, will output a high-level pulse at maximum count that is used to enable successive stages.

These counters feature a fully independent clock. Changes at control inputs other than the clear will have no effect on the counter until clocking occurs. The functions of the counter are dictated solely by conditions meeting setup, hold, and duration recommendations.

S161ALJ SYNCHRONOUS 4-BIT BINARY COUNTER WITH DIRECT CLEAR

D3015, OCTOBER 1987

logic diagram



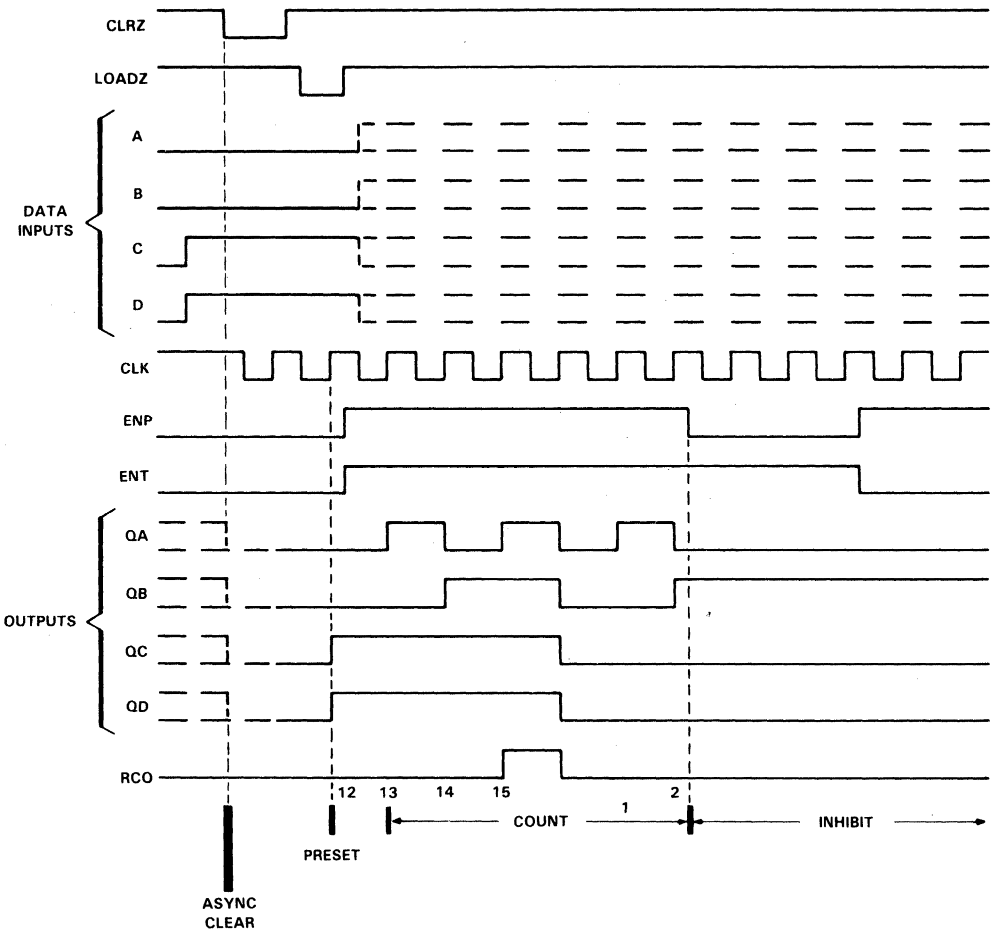
absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

S161ALJ output sequence

Illustrated below is the following sequence:

1. Asynchronously clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit.



timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	A,B,C,D,CLRZ,ENP		0.07		pF
		ENT		0.14		
		LOADZ		0.22		
		CLK		0.15		
C_{pd}	Equivalent power dissipation capacitance‡		t_r = t_f = 1 ns	18.58		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	CLK	RCO		3.9	7.1	ns
t_{PHL}				3.5	7.1	
t_{PLH}	CLK	Q		1.7	3.2	ns
t_{PHL}				1.9	3.8	
t_{PLH}	ENT	RCO		1.5	2.9	ns
t_{PHL}				1	2.1	
t_{PHL}	CLRZ	Q		1.9	3.4	ns
t_{PHL}	CLRZ	RCO		3.4	6.9	ns
Δt_{PLH}	CLK	Q	0.37	0.9	1.73	ns/pF
Δt_{PHL}			0.25	0.52	0.96	
Δt_{PLH}	Any	RCO	0.22	0.44	0.84	ns/pF
Δt_{PHL}			0.22	0.32	0.44	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

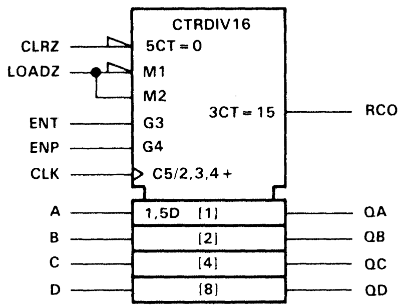
S163ALJ SYNCHRONOUS 4-BIT BINARY COUNTER

D3015, OCTOBER 1987—REVISED FEBRUARY 1989

SOFTWARE MACRO

- **Internal Look-Ahead Enhances Performance of Cascaded Counters**
- **Synchronous Clear Initializes Sequence Regardless of Mode**
- **Parallel Synchronously Presettable for Full-Cycle Modulo-N Sequences**
- **Gated Enables and RCO Implement Local and Global Carry Status**

logic symbol†



Equivalent to 74163A

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S163ALJ gate-array software macro implements a synchronous 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the count-enable inputs and other gating. This mode of operation eliminates output counting spikes associated with asynchronous (ripple) counters. The clear and load inputs are buffered to enhance performance and clocking of the register occurs on the rising (positive-going) edge of the clock waveform. The S163ALJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
AN410LJ	3	1	3	0.57
IV110LJ	1	3	3	0.63
IV120LJ	1	3	3	1.17
IV140LJ	2	1	2	0.8
NA210LJ	1	6	6	1.62
NA310LJ	2	10	20	2.8
NA410LJ	2	2	4	0.58
NA510LJ	3	2	6	0.68
NO220LJ	2	2	4	0.6
R2406LJ	28	1	28	17.62
TO010LJ	2	1	2	—
TOTALS		32	81	27.07

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the counter is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S163ALJ D,C,B,A,CLK,CLRZ,ENP,ENT,LOADZ,QD,QC,QB,QA,RCO;

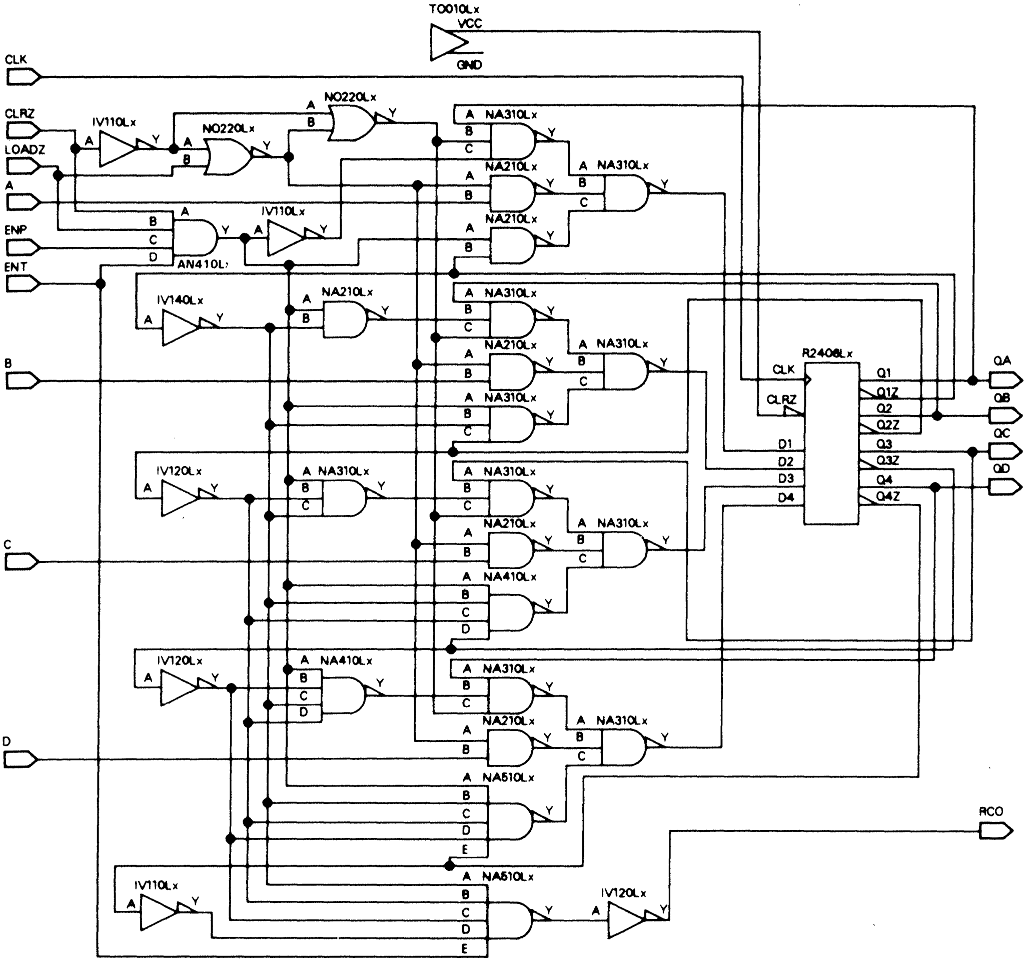
These counters are fully programmable; that is, they may be preset to any number between 0 and 15. Since presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

Clearing is sychronous. A low level at the clear input will set all outputs low on the next positive transition of the clock.

The carry look-ahead circuitry provides for cascading counters in n-bit synchronous applications without additional gating. Instrumental in achieving this are two count-enable inputs and a ripple-carry output. Both count-enable inputs (ENP and ENT) must be high to count. ENP enables the local 4-bits and the ENT is fed forward to globally extend the enable/disable of previous/next 4-bit cascaded counters. The ripple-carry out (RCO), when locally and globally enabled, will output a high-level pulse that is used to enable successive stages.

These counters feature a fully independent clock. Changes at control inputs, including clear, will have no effect on the counter until clocking occurs. The functions of the counter are dictated solely by conditions meeting setup, hold, and duration recommendations.

logic diagram

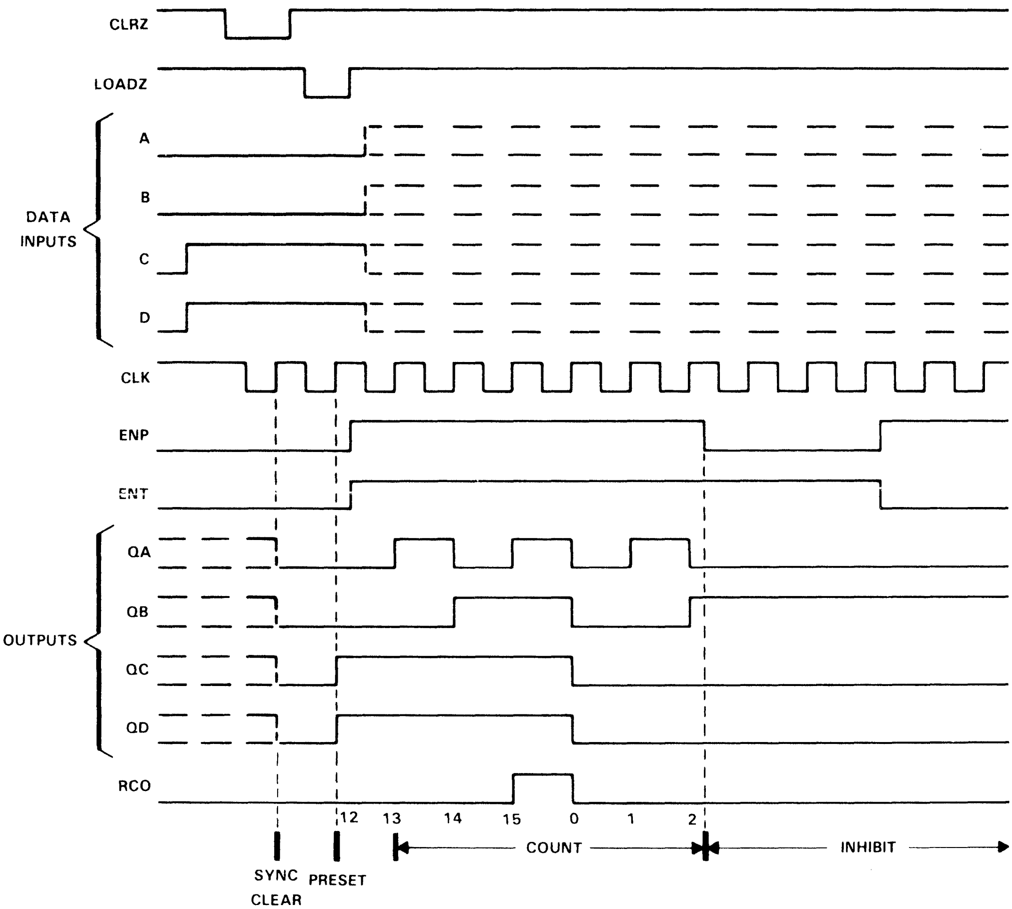


D3015, OCTOBER 1987

S163ALJ output sequence

Illustrated below is the following sequence:

1. Synchronously clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit.



D3015, OCTOBER 1987—REVISED FEBRUARY 1989

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	A,B,C,D,ENP		0.07		pF
		CLRZ,ENT		0.14		
		CLK		0.15		
		LOADZ		0.22		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	27.07		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	CLK	RCO		3.9	7.1	ns
t_{PHL}				3.5	7.1	
t_{PLH}	CLK	Q		1.7	3.2	ns
t_{PHL}				1.9	3.8	
t_{PLH}	ENT	RCO		1.5	2.9	ns
t_{PHL}				1	2.1	
Δt_{PLH}	CLK	Q	0.37	0.9	1.73	ns/pF
Δt_{PHL}			0.25	0.52	0.96	
Δt_{PLH}	Any	RCO	0.22	0.44	0.84	ns/pF
Δt_{PHL}			0.22	0.32	0.44	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

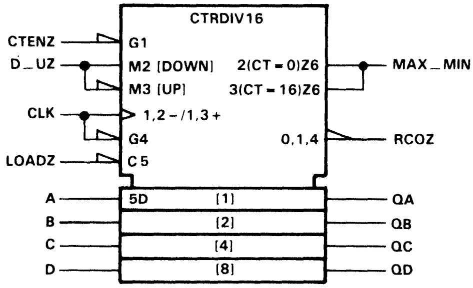
S191LJ
SYNCHRONOUS UP/DOWN BINARY COUNTER WITH DOWN/UP MODE CONTROL

D3015, OCTOBER 1987—REVISED OCTOBER 1988

SOFTWARE MACRO

- Single Down/Up Control Line
- Look-Ahead Circuitry Enhances Performance of Cascaded Counters
- Fully Synchronous in Count Mode
- Parallel Asynchronous Load for Modulo-N Count Sequences
- Count Enable Input for Setting Sequence Start and Stop

logic symbol†



Equivalent to 74191

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S191LJ gate-array software macro implements a synchronous, reversible up/down 4-bit binary counter. A synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates output counting spikes normally associated with asynchronous (ripple clock) counters. The S191LJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
DFB20LJ	10	4	40	10.4
IV110LJ	1	13	13	2.73
IV120LJ	1	1	1	0.39
NA210LJ	1	26	26	7.02
NA310LJ	2	3	6	0.84
NA410LJ	2	2	4	0.58
NA510LJ	3	2	6	0.68
NO210LJ	1	2	2	0.36
TOTALS		53	98	23

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the counter is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S191LJ D,C,B,A,CLK,D_UZ,CTENZ,LOADZ,QD,QC,QB,QA,RCOZ,MAX_MIN;

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input (CTENZ) is low. A high at CTENZ inhibits counting. The direction of the count is determined by the level of the down/up (D_UZ) input. When D_UZ is low, the counter counts up and when the D_UZ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs (CTENZ and D_UZ) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

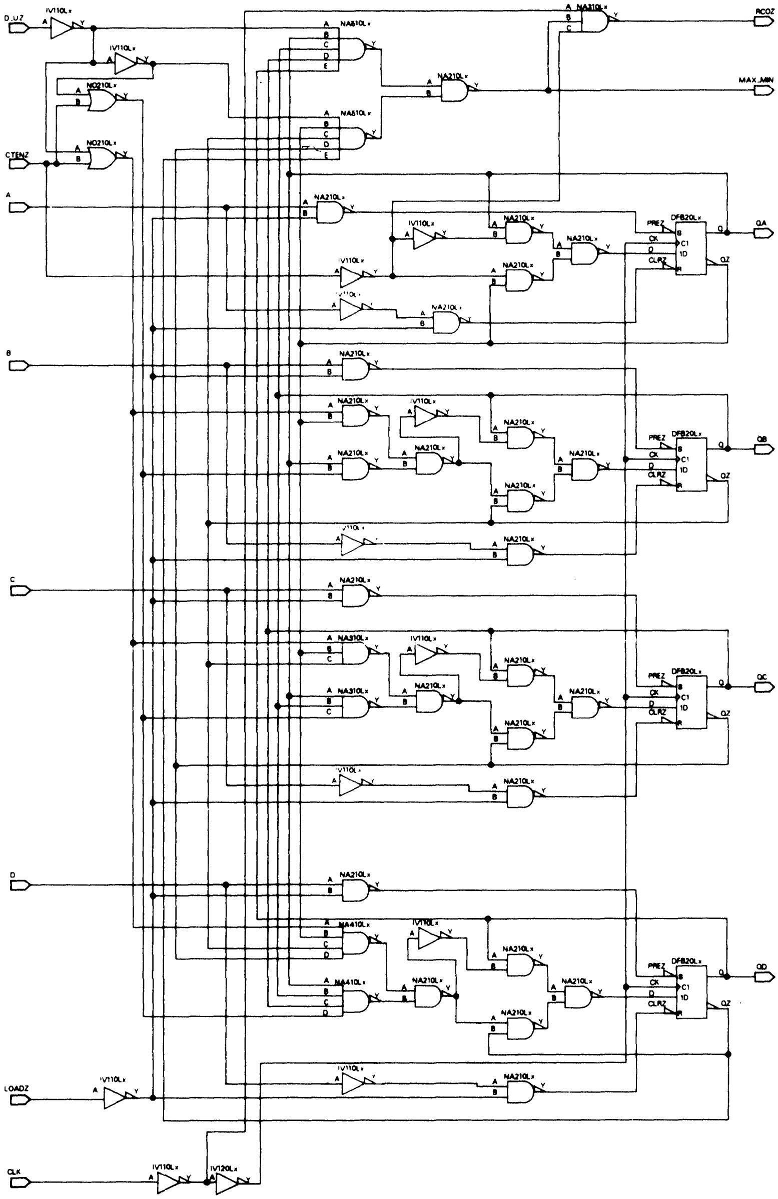
These counters are fully programmable; that is, they may be preset to any number between 0 and 15 by placing a low on the load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple and maximum/minimum count. The latter output (MAX_MIN) produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (all outputs high) counting up. The ripple clock output (RCOZ) produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple-clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

S191LJ
SYNCHRONOUS UP/DOWN BINARY COUNTER WITH DOWN/UP MODE CONTROL

D3015, OCTOBER 1987—REVISED OCTOBER 1988

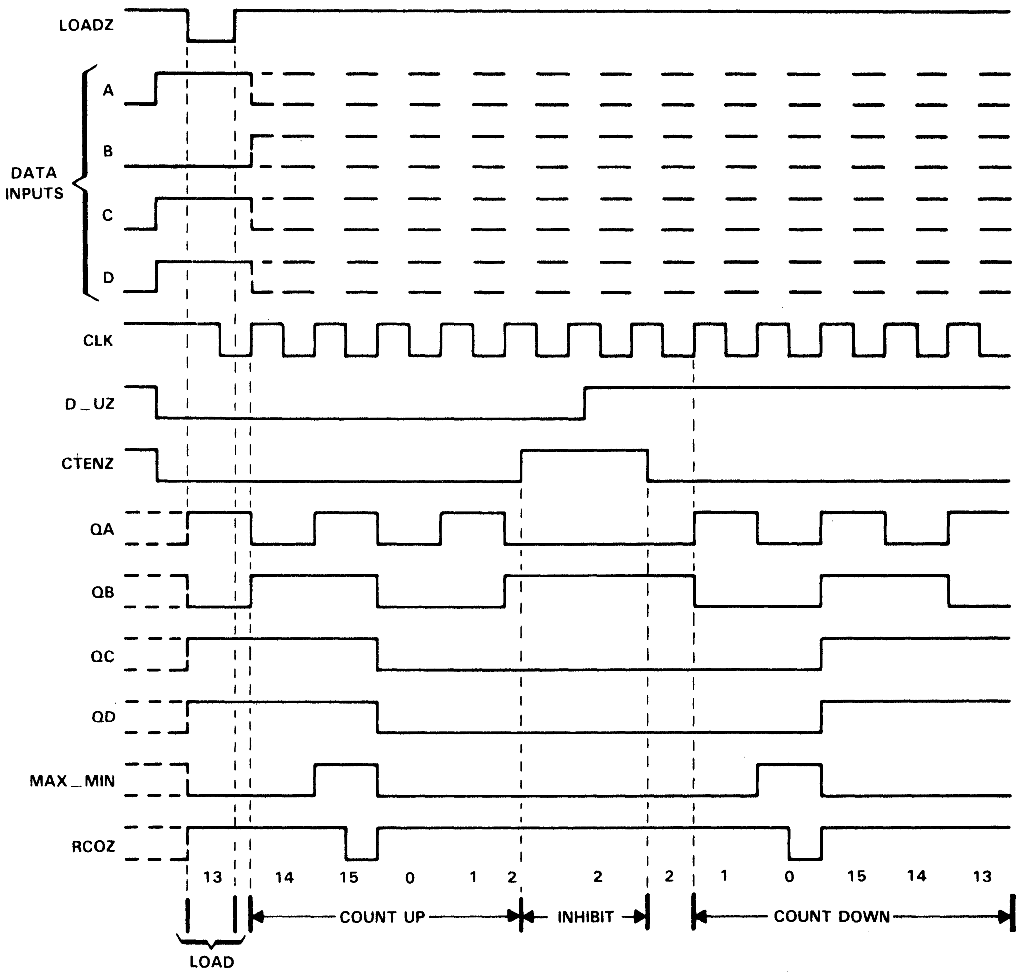
logic diagram



typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



S191LJ SYNCHRONOUS UP/DOWN BINARY COUNTER WITH DOWN/UP MODE CONTROL

D3015, OCTOBER 1987—REVISED OCTOBER 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	CTENZ		0.21		pF
		A,B,C,D		0.14		
		All others		0.07		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	23		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	LOADZ	Q		2.9	4.9	ns
t_{PHL}				2.7	5	
t_{PLH}	A,B,C,D	Q		1.7	2.9	ns
t_{PHL}				2.2	4.3	
t_{PLH}	CLK	RCOZ		1	1.5	ns
t_{PHL}				1.1	1.9	
t_{PLH}	CLK	Q		3.1	6.1	ns
t_{PHL}				3	5.5	
t_{PLH}	CLK	MAX_MIN		4.7	9	ns
t_{PHL}				3.9	7.5	
t_{PLH}	D_UZ	RCOZ		2.9	5.1	ns
t_{PHL}				3.7	6	
t_{PLH}	D_UZ	MAX_MIN		2.6	5.3	ns
t_{PHL}				2.5	4.4	
t_{PLH}	CTENZ	RCOZ		1.1	1.6	ns
t_{PHL}				1.1	1.9	
Δt_{PLH}	Any	Q	0.18	0.46	0.92	ns/pF
Δt_{PHL}			0.16	0.35	0.64	
Δt_{PLH}	Any	RCOZ	0.34	0.88	1.72	ns/pF
Δt_{PHL}			0.38	0.99	2.04	
Δt_{PLH}	Any	MAX_MIN	0.34	0.87	1.7	ns/pF
Δt_{PHL}			0.34	0.72	1.44	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

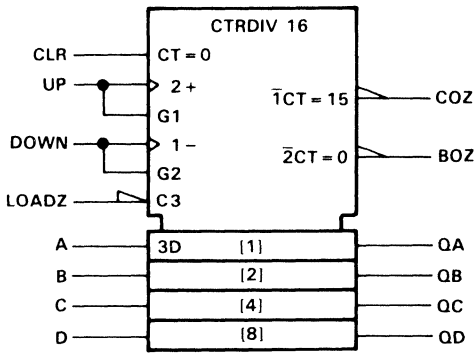
S193LJ SYNCHRONOUS 4-BIT UP/DOWN COUNTER (DUAL CLOCK WITH CLEAR)

D3015, OCTOBER 1987—REVISED OCTOBER 1988

SOFTWARE MACRO

- **Dual Clock Inputs for Sourcing Count Direction**
- **Fully Synchronous in Count Modes**
- **Parallel Asynchronous Load for Modulo-N Count Sequences**
- **Asynchronous Clear**
- **Look-Ahead Circuitry Enhances Performance of Cascaded Counters**

logic symbol†



Equivalent to 74193

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S193LJ gate-array software macro implements a synchronous, reversible up/down, 4-bit binary counter with dual clock inputs and a separate clear input. Its 4-bit length means that testability is simplified when constructing large counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters. The S193LJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
AN210LJ	2	7	14	3.08
AN310LJ	2	2	4	1.12
IV110LJ	1	4	4	0.84
IV120LJ	1	4	4	1.56
NA210LJ	1	4	4	1.08
NA310LJ	2	4	8	1.12
NA410LJ	2	2	4	0.58
NA510LJ	3	2	6	0.68
NO210LJ	1	3	3	0.54
TAB20LJ	9	4	36	12
TOTALS		36	87	22.6

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the counter is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

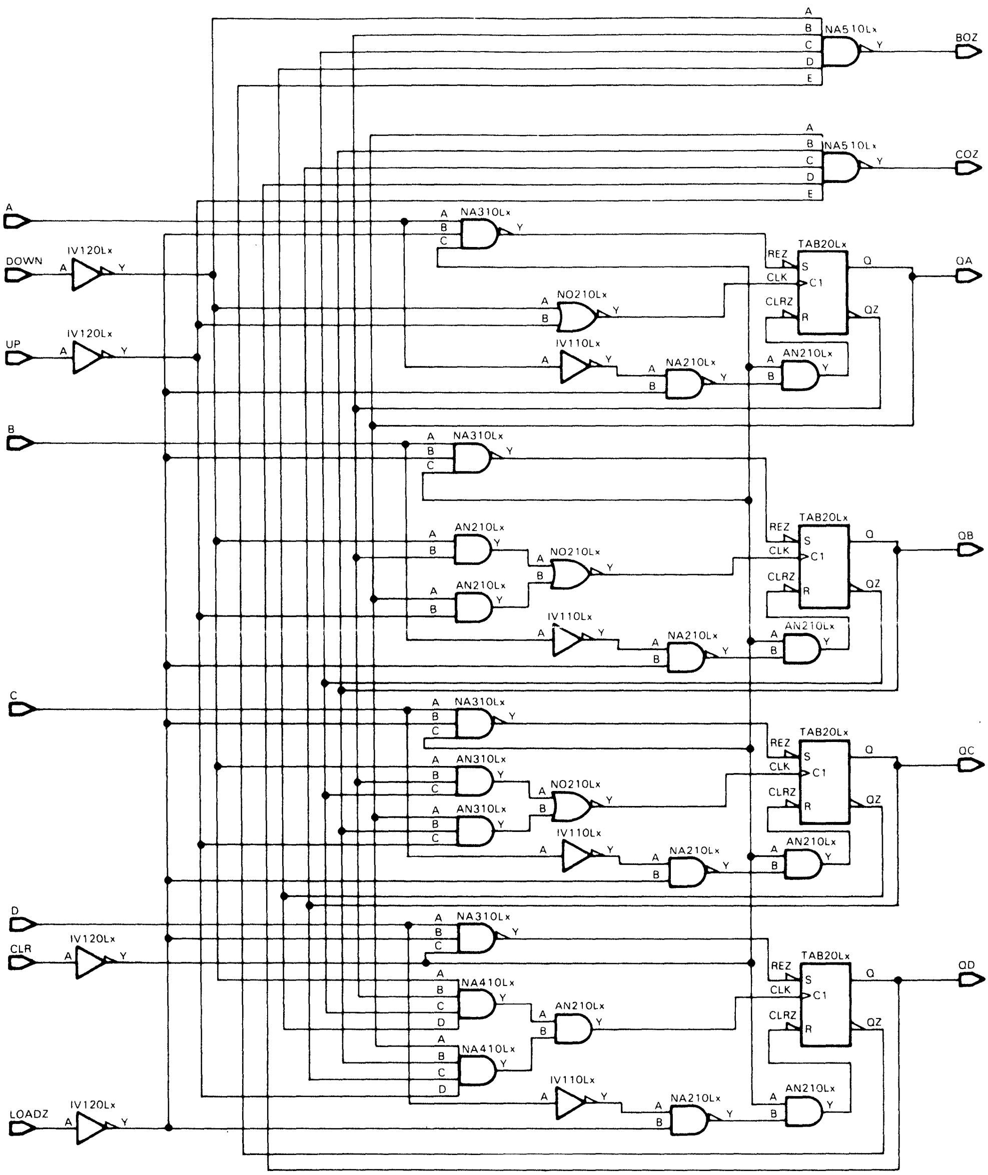
Label: S193LJ A,B,C,D,UP,DOWN,LOADZ,CLR,BOZ,COZ,QA,QB,QC,QD;

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (UP or DOWN). The direction of counting is determined by which count input is pulsed while the other count input is high. These counters are fully programmable; that is, they may be preset to any number between 0 and 15 by placing a low on the load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters are designed to be cascased without the need for additional circuitry. The borrow output (BOZ) produces a low-level pulse while the count is zero (all outputs low) and the count-down is low. Similarly, the carry output (COZ) produces a low-level pulse while the count is maximum (all outputs high) and the count-up input is low. The counters are cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

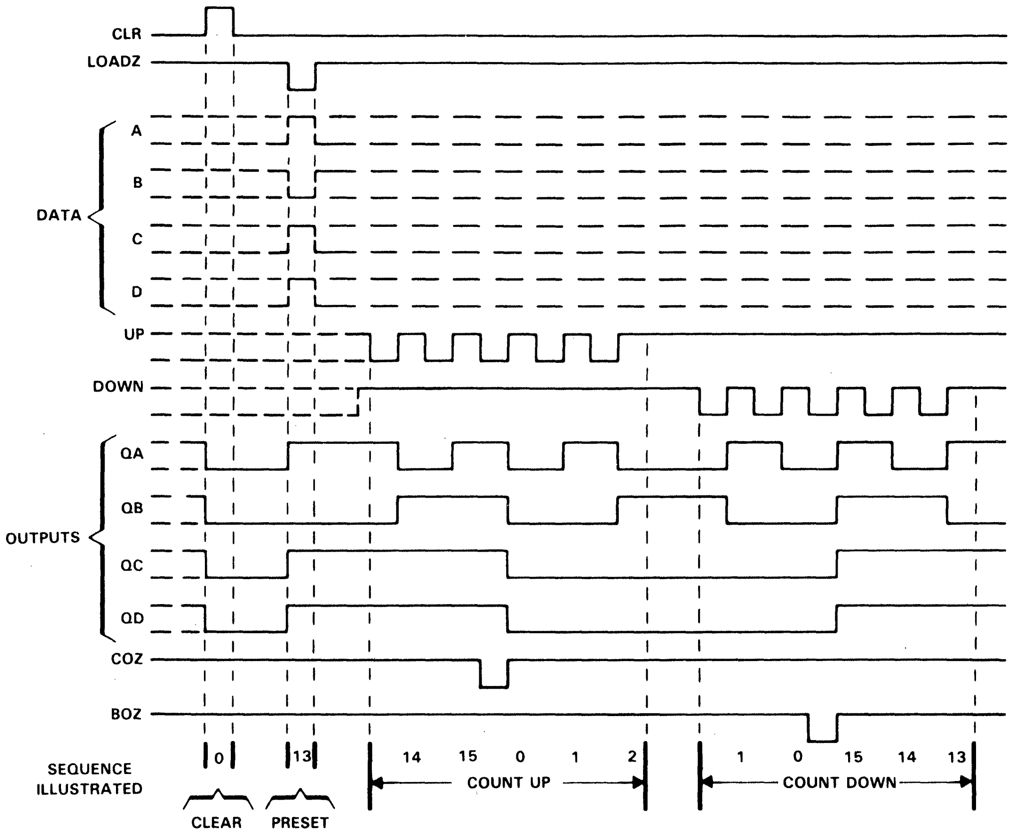
logic diagram



typical clear, load, and count sequences (see Notes A and B)

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Load (preset) to binary thirteen
3. Count up to fourteen, fifteen (carry), zero, one, and two
4. Count down to one, zero (borrow), fifteen, fourteen and thirteen.



NOTES: A. Clear overrides load, data and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	A,B,C,D		0.14		pF
		All others		0.15		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	22.6		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	UP	COZ		0.9	1.7	ns
t_{PHL}				1.2	2.3	
t_{PLH}	DOWN	BOZ		0.8	1.3	ns
t_{PHL}				1	1.8	
t_{PLH}	DOWN,UP	Q		3.8	7.4	ns
t_{PHL}				3.7	7.2	
t_{PLH}	LOADZ	Q		3.4	6	ns
t_{PHL}				3.4	6.3	
t_{PHL}	Any	Q		2.6	5	ns
Δt_{PLH}	Any	Q	0.2	0.48	0.98	ns/pF
Δt_{PHL}			0.18	0.44	0.84	
Δt_{PLH}	Any	BOZ,COZ	0.34	0.88	1.76	ns/pF
Δt_{PHL}			0.5	1.56	3.3	

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

D3015, OCTOBER 1987—REVISED OCTOBER 1988

DECODERS/DEMULTIPLEXERS

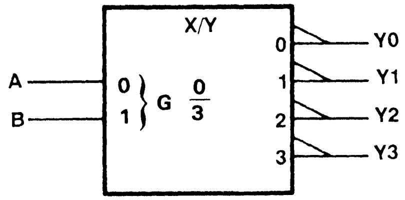
DESCRIPTION	MACRO NAME	OUTPUT DRIVE	COMMENTS	CELLS USED	PAGE
2- to 4-Line	DE210LJ	1X		5	16-3
3- to 8-Line	S138LJ	1X	3 Enables	25	16-4
Dual 2- to 4-Line	S139LJ	1X	1 Enable	26	16-7

INTERNAL DECODER/DEMULTIPLEXER MACRO

FUNCTION TABLE

INPUTS		OUTPUTS			
A	B	Y0	Y1	Y2	Y3
L	L	L	H	H	H
H	L	H	L	H	H
L	H	H	H	L	H
H	H	H	H	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DE210LJ is a 2-line to 4-line decoder/demultiplexer. When the decoder/demultiplexer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DE210LJ A,B,Y0,Y1,Y2,Y3;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.23		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	1.52		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B	Y	0.2	0.39	0.97	ns
t_{PHL}			0.16	0.47	1.18	
Δt_{PLH}	A,B	Y	0.2	0.87	1.7	ns/pF
Δt_{PHL}			0.32	0.73	1.46	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

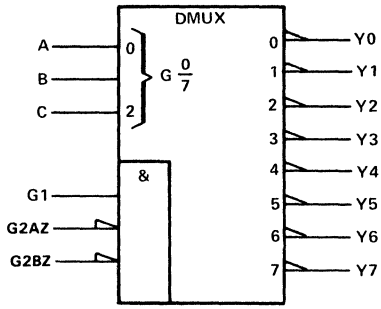
3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

D3015, OCTOBER 1987—REVISED OCTOBER 1988

SOFTWARE MACRO

- Three Enable Inputs for Expandability
- Choice of an Active-High or Two Active-Low Enables
- Use Decoders in Parallel for Multiple Bit Words

logic symbol†



Equivalent to 74138

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S138LJ gate-array software macro implements a 3-line to 8-line decoder/demultiplexer. Also provided in the macro are strobe inputs, G1, G2AZ, and G2BZ, which enable and disable the outputs. All of the outputs are disabled (high), unless G1 is high and G2AZ and G2BZ are low. When enabled, the selected output assumes a low logic level. These strobes also permit the S138LJ to be cascaded to accommodate wider multiplexers, as only the enabled 8-bit field will contain an active data bit. The S138LJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
IV110LJ	1	1	1	0.21
IV120LJ	1	6	6	2.34
NA410LJ	2	8	16	2.32
NO310LJ	2	1	2	0.21
TOTALS		16	25	5.08

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the decoder is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S138LJ G1,G2AZ,G2BZ,A,B,C,Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7;

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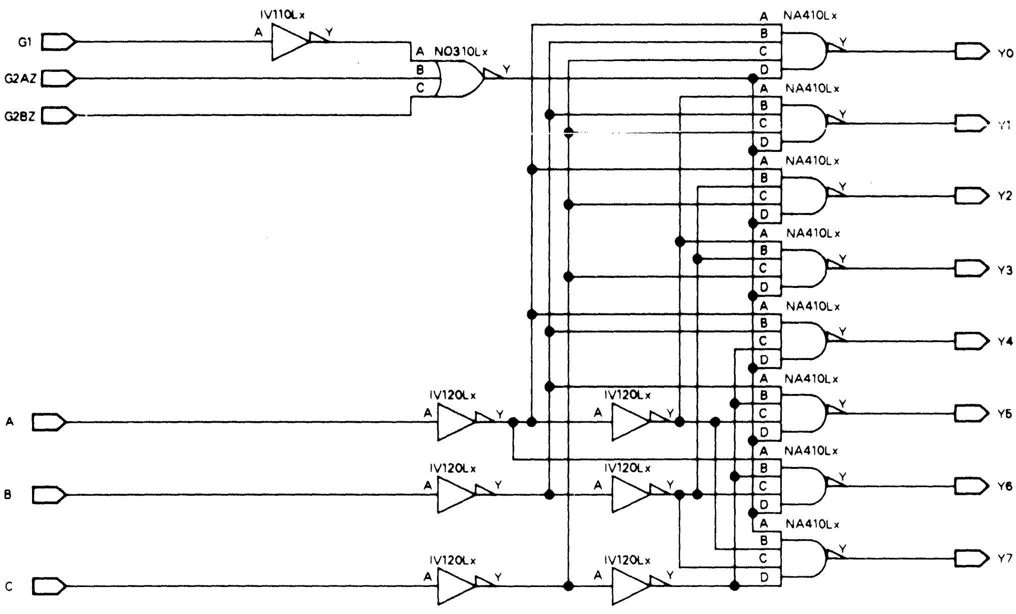
D3015, OCTOBER 1987

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	G2AZ	G2BZ	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

logic diagram



Lx = LJ for 1-μm gate arrays

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absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	G1,G2AZ,G2BZ		0.07		pF
		A,B,C		0.15		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	5.08		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A	Any		1.3	2.2	ns
t_{PHL}				1.5	2.6	
t_{PLH}	B	Any		1.4	2.3	ns
t_{PHL}				1.5	2.5	
t_{PLH}	C	Any		1.4	2.5	ns
t_{PHL}				1.5	2.5	
t_{PLH}	G1	Any		1.6	2.5	ns
t_{PHL}				2.7	5.3	
t_{PLH}	G2AZ,G2BZ	Any		1.1	1.8	ns
t_{PHL}				2.3	4.7	
Δt_{PLH}	Any	Any	0.34	0.88	1.74	ns/pF
Δt_{PHL}			0.44	1.27	2.66	

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

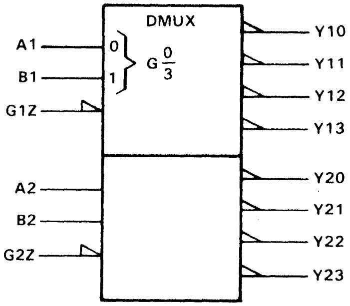
DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

D3015, OCTOBER 1987

SOFTWARE MACRO

- **Enable Input Permits Expansion of Each Decoder**
- **Use Decoders in Parallel for Multiple Bit Words**

logic symbol†



Equivalent to 74139

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S139LJ gate-array software macro implements a dual 2-line to 4-line decoder/demultiplexer. Also provided in the macro are two strobe inputs, G1Z and G2Z, that enable and disable the outputs. The four outputs of a decoder are high when its corresponding strobe is high. When the strobe is low, the selected output is low. These strobes, G1Z for decoder 1 and G2Z for decoder 2, permit the S139LJ decoders to be cascaded to accommodate wider multiplexers, as only the enabled 4-bit field will contain an active data bit. The S139LJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
IV110LJ	1	4	4	0.84
IV120LJ	1	6	6	2.34
NA310LJ	2	8	16	4.48
TOTALS		18	26	7.66

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the decoder is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

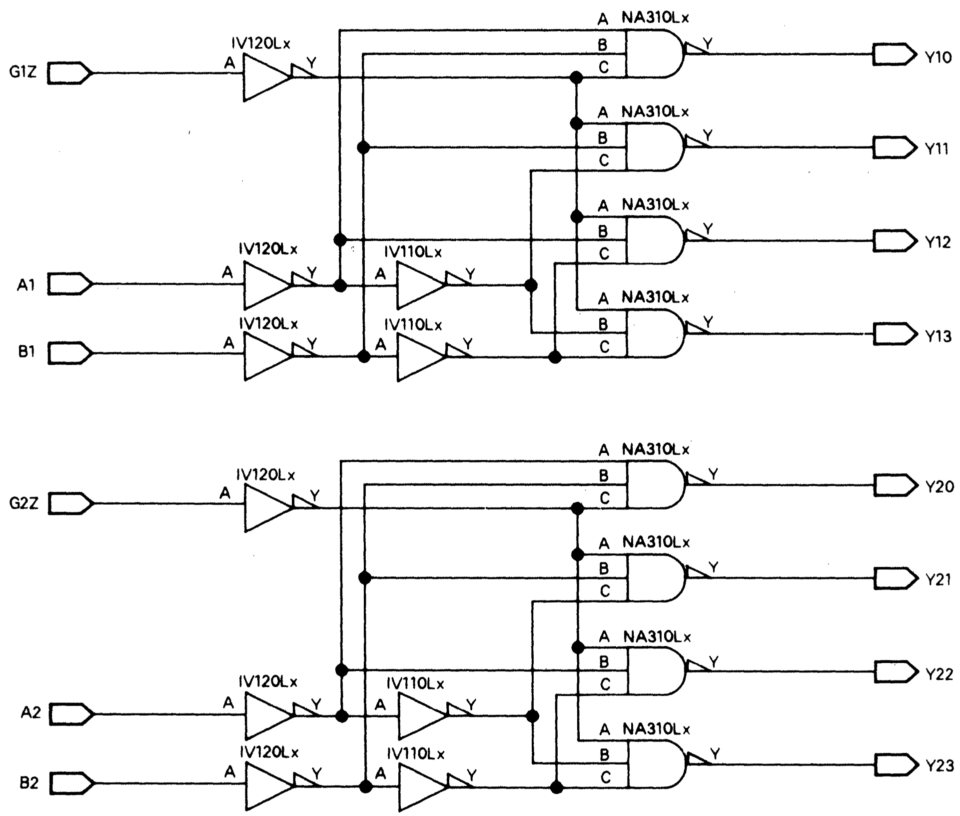
Label: S139LJ A1,B1,G1Z,A2,B2,G2Z,Y10,Y11,Y12,Y13,Y20,Y21,Y22,Y23;

D3015, OCTOBER 1987

FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
GnZ	Bn	An	Yn0	Yn1	Yn2	Yn3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

logic diagram



DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

D3015, OCTOBER 1987

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	A1,A2,B1,B2		0.07		pF
		G1Z,G2Z		0.15		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	7.66		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A or B	Any		1.3	2.1	ns
t_{PHL}				1.4	2.4	
t_{PLH}	GZ	Any		0.8	1.4	ns
t_{PHL}				0.8	1.4	
Δt_{PLH}	Any	Any	0.34	0.88	1.72	ns/pF
Δt_{PHL}			0.38	0.99	2.04	

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

D3015, OCTOBER 1987—REVISED OCTOBER 1988

MULTIPLEXERS

DESCRIPTION	MACRO NAME	OUTPUTS	OUTPUT DRIVE	COMMENTS	CELLS USED	PAGE
2- to 1-Line	MU111LJ	Y	1X	Low Enable	3	17-3
4- to 1-Line	MU220LJ	Y	1X		7	17-4
8- to 1-Line	MU311LJ	Y	1X	Low Enable	13	17-6
16- to 1-Line	S150LJ	W	2X	Low Enable	123	17-8
8- to 1-Line	S151LJ	Y,W	2X		40	17-12
Dual 4- to 1-Line	S153LJ	Yn	1X	Strobe	26	17-16
Quad 2- to 1-Line	S157LJ	Yn	1X		18	17-19

MU111LJ
2-LINE TO 1-LINE MULTIPLEXER

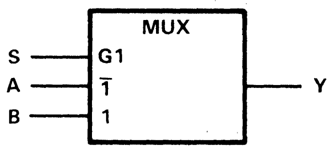
D3015, OCTOBER 1987

INTERNAL MULTIPLEXER MACRO

FUNCTION TABLE

INPUT S	OUTPUT Y
L	A
H	B

logic symbol†



Similar to 1/4 of 74157

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The MU111LJ is an internal 2-line to 1-line multiplexer. When the multiplexer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: MU111LJ A,B,S,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			1.8		V
C_i	Input capacitance	A,B		0.07		pF
		S		0.18		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	0.68		pF

‡For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B	Y	0.23	0.62	1.36	ns
t_{PHL}			0.28	0.81	1.87	
t_{PLH}	S	Y	0.2	0.51	1	ns
t_{PHL}			0.36	0.83	1.36	
Δt_{PLH}	A,B	Y	0.36	0.89	1.72	ns/pF
Δt_{PHL}			0.26	0.57	1.1	
Δt_{PLH}	S	Y	0.36	0.9	1.72	ns/pF
Δt_{PHL}			0.28	0.6	1.14	

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

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MU220LJ
4-LINE TO 1-LINE MULTIPLEXER WITH 1X OUTPUT

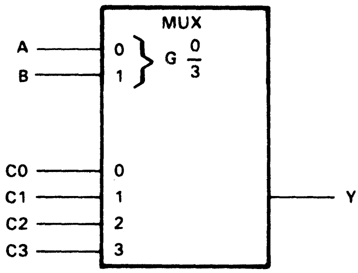
D3015, OCTOBER 1988

SOFTWARE MACRO

FUNCTION TABLE

INPUTS		OUTPUT
B	A	Y
L	L	C0
L	H	C1
H	L	C2
H	H	C3

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The MU220LJ is an internal 4-line to 1-line multiplexer. When the multiplexer is called from the engineering work-station input, the following label format is developed and will be captured in the design netlist:

Label: MU220LJ C0,C1,C2,C3,A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	A		0.24		pF
		B		0.15		
		Any C		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.4		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	A,B	Y	0.24	0.75	1.65	ns
t_{PHL}			0.33	0.88	2.19	
t_{PLH}	Any C	Y	0.42	0.95	1.87	ns
t_{PHL}			0.45	1.11	2.33	
Δt_{PLH}	Any		0.17	0.47	0.94	ns/pF
Δt_{PHL}			0.16	0.49	1	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

MU311LJ
8-LINE TO 1-LINE MULTIPLEXER

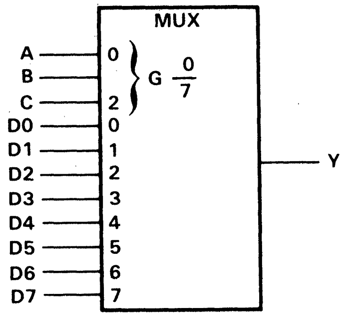
D3015, OCTOBER 1988

INTERNAL MULTIPLEXER MACRO

FUNCTION TABLE

INPUTS			OUTPUT
C	B	A	Y
X	X	X	L
L	L	L	D0
L	L	H	D1
L	H	L	D2
L	H	H	D3
H	L	L	D4
H	L	H	D5
H	H	L	D6
H	H	H	D7

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The MU311LJ is an internal 8-line to 1-line multiplexer. When the multiplexer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: MU311LJ D0,D1,D2,D3,D4,D5,D6,D7,A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	A		0.42		pF
		B		0.24		
		C		0.16		
		D0 thru D7		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	1.32		pF

‡ For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	A,B,C	Y	0.23	0.85	2.4	ns
t_{PHL}			0.34	1.12	3.39	
t_{PLH}	D0-D7	Y	0.53	1.28	2.61	ns
t_{PHL}			0.54	1.5	3.27	
Δt_{PLH}	Any	Y	0.35	0.91	1.81	ns/pF
Δt_{PHL}			0.32	0.88	1.8	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

S150LJ
16-LINE TO 1-LINE MULTIPLEXER

D3015, OCTOBER 1987

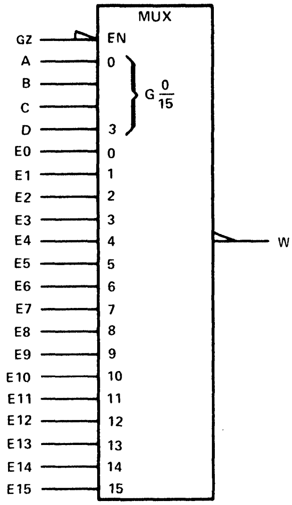
SOFTWARE MACRO

- **Active-Low Strobe for Expandability**
- **Use Multiplexers in Parallel for Multiple-Bit Words**

description

The S150LJ gate-array software macro implements a 16-line to 1-line multiplexer. The macro has a strobe input, GZ, that enables and disables the inputs. The W output is high when GZ is high. When GZ is low, the W output assumes the level of the selected input. This strobe permits the macro to be employed for designing wider multiplexers, as only the enabled 16-bit field will output an active data bit. The S150LJ is implemented with the macro functions indicated.

logic symbol†



Equivalent to 74150

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
IV110LJ	1	1	1	0.21
IV120LJ	1	10	10	3.9
NA810LJ	6	18	108	21.6
OR210LJ	2	1	2	0.48
TO010LJ	2	1	2	–
TOTALS		31	123	26.19

‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S150LJ 16-LINE TO 1-LINE MULTIPLEXER

D3015, OCTOBER 1987

When the multiplexer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S150LJ GZ,E0,E1,E2,E3,E4,E5,E6,E7,E8,E9,E10,E11, E12,E13,E14,E15,A,B,C,D,W;

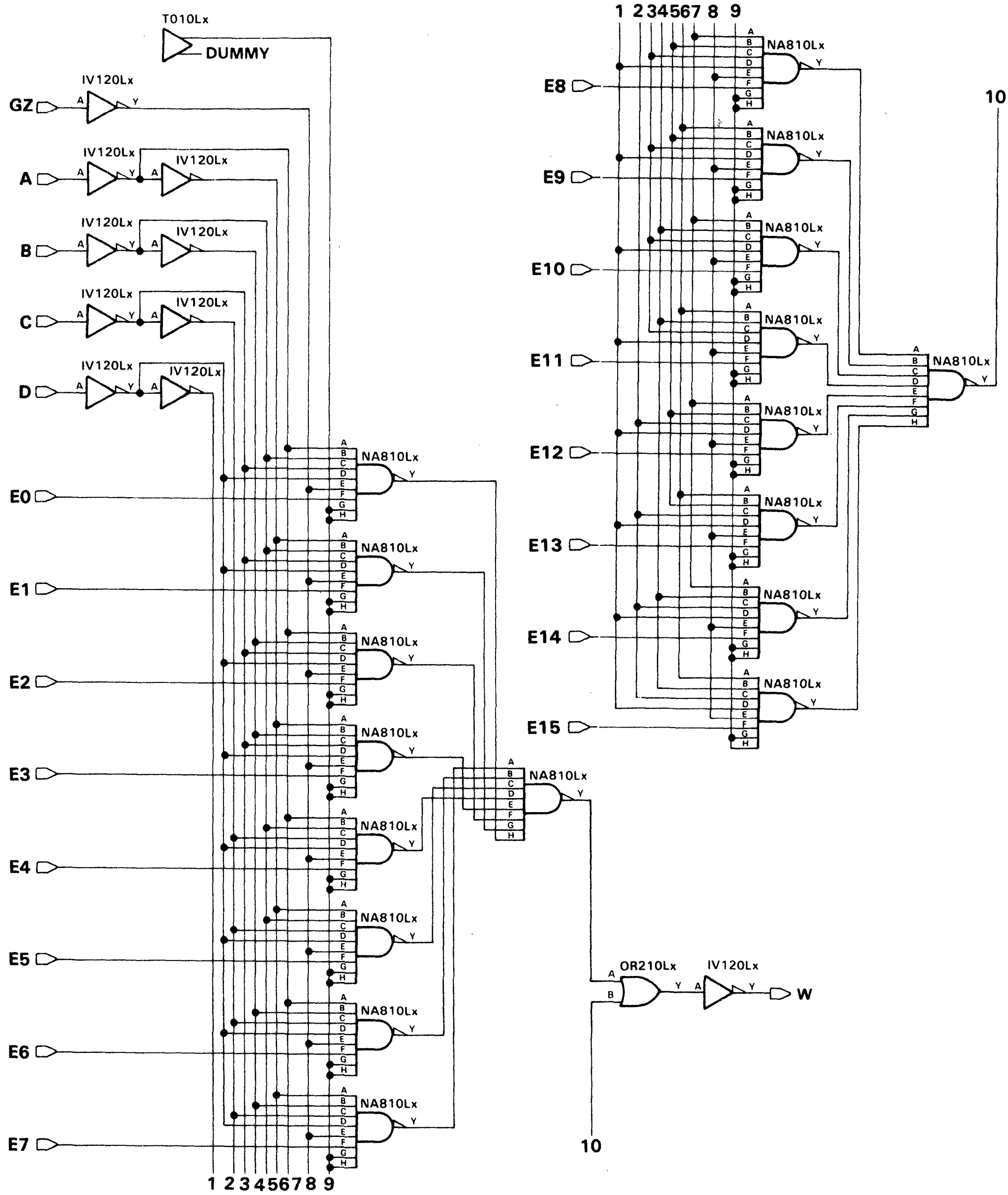
FUNCTION TABLE

INPUTS					OUTPUT
SELECT				STROBE	W
D	C	B	A	GZ	
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

See explanation of Function Tables in Section 1.
E0, E1. . .E15 = the level of the respective E input.

D3015, OCTOBER 1987

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	GZ,A,B,C,D		0.15		pF
		All others		0.07		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	26.19		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A,B,C or D	W		4.3	8.2	ns
t_{PHL}				4.5	9	
t_{PLH}	Any E	W		3.1	6.2	ns
t_{PHL}				3.3	6.9	
t_{PLH}	GZ	W		4.2	8	ns
t_{PHL}				4.8	8.8	
Δt_{PLH}	Any	W	0.22	0.44	0.84	ns/pF
Δt_{PHL}			0.22	0.32	0.44	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

S151LJ
8-LINE TO 1-LINE MULTIPLEXER

D3015, OCTOBER 1987

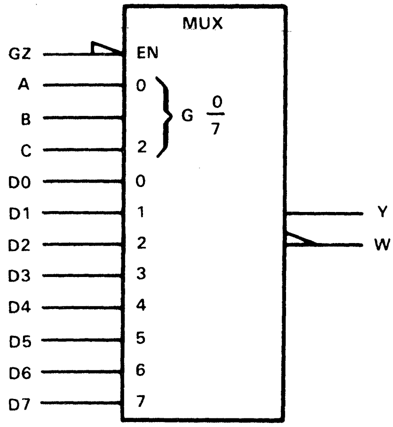
SOFTWARE MACRO

- **Active-Low Strobe for Expandability**
- **Use Multiplexers in Parallel for Multiple-Bit Words**

description

The S151LJ gate-array software macro implements a 8-line to 1-line multiplexer. The macro has a strobe input, GZ, that enables and disables the inputs. When GZ is high, the Y output is low and the W output is high. When GZ is low, the Y output assumes the level of the selected input and the W output assumes the complement of that level. This strobe permits the macro to be employed for designing wider multiplexers, as only the enabled 8-bit field will output an active data bit. The S151LJ is implemented with the macro functions indicated.

logic symbol†



Equivalent to 74151

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
IV120LJ	1	10	10	3.9
NA510LJ	3	8	24	2.72
NA810LJ	6	1	6	1.2
TOTALS		19	40	7.82

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the multiplexer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S151LJ GZ,A,B,C,D0,D1,D2,D3,D4,D5,D6,D7,Y,W;

TEXAS INSTRUMENTS
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S151LJ
8-LINE TO 1-LINE MULTIPLEXER

D3015, OCTOBER 1987

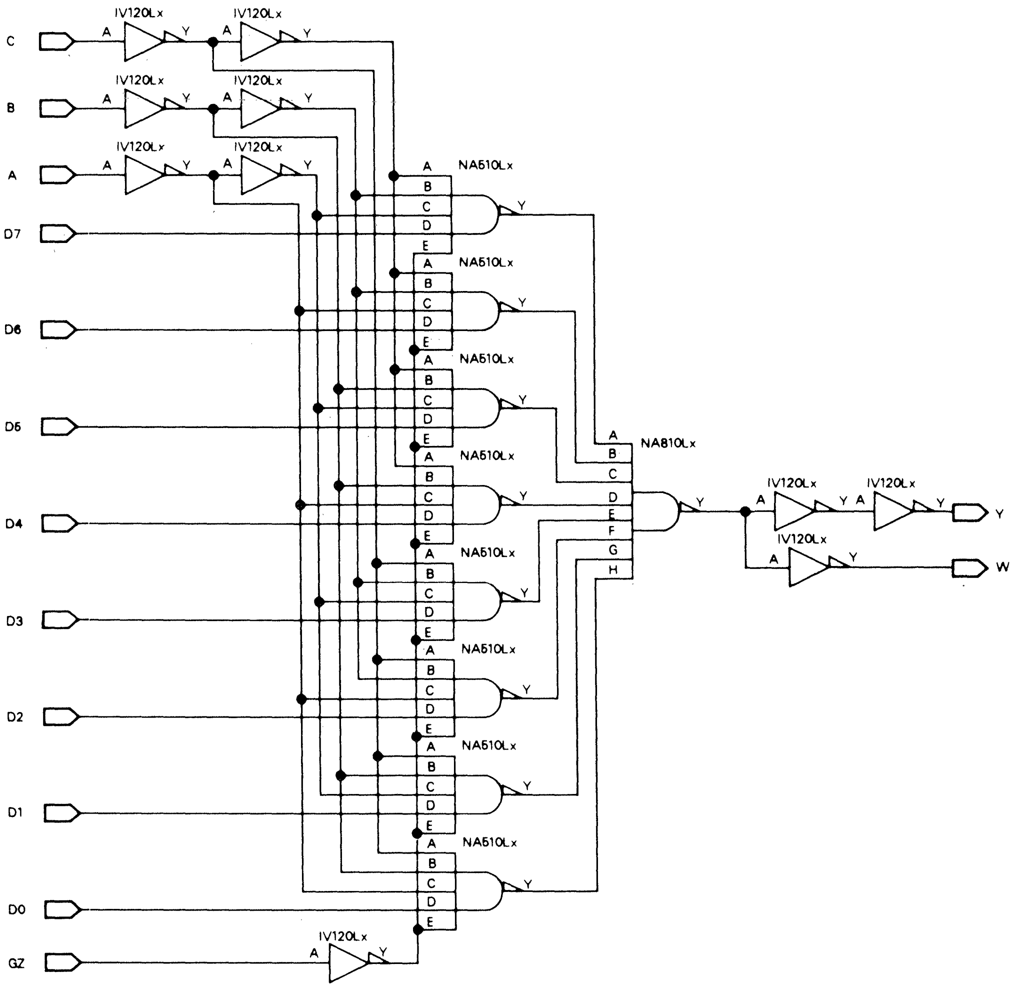
FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	GZ	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

D0, D1 . . . D7 - the level of the respective D input.

D3015, OCTOBER 1987

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	GZ		0.15		pF
		All others		0.07		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f$ = 1 ns	7.82		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A, B, or C	Y		3.3	6.5	ns
t_{PHL}				3.3	6.3	
t_{PLH}		W		3.5	6.6	ns
t_{PHL}				3.5	6.8	
t_{PLH}	Any D	Y		2.4	4.9	ns
t_{PHL}				2.3	4.7	
t_{PLH}		W		2.5	5.2	ns
t_{PHL}				2.6	5	
t_{PLH}	GZ	Y		3.1	6.1	ns
t_{PHL}				2.8	5.5	
t_{PLH}		W		3	5.8	ns
t_{PHL}				3.3	6.4	
Δt_{PLH}	Any	Y	0.22	0.44	0.84	ns/pF
Δt_{PHL}			0.22	0.32	0.44	
Δt_{PLH}	Any	W	0.22	0.44	0.84	ns/pF
Δt_{PHL}			0.22	0.32	0.44	

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

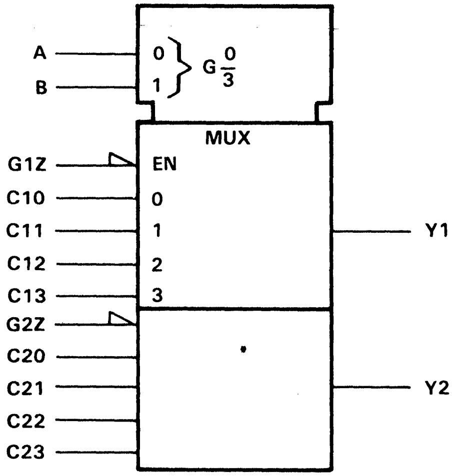
NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

D3015, OCTOBER 1987

SOFTWARE MACRO

- **Active-Low Strobe for Expandability**
- **Use Multiplexers in Parallel for Multiple-Bit Words**

logic symbol†



Equivalent to 74153

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S153LJ gate-array software macro implements a dual 4-line to 1-line multiplexer. Each 4-bit half of the macro has a strobe input, GnZ, that enables and disables its associated inputs. The Yn output is low when GnZ is high. When GnZ is low, the output assumes the level of the selected input. These strobes permit the macro to be employed for designing wider multiplexers, as only the enabled 4-bit field will output and active data bit. The S153LJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
IV120LJ	1	6	6	2.34
NA410LJ	2	10	20	2.9
TOTALS		16	26	5.24

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the multiplexer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S153LJ G1Z,G2Z,A,B,C10,C11,C12,C13,C20,C21,C22,C23,Y1,Y2;

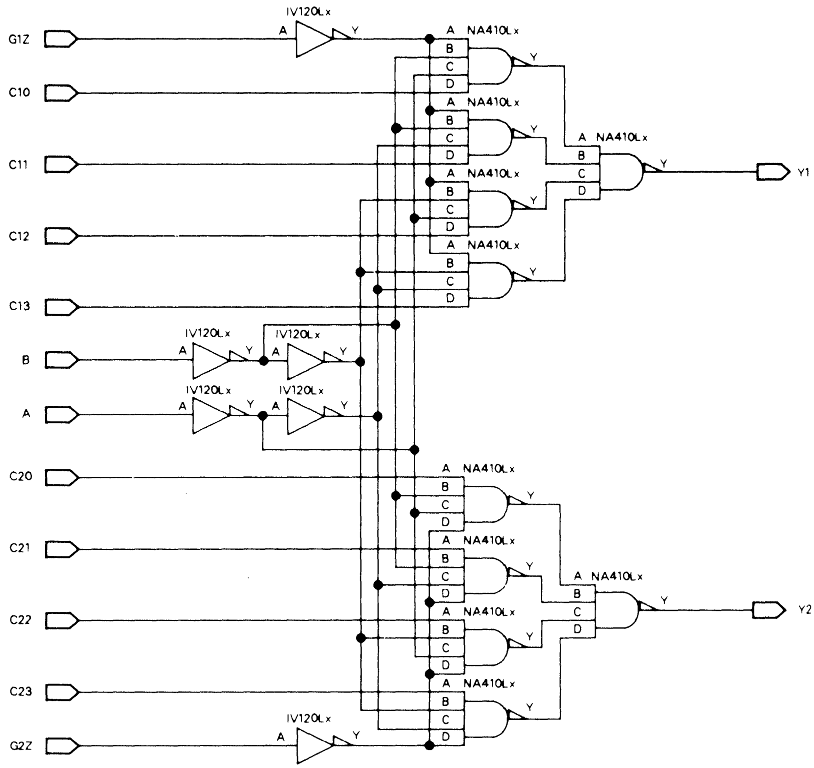
S153LJ
DUAL 4-LINE TO 1-LINE MULTIPLEXER

D3015, OCTOBER 1987

FUNCTION TABLE

INPUTS						STROBE	OUTPUT
SELECT		DATA				GnZ	Yn
B	A	Cn0	Cn1	Cn2	Cn3		
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

logic diagram



D3015, OCTOBER 1987

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†		TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance‡	$t_r = t_f = 1$ ns	5.24		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A or B	Y		2.4	4.1	ns
t_{PHL}				2.2	3.9	
t_{PLH}	C	Y		1.4	2.6	ns
t_{PHL}				1.3	2.3	
t_{PLH}	G1Z or G2Z	Y		1.9	3.4	ns
t_{PHL}				1.7	2.9	
Δt_{PLH}	Any	Y	0.34	0.88	1.74	ns/pF
Δt_{PHL}			0.44	1.27	2.66	

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

S157LJ
QUADRUPLE 2-LINE TO 1-LINE NONINVERTING MULTIPLEXER

D3015, OCTOBER 1987

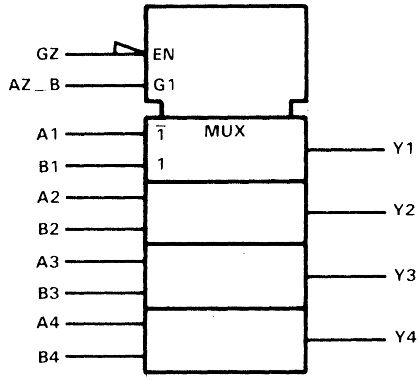
SOFTWARE MACRO

- **Active-Low Strobe for Expandability**
- **Use Multiplexers in Parallel for Multiple-Bit Words**

description

The S157LJ gate-array software macro implements a quadruple 2-line to 1-line multiplexer. The macro has a strobe input, GZ, that enables and disables the outputs. The Y outputs are forced low when GZ is high. When GZ is low, the outputs assume the level of the selected inputs. This strobe permits the macro to be employed for designing wider multiplexers, as only the enabled 4-bit field will output an active data bit. The S157LJ is implemented with the macro functions indicated.

logic symbol†



Equivalent to 74157

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
IV110LJ	1	2	2	0.42
IV120LJ	1	2	2	0.78
NA210LJ	1	14	14	3.78
TOTALS		18	18	4.98

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the multiplexer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S157LJ A1,A2,A3,A4,B1,B2,B3,B4,AZ_B,GZ,Y1,Y2,Y3,Y4;

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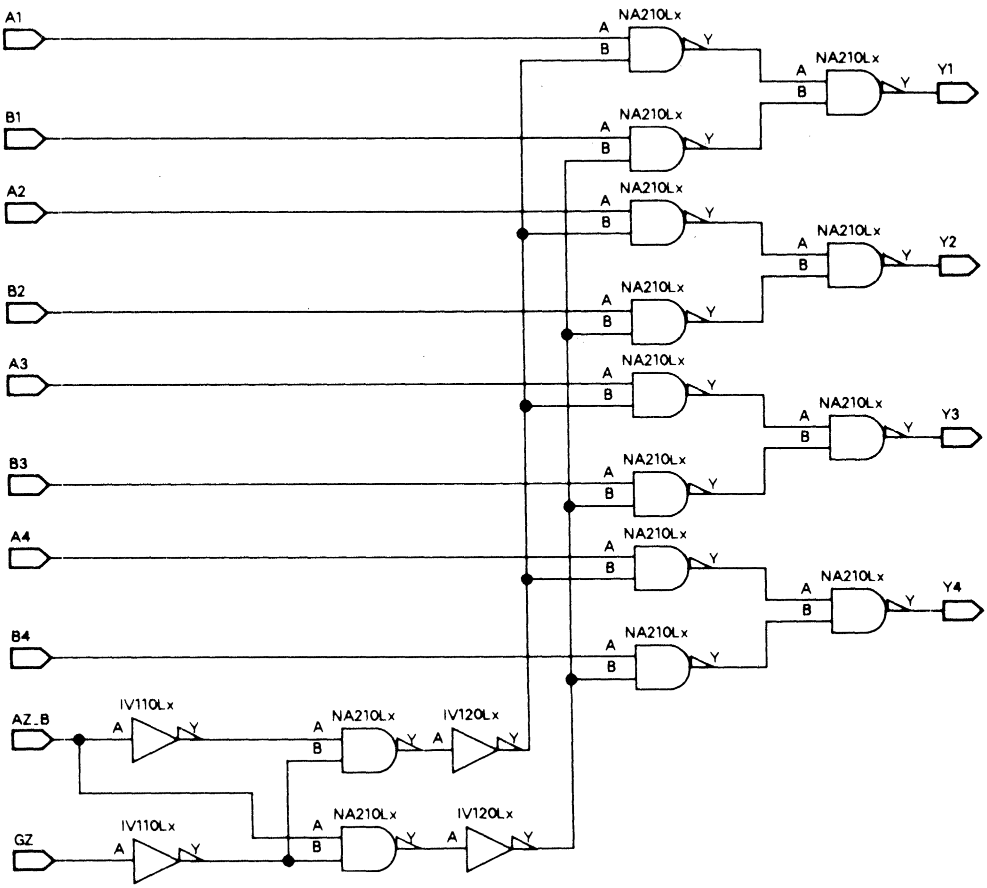
S157LJ QUADRUPLE 2-LINE TO 1-LINE NONINVERTING MULTIPLEXER

D3015, OCTOBER 1987

FUNCTION TABLE

INPUTS				OUTPUT
STROBE GZ	SELECT AZ_B	DATA An	DATA Bn	Yn
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	AZ_B		0.14		pF
		All others		0.07		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	4.98		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	A or B	Y		0.8	1.4	ns
t_{PHL}				0.9	1.4	
t_{PLH}	AZ_B	Y		2.5	4.1	ns
t_{PHL}				2.4	3.9	
t_{PLH}	GZ	Y		2.5	4.1	ns
t_{PHL}				2.4	3.9	
Δt_{PLH}	Any	Y	0.34	0.87	1.7	ns/pF
Δt_{PHL}			0.34	0.72	1.44	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

REGISTERS FUNCTIONAL INDEX

D3015, OCTOBER 1987—REVISED OCTOBER 1988

REGISTERS (HARDWIRED)

DESCRIPTION	MACRO NAME	f_{clock} (MHz)	OUTPUTS	OUTPUT DRIVE	COMMENTS	CELLS USED	PAGE
4-Bit D-Type	R2401LJ	135	Qn	1X	Async Clear	26	18-3
	R2402LJ	135	Qn,QnZ	1X		27	18-5
	R2403LJ	135	Qn	1X		27	18-7
	R2404LJ	135	Qn,QnZ	1X		31	18-9
	R2405LJ	135	Qn	1X	Async Clear	26	18-11
	R2406LJ	135	Qn, QnZ	1X		28	18-13

REGISTERS (SOFTWARE)

DESCRIPTION	MACRO NAME	OUTPUTS	OUTPUT DRIVE	COMMENTS	CELLS USED	PAGE
8-Bit Parallel Out SR	S164LJ	Qn	2X	Async Clear	88	18-15
8-Bit Parallel Load SR	S165ALJ	QH, QHZ	2X	Clock Inhibit	124	18-19
4-Bit Directional SR	S194ALJ	Qn	1X	Async Clear	73	18-23

R2401LJ
4-BIT SHIFT REGISTER
WITH SERIAL INPUT AND ASYNCHRONOUS CLEAR

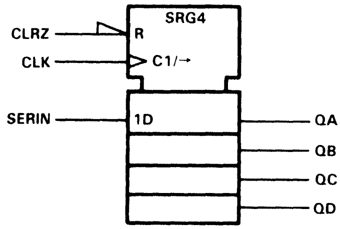
D3015, OCTOBER 1988

INTERNAL REGISTER HARDWIRED MACRO

FUNCTION TABLE

INPUTS			OUTPUTS			
CLRZ	CLK	SERIN	QA	QB	QC	QD
L	X	X	L	L	L	L
H	↑	H	H	QA_n	QB_n	QC_n
H	↑	L	L	QA_n	QB_n	QC_n
H	L	X	Q_0	Q_0	Q_0	Q_0

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The R2401LJ macro implements a 4-bit serial-input shift register with true outputs. Its 4-bit length simplifies construction of large registers. The register contains an embedded clock driver that buffers the clock input so that standard library buffers can be used to drive multiple clock inputs. When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: R2401LJ CLRZ,SERIN,CLK,QA,QB,QC,QD;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	135	MHz
t_w	Pulse duration	CLRZ low	2		ns
		CLK (H or L)	3.7		
t_{su}	Setup time before clock	SERIN (H or L)	2		ns
		CLRZ inactive	0		
t_h	Hold time after clock	SERIN (H or L)	0		ns
		CLRZ active	2		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLK		0.16		pF
		CLRZ		0.75		
		SERIN		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	6.4		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
t_{PLH}	CLK	Q	0.53	1.38	2.77	ns
t_{PHL}			0.57	1.59	3.21	
t_{PHL}	CLRZ	Q	0.33	0.71	1.34	ns
Δt_{PLH}	CLK	Q	0.36	0.89	1.73	ns/pF
Δt_{PHL}	CLRZ	Q	0.26	0.51	0.95	ns/pF
Δt_{PHL}			0.26	0.53	0.97	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

R2402LJ 4-BIT SHIFT REGISTER WITH SERIAL INPUT AND COMPLEMENTARY OUTPUTS

D3015, OCTOBER 1988

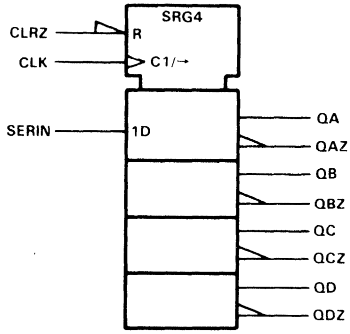
INTERNAL REGISTER HARDWIRED MACRO

FUNCTION TABLE

INPUTS			OUTPUTS			
CLRZ	CLK	SERIN	QA*	QB*	QC*	QD*
L	X	X	L	L	L	L
H	↑	H	H	QA_n	QB_n	QC_n
H	↑	L	L	QA_n	QB_n	QC_n
H	L	X	Q_0	Q_0	Q_0	Q_0

*The QXZ output is the complement of QX.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The R2402LJ macro implements a 4-bit serial-input shift register with complementary outputs. Its 4-bit length simplifies construction of large registers. The register contains an embedded clock driver that buffers the clock input so that standard library buffers can be used to drive multiple clock inputs. When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: R2402LJ CLRZ,SERIN,CLK,QA,QAZ,QB,QBZ,QC,QCZ,QD,QDZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	135	MHz
t_w	Pulse duration	CLRZ low	2		ns
		CLK (H or L)	3.7		
t_{su}	Setup time before clock	SERIN (H or L)	2		ns
		CLRZ inactive	0		
t_h	Hold time after clock	SERIN (H or L)	0		ns
		CLRZ active	2		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLK		0.16		pF
		CLRZ		0.75		
		SERIN		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	6.8		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
t_{PLH}	CLK	Q	0.53	1.49	3.07	ns
t_{PHL}			0.57	1.66	3.43	
t_{PLH}	CLK	QZ	0.68	1.86	3.85	ns
t_{PHL}			0.64	1.7	3.44	
t_{PLH}	CLRZ	QZ	0.42	1.08	2.15	ns
t_{PHL}	CLRZ	Q	0.33	0.77	1.47	
Δt_{PLH}	CLK	Q	0.36	0.89	1.74	ns/pF
Δt_{PHL}			0.26	0.55	1.01	
Δt_{PLH}	CLK	QZ	0.36	0.88	1.7	ns/pF
Δt_{PHL}			0.24	0.51	0.92	
Δt_{PLH}	CLRZ	QZ	0.36	0.88	1.72	ns/pF
Δt_{PHL}	CLRZ	Q	0.26	0.6	1.19	ns/pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

R2403LJ
4-BIT SHIFT REGISTER WITH SERIAL AND PARALLEL INPUTS

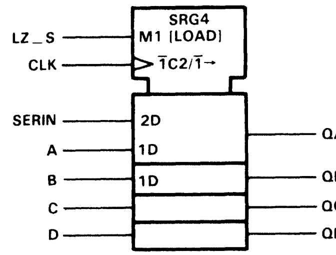
D3015, OCTOBER 1988

INTERNAL REGISTER HARDWIRED MACRO

FUNCTION TABLE

INPUTS							OUTPUTS			
			DATA							
LZ_S	CLK	SERIN	A	B	C	D	QA	QB	QC	QD
L	↑	X	a	b	c	d	a	b	c	d
H	↑	H	X	X	X	X	H	QA_n	QB_n	QC_n
H	↑	L	X	X	X	X	L	QA_n	QB_n	QC_n
X	L	X	X	X	X	X	Q_0	Q_0	Q_0	Q_0

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The R2403LJ macro implements a 4-bit serial-input or parallel-input shift register with true outputs. The 4-bit length simplifies construction of large registers. The register contains an embedded clock driver that buffers the clock input so that standard library buffers can be used to drive multiple clock inputs, which are used in the longer registers. When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: R2403LJ SERIN,LZ_S,CLK,A,B,C,D,QA,QB,QC,QD;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	135	MHz
t_w	Pulse duration	CLK (H or L)	3.7		ns
t_{su}	Setup time before clock	SERIN (H or L)	2		ns
		LZ_S (H or L)	4		
		A..D (H or L)	2		
t_h	Hold time after clock	SERIN (H or L)	0		ns
		LZ_S (H or L)	0		
		A..D (H or L)	0		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.16		pF
		Dn		0.09		
		LZ_S		0.07		
		SERIN		0.12		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	6		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
t_{PLH}	CLK	Q	0.52	1.25	2.46	ns
t_{PHL}			0.58	1.58	3.19	
Δt_{PLH}	CLK	Q	0.35	0.89	1.71	ns/pF
Δt_{PHL}			0.26	0.51	0.93	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

R2404LJ
4-BIT SHIFT REGISTER WITH SERIAL/ PARALLEL INPUTS AND COMPLEMENTARY OUTPUTS

D3015, OCTOBER 1988

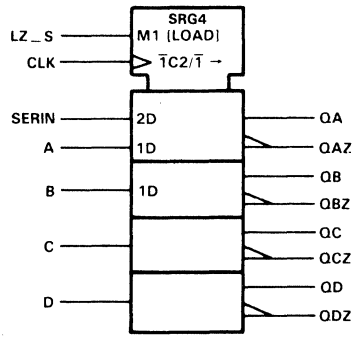
INTERNAL REGISTER HARDWIRED MACRO

FUNCTION TABLE

INPUTS							OUTPUTS			
			DATA							
LZ_S	CLK	SERIN	A	B	C	D	QA*	QB*	QC*	QD*
L	↑	X	a	b	c	d	a	b	c	d
H	↑	H	X	X	X	X	H	QA_n	QB_n	QC_n
H	↑	L	X	X	X	X	L	QA_n	QB_n	QC_n
X	L	X	X	X	X	X	Q_0	Q_0	Q_0	Q_0

*The QXZ output is the complement of QX.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The R2404LJ macro implements a 4-bit serial-input or parallel-input shift register with complementary outputs. The 4-bit length simplifies construction of large registers. The register contains an embedded clock driver that buffers the clock input so that standard library buffers can be used to drive multiple clock inputs. When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: R2404LJ SERIN,LZ_S,CLK,A,B,C,D,QA,QAZ,QB,QBZ,QC,QCZ,QD,QDZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	135	MHz
t_w	Pulse duration	CLK (H or L)	3.7		ns
t_{su}	Setup time before clock	SERIN (H or L)	2		ns
		LZ_S (H or L)	4		
		A..D (H or L)	2		
t_h	Hold time after clock	SERIN (H or L)	0		ns
		LZ_S (H or L)	0		
		A..D (H or L)	0		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLK		0.16		pF
		Dn		0.09		
		LZ_S		0.07		
		SERIN		0.12		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	8		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
t_{PLH}	CLK	Q	0.52	1.26	2.48	ns
t_{PHL}			0.58	1.58	3.22	
t_{PLH}	CLK	QZ	0.71	1.96	4.06	ns
t_{PHL}			0.63	1.85	3.9	
Δt_{PLH}	CLK	Q	0.35	0.89	1.72	ns/pF
Δt_{PHL}			0.26	0.51	0.94	
Δt_{PLH}	CLK	QZ	0.17	0.45	0.89	ns/pF
Δt_{PHL}			0.15	0.37	0.74	

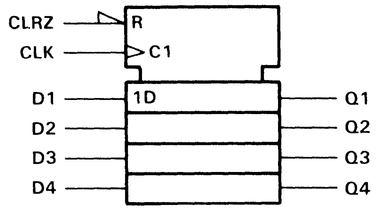
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

INTERNAL REGISTER HARDWIRED MACRO

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLRZ	CLK	Dn	Qn
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The R2405 is a dedicated, hardwired function implementing a 4-bit flip-flop register element. Its 4-bit length means that larger blocks of custom logic can be handled efficiently to construct large registers.

The 4-bit register contains an embedded clock driver that buffers the clock input. This further simplifies implementation of longer registers, as standard library buffer cells can be used to drive multiple clock inputs, which are used in the longer registers. When the 4-bit register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: R2405LJ CLRZ,D1,D2,D3,D4,CLK,Q1,Q2,Q3,Q4;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	135	MHz
t_w	Pulse duration	CLRZ low	2		ns
		CLK high or low	3.7		
t_{su}	Setup time before clock	D (high or low)	2		ns
		CLRZ inactive	0		
t_h	Hold time after clock	D (high or low)	0		ns
		CLRZ active	2		

D3015, OCTOBER 1987

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLK		0.16		pF
		CLRZ		0.72		
		D		0.08		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	7.02		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
t_{PLH}	CLK	Q	0.53	1.42	2.85	ns
t_{PHL}			0.58	1.63	3.33	
t_{PHL}	CLRZ	Q	0.33	0.71	1.34	ns
Δt_{PLH}	CLK	Q	0.36	0.89	1.72	ns/pF
Δt_{PHL}			0.26	0.51	0.95	
Δt_{PHL}	CLRZ	Q	0.25	0.52	0.95	ns/pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

R2406LJ 4-BIT REGISTER WITH COMPLEMENTARY OUTPUTS

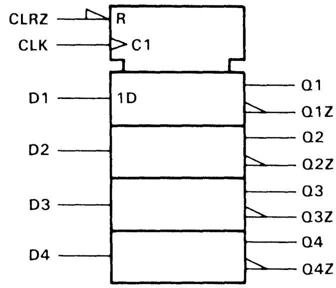
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

INTERNAL REGISTER HARDWIRED MACRO

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLRZ	CLK	Dn	Qn	QnZ
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The R2406 is a dedicated, hardwired function implementing a 4-bit flip-flop register element with complementary outputs. Its 4-bit length means that larger blocks of custom logic can be handled efficiently to construct large registers.

The register contains an embedded clock driver that buffers the clock input. This further simplifies implementation of longer registers, as standard library buffer cells can be used to drive multiple clock inputs, which are used in the longer registers. When the 4-bit register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: R2406LJ CLRZ,D1,D2,D3,D4,CLK,Q1,Q1Z,Q2,Q2Z,Q3,Q3Z,Q4,Q4Z;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	135	MHz
t_w	Pulse duration	CLRZ low	2		ns
		CLK high or low	3.7		
t_{su}	Setup time before clock	D (high or low)	2		ns
		CLRZ inactive	0		
t_h	Hold time after clock	D (high or low)	0		ns
		CLRZ active	2		

D3015, OCTOBER 1987

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLK		0.15		pF
		CLRZ		0.72		
		D		0.08		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	8.17		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
t_{PLH}	CLK	Q	0.52	1.36	2.73	ns
t_{PHL}			0.59	1.68	3.49	
t_{PLH}	CLK	QZ	0.64	1.85	3.86	ns
t_{PHL}			0.63	1.69	3.43	
t_{PLH}	CLRZ	QZ	0.41	0.95	1.88	ns
t_{PHL}		Q	0.29	0.62	1.18	
Δt_{PLH}	CLK	Q	0.37	0.9	1.73	ns/pF
Δt_{PHL}			0.25	0.52	0.96	
Δt_{PLH}	CLK	QZ	0.37	0.89	1.7	ns/pF
Δt_{PHL}			0.25	0.51	0.92	
Δt_{PLH}	CLRZ	QZ	0.37	0.88	1.7	ns/pF
Δt_{PHL}		Q	0.24	0.51	0.95	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

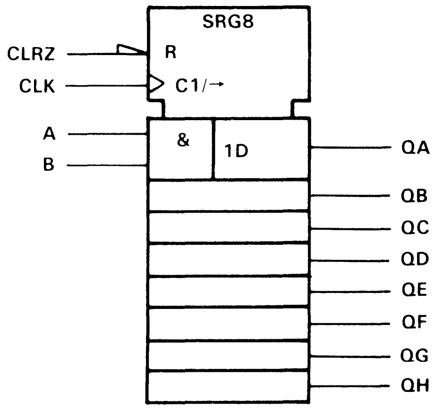
S164LJ 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

D3015, OCTOBER 1987

SOFTWARE MACRO

- AND-Gated (Enable/Disable) Serial Inputs
- Buffered Clear and Serial Inputs
- Direct Clear
- Embedded Clock Drivers Provide Clock Buffering

logic symbol†



Equivalent to 74164

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S164LJ gate-array software macro implements an 8-bit parallel-out shift register. The 8-bit shift register features AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data, since a low at either input inhibits entry of new data and resets the first flip-flop to a low level at the next clock pulse. A high level input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock input. The S164LJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
AN210LJ	2	1	2	0.44
BU150LJ	3	2	6	6
DTC20LJ	9	8	72	20.8
IV120LJ	1	8	8	3.12
TOTALS		19	88	30.36

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

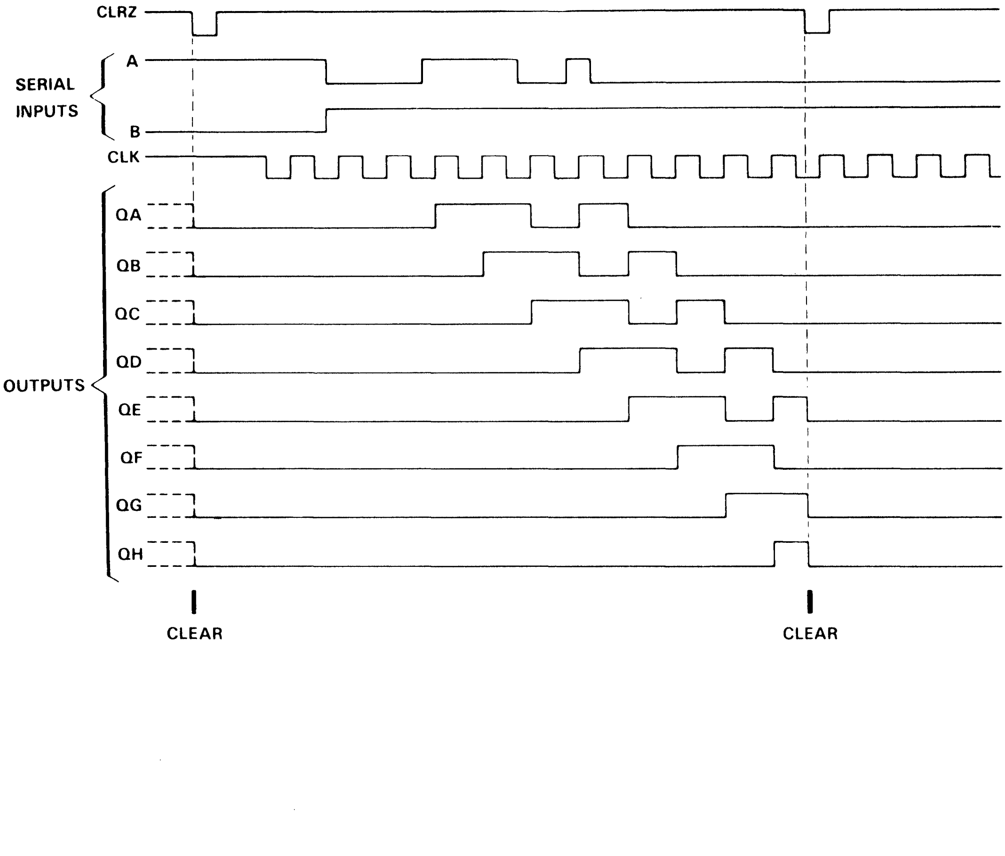
When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S164LJ A,B,CLK,CLRZ,QA,QB,QC,QD,QE,QF,QG,QH;

FUNCTION TABLE

INPUTS				OUTPUTS		
CLRZ	CLK	A	B	QA	QB...	QH
L	X	X	X	L	L	L
H	L	X	X	QA_0	QB_0	QH_0
H	↑	H	H	H	QA_n	QG_n
H	↑	L	X	L	QA_n	QG_n
H	↑	X	L	L	QA_n	QG_n

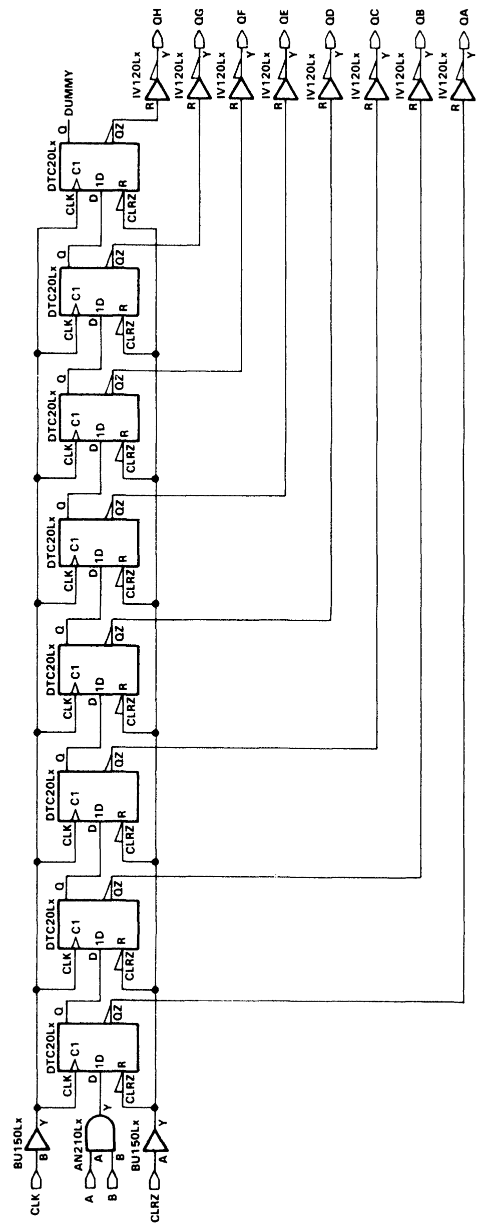
typical clear, shift, and clear sequences



S164LJ
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

D3015, OCTOBER 1987

logic diagram



D3015, OCTOBER 1987

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†		TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance		0.07		pF
C_{pd}	Equivalent power dissipation capacitance‡	$t_r = t_f = 1$ ns	30.36		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	CLK	Q		2.5	4.7	ns
t_{PHL}				2.5	4.7	
t_{PHL}	CLRZ	Q		2	3.7	ns
Δt_{PLH}	Any	Q	0.22	0.44	0.84	ns/pF
Δt_{PHL}			0.22	0.32	0.44	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

S165ALJ
PARALLEL-LOAD 8-BIT SHIFT REGISTER

D3015, OCTOBER 1987–REVISED OCTOBER 1988

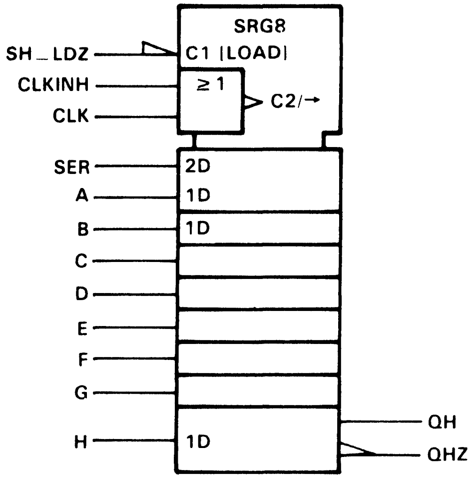
SOFTWARE MACRO

- **Gated (Enable/Inhibit) Clock Inputs**
- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Parallel-to-Serial Data Conversion**
- **Clock Driver Provides Clock Buffering**

description

The S165ALJ gate-array software macro implements an 8-bit parallel-in shift register. When clocked, the 8-bit serial-shift register shifts the data toward serial output QH. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH_LDZ input. The S165ALJ also features a clock-inhibit function and a complementary serial output QHZ. The S165ALJ is implemented with the macro functions indicated.

logic symbol†



Equivalent to 74165

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
DFB20LJ	12	8	96	16.48
IV110LJ	1	8	8	1.68
IV140LJ	2	1	2	0.8
NA210LJ	1	16	16	4.32
OR220LJ	2	1	2	0.8
TOTALS		34	124	24.08

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S165ALJ A,B,C,D,E,F,G,H,CLK,CLKINH,SH_LDZ,SER,QH,QHZ;

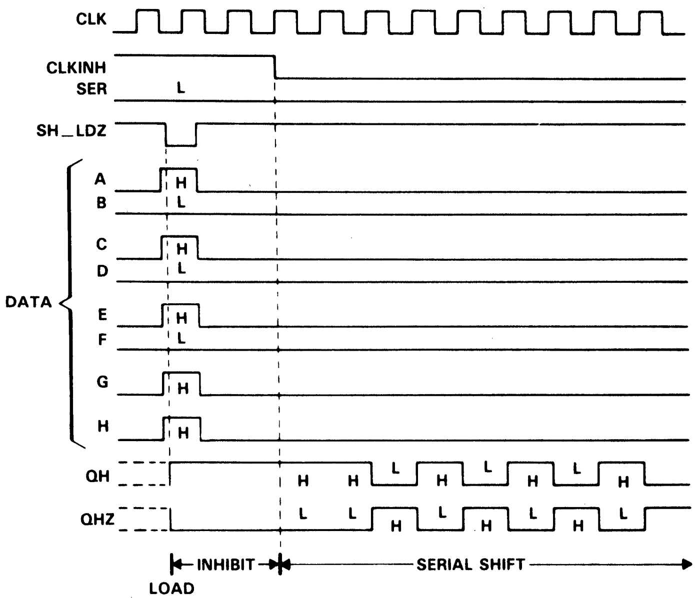
Clocking is accomplished by a low-to-high transition of the CLK input while SH_LDZ is held high and CLKINH is held low. The functions of the CLK and CLKINH (clock inhibit) inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLKINH will also accomplish clocking, CLKINH should be changed to the high level only while the CLK input is high. Parallel loading is inhibited when SH_LDZ is held high. The parallel inputs to the register are enabled while SH_LDZ is low independently of the levels of CLK, CLKINH, or SER inputs.

FUNCTION TABLE

INPUTS			FUNCTION
SH_LDZ	CLK	CLKINH	
L	X	X	Parallel load A thru H
H	H	X	No change
H	X	H	No change
H	L	↑	Shift
H	↑	L	Shift

Shift = Content of each internal register shifts toward serial output QH. Data at serial input is shifted into first register.

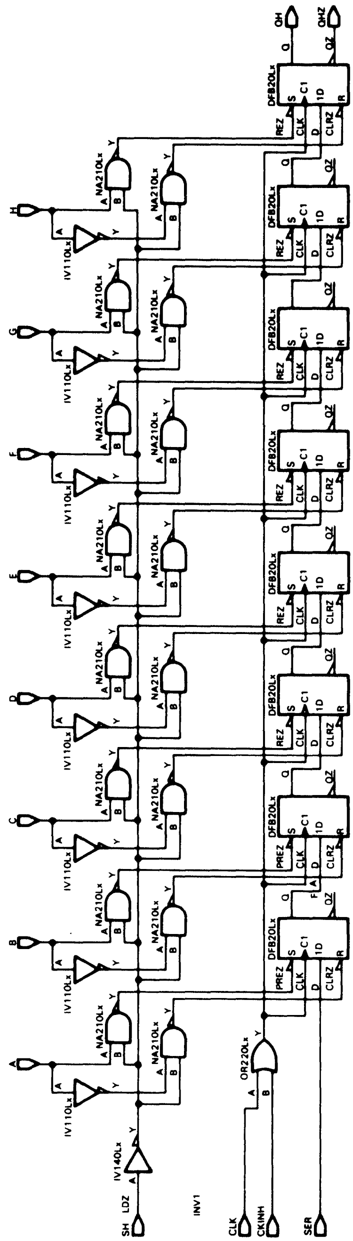
typical load, inhibit, and shift sequences



S165ALJ
PARALLEL-LOAD 8-BIT SHIFT REGISTER

D3015, OCTOBER 1987—REVISED OCTOBER 1988

logic diagram



D3015, OCTOBER 1987—REVISED OCTOBER 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	SH_LDZ		0.31		pF
		All others		0.14		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	24.08		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	SH_LDZ	QH		2.1	3.5	ns
t_{PHL}				2.1	3.5	
t_{PLH}		QHZ		2.8	5.2	ns
t_{PHL}				2.1	3.5	
t_{PLH}	CLK	QH		3	6.2	ns
t_{PHL}				2.4	4.9	
t_{PLH}		QHZ		3	6.4	ns
t_{PHL}				2.3	4.7	
t_{PLH}	H	QH		1.4	2.4	ns
t_{PHL}				1.5	2.7	
t_{PLH}	H	QHZ		1.5	2.7	ns
t_{PHL}				1.4	2.4	
Δt_{PLH}	Any	Q	0.18	0.46	0.92	ns/pF
Δt_{PHL}			0.16	0.34	0.65	

§Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

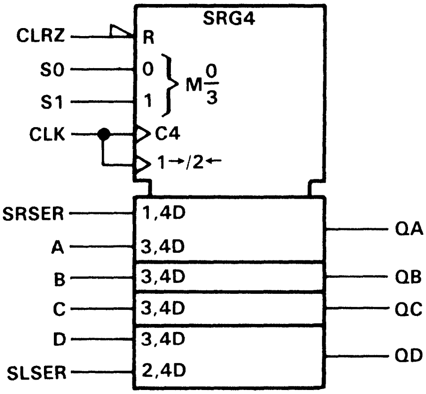
S194ALJ
BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

D3015, OCTOBER 1987

SOFTWARE MACRO

- Parallel Inputs and Outputs
- Four Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Left Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Embedded Clock Drivers Provide Clock Buffering
- Direct Overriding Clear

logic symbol†



Equivalent to 74194A

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S194ALJ gate-array software macro implements a 4-bit parallel-in/parallel-out bidirectional, universal shift register. The 4-bit length simplifies construction of large registers. These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit features parallel inputs, parallel outputs, right-shift and left-shift inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Inhibit clocking (do nothing)
Shift right (in the direction QA toward QD)
Shift left (in the direction QD toward QA)
Parallel (broadside load)

The S194ALJ is implemented with the macro functions indicated.

MACRO NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
IV110LJ	1	1	1	0.21
IV120LJ	1	4	4	1.56
IV140LJ	2	1	2	0.8
NA310LJ	2	16	32	4.48
NA410LJ	2	4	8	1.16
R2405LJ	26	1	26	7.02
TOTALS		27	73	15.23

‡The equivalent power dissipation capacitance does not include interconnect capacitance.

When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S194ALJ A,B,C,D, SRSER,SLSER,CLK,CLRZ,S1,S0,QA,QB,QC,QD;

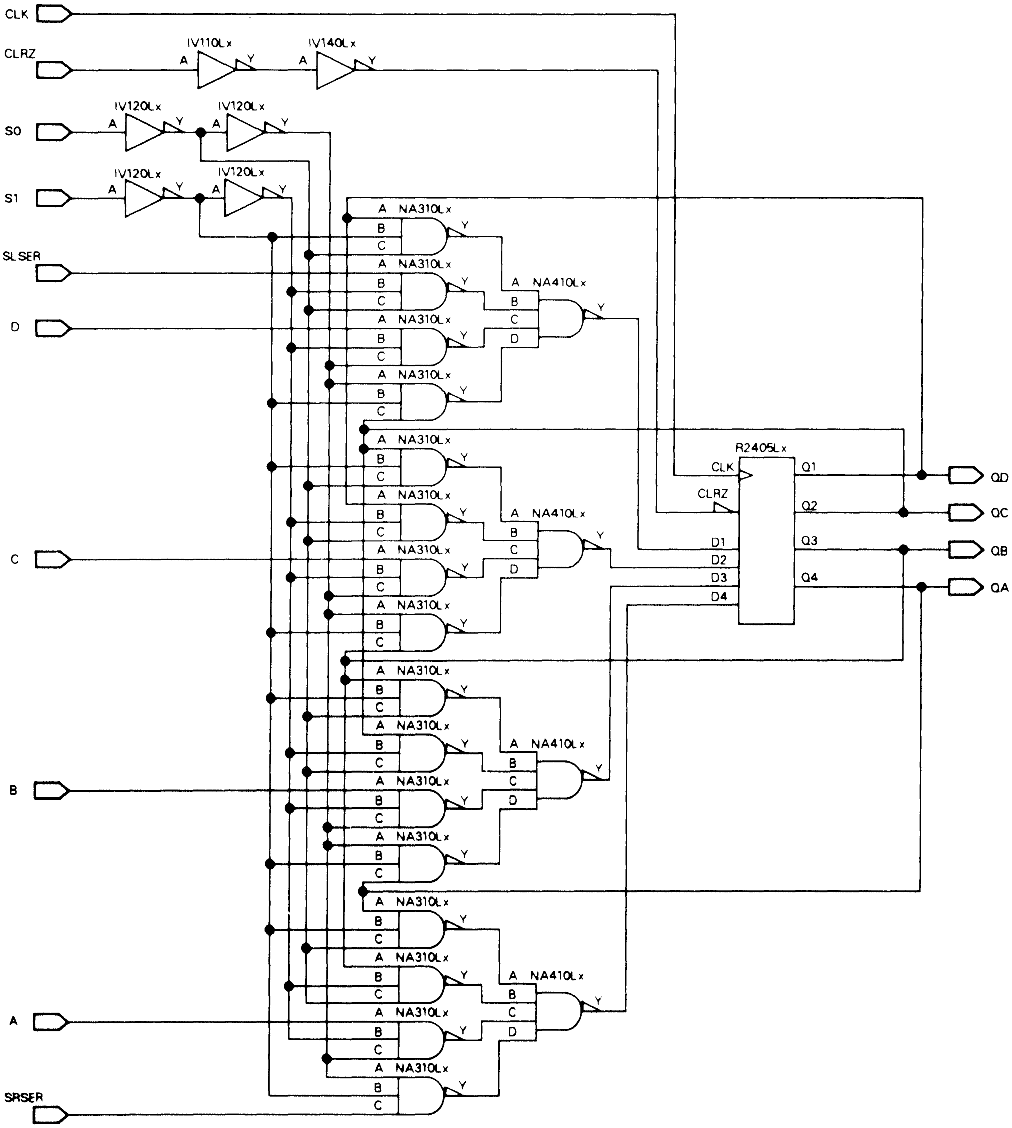
Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. When both mode control inputs are low, a free-running clock will reload the present state of each flip-flop on each clock transition to implement the do-nothing mode.

S194ALJ
BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

D3015, OCTOBER 1987

logic diagram



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TEXAS INSTRUMENTS

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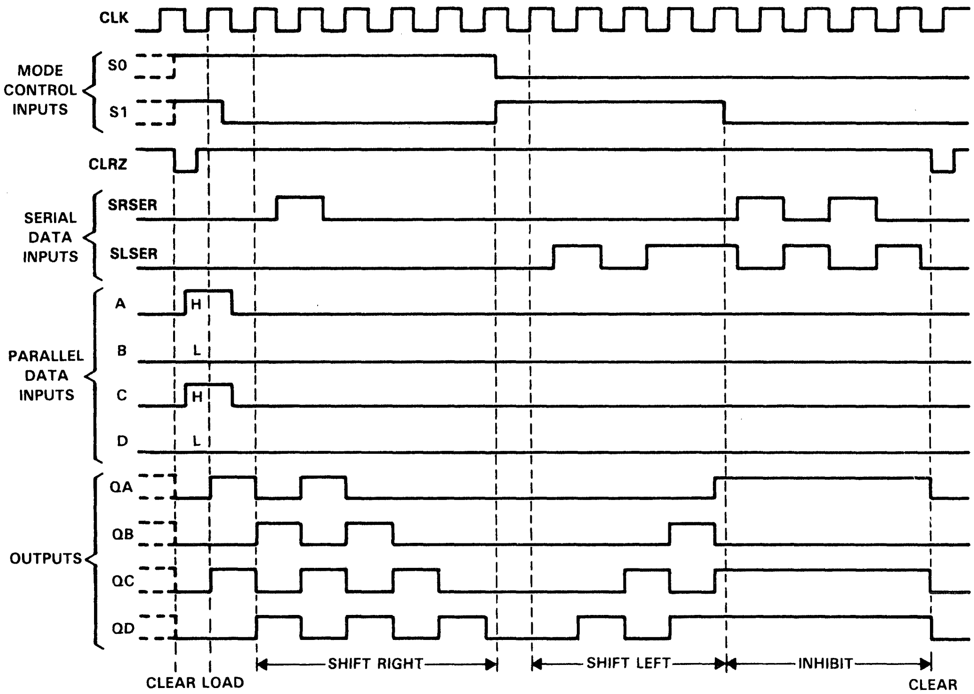
D3015, OCTOBER 1987—REVISED FEBRUARY 1989

FUNCTION TABLE

INPUTS											OUTPUTS			
CLRZ	MODE		CLK	SERIAL		PARALLEL					QA	QB	QC	QD
	S1	S0		SLSER	SRSER	A	B	C	D					
L	X	X	X	X	X	X	X	X	X		L	L	L	L
H	X	X	L	X	X	X	X	X	X		QA_0	QB_0	QC_0	QD_0
H	H	H	↑	X	X	a	b	c	d		a	b	c	d
H	L	H	↑	X	H	X	X	X	X		H	QA_n	QB_n	QC_n
H	L	H	↑	X	L	X	X	X	X		L	QA_n	QB_n	QC_n
H	H	L	↑	H	X	X	X	X	X		QB_n	QC_n	QD_n	H
H	H	L	↑	L	X	X	X	X	X		QB_n	QC_n	QD_n	L
H	L	L	X	X	X	X	X	X	X		QA_0	QB_0	QC_0	QD_0

typical clear, load, right-shift, left-shift, inhibit, and clear sequences



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†			TEST CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	S0,S1		0.15		pF
		CLK		0.16		
		All others		0.07		
C_{pd}	Equivalent power dissipation capacitance‡		$t_r = t_f = 1$ ns	15.23		pF

† For Supply Current, I_{CC}, see the TGC100 Series Data.
‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	CLK	Q		1.8	3.7	ns
t_{PHL}				1.9	3.8	
t_{PHL}	CLRZ	Q		2.1	3.7	ns
Δt_{PLH}	Any	Q	0.36	0.89	1.72	ns/pF
Δt_{PHL}			0.26	0.51	0.95	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4,000 gates. Post-layout simulation uses actual interconnect capacitance values.

GENERAL DATA
EDGE-TRIGGERED 3-PORT REGISTER FILES

D3015, OCTOBER 1988

- **Full Parallel Access with One Independent Write Port and Two Independent Read Ports**
- **Use Register Files in Parallel for Multiple Word Lengths**

3-PORT REGISTER FILE SUMMARY

CELL NAME	WORD DEPTH	BIT WIDTH	AVERAGE READ ACCESS TIME (ns)
RF400LJ	16	8	6.4
RF402LJ	16	9	6.4

description

Each 3-port register file is provided with an independently addressed data-input port and two independently addressed read ports. The read mode is asynchronous, so data entry and data retrieval can occur simultaneously.

The write enable input, WEZ, provides a simple implementation of the write cycle. When high, the write enable input inhibits new data entry; when low, the write function is enabled and a positive transition at the clock input will store data present at the data inputs in the addressed register word.

Two read enables are provided to implement the read cycle:

- G1Z controls output data lines Q1n – Q1n, which are addressed by address lines RA10 – RA1n.
- G2Z controls output data lines Q2n – Q2n, which are addressed by address lines RA20 – RA2n.

When high, a read enable places its associated output lines in a high impedance state; when low, a read is enabled from the register word that is addressed by the associated read address inputs.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

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PARAMETER MEASUREMENT INFORMATION

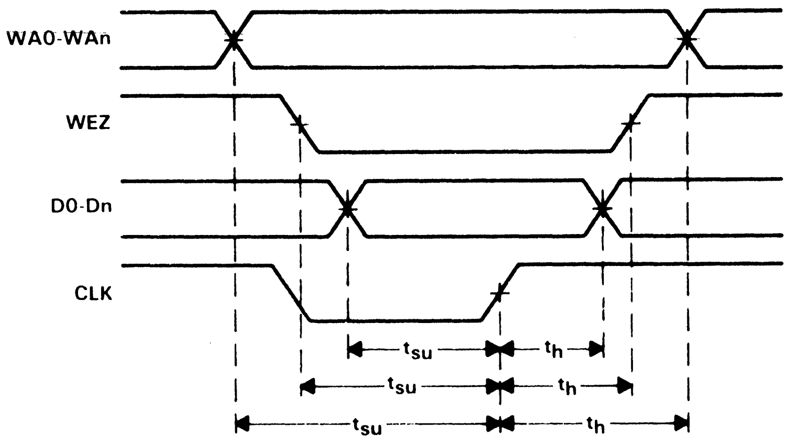
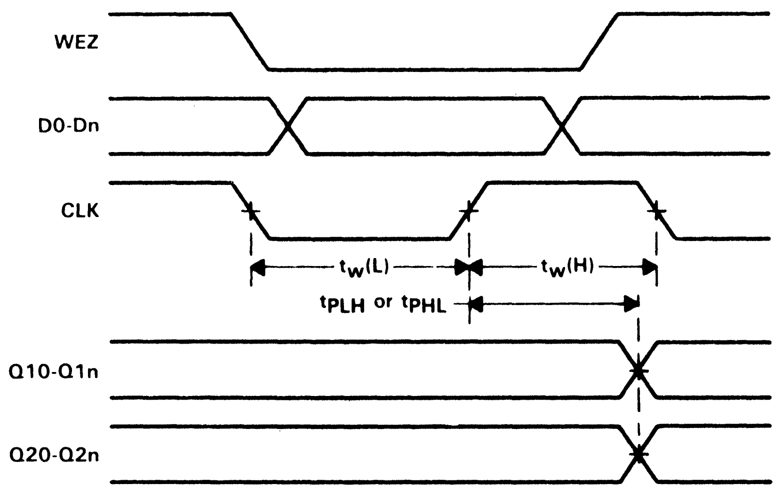


FIGURE 1. SETUP AND HOLD TIMES



NOTE A: Addresses for write and both reads are the same.

FIGURE 2. CLOCK PULSE DURATION, PROPAGATION DELAY TIMES FROM CLOCK

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PARAMETER MEASUREMENT INFORMATION (Continued)

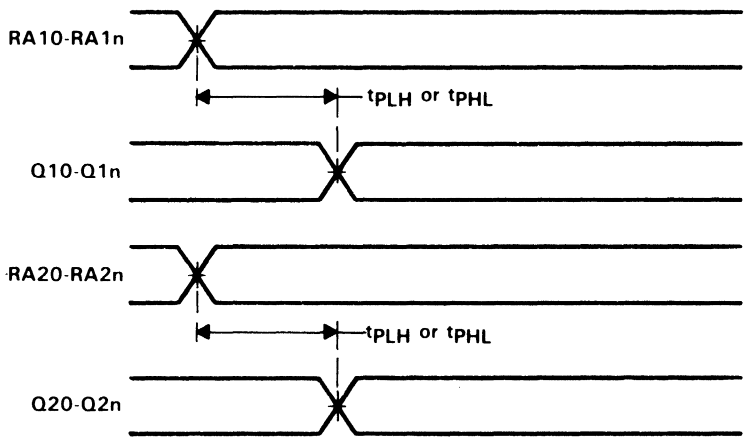

FIGURE 3. PROPAGATION DELAY TIMES FROM READ ADDRESS LOAD

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RF400LJ
16-WORD BY 8-BIT EDGE-TRIGGERED 3-PORT REGISTER FILE WITH 3-STATE OUTPUTS

D3015, OCTOBER 1988

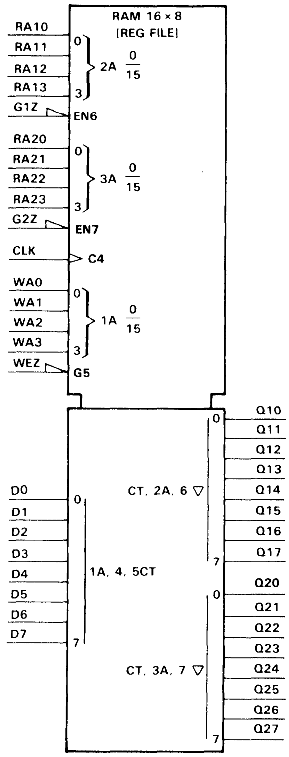
- **Full Parallel Access with One Independent Write Port and Two Independent Read Ports**
- **Use Register Files in Parallel for 16-Bit, 32-Bit, or 64-Bit Word Lengths**

description

The RF400LJ hardwired gate array MegaModule™ implements a 16-word by 8-bit, 3-port, high-speed register file. When the macro is called from the engineering workstation input, the following label format is developed and captured in the design netlist:

LABEL: RF400LJ CLK,WEZ,WA0,WA1, WA2,WA3,RA10,RA11,RA12,RA13, RA20,RA21,RA22,RA23,DO,D1,D2, D3,D4,D5,D6,D7,G1Z,G2Z,Q10, Q11,Q12,Q13,Q14,Q15,Q16,Q17, Q2O,Q21,Q22,Q23,Q24,Q25,Q26, Q27;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS				FUNCTION
CLK	WEZ	G1Z	G2Z	
↑	L	X	X	Store data from D0-D7 in location determined by WA0-WA3.
L	X	X	X	No change in stored data
X	H	X	X	No change in stored data
X	X	L	X	Output data through Q10-Q17 from location determined by RA10-RA13.
X	X	X	L	Output data through Q20-Q27 from location determined by RA20-RA23.
X	X	H	X	Outputs Q10-Q17 are in high-impedance state.
X	X	X	H	Outputs Q20-Q27 are in high-impedance state.

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D3015, OCTOBER 1988

SIGNAL DESCRIPTIONS

NAME	FUNCTION
CLK	Clock input. When WEZ is low, data present at the enabled data input port is stored in the addressed location during a low-to-high transition at the clock input. The clock is inactive while at the high or low level.
D0-D7	8-bit data input port
G1Z	Output enable for output port Q10-Q17; active when low
G2Z	Output enable for output port Q20-Q27; active when low
Q10-Q17 Q20-Q27	Two 8-bit data output ports
RA10-RA13	Read address for output port Q10-Q17
RA20-RA23	Read address for output port Q20-Q27
WA0-WA3	Write address
WEZ	Write enable, active when low

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
t_W	Clock pulse duration	High	3		ns
		Low	5		
t_{su}	Setup time before CLK↑	Write address	5		ns
		Data	1		
		Write enable	5		
t_h	Hold time after CLK↑	Write address	2		ns
		Data	2		
		Write enable	0		

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RF402LJ
16-WORD BY 9-BIT EDGE-TRIGGERED 3-PORT REGISTER FILE WITH 3-STATE OUTPUTS

D3015, OCTOBER 1988

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP†	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.16		pF
		Dn		0.19		
		GnZ		0.17		
		RBn		0.16		
		WAn		0.16		
		WEZ		0.19		
C_o	Output capacitance			0.19		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	48		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	RAn	Any	$R_L = \infty$	1.83	5.05	10.69	ns
t_{PHL}				2.12	5.39	10.89	
t_{PLH}	CLK	Any	$R_L = \infty$	2.04	5.59	11.77	ns
t_{PHL}				2.09	5.52	11.27	
t_{PZH}	GnZ	Qn	R_L = 40 kΩ to GND	0.59	1.57	3.23	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.44	1.07	2.12	
t_{PHZ}	GnZ	Qn	R_L = 40 kΩ to GND		7.03		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		3.04		
Δt_{PLH}	RAn	Any		0.11	0.31	0.64	ns/pF
Δt_{PHL}				0.14	0.31	0.56	
Δt_{PLH}	CLK	Any		0.12	0.31	0.62	ns/pF
Δt_{PHL}				0.14	0.29	0.56	
Δt_{PZH}	GnZ	Qn		0.16	0.36	0.66	ns/pF
Δt_{PZL}				0.23	0.53	1.02	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

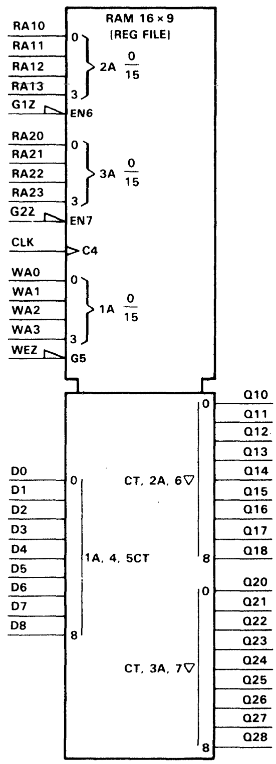
See general data on 3-port register files.

RF402LJ
16-WORD BY 9-BIT EDGE-TRIGGERED 3-PORT REGISTER FILE WITH 3-STATE OUTPUTS

D3015, OCTOBER 1988

- **Full Parallel Access with One Independent Write Port and Two Independent Read Ports**
- **Use Register Files in Parallel for 18-Bit, 36-Bit, or 72-Bit Word Lengths**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The RF402LJ hardwired gate-array MegaModule™ implements a 16-word by 9-bit, 3-port, high-speed register file. The 9-bit organization simplifies implementing data paths requiring parity or additional control bits. When the macro is called from the engineering workstation input, the following label format is developed and captured in the design netlist:

LABEL: RF402LJ CLK,WEZ,WA0,WA1, WA2,WA3,RA10,RA11,RA12,RA13, RA20,RA21,RA22,RA23,DO,D1,D2, D3,D4,D5,D6,D7,D8,G1Z,G2Z,Q10, Q11,Q12,Q13,Q14,Q15,Q16,Q17, Q18,Q2O,Q21,Q22,Q23,Q24,Q25, Q26,Q27,Q28;

FUNCTION TABLE

INPUTS				FUNCTION
CLK	WEZ	G1Z	G2Z	
↑	L	X	X	Store data from D0-D8 in location determined by WA0-WA3.
L	X	X	X	No change in stored data
X	H	X	X	No change in stored data
X	X	L	X	Output data through Q10-Q18 from location determined by RA10-RA13
X	X	X	L	Output data through Q20-Q28 from location determined by RA20-RA23.
X	X	H	X	Outputs Q10-Q18 are in high-impedance state.
X	X	X	H	Outputs Q20-Q28 are in high-impedance state.

MegaModule is a trademark of Texas Instruments Incorporated.

RF402LJ
16-WORD BY 9-BIT EDGE-TRIGGERED 3-PORT REGISTER FILE WITH 3-STATE OUTPUTS

D3015, OCTOBER 1988

SIGNAL DESCRIPTIONS

NAME	FUNCTION
CLK	Clock input. When WEZ is low, data present at the enabled data input port is stored in the addressed location during a low-to-high transition at the clock input. The clock is inactive while at the high or low level.
D0-D8	9-bit data input port
G1Z	Output enable for output port Q10-Q18; active when low
G2Z	Output enable for output port Q20-Q28; active when low
Q10-Q18 Q20-Q28	Two 9-bit data output ports
RA10-RA13	Read address for output port Q10-Q18
RA20-RA23	Read address for output port Q20-Q28
WA0-WA3	Write address
WEZ	Write enable, active when low

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TGC100 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
t_w	Clock pulse duration	High	3		ns
		Low	5		
t_{su}	Setup time before CLK↑	Write address	5		ns
		Data	1		
		Write enable	5		
t_h	Hold time after CLK↑	Write address	0		ns
		Data	2		
		Write enable	0		

MegaModule is a trademark of Texas Instruments Incorporated.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TYP†	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.16		pF
		Dn		0.19		pF
		GnZ		0.17		pF
		RAn		0.16		pF
		WAn		0.16		pF
		WEZ		0.19		pF
C_o	Output capacitance			0.19		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	54		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	RAn	Any	$R_L = \infty$	1.85	5.14	10.88	ns
t_{PHL}				2.16	5.47	11.03	
t_{PLH}	CLK	Any	$R_L = \infty$	2.05	5.63	11.83	ns
t_{PHL}				2.11	5.55	11.33	
t_{PZH}	GnZ	Qn	R_L = 40 kΩ to GND	0.66	1.71	3.4	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.47	1.13	2.17	
t_{PHZ}	GnZ	Qn	R_L = 40 kΩ to GND		7.14		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		3.04		
Δt_{PLH}	CLK	Any		0.12	0.31	0.62	ns/pF
Δt_{PHL}				0.13	0.3	0.56	
Δt_{PLH}	RAn	Any		0.12	0.29	0.62	ns/pF
Δt_{PHL}				0.12	0.29	0.58	
Δt_{PZH}	GnZ	Qn		0.17	0.36	0.68	ns/pF
Δt_{PZL}				0.25	0.56	1.07	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

See general data on 3-port register files.

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