TEXAS INSTRUMENTS

TSC500 Series

1-μm CMOS Standard Cells

Data Manual

Data Manual

TSC500 Series

1-μm CMOS Standard Cells

1989

1989 Application Specific Integrated Circuits

TSC500 Series
1-μm CMOS Standard Cells
Data Manual

Application Specific Integrated Circuits

TEXAS
INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to or to discontinue any semiconductor product or service identified in this publication without notice. TI advises its customers to obtain the latest version of the relevant information to verify, before placing orders, that the information being relied upon is current.

TI warrants performance of its semiconductor products to current specifications in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Unless mandated by government requirements, specific testing of all parameters of each device is not necessarily performed.

TI assumes no liability for TI applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Printed in the U.S.A.

Contents

1 Introduction

INTRODUCTION

Texas Instruments presents the *TSC500 Series 1-μm CMOS Standard Cell Data Manual*, a comprehensive reference document providing detailed specifications for each cell and macro included in TI's TSC500 Series software logic library, release 1.2.

how to use this manual

Sufficient detail is provided for a system designer to evaluate the availability, performance, and suitability of standard cells and macros to employ in the design of custom ASICs. For the evaluation process, the cell or macro data sheet contains the following detailed information:

- Cell or macro identification including a description supported with logic symbol and truth table or typical functional sequences
- Electrical and switching time parametric specifications
- Detailed logic diagram showing the standard cells used in the creation of the software macros
- Notes cross-referencing the standard cells and macro to similar CMOS and TTL functions

Other sections of the manual contain data to match the design evaluation with the packages offered in the TSC500 Series. For example:

- The TSC500 Series data, Section 2, includes data pertinent to the TSC500 Series technology, performance range, and application-related characteristics. Package availability is summarized.
- The library cell summary, Section 5, includes a listing of individual cells and macros in each of the functional categories offered.

Beyond use as a design evaluation tool, this manual can be used as a supplement to the TI library software and the TI *CMOS Standard Cell Design Manual*.

As a supplement to the software library, the individual data sheets in this manual show the extent of worst case ranges for the specifications, whereas the functional and simulation models contained in the TI library software include fully expanded, node-by-node specifications. With respect to the completed design, the TI-supplied library software will be used to determine the final design specifications.

As a supplement to the *CMOS Standard Cell Design Manual*, techniques presented in this manual include explanations of CMOS technology and TSC500 Series characteristics that can simplify the evaluation, selection, and application of cells and macros required for the execution of a custom standard cell design.

organization of this manual

SECTION 1 — Introduction. Presents a brief description of the contents of each data manual section. Also provides an alphanumeric listing of the TSC500 Series cells and macros, including a cross-reference for similar CMOS and TTL functions.

SECTION 2 — TSC500 Series Data. Provides a brief technology discussion, packaging options, and series-related specifications.

SECTION 3 — Mechanical Data. Provides drawings with dimensions and descriptive material for the packages offered in the TSC500 series.

SECTION 4 — Definitions and Ratings. Details the methodologies used in the characterization of functional and parametric ratings. Also defines abbreviations and terms.

SECTION 5 — Library Summary. Contains a complete listing of the cells and macros available in the software library and summarizes key specifications portraying the performance of the functions offered. Also provides equivalent sizes for each of the cells and macros.

SECTIONS 6 through 22 — Data Sheets. Contain the description, electrical, and switching characteristics for each individual function available in the library. The data sheets are grouped under the following tabs:

SPECIAL FUNCTIONS
BUFFERS/DRIVERS (Internal)
GATES
FLIP-FLOPS/LATCHES
OSCILLATORS
INPUT BUFFERS
BIDIRECTIONAL (I/O) BUFFERS
OUTPUT BUFFERS
ARITHMETIC FUNCTIONS
COUNTERS
DEMULTIPLEXERS
MULTIPLEXERS
REGISTERS
TESTABILITY FUNCTIONS
RANDOM ACCESS MEMORIES
FIFO MEMORIES
REGISTER FILES

Each tabbed section is preceded by a functional selection guide or general information related to that group of data sheets.

ALPHANUMERIC CROSS-REFERENCE INDEX

DECEMBER 1988

ALPHANUMERIC CROSS-REFERENCE INDEX

DECEMBER 1988

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

ALPHANUMERIC CROSS-REFERENCE INDEX

DECEMBER 1988

ALPHANUMERIC CROSS-REFERENCE INDEX

DECEMBER 1988

CMOS/TTL-TO-STANDARD CELL CROSS-REFERENCE INDEX

TSC500 SERIES

DECEMBER 1988

This cross-reference index lists TTL/CMOS device types and shows the equivalent and/or similar TSC500 Series cell type for each. The functions shown are intended for internal cells utilized as the core logic of a 5-V CMOS ASIC custom design. As such, the bus-driver functions referenced are for driving on-chip buses. A subset cell may require multiple cells of that type or other cell types to achieve a replacement function. A superset cell contains either multiples of or additional circuitry when compared to the referenced TTL/CMOS type.

TTL/CMOS TYPE	SEE NOTE	CELL TYPE	TTL/CMOS TYPE	SEE NOTE	CELL TYPE
7C122		RH004LJ	4011	(1)	NA210LJ
7C149		RH008LJ	4011	(1)	NA220LJ
7C150		RH008LJ	4011	(1)	NA230LJ
8X350		RH005LJ	4011	(1)	NA240LJ
65HC68		RH003LJ	4011	(1)	NA260LJ
68B10		RH003LJ	4012	(1)	NA410LJ
68HC68		RH005LJ	4012	(1)	NA420LJ
1223		RH008LJ	4012	(1)	NA430LJ
1433		RH011LJ	4013	(1)	DFB20LJ
1822		RH004LJ	4013	(1)	DTB10LJ
1823		RH003LJ	4015		S164LJ
1826		RH001LJ	4015	(2)	R2401LJ
2016		RH011LJ	4020	(1)	R2408LJ
2017		RH011LJ	4023	(1)	NA310LJ
2018		RH011LJ	4023	(1)	NA320LJ
2114		RH009LJ	4023	(1)	NA330LJ
2125	(4)	RH008LJ	4023	(1)	NA340LJ
2149		RH008LJ	4024	(1)	R2408LJ
4000	(1)	NO310LJ	4027	(2)	JKB20LJ
4000	(1)	NO320LJ	4030	(1)	EX210LJ
4000	(1)	NO330LJ	4030	(1)	EX220LJ
4001	(1)	NO210LJ	4030	(1)	EX240LJ
4001	(1)	NO220LJ	4040	(1)	R2408LJ
4001	(1)	NO230LJ	4042	(2)	LAH23LJ
4001	(1)	NO240LJ	4044	(1)	LAB10LJ
4002	(1)	NO410LJ	4044	(1)	LAB20LJ
4002	(1)	NO420LJ	4063		S085LJ

NOTES: 1. Cell is a subset of the referenced function.
2. Cell is similar to a subset of the referenced function.
3. Cell is a subset of the referenced function but may contain additional inputs.
4. Cell is a superset to the referenced function.

CMOS/TTL-TO-STANDARD CELL CROSS-REFERENCE INDEX

DECEMBER 1988

TTL/CMOS TYPE	SEE NOTE	CELL TYPE
4068	(1)	NA810LJ
4068	(1)	NA820LJ
4069	(1)	IV101LJ
4069	(1)	IV110LJ
4069	(1)	IV120LJ
4069	(1)	IV130LJ
4069	(1)	IV140LJ
4069	(1)	IV160LJ
4069	(1)	IV180LJ
4070	(1)	EX210LJ
4070	(1)	EX220LJ
4070	(1)	EX240LJ
4071	(1)	OR210LJ
4071	(1)	OR220LJ
4071	(1)	OR240LJ
4071	(1)	OR260LJ
4072	(1)	OR410LJ
4072	(1)	OR420LJ
4072	(1)	OR440LJ
4072	(1)	OR460LJ
4073	(1)	AN310LJ
4073	(1)	AN320LJ
4073	(1)	AN340LJ
4073	(1)	AN360LJ
4075	(1)	OR310LJ
4075	(1)	OR320LJ
4075	(1)	OR340LJ
4075	(1)	OR360LJ
4076		S173LJ
4077	(1)	EN210LJ
4078		NO810LJ
4078		NO820LJ
4081	(1)	AN210LJ
4081	(1)	AN220LJ
4081	(1)	AN240LJ
4081	(1)	AN260LJ
4082	(1)	AN410LJ
4082	(1)	AN420LJ
4082	(1)	AN440LJ
4082	(1)	AN460LJ
4085	(1)	AO221LJ
4095	(1)	JKB20LJ
4099	(1)	S259LJ
4334		RH008LJ
4512		MU310LJ
4512		MU320LJ
4514		S137LJ
4515		S137LJ
4520		S161ALJ
4520	(2)	S163ALJ
4539	(1)	MU210LJ
4585		SO85LJ
4703	(4)	FI503LJ
4801		RH009LJ
5101		RH004LJ
5102		RH006LJ
5114		RH008LJ
5115		RH011LJ
5116		RH011LJ
5117		RH011LJ
5118		RH011LJ
5514		RH008LJ
6116		RH011LJ
6514		RH008LJ
6516		RH011LJ
6551		RH004LJ
6561		RH004LJ
7266	(1)	EN210LJ

NOTES: 1. Cell is a subset of the referenced function.
2. Cell is similar to a subset of the referenced function.
3. Cell is a subset of the referenced function but may contain additional inputs.
4. Cell is a superset to the referenced function.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

CMOS/TTL-TO-STANDARD CELL CROSS-REFERENCE INDEX

DECEMBER 1988

TTL/CMOS TYPE	SEE NOTE	CELL TYPE	TTL/CMOS TYPE	SEE NOTE	CELL TYPE
9122		RH004LJ	54/7404	(1)	IV180LJ
9150		RH008LJ	54/7404	(1)	AN210LJ
14505	(4)	RH000LJ	54/7408	(1)	AN220LJ
40101		S280LJ	54/7408	(1)	AN240LJ
40104	(2)	S194ALJ	54/7408	(1)	AN260LJ
40105	(4)	FI503LJ	54/7410	(1)	NA310LJ
40181		S181LJ	54/7410	(1)	NA320LJ
40193		S193LJ	54/7410	(1)	NA330LJ
65162		RH011LJ	54/7410	(1)	NA340LJ
67401	(4)	FI603LJ	54/7411	(1)	AN310LJ
67402	(4)	FI603LJ	54/7411	(1)	AN320LJ
67413	(4)	FI603LJ	54/7411	(1)	AN340LJ
72401	(4)	FI603LJ	54/7411	(1)	AN360LJ
72402	(4)	FI603LJ	54/7414	(2)	IPI09LJ
72403	(4)	FI603LJ	54/7420	(1)	NA410LJ
72404	(4)	FI603LJ	54/7420	(1)	NA420LJ
72413	(4)	FI603LJ	54/7421	(1)	AN410LJ
93422		RH004LJ	54/7421	(1)	AN420LJ
93425	(4)	RH008LJ	54/7421	(1)	AN440LJ
54/7400	(1)	NA210LJ	54/7421	(1)	AN460LJ
54/7400	(1)	NA220LJ	54/7427	(1)	NO310LJ
54/7400	(1)	NA230LJ	54/7427	(1)	NO320LJ
54/7400	(1)	NA240LJ	54/7427	(1)	NO330LJ
54/7400	(1)	NA260LJ	54/7430		AN810LJ
54/7402	(1)	NO210LJ	54/7430	(1)	NA810LJ
54/7402	(1)	NO220LJ	54/7430	(1)	NA820LJ
54/7402	(1)	NO230LJ	54/7432	(1)	OR210LJ
54/7400	(1)	NO240LJ	54/7432	(1)	OR220LJ
54/7404	(1)	IV101LJ	54/7432	(1)	OR240LJ
54/7404	(1)	IV110LJ	54/7432	(1)	OR260LJ
54/7404	(1)	IV120LJ	54/7440	(1)	NA430LJ
54/7404	(1)	IV130LJ	54/7450	(2)	AO220LJ
54/7404	(1)	IV140LJ	54/74S51	(1)	AO221LJ
54/7404	(1)	IV160LJ	54/7451	(3)	AO421LJ

NOTES: 1. Cell is a subset of the referenced function.
2. Cell is similar to a subset of the referenced function.
3. Cell is a subset of the referenced function but may contain additional inputs.
4. Cell is a superset to the referenced function.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

CMOS/TTL-TO-STANDARD CELL CROSS-REFERENCE INDEX

DECEMBER 1988

TTL/CMOS TYPE	SEE NOTE	CELL TYPE
54/7451	(3)	BF005LJ
54/7458	(3)	AO320LJ
54/7474	(1)	DFB20LJ
54/7474	(1)	DTB10LJ
54/7475	(1)	LAH10LJ
54/7475	(1)	LAH20LJ
54/7475	(1)	LAH40LJ
54/7485		SO85LJ
54/7486	(1)	EX210LJ
54/7486	(1)	EX220LJ
54/7486	(1)	EX240LJ
54/7494	(1)	R2403LJ
54/7494	(1)	R2404LJ
54/74109	(1)	JKB20LJ
54/74137		S137LJ
54/74138		S138LJ
54/74139		S139LJ
54/74139	(1)	DE212LJ
54/74151		S151LJ
54/74153		S153LJ
54/74155		S155LJ
54/74155	(1)	DE212LJ
54/74157		S157LJ
54/74157	(1)	MU110LJ
54/74157	(1)	MU111LJ
54/74158		S158LJ
54/74161A		S161ALJ
54/74163A	(2)	S163ALJ
54/74164		S164LJ
54/74165A		S165ALJ
54/74166		S166LJ
54/74173		S173LJ
54/74174		S174LJ
54/74174	(1)	R2405LJ
54/74175		R2406LJ
54/74175		S175LJ
54/74177		S177LJ
54/74181		S181LJ
54/74191		S191LJ
54/74193		S193LJ
54/74194A		S194ALJ
54/74195A		S195ALJ
54/74222	(4)	FI503LJ
54/74224	(4)	FI503LJ
54/74225	(4)	FI503LJ
54/74244		S244LJ
54/74245		S245LJ
54/74251		S251LJ
54/74257A		S257ALJ
54/74258A		S258ALJ
54/74259		S259LJ
54/74266	(1)	EN210LJ
54/74273		S273LJ
54/74280		S280LJ
54/74283		S283LJ
54/74298		S298LJ
54/74299		S299LJ
54/74299	(1)	S299XLJ
54/74373		S373LJ
54/74374		S374LJ
54/74375		S375LJ
54/74393		S393LJ
54/74398		S398LJ
54/74399		S399LJ
54/74425	(1)	BU221LJ
54/74425	(1)	BU261LJ
54/74426	(1)	BU222LJ
54/74426	(1)	BU262LJ

NOTES: 1. Cell is a subset of the referenced function.
2. Cell is similar to a subset of the referenced function.
3. Cell is a subset of the referenced function but may contain additional inputs.
4. Cell is a superset to the referenced function.

CMOS/TTL-TO-STANDARD CELL CROSS-REFERENCE INDEX

DECEMBER 1988

TTL/CMOS TYPE	SEE NOTE	CELL TYPE
54/74468	(1)	IV211LJ
54/74468	(1)	IV221LJ
54/74468	(1)	IV241LJ
54/74590		S590LJ
54/74593	(1)	S593XLJ
54/74595		S595LJ
54/74598	(1)	S598XLJ
54/74651		S651LJ
54/74652		S652LJ
54/74669		S669LJ
54/74670	(4)	RF400LJ
54/74670	(4)	RF401LJ
54/74670	(4)	RF402LJ
54/74670	(4)	RF403LJ
54/74686		S686LJ
54/74688		S688LJ
54/747030	(4)	FI603LJ

NOTES: 1. Cell is a subset of the referenced function.
2. Cell is similar to a subset of the referenced function.
3. Cell is a subset of the referenced function but may contain additional inputs.
4. Cell is a superset to the referenced function.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

2

TSC500 Series Data

TSC500 SERIES
1-μm CMOS STANDARD CELLS

D3030, APRIL 1989

- **High-Performance, 1-μm EPIC™ CMOS Process Efficiently Achieves System-Level Designs**
- **TSC500 Library Includes Macros for:**
  - **Static RAMs and Register Files**
  - **First-In First-Out Memories**
  - **Oscillators**
- **TSC500 Library Supports Designs Using:**
  - **Application Toolkit Products**
  - **MegaModule™ Design Kits**
- **TSC500 1-μm EPIC™ CMOS Process Features:**
  - **Double-Level Metal, Silicided-Poly**
  - **Typical Gate Delay 490 ps (FO = 3)**
  - **Flip-Flop Toggle Rates Up to 185 MHz**
  - **ESD and Latch-Up Protected I/Os**
  - **Outputs with Up to 64-mA Sink Current**
  - **di/dt-Controlled or Full-Speed Buffers**
- **Extensive Design Support Including:**
  - **Design Libraries Compatible with Daisy and Mentor CAE Systems**
  - **TI Regional ASIC Design Centers**
  - **Design Kits Available for Daisy and Mentor Engineering Workstations**

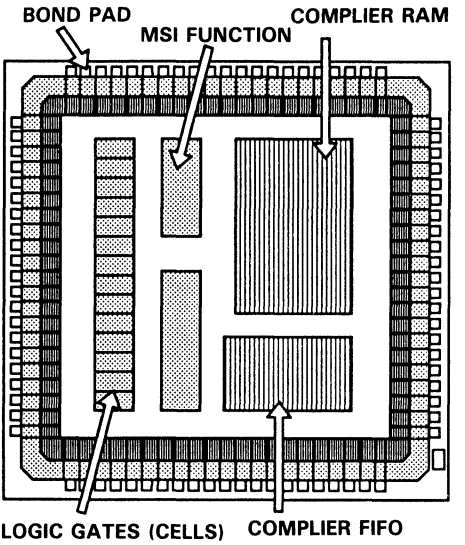


FIGURE 2-1. TYPICAL TSC500 SERIES CUSTOM DESIGN

technology description

The Texas Instruments TSC500 Series CMOS Standard Cell library comprises productivity-enhanced engineering workstation support software for the design of custom ICs to be fabricated with TI's 1-μm EPIC™ CMOS process and assembled in high-density, industry-standard packages. The advanced silicon-gate process features two levels of copper-doped-aluminum metallization to achieve increased performance and densities that support system-level integration. Silicided gate, source, and drain elements reduce resistance and enhance performance.

EPIC and MegaModule are trademarks of Texas Instruments Incorporated.

TSC500 SERIES
1-μm CMOS STANDARD CELLS

D3030, APRIL 1989

library description

The TSC500 Series Standard Cell library includes gate, buffer, MSI-level, and memory functions. Within the 452 cells, macros, and memories offered, 402 are hardwired macros and 50 are software macros. The hardwired macros provide a broad selection of fully characterized cells. The software macros provide popular TTL/CMOS-type MSI functions that can be used as designed or modified at your workstation to suit your design requirements. Additional user-defined software macros can be created using the TSC500 libraries to further enhance EWS productivity. Library release 1.2 contains the following classes of cells and macros:

- 22 Hardwired MegaModule™ Memory Cells and 50 MSI Software Macros
- 66 Register, Scan FFs/Latches, Delay Elements, and Oscillator Cells
- 148 Gate, Bus Buffers, and Macro Building Blocks
- 166 External Input, Output, and Bidirectional Buffer Cells

A complete TSC500 Series Design Kit, for applicable workstations, includes the following:

- *TSC500 Series 1-μm CMOS Standard Cell Data Manual*
- *CMOS Standard Cell Design Manual*
- *Design Support Software User's Manual*
- *TSC500 Series Design Library*

The design kit is arranged to accommodate revised material as it is issued.

design flow

Custom functions, which are designed using an engineering workstation in conjunction with TI's TSC500 Series Standard Cell library, can be simulated and verified prior to creating the design database files. The database files generated are used to create tooling for the fabrication and test programs for acceptance of the user-defined custom IC. A detailed design flow diagram is presented in Figure 2-2.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

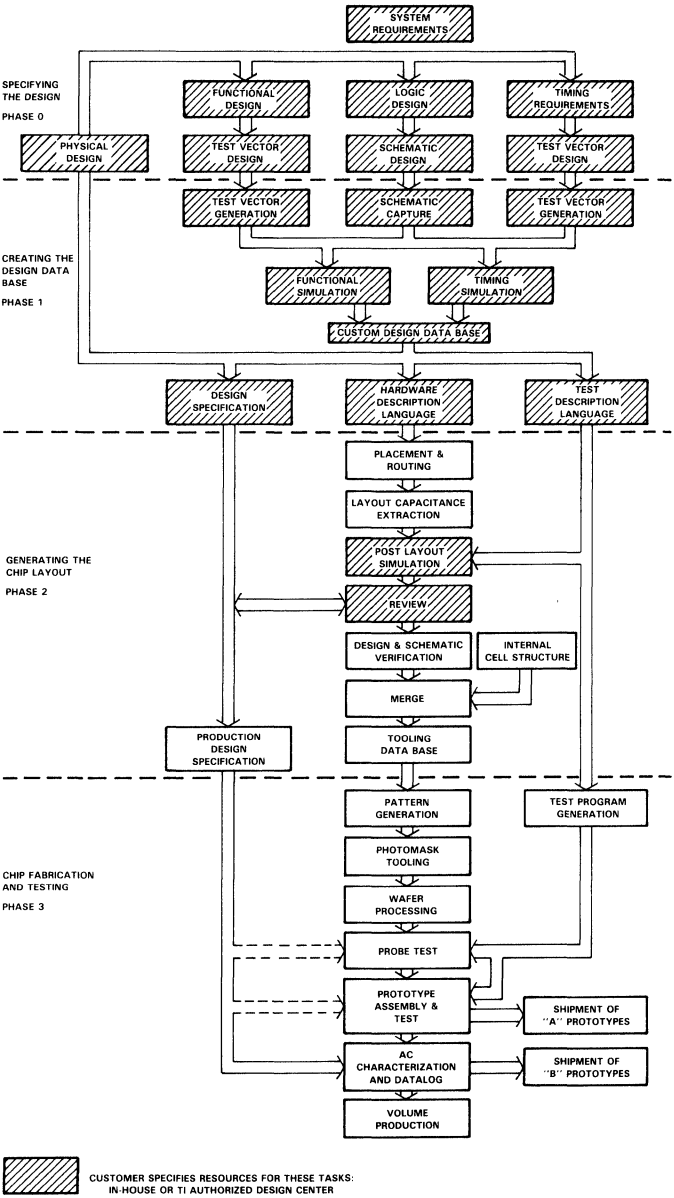


FIGURE 2-2. TSC500 SERIES DESIGN FLOW

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I . . . . . −0.5 V to 7 V
Output voltage, V_O . . . . . −0.5 V to 7 V
Input clamp current‡, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current§, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current§, (V_O = 0 to V_{CC}) . . . . . ±25 mA
Operating free-air temperature: Military temperature range . . . . . −55°C to 150°C
Commercial temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other condition(s) beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

‡ Applies to external input and bidirectional buffers.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage¶	CMOS-compatible inputs	$0.7V_{CC}$			V
		TTL-compatible inputs	2			
V_{IL}	Low-level input voltage¶	CMOS-compatible inputs			$0.2V_{CC}$	V
		TTL-compatible inputs			0.8	
V_I	Input voltage¶ #		0		V_{CC}	V
V_{T+}	Positive-going threshold voltage#	CMOS-compatible inputs	$0.7V_{CC}$			V
		TTL-compatible inputs	2			
V_{T-}	Negative-going threshold voltage#	CMOS-compatible inputs			$0.2V_{CC}$	V
		TTL-compatible inputs			0.8	
V_{hys}	Hysteresis# ($V_{T+} - V_{T-}$)	CMOS-compatible inputs		1.7		V
		TTL-compatible inputs		0.4		
V_O	Output voltage§		0		V_{CC}	V
I_{OH}	High-level output current§		As specified on data sheets			mA
I_{OL}	Low-level output current§					
t_t	Input transition (rise and fall) times¶		0		25	ns
T_A	Operating temperature	Military temp range	−55		125	°C
		Commercial temp range	0		70	

§ Applies to external bidirectional and output buffers.
¶ Applies to external input and bidirectional buffers without hysteresis.
# Applies to external input buffers with hysteresis.

electrical and mechanical data summary

Electrical characteristics are presented on individual data sheets in this manual and unless otherwise noted, apply to standard cells prior to interconnect routing and mechanical packaging. Characteristics and effects of cell layout, routing, and interconnection of a completed ASIC design are covered in the post-layout simulation software. The capacitive loading effects of the package bond wire(s) and terminal(s) are assumed to be a portion of the 15-pF or 50-pF switching-characteristics load shown for the output and I/O cells. Typically, the packaging bond wire and terminal capacitance values range from 1 to 2 pF. Consult TI's design-center personnel when choosing ASIC packaging options.

recommended package selection

The following classes of conventional through-hole and surface-mount packages are recommended for ASIC designs:

- Dual-in-line (DIP): ceramic (J) and plastic (N)
- Plastic leaded chip carrier (PLCC): plastic (FN)
- Leadless chip carrier (LCC): ceramic (FK)
- Pin-grid-array (PGA): plastic (GP), and ceramic (GB)
- Quad flatpack (QFP): JEDEC plastic (PQ), EIAJ plastic (PB, PC, PJ), and ceramic (HQ).

Tables 2-1 through 2-3 list package options which satisfy a wide range of ASIC applications. TI will consider package requirements other than those listed.

TABLE 2-1. DUAL-IN-LINE AND CHIP CARRIER†

PIN COUNT	DUAL-IN-LINE (DIP)		CHIP CARRIER (CC)	
	PLASTIC N	CERAMIC J	PLASTIC (PLCC) FN	CERAMIC (LCC) FK
28	C	M	C	M
40	C	M		
44			C	M
48	C	M		
68			C	M
84			C	M

† C = Commercial, M = Military

TABLE 2-2. PIN-GRID ARRAY AND QUAD FLATPACKS†

PIN COUNT	PIN-GRID ARRAY (PGA)		QUAD FLATPACKS (QFP)		
			PLASTIC		CERAMIC
	PLASTIC GP	CERAMIC GB	EIAJ PB, PC, PJ	JEDEC PQ	HQ
68		M			
84		M			
100	C	M	C	C	M
120	C	M	C		
132	C	M		C	M
144	C	M			
160			C		
180	C	M			
208	C	M			
256		C,M			
264		M			

† C = Commercial, M = Military

TABLE 2-3. EIAJ QUAD FLATPACKS

PACKAGE DESIGNATOR	PINS	PIN DISTRIBUTION	BODY MOLD SIZE			PIN SPACING
			LENGTH	WIDTH	HEIGHT	
PB	120	30,30,30,30	28 mm	28 mm	3.85 mm	0.8 mm
PC	160	40,40,40,40	28 mm	28 mm	3.85 mm	0.65 mm
PJ	100	30,30,20,20	20 mm	14 mm	2.7 mm	0.65 mm

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

cell name prefixes and codes

Table 2-4 lists the prefixes used to name standard cells. Each standard cell is further coded, as in the example below, using the data in Table 2-5.

cell name example

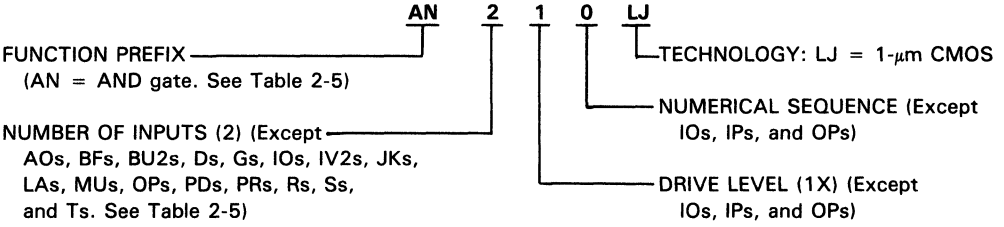


TABLE 2-4. INDEX TO MACRO FUNCTION PREFIXES

AN	AND Gates
AO	AND-OR Gates
BF	Multi-stage AND, NAND, NOR, OR Gates
BU	Buffers
CK	Clock Generator/Drivers
DE	Decoders/Demultiplexers
DF/DT	Flip-Flops, D-Type
EN	Exclusive-NOR Gates
EX	Exclusive-OR Gates
FI	First-In First-Out Memories
IO	Bidirectional I/O Buffers
IP	Input Buffers
IV	Inverters
JK	Flip-Flops, J-K Type
LA	Latches, D-Type and S-R
LH	Latches
MU	Multiplexers
NA	NAND Gates
NO	NOR Gates
OA	OR-AND/OR-NAND Gates
OP	Output Buffers
OR	OR Gates
OS	Oscillators
PD, PR	Pull-Down/Pull-Up Terminators
R	Registers
RF	Register Files
RH	Random Access Memories
S	Software Macros
TA	Flip-FLops, Toggle Type
TD	Scan Flip-Flops
TO	High- and Low-Level Tie-Off Gate
TP	Testability Functions

TABLE 2-5. CODING DEFINITIONS FOR FUNCTION PREFIXES

AOs (3rd and 4th characters):
- 22 = 2-wide, 2-inputs
- 24 = 2-wide, 4-inputs

BFs, Gs, and TOs (3rd, 4th, 5th characters):
- Three digit numerical sequence

BUs and IVs (3rd character):
- 2 = 3-State output

Ds, JKs, LAs, and TAs (3rd character):
- B = Both preset and clear inputs
- C = Clear input
- P = Preset input
- N = Neither preset nor clear input

DEs and MUs (3rd character):
- 1 = 1 select line (2-wide)
- 2 = 2 select lines (4-wide)
- 3 = 3 select lines (8-wide)

IOs and OPs (3rd character):
- H = IO or OP 1/8 speed
- I = IO or OP full speed
- J = IO or OP 1/2 speed
- K = IO or OP 1/4 speed

IOs and OPs (4th character):
- A = 16/16-mA sink/source current
- B = 24/16-mA sink/source current
- E = 48/16-mA sink/source current

IOs and OPs (4th character, cont'd):
- G = 64/16-mA sink/source current
- O = 10/16-mA sink/source current
- 2 = 2/2-mA sink/source current
- 4 = 4/4-mA sink/source current
- 6 = 6/6-mA sink/source current

IOs and OPs (5th character):
- 1 = CMOS input
- 4 = TTL input
- 7 = CMOS input with hysteresis
- 9 = TTL input with hysteresis

LA (3rd character):
- H = High enable
- L = Low enable

OPs (5th character):
- 0 = Totem-pole
- 1 = N-channel open drain
- 3 = 3-State

PDs and PRs (3rd, 4th, 5th character):
- 005 = 5-μA typical current
- 095 = 95-μA typical current
- 250 = 250-μA typical current
- 400 = 400-μA typical current

Rs and Ss (2nd, 3rd, 4th, 5th characters):
- Three or four digit numerical sequence

static random-access memories

The TSC500 Series includes 12 versions of hardwired static RAMs. Full parallel access is provided with data inputs, data outputs, and separate write or memory enables. When the memory is disabled, it is powered down. Access time and write-cycle time is the same from either the powered-up or powered-down states. The SRAM cells incorporate built-in testability circuits to accommodate parallel module testing (PMT). Other features are:

- Power-Down Current < 10 μA
- 3-State Outputs
- 12 Popular Organizations Available

SRAM SELECTION GUIDE

WRITE $t_{c(W)}$ (ns)	READ $t_{a(A)}$ (ns)	ORGANIZATION	CELL NAME
30	18.2	64W × 4B	RH000LJ
30	18.3	64W × 8B	RH001LJ
30	19.4	128W × 4B	RH002LJ
30	19.5	128W × 8B	RH003LJ
30	21.8	256W × 4B	RH004LJ
30	21.9	256W × 8B	RH005LJ
30	21.5	512W × 4B	RH006LJ
30	22	512W × 8B	RH007LJ
32	23.9	1024W × 4B	RH008LJ
32	24.4	1024W × 8B	RH009LJ
35	26.7	2048W × 4B	RH010LJ
36	27.7	2048W × 8B	RH011LJ

first-in first-out buffer memories

The TSC500 Series offers three versions of universal first-in first-out memories featuring status indicators for:

- Full
- Almost Full (Programmable)
- Half Full
- Almost Empty (Programmable)
- Empty

Programmability of the "almost" functions ranges from 1-to-4 for the 32-word FIFO to 1-to-8 for the 64-word and 128-word FIFOs with respect to either "Empty" or "Full".

FIFO SELECTION GUIDE

WRITE $t_{c(W)}$ (ns)	READ $t_{a(A)}$ (ns)	ORGANIZATION	CELL NAME
24.5	25.8	32W × 9B	FI503LJ
25	29	64W × 9B	FI603LJ
25.5	34.2	128W × 9B	FI703LJ

register files

The TSC500 Series provides seven high-performance register files that provide closely coupled memory for high-speed processors. Word widths of 8-, 9-, and 12-bits are implemented. Various levels of system parallelism are supported by 3- and 4-I/O port configurations. Both 16- and 64-word memories are offered.

REGISTER-FILE SELECTION GUIDE

PORTS	WRITE $t_{c(W)}$ (ns)	READ $t_{a(A)}$ (ns)	ORGANIZATION	CELL NAME
1 WRITE 2 READ	6	10.7	16W × 8B	RF400LJ
	6	10.9	16W × 9B	RF402LJ
	6	13.6	16W × 12B	RF403LJ
	6	12.3	64W × 8B	RF600LJ
	6	12.5	64W × 9B	RF602LJ
2 WRITE 2 READ	6	11	16W × 8B	RF401LJ
	6	12.5	64W × 8B	RF601LJ

input, output and bidirectional buffers

The TSC500 Series library contains a wide selection of input, output, and bidirectional buffers that facilitate design optimization. The input and bidirectional buffers are designed to accommodate the active pull-up or pull-down terminators as shown on page 2-15.

input buffers

Input buffers are available with CMOS- or TTL-level thresholds that feature noninverting versions with and without hysteresis. Also, clock buffers with CMOS-level or TTL-level thresholds are available. The clock buffers feature five separate clock-driver outputs with each output capable of driving a 3-pF load for a total of 15 pF. A guide to input buffer selection is shown below:

INPUT BUFFER SELECTION GUIDE

INPUT THRESHOLD	LOGIC TYPE	CELL NAME
CMOS	STANDARD	IPI01LJ
	HYSTERESIS	IPI07LJ
TTL	STANDARD	IPI04LJ
	HYSTERESIS	IPI09LJ
CMOS	CLOCK BUFFER	IPI11LJ
TTL	CLOCK BUFFER	IPI14LJ

All input buffers are designed to accommodate active pull-up or pull-down terminators.

Additionally, another class of input buffers features 2-pin crystal-controlled oscillator circuits embedded in an input design.

CRYSTAL-CONTROLLED OSCILLATOR SELECTION GUIDE

FREQUENCY (MHz)	OUTPUT DRIVE	CELL NAME
55 to 75	1X	OSI01LJ
35 to 55	1X	OSI02LJ
20 to 35	1X	OSI03LJ
1 to 20 (CMOS input)	1X	OSI04LJ
1 to 20 (TTL input)	1X	OSI24LJ

di/dt control

The rapid rate of change of current (di/dt) developed during high-speed logic-level transitions of output and bidirectional buffers creates unwanted voltage transients if the IC is installed in a system having high V_{CC} and/or ground impedances. See Figure 2-3(A). To assist designers in minimizing unwanted voltage transients, the TSC500 Series Standard Cell library includes output and bidirectional buffers having three levels of integral di/dt control. See Figure 2-3(B). Full-speed, non-di/dt-controlled versions are also offered for critical paths.

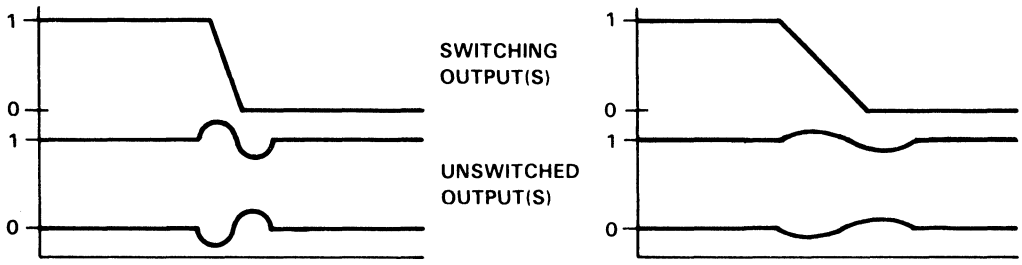


FIGURE 2-3. TYPICAL EFFECTS OF di/dt

When using non-di/dt-controlled output buffers, the following methods minimize the di/dt-related transients and reduce V_{CC} and ground trace impedances.

- Locate non-di/dt-controlled output and bidirectional buffers on low-inductance pins and adjacent to V_{CC} and ground pins
- Increase the width of V_{CC} and ground traces on printed circuit boards or use dedicated planes
- Increase the number of power V_{CC} and ground pins
- Minimize the number of simultaneously switching outputs

To assist designers in minimizing such effects, all output and bidirectional buffers in the TSC500 Series library are offered with three degrees of di/dt-control circuits and a full-speed version for critical paths. This permits the designer to achieve the levels of performance needed at each output and offers an opportunity to optimize the number of V_{CC} and ground pins needed.

The various degrees of di/dt control offered for different applications are shown in Table 2-6:

TABLE 2-6. di/dt BUFFER SELECTION ACCORDING TO APPLICATION

APPLICATION (TYPE OF LOAD DRIVEN)				CONSIDER USING BUFFER TYPE		di/dt LEVEL
CMOS/MOS LS	AC/ACT ALS/S/AS/F	TERMINATED LINES	CRITICAL PATHS	I/Os	OUTPUTS	
✓	✓	✓		IOHXXLJ	OPHXXLJ	1/8 Speed
✓	✓	✓		IOKXXLJ	OPKXXLJ	1/4 Speed
✓	✓	✓	✓	IOJXXLJ	OPJXXLJ	1/2 Speed
	✓	✓	✓	IOIXXLJ	OPIXXLJ	Full Speed

Detailed design guidelines on the selection of output and bidirectional buffers, and V_{CC} and ground pin requirements, are contained in the *CMOS Standard Cell Design Manual*.

output and bidirectional I/O characteristics

The high-level and low-level output voltage characteristics of external outputs and bidirectional I/Os are common for all types of cells. The following table provides the V_{OH} and V_{OL} parameters:

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage†	CMOS threshold	$I_{OH} \geq$ Rated	3.7			V
		TTL threshold		2.4			
		Any output without a terminator	$I_{OH} = -20\ \mu A$ See Note 1	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage	CMOS threshold	$I_{OL} \leq$ Rated			0.5	V
		TTL threshold				0.5	
		Any output without a terminator	$I_{OL} = 20\ \mu A$ See Note 1			0.1	

† Not applicable for external open-drain output buffers

NOTE 1: These limits apply when all other outputs are open.

output buffers

Output buffers are available in totem-pole, 3-state, or N-channel open-drain output configurations, with drive current ratings from 2 to 64 mA. Performance specifications are contained in the Workstation Library Summary (Section 5) and in the *TSC500 Series Family Data Sheet*. A guide to output buffer selection is shown in Table 2-7.

FIGURE 2-7. OUTPUT BUFFER SELECTION GUIDE (See Note 2)
(Each is characterized for CMOS and TTL loads)

OUTPUT CONFIGURATION	OUTPUT CURRENT (Sink/Source) (mA)	CELL NAME (and performance class)			
		1/8-SPEED	1/4-SPEED	1/2-SPEED	FULL-SPEED
TOTEM-POLE	2/2	OPH20LJ	OPK20LJ	OPJ20LJ	OPI20LJ
	4/4	OPH40LJ	OPK40LJ	OPJ40LJ	OPI40LJ
	6/6	OPH60LJ	OPK60LJ	OPJ60LJ	OPI60LJ
	10/10	OPH00LJ	OPK00LJ	OPJ00LJ	OPI00LJ
	16/16	OPHA0LJ	OPKA0LJ	OPJA0LJ	OPIA0LJ
	24/16	OPHB0LJ	OPKB0LJ	OPJB0LJ	OPIB0LJ
	48/16	OPHE0LJ	OPKE0LJ	OPJE0LJ	OPIE0LJ
	64/16	OPHG0LJ	OPKG0LJ	OPJG0LJ	OPIG0LJ
OPEN-DRAIN N-CHANNEL (See Note 3)	2	OPH21LJ	OPK21LJ	OPJ21LJ	OPI21LJ
	4	OPH41LJ	OPK41LJ	OPJ41LJ	OPI41LJ
	6	OPH61LJ	OPK61LJ	OPJ61LJ	OPI61LJ
	10	OPH01LJ	OPK01LJ	OPJ01LJ	OPI01LJ
	16	OPHA1LJ	OPKA1LJ	OPJA1LJ	OPIA1LJ
	24	OPHB1LJ	OPKB1LJ	OPJB1LJ	OPIB1LJ
	48	OPHE1LJ	OPKE1LJ	OPJE1LJ	OPIE1LJ
	64	OPHG1LJ	OPKG1LJ	OPJG1LJ	OPIG1LJ
3-STATE	2/2	OPH23LJ	OPK23LJ	OPJ23LJ	OPI23LJ
	4/4	OPH43LJ	OPK43LJ	OPJ43LJ	OPI43LJ
	6/6	OPH63LJ	OPK63LJ	OPJ63LJ	OPI63LJ
	10/10	OPH03LJ	OPK03LJ	OPJ03LJ	OPI03LJ
	16/16	OPHA3LJ	OPKA3LJ	OPJA3LJ	OPIA3LJ
	24/16	OPHB3LJ	OPKB3LJ	OPJB3LJ	OPIB3LJ
	48/16	OPHE3LJ	OPKE3LJ	OPJE3LJ	OPIE3LJ
	64/16	OPHG3LJ	OPKG3LJ	OPJG3LJ	OPIG3LJ

NOTES: 2. All output buffers are noninverting.
3. N-channel open-drain outputs are for sink current.

bidirectional input/output buffers

Bidirectional I/O buffers are available in 3-state output configurations, with drive current ratings from 2 to 64 mA. Performance specifications are contained in the Workstation Library Summary (Section 5) and in the *TSC500 Series Family Data Sheet*. A guide to bidirectional buffer selection is shown in Table 2-8.

TABLE 2-8. BIDIRECTIONAL I/O BUFFER SELECTION GUIDE (See Notes 4 and 5)
(Each is characterized for CMOS and TTL loads)

OUTPUT CURRENT (Sink/Source) (mA)	INPUT THRESHOLD	CELL NAME (and performance class)			
		1/8-SPEED	1/4-SPEED	1/2-SPEED	FULL-SPEED
2/2	CMOS	IOH21LJ	IOK21LJ	IOJ21LJ	IOI21LJ
	TTL	IOH24LJ	IOK24LJ	IOJ24LJ	IOI24LJ
4/4	CMOS	IOH41LJ	IOK41LJ	IOJ41LJ	IOI41LJ
	TTL	IOH44LJ	IOK44LJ	IOJ44LJ	IOI44LJ
6/6	CMOS	IOH61LJ	IOK61LJ	IOJ61LJ	IOI61LJ
	TTL	IOH64LJ	IOK64LJ	IOJ64LJ	IOI64LJ
10/10	CMOS	IOH01LJ	IOK01LJ	IOJ01LJ	IOI01LJ
	TTL	IOH04LJ	IOK04LJ	IOJ04LJ	IOI04LJ
16/16	CMOS	IOHA1LJ	IOKA1LJ	IOJA1LJ	IOIA1LJ
	TTL	IOHA4LJ	IOKA4LJ	IOJA4LJ	IOIA4LJ
24/16	CMOS	IOHB1LJ	IOKB1LJ	IOJB1LJ	IOIB1LJ
	TTL	IOHB4LJ	IOKB4LJ	IOJB4LJ	IOIB4LJ
48/OPEN	TTL w/hyst	IOHEPLJ	IOKEPLJ	IOJEPLJ	IOIEPLJ
48/16	CMOS	IOHE1LJ	IOKE1LJ	IOJE1LJ	IOIE1LJ
	TTL	IOHE4LJ	IOKE4LJ	IOJE4LJ	IOIE4LJ
64/16	CMOS	IOHG1LJ	IOKG1LJ	IOJG1LJ	IOIG1LJ
	TTL	IOHG4LJ	IOKG4LJ	IOJG4LJ	IOIG4LJ

NOTES: 4. All input buffers are noninverting.
5. All output buffers are 3-state and noninverting.

pull-up and pull-down active terminators

The following pull-up and pull-down terminators are offered for use with the input buffers and bidirectional I/O buffers:

TERMINATOR SELECTION GUIDE

TERMINATION	TYPICAL CURRENT (μA)	CELL NAME
PULL-DOWN	95	PD095LJ
PULL-UP	−400	PR400LJ
PULL-UP	−250	PR250LJ
PULL-UP	−95	PR095LJ
PULL-UP	−5	PR005LJ

3 Mechanical Data

D3030, DECEMBER 1988

mechanical data summary

Electrical characteristics presented in this data manual, unless otherwise noted, apply to standard cells prior to interconnect routing and packaging. Characteristics and effects of cell layout, routing, and interconnection of a completed ASIC design are covered in the post-layout simulation software. The capacitive loading effects of the package bond wire(s) and terminal(s) are assumed to be a portion of the 15-pF or 50-pF switching-characteristics load shown for the output and I/O cells. Typically, the packaging bond wire and terminal capacitance values range from 1 to 2 pF. Consult TI's design-center personnel for further assistance in choosing and specifying ASIC packaging options.

package selection

The following classes of conventional through-hole and surface-mount packages are recommended for ASIC designs:

- Dual-in-line (DIP), ceramic (J), and plastic (N)
- Leaded chip carrier (PLCC), plastic (FN)
- Leadless chip carrier (LCC) and ceramic (FK)
- Pin-grid-array (PGA), low-cost (GP), and ceramic (GB)
- Quad flatpack, JEDEC plastic (PQ), EIAJ plastic (PB,PC,PJ), and ceramic (HQ)

TI will review and consider supplying package requirements other than those listed.

ordering instructions

Implementing semiconductor solutions using TSC500 components normally results in an application-specific integrated circuit. Total specifications, including packaging and ordering instructions, are developed as a part of this Design Specification described in Section 1. Contact your TI representative for further information on getting started with an ASIC design.

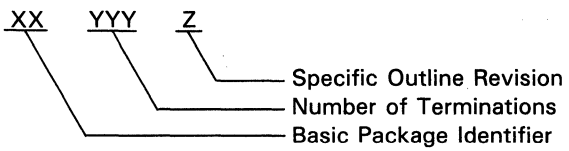
mechanical data — military

Military ASIC products are offered in a variety of hermetic ceramic packages. Included are the side-brazed ceramic dual-in-line (CDIP), leadless ceramic chip carrier, leaded ceramic chip carrier, and the ceramic pin grid array. Most packages conform to the mechanical outlines contained in Appendix C of MIL-M-38510. In the event of a conflict between the packages contained in MIL-M-38510 and other TI published mechanical outlines, MIL-M-38510 will take precedence.

Mechanical outlines of packages that are not contained in MIL-M-38510 are included in this document.

The published mechanical outlines for a given package may vary slightly from product to product. To identify the detailed outline drawing for a particular product, refer to the specific data sheet for that product.

There will be detail outline subsets within a generic package category that will be identified as follows:



A guide for the Military package selection is shown on the next page. These packages are recommended as a representative selection that satisfies a wide range of ASIC applications.

MIL-M-38510 Appendix C Outlines

NUMBER LEADS/ CONTACTS	CERAMIC DUAL-IN-LINE			FLAT PACKAGE			CHIP CARRIER PIN GRID ARRAY		
	MIL ID	TI ID	APPENDIX C OUTLINE	MIL ID	TI ID	APPENDIX C OUTLINE	MIL ID	TI ID	APPENDIX C OUTLINE
28		JD	D-10	3	FD	C-4			
40	Q	JD	D-5						
44					FD	C-5			
44					FJ	C-J4			
68					FD	C-7		GB	P-BC
68					FJ	C-J5			
84									P-AC
84									P-BB
84					FD	C-8			P-BC
84					FJ	C-J6			
100								GB	P-BE
108								GB	P-BD
120								GB	P-BE
132									P-BF
144									P-AG
180									P-AG
208									P-BJ
264									P-BJ

mechanical data — commercial

A guide for the commercial package selection is shown below. These packages are recommended as a representative selection that satisfies a wide range of ASIC applications.

COMMERCIAL PACKAGES

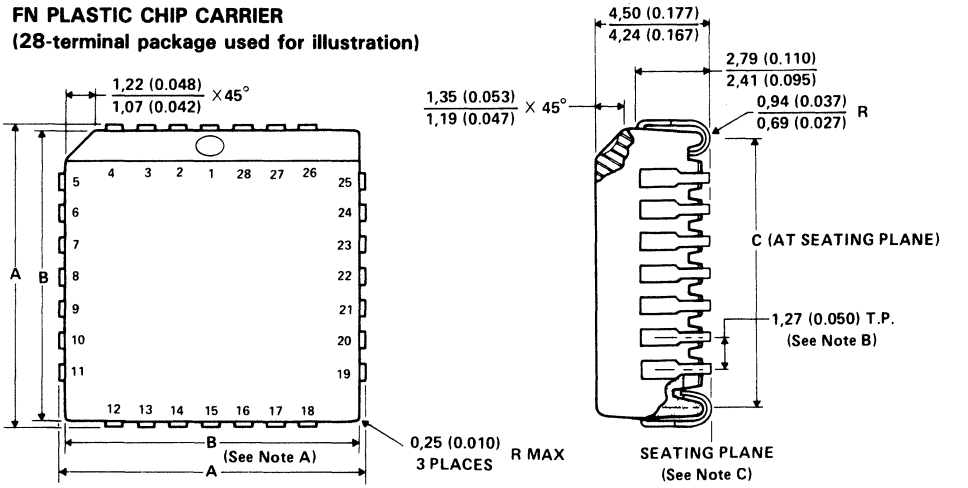
PLASTIC DIP		PLASTIC LCC				PLASTIC QFP (See Note 1)				PLASTIC PGA					
28 PIN	40 PIN	28 PIN	44 PIN	68 PIN	84 PIN	100 PIN	120 PIN	132 PIN	160 PIN	100 PIN	120 PIN	132 PIN	144 PIN	180 PIN	208 PIN
✓	✓	✓	✓	✓	✓					✓					
✓	✓		✓	✓	✓	✓●	●			✓	✓				
✓	✓		✓	✓	✓	✓●	●	✓		✓	✓	✓	✓		
				✓	✓		●	✓	●	✓	✓	✓	✓	✓	
							●	✓	●			✓	✓	✓	✓
							●	✓	●			✓	✓	✓	✓

NOTE 1: For the quad flatpack (QFP), ✓ = JEDEC and ● = EIAJ

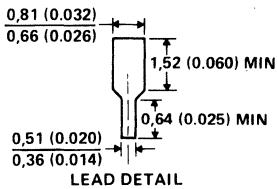
FN plastic chip carrier package

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN PLASTIC CHIP CARRIER
(28-terminal package used for illustration)



JEDEC OUTLINE	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
MO-047AB	28	12,32 (0.485)	12,57 (0.495)	11.43 (0.450)	11,58 (0.456)	10,41 (0.410)	10,92 (0.430)
MO-047AC	44	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,49 (0.610)	16,00 (0.630)
MO-047AE	68	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.956)	23,11 (0.910)	23.62 (0.930)
MO-047AF	84	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)



All dimensions and notes for the specified JEDEC outline apply.

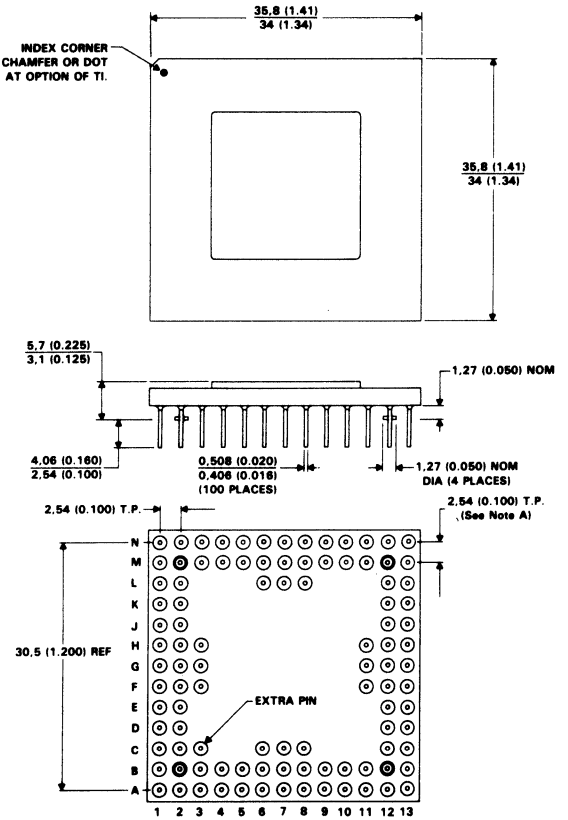
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. The centerline of the center pin on each side is within 0,10 (0.004) of the package centerline as determined by dimension B.
B. The location of each pin is within 0,127 (0.005) of its true position with respect to the center pin on each side.
C. The lead contact points are planar within 0,10 (0.004).

GP pin-grid-array plastic package

The GP family of plastic pin-grid-array packages consists of a high-temperature epoxy circuit board that positions and supports the package terminals, interconnections, bond pads, and metallized cavity. The conductively mounted die, bonding wires, and pads are enclosed within a moisture-resistant envelope. The anodized aluminum cover is secured with an epoxy preform. The solder-dipped terminals require no additional cleaning or processing when used in soldered assembly.

100-PIN GP



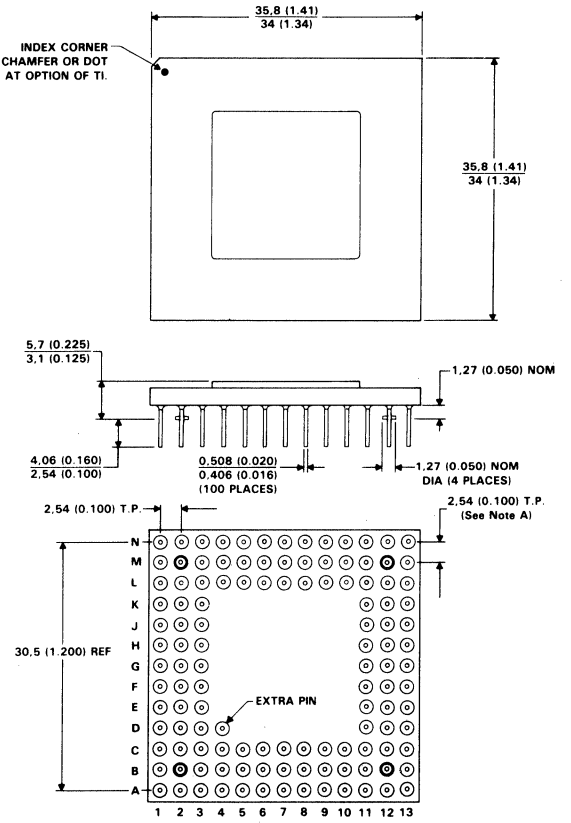
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the plastic.

GP pin-grid-array plastic package

The GP family of plastic pin-grid-array packages consists of a high-temperature epoxy circuit board that positions and supports the package terminals, interconnections, bond pads, and metallized cavity. The conductively mounted die, bonding wires, and pads are enclosed within a moisture-resistant envelope. The anodized aluminum cover is secured with an epoxy preform. The solder-dipped terminals require no additional cleaning or processing when used in soldered assembly.

120-PIN GP



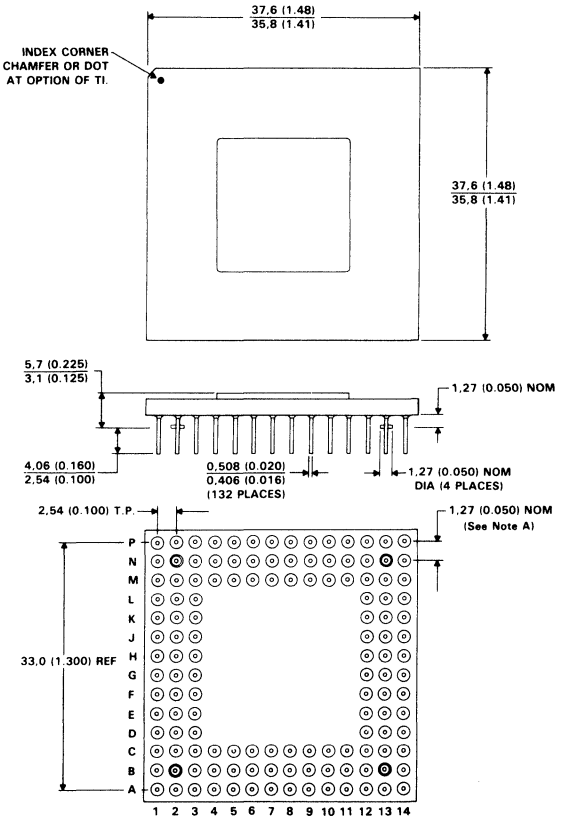
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the plastic.

GP pin-grid-array plastic package

The GP family of plastic pin-grid-array packages consists of a high-temperature epoxy circuit board that positions and supports the package terminals, interconnections, bond pads, and metallized cavity. The conductively mounted die, bonding wires, and pads are enclosed within a moisture-resistant envelope. The anodized aluminum cover is secured with an epoxy preform. The solder-dipped terminals require no additional cleaning or processing when used in soldered assembly.

132-PIN GP



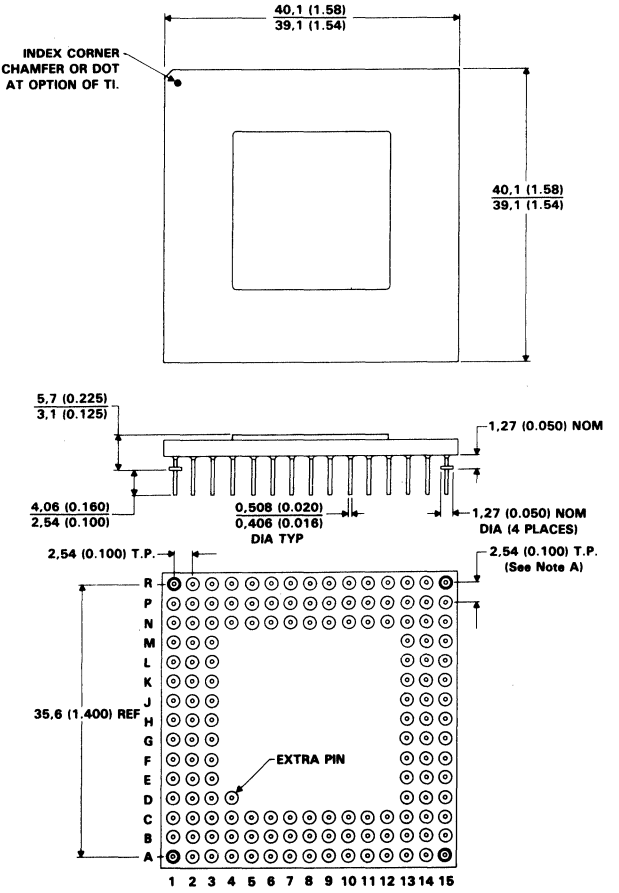
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the plastic.

GP pin-grid-array plastic package

The GP family of plastic pin-grid-array packages consists of a high-temperature epoxy circuit board that positions and supports the package terminals, interconnections, bond pads, and metallized cavity. The conductively mounted die, bonding wires, and pads are enclosed within a moisture-resistant envelope. The anodized aluminum cover is secured with an epoxy preform. The solder-dipped terminals require no additional cleaning or processing when used in soldered assembly.

144-PIN GP



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the plastic.

GP pin-grid-array plastic package

The GP family of plastic pin-grid-array packages consists of a high-temperature epoxy circuit board that positions and supports the package terminals, interconnections, bond pads, and metallized cavity. The conductively mounted die, bonding wires, and pads are enclosed within a moisture-resistant envelope. The anodized aluminum cover is secured with an epoxy preform. The solder-dipped terminals require no additional cleaning or processing when used in soldered assembly.

180-PIN GP

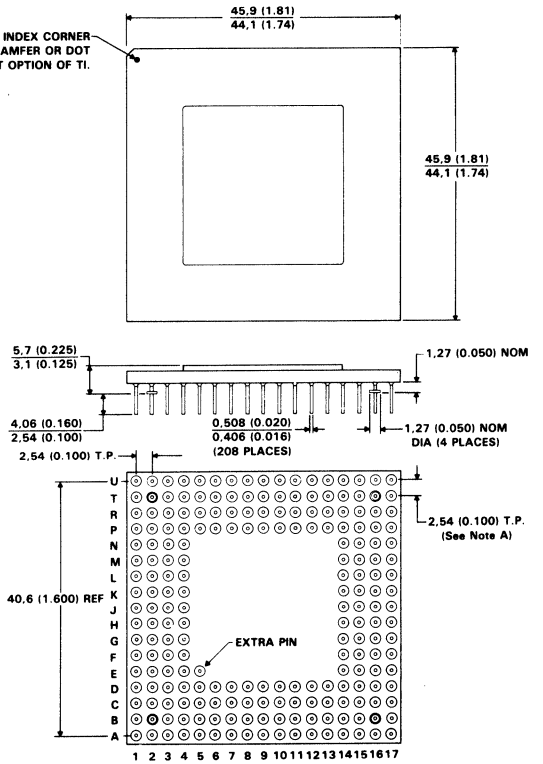
CONTACT ASIC FIELD SALES SPECIALIST
OR
REGIONAL TECHNOLOGY CENTER

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

GP pin-grid-array plastic package

The GP family of plastic pin-grid-array packages consists of a high-temperature epoxy circuit board that positions and supports the package terminals, interconnections, bond pads, and metallized cavity. The conductively mounted die, bonding wires, and pads are enclosed within a moisture-resistant envelope. The anodized aluminum cover is secured with an epoxy preform. The solder-dipped terminals require no additional cleaning or processing when used in soldered assembly.

208-PIN GP



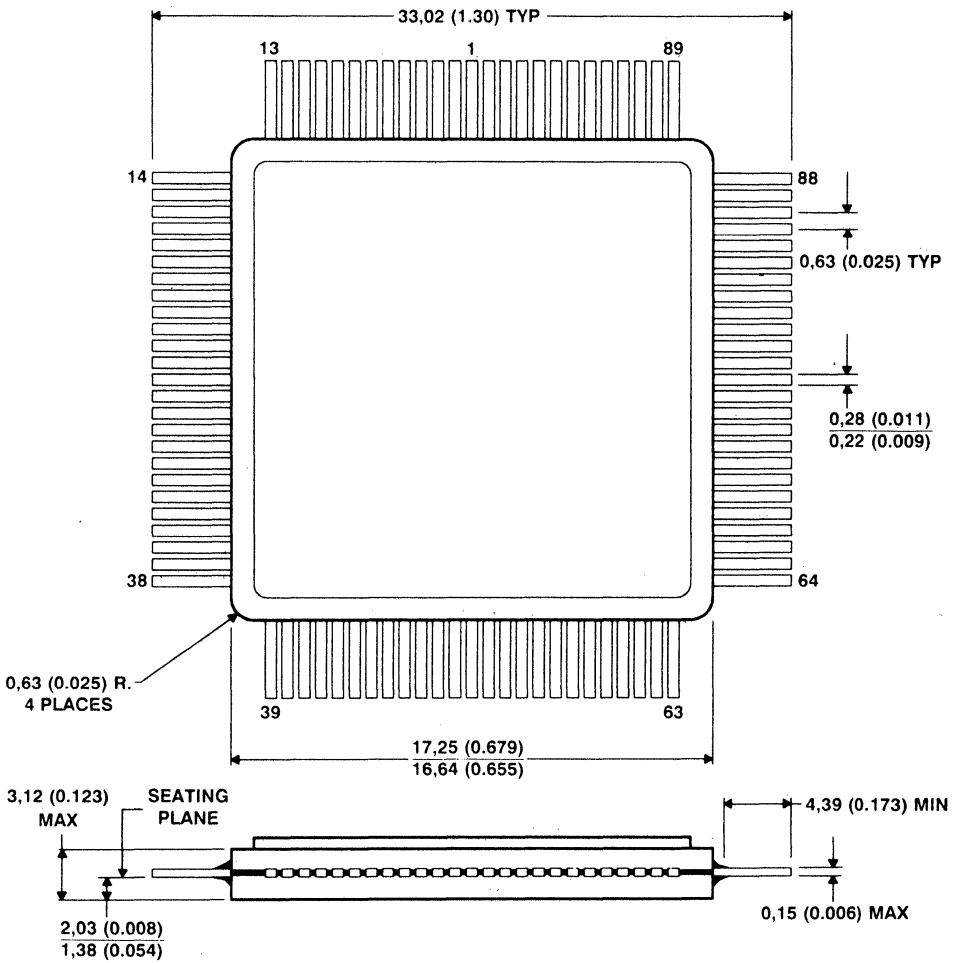
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,25 (0.010) radius relative to the center of the plastic.

HQ ceramic quadiform flat package

The 100-pin HQ ceramic package is housed in a quadiform flat package. It is hermetically sealed with 0.05-inch-lead spacing configured with straight leads for surface mounting capability.

100 PIN HQ

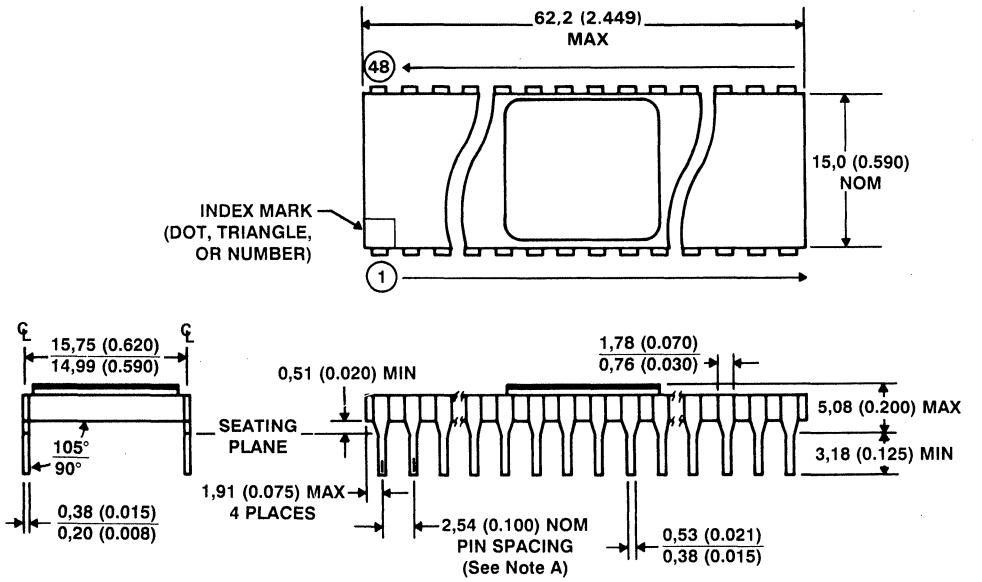


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

JD ceramic side-braze dual-in-line package

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.

48-PIN JD CERAMIC—SIDE-BRAZE



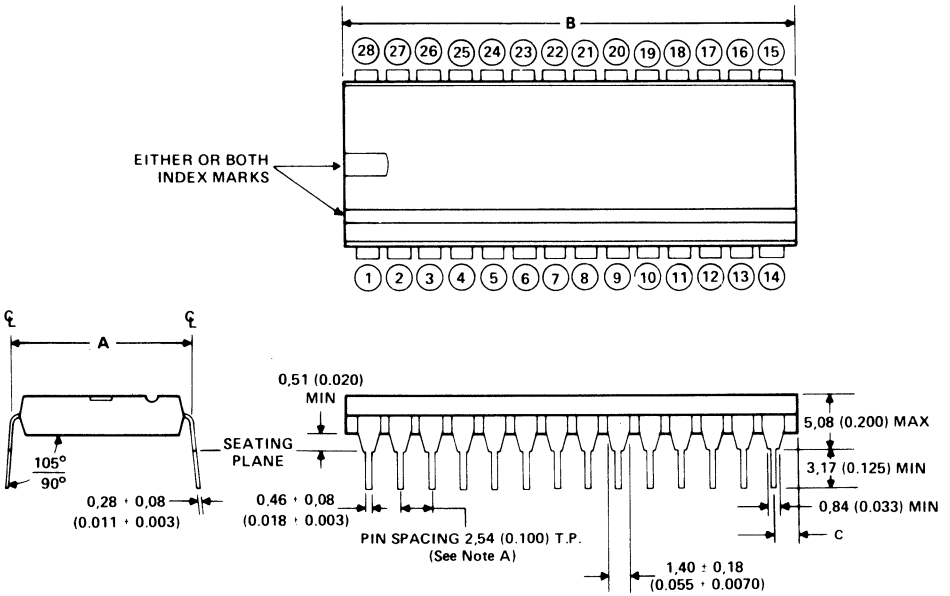
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

NW plastic dual-in-line packages

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remaining stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NW PLASTIC
(28-PIN PACKAGE SHOWN)



DIM \ PINS (N)	28	40
A ±0,25 (0.600)	15,24 (0.600)	15,24 (0.600)
B (MAX)	36,6 (1.440)	53,1 (2.090)
C ±0,51 (0.020)	1,27 (0.050)	1,91 (0.075)

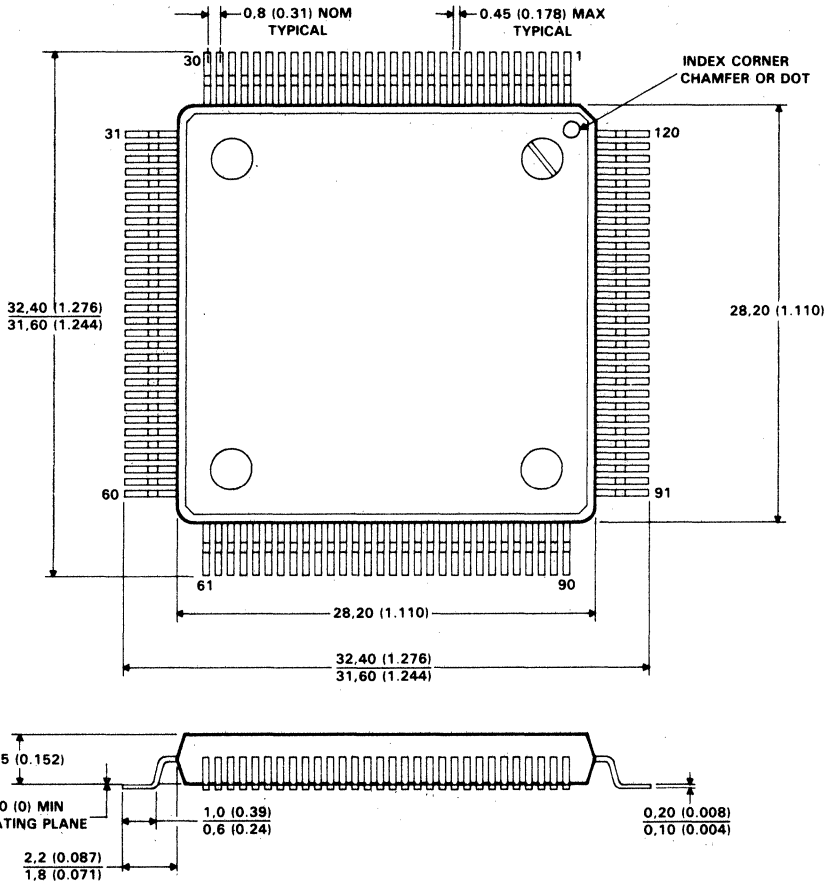
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located with 0,25 (0.010) of its true longitudinal position.

PB plastic quad-flat package (EIAJ)

The following quad-flat packages, PB, PC, PJ, and PQ, consist of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperature with no deformation, and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for surface-mount assembly. The solder-dipped leads require no additional cleaning or processing when used in soldered assembly.

120-PIN PB PLASTIC PACKAGE†

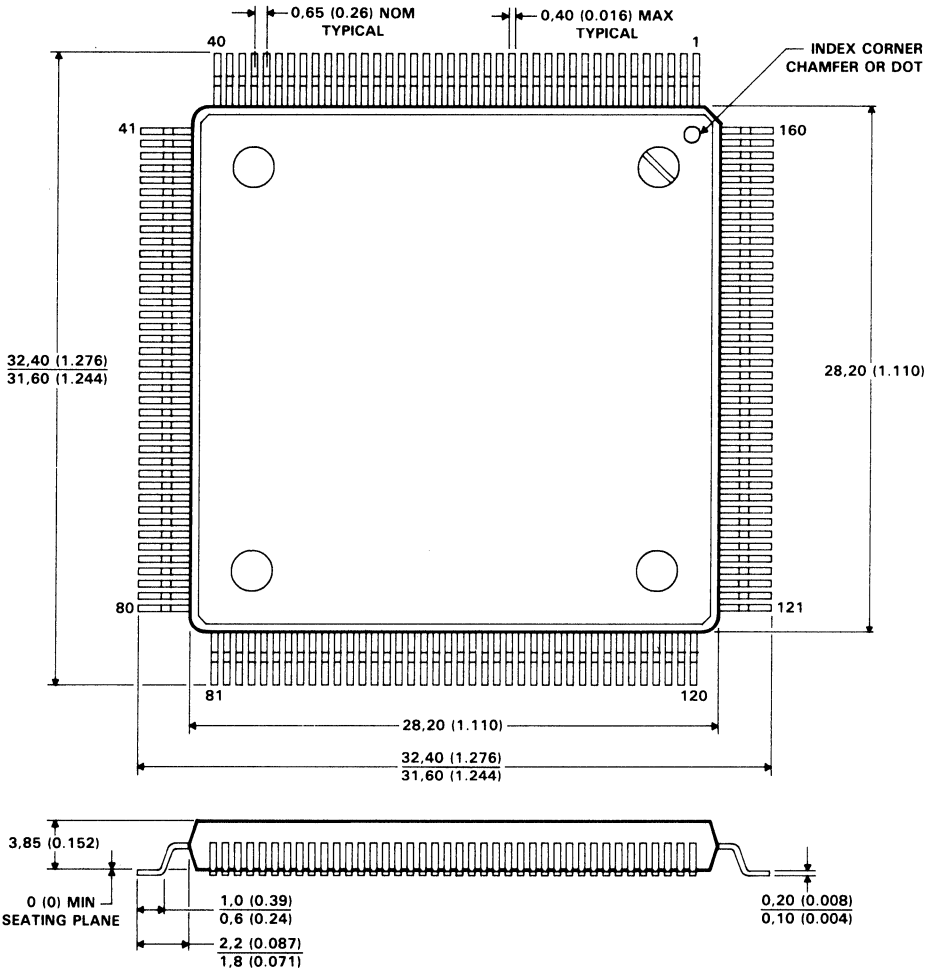


†All dimensions and notes for EIAJ QFP mechanical outline apply.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

PC plastic quad-flat package (EIAJ)

160-PIN PC PLASTIC PACKAGE†

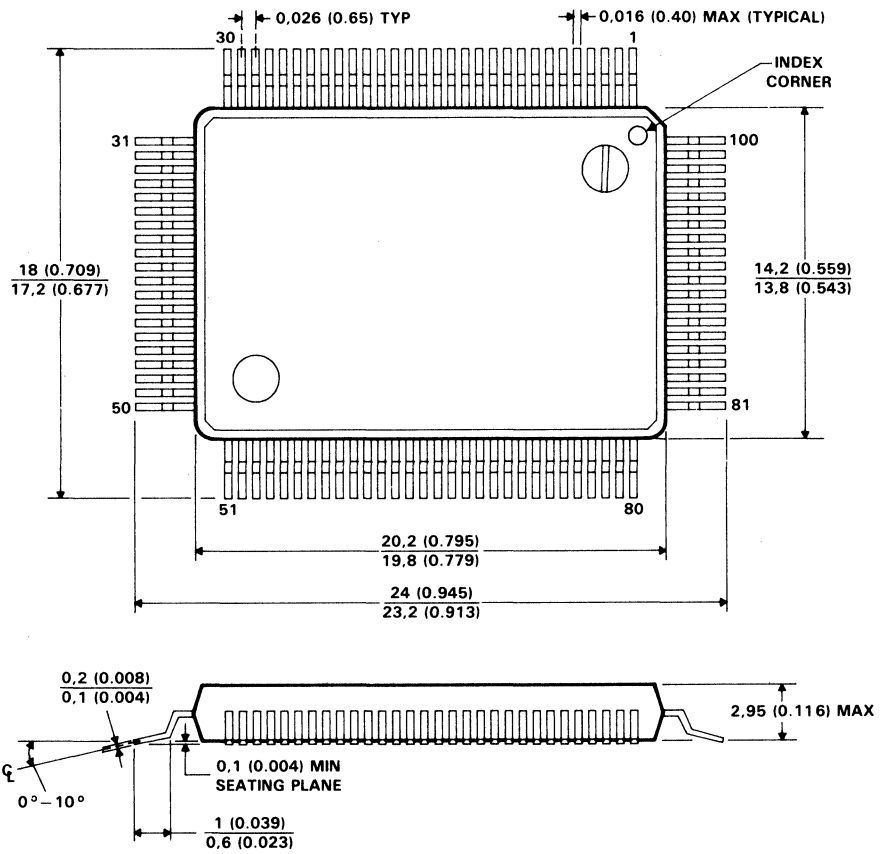


†All dimensions and notes for EIAJ QFP mechanical outline apply.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

PJ plastic quad-flat package (EIAJ)

100 PIN PJ†

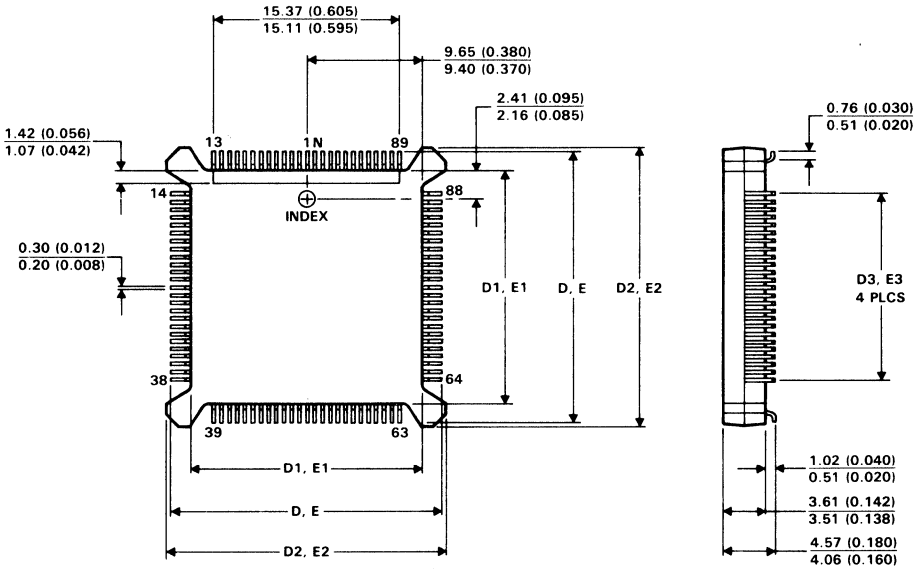


†All dimensions and notes for EIAJ QFP mechanical outline apply.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

PQ plastic quad-flat package

PQ QUAD FLAT PACKAGE
(100-lead package used for illustration)



JEDEC OUTLINE DESIGNATION†

DIMENSION	MO-069AD		MO-069AE	
	MIN	MAX	MIN	MAX
D, E	22,23 (0.875)	22,48 (0.885)	27.31 (1.075)	27,56 (1.085)
D1, E1	18,97 (0.747)	19,13 (0.753)	24,05 (0.947)	24,21 (0.953)
D2, E2	22,78 (0.897)	22,94 (0.903)	27,86 (1.097)	28,02 (1.103)
D3, E3	15,24 (0.6) REF		20,32 (0.8) REF	
N	100		132	

†All dimensions and notes for the specified JEDEC outline apply.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

4 Definitions and Ratings

This section provides an explanation of function tables, parameter measurement information, and a glossary.

explanation of function tables

Function tables used in this data manual employ symbols to describe the states of input stimuli and the resultant output response. Definitions of the symbols are provided followed by an explanation of how the symbols are used to construct an actual function table. The function table example is a sequential storage macro that includes a description of the relationships between the application of static conditions versus the dynamic inputs. Sufficient detail is included to provide for interpretation of truth tables used in this manual.

parameter measurement information

Test conditions used for measurement of electrical characteristics are provided in the TSC500 Series data or on each individual data sheet. Conditions used for measurement of switching characteristics are shown in this section in the form of load circuits and voltage waveforms. Test points are illustrated schematically on the load circuits and reference points are plotted on the voltage waveforms.

glossary

A glossary in this section defines the symbols, terms, and definitions used in this manual. They are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

EXPLANATION OF FUNCTION TABLES

The following symbols are now being used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . h	=	the level of steady-state inputs at inputs A through H, respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↑ or ↓
	=	one high-level pulse
	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↑ or ↓
?	=	unknown

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse,  or  , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables in this book are those of the shift registers. They use most of the symbols used in the other function tables, plus several others. The function table of a 4-bit bidirectional universal shift register, e.g., S194LJ is shown below:

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		SLSER	SRSER	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	QA_0	QB_0	QC_0	QD_0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QA_n	QB_n	QC_n
H	L	H	↑	X	L	X	X	X	X	L	QA_n	QB_n	QC_n
H	H	L	↑	H	X	X	X	X	X	QB_n	QC_n	QD_n	H
H	H	L	↑	L	X	X	X	X	X	QB_n	QC_n	QD_n	L
H	L	L	X	X	X	X	X	X	X	QA_0	QB_0	QC_0	QD_0

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs are reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

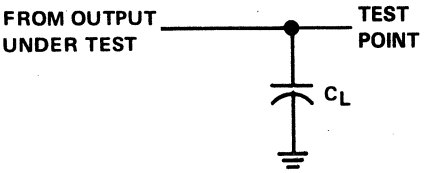
The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high, then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D, respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of the high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

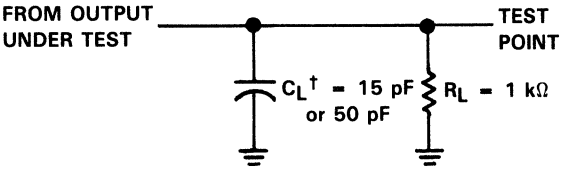


LOAD CIRCUIT

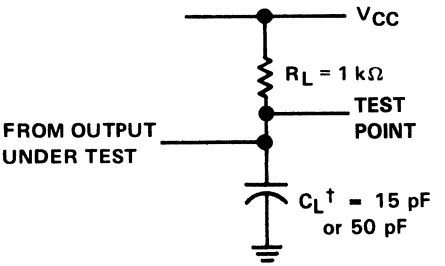
PARAMETER	CELLS	C_L†
t_{pd}	INTERNAL and INPUT	0
	OUTPUTS	15 pF or 50 pF

†C_L includes probe and test fixture capacitance.

FIGURE 4-1. TOTEM-POLE OUTPUTS



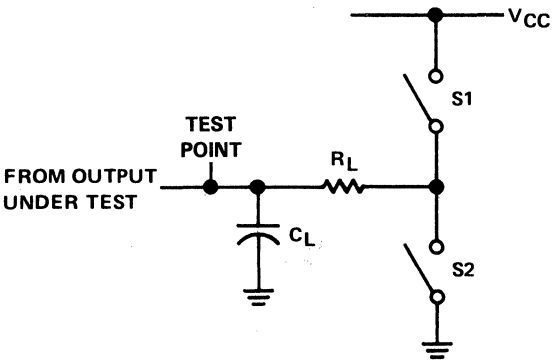
P-CHANNEL LOAD CIRCUIT



N-CHANNEL LOAD CIRCUIT

†C_L includes probe and test fixture capacitance.

FIGURE 4-2. OPEN-DRAIN OUTPUTS



LOAD CIRCUIT

PARAMETER		INTERNAL BUFFER		OUTPUT OR I/O		S1	S2
		R_L	C_L†	R_L	C_L†		
t_{en}	t_{PZH}	40 kΩ	0	1 kΩ	15 pF or 50 pF	OPEN	CLOSED
	t_{PZL}	20 kΩ				CLOSED	OPEN
t_{dis}	t_{PHZ}	40 kΩ	0	1 kΩ	50 pF	OPEN	CLOSED
	t_{PLZ}	20 kΩ				CLOSED	OPEN
t_{pd}	t_{PLH}	—	0	—	15 pF or 50 pF	OPEN	OPEN
	t_{PHL}						

†C_L includes probe and test fixture capacitance.

FIGURE 4-3. 3-STATE OUTPUTS

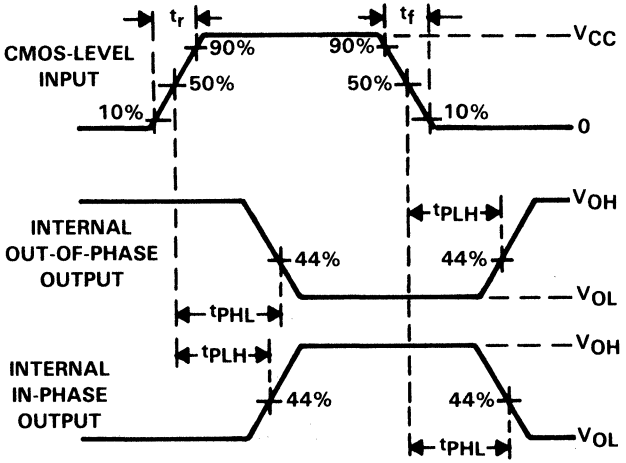


FIGURE 4-4. CMOS INPUT CELL AND CMOS 3-STATE BIDIRECTIONAL INPUT PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

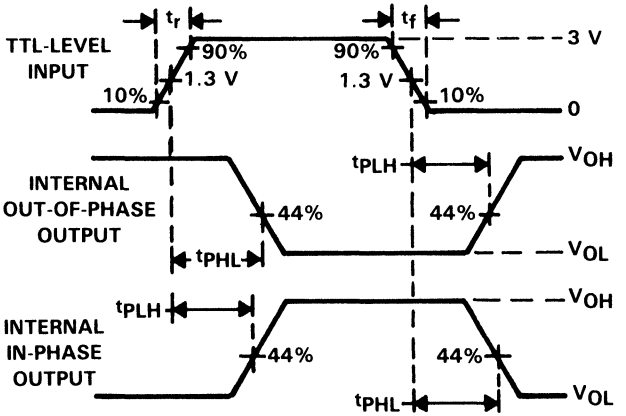


FIGURE 4-5. TTL INPUT CELL AND TTL 3-STATE BIDIRECTIONAL INPUT PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

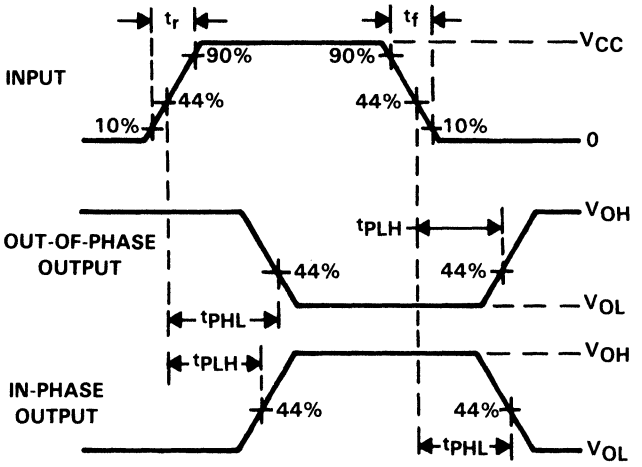


FIGURE 4-6. INTERNAL TOTEM-POLE OUTPUT PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

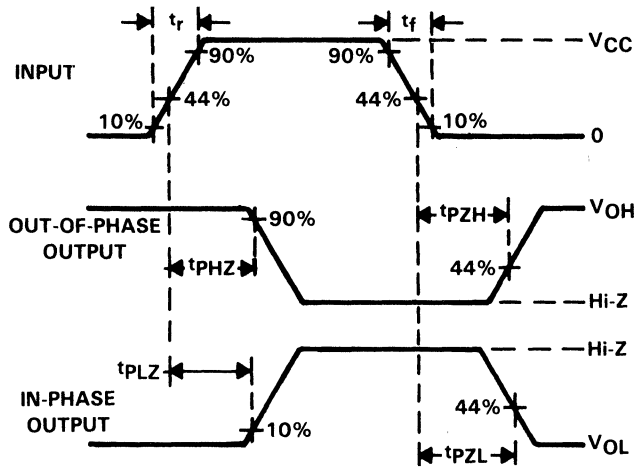


FIGURE 4-7. INTERNAL 3-STATE OUTPUT BUFFER DISABLE AND ENABLE VOLTAGE WAVEFORMS

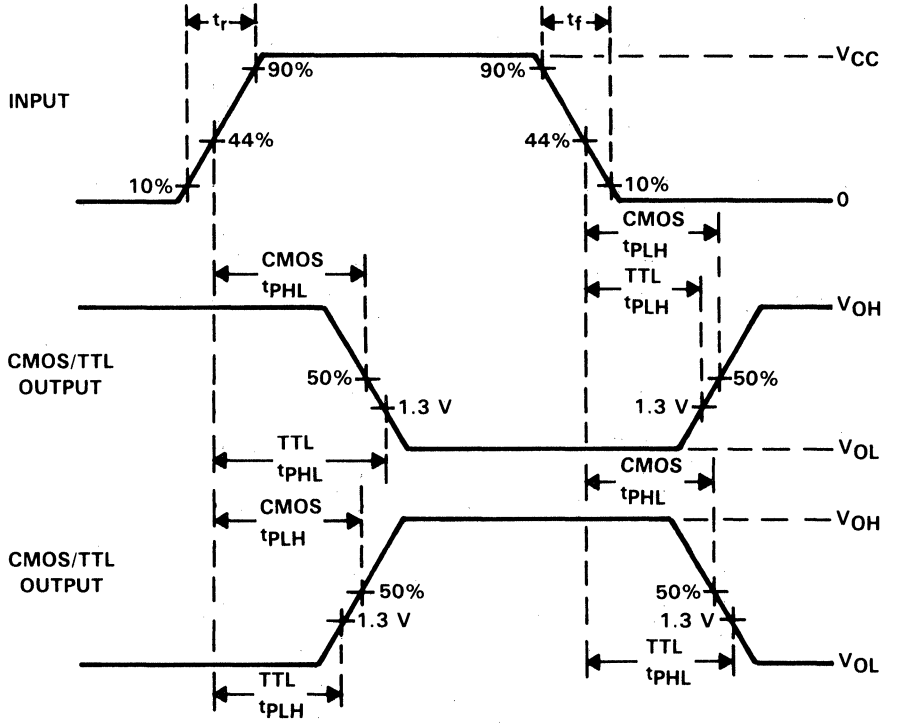


FIGURE 4-8. CMOS/TTL OUTPUT AND 3-STATE BIDIRECTIONAL INPUT/OUTPUT PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

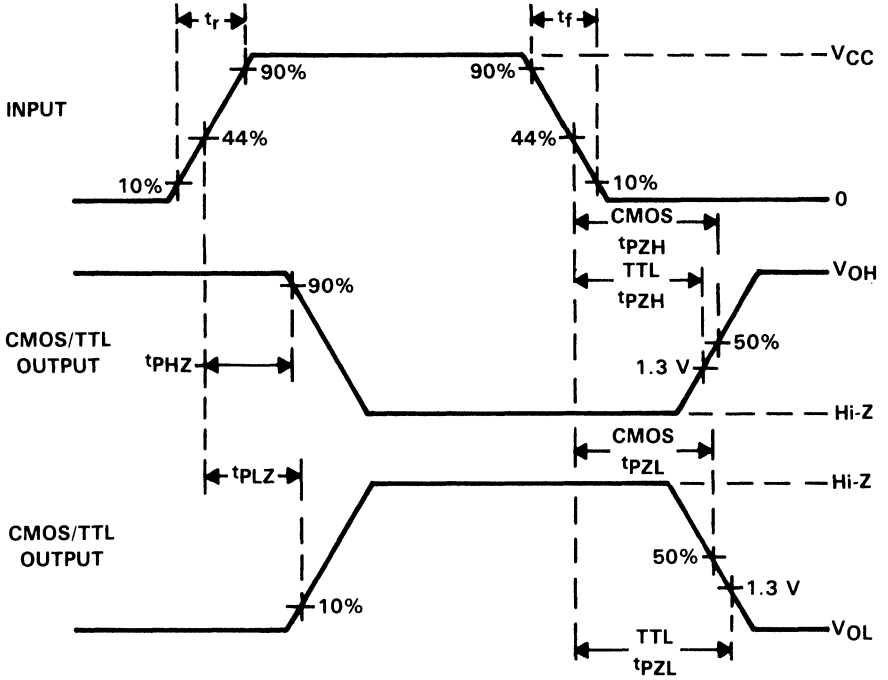


FIGURE 4-9. CMOS/TTL 3-STATE BIDIRECTIONAL INPUT/OUTPUT DISABLE AND ENABLE VOLTAGE WAVEFORMS

PART 1 — GENERAL CONCEPTS

Address — Any given memory location in which data can be stored or from which it can be retrieved.

Automatic Chip-Select/Power Down — (see Chip Enable Input)

Bit — Contraction of Binary digIT, i.e., a 1 or a 0; in electrical terms the value of a bit may be represented by the presence or absence of charge, voltage, or current.

Byte — A word of 8 bits (see word)

Chip Enable Input — A control input to an integrated circuit that when active permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and when inactive causes the integrated circuit to be in a reduced power standby mode.

Chip Select Input — Chip select inputs are gating inputs that control the input to and output from the memory. They may be of two kinds:

1. Synchronous — Clocked/latched with the memory clock. Affects the inputs and outputs for the duration of that memory cycle.
2. Asynchronous — Has direct asynchronous control of the inputs and outputs. In the read mode, an asynchronous chip select functions like an output enable.

Data — Any information stored or retrieved from a memory device.

Fully Static RAM — In a fully static RAM, the periphery as well as the memory array is fully static. The periphery is thus always active and ready to respond to input changes without the need for clocks. There is no precharge required for static periphery.

K — When used in the context of specifying a given number of bits of information, $1K = 2^{10} = 1024$ bits. Thus, $64K = 64 \times 1024 = 65{,}536$ bits.

Large-Scale Integration (LSI) — The description of any IC technology that enables condensing more than 100 gates onto a single chip.

Memory — A medium capable of storage of information from which the information can be retrieved.

Memory Cell — The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

Metal-Oxide Semiconductor (MOS) — The technology involving photolithographic layering of metal and oxide to produce a semiconductor device.

Mux-Factor — The number of multiplexed inputs that are made available on a single output.

Output Enable — A control input that, when true, permits data to appear at the memory output, and when false, causes the output to assume a high-impedance state. (See also chip select)

Parallel Access — A feature of a memory by which all the bits of a byte or word are entered simultaneously at several inputs or retrieved simultaneously from several outputs.

Power Down — A mode of a memory device during which the device is operating in a low-power or standby mode. Normally read or write operations of the memory are not possible under this condition.

Read — A memory operation whereby data is output from a desired address location.

Read/Write Memory — A memory in which each cell may be selected by applying appropriate electrical input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similiar electrical input signals.

Static RAM (SRAM) — A read/write random-access device within which information is stored as latched voltage levels. The memory cell is a static latch that retains data as long as power is applied to the memory array. No refresh is required. The type of periphery circuitry sub-categorizes static RAMs.

Very-Large-Scale Integration (VLSI) — The description of any IC technology that is much more complex than large-scale integration (LSI), and involves a much higher equivalent gate count. At this time, an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.

Volatile Memory — A memory in which the data content is lost when power supplied is disconnected.

Word — A series of one or more bits that occupy a given address location and that can be stored and retrieved in parallel.

Write — A memory operation whereby data is written into a desired address location.

Write Enable — A control signal that when true causes the memory to assume the write mode, and when false causes it to assume the read mode.

PART 2 — OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_i **Input Capacitance**
The inherent input capacitance on every input pin, which can vary with various inputs and outputs.

C_o **Output Capacitance**
The inherent output capacitance on every output pin, which can vary with various inputs and outputs.

C_{pd} **Power dissipation capacitance**
Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

f_{clock} **Clock frequency**
The rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of the output logic level in accordance with the specification.

f_{opr} **Operating frequency**
The rate at which the inputs of a circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes at the output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into† the V_{CC} supply terminal of an integrated circuit.

I_{IH} **High-level input current**
The current into† an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into† an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into† an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into† an output with input conditions applied that, according to the product specification, will establish a low level at the output.

† Current out of a terminal is given as a negative value.

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

V_{T+} **Positive-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} **Negative-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

T_A **Operating Free-Air Temperature**
The temperature range over which the device will operate and meet the specified electrical characteristics.

t_a **Access time**
The time interval between the application of a specified input pulse and the availability of valid signals at an output.

$t_{a(A)}$ **Access time from address**

$t_{a(S)}$, $t_{a(CS)}$ **Access time from chip select (low)**

t_c **Cycle time**
The time interval between the start and end of a cycle.

$t_{c(W)}$ **Write cycle time**
The minimum value is specified that must be allowed for the write digital circuit to perform correctly.

t_{dis} **Disable time (of a 3-state output)**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state: $t_{dis} = \frac{(t_{PHZ} + t_{PLZ})}{2}$.

$t_{dis(E)}$ **Output disable time after memory enable (high)**

$t_{dis(G)}$ **Output disable time after output enable (high)**

t_{en} **Enable time (of a 3-state output)**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low): $t_{en} = \frac{(t_{PZH} + t_{PZL})}{2}$.

NOTE: For memories, these intervals are often classified as access times.

$t_{en(E)}$ **Output enable time after memory enable (low)**

t_f **Fall time**
The time interval between two reference points (90% and 10% unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level.

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The hold time may have a negative value, in which case, the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

$t_{h(D)}$ **Data hold time (after write high)**

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level: $t_{pd} = \frac{(t_{PHL} + t_{PLH})}{2}$.

t_{PHL} **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a 3-state output) from high level**
The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a 3-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a 3-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a 3-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_r **Rise time**
The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level.

t_{sr} **Sense recovery time**
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.
NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The setup time may have a negative value, in which case, the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

$t_{su(D)}$ **Data setup time (before write high)**

t_t **Transition time (general)**
The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

$t_{w(W)}$ **Write pulse duration**

Δt_{PHL} **Delta propagation delay time, high-to-low level output**
The change in propagation delay time (t_{PHL}) with load capacitance.

Δt_{PHZ} **Delta disable time (of a 3-state output) from high level**
The change in disable time (t_{PHZ}) with load capacitance.

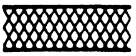
Δt_{PLH} **Delta propagation delay time, low-to-high level output**
The change in propagation delay time (t_{PLH}) with load capacitance.

Δt_{PLZ} **Delta disable time (of a 3-state output) from low level**
The change in disable time (t_{PLZ}) with load capacitance.

Δt_{PZH} **Delta enable time (of a 3-state output) to high level**
The change in enable time (t_{PZH}) with load capacitance.

Δt_{PZL} **Delta enable time (of a 3-state output) to low level**
The change in enable time (t_{PZL}) with load capacitance.

PART 3 — TIMING DIAGRAM CONVENTIONS

TIMING DIAGRAM SYMBOL	INPUT FORCING FUNCTIONS	OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low some time during a designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during a designated inverval
	Don't Care	State unknown or changing
	(Does not apply)	Centerline represents high-impedance (off) state

5 Library Summary

WORKSTATION LIBRARY SUMMARY
1-μm CMOS STANDARD CELLS

D3030, APRIL 1989

This section provides summary tables of functionally similar standard cells from which the designers can select specific functions having the performance criteria that best meet their design requirements. Grouped into functional categories, the summary provides:

- Standard cell identification (name)
- General description, such as number of inputs, width, size, or scope of the cell
- Output drive of internal cells and output current ratings of outputs and bidirectional I/Os
- The area of the cell or macro ratioed to the area of an NA210LJ cell
- Typical and maximum delay and delta delay times for the primary or data path
- Setup and hold times of the data path input for hardwired sequential functions

Maximum delay times are the worst-case path or input. The worst-case propagation times for the low-to-high and high-to-low transition may occur in different paths or inputs.

For complete specifications, consult the standard cell data sheets in Sections 6 through 22.

Data is from the 0°C to 70°C temperature range.

AND GATES

FUNCTION GATES HARDWIRED	CELL NAME	NO. OF INPUTS	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS C_L = 0 DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
AND	AN210LJ	2	1X	1.5	TYP	0.46	0.54	1.12	0.59
					MAX	0.86	1	2.16	1.08
	AN220LJ	2	2X	1.75	TYP	0.55	0.59	0.55	0.35
					MAX	1.03	1.13	0.06	0.64
	AN240LJ	2	4X	2.25	TYP	0.72	0.75	0.28	0.22
					MAX	1.34	1.44	0.58	0.46
	AN260LJ	2	6X	3	TYP	0.56	0.6	0.22	0.16
					MAX	1.07	1.11	0.4	0.32
	AN310LJ	3	1X	1.75	TYP	0.58	0.63	1.08	0.59
					MAX	1.18	1.2	2.1	1.1
	AN320LJ	3	2X	2	TYP	0.69	0.7	0.54	0.34
					MAX	1.4	1.33	1.06	0.7
	AN340LJ	3	4X	2.5	TYP	0.86	0.84	0.3	0.26
					MAX	1.78	1.78	0.64	0.52
	AN360LJ	3	6X	3.5	TYP	0.7	0.68	0.22	0.15
					MAX	1.39	1.35	0.44	0.32
	AN410LJ	4	1X	2	TYP	0.71	0.68	1.12	0.62
					MAX	1.53	1.36	2.18	1.14
	AN420LJ	4	2X	2.25	TYP	0.81	0.74	0.58	0.37
					MAX	1.75	1.54	1.16	0.7
	AN440LJ	4	4X	2.75	TYP	1.01	0.89	0.34	0.26
					MAX	2.27	1.95	0.68	0.52
	AN460LJ	4	6X	4	TYP	0.85	0.75	0.24	0.19
					MAX	1.82	1.54	0.46	0.4
	AN510LJ	5	1X	2.5	TYP	0.67	0.57	1.74	0.57
					MAX	1.37	1.18	3.52	0.94
	AN810LJ	8	1X	3.25	TYP	0.78	0.63	2.1	0.6
					MAX	1.68	1.38	4.23	1.14

AND-NOR, AND-OR, ARITHMETIC FUNCTIONS, AND COMPARATORS

FUNCTION GATES HARDWIRED	CELL NAME	NO. OF INPUTS	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS C_L = 0 DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
AND-OR	AO220LJ	4	2X	2	TYP	0.51	0.88	1.1	0.79
	$Y = (A \cdot B) + (C \cdot D)$				MAX	1.03	1.93	2.14	1.46
AND-NOR	AO221LJ	4	2X	1.75	TYP	0.43	0.36	2.03	0.91
	$Y = \overline{(A \cdot B) + (C \cdot D)}$				MAX	1.05	0.66	4.22	1.82
AND-OR	AO230LJ	6	X	2.75	TYP	0.56	1.31	1.11	0.91
	$Y = (A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2)$				MAX	1.22	3.64	2.18	1.73
	AO250LJ	9	X	4	TYP	0.63	1.31	1.28	1.04
	$Y = (A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2) + (D1 \cdot D2) + E1$				MAX	1.38	3.82	2.47	2.15
	AO320LJ	6	X	2.5	TYP	0.68	1.06	1.1	0.83
	$Y = (A1 \cdot A2 \cdot A3) + (B1 \cdot B2 \cdot B3)$				MAX	1.43	2.61	2.15	1.56
	AO420LJ	8	X	3.25	TYP	0.91	1.22	1.13	0.86
	$Y = (A1 \cdot A2 \cdot A3 \cdot A4) + (B1 \cdot B2 \cdot B3 \cdot B4)$				MAX	2.05	3.11	2.26	1.67
AND-NOR	AO421LJ	8	X	3.5	TYP	1.26	1.1	1.1	0.73
	$Y = \overline{(A1 \cdot A2 \cdot A3 \cdot A4) + (B1 \cdot B2 \cdot B3 \cdot B4)}$				MAX	3.16	2.46	2.11	1.32

FUNCTION ARITHMETIC OPERATORS SOFTWARE	MACRO NAME	WIDTH OR SIZE	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS C_L = 0 DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
MAGNITUDE COMPARATOR	S085LJ	4-BITS	2X	50	TYP	4.6	5.6	0.52	0.42
					MAX	7.4	8.6	1	0.62
ALU WITH LOOK-AHEAD	S181LJ	4-BITS	1X	89	TYP	5.3	4.6	1.88	1.64
					MAX	10.3	10	3.64	3.46
ODD-EVEN PARITY	S280LJ	9-BITS	2X	54	TYP	4.8	4.8	0.52	0.42
					MAX	8.7	9.2	1	0.62
BINARY FULL ADDER	S283LJ	4-BITS	2X	66.25	TYP	3	3.1	0.52	0.6
					MAX	5.5	6.2	1.04	1.24
MAGNITUDE COMPARATOR	S686LJ	8-BITS	2X	75.25	TYP	2.6	2.9	0.98	0.78
					MAX	5.6	7.6	2.04	1.62
IDENTITY COMPARATOR	S688LJ	8-BITS	2X	28.25	TYP	2.4	2.5	0.68	0.78
					MAX	3.9	4.8	1.34	1.62

MULTISTAGE-GATE BOOLEAN FUNCTIONS (AND-NOR)

FUNCTION MULTISTAGE GATES HARDWIRED	CELL NAME	NO. OF INPUTS	OUTPUT DRIVE	EQUIV NA210 NAND GATES	SWITCHING CHARACTERISTICS C_L = 0	DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
AND-NOR	BF001LJ	3	1X	1.5	TYP	0.41	0.36	2.1	0.92
	$Y = \overline{A1+(B1 \cdot B2)}$				MAX	0.97	0.58	4.26	1.82
	BF002LJ	4	1X	1.5	TYP	0.44	0.41	2.11	1.25
	$Y = \overline{A1+(B1 \cdot B2 \cdot B3)}$				MAX	1.24	0.75	4.22	2.56
	BF004LJ	5	1X	1.75	TYP	0.52	0.45	2.11	1.25
	$Y = \overline{(A1 \cdot A2)+(B1 \cdot B2 \cdot B3)}$				MAX	1.29	0.82	4.26	2.58
	BF005LJ	6	1X	2	TYP	0.64	0.5	2.09	2.6
	$Y = \overline{(A1 \cdot A2 \cdot A3)+(B1 \cdot B2 \cdot B3)}$				MAX	1.51	0.93	4.24	1.24
	BF006LJ	4	1X	1.75	TYP	0.68	0.39	3.1	0.93
	$Y = \overline{A1+A2+(B1 \cdot B2)}$				MAX	1.67	0.63	6.34	1.86
	BF007LJ	5	1X	1.75	TYP	0.77	0.45	3.09	1.28
	$Y = \overline{A1+A2+(B1 \cdot B2 \cdot B3)}$				MAX	2.09	0.86	6.34	2.64
	BF008LJ	5	1X	2	TYP	0.88	0.43	3.12	0.94
	$Y = \overline{A1+(B1 \cdot B2)+(C1 \cdot C2)}$				MAX	2.16	0.7	6.36	1.88
	BF009LJ	6	1X	2	TYP	0.99	0.51	3.11	1.28
	$Y = \overline{A1+(B1 \cdot B2)+(C1 \cdot C2 \cdot C3)}$				MAX	2.54	0.99	6.36	2.64
	BF010LJ	7	1X	2.25	TYP	1.01	0.48	3.1	1.31
	$Y = \overline{A1+(B1 \cdot B2 \cdot B3)+(C1 \cdot C2 \cdot C3)}$				MAX	2.61	0.93	6.34	2.7
	BF011LJ	6	1X	2.5	TYP	0.98	0.45	3.09	0.96
	$Y = \overline{(A1 \cdot A2)+(B1 \cdot B2)+(C1 \cdot C2)}$				MAX	2.36	0.73	6.36	1.9
	BF012LJ	7	1X	2.5	TYP	1.08	0.53	3.12	1.25
	$Y = \overline{(A1 \cdot A2)+(B1 \cdot B2)+(C1 \cdot C2 \cdot C3)}$				MAX	2.79	1.01	6.36	2.58
	BF013LJ	8	1X	2.5	TYP	1.24	0.54	3.11	1.32
	$Y = \overline{(A1 \cdot A2)+(B1 \cdot B2 \cdot B3)+(C1 \cdot C2 \cdot C3)}$				MAX	3.12	1.05	6.34	2.7
	BF014LJ	9	1X	2.75	TYP	1.47	0.62	3.11	1.31
	$Y = \overline{(A1 \cdot A2 \cdot A3)+(B1 \cdot B2 \cdot B3)+(C1 \cdot C2 \cdot C3)}$				MAX	3.66	1.2	6.34	2.7

MULTISTAGE-GATE BOOLEAN FUNCTIONS (OR-AND-NOR, AND-OR-AND-NOR)

FUNCTION MULTISTAGE GATES HARDWIRED	CELL NAME	NO. OF INPUTS	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS C_L = 0 DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
OR-AND-NOR	BF015LJ	4	1X	1.75	TYP	0.72	0.36	3.1	0.93
	$Y = \overline{A1+[B1\cdot(C1+C2)]}$				MAX	1.67	0.62	6.34	1.84
	BF016LJ	5	1X	2	TYP	0.95	0.4	3.13	0.93
	$Y = \overline{A1+[(B1+B2)\cdot(C1+C2)]}$				MAX	2.16	0.69	6.36	1.9
	BF017LJ	5	1X	1.75	TYP	0.88	0.44	3.11	1.25
	$Y = \overline{A1+[B1\cdot B2\cdot(C1+C2)]}$				MAX	2.04	0.87	6.34	2.62
	BF020LJ	5	1X	2	TYP	0.78	0.38	3.11	0.94
	$Y = \overline{(A1\cdot A2)+[B1\cdot(C1+C2)]}$				MAX	1.8	0.65	6.32	1.86
	BF022LJ	6	1X	2	TYP	0.97	0.47	3.09	1.28
	$Y = \overline{(A1\cdot A2)+[B1\cdot B2\cdot(C1+C2)]}$				MAX	2.23	0.93	6.34	2.64
	BF025LJ	6	1X	2.25	TYP	0.86	0.42	3.08	1.24
	$Y = \overline{(A1\cdot A2)\cdot A3+[B1\cdot(C1+C2)]}$				MAX	1.97	0.7	6.36	2.56
	BF027LJ	7	1X	2.25	TYP	0.88	0.62	2.33	1.18
	$Y = \overline{(A1\cdot A2\cdot A3)+[B1\cdot B2\cdot(C1+C2)]}$				MAX	1.99	1.32	4.76	2.46
	BF028LJ	8	1X	2.75	TYP	1.03	0.61	2.39	1.03
	$Y = \overline{(A1\cdot A2\cdot A3)+[B1\cdot(C1+C2)\cdot(D1+D2)]}$				MAX	2.36	1.24	4.86	2.38
AND-OR-AND-NOR	BF030LJ	5	1X	2	TYP	0.87	0.45	3.04	1.26
	$Y = \overline{A1+\{B1\cdot[C1+(D1\cdot D2)]\}}$				MAX	2.05	0.85	6.22	2.6
	BF034LJ	6	1X	2.25	TYP	0.76	0.51	2.58	1.25
	$Y = \overline{(A1\cdot A2)+\{B1\cdot[C1+(D1\cdot D2)]\}}$				MAX	1.74	1.02	5.26	2.56
	BF035LJ	7	1X	2.25	TYP	0.79	0.62	2.02	1.25
	$Y = \overline{(A1\cdot A2)+\{B1\cdot[(C1\cdot C2)+(D1\cdot D2)]\}}$				MAX	1.83	1.23	4.14	2.58

MULTISTAGE-GATE BOOLEAN FUNCTIONS (OR-NAND)

FUNCTION MULTISTAGE GATES HARDWIRED	CELL NAME	NO. OF INPUTS	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS C_L = 0 DELAY TIME t_{PLH} (ns)	 t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	 Δt_{PHL} (ns/pF)
OR-NAND	BF051LJ	3	1X	1.5	TYP	0.46	0.38	2.08	0.91
	$Y = \overline{A1 \cdot (B1 + B2)}$				MAX	0.97	0.57	4.21	1.79
	BF052LJ	4	1X	1.5	TYP	0.65	0.41	3.08	0.92
	$Y = \overline{A1 \cdot (B1 + B2 + B3)}$				MAX	1.62	0.62	6.32	1.83
	BF053LJ	4	1X	1.75	TYP	0.52	0.42	2.11	0.91
	$Y = \overline{(A1 + A2) \cdot (B1 + B2)}$				MAX	1.09	0.68	4.24	1.8
	BF054LJ	5	1X	1.75	TYP	0.74	0.45	3.09	0.92
	$Y = \overline{(A1 + A2) \cdot (B1 + B2 + B3)}$				MAX	1.81	0.74	6.31	1.84
	BF055LJ	6	1X	2	TYP	0.82	0.47	3.13	0.93
	$Y = \overline{(A1 + A2 + A3) \cdot (B1 + B2 + B3)}$				MAX	1.98	0.83	6.39	1.87
	BF056LJ	4	1X	1.75	TYP	0.59	0.38	2.09	1.24
	$Y = \overline{A1 \cdot A2 \cdot (B1 + B2)}$				MAX	1.28	0.79	4.23	2.55
	BF057LJ	5	1X	1.75	TYP	0.85	0.42	3.09	1.26
	$Y = \overline{A1 \cdot A2 \cdot (B1 + B2 + B3)}$				MAX	2.12	0.91	6.32	2.6
	BF058LJ	5	1X	2	TYP	0.67	0.48	2.11	1.24
	$Y = \overline{A1 \cdot (B1 + B2) \cdot (C1 + C2)}$				MAX	1.43	1.02	4.25	2.56
	BF059LJ	6	1X	2.25	TYP	0.78	0.52	3.12	1.25
	$Y = \overline{A1 \cdot (B1 + B2) \cdot (C1 + C2 + C3)}$				MAX	1.87	1.08	6.37	2.6
	BF060LJ	7	1X	2.25	TYP	1.01	0.57	3.13	1.27
	$Y = \overline{A1 \cdot (B1 + B2 + B3) \cdot (C1 + C2 + C3)}$				MAX	2.45	1.21	6.36	2.63
	BF062LJ	7	1X	2.5	TYP	0.92	0.62	3.13	1.25
	$Y = \overline{(A1 + A2) \cdot (B1 + B2) \cdot (C1 + C2 + C3)}$				MAX	2.11	1.32	6.39	2.59
	BF063LJ	8	1X	2.5	TYP	1.13	0.68	3.14	1.26
	$Y = \overline{(A1 + A2) \cdot (B1 + B2 + B3) \cdot (C1 + C2 + C3)}$				MAX	2.69	1.46	6.38	2.63
	BF064LJ	9	1X	2.75	TYP	1.22	0.76	3.16	1.28
	$Y = \overline{(A1 + A2 + A3) \cdot (B1 + B2 + B3) \cdot (C1 + C2 + C3)}$				MAX	2.85	1.66	6.38	2.65

MULTISTAGE-GATE BOOLEAN FUNCTIONS (AND-OR-NAND, OR-AND-OR-NAND)

FUNCTION						SWITCHING CHARACTERISTICS C_L = 0			
						DELAY TIME		DELTA DELAY	
MULTISTAGE GATES HARDWIRED	CELL NAME	NO. OF INPUTS	OUTPUT DRIVE	EQUIV NA210 NAND GATES		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
AND-OR-NAND	BF065LJ	4	1X	1.75	TYP	0.56	0.42	2.07	1.25
	$Y = \overline{A1 \cdot [B1 + (C1 \cdot C2)]}$				MAX	1.31	0.78	4.21	1.56
	BF066LJ	5	1X	2	TYP	0.72	0.51	2.1	1.25
	$Y = \overline{A1 \cdot [(B1 \cdot B2) + (C1 \cdot C2)]}$				MAX	1.65	0.97	4.23	2.57
	BF067LJ	5	1X	1.75	TYP	0.84	0.45	3.11	1.27
	$Y = \overline{A1 \cdot [B1 + B2 + (C1 \cdot C2)]}$				MAX	2.07	0.85	6.34	2.62
	BF068LJ	6	1X	2.25	TYP	0.93	0.48	3.11	1.29
	$Y = \overline{A1 \cdot [B1 \cdot (C1 \cdot C2) + (D1 \cdot D2)]}$				MAX	2.23	0.91	6.33	2.69
	BF069LJ	7	1X	2.5	TYP	1.17	0.65	3.11	1.3
	$Y = \overline{A1 \cdot [(B1 \cdot B2) + (C1 \cdot C2) + (D1 \cdot D2)]}$				MAX	2.78	1.18	6.35	2.67
	BF070LJ	5	1X	2	TYP	0.6	0.49	2.12	1.24
	$Y = \overline{(A1 + A2) \cdot [B1 + (C1 \cdot C2)]}$				MAX	1.44	0.89	4.25	2.57
	BF071LJ	6	1X	2.25	TYP	0.74	0.57	2.12	1.25
	$Y = \overline{(A1 + A2) \cdot [(B1 \cdot B2) + (C1 \cdot C2)]}$				MAX	1.71	1.1	4.27	2.56
	BF072LJ	6	1X	2	TYP	1	0.45	3.08	1.03
	$Y = \overline{(A1 + A2) \cdot [B1 + B2 + (C1 \cdot C2)]}$				MAX	2.45	0.79	6.28	2.13
	BF075LJ	6	1X	2	TYP	0.99	0.39	3.04	0.96
	$Y = \overline{(A1 + A2 + A3) \cdot [B1 + (C1 \cdot C2)]}$				MAX	2.45	0.65	6.22	1.93
OR-AND-OR-NAND	BF080LJ	5	1X	2	TYP	0.78	0.46	3.09	1.21
	$Y = \overline{A1 \cdot \{B1 + [C1 \cdot (D1 + D2)]\}}$				MAX	1.8	0.86	6.29	2.52
	BF081LJ	6	1X	2.25	TYP	1.07	0.45	3.05	1.09
	$Y = \overline{A1 \cdot \{B1 + [(C1 \cdot C2) \cdot (D1 + D2)]\}}$				MAX	2.49	0.85	6.23	2.25
	BF082LJ	6	1X	2.25	TYP	0.9	0.54	2.54	1.25
	$Y = \overline{A1 \cdot \{(B1 \cdot B2) + [C1 \cdot (D1 + D2)]\}}$				MAX	2.04	1.15	5.17	2.59
	BF088LJ	7	1X	2.5	TYP	1.27	0.47	3.16	0.92
	$Y = \overline{(A1 + A2 + A3) \cdot \{B1 + [C1 \cdot (D1 + D2)]\}}$				MAX	2.97	0.86	6.47	2.19

BUFFERS AND BUS INTERFACE

FUNCTION BUFFERS/ BUS INTERFACE	MACRO OR CELL NAME	NO. OF INPUTS	OUTPUT DRIVE	EQUIV NA210 NAND GATES	SWITCHING CHARACTERISTICS C_L = 0				
						DELAY TIME		DELTA DELAY	
						t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
TOTEM-POLE OUTPUTS (HARDWIRED)	BU110LJ	1	1X	2	TYP	2.4	3.89	1.2	1.32
					MAX	4.4	8	2.4	2.58
	BU111LJ	1	1X	2.5	TYP	4.74	4.65	1.16	1.48
					MAX	9.16	9.21	2.28	2.9
	BU112LJ	1	1X	2	TYP	1.6	2.04	1.16	1.32
					MAX	2.91	4.03	2.28	2.5
	BU113LJ	1	1X	3.25	TYP	4.77	5.17	0.54	0.4
					MAX	8.62	9.34	1.05	0.73
	BU114LJ	1	1X	3.25	TYP	8.11	8.29	0.54	0.4
					MAX	14.48	14.39	1	0.74
	BU120LJ	1	2X	1.25	TYP	0.39	0.55	0.54	0.32
					MAX	0.72	0.97	1.04	0.6
	BU130LJ	1	3X	1.75	TYP	0.49	0.62	0.34	0.25
					MAX	0.82	1.13	0.7	0.48
3-STATE OUTPUTS (HARDWIRED)	BU221LJ	2	2X	2.5	TYP	0.61	0.62	1.04	0.47
					MAX	1.25	1.15	2.09	0.92
	BU222LJ	2	2X	2.5	TYP	0.62	0.61	1.04	0.46
					MAX	1.28	1.12	2.08	0.91
	BU261LJ	2	6X	3.75	TYP	0.55	0.74	0.22	0.2
					MAX	0.99	1.41	0.45	0.43
	BU262LJ	2	6X	3.75	TYP	0.55	0.73	0.22	0.2
					MAX	0.99	1.41	0.45	0.43
3-STATE OUTPUTS (SOFTWARE)	S244LJ	2×4 BITS 2 EN	1X	18	TYP	0.8	0.8	2.08	1.22
					MAX	1.4	1.4	4.16	2.42
3-STATE OUTPUTS (SOFTWARE)	S245LJ	2×4 BITS 2 EN	1X	36	TYP	0.9	0.9	2.08	1.22
					MAX	1.6	1.5	4.16	2.42

CLOCK GENERATOR AND COUNTERS

FUNCTION CLOCK GENERATOR HARDWIRED	CELL NAME	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS C_L = 0 (See Note 1) DELAY TIME t_{PLH} (ns)	t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
TWO-PHASE NON-OVERLAP	CK120LJ	1X	5	TYP	5.99	1.01	2.04	0.86
				MAX	13.61	2.46	4.58	2.11

FUNCTION BINARY COUNTERS SOFTWARE	MACRO NAME	TYPE OF CLEAR	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS C_L = 0 (See Note 1) DELAY TIME t_{PLH} (ns)	t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
4-BIT BINARY	S161ALJ	ASYNCH (LOW)	1X	63	TYP	3.7	3.7	1.12	0.76
					MAX	7.4	7	2.12	1.4
4-BIT BINARY	S163ALJ	SYNCH (LOW)	1X	65.25	TYP	3.7	3.7	1.12	0.76
					MAX	7.4	7	2.12	1.4
4-BIT RIPPLE BINARY	S177LJ	ASYNCH (LOW)	1X	47.5	TYP	6.6	6	0.56	0.36
					MAX	14.1	12.8	1.1	0.7
4-BIT UP/DOWN BINARY	S191LJ	NONE (USE LOAD)	1X	80.5	TYP	4.9	3.7	1.54	1.32
					MAX	9.4	7.1	3	2.74
4-BIT UP/DOWN BINARY	S193LJ	ASYNCH (HIGH)	1X	73	TYP	4.2	3.5	0.56	0.38
					MAX	8.7	7.1	1.14	0.74
DUAL 4-BIT RIPPLE BINARY	S393LJ	ASYNCH (HIGH)	1X	50	TYP	4.8	4.5	0.46	0.46
					MAX	8.6	9.8	0.88	0.88
8-BIT BINARY 3-STATE	S590LJ	ASYNCH (LOW)	1X	130	TYP	3	4	2.14	1.33
					MAX	5.6	7.6	4.27	2.54
8-BIT BINARY 3-STATE	S593XLJ	ASYNCH (LOW)	1X	179	TYP	3.4	3.9	2.08	1.22
					MAX	6.3	7.3	4.16	2.42
4-BIT UP/DOWN BINARY	S669LJ	NONE (USE LOAD)	1X	69	TYP	2.7	4.5	1.12	0.76
					MAX	5.4	9.4	2.12	1.4

NOTE 1: Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in the engineering workstation library.

DECODERS, DEMULTIPLEXERS, AND PROGRAMMABLE DELAYS

FUNCTION DECODERS/ DEMULTI-PLEXERS	MACRO OR CELL NAME	SIZE	OUTPUT DRIVE	EQUIV NA210 NAND GATES	SWITCHING CHARACTERISTICS C_L = 0				
						DELAY TIME		DELTA DELAY	
						t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
HARDWIRED	DE210LJ	2-to-4	1X	4	TYP	0.41	0.46	1.08	0.94
					MAX	1.03	1.15	2.42	1.98
HARDWIRED	DE212LJ	2-to-4	1X	4	TYP	0.45	0.52	1.22	1.31
					MAX	1.05	1.34	2.82	2.78
3-ENABLES (SOFTWARE)	S137LJ	3-to-8	1X	40.25	TYP	2.9	4.9	0.68	0.78
					MAX	5.9	9.9	1.34	1.62
3-ENABLES (SOFTWARE)	S138LJ	3-to-8	1X	29.5	TYP	1.6	2.3	0.68	0.78
					MAX	3.2	5	1.34	1.62
1-ENABLE (SOFTWARE)	S139LJ	DUAL 2-to-4	1X	24	TYP	1.7	1.7	0.58	0.62
					MAX	2.9	2.8	1.14	1.28
1-ENABLE (SOFTWARE)	S155LJ	DUAL 2-to-4	1X	23.75	TYP	1.1	1.5	0.58	0.62
					MAX	2.5	3.3	1.14	1.28

D3030, APRIL 1989

D-TYPE FLIP-FLOPS

FUNCTION D-TYPE FLIP-FLOPS HARDWIRED (f_{clock})	CELL NAME	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS C_L = 0					
					DELAY TIME		DELTA DELAY		SETUP (MIN)	HOLD (MIN)
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)	t_{su} (ns)	t_h (ns)
130 MHz WITH CLRZ AND PREZ	DFB20LJ	2X	7.25	TYP	1.92	1.33	0.54	0.36	2	0.5
				MAX	4.19	2.83	1.1	0.7		
155 MHz WITH CLRZ	DFC20LJ	2X	6.75	TYP	1.86	1.26	0.52	0.36	2	0.25
				MAX	3.99	2.65	1.06	0.72		
165 MHz	DFN20LJ	2X	5.75	TYP	1.54	1.12	0.54	0.36	2	0.5
				MAX	3.25	2.31	1.04	0.68		
140 MHz WITH PREZ	DFP20LJ	2X	6.5	TYP	1.8	1.2	0.54	0.38	2	0.75
				MAX	3.91	2.62	1.08	0.66		
170 MHz WITH CLRZ AND PREZ	DTB10LJ	1X	6.25	TYP	1.64	1.55	1.14	1.38	2	0
				MAX	3.53	3.12	2.3	2.54		
150 MHz WITH CLRZ	DTC10LJ	1X	5.5	TYP	1.26	1.54	1.32	1.32	2	0.25
				MAX	2.49	3.12	2.56	2.36		
165 MHz	DTN10LJ	1X	5.25	TYP	1.43	1.37	1.12	1.34	2	0.25
				MAX	2.86	2.71	2.18	2.44		
165 MHz WITH PREZ	DTP10LJ	1X	5.5	TYP	1.48	1.42	1.22	1.36	2	0.25
				MAX	2.96	2.79	2.34	2.48		

D-TYPE FLIP-FLOPS

FUNCTION D-TYPE FLIP-FLOPS SOFTWARE (f_{clock})	CELL NAME	OUTPUT DRIVE	EQUIV NA210 NAND GATES	SWITCHING CHARACTERISTICS C_L = 0 (See Note 1)				
					DELAY TIME		DELTA DELAY	
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
4-BIT 3-STATE	S173LJ	1X	48	TYP	2.3	2.4	1.02	0.64
WITH CLRZ				MAX	4.5	4.6	2.08	1.2
6-BIT WITH CLRZ	S174LJ	1X	45	TYP	2.9	2.1	0.52	0.36
				MAX	5.5	3.9	1.06	0.72
4-BIT COMP OUT	S175LJ	1X	25.75	TYP	1.8	1.8	1.12	0.76
WITH CLRZ				MAX	3.5	3.5	2.12	1.4
8-BIT WITH CLRZ	S273LJ	1X	43.25	TYP	1.4	1.6	1.06	0.78
				MAX	2.9	3.3	2.04	1.4
8-BIT WITH 3-STATE	S374LJ	1X	51.5	TYP	1.6	1.7	2.2	1.38
				MAX	3.2	3.6	4.51	2.88

NOTE 1: Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in the engineering workstation library.

D3030, APRIL 1989

EXCLUSIVE-NOR, EXCLUSIVE-OR, AND FIRST-IN FIRST-OUT MEMORIES

FUNCTION GATES HARDWIRED	CELL NAME	NO. OF INPUTS	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS C_L = 0 DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
EX-NOR GATE	EN210LJ	2	1X	2.25	TYP	0.47	0.32	1.96	0.91
					MAX	0.98	0.59	3.97	1.77
EX-OR	EX210LJ	2	1X	1.75	TYP	0.44	0.54	1.09	0.88
					MAX	0.79	1.19	2.12	1.68
	EX220LJ	2	2X	2	TYP	0.51	0.52	0.52	0.6
					MAX	0.93	1.17	1.04	1.24
	EX240LJ	2	4X	2.5	TYP	0.64	0.63	0.28	0.4
					MAX	1.21	1.38	0.58	0.9

FUNCTION FIRST-IN FIRST-OUT MEMORIES WITH 3-STATE OUTPUTS† HARDWIRED	CELL NAME	OUTPUT DRIVE	EQUIV NA210 NAND GATES	CHARACTERISTICS DATA RATES READ (MHz)	DATA RATES WRITE (MHz)		FLAG TIMES (C_L = 1 pF) WRITE TO FULL (ns)	FLAG TIMES (C_L = 1 pF) READ TO EMPTY (ns)
32-WORD BY 9-BITS	FI503LJ	1X	3896			TYP	9.18	8.36
				45	40	MAX	19.56	17.47
64-WORD BY 9-BITS	FI603LJ	1X	6996			TYP	11.29	9.55
				45	40	MAX	23.78	20.03
128-WORD BY 9-BITS	FI703LJ	1X	12125			TYP	10.69	10.04
				40	39	MAX	22.35	21.06

† The above memories have the following status indicators:
FULL, ALMOST-FULL, HALF-FULL, ALMOST-EMPTY, AND EMPTY.

INPUT BUFFERS

FUNCTION INPUT BUFFERS NON-INVERTING† HARDWIRED	CELL NAME	INPUT THRESHOLD (V)	EQUIV NA210 NAND GATES	SWITCHING CHARACTERISTICS C_L = 0				
					DELAY TIME		DELTA DELAY	
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
	IPI01LJ	2.5 TYP (CMOS)	55	TYP	0.9	0.63	0.18	0.12
				MAX	1.42	1.13	0.29	0.26
	IPI04LJ	1.3 TYP (TTL)	55	TYP	1.41	1.16	0.18	0.24
				MAX	2.14	2.96	0.32	0.53
WITH HYSTERESIS	IPI07LJ	0.9/3.85 (CMOS)	56	TYP	1.62	2.06	0.2	0.19
				MAX	2.18	3.13	0.36	0.35
	IPI09LJ	0.8/2 (TTL)	56	TYP	1.29	1.77	0.18	0.25
				MAX	1.88	4.79	0.31	0.58
CLOCK DRIVER	IPI11LJ	2.5 TYP (CMOS)	65	TYP	1.55	1.45	0.15	0.19
				MAX	2.49	2.52	0.33	0.32
	IPI14LJ	1.3 TYP (TTL)	65	TYP	2.39	2.21	0.19	0.12
				MAX	4.49	4.44	0.32	0.26

† Use active terminator cell(s) to eliminate floating input(s).

1/8-SPEED BIDIRECTIONAL INPUTS/OUTPUTS

FUNCTION I/O 3-STATE BIDIRECTIONAL‡ HARDWIRED	CELL NAME	OUTPUT CURRENT Sink/Source (mA)	INPUT THRESHOLD (V)		OUTPUT SWITCHING CHARACTERISTICS† C_L = 15 pF			
					DELAY TIME		DELTA DELAY	
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
1/8-SPEED CMOS/ TTL OUTPUT WITH CMOS INPUT	IOHA1LJ	16/16	2.5 (CMOS)	TYP	6.92	7.4	40	50
				MAX	13.98	14.63	80	80
	IOHB1LJ	24/16	2.5 (CMOS)	TYP	6.91	8.98	40	40
				MAX	13.96	17.42	80	80
	IOHE1LJ	48/16	2.5 (CMOS)	TYP	6.99	8.32	40	30
				MAX	14.14	16.28	80	50
	IOHG1LJ	64/16	2.5 (CMOS)	TYP	7.08	8.04	40	20
				MAX	14.32	15.82	80	40
	IOH01LJ	10/10	2.5 (CMOS)	TYP	7.47	8.48	60	60
				MAX	15.03	16.62	110	110
	IOH21LJ	2/2	2.5 (CMOS)	TYP	13.98	18.08	190	200
				MAX	27.62	34.58	350	360
	IOH41LJ	4/4	2.5 (CMOS)	TYP	10.12	12.08	110	120
				MAX	20.07	23.24	200	210
	IOH61LJ	6/6	2.5 (CMOS)	TYP	8.82	10.15	80	90
				MAX	17.59	19.69	150	160

† CMOS output delay times are shown.
‡ Use active terminator cell(s) to eliminate floating I/O(s).

1/8-SPEED BIDIRECTIONAL INPUTS/OUTPUTS

FUNCTION I/O 3-STATE BIDIRECTIONAL‡ HARDWIRED	CELL NAME	OUTPUT CURRENT Sink/Source (mA)	INPUT THRESHOLD (V)		OUTPUT SWITCHING CHARACTERISTICS† C_L = 15 pF			
					DELAY TIME		DELTA DELAY	
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
1/8-SPEED CMOS/ TTL OUTPUT WITH TTL INPUT	IOHA4LJ	16/16	1.3	TYP	5.97	8.21	30	60
			(TTL)	MAX	12.4	15.94	60	100
	IOHB4LJ	24/16	1.3	TYP	5.96	9.82	30	50
			(TTL)	MAX	12.38	18.75	60	90
	IOHEPLJ	48/OPEN	0.8/2	TYP	7.38§	7.37¶	–	30¶
		(R_L = 1 kΩ)	(TTL w/hyst)	MAX	–	14.36¶	–	60¶
	IOHE4LJ	48/16	1.3	TYP	6.03	8.96	30	30
			(TTL)	MAX	12.55	17.28	60	60
	IOHG4LJ	64/16	1.3	TYP	6.11	8.61	30	30
			(TTL)	MAX	12.71	16.72	60	50
	IOH04LJ	10/10	1.3	TYP	6.31	9.53	40	80
			(TTL)	MAX	13.1	18.29	80	140
	IOH24LJ	2/2	1.3	TYP	10.92	21.17	110	270
			(TTL)	MAX	22.59	39.46	230	470
	IOH44LJ	4/4	1.3	TYP	8.19	13.91	70	150
			(TTL)	MAX	16.91	26.15	140	260
	IOH64LJ	6/6	1.3	TYP	7.28	11.56	50	110
			(TTL)	MAX	15.06	21.93	110	200

† TTL output delay times are shown.
‡ Use active terminator cell(s) to eliminate floating I/O(s).
§ = t_{PLZ}
¶ = t_{PZL} and Δt_{PZL}

FULL-SPEED BIDIRECTIONAL INPUTS/OUTPUTS

FUNCTION I/O 3-STATE BIDIRECTIONAL‡ HARDWIRED	CELL NAME	OUTPUT CURRENT Sink/Source (mA)	INPUT THRESHOLD (V)		OUTPUT SWITCHING CHARACTERISTICS† C_L = 15 pF			
					DELAY TIME		DELTA DELAY	
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
FULL-SPEED CMOS/TTL OUTPUT WITH CMOS INPUT	IOIA1LJ	16/16	2.5 (CMOS)	TYP	2.6	2.36	20	20
				MAX	5.3	4.75	40	40
	IOIB1LJ	24/16	2.5 (CMOS)	TYP	2.7	2.21	20	20
				MAX	5.45	4.5	40	30
	IOIE1LJ	48/16	2.5 (CMOS)	TYP	3.1	2.05	20	10
				MAX	6.28	4.26	40	20
	IOIG1LJ	64/16	2.5 (CMOS)	TYP	3.42	2.05	20	10
				MAX	6.98	4.3	30	20
	IOI01LJ	10/10	2.5 (CMOS)	TYP	2.77	2.67	30	30
				MAX	5.56	5.32	60	60
	IOI21LJ	2/2	2.5 (CMOS)	TYP	6.23	6.28	170	150
				MAX	12.15	11.99	320	260
	IOI41LJ	4/4	2.5 (CMOS)	TYP	3.98	4.05	80	80
				MAX	7.82	7.86	160	130
	IOI61LJ	6/6	2.5 (CMOS)	TYP	3.27	3.27	60	50
				MAX	6.47	6.42	110	90

† CMOS output delay times are shown.
‡ Use active terminator cell(s) to eliminate floating I/O(s).

FULL-SPEED BIDIRECTIONAL INPUTS/OUTPUTS

FUNCTION I/O 3-STATE BIDIRECTIONAL‡ HARDWIRED	CELL NAME	OUTPUT CURRENT Sink/Source (mA)	INPUT THRESHOLD (V)		OUTPUT SWITCHING CHARACTERISTICS† C_L = 15 pF			
					DELAY TIME		DELTA DELAY	
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
FULL-SPEED CMOS/TTL OUTPUT WITH TTL INPUT	IOIA4LJ	16/16	1.3 (TTL)	TYP	2.25	2.7	10	30
				MAX	4.65	5.34	30	50
	IOIB4LJ	24/16	1.3 (TTL)	TYP	2.35	2.48	10	20
				MAX	4.82	4.99	30	40
	IOIEPLJ	48/OPEN (R_L = 1 kΩ)	0.8/2 (TTL w/hyst)	TYP	7.61§	1.04¶	–	10¶
				MAX	–	2.02¶	–	30¶
	IOIE4LJ	48/16	1.3 (TTL)	TYP	2.77	2.24	10	10
				MAX	5.68	4.61	20	20
	IOIG4LJ	64/16	1.3 (TTL)	TYP	3.09	2.22	10	10
				MAX	6.39	4.61	20	20
	IOI04LJ	10/10	1.3 (TTL)	TYP	2.27	3.14	20	50
				MAX	4.67	6.13	40	80
	IOI24LJ	2/2	1.3 (TTL)	TYP	4.07	8.3	80	230
				MAX	8.45	15.24	180	390
	IOI44LJ	4/4	1.3 (TTL)	TYP	2.88	5.09	40	110
				MAX	5.91	9.58	90	190
	IOI64LJ	6/6	1.3 (TTL)	TYP	2.51	4	30	80
				MAX	5.14	7.64	60	130

† TTL output delay times are shown.
‡ Use active terminator cell(s) to eliminate floating I/O(s).
§ = t_{PLZ}
¶ = t_{PZL} and Δt_{PZL}

D3030, APRIL 1989

1/2-SPEED BIDIRECTIONAL INPUTS/OUTPUTS

FUNCTION I/O 3-STATE BIDIRECTIONAL‡ HARDWIRED	CELL NAME	OUTPUT CURRENT Sink/Source (mA)	INPUT THRESHOLD (V)		OUTPUT SWITCHING CHARACTERISTICS† C_L = 15 pF			
					DELAY TIME		DELTA DELAY	
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
1/2-SPEED CMOS/ TTL OUTPUT WITH CMOS INPUT	IOJA1LJ	16/16	2.5 (CMOS)	TYP	4.21	4.04	30	30
				MAX	8.53	8.12	60	50
	IOJB1LJ	24/16	2.5 (CMOS)	TYP	4.21	4.44	30	30
				MAX	8.55	8.91	60	50
	IOJE1LJ	48/16	2.5 (CMOS)	TYP	4.28	4.24	30	20
				MAX	8.69	8.65	60	30
	IOJG1LJ	64/16	2.5 (CMOS)	TYP	4.35	4.21	30	20
				MAX	8.81	8.64	50	30
	IOJ01LJ	10/10	2.5 (CMOS)	TYP	4.47	4.63	40	40
				MAX	8.97	9.17	80	80
	IOJ21LJ	2/2	2.5 (CMOS)	TYP	8.75	10.29	170	160
				MAX	17.18	19.55	320	280
	IOJ41LJ	4/4	2.5 (CMOS)	TYP	6.07	6.76	90	90
				MAX	11.99	13.03	170	150
	IOJ61LJ	6/6	2.5 (CMOS)	TYP	5.21	5.6	60	60
				MAX	10.36	10.92	120	110

† CMOS output delay times are shown.
‡ Use active terminator cell(s) to eliminate floating I/O(s).

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

1/2-SPEED BIDIRECTIONAL INPUTS/OUTPUTS

FUNCTION I/O 3-STATE BIDIRECTIONAL‡ HARDWIRED	CELL NAME	OUTPUT CURRENT Sink/Source (mA)	INPUT THRESHOLD (V)		OUTPUT SWITCHING CHARACTERISTICS† C_L = 15 pF			
					DELAY TIME		DELTA DELAY	
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
1/2-SPEED CMOS/ TTL OUTPUT WITH TTL INPUT	IOJA4LJ	16/16	1.3 (TTL)	TYP	3.64	4.53	20	40
				MAX	7.56	8.94	40	70
	IOJB4LJ	24/16	1.3 (TTL)	TYP	3.65	4.91	20	30
				MAX	7.58	9.68	40	60
	IOJEPLJ	48/OPEN (R_L = 1 kΩ)	0.8/2 (TTL w/hyst)	TYP	7.39§	3.24¶	–	20¶
				MAX	–	6.58¶	–	40¶
	IOJE4LJ	48/16	1.3 (TTL)	TYP	3.71	4.59	20	20
				MAX	7.71	9.24	40	40
	IOJG4LJ	64/16	1.3 (TTL)	TYP	3.77	4.53	20	20
				MAX	7.82	9.17	40	30
	IOJ04LJ	10/10	1.3 (TTL)	TYP	3.75	5.29	30	60
				MAX	7.75	10.25	50	100
	IOJ24LJ	2/2	1.3 (TTL)	TYP	6.41	12.57	90	230
				MAX	13.22	23.19	180	400
	IOJ44LJ	4/4	1.3 (TTL)	TYP	4.73	8.02	50	120
				MAX	9.75	15.07	100	210
	IOJ64LJ	6/6	1.3 (TTL)	TYP	4.2	6.53	40	80
				MAX	8.67	12.44	70	150

† TTL output delay times are shown.
‡ Use active terminator cell(s) to eliminate floating I/O(s).
§ = t_{PLZ}
¶ = t_{PLZ} and Δt_{PLZ}

1/4-SPEED BIDIRECTIONAL INPUTS/OUTPUTS

FUNCTION I/O 3-STATE BIDIRECTIONAL‡ HARDWIRED	CELL NAME	OUTPUT CURRENT Sink/Source (mA)	INPUT THRESHOLD (V)		OUTPUT SWITCHING CHARACTERISTICS† C_L = 15 pF			
					DELAY TIME		DELTA DELAY	
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
1/4-SPEED CMOS/ TTL OUTPUT WITH CMOS INPUT	IOKA1LJ	16/16	2.5 (CMOS)	TYP	5.56	5.63	40	40
				MAX	11.27	11.24	70	70
	IOKB1LJ	24/16	2.5 (CMOS)	TYP	5.56	6.53	40	40
				MAX	11.28	12.88	70	70
	IOKE1LJ	48/16	2.5 (CMOS)	TYP	5.63	6.11	40	20
				MAX	11.43	12.2	70	40
	IOKG1LJ	64/16	2.5 (CMOS)	TYP	5.71	5.98	40	20
				MAX	11.57	12.02	70	40
	IOK01LJ	10/10	2.5 (CMOS)	TYP	5.97	6.47	50	50
				MAX	12.03	12.77	90	90
	IOK21LJ	2/2	2.5 (CMOS)	TYP	11.38	14.14	170	180
				MAX	22.41	27.01	330	320
	IOK41LJ	4/4	2.5 (CMOS)	TYP	8.1	9.36	100	100
				MAX	15.06	18.04	180	180
	IOK61LJ	6/6	2.5 (CMOS)	TYP	7.02	7.81	70	50
				MAX	14.01	15.19	130	130

† CMOS output delay times are shown.
‡ Use active terminator cell(s) to eliminate floating I/O(s).

1/4-SPEED BIDIRECTIONAL INPUTS/OUTPUTS

FUNCTION I/O 3-STATE BIDIRECTIONAL‡ HARDWIRED	CELL NAME	OUTPUT CURRENT Sink/Source (mA)	INPUT THRESHOLD (V)		OUTPUT SWITCHING CHARACTERISTICS† C_L = 15 pF			
					DELAY TIME		DELTA DELAY	
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
1/4-SPEED CMOS/ TTL OUTPUT WITH TTL INPUT	IOKA4LJ	16/16	1.3 (TTL)	TYP	4.8	6.29	30	50
				MAX	9.99	12.31	50	90
	IOKB4LJ	24/16	1.3 (TTL)	TYP	4.79	7.19	30	40
				MAX	9.99	13.95	50	80
	IOKEPLJ	48/OPEN (R_L = 1 kΩ)	0.8/2 (TTL w/hyst)	TYP	7.38§	5.15¶	–	30¶
				MAX	–	10.24¶	–	50¶
	IOKE4LJ	48/16	1.3 (TTL)	TYP	4.86	6.6	30	30
				MAX	10.13	13	50	50
	IOKG4LJ	64/16	1.3 (TTL)	TYP	4.92	6.43	20	20
				MAX	10.26	12.75	50	40
	IOK04LJ	10/10	1.3 (TTL)	TYP	5.02	7.33	30	70
				MAX	10.44	14.16	70	120
	IOK24LJ	2/2	1.3 (TTL)	TYP	8.69	16.82	100	250
				MAX	17.94	31.26	200	430
	IOK44LJ	4/4	1.3 (TTL)	TYP	6.47	10.91	60	140
				MAX	13.36	20.51	120	230
	IOK64LJ	6/6	1.3 (TTL)	TYP	5.74	8.98	50	100
				MAX	11.89	17.07	90	170

† TTL output delay times are shown.
‡ Use active terminator cell(s) to eliminate floating I/O(s).
§ = t_{PLZ}
¶ = t_{PZL} and Δt_{PZL}

D3030, APRIL 1989

INVERTERS

FUNCTION INVERTERS HARDWIRED	CELL NAME	NO. OF INPUTS	OUTPUT DRIVE	EQUIV NA210 NAND GATES	SWITCHING CHARACTERISTICS C_L = 0 (A to Y)				
						DELAY TIME		DELTA DELAY	
						t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
INVERTERS	IV101LJ	1	10X	4.5	TYP	0.88	0.8	0.18	0.1
					MAX	1.69	1.58	0.23	0.21
	IV110LJ	1	1X	0.75	TYP	0.24	0.31	1.08	0.74
					MAX	0.31	0.39	2.12	1.32
	IV120LJ	1	2X	1	TYP	0.23	0.24	0.52	0.42
					MAX	0.31	0.39	1	0.62
	IV130LJ	1	3X	1.25	TYP	0.23	0.15	0.36	0.3
					MAX	0.33	0.34	0.66	0.37
	IV140LJ	1	4X	1.5	TYP	0.19	0.18	0.3	0.26
					MAX	0.32	0.33	0.48	0.36
	IV160LJ	1	6X	2	TYP	0.17	0.16	0.22	0.2
					MAX	0.29	0.3	0.34	0.28
	IV180LJ	1	8X	2.5	TYP	0.16	0.15	0.18	0.16
					MAX	0.27	0.27	0.28	0.24
3-STATE INVERTERS	IV211LJ	2	1X	1.25	TYP	0.33	0.34	2.06	1.22
					MAX	0.67	0.57	4.18	2.42
	IV212LJ	2	1X	1.25	TYP	0.33	0.34	2.08	1.22
					MAX	0.71	0.56	4.16	2.42
	IV221LJ	2	2X	2	TYP	0.36	0.35	1	0.6
					MAX	0.71	0.58	2.04	1.2
	IV222LJ	2	2X	2	TYP	0.36	0.34	1	0.6
					MAX	0.72	0.55	2.06	1.2
	IV241LJ	2	4X	3	TYP	0.34	0.31	0.17	0.4
					MAX	0.67	0.58	0.35	0.76
	IV242LJ	2	4X	3	TYP	0.36	0.3	0.5	0.32
					MAX	0.73	0.52	1.02	0.6

J-$\overline{K}$ FLIP-FLOPS AND LATCH BUS HOLDER

FUNCTION J-$\overline{K}$ FLIP-FLOPS HARDWIRED (f_{clock})	CELL NAME	OUTPUT DRIVE	EQUIV NA210 NAND GATES	SWITCHING CHARACTERISTICS C_L = 0 (CLK to Q)					TIMING RQMTS	
					DELAY TIME		DELTA DELAY		SETUP (min)	HOLD (min)
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)	t_{su} (ns)	t_h (ns)
127 MHz W/CLRZ AND PREZ	JKB20LJ (POS. EDGE CLOCK)	2X	9.5	TYP	1.78	1.74	0.58	0.5		
				MAX	3.86	3.69	1.16	0.97	3	0.25
125 MHz W/CLRZ AND PREZ	JKB21LJ (NEG. EDGE CLOCK)	2X	9.5	TYP	1.8	1.7	0.58	0.5		
				MAX	3.96	3.62	1.16	0.97	3	0.25

FUNCTION LATCH INTERNAL BUS HOLDER HARDWIRED	CELL NAME	OUTPUT DRIVE	EQUIV NA210 NAND GATES	ELECTRICAL CHARACTERISTICS			
					C_i (pF)	C_{pd} (pF)	
BUS HOLDER FOR 3-STATE BUS	LH110LJ	1X	1	TYP	0.56	0.17	When connected to a bus the $C_{i/O}$ of 0.56 pF becomes a part of the load driven.

LATCHES

FUNCTION LATCHES HARDWIRED	CELL NAME	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS C_L = 0 (CLK to Q) DELAY TIME t_{PLH} (ns)	 t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	 Δt_{PHL} (ns/pF)
$\overline{S}$-$\overline{R}$	LAB10LJ	1X	2.5	TYP	0.92	0.65	1.12	0.6
				MAX	1.82	1.23	2.1	1.08
$\overline{S}$-$\overline{R}$	LAB20LJ	2X	2.75	TYP	1.11	0.71	0.52	0.34
				MAX	2.22	1.32	1.02	0.68
D-TYPE HIGH ENABLE (C)	LAH10LJ	1X	3.75	TYP	0.58	0.64	1.06	0.56
				MAX	1.12	1.23	2.06	1.02
D-TYPE HIGH ENABLE (C)	LAH20LJ	2X	4	TYP	0.6	0.71	0.54	0.34
				MAX	1.2	1.36	1.06	0.66
D-TYPE HIGH ENABLE (C)	LAH23LJ	2X	6.5	TYP	0.78	0.77	0.55	0.49
				MAX	1.55	1.51	1.09	0.99
D-TYPE HIGH ENABLE (C)	LAH40LJ	4X	5.25	TYP	0.65	0.74	0.28	0.22
				MAX	1.32	1.43	0.53	0.45
D-TYPE LOW ENABLE (C)	LAL20LJ	2X	4.25	TYP	1.79	1.1	0.5	0.42
				MAX	3.99	2.38	0.96	0.86

FUNCTION LATCHES SOFTWARE	MACRO NAME	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS C_L = 0 (CLK to Q, See Note 1) DELAY TIME t_{PLH} (ns)	 t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	 Δt_{PHL} (ns/pF)
8-BIT ADDRESSABLE	S259LJ	2X	59.75	TYP	2.6	2.5	0.5	0.48
				MAX	4.6	4.5	1	0.9
8-BIT 3-S D-TYPE HIGH	S373LJ	1X	34.5	TYP	2	1.7	2.14	1.26
ENABLE (C)				MAX	3.3	3.2	4.38	2.56
4-BIT D-TYPE HIGH	S375LJ	2X	14	TYP	1.9	1.7	2.02	0.94
ENABLES (C)				MAX	3.1	2.7	4.08	1.82

NOTE 1: Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in the engineering workstation library.

MULTIPLEXERS

FUNCTION MULTIPLEXERS	CELL OR MACRO NAME	NO. OF INPUTS	OUTPUT DRIVE	EQUIV NA210 NAND GATES	SWITCHING CHARACTERISTICS C_L = 0				
						DELAY TIME		DELTA DELAY	
						t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
HARDWIRED	MU110LJ	2-to-1	1X	3.5	TYP	0.94	0.87	2	0.86
					MAX	1.88	1.66	4	1.7
	MU111LJ	2-to-1	1X	2.25	TYP	0.65	0.77	1.07	0.65
					MAX	1.23	1.67	2.1	1.2
	MU210LJ	4-to-1	1X	5	TYP	0.71	0.87	1.08	0.67
					MAX	1.86	2.28	2.08	1.24
	MU310LJ	8-to-1	1X	14.75	TYP	1.15	1.3	2.06	1.08
					MAX	3.16	3.63	4.12	2.18
	MU320LJ	8-to-1	2X	11.25	TYP	1.42	1.61	0.55	0.44
					MAX	4.59	5.24	1.1	0.84
SOFTWARE	S151LJ	8-to-1	1X	35	TYP	2.9	3.1	0.92	0.56
					MAX	5.7	6.1	1.76	1.02
	S153LJ	DUAL 4-to-1	1X	21.5	TYP	2.7	1.9	0.68	0.78
					MAX	4.8	3.6	1.34	1.62
	S157LJ	QUAD 2-to-1	1X	17	TYP	2.2	2.2	1.26	1
					MAX	3.9	3.7	2.46	1.98
	S158LJ	QUAD 2-to-1	1X	20	TYP	2.5	2.5	0.56	0.36
					MAX	4.2	4.6	1.06	0.64
	S251LJ	8-to-1	1X	24.5	TYP	3.5	3.6	2.14	1.26
					MAX	6.9	8.2	4.38	2.56
	S257ALJ	QUAD 2-to-1	1X	21	TYP	1.9	2.9	2.08	1.22
					MAX	2.8	3.7	4.16	2.42
	S258ALJ	QUAD 2-to-1	1X	15	TYP	1.9	2.9	2.08	1.22
					MAX	3.3	3.7	4.16	2.42
	S298LJ	QUAD 2-to-1	1X	37	TYP	1.8	2	1.06	0.78
					MAX	3.5	3.9	2.04	1.4
	S398LJ	QUAD 2-to-1	1X	39	TYP	1.8	1.7	1.12	2.12
					MAX	3.5	3.5	0.76	1.4
	S399LJ	QUAD 2-to-1	1X	36	TYP	1.4	1.6	1.06	0.78
					MAX	2.9	3.3	2.04	1.4

NAND GATES

FUNCTION GATES HARDWIRED	CELL NAME	NO. OF INPUTS	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS C_L = 0 DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
NAND	NA210LJ	2	1X	1	TYP	0.29	0.32	1.14	0.99
					MAX	0.44	0.46	2.46	1.98
	NA220LJ	2	2X	1.5	TYP	0.27	0.29	0.5	0.48
					MAX	0.4	0.45	1	0.9
	NA230LJ	2	3X	2	TYP	0.28	0.27	0.35	0.34
					MAX	0.43	0.42	0.7	0.62
	NA240LJ	2	4X	2.5	TYP	0.25	0.24	0.28	0.27
					MAX	0.42	0.44	0.48	0.44
	NA260LJ	2	6X	3.5	TYP	0.23	0.22	0.2	0.22
					MAX	0.4	0.43	0.32	0.3
	NA310LJ	3	1X	1.25	TYP	0.34	0.35	1.29	1.32
					MAX	0.61	0.63	3	2.74
	NA320LJ	3	2X	2	TYP	0.31	0.33	0.55	0.61
					MAX	0.51	0.55	1.14	1.28
	NA330LJ	3	3X	2.75	TYP	0.33	0.33	0.36	0.42
					MAX	0.52	0.55	0.74	0.84
	NA340LJ	3	4X	3.5	TYP	0.32	0.31	0.29	0.32
					MAX	0.53	0.54	0.58	0.64
	NA410LJ	4	1X	1.5	TYP	0.4	0.4	1.45	1.64
					MAX	0.73	0.85	3.64	3.46
	NA420LJ	4	2X	2.5	TYP	0.37	0.38	0.63	0.77
					MAX	0.64	0.74	1.34	1.62
	NA430LJ	4	3X	3.5	TYP	0.38	0.39	0.41	0.52
					MAX	0.66	0.75	0.94	1.1
	NA510LJ	5	1X	3	TYP	0.68	1.01	0.91	0.54
					MAX	1.4	2.12	1.76	1.02
	NA520LJ	5	2X	3.25	TYP	0.74	1.11	0.45	0.35
					MAX	1.49	2.39	0.88	0.68
	NA810LJ	8	1X	3.75	TYP	0.8	1.17	0.92	0.55
					MAX	1.63	2.54	1.76	1.02
	NA820LJ	8	2X	4	TYP	0.85	1.27	0.45	0.35
					MAX	1.71	2.8	0.9	0.7

NOR GATES

FUNCTION GATES HARDWIRED	CELL NAME	NO. OF INPUTS	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS C_L = 0 DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
NOR	NO210LJ	2	1X	1	TYP	0.29	0.37	2.07	1
					MAX	0.58	0.5	4.22	2.14
	NO220LJ	2	2X	1.5	TYP	0.28	0.34	0.98	0.46
					MAX	0.46	0.5	2.04	0.8
	NO230LJ	2	3X	2	TYP	0.28	0.3	0.66	0.37
					MAX	0.48	0.49	1.38	0.62
	NO240LJ	2	4X	2.5	TYP	0.29	0.27	0.49	0.3
					MAX	0.45	0.46	1.02	0.44
	NO310LJ	3	1X	1.25	TYP	0.38	0.43	3.07	1.29
					MAX	1.04	0.65	6.28	2.96
	NO320LJ	3	2X	2	TYP	0.36	0.41	1.47	0.61
					MAX	0.75	0.6	3.04	1.14
	NO330LJ	3	3X	2.75	TYP	0.36	0.38	1.01	0.42
					MAX	0.71	0.57	2.1	0.76
	NO410LJ	4	1X	1.5	TYP	0.52	0.49	4.1	1.51
					MAX	1.62	0.8	8.44	3.46
	NO420LJ	4	2X	2.5	TYP	0.47	0.47	2.02	0.78
					MAX	1.1	0.71	4.18	1.46
	NO510LJ	5	1X	3.5	TYP	0.96	0.89	1.01	0.56
					MAX	2.5	1.69	1.96	1.02
	NO520LJ	5	2X	3.75	TYP	1.05	0.97	0.5	0.33
					MAX	2.73	1.84	1	0.64
	NO810LJ	8	1X	3.75	TYP	1.29	0.99	1.01	0.55
					MAX	3.36	2	1.98	1.02
	NO820LJ	8	2X	4	TYP	1.39	1.05	0.51	0.33
					MAX	3.6	2.15	1.02	0.62

1/8-SPEED TOTEM-POLE OUTPUTS

FUNCTION OUTPUTS HARDWIRED	CELL NAME	OUTPUT CURRENT Sink/Source (mA)		SWITCHING CHARACTERISTICS† (C_L = 15 pF)			
				DELAY TIME		DELTA DELAY	
				t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
1/8-SPEED TOTEM-POLE OUTPUT	OPHA0LJ	16/16	TYP	5.76	6.13	50	50
			MAX	11.83	12.15	90	90
	OPHB0LJ	24/16	TYP	5.74	7.46	50	50
			MAX	11.79	14.33	90	80
	OPHE0LJ	48/16	TYP	5.92	6.72	40	30
			MAX	12.16	12.94	90	60
	OPHG0LJ	64/16	TYP	6.01	6.36	40	20
			MAX	12.33	12.28	80	50
	OPH00LJ	10/10	TYP	6.34	7.13	60	60
			MAX	12.96	14.01	110	120
	OPH20LJ	2/2	TYP	12.14	16.26	190	200
			MAX	24.18	31.11	360	200
	OPH40LJ	4/4	TYP	8.66	10.62	110	120
			MAX	17.39	20.47	210	210
	OPH60LJ	6/6	TYP	7.47	8.72	80	90
			MAX	15.12	16.93	160	160

† CMOS output delay times are shown.

1/8-SPEED OPEN-DRAIN OUTPUTS

FUNCTION OUTPUTS HARDWIRED	CELL NAME	OUTPUT SINK CURRENT (mA)	SWITCHING CHARACTERISTICS† (C_L = 15 pF)		
				DELAY	DELTA
				t_{PZL} (ns)	Δt_{PZL} (ps/pF)
1/8-SPEED OPEN-DRAIN OUTPUT	OPHA1LJ	16	TYP	5.89	50
			MAX	11.89	90
	OPHB1LJ	24	TYP	7.1	40
			MAX	14	80
	OPHE1LJ	48	TYP	6.82	30
			MAX	13.47	60
	OPHG1LJ	64	TYP	6.59	30
			MAX	13.05	50
	OPH01LJ	10	TYP	6.82	60
			MAX	13.69	120
	OPH21LJ	2	TYP	15.66	210
			MAX	31.73	380
	OPH41LJ	4	TYP	10.14	120
			MAX	20.21	220
	OPH61LJ	6	TYP	8.35	90
			MAX	16.67	160

† CMOS output delay times are shown.

1/8-SPEED 3-STATE OUTPUTS

FUNCTION OUTPUTS HARDWIRED	CELL NAME	OUTPUT CURRENT Sink/Source (mA)		SWITCHING CHARACTERISTICS† (C_L = 15 pF) DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ps/pF)	DELTA DELAY Δt_{PHL} (ps/pF)
1/8-SPEED 3-STATE OUTPUT	OPHA3LJ	16/16	TYP	6.84	7.32	40	50
			MAX	13.82	14.48	90	80
	OPHB3LJ	24/16	TYP	6.83	8.91	40	40
			MAX	13.81	17.28	90	80
	OPHE3LJ	48/16	TYP	6.91	8.26	40	30
			MAX	13.98	16.15	80	50
	OPHG3LJ	64/16	TYP	7	7.99	40	20
			MAX	14.15	15.72	80	40
	OPH03LJ	10/10	TYP	7.37	8.34	60	60
			MAX	14.81	16.34	110	110
	OPH23LJ	2/2	TYP	13.39	17.89	190	200
			MAX	26.48	34.41	350	360
	OPH43LJ	4/4	TYP	9.71	11.95	110	120
			MAX	19.29	23.07	200	210
	OPH63LJ	6/6	TYP	8.49	9.98	80	90
			MAX	16.99	19.37	150	160

† CMOS output delay times are shown.

FULL-SPEED TOTEM-POLE OUTPUTS

FUNCTION OUTPUTS HARDWIRED	CELL NAME	OUTPUT CURRENT Sink/Source (mA)		SWITCHING CHARACTERISTICS† (C_L = 15 pF)			
				DELAY TIME		DELTA DELAY	
				t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
FULL-SPEED TOTEM-POLE OUTPUT	OPIA0LJ	16/16	TYP	1.52	1.54	20	20
			MAX	2.77	2.95	40	40
	OPIB0LJ	24/16	TYP	1.56	1.33	20	20
			MAX	2.84	2.55	40	30
	OPIE0LJ	48/16	TYP	1.68	1	20	10
			MAX	3.07	1.94	40	20
	OPIG0LJ	64/16	TYP	1.71	0.88	20	10
			MAX	3.13	1.71	40	20
	OPI00LJ	10/10	TYP	1.84	1.87	30	30
			MAX	3.42	3.58	70	60
	OPI20LJ	2/2	TYP	4.94	5.25	170	150
			MAX	9.44	10.01	320	230
	OPI40LJ	4/4	TYP	3.01	3.18	80	80
			MAX	5.71	6.06	160	130
	OPI60LJ	6/6	TYP	2.39	2.46	60	50
			MAX	4.52	4.7	110	90

† CMOS output delay times are shown.

FULL-SPEED OPEN-DRAIN OUTPUTS

FUNCTION OUTPUTS HARDWIRED	CELL NAME	OUTPUT SINK CURRENT (mA)	SWITCHING CHARACTERISTICS† (C_L = 15 pF)		
				DELAY	DELTA
				t_{PZL} (ns)	Δt_{PZL} (ps/pF)
FULL-SPEED OPEN-DRAIN OUTPUT	OPIA1LJ	16	TYP	1.29	20
			MAX	2.49	40
	OPIB1LJ	24	TYP	1.08	20
			MAX	2.09	30
	OPIE1LJ	48	TYP	0.82	10
			MAX	1.6	20
	OPIG1LJ	64	TYP	0.75	10
			MAX	1.46	20
	OPI01LJ	10	TYP	1.65	30
			MAX	3.2	60
	OPI21LJ	2	TYP	5	160
			MAX	9.94	300
	OPI41LJ	4	TYP	2.93	80
			MAX	5.69	140
	OPI61LJ	6	TYP	2.23	50
			MAX	4.31	100

† CMOS output delay times are shown.

FULL-SPEED 3-STATE OUTPUTS

FUNCTION OUTPUTS HARDWIRED	CELL NAME	OUTPUT CURRENT Sink/Source (mA)		SWITCHING CHARACTERISTICS† (C_L = 15 pF)			
				DELAY TIME		DELTA DELAY	
				t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
FULL-SPEED 3-STATE OUTPUT	OPIA3LJ	16/16	TYP	2.56	2.31	20	20
			MAX	5.25	4.63	40	40
	OPIB3LJ	24/16	TYP	2.65	2.16	20	20
			MAX	5.37	4.39	40	30
	OPIE3LJ	48/16	TYP	3.03	2	20	10
			MAX	6.14	4.19	40	20
	OPIG3LJ	64/16	TYP	3.34	2.01	20	10
			MAX	6.82	4.22	30	20
	OPI03LJ	10/10	TYP	2.71	2.62	30	30
			MAX	5.46	5.23	70	60
	OPI23LJ	2/2	TYP	5.87	6.25	170	150
			MAX	11.47	12.09	320	260
	OPI43LJ	4/4	TYP	3.79	3.98	80	80
			MAX	7.47	7.77	160	130
	OPI63LJ	6/6	TYP	3.18	3.22	60	50
			MAX	6.34	6.33	110	90

† CMOS output delay times are shown.

D3030, APRIL 1989

1/2-SPEED TOTEM-POLE OUTPUTS

FUNCTION OUTPUTS HARDWIRED	CELL NAME	OUTPUT CURRENT Sink/Source (mA)		SWITCHING CHARACTERISTICS† (C_L = 15 pF)			
				DELAY TIME		DELTA DELAY	
				t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
1/2-SPEED TOTEM-POLE OUTPUT	OPJA0LJ	16/16	TYP	3.12	3.04	30	30
			MAX	6.29	6.08	60	60
	OPJB0LJ	24/16	TYP	3.11	3.35	30	30
			MAX	6.28	6.68	60	50
	OPJE0LJ	48/16	TYP	3.24	3.02	30	20
			MAX	6.52	6.1	60	30
	OPJG0LJ	64/16	TYP	3.28	2.88	30	20
			MAX	6.61	5.86	60	30
	OPJ00LJ	10/10	TYP	3.47	3.61	40	40
			MAX	6.94	7.13	80	80
	OPJ20LJ	2/2	TYP	7.3	9.03	170	160
			MAX	14.3	17.22	320	230
	OPJ40LJ	4/4	TYP	4.95	5.7	90	90
			MAX	9.74	10.99	170	160
	OPJ60LJ	6/6	TYP	4.17	4.57	60	60
			MAX	8.27	8.89	120	110

† CMOS output delay times are shown.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

1/2-SPEED OPEN-DRAIN OUTPUTS

FUNCTION OUTPUTS HARDWIRED	CELL NAME	OUTPUT SINK CURRENT (mA)	SWITCHING CHARACTERISTICS† (C_L = 15 pF)		
				DELAY	DELTA
				t_{PZL} (ns)	Δt_{PZL} (ps/pF)
1/2-SPEED OPEN-DRAIN OUTPUT	OPJA1LJ	16	TYP	2.84	30
			MAX	5.77	60
	OPJB1LJ	24	TYP	3.05	30
			MAX	6.2	50
	OPJE1LJ	48	TYP	2.94	20
			MAX	6.05	40
	OPJG1LJ	64	TYP	2.89	20
			MAX	5.99	30
	OPJ01LJ	10	TYP	3.37	40
			MAX	6.76	80
	OPJ21LJ	2	TYP	8.49	170
			MAX	16.92	320
	OPJ41LJ	4	TYP	5.31	90
			MAX	10.49	160
	OPJ61LJ	6	TYP	4.25	60
			MAX	8.44	120

† CMOS output delay times are shown.

1/2-SPEED 3-STATE OUTPUTS

FUNCTION OUTPUTS HARDWIRED	CELL NAME	OUTPUT CURRENT Sink/Source (mA)	SWITCHING CHARACTERISTICS† (C_L = 15 pF)				
				DELAY TIME		DELTA DELAY	
				t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
1/2-SPEED 3-STATE OUTPUT	OPJA3LJ	16/16	TYP	4.17	3.96	30	30
			MAX	8.45	7.96	60	60
	OPJB3LJ	24/16	TYP	4.17	4.38	30	30
			MAX	8.46	8.79	60	50
	OPJE3LJ	48/16	TYP	4.24	4.19	30	20
			MAX	8.6	8.55	60	30
	OPJG3LJ	64/16	TYP	4.3	4.16	30	20
			MAX	8.72	8.55	60	30
	OPJ03LJ	10/10	TYP	4.39	4.53	40	40
			MAX	8.84	8.98	80	80
	OPJ23LJ	2/2	TYP	8.33	10.19	170	160
			MAX	16.39	19.55	320	280
	OPJ43LJ	4/4	TYP	5.81	6.68	90	90
			MAX	11.52	12.94	170	150
	OPJ63LJ	6/6	TYP	5.04	5.48	60	60
			MAX	10.07	10.72	130	110

† CMOS output delay times are shown.

1/4-SPEED TOTEM-POLE OUTPUTS

FUNCTION OUTPUTS HARDWIRED	CELL NAME	OUTPUT CURRENT Sink/Source (mA)		SWITCHING CHARACTERISTICS† (C_L = 15 pF)			
				DELAY TIME		DELTA DELAY	
				t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
1/4-SPEED TOTEM-POLE OUTPUT	OPKA0LJ	16/16	TYP	4.44	4.51	40	40
			MAX	9.07	9.01	70	70
	OPKB0LJ	24/16	TYP	4.43	5.27	40	40
			MAX	9.04	10.33	70	70
	OPKE0LJ	48/16	TYP	4.58	4.74	40	20
			MAX	9.36	9.36	70	40
	OPKG0LJ	64/16	TYP	4.65	4.51	40	20
			MAX	9.48	8.94	70	40
	OPK00LJ	10/10	TYP	4.91	5.3	50	50
			MAX	9.95	10.46	100	100
	OPK20LJ	2/2	TYP	9.73	12.64	180	180
			MAX	19.24	24.19	340	230
	OPK40LJ	4/4	TYP	6.81	8.12	100	100
			MAX	13.58	15.66	190	180
	OPK60LJ	6/6	TYP	5.83	6.59	70	80
			MAX	11.72	12.84	140	140

† CMOS output delay times are shown.

1/4-SPEED OPEN-DRAIN OUTPUTS

FUNCTION OUTPUTS HARDWIRED	CELL NAME	OUTPUT SINK CURRENT (mA)	SWITCHING CHARACTERISTICS† (C_L = 15 pF)		
				DELAY	DELTA
				t_{PZL} (ns)	Δt_{PZL} (ps/pF)
1/4-SPEED OPEN-DRAIN OUTPUT	OPKA1LJ	16	TYP	4.27	40
			MAX	8.67	70
	OPKB1LJ	24	TYP	4.88	40
			MAX	9.8	70
	OPKE1LJ	48	TYP	4.71	30
			MAX	9.48	50
	OPKG1LJ	64	TYP	4.61	20
			MAX	9.3	40
	OPK01LJ	10	TYP	5	50
			MAX	10.07	100
	OPK21LJ	2	TYP	4.48	190
			MAX	8.78	350
	OPK41LJ	4	TYP	7.64	100
			MAX	15.2	190
	OPK61LJ	6	TYP	6.21	80
			MAX	12.4	140

† CMOS output delay times are shown.

1/4-SPEED 3-STATE OUTPUTS

FUNCTION OUTPUTS HARDWIRED	CELL NAME	OUTPUT CURRENT Sink/Source (mA)		SWITCHING CHARACTERISTICS† (C_L = 15 pF) DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ps/pF)	DELTA DELAY Δt_{PHL} (ps/pF)
1/4-SPEED 3-STATE OUTPUT	OPKA3LJ	16/16	TYP	5.5	5.54	40	40
			MAX	11.18	11.06	70	70
	OPKB3LJ	24/16	TYP	5.5	6.46	40	40
			MAX	11.14	12.75	70	70
	OPKE3LJ	48/16	TYP	5.57	6.05	40	20
			MAX	11.3	12.1	70	40
	OPKG3LJ	64/16	TYP	5.64	5.94	40	20
			MAX	11.44	11.93	70	40
	OPK03LJ	10/10	TYP	5.88	6.34	50	50
			MAX	11.87	12.52	90	90
	OPK23LJ	2/2	TYP	10.87	14.01	180	180
			MAX	22.44	26.93	330	320
	OPK43LJ	4/4	TYP	7.77	9.26	100	100
			MAX	15.42	17.9	180	180
	OPK63LJ	6/6	TYP	6.77	7.65	70	70
			MAX	13.56	14.91	130	130

† CMOS output delay times are shown.

D3030, APRIL 1989

OR GATES

FUNCTION GATES HARDWIRED	CELL NAME	NO. OF INPUTS	OUTPUT DRIVE	EQUIV NA210 NAND GATES	SWITCHING CHARACTERISTICS C_L = 0				
								DELTA DELAY	
						t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
OR	OR210LJ	2	1X	1.25	TYP	0.49	0.65	1.09	0.63
					MAX	0.88	1.34	2.12	1.16
	OR220LJ	2	2X	1.5	TYP	0.58	0.76	0.53	0.38
					MAX	1.06	1.63	1.04	0.76
	OR240LJ	2	4X	2.5	TYP	0.55	0.67	0.27	0.25
					MAX	0.96	1.39	0.54	0.48
	OR260LJ	2	6X	3.75	TYP	0.55	0.68	0.18	0.17
					MAX	0.95	1.41	0.36	0.32
	OR310LJ	3	1X	1.5	TYP	0.61	0.87	1.09	0.71
					MAX	1.09	2.06	2.14	1.32
	OR320LJ	3	2X	1.75	TYP	0.71	1.02	0.53	0.46
					MAX	1.31	2.47	1.04	0.92
	OR340LJ	3	4X	3	TYP	0.68	0.91	0.28	0.27
					MAX	1.19	2.06	0.54	0.58
	OR360LJ	3	6X	4.5	TYP	0.65	0.89	0.2	0.22
					MAX	1.12	1.97	0.38	0.44
	OR410LJ	4	1X	1.75	TYP	0.71	1.05	1.1	0.8
					MAX	1.28	2.77	2.18	1.5
	OR420LJ	4	2X	2.25	TYP	0.85	1.26	0.54	0.52
					MAX	1.63	3.34	1.1	1.02
	OR440LJ	4	4X	3.5	TYP	0.79	1.16	0.28	0.31
					MAX	1.39	2.74	0.58	0.64
	OR460LJ	4	6X	5.25	TYP	0.79	1.16	0.18	0.24
					MAX	1.35	2.84	0.42	0.5
	OR510LJ	5	1X	3.75	TYP	0.58	0.84	1.73	0.96
					MAX	1.09	2.26	2.2	1.98
	OR810LJ	8	1X	3.75	TYP	0.65	1.19	1.06	1.02
					MAX	1.3	3.14	2.11	2.11

OR-AND GATES, OR-NAND GATES, AND OSCILLATORS

FUNCTION GATES HARDWIRED	CELL NAME	NO. OF INPUTS	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS C_L = 0 DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)
OR-AND	OA220LJ	4	1X	2.25	TYP	0.54	0.95	1.1	0.85
	$Y = (A1+A2)\cdot(B1+B2)$				MAX	1.1	2.18	2.13	1.58
	OA230LJ	6	1X	3	TYP	0.83	1.15	1.1	0.93
	$Y = (A1+A2)\cdot(B1+B2)\cdot(C1+C2)$				MAX	1.92	2.89	2.13	1.79
OR-NAND	OA231LJ	6	1X	3.25	TYP	1.18	1.05	1.09	0.74
	$Y = \overline{(A1+A2)\cdot(B1+B2)\cdot(C1+C2)}$				MAX	2.91	2.27	2.11	1.32
OR-AND	OA240LJ	8	1X	3.75	TYP	1.2	1.38	1.11	1.01
	$Y = (A1+A2)\cdot(B1+B2)\cdot(C1+C2)\cdot(D1+D2)$				MAX	2.84	3.59	2.18	2.01
OR-NAND	OA241LJ	8	1X	4	TYP	1.36	1.4	1.1	0.74
	$Y = \overline{(A1+A2)\cdot(B1+B2)\cdot(C1+C2)\cdot(D1+D2)}$				MAX	3.58	3.25	2.12	1.32
OR-AND	OA320LJ	6	1X	2.5	TYP	0.59	1.28	1.1	0.97
	$Y = (A1+A2+A3)\cdot(B1+B2+B3)$				MAX	1.29	3.22	2.16	1.98

FUNCTION OSCILLATORS HARDWIRED	CELL NAME	FREQUENCY RANGE (MHz)	OUTPUT DRIVE		SWITCHING CHARACTERISTICS† (C_L = 15 pF) DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ps/pF)	DELTA DELAY Δt_{PHL} (ps/pF)
THIRD OVERTONE	OSI01LJ	55 to 75	8X	TYP	2.3	1.9	50	40
				MAX	3.3	2.9	90	70
THIRD OVERTONE	OSI02LJ	35 to 55	4X	TYP	3.2	2.7	110	80
				MAX	4.8	4.1	190	150
THIRD OVERTONE	OSI03LJ	20 to 35	2X	TYP	5.2	4.3	220	170
				MAX	8.3	6.9	370	300
FUNDAMENTAL	OSI04LJ (CMOS input)	1 to 20	1X	TYP	9.3	7.5	440	340
				MAX	15.3	12.6	750	590
FUNDAMENTAL	OSI24LJ (TTL input)	1 to 20	1X	TYP	14.01	9.92	740	480
				MAX	29.19	17.01	1410	840

† CMOS output delay times are shown.

REGISTERS

FUNCTION REGISTERS/ FLIP-FLOPS/ RIPPLE COUNTER HARDWIRED	CELL NAME	f_{clock}	OUTPUT DRIVE	EQUIV NA210 NAND GATES	SWITCHING CHARACTERISTICS C_L = 0 (CLK to Q OUT)					TIMING RQMTS	
						DELAY TIME		DELTA DELAY		SETUP (MIN)	HOLD (MIN)
						t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)	t_{su} (ns)	t_h (ns)
4-BIT WITH SERIN	R2401LJ	175 MHz	1X	23.5	TYP	1.51	1.64	0.62	0.42	2	0
					MAX	2.97	3.31	1.22	0.78		
4-BIT WITH SERIN	R2402LJ	175 MHz	1X	25.5	TYP	1.83	1.71	1.02	1.2	2	0
					MAX	3.71	3.46	1.98	2.38		
4-BIT WITH SERIN AND PARALLEL	R2403LJ	170 MHz	1X	29.5	TYP	1.38	1.6	0.6	0.42	2	0
					MAX	2.69	3.22	1.16	0.76		
4-BIT WITH SERIN AND PARALLEL	R2404LJ	170 MHz	1X	31.5	TYP	1.78	1.68	1.02	1.22	2	0
					MAX	3.6	3.37	1.96	2.34		
4-BIT WITH CLRZ	R2405LJ	150 MHz	1X	20.5	TYP	1.45	1.62	1.06	0.78	2	0
					MAX	2.88	3.31	2.04	1.4		
4-BIT WITH CLRZ AND COMP. OUT.	R2406LJ	150 MHz	1X	23.5	TYP	1.76	1.76	1.12	0.76	2	0
					MAX	3.54	3.51	2.12	1.4		
4-BIT WITH CLRZ	R2407LJ	150 MHz	1X	24.5	TYP	1.59	1.72	2.14	1.33	2	0
					MAX	3.22	3.57	4.27	2.54		
4-BIT RIPPLE COUNTER	R2408LJ	185 MHz	1X	23.5	TYP	4.34	4.05	0.62	0.46	0	–
					MAX	9.49	8.89	1.24	0.88		

REGISTER FILES

FUNCTION	CELL NAME	ORGANIZATION (W X B)	OUTPUT DRIVE	EQUIV NA210 NAND GATES AREA		ACCESS/CYCLE TIME CHARACTERISTICS				TIMING RQMTS	
						WRITE CYCLE	ADDR. ACCESS	ENABLE ACCESS	DELTA DELAY	WRITE SETUP (MIN)	WRITE HOLD (MIN)
REGISTER FILES HARD-WIRED						$t_{c(W)}$ (MIN)	$t_{a(A)}$ (ns)	$t_{en(G)}$ (ns)	$\Delta t_{a(A)}$ (ns/pF)	t_{su} (ns)	t_h (ns)
3-PORT: 1 WRITE, 2 READ	RF400LJ	16 × 8	1X	710	TYP		5.2	1.3	0.6		
					MAX	9	10.7	2.9	1.2	5	0
	RF402LJ	16 × 9	1X	781	TYP		5.2	1.3	0.6		
					MAX	9	10.9	2.9	1.2	5	0
	RF403LJ	16 × 12	2X	930	TYP		6.6	1.7	0.4		
					MAX	12.1	13.6	3.8	0.9	5	0
	RF600LJ	64 × 8	1X	3516	TYP		5.5	1.6	0.7		
					MAX	8	12.3	3.5	1.3	4	0
	RF602LJ	64 × 9	1X	3844	TYP		5.6	1.6	0.7		
					MAX	8	12.5	3.5	1.3	4	0
4-PORT: 2 WRITE, 2 READ	RF401LJ	16 × 8	1X	985	TYP		5.2	1.3	0.6		
					MAX	10	11	2.9	1.3	6	0
	RF601LJ	64 × 8	1X	5007	TYP		5.5	1.6	0.7		
					MAX	8	12.5	3.5	1.3	4	0

D3030, APRIL 1989

STATIC RANDOM ACCESS MEMORIES

FUNCTION					ACCESS/CYCLE TIME CHARACTERISTICS				TIMING RQMTS	
					WRITE CYCLE	ADDR. ACCESS	ENABLE ACCESS	DELTA DELAY	DATA SETUP (MIN)	ADDR. HOLD (MIN)
RAMS (ORGANIZATION)	MACRO NAME (MUX-FACTOR)	OUT-PUT DRIVE	EQUIV NA210 NAND GATES (AREA)		$t_{c(W)}$ (ns)	$t_{a(A)}$ (ns)	$t_{a(E)}$ (ns)	$\Delta t_{a(A)}$ (ns/pF)	$t_{su(D)}$ (ns)	$t_{h(WA)}$ (ns)
64W × 4B	RH000LJ	1X	3866†	TYP		7.6	7.6	1		
	(2:1)			MAX	30	18.2	18.2	2.1	10	5
64W × 8B	RH001LJ	1X	3866	TYP		7.7	7.7	1		
	(2:1)			MAX	30	18.3	18.3	2.1	10	5
128W × 4B	RH002LJ	1X	5855†	TYP		8.2	8.2	1		
	(2:1)			MAX	30	19.4	19.4	2.1	10	5
128W × 8B	RH003LJ	1X	5855	TYP		8.3	8.3	1		
	(2:1)			MAX	30	19.5	19.5	2.1	10	5
256W × 4B	RH004LJ	1X	9834†	TYP		9.3	9.3	1		
	(2:1)			MAX	30	21.8	21.8	2.1	10	5
256W × 8B	RH005LJ	1X	9834	TYP		9.4	9.4	1		
	(2:1)			MAX	30	21.9	21.9	2.1	10	5
512W × 4B	RH006LJ	1X	6526†	TYP		9.2	9.2	1		
	(8:1)			MAX	30	21.5	21.5	2.1	10	5
512W × 8B	RH007LJ	1X	6526	TYP		9.5	9.5	1		
	(8:1)			MAX	30	22	22	2.1	10	5
1024W × 4B	RH008LJ	1X	5564	TYP		10.4	10.4	1		
	(8:1)			MAX	32	23.9	23.9	2.1	10	5
1024W × 8B	RH009LJ	1X	8209	TYP		10.8	10.8	1		
	(8:1)			MAX	32	24.4	24.4	2.1	10	5
2048W × 4B	RH010LJ	1X	12114†	TYP		11.9	11.9	1		
	(16:1)			MAX	35	26.7	26.7	2.1	10	5
2048W × 8B	RH011LJ	1X	12114	TYP		12.6	12.6	1		
	(16:1)			MAX	36	27.7	27.7	2.1	10	5

† Overall area is determined by factors other than bit density.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SHIFT REGISTERS

FUNCTION SHIFT REGISTERS SOFTWARE	MACRO NAME	LENGTH	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS (See Note 1)			
						DELAY TIME		DELTA DELAY	
						t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
SIPO WITH CLRZ	S164LJ	8-BITS	2X	50.75	TYP	1.5	1.6	0.62	0.42
					MAX	3	3.3	1.22	0.78
PISO WITH CLKINH	S165ALJ	8-BITS	1X	85.5	TYP	2.7	2.1	0.56	0.36
					MAX	5.8	4.4	1.1	0.7
PISO WITH CLRZ	S166LJ	8-BITS	1X	66.5	TYP	2.3	2.5	1.06	0.78
					MAX	4.6	5	2.04	1.4
PIPO BIDIRECT. WITH CLRZ	S194ALJ	4-BITS	1X	52.75	TYP	1.6	1.7	1.06	0.78
					MAX	3.2	3.5	2.04	1.4
PIPO WITH CLRZ	S195ALJ	4-BITS	1X	41.5	TYP	1.8	1.7	1.12	0.76
					MAX	3.5	3.5	2.12	1.4
PIPO BIDIRECT. WITH CLRZ	S299LJ	8-BITS	1X	127	TYP	2.3	2.4	1	0.6
					MAX	4.6	4.7	2.06	1.2
PIPO BIDIRECT. WITH CLRZ	S299XLJ	8-BITS	1X	101.25	TYP	1.6	1.7	1.06	0.78
					MAX	3.2	3.5	2.04	1.4
SIPO 3-STATE WITH CLRZ	S595LJ	8-BITS	1X	99.5	TYP	1.6	1.7	2.14	1.33
					MAX	3.2	3.6	4.27	2.54
SIPO WITH CLRZ	S598XLJ	8-BITS	1X	160.25	TYP	3.1	3.7	2.08	1.22
					MAX	6.4	7.6	4.16	2.42
PIPO BIDIRECT.	S651LJ	8-BITS	1X	172.5	TYP	3.5	3.2	1	0.6
					MAX	6.5	6.1	2.06	1.2
PIPO BIDIRECT.	S652LJ	8-BITS	1X	196.5	TYP	3.5	3.6	1	0.6
					MAX	6.7	6.7	2.06	1.2

NOTE 1: Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in the engineering workstation library.

D3030, APRIL 1989

TOGGLE FLIP-FLOPS, SCAN FLIP-FLOPS, AND LATCHES

FUNCTION TOGGLE FLIP-FLOPS HARDWIRED (f_{clock})	CELL NAME	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS C_L = 0 (CLK TO Q OUT)			
					DELAY TIME		DELTA DELAY	
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
145 MHz WITH CLRZ AND PREZ	TAB20LJ	2X	7.5	TYP	2.03	1.34	0.56	0.38
				MAX	4.43	2.94	1.12	0.7
165 MHz WITH CLRZ	TAC20LJ	2X	6.75	TYP	1.96	1.2	0.54	0.36
				MAX	4.24	2.52	1.1	0.7
165 MHz WITH PREZ	TAP20LJ	2X	6.5	TYP	1.87	1.31	0.56	0.36
				MAX	4.11	2.81	1.08	0.7

FUNCTION SCAN FLIP-FLOPS AND LATCHES HARDWIRED (f_{clock})	CELL NAME	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS (CLK to Q OUT)				TIMING RQMTS	
					DELAY TIME		DELTA DELAY		SETUP (MIN)	HOLD (MIN)
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)	t_{su} (ns)	t_h (ns)
76 MHz	TDB10LJ	1X	7	TYP	0.87	1.12	1.12	1.12	4	0
				MAX	1.73	2.32	2.2	2.35		
135 MHz WITH CLRZ	TDC10LJ	1X	7.75	TYP	1.31	1.54	1.31	0.85		
				MAX	2.6	3.12	2.54	1.58	12	0
100 MHz WITH CLRZ	TDC11LJ	1X	4.25	TYP	1.56	1.9	1.09	0.72		
				MAX	3.41	3.99	2.09	1.29	3	0
155 MHz	TDN10LJ	1X	7.25	TYP	1.46	1.34	1.13	1.17		
				MAX	2.93	2.65	2.18	2.13	3	0
111 MHz	TDN11LJ	1X	4	TYP	1.19	1.63	1.09	0.74		
				MAX	2.68	3.31	2.1	1.32	3	0
100 MHz	TDD12LJ	1X	3.75	TYP	1.4	1.86	1.09	0.72		
				MAX	3.08	3.9	2.09	1.28	3	0
100 MHz	TDN13LJ	1X	6	TYP	1.32	1.93	1.09	0.98		
				MAX	2.67	4.26	2.12	1.98	3	0
83 MHz	TDN22LJ	2X	6	TYP	1.56	1.94	0.53	0.35		
				MAX	3.39	4.19	1.04	0.62	3	0

POWER-UP CLEAR, PULL-UP, PULL-DOWN TERMINATORS, AND HI/LO

FUNCTION POWER-UP CLEAR CELL HARDWIRED	CELL NAME	OUTPUT DRIVE	EQUIV NA210 GATES	CHARACTERISTICS	
				ELECTRICAL	SWITCHING
OPERATES FROM V_{CC}	PUC00LJ	1X	14.75	POWERED DIRECTLY BY V_{CC}	MIN OUTPUT PULSE WIDTH = 30 ns AT V_{CC} RISE TIME = 50 ns

FUNCTION TERMINATORS HARDWIRED	CELL NAME	EQUIVALENT NA210s	TYPE OF TERMINATION	TYPICAL CURRENT (μA)
FOR 3-STATE I/Os AND INPUTS	PD095LJ	2.5	PULL-DOWN	95
	PR005LJ	4.25	PULL-UP	−5
	PR095LJ	4	PULL-UP	−95
	PR250LJ	3	PULL-UP	−250
	PR400LJ	3	PULL-UP	−400

FUNCTION TIEOFF FOR UNUSED INPUTS HARDWIRED	CELL NAME	OUTPUT DRIVE	EQUIV NA210 NAND GATES		SWITCHING CHARACTERISTICS			
					DELAY TIME		DELTA DELAY	
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
HI/LO WITH ESD PROTECTION	TO010LJ	1X	2	TYP	N/A	N/A	N/A	N/A
				MAX	N/A	N/A	N/A	N/A

TEST-PORT CONTROLLERS

FUNCTION PARALLEL MegaModule™ TEST-PORT CONTROLLERS HARDWIRED (f_{clock})	CELL NAME	OUTPUT DRIVE	EQUIV NA210 NAND GATES	SWITCHING CHARACTERISTICS C_L = 0 (CLK TO Q OUT)					TIMING RQMTS	
					DELAY TIME		DELTA DELAY		SETUP (MIN)	HOLD (MIN)
					t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)	t_{su} (ns)	t_h (ns)
123 MHz	TP000LJ	1X	3.75	TYP	1.24	0.95	3.11	1.23		
PORT CONT.				MAX	2.48	2.08	6.27	2.22	2.5	0
GLOBAL EN	TP006LJ	4X	6.25	TYP	1.33	1.49	0.69	0.54	N/A	
CK CONT.				MAX	2.65	3.07	1.43	1.06		
TEST OUTPUT	TP008LJ	4X	3.5	TYP	0.33	0.33	0.37	0.34	N/A	
				MAX	0.55	0.57	0.74	0.61		
INPUT BUFFER	TP009LJ	4X	4	TYP	0.47	0.46	0.59	0.45	N/A	
				MAX	0.79	0.71	1.2	0.86		
OUTPUT	TP010LJ	4X	2.5	TYP	0.23	0.22	0.29	0.25	N/A	
BUFFER				MAX	0.38	0.41	0.47	0.32		

MegaModule is a trademark of Texas Instruments Incorporated.

6 Special Functions

D3030, JANUARY 1989

INPUT AND OUTPUT TERMINATORS/POWER-UP CLEAR/UNUSED-INPUT TIE-OFF

DESCRIPTION	CELL NAME	OUTPUT DRIVE	COMMENTS	EQUIVALENT NA210s	PAGE
Clock Generator	CK120LJ	1X	2-phase, nonoverlap clock generator for use with TDN latches	5	6-10
Terminator	PD095LJ	–	95-µA pull-down	0	6-3
Terminator	PR005LJ	–	5-µA pull-up	0	6-4
Terminator	PR095LJ	–	95-µA pull-up	0	6-5
Terminator	PR250LJ	–	250-µA pull-up	0	6-6
Terminator	PR400LJ	–	400-µA pull-up	0	6-7
Power-Up Clear One-Shot	PUC00LJ	–	Positive-edge triggered	0	6-8
Tie-Off Gate	TO010LJ	1X	H- and L-logic level tie-off for unused inputs	2	6-9

PD095LJ
95-μA PULL-DOWN ACTIVE TERMINATOR

D3030, DECEMBER 1988

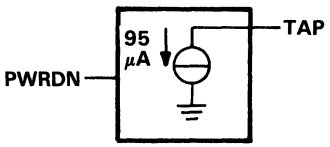
INTERNAL CELL

description

The PD095LJ is a dedicated standard-cell pull-down terminator that can be incorporated into an ASIC design on input, output, or I/O cells. The connection is made at the input, output, or I/O node. The terminator is used to ensure that the input, output, or I/O will be driven to a low logic level, thereby avoiding exposure to a high-impedance or floating condition. The terminator is ESD and latch-up protected by the input, output, or I/O cell. When the terminator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: PD095LJ (input,output,or I/O node name);

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), PWRDN = L‡

PARAMETER	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
I_O Output current	V_O = 1 V	21	47	94	23	47	88	μA
	V_O = 2.5 V	36	87	182	39	87	170	
	V_O = 4.5 V	35	95	208	38	95	195	

‡ When PWRDN = H, the current source is turned off.
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

PR005LJ
5-μA PULL-UP ACTIVE TERMINATOR

D3030, DECEMBER 1988

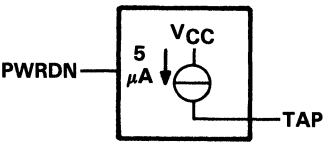
INTERNAL CELL

description

The PR005LJ is a dedicated standard-cell pull-up terminator that can be incorporated into an ASIC design on input, output, or I/O cells. The connection is made at the input, output, or I/O node. The terminator is used to ensure that the input, output, or I/O will be driven to a high logic level, thereby avoiding exposure to a high-impedance or floating condition. The terminator is ESD and latch-up protected by the input, output, or I/O cell. When the terminator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: PR005LJ (input,output,or I/O node name);

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), PWRDN = L‡

PARAMETER	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
I_O Output current	V_O = 4 V	0.52	2.46	6.18	0.56	2.46	5.83	μA
	V_O = 2.5 V	1.7	4.62	9.78	1.88	4.62	9.24	
	V_O = 0	1.9	4.97	10.5	2	4.97	9.92	

‡ When PWRDN = H, the current source is turned off.
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PR095LJ
95-μA PULL-UP ACTIVE TERMINATOR

D3030, DECEMBER 1988

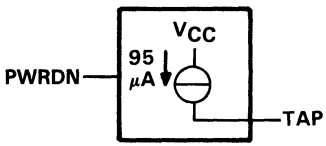
INTERNAL CELL

description

The PR095LJ is a dedicated standard-cell pull-up terminator that can be incorporated into an ASIC design on input, output, or I/O cells. The connection is made at the input, output, or I/O node. The terminator is used to ensure that the input, output, or I/O will be driven to a high logic level, thereby avoiding exposure to a high-impedance or floating condition. The terminator is ESD and latch-up protected by the input, output, or I/O cell. When the terminator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: PR095LJ (input,output,or I/O node name);

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), PWRDN = L‡

PARAMETER	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
I_O Output current	V_O = 4 V	10	47	115	11	47	109	μA
	V_O = 2.5 V	36	88	179	38	88	169	
	V_O = 0	40	95	192	42	95	182	

‡ When PWRDN = H, the current source is turned off.

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

PR250LJ
250-μA PULL-UP ACTIVE TERMINATOR

D3030, DECEMBER 1988

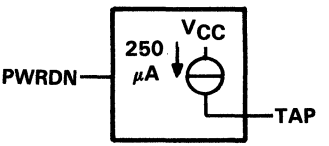
INTERNAL CELL

description

The PR250LJ is a dedicated standard-cell pull-up terminator that can be incorporated into an ASIC design on input, output, or I/O cells. The connection is made at the input, output, or I/O node. The terminator is used to ensure that the input, output, or I/O will be driven to a high logic level, thereby avoiding exposure to a high-impedance or floating condition. The terminator is ESD and latch-up protected by the input, output, or I/O cell. When the terminator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: PR250LJ (input,output,or I/O node name);

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), PWRDN = L‡

PARAMETER	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
I_O Output current	V_O = 4 V	21	96	235	23	96	222	μA
	V_O = 2.5 V	73	179	366	78	179	346	
	V_O = 0	83	197	398	88	197	377	

‡ When PWRDN = H, the current source is turned off.
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

PR400LJ
400-μA PULL-UP ACTIVE TERMINATOR

D3030, DECEMBER 1988

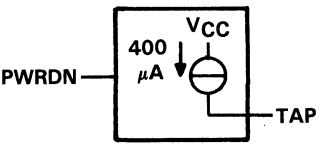
INTERNAL CELL

description

The PR400LJ is a dedicated standard-cell pull-up terminator that can be incorporated into an ASIC design on input, output, or I/O cells. The connection is made at the input, output, or I/O node. The terminator is used to ensure that the input, output, or I/O will be driven to a high logic level, thereby avoiding exposure to a high-impedance or floating condition. The terminator is ESD and latch-up protected by the input, output, or I/O cell. When the terminator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: PR400LJ (input,output,or I/O node name);

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), PWRDN = L‡

PARAMETER	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
I_O Output current	V_O = 4 V	44	196	478	47	196	451	μA
	V_O = 2.5 V	150	365	742	161	365	701	
	V_O = 0	170	400	805	180	400	762	

‡ When PWRDN = H, the current source is turned off.

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

PUC00LJ
POWER-UP CLEAR ONE-SHOT

D3030, DECEMBER 1988

INTERNAL CELL

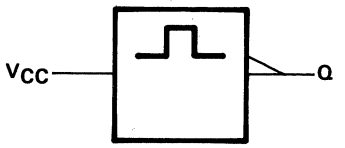
description

The PUC00LJ is a dedicated standard-cell implementing a positive-edge triggered one-shot that is automatically triggered by the rising edge of the 5-V power-up supply voltage.

When the PUC00LJ is incorporated in a standard-cell design, its output rises with V_{CC}. It produces a low-logic-level pulse when V_{CC} reaches the trigger level V1. As V_{CC} continues to rise, the pulse terminates and the output goes high when V_{CC} reaches V2. Another pulse will be initiated only if V_{CC} falls below V1. The duration of the low-logic-level pulse is dependent on the rise time of the supply voltage. The output of the PUC00LJ is used to initialize storage elements that can be preset or cleared asynchronously. For most applications, a single PUC00LJ is adequate to execute the power-up initialization. When the one-shot is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: PUC00LJ Q;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V1	Level of V_{CC} to initiate pulse	V_{CC} rising from 0 to 4.5 V		2	V
V2	Level of V_{CC} to terminate pulse			4	V

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS‡	MIN	MAX	UNIT
t_{wQ}	V_{CC}	Q	t_r = 50 ns	30		ns
			t_r = 1 µs	100		
			t_r = 100 µs	21		
			t_r = 10 ms	2.2		ms

‡ Rise times are measured between the 0.5 V and 4.5 V points of V_{CC}.

TO010LJ
ESD PROTECTED TIE-OFF WITH COMPLEMENTARY OUTPUTS

D3030, DECEMBER 1988

INTERNAL CELL

FUNCTION TABLE

OUTPUTS	
HI	LO
H	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE STD 91-1984.

AT APPLICATION OF V_{CC}: HI = H, LO = L

description

The TO010LJ internal tie-off cell is offered for managing unused inputs. The tie-off cell features complementary high-logic-level HI and low-logic-level LO outputs each capable of handling all unused inputs encountered in the standard cell design. When the cell is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TO010LJ LO,HI;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the applicable cell library.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER‡	TEST CONDITIONS	TYP	MAX	UNIT
C_{pd} Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	nil		pF

‡ For Supply Current, I_{CC}, see the TSC500 Series Data.

CK120LJ
CLOCK GENERATOR
WITH NONOVERLAPPING TWO-PHASE OUTPUTS

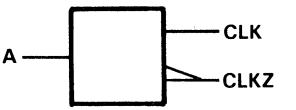
D3030, MARCH 1989

INTERNAL CLOCK GENERATOR CELL

FUNCTION TABLE

INPUT	OUTPUTS	
A	CLK	CLKZ
L	L	H
H	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The CK120LJ clock generator provides two-phase nonoverlapping clock outputs from a single clock input. The generator is compatible for use with the dual clocks needed to strobe the TDXXXLJ scan latches. When the clock generator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: CK120LJ A,CLK,CLKZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.11		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	3.96		pF

‡ For Supply Current, I_{CC}, see the TSC500 Series Data.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{PLH}	A	CLK	1.76	5.99	15.38	1.95	5.99	13.61	ns
t_{PHL}			0.2	1.01	2.71	0.22	1.01	2.46	
t_{PLH}	A	CLKZ	1.75	5.85	15.06	1.9	5.85	13.34	ns
t_{PHL}			0.27	2.01	3.13	0.31	2.01	2.83	
Δt_{PLH}	A	CLK	0.64	2.04	5.04	0.68	2.04	4.58	ns/pF
Δt_{PHL}			0.19	0.86	2.29	0.21	0.86	2.11	
Δt_{PLH}	A	CLKZ	0.6	2.02	5.04	0.66	2.02	4.54	ns/pF
Δt_{PHL}			0.21	0.88	2.32	0.22	0.88	2.14	

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

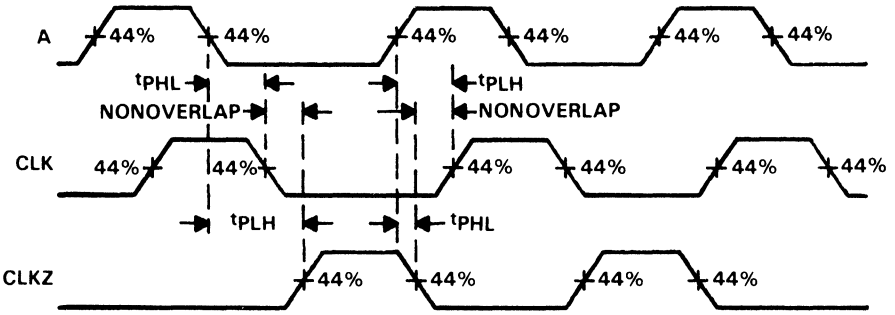


FIGURE 1. A TO CLK OR CLKZ TIMING DIAGRAM

7 Buffers/Drivers (Internal)

BUFFERS/DRIVERS FUNCTIONAL INDEX

D3030, JANUARY 1989

INTERNAL BUFFER CELLS

DESCRIPTION	CELL NAME	OUTPUT DRIVE	COMMENTS	EQUIVALENT NA210s	PAGE
1-Input	BU110LJ	1X	Noninverting	2	7-3
1-Input	BU111LJ	1X	Inverting	2.5	7-4
1-Input	BU112LJ	1X	Noninverting	2	7-5
1-Input	BU113LJ	1X	Noninverting	3.25	7-6
1-Input	BU114LJ	1X	Noninverting	3.25	7-7
1-Input	BU120LJ	2X	Noninverting	1.25	7-8
1-Input	BU130LJ	3X	Noninverting	1.75	7-9
2-Input 3-State	BU221LJ	2X	Noninverting, Active L enable	2.5	7-10
2-Input 3-State	BU222LJ	2X	Noninverting, Active H enable	2.5	7-12
2-Input 3-State	BU261LJ	6X	Noninverting, Active L enable	3.75	7-14
2-Input 3-State	BU262LJ	6X	Noninverting, Active H enable	3.75	7-16

INTERNAL INVERTER CELLS

DESCRIPTION	CELL NAME	OUTPUT DRIVE	COMMENTS	EQUIVALENT NA210s	PAGE
Inverters	IV101LJ	10X		4.5	7-18
	IV110LJ	1X		0.75	7-19
	IV120LJ	2X		1	7-20
	IV130LJ	3X		1.25	7-21
	IV140LJ	4X		1.5	7-22
	IV160LJ	6X		2	7-23
	IV180LJ	8X		2.5	7-24
Inverters with 3-State Outputs	IV211LJ	1X	Active L enable	1.25	7-25
	IV212LJ	1X	Active H enable	1.25	7-27
	IV221LJ	2X	Active L enable	2	7-29
	IV222LJ	2X	Active H enable	2	7-31
	IV241LJ	4X	Active L enable	3	7-33
	IV242LJ	4X	Active H enable	3	7-35

D3030, JANUARY 1989

INTERNAL BUFFERS (SOFTWARE)

DESCRIPTION	MACRO NAME	OUTPUT DRIVE	COMMENTS	EQUIVALENT NA210s	PAGE
Dual 4-Bit Drivers with 3-State Outputs	S244LJ	1X	Noninverting, Separate Active L enables	18	7-37
8-Bit Bidirect. with 3-State Outputs	S245LJ	1X	Noninverting, Active L enable	36	7-41

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BU110LJ
NONINVERTING BUFFER

D3030, JANUARY 1989

INTERNAL BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The BU110LJ cell is a noninverting buffer. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BU110LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.02		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.49		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	1.14	2.4	4.84	1.2	2.4	4.4	ns
t_{PHL}			1.41	3.89	8.67	1.49	3.89	8	
Δt_{PLH}	A	Y	0.42	1.2	2.6	0.46	1.2	2.4	ns/pF
Δt_{PHL}			0.52	1.32	2.84	0.56	1.32	2.58	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BU111LJ
INVERTING BUFFER

D3030, JANUARY 1989

INTERNAL BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$

description

The BU110LJ cell is an inverting buffer. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BU111LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.02		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.37		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	1.79	4.74	10.45	1.91	4.74	9.61	ns
t_{PHL}			1.83	4.65	10.06	1.95	4.65	9.21	
Δt_{PLH}	A	Y	0.44	1.16	2.5	0.46	1.16	2.28	ns/pF
Δt_{PHL}			0.6	1.48	3.18	0.64	1.48	2.9	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BU112LJ
NONINVERTING BUFFER

D3030, JANUARY 1989

INTERNAL BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The BU112LJ cell is a noninverting buffer. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BU112LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.03		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.7		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	0.79	1.6	3.18	0.82	1.6	2.91	ns
t_{PHL}			0.81	2.04	4.37	0.87	2.04	4.03	
Δt_{PLH}	A	Y	0.42	1.16	2.48	0.46	1.16	2.28	ns/pF
Δt_{PHL}			0.56	1.32	2.76	0.58	1.32	2.5	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BU113LJ
NONINVERTING BUFFER

D3030, MARCH 1989

INTERNAL BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The BU113LJ is a noninverting buffer. When called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BU113LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	2.7		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	2.3	4.77	9.52	2.45	4.77	8.62	ns
t_{PHL}			2.42	5.17	10.16	2.57	5.17	9.34	
Δt_{PLH}	A	Y	0.22	0.54	1.14	0.23	0.54	1.05	ns/pF
Δt_{PHL}			0.21	0.4	0.8	0.22	0.4	0.73	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BU114LJ
NONINVERTING BUFFER

D3030, MARCH 1989

INTERNAL BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The BU114LJ is a noninverting buffer. When called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BU114LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.08		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.69		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	3.99	8.11	15.99	4.26	8.11	14.48	ns
t_{PHL}			4.12	8.29	15.62	4.37	8.29	14.39	
Δt_{PLH}	A	Y	0.21	0.54	1.1	0.23	0.54	1	ns/pF
Δt_{PHL}			0.16	0.4	0.8	0.19	0.4	0.74	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BU120LJ
NONINVERTING BUFFER
WITH 2X OUTPUT

D3030, JANUARY 1989

INTERNAL BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The BU120LJ cell is a noninverting buffer featuring twice the capability of buffer BU110LJ to drive capacitive loads. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BU120LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.47		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	0.19	0.39	0.77	0.2	0.39	0.72	ns
t_{PHL}			0.27	0.55	1.04	0.28	0.55	0.97	
Δt_{PLH}	A	Y	0.19	0.54	1.13	0.2	0.54	1.04	ns/pF
Δt_{PHL}			0.13	0.32	0.68	0.15	0.32	0.6	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BU130LJ
NONINVERTING BUFFER
WITH 3X OUTPUT

D3030, JANUARY 1989

INTERNAL BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The BU130LJ cell is a noninverting buffer featuring three times the capability of buffer BU110LJ to drive capacitive loads. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BU130LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.71		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	0.21	0.49	0.87	0.22	0.49	0.82	ns
t_{PHL}			0.3	0.62	1.22	0.31	0.62	1.13	
Δt_{PLH}	A	Y	0.14	0.34	0.77	0.14	0.34	0.7	ns/pF
Δt_{PHL}			0.09	0.25	0.54	0.1	0.25	0.48	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BU221LJ
NONINVERTING 3-STATE BUFFER WITH ACTIVE-LOW ENABLE AND 2X OUTPUT

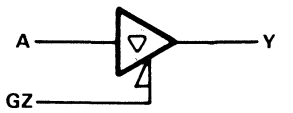
D3030, JANUARY 1989

INTERNAL BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The BU221LJ cell is a noninverting 3-state internal buffer that interfaces internal cells with internal buses. The buffer features twice the capability of buffer BU110LJ to drive capacitive loads. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BU221LJ A,GZ,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A		0.06		pF
		GZ		0.14		
C_o	Output capacitance			0.11		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		0.66	pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BU221LJ
NONINVERTING 3-STATE BUFFER WITH ACTIVE-LOW ENABLE AND 2X OUTPUT

D3030, JANUARY 1989

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.21	0.61	1.36	0.22	0.61	1.25	ns
t_{PHL}				0.3	0.62	1.24	0.31	0.62	1.15	
t_{PZH}	GZ	Y	R_L = 40 kΩ to GND	0.01	0.11	0.17	0.01	0.11	0.18	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.17	0.37	0.71	0.18	0.37	0.66	
t_{PHZ}	GZ	Y	R_L = 40 kΩ to GND		4.67			4.67		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		2.43			2.43		
Δt_{PLH}	A	Y		0.35	1.04	2.28	0.38	1.04	2.09	ps/pF
Δt_{PHL}				0.18	0.47	1.02	0.19	0.47	0.92	
Δt_{PZH}	GZ	Y		0.4	1.04	2.33	0.42	1.04	2.13	ps/pF
Δt_{PZL}				0.23	0.47	1.02	0.23	0.47	0.92	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BU222LJ
NONINVERTING 3-STATE BUFFER WITH ACTIVE-HIGH ENABLE AND 2X OUTPUT

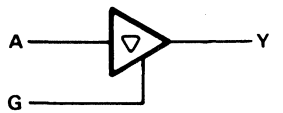
D3030, JANUARY 1989

INTERNAL BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
G	A	Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if G is H)

description

The BU222LJ cell is a noninverting 3-state internal buffer that interfaces internal cells with internal buses. The buffer features twice the capability of buffer BU110LJ to drive capacitive loads. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BU222LJ A,G,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A		0.06		pF
		GZ		0.1		
C_o	Output capacitance			0.11		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.65		pF

BU222LJ
NONINVERTING 3-STATE BUFFER WITH ACTIVE-HIGH ENABLE AND 2X OUTPUT

D3030, JANUARY 1989

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.21	0.62	1.38	0.22	0.62	1.28	ns
t_{PHL}				0.3	0.61	1.21	0.3	0.61	1.12	
t_{PZH}	GZ	Y	R_L = 40 kΩ to GND	0.11	0.3	0.67	0.11	0.3	0.62	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.11	0.22	0.39	0.1	0.22	0.4	
t_{PHZ}	GZ	Y	R_L = 40 kΩ to GND		5.1			5.1		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		2.11			2.11		
Δt_{PLH}	A	Y		0.35	1.04	2.27	0.38	1.04	2.08	ps/pF
Δt_{PHL}				0.17	0.46	1.02	0.19	0.46	0.91	
Δt_{PZH}	GZ	Y		0.34	1.05	2.31	0.37	1.05	2.12	ps/pF
Δt_{PZL}				0.32	0.51	1	0.36	0.51	0.88	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BU261LJ
NONINVERTING 3-STATE BUFFER WITH ACTIVE-LOW ENABLE AND 6X OUTPUT

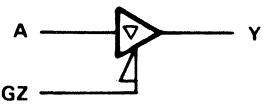
D3030, JANUARY 1989

INTERNAL BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The BU261LJ cell is a noninverting 3-state internal buffer that interfaces internal cells with internal buses. The buffer features six times the capability of buffer BU110LJ to drive capacitive loads. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BU261LJ A,GZ,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A		0.1		pF
		GZ		0.12		
C_o	Output capacitance			0.23		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.44		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BU261LJ
NONINVERTING 3-STATE BUFFER WITH ACTIVE-LOW ENABLE AND 6X OUTPUT

D3030, JANUARY 1989

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.21	0.55	1.05	0.22	0.55	0.99	ns
t_{PHL}				0.33	0.74	1.54	0.34	0.74	1.41	
t_{PZH}	GZ	Y	R_L = 40 kΩ to GND	0.29	0.69	1.49	0.3	0.69	1.37	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.23	0.62	1.51	0.22	0.62	1.43	
t_{PHZ}	GZ	Y	R_L = 40 kΩ to GND		7.13			7.13		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		3.34			3.34		
Δt_{PLH}	A	Y		0.11	0.22	0.49	0.11	0.22	0.45	ps/pF
Δt_{PHL}				0.08	0.2	0.46	0.09	0.2	0.43	
Δt_{PZH}	GZ	Y		0.09	0.24	0.49	0.09	0.24	0.45	ps/pF
Δt_{PZL}				0.09	0.25	0.52	0.11	0.25	0.47	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BU262LJ
NONINVERTING 3-STATE BUFFER WITH ACTIVE-HIGH ENABLE AND 6X OUTPUT

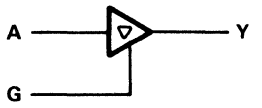
D3030, JANUARY 1989

INTERNAL BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
G	A	Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if G is H)

description

The BU262LJ cell is a noninverting 3-state internal buffer that interfaces internal cells with internal buses. The buffer features six times the capability of buffer BU110LJ to drive capacitive loads. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BU262LJ A,G,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A		0.11		pF
		GZ		0.12		
C_o	Output capacitance			0.23		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.42		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BU262LJ
NONINVERTING 3-STATE BUFFER WITH ACTIVE-HIGH ENABLE AND 6X OUTPUT

D3030, JANUARY 1989

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.21	0.55	1.05	0.22	0.55	0.99	ns
t_{PHL}				0.33	0.73	1.54	0.34	0.73	1.41	
t_{PZH}	GZ	Y	R_L = 40 kΩ to GND	0.1	0.47	1.01	0.12	0.47	0.94	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.22	0.78	1.91	0.24	0.78	1.75	
t_{PHZ}	GZ	Y	R_L = 40 kΩ to GND		7.03			7.03		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		3.41			3.41		
Δt_{PLH}	A	Y		0.11	0.22	0.49	0.11	0.22	0.45	ps/pF
Δt_{PHL}				0.08	0.2	0.46	0.09	0.2	0.43	
Δt_{PZH}	GZ	Y		0.16	0.23	0.45	0.15	0.23	0.41	ps/pF
Δt_{PZL}				0.05	0.24	0.51	0.06	0.24	0.46	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IV101LJ
INVERTER WITH 10X OUTPUT

D3030, JANUARY 1989

INTERNAL INVERTER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$

description

The IV101LJ cell is an inverter featuring ten times the capability of inverter IV110LJ to drive capacitive loads. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV101LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	3.11		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	0.36	0.88	1.84	0.38	0.88	1.69	ns
t_{PHL}			0.3	0.8	1.71	0.31	0.8	1.58	
Δt_{PLH}	A	Y	0.05	0.11	0.25	0.05	0.11	0.23	ns/pF
Δt_{PHL}			0.02	0.1	0.23	0.04	0.1	0.21	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

INTERNAL INVERTER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$

description

The IV110LJ cell is a minimum-size inverter. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV110LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance			0.05	pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		0.16	pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	0.19	0.24	0.32	0.2	0.24	0.31	ns
t_{PHL}			0.18	0.31	0.4	0.19	0.31	0.39	
Δt_{PLH}	A	Y	0.4	1.08	2.3	0.42	1.08	2.12	ns/pF
Δt_{PHL}			0.4	0.74	1.46	0.42	0.74	1.32	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

IV120LJ
INVERTER WITH 2X OUTPUT

D3030, JANUARY 1989

INTERNAL INVERTER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$

description

The IV120LJ cell is an inverter featuring twice the capability of inverter IV110LJ to drive capacitive loads. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV120LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.11		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.31		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	0.14	0.23	0.31	0.14	0.23	0.31	ns
t_{PHL}			0.09	0.24	0.41	0.11	0.24	0.39	
Δt_{PLH}	A	Y	0.24	0.52	1.1	0.26	0.52	1	ns/pF
Δt_{PHL}			0.28	0.42	0.68	0.28	0.42	0.62	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

IV130LJ
INVERTER WITH 3X OUTPUT

D3030, JANUARY 1989

INTERNAL INVERTER CELL

FUNCTION TABLE

INPUT	OUTPUT
A	Y
H	L
L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$

description

The IV130LJ cell is an inverter featuring three times the capability of inverter IV110LJ to drive capacitive loads. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV130LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.18		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.49		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	0.15	0.23	0.34	0.15	0.23	0.33	ns
t_{PHL}			0.05	0.15	0.35	0.05	0.15	0.34	
Δt_{PLH}	A	Y	0.18	0.36	0.72	0.19	0.36	0.66	ns/pF
Δt_{PHL}			0.16	0.3	0.41	0.18	0.3	0.37	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

IV140LJ
INVERTER WITH 4X OUTPUT

D3030, JANUARY 1989

INTERNAL INVERTER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$

description

The IV140LJ cell is an inverter featuring four times the capability of inverter IV110LJ to drive capacitive loads. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV140LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.23		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.63		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	0.12	0.19	0.33	0.13	0.19	0.32	ns
t_{PHL}			0.05	0.18	0.35	0.06	0.18	0.33	
Δt_{PLH}	A	Y	0.14	0.3	0.52	0.14	0.3	0.48	ns/pF
Δt_{PHL}			0.18	0.26	0.38	0.18	0.26	0.36	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

IV160LJ INVERTER WITH 6X OUTPUT

D3030, JANUARY 1989

INTERNAL INVERTER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$

description

The IV160LJ cell is an inverter featuring six times the capability of inverter IV110LJ to drive capacitive loads. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV160LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.35		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.93		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	0.1	0.17	0.29	0.1	0.17	0.29	ns
t_{PHL}			0.04	0.16	0.31	0.05	0.16	0.3	
Δt_{PLH}	A	Y	0.12	0.22	0.38	0.12	0.22	0.34	ns/pF
Δt_{PHL}			0.14	0.2	0.3	0.14	0.2	0.28	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

IV180LJ
INVERTER WITH 8X OUTPUT

D3030, JANUARY 1989

INTERNAL INVERTER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$

description

The IV180LJ cell is an inverter featuring eight times the capability of inverter IV110LJ to drive capacitive loads. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV180LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.46		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.23		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	0.09	0.16	0.28	0.11	0.16	0.27	ns
t_{PHL}			0.04	0.15	0.28	0.05	0.15	0.27	
Δt_{PLH}	A	Y	0.09	0.18	0.3	0.11	0.18	0.28	ns/pF
Δt_{PHL}			0.1	0.16	0.26	0.1	0.16	0.24	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

IV211LJ
INVERTER WITH 3-STATE OUTPUT AND ACTIVE-LOW ENABLE

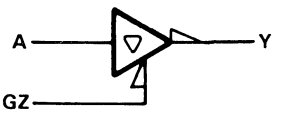
D3030, JANUARY 1989

INTERNAL INVERTER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$ (if GZ is L)

description

The IV211LJ cell is a minimum-size internal 3-state inverting buffer that interfaces CMOS cells with 3-state bus lines. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV211LJ A,GZ,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A		0.06		pF
		GZ		0.07		
C_o	Output capacitance			0.06		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.18		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.16	0.33	0.73	0.17	0.33	0.67	ns
t_{PHL}				0.2	0.34	0.62	0.2	0.34	0.57	
t_{PZH}	GZ	Y	R_L = 40 kΩ to GND	0.07	0.18	0.35	0.07	0.18	0.33	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.19	0.38	0.74	0.21	0.38	0.68	
t_{PHZ}	GZ	Y	R_L = 40 kΩ to GND		3.49			3.49		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		1.87			1.87		
Δt_{PLH}	A	Y		0.7	2.06	4.54	0.74	2.06	4.18	ps/pF
Δt_{PHL}				0.48	1.22	2.68	0.52	1.22	2.42	
Δt_{PZH}	GZ	Y		0.74	2.14	4.8	0.8	2.14	4.4	ps/pF
Δt_{PZL}				0.48	1.26	2.86	0.5	1.26	2.56	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IV212LJ
INVERTER 3-STATE OUTPUT AND ACTIVE-HIGH ENABLE

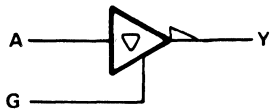
D3030, JANUARY 1989

INTERNAL INVERTER CELL

FUNCTION TABLE

INPUTS		OUTPUT
G	A	Y
H	H	L
H	L	H
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$ (if G is H)

description

The IV212LJ cell is a minimum-size internal 3-state buffer that interfaces CMOS cells with 3-state bus lines. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV212LJ A,G,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A		0.06		pF
		GZ		0.07		
C_o	Output capacitance			0.06		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.18		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.16	0.33	0.78	0.16	0.33	0.71	ns
t_{PHL}				0.2	0.34	0.6	0.2	0.34	0.56	
t_{PZH}	G	Y	R_L = 40 kΩ to GND	0.1	0.33	0.69	0.12	0.33	0.62	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.17	0.31	0.45	0.17	0.31	0.44	
t_{PHZ}	G	Y	R_L = 40 kΩ to GND		3.7			3.7		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		1.66			1.66		
Δt_{PLH}	A	Y		0.7	2.08	4.52	0.76	2.08	4.16	ps/pF
Δt_{PHL}				0.48	1.22	2.7	0.52	1.22	2.42	
Δt_{PZH}	G	Y		0.76	2.14	4.8	0.8	2.14	4.38	ps/pF
Δt_{PZL}				0.52	1.26	2.88	0.56	1.26	2.56	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IV221LJ
INVERTER WITH 3-STATE 2X OUTPUT AND ACTIVE-LOW ENABLE

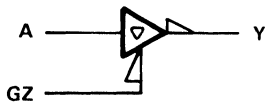
D3030, JANUARY 1989

INTERNAL INVERTER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$ (if GZ is L)

description

The IV221LJ cell is an internal 3-state internal inverter that interfaces CMOS cells with 3-state bus lines. The inverter features two times the capability of inverter IV211LJ to drive capacitive loads. When the cell is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV221LJ A,GZ,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A		0.11		pF
		GZ		0.1		
C_o	Output capacitance			0.11		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.38		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.17	0.36	0.77	0.19	0.36	0.71	ns
t_{PHL}				0.16	0.35	0.62	0.18	0.35	0.58	
t_{PZH}	GZ	Y	R_L = 40 kΩ to GND	0.02	0.17	0.31	0.04	0.17	0.3	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.19	0.4	0.76	0.19	0.4	0.72	
t_{PHZ}	GZ	Y	R_L = 40 kΩ to GND		4.1			4.1		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		2.04			2.04		
Δt_{PLH}	A	Y		0.34	1	2.22	0.34	1	2.04	ps/pF
Δt_{PHL}				0.28	0.6	1.34	0.28	0.6	1.2	
Δt_{PZH}	GZ	Y		0.42	1.04	2.3	0.42	1.04	2.1	ps/pF
Δt_{PZL}				0.24	0.6	1.36	0.26	0.6	1.2	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IV222LJ
INVERTER WITH 3-STATE 2X OUTPUT AND ACTIVE-HIGH ENABLE

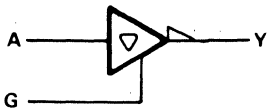
D3030, JANUARY 1989

INTERNAL INVERTER CELL

FUNCTION TABLE

INPUTS		OUTPUT
G	A	Y
H	H	L
H	L	H
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$ (if G is H)

description

The IV222LJ cell is an internal 3-state inverter that interfaces CMOS cells with 3-state bus lines. The inverter features two times the capability of inverter IV212LJ to drive capacitive loads. When the cell is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV222LJ A,G,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A		0.11		pF
		GZ		0.1		
C_o	Output capacitance			0.11		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.38		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.17	0.36	0.8	0.19	0.36	0.72	ns
t_{PHL}				0.17	0.34	0.59	0.18	0.34	0.55	
t_{PZH}	G	Y	R_L = 40 kΩ to GND	0.15	0.36	0.74	0.15	0.36	0.67	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.04	0.27	0.43	0.06	0.27	0.43	
t_{PHZ}	G	Y	R_L = 40 kΩ to GND		4.48			4.48		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		1.74			1.74		
Δt_{PLH}	A	Y		0.34	1	2.22	0.34	1	2.06	ps/pF
Δt_{PHL}				0.26	0.6	1.34	0.28	0.6	1.2	
Δt_{PZH}	G	Y		0.34	1.02	2.26	0.38	1.02	2.08	ps/pF
Δt_{PZL}				0.38	0.64	1.36	0.38	0.64	1.2	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IV241LJ
INVERTER WITH 3-STATE 4X OUTPUT AND ACTIVE-LOW ENABLE

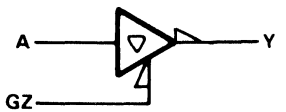
D3030, JANUARY 1989

INTERNAL INVERTER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$ (if GZ is L)

description

The IV241LJ cell is an internal 3-state inverter that interfaces CMOS cells with 3-state bus lines. The inverter features four times the capability of inverter IV211LJ to drive capacitive loads. When the cell is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV241LJ A,GZ,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A		0.22		pF
		GZ		0.15		
C_o	Output capacitance			0.18		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		0.72	pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.16	0.34	0.72	0.17	0.34	0.67	ns
t_{PHL}				0.12	0.3	0.62	0.13	0.31	0.58	
t_{PZH}	GZ	Y	R_L = 40 kΩ to GND	0.18	0.5	1.12	0.18	0.5	1.02	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.18	0.34	0.7	0.18	0.34	0.62	
t_{PHZ}	GZ	Y	R_L = 40 kΩ to GND		4.61			4.61		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		2.19			2.19		
Δt_{PLH}	A	Y		0.1	0.17	0.36	0.1	0.17	0.35	ps/pF
Δt_{PHL}				0.19	0.4	0.83	0.19	0.4	0.76	
Δt_{PZH}	GZ	Y		0.34	0.5	1.06	0.36	0.5	0.96	ps/pF
Δt_{PZL}				0.14	0.36	0.72	0.16	0.36	0.66	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IV242LJ
INVERTER WITH 3-STATE 4X OUTPUT AND ACTIVE-HIGH ENABLE

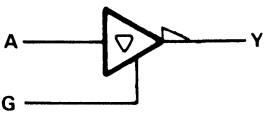
D3030, JANUARY 1989

INTERNAL INVERTER CELL

FUNCTION TABLE

INPUTS		OUTPUT
G	A	Y
H	H	L
H	L	H
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A}$ (if G is H)

description

The IV242LJ cell is an internal 3-state inverter that interfaces CMOS cells with 3-state bus lines. The inverter features four times the capability of inverter IV212LJ to drive capacitive loads. When the cell is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IV242LJ A,G,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A		0.22		pF
		GZ		0.15		
C_o	Output capacitance			0.18		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.75		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.16	0.36	0.8	0.16	0.36	0.73	ns
t_{PHL}				0.11	0.3	0.55	0.12	0.3	0.52	
t_{PZH}	G	Y	R_L = 40 kΩ to GND	0.16	0.41	0.79	0.18	0.41	0.73	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.1	0.19	0.44	0.1	0.19	0.41	
t_{PHZ}	G	Y	R_L = 40 kΩ to GND		5.34			5.34		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		1.7			1.7		
Δt_{PLH}	A	Y		0.18	0.5	1.1	0.2	0.5	1.02	ps/pF
Δt_{PHL}				0.18	0.32	0.68	0.18	0.32	0.6	
Δt_{PZH}	G	Y		0.2	0.5	1.14	0.2	0.5	1.06	ps/pF
Δt_{PZL}				0.3	0.38	0.62	0.3	0.38	0.58	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

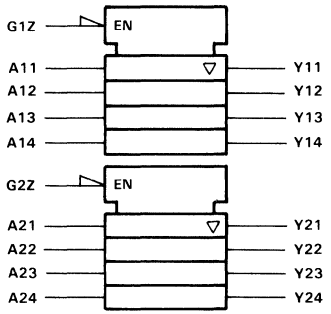
S244LJ
OCTAL INTERNAL BUS BUFFER WITH 3-STATE OUTPUTS

D3030, JANUARY 1989

SOFTWARE MACRO

- **3-State Outputs Directly Interface Internal Data Buses**
- **Active-Low Enables for Expandability**
- **Use Parallel Bus Interfaces for Wide Words**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S244LJ software macro implements an octal internal 3-state bus buffer. The macro is organized as dual 4-bit drivers with individual enables, G1Z and G2Z, which enable and disable the 3-state outputs to permit interfacing the internal bus directly in either a 4-bit parallel or an 8-bit word mode. The Yn outputs are in a high-impedance state when GnZ is high. When GnZ is low, the outputs drive the bus lines. The S244LJ is implemented with the standard cell functions indicated:

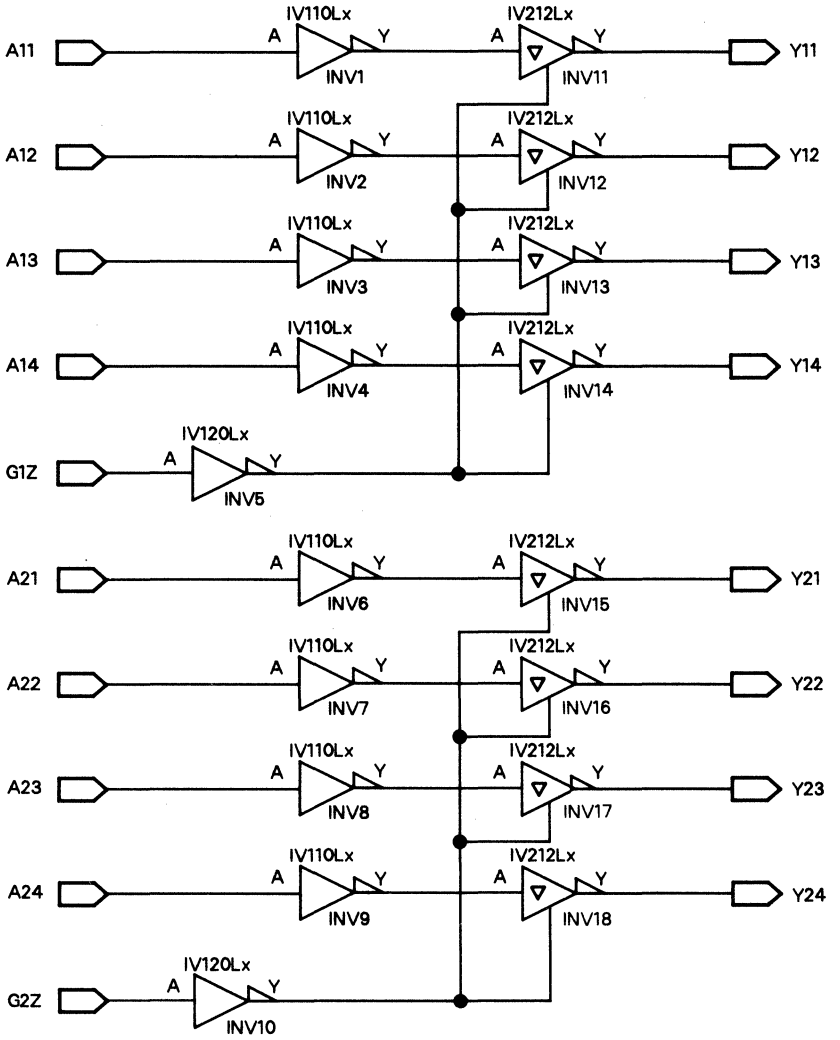
CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
IV110LJ	0.75	8	6	1.28
IV120LJ	1	2	2	0.62
IV212LJ	1.25	8	10	1.44
TOTALS		18	18	3.34

‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S244LJ A11,A12,A13,A14,G1Z,A21,A22,A23,A24,
G2Z,Y11,Y12,Y13,Y14,Y21,Y22,Y23,Y24;

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A inputs		0.05		pF
		G1Z, G2Z		0.11		
C_{pd}	Equivalent power dissipation capacitance†		$t_r = t_f$ = 1 ns	3.4		pF

† The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Notes 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Any Y		0.8	1.6		0.8	1.4	ns
t_{PHL}				0.8	1.5		0.8	1.4	
t_{PZH}	GnZ	Any Y		0.8	1.6		0.8	1.4	ns
t_{PZL}				0.8	1.4		0.8	1.2	
Δt_{PLH}	Any A	Any Y	0.7	2.08	4.52	0.76	2.08	4.16	ns/pF
Δt_{PHL}			0.48	1.22	2.7	0.52	1.22	2.42	
Δt_{PZH}	GnZ	Any Y	0.76	2.14	4.8	0.8	2.14	4.38	ns/pF
Δt_{PZL}			0.52	1.26	2.88	0.56	1.26	2.56	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

2. Enable and delta-enable times are measured using the conditions specified for the IV212LJ.

HDL FILE†

```
BLOCK S244LJ;                    STRUCTURE
A11     @INPUT;                  INV1    :IV110LJ   A11,INV1O;
A12     @INPUT;                  INV10   :IV120LJ   G2Z,INV10O;
A13     @INPUT;                  INV11   :IV212LJ   INV1O,INV5O,Y11;
A14     @INPUT;                  INV12   :IV212LJ   INV2O,INV5O,Y12;
G1Z     @INPUT;                  INV13   :IV212LJ   INV3O,INV5O,Y13;
A21     @INPUT;                  INV14   :IV212LJ   INV4O,INV5O,Y14;
A22     @INPUT;                  INV15   :IV212LJ   INV6O,INV10O,Y21;
A23     @INPUT;                  INV16   :IV212LJ   INV7O,INV10O,Y22;
A24     @INPUT;                  INV17   :IV212LJ   INV8O,INV10O,Y23;
G2Z     @INPUT;                  INV18   :IV212LJ   INV9O,INV10O,Y24;
Y11     @OUTPUT;                 INV2    :IV110LJ   A12,INV2O;
Y12     @OUTPUT;                 INV3    :IV110LJ   A13,INV3O;
Y13     @OUTPUT;                 INV4    :IV110LJ   A14,INV4O;
Y14     @OUTPUT;                 INV5    :IV120LJ   G1Z,INV5O;
Y21     @OUTPUT;                 INV6    :IV110LJ   A21,INV6O;
Y22     @OUTPUT;                 INV7    :IV110LJ   A22,INV7O;
Y23     @OUTPUT;                 INV8    :IV110LJ   A23,INV8O;
Y24     @OUTPUT;                 INV9    :IV110LJ   A24,INV9O;
                                 END S244LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S245LJ
OCTAL INTERNAL 3-STATE BUS TRANSCEIVER

D3030, JANUARY 1989

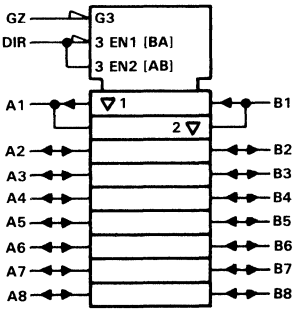
SOFTWARE MACRO

- **3-State Outputs Directly Interface Internal Data Buses**
- **Active-Low Enables for Expandability**
- **Use Parallel Bus Interfaces for Wide Words**

description

The S245LJ software macro implements an octal internal 3-state bidirectional I/O port. The macro is organized as an octal transceiver with direction control DIR and an output enable GZ. The GZ input enables and disables the 3-state outputs to permit interfacing or isolating the internal bus directly in a parallel mode. The outputs are in a high-impedance state when GZ is high. When GZ is low, the outputs selected by the DIR control drive the bus lines. The S245LJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

CONTROL INPUTS		OPERATION
GZ	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

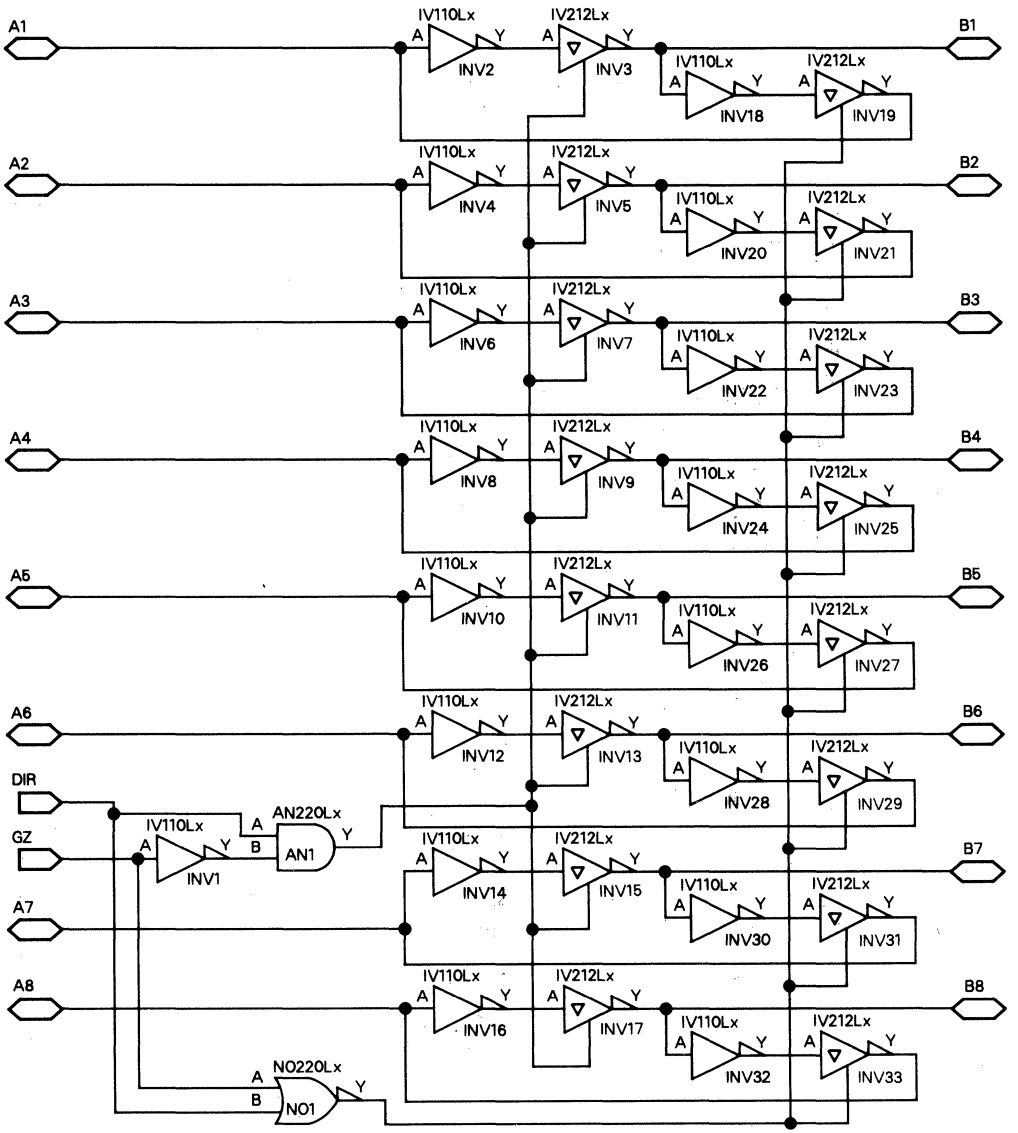
CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd}‡ (pF)
AN220LJ	1.75	1	1.75	0.47
IV110LJ	0.75	17	12.75	2.72
IV212LJ	1.25	16	20	2.88
NO220LJ	1.5	1	1.5	0.23
TOTALS		35	36	6.3

‡ The equivalent power dissipation capacitance does not include interconnect capacitance.

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S245LJ A1,A2,A3,A4,A5,A6,A7,A8,B1,B2,B3,B4,B5,B6,B7,B8,GZ,DIR;

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A or B		0.05		pF
		DIR		0.17		
		GZ		0.16		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	6.3		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Notes 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	An or Bn	Bn or An		0.9	1.8		0.9	1.6	ns
t_{PHL}				0.9	1.6		0.9	1.5	
t_{PZH}	GZ	An or Bn		1.8	4		1.8	3.6	ns
t_{PZL}				1.8	3.7		1.8	3.3	
Δt_{PLH}	An or Bn	Bn or An	0.7	2.08	4.52	0.76	2.08	4.16	ns/pF
Δt_{PHL}			0.48	1.22	2.7	0.52	1.22	2.42	
Δt_{PZH}	An or Bn	Bn or An	0.76	2.14	4.8	0.8	2.14	4.38	ns/pF
Δt_{PZL}			0.52	1.26	2.88	0.56	1.26	2.56	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

2. Enable and delta-enable times are measured using the conditions specified for the IV212LJ.

HDL FILE†

```
BLOCK S245LJ;
GZ          @INPUT;
DIR         @INPUT;
A1          @INOUT;
A2          @INOUT;
A3          @INOUT;
A4          @INOUT;
A5          @INOUT;
A6          @INOUT;
A7          @INOUT;
A8          @INOUT;
B1          @INOUT;
B2          @INOUT;
B3          @INOUT;
B4          @INOUT;
B5          @INOUT;
B6          @INOUT;
B7          @INOUT;
B8          @INOUT;

STRUCTURE
AN1         :AN220LJ    DIR,INV1O,AN1O;
INV1        :IV110LJ    GZ,INV1O;
INV10       :IV110LJ    A5,INV10O;
INV11       :IV212LJ    INV10O,AN1O,B5;
INV12       :IV110LJ    A6,INV12O;
INV13       :IV212LJ    INV12O,AN1O,B6;
INV14       :IV110LJ    A7,INV14O;
INV15       :IV212LJ    INV14O,AN1O,B7;
INV16       :IV110LJ    A8,INV16O;
INV17       :IV212LJ    INV16O,AN1O,B8;
INV18       :IV110LJ    B1,INV18O;
INV19       :IV212LJ    INV18O,NO1O,A1;
INV2        :IV110LJ    A1,INV2O;
INV20       :IV110LJ    B2,INV20O;
INV21       :IV212LJ    INV20O,NO1O,A2;
INV22       :IV110LJ    B3,INV22O;
INV23       :IV212LJ    INV22O,NO1O,A3;
INV24       :IV110LJ    B4,INV24O;
INV25       :IV212LJ    INV24O,NO1O,A4;
INV26       :IV110LJ    B5,INV26O;
INV27       :IV212LJ    INV26O,NO1O,A5;
INV28       :IV110LJ    B6,INV28O;
INV29       :IV212LJ    INV28O,NO1O,A6;
INV3        :IV212LJ    INV2O,AN1O,B1;
INV30       :IV110LJ    B7,INV30O;
INV31       :IV212LJ    INV30O,NO1O,A7;
INV32       :IV110LJ    B8,INV32O;
INV33       :IV212LJ    INV32O,NO1O,A8;
INV4        :IV110LJ    A2,INV4O;
INV5        :IV212LJ    INV4O,AN1O,B2;
INV6I       :IV110LJ    A3,INV6O;
INV7        :IV212LJ    INV6O,AN1O,B3;
INV8        :IV110LJ    A4,INV8O;
INV9        :IV212LJ    INV8O,AN1O,B4;
NO1         :NO220LJ    GZ,DIR,NO1O;
END S245LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

Gates

AND GATES

DESCRIPTION	CELL NAME	OUTPUT DRIVE	EQUIVALENT NA210s	PAGE
2-Input AND	AN210LJ	1X	1.5	8-7
	AN220LJ	2X	1.75	8-8
	AN240LJ	4X	2.25	8-9
	AN260LJ	6X	3	8-10
3-Input AND	AN310LJ	1X	1.75	8-11
	AN320LJ	2X	2	8-12
	AN340LJ	4X	2.5	8-13
	AN360LJ	6X	3.5	8-14
4-Input AND	AN410LJ	1X	2	8-15
	AN420LJ	2X	2.25	8-16
	AN440LJ	4X	2.75	8-17
	AN460LJ	6X	4	8-18
5-Input AND	AN510LJ	1X	2.5	8-19
8-Input AND	AN810LJ	1X	3.25	8-20

AND-OR/AND-NOR GATES

DESCRIPTION	CELL NAME	OUTPUT DRIVE	EQUIVALENT NA210s	PAGE
AND-OR	AO220LJ	2X	2	8-21
AND-NOR	AO221LJ	2X	1.75	8-22
AND-OR	AO230LJ	1X	2.75	8-23
	AO250LJ	1X	4	8-24
	AO320LJ	1X	2.5	8-25
	AO420LJ	1X	3.25	8-26
AND-NOR	AO421LJ	1X	3.5	8-27

D3030, APRIL 1988

MULTI-STAGE GATES

DESCRIPTION	CELL NAME	OUTPUT DRIVE	EQUIVALENT NA210s	PAGE
AND-NOR	BF001LJ	1X	1.5	8-28
	BF002LJ	1X	1.5	8-29
	BF004LJ	1X	1.75	8-30
	BF005LJ	1X	2	8-31
	BF006LJ	1X	1.75	8-32
	BF007LJ	1X	1.75	8-33
	BF008LJ	1X	2	8-34
	BF009LJ	1X	2	8-36
	BF010LJ	1X	2.25	8-38
	BF011LJ	1X	2.5	8-40
	BF012LJ	1X	2.5	8-42
	BF013LJ	1X	2.5	8-44
	BF014LJ	1X	2.75	8-46
OR-AND-NOR	BF015LJ	1X	1.75	8-48
	BF016LJ	1X	2	8-50
	BF017LJ	1X	1.75	8-52
	BF020LJ	1X	2	8-54
	BF022LJ	1X	2	8-56
	BF025LJ	1X	2.25	8-58
	BF027LJ	1X	2.25	8-60
	BF028LJ	1X	2.75	8-62
AND-OR-AND-NOR	BF030LJ	1X	2	8-64
	BF034LJ	1X	2.25	8-66
	BF035LJ	1X	2.25	8-68

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

MULTI-STAGE GATES (Continued)

DESCRIPTION	CELL NAME	OUTPUT DRIVE	EQUIVALENT NA210s	PAGE
OR-NAND	BF051LJ	1X	1.5	8-70
	BF052LJ	1X	1.5	8-71
	BF053LJ	1X	1.75	8-72
	BF054LJ	1X	1.75	8-73
	BF055LJ	1X	2	8-74
	BF056LJ	1X	1.75	8-76
	BF057LJ	1X	1.75	8-77
	BF058LJ	1X	2	8-78
	BF059LJ	1X	2.25	8-80
	BF060LJ	1X	2.25	8-82
	BF062LJ	1X	2.5	8-84
	BF063LJ	1X	2.5	8-86
	BF064LJ	1X	2.75	8-88
AND-OR-NAND	BF065LJ	1X	1.75	8-90
	BF066LJ	1X	2	8-92
	BF067LJ	1X	1.75	8-94
	BF068LJ	1X	2.25	8-96
	BF069LJ	1X	2.5	8-98
	BF070LJ	1X	2	8-100
	BF071LJ	1X	2.25	8-102
	BF072LJ	1X	2	8-104
	BF075LJ	1X	2	8-106
OR-AND-OR-NAND	BF080LJ	1X	2	8-108
	BF081LJ	1X	2.25	8-110
	BF082LJ	1X	2.25	8-112
	BF088LJ	1X	2.5	8-114

EX-NOR/EX-OR GATES

DESCRIPTION	CELL NAME	OUTPUT DRIVE	EQUIVALENT NA210s	PAGE
EX-NOR	EN210LJ	1X	2.25	8-116
EX-OR	EX210LJ	1X	1.75	8-117
	EX220LJ	2X	2	8-118
	EX240LJ	4X	2.5	8-119

D3030, APRIL 1988

NAND GATES

DESCRIPTION	CELL NAME	OUTPUT DRIVE	EQUIVALENT NA210s	PAGE
2-Input NAND	NA210LJ	1X	1	8-120
	NA220LJ	2X	1.5	8-121
	NA230LJ	3X	2	8-122
	NA240LJ	4X	2.5	8-123
	NA260LJ	6X	3.5	8-124
3-Input NAND	NA310LJ	1X	1.25	8-125
	NA320LJ	2X	2	8-126
	NA330LJ	3X	2.75	8-127
	NA340LJ	4X	3.5	8-128
4-Input NAND	NA410LJ	1X	1.5	8-129
	NA420LJ	2X	2.5	8-130
	NA430LJ	3X	3.5	8-131
5-Input NAND	NA510LJ	1X	3	8-132
	NA520LJ	2X	3.25	8-133
8-Input NAND	NA810LJ	1X	3.75	8-134
	NA820LJ	2X	4	8-135

NOR GATES

DESCRIPTION	CELL NAME	OUTPUT DRIVE	EQUIVALENT NA210s	PAGE
2-Input NOR	NO210LJ	1X	1	8-136
	NO220LJ	2X	1.5	8-137
	NO230LJ	3X	2	8-138
	NO240LJ	4X	2.5	8-139
3-Input NOR	NO310LJ	1X	1.25	8-140
	NO320LJ	2X	2	8-141
	NO330LJ	3X	2.75	8-142
4-Input NOR	NO410LJ	1X	1.5	8-143
	NO420LJ	2X	2.5	8-144
5-Input NOR	NO510LJ	1X	3.5	8-145
	NO520LJ	2X	3.75	8-146
8-Input NOR	NO810LJ	1X	3.75	8-147
	NO820LJ	2X	4	8-148

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OR-AND/OR-NAND GATES

DESCRIPTION	CELL NAME	OUTPUT DRIVE	EQUIVALENT NA210s	PAGE
OR-AND	OA220LJ	2X	2.25	8-149
	OA230LJ	1X	3	8-150
OR-NAND	OA231LJ	1X	3.25	8-151
OR-AND	OA240LJ	1X	3.75	8-152
OR-NAND	OA241LJ	1X	4	8-153
OR-AND	OA320LJ	2X	2.5	8-154

OR GATES

DESCRIPTION	CELL NAME	OUTPUT DRIVE	EQUIVALENT NA210s	PAGE
2-Input OR	OR210LJ	1X	1.25	8-155
	OR220LJ	2X	1.5	8-156
	OR240LJ	4X	2.5	8-157
	OR260LJ	6X	3.75	8-158
3-Input OR	OR310LJ	1X	1.5	8-159
	OR320LJ	2X	1.75	8-160
	OR340LJ	4X	3	8-161
	OR360LJ	6X	4.5	8-162
4-Input OR	OR410LJ	1X	1.75	8-163
	OR420LJ	2X	2.25	8-164
	OR440LJ	4X	3.5	8-165
	OR460LJ	6X	5.25	8-166
5-Input OR	OR510LJ	1X	3.75	8-167
8-Input OR	OR810LJ	1X	3.75	8-168

AN210LJ
2-INPUT POSITIVE-AND GATE

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

Equivalent to 1/4 7408

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \cdot B = \overline{\overline{A} + \overline{B}}$

description

The AN210LJ cell is a minimum-size, 2-input positive-AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN210LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.33		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.19	0.46	0.93	0.19	0.46	0.86	ns
t_{PHL}			0.26	0.54	1.09	0.26	0.54	1	
Δt_{PLH}	A, B	Y	0.42	1.12	2.36	0.46	1.12	2.16	ns/pF
Δt_{PHL}			0.26	0.59	1.2	0.3	0.59	1.08	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AN220LJ
2-INPUT POSITIVE-AND GATE WITH 2X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

Equivalent to 1/4 7408

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \cdot B = \overline{\overline{A} + \overline{B}}$

description

The AN220LJ cell is a 2-input positive-AND gate featuring twice the capacitive-drive capability when compared to the AN210LJ AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN220LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.47		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.24	0.55	1.11	0.26	0.55	1.03	ns
t_{PHL}			0.28	0.59	1.21	0.28	0.59	1.13	
Δt_{PLH}	A, B	Y	0.2	0.55	1.16	0.2	0.55	1.06	ns/pF
Δt_{PHL}			0.14	0.35	0.72	0.16	0.35	0.64	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

AN240LJ
2-INPUT POSITIVE-AND GATE WITH 4X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

Equivalent to 1/4 7408

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \cdot B = \overline{\overline{A} + \overline{B}}$

description

The AN240LJ cell is a 2-input positive-AND gate featuring four times the capacitive-drive capability when compared to the AN210LJ AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN240LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.96		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.28	0.72	1.46	0.3	0.72	1.34	ns
t_{PHL}			0.3	0.75	1.55	0.32	0.75	1.44	
Δt_{PLH}	A, B	Y	0.12	0.28	0.64	0.12	0.28	0.58	ns/pF
Δt_{PHL}			0.1	0.22	0.52	0.1	0.22	0.46	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AN260LJ
2-INPUT POSITIVE-AND GATE WITH 6X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

Equivalent to 1/4 7408

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \cdot B = \overline{\overline{A} + \overline{B}}$

description

The AN260LJ cell is a 2-input positive-AND gate featuring six times the capacitive-drive capability when compared to the AN210LJ AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN260LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.12		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.3		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.21	0.56	1.17	0.24	0.56	1.07	ns
t_{PHL}			0.18	0.6	1.21	0.2	0.6	1.11	
Δt_{PLH}	A, B	Y	0.1	0.22	0.44	0.1	0.22	0.4	ns/pF
Δt_{PHL}			0.12	0.16	0.36	0.12	0.16	0.32	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AN310LJ
3-INPUT POSITIVE-AND GATE

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol†

Equivalent to 1/3 7411

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \cdot B \cdot C = \overline{\overline{A} + \overline{B} + \overline{C}}$

description

The AN310LJ cell is a minimum-size, 3-input positive-AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN310LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.38		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C	Y	0.23	0.58	1.3	0.23	0.58	1.18	ns
t_{PHL}			0.26	0.63	1.3	0.27	0.63	1.2	
Δt_{PLH}	A, B, C	Y	0.4	1.08	2.28	0.44	1.08	2.1	ns/pF
Δt_{PHL}			0.3	0.59	1.22	0.32	0.59	1.1	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AN320LJ
3-INPUT POSITIVE-AND GATE WITH 2X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol†

Equivalent to 1/3 7411

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \cdot B \cdot C = \overline{\overline{A}+\overline{B}+\overline{C}}$

description

The AN320LJ cell is a 3-input positive-AND gate featuring twice the capacitive-drive capability when compared to the AN310LJ AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN320LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.55		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C	Y	0.24	0.69	1.52	0.27	0.69	1.4	ns
t_{PHL}			0.18	0.7	1.45	0.28	0.7	1.33	
Δt_{PLH}	A, B, C	Y	0.22	0.54	1.18	0.22	0.54	1.06	ns/pF
Δt_{PHL}			0.18	0.34	0.76	0.18	0.34	0.7	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

AN340LJ
3-INPUT POSITIVE-AND GATE WITH 4X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol†

Equivalent to 1/3 7411

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \cdot B \cdot C = \overline{\overline{A} + \overline{B} + \overline{C}}$

description

The AN340LJ cell is a 3-input positive-AND gate featuring four times the capacitive-drive capability when compared to the AN310LJ AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN340LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.98		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C	Y	0.32	0.86	1.95	0.33	0.86	1.78	ns
t_{PHL}			0.3	0.84	1.93	0.3	0.84	1.78	
Δt_{PLH}	A, B, C	Y	0.12	0.3	0.7	0.12	0.3	0.64	ns/pF
Δt_{PHL}			0.08	0.26	0.58	0.08	0.26	0.52	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AN360LJ
3-INPUT POSITIVE-AND GATE WITH 6X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol†

Equivalent to 1/3 7411

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \cdot B \cdot C = \overline{\overline{A} + \overline{B} + \overline{C}}$

description

The AN360LJ cell is a 3-input positive-AND gate featuring six times the capacitive-drive capability when compared to the AN310LJ AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN360LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.12		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.48		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C	Y	0.27	0.7	1.53	0.29	0.7	1.39	ns
t_{PHL}			0.26	0.68	1.45	0.28	0.68	1.35	
Δt_{PLH}	A, B, C	Y	0.08	0.22	0.46	0.08	0.22	0.44	ns/pF
Δt_{PHL}			0.06	0.15	0.36	0.08	0.15	0.32	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AN410LJ
4-INPUT POSITIVE-AND GATE

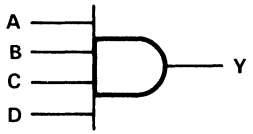
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
Any other combination				L

logic symbol†



Equivalent to 1/2 7421

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \cdot B \cdot C \cdot D = \overline{\overline{A} + \overline{B} + \overline{C} + \overline{D}}$

description

The AN410LJ cell is a minimum-size, 4-input positive-AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN410LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.42		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C, D	Y	0.24	0.71	1.7	0.26	0.71	1.53	ns
t_{PHL}			0.28	0.68	1.48	0.29	0.68	1.36	
Δt_{PLH}	A, B, C, D	Y	0.42	1.12	2.38	0.46	1.12	2.18	ns/pF
Δt_{PHL}			0.28	0.62	1.26	0.3	0.62	1.14	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AN420LJ
4-INPUT POSITIVE-AND GATE WITH 2X OUTPUT

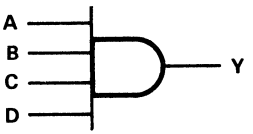
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
Any other combination				L

logic symbol†



Equivalent to 1/2 7421

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \cdot B \cdot C \cdot D = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}}$

description

The AN420LJ cell is a 4-input positive-AND gate featuring twice the capacitive-drive capability when compared to the AN410LJ AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN420LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.6		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C, D	Y	0.31	0.81	1.94	0.32	0.81	1.75	ns
t_{PHL}			0.26	0.74	1.67	0.28	0.74	1.54	
Δt_{PLH}	A, B, C, D	Y	0.18	0.58	1.26	0.2	0.58	1.16	ns/pF
Δt_{PHL}			0.16	0.37	0.78	0.18	0.37	0.7	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AN440LJ
4-INPUT POSITIVE-AND GATE WITH 4X OUTPUT

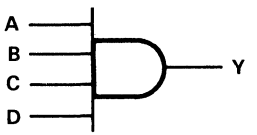
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
Any other combination				L

logic symbol†



Equivalent to 1/2 7421

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \cdot B \cdot C \cdot D = \overline{\overline{A} + \overline{B} + \overline{C} + \overline{D}}$

description

The AN440LJ cell is a 4-input positive-AND gate featuring four times the capacitive-drive capability when compared to the AN410LJ AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN440LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.01		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C, D	Y	0.36	1.01	2.54	0.37	1.01	2.27	ns
t_{PHL}			0.29	0.89	2.12	0.3	0.89	1.95	
Δt_{PLH}	A, B, C, D	Y	0.1	0.34	0.72	0.1	0.34	0.68	ns/pF
Δt_{PHL}			0.08	0.26	0.58	0.08	0.26	0.52	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AN460LJ
4-INPUT POSITIVE-AND GATE WITH 6X OUTPUT

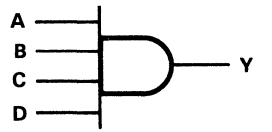
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
Any other combination				L

logic symbol†



Equivalent to 1/2 7421

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \cdot B \cdot C \cdot D = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}}$

description

The AN460LJ cell is a 4-input positive-AND gate featuring six times the capacitive-drive capability when compared to the AN410LJ AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN460LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.12		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.61		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C, D	Y	0.28	0.85	2	0.3	0.85	1.82	ns
t_{PHL}			0.32	0.75	1.67	0.32	0.75	1.54	
Δt_{PLH}	A, B, C, D	Y	0.1	0.24	0.5	0.1	0.24	0.46	ns/pF
Δt_{PHL}			0.04	0.19	0.42	0.04	0.19	0.4	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AN510LJ
5-INPUT POSITIVE-AND GATE

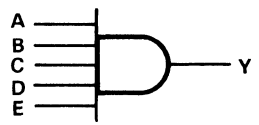
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
H	H	H	H	H	H
Any other combination					L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \cdot B \cdot C \cdot D \cdot E = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}+\overline{E}}$

description

The AN510LJ cell is a minimum-size, 5-input positive-AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN510LJ A,B,C,D,E,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.69		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C,D,E	Y	0.24	0.67	1.52	0.25	0.67	1.37	ns
t_{PHL}			0.24	0.57	1.28	0.24	0.57	1.18	
Δt_{PLH}	A,B,C,D,E	Y	0.6	1.74	3.82	0.66	1.74	3.52	ns/pF
Δt_{PHL}			0.22	0.57	1.04	0.25	0.57	0.94	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AN810LJ
8-INPUT POSITIVE-AND GATE

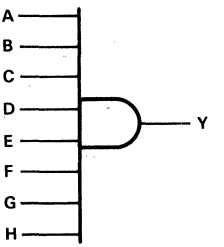
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
H	H	H	H	H	H	H	H	H
Any other combination								L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}+\overline{E}+\overline{F}+\overline{G}+\overline{H}}$

description

The AN810LJ cell is a minimum-size, 8-input positive-AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AN810LJ A,B,C,D,E,F,G,H,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.71		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A thru H	Y	0.25	0.78	1.86	0.27	0.78	1.68	ns
t_{PHL}			0.31	0.63	1.5	0.32	0.63	1.38	
Δt_{PLH}	A thru H	Y	0.74	2.1	4.61	0.78	2.1	4.23	ns/pF
Δt_{PHL}			0.3	0.6	1.27	0.32	0.6	1.14	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AO220LJ
AND-OR GATE WITH 2X OUTPUT
$Y = (A \cdot B) + (C \cdot D)$

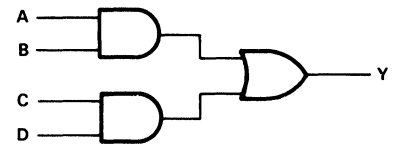
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	X	X	H
X	X	H	H	H
Any other combination				H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = (A \cdot B) + (C \cdot D)$

description

The AO220LJ cell is a 2-wide, 2-input AND-OR gate, featuring a 2X output drive capability to enhance its performance. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AO220LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.36		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C,D	Y	0.16	0.51	1.12	0.18	0.51	1.03	ns
t_{PHL}			0.3	0.88	2.12	0.32	0.88	1.93	
Δt_{PLH}	A,B,C,D	Y	0.42	1.1	2.34	0.44	1.1	2.14	ns/pF
Δt_{PHL}			0.34	0.79	1.62	0.36	0.79	1.46	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AO221LJ
AND-NOR GATE WITH 2X OUTPUT
$Y = \overline{(A \cdot B) + (C \cdot D)}$

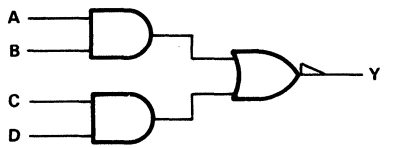
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	X	X	L
X	X	H	H	L
Any other combination				H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A \cdot B) + (C \cdot D)}$

description

The AO221LJ cell is a 2-wide, 2-input AND-NOR gate, featuring a 2X output drive capability to enhance its performance. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AO221LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.22		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C,D	Y	0.2	0.43	1.16	0.21	0.43	1.05	ns
t_{PHL}			0.17	0.36	0.71	0.17	0.36	0.66	
Δt_{PLH}	A,B,C,D	Y	0.68	2.03	4.58	0.72	2.03	4.22	ns/pF
Δt_{PHL}			0.36	0.91	2.02	0.4	0.91	1.82	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AO230LJ
3-WIDE, 2-INPUT AND-OR GATE
$Y = (A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2)$

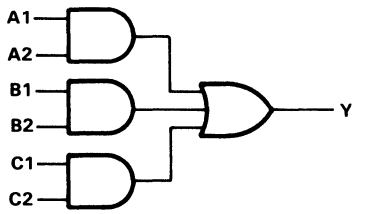
D3030, MARCH 1989

INTERNAL CELL

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	B1	B2	C1	C2	Y
H	H	X	X	X	X	H
X	X	H	H	X	X	H
X	X	X	X	H	H	H
Any other combination						L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = (A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2)$

description

The AO230LJ is a 3-wide, 2-input AND-OR gate. When called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AO230LJ A1,A2,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.44		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	0.16	0.56	1.32	0.17	0.56	1.22	ns
t_{PHL}			0.43	1.31	4.01	0.45	1.31	3.64	
Δt_{PLH}	Any	Y	0.41	1.11	2.38	0.44	1.11	2.18	ns/pF
Δt_{PHL}			0.38	0.91	1.9	0.42	0.91	1.73	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AO250LJ
5-WIDE AND-OR GATE
$Y = (A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2) + (D1 \cdot D2) + E1$

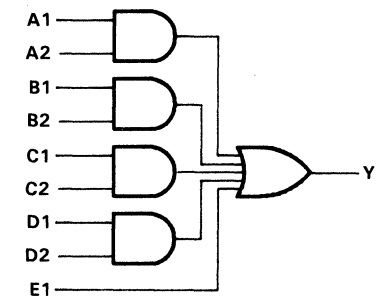
D3030, MARCH 1989

INTERNAL CELL

FUNCTION TABLE

INPUTS									OUTPUT
A1	A2	B1	B2	C1	C2	D1	D2	E1	Y
H	H	X	X	X	X	X	X	X	H
X	X	H	H	X	X	X	X	X	H
X	X	X	X	H	H	X	X	X	H
X	X	X	X	X	X	H	H	X	H
X	X	X	X	X	X	X	X	H	H
Any other combination									L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = (A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2) + (D1 \cdot D2) + E1$

description

The AO250LJ is a 5-wide, 2-2-2-2-1 input AND-OR gate. When called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AO250LJ A1,A2,B1,B2,C1,C2,D1,D2,E1,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.77		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	0.21	0.63	1.5	0.23	0.63	1.38	ns
t_{PHL}			0.38	1.31	4.19	0.4	1.31	3.82	
Δt_{PLH}	Any	Y	0.4	1.28	2.69	0.43	1.28	2.47	ns/pF
Δt_{PHL}			0.39	1.04	2.39	0.42	1.04	2.15	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AO320LJ
2-WIDE, 3-INPUT AND-OR GATE
Y = (A1·A2·A3) + (B1·B2·B3)

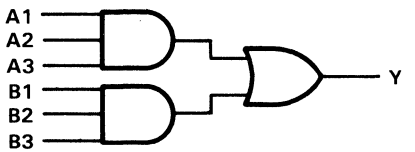
D3030, MARCH 1989

INTERNAL MACRO

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	A3	B1	B2	B3	Y
H	H	H	X	X	X	H
X	X	X	H	H	H	H
Any other combination						L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = (A1·A2·A3) + (B1·B2·B3)

description

The AO320LJ is a 2-wide, 3-input AND-OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AO320LJ A1,A2,A3,B1,B2,B3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.38		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	0.22	0.68	1.59	0.24	0.68	1.43	ns
t_{PHL}			0.33	1.06	2.84	0.34	1.06	2.61	
Δt_{PLH}	Any	Y	0.42	1.1	2.34	0.45	1.1	2.15	ns/pF
Δt_{PHL}			0.36	0.83	1.74	0.39	0.83	1.56	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

AO420LJ
2-WIDE, 4-INPUT AND-OR GATE
Y = (A1·A2·A3·A4) + (B1·B2·B3·B4)

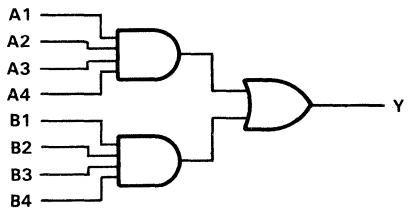
D3030, MARCH 1989

INTERNAL MACRO

FUNCTION TABLE

INPUTS								OUTPUT
A1	A2	A3	A4	B1	B2	B3	B4	Y
H	H	H	H	X	X	X	X	H
X	X	X	X	H	H	H	H	H
Any other combination								L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = (A1·A2·A3·A4) + (B1·B2·B3·B4)

description

The AO420LJ is a 2-wide, 4-input AND-OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AO420LJ A1,A2,A3,A4,B1,B2,B3,B4,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.43		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	0.28	0.91	2.28	0.3	0.91	2.05	ns
t_{PHL}			0.35	1.22	3.4	0.37	1.22	3.11	
Δt_{PLH}	Any	Y	0.42	1.13	2.47	0.45	1.13	2.26	ns/pF
Δt_{PHL}			0.37	0.86	1.85	0.4	0.86	1.67	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

AO421LJ
2-WIDE, 4-INPUT AND-NOR GATE
$Y = \overline{(A1 \cdot A2 \cdot A3 \cdot A4) + (B1 \cdot B2 \cdot B3 \cdot B4)}$

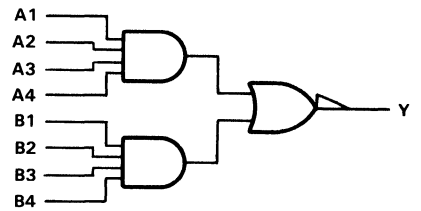
D3030, MARCH 1989

INTERNAL MACRO

FUNCTION TABLE

INPUTS								OUTPUT
A1	A2	A3	A4	B1	B2	B3	B4	Y
H	H	H	H	X	X	X	X	L
X	X	X	X	H	H	H	H	L
Any other combination								H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2 \cdot A3 \cdot A4) + (B1 \cdot B2 \cdot B3 \cdot B4)}$

description

The AO421LJ is a 2-wide, 4-input AND-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: AO421LJ A1,A2,A3,A4,B1,B2,B3,B4,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.58		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	0.36	1.26	3.45	0.38	1.26	3.16	ns
t_{PHL}			0.33	1.1	2.75	0.36	1.1	2.46	
Δt_{PLH}	Any	Y	0.41	1.1	2.3	0.45	1.1	2.11	ns/pF
Δt_{PHL}			0.34	0.73	1.47	0.37	0.73	1.32	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF001LJ
AND-NOR GATE
$Y = \overline{A1 + (B1 \cdot B2)}$

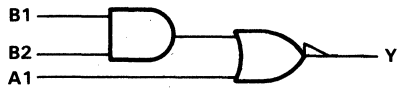
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A1	B1	B2	Y
H	X	X	L
X	H	H	L
L	L	X	H
L	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 + (B1 \cdot B2)}$

description

The BF001LJ cell is an expandable 1-2-input AND-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF001LJ A1,B1,B2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.12		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	0.27	0.42	0.77	0.28	0.42	0.71	ns
t_{PHL}			0.14	0.31	0.43	0.15	0.31	0.42	
t_{PLH}	Any B	Y	0.19	0.41	1.05	0.19	0.41	0.97	ns
t_{PHL}			0.18	0.36	0.62	0.19	0.36	0.58	
Δt_{PLH}	A1	Y	0.7	2.06	4.58	0.74	2.06	4.22	ns/pF
Δt_{PHL}			0.36	0.6	1.16	0.38	0.6	1.04	
Δt_{PLH}	Any B	Y	0.7	2.1	4.62	0.76	2.1	4.26	ns/pF
Δt_{PHL}			0.38	0.92	2	0.4	0.92	1.82	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF002LJ
AND-NOR GATE
$Y = \overline{A1 + (B1 \cdot B2 \cdot B3)}$

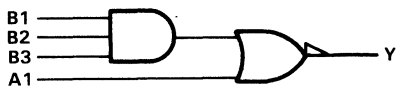
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A1	B1	B2	B3	Y
H	X	X	X	L
X	H	H	H	L
L	L	X	X	H
L	X	L	X	H
L	X	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 + (B1 \cdot B2 \cdot B3)}$

description

The BF002LJ cell is an expandable 1-3-input AND-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF002LJ A1,B1,B2,B3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.16		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	0.29	0.5	1.01	0.3	0.5	0.94	ns
t_{PHL}			0.15	0.32	0.42	0.16	0.32	0.41	
t_{PLH}	Any B	Y	0.17	0.44	1.38	0.18	0.44	1.24	ns
t_{PHL}			0.19	0.41	0.8	0.18	0.41	0.75	
Δt_{PLH}	A1	Y	0.7	2.08	4.6	0.74	2.08	4.22	ns/pF
Δt_{PHL}			0.36	0.6	1.18	0.38	0.6	1.06	
Δt_{PLH}	Any B	Y	0.72	2.11	4.54	0.76	2.11	4.22	ns/pF
Δt_{PHL}			0.42	1.25	2.88	0.48	1.25	2.56	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF004LJ
AND-NOR GATE
$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2 \cdot B3)}$

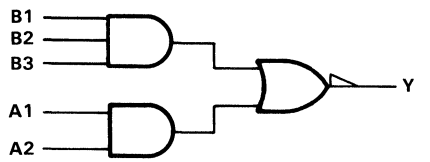
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A1	A2	B1	B2	B3	Y
H	H	X	X	X	L
X	X	H	H	H	L
Any other combination					H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2) + (B1 \cdot B2 \cdot B3)}$

description

The BF004LJ cell is a 2-wide, 2-3-input AND-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF004LJ A1,A2,B1,B2,B3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.22		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	0.27	0.56	1.3	0.27	0.56	1.21	ns
t_{PHL}			0.18	0.34	0.54	0.19	0.34	0.51	
t_{PLH}	Any B	Y	0.17	0.52	1.44	0.19	0.52	1.29	ns
t_{PHL}			0.19	0.45	0.9	0.21	0.45	0.82	
Δt_{PLH}	Any A	Y	0.7	2.08	4.6	0.74	2.08	4.22	ns/pF
Δt_{PHL}			0.38	0.91	2	0.4	0.91	1.8	
Δt_{PLH}	Any B	Y	0.72	2.11	4.6	0.78	2.11	4.26	ns/pF
Δt_{PHL}			0.44	1.25	2.88	0.46	1.25	2.58	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF005LJ
AND-NOR GATE
$Y = \overline{(A1 \cdot A2 \cdot A3) + (B1 \cdot B2 \cdot B3)}$

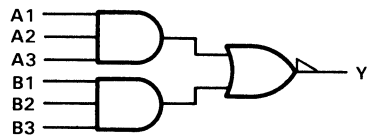
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	A3	B1	B2	B3	Y
H	H	H	X	X	X	L
X	X	X	H	H	H	L
Any other combination						H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2 \cdot A3) + (B1 \cdot B2 \cdot B3)}$

description

The BF005LJ cell is a 2-wide, 3-input AND-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF005LJ A1,A2,A3,B1,B2,B3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.26		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	0.2	0.57	1.58	0.2	0.57	1.46	ns
t_{PHL}			0.21	0.5	1.02	0.21	0.5	0.93	
t_{PLH}	Any B	Y	0.26	0.64	1.65	0.27	0.64	1.51	ns
t_{PHL}			0.2	0.41	0.77	0.19	0.41	0.71	
Δt_{PLH}	Any A	Y	0.72	2.11	4.6	0.78	2.11	4.18	ns/pF
Δt_{PHL}			0.44	1.24	2.88	0.48	1.24	2.6	
Δt_{PLH}	Any B	Y	0.7	2.09	4.6	0.76	2.09	4.24	ns/pF
Δt_{PHL}			0.42	1.24	2.86	0.46	1.24	2.56	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF006LJ
AND-NOR GATE
$Y = \overline{A1 + A2 + (B1 \cdot B2)}$

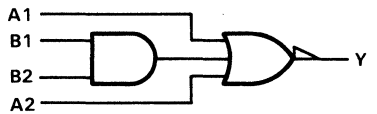
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A1	A2	B1	B2	Y
H	X	X	X	L
X	H	X	X	L
X	X	H	H	L
L	L	L	X	H
L	L	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1+A2+(B1 \cdot B2)}$

description

The BF006LJ cell is a 1-1-2-input AND-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF006LJ A1,A2,B1,B2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.15		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	0.29	0.59	1.52	0.29	0.59	1.37	ns
t_{PHL}			0.13	0.34	0.5	0.15	0.34	0.48	
t_{PLH}	Any B	Y	0.21	0.68	1.84	0.21	0.68	1.67	ns
t_{PHL}			0.19	0.39	0.68	0.2	0.39	0.63	
Δt_{PLH}	Any A	Y	1	3.09	6.88	1.06	3.09	6.34	ns/pF
Δt_{PHL}			0.36	0.6	1.18	0.38	0.6	1.06	
Δt_{PLH}	Any B	Y	1.02	3.1	6.88	1.1	3.1	6.34	ns/pF
Δt_{PHL}			0.38	0.93	2.06	0.4	0.93	1.86	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF007LJ
AND-NOR GATE
$Y = \overline{A1 + A2 + (B1 \cdot B2 \cdot B3)}$

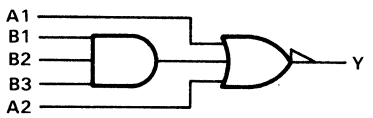
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A1	A2	B1	B2	B3	Y
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	H	H	L
L	L	L	X	X	H
L	L	X	L	X	H
L	L	X	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1+A2+(B1 \cdot B2 \cdot B3)}$

description

The BF007LJ cell is a 1-1-3-input AND-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF007LJ A1,A2,B1,B2,B3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.16		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	0.32	0.74	1.99	0.32	0.74	1.74	ns
t_{PHL}			0.15	0.35	0.51	0.16	0.35	0.49	
t_{PLH}	Any B	Y	0.21	0.77	2.27	0.22	0.77	2.09	ns
t_{PHL}			0.19	0.45	0.95	0.18	0.45	0.86	
Δt_{PLH}	Any A	Y	1	3.09	6.9	1.08	3.09	6.34	ns/pF
Δt_{PHL}			0.36	0.59	1.18	0.36	0.59	1.06	
Δt_{PLH}	Any B	Y	1.04	3.11	6.9	1.12	3.11	6.3	ns/pF
Δt_{PHL}			0.44	1.28	2.94	0.5	1.28	2.64	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF008LJ
AND-NOR GATE
$Y = \overline{A1 + (B1 \cdot B2) + (C1 \cdot C2)}$

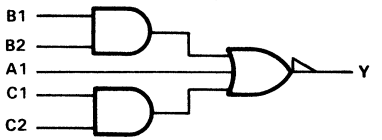
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A1	B1	B2	C1	C2	Y
H	X	X	X	X	L
X	H	H	X	X	L
X	X	X	H	H	L
Any other combinantion					H

logic symbol†



† This symbol is in accordance with ANSI/IEEE STD 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 + (B1 \cdot B2) + (C1 \cdot C2)}$

description

The BF008LJ cell is a 1-2-2-input AND-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF008LJ A1,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.21		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF008LJ
AND-NOR GATE
$Y = \overline{A1 + (B1 \cdot B2) + (C1 \cdot C2)}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.32	0.88	2.1	0.34	0.88	1.9	ns
t_{PHL}			0.18	0.38	0.56	0.2	0.38	0.53	
t_{PLH}	Any B	Y	0.26	0.88	2.39	0.27	0.88	2.16	ns
t_{PHL}			0.21	0.43	0.76	0.22	0.43	0.7	
t_{PLH}	Any C	Y	0.31	0.61	1.47	0.31	0.61	1.36	ns
t_{PHL}			0.17	0.34	0.55	0.18	0.34	0.52	
Δt_{PLH}	A1	Y	1.04	3.08	6.88	1.1	3.08	6.34	ns/pF
Δt_{PHL}			0.36	0.6	1.18	0.36	0.6	1.06	
Δt_{PLH}	Any B	Y	1.02	3.12	6.9	1.1	3.12	6.36	ns/pF
Δt_{PHL}			0.38	0.94	2.08	0.4	0.94	1.88	
Δt_{PLH}	Any C	Y	1	3.08	6.88	1.08	3.08	6.34	ns/pF
Δt_{PHL}			0.38	0.91	2	0.4	0.91	1.8	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF009LJ
AND-NOR GATE
$Y = \overline{A1 + (B1 \cdot B2) + (C1 \cdot C2 \cdot C3)}$

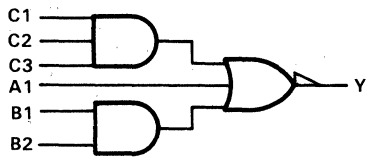
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS						OUTPUT
A1	B1	B2	C1	C2	C3	Y
H	X	X	X	X	X	L
X	H	H	X	X	X	L
X	X	X	H	H	H	L
Any other combination						H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 + (B1 \cdot B2) + (C1 \cdot C2 \cdot C3)}$

description

The BF009LJ cell is a 1-2-3-input AND-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF009LJ A1,B1,B2,C1,C2,C3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.2		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF009LJ
AND-NOR GATE
$Y = \overline{A1 + (B1 \cdot B2) + (C1 \cdot C2 \cdot C3)}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.35	1.02	2.51	0.37	1.02	2.28	ns
t_{PHL}			0.2	0.39	0.57	0.21	0.39	0.54	
t_{PLH}	Any B	Y	0.34	0.77	1.88	0.34	0.77	1.74	ns
t_{PHL}			0.18	0.37	0.58	0.19	0.37	0.54	
t_{PLH}	Any C	Y	0.25	0.99	2.79	0.29	0.99	2.54	ns
t_{PHL}			0.2	0.51	1.08	0.22	0.51	0.99	
Δt_{PLH}	A1	Y	1.04	3.01	6.88	1.1	3.1	6.34	ns/pF
Δt_{PHL}			0.34	0.6	1.18	0.36	0.6	1.06	
Δt_{PLH}	Any B	Y	1	3.08	6.9	1.08	3.08	6.34	ns/pF
Δt_{PHL}			0.38	0.9	2	0.4	0.9	1.8	
Δt_{PLH}	Any C	Y	1.04	3.11	6.9	1.1	3.11	6.36	ns/pF
Δt_{PHL}			0.44	1.28	2.94	0.48	1.28	2.64	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF010LJ
AND-NOR GATE
$Y = \overline{A1 + (B1 \cdot B2 \cdot B3) + (C1 \cdot C2 \cdot C3)}$

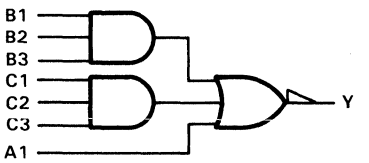
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS							OUTPUT
A1	B1	B2	B3	C1	C2	C3	Y
H	X	X	X	X	X	X	L
X	H	H	H	X	X	X	L
X	X	X	X	H	H	H	L
Any other combination							H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 + (B1 \cdot B2 \cdot B3) + (C1 \cdot C2 \cdot C3)}$

description

The BF010LJ cell is a 1-3-3-input AND-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF010LJ A1,B1,B2,B3,C1,C2,C3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.19		pF

BF010LJ
AND-NOR GATE
$Y = \overline{A1 + (B1 \cdot B2 \cdot B3) + (C1 \cdot C2 \cdot C3)}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.35	0.64	1.36	0.35	0.64	1.25	ns
t_{PHL}			0.15	0.33	0.44	0.16	0.33	0.43	
t_{PLH}	Any B	Y	0.26	0.88	2.48	0.27	0.88	2.26	ns
t_{PHL}			0.19	0.48	1.02	0.2	0.48	0.93	
t_{PLH}	Any C	Y	0.28	1.01	2.86	0.3	1.01	2.61	ns
t_{PHL}			0.2	0.49	0.98	0.21	0.49	0.89	
Δt_{PLH}	A1	Y	1	3.08	6.88	1.08	3.08	6.32	ns/pF
Δt_{PHL}			0.36	0.6	1.18	0.38	0.6	1.06	
Δt_{PLH}	Any B	Y	1.04	3.12	6.88	1.1	3.12	6.32	ns/pF
Δt_{PHL}			0.46	1.31	3	0.5	1.31	2.7	
Δt_{PLH}	Any C	Y	1.04	3.1	6.9	1.12	3.1	6.34	ns/pF
Δt_{PHL}			0.44	1.25	2.88	0.48	1.25	2.58	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF011LJ
AND-NOR GATE
$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2)}$

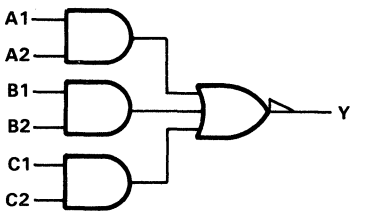
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	B1	B2	C1	C2	Y
H	H	X	X	X	X	L
X	X	H	H	X	X	L
X	X	X	X	H	H	L
Any other combination						H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2)}$

description

The BF011LJ cell is a 3-wide, 2-input AND-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF011LJ A1,A2,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.24		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF011LJ
AND-NOR GATE
$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2)}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.27	1	2.57	0.3	1	2.34	ns
t_{PHL}			0.2	0.44	0.8	0.22	0.44	0.73	
t_{PLH}	Any B	Y	0.32	0.98	2.59	0.34	0.98	2.36	ns
t_{PHL}			0.21	0.45	0.79	0.22	0.45	0.73	
t_{PLH}	Any C	Y	0.3	0.58	1.38	0.3	0.58	1.25	ns
t_{PHL}			0.17	0.34	0.55	0.18	0.34	0.54	
Δt_{PLH}	Any A	Y	1.06	3.09	6.9	1.12	3.09	6.36	ns/pF
Δt_{PHL}			0.38	0.96	2.1	0.4	0.96	1.9	
Δt_{PLH}	Any B	Y	1.04	3.11	6.9	1.1	3.11	6.32	ns/pF
Δt_{PHL}			0.38	0.91	2.02	0.4	0.91	1.82	
Δt_{PLH}	Any C	Y	1	3.07	6.88	1.08	3.07	6.36	ns/pF
Δt_{PHL}			0.38	0.91	1.98	0.4	0.91	1.78	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF012LJ
AND-NOR GATE
$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2 \cdot C3)}$

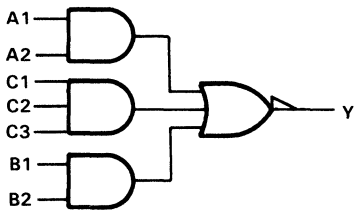
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS							OUTPUT
A1	A2	B1	B2	C1	C2	C3	Y
H	H	X	X	X	X	X	L
X	X	H	H	X	X	X	L
X	X	X	X	H	H	H	L
Any other combination							H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2 \cdot C3)}$

description

The BF012LJ cell is a 3-wide, 2-2-3-input AND-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF012LJ A1,A2,B1,B2,C1,C2,C3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.26		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF012LJ
AND-NOR GATE
$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2 \cdot C3)}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.29	1.02	2.67	0.3	1.02	2.43	ns
t_{PHL}			0.22	0.45	0.81	0.22	0.45	0.74	
t_{PLH}	Any B	Y	0.3	0.56	1.32	0.28	0.56	1.23	ns
t_{PHL}			0.17	0.35	0.57	0.17	0.35	0.54	
t_{PLH}	Any C	Y	0.32	1.08	3.07	0.33	1.08	2.79	ns
t_{PHL}			0.22	0.53	1.11	0.22	0.53	1.01	
Δt_{PLH}	A1	Y	1.06	3.12	6.9	1.12	3.12	6.36	ns/pF
Δt_{PHL}			0.38	0.96	2.12	0.4	0.96	1.92	
Δt_{PLH}	Any B	Y	1	3.07	6.88	1.08	3.07	6.34	ns/pF
Δt_{PHL}			0.38	0.91	1.98	0.42	0.91	1.78	
Δt_{PLH}	Any C	Y	1.04	3.11	6.9	1.12	3.11	6.34	ns/pF
Δt_{PHL}			0.44	1.25	2.86	0.46	1.25	2.56	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF013LJ
AND-NOR GATE
$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2 \cdot B3) + (C1 \cdot C2 \cdot C3)}$

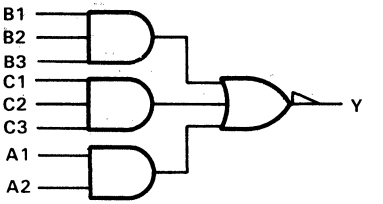
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS								OUTPUT
A1	A2	B1	B2	B3	C1	C2	C3	Y
H	H	X	X	X	X	X	X	H
X	X	H	H	H	X	X	X	L
X	X	X	X	X	H	H	H	L
Any other combination								H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2) + (B1 \cdot B2 \cdot B3) + (C1 \cdot C2 \cdot C3)}$

description

The BF013LJ cell is a 3-wide, 2-3-3-input AND-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF013LJ A1,A2,B1,B2,B3,C1,C2,C3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.25		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF013LJ
AND-NOR GATE

$$Y = \overline{(A1 \cdot A2) + (B1 \cdot B2 \cdot B3) + (C1 \cdot C2 \cdot C3)}$$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.31	0.7	1.71	0.31	0.7	1.58	ns
t_{PHL}			0.18	0.36	0.58	0.19	0.36	0.55	
t_{PLH}	Any B	Y	0.29	1.11	3.04	0.3	1.11	2.8	ns
t_{PHL}			0.22	0.54	1.16	0.24	0.54	1.05	
t_{PLH}	Any C	Y	0.33	1.24	3.42	0.34	1.24	3.12	ns
t_{PHL}			0.23	0.56	1.14	0.25	0.56	1.02	
Δt_{PLH}	Any A	Y	1.02	3.08	6.88	1.08	3.08	6.34	ns/pF
Δt_{PHL}			0.38	0.91	2	0.4	0.91	1.82	
Δt_{PLH}	Any B	Y	1.04	3.11	6.92	1.14	3.11	6.34	ns/pF
Δt_{PHL}			0.44	1.32	3.02	0.48	1.32	2.7	
Δt_{PLH}	Any C	Y	1.04	3.11	6.9	1.12	3.11	6.34	ns/pF
Δt_{PHL}			0.44	1.25	2.88	0.46	1.25	2.6	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF014LJ
AND-NOR GATE
$Y = \overline{(A1 \cdot A2 \cdot A3) + (B1 \cdot B2 \cdot B3) + (C1 \cdot C2 \cdot C3)}$

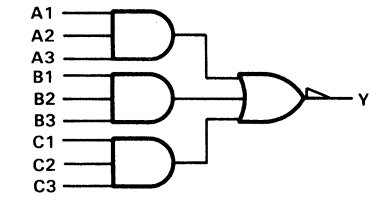
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS									OUTPUT
A1	A2	A3	B1	B2	B3	C1	C2	C3	Y
H	H	H	X	X	X	X	X	X	L
X	X	X	H	H	H	X	X	X	L
X	X	X	X	X	X	H	H	H	L
Any other combination									H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2 \cdot A3) + (B1 \cdot B2 \cdot B3) + (C1 \cdot C2 \cdot C3)}$

description

The BF014LJ cell is a 3-wide, 3-input AND-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF014LJ A1,A2,A3,B1,B2,B3,C1,C2,C3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.29		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF014LJ
AND-NOR GATE

$$Y = \overline{(A1 \cdot A2 \cdot A3) + (B1 \cdot B2 \cdot B3) + (C1 \cdot C2 \cdot C3)}$$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.35	1.35	3.67	0.38	1.35	3.33	ns
t_{PHL}			0.26	0.62	1.35	0.27	0.62	1.2	
t_{PLH}	Any B	Y	0.39	1.47	4.03	0.42	1.47	3.66	ns
t_{PHL}			0.25	0.63	1.31	0.26	0.63	1.18	
t_{PLH}	Any C	Y	0.31	0.83	2.22	0.33	0.83	2.03	ns
t_{PHL}			0.19	0.44	0.82	0.21	0.44	0.75	
Δt_{PLH}	Any A	Y	1.04	3.11	6.88	1.12	3.11	6.32	ns/pF
Δt_{PHL}			0.44	1.31	3.02	0.48	1.31	2.7	
Δt_{PLH}	Any B	Y	1.04	3.11	6.88	1.12	3.11	6.34	ns/pF
Δt_{PHL}			0.42	1.25	2.9	0.46	1.25	2.6	
Δt_{PLH}	Any C	Y	1.02	3.08	6.88	1.08	3.08	6.34	ns/pF
Δt_{PHL}			0.44	1.24	2.86	0.46	1.24	2.58	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF015LJ
OR-AND-NOR GATE
$Y = \overline{A1 + [B1 \cdot (C1 + C2)]}$

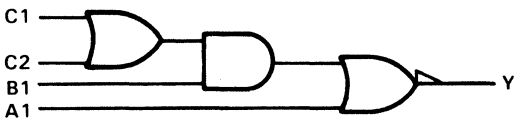
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A1	B1	C1	C2	Y
H	X	X	X	L
X	H	H	X	L
X	H	X	H	L
L	L	X	X	H
L	X	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 + [B1 \cdot (C1 + C2)]}$

description

The BF015LJ cell is a 2-input sum-of-products NOR gate with a dedicated 2-input OR, 2-input AND product term. One available input to the 2-input AND gate and the 2-input NOR gate provides expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF015LJ A1,B1,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.15		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF015LJ
OR-AND-NOR GATE
$Y = \overline{A1 + [B1 \cdot (C1 + C2)]}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.32	0.52	1.04	0.32	0.52	0.96	ns
t_{PHL}			0.14	0.33	0.43	0.15	0.33	0.43	
t_{PLH}	B1	Y	0.19	0.36	0.78	0.19	0.36	0.72	ns
t_{PHL}			0.22	0.39	0.6	0.23	0.39	0.58	
t_{PLH}	Any C	Y	0.24	0.72	1.85	0.26	0.72	1.67	ns
t_{PHL}			0.18	0.36	0.66	0.19	0.36	0.62	
Δt_{PLH}	A1	Y	1	3.08	6.88	1.08	3.08	6.32	ns/pF
Δt_{PHL}			0.36	0.58	1.16	0.38	0.58	1.04	
Δt_{PLH}	B1	Y	0.7	2.1	4.62	0.76	2.1	4.24	ns/pF
Δt_{PHL}			0.38	0.9	2.02	0.4	0.9	1.8	
Δt_{PLH}	Any C	Y	1.02	3.1	6.88	1.1	3.1	6.34	ns/pF
Δt_{PHL}			0.38	0.93	2.06	0.4	0.93	1.84	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF016LJ
OR-AND-NOR GATE
$Y = \overline{A1 + [(B1 + B2)\cdot(C1 + C2)]}$

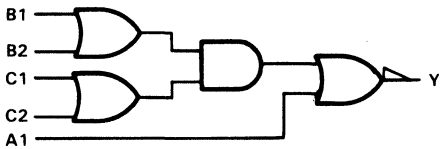
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A1	B1	B2	C1	C2	Y
H	X	X	X	X	L
X	H	X	H	X	L
X	X	H	H	X	L
X	H	X	X	H	L
X	X	H	X	H	L
L	L	L	X	X	H
L	X	X	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 + [(B1 + B2)\cdot(C1 + C2)]}$

description

The BF016LJ cell is a 2-input sum-of-products NOR gate with a dedicated 2-wide, 2-input OR-AND product term. The available NOR input can be used to combine other custom product terms with the 2-wide, 2-input OR-AND term. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF016LJ A1,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.17		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF016LJ
OR-AND-NOR GATE
$Y = \overline{A1 + [(B1 + B2) \cdot (C1 + C2)]}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.35	0.73	1.57	0.37	0.73	1.43	ns
t_{PHL}			0.14	0.35	0.47	0.16	0.35	1.46	
t_{PLH}	Any B	Y	0.3	0.95	2.38	0.31	0.95	2.16	ns
t_{PHL}			0.2	0.4	0.74	0.21	0.4	0.69	
t_{PLH}	Any C	Y	0.23	0.68	1.73	0.25	0.68	1.57	ns
t_{PHL}			0.22	0.44	0.7	0.25	0.44	0.66	
Δt_{PLH}	A1	Y	1.02	3.06	6.86	1.08	3.06	6.32	ns/pF
Δt_{PHL}			0.38	0.58	1.16	0.38	0.58	1.04	
Δt_{PLH}	Any B	Y	1.04	3.1	6.88	1.12	3.1	6.32	ns/pF
Δt_{PHL}			0.38	0.95	2.12	0.4	0.95	1.9	
Δt_{PLH}	Any C	Y	1.04	3.13	6.92	1.1	3.13	6.36	ns/pF
Δt_{PHL}			0.4	0.93	2.1	0.4	0.93	1.9	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF017LJ
OR-AND-NOR GATE
$Y = \overline{A1 + [B1 \cdot B2 \cdot (C1 + C2)]}$

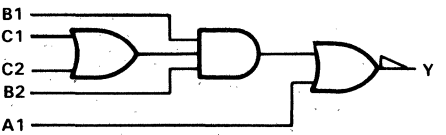
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A1	B1	B2	C1	C2	Y
L	L	X	X	X	H
L	X	L	X	X	H
L	X	X	L	L	H
L	L	X	L	L	H
L	X	L	L	L	H
X	H	H	H	X	L
X	H	H	X	H	L
H	X	X	X	X	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 + [B1 \cdot B2 \cdot (C1 + C2)]}$

description

The BF017LJ cell is a 2-input sum-of-products NOR gate with a dedicated 2-input OR, 3-input AND product term. Two available inputs to the 3-input AND gate and one to the other 2-input NOR gate provides expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF017LJ A1,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.16		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF017LJ
OR-AND-NOR GATE
$Y = \overline{A1 + [B1 \cdot B2 \cdot (C1 + C2)]}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.35	0.66	1.41	0.35	0.66	1.3	ns
t_{PHL}			0.15	0.32	0.44	0.16	0.32	0.43	
t_{PLH}	Any B	Y	0.2	0.5	1.28	0.21	0.5	1.16	ns
t_{PHL}			0.23	0.47	0.92	0.23	0.47	0.83	
t_{PLH}	Any C	Y	0.25	0.88	2.25	0.26	0.88	2.04	ns
t_{PHL}			0.18	0.44	0.95	0.2	0.44	0.87	
Δt_{PLH}	A1	Y	1	3.08	6.88	1.08	3.08	6.32	ns/pF
Δt_{PHL}			0.36	0.6	1.16	0.38	0.6	1.04	
Δt_{PLH}	Any B	Y	0.72	2.12	4.6	0.76	2.12	4.22	ns/pF
Δt_{PHL}			0.44	1.27	2.92	0.48	1.27	2.62	
Δt_{PLH}	Any C	Y	1.04	3.11	6.9	1.1	3.11	6.34	ns/pF
Δt_{PHL}			0.44	1.25	2.92	0.46	1.25	2.62	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF020LJ
OR-AND-NOR GATE
$Y = \overline{(A1 \cdot A2) + [B1 \cdot (C1 + C2)]}$

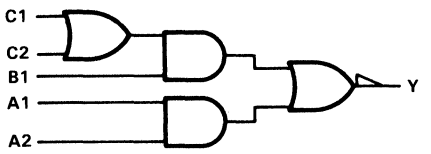
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A1	A2	B1	C1	C2	Y
H	H	X	X	X	L
X	X	H	H	X	L
X	X	H	X	H	L
Any other combination					L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2) + [B1 \cdot (C1 + C2)]}$

description

The BF020LJ cell is a 2-wide 2-input sum-of-products OR-AND-NOR gate with a dedicated 2-input OR, 2-input AND product term. One available input to one 2-input AND gate and two to the other 2-input AND gate provide expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF020LJ A1,A2,B1,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.21		pF

BF020LJ
OR-AND-NOR GATE
$Y = \overline{(A1 \cdot A2) + [B1 \cdot (C1 + C2)]}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.3	0.58	1.39	0.3	0.58	1.29	ns
t_{PHL}			0.17	0.34	0.53	0.18	0.34	0.5	
t_{PLH}	B1	Y	0.21	0.41	0.88	0.21	0.41	0.83	ns
t_{PHL}			0.23	0.42	0.66	0.23	0.42	0.62	
t_{PLH}	Any C	Y	0.26	0.78	2	0.28	0.78	1.8	ns
t_{PHL}			0.19	0.38	0.7	0.2	0.38	0.65	
Δt_{PLH}	Any A	Y	1	3.08	6.88	1.06	3.08	6.32	ns/pF
Δt_{PHL}			0.38	0.91	2	0.4	0.91	1.8	
Δt_{PLH}	B1	Y	0.7	2.1	4.62	0.76	2.1	4.22	ns/pF
Δt_{PHL}			0.38	0.9	2.02	0.42	0.9	1.82	
Δt_{PLH}	Any C	Y	1.02	3.11	6.86	1.1	3.11	6.32	ns/pF
Δt_{PHL}			0.38	0.94	2.08	0.4	0.94	1.86	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF022LJ
OR-AND-NOR GATE
$Y = \overline{(A1 \cdot A2) + [B1 \cdot B2 \cdot (C1 + C2)]}$

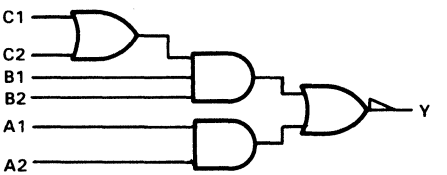
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	B1	B2	C1	C2	Y
H	H	X	X	X	X	L
X	X	H	H	H	X	L
X	X	H	H	X	H	L
Any other combination						H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2) + [B1 \cdot B2 \cdot (C1 + C2)]}$

description

The BF022LJ cell is a 2-wide 2-3-input sum-of-products AND-NOR gate with a dedicated 2-input OR, 3-input AND product term. Two available inputs to the 3-input AND gate and two to the other 2-input AND gate provide expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF022LJ A1,A2,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.22		pF

BF022LJ
OR-AND-NOR GATE
$Y = \overline{(A1 \cdot A2) + [B1 \cdot B2(C1 + C2)]}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.32	0.72	1.78	0.33	0.72	1.64	ns
t_{PHL}			0.18	0.34	0.53	0.19	0.34	0.5	
t_{PLH}	Any B	Y	0.22	0.56	1.39	0.23	0.56	1.27	ns
t_{PHL}			0.24	0.5	0.98	0.26	0.5	0.89	
t_{PLH}	Any C	Y	0.3	0.97	2.45	0.3	0.97	2.23	ns
t_{PHL}			0.18	0.47	1.03	0.2	0.47	0.93	
Δt_{PLH}	Any A	Y	1.02	3.09	6.9	1.08	3.09	6.34	ns/pF
Δt_{PHL}			0.38	0.92	2.02	0.4	0.92	1.82	
Δt_{PLH}	Any B	Y	0.72	2.1	4.62	0.76	2.1	4.24	ns/pF
Δt_{PHL}			0.44	1.28	2.94	0.48	1.28	2.64	
Δt_{PLH}	Any C	Y	1.02	3.1	6.84	1.12	3.1	6.28	ns/pF
Δt_{PHL}			0.46	1.26	2.94	0.48	1.26	2.64	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF025LJ
OR-AND-NOR GATE
$Y = \overline{(A1 \cdot A2 \cdot A3) + [B1 \cdot (C1 + C2)]}$

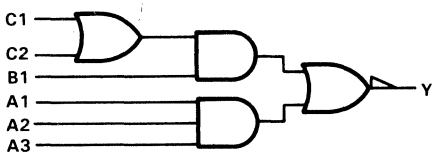
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	A3	B1	C1	C2	Y
H	H	H	X	X	X	L
X	X	X	H	H	X	L
X	X	X	H	X	H	L
Any other combination						H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2 \cdot A3) + [B1 \cdot (C1 + C2)]}$

description

The BF025LJ cell is a 2-wide 3-2-input sum-of-products AND-NOR gate with a dedicated 2-input OR, 2-input AND product term. One available input to the 2-input AND gate and three to the other 3-input AND gate provide expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF025LJ A1,A2,A3,B1,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.26		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF025LJ
OR-AND-NOR GATE
$Y = \overline{(A1 \cdot A2 \cdot A3) + [B1 \cdot (C1 + C2)]}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.29	0.64	1.87	0.29	0.64	1.72	ns
t_{PHL}			0.19	0.4	0.75	0.18	0.4	0.68	
t_{PLH}	B1	Y	0.23	0.46	1.01	0.23	0.46	0.93	ns
t_{PHL}			0.23	0.45	0.72	0.26	0.45	0.68	
t_{PLH}	Any C	Y	0.3	0.86	2.16	0.29	0.86	1.97	ns
t_{PHL}			0.2	0.42	0.77	0.21	0.42	0.7	
Δt_{PLH}	Any A	Y	1.02	3.08	6.9	1.1	3.08	6.36	ns/pF
Δt_{PHL}			0.42	1.24	2.84	0.48	1.24	2.56	
Δt_{PLH}	B1	Y	0.7	2.1	4.62	0.76	2.1	4.24	ns/pF
Δt_{PHL}			0.4	0.9	2.04	0.4	0.9	1.82	
Δt_{PLH}	Any C	Y	1.02	3.11	6.86	1.1	3.11	6.3	ns/pF
Δt_{PHL}			0.38	0.93	2.08	0.4	0.93	1.88	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF027LJ
OR-AND-NOR GATE
$Y = \overline{(A1 \cdot A2 \cdot A3) + [B1 \cdot B2 \cdot (C1 + C2)]}$

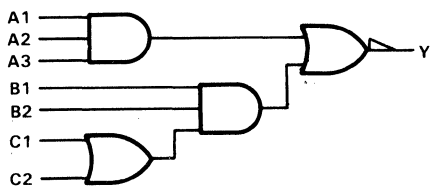
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS							OUTPUT
A1	A2	A3	B1	B2	C1	C2	Y
H	H	H	X	X	X	X	L
X	X	X	H	H	H	X	L
X	X	X	H	H	X	H	L
Any other combination							H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2 \cdot A3) + [B1 \cdot B2 \cdot (C1 + C2)]}$

description

The BF027LJ cell is a 2-wide 3-3-input sum-of-products AND-NOR gate with a dedicated 2-input OR, 3-input AND product term. Two available inputs to the 3-input AND gate and two to the other 3-input AND gate provide expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF027LJ A1,A2,A3,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.26		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF027LJ
OR-AND-NOR GATE
$Y = \overline{(A1 \cdot A2 \cdot A3) + [B1 \cdot B2 \cdot (C1 + C2)]}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.22	0.39	0.86	0.22	0.39	0.8	ns
t_{PHL}			0.17	0.37	0.68	0.18	0.37	0.63	
t_{PLH}	Any B	Y	0.24	0.46	1.12	0.24	0.46	1.01	ns
t_{PHL}			0.26	0.55	1.09	0.29	0.55	1	
t_{PLH}	Any C	Y	0.3	0.88	2.17	0.31	0.88	1.99	ns
t_{PHL}			0.24	0.62	1.48	0.24	0.62	1.32	
Δt_{PLH}	Any A	Y	0.48	1.39	3.1	0.52	1.39	2.86	ns/pF
Δt_{PHL}			0.42	1.19	2.72	0.44	1.19	2.44	
Δt_{PLH}	Any B	Y	0.44	1.35	2.88	0.48	1.35	2.68	ns/pF
Δt_{PHL}			0.38	1.01	2.28	0.38	1.01	2.04	
Δt_{PLH}	Any C	Y	0.74	2.33	5.16	0.8	2.33	4.76	ns/pF
Δt_{PHL}			0.4	1.18	2.72	0.44	1.18	2.46	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF028LJ
OR-AND-NOR GATE

$$Y = \overline{(A1 \cdot A2 \cdot A3) + [B1 \cdot (C1 + C2) \cdot (D1 + D2)]}$$

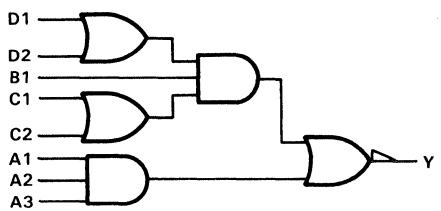
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS								OUTPUT
A1	A2	A3	B1	C1	C2	D1	D2	Y
H	H	H	X	X	X	X	X	L
X	X	X	H	H	X	H	X	L
X	X	X	H	H	X	X	H	L
X	X	X	H	X	H	H	X	L
X	X	X	H	X	H	X	H	L
Any other combination								H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2 \cdot A3) + [B1 \cdot (C1 + C2) \cdot (D1 + D2)]}$

description

The BF028LJ cell is a 2-wide AND-NOR gate with OR gates comprising 2 inputs to the second AND gate. The first AND gate has three available inputs. The second AND gate has one available input plus the 4 ORed inputs. This combination provides expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF028LJ A1,A2,A3,B1,C1,C2,D1,D2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.29		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF028LJ
OR-AND-NOR GATE

$$Y = \overline{(A1 \cdot A2 \cdot A3) + [B1 \cdot (C1 + C2) \cdot (D1 + D2)]}$$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.21	0.39	0.89	0.21	0.39	0.83	ns
t_{PHL}			0.18	0.37	0.71	0.18	0.37	0.63	
t_{PLH}	B1	Y	0.25	0.45	0.91	0.25	0.45	0.83	ns
t_{PHL}			0.28	0.52	0.93	0.31	0.52	0.86	
t_{PLH}	Any C	Y	0.32	1.03	2.6	0.33	1.03	2.36	ns
t_{PHL}			0.27	0.61	1.37	0.27	0.61	1.24	
t_{PLH}	Any D	Y	0.27	0.8	1.98	0.28	0.8	1.78	ns
t_{PHL}			0.27	0.59	1.25	0.27	0.59	1.15	
Δt_{PLH}	Any A	Y	0.52	1.51	3.38	0.54	1.51	3.1	ns/pF
Δt_{PHL}			0.42	1.22	2.78	0.46	1.22	2.52	
Δt_{PLH}	B1	Y	0.48	1.42	3.1	0.52	1.42	2.86	ns/pF
Δt_{PHL}			0.34	0.84	1.88	0.34	0.84	1.68	
Δt_{PLH}	Any C	Y	0.78	2.39	5.28	0.84	2.39	4.86	ns/pF
Δt_{PHL}			0.3	1.03	2.64	0.34	1.03	2.38	
Δt_{PLH}	Any D	Y	0.8	2.39	5.28	0.86	2.39	4.84	ns/pF
Δt_{PHL}			0.38	1.02	2.36	0.42	1.02	2.1	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF030LJ
AND-OR-AND-NOR GATE
$Y = \overline{A1 + \{B1 \cdot [C1 + (D1 \cdot D2)]\}}$

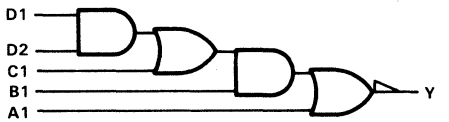
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A1	B1	C1	D1	D2	Y
H	X	X	X	X	L
X	H	H	X	X	L
X	H	X	H	H	L
Any other combination					H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 + \{B1 \cdot [C1 + (D1 \cdot D2)]\}}$

description

The BF030LJ cell is a 2-wide 1-2-input sum-of-products OR-AND-NOR gate with 2-input AND and one available input each to the 2-input AND and OR gates to provide expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF030LJ A1,B1,C1,D1,D2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.16		pF

BF030LJ
AND-OR-AND-NOR GATE
$Y = \overline{A1 + \{B1 \cdot [C1 + (D1 \cdot D2)]\}}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.24	0.3	0.46	0.24	0.3	0.44	ns
t_{PHL}			0.12	0.29	0.42	0.12	0.29	0.42	
t_{PLH}	B1	Y	0.19	0.37	0.76	0.2	0.37	0.7	ns
t_{PHL}			0.19	0.37	0.55	0.22	0.37	0.53	
t_{PLH}	C1	Y	0.25	0.6	1.36	0.25	0.6	1.24	ns
t_{PHL}			0.18	0.34	0.63	0.19	0.34	0.57	
t_{PLH}	Any D	Y	0.24	0.87	2.26	0.25	0.87	2.05	ns
t_{PHL}			0.17	0.45	0.95	0.19	0.45	0.85	
Δt_{PLH}	A1	Y	0.56	1.64	3.62	0.6	1.64	3.32	ns/pF
Δt_{PHL}			0.36	0.6	1.14	0.4	0.6	1	
Δt_{PLH}	B1	Y	0.7	2.06	4.58	0.74	2.06	4.2	ns/pF
Δt_{PHL}			0.38	0.78	1.7	0.38	0.78	1.52	
Δt_{PLH}	C1	Y	0.84	2.54	5.66	0.92	2.54	5.2	ns/pF
Δt_{PHL}			0.38	0.92	1.98	0.4	0.92	1.8	
Δt_{PLH}	Any D	Y	1.02	3.04	6.76	1.1	3.04	6.22	ns/pF
Δt_{PHL}			0.46	1.26	2.9	0.48	1.26	2.6	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF034LJ
AND-OR-AND-NOR GATE
$Y = \overline{(A1 \cdot A2) + \{B1 \cdot [C1 + (D1 \cdot D2)]\}}$

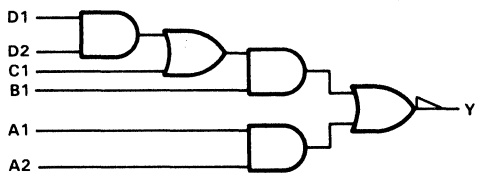
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	B1	C1	D1	D2	Y
H	H	X	X	X	X	L
X	X	H	H	X	X	L
X	X	H	X	H	H	L
Any other combination						H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2) + \{B1 \cdot [C1 + (D1 \cdot D2)]\}}$

description

The BF034LJ cell is a 2-wide 2-2-input sum-of-products AND-NOR gate with 2-input AND and one available input each to the 2-input AND and OR gates to provide expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF034LJ A1,A2,B1,C1,D1,D2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.23		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF034LJ
AND-OR-AND-NOR GATE

$$Y = \overline{(A1 \cdot A2) + \{B1 \cdot [C1 + (D1 \cdot D)]\}}$$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.22	0.33	0.65	0.22	0.33	0.62	ns
t_{PHL}			0.16	0.31	0.49	0.17	0.31	0.46	
t_{PLH}	B1	Y	0.22	0.41	0.8	0.22	0.41	0.73	ns
t_{PHL}			0.22	0.44	0.71	0.25	0.44	0.67	
t_{PLH}	C1	Y	0.25	0.7	1.66	0.28	0.7	1.53	ns
t_{PHL}			0.24	0.46	0.91	0.24	0.46	0.84	
t_{PLH}	Any D	Y	0.3	0.76	1.91	0.3	0.76	1.74	ns
t_{PHL}			0.21	0.51	1.12	0.21	0.51	1.02	
Δt_{PLH}	Any A	Y	0.54	1.64	3.6	0.58	1.64	3.3	ns/pF
Δt_{PHL}			0.36	0.86	1.88	0.38	0.86	1.7	
Δt_{PLH}	B1	Y	0.52	1.54	3.42	0.56	1.54	3.16	ns/pF
Δt_{PHL}			0.38	0.78	1.7	0.38	0.78	1.52	
Δt_{PLH}	C1	Y	0.7	2.08	4.58	0.72	2.08	4.2	ns/pF
Δt_{PHL}			0.36	0.94	2.06	0.4	0.94	1.84	
Δt_{PLH}	Any D	Y	0.84	2.58	5.72	0.92	2.58	5.26	ns/pF
Δt_{PHL}			0.44	1.25	2.84	0.48	1.25	2.56	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF035LJ
AND-OR-AND-NOR GATE

$$Y = \overline{(A1 \cdot A2) + \{B1 \cdot [(C1 \cdot C2) + (D1 \cdot D2)]\}}$$

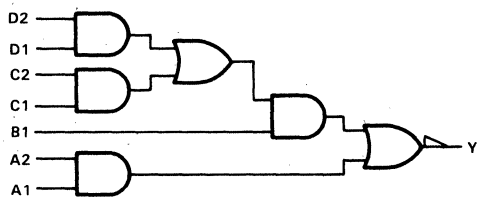
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS							OUTPUT
A1	A2	B1	C1	C2	D1	D2	Y
H	H	X	X	X	X	X	L
X	X	H	H	H	X	X	L
X	X	H	X	X	H	H	L
Any other combination							H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1 \cdot A2) + \{B1 \cdot [(C1 \cdot C2) + (D1 \cdot D2)]\}}$

description

The BF035LJ cell is a expandable sum-of-products AND-OR-AND-NOR gate for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF035LJ A1,A2,B1,C1,C2,D1,D2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.23		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF035LJ
AND-OR-AND-NOR GATE
$Y = \overline{(A1 \cdot A2) + \{B1 \cdot [(C1 \cdot C2) + (D1 \cdot D2)]\}}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0,22	0.34	0.66	0.23	0.34	0.61	ns
t_{PHL}			0.17	0.32	0.5	0.17	0.32	0.48	
t_{PLH}	B1	Y	0.21	0.39	0.8	0.21	0.39	0.74	ns
t_{PHL}			0.26	0.46	0.78	0.27	0.46	0.72	
t_{PLH}	Any C	Y	0.26	0.79	2.01	0.27	0.79	1.83	ns
t_{PHL}			0.25	0.62	1.38	0.26	0.62	1.23	
t_{PLH}	Any D	Y	0.27	0.67	1.62	0.28	0.67	1.49	ns
t_{PHL}			0.22	0.53	1.12	0.22	0.53	1.01	
Δt_{PLH}	Any A	Y	0.51	1.49	3.23	0.54	1.49	3.05	ns/pF
Δt_{PHL}			0.36	0.88	1.92	0.39	0.88	1.72	
Δt_{PLH}	B1	Y	0.5	1.46	3.23	0.53	1.46	2.97	ns/pF
Δt_{PHL}			0.35	0.85	1.91	0.37	0.85	1.71	
Δt_{PLH}	Any C	Y	0.67	2.02	4.48	0.72	2.02	4.12	ns/pF
Δt_{PHL}			0.43	1.25	2.86	0.47	1.25	2.58	
Δt_{PLH}	Any D	Y	0.66	2.02	4.5	0.71	2.02	4.14	ns/pF
Δt_{PHL}			0.42	1.2	2.75	0.46	1.2	2.47	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF051LJ
OR-NAND GATE
$Y = \overline{A1 \cdot (B1 + B2)}$

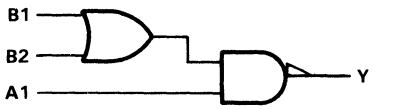
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A1	B1	B2	Y
H	H	X	L
H	X	H	L
L	X	X	H
X	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot (B1 + B2)}$

description

The BF051LJ cell is an expandable 2-wide, 1-2-input OR-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF051LJ A1,B1,B2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.21		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	0.21	0.27	0.41	0.21	0.27	0.39	ns
t_{PHL}			0.22	0.38	0.6	0.24	0.38	0.57	
t_{PLH}	Any B	Y	0.22	0.46	1.08	0.22	0.46	0.97	ns
t_{PHL}			0.16	0.31	0.59	0.17	0.31	0.55	
Δt_{PLH}	A1	Y	0.4	1.09	2.31	0.43	1.09	2.12	ns/pF
Δt_{PHL}			0.38	0.9	1.99	0.4	0.9	1.79	
Δt_{PLH}	Any B	Y	0.69	2.08	4.58	0.74	2.08	4.21	ns/pF
Δt_{PHL}			0.37	0.91	2	0.4	0.91	1.79	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF052LJ
OR-NAND GATE
$Y = \overline{A1 \cdot (B1 + B2 + B3)}$

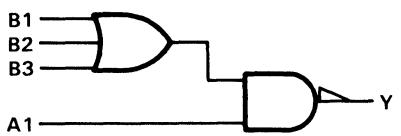
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A1	B1	B2	B3	Y
H	H	X	X	L
H	X	H	X	L
H	X	X	H	L
L	X	X	X	H
X	L	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot (B1 + B2 + B3)}$

description

The BF052LJ cell is an expandable 2-wide, 1-3-input OR-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF052LJ A1,B1,B2,B3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.22		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A1	Y	0.21	0.27	0.4	0.21	0.27	0.38	ns
t_{PHL}			0.25	0.41	0.66	0.26	0.41	0.62	
t_{PLH}	Any B	Y	0.25	0.65	1.78	0.26	0.65	1.62	ns
t_{PHL}			0.16	0.33	0.66	0.16	0.33	0.61	
Δt_{PLH}	A1	Y	0.4	1.09	2.31	0.43	1.09	2.13	ns/pF
Δt_{PHL}			0.38	0.92	2.04	0.4	0.92	1.83	
Δt_{PLH}	Any B	Y	1	3.08	6.87	1.07	3.08	6.32	ns/pF
Δt_{PHL}			0.38	0.92	2.04	0.4	0.92	1.83	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF053LJ
OR-NAND GATE
$Y = \overline{(A1 + A2)\cdot(B1 + B2)}$

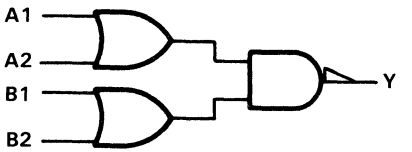
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A1	A2	B1	B2	Y
H	X	H	X	L
H	X	X	H	L
X	H	H	X	L
X	H	X	H	L
L	L	X	X	H
X	X	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1+A2)\cdot(B1+B2)}$

description

The BF053LJ cell is a 2-wide, 2-input OR-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF053LJ A1,A2,B1,B2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.21		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	0.23	0.52	1.21	0.24	0.52	1.09	ns
t_{PHL}			0.17	0.33	0.63	0.18	0.33	0.58	
t_{PLH}	Any B	Y	0.2	0.37	0.83	0.21	0.37	0.74	ns
t_{PHL}			0.21	0.42	0.73	0.22	0.42	0.68	
Δt_{PLH}	Any A	Y	0.7	2.08	4.58	0.75	2.08	4.21	ns/pF
Δt_{PHL}			0.37	0.92	1.99	0.4	0.92	1.79	
Δt_{PLH}	Any B	Y	0.7	2.11	4.59	0.75	2.11	4.24	ns/pF
Δt_{PHL}			0.38	0.91	1.99	0.4	0.91	1.8	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF054LJ
OR-NAND GATE
$Y = \overline{(A1 + A2)\cdot(B1 + B2 + B3)}$

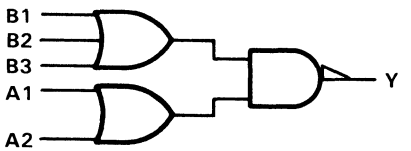
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A1	A2	B1	B2	B3	Y
H	X	H	X	X	L
H	X	X	H	X	L
H	X	X	X	H	L
X	H	H	X	X	L
X	H	X	H	X	L
X	H	X	X	H	L
Any other combination					H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1+A2)\cdot(B1+B2+B3)}$

description

The BF054LJ cell is a 2-wide, 2-3-input OR-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF054LJ A1,A2,B1,B2,B3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.21		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	0.21	0.37	0.8	0.21	0.37	0.73	ns
t_{PHL}			0.23	0.45	0.8	0.25	0.45	0.74	
t_{PLH}	Any B	Y	0.27	0.74	1.99	0.28	0.74	1.81	ns
t_{PHL}			0.17	0.45	0.69	0.18	0.45	0.64	
Δt_{PLH}	Any A	Y	0.71	2.11	4.63	0.76	2.11	4.25	ns/pF
Δt_{PHL}			0.37	0.92	2.05	0.39	0.92	1.84	
Δt_{PLH}	Any B	Y	1	3.09	6.86	1.08	3.09	6.31	ns/pF
Δt_{PHL}			0.38	0.92	2.04	0.4	0.92	1.83	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF055LJ
OR-NAND GATE

$$Y = \overline{(A1 + A2 + A3) \cdot (B1 + B2 + B3)}$$

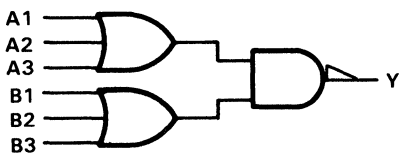
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	A3	B1	B2	B3	Y
H	X	X	H	X	X	L
H	X	X	X	H	X	L
H	X	X	X	X	H	L
X	H	X	H	X	X	L
X	H	X	X	H	X	L
X	H	X	X	X	H	L
X	X	H	H	X	X	L
X	X	H	X	H	H	L
X	X	H	X	X	H	L
Any other combination						H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1+A2+A3)\cdot(B1+B2+B3)}$

description

The BF055LJ cell is a 2-wide, 3-input OR-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF055LJ A1,A2,A3,B1,B2,B3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.23		pF

BF055LJ
OR-NAND GATE
$Y = \overline{(A1 + A2 + A3) \cdot (B1 + B2 + B3)}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.29	0.82	2.17	0.3	0.82	1.98	ns
t_{PHL}			0.18	0.37	0.73	0.19	0.37	0.67	
t_{PLH}	Any B	Y	0.25	0.55	1.47	0.25	0.55	1.33	ns
t_{PHL}			0.23	0.47	0.9	0.25	0.47	0.83	
Δt_{PLH}	Any A	Y	1.01	3.08	6.88	1.08	3.08	6.31	ns/pF
Δt_{PHL}			0.38	0.92	2.04	0.4	0.92	1.83	
Δt_{PLH}	Any B	Y	1.03	3.13	6.95	1.11	3.13	6.39	ns/pF
Δt_{PHL}			0.36	0.93	2.08	0.39	0.93	1.87	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF056LJ
OR-NAND GATE
$Y = \overline{A1 \cdot A2 \cdot (B1 + B2)}$

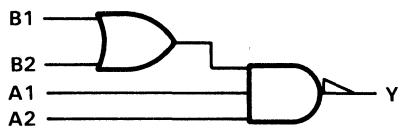
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A1	A2	B1	B2	Y
H	H	H	X	L
H	H	X	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot A2 \cdot (B1 + B2)}$

description

The BF056LJ cell is an expandable 3-wide, 1-1-2-input OR-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF056LJ A1,A2,B1,B2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.22		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	0.2	0.32	0.58	0.21	0.32	0.55	ns
t_{PHL}			0.25	0.45	0.83	0.25	0.45	0.76	
t_{PLH}	Any B	Y	0.24	0.59	1.39	0.25	0.59	1.28	ns
t_{PHL}			0.18	0.38	0.87	0.18	0.38	0.79	
Δt_{PLH}	Any A	Y	0.4	1.09	2.32	0.43	1.09	2.13	ns/pF
Δt_{PHL}			0.43	1.24	2.84	0.46	1.24	2.55	
Δt_{PLH}	Any B	Y	0.7	2.09	4.59	0.75	2.09	4.23	ns/pF
Δt_{PHL}			0.43	0.38	2.84	0.46	0.38	2.55	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF057LJ
OR-NAND GATE
$Y = \overline{A1 \cdot A2 \cdot (B1 + B2 + B3)}$

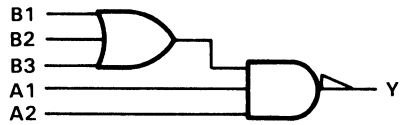
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A1	A2	B1	B2	B3	Y
H	H	H	X	X	L
H	H	X	H	X	L
H	H	X	X	H	L
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot A2 \cdot (B1 + B2 + B3)}$

description

The BF057LJ cell is an expandable 3-wide, 1-1-3-input OR-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF057LJ A1,A2,B1,B2,B3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.23		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any A	Y	0.21	0.32	0.58	0.21	0.32	0.55	ns
t_{PHL}			0.27	0.5	0.92	0.27	0.5	0.88	
t_{PLH}	Any B	Y	0.28	0.85	2.33	0.29	0.85	2.12	ns
t_{PHL}			0.17	0.42	1.01	0.18	0.42	0.91	
Δt_{PLH}	Any A	Y	0.4	1.09	2.31	0.43	1.09	2.13	ns/pF
Δt_{PHL}			0.42	1.26	2.89	0.46	1.26	2.6	
Δt_{PLH}	Any B	Y	1.01	3.09	6.88	1.09	3.09	6.32	ns/pF
Δt_{PHL}			0.43	1.24	2.89	0.47	1.24	2.59	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF058LJ
OR-NAND GATE
$Y = \overline{A1 \cdot (B1 + B2) \cdot (C1 + C2)}$

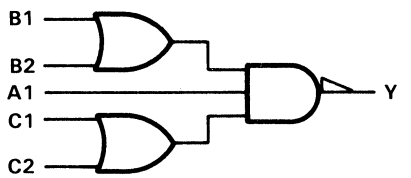
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A1	B1	B2	C1	C2	Y
H	H	X	H	X	L
H	H	X	X	H	L
H	X	H	H	X	L
H	X	H	X	H	L
L	X	X	X	X	H
X	L	L	X	X	H
X	X	X	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot (B1 + B2) \cdot (C1 + C2)}$

description

The BF058LJ cell is a 3-wide, 1-2-2-input OR-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF058LJ A1,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.25		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF058LJ
OR-NAND GATE
$Y = \overline{A1 \cdot (B1 + B2) \cdot (C1 + C2)}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.23	0.39	0.67	0.24	0.39	0.62	ns
t_{PHL}			0.28	0.53	1.08	0.28	0.53	0.99	
t_{PLH}	Any B	Y	0.27	0.67	1.57	0.28	0.67	1.43	ns
t_{PHL}			0.2	0.48	1.13	0.21	0.48	1.02	
t_{PLH}	Any C	Y	0.2	0.41	0.94	0.2	0.41	0.84	ns
t_{PHL}			0.27	0.49	0.99	0.27	0.49	0.9	
Δt_{PLH}	A1	Y	0.41	1.09	2.3	0.44	1.09	2.12	ns/pF
Δt_{PHL}			0.43	1.24	2.85	0.47	1.24	2.56	
Δt_{PLH}	Any B	Y	0.71	2.1	4.6	0.76	2.1	4.24	ns/pF
Δt_{PHL}			0.43	1.24	2.84	0.47	1.24	2.55	
Δt_{PLH}	Any C	Y	0.71	2.11	4.61	0.76	2.11	4.25	ns/pF
Δt_{PHL}			0.43	1.24	2.84	0.46	1.24	2.56	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF059LJ
OR-NAND GATE
$Y = \overline{A1 \cdot (B1 + B2) \cdot (C1 + C2 + C3)}$

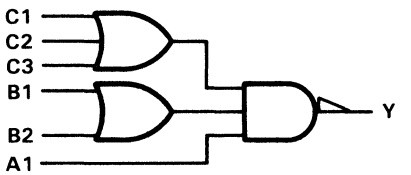
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS						OUTPUT
A1	B1	B2	C1	C2	C3	Y
H	H	X	H	X	X	L
H	H	X	X	H	X	L
H	H	X	X	X	H	L
H	X	H	H	X	X	L
H	X	H	X	H	X	L
H	X	H	X	X	H	L
L	X	X	X	X	X	H
X	L	L	X	X	X	H
X	X	X	L	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot (B1 + B2) \cdot (C1 + C2 + C3)}$

description

The BF059LJ cell is a 3-wide, 1-2-3-input OR-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF059LJ A1,B1,B2,C1,C2,C3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.25		pF

BF059LJ
OR-NAND GATE
$Y = \overline{A1 \cdot (B1 + B2) \cdot (C1 + C2 + C3)}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.21	0.29	0.46	0.21	0.29	0.44	ns
t_{PHL}			0.28	0.45	0.77	0.29	0.45	0.72	
t_{PLH}	Any B	Y	0.27	0.69	1.67	0.28	0.69	1.51	ns
t_{PHL}			0.19	0.42	0.96	0.2	0.42	0.87	
t_{PLH}	Any C	Y	0.28	0.78	2.05	0.29	0.78	1.87	ns
t_{PHL}			0.23	0.52	1.19	0.24	0.52	1.08	
Δt_{PLH}	A1	Y	0.4	1.09	2.32	0.43	1.09	2.13	ns/pF
Δt_{PHL}			0.43	1.23	2.83	0.46	1.23	2.55	
Δt_{PLH}	Any B	Y	0.7	2.09	4.6	0.75	2.09	4.23	ns/pF
Δt_{PHL}			0.43	1.24	2.83	0.47	1.24	2.55	
Δt_{PLH}	Any C	Y	1.02	3.12	6.93	1.09	3.12	6.37	ns/pF
Δt_{PHL}			0.44	1.25	2.89	0.48	1.25	2.6	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF060LJ
OR-NAND GATE

$$Y = \overline{A1 \cdot (B1 + B2 + B3) \cdot (C1 + C2 + C3)}$$

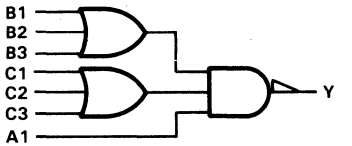
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS							OUTPUT
A1	B1	B2	B3	C1	C2	C3	Y
H	H	X	X	H	X	X	L
H	X	H	X	X	H	X	L
H	X	X	H	X	X	H	L
H	(Any H)			(Any H)			L
Any other combination							H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot (B1+B2+B3) \cdot (C1+C2+C3)}$

description

The BF060LJ cell is a 3-wide, 1-3-3-input OR-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF060LJ A1,B1,B2,B3,C1,C2,C3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.25		pF

BF060LJ
OR-NAND GATE

$$Y = \overline{A1 \cdot (B1 + B2 + B3) \cdot (C1 + C2 + C3)}$$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.21	0.29	0.45	0.21	0.29	0.43	ns
t_{PHL}			0.3	0.5	0.89	0.31	0.5	0.82	
t_{PLH}	Any B	Y	0.32	1.01	2.7	0.34	1.01	2.45	ns
t_{PHL}			0.19	0.45	1.08	0.19	0.45	0.98	
t_{PLH}	Any C	Y	0.28	0.77	2.05	0.29	0.77	1.87	ns
t_{PHL}			0.25	0.57	1.35	0.26	0.57	1.21	
Δt_{PLH}	A1	Y	0.4	1.09	2.32	0.43	1.09	2.13	ns/pF
Δt_{PHL}			0.42	1.25	2.89	0.46	1.25	2.59	
Δt_{PLH}	Any B	Y	1.02	3.1	6.88	1.09	3.1	6.33	ns/pF
Δt_{PHL}			0.43	1.25	2.85	0.47	1.25	2.59	
Δt_{PLH}	Any C	Y	1.04	3.13	6.93	1.12	3.13	6.36	ns/pF
Δt_{PHL}			0.44	1.27	2.92	0.48	1.27	2.63	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF062LJ
OR-NAND GATE

$$Y = \overline{(A1 + A2)\cdot(B1 + B2)\cdot(C1 + C2 + C3)}$$

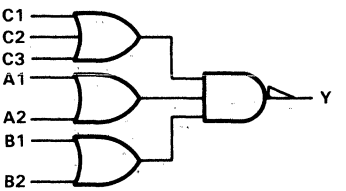
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS							OUTPUT
A1	A2	B1	B2	C1	C2	C3	Y
H	X	H	X	H	X	X	L
X	H	X	H	X	H	X	L
H	X	H	X	X	X	H	L
(Any H)		(Any H)		(Any H)			L
Any other combination							H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1+A2)\cdot(B1+B2)\cdot(C1+C2+C3)}$

description

The BF062LJ cell is a 3-wide, 2-3-3-input OR-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF062LJ A1,A2,B1,B2,C1,C2,C3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.27		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF062LJ
OR-NAND GATE

$$Y = \overline{(A1 + A2)\cdot(B1 + B2)\cdot(C1 + C2 + C3)}$$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.31	0.78	1.85	0.32	0.78	1.67	ns
t_{PHL}			0.22	0.52	1.2	0.22	0.52	1.09	
t_{PLH}	Any B	Y	0.2	0.42	0.95	0.2	0.42	0.85	ns
t_{PHL}			0.27	0.49	0.97	0.27	0.49	0.89	
t_{PLH}	Any C	Y	0.35	0.92	2.36	0.37	0.92	2.11	ns
t_{PHL}			0.27	0.62	1.46	0.28	0.62	1.32	
Δt_{PLH}	Any A	Y	0.71	2.1	4.6	0.76	2.1	4.23	ns/pF
Δt_{PHL}			0.43	1.24	2.85	0.47	1.24	2.56	
Δt_{PLH}	Any B	Y	0.71	2.1	4.61	0.76	2.1	4.25	ns/pF
Δt_{PHL}			0.43	1.24	2.84	0.46	1.24	2.55	
Δt_{PLH}	Any C	Y	1.01	3.13	6.92	1.09	3.13	6.39	ns/pF
Δt_{PHL}			0.44	1.25	2.89	0.48	1.25	2.59	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF063LJ
OR-NAND GATE

$$Y = \overline{(A1 + A2)\cdot(B1 + B2 + B3)\cdot(C1 + C2 + C3)}$$

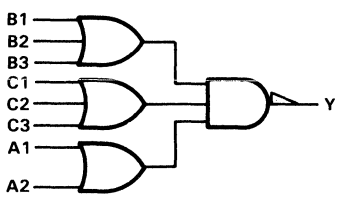
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS								OUTPUT
A1	A2	B1	B2	B3	C1	C2	C3	Y
H	X	H	X	X	H	X	X	L
X	H	X	H	X	X	H	X	L
H	X	X	X	H	X	X	H	L
(Any H)		(Any H)			(Any H)			L
Any other combination								H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1+A2)\cdot(B1+B2+B3)\cdot(C1+C2+C3)}$

description

The BF063LJ cell is a 3-wide, 2-3-3-input OR-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF063LJ A1,A2,B1,B2,B3,C1,C2,C3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.27		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF063LJ
OR-NAND GATE

$$Y = \overline{(A1 + A2)\cdot(B1 + B2 + B3)\cdot(C1 + C2 + C3)}$$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.2	0.42	0.93	0.21	0.42	0.84	ns
t_{PHL}			0.29	0.54	1.11	0.3	0.54	1.01	
t_{PLH}	Any B	Y	0.37	1.13	2.98	0.39	1.13	2.69	ns
t_{PHL}			0.21	0.55	1.34	0.22	0.55	1.2	
t_{PLH}	Any C	Y	0.33	0.91	2.36	0.34	0.91	2.11	ns
t_{PHL}			0.28	0.68	1.62	0.3	0.68	1.46	
Δt_{PLH}	Any A	Y	0.72	2.11	4.62	0.77	2.11	4.25	ns/pF
Δt_{PHL}			0.43	1.26	2.89	0.46	1.26	2.6	
Δt_{PLH}	Any B	Y	1.03	3.11	6.87	1.1	3.11	6.33	ns/pF
Δt_{PHL}			0.44	1.25	2.89	0.47	1.25	2.6	
Δt_{PLH}	Any C	Y	1.03	3.14	6.92	1.11	3.14	6.38	ns/pF
Δt_{PHL}			0.44	1.26	2.92	0.48	1.26	2.63	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF064LJ
OR-NAND GATE

$$Y = \overline{(A1 + A2 + A3)\cdot(B1 + B2 + B3)\cdot(C1 + C2 + C3)}$$

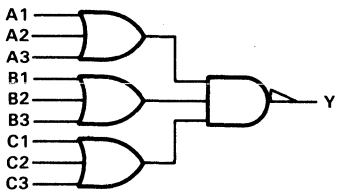
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS									OUTPUT
A1	A2	A3	B1	B2	B3	C1	C2	C3	Y
H	X	X	H	X	X	H	X	X	L
X	H	X	X	H	X	X	H	X	L
X	X	H	X	X	H	X	X	H	L
(Any H)			(Any H)			(Any H)			L
Any other combination									H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1+A2+A3)\cdot(B1+B2+B3)\cdot(C1+C2+C3)}$

description

The BF064LJ cell is a 3-wide, 3-input OR-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF064LJ A1,A2,A3,B1,B2,B3,C1,C2,C3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.31		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF064LJ
OR-NAND GATE

$$Y = \overline{(A1 + A2 + A3) \cdot (B1 + B2 + B3) \cdot (C1 + C2 + C3}$$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.4	1.22	3.15	0.42	1.22	2.85	ns
t_{PHL}			0.24	0.63	1.55	0.25	0.63	1.4	
t_{PLH}	Any B	Y	0.37	0.99	2.55	0.39	0.99	2.31	ns
t_{PHL}			0.31	0.76	1.85	0.32	0.76	1.66	
t_{PLH}	Any C	Y	0.26	0.65	1.71	0.26	0.65	1.55	ns
t_{PHL}			0.29	0.59	1.31	0.3	0.59	1.18	
Δt_{PLH}	Any A	Y	1.04	3.12	6.92	1.12	3.12	6.35	ns/pF
Δt_{PHL}			0.44	1.26	2.92	0.47	1.26	2.62	
Δt_{PLH}	Any B	Y	1.06	3.16	6.95	1.14	3.16	6.38	ns/pF
Δt_{PHL}			0.45	1.28	2.94	0.48	1.28	2.65	
Δt_{PLH}	Any C	Y	1.04	3.14	6.94	1.12	3.14	6.37	ns/pF
Δt_{PHL}			0.43	1.26	2.92	0.47	1.26	2.62	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF065LJ
AND-OR-NAND GATE
$Y = \overline{A1 \cdot [B1 + (C1 \cdot C2)]}$

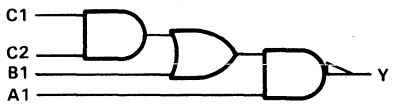
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A1	B1	C1	C2	Y
H	H	X	X	L
H	X	H	H	L
L	X	X	X	H
X	L	L	X	H
X	L	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot [B1 + (C1 \cdot C2)]}$

description

The BF065LJ cell is a 2-input sum-of-products NAND gate with a dedicated 2-input OR, 2-input AND product term. One available input to the 2-input OR gate and one available input to the 2-input NAND gate provides expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF065LJ A1,B1,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f = 1$ ns	0.22		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF065LJ
AND-OR-NAND GATE
$Y = \overline{A1 \cdot [B1 + (C1 \cdot C2)]}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.2	0.27	0.41	0.2	0.27	0.39	ns
t_{PHL}			0.28	0.44	0.76	0.29	0.44	0.7	
t_{PLH}	B1	Y	0.28	0.45	0.87	0.28	0.45	0.81	ns
t_{PHL}			0.16	0.29	0.49	0.17	0.29	0.46	
t_{PLH}	Any C	Y	0.21	0.56	1.45	0.22	0.56	1.31	ns
t_{PHL}			0.19	0.42	0.85	0.2	0.42	0.78	
Δt_{PLH}	A1	Y	0.4	1.1	2.31	0.43	1.1	2.13	ns/pF
Δt_{PHL}			0.43	1.24	2.85	0.46	1.24	2.56	
Δt_{PLH}	B1	Y	0.69	2.07	4.58	0.74	2.07	4.21	ns/pF
Δt_{PHL}			0.38	0.91	1.97	0.41	0.91	1.78	
Δt_{PLH}	Any C	Y	0.71	2.11	4.54	0.77	2.11	4.2	ns/pF
Δt_{PHL}			0.43	1.25	2.85	0.47	1.25	2.56	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF066LJ
AND-OR-NAND GATE
$Y = \overline{A1 \cdot [(B1 \cdot B2) + (C1 \cdot C2)]}$

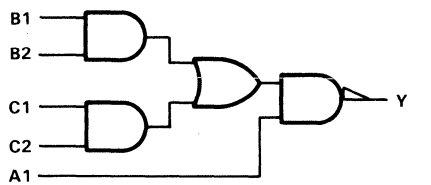
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A1	B1	B2	C1	C2	Y
H	H	H	X	X	L
H	X	X	H	H	L
Any other combination					H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot [(B1 \cdot B2) + (C1 \cdot C2)]}$

description

The BF066LJ cell is a 2-input sum-of-products NAND gate with a dedicated 2-wide, 2-input AND-OR product term. The available NAND input can be used to combine other custom product terms with the 2-wide, 2-input AND-OR term. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF066LJ A1,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.24		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF066LJ
AND-OR-NAND GATE
$Y = \overline{A1 \cdot [(B1 \cdot B2) + (C1 \cdot C2)]}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.22	0.3	0.48	0.22	0.3	0.45	ns
t_{PHL}			0.32	0.54	1.03	0.32	0.54	0.94	
t_{PLH}	Any B	Y	0.25	0.72	1.8	0.26	0.72	1.65	ns
t_{PHL}			0.21	0.51	1.09	0.22	0.51	0.97	
t_{PLH}	Any C	Y	0.28	0.61	1.43	0.28	0.61	1.31	ns
t_{PHL}			0.19	0.4	0.79	0.19	0.4	0.72	
Δt_{PLH}	A1	Y	0.4	1.1	2.32	0.43	1.1	2.13	ns/pF
Δt_{PHL}			0.42	1.24	2.86	0.46	1.24	2.57	
Δt_{PLH}	Any B	Y	0.71	2.1	4.6	0.77	2.1	4.23	ns/pF
Δt_{PHL}			0.44	1.25	2.85	0.47	1.25	2.57	
Δt_{PLH}	Any C	Y	0.7	2.09	4.6	0.75	2.09	4.23	ns/pF
Δt_{PHL}			0.43	1.24	2.8	0.47	1.24	2.53	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF067LJ
AND-OR-NAND GATE
$Y = \overline{A1 \cdot [B1 + B2 + (C1 \cdot C2)]}$

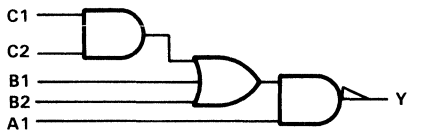
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A1	B1	B2	C1	C2	Y
H	H	X	X	X	L
H	X	H	X	X	L
H	X	X	H	H	L
L	X	X	X	X	H
X	L	L	L	X	H
X	L	L	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot [B1 + B2 + (C1 \cdot C2)]}$

description

The BF067LJ cell is a 2-input sum-of-products NAND gate with a dedicated 3-input OR, 2-input AND product term. Two available inputs to the 3-input OR gate and one available input to the 2-input NAND gate provides expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF067LJ A1,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.22		pF

BF067LJ
AND-OR-NAND GATE
$Y = \overline{A1 \cdot [B1 + B2 + (C1 \cdot C2)]}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.2	0.27	0.41	0.2	0.27	0.39	ns
t_{PHL}			0.3	0.48	0.85	0.3	0.48	0.78	
t_{PLH}	Any B	Y	0.31	0.76	1.97	0.32	0.76	1.79	ns
t_{PHL}			0.17	0.35	0.68	0.18	0.35	0.63	
t_{PLH}	Any C	Y	0.24	0.84	2.27	0.26	0.84	2.07	ns
t_{PHL}			0.18	0.45	0.94	0.19	0.45	0.85	
Δt_{PLH}	A1	Y	0.4	1.09	2.32	0.43	1.09	2.13	ns/pF
Δt_{PHL}			0.43	1.26	2.92	0.46	1.26	2.62	
Δt_{PLH}	Any B	Y	1.01	3.08	6.87	1.08	3.08	6.31	ns/pF
Δt_{PHL}			0.38	0.91	1.99	0.4	0.91	1.79	
Δt_{PLH}	Any C	Y	1.03	3.11	6.89	1.11	3.11	6.34	ns/pF
Δt_{PHL}			0.45	1.27	2.92	0.49	1.27	2.62	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF068LJ
AND-OR-NAND GATE
$Y = \overline{A1 \cdot [B1 + (C1 \cdot C2) + (D1 \cdot D2)]}$

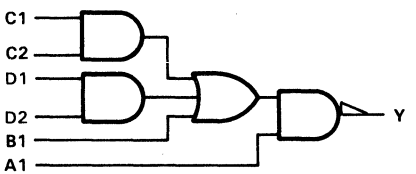
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS						OUTPUT
A1	B1	C1	C2	D1	D2	Y
H	H	X	X	X	X	L
H	X	H	H	X	X	L
H	X	X	X	H	H	L
L	X	X	X	X	X	H
X	L	L	X	L	X	H
X	L	X	L	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot [B1 + (C1 \cdot C2) + (D1 \cdot D2)]}$

description

The BF068LJ cell is a 2-input sum-of-products NAND gate with a dedicated 2-wide AND and 3-input OR product term. The available NAND and OR inputs can be used to combine other custom product terms with the 2-wide, 2-input AND-OR term. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF068LJ A1,B1,C1,C2,D1,D2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.22		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF068LJ
AND-OR-NAND GATE
$Y = \overline{A1 \cdot [B1 + (C1 \cdot C2) + (D1 \cdot D2)]}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.2	0.27	0.41	0.2	0.27	0.39	ns
t_{PHL}			0.32	0.52	0.95	0.33	0.52	0.87	
t_{PLH}	B1	Y	0.34	0.67	1.43	0.34	0.67	1.32	ns
t_{PHL}			0.17	0.33	0.55	0.18	0.33	0.53	
t_{PLH}	Any C	Y	0.27	0.93	2.46	0.28	0.93	2.23	ns
t_{PHL}			0.19	0.48	1	0.2	0.48	0.91	
t_{PLH}	Any D	Y	0.3	0.92	2.45	0.31	0.92	2.22	ns
t_{PHL}			0.19	0.47	0.96	0.2	0.47	0.87	
Δt_{PLH}	A1	Y	0.4	1.09	2.31	0.44	1.09	2.13	ns/pF
Δt_{PHL}			0.43	1.29	3	0.46	1.29	2.69	
Δt_{PLH}	B1	Y	1	3.07	6.88	1.08	3.07	6.32	ns/pF
Δt_{PHL}			0.38	0.91	1.99	0.4	0.91	1.78	
Δt_{PLH}	Any C	Y	1.04	3.11	6.86	1.12	3.11	6.32	ns/pF
Δt_{PHL}			0.46	1.29	2.97	0.49	1.29	2.67	
Δt_{PLH}	Any D	Y	1.03	3.11	6.88	1.11	3.11	6.33	ns/pF
Δt_{PHL}			0.44	1.24	2.85	0.48	1.24	2.56	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF069LJ
AND-OR-NAND GATE
$Y = A1 \cdot [(B1 \cdot B2) + (C1 \cdot C2) + (D1 \cdot D2)]$

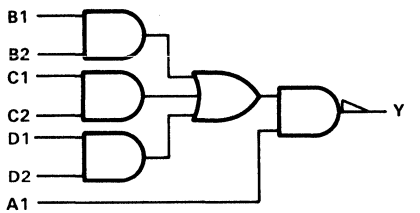
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS							OUTPUT
A1	B1	B2	C1	C2	D1	D2	Y
H	H	H	X	X	X	X	L
H	X	X	H	H	X	X	L
H	X	X	X	X	H	H	L
Any other combination							H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot [(B1 \cdot B2) + (C1 \cdot C2) + (D1 \cdot D2)]}$

description

The BF069LJ cell is a 2-input sum-of-products NAND gate with a dedicated 3-wide AND-OR product term. The available NAND can be used to combine other custom product terms with the 3-wide, 2-input AND-OR term. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF069LJ A1,B1,B2,C1,C2,D1,D2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.25		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF069LJ
AND-OR-NAND GATE
$Y = \overline{A1 \cdot [(B1 \cdot B2) + (C1 \cdot C2) + (D1 \cdot D2)]}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.22	0.3	0.48	0.22	0.3	0.45	ns
t_{PHL}			0.34	0.65	1.3	0.35	0.65	1.18	
t_{PLH}	Any B	Y	0.32	1.17	3.06	0.33	1.17	2.78	ns
t_{PHL}			0.23	0.56	1.19	0.24	0.56	1.07	
t_{PLH}	Any C	Y	0.35	1.17	3.05	0.37	1.17	2.77	ns
t_{PHL}			0.24	0.54	1.15	0.24	0.54	1.04	
t_{PLH}	Any D	Y	0.33	0.79	1.93	0.34	0.79	1.77	ns
t_{PHL}			0.19	0.41	0.79	0.2	0.41	0.73	
Δt_{PLH}	A1	Y	0.41	1.1	2.32	0.44	1.1	2.13	ns/pF
Δt_{PHL}			0.43	1.28	2.93	0.47	1.28	2.64	
Δt_{PLH}	Any B	Y	1.05	3.12	6.88	1.12	3.12	6.33	ns/pF
Δt_{PHL}			0.45	1.3	2.98	0.49	1.3	2.67	
Δt_{PLH}	Any C	Y	1.04	3.11	6.9	1.12	3.11	6.35	ns/pF
Δt_{PHL}			0.43	1.26	2.86	0.46	1.26	2.58	
Δt_{PLH}	Any D	Y	1.01	3.09	6.89	1.09	3.09	6.33	ns/pF
Δt_{PHL}			0.43	1.24	2.82	0.46	1.24	2.55	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF070LJ
AND-OR-NAND GATE
$Y = \overline{(A1 + A2)\cdot[B1 + (C1\cdot C2)]}$

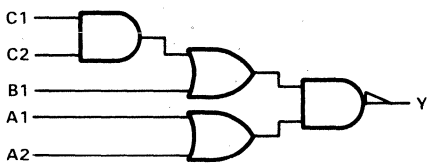
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A1	A2	B1	C1	C2	Y
H	X	H	X	X	L
X	H	H	X	X	L
H	X	X	H	H	L
X	H	X	H	H	L
L	L	X	X	X	H
X	X	L	L	X	H
X	X	L	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1+A2)\cdot[B1+(C1\cdot C2)]}$

description

The BF070LJ cell is a 2-wide 2-input sum-of-products OR-NAND gate with a dedicated 2-input OR product term. One available input to one 2-input OR gate and two available inputs to the other 2-input OR gate provide expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF070LJ A1,A2,B1,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.22		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF070LJ
AND-OR-NAND GATE
$Y = \overline{(A1 + A2) \cdot [B1 + (C1 \cdot C2)]}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.19	0.37	0.84	0.19	0.37	0.76	ns
t_{PHL}			0.27	0.49	0.96	0.27	0.49	0.89	
t_{PLH}	B1	Y	0.27	0.43	0.81	0.27	0.43	0.75	ns
t_{PHL}			0.18	0.31	0.51	0.19	0.31	0.49	
t_{PLH}	Any C	Y	0.23	0.6	1.58	0.23	0.6	1.44	ns
t_{PHL}			0.2	0.44	0.9	0.2	0.44	0.82	
Δt_{PLH}	Any A	Y	0.73	2.12	4.62	0.77	2.12	4.25	ns/pF
Δt_{PHL}			0.43	1.24	2.85	0.46	1.24	2.57	
Δt_{PLH}	B1	Y	0.53	1.56	3.43	.0.57	1.56	3.15	ns/pF
Δt_{PHL}			0.37	0.91	1.98	0.4	0.91	1.78	
Δt_{PLH}	Any C	Y	0.71	2.11	4.54	0.76	2.11	4.18	ns/pF
Δt_{PHL}			0.44	1.24	2.85	0.47	1.24	2.56	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF071LJ
AND-OR-NAND GATE
$Y = \overline{(A1 + A2)\cdot[(B1\cdot B2) + (C1\cdot C2)]}$

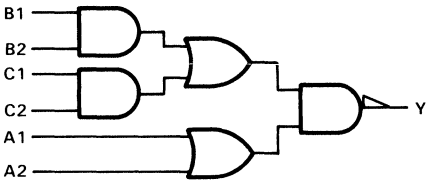
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	B1	B2	C1	C2	Y
H	X	H	H	X	X	L
X	H	H	H	X	X	L
H	X	X	X	H	H	L
X	H	X	X	H	H	L
Any other combination						H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1+A2)\cdot[(B1\cdot B2)+(C1\cdot C2)]}$

description

The BF071LJ cell is a 2-wide 2-input sum-of-products OR-NAND gate with a dedicated 2-wide, 2-input AND-OR product term. The available 2-input OR gate provides expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF071LJ A1,A2,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.25		pF

BF071LJ
AND-OR-NAND GATE
$Y = \overline{(A1 + A2)\cdot[(B1\cdot B2) + (C1\cdot C2)]}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.22	0.44	0.95	0.22	0.44	0.87	ns
t_{PHL}			0.3	0.57	1.22	0.3	0.57	1.1	
t_{PLH}	Any B	Y	0.26	0.74	1.88	0.27	0.74	1.71	ns
t_{PHL}			0.22	0.52	1.08	0.23	0.52	0.98	
t_{PLH}	Any C	Y	0.3	0.67	1.56	0.33	0.67	1.43	ns
t_{PHL}			0.2	0.42	0.82	0.2	0.42	0.76	
Δt_{PLH}	Any A	Y	0.72	2.12	4.65	0.77	2.12	4.27	ns/pF
Δt_{PHL}			0.43	1.24	2.8	0.46	1.24	2.53	
Δt_{PLH}	Any B	Y	0.71	2.1	4.6	0.77	2.1	4.23	ns/pF
Δt_{PHL}			0.44	1.25	2.84	0.47	1.25	2.56	
Δt_{PLH}	Any C	Y	0.7	2.09	4.6	0.75	2.09	4.23	ns/pF
Δt_{PHL}			0.43	1.24	2.81	0.47	1.24	2.53	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF072LJ
AND-OR-NAND GATE
$Y = \overline{(A1 + A2)\cdot[B1 + B2 + (C1\cdot C2)]}$

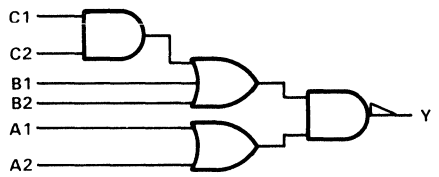
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	B1	B2	C1	C2	Y
H	X	H	X	X	X	L
X	H	H	X	X	X	L
H	X	X	H	X	X	L
X	H	X	H	X	X	L
H	X	X	X	H	H	L
X	H	X	X	H	H	L
L	L	X	X	X	X	H
X	X	L	L	L	X	H
X	X	L	L	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITION LOGIC EQUATION: $Y = \overline{(A1+A2)\cdot[B1+B2+(C1\cdot C2)]}$

description

The BF072LJ cell is a 2-wide, 2-3-input sum-of-products OR-NAND gate with a dedicated 2-input AND, 2-input OR product term. Two available inputs to the 3-input OR gate and two available inputs to the 2-input OR gate provide expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF072LJ A1,A2,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.22		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF072LJ
AND-OR-NAND GATE
$Y = \overline{(A1 + A2)\cdot[B1 + B2 + (C1\cdot C2)]}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.2	0.35	0.74	0.2	0.35	0.68	ns
t_{PHL}			0.16	0.35	0.52	0.17	0.35	0.51	
t_{PLH}	Any B	Y	0.29	0.69	1.7	0.3	0.69	1.55	ns
t_{PHL}			0.18	0.37	0.58	0.19	0.37	0.56	
t_{PLH}	Any C	Y	0.28	1	2.69	0.29	1	2.45	ns
t_{PHL}			0.21	0.45	0.86	0.22	0.45	0.79	
Δt_{PLH}	Any A	Y	0.66	2	4.41	0.71	2	4.05	ns/pF
Δt_{PHL}			0.36	0.69	1.45	0.37	0.69	1.3	
Δt_{PLH}	Any B	Y	0.84	2.55	5.67	0.9	2.55	5.21	ns/pF
Δt_{PHL}			0.34	0.67	1.46	0.35	0.67	1.31	
Δt_{PLH}	Any C	Y	1.01	3.08	6.82	1.09	3.08	6.28	ns/pF
Δt_{PHL}			0.37	1.03	2.38	0.39	1.03	2.13	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF075LJ
AND-OR-NAND GATE
$Y = \overline{(A1 + A2 + A3) \cdot [B1 + (C1 \cdot C2)]}$

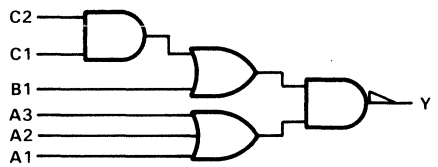
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	A3	B1	C1	C2	Y
H	X	X	H	X	X	L
X	H	X	H	X	X	L
X	X	H	H	X	X	L
(Any H)			X	H	H	L
L	L	L	X	X	X	H
X	X	X	L	L	X	H
X	X	X	L	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1+A2+A3)\cdot[B1+(C1\cdot C2)]}$

description

The BF075LJ cell is a 2-wide, 2-3-input sum-of-products OR-NAND gate with a dedicated 2-input AND, 2-input OR product term. One available input to the 2-input OR gate and three available inputs to the 3-input OR gate provide expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF075LJ A1,A2,A3,B1,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.23		pF

BF075LJ
AND-OR-NAND GATE
$Y = \overline{(A1 + A2 + A3) \cdot [B1 + (C1 \cdot C2)]}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.31	0.99	2.7	0.32	0.99	2.45	ns
t_{PHL}			0.19	0.39	0.69	0.21	0.39	0.65	
t_{PLH}	B1	Y	0.23	0.3	0.47	0.23	0.3	0.45	ns
t_{PHL}			0.17	0.33	0.46	0.19	0.33	0.45	
t_{PLH}	Any C	Y	0.19	0.43	1.07	0.2	0.43	0.99	ns
t_{PHL}			0.2	0.4	0.69	0.2	0.4	0.64	
Δt_{PLH}	Any A	Y	1	3.04	6.76	1.07	3.04	6.22	ns/pF
Δt_{PHL}			0.33	0.72	1.63	0.34	0.72	1.46	
Δt_{PLH}	B1	Y	0.49	1.42	3.13	0.52	1.42	2.88	ns/pF
Δt_{PHL}			0.37	0.68	1.43	0.38	0.68	1.28	
Δt_{PLH}	Any C	Y	0.63	1.93	4.28	0.68	1.93	3.94	ns/pF
Δt_{PHL}			0.37	0.96	2.15	0.4	0.96	1.93	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF080LJ
OR-AND-OR-NAND GATE
$Y = \overline{A1 \cdot \{B1 + [C1 \cdot (D1 + D2)]\}}$

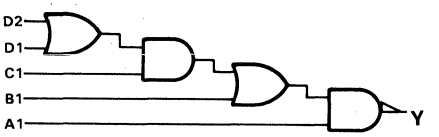
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A1	B1	C1	D1	D2	Y
H	H	X	X	X	L
H	X	H	H	X	L
H	X	H	X	H	L
Any other combination					H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot \{B1 + [C1 \cdot (D1 + D2)]\}}$

description

The BF080LJ cell is a 2-wide 1-2-input sum-of-products OR-NAND gate with a dedicated 2-input OR, and one available input each to the 2-input AND and OR gates to provide expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF080LJ A1,B1,C1,D1,D2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.23		pF

BF080LJ
OR-AND-OR-NAND GATE
$Y = \overline{A1 \cdot \{B1 + [C1 \cdot (D1 + D2)]\}}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.21	0.27	0.38	0.21	0.27	0.37	ns
t_{PHL}			0.18	0.32	0.43	0.19	0.32	0.42	
t_{PLH}	B1	Y	0.27	0.43	0.8	0.28	0.43	0.74	ns
t_{PHL}			0.16	0.29	0.48	0.17	0.29	0.46	
t_{PLH}	C1	Y	0.26	0.68	1.63	0.26	0.68	1.49	ns
t_{PHL}			0.21	0.42	0.83	0.21	0.42	0.76	
t_{PLH}	Any D	Y	0.25	0.78	1.98	0.25	0.78	1.8	ns
t_{PHL}			0.22	0.46	0.94	0.23	0.46	0.86	
Δt_{PLH}	A1	Y	0.38	1.02	2.19	0.4	1.02	2.02	ns/pF
Δt_{PHL}			0.35	0.71	1.53	0.37	0.71	1.37	
Δt_{PLH}	B1	Y	0.57	1.69	3.72	0.61	1.69	3.42	ns/pF
Δt_{PHL}			0.36	0.85	1.86	0.38	0.85	1.67	
Δt_{PLH}	C1	Y	0.69	2.05	4.48	0.74	2.05	4.12	ns/pF
Δt_{PHL}			0.38	1.01	2.3	0.4	1.01	2.06	
Δt_{PLH}	Any D	Y	1.02	3.09	6.84	1.1	3.09	6.29	ns/pF
Δt_{PHL}			0.43	1.21	2.81	0.46	1.21	2.52	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF081LJ
OR-AND-OR-NAND GATE
$Y = \overline{A1 \cdot \{B1 + [(C1 + C2) \cdot (D1 + D2)]\}}$

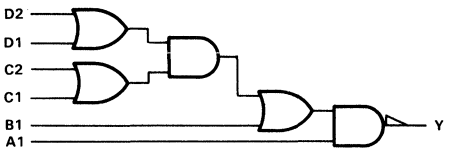
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS						OUTPUT
A1	B1	C1	C2	D1	D2	Y
H	H	X	X	X	X	L
H	X	H	X	H	X	L
H	X	H	X	X	H	L
H	X	X	H	H	X	L
H	X	X	H	X	H	L
Any other combination						H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot \{B1 + [(C1 + C2) \cdot (D1 + D2)]\}}$

description

The BF081LJ cell is a 2-wide 1-2-input sum-of-products OR-NAND gate with a dedicated 2-input OR, dual 2-input OR, and one available input to the 2-input OR gate to provide expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF081LJ A1,B1,C1,C2,D1,D2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.23		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF081LJ
OR-AND-OR-NAND GATE

$$Y = \overline{A1 \cdot \{B1 + [(C1 + C2) \cdot (D1 + D2)]\}}$$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.21	0.27	0.39	0.21	0.27	0.38	ns
t_{PHL}			0.18	0.33	0.44	0.2	0.33	0.43	
t_{PLH}	B1	Y	0.29	0.45	0.87	0.29	0.45	0.8	ns
t_{PHL}			0.16	0.3	0.51	0.17	0.3	0.47	
t_{PLH}	Any C	Y	0.31	1.07	2.77	0.32	1.07	2.49	ns
t_{PHL}			0.21	0.45	0.94	0.22	0.45	0.85	
t_{PLH}	Any D	Y	0.27	0.8	2	0.28	0.8	1.81	ns
t_{PHL}			0.21	0.43	0.85	0.22	0.43	0.78	
Δt_{PLH}	A1	Y	0.4	1.1	2.35	0.43	1.1	2.16	ns/pF
Δt_{PHL}			0.37	0.73	1.55	0.38	0.73	1.39	
Δt_{PLH}	B1	Y	0.65	1.99	4.43	0.7	1.99	4.07	ns/pF
Δt_{PHL}			0.37	0.9	1.95	0.4	0.9	1.75	
Δt_{PLH}	Any C	Y	1.01	3.05	6.75	1.09	3.05	6.20	ns/pF
Δt_{PHL}			0.39	1.08	2.46	0.42	1.08	2.22	
Δt_{PLH}	Any D	Y	1.01	3.05	6.78	1.09	3.05	6.23	ns/pF
Δt_{PHL}			0.4	1.09	2.5	0.43	1.09	2.25	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF082LJ
OR-AND-OR-NAND GATE
$Y = \overline{A1 \cdot \{(B1 \cdot B2) + [C1 \cdot (D1 + D2)]\}}$

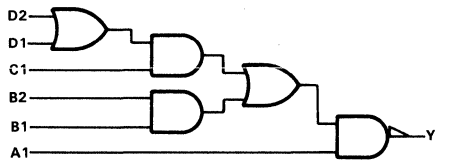
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS						OUTPUT
A1	B1	B2	C1	D1	D2	Y
H	H	H	X	X	X	L
H	X	X	H	H	X	L
H	X	X	H	X	H	L
Any other combination						H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A1 \cdot \{(B1 \cdot B2) + [C1 \cdot (D1 + D2)]\}}$

description

The BF082LJ cell is a 2-wide 1-2-input sum-of-products OR-NAND gate with a dedicated 2-input OR, 2-input AND, and one available input to the 2-input AND gate to provide expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF082LJ A1,B1,B2,C1,D1,D2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.26		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BF082LJ
OR-AND-OR-NAND GATE
$Y = \overline{A1 \cdot \{(B1 \cdot B2) + [C1 \cdot (D1 + D2)]\}}$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A1	Y	0.21	0.28	0.43	0.21	0.28	0.41	ns
t_{PHL}			0.21	0.36	0.52	0.23	0.36	0.5	
t_{PLH}	Any B	Y	0.26	0.48	1.04	0.26	0.48	0.96	ns
t_{PHL}			0.18	0.37	0.71	0.18	0.37	0.65	
t_{PLH}	C1	Y	0.24	0.5	1.12	0.24	0.5	1.02	ns
t_{PHL}			0.25	0.48	0.95	0.26	0.48	0.87	
t_{PLH}	Any D	Y	0.28	0.9	2.26	0.3	0.9	2.04	ns
t_{PHL}			0.21	0.54	1.28	0.22	0.54	1.15	
Δt_{PLH}	A1	Y	0.37	1.01	2.15	0.4	1.01	1.98	ns/pF
Δt_{PHL}			0.37	0.84	1.83	0.39	0.84	1.65	
Δt_{PLH}	Any B	Y	0.57	1.7	3.73	0.61	1.7	3.43	ns/pF
Δt_{PHL}			0.42	1.22	2.8	0.46	1.22	2.52	
Δt_{PLH}	C1	Y	0.53	1.56	3.37	0.57	1.56	3.12	ns/pF
Δt_{PHL}			0.39	1.07	2.42	0.42	1.07	2.18	
Δt_{PLH}	Any D	Y	0.84	2.54	5.60	0.9	2.54	5.17	ns/pF
Δt_{PHL}			0.44	1.25	2.88	0.47	1.25	2.59	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

BF088LJ
OR-AND-OR-NAND GATE

$$Y = \overline{(A1 + A2 + A3)\cdot\{B1 + [C1\cdot(D1 + D2)]\}}$$

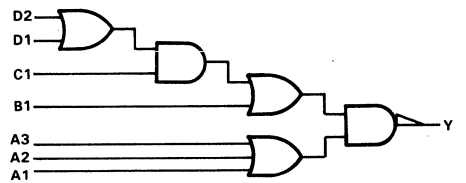
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS							OUTPUT
A1	A2	A3	B1	C1	D1	D2	Y
H	X	X	H	X	X	X	L
X	H	X	H	X	X	X	L
X	X	H	H	X	X	X	L
(Any H)			X	H	H	X	L
(Any H)			X	H	X	H	L
Any other combination							H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1+A2+A3)\cdot\{B1+[C1\cdot(D1+D2)]\}}$

description

The BF088LJ cell is a 2-wide 2-3-input sum-of-products OR-NAND gate with a dedicated 2-input OR, and one available input each to the 2-input AND and OR gates to provide expandability for implementing customized product terms. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: BF088LJ A1,A2,A3,B1,C1,D1,D2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.26		pF

BF088LJ
OR-AND-OR-NAND GATE

$$Y = \overline{(A1 + A2 + A3) \cdot \{B1 + [C1 \cdot (D1 + D2)]\}}$$

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A	Y	0.23	0.55	1.49	0.24	0.55	1.35	ns
t_{PHL}			0.17	0.37	0.62	0.19	0.37	0.58	
t_{PLH}	B1	Y	0.3	0.58	1.2	0.31	0.58	1.11	ns
t_{PHL}			0.19	0.38	0.55	0.2	0.38	0.53	
t_{PLH}	C1	Y	0.26	0.7	1.64	0.27	0.7	1.52	ns
t_{PHL}			0.24	0.45	0.74	0.25	0.45	0.69	
t_{PLH}	Any D	Y	0.35	1.27	3.27	0.37	1.27	2.97	ns
t_{PHL}			0.24	0.47	0.94	0.25	0.47	0.86	
Δt_{PLH}	Any A	Y	1.02	3.16	7.03	1.1	3.16	6.47	ns/pF
Δt_{PHL}			0.37	0.75	1.67	0.38	0.75	1.5	
Δt_{PLH}	B1	Y	0.54	1.6	3.52	0.58	1.6	3.24	ns/pF
Δt_{PHL}			0.34	0.59	1.24	0.35	0.59	1.11	
Δt_{PLH}	C1	Y	0.65	1.92	4.26	0.7	1.92	3.88	ns/pF
Δt_{PHL}			0.34	0.74	1.65	0.35	0.74	1.48	
Δt_{PLH}	Any D	Y	1	2.98	6.6	1.07	2.98	6.1	ns/pF
Δt_{PHL}			0.28	0.92	2.42	0.3	0.92	2.19	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

EN210LJ
2-INPUT EXCLUSIVE-NOR GATE

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A \oplus B} = \overline{\bar{A}B + A\bar{B}}$

description

The EN210LJ cell is a minimum-size, 2-input exclusive-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: EN210LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.17		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.52		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.23	0.47	1.08	0.23	0.47	0.98	ns
t_{PHL}			0.16	0.32	0.63	0.17	0.32	0.59	
Δt_{PLH}	A, B	Y	0.65	1.96	4.31	0.7	1.96	3.97	ns/pF
Δt_{PHL}			0.37	0.91	1.97	0.39	0.91	1.77	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

EX210LJ
2-INPUT EXCLUSIVE-OR GATE

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = A \oplus B = \overline{A} \cdot B + A \cdot \overline{B}$

description

The EX210LJ cell is a minimum-size, 2-input exclusive-OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: EX210LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.08		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.36		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.21	0.44	0.86	0.22	0.44	0.79	ns
t_{PHL}			0.13	0.54	1.3	0.16	0.54	1.19	
Δt_{PLH}	A, B	Y	0.4	1.09	2.3	0.44	1.09	2.12	ns/pF
Δt_{PHL}			0.4	0.88	1.86	0.4	0.88	1.68	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

EX220LJ
2-INPUT EXCLUSIVE-OR GATE WITH 2X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = A \oplus B = \overline{A} \cdot B + A \cdot \overline{B}$

description

The EX220LJ cell is a 2-input exclusive-OR gate featuring twice the capacitive-drive capability when compared to the EX210LJ exclusive-OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: EX220LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.08		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.53		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.02	0.51	0.99	0.2	0.51	0.93	ns
t_{PHL}			0.14	0.52	1.26	0.13	0.52	1.17	
Δt_{PLH}	A, B	Y	0.2	0.52	1.14	0.22	0.52	1.04	ns/pF
Δt_{PHL}			0.2	0.6	1.36	0.24	0.6	1.24	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

EX240LJ
2-INPUT EXCLUSIVE-OR GATE WITH 4X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = A \oplus B = \overline{A}\cdot B + A\cdot\overline{B}$

description

The EX240LJ cell is a 2-input exclusive-OR gate featuring four times the capacitive-drive capability when compared to the EX210LJ exclusive-OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: EX240LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.08		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.06		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.23	0.64	1.31	0.25	0.64	1.21	ns
t_{PHL}			0.14	0.63	1.48	0.15	0.63	1.38	
Δt_{PLH}	A, B	Y	0.12	0.28	0.64	0.12	0.28	0.58	ns/pF
Δt_{PHL}			0.12	0.4	1	0.14	0.4	0.9	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA210LJ
2-INPUT POSITIVE-NAND GATE

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A \cdot B} = \overline{A} + \overline{B}$

description

The NA210LJ cell is a minimum-size, 2-input positive-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA210LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.19		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.2	0.29	0.46	0.21	0.29	0.44	ns
t_{PHL}			0.21	0.32	0.49	0.22	0.32	0.46	
Δt_{PLH}	A, B	Y	0.38	1.14	2.66	0.4	1.14	2.46	ns/pF
Δt_{PHL}			0.4	0.99	2.2	0.42	0.99	1.98	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

NA220LJ
2-INPUT POSITIVE-NAND GATE WITH 2X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A \cdot B} = \overline{A} + \overline{B}$

description

The NA220LJ cell is a 2-input positive-NAND gate featuring twice the capacitive-drive capability when compared to the NA210LJ NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA220LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.12		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.38		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.16	0.27	0.42	0.16	0.27	0.4	ns
t_{PHL}			0.11	0.29	0.47	0.13	0.29	0.45	
Δt_{PLH}	A, B	Y	0.22	0.5	1.08	0.24	0.5	1	ns/pF
Δt_{PHL}			0.28	0.48	1.02	0.28	0.48	0.9	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA230LJ
2-INPUT POSITIVE-NAND GATE WITH 3X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A \cdot B} = \overline{A} + \overline{B}$

description

The NA230LJ cell is a 2-input positive-NAND gate featuring three times the capacitive-drive capability when compared to the NA210LJ NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA230LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.18		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.56		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.14	0.28	0.45	0.15	0.28	0.43	ns
t_{PHL}			0.1	0.27	0.46	0.11	0.27	0.42	
Δt_{PLH}	A, B	Y	0.18	0.35	0.76	0.18	0.35	0.7	ns/pF
Δt_{PHL}			0.18	0.34	0.68	0.2	0.34	0.62	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

NA240LJ
2-INPUT POSITIVE-NAND GATE WITH 4X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A \cdot B} = \overline{A} + \overline{B}$

description

The NA240LJ cell is a 2-input positive-NAND gate featuring four times the capacitive-drive capability when compared to the NA210LJ NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA240LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.25		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.78		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.14	0.25	0.44	0.14	0.25	0.42	ns
t_{PHL}			0.08	0.24	0.47	0.08	0.24	0.44	
Δt_{PLH}	A, B	Y	0.12	0.28	0.52	0.14	0.28	0.48	ns/pF
Δt_{PHL}			0.14	0.27	0.48	0.16	0.27	0.44	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA260LJ
2-INPUT POSITIVE-NAND GATE WITH 6X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A \cdot B} = \overline{A} + \overline{B}$

description

The NA260LJ cell is a 2-input positive-NAND gate featuring six times the capacitive-drive capability when compared to the NA210LJ NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA260LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.37		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.14		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.13	0.23	0.41	0.13	0.23	0.4	ns
t_{PHL}			0.08	0.22	0.45	0.09	0.22	0.43	
Δt_{PLH}	A, B	Y	0.08	0.02	0.36	0.08	0.2	0.32	ns/pF
Δt_{PHL}			0.12	0.22	0.36	0.12	0.22	0.3	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA310LJ
3-INPUT POSITIVE-NAND GATE

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A \cdot B \cdot C} = \overline{A} + \overline{B} + \overline{C}$

description

The NA310LJ cell is a minimum-size, 3-input positive-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA310LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.19		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C	Y	0.2	0.34	0.65	0.21	0.34	0.61	ns
t_{PHL}			0.21	0.35	0.68	0.23	0.35	0.63	
Δt_{PLH}	A, B, C	Y	0.42	1.29	3.26	0.44	1.29	3	ns/pF
Δt_{PHL}			0.46	1.32	3.04	0.48	1.32	2.74	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA320LJ
3-INPUT POSITIVE-NAND GATE WITH 2X OUTPUT

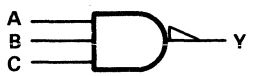
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A \cdot B \cdot C} = \overline{A} + \overline{B} + \overline{C}$

description

The NA320LJ cell is a 3-input positive-NAND gate featuring twice the capacitive-drive capability when compared to the NA310LJ NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA320LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.12		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.37		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C	Y	0.16	0.31	0.54	0.18	0.31	0.51	ns
t_{PHL}			0.15	0.33	0.59	0.17	0.33	0.55	
Δt_{PLH}	A, B, C	Y	0.22	0.55	1.24	0.24	0.55	1.14	ns/pF
Δt_{PHL}			0.26	0.61	1.42	0.26	0.61	1.28	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA330LJ
3-INPUT POSITIVE-NAND GATE WITH 3X OUTPUT

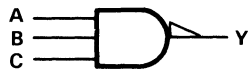
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A \cdot B \cdot C} = \overline{A} + \overline{B} + \overline{C}$

description

The NA330LJ cell is a 3-input positive-NAND gate featuring three times the capacitive-drive capability when compared to the NA310LJ NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA330LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.17		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.56		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C	Y	0.16	0.33	0.54	0.16	0.33	0.52	ns
t_{PHL}			0.12	0.33	0.6	0.14	0.33	0.55	
Δt_{PLH}	A, B, C	Y	0.18	0.36	0.82	0.18	0.36	0.74	ns/pF
Δt_{PHL}			0.22	0.42	0.94	0.22	0.42	0.84	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA340LJ
3-INPUT POSITIVE-NAND GATE WITH 4X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A \cdot B \cdot C} = \overline{A} + \overline{B} + \overline{C}$

description

The NA340LJ cell is a 3-input positive-NAND gate featuring four times the capacitive-drive capability when compared to the NA310LJ NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA340LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.23		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.74		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C	Y	0.15	0.32	0.55	0.16	0.32	0.53	ns
t_{PHL}			0.12	0.31	0.57	0.13	0.31	0.54	
Δt_{PLH}	A, B, C	Y	0.14	0.29	0.64	0.14	0.29	0.58	ns/pF
Δt_{PHL}			0.14	0.32	0.72	0.16	0.32	0.64	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

NA410LJ
4-INPUT POSITIVE-NAND GATE

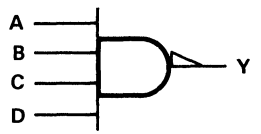
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
Any other combination				H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \cdot B \cdot C \cdot D} = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

description

The NA410LJ cell is a minimum-size, 4-input positive-AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA410LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.19		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C, D	Y	0.22	0.4	0.78	0.22	0.4	0.73	ns
t_{PHL}			0.21	0.4	0.93	0.22	0.4	0.85	
Δt_{PLH}	A, B, C, D	Y	0.4	1.45	3.96	0.44	1.45	3.64	ns/pF
Δt_{PHL}			0.52	1.64	3.84	0.56	1.64	3.46	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA420LJ
4-INPUT POSITIVE-NAND GATE WITH 2X OUTPUT

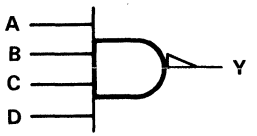
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
Any other combination				H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \cdot B \cdot C \cdot D} = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

description

The NA420LJ cell is a 4-input positive-NAND gate featuring twice the capacitive-drive capability when compared to the NA410LJ NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA420LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.12		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.39		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C, D	Y	0.21	0.37	0.68	0.21	0.37	0.64	ns
t_{PHL}			0.18	0.38	0.8	0.2	0.38	0.74	
Δt_{PLH}	A, B, C, D	Y	0.22	0.63	1.46	0.24	0.63	1.34	ns/pF
Δt_{PHL}			0.26	0.77	1.82	0.28	0.77	1.62	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

NA430LJ
4-INPUT POSITIVE-NAND GATE WITH 3X OUTPUT

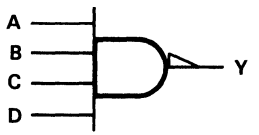
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
Any other combination				H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \cdot B \cdot C \cdot D} = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

description

The NA430LJ cell is a 4-input positive-AND gate featuring three times the capacitive-drive capability when compared to the NA410LJ NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA430LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.18		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.62		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C, D	Y	0.18	0.38	0.71	0.18	0.38	0.66	ns
t_{PHL}			0.15	0.39	0.81	0.17	0.39	0.75	
Δt_{PLH}	A, B, C, D	Y	0.18	0.41	1.02	0.18	0.41	0.94	ns/pF
Δt_{PHL}			0.2	0.52	1.24	0.2	0.52	1.1	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA510LJ
5-INPUT POSITIVE-NAND GATE

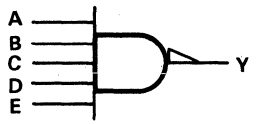
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
H	H	H	H	H	L
Any other combination					H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \cdot B \cdot C \cdot D \cdot E} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E}$

description

The NA510LJ cell is a minimum-size, 5-input positive-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA510LJ A,B,C,D,E,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.88		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C,D,E	Y	0.24	0.68	1.53	0.27	0.68	1.4	ns
t_{PHL}			0.34	1.01	2.35	0.36	1.01	2.12	
Δt_{PLH}	A,B,C,D,E	Y	0.36	0.91	1.92	0.38	0.91	1.76	ns/pF
Δt_{PHL}			0.24	0.54	1.12	0.24	0.54	1.02	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

NA520LJ
5-INPUT POSITIVE-NAND GATE WITH 2X OUTPUT

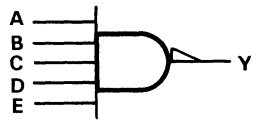
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
H	H	H	H	H	L
Any other combination					H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \cdot B \cdot C \cdot D \cdot E} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E}$

description

The NA520LJ cell is a 5-input positive-NAND gate featuring twice the capacitive-drive capability when compared to the NA510LJ NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA520LJ A,B,C,D,E,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.05		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C,D,E	Y	0.25	0.74	1.62	0.28	0.74	1.49	ns
t_{PHL}			0.35	1.11	2.63	0.37	1.11	2.39	
Δt_{PLH}	A,B,C,D,E	Y	0.16	0.45	0.96	0.18	0.45	0.88	ns/pF
Δt_{PHL}			0.14	0.35	0.76	0.16	0.35	0.68	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA810LJ
8-INPUT POSITIVE-NAND GATE

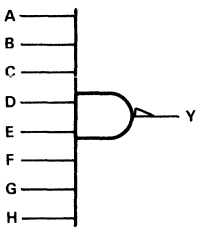
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
H	H	H	H	H	H	H	H	L
Any other combination								H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$

description

The NA810LJ cell is a minimum-size, 8-input positive-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA810LJ A,B,C,D,E,F,G,H,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.91		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A thru H	Y	0.24	0.8	1.76	0.26	0.8	1.63	ns
t_{PHL}			0.4	1.17	2.8	0.43	1.17	2.54	
Δt_{PLH}	A thru H	Y	0.34	0.92	1.92	0.36	0.92	1.76	ns/pF
Δt_{PHL}			0.24	0.55	1.14	0.26	0.55	1.02	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA820LJ
8-INPUT POSITIVE-NAND GATE WITH 2X OUTPUT

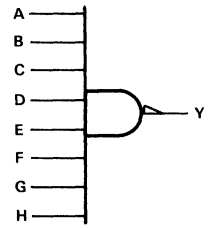
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
H	H	H	H	H	H	H	H	L
Any other combination								H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$

description

The NA820LJ cell is a 8-input positive-NAND gate featuring twice the capacitive-drive capability when compared to the NA810LJ NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NA820LJ A,B,C,D,E,F,G,H,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.31		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A thru H	Y	0.27	0.85	1.87	0.28	0.85	1.71	ns
t_{PHL}			0.42	1.27	3.1	0.44	1.27	2.8	
Δt_{PLH}	A thru H	Y	0.16	0.45	0.96	0.18	0.45	0.9	ns/pF
Δt_{PHL}			0.14	0.35	0.76	0.14	0.35	0.7	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NO210LJ
2-INPUT POSITIVE-NOR GATE

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A+B} = \overline{A} \cdot \overline{B}$

description

The NO210LJ cell is a minimum-size, 2-input positive-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO210LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.12		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.17	0.29	0.62	0.18	0.29	0.58	ns
t_{PHL}			0.22	0.37	0.53	0.23	0.37	0.5	
Δt_{PLH}	A, B	Y	0.7	2.07	4.6	0.74	2.07	4.22	ns/pF
Δt_{PHL}			0.42	1	2.38	0.44	1	2.14	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NO220LJ
2-INPUT POSITIVE-NOR GATE WITH 2X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A+B} = \overline{A} \cdot \overline{B}$

description

The NO220LJ cell is a 2-input positive-NOR gate featuring twice the capacitive-drive capability when compared to the NO210LJ NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO220LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.11		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.23		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.18	0.28	0.49	0.2	0.28	0.46	ns
t_{PHL}			0.15	0.34	0.51	0.15	0.34	0.5	
Δt_{PLH}	A, B	Y	0.34	0.98	2.22	0.34	0.98	2.04	ns/pF
Δt_{PHL}			0.3	0.46	0.9	0.32	0.46	0.8	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NO230LJ
2-INPUT POSITIVE-NOR GATE WITH 3X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A+B} = \overline{A} \cdot \overline{B}$

description

The NO230LJ cell is a 2-input positive-NOR gate featuring three times the capacitive-drive capability when compared to the NO210LJ NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO230LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.16		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.34		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.17	0.28	0.51	0.17	0.28	0.48	ns
t_{PHL}			0.08	0.3	0.5	0.11	0.3	0.49	
Δt_{PLH}	A, B	Y	0.22	0.66	1.48	0.24	0.66	1.38	ns/pF
Δt_{PHL}			0.26	0.37	0.7	0.26	0.37	0.62	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

NO240LJ
2-INPUT POSITIVE-NOR GATE WITH 4X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A+B} = \overline{A} \cdot \overline{B}$

description

The NO240LJ cell is a 2-input positive-NOR gate featuring four times the capacitive-drive capability when compared to the NO210LJ NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO240LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.22		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.44		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.17	0.29	0.49	0.17	0.29	0.45	ns
t_{PHL}			0.1	0.27	0.47	0.11	0.27	0.46	
Δt_{PLH}	A, B	Y	0.18	0.49	1.12	0.2	0.49	1.02	ns/pF
Δt_{PHL}			0.2	0.3	0.48	0.2	0.3	0.44	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NO310LJ
3-INPUT POSITIVE-NOR GATE

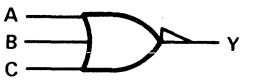
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A+B+C} = \overline{A}\cdot\overline{B}\cdot\overline{C}$

description

The NO310LJ cell is a minimum-size, 3-input positive-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO310LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.13		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C	Y	0.16	0.38	1.13	0.16	0.38	1.04	ns
t_{PHL}			0.3	0.43	0.68	0.3	0.43	0.65	
Δt_{PLH}	A, B, C	Y	1.02	3.07	6.82	1.08	3.07	6.28	ns/pF
Δt_{PHL}			0.46	1.29	3.3	0.5	1.29	2.96	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

NO320LJ
3-INPUT POSITIVE-NOR GATE WITH 2X OUTPUT

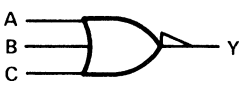
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A+B+C} = \overline{A}\cdot\overline{B}\cdot\overline{C}$

description

The NO320LJ cell is a 3-input positive-NOR gate featuring twice the capacitive-drive capability when compared to the NO310LJ NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO320LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.11		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.24		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C	Y	0.18	0.36	0.82	0.18	0.36	0.75	ns
t_{PHL}			0.2	0.41	0.63	0.23	0.41	0.6	
Δt_{PLH}	A, B, C	Y	0.48	1.47	3.3	0.5	1.47	3.04	ns/pF
Δt_{PHL}			0.34	0.61	1.28	0.36	0.61	1.14	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NO330LJ
3-INPUT POSITIVE-NOR GATE WITH 3X OUTPUT

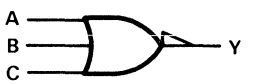
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A+B+C} = \overline{A} \cdot \overline{B} \cdot \overline{C}$

description

The NO330LJ cell is a 3-input positive-NOR gate featuring three times the capacitive-drive capability when compared to the NA310LJ NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO330LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.16		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.35		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C	Y	0.19	0.36	0.76	0.19	0.36	0.71	ns
t_{PHL}			0.19	0.38	0.59	0.19	0.38	0.57	
Δt_{PLH}	A, B, C	Y	0.32	1.01	2.28	0.34	1.01	2.1	ns/pF
Δt_{PHL}			0.24	0.42	0.86	0.26	0.42	0.76	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

NO410LJ
4-INPUT POSITIVE-NOR GATE

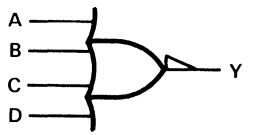
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	L	L	L	H
Any other combination				L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A+B+C+D} = \overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}$

description

The NO410LJ cell is a minimum-size, 4-input positive-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO410LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.14		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C, D	Y	0.17	0.52	1.79	0.17	0.52	1.62	ns
t_{PHL}			0.31	0.49	0.85	0.32	0.49	0.8	
Δt_{PLH}	A, B, C, D	Y	1.34	4.1	9.2	1.46	4.1	8.44	ns/pF
Δt_{PHL}			0.54	1.51	3.84	0.58	1.51	3.46	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NO420LJ
4-INPUT POSITIVE-NOR GATE WITH 2X OUTPUT

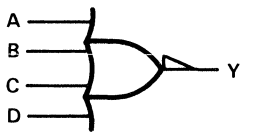
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	L	L	L	H
Any other combination				L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A+B+C+D} = \overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}$

description

The NO420LJ cell is a 4-input positive-NOR gate featuring twice the capacitive-drive capability when compared to the NA410LJ NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO420LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.1		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.24		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C, D	Y	0.19	0.47	1.19	0.2	0.47	1.1	ns
t_{PHL}			0.28	0.47	0.77	0.29	0.47	0.71	
Δt_{PLH}	A, B, C, D	Y	0.66	2.02	4.56	0.7	2.02	4.18	ns/pF
Δt_{PHL}			0.36	0.78	1.62	0.38	0.78	1.46	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NO510LJ
5-INPUT POSITIVE-NOR GATE

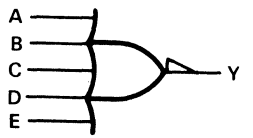
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
L	L	L	L	L	H
Any other combination					L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A+B+C+D+E} = \overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}\cdot\overline{E}$

description

The NO510LJ cell is a minimum-size, 5-input positive-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO510LJ A,B,C,D,E,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.7		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C,D,E	Y	0.28	0.96	2.77	0.28	0.96	2.5	ns
t_{PHL}			0.35	0.89	1.83	0.38	0.89	1.69	
Δt_{PLH}	A,B,C,D,E	Y	0.38	1.01	2.12	0.4	1.01	1.96	ns/pF
Δt_{PHL}			0.24	0.56	1.14	0.26	0.56	1.02	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NO520LJ
5-INPUT POSITIVE-NOR GATE WITH 2X OUTPUT

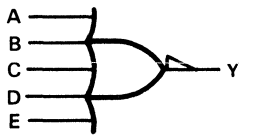
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
L	L	L	L	L	H
Any other combination					L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A+B+C+D+E} = \overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}\cdot\overline{E}$

description

The NO520LJ cell is a 5-input positive-NOR gate featuring twice the capacitive-drive capability when compared to the NO510LJ NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO520LJ A,B,C,D,E,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.81		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C,D,E	Y	0.33	1.05	3.02	0.34	1.05	2.73	ns
t_{PHL}			0.37	0.97	2.02	0.39	0.97	1.84	
Δt_{PLH}	A,B,C,D,E	Y	0.18	0.5	1.08	0.2	0.5	1	ns/pF
Δt_{PHL}			0.12	0.33	0.68	0.14	0.33	0.64	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

NO810LJ
8-INPUT POSITIVE-NOR GATE

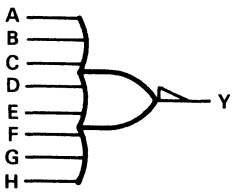
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
L	L	L	L	L	L	L	L	H
Any other combination								L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A+B+C+D+E+F+G+H} = \overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}\cdot\overline{E}\cdot\overline{F}\cdot\overline{G}\cdot\overline{H}$

description

The NO810LJ cell is a minimum-size, 8-input positive-NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO810LJ A,B,C,D,E,F,G,H,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.83		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A thru H	Y	0.39	1.29	3.7	0.42	1.29	3.36	ns
t_{PHL}			0.36	0.99	2.08	0.39	0.99	2	
Δt_{PLH}	A thru H	Y	0.38	1.01	2.12	0.42	1.01	1.98	ns/pF
Δt_{PHL}			0.26	0.55	1.14	0.28	0.55	1.02	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NO820LJ
8-INPUT POSITIVE-NOR GATE

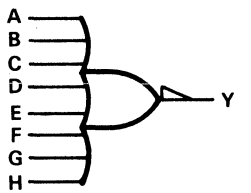
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
L	L	L	L	L	L	L	L	H
Any other combination								L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = \overline{A+B+C+D+E+F+G+H} = \overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}\cdot\overline{E}\cdot\overline{F}\cdot\overline{G}\cdot\overline{H}$

description

The NO820LJ cell is a 8-input positive-NOR gate featuring twice the capacitive-drive capability when compared to the NO810LJ NOR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: NO820LJ A,B,C,D,E,F,G,H,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.22		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A thru H	Y	0.43	1.39	3.99	0.45	1.39	3.6	ns
t_{PHL}			0.39	1.05	2.34	0.41	1.05	2.15	
Δt_{PLH}	A thru H	Y	0.18	0.51	1.1	0.2	0.51	1.02	ns/pF
Δt_{PHL}			0.12	0.33	0.7	0.14	0.33	0.62	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OA220LJ
2-WIDE, 2-INPUT OR-AND GATE WITH 2X OUTPUT
$Y = (A1 + A2)\cdot(B1 + B2)$

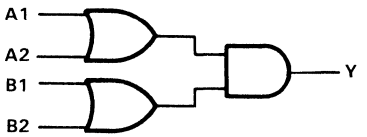
D3030, MARCH 1989

INTERNAL MACRO

FUNCTION TABLE

INPUTS				OUTPUT
A1	A2	B1	B2	Y
L	L	X	X	L
X	X	L	L	L
(Any H)		(Any H)		H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = (A1+A2)\cdot(B1+B2)$

description

The OA220LJ is a 2-wide, 2-input OR-AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OA220LJ A1,A2,B1,B2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.35		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	0.2	0.54	1.21	0.21	0.54	1.1	ns
t_{PHL}			0.34	0.95	2.41	0.37	0.95	2.18	
Δt_{PLH}	Any	Y	0.41	1.1	2.31	0.45	1.1	2.13	ns/pF
Δt_{PHL}			0.36	0.85	1.76	0.38	0.85	1.58	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OA230LJ
3-WIDE, 2-INPUT OR-AND GATE WITH 1X OUTPUT
$Y = (A1 + A2)\cdot(B1 + B2)\cdot(C1 + C2)$

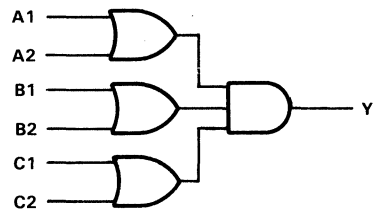
D3030, MARCH 1989

INTERNAL MACRO

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	B1	B2	C1	C2	Y
L	L	X	X	X	X	L
X	X	L	L	X	X	L
X	X	X	X	L	L	L
(Any H)		(Any H)		(Any H)		H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = (A1+A2)\cdot(B1+B2)\cdot(C1+C2)$

description

The OA230LJ is a 3-wide, 2-input OR-AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OA230LJ A1,A2,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.39		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	0.31	0.83	2.02	0.32	0.83	1.92	ns
t_{PHL}			0.36	1.15	3.19	0.38	1.15	2.89	
Δt_{PLH}	Any	Y	0.42	1.1	2.32	0.45	1.1	2.13	ns/pF
Δt_{PHL}			0.36	0.93	1.98	0.4	0.93	1.79	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OA231LJ
3-WIDE, 2-INPUT OR-NAND GATE WITH 1X OUTPUT
$Y = \overline{(A1+A2)\cdot(B1+B2)\cdot(C1+C2)}$

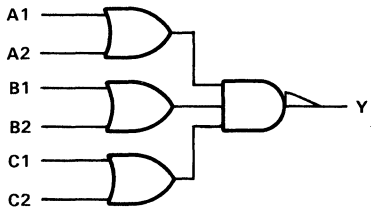
D3030, MARCH 1989

INTERNAL MACRO

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	B1	B2	C1	C2	Y
L	L	X	X	X	X	H
X	X	L	L	X	X	H
X	X	X	X	L	L	H
(Any H)		(Any H)		(Any H)		L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1+A2)\cdot(B1+B2)\cdot(C1+C2)}$

description

The OA231LJ is a 3-wide, 2-input OR-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OA231LJ A1,A2,B1,B2,C1,C2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.55		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	0.38	1.18	3.22	0.39	1.18	2.91	ns
t_{PHL}			0.38	1.05	2.51	0.39	1.05	2.27	
Δt_{PLH}	Any	Y	0.42	1.09	2.3	0.46	1.09	2.11	ns/pF
Δt_{PHL}			0.34	0.74	1.46	0.37	0.74	1.32	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OA240LJ
4-WIDE, 2-INPUT OR-AND GATE WITH 1X OUTPUT
$Y = (A1 + A2)\cdot(B1 + B2)\cdot(C1 + C2)\cdot(D1 + D2)$

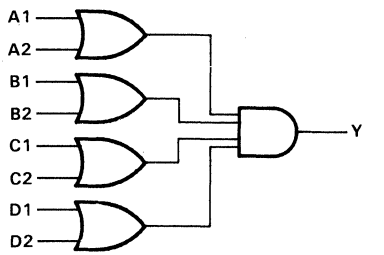
D3030, MARCH 1989

INTERNAL MACRO

FUNCTION TABLE

INPUTS								OUTPUT
A1	A2	B1	B2	C1	C2	D1	D2	Y
L	L	X	X	X	X	X	X	L
X	X	L	L	X	X	X	X	L
X	X	X	X	L	L	X	X	L
X	X	X	X	X	X	L	L	L
(Any H)		(Any H)		(Any H)		(Any H)		H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = (A1+A2)\cdot(B1+B2)\cdot(C1+C2)\cdot(D1+D2)$

description

The OA240LJ is a 4-wide, 2-input OR-AND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OA240LJ A1,A2,B1,B2,C1,C2,D1,D2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.46		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	0.4	1.2	3.17	0.42	1.2	2.84	ns
t_{PHL}			0.38	1.38	3.98	0.41	1.38	3.59	
Δt_{PLH}	Any	Y	0.41	1.11	2.38	0.44	1.11	2.18	ns/pF
Δt_{PHL}			0.38	1.01	2.21	0.42	1.01	2.01	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OA241LJ
3-WIDE, 2-INPUT OR-NAND GATE
$Y = \overline{(A1+A2)\cdot(B1+B2)\cdot(C1+C2)\cdot(D1+D2)}$

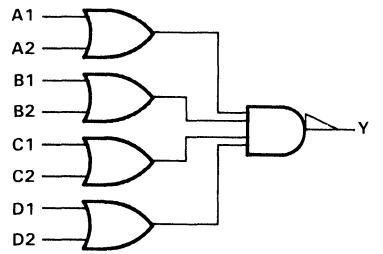
D3030, MARCH 1989

INTERNAL MACRO

FUNCTION TABLE

INPUTS								OUTPUT
A1	A2	B1	B2	C1	C2	D1	D2	Y
L	L	X	X	X	X	X	X	H
X	X	L	L	X	X	X	X	H
X	X	X	X	L	L	X	X	H
X	X	X	X	X	X	L	L	H
(Any H)		(Any H)		(Any H)		(Any H)		L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = \overline{(A1+A2)\cdot(B1+B2)\cdot(C1+C2)\cdot(D1+D2)}$

description

The OA241LJ is a 4-wide, 2-input OR-NAND gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OA241LJ A1,A2,B1,B2,C1,C2,D1,D2,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.61		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	0.38	1.36	3.95	0.41	1.36	3.58	ns
t_{PHL}			0.45	1.4	3.63	0.48	1.4	3.25	
Δt_{PLH}	Any	Y	0.42	1.1	2.31	0.45	1.1	2.12	ns/pF
Δt_{PHL}			0.33	0.74	1.46	0.36	0.74	1.32	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OA320LJ
2-WIDE, 3-INPUT OR-AND GATE WITH 2X OUTPUT
$Y = (A1 + A2 + A3) \cdot (B1 + B2 + B3)$

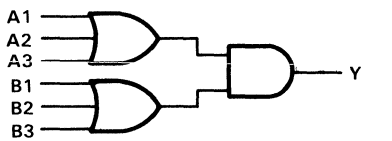
D3030, MARCH 1989

INTERNAL MACRO

FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	A3	B1	B2	B3	Y
L	L	L	X	X	X	L
X	X	X	L	L	L	L
(Any H)			(Any H)			H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = (A1+A2+A3)\cdot(B1+B2+B3)$

description

The OA320LJ is a 2-wide, 3-input OR-AND gate with a 2X output. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OA320LJ A1,A2,A3,B1,B2,B3,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.44		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	Any	Y	0.19	0.59	1.4	0.2	0.59	1.29	ns
t_{PHL}			0.44	1.28	3.54	0.47	1.28	3.22	
Δt_{PLH}	Any	Y	0.41	1.1	2.35	0.45	1.1	2.16	ns/pF
Δt_{PHL}			0.39	0.97	2.19	0.42	0.97	1.98	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OR210LJ
2-INPUT POSITIVE-OR GATE

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = A+B = \overline{\overline{A}\cdot\overline{B}}$

description

The OR210LJ cell is a minimum-size, 2-input positive-OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR210LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.06		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.37		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.21	0.49	0.95	0.21	0.49	0.88	ns
t_{PHL}			0.27	0.65	1.45	0.28	0.65	1.34	
Δt_{PLH}	A, B	Y	0.4	1.09	2.32	0.44	1.09	2.12	ns/pF
Δt_{PHL}			0.28	0.63	1.28	0.3	0.63	1.16	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OR220LJ
2-INPUT POSITIVE-OR GATE WITH 2X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = A+B = \overline{\overline{A}\cdot\overline{B}}$

description

The OR220LJcell is a 2-input positive-OR gate featuring twice the capacitive-drive capability when compared to the OR210LJ OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR220LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.6		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.26	0.58	1.15	0.27	0.58	1.06	ns
t_{PHL}			0.27	0.76	1.78	0.29	0.76	1.63	
Δt_{PLH}	A, B	Y	0.18	0.53	1.12	0.2	0.53	1.04	ns/pF
Δt_{PHL}			0.18	0.38	0.82	0.18	0.38	0.76	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OR240LJ
2-INPUT POSITIVE-OR GATE WITH 4X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = A+B = \overline{\overline{A}\cdot\overline{B}}$

description

The OR240LJ cell is a 2-input positive-OR gate featuring four times the capacitive-drive capability when compared to the OR210LJ OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR240LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.1		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.16		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.24	0.55	1.02	0.27	0.55	0.96	ns
t_{PHL}			0.28	0.67	1.53	0.28	0.67	1.39	
Δt_{PLH}	A, B	Y	0.1	0.27	0.6	0.1	0.27	0.54	ns/pF
Δt_{PHL}			0.08	0.25	0.52	0.08	0.25	0.48	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OR260LJ
2-INPUT POSITIVE-OR GATE WITH 6X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = A+B = \overline{\overline{A}\cdot\overline{B}}$

description

The OR260LJ cell is a 2-input positive-OR gate featuring six times the capacitive-drive capability when compared to the OR210LJ OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR260LJ A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.16		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.73		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.2	0.55	1.02	0.22	0.55	0.95	ns
t_{PHL}			0.26	0.68	1.52	0.26	0.68	1.41	
Δt_{PLH}	A, B	Y	0.1	0.18	0.4	0.12	0.18	0.36	ns/pF
Δt_{PHL}			0.08	0.17	0.38	0.08	0.17	0.32	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OR310LJ
3-INPUT POSITIVE-OR GATE

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	H
X	H	X	H
X	X	H	H
L	L	L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = A+B+C = \overline{\overline{A}\cdot\overline{B}\cdot\overline{C}}$

description

The OR310LJ cell is a minimum-size, 3-input positive-OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR310LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.39		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C	Y	0.26	0.61	1.18	0.28	0.61	1.09	ns
t_{PHL}			0.3	0.87	2.25	0.32	0.87	2.06	
Δt_{PLH}	A, B, C	Y	0.42	1.09	2.34	0.44	1.09	2.14	ns/pF
Δt_{PHL}			0.3	0.71	1.48	0.32	0.71	1.32	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OR320LJ
3-INPUT POSITIVE-OR GATE WITH 2X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	H
X	H	X	H
X	X	H	H
L	L	L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = A+B+C = \overline{\overline{A}\cdot\overline{B}\cdot\overline{C}}$

description

The OR320LJ cell is a 3-input positive-OR gate featuring twice the capacitive-drive capability when compared to the OR310LJ OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR320LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.62		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C	Y	0.27	0.71	1.4	0.3	0.71	1.31	ns
t_{PHL}			0.33	1.02	2.71	0.34	1.02	2.47	
Δt_{PLH}	A, B, C	Y	0.16	0.53	1.16	0.18	0.53	1.04	ns/pF
Δt_{PHL}			0.18	0.46	1.02	0.18	0.46	0.92	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OR340LJ
3-INPUT POSITIVE-OR GATE WITH 4X OUTPUT

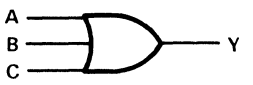
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	H
X	H	X	H
X	X	H	H
L	L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = A+B+C = \overline{\overline{A}\cdot\overline{B}\cdot\overline{C}}$

description

The OR340LJ cell is a 3-input positive-OR gate featuring four times the capacitive-drive capability when compared to the OR310LJ OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR340LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.1		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.23		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C	Y	0.31	0.68	1.29	0.32	0.68	1.19	ns
t_{PHL}			0.31	0.91	2.25	0.33	0.91	2.06	
Δt_{PLH}	A, B, C	Y	0.12	0.28	0.6	0.14	0.28	0.54	ns/pF
Δt_{PHL}			0.1	0.27	0.62	0.1	0.27	0.58	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OR360LJ
3-INPUT POSITIVE-OR GATE WITH 6X OUTPUT

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	H
X	H	X	H
X	X	H	H
L	L	L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: $Y = A+B+C = \overline{\overline{A}\cdot\overline{B}\cdot\overline{C}}$

description

The OR360LJ cell is a 3-input positive-OR gate featuring six times the capacitive-drive capability when compared to the OR310LJ OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR360LJ A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.15		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.87		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C	Y	0.31	0.65	1.2	0.32	0.65	1.12	ns
t_{PHL}			0.3	0.89	2.15	0.32	0.89	1.97	
Δt_{PLH}	A, B, C	Y	0.06	0.2	0.42	0.08	0.2	0.38	ns/pF
Δt_{PHL}			0.08	0.22	0.48	0.08	0.22	0.44	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OR410LJ
4-INPUT POSITIVE-OR GATE

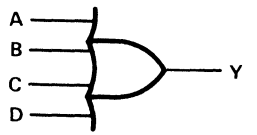
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	L	L	L	L
Any other combination				H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A+B+C+D = \overline{\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}}$

description

The OR410LJ cell is a minimum-size, 4-input positive-OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR410LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.39		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C, D	Y	0.27	0.71	1.38	0.3	0.71	1.28	ns
t_{PHL}			0.32	1.05	3.03	0.35	1.05	2.77	
Δt_{PLH}	A, B, C, D	Y	0.4	1.1	2.38	0.44	1.1	2.18	ns/pF
Δt_{PHL}			0.32	0.8	1.66	0.34	0.8	1.5	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OR420LJ
4-INPUT POSITIVE-OR GATE WITH 2X OUTPUT

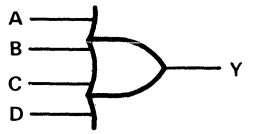
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	L	L	L	L
Any other combination				H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A+B+C+D = \overline{\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}}$

description

The OR420LJ cell is a 4-input positive-OR gate featuring twice the capacitive-drive capability when compared to the OR410LJ OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR420LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C, D	Y	0.41	0.85	1.77	0.41	0.85	1.63	ns
t_{PHL}			0.34	1.26	3.67	0.35	1.26	3.34	
Δt_{PLH}	A, B, C, D	Y	0.18	0.54	1.22	0.2	0.54	1.1	ns/pF
Δt_{PHL}			0.18	0.52	1.12	0.2	0.52	1.02	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OR440LJ
4-INPUT POSITIVE-OR GATE WITH 4X OUTPUT

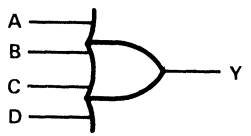
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	L	L	L	L
Any other combination				H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A+B+C+D = \overline{\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}}$

description

The OR440LJ cell is a 4-input positive-OR gate featuring four times the capacitive-drive capability when compared to the OR410LJ OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR440LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.1		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.61		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C, D	Y	0.36	0.79	1.49	0.38	0.79	1.39	ns
t_{PHL}			0.32	1.16	3.01	0.35	1.16	2.74	
Δt_{PLH}	A, B, C, D	Y	0.12	0.28	0.62	0.12	0.28	0.58	ns/pF
Δt_{PHL}			0.12	0.31	0.68	0.12	0.31	0.64	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OR460LJ
4-INPUT POSITIVE-OR GATE WITH 6X OUTPUT

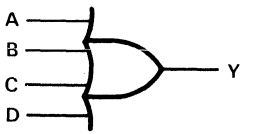
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	L	L	L	L
Any other combination				H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A+B+C+D = \overline{\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}}$

description

The OR460LJ cell is a 4-input positive-OR gate featuring six times the capacitive-drive capability when compared to the OR410LJ OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR460LJ A,B,C,D,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.15		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	2.45		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B, C, D	Y	0.35	0.79	1.47	0.37	0.79	1.35	ns
t_{PHL}			0.33	1.16	3.11	0.34	1.16	2.84	
Δt_{PLH}	A, B, C, D	Y	0.12	0.18	0.44	0.12	0.18	0.42	ns/pF
Δt_{PHL}			0.1	1.24	0.54	0.1	0.24	0.5	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OR510LJ
5-INPUT POSITIVE-OR GATE

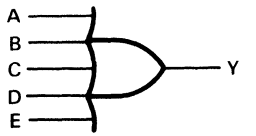
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
L	L	L	L	L	L
Any other combination					H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A+B+C+D+E = \overline{\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}\cdot\overline{E}}$

description

The OR510LJ cell is a minimum-size, 5-input positive-OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR510LJ A,B,C,D,E,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.59		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A,B,C,D,E	Y	0.22	0.58	1.17	0.23	0.58	1.09	ns
t_{PHL}			0.26	0.84	2.48	0.27	0.84	2.26	
Δt_{PLH}	A,B,C,D,E	Y	0.41	1.73	2.32	0.44	1.73	2.2	ns/pF
Δt_{PHL}			0.36	0.96	2.21	0.39	0.96	1.98	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OR810LJ
8-INPUT POSITIVE-OR GATE

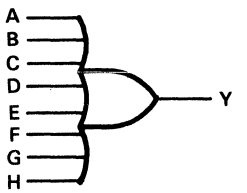
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
L	L	L	L	L	L	L	L	L
Any other combination								H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: $Y = A+B+C+D+E+F+G+H = \overline{\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}\cdot\overline{E}\cdot\overline{F}\cdot\overline{G}\cdot\overline{H}}$

description

The OR810LJ cell is a minimum-size, 8-input positive-OR gate. When the gate is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OR810LJ A,B,C,D,E,F,G,H,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	0.63		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A thru H	Y	0.25	0.65	1.4	0.28	0.65	1.3	ns
t_{PHL}			0.4	1.19	3.46	0.42	1.19	3.14	
Δt_{PLH}	A thru H	Y	0.39	1.06	2.29	0.42	1.06	2.11	ns/pF
Δt_{PHL}			0.36	1.02	2.34	0.39	1.02	2.11	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

FLIP-FLOPS/LATCHES
FUNCTIONAL INDEX

D3030, APRIL 1988

D-TYPE FLIP-FLOPS

DESCRIPTION	f_{max} (MHz)	CELL NAME	OUTPUT DRIVE	EQUIVALENT NA210s	PAGE
Preset and Clear	130	DFB20LJ	2X	7.25	9-3
Clear	155	DFC20LJ	2X	6.75	9-5
	165	DFN20LJ	2X	5.75	9-7
Preset	140	DFP20LJ	2X	6.5	9-9
Preset and Clear	170	DTB10LJ	1X	6.25	9-11
Clear	150	DTC10LJ	1X	5.5	9-13
	165	DTN10LJ	1X	5.25	9-15
Preset	165	DTP10LJ	1X	5.5	9-17

J-$\overline{K}$ FLIP-FLOPS

DESCRIPTION	f_{max} (MHz)	CELL NAME	OUTPUT DRIVE	EQUIVALENT NA210s	PAGE
Positive-Edge Trigger with Preset and Clear	127	JKB20LJ	2X	9.5	9-19
Negative-Edge Trigger with Preset and Clear	125	JKB21LJ	2X	9.5	9-21

LATCHES

DESCRIPTION	CELL NAME	OUTPUT DRIVE	COMMENTS	EQUIVALENT NA210s	PAGE
Set-Reset	LAB10LJ	1X		2.5	9-23
Set-Reset	LAB20LJ	2X		2.75	9-25
D-Type	LAH10LJ	1X	Active H enable	3.75	9-27
D-Type	LAH20LJ	2X	Active H enable	4	9-29
D-Type	LAH23LJ	2X	Clear and Preset	6.5	9-31
D-Type	LAH40LJ	4X	Active H enable	5.25	9-33
D-Type	LAL20LJ	2X	Active L enable	4.25	9-35
3-S Bus Holder	LH110LJ	1X		1	9-37

D3030, APRIL 1988

TOGGLE FFs AND SCAN FFs/LATCHES

DESCRIPTION	f_{max} (MHz)	CELL NAME	OUTPUT DRIVE	EQUIVALENT NA210s	PAGE
Preset and Clear	145	TAB20LJ	2X	7.5	9-38
Clear	165	TAC20LJ	2X	6.75	9-40
Preset	165	TAP20LJ	2X	6.5	9-42
Scan Latch, Master and Slave Outputs	76	TDB10LJ	1X	7	9-44
Multiplexed Scan FF, Clear	135	TDC10LJ	1X	7.75	9-50
Scan Latch, Clear, Master and Slave Outputs	100	TDC11LJ	1X	4.25	9-53
Multiplexed Scan FF	155	TDN10LJ	1X	7.25	9-60
Scan Latch	100	TDN11LJ	1X	4	9-62
Scan Latch, Master and Slave Outputs	100	TDN12LJ	1X	3.75	9-67
Scan Latch, Master and Slave Outputs, Slave D Input	100	TDN13LJ	1X	6	9-73
Scan Latch, Master and Slave Outputs	83	TDN22LJ	2X	6	9-80

D-TYPE FLIP-FLOPS (SOFTWARE)

DESCRIPTION	CELL NAME	OUTPUT DRIVE	EQUIVALENT NA210s	PAGE
4-Bit, 3-State Outputs, Active H Clear	S173LJ	1X	47.5	9-86
6-Bit, Active L Clear	S174LJ	1X	45	9-91
4-Bit, Complementary Outputs, Active L Clear	S175LJ	1X	25.75	9-95
8-Bit, Active L Clear	S273LJ	1X	43.25	9-99
8-Bit, 3-State Outputs	S374LJ	1X	50.75	9-103

LATCHES (SOFTWARE)

DESCRIPTION	CELL NAME	OUTPUT DRIVE	COMMENTS	EQUIVALENT NA210s	PAGE
8-Bit Addressable	S259LJ	2X		59.75	9-107
8-Bit D-Type	S373LJ	1X	3-state outputs, Active H enable	34.5	9-113
4-Bit D-Type	S375LJ	2X	Active H enable	14	9-117

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

DFB20LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET, CLEAR, AND 2X OUTPUTS

D3030, APRIL 1988

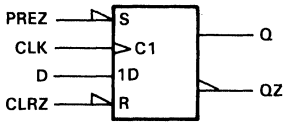
INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUTS	
PREZ	CLRZ	CLK	D	Q	QZ
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	L*	L*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

* This configuration is nonstable; that is, it will not persist when PREZ or CLRZ returns to its inactive (high) level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DFB20LJ cell implements a D-type flip-flop with preset, clear, and 2X drive outputs. The flip-flop can be used as a stand-alone bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DFB20LJ CLRZ,PREZ,D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	130	MHz
t_w	Pulse duration	CLRZ low	3		ns
		PREZ low	3		
		CLK high or low	3.8		
t_{su}	Setup time before clock	CLRZ inactive (high)	3		ns
		PREZ inactive (high)	0		
		D high or low	2		
t_h	Hold time after clock	D high or low	0.5		ns

DFB20LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET, CLEAR, AND 2X OUTPUTS

D3030, APRIL 1988

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLRZ		0.16		pF
		PREZ		0.15		
		D		0.05		
		CLK		0.11		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.78		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.63	1.92	4.64	0.68	1.92	4.19	ns
t_{PHL}			0.44	1.31	3.08	0.45	1.31	2.8	
t_{PLH}	CLK	QZ	0.62	1.89	4.55	0.65	1.89	4.12	ns
t_{PHL}			0.44	1.33	3.11	0.47	1.33	2.83	
t_{PLH}	CLRZ	QZ	0.56	1.52	3.5	0.58	1.52	3.18	ns
t_{PHL}		Q	0.31	0.76	1.6	0.33	0.76	1.48	
t_{PLH}	PREZ	Q	0.56	1.5	3.47	0.57	1.5	3.14	ns
t_{PHL}		QZ	0.3	0.78	1.7	0.33	0.78	1.55	
Δt_{PLH}	CLK	Q	0.2	0.56	1.16	0.2	0.56	1.08	ns/pF
Δt_{PHL}			0.14	0.34	0.76	0.16	0.34	0.68	
Δt_{PLH}	CLK	QZ	0.18	0.54	1.18	0.2	0.54	1.08	ns/pF
Δt_{PHL}			0.18	0.36	0.78	0.18	0.36	0.7	
Δt_{PLH}	CLRZ	QZ	0.18	0.54	1.18	0.2	0.54	1.08	ns/pF
Δt_{PHL}		Q	0.16	0.36	0.78	0.16	0.36	0.7	
Δt_{PLH}	PREZ	Q	0.16	0.54	1.18	0.2	0.54	1.1	ns/pF
Δt_{PHL}		QZ	0.16	0.36	0.74	0.16	0.36	0.68	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

DFC20LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH CLEAR AND 2X OUTPUTS

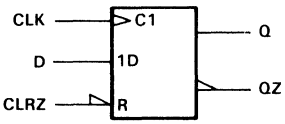
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
CLRZ	CLK	D	Q	QZ
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q_0}$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DFC20LJ cell implements a D-type flip-flop with clear and 2X drive outputs. The flip-flop can be used as a stand-alone bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DFC20LJ CLRZ,D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	155	MHz
t_w	Pulse duration	CLRZ low	3		ns
		CLK high or low	3.2		
t_{su}	Setup time before clock	CLRZ inactive (high)	2		ns
		D high or low	2		
t_h	Hold time after clock	D high or low	0.25		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLRZ		0.11		pF
		D		0.05		
		CLK		0.16		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.88		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.64	1.86	4.4	0.68	1.86	3.99	ns
t_{PHL}			0.38	1.14	2.65	0.41	1.14	2.39	
t_{PLH}	CLK	QZ	0.54	1.58	3.67	0.57	1.58	3.34	ns
t_{PHL}			0.45	1.26	2.91	0.46	1.26	2.65	
t_{PLH}	CLRZ	QZ	0.53	1.37	3.12	0.57	1.37	2.84	ns
t_{PHL}		Q	0.31	0.77	1.61	0.33	0.77	1.49	
Δt_{PLH}	CLK	Q	0.18	0.52	1.16	0.18	0.52	1.06	ns/pF
Δt_{PHL}			0.16	0.36	0.7	0.16	0.36	0.66	
Δt_{PLH}	CLK	QZ	0.18	0.52	1.1	0.2	0.52	1	ns/pF
Δt_{PHL}			0.14	0.34	0.74	0.16	0.34	0.66	
Δt_{PLH}	CLRZ	QZ	0.18	0.52	1.1	0.18	0.52	1.02	ns/pF
Δt_{PHL}		Q	0.16	0.36	0.8	0.16	0.36	0.72	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

DFN20LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH 2X OUTPUTS

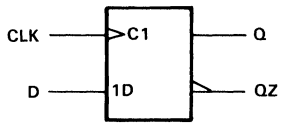
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUTS	
CLK	D	Q	QZ
↑	H	H	L
↑	L	L	H
L	X	Q_0	$\overline{Q_0}$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DFN20LJ cell implements a D-type flip-flop with 2X drive outputs. The flip-flop can be used as a stand-alone bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DFN20LJ D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	165	MHz
t_w	Pulse duration	CLK high or low	3		ns
t_{su}	Setup time before clock	D high or low	2		ns
t_h	Hold time after clock	D high or low	0.5		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.12		pF
		D		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.63		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.45	1.42	3.21	0.49	1.42	2.93	ns
t_{PHL}			0.37	1.12	2.53	0.39	1.12	2.31	
t_{PLH}	CLK	QZ	0.53	1.54	3.59	0.56	1.54	3.25	ns
t_{PHL}			0.36	1.02	2.23	0.39	1.02	2.05	
Δt_{PLH}	CLK	Q	0.2	0.54	1.14	0.22	0.54	1.04	ns/pF
Δt_{PHL}			0.16	0.36	0.76	0.18	0.36	0.68	
Δt_{PLH}	CLK	QZ	0.18	0.54	1.12	0.2	0.54	1.04	ns/pF
Δt_{PHL}			0.12	0.34	0.72	0.12	0.34	0.64	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

DFP20LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET AND 2X OUTPUTS

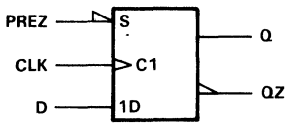
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
PREZ	CLK	D	Q	QZ
L	X	X	H	L
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q_0}$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DFP20LJ cell implements a D-type flip-flop with preset and 2X drive outputs. The flip-flop can be used as a stand-alone bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DFP20LJ PREZ,D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	140	MHz
t_w	Pulse duration	PREZ low	3		ns
		CLK high or low	3.6		
t_{su}	Setup time before clock	PREZ inactive (high)	0		ns
		D high or low	2		
t_h	Hold time after clock	D high or low	0.75		ns

DFP20LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET AND 2X OUTPUTS

D3030, APRIL 1988

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	PREZ		0.16		pF
		CLK		0.12		
		D		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.67		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.54	1.59	3.69	0.58	1.59	3.35	ns
t_{PHL}			0.43	1.2	2.88	0.44	1.2	2.62	
t_{PLH}	CLK	QZ	0.6	1.8	4.32	0.63	1.8	3.91	ns
t_{PHL}			0.4	1.14	2.61	0.42	1.14	2.39	
t_{PLH}	PREZ	Q	0.46	1.32	2.99	0.5	1.32	2.71	ns
t_{PHL}		QZ	0.29	0.79	1.72	0.32	0.79	1.56	
Δt_{PLH}	CLK	Q	0.2	0.54	1.1	0.22	0.54	1.02	ns/pF
Δt_{PHL}			0.12	0.36	0.72	0.14	0.36	0.64	
Δt_{PLH}	CLK	QZ	0.18	0.54	1.18	0.2	0.54	1.08	ns/pF
Δt_{PHL}			0.16	0.38	0.74	0.18	0.38	0.66	
Δt_{PLH}	PREZ	Q	0.22	0.52	1.12	0.22	0.52	1.04	ns/pF
Δt_{PHL}		QZ	0.16	0.34	0.7	0.16	0.34	0.66	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

DTB10LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET, CLEAR, AND 1X OUTPUTS

D3030, APRIL 1988

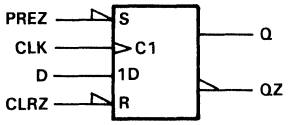
INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUTS	
PREZ	CLRZ	CLK	D	Q	QZ
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	L*	L*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

* This configuration is nonstable; that is, it will not persist when PREZ or CLRZ returns to its inactive (high) level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DTB10LJ cell implements a D-type flip-flop with preset, clear, and 1X drive outputs. The flip-flop can be used as a stand-alone bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DTB10LJ CLRZ,PREZ,D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	170	MHz
t_w	Pulse duration	CLRZ low	3		ns
		PREZ low	4		
		CLK high or low	2.9		
t_{su}	Setup time before clock	CLRZ inactive (high)	0		ns
		PREZ inactive (high)	0		
		D high or low	2		
t_h	Hold time after clock	CLRZ active (low)	2		ns
		PREZ active (low)	1		
		D high or low	0		

DTB10LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET, CLEAR, AND 1X OUTPUTS

D3030, APRIL 1988

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLRZ		0.05		pF
		PREZ		0.08		
		D		0.08		
		CLK		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.51		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.52	1.3	2.83	0.55	1.3	2.6	ns
t_{PHL}			0.61	1.55	3.41	0.65	1.55	3.12	
t_{PLH}	CLK	QZ	0.47	1.1	2.34	0.49	1.1	2.14	ns
t_{PHL}			0.54	1.33	2.9	0.57	1.33	2.66	
t_{PLH}	CLRZ	QZ	0.56	1.64	3.9	0.58	1.64	3.53	ns
t_{PHL}		Q	0.29	0.58	1.14	0.3	0.58	1.05	
t_{PLH}	PREZ	Q	0.45	1.17	2.64	0.47	1.17	2.42	ns
t_{PHL}		QZ	0.48	1.25	2.79	0.49	1.25	2.56	
Δt_{PLH}	CLK	Q	0.48	1.18	2.46	0.5	1.18	2.26	ns/pF
Δt_{PHL}			0.62	1.32	2.62	0.66	1.32	2.36	
Δt_{PLH}	CLK	QZ	0.42	1.1	2.34	0.44	1.1	2.16	ns/pF
Δt_{PHL}			0.62	1.38	2.82	0.66	1.38	2.54	
Δt_{PLH}	CLRZ	QZ	0.42	1.14	2.5	0.46	1.14	2.3	ns/pF
Δt_{PHL}		Q	0.6	1.32	2.66	0.64	1.32	2.4	
Δt_{PLH}	PREZ	Q	0.44	1.18	2.46	0.48	1.18	2.26	ns/pF
Δt_{PHL}		QZ	0.6	1.34	2.76	0.66	1.34	2.48	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

DTC10LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH CLEAR AND 1X OUTPUTS

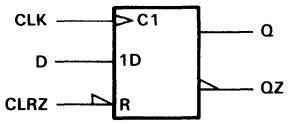
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
CLRZ	CLK	D	Q	QZ
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q_0}$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DTC10LJ cell implements a D-type flip-flop with clear and 1X drive outputs. The flip-flop can be used as a stand-alone bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DTC10LJ CLRZ,D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	150	MHz
t_w	Pulse duration	CLRZ low	3		ns
		CLK high or low	3.3		
t_{su}	Setup time before clock	CLRZ inactive (high)	0		ns
		D high or low	2		
t_h	Hold time after clock	D high or low	0.25		ns
		CLRZ active (low)	3		

DTC10LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH CLEAR AND 1X OUTPUTS

D3030, APRIL 1988

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLRZ		0.05		pF
		CLK		0.06		
		D		0.09		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.44		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.49	1.26	2.71	0.52	1.26	2.49	ns
t_{PHL}			0.61	1.54	3.41	0.63	1.54	3.12	
t_{PLH}	CLK	QZ	0.47	1.14	2.45	0.49	1.14	2.25	ns
t_{PHL}			0.51	1.25	2.73	0.53	1.25	2.52	
t_{PLH}	CLRZ	QZ	0.55	1.56	3.61	0.59	1.56	3.3	ns
t_{PHL}		Q	0.3	0.57	1.12	0.3	0.57	1.03	
Δt_{PLH}	CLK	Q	0.48	1.16	2.46	0.5	1.16	2.26	ns/pF
Δt_{PHL}			0.6	1.32	2.62	0.66	1.32	2.36	
Δt_{PLH}	CLK	QZ	0.5	1.32	2.78	0.54	1.32	2.56	ns/pF
Δt_{PHL}			0.58	1.3	2.64	0.62	1.3	2.36	
Δt_{PLH}	CLRZ	QZ	0.52	1.32	2.86	0.54	1.32	2.6	ns/pF
Δt_{PHL}		Q	0.58	1.32	2.66	0.64	1.32	2.4	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

DTN10LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH 1X OUTPUTS

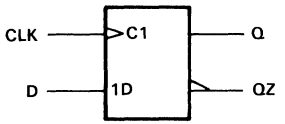
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUTS	
CLK	D	Q	QZ
↑	H	H	L
↑	L	L	H
L	X	Q_0	$\overline{Q_0}$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DTN10LJ cell implements a D-type flip-flop with 1X drive outputs. The flip-flop can be used as a stand-alone bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DTN10LJ D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	165	MHz
t_w	Pulse duration	CLK high or low	3		ns
t_{su}	Setup time before clock	D high or low	2		ns
t_h	Hold time after clock	D high or low	0.5		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.05		pF
		D		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.89		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.59	1.43	3.14	0.61	1.43	2.86	ns
t_{PHL}			0.53	1.37	2.96	0.55	1.37	2.71	
t_{PLH}	CLK	QZ	0.44	1.03	2.15	0.45	1.03	1.98	ns
t_{PHL}			0.51	1.2	2.56	0.52	1.2	2.35	
Δt_{PLH}	CLK	Q	0.4	1.06	2.2	0.44	1.06	2.04	ns/pF
Δt_{PHL}			0.56	1.22	2.44	0.62	1.22	2.2	
Δt_{PLH}	CLK	QZ	0.42	1.12	2.38	0.46	1.12	2.18	ns/pF
Δt_{PHL}			0.6	1.34	2.7	0.66	1.34	2.44	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

DTP10LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET AND 1X OUTPUTS

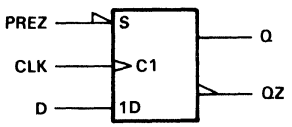
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
PREZ	CLK	D	Q	QZ
L	X	X	H	L
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q_0}$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DTP10LJ cell implements a D-type flip-flop with preset and 1X drive outputs. The flip-flop can be used as a stand-alone bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DTP10LJ PREZ,D,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	165	MHz
t_w	Pulse duration	PREZ low	4		ns
		CLK high or low	3		
t_{su}	Setup time before clock	PREZ inactive (high)	0		ns
		D high or low	2		
t_h	Hold time after clock	D high or low	0.25		ns
		PREZ active (low)	0.75		

DTP10LJ
D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET AND 1X OUTPUTS

D3030, APRIL 1988

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	PREZ		0.08		pF
		CLK		0.05		
		D		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.32		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.61	1.48	3.25	0.63	1.48	2.96	ns
t_{PHL}			0.57	1.42	3.04	0.6	1.42	2.79	
t_{PLH}	CLK	QZ	0.46	1.04	2.2	0.49	1.04	2.02	ns
t_{PHL}			0.53	1.21	2.58	0.54	1.21	2.38	
t_{PLH}	PREZ	Q	0.53	1.34	3.03	0.55	1.34	2.75	ns
t_{PHL}		QZ	0.43	1.09	2.4	0.44	1.09	2.21	
Δt_{PLH}	CLK	Q	0.46	1.18	2.46	0.5	1.18	2.28	ns/pF
Δt_{PHL}			0.6	1.3	2.64	0.64	1.3	2.38	
Δt_{PLH}	CLK	QZ	0.46	1.22	2.54	0.48	1.22	2.34	ns/pF
Δt_{PHL}			0.6	1.36	2.76	0.66	1.36	2.48	
Δt_{PLH}	PREZ	Q	0.46	1.18	2.44	0.5	1.18	2.26	ns/pF
Δt_{PLH}		QZ	0.6	1.34	2.72	0.66	1.34	2.44	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

JKB20LJ
J-K-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET, CLEAR, AND 2X OUTPUTS

D3030, APRIL 1988

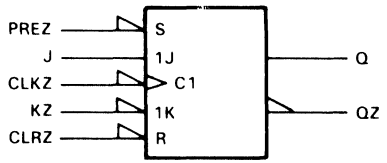
INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUTS	
PREZ	CLRZ	CLK	J	KZ	Q	QZ
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

* This configuration is nonstable; that is, it will not persist when PREZ or CLRZ return to their inactive (high) level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The JKB20LJ cell implements a positive-edge-triggered J-K flip-flop with preset, clear and 2X drive outputs. The flip-flop can be used as a stand-alone bit-resolution device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: JKB20LJ CLRZ,PREZ,KZ,J,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	127	MHz
t_w	Pulse duration	CLRZ low	4		ns
		PREZ low	3		
		CLK high or low	3.9		
t_{su}	Setup time before clock	CLRZ inactive (high)	0.25		ns
		PREZ inactive (high)	0		
		J or KZ high or low	3		
t_h	Hold time after clock	J or KZ high or Low	0		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLRZ		0.11		pF
		PREZ		0.11		
		J, KZ		0.06		
		CLK		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	3.69		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.43	1.22	2.7	0.45	1.22	2.47	ns
t_{PHL}			0.37	1.09	2.46	0.4	1.09	2.27	
t_{PLH}	CLK	QZ	0.54	1.78	4.23	0.58	1.78	3.86	ns
t_{PHL}			0.54	1.74	4.03	0.58	1.74	3.69	
t_{PLH}	CLRZ	QZ	0.63	1.84	4.42	0.65	1.84	4.02	ns
t_{PHL}		Q	0.43	1.1	2.49	0.45	1.1	2.3	
t_{PLH}	PREZ	Q	0.57	1.7	3.97	0.61	1.7	3.6	ns
t_{PHL}		QZ	0.31	0.77	1.64	0.33	0.77	1.51	
Δt_{PLH}	CLK	Q	0.21	0.58	1.26	0.23	0.58	1.16	ns/pF
Δt_{PHL}			0.18	0.5	1.08	0.2	0.5	0.97	
Δt_{PLH}	CLK	QZ	0.21	0.53	1.12	0.22	0.53	1.03	ns/pF
Δt_{PHL}			0.2	0.4	0.83	0.2	0.4	0.75	
Δt_{PLH}	CLRZ	QZ	0.19	0.52	1.12	0.21	0.52	1.03	ns/pF
Δt_{PHL}		Q	0.18	0.52	1.15	0.19	0.52	1.04	
Δt_{PLH}	PREZ	Q	0.22	0.55	1.19	0.23	0.55	1.09	ns/pF
Δt_{PHL}		QZ	0.17	0.39	0.81	0.17	0.39	0.74	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

JKB21LJ
J-K-TYPE NEGATIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET, CLEAR, AND 2X OUTPUTS

D3030, APRIL 1988

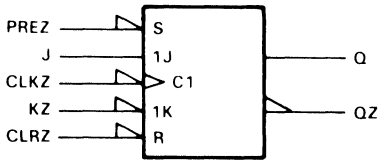
INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUTS	
PREZ	CLRZ	CLKZ	J	KZ	Q	QZ
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	L	H
H	H	↓	H	L	TOGGLE	
H	H	↓	L	H	Q_0	$\overline{Q}_0$
H	H	↓	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

* This configuration is nonstable; that is, it will not persist when PREZ or CLRZ return to their inactive (high) level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The JKB21LJ cell implements a negative-edge-triggered J-K flip-flop with preset, clear, and 2X drive outputs. The flip-flop can be used as a stand-alone bit-resolution device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: JKB21LJ CLRZ,PREZ,KZ,J,CLKZ,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	125	MHz
t_w	Pulse duration	CLRZ low	4		ns
		PREZ low	3		
		CLKZ high or low	4		
t_{su}	Setup time before clock	CLRZ inactive (high)	0.5		ns
		PREZ inactive (high)	0		
		J or KZ high or low	3		
t_h	Hold time after clock	CLRZ active (low)	0.25		ns
		PREZ active (low)	2		
		J or KZ high or low	0.5		

JKB21LJ
J-K-TYPE NEGATIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET, CLEAR, AND 2X OUTPUTS

D3030, APRIL 1988

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	input capacitance	CLRZ		0.11		pF
		PREZ		0.11		
		J, KZ		0.06		
		CLKZ		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.91		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLKZ	Q	0.43	1.16	2.63	0.45	1.16	2.4	ns
t_{PHL}			0.41	1.12	2.59	0.43	1.12	2.38	
t_{PLH}	CLKZ	QZ	0.52	1.8	4.36	0.57	1.8	3.96	ns
t_{PHL}			0.55	1.7	3.97	0.59	1.7	3.62	
t_{PLH}	CLRZ	QZ	0.62	1.84	4.4	0.64	1.84	4.01	ns
t_{PHL}		Q	0.43	1.11	2.5	0.45	1.11	2.3	
t_{PLH}	PREZ	Q	0.57	1.69	3.96	0.6	1.69	3.59	ns
t_{PHL}		QZ	0.31	0.76	1.63	0.33	0.76	1.5	
Δt_{PLH}	CLKZ	Q	0.21	0.58	1.27	0.22	0.58	1.16	ns/pF
Δt_{PHL}			0.15	0.5	1.08	0.18	0.5	0.97	
Δt_{PLH}	CLKZ	QZ	0.23	0.53	1.12	0.24	0.53	1.03	ns/pF
Δt_{PHL}			0.17	0.39	0.83	0.18	0.39	0.75	
Δt_{PLH}	CLRZ	QZ	0.19	0.53	1.12	0.21	0.53	1.03	ns/pF
Δt_{PHL}		Q	0.18	0.51	1.14	0.19	0.51	1.03	
Δt_{PLH}	PREZ	Q	0.22	0.55	1.19	0.23	0.55	1.09	ns/pF
Δt_{PHL}		QZ	0.17	0.39	0.82	0.17	0.39	0.74	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

LAB10LJ
S̄-R̄ LATCH
WITH 1X OUTPUTS

D3030, APRIL 1988

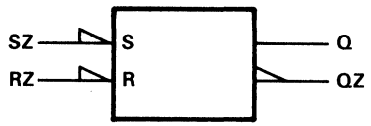
INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUTS	
SZ	RZ	Q	QZ
H	H	Q_0	$\overline{Q}_0$
L	H	H	L
H	L	L	H
L	L	L*	L*

* This configuration is nonstable; that is, it will not persist when either SZ or RZ returns to its inactive (H) level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The LAB10LJ cell implements a S̄-R̄ latch with 1X drive outputs. The cell incorporates direct inputs for both set (SZ) and reset (RZ) providing a stand-alone bit-storage device or an addition to larger latched functions.

When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: LAB10LJ SZ,RZ,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
t_w	Pulse duration	RZ low	2		ns
		SZ low	2		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	RZ, SZ		0.06		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.83		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	SZ	Q	0.36	0.89	1.97	0.37	0.89	1.8	ns
t_{PHL}	R̄Z		0.26	0.65	1.31	0.28	0.65	1.2	
t_{PLH}	RZ	QZ	0.36	0.92	1.99	0.37	0.92	1.82	ns
t_{PHL}	SZ		0.27	0.65	1.33	0.28	0.65	1.23	
Δt_{PLH}	SZ	Q	0.4	1.12	2.28	0.44	1.12	2.1	ns/pF
Δt_{PHL}		QZ	0.28	0.6	1.2	0.3	0.6	1.08	
Δt_{PLH}	RZ	QZ	0.4	1.08	2.24	0.44	1.08	2.06	ns/pF
Δt_{PHL}		Q	0.28	0.58	1.18	0.3	0.58	1.08	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

LAB20LJ
$\overline{S}$-$\overline{R}$ LATCH
WITH 2X OUTPUTS

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUTS	
SZ	RZ	Q	QZ
H	H	Q_0	$\overline{Q}_0$
L	H	H	L
H	L	L	H
L	L	L*	L*

* This configuration is nonstable; that is, it will not persist when either SZ or RZ returns to its inactive (H) level.

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The LAB20LJ cell implements a $\overline{S}$-$\overline{R}$ latch with 2X drive outputs. The cell incorporates direct inputs for both set (SZ) and reset (RZ) providing a stand-alone bit-storage device or an addition to larger latched functions.

When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: LAB20LJ SZ,RZ,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
t_w	Pulse duration	RZ low	2		ns
		SZ low	2		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	RZ, SZ		0.06		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.32		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	SZ	Q	0.38	1.05	2.31	0.4	1.05	2.1	ns
t_{PHL}	RZ		0.28	0.71	1.44	0.3	0.71	1.32	
t_{PLH}	RZ	QZ	0.44	1.11	2.42	0.46	1.11	2.22	ns
t_{PHL}	SZ		0.27	0.64	1.35	0.29	0.64	1.24	
Δt_{PLH}	SZ	Q	0.2	0.52	1.1	0.22	0.52	1.02	ns/pF
Δt_{PHL}	SZ	QZ	0.16	0.36	0.72	0.16	0.36	0.66	
Δt_{PLH}	RZ	QZ	0.1	0.52	1.12	0.2	0.52	1.02	ns/pF
Δt_{PHL}	RZ	Q	0.18	0.34	0.74	0.1	0.34	0.68	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

LAH10LJ
D-TYPE LATCH
WITH ACTIVE-HIGH ENABLE AND 1X OUTPUTS

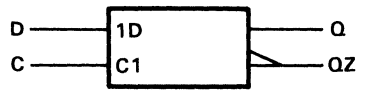
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUTS	
D	C	Q	QZ
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The LAH10LJ cell implements a D-type latch with active-high enable and 1X drive outputs. Information present at the data input is transferred to the Q output when the enable input is high, and the Q output will follow the data input as long as enable remains high. When enable goes low, the data that was present at the data input when the transition occurred is retained at the Q output until enable is taken high.

When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: LAH10LJ D,C,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
t_w	Pulse duration, C high	2		ns
t_{su}	Setup time, D high or low	0.75		
t_h	Hold time, D high or low	0		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	D		0.09		pF
		C		0.12		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.78		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	C	Q	0.29	0.78	1.58	0.34	0.78	1.47	ns
t_{PHL}			0.19	0.67	1.47	0.22	0.67	1.36	
t_{PLH}	C	QZ	0.2	0.82	1.85	0.23	0.82	1.71	ns
t_{PHL}			0.41	1.08	2.29	0.44	1.08	2.11	
t_{PLH}	D	Q	0.24	0.58	1.22	0.24	0.58	1.12	ns
t_{PHL}			0.25	0.64	1.33	0.26	0.64	1.23	
t_{PLH}	D	QZ	0.27	0.79	1.68	0.3	0.79	1.54	ns
t_{PHL}			0.36	0.88	1.91	0.37	0.88	1.77	
Δt_{PLH}	C	Q	0.42	1.06	2.24	0.42	1.06	2.06	ns/pF
Δt_{PHL}			0.24	0.58	1.16	0.26	0.58	1.04	
Δt_{PLH}	C	QZ	0.44	1.12	2.34	0.48	1.12	2.14	ns/pF
Δt_{PHL}			0.28	0.62	1.22	0.3	0.62	1.1	
Δt_{PLH}	D	Q	0.4	1.06	2.24	0.44	1.06	2.06	ns/pF
Δt_{PHL}			0.28	0.56	1.14	0.3	0.56	1.02	
Δt_{PLH}	D	QZ	0.44	1.12	2.34	0.46	1.12	2.16	ns/pF
Δt_{PHL}			0.26	0.62	1.24	0.28	0.62	1.1	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

LAH20LJ
D-TYPE LATCH
WITH ACTIVE-HIGH ENABLE AND 2X OUTPUTS

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUTS	
D	C	Q	QZ
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The LAH20LJ cell implements a D-type latch with active-high enable and 2X drive outputs. Information present at the data input is transferred to the Q output when the enable input is high, and the Q output will follow the data input as long as enable remains high. When enable goes low, the data that was present at the data input when the transition occurred is retained at the Q output until enable is taken high.

When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: LAH20LJ D,C,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
t_w	Pulse duration, C high	2		ns
t_{su}	Setup time, D high or low	1		
t_h	Hold time, D high or low	0		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	D, C		0.09		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.22		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	C	Q	0.26	0.82	1.64	0.28	0.82	1.51	ns
t_{PHL}			0.26	0.76	1.68	0.27	0.76	1.54	
t_{PLH}	C	QZ	0.35	1.02	2.28	0.37	1.02	2.1	ns
t_{PHL}			0.37	1.16	2.52	0.4	1.16	2.31	
t_{PLH}	D	Q	0.26	0.6	1.3	0.26	0.6	1.2	ns
t_{PHL}			0.27	0.71	1.49	0.29	0.71	1.36	
t_{PLH}	D	QZ	0.37	0.97	2.09	0.38	0.97	1.92	ns
t_{PHL}			0.35	0.96	2.18	0.36	0.96	2.01	
Δt_{PLH}	C	Q	0.2	0.52	1.14	0.22	0.52	1.06	ns/pF
Δt_{PHL}			0.16	0.36	0.74	0.18	0.36	0.68	
Δt_{PLH}	C	QZ	0.2	0.54	1.12	0.22	0.54	1.02	ns/pF
Δt_{PHL}			0.14	0.36	0.72	0.16	0.36	0.66	
Δt_{PLH}	D	Q	0.18	0.54	1.14	0.2	0.54	1.06	ns/pF
Δt_{PHL}			0.18	0.34	0.72	0.18	0.34	0.66	
Δt_{PLH}	D	QZ	0.22	0.52	1.1	0.24	0.52	1	ns/pF
Δt_{PHL}			0.14	0.36	0.72	0.16	0.36	0.64	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

LAH23LJ
D-TYPE TRANSPARENT LATCH WITH ACTIVE-HIGH ENABLE, CLEAR, PRESET AND 2X OUTPUTS

D3030, MARCH 1989

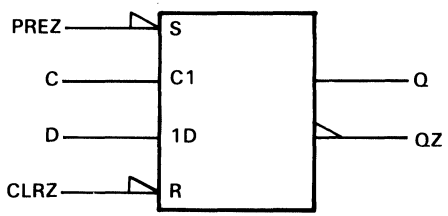
INTERNAL LATCH CELL

FUNCTION TABLE

INPUTS				OUTPUTS	
CLRZ	PREZ	D	C	Q	QZ
H	H	L	H	L	H
H	H	H	H	H	L
H	H	X	L	Q_0	$\overline{Q}_0$
L	H	X	X	L	H
H	L	X	X	H	L
L	L	X	X	H*	H*

* This configuration is nonstable; that is, it will not persist when PREZ or CLRZ returns to its inactive (high) level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The LAH23LJ cell implements a D-type transparent latch with active-high enable, asynchronous clear and preset, and 2X drive outputs. Transparent latches have level-operated control inputs rather than edge- or pulse-triggered inputs. The D input is active as long as the C, clear, and preset inputs are at their internal 1 state. The outputs respond immediately. Information present at the data input is transferred to the Q output when the enable input is high, and the Q output will follow the data input as long as enable remains high. When enable goes low, the data that was present at the data input when the transition occurred is retained at the Q output until enable is taken high.

When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: LAH23LJ D,C,CLRZ,PREZ,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
t_w	Pulse duration	C high	1		ns
		CLRZ low	2		
		PREZ low	3		
t_{su}	Setup time	D high or low	1		ns
t_h	Hold time	D high or low	0		ns
		CLRZ inactive	0.5		
		PREZ inactive	0.5		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	C		0.13		pF
		CLRZ		0.19		
		D		0.07		
		PREZ		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.25		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	C	Q	0.26	0.92	1.98	0.29	0.92	1.81	ns
t_{PHL}			0.24	0.81	1.81	0.26	0.81	1.66	
t_{PLH}	C	QZ	0.32	1.18	2.74	0.36	1.18	2.5	ns
t_{PHL}			0.4	1.37	3.09	0.43	1.37	2.82	
t_{PLH}	CLRZ	QZ	0.21	0.3	0.45	0.21	0.3	0.43	ns
t_{PHL}		Q	0.32	0.76	1.57	0.34	0.76	1.44	
t_{PLH}	D	Q	0.29	0.78	1.68	0.3	0.78	1.55	ns
t_{PHL}			0.3	0.77	1.65	0.32	0.77	1.51	
t_{PLH}	D	QZ	0.44	1.16	2.58	0.46	1.16	2.35	ns
t_{PHL}			0.41	1.25	2.8	0.45	1.25	2.55	
t_{PLH}	PREZ	Q	0.31	0.76	1.61	0.33	0.76	1.48	ns
t_{PHL}		QZ	0.5	1.44	3.23	0.53	1.44	2.94	
Δt_{PLH}	C	Q	0.21	0.55	1.18	0.22	0.55	1.09	ns/pF
Δt_{PHL}			0.18	0.49	1.1	0.2	0.49	1	
Δt_{PLH}	C	QZ	0.21	0.54	1.14	0.22	0.54	1.05	ns/pF
Δt_{PHL}			0.2	0.48	1.05	0.21	0.48	0.95	
Δt_{PLH}	CLRZ	QZ	0.2	0.55	1.19	0.21	0.55	1.1	ns/pF
Δt_{PHL}		Q	0.21	0.49	1.1	0.21	0.49	1	
Δt_{PLH}	D	Q	0.21	0.55	1.19	0.23	0.55	1.09	ns/pF
Δt_{PHL}			0.21	0.49	1.09	0.21	0.49	0.99	
Δt_{PLH}	D	QZ	0.18	0.53	1.14	0.2	0.53	1.05	ns/pF
Δt_{PHL}			0.21	0.47	1.04	0.21	0.47	0.95	
Δt_{PLH}	PREZ	Q	0.22	0.56	1.15	0.23	0.56	1.06	ns/pF
Δt_{PHL}		QZ	0.19	0.52	1.16	0.21	0.52	1.05	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

LAH40LJ
D-TYPE TRANSPARENT LATCH WITH ACTIVE-HIGH ENABLE AND 4X OUTPUTS

D3030, MARCH 1989

INTERNAL LATCH CELL

FUNCTION TABLE

INPUTS		OUTPUTS	
D	C	Q	QZ
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

description

The LAH40LJ cell implements a D-type transparent latch with active-high enable and 4X drive outputs. Transparent latches have level-operated control inputs rather than edge- or pulse-triggered inputs. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Information present at the data input is transferred to the Q output when the enable input is high, and the Q output will follow the data input as long as enable remains high. When enable goes low, the data that was present at the data input when the transition occurred is retained at the Q output until enable is taken high.

When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: LAH40LJ D,C,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
t_w	Pulse duration, C high	1		ns
t_{su}	Setup time, D high or low	1.5		
t_h	Hold time, D high or low	0.1		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	D		0.09		pF
		C		0.1		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	2.12		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	C	Q	0.3	0.86	1.74	0.31	0.86	1.61	ns
t_{PHL}			0.27	0.81	1.78	0.29	0.81	1.63	
t_{PLH}	C	QZ	0.38	1.18	2.61	0.41	1.18	2.39	ns
t_{PHL}			0.38	1.24	2.72	0.42	1.24	2.49	
t_{PLH}	D	Q	0.23	0.65	1.43	0.24	0.65	1.32	ns
t_{PHL}			0.32	0.74	1.55	0.33	0.74	1.43	
t_{PLH}	D	QZ	0.39	1.07	2.41	0.41	1.07	2.21	ns
t_{PHL}			0.42	1.03	2.37	0.42	1.03	2.17	
Δt_{PLH}	C	Q	0.08	0.28	0.6	0.1	0.28	0.55	ns/pF
Δt_{PHL}			0.1	0.24	0.49	0.1	0.24	0.46	
Δt_{PLH}	C	QZ	0.11	0.24	0.5	0.11	0.24	0.47	ns/pF
Δt_{PHL}			0.1	0.23	0.43	0.1	0.23	0.4	
Δt_{PLH}	D	Q	0.12	0.28	0.57	0.13	0.28	0.53	ns/pF
Δt_{PHL}			0.08	0.22	0.5	0.09	0.22	0.45	
Δt_{PLH}	D	QZ	0.11	0.26	0.51	0.12	0.26	0.46	ns/pF
Δt_{PHL}			0.02	0.23	0.45	0.05	0.23	0.41	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

LAL20LJ
D-TYPE LATCH
WITH ACTIVE-LOW ENABLE AND 2X OUTPUTS

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUTS	
D	C	Q	QZ
L	L	L	H
H	L	H	L
X	H	Q_0	$\overline{Q}_0$

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The LAL20LJ cell implements a D-type latch with active-low enable and 2X drive outputs. Information present at the data input is transferred to the Q output when the enable input is high, and the Q output will follow the data input as long as enable remains high. When enable goes low, the data that was present at the data input at the time the transition occurred is retained at the Q output until enable is taken high. When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: LAL20LJ D,C,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
t_w	Pulse duration, C high	2		ns
t_{su}	Setup time, D high or low	2		
t_h	Hold time, D high or low	0		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	D		0.12		pF
		C		0.11		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	2.27		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	C	Q	0.55	1.61	3.84	0.58	1.61	3.49	ns
t_{PHL}			0.46	1.1	2.47	0.47	1.1	2.25	
t_{PLH}	C	QZ	0.58	1.69	4	0.61	1.69	3.63	ns
t_{PHL}			0.46	1.09	2.44	0.47	1.09	2.24	
t_{PLH}	D	Q	0.47	1.79	4.4	0.51	1.79	3.99	ns
t_{PHL}			0.41	1.1	2.62	0.42	1.1	2.38	
t_{PLH}	D	QZ	0.53	1.71	4.20	0.57	1.71	3.8	ns
t_{PHL}			0.31	1.24	2.96	0.34	1.24	2.71	
Δt_{PLH}	C	Q	0.21	0.5	1.04	0.22	0.5	0.96	ns/pF
Δt_{PHL}			0.13	0.42	0.91	0.15	0.42	0.83	
Δt_{PLH}	C	QZ	0.22	0.51	1.07	0.23	0.51	0.99	ns/pF
Δt_{PHL}			0.13	0.42	0.92	0.15	0.42	0.84	
Δt_{PLH}	D	Q	0.19	0.5	1.04	0.2	0.5	0.96	ns/pF
Δt_{PHL}			0.13	0.42	0.93	0.15	0.42	0.86	
Δt_{PLH}	D	QZ	0.22	0.52	1.08	0.23	0.52	1	ns/pF
Δt_{PHL}			0.16	0.42	0.94	0.18	0.42	0.85	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

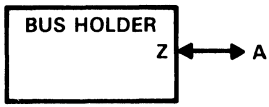
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

LH110LJ
3-STATE BUS HOLDER

D3030, APRIL 1988

INTERNAL CELL

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The LH110LJ cell implements a bus-holder latch. When driven to either a high logic level or low logic level, the output of the holder latch reinforces or maintains the bus state. The holder is particularly useful in providing stable bus levels during a system period when all 3-state bus drivers transition through the high-impedance state prior to the next driven level. When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: LH110LJ A;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
$C_{i/o}$	Input/output capacitance	A		0.07		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.17		pF

TAB20LJ
TOGGLE FLIP-FLOP
WITH PRESET, CLEAR, AND 2X OUTPUTS

D3030, APRIL 1988

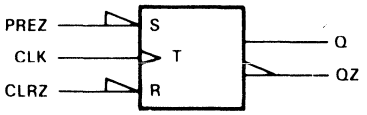
INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
PREZ	CLRZ	CLK	Q	QZ
L	H	X	H	L
H	L	X	L	H
L	L	X	L*	L*
H	H	↑	$\overline{Q}_0$	Q_0
H	H	L	Q_0	$\overline{Q}_0$

* This configuration is nonstable; that is, it will not persist when PREZ or CLRZ returns to its inactive (high) level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TAB20LJ cell implements a toggle flip-flop with preset and clear inputs. The flip-flop can be used as a stand-alone bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TAB20LJ CLRZ,PREZ,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	145	MHz
t_w	Pulse duration	CLRZ low	3		ns
		PREZ low	3		
		CLK high or low	3.4		
t_{su}	Setup time before clock	CLRZ inactive (high)	3		ns
		PREZ inactive (high)	0		
t_h	Hold time after clock	CLRZ active (low)	0		ns
		PREZ active (low)	0.75		

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TAB20LJ
TOGGLE FLIP-FLOP
WITH PRESET, CLEAR, AND 2X OUTPUTS

D3030, APRIL 1988

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLRZ		0.11		pF
		PREZ		0.16		
		CLK		0.15		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.61		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.65	2.03	4.91	0.69	2.03	4.43	ns
t_{PHL}			0.44	1.34	3.24	0.45	1.34	2.94	
t_{PLH}	CLK	QZ	0.61	1.95	4.74	0.64	1.95	4.28	ns
t_{PHL}			0.46	1.32	3.13	0.47	1.32	2.85	
t_{PLH}	CLRZ	QZ	0.55	1.56	3.59	0.59	1.56	3.28	ns
t_{PHL}		Q	0.34	0.84	1.82	0.36	0.84	1.68	
t_{PLH}	PREZ	Q	0.53	1.55	3.61	0.56	1.55	3.28	ns
t_{PHL}		QZ	0.32	0.8	1.7	0.33	0.8	1.5	
Δt_{PLH}	CLK	Q	0.2	0.56	1.2	0.22	0.56	1.12	ns/pF
Δt_{PHL}			0.16	0.38	0.78	0.18	0.38	0.7	
Δt_{PLH}	CLK	QZ	0.2	0.54	1.16	0.22	0.54	1.08	ns/pF
Δt_{PHL}			0.16	0.38	0.78	0.18	0.38	0.7	
Δt_{PLH}	CLRZ	QZ	0.2	0.54	1.2	0.2	0.54	1.08	ns/pF
Δt_{PHL}		Q	0.16	0.38	0.82	0.16	0.38	0.74	
Δt_{PLH}	PREZ	Q	0.2	0.56	1.24	0.22	0.56	1.14	ns/pF
Δt_{PHL}		QZ	0.14	0.34	0.74	0.16	0.34	0.68	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TAC20LJ
TOGGLE FLIP-FLOP
WITH CLEAR AND 2X OUTPUTS

D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUTS	
CLRZ	CLK	Q	QZ
L	X	L	H
H	↑	$\overline{Q}_0$	Q_0
H	L	Q_0	$\overline{Q}_0$

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TAC20LJ cell implements a toggle flip-flop with clear input. The flip-flop can be used as a stand-alone bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TAC20LJ CLRZ,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	165	MHz
t_w	Pulse duration	CLRZ low	3		ns
		CLK high or low	3		
t_{su}	Setup time before clock	CLRZ inactive (high)	2		ns
t_h	Hold time after clock	CLRZ active (low)	0		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLRZ		0.16		pF
		CLK		0.11		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.72		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TAC20LJ
TOGGLE FLIP-FLOP
WITH CLEAR AND 2X OUTPUTS

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.63	1.96	4.69	0.68	1.96	4.24	ns
t_{PHL}			0.41	1.2	2.76	0.44	1.2	2.52	
t_{PLH}	CLK	QZ	0.53	1.66	3.85	0.57	1.66	3.49	ns
t_{PHL}			0.46	1.27	2.93	0.47	1.27	2.66	
t_{PLH}	CLRZ	QZ	0.54	1.4	3.2	0.56	1.4	2.91	ns
t_{PHL}		Q	0.34	0.84	1.82	0.37	0.84	1.68	
Δt_{PLH}	CLK	Q	0.2	0.54	1.2	0.2	0.54	1.1	ns/pF
Δt_{PHL}			0.14	0.36	0.78	0.14	0.36	0.7	
Δt_{PLH}	CLK	QZ	0.2	0.5	1.1	0.22	0.5	1.02	ns/pF
Δt_{PHL}			0.14	0.34	0.76	0.16	0.34	0.68	
Δt_{PLH}	CLRZ	QZ	0.18	0.52	1.1	0.2	0.52	1.02	ns/pF
Δt_{PHL}		Q	0.14	0.36	0.8	0.14	0.36	0.72	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TAP20LJ
TOGGLE FLIP-FLOP
WITH PRESET AND 2X OUTPUTS

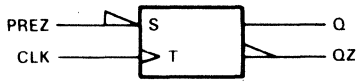
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUTS	
PREZ	CLK	Q	QZ
L	X	H	L
H	↑	$\overline{Q}_0$	Q_0
H	L	Q_0	$\overline{Q}_0$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TAP20LJ cell implements a toggle flip-flop with preset input. The flip-flop can be used as a stand-alone bit-storage device or as an addition to larger synchronous functions such as registers or counters. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TAP20LJ PREZ,CLK,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	165	MHz
t_w	Pulse duration	PREZ low	3		ns
		CLK high or low	3		
t_{su}	Setup time before clock	PREZ inactive (high)	0		ns
t_h	Hold time after clock	PREZ active (low)	0.5		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	PREZ		0.16		pF
		CLK		0.12		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	2.07		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.56	1.7	3.9	0.61	1.7	3.55	ns
t_{PHL}			0.44	1.31	3.09	0.44	1.31	2.81	
t_{PLH}	CLK	QZ	0.62	1.87	4.54	0.66	1.87	4.11	ns
t_{PHL}			0.41	1.15	2.6	0.43	1.15	2.38	
t_{PLH}	PREZ	Q	0.48	1.37	3.09	0.52	1.37	2.83	ns
t_{PHL}		QZ	0.29	0.8	1.73	0.32	0.8	1.58	
Δt_{PLH}	CLK	Q	0.22	0.54	1.16	0.22	0.54	1.06	ns/pF
Δt_{PHL}			0.14	0.36	0.78	0.18	0.36	0.7	
Δt_{PLH}	CLK	QZ	0.18	0.56	1.18	0.18	0.56	1.08	ns/pF
Δt_{PHL}			0.14	0.36	0.74	0.16	0.36	0.66	
Δt_{PLH}	PREZ	Q	0.22	0.54	1.18	0.22	0.54	1.06	ns/pF
Δt_{PHL}		QZ	0.16	0.34	0.7	0.16	0.34	0.64	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TDB10LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH CLEAR AND 1X OUTPUTS

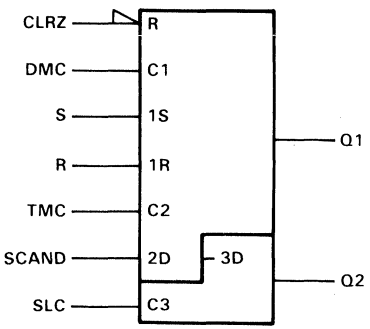
D3030, MARCH 1989

INTERNAL MACRO

FUNCTION TABLE

INPUTS							OUTPUTS	
DATA PATH			SCAN PATH		MASTER	SLAVE	MASTER SLAVE	
S	R	DMC	SCAND	TMC	CLRZ	SLC	Q1	Q2
X	X	X	X	X	L	L	L	$Q2_0$
X	X	X	X	X	L	H	L	L
X	X	L	X	L	H	L	$Q1_0$	$Q2_0$
L	L	H	X	L	H	L	$Q1_0$	$Q2_0$
H	X	H	X	L	H	L	H	$Q2_0$
L	H	H	X	L	H	L	L	$Q2_0$
X	X	L	d1	H	H	L	d1	$Q2_0$
X	X	H	X	H	H	L	?	$Q2_0$
X	X	L	X	L	H	H	$Q1_0$	$Q1_0$
L	L	H	X	L	H	H	$Q1_0$	$Q1_0$
H	X	H	X	L	H	H	H	H
L	H	H	X	L	H	H	L	L
X	X	L	d1	H	H	H	d1	d1
X	X	H	X	H	H	H	?	?

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TDB10LJ implements a scan-input R-S/D-type latch with 1X drive master and slave outputs. The cell consists of an R-S/D-type master input data and scan-data latch with active-low clear and a single slave latch. In the data- or scan-path mode, either DMC or TMC can be used to select the entry and storage of data. When TMC is low and DMC is high, the Q1 output follows the R-S inputs. When DMC is subsequently taken low, the Q1 output is latched. When DMC is low and TMC is high, the Q1 output follows the SCAND input. When TMC is subsequently taken low, the Q1 output is latched. Data entered is available to the slave output latch, which follows the selected master input latch while SLC is high. Data at the Q2 output can be latched by taking SLC low. The clock generator, CK120LJ, provides nonoverlapping clock signals timed specifically for driving the DMC, TMC, and SLC clocks. When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TDB10LJ DMC,TMC,SLC,S,R,SCAND,CLRZ,Q1,Q2;

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TDB10LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH CLEAR AND 1X OUTPUTS

D3030, MARCH 1989

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

			MIN	MAX	UNIT
f_{opr}	Operating frequency			76	MHz
t_w	Pulse duration	CLRZ low	3		ns
		DMC or TMC high	3		
		SLC high	3		
		R-S high	3		
t_{su}	Setup time	S high or low before DMC↓	4		ns
		R high or low before DMC↓	4		
		SCAND high or low before TMC↓	3		
		DMC or TMC low before SLC↑ (nonoverlap)	3.5		
		SLC low before DMC or TMC↑ (nonoverlap)	3.5		
t_h	Hold time	R-S high or low after DMC↓	0		ns
		SCAND high or low after TMC↓	0		
		DMC or TMC low after SLC↓ (nonoverlap)	3.5		

NOTE 1: Additional timing data regarding pulse-duration, setup-time, and hold-time models are incorporated in the engineering workstation library.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLRZ		0.23		pF
		DMC		0.04		
		R		0.05		
		S		0.09		
		SCAND		0.06		
		SLC		0.03		
		TMC		0.04		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLRZ	Q1	0.44	1.15	2.61	0.47	1.15	2.36	ns
t_{PHL}			0.34	1.08	2.65	0.36	1.08	2.45	
t_{PLH}	CLRZ	Q2	0.57	1.7	4.07	0.6	1.7	3.7	ns
t_{PHL}			0.56	1.67	4.1	0.58	1.67	3.74	
t_{PLH}	DMC	Q1	0.3	0.87	1.88	0.32	0.87	1.73	ns
t_{PHL}			0.48	1.12	2.48	0.48	1.12	2.32	
t_{PLH}	DMC	Q2	0.41	1.42	3.35	0.45	1.42	3.06	ns
t_{PHL}			0.71	1.72	3.95	0.72	1.72	3.64	
t_{PLH}	R	Q1	0.38	1.57	3.89	0.43	1.57	3.57	ns
t_{PHL}		Q2	0.61	2.18	5.39	0.65	2.18	4.92	
t_{PLH}	S	Q1	0.55	1.23	2.7	0.57	1.23	2.44	ns
t_{PHL}			0.36	1.39	3.61	0.38	1.39	3.31	
t_{PLH}	S	Q2	0.69	1.79	4.15	0.72	1.79	3.77	ns
t_{PHL}			0.56	2	5.09	0.59	2	4.64	
t_{PLH}	SCAND	Q1	0.48	1.04	2.23	0.5	1.04	2.04	ns
t_{PHL}			0.37	1.14	2.8	0.38	1.14	2.58	
t_{PLH}	SCAND	Q2	0.61	2.59	3.7	0.65	2.59	3.37	ns
t_{PHL}			0.61	1.76	4.25	0.63	1.76	3.89	
t_{PLH}	SLC	Q2	0.41	0.92	1.78	0.42	0.92	1.68	ns
t_{PHL}			0.15	0.68	1.55	0.17	0.68	1.42	
t_{PLH}	TMC	Q1	0.3	0.89	1	0.32	0.89	1.75	ns
t_{PHL}			0.47	1.11	2.46	0.48	1.11	2.29	
t_{PLH}	TMC	Q2	0.42	1.42	3.37	0.45	1.42	3.08	ns
t_{PHL}			0.7	1.71	3.91	0.72	1.71	3.59	
Δt_{PLH}	CLRZ	Q1	0.42	1.12	2.4	0.45	1.12	2.2	ns/pF
Δt_{PHL}			0.38	1.11	2.57	0.41	1.11	2.34	
Δt_{PLH}	CLRZ	Q2	0.43	1.09	2.29	0.46	1.09	2.1	ns/pF
Δt_{PHL}			0.33	0.73	1.44	0.36	0.73	1.3	
Δt_{PLH}	DMC	Q1	0.42	1.12	2.4	0.45	1.12	2.2	ns/pF
Δt_{PHL}			0.38	1.12	2.59	0.41	1.12	2.35	
Δt_{PLH}	DMC	Q2	0.43	1.1	2.29	0.46	1.1	2.11	ns/pF
Δt_{PHL}			0.34	0.73	1.44	0.37	0.73	1.29	
Δt_{PLH}	R	Q1	0.39	1.12	2.58	0.41	1.12	2.35	ns/pF
Δt_{PHL}		Q2	0.33	0.73	1.43	0.36	0.73	1.29	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	S	Q1	0.43	1.13	2.39	0.46	1.13	2.2	ns/pF
Δt_{PHL}			0.37	1.12	2.57	0.4	1.12	2.34	
Δt_{PLH}	S	Q2	0.43	1.1	2.29	0.46	1.1	2.11	ns/pF
Δt_{PHL}			0.33	0.73	1.44	0.36	0.73	1.29	
Δt_{PLH}	SCAND	Q1	0.41	1.12	2.39	0.44	1.12	2.19	ns/pF
Δt_{PHL}			0.37	1.12	2.58	0.4	1.12	2.35	
Δt_{PLH}	SCAND	Q2	0.43	1.1	2.29	0.45	1.1	2.11	ns/pF
Δt_{PHL}			0.32	0.72	1.44	0.35	0.72	1.3	
Δt_{PLH}	SLC	Q2	0.43	1.1	2.3	0.46	1.1	2.11	ns/pF
Δt_{PHL}			0.33	0.73	1.47	0.36	0.73	1.32	
Δt_{PLH}	TMC	Q1	0.42	1.11	2.39	0.45	1.11	2.19	ns/pF
Δt_{PHL}			0.38	1.12	2.58	0.41	1.12	2.35	
Δt_{PLH}	TMC	Q2	0.43	1.1	2.29	0.46	1.1	2.11	ns/pF
Δt_{PHL}			0.34	0.73	1.44	0.37	0.73	1.3	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

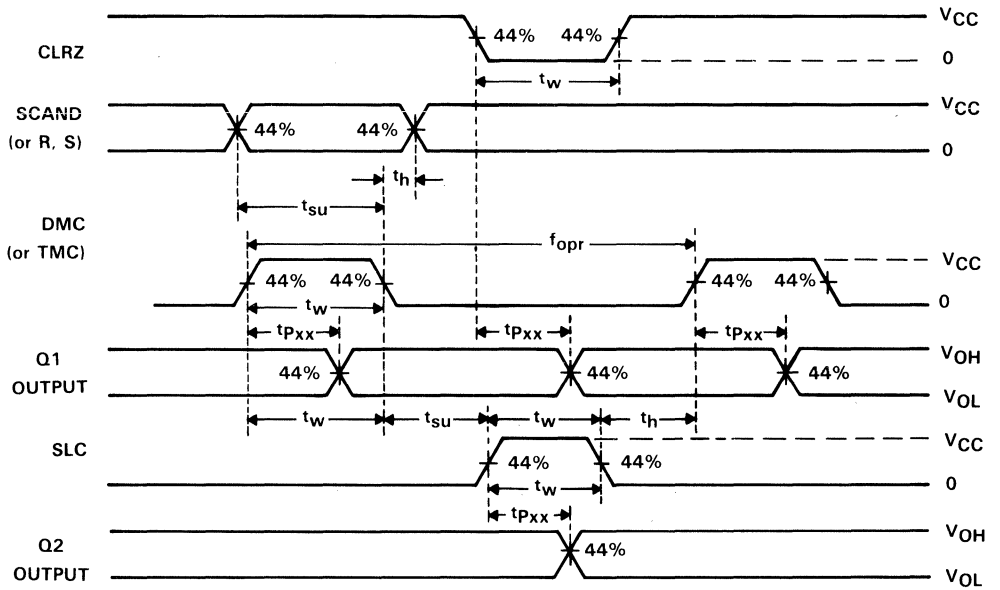
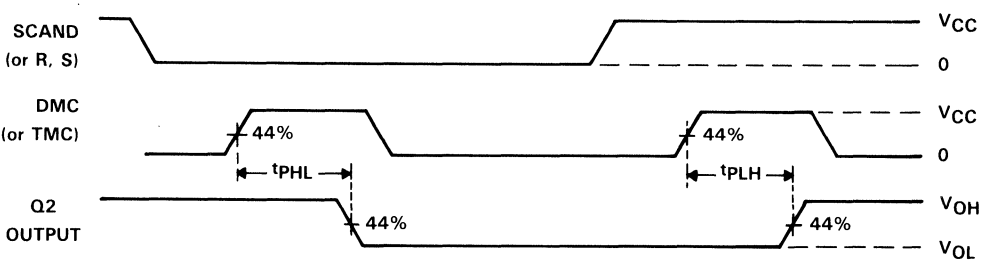


FIGURE 1. TIMING DIAGRAM

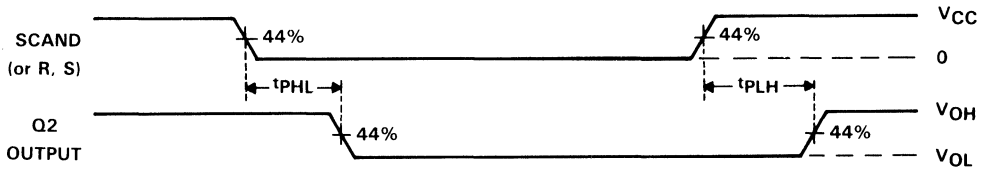


NOTE: SLC is high.

FIGURE 2. DMC OR TMC TO Q2 TIMING DIAGRAM

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



NOTE: DMC, TMC, SLC are high.

FIGURE 3. SCAND (OR R-S) TO Q2 OR QZ2 TIMING DIAGRAM

TDC10LJ
SCAN-INPUT D-TYPE FLIP-FLOP WITH CLEAR AND 1X OUTPUTS

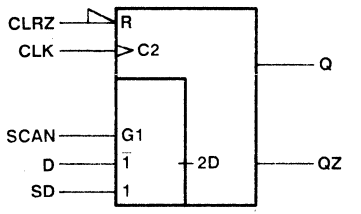
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUTS	
CLRZ	CLK	SCAN	D	SD	Q	QZ
L	X	X	X	X	L	H
H	↑	L	L	X	L	H
H	↑	L	H	X	H	L
H	↑	H	X	L	L	H
H	↑	H	X	H	H	L
H	L	X	X	X	Q_0	$\overline{Q}_0$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TDC10LJ cell implements a scan-input D-type flip-flop with clear and 1X drive outputs. The cell functions as a D-type flip-flop with data input from a 2-to-1 multiplexer that selects either the D or SD input, depending on the level of the SCAN input. When the clear input is inactive (H) and the clock input makes a low-to-high transition, the state of each complementary output Q and QZ will be determined by the state of the selected D or SD input logic level. While the clock CLK remains high or transitions to the low level and remains low, the outputs will remain stable while the clear is inactive. The cell provides intentionally long setup times in the scan data (SD) path to simplify implementation of the serial clocking scheme required for shifting data through the scan data path. Conventional implementation of the data (D) path produces relatively short setup times that support normal operating frequency ranges.

When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TDC10LJ CLRZ,CLK,SCAN,D,SD,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TDC10LJ
SCAN-INPUT D-TYPE FLIP-FLOP WITH CLEAR AND 1X OUTPUTS

D3030, APRIL 1988

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency	SCAN low	0	135	MHz
		SCAN high	0	32.5	
t_w	Pulse duration	CLRZ low	3		ns
		CLK high or low	3.7		
t_{su}	Setup time before clock↑	CLRZ inactive (high)	0		ns
		D high or low	3.5		
		SD high or low	27		
		SCAN high or low	12		
t_h	Hold time after clock↑	CLRZ active (low)	3		ns
		D high or low	0		
		SD high or low	0		
		SCAN high or low	0		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLRZ		0.08		pF
		CLK, SD		0.05		
		D, SCAN		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.16		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.53	1.31	2.84	0.55	1.31	2.6	ns
t_{PHL}			0.62	1.54	3.41	0.64	1.54	3.12	
t_{PLH}	CLK	QZ	0.49	1.19	2.55	0.51	1.19	2.34	ns
t_{PHL}			0.5	1.17	2.52	0.51	1.17	2.33	
t_{PLH}	CLRZ	Q	0.26	0.54	1.06	0.27	0.54	0.98	ns
t_{PHL}		QZ	0.57	1.61	3.79	0.6	1.61	3.44	
Δt_{PLH}	CLK	Q	0.46	1.17	2.46	0.49	1.17	2.26	ns/pF
Δt_{PHL}			0.33	0.74	1.47	0.36	0.74	1.33	
Δt_{PLH}	CLK	QZ	0.5	1.31	2.77	0.54	1.31	2.54	ns/pF
Δt_{PHL}			0.36	0.85	1.75	0.39	0.85	1.58	
Δt_{PLH}	CLRZ	Q	0.35	0.74	1.49	0.37	0.74	1.34	ns/pF
Δt_{PHL}		QZ	0.5	1.31	2.79	0.53	1.31	2.56	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TDC11LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH MASTER CLEAR AND MASTER AND SLAVE 1X OUTPUTS

D3030, APRIL 1988

INTERNAL CELL

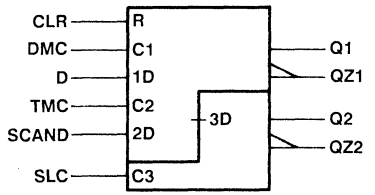
FUNCTION TABLE

INPUTS						OUTPUTS			
MASTER	DATA PATH		SCAN PATH		SLAVE	MASTER		SLAVE	
CLR	D	DMC	SCAND	TMC	SLC	Q1	QZ1	Q2	QZ2
H	X	X	X	X	X	L	H	L	H
L	X	L	X	L	L	$Q1_0$	$\overline{Q1}_0$	$Q2_0$	$\overline{Q2}_0$
L	d1	H	X	L	L	d1	$\overline{d1}$	$Q2_0$	$\overline{Q2}_0$
L	X	L	d2	H	L	d2	$\overline{d2}$	$Q2_0$	$\overline{Q2}_0$
L	d1	H	d2	H	L	?	?	$Q2_0$	$\overline{Q2}_0$
L	X	L	X	L	H	$Q1_0$	$\overline{Q1}_0$	$Q1_0$	$\overline{Q1}_0$
L	d1	H	X	L	H	d1	$\overline{d1}$	d1	$\overline{d1}$
L	X	L	d2	H	H	d2	$\overline{d2}$	d2	$\overline{d2}$
L	d1	H	d2	H	H	?	?	?	?

description

The TDC11LJ cell implements a scan-input D-type latch with 1X-drive master and slave outputs. The cell consists of a dual D-type master input-data and scan-data latch with active-high clear and complementary outputs and a single slave latch with complementary outputs. In the data- or scan-path mode, either DMC or TMC can be used to select the entry and storage of data. When TMC is low and DMC is high, the Q1 output follows the D input. When DMC is subsequently taken low, the Q1 output is latched. When DMC is low and TMC is high, the Q1 output follows the SCAND input. When TMC is subsequently taken low, the Q1 output is latched. Data entered is available to the slave output latch, which follows the selected master input latch while SLC is high. Data at the Q2 and QZ2 outputs can be latched by taking SLC low.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TDC11LJ D,SCAND,CLR,DMC,TMC,SLC,Q1,QZ1,Q2,QZ2;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

			MIN	MAX	UNIT
f_{opr}	Operating frequency		0	100	MHz
t_w	Pulse duration	CLR high	3.5		ns
		DMC or TMC high	2.5		
		SLC high	2.5		
t_{su}	Setup time	D high or low before DMC↓	3		ns
		SCAND high or low before TMC↓	3		
		DMC or TMC low before SLC↑ (nonoverlap)	2.5		
t_h	Hold time	D high or low after DMC↓	0		ns
		SCAND high or low after TMC↓	0		
		DMC or TMC low after SLC↓ (nonoverlap)	2.5		

NOTE 1: Additional timing data regarding pulse-duration, setup-time, and hold-time are incorporated in the engineering workstation library.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2		V
C_i	Input capacitance	CLR		0.08		pF
		D, SCAND		0.06		
		DMC, TMC		0.04		
		SLC		0.03		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.38		pF

TDC11LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH MASTER CLEAR AND MASTER AND SLAVE 1X OUTPUTS

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLR	QZ1	0.61	1.55	3.75	0.61	1.55	3.45	ns
t_{PHL}		Q1	0.46	1.17	2.82	0.46	1.17	2.6	
t_{PLH}	CLR	QZ2	0.62	1.7	4.18	0.63	1.7	3.83	ns
t_{PHL}		Q2	0.75	1.99	4.88	0.76	1.99	4.46	
t_{PLH}	D	Q1	0.42	0.93	1.94	0.44	0.93	1.76	ns
t_{PHL}			0.32	1.04	2.54	0.34	1.04	2.35	
t_{PLH}	D	QZ1	0.47	1.42	3.48	0.48	1.42	3.2	ns
t_{PHL}			0.57	1.46	3.19	0.6	1.46	2.9	
t_{PLH}	D	Q2	0.63	1.75	4.07	0.66	1.75	3.71	ns
t_{PHL}			0.6	1.89	4.64	0.63	1.89	4.24	
t_{PLH}	D	QZ2	0.49	1.59	3.93	0.51	1.59	3.6	ns
t_{PHL}			0.56	1.72	4.11	0.6	1.72	3.75	
t_{PLH}	DMC	Q1	0.24	0.75	1.6	0.26	0.75	1.48	ns
t_{PHL}			0.46	1.04	2.26	0.47	1.04	2.11	
t_{PLH}	DMC	QZ1	0.62	1.42	3.19	0.63	1.42	2.96	ns
t_{PHL}			0.4	1.29	2.85	0.43	1.29	2.61	
t_{PLH}	DMC	Q2	0.4	1.56	3.72	0.44	1.56	3.41	ns
t_{PHL}			0.77	1.9	4.34	0.79	1.9	3.99	
t_{PLH}	DMC	QZ2	0.64	1.57	3.63	0.66	1.57	3.35	ns
t_{PHL}			0.38	1.55	3.77	0.42	1.55	3.47	
t_{PLH}	SCAND	Q1	0.42	0.93	1.93	0.44	0.93	1.76	ns
t_{PHL}			0.32	1.03	2.54	0.34	1.03	2.35	
t_{PLH}	SCAND	QZ1	0.47	1.42	3.49	0.48	1.42	3.21	ns
t_{PHL}			0.58	1.47	3.2	0.61	1.47	2.91	
t_{PLH}	SCAND	Q2	0.63	1.75	4.06	0.66	1.75	3.71	ns
t_{PHL}			0.6	1.89	4.64	0.63	1.89	4.24	
t_{PLH}	SCAND	QZ2	0.48	1.58	3.93	0.5	1.58	3.6	ns
t_{PHL}			0.56	1.72	4.11	0.6	1.72	3.75	
t_{PLH}	SLC	Q2	0.48	1	2.03	0.49	1	1.9	ns
t_{PHL}			0.25	0.81	1.79	0.26	0.81	1.66	
t_{PLH}	SLC	QZ2	0.13	0.5	1.08	0.14	0.5	1	ns
t_{PHL}			0.45	0.98	2.1	0.45	0.98	1.97	
t_{PLH}	TMC	Q1	0.24	0.75	1.6	0.26	0.75	1.48	ns
t_{PHL}			0.46	1.04	2.26	0.47	1.04	2.11	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	TMC	QZ1	0.62	1.42	3.19	0.63	1.42	2.96	ns
t_{PHL}			0.4	1.29	2.86	0.43	1.29	2.61	
t_{PLH}	TMC	Q2	0.4	1.56	3.72	0.44	1.56	3.41	ns
t_{PHL}			0.77	1.9	4.34	0.79	1.9	3.99	
t_{PLH}	TMC	QZ2	0.64	1.57	3.63	0.66	1.57	3.35	ns
t_{PHL}			0.38	1.55	3.77	0.42	1.55	3.47	
Δt_{PLH}	CLR	QZ1	0.4	1.07	2.25	0.44	1.07	2.07	ns/pF
Δt_{PHL}		Q1	0.38	1.07	2.41	0.41	1.07	2.19	
Δt_{PLH}	CLR	QZ2	0.43	1.08	2.27	0.46	1.08	2.09	ns/pF
Δt_{PHL}		Q2	0.32	0.73	1.43	0.35	0.73	1.29	
Δt_{PLH}	D	Q1	0.43	1.11	2.38	0.45	1.11	2.18	ns/pF
Δt_{PHL}			0.38	1.07	2.4	0.41	1.07	2.19	
Δt_{PLH}	D	QZ1	0.41	1.07	2.25	0.44	1.07	2.07	ns/pF
Δt_{PHL}			0.34	0.74	1.48	0.37	0.74	1.34	
Δt_{PLH}	D	Q2	0.43	1.08	2.27	0.46	1.08	2.09	ns/pF
Δt_{PHL}			0.32	0.72	1.43	0.35	0.72	1.29	
Δt_{PLH}	D	QZ2	0.43	1.08	2.27	0.46	1.08	2.09	ns/pF
Δt_{PHL}			0.37	0.95	2.11	0.39	0.95	1.92	
Δt_{PLH}	DMC	Q1	0.43	1.11	2.37	0.45	1.11	2.18	ns/pF
Δt_{PHL}			0.38	1.06	2.4	0.4	1.06	2.18	
Δt_{PLH}	DMC	QZ1	0.4	1.08	2.26	0.44	1.08	2.08	ns/pF
Δt_{PHL}			0.33	0.74	1.51	0.36	0.74	1.36	
Δt_{PLH}	DMC	Q2	0.44	1.09	2.27	0.47	1.09	2.09	ns/pF
Δt_{PHL}			0.32	0.72	1.43	0.35	9.72	1.29	
Δt_{PLH}	DMC	QZ1	0.42	1.09	2.27	0.45	1.09	2.09	ns/pF
Δt_{PHL}			0.37	0.95	2.11	0.39	0.95	1.91	
Δt_{PLH}	SCAND	Q1	0.43	1.11	2.37	0.45	1.11	2.18	ns/pF
Δt_{PHL}			0.38	1.07	2.4	0.41	1.07	2.18	
Δt_{PLH}	SCAND	QZ1	0.41	1.07	2.26	0.44	1.07	2.08	ns/pF
Δt_{PHL}			0.34	0.74	1.49	0.37	0.74	1.35	
Δt_{PLH}	SCAND	Q2	0.43	1.08	2.27	0.46	1.08	2.09	ns/pF
Δt_{PHL}			0.32	0.72	1.43	0.35	0.72	1.29	
Δt_{PLH}	SCAND	QZ2	0.43	1.05	2.27	0.46	1.08	2.09	ns/pF
Δt_{PHL}			0.37	0.95	2.11	0.39	0.95	1.92	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	SLC	Q2	0.4	1.1	2.28	0.44	1.1	2.1	ns/pF
Δt_{PHL}			0.32	0.74	1.48	0.35	0.74	1.33	
Δt_{PLH}	SLC	QZ2	0.4	1.09	2.32	0.44	1.09	2.13	ns/pF
Δt_{PHL}			0.35	0.95	2.12	0.38	0.95	1.92	
Δt_{PLH}	TMC	Q1	0.43	1.11	2.37	0.45	1.11	2.18	ns/pF
Δt_{PHL}			0.38	1.06	2.4	0.4	1.06	2.18	
Δt_{PLH}	TMC	QZ1	0.4	1.08	2.26	0.44	1.08	2.08	ns/pF
Δt_{PHL}			0.33	0.74	1.51	0.36	0.74	1.36	
Δt_{PLH}	TMC	Q2	0.44	1.09	2.27	0.47	1.09	2.09	ns/pF
Δt_{PHL}			0.32	0.72	1.43	0.35	0.72	1.29	
Δt_{PLH}	TMC	QZ1	0.42	1.09	2.27	0.45	1.09	2.09	ns/pF
Δt_{PHL}			0.37	0.75	2.11	0.39	0.95	1.91	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

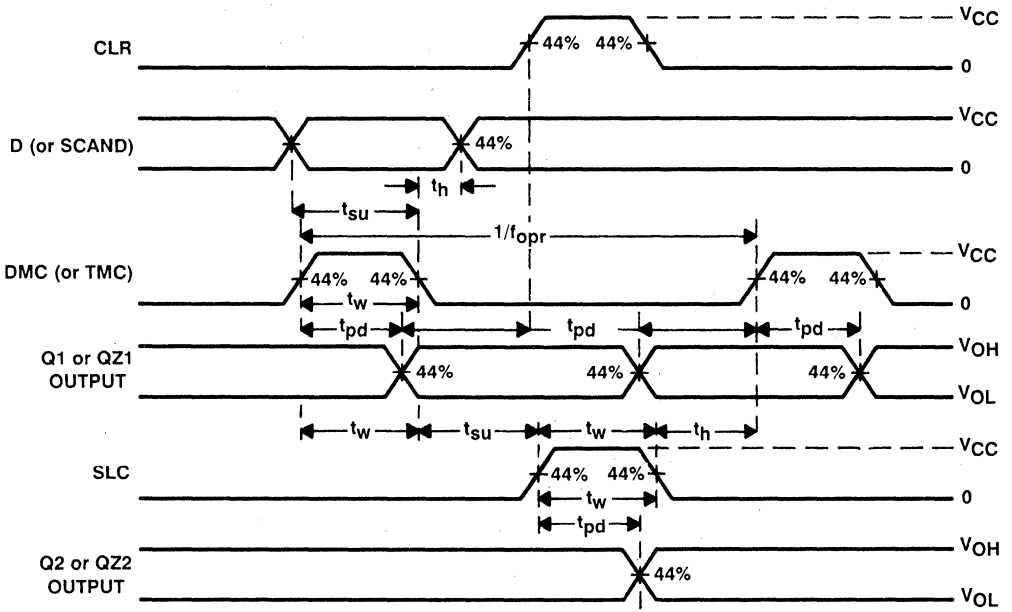
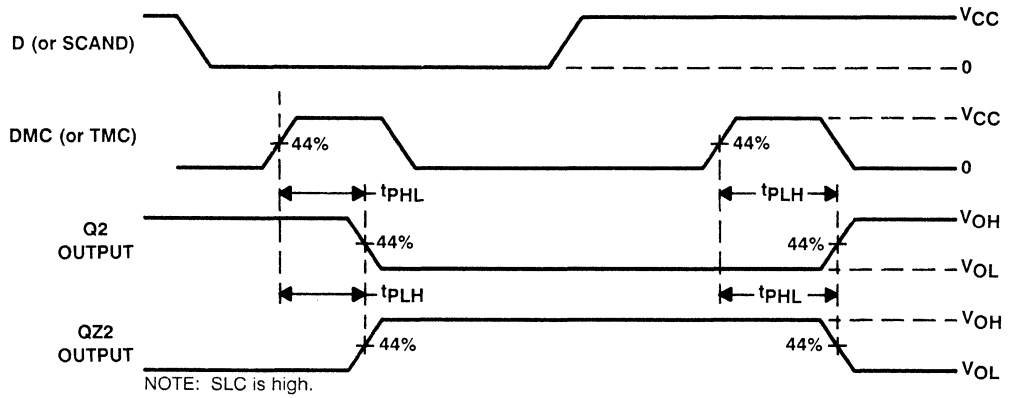


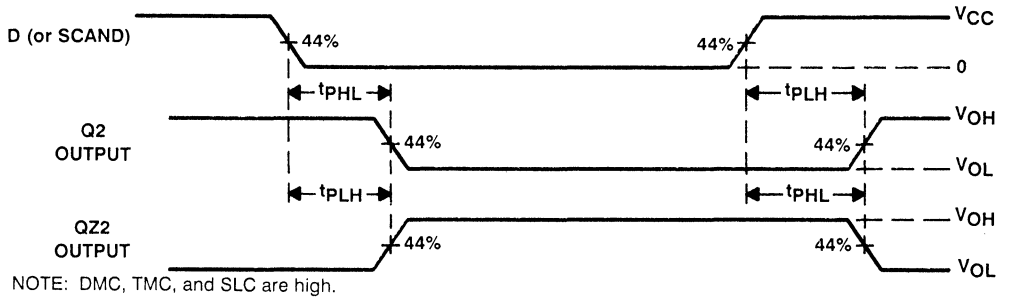
FIGURE 1. TIMING DIAGRAM

PARAMETER MEASUREMENT INFORMATION



NOTE: SLC is high.

FIGURE 2. DMC OR TMC TO Q2 OR QZ2 TIMING DIAGRAM



NOTE: DMC, TMC, and SLC are high.

FIGURE 3. D OR SCAND TO Q2 OR QZ2 TIMING DIAGRAM

TDN10LJ
SCAN-INPUT D-TYPE FLIP-FLOP WITH 1X OUPUTS

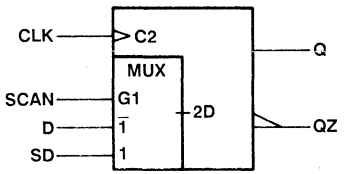
D3030, AUGUST 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUTS	
CLK	SCAN	D	SD	Q	QZ
↑	L	L	X	L	H
↑	L	H	X	H	L
↑	H	X	L	L	H
↑	H	X	H	H	L
L	X	X	X	Q_0	$\overline{Q}_0$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TDN10LJ cell implements a scan-input D-type flip-flop with 1X drive outputs. The cell functions as a D-type flip-flop with data input from a 2-to-1 multiplexer that selects either the D or SD input, depending on the level of the SCAN input. When the clock input makes a low-to-high transition, the state of each complementary output Q and QZ will be determined by the state of the selected D or SD input logic level. While the clock CLK remains high or transitions to the low level and remains low, the outputs will remain stable. The cell provides intentionally long setup times in the scan data (SD) path to simplify implementation of the serial clocking scheme required for shifting data through the scan data path. Conventional implementation of the data (D) path produces relatively short setup times that support normal operating frequency ranges.

When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TDN10LJ CLK,SCAN,D,SD,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

TDN10LJ
SCAN-INPUT D-TYPE FLIP-FLOP WITH 1X OUTPUTS

D3030, AUGUST 1988

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency	SCAN low	0	155	MHz
		SCAN high	0	35	
t_w	Pulse duration	CLK high or low	3.2		ns
t_{su}	Setup time before clock	D high or low	3		ns
		SD high or low	24		
		SCAN high or low	9		
t_h	Hold time after clock	D high or low	0		ns
		SD high or low	0		
		SCAN high or low	0		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK, SD		0.05		pF
		D, SCAN		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.94		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.6	1.46	3.19	0.63	1.46	2.93	ns
t_{PHL}			0.52	1.34	2.89	0.55	1.34	2.65	
t_{PLH}	CLK	QZ	0.43	1.01	2.12	0.45	1.01	1.95	ns
t_{PHL}			0.49	1.15	2.45	0.51	1.15	2.26	
Δt_{PLH}	CLK	Q	0.4	1.06	2.21	0.43	1.06	2.03	ns/pF
Δt_{PHL}			0.34	0.74	1.47	0.37	0.74	1.33	
Δt_{PLH}	CLK	QZ	0.43	1.13	2.37	0.46	1.13	2.18	ns/pF
Δt_{PHL}			0.53	1.17	2.37	0.57	1.17	2.13	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TDN11LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH 1X OUTPUTS

D3030, APRIL 1988

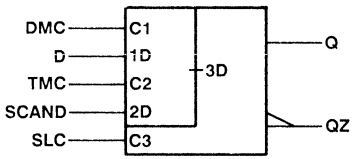
INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUTS	
DATA PATH		SCAN PATH		SLAVE		
D	DMC	SCAND	TMC	SLC	Q	QZ
X	L	X	L	L	Q_0	$\overline{Q}_0$
d1	H	X	L	L	Q_0	$\overline{Q}_0$
X	L	d2	H	L	Q_0	$\overline{Q}_0$
d1	H	d2	H	L	Q_0	$\overline{Q}_0$
X	L	X	L	H	Q_0'	$\overline{Q}_0'$
d1	H	X	L	H	d1	$\overline{d1}$
X	L	d2	H	H	d2	$\overline{d2}$
d1	H	d2	H	H	?	?

Q_0' = state of master latch setup prior to DMC and TMC both being low.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TDN11LJ cell implements a scan-input D-type latch with 1X-drive outputs. The cell consists of a dual D-type input master latch for data and scan data, and a single slave latch with complementary outputs. In the data- or scan-path mode, either DMC or TMC can select the entry and storage of data. When TMC is low and DMC is high, the Q1 output follows the D input. When DMC is subsequently taken low, the Q1 output is latched. When DMC is low and TMC is high, the Q1 output follows the SCAND input. When TMC is subsequently taken low, the Q1 output is latched. Data entered is available to the slave output latch, which follows the selected master input latch while SLC is high. Data at the Q and QZ outputs can be latched by taking SLC low.

When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TDN11LJ D,SCAND,DMC,TMC,SLC,Q,QZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

			MIN	MAX	UNIT
f_{opr}	Operating frequency		0	100	MHz
t_w	Pulse duration	DMC or TMC high	2.5		ns
		SLC high	2.5		
t_{su}	Setup time	D high or low before DMC↓	3		ns
		SCAND high or low before TMC↓	3		
		DMC or TMC low before SLC↑ (nonoverlap)	2		
t_h	Hold time	D high or low after DMC↓	0		ns
		SCAND high or low after TMC↓	0		
		DMC or TMC low after SLC↓ (nonoverlap)	2		

NOTE 1: Additional data regarding pulse-duration, setup-time, and hold-time are incorporated in the engineering workstation library.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	D, SCAND		0.06		pF
		DMC, TMC		0.04		
		SLC		0.03		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.56		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	D	Q	0.45	1.34	3.1	0.48	1.34	2.83	ns
t_{PHL}			0.52	1.58	3.78	0.55	1.58	3.46	
t_{PLH}	D	QZ	0.41	1.26	3.07	0.44	1.26	2.8	ns
t_{PHL}			0.42	1.32	3.13	0.46	1.32	2.88	
t_{PLH}	DMC	Q	0.27	1.19	2.91	0.29	1.19	2.68	ns
t_{PHL}			0.68	1.63	3.68	0.71	1.63	3.31	
t_{PLH}	DMC	QZ	0.58	1.33	2.87	0.59	1.33	2.65	ns
t_{PHL}			0.22	1.17	2.97	0.25	1.17	2.73	
t_{PLH}	SCAND	Q	0.45	1.34	3.1	0.48	1.34	2.83	ns
t_{PHL}			0.52	1.58	3.78	0.55	1.58	3.46	
t_{PLH}	SCAND	QZ	0.41	1.26	3.07	0.44	1.26	2.8	ns
t_{PHL}			0.42	1.32	3.13	0.46	1.32	2.88	
t_{PLH}	SLC	Q	0.46	0.99	2.04	0.47	0.99	1.91	ns
t_{PHL}			0.21	0.8	1.86	0.23	0.8	1.69	
t_{PLH}	SLC	QZ	0.11	0.49	1.19	0.12	0.49	1.08	ns
t_{PHL}			0.45	0.97	2.22	0.45	0.97	2.03	
t_{PLH}	TMC	Q	0.27	1.19	2.92	0.29	1.19	2.69	ns
t_{PHL}			0.68	1.63	3.68	0.7	1.63	3.3	
t_{PLH}	TMC	QZ	0.57	1.33	2.87	0.59	1.33	2.65	ns
t_{PHL}			0.22	1.17	2.98	0.25	1.17	2.74	
Δt_{PLH}	D	Q	0.44	1.09	2.28	0.47	1.09	2.1	ns/pF
Δt_{PHL}			0.35	0.73	1.46	0.37	0.73	1.31	
Δt_{PLH}	D	QZ	0.42	1.1	2.3	0.45	1.1	2.12	ns/pF
Δt_{PHL}			0.37	0.96	2.13	0.39	0.96	1.93	
Δt_{PLH}	DMC	Q	0.44	1.09	2.28	0.47	1.09	2.1	ns/pF
Δt_{PHL}			0.35	0.74	1.47	0.37	0.74	1.32	
Δt_{PLH}	DMC	QZ	0.42	1.09	2.3	0.45	1.09	2.12	ns/pF
Δt_{PHL}			0.36	0.96	2.12	0.39	0.96	1.93	
Δt_{PLH}	SCAND	Q	0.44	1.09	2.28	0.47	1.09	2.1	ns/pF
Δt_{PHL}			0.35	0.73	1.46	0.37	0.73	1.31	
Δt_{PLH}	SCAND	QZ	0.42	1.1	2.3	0.45	1.1	2.12	ns/pF
Δt_{PHL}			0.37	0.96	2.13	0.39	0.96	1.93	
Δt_{PLH}	SLC	Q	0.42	1.1	2.29	0.45	1.1	2.1	ns/pF
Δt_{PHL}			0.35	0.74	1.47	0.37	0.74	1.32	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	SLC	QZ	0.42	1.1	2.22	0.45	1.1	2.06	ns/pF
Δt_{PHL}			0.35	0.96	2.08	0.38	0.96	1.93	
Δt_{PLH}	TMC	Q	0.44	1.09	2.28	0.47	1.09	2.09	ns/pF
Δt_{PHL}			0.35	0.74	1.47	0.37	0.74	1.32	
Δt_{PLH}	TMC	QZ	0.42	1.09	2.3	0.45	1.09	2.12	ns/pF
Δt_{PHL}			0.36	0.96	2.12	0.39	0.96	1.93	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

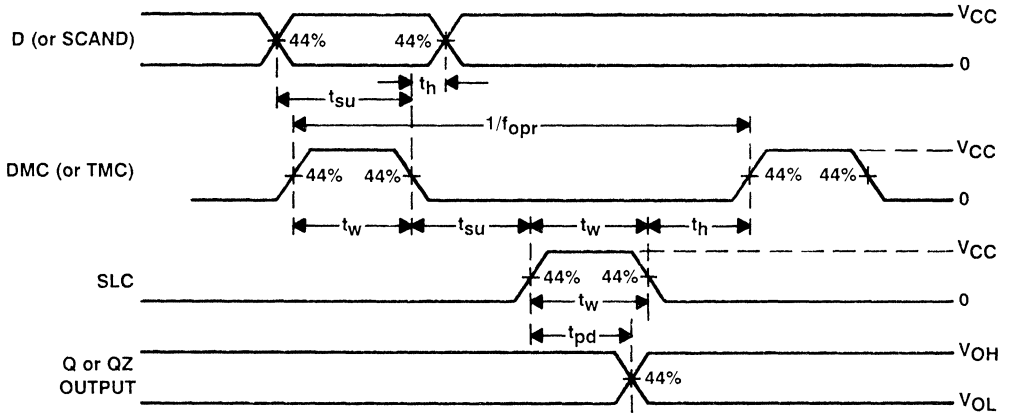
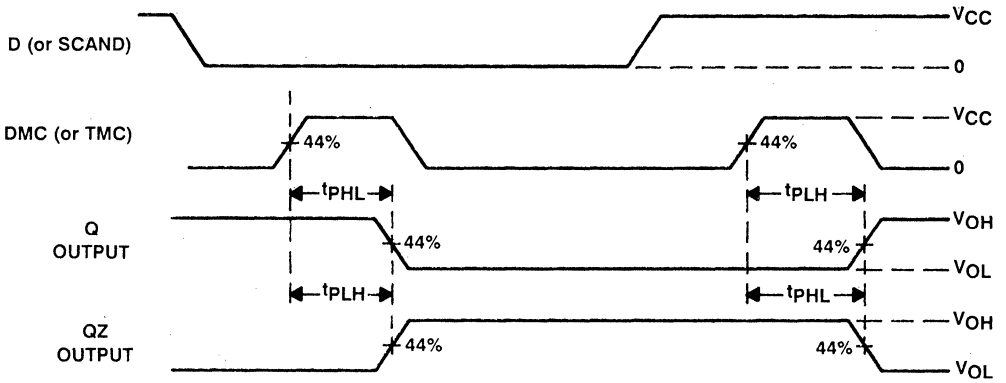


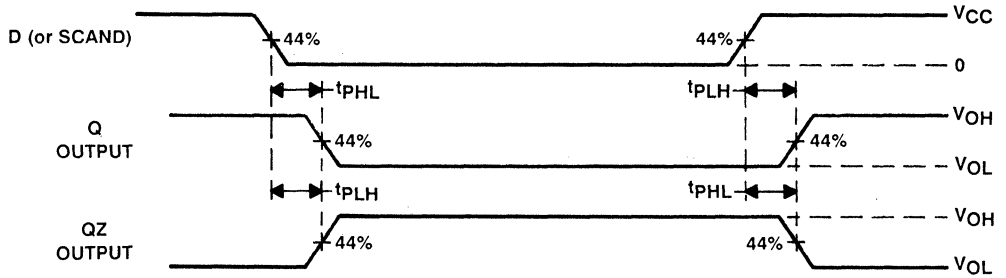
FIGURE 1. TIMING DIAGRAM

PARAMETER MEASUREMENT INFORMATION



NOTE: SLC is high.

FIGURE 2. DMC OR TMC TO Q OR QZ TIMING DIAGRAM



NOTE: DMC, TMC, and SLC are high.

FIGURE 3. D OR SCAND TO Q OR QZ TIMING DIAGRAM

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TDN12LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH MASTER AND SLAVE 1X OUTPUTS

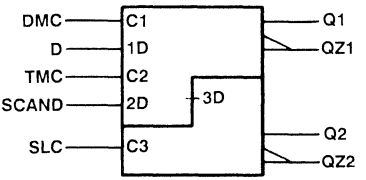
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUTS			
DATA PATH		SCAN PATH		SLAVE	MASTER		SLAVE	
D	DMC	SCAND	TMC	SLC	Q1	QZ1	Q2	QZ2
X	L	X	L	L	$Q1_0$	$\overline{Q1}_0$	$Q2_0$	$\overline{Q2}_0$
d1	H	X	L	L	d1	$\overline{d1}$	$Q2_0$	$\overline{Q2}_0$
X	L	d2	H	L	d2	$\overline{d2}$	$Q2_0$	$\overline{Q2}_0$
d1	H	d2	H	L	?	?	$Q2_0$	$\overline{Q2}_0$
X	L	X	L	H	$Q1_0$	$\overline{Q1}_0$	$Q1_0$	$\overline{Q1}_0$
d1	H	X	L	H	d1	$\overline{d1}$	d1	$\overline{d1}$
X	L	d2	H	H	d2	$\overline{d2}$	d2	$\overline{d2}$
d1	H	d2	H	H	?	?	?	?

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TDN12LJ cell implements a scan-input D-type latch with 1X-drive master and slave outputs. The cell consists of a dual D-type master input data and scan-data latch with complementary outputs, and a single slave latch with complementary outputs. In the data- or scan-path mode, either DMC or TMC can select the entry and storage of data. When TMC is low and DMC is high, the Q1 output follows the D input. When DMC is subsequently taken low, the Q1 output is latched. When DMC is low and TMC is high, the Q1 output follows the SCAND input. When TMC is subsequently taken low, the Q1 output is latched. Data entered is available to the slave output latch, which follows the selected master input latch while SLC is high. Data at the Q2 and QZ2 outputs can be latched by taking SLC low.

When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TDN12LJ D,SCAND,DMC,TMC,SLC,Q1,QZ1,Q2,QZ2;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{opr}	Operating frequency		0	100	MHz
t_w	Pulse duration	DMC or TMC high	2.5		ns
		SLC high	2.5		
t_{su}	Setup time	D high or low before DMC↓	3		ns
		SCAND high or low before TMC↓	3		
		DMC or TMC low before SLC↑ (nonoverlap)	2.5		
t_h	Hold time	D high or low after DMC↓	0		ns
		SCAND high or low after TMC↓	0		
		DMC or TMC low after SLC↓ (nonoverlap)	2.5		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	D, SCAND		0.06		pF
		DMC, TMC		0.04		
		SLC		0.03		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.21		pF

TDN12LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH MASTER AND SLAVE 1X OUTPUTS

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	D	Q1	0.37	0.72	1.41	0.38	0.72	1.29	ns
t_{PHL}			0.32	1	2.43	0.34	1	2.24	
t_{PLH}	D	QZ1	0.47	1.38	3.35	0.48	1.38	3.08	ns
t_{PHL}			0.54	1.25	2.63	0.56	1.25	2.41	
t_{PLH}	D	Q2	0.57	1.54	3.52	0.59	1.54	3.22	ns
t_{PHL}			0.61	1.83	4.5	0.63	1.83	4.12	
t_{PLH}	D	QZ2	0.48	1.54	3.79	0.5	1.54	3.47	ns
t_{PHL}			0.54	1.5	3.56	0.56	1.5	3.27	
t_{PLH}	DMC	Q1	0.19	0.59	1.24	0.2	0.59	1.15	ns
t_{PHL}			0.46	1.01	2.18	0.46	1.01	2.04	
t_{PLH}	DMC	QZ1	0.61	1.39	3.09	0.62	1.39	2.86	ns
t_{PHL}			0.35	1.12	2.46	0.37	1.12	2.26	
t_{PLH}	DMC	Q2	0.38	1.4	3.36	0.42	1.4	3.08	ns
t_{PHL}			0.78	1.86	4.23	0.78	1.86	3.9	
t_{PLH}	DMC	QZ2	0.63	1.55	3.52	0.65	1.55	3.25	ns
t_{PHL}			0.35	1.38	3.4	0.38	1.38	3.12	
t_{PLH}	SCAND	Q1	0.37	0.72	1.41	0.38	0.72	1.29	ns
t_{PHL}			0.32	1	2.43	0.34	1	2.24	
t_{PLH}	SCAND	QZ1	0.47	1.38	3.35	0.48	1.38	3.08	ns
t_{PHL}			0.54	1.25	2.63	0.56	1.25	2.41	
t_{PLH}	SCAND	Q2	0.57	1.54	3.52	0.59	1.54	3.22	ns
t_{PHL}			0.61	1.83	4.5	0.63	1.83	4.12	
t_{PLH}	SCAND	QZ2	0.48	1.54	3.79	0.5	1.54	3.47	ns
t_{PHL}			0.54	1.5	3.56	0.56	1.5	3.27	
t_{PLH}	SLC	Q2	0.48	1	2.03	0.49	1	1.9	ns
t_{PHL}			0.25	0.81	1.79	0.26	0.81	1.65	
t_{PLH}	SLC	QZ2	0.13	0.5	1.08	0.14	0.5	1	ns
t_{PHL}			0.45	0.98	2.1	0.38	0.95	1.92	
t_{PLH}	TMC	Q1	0.19	0.59	1.24	0.2	0.59	1.15	ns
t_{PHL}			0.46	1.01	2.18	0.46	1.01	2.04	
t_{PLH}	TMC	QZ1	0.61	1.39	3.09	0.62	1.39	2.86	ns
t_{PHL}			0.35	1.12	2.46	0.37	1.12	2.26	
t_{PLH}	TMC	Q2	0.38	1.4	3.36	0.41	1.4	3.08	ns
t_{PHL}			0.78	1.86	4.23	0.78	1.86	3.9	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	TMC	QZ2	0.63	1.55	3.52	0.65	1.55	3.25	ns
t_{PHL}			0.35	1.38	3.4	0.38	1.38	3.12	
Δt_{PLH}	D	Q1	0.42	1.1	2.33	0.45	1.1	2.14	ns/pF
Δt_{PHL}			0.38	1.05	2.36	0.41	1.05	2.15	
Δt_{PLH}	D	QZ1	0.41	1.07	2.26	0.44	1.07	2.08	ns/pF
Δt_{PHL}			0.34	0.74	1.51	0.36	0.74	1.36	
Δt_{PLH}	D	Q2	0.42	1.08	2.27	0.45	1.08	2.09	ns/pF
Δt_{PHL}			0.32	0.73	1.43	0.35	0.73	1.28	
Δt_{PLH}	D	QZ2	0.43	1.08	2.27	0.46	1.08	2.09	ns/pF
Δt_{PHL}			0.34	0.96	2.12	0.37	0.96	1.92	
Δt_{PLH}	DMC	Q1	0.42	1.1	2.34	0.45	1.1	2.15	ns/pF
Δt_{PHL}			0.37	1.05	2.36	0.4	1.05	2.15	
Δt_{PLH}	DMC	QZ1	0.41	1.08	2.27	0.44	1.08	2.08	ns/pF
Δt_{PHL}			0.34	0.75	1.51	0.37	0.75	1.36	
Δt_{PLH}	DMC	Q2	0.42	1.09	2.27	0.44	1.09	2.09	ns/pF
Δt_{PHL}			0.31	0.72	1.43	0.35	0.72	1.28	
Δt_{PLH}	DMC	QZ2	0.42	1.08	2.28	0.45	1.08	2.09	ns/pF
Δt_{PHL}			0.36	0.96	2.12	0.38	0.96	1.93	
Δt_{PLH}	SCAND	Q1	0.42	1.1	2.33	0.45	1.1	2.14	ns/pF
Δt_{PHL}			0.38	1.05	2.36	0.41	1.05	2.15	
Δt_{PLH}	SCAND	QZ1	0.41	1.07	2.26	0.44	1.07	2.08	ns/pF
Δt_{PHL}			0.34	0.74	1.51	0.36	0.74	1.36	
Δt_{PLH}	SCAND	Q2	0.42	1.08	2.27	0.45	1.08	2.09	ns/pF
Δt_{PHL}			0.32	0.73	1.43	0.35	0.73	1.28	
Δt_{PLH}	SCAND	QZ2	0.43	1.08	2.27	0.46	1.08	2.09	ns/pF
Δt_{PHL}			0.34	0.96	2.12	0.37	0.96	1.92	
Δt_{PLH}	SLC	Q2	0.4	1.1	2.28	0.44	1.1	2.1	ns/pF
Δt_{PHL}			0.32	0.74	1.48	0.35	0.74	1.33	
Δt_{PLH}	SLC	QZ2	0.4	1.09	2.32	0.44	1.09	2.13	ns/pF
Δt_{PHL}			0.35	0.95	2.12	0.38	0.95	1.92	
Δt_{PLH}	TMC	Q1	0.42	1.1	2.34	0.45	1.1	2.14	ns/pF
Δt_{PHL}			0.37	1.05	2.36	0.4	1.05	2.15	
Δt_{PLH}	TMC	QZ1	0.41	1.08	2.27	0.44	1.08	2.08	ns/pF
Δt_{PHL}			0.34	0.75	1.51	0.37	0.75	1.36	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	TMC	Q2	0.42	1.09	2.27	0.45	1.09	2.09	ns/pF
Δt_{PHL}			0.31	0.72	1.43	0.35	0.72	1.28	
Δt_{PLH}	TMC	QZ2	0.42	1.08	2.28	0.45	1.08	2.09	ns/pF
Δt_{PHL}			0.36	0.96	2.12	0.38	0.96	1.93	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

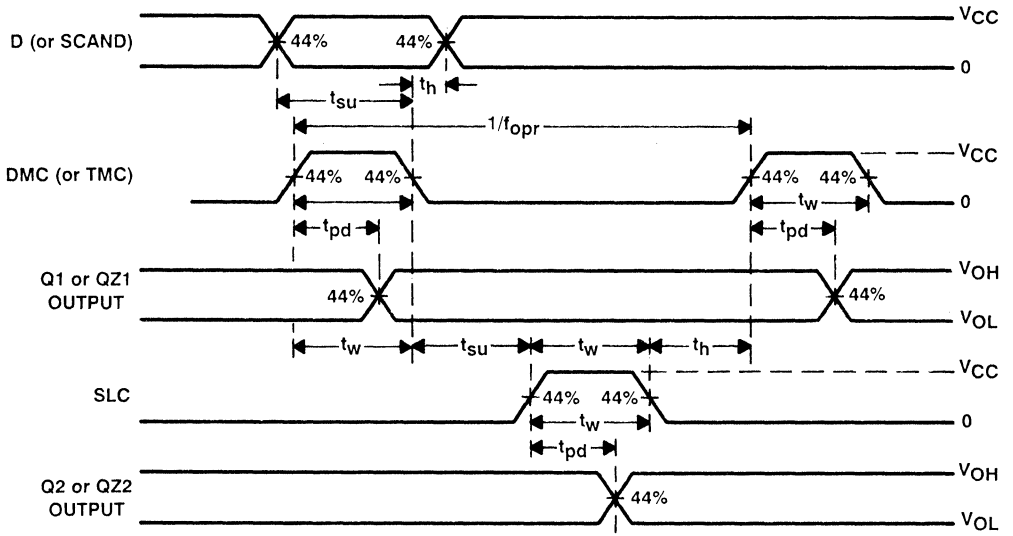
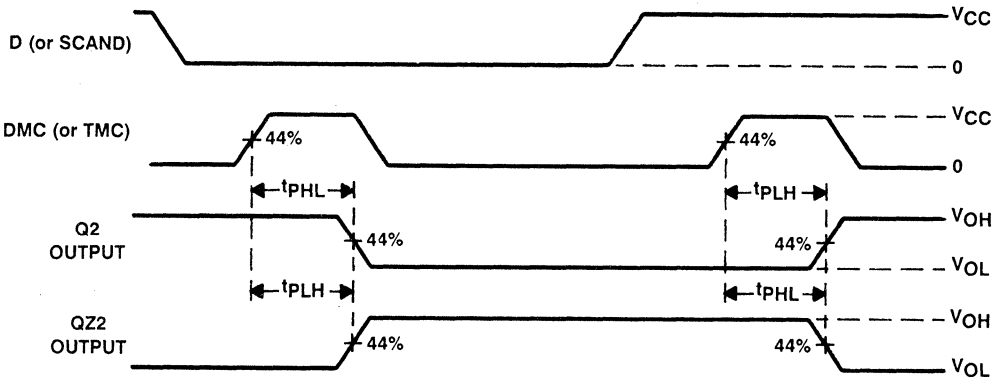


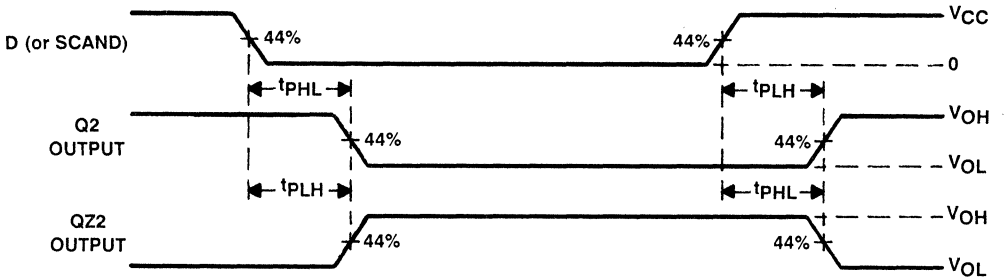
FIGURE 1. TIMING DIAGRAM

PARAMETER MEASUREMENT INFORMATION



NOTE: SLC is high.

FIGURE 2. DMC OR TMC TO Q2 OR QZ2 TIMING DIAGRAM



NOTE: DMC, TMC, and SLC are high.

FIGURE 3. D OR SCAND TO Q2 OR QZ2 TIMING DIAGRAM

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TDN13LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH SLAVE D-INPUT AND MASTER AND SLAVE 1X OUTPUTS

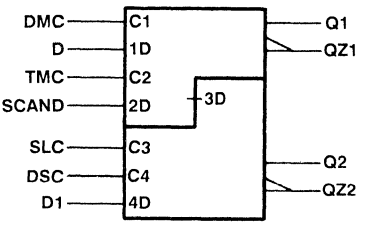
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

MASTER INPUTS				SLAVE INPUTS			OUTPUTS			
DATA PATH		SCAN PATH		SLAVE	SLAVE DATA		MASTER		SLAVE	
D	DMC	SCAND	TMC	SLC	D1	DSC	Q1	QZ1	Q2	QZ2
X	L	X	L	L	X	L	$Q1_0$	$\overline{Q1}_0$	$Q2_0$	$\overline{Q2}_0$
d1	H	X	L	L	X	L	d1	$\overline{d1}$	$Q2_0$	$\overline{Q2}_0$
X	L	d2	H	L	X	L	d2	$\overline{d2}$	$Q2_0$	$\overline{Q2}_0$
d1	H	d2	H	L	X	L	?	?	$Q2_0$	$\overline{Q2}_0$
X	L	X	L	H	X	L	$Q1_0$	$\overline{Q1}_0$	$Q1_0$	$\overline{Q1}_0$
d1	H	X	L	H	X	L	d1	$\overline{d1}$	d1	$\overline{d1}$
X	L	d2	H	H	X	L	d2	$\overline{d2}$	d2	$\overline{d2}$
d1	H	d2	H	H	X	L	?	?	?	?
X	L	X	L	L	d3	H	$Q1_0$	$\overline{Q1}_0$	d3	$\overline{d3}$
d1	H	X	L	L	d3	H	d1	$\overline{d1}$	d3	$\overline{d3}$
X	L	d2	H	L	d3	H	d2	$\overline{d2}$	d3	$\overline{d3}$
d1	H	d2	H	L	d3	H	?	?	d3	$\overline{d3}$
X	L	X	L	H	d3	H	$Q1_0$	$\overline{Q1}_0$	?	?
d1	H	X	L	H	d3	H	d1	$\overline{d1}$	?	?
X	L	d2	H	H	d3	H	d2	$\overline{d2}$	?	?
d1	H	d2	H	H	d3	H	?	?	?	?

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TDN13LJ cell implements a scan-input D-type latch with 1X drive master and slave outputs. The cell consists of a dual D-type master input data and scan-data latch with complementary outputs and a single slave latch with a data input and complementary outputs. In the data- or scan-path mode, either DMC or TMC can be used to select the entry and storage of data. When TMC is low and DMC is high, the Q1 output follows the D input. When DMC is subsequently taken low, the Q1 output is latched. When DMC is low and TMC is high, the Q1 output follows the SCAND input. When TMC is subsequently taken low, the Q1 output is latched. Data entered is available to the slave output latch, which follows the selected master input latch while SLC is high and DSC is low. Data at the Q2 and QZ2 outputs is latched by taking SLC low. When SLC is low and DSC is high, the Q2 output follows the D1 input. When DSC is subsequently taken low, the Q2 output is latched.

When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TDN13LJ D,D1,SCAND,DMC,DSC,TMC,SLC,Q1,QZ1,Q2,QZ2;

TDN13LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH SLAVE D-INPUT AND MASTER AND SLAVE 1X OUTPUTS

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{opr}	Operating frequency		0	100	MHz
t_w	Pulse duration	DMC or TMC high	2.5		ns
		SLC or DSC high	2.5		
t_{su}	Setup time	D high or low before DMC↓	3		ns
		SCAND high or low before TMC↓	3		
		D1 high or low before DSC↓	3		
		DMC or TMC low before SLC↑ (nonoverlap)	2.5		
t_h	Hold time	D high or low after DMC↓	0		ns
		SCAND high or low after TMC↓	0		
		D1 high or low after DSC↓	0		
		DMC or TMC low after SLC↓ (nonoverlap)	2.5		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	D,D1,SCAND		0.06		pF
		DMC,DSC,TMC,SLC		0.04		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.62		pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TDN13LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH SLAVE D-INPUT AND MASTER AND SLAVE 1X OUTPUTS

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	D	Q1	0.37	0.72	1.42	0.38	0.72	1.3	ns
t_{PHL}			0.32	1.01	2.47	0.34	1.01	2.28	
t_{PLH}	D	QZ1	0.37	1.16	2.78	0.39	1.16	2.56	ns
t_{PHL}			0.47	1.05	2.2	0.49	1.05	2.01	
t_{PLH}	D	Q2	0.61	1.43	3.09	0.63	1.43	2.82	ns
t_{PHL}			0.53	1.91	4.85	0.56	1.91	4.47	
t_{PLH}	D	QZ2	0.59	1.94	4.84	0.61	1.94	4.44	ns
t_{PHL}			0.71	1.75	3.83	0.75	1.75	3.48	
t_{PLH}	DMC	Q1	0.19	0.6	1.25	0.2	0.6	1.16	ns
t_{PHL}			0.46	1.02	2.22	0.46	1.02	2.08	
t_{PLH}	DMC	QZ1	0.49	1.17	2.53	0.51	1.17	2.35	ns
t_{PHL}			0.28	0.93	2.03	0.3	0.93	1.87	
t_{PLH}	DMC	Q2	0.44	1.32	2.93	0.47	1.32	2.67	ns
t_{PHL}			0.64	1.93	4.61	0.66	1.93	4.26	
t_{PLH}	DMC	QZ2	0.64	1.96	4.59	0.68	1.96	4.23	ns
t_{PHL}			0.55	1.64	3.66	0.58	1.64	3.34	
t_{PLH}	DSC	Q2	0.17	0.55	1.16	0.18	0.55	1.07	ns
t_{PHL}			0.45	1	2.18	0.46	1	2.04	
t_{PLH}	DSC	QZ2	0.5	1.03	2.12	0.5	1.03	1.99	ns
t_{PHL}			0.29	0.87	1.89	0.3	0.87	1.74	
t_{PLH}	D1	Q2	0.35	0.69	1.33	0.37	0.69	1.22	ns
t_{PHL}			0.31	0.99	2.41	0.32	0.99	2.23	
t_{PLH}	D1	QZ2	0.34	1.02	2.38	0.36	1.02	2.2	ns
t_{PHL}			0.46	1	2.06	0.48	1	1.89	
t_{PLH}	SCAND	Q1	0.37	0.72	1.42	0.38	0.72	1.3	ns
t_{PHL}			0.32	1.01	2.47	0.34	1.01	2.28	
t_{PLH}	SCAND	QZ1	0.37	1.16	2.79	0.39	1.16	2.56	ns
t_{PHL}			0.47	1.05	2.2	0.49	1.05	2.01	
t_{PLH}	SCAND	Q2	0.61	1.43	3.09	0.63	1.43	2.82	ns
t_{PHL}			0.53	1.91	4.85	0.56	1.91	4.47	
t_{PLH}	SCAND	QZ2	0.59	1.94	4.84	0.61	1.94	4.43	ns
t_{PHL}			0.71	1.75	3.83	0.75	1.75	3.48	
t_{PLH}	SLC	Q2	0.17	0.55	1.15	0.18	0.55	1.07	ns
t_{PHL}			0.45	1	2.18	0.46	1	2.04	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	SLC	QZ2	0.5	1.03	2.12	0.5	1.03	1.99	ns
t_{PHL}			0.29	0.87	1.89	0.3	0.87	1.74	
t_{PLH}	TMC	Q1	0.19	0.6	1.25	0.2	0.6	1.16	ns
t_{PHL}			0.46	1.02	2.22	0.46	1.02	2.08	
t_{PLH}	TMC	QZ1	0.49	1.17	2.53	0.51	1.17	2.35	ns
t_{PHL}			0.28	0.93	2.03	0.3	0.93	1.87	
t_{PLH}	TMC	Q2	0.44	1.32	2.92	0.47	1.32	2.67	ns
t_{PHL}			0.64	1.93	4.61	0.66	1.93	4.26	
t_{PLH}	TMC	QZ2	0.64	1.96	4.59	0.68	1.96	4.23	ns
t_{PHL}			0.54	1.64	3.66	0.58	1.64	3.34	
Δt_{PLH}	D	Q1	0.42	1.1	2.33	0.45	1.1	2.14	ns/pF
Δt_{PHL}			0.37	1.04	2.34	0.4	1.04	2.13	
Δt_{PLH}	D	QZ1	0.43	1.09	2.29	0.46	1.09	2.1	ns/pF
Δt_{PHL}			0.34	0.74	1.49	0.37	0.74	1.34	
Δt_{PLH}	D	Q2	0.42	1.1	2.31	0.45	1.1	2.12	ns/pF
Δt_{PHL}			0.37	0.98	2.19	0.4	0.98	1.98	
Δt_{PLH}	D	QZ2	0.42	1.08	2.25	0.46	1.08	2.07	ns/pF
Δt_{PHL}			0.35	0.73	1.45	0.37	0.73	1.32	
Δt_{PLH}	DMC	Q1	0.42	1.1	2.33	0.45	1.1	2.14	ns/pF
Δt_{PHL}			0.36	1.04	2.35	0.39	1.04	2.13	
Δt_{PLH}	DMC	QZ1	0.43	1.1	2.29	0.46	1.1	2.1	ns/pF
Δt_{PHL}			0.34	0.74	1.48	0.37	0.74	1.33	
Δt_{PLH}	DMC	Q2	0.41	1.09	2.3	0.44	1.09	2.12	ns/pF
Δt_{PHL}			0.35	0.98	2.19	0.38	0.98	1.98	
Δt_{PLH}	DMC	QZ2	0.43	1.08	2.25	0.46	1.08	2.07	ns/pF
Δt_{PHL}			0.33	0.73	1.46	0.36	0.73	1.31	
Δt_{PLH}	DSC	Q2	0.41	1.1	2.32	0.44	1.1	2.13	ns/pF
Δt_{PHL}			0.36	0.99	2.21	0.39	0.99	2.01	
Δt_{PLH}	DSC	QZ2	0.4	1.1	2.29	0.44	1.1	2.1	ns/pF
Δt_{PHL}			0.33	0.73	1.47	0.36	0.73	1.32	
Δt_{PLH}	D1	Q2	0.42	1.1	2.32	0.45	1.1	2.13	ns/pF
Δt_{PHL}			0.37	0.99	2.21	0.39	0.99	2	
Δt_{PLH}	D1	QZ2	0.43	1.09	2.28	0.46	1.09	2.09	ns/pF
Δt_{PHL}			0.34	0.74	1.47	0.36	0.74	1.32	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	SCAND	QZ1	0.42	1.1	2.33	0.45	1.1	2.14	ns/pF
Δt_{PHL}			0.37	1.04	2.34	0.4	1.04	2.13	
Δt_{PLH}	SCAND	QZ1	0.43	1.09	2.29	0.46	1.09	2.1	ns/pF
Δt_{PHL}			0.34	0.74	1.49	0.37	0.74	1.34	
Δt_{PLH}	SCAND	Q2	0.42	1.1	2.31	0.45	1.1	2.12	ns/pF
Δt_{PHL}			0.37	0.98	2.19	0.4	0.98	1.98	
Δt_{PLH}	SCAND	QZ1	0.42	1.08	2.25	0.46	1.08	2.07	ns/pF
Δt_{PHL}			0.35	0.73	1.45	0.37	0.73	1.32	
Δt_{PLH}	SLC	Q2	0.41	1.1	2.32	0.44	1.1	2.13	ns/pF
Δt_{PHL}			0.36	0.99	2.21	0.39	0.99	2.01	
Δt_{PLH}	SLC	QZ2	0.41	1.1	2.32	0.44	1.1	2.1	ns/pF
Δt_{PHL}			0.33	0.73	1.47	0.36	0.73	1.32	
Δt_{PLH}	TMC	Q1	0.42	1.1	2.33	0.45	1.1	2.14	ns/pF
Δt_{PHL}			0.36	1.04	2.35	0.39	1.04	2.13	
Δt_{PLH}	TMC	QZ1	0.43	1.1	2.29	0.46	1.1	2.1	ns/pF
Δt_{PHL}			0.34	0.74	1.48	0.37	0.74	1.33	
Δt_{PLH}	TMC	Q2	0.41	1.09	2.31	0.44	1.09	2.12	ns/pF
Δt_{PHL}			0.35	0.98	2.19	0.38	0.98	1.98	
Δt_{PLH}	TMC	QZ2	0.43	1.08	2.25	0.46	1.08	2.07	ns/pF
Δt_{PHL}			0.34	0.73	1.46	0.36	0.73	1.31	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

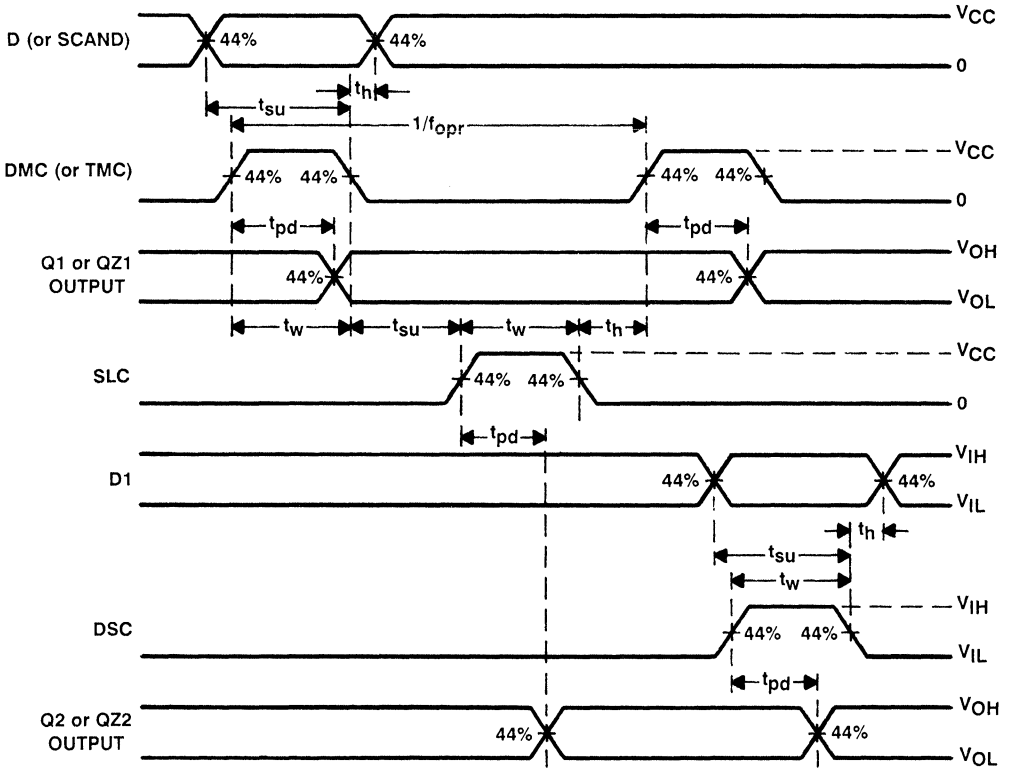


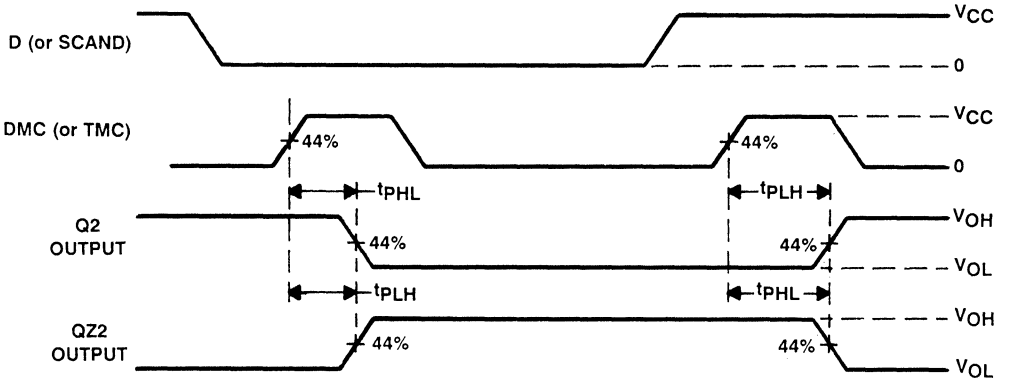
FIGURE 1. TIMING DIAGRAM

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TDN13LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH SLAVE D-INPUT AND MASTER AND SLAVE 1X OUTPUTS

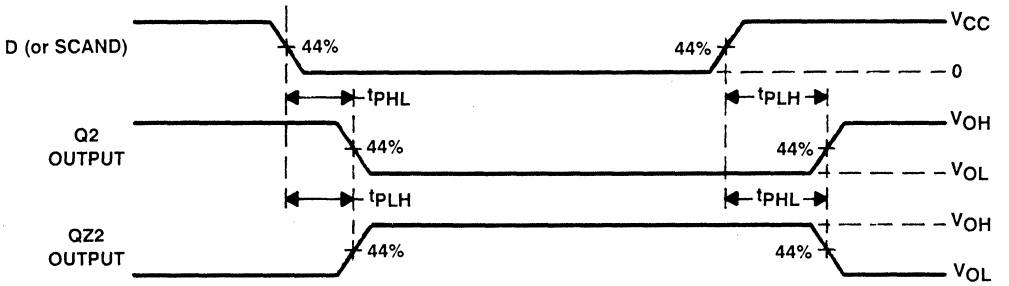
D3030, APRIL 1988

PARAMETER MEASUREMENT INFORMATION



NOTE: SLC is high.

FIGURE 2. DMC OR TMC TO Q2 OR QZ2 TIMING DIAGRAM



NOTE: DMC, TMC, SLC are high.

FIGURE 3. D OR SCAND TO Q2 OR QZ2 TIMING DIAGRAM

TDN22LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH MASTER AND SLAVE 2X OUTPUTS

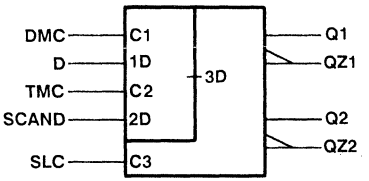
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS					OUTPUTS			
DATA PATH		SCAN PATH		SLAVE	MASTER		SLAVE	
D	DMC	SCAND	TMC	SLC	Q1	QZ1	Q2	QZ2
X	L	X	L	L	$Q1_0$	$\overline{Q1}_0$	$Q2_0$	$\overline{Q2}_0$
d1	H	X	L	L	d1	$\overline{d1}$	Q20	$\overline{Q20}$
X	L	d2	H	L	d2	$\overline{d2}$	$Q2_0$	$\overline{Q2}_0$
d1	H	d2	H	L	?	?	$Q2_0$	$\overline{Q2}_0$
X	L	X	L	H	$Q1_0$	$\overline{Q1}_0$	$Q1_0$	$\overline{Q1}_0$
d1	H	X	L	H	d1	$\overline{d1}$	d1	$\overline{d1}$
X	L	d2	H	H	d2	$\overline{d2}$	d2	$\overline{d2}$
d1	H	d2	H	H	?	?	?	?

logic symbol†



† This symbol is in accordance with ANSI/ IEEE Std 91-1984 and IEC Publication 617-12.

description

The TDN22LJ cell implements a scan-input D-type latch with 2X drive master and slave outputs. The cell consists of a dual D-type master input data and scan-data latch with complementary outputs and a single slave latch with complementary outputs. In the data- or scan-path mode, either DMC or TMC can be used to select the entry and storage of data. When TMC is low and DMC is high, the Q1 output follows the D input. When DMC is subsequently taken low, the Q1 output is latched. When DMC is low and TMC is high, the Q1 output follows the SCAND input. When TMC is subsequently taken low, the Q1 output is latched. Data entered is available to the slave output latch, which follows the selected master input latch while SLC is high. Data at the Q2 and QZ2 outputs is latched by taking SLC low.

When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TDN22LJ D,SCAND,DMC,TMC,SLC,Q1,QZ1,Q2,QZ2;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TDN22LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH MASTER AND SLAVE 2X OUTPUTS

D3030, APRIL 1988

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{opr}	Operating frequency		0	83	MHz
t_w	Pulse duration	DMC or TMC high	3		ns
		SLC high	3		
t_{su}	Setup time	D high or low before DMC↓	3		ns
		SCAND high or low before TMC↓	3		
		DMC or TMC low before SLC↑ (nonoverlap)	3		
t_h	Hold time	D high or low after DMC↓	0		ns
		SCAND high or low after TMC↓	0		
		DMC or TMC low after SLC↓ (nonoverlap)	3		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	D, SCAND		0.06		pF
		DMC, TMC		0.04		
		SLC		0.03		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	2.46		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	D	Q1	0.4	0.85	1.72	0.42	0.85	1.57	ns
t_{PHL}			0.37	1.09	2.62	0.39	1.09	2.42	
t_{PLH}	D	QZ1	0.49	1.45	3.5	0.51	1.45	3.22	ns
t_{PHL}			0.53	1.26	2.67	0.57	1.26	2.44	
t_{PLH}	D	Q2	0.61	1.65	3.91	0.64	1.65	3.57	ns
t_{PHL}			0.63	1.99	4.96	0.66	1.99	4.52	
t_{PLH}	D	QZ2	0.51	1.73	4.32	0.54	1.73	3.95	ns
t_{PHL}			0.54	1.56	3.7	0.58	1.56	3.39	
t_{PLH}	DMC	Q1	0.25	0.75	1.54	0.27	0.75	1.41	ns
t_{PHL}			0.48	1.04	2.27	0.48	1.04	2.11	
t_{PLH}	DMC	QZ1	0.59	1.4	3.14	0.6	1.4	2.9	ns
t_{PHL}			0.38	1.14	2.49	0.4	1.14	2.28	
t_{PLH}	DMC	Q2	0.45	1.56	3.7	0.48	1.56	3.39	ns
t_{PHL}			0.69	1.94	4.58	0.72	1.94	4.19	
t_{PLH}	DMC	QZ2	0.66	1.68	3.95	0.67	1.68	3.63	ns
t_{PHL}			0.41	1.46	3.52	0.44	1.46	3.23	
t_{PLH}	SCAND	Q1	0.4	0.85	1.72	0.42	0.85	1.57	ns
t_{PHL}			0.37	1.09	2.62	0.39	1.09	2.42	
t_{PLH}	SCAND	QZ1	0.49	1.45	3.5	0.51	1.45	3.22	ns
t_{PHL}			0.53	1.26	2.67	0.57	1.26	2.44	
t_{PLH}	SCAND	Q2	0.61	1.65	3.91	0.64	1.65	3.57	ns
t_{PHL}			0.63	1.99	4.96	0.66	1.99	4.52	
t_{PLH}	SCAND	QZ2	0.51	1.73	4.32	0.54	1.73	3.95	ns
t_{PHL}			0.54	1.56	3.7	0.58	1.56	3.39	
t_{PLH}	SLC	Q2	0.48	1.04	2.2	0.49	1.04	2.05	ns
t_{PHL}			0.25	0.8	1.71	0.27	0.8	1.57	
t_{PLH}	SLC	QZ2	0.21	0.55	1.11	0.21	0.55	1.03	ns
t_{PHL}			0.46	0.95	2.02	0.46	0.95	1.89	
t_{PLH}	TMC	Q1	0.25	0.75	1.54	0.28	0.75	1.42	ns
t_{PHL}			0.48	1.04	2.27	0.48	1.04	2.11	
t_{PLH}	TMC	QZ1	0.59	1.4	3.14	0.6	1.4	2.9	ns
t_{PHL}			0.38	1.14	2.5	0.4	1.14	2.28	
t_{PLH}	TMC	Q2	0.45	1.56	3.7	0.48	1.56	3.39	ns
t_{PHL}			0.69	1.94	4.51	0.72	1.94	4.19	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TDN22LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH MASTER AND SLAVE 2X OUTPUTS

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	TMC	QZ2	0.66	1.68	3.95	0.67	1.68	3.63	ns
t_{PHL}			0.41	1.47	3.53	0.44	1.47	3.24	
Δt_{PLH}	D	Q1	0.22	0.58	1.25	0.23	0.58	1.15	ns/pF
Δt_{PHL}			0.2	0.7	1.7	0.22	0.7	1.55	
Δt_{PLH}	D	QZ1	0.18	0.58	1.31	0.2	0.58	1.2	ns/pF
Δt_{PHL}			0.18	0.41	0.85	0.19	0.41	0.76	
Δt_{PLH}	D	Q2	0.2	0.53	1.11	0.21	0.53	1.02	ns/pF
Δt_{PHL}			0.14	0.35	0.68	0.16	0.35	0.61	
Δt_{PLH}	D	QZ2	0.23	0.55	1.18	0.24	0.55	1.08	ns/pF
Δt_{PHL}			0.2	0.66	1.59	0.21	0.66	1.45	
Δt_{PLH}	DMC	Q1	0.23	0.58	1.27	0.24	0.58	1.16	ns/pF
Δt_{PHL}			0.19	0.7	1.7	0.21	0.7	1.55	
Δt_{PLH}	DMC	QZ1	0.22	0.58	1.31	0.23	0.58	1.2	ns/pF
Δt_{PHL}			0.19	0.42	0.85	0.21	0.42	0.77	
Δt_{PLH}	DMC	Q2	0.18	0.53	1.13	0.2	0.53	1.04	ns/pF
Δt_{PHL}			0.21	0.35	0.68	0.21	0.35	0.62	
Δt_{PLH}	DMC	QZ2	0.19	0.55	1.18	0.21	0.55	1.08	ns/pF
Δt_{PHL}			0.18	0.65	1.59	0.2	0.65	1.45	
Δt_{PLH}	SCAND	Q1	0.22	0.58	1.25	0.23	0.58	1.15	ns/pF
Δt_{PHL}			0.2	0.7	1.7	0.22	0.7	1.55	
Δt_{PLH}	SCAND	QZ1	0.18	0.58	1.31	0.2	0.58	1.2	ns/pF
Δt_{PHL}			0.18	0.41	0.85	0.19	0.41	0.76	
Δt_{PLH}	SCAND	Q2	0.2	0.53	1.11	0.21	0.53	1.02	ns/pF
Δt_{PHL}			0.14	0.35	0.68	0.16	0.35	0.61	
Δt_{PLH}	SCAND	QZ2	0.23	0.55	1.18	0.24	0.55	1.08	ns/pF
Δt_{PHL}			0.2	0.66	1.59	0.21	0.66	1.45	
Δt_{PLH}	SLC	Q2	0.21	0.54	1.13	0.23	0.54	1.04	ns/pF
Δt_{PHL}			0.19	0.38	0.76	0.2	0.38	0.7	
Δt_{PLH}	SLC	QZ2	0.19	0.56	1.21	0.21	0.56	1.11	ns/pF
Δt_{PHL}			0.18	0.66	1.61	0.2	0.66	1.47	
Δt_{PLH}	TMC	Q1	0.23	0.58	1.27	0.24	0.58	1.16	ns/pF
Δt_{PHL}			0.19	0.7	1.7	0.21	0.7	1.55	
Δt_{PLH}	TMC	QZ1	0.22	0.58	1.31	0.23	0.58	1.2	ns/pF
Δt_{PHL}			0.19	0.42	0.85	0.21	0.42	0.77	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	TMC	Q2	0.18	0.53	1.13	0.2	0.53	1.04	ns/pF
Δt_{PHL}			0.21	0.35	0.68	0.21	0.35	0.62	
Δt_{PLH}	TMC	QZ2	0.19	0.55	1.18	0.21	0.55	1.08	ns/pF
Δt_{PHL}			0.18	0.65	1.59	0.2	0.65	1.45	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

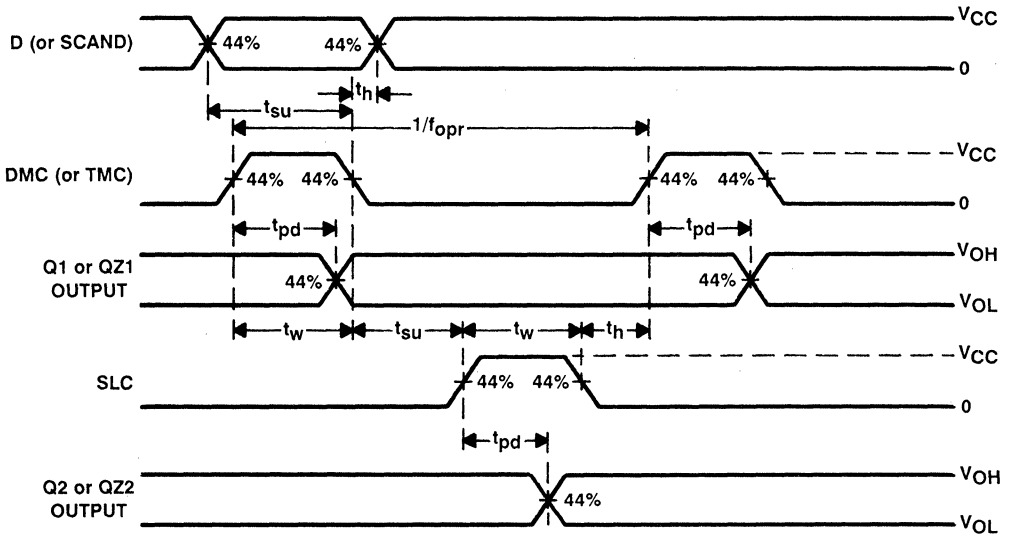
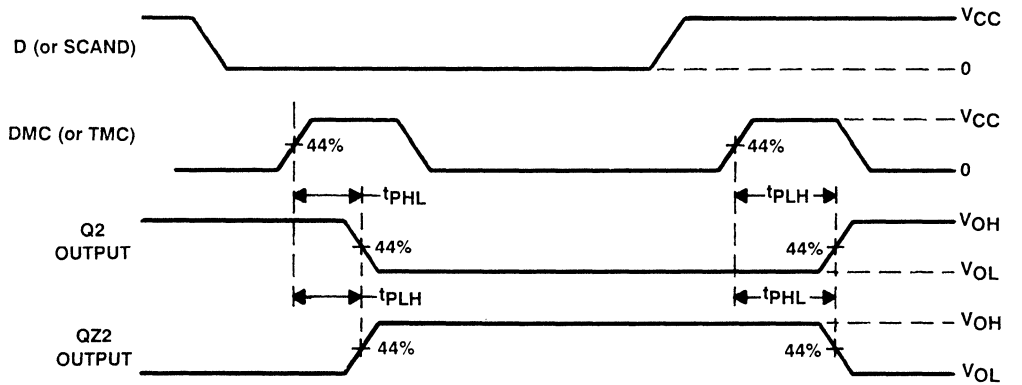


FIGURE 1. TIMING DIAGRAM

TDN22LJ
MASTER-SLAVE SCAN-INPUT D-TYPE LATCH WITH MASTER AND SLAVE 2X OUTPUTS

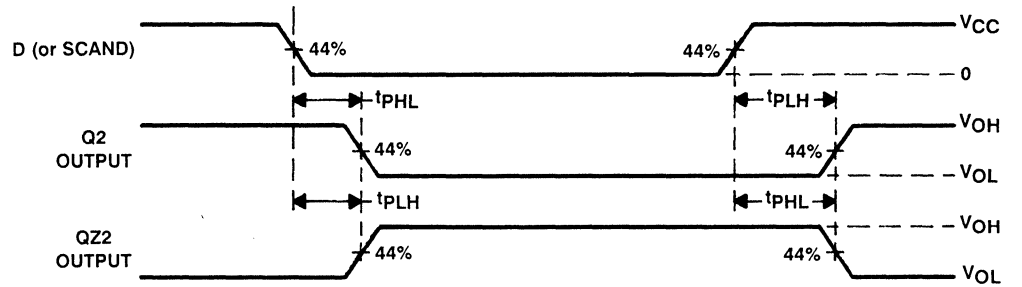
D3030, APRIL 1988

PARAMETER MEASUREMENT INFORMATION



NOTE: SLC is high.

FIGURE 2. DMC OR TMC TO Q2 OR QZ2 TIMING DIAGRAM



NOTE: DMC, TMC, SLC are high.

FIGURE 3. D OR SCAND TO Q2 OR QZ2 TIMING DIAGRAM

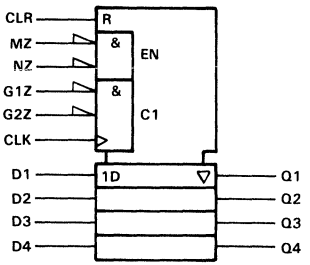
S173LJ
4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

D3030, APRIL 1988

SOFTWARE MACRO

- **3-State Outputs Interface Internal Data Buses Directly**
- **Direct Clear Input Simplifies Initialization or Pattern Length**
- **Embedded Clock Driver Provides Symmetrical Performance Across Long Registers**
- **Parallel Registers for 8-Bit, 16-Bit, 32-Bit Word Widths**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S173LJ software macro implements a 4-bit D-type register. The four-bit length simplifies testability when constructing large registers. Gated enable inputs are provided on these macros for controlling the entry of data into the register. When both data enable inputs, GnZ, are low, data at the D inputs are loaded on the next positive transition of the clock input. Buffer output enable inputs, MZ and NZ, are also provided. When both are low, the normal logic states (high or low levels) of the four outputs are impressed on the data bus. The outputs are disabled by a high logic level at either output control input. The outputs then present a high impedance to the internal bus. When the outputs are disabled, sequential operation of the flip-flops is not affected.

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV120LJ	1	2	2	0.62
IV222LJ	2	4	8	1.52
NA210LJ	1	12	12	2.28
NO210LJ	1	1	1	0.12
NO220LJ	1.5	1	1.5	0.23
R2406LJ	23.5	1	23.5	5.16
TOTALS		21	48	9.93

When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S173LJ D1,D2,D3,D4,CLK,CLR,G1Z,G2Z,MZ,NZ,Q1,Q2,Q3,Q4;

S173LJ
4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

D3030, APRIL 1988

FUNCTION TABLE

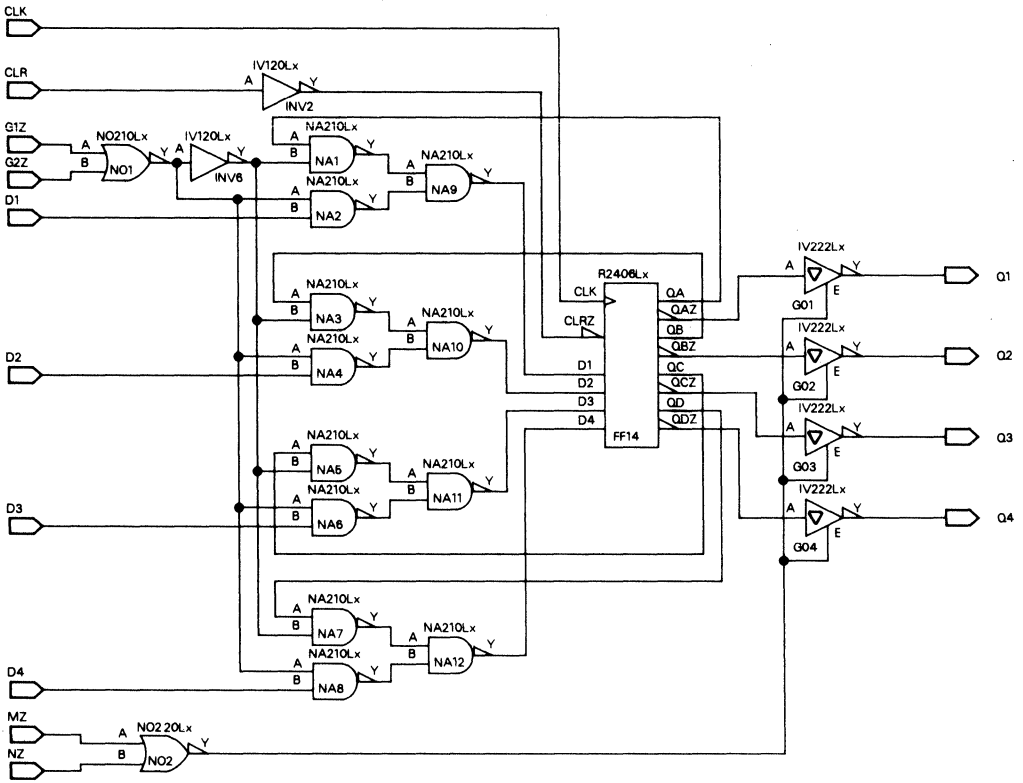
(EACH FLIP-FLOP) (see Note 1)

INPUTS					OUTPUT
CLR	CLK	G1Z	G2Z	Dn	Qn
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

Q_0 = level of Q before the indicated steady-state input conditions were established.

NOTE 1: When either MZ or NZ (or both) is (are) high, the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

logic diagram



S173LJ
4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLR		0.11		pF
		CLK		0.11		
		Dn		0.06		
		GnZ		0.05		
		MZ, NZ		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	9.93		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Notes 2 and 3)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Qn		2.3	4.9		2.3	4.5	ns
t_{PHL}				2.4	5.2		2.4	4.6	
t_{PHL}	CLR	Qn		1.1	2.1		1.1	1.9	ns
t_{PZH}	MZ, NZ	Qn		2.1	4.3		2.1	4.1	ns
t_{PZL}				2	4		2	3.8	
Δt_{PLH}	Any	Qn	0.34	1	2.22	0.34	1	2.06	ns/pF
Δt_{PHL}			0.26	0.6	1.34	0.28	0.6	1.2	
Δt_{PZH}	MZ, NZ	Qn	0.34	1.02	2.26	0.38	1.02	2.08	ns/pF
Δt_{PZL}			0.38	0.64	1.36	0.38	0.64	1.2	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 2. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

3. Enable and delta-enable times are measured using the conditions specified for the IV222LJ.

HDL FILE†

```
BLOCK S173LJ;                    STRUCTURE
D1          @INPUT;              G01     :IV222LJ   QAZ,NO2O,Q1;
D2          @INPUT;              G02     :IV222LJ   QBZ,NO2O,Q2;
D3          @INPUT;              G03     :IV222LJ   QCZ,NO2O,Q3;
D4          @INPUT;              G04     :IV222LJ   QDZ,NO2O,Q4;
CLK         @INPUT;              INV2    :IV120LJ   CLR,INV2O;
CLR         @INPUT;              INV6    :IV120LJ   NO1O,INV6O;
G1Z         @INPUT;              NA1     :NA210LJ   QA,INV6O,NA1O;
G2Z         @INPUT;              NA10    :NA210LJ   NA3O,NA4O,NA10O;
MZ          @INPUT;              NA11    :NA210LJ   NA5O,NA6O,NA11O;
NZ          @INPUT;              NA12    :NA210LJ   NA7O,NA8O,NA12O;
Q1          @OUTPUT;             NA2     :NA210LJ   NO1O,D1,NA2O;
Q2          @OUTPUT;             NA3     :NA210LJ   QB,INV6O,NA3O;
Q3          @OUTPUT;             NA4     :NA210LJ   NO1O,D2,NA4O;
Q4          @OUTPUT;             NA5     :NA210LJ   QC,INV6O,NA5O;
                                 NA6     :NA210LJ   NO1O,D3,NA6O;
                                 NA7     :NA210LJ   QD,INV6O,NA7O;
                                 NA8     :NA210LJ   NO1O,D4,NA8O;
                                 NA9     :NA210LJ   NA1O,NA2O,NA9O;
                                 NO1     :NO210LJ   G1Z,G2Z,NO1O;
                                 NO2     :NO220LJ   MZ,NZ,NO2O;
                                 FF14    :R2406LJ   INV20,NA9O,NA10O,NA11O,NA12O,CLK,
                                                    QAZ,QB,QBZ,QC,QCZ,QD,QDZ;
                                 END S173LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

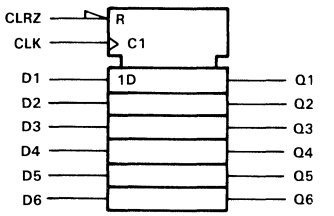
S174LJ
HEX D-TYPE FLIP-FLOP

D3030, APRIL 1988

SOFTWARE MACRO

- **Six-Bit Register**
- **Direct Clear Input Simplifies Initialization or Pattern Length**
- **Clock Buffer Provides Symmetrical Performance Across Long Registers**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

dThe S174LJ software macro implements a 64-bit D-type register. Its 6-bit length simplifies construction of large counters. It may be customized to meet specific system requirements. This software macro reduces the input loading for implementing of larger registers because standard library cells are used to buffer the clear and clock inputs to further enhance performance across long registers. The S174LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
DFC20LJ	6.75	6	40.5	11.28
IV110LJ	0.75	2	1.5	0.32
IV140LJ	1.5	2	3	1.26
TOTALS		10	45	12.86

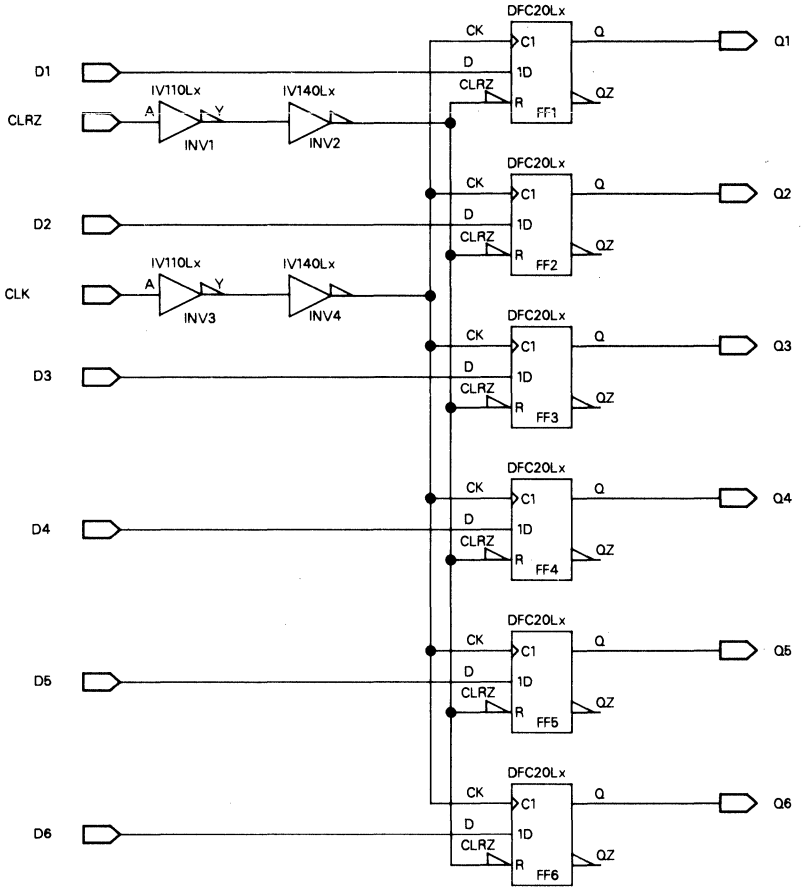
When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S174LJ D1,D2,D3,D4,D5,D6,CLK,CLRZ,Q1,Q2,Q3,Q4,Q5,Q6;

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLRZ	CLK	Dn	Qn
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.05		pF
		CLRZ		0.05		
		Dn		0.16		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	12.86		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Qn		2.9	6		2.9	5.5	ns
t_{PHL}				2.1	4.2		2.1	3.9	
t_{PHL}	CLRZ	Qn		1.9	3.5		1.9	3.4	ns
Δt_{PLH}	Any	Qn	0.18	0.52	1.16	0.18	0.52	1.06	ns/pF
Δt_{PHL}			0.14	0.36	0.8	0.16	0.36	0.72	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

D3030, APRIL 1988

HDL FILE†

```
BLOCK S174LJ;
D1          @INPUT;
D2          @INPUT;
D3          @INPUT;
D4          @INPUT;
D5          @INPUT;
D6          @INPUT;
CLK         @INPUT;
CLRZ        @INPUT;
Q1          @OUTPUT;
Q2          @OUTPUT;
Q3          @OUTPUT;
Q4          @OUTPUT;
Q5          @OUTPUT;
Q6          @OUTPUT;

STRUCTURE
FF1         :DFC20LJ    INV2O,D1,INV4O,Q1,DUM;
FF2         :DFC20LJ    INV2O,D2,INV4O,Q2,DUM;
FF3         :DFC20LJ    INV2O,D3,INV4O,Q3,DUM;
FF4         :DFC20LJ    INV2O,D4,INV4O,Q4,DUM;
FF5         :DFC20LJ    INV2O,D5,INV4O,Q5,DUM;
FF6         :DFC20LJ    INV2O,D6,INV4O,Q6,DUM;
INV1        :IV110LJ    CLRZ,INV1O;
INV2        :IV140LJ    INV1O,INV2O;
INV3        :IV110LJ    CLK,INV3O;
INV4        :IV140LJ    INV3O,INV4O;
END S174LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

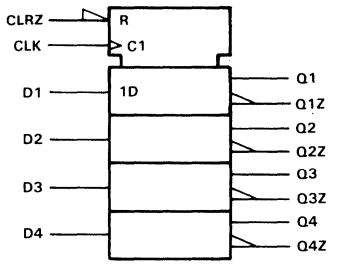
S175LJ
QUADRUPLE D-TYPE FLIP-FLOP WITH COMPLEMENTARY OUTPUTS

D3030, APRIL 1988

SOFTWARE MACRO

- **Four-Bit Register with Complementary Outputs**
- **Direct Clear Input Simplifies Initialization or Pattern Length**
- **Embedded Clock Driver Provides Clock Buffering**
- **Parallel Registers for 8-Bit, 16-Bit, 32-Bit Word Widths**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S175LJ software macro implements a 4-bit register. Its 4-bit length simplifies construction of large registers. This software macro reduces the input loading for implementing larger registers because standard library cells are used to buffer the clear input and the R2406LH register clock input is internally buffered. The S175LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV110LJ	0.75	1	0.75	0.16
IV140LJ	1.5	1	1.5	0.63
R2406LJ	23.5	1	23.5	5.16
TOTALS		3	25.75	5.95

When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S175LJ D1,D2,D3,D4,CLK,CLRZ,Q1,Q1Z,Q2,Q2Z,Q3,Q3Z,Q4,Q4Z;

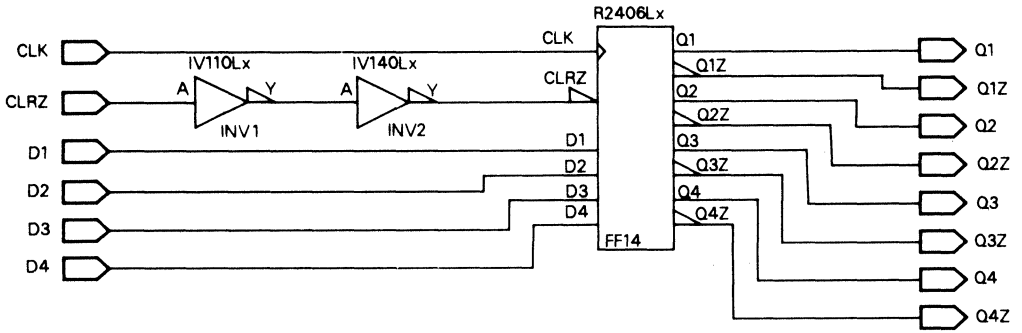
S175LJ
QUADRUPLE D-TYPE FLIP-FLOP WITH COMPLEMENTARY OUTPUTS

D3030, APRIL 1988

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLRZ	CLK	Dn	Qn	QZ
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q_0}$

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S175LJ
QUADRUPLE D-TYPE FLIP-FLOP WITH COMPLEMENTARY OUTPUTS

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.11		pF
		CLRZ		0.05		
		Dn		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	5.95		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAM-ETER	FROM (INPUT)	TO (QUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Qn		1.4	3.1		1.4	2.9	ns
t_{PHL}				1.6	3.6		1.6	3.3	
t_{PLH}	CLK	QnZ		1.8	3.9		1.8	3.5	ns
t_{PHL}				1.8	3.8		1.8	3.5	
t_{PLH}	CLRZ	QnZ		1	1.8		1	1.7	ns
t_{PHL}		Qn		1.6	3.1		1.6	2.9	
Δt_{PLH}	CLK	Qn	0.42	1.12	2.32	0.44	1.12	2.12	ns/pF
Δt_{PHL}			0.34	0.76	1.54	0.36	0.76	1.4	
Δt_{PLH}	CLK	QnZ	0.42	1.08	2.26	0.44	1.08	2.08	ns/pF
Δt_{PHL}			0.26	0.6	1.18	0.28	0.6	1.06	
Δt_{PHL}	CLRZ	Qn	0.34	0.76	1.54	0.36	0.76	1.4	ns/pF
Δt_{PLH}		QnZ	0.4	1.08	2.26	0.42	1.08	2.08	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE†

```
BLOCK S175LJ;
D1          @INPUT;
D2          @INPUT;
D3          @INPUT;
D4          @INPUT;
CLK         @INPUT;
CLRZ        @INPUT;
Q1          @OUTPUT;
Q1Z         @OUTPUT;
Q2          @OUTPUT;
Q2Z         @OUTPUT;
Q3          @OUTPUT;
Q3Z         @OUTPUT;
Q4          @OUTPUT;
Q4Z         @OUTPUT;

STRUCTURE
FF14        :R2406LJ    INV2O,D1,D2,D3,D4,CLK,
                        Q1,Q1Z,Q2,Q2Z,Q3,
                        Q3Z,Q4,Q4Z;
INV1        :IV110LJ    CLRZ,INV1O;
INV2        :IV140LJ    INV1O,INV2O;
END S175LJ;
```

† The HDL netlist format requires "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

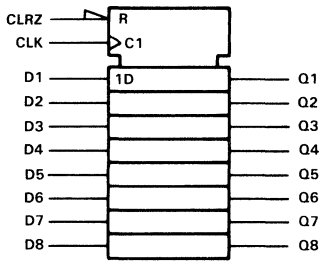
S273LJ
OCTAL D-TYPE FLIP-FLOP

D3030, APRIL 1988

SOFTWARE MACRO

- **8-Bit Software Register**
- **Direct Clear Input Simplifies Initialization or Pattern Length**
- **Buffered Clear Simplifies System Design**
- **Cascadable and Expandable for Wide Words**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S273LJ software macro implements an 8-bit register. The 8-bit length simplifies construction of large registers. This software macro reduces the input loading for implementing of larger registers because standard library cells are used to buffer the clear input. The S273LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV110LJ	0.75	1	0.75	0.16
IV140LJ	1.5	1	1.5	0.63
R2405LJ	20.5	2	41	9.24
TOTALS		4	43.25	10.03

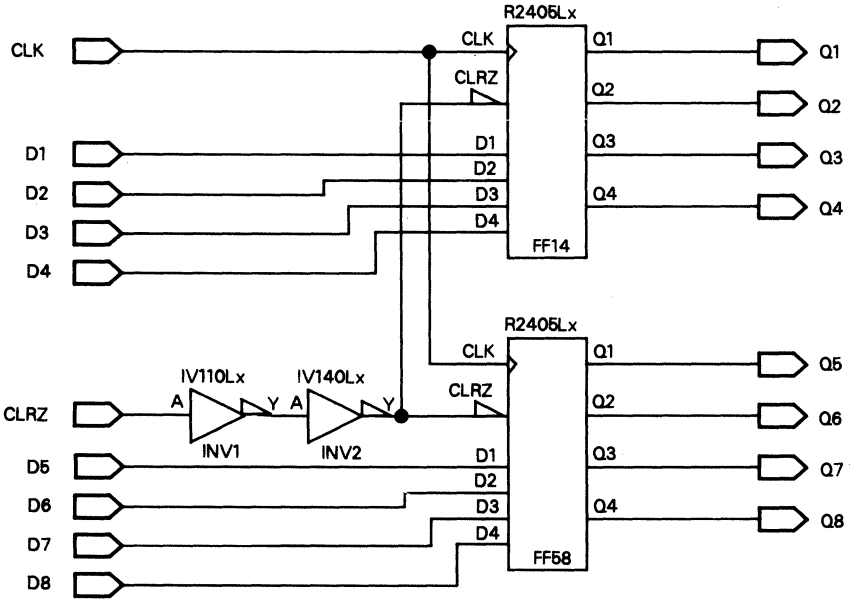
When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S273LJ D1,D2,D3,D4,D5,D6,D7,D8,CLK,CLRZ,Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8;

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLRZ	CLK	Dn	Qn
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.11		pF
		CLRZ		0.05		
		Dn		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	10.03		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Qn		1.4	3.1		1.4	2.9	ns
t_{PHL}				1.6	3.6		1.6	3.3	
t_{PHL}	CLRZ	Qn		1.8	3.2		1.8	3.1	ns
Δt_{PLH}	Any	Qn	0.42	1.06	2.24	0.44	1.06	2.04	ns/pF
Δt_{PHL}			0.34	0.78	1.58	0.36	0.78	1.4	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE†

```
BLOCK S273LJ;
D1          @INPUT;
D2          @INPUT;
D3          @INPUT;
D4          @INPUT;
D5          @INPUT;
D6          @INPUT;
D7          @INPUT;
D8          @INPUT;
CLK         @INPUT;
CLRZ        @INPUT;
Q1          @OUTPUT;
Q2          @OUTPUT;
Q3          @OUTPUT;
Q4          @OUTPUT;
Q5          @OUTPUT;
Q6          @OUTPUT;
Q7          @OUTPUT;
Q8          @OUTPUT;

STRUCTURE
FF14        :R2405LJ    INV2O,D1,D2,D3,D4,CLK,Q1,Q2,Q3,Q4;
FF58        :R2405LJ    INV2O,D5,D6,D7,D8,CLK,Q5,Q6,Q7,Q8;
INV1        :IV110LJ    CLRZ,INV1O;
INV2        :IV140LJ    INV1O,INV2O;
END S273LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

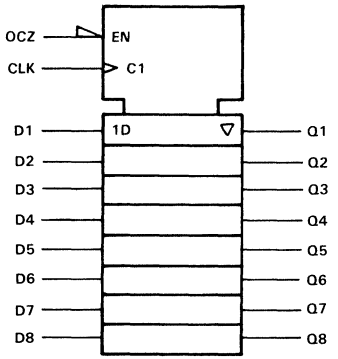
S374LJ
8-BIT D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

D3030, APRIL 1988

SOFTWARE MACRO

- **3-State Outputs Interface with Internal Data Buses Directly**
- **Buffered Output Control Simplifies System Design**
- **Embedded Clock Drivers Provide Symmetrical Performance Across Long Registers**
- **Parallel Latches for 16-Bit, 32-Bit, 64-Bit Word Widths**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S374LJ software macro implements an 8-bit D-type register and is designed specifically for interfacing internal bus lines. The 8-bit length simplifies construction of large registers. The Output-Control input, OCZ, can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. When the outputs are enabled with OCZ low, the logic level at each of the eight outputs is impressed on the data bus. The outputs are disabled by a high logic level at OCZ. The outputs then preset a high impedance to the internal bus. When the outputs are disabled, sequential operation of the flip-flops is not affected. The S374LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV120LJ	1	1	1	31
R2407LJ	24.5	2	49	9.92
TO010LJ	1.5	1	1.5	NIL
TOTALS		4	51.5	10.23

When the flip-flop is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S374LJ D1,D2,D3,D4,D5,D6,D7,D8,CLK,OCZ,Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8;

FUNCTION TABLE

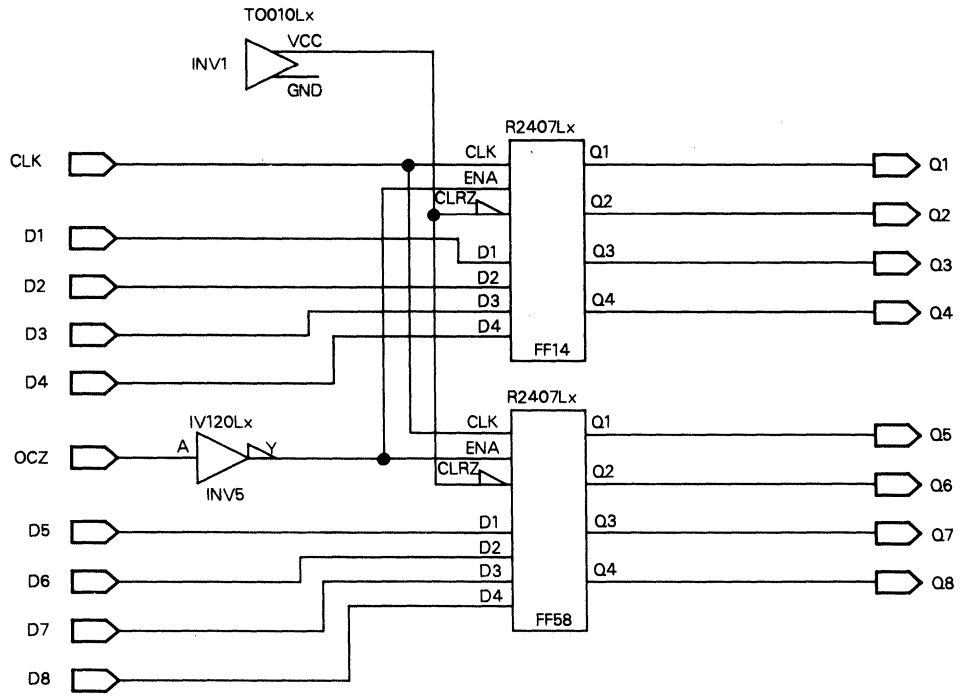
(EACH FLIP-FLOP) (see Note 1)

INPUTS			OUTPUT
OCZ	CLK	Dn	Qn
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Q_0 = level of Q before the indicated steady-state input conditions were established.

Note 1: When OCZ is high, the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

logic diagram



S374LJ
8-BIT D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.22		pF
		Dn		0.06		
		OCZ		0.11		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	10.23		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Notes 2 and 3)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Qn		1.6	3.5		1.6	3.2	ns
t_{PHL}				1.7	3.9		1.7	3.6	
t_{PZH}	OCZ	Qn		0.9	1.9		0.9	1.9	ns
t_{PZL}				0.9	1.6		0.9	1.6	
Δt_{PLH}	CLK	Qn	0.77	2.14	4.64	0.82	2.14	4.27	ns/pF
Δt_{PHL}			0.51	1.33	2.76	0.55	1.33	2.54	
Δt_{PZH}	Any	Qn	0.77	2.2	4.93	0.82	2.2	4.51	ns/pF
Δt_{PZL}			0.51	1.38	3.23	0.55	1.38	2.88	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 2. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

3. Enable and delta-enable times are measured using the conditions specified for the R2407LJ.

HDL FILE†

```
BLOCK S374LJ;
D1          @INPUT;
D2          @INPUT;
D3          @INPUT;
D4          @INPUT;
D5          @INPUT;
D6          @INPUT;
D7          @INPUT;
D8          @INPUT;
CLK         @INPUT;
OCZ         @INPUT;
Q1          @OUTPUT;
Q2          @OUTPUT;
Q3          @OUTPUT;
Q4          @OUTPUT;
Q5          @OUTPUT;
Q6          @OUTPUT;
Q7          @OUTPUT;
Q8          @OUTPUT;

STRUCTURE
INV1        :TO010LJ    DUM,ICLRZ;
INV5        :IV120LJ    OCZ,INV5O;
FF14        :R2407LJ    ICLRZ,D1,D2,D3,D4,CLK,
                        INV5O,Q1,Q2,Q3,Q4;
FF58        :R2407LJ    ICLRZ,D5,D6,D7,D8,CLK,
                        INV5O,Q5,Q6,Q7,Q8;
END S374LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

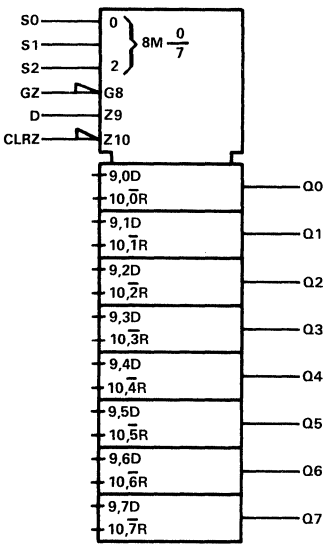
S259LJ
8-BIT ADDRESSABLE LATCH

D3030, APRIL 1988

SOFTWARE MACRO

- **Parallel-Out Register Performs Serial-to-Parallel Conversion with Storage**
- **Expandable for N-Bit Applications**
- **Enable/Disable Input Simplifies Expansion**
- **Four Functional Modes:**
  Addressable Transparent Latch
  Parallel 8-Bit Storage Latch
  1-of-8 Demultiplexer
  Asynchronous Parallel Clear

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S259LJ software macro implements an addressable 8-bit parallel latch. The 8-bit configuration length simplifies construction of large latches. These 8-bit addressable latches are designed for general purpose storage applications where demultiplexing and/or addressable bit storage locations are needed. Some uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunction macros capable of storing single-line data in eight addressable latches or of implementing a 1-of-N line decoder or demultiplexer with active-high outputs.

The S259LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN240LJ	2.25	1	2.25	0.96
IV110LJ	0.75	2	1.5	0.32
IV120LJ	1	6	6	1.86
IV140LJ	1.5	1	1.5	0.63
NA220LJ	1.5	8	12	3.04
NA310LJ	1.25	8	10	1.52
NA410LJ	1.5	16	24	3.04
NO240LJ	2.5	1	2.5	0.44
TOTALS		43	59.75	11.81

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S259LJ CLRZ,D,GZ,S0,S1,S2,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7;

Four distinct modes of operation are selectable by controlling the clear (CLRZ) and enable (GZ) inputs as shown in the function table. In the addressable-latch mode, data at the data-in input D are written into the addressed latch. The addressed latch will follow the data input with remaining unaddressed latches retaining their previous states. In the memory mode, all latches remain in their previous states and are not affected by changes at the data or address inputs. To preclude entering erroneous data in the latches, enable GZ should be held high (inactive) while the address lines are changed. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level at the D input with the remaining outputs low. In the clear mode, all outputs are set low and are not affected by address and data changes.

FUNCTION TABLE

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLRZ	GZ			
H	L	D	Qi_0	Addressable Latch
H	H	Qi_0	Qi_0	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

D = the level at the data input
Qi0 = the level of Qi (i = 0,1,...7, as appropriate) before the indicated steady- state input conditions were established.

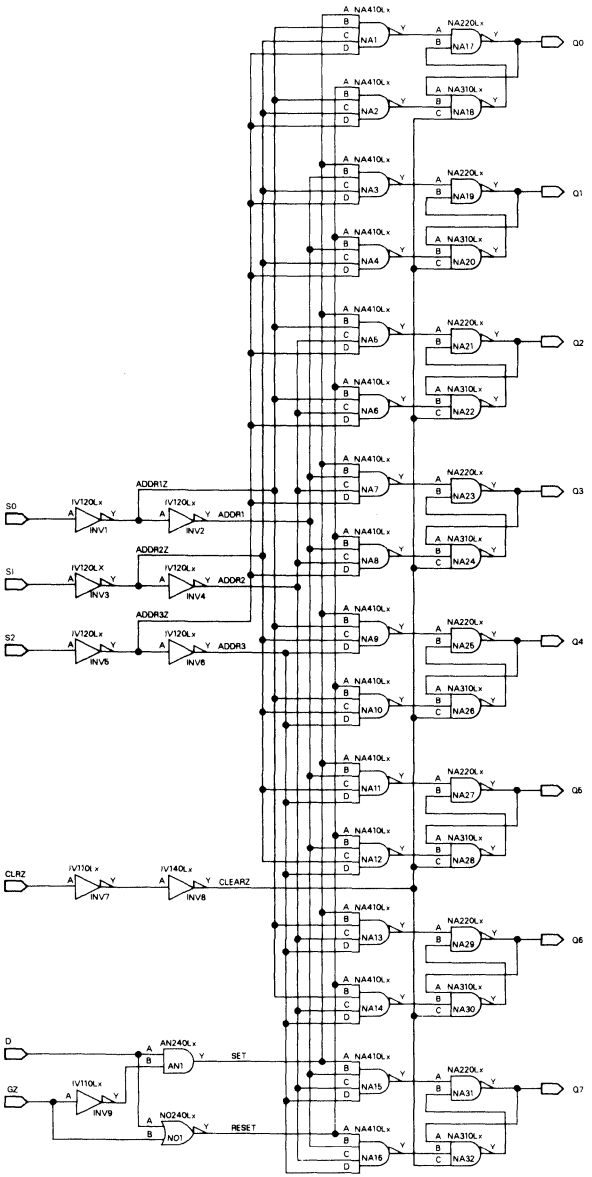
LATCH SELECTION TABLE

SELECT INPUTS			LATCH
S2	S1	S0	ADDRESSED
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

S259LJ
8-BIT ADDRESSABLE LATCH

D3030, APRIL 1988

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristicsded, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLRZ		0.05		pF
		D		0.28		
		GZ		0.27		
		S0, S1, S2		0.11		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	11.9		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	S0, S1, S2	Qn		2.2	4.5		2.2	3.6	ns
t_{PHL}				2.3	4.8		2.3	4.3	
t_{PLH}	D	Qn		2.1	4.1		2.1	3.8	ns
t_{PHL}				2.5	5.1		2.5	4.5	
t_{PLH}	GZ	Qn		2.6	5.1		2.6	4.6	ns
t_{PHL}				2.5	5.1		2.5	4.5	
t_{PHL}	CLR	Qn		2.1	4.1		2.1	3.7	ns
Δt_{PLH}	Any	Any	0.22	0.5	1.08	0.24	0.5	1	ns/pF
Δt_{PHL}			0.28	0.48	1.02	0.28	0.48	0.9	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE†

```
BLOCK S259LJ;
CLRZ    @INPUT;
D       @INPUT;
GZ      @INPUT;
S0      @INPUT;
S1      @INPUT;
S2      @INPUT;
Q0      @OUTPUT;
Q1      @OUTPUT;
Q2      @OUTPUT;
Q3      @OUTPUT;
Q4      @OUTPUT;
Q5      @OUTPUT;
Q6      @OUTPUT;
Q7      @OUTPUT;

STRUCTURE
AN1     :AN240LJ    D,G,SET;
INV1    :IV120LJ    S0,ADDR1Z;
INV2    :IV120LJ    ADDR1Z,ADDR1;
INV3    :IV120LJ    S1,ADDR2Z;
INV4    :IV120LJ    ADDR2Z,ADDR2;
INV5    :IV120LJ    S2,ADDR3Z;
INV6    :IV120LJ    ADDR3Z,ADDR3;
INV7    :IV110LJ    CLRZ,CLEAR;
INV8    :IV140LJ    CLEAR,CLEARZ;
INV9    :IV110LJ    GZ,G;
NA1     :NA410LJ    SET,ADDR1Z,ADDR2Z.ADDR3Z,SET0Z;
NA2     :NA410LJ    RESET,ADDR1Z,ADDR2Z,ADDR3Z,
                    RESET0Z;
NA3     :NA410LJ    SET,ADDR1,ADDR2Z,ADDR3Z,SET1Z;
NA4     :NA410LJ    RESET,ADDR1,ADDR2Z,ADDR3Z,RESET1Z;
NA5     :NA410LJ    SET,ADDR1Z,ADDR2,ADDR3Z,SET2Z;
NA6     :NA410LJ    RESET,ADDR1Z,ADDR2,ADDR3Z,RESET2Z;
NA7     :NA410LJ    SET,ADDR1,ADDR2,ADDR3Z,SET3Z;
NA8     :NA410LJ    RESET,ADDR1,ADDR2,ADDR3Z,RESET3Z;
NA9     :NA410LJ    SET,ADDR1Z,ADDR2Z,ADDR3,SET4Z;
NA10    :NA410LJ    RESET,ADDR1Z,ADDR2Z,ADDR3,RESET4Z;
NA11    :NA410LJ    SET,ADDR1,ADDR2Z,ADDR3,SET5Z;
NA12    :NA410LJ    RESET,ADDR1,ADDR2Z,ADDR3,RESET5Z;
NA13    :NA410LJ    SET,ADDR1Z,ADDR2,ADDR3,SET6Z;
NA14    :NA410LJ    RESET,ADDR1Z,ADDR2,ADDR3,RESET6Z;
NA15    :NA410LJ    SET,ADDR1,ADDR2,ADDR3,SET7Z;
NA16    :NA410LJ    RESET,ADDR1,ADDR2,ADDR3,RESET7Z
NA17    :NA220LJ    SET0Z,Q0Z,Q0;
NA18    :NA310LJI   Q0,RESET0Z,CLEARZ,Q0Z;
NA19    :NA220LJ    SET1Z,Q1Z,Q1;
NA20    :NA310LJ    Q1,RESET1Z,CLEARZ,Q1Z
NA21    :NA220LJ    SET2Z,Q2Z,Q2;
NA22    :NA310LJ    Q2,RESET2Z,CLEARZ,Q2Z;
NA23    :NA220LJ    SET3Z,Q3Z,Q3;
NA24    :NA310LJ    Q3,RESET3Z,CLEARZ,Q3Z;
NA25    :NA220LJ    SET4Z,Q4Z,Q4;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

HDL FILE† - Continued

```
NA26        :NA310LJ   Q4,RESET4Z,CLEARZ,Q4Z;
NA27        :NA220LJ   SET5Z,Q5Z,Q5;
NA28        :NA310LJ   Q5,RESET5Z,CLEARZ,Q5Z;
NA29        :NA220LJ   SET6Z,Q6Z,Q6;
NA30        :NA310LJ   Q6,RESET6Z,CLEARZ,Q6Z;
NA31        :NA220LJ   SET7Z,Q7Z,Q7;
NA32        :NA310LJ   Q7,RESET7Z,CLEARZ,Q7Z;
NO1         :NO240LJ   DIN,GZ,RESET;
END S259LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

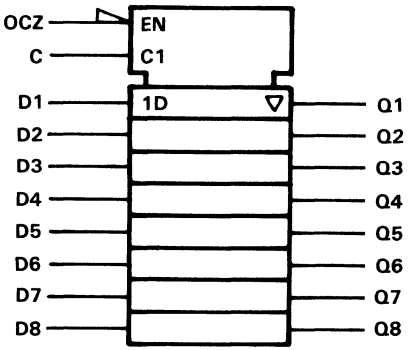
S373LJ
8-BIT D-TYPE LATCH
WITH 3-STATE OUTPUTS

D3030, APRIL 1988

SOFTWARE MACRO

- **3-State Outputs Interface with Internal Data Buses Directly**
- **Buffered Output Enable Simplifies System Design**
- **Full Parallel Access for Loading**
- **Parallel Latches for 16-Bit, 32-Bit, 64-Bit Word Widths**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S373LJ software macro implements an 8-bit D-type latch. The macro is designed specifically for interfacing with internal bus lines. The 8-bit length simplifies construction of large latches. The eight latches of the S373LJ are transparent D-type latches. While the enable (C) is high, the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs. The output-control input (OCZ) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. When the outputs are enabled with OCZ low, the logic level at each of the eight outputs is impressed on the data bus. The outputs are disabled by a high logic level at OCZ. The outputs then present a high impedance to the internal bus. The output control does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off. The S373LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AO221LJ	1.75	8	14	1.76
IV110LJ	0.75	8	6	1.28
IV140LJ	1.5	3	4.5	1.89
IV212LJ	1.25	8	10	1.44
TOTALS		27	34.5	6.37

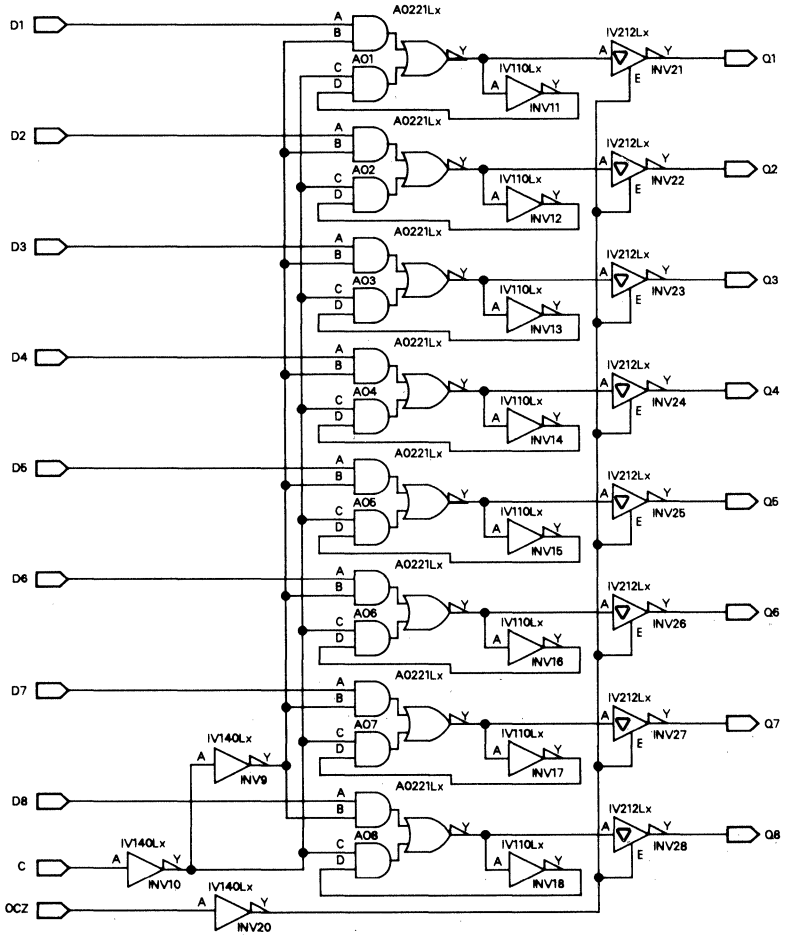
When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S373LJ D1,D2,D3,D4,D5,D6,D7,D8,C,OCZ,Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8;

FUNCTION TABLE
(EACH LATCH)

INPUTS			OUTPUT
OCZ	C	Dn	Qn
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram



S373LJ
8-BIT D-TYPE LATCH
WITH 3-STATE OUTPUTS

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	C		0.23		pF
		Dn		0.06		
		OCZ		0.23		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	6.4		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Notes 1 and 2)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Dn	Qn		1	2.1		1	2	ns
t_{PHL}				1.3	2.9		1.3	2.7	
t_{PZH}	OCZ	Qn		0.8	1.5		0.8	1.3	ns
t_{PZL}				0.8	1.3		0.8	1.1	
t_{PLH}	C	Qn		2	3.5		2	3.3	ns
t_{PHL}				1.7	3.3		1.7	3.2	
Δt_{PLH}	Dn	Qn	0.7	2.08	4.52	0.76	2.08	4.16	ns/pF
Δt_{PHL}			0.48	1.22	2.7	0.52	1.22	2.42	
Δt_{PZH}	Any	Qn	0.76	2.14	4.8	0.8	2.14	4.38	ns/pF
Δt_{PZL}			0.52	1.26	2.88	0.56	1.26	2.56	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Actual performance can be evaluated at post-layout simulation.

2. Enable and delta-enable times are measured using the conditions specified for the IV212LJ.

HDL FILE†

```
BLOCK S373LJ;                STRUCTURE
D1          @INPUT;          AO1     :AO221LJ  D1,INV9O,INV10O,INV11O,AO1O;
D2          @INPUT;          AO2     :AO221LJ  D2,INV9O,INV10O,INV12O,AO2O;
D3          @INPUT;          AO3     :AO221LJ  D3,INV9O,INV10O,INV13O,AO3O;
D4          @INPUT;          AO4     :AO221LJ  D4,INV9O,INV10O,INV14O,AO4O;
D5          @INPUT;          AO5     :AO221LJ  D5,INV9O,INV10O,INV15O,AO5O;
D6          @INPUT;          AO6     :AO221LJ  D6,INV9O,INV10O,INV16O,AO6O;
D7          @INPUT;          AO7     :AO221LJ  D7,INV9O,INV10O,INV17O,AO7O;
D8          @INPUT;          AO8     :AO221LJ  D8,INV9O,INV10O,INV18O,AO8O;
C           @INPUT;          INV10   :IV140LJ  C,INV10O;
OCZ         @INPUT;          INV11   :IV110LJ  AO1O,INV11O;
Q1          @OUTPUT;         INV12   :IV110LJ  AO2O,INV12O;
Q2          @OUTPUT;         INV13   :IV110LJ  AO3O,INV13O;
Q3          @OUTPUT;         INV14   :IV110LJ  AO4O,INV14O;
Q4          @OUTPUT;         INV15   :IV110LJ  AO5O,INV15O;
Q5          @OUTPUT;         INV16   :IV110LJ  AO6O,INV16O;
Q6          @OUTPUT;         INV17   :IV110LJ  AO7O,INV17O;
Q7          @OUTPUT;         INV18   :IV110LJ  AO8O,INV18O;
Q8          @OUTPUT;         INV20   :IV140LJ  OCZ,INV20O;
                             INV21   :IV212LJ  AO1O,INV20O,Q1;
                             INV22   :IV212LJ  AO2O,INV20O,Q2;
                             INV23   :IV212LJ  AO3O,INV20O,Q3;
                             INV24   :IV212LJ  AO4O,INV20O,Q4;
                             INV25   :IV212LJ  AO5O,INV20O,Q5;
                             INV26   :IV212LJ  AO6O,INV20O,Q6;
                             INV27   :IV212LJ  AO7O,INV20O,Q7;
                             INV28   :IV212LJ  AO8O,INV20O,Q8;
                             INV9    :IV140LJ  INV10O,INV9O;
                             END S373LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

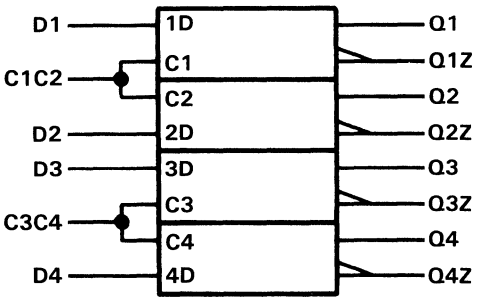
S375LJ
4-BIT BISTABLE LATCH

D3030, APRIL 1988

SOFTWARE MACRO

- **Four-Bit Software Latches with Complementary Outputs**
- **Eliminates Skew and Mismatch of Long Versus Short Data Paths**
- **Parallel Latches for 8-Bit, 16-Bit, 32-Bit Word Widths**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S375LJ software macro implements a 4-bit bistable latch. The 4-bit length simplifies construction of large registers. Information present at a Dn input is transferred to the Qn output when the CnCm input is high, and the Qn output will follow the data input as long as CnCm remains high. When CnCm goes low, the data (that was present at the Dn input at the time the transition occurred) is retained at the Qn output until CnCm is taken high. The S375LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AO221LJ	1.75	4	7	0.88
IV110LJ	0.75	4	3	0.64
IV120LJ	1	4	4	1.24
TOTALS		12	14	2.76

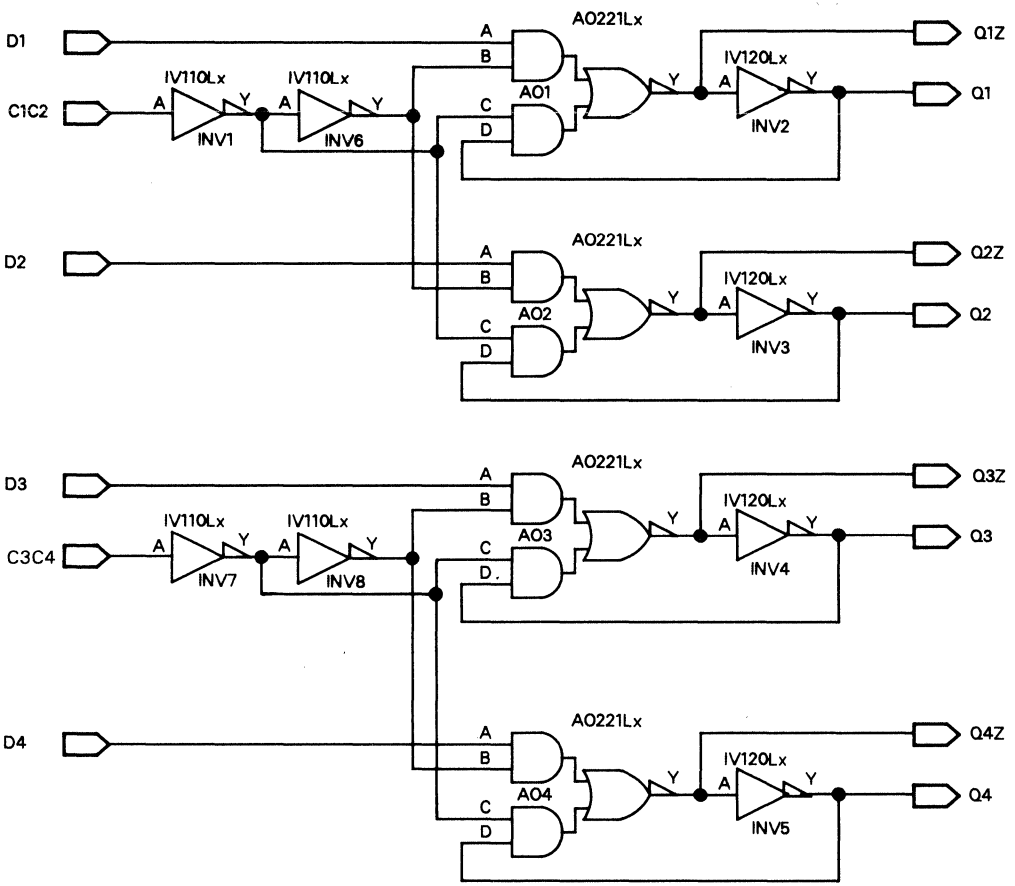
When the latch is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S375LJ D1,D2,D3,D4,C1C2,C3C4,Q1,Q1Z,Q2,Q2Z,Q3,Q3Z,Q4,Q4Z;

FUNCTION TABLE
(EACH LATCH)

INPUTS		OUTPUTS	
Dn	CnCm	Qn	QnZ
L	H	L	H
H	H	H	L
X	L	Qn_0	$\overline{Qn}_0$

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	Cn, Cm		0.05		pF
		Dn		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	10.1		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Dn	Qn		0.7	1.3		0.7	1.3	ns
t_{PHL}				0.8	1.8		0.8	1.7	
t_{PLH}	Dn	QnZ		0.6	1.4		0.6	1.3	ns
t_{PHL}				0.5	0.9		0.5	0.9	
t_{PLH}	CnCm	Qn		1.9	3.3		1.9	3.1	ns
t_{PHL}				1.3	2.5		1.3	2.4	
t_{PLH}	CnCm	QnZ		1.1	2.1		1.1	2	ns
t_{PHL}				1.7	2.9		1.7	2.7	
Δt_{PLH}	Any	Qn	0.24	0.52	1.1	0.26	0.52	1	ns/pF
Δt_{PHL}			0.28	0.42	10.68	0.28	0.42	0.62	
Δt_{PLH}	Any	Any QnZ	0.68	2.02	4.44	0.72	2.02	4.08	ns/pF
Δt_{PHL}			0.36	0.94	2.02	0.4	0.94	1.82	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE†

```
BLOCK S375LJ;                  STRUCTURE
D1          @INPUT;            AO1     :AO221LJ   D1,INV6O,INV1O,Q1,Q1Z;
D2          @INPUT;            AO2     :AO221LJ   D2,INV6O,INV1O,Q2,Q2Z;
D3          @INPUT;            AO3     :AO221LJ   D3,INV8O,INV7O,Q3,Q3Z;
D4          @INPUT;            AO4     :AO221LJ   D4,INV8O,INV7O,Q4,Q4Z;
C1C2        @INPUT;            INV1    :IV110LJ   C1C2,INV1O;
C3C4        @INPUT;            INV2    :IV120LJ   Q1Z,Q1;
Q1          @OUTPUT;           INV3    :IV120LJ   Q2Z,Q2;
Q1Z         @OUTPUT;           INV4    :IV120LJ   Q3Z,Q3;
Q2          @OUTPUT;           INV5    :IV120LJ   Q4Z,Q4;
Q2Z         @OUTPUT;           INV6    :IV110LJ   INV1O,INV6O;
Q3          @OUTPUT;           INV7    :IV110LJ   C3C4,INV7O;
Q3Z         @OUTPUT;           INV8    :IV110LJ   INV7O,INV8O;
Q4          @OUTPUT;           END S375LJ;
Q4Z         @OUTPUT;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

Oscillators 10

D3030, APRIL 1989

OSCILLATOR (INPUT MACRO) CELLS

- Crystal-Controlled Oscillator for Generating On-Chip Clock Signals
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Dependable Texas Instruments Quality and Reliability

OSCILLATOR FUNCTIONAL INDEX

CELL NAME	FREQUENCY RANGE (MHz)	CRYSTAL TYPE	THRES-HOLD	PAGE
OSI01LJ	55 to 75	3rd Overtone	2.5 V	10-5
OSI02LJ	35 to 55	3rd Overtone	2.5 V	10-7
OSI03LJ	20 to 35	3rd Overtone	2.5 V	10-9
OSI04LJ	1 to 20	Fundamental	2.5 V	10-11
OSI24LJ	1 to 20	Fundamental	1.5 V	10-13

description

These cells are crystal oscillators designed for use with a minimum of external components. The input XI and feedback output XO provide connections for use with an external series- or parallel-resonant crystal. An internal 91-kΩ biasing resistor can be placed between nodes XI and XO by internal logic. On-chip frequencies from 1 to 75 MHz can be generated.

DESIGN CONSIDERATIONS

series- or parallel-mode crystal operation

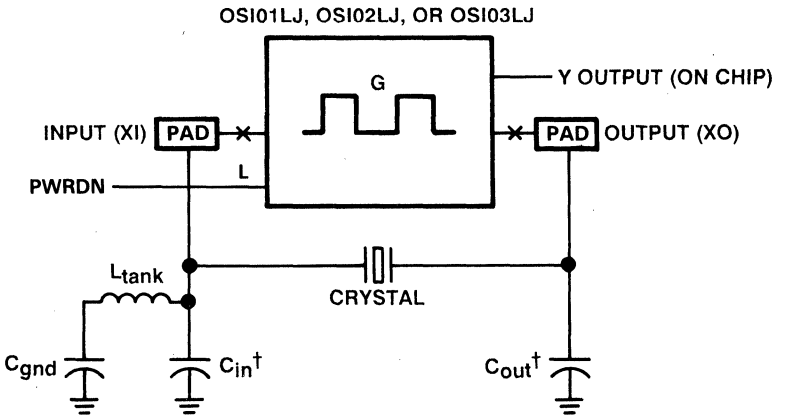
A series- or parallel-mode crystal can be used, but a parallel-mode crystal should be used if frequency accuracy is important. Series- and parallel-mode crystals are identical except that the frequency of a series-mode crystal is set at the series resonant, low impedance frequency of operation. Parallel-mode crystals are tuned with a load capacitor in series that causes them to be tuned for operation between the series resonant frequency and the antiresonant, high- impedance frequency. The value of the load capacitor is specified and is typically 12 pF to 32 pF. This load capacitance value should be equal to the equivalent capacitance between the pins of the oscillator to which the crystal is connected. If accurate frequency of operation is desired, either the input or output capacitance can be set to produce the correct frequency with a given crystal or the crystal manufacturer can make a crystal that will operate at the correct frequency with the existing capacitance.

third-overtone frequency operation

The capacitance loading the input and output should be larger at lower frequencies and smaller at higher frequencies to provide sufficient gain for oscillation yet insufficient gain to produce oscillation at unwanted overtone frequencies. Third-overtone frequency operation is achieved by adding an external LC circuit consisting of an inductor to ground through a capacitor. (See Figure 1). The input pin capacitance and the inductor-capacitor combination form a tank circuit. The tank values are chosen so that its resonant frequency is at the second overtone frequency of the third overtone crystal. This produces a phase shift that prevents oscillation at the fundamental frequency. Smaller values of output capacitance are used at higher frequencies to provide sufficient gain for oscillation.

power down

The PWRDN pin connects or disconnects an internal 90-kΩ bias resistor by controlling a series transmission gate. If PWRDN is low, the resistor is connected between the input and output of the CMOS inverter oscillator circuit. If PWRDN is high, the transmission gate is open and the resistor is taken out of the circuit. Designs using an external power-down pin can tie the oscillator PWRDN pin to the chip power-down. pin. To use an external resistor, the oscillator PWRDN pin should be tied to the HI node of a TO010LJ tie-off cell, removing the internal resistor from the circuit. If the internal resistor is to be used, PWRDN should be low for normal operation and high for test to allow for I_{CCQ} measurement.



† C_{in} and C_{out} are the total capacitance of the circuit board and components, excluding the integrated circuit.

FIGURE 1. OVERTONE FREQUENCY OPERATION OF OSI01LJ, OSI02LJ, OR OSI03LJ

Insufficient capacitance may produce oscillation at the fifth overtone. It is important to operate with as little capacitance as practical (loading the crystal at third-overtone frequencies) to keep the crystal drive level low. Operation at 15 pF or less equivalent load capacitance allows the crystal to behave more as an inductor. High drive level can cause excessive frequency drift and possible crystal failure.

Good design practices include:

- Placing the oscillator pins in the least "noisy" area of the package pins.
- Placing the oscillator on two adjacent pin locations.
- Placing the oscillator between a V_{CC} and ground pin utilizing primary or secondary power pin locations.
- Placing large outputs, especially those operating at data rates near the oscillator frequency, away from the oscillator pins.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

trial values recommended for third-overtone operation

OSI01LJ (See Figure 1)

3RD-OVERTONE FREQUENCY	L_{tank}	C_{gnd}	C_{in}†	C_{out}†
75 MHz	0.47 µH	1000 pF	10 pF	10 pF
64 MHz	0.68 µH	1000 pF	10 pF	10 pF
55 MHz	1 µH	1000 pF	10 pF	10 pF

OSI02LJ (See Figure 1)

3RD-OVERTONE FREQUENCY	L_{tank}	C_{gnd}	C_{in}†	C_{out}†
55 MHz	1 µH	1000 pF	10 pF	10 pF
48 MHz	1.5 µH	1000 pF	10 pF	10 pF
35 MHz	2.2 µH	1000 pF	10 pF	10 pF

OSI03LJ (See Figure 1)

3RD-OVERTONE FREQUENCY	L_{tank}	C_{gnd}	C_{in}†	C_{out}†
35 MHz	2.2 µH	1000 pF	10 pF	10 pF
28 MHz	3.3 µH	1000 pF	10 pF	10 pF
20 MHz	N/A	N/A	27 pF	27 pF

† C_{in} and C_{out} are the total capacitance of the circuit board and components, excluding the integrated circuit.

trial values recommended for fundamental operation

OSI04LJ OR OSI24LJ (See Figure 2)

FUNDAMENTAL FREQUENCY	R_{ext} (C_{in}† = C_{out}† = 30 pF)	R_{ext} (C_{in}† = C_{out}† = 64 pF)
20 MHz	0	0
16 MHz	220 Ω	0
12 MHz	470 Ω	220 Ω
8 MHz	1 kΩ	470 Ω
4 MHz	3.3 kΩ	1.5 kΩ
3 MHz	6.8 kΩ	3.3 kΩ
2 MHz	10 kΩ	4.7 kΩ
1 MHz	33 kΩ	15 kΩ

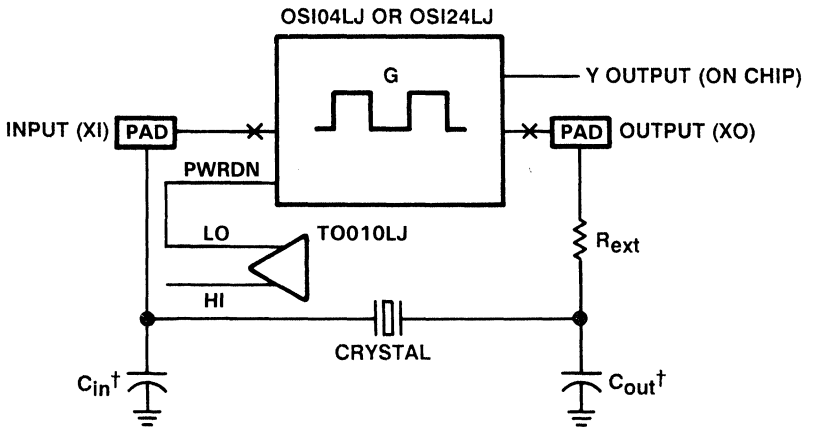


FIGURE 2. FUNDAMENTAL FREQUENCY OPERATION OF OSI04LJ OR OSI24LJ

† C_{in} and C_{out} are the total capacitance of the circuit board and components, excluding the integrated circuit. Typical values range from 10 pF to 64 pF. For operation at lower frequencies, it is necessary to increase the size of C_{out} and/or R_{ext}.

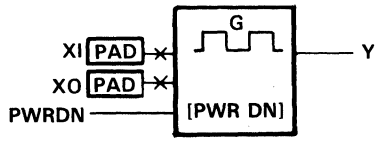
OSI01LJ
55- TO 75-MHz CRYSTAL-CONTROLLED OSCILLATOR

D3030, APRIL 1989

OSCILLATOR CELL

- **Crystal-Controlled Oscillator for Generating On-Chip Clock Signals from 55 to 75 MHz**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The OSI01LJ is a crystal oscillator designed for use with a minimum of external components. The input XI and feedback output XO provide two connections for use with an external series- or parallel-resonant crystal. As a third-harmonic, crystal-controlled oscillator, on-chip frequencies from 55 to 75 MHz can be generated. An internal 91-kΩ biasing resistor can be placed between notes XI and XO by internal logic. When the oscillator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OSI01LJ XI,PWRDN,XO,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.5		V
I_{CC}	Supply current		$V_I = V_{CC}$ or 0, f_{osc} = 64 MHz	16.2		mA
C_i	Input capacitance	XI		8.51		pF
C_o	Output capacitance	XO		10.19		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns, f_{osc} = 1 MHz	18.4		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	XI	Y	1.2	2.6	5.1	1.3	2.6	4.7	ns
t_{PHL}			1.4	2.8	5	1.5	2.8	4.6	
Δt_{PLH}	XI	Y	80	190	390	80	190	360	ps/pF
Δt_{PHL}			110	150	370	100	150	340	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

series- or parallel-mode crystal operation

A series- or parallel-mode crystal can be used. See oscillators' general information for more detailed information on the selection of crystals.

third-overtone frequency operation

The capacitance loading the input and output should be larger at lower frequencies and smaller at higher frequencies to provide sufficient gain for oscillation yet insufficient gain to produce oscillation at unwanted overtone frequencies. Third-overtone frequency operation is achieved by adding an external LC circuit consisting of an inductor to ground through a capacitor. For more detailed design considerations, including a schematic of the external component hookup, see the oscillators' general information.

trial values recommended for third-overtone operation (See Figure 1 in the Oscillators' General Information Section)

OSI01LJ

3RD-OVERTONE FREQUENCY	L_{tank}	C_{gnd}	C_{in}‡	C_{out}‡
75 MHz	0.47 µH	1000 pF	10 pF	10 pF
64 MHz	0.68 µH	1000 pF	10 pF	10 pF
55 MHz	1 µH	1000 pF	10 pF	10 pF

‡ C_{in} and C_{out} are the total capacitance of the circuit board and components, excluding the integrated circuit.

Good design practices include:

- Placing the oscillator pins in the least "noisy" area of the package pins.
- Placing the oscillator on two adjacent pin locations.
- Placing the oscillator between a V_{CC} and ground pin utilizing primary or secondary power pin locations.
- Placing large outputs, especially those operating at data rates near the oscillator frequency, away from the oscillator pins.

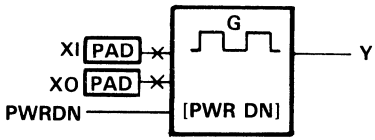
OSI02LJ
35- TO 55-MHz CRYSTAL-CONTROLLED OSCILLATOR

D3030, APRIL 1989

OSCILLATOR CELL

- **Crystal-Controlled Oscillator for Generating On-Chip Clock Signals from 35 to 55 MHz**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The OSI02LJ is a crystal oscillator designed for use with a minimum of external components. The input XI and feedback output XO provide two connections for use with an external series- or parallel-resonant crystal. As a third-harmonic, crystal-controlled oscillator, on-chip frequencies from 35 to 55 MHz can be generated. An internal 91-kΩ biasing resistor can be placed between nodes XI and XO by internal logic. When the oscillator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OSI02LJ XI,PWRDN,XO,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.5		V
I_{CC}	Supply current		$V_I = V_{CC}$ or 0, f_{osc} = 48 MHz	9.4		mA
C_i	Input capacitance	XI		6.53		pF
C_o	Output capacitance	XO		5.75		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns, f_{osc} = 1 MHz	14.5		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	XI	Y	1.2	2.6	5.1	1.3	2.6	4.7	ns
t_{PHL}			1.4	2.8	5	1.5	2.8	4.6	
Δt_{PLH}	XI	Y	80	190	390	80	190	360	ps/pF
Δt_{PHL}			110	150	360	100	150	340	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

series- or parallel-mode crystal operation

A series- or parallel-mode crystal can be used. See oscillators' general information for more detailed information on the selection of crystals.

third-overtone frequency operation

The capacitance loading at the input and output should be larger at lower frequencies and smaller at higher frequencies to provide sufficient gain for oscillation and insufficient gain to produce oscillation at unwanted overtone frequencies. Third-overtone frequency operation is achieved by adding an external LC circuit consisting of an inductor to ground through a capacitor. For more detailed design considerations, including a schematic of the external component hookup, see the oscillators' general information.

trial values recommended for third-overtone operation (See Figure 1 in the Oscillators' General Information Section)

OSI02LJ

3RD-OVERTONE FREQUENCY	L_{tank}	C_{gnd}	C_{in}‡	C_{out}‡
55 MHz	1 µH	1000 pF	10 pF	10 pF
48 MHz	1.5 µH	1000 pF	10 pF	10 pF
35 MHz	2.2 µH	1000 pF	10 pF	10 pF

‡ C_{in} and C_{out} are the total capacitance of the circuit board and components, excluding the integrated circuit.

Good design practices include:

- Placing the oscillator pins in the least "noisy" area of the package pins.
- Placing the oscillator on two adjacent pin locations.
- Placing the oscillator between a V_{CC} and ground pin utilizing primary or secondary power pin locations.
- Placing large outputs, especially those operating at data rates near the oscillator frequency, away from the oscillator pins.

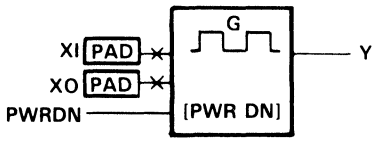
OSI03LJ
20- TO 35-MHz CRYSTAL-CONTROLLED OSCILLATOR

D3030, APRIL 1989

OSCILLATOR CELL

- **Crystal-Controlled Oscillator for Generating On-Chip Clock Signals from 20 to 35 MHz**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The OSI03LJ is a crystal oscillator designed for use with a minimum of external components. The input XI and feedback output XO provide two connections for use with an external series- or parallel-resonant crystal. As a third-harmonic, crystal-controlled oscillator, on-chip frequencies from 20 to 35 MHz can be generated. An internal 91-kΩ biasing resistor can be placed between nodes XI and XO by internal logic. When the oscillator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OSI03LJ XI,PWRDN,XO,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.5		V
I_{CC}	Supply current		V_I = V_{CC} or 0, f_{osc} = 32 MHz	4.8		mA
C_i	Input capacitance	XI		5.54		pF
C_o	Output capacitance	XO		5.4		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns, f_{osc} = 1 MHz	14.8		pF

D3030, APRIL 1989

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	XI	Y	1.2	2.7	5.1	1.3	2.7	4.7	ns
t_{PHL}			1.6	2.8	5	1.6	2.8	4.7	
Δt_{PLH}	XI	Y	60	180	390	100	180	350	ps/pF
Δt_{PHL}			50	100	290	60	100	250	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

series- or parallel-mode crystal operation

A series- or parallel-mode crystal can be used. See oscillators' general information for more detailed information on the selection of crystals.

third-overtone frequency operation

The capacitance loading the input and output should be larger at lower frequencies and smaller at higher frequencies to provide sufficient gain for oscillation and insufficient gain to produce oscillation at unwanted overtone frequencies. Third-overtone frequency operation is achieved by adding an external LC circuit consisting of an inductor to ground through a capacitor. For more detailed design considerations, including a schematic of the external component hookup, see the oscillators' general information.

trial values recommended for third-overtone operation (See Figure 1 in the Oscillators' General Information Section)

OSI03LJ

3RD-OVERTONE FREQUENCY	L_{tank}	C_{gnd}	C_{in}‡	C_{out}‡
35 MHz	2.2 µH	1000 pF	10 pF	10 pF
28 MHz	3.3 µH	1000 pF	10 pF	10 pF
20 MHz	N/A	N/A	27 pF	27 pF

‡ C_{in} and C_{out} are the total capacitance of the circuit board and components, excluding the integrated circuit.

Good design practices include:

- Placing the oscillator pins in the least "noisy" area of the package pins.
- Placing the oscillator on two adjacent pin locations.
- Placing the oscillator between a V_{CC} and ground pin utilizing primary or secondary power pin locations.
- Placing large outputs, especially those operating at data rates near the oscillator frequency, away from the oscillator pins.

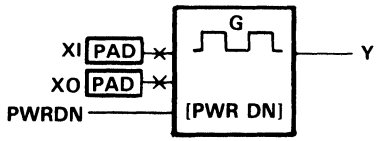
OSI04LJ 1- TO 20-MHz CRYSTAL-CONTROLLED OSCILLATOR

D3030, APRIL 1989

OSCILLATOR CELL

- **Crystal-Controlled Oscillator for Generating On-Chip Clock Signals from 1 to 20 MHz**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Dependable Texas Instruments Quality and Reliability**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The OSI04LJ is a crystal oscillator designed for use with a minimum of external components. The input XI and feedback output XO provide two connections for use with an external series- or parallel-resonant fundamental crystal. As a crystal-controlled oscillator, on-chip frequencies from 1 to 20 MHz can be generated. An internal 91-kΩ biasing resistor can be placed between nodes XI and XO by internal logic. When the oscillator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OSI04LJ XI,PWRDN,XO,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.5		V
I_{CC}	Supply current		$V_I = V_{CC}$ or 0, f_{osc} = 16 MHz	3.2		mA
C_i	Input capacitance	XI		5.06		pF
C_o	Output capacitance	XO		5.22		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns, f_{osc} = 1 MHz	14.5		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	XI	Y	1.2	2.7	5.1	1.3	2.7	4.7	ns
t_{PHL}			1.6	2.8	5	1.6	2.8	4.7	
Δt_{PLH}	XI	Y	60	180	390	100	180	350	ps/pF
Δt_{PHL}			50	100	290	60	100	250	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

series- or parallel-mode crystal operation

A series- or parallel-mode crystal can be used. See oscillators' general information for more detailed information on the selection of crystals. The capacitance loading the input and output should be larger at lower frequencies and smaller at higher frequencies to provide sufficient gain for oscillation and insufficient gain to produce oscillation at unwanted overtone frequencies.

trial RC values recommended for use with fundamental crystals

FUNDAMENTAL FREQUENCY	R_{ext} (C_{in}‡ = C_{out}‡ = 30 pF)	R_{ext} (C_{in}‡ = C_{out}‡ = 64 pF)
20 MHz	0	0
16 MHz	220 Ω	0
12 MHz	470 Ω	220 Ω
8 MHz	1 kΩ	470 Ω
4 MHz	3.3 kΩ	1.5 kΩ
3 MHz	6.8 kΩ	3.3 kΩ
2 MHz	10 kΩ	4.7 kΩ
1 MHz	33 kΩ	15 kΩ

‡ C_{in} and C_{out} are the total capacitance of the circuit board and components, excluding the integrated circuit. Typical values range from 10 pF to 64 pF. For operation at lower frequencies, it is necessary to increase the size of C_{out} and/or R_{ext}.

Good design practices include:

- Placing the oscillator pins in the least "noisy" area of the package pins.
- Placing the oscillator on two adjacent pin locations.
- Placing the oscillator between a V_{CC} and ground pin utilizing primary or secondary power pin locations.
- Placing large outputs, especially those operating at data rates near the oscillator frequency, away from the oscillator pins.

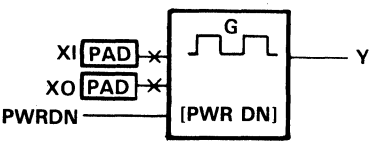
OSI24LJ
1- TO 20-MHz CRYSTAL-CONTROLLED OSCILLATOR WITH TTL THRESHOLD INPUT

D3030, APRIL 1989

OSCILLATOR CELL

- **Crystal-Controlled Oscillator for Generating On-Chip Clock Signals from 1 to 20 MHz**
- **Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V**
- **Dependable Texas Instruments Quality and Reliability**
- **TTL Input Threshold Voltage**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The OSI24LJ is a crystal oscillator designed for use with a minimum of external components. The input XI and feedback output XO provide two connections for use with an external series- or parallel-resonant fundamental crystal. As a crystal-controlled oscillator, on-chip frequencies from 1 to 20 MHz can be generated. An internal 91-kΩ biasing resistor can be placed between nodes XI and XO by internal logic. When the oscillator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OSI24LJ XI,PWRDN,XO,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			1.5		V
I_{CC}	Supply current		$V_I = V_{CC}$ or 0, f_{osc} = 16 MHz	3.2		mA
C_i	Input capacitance	XI		5.06		pF
C_o	Output capacitance	XO		5.22		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns, f_{osc} = 1 MHz	14.5		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	XI	Y	1.89	3.78	7	2	3.78	6.44	ns
t_{PHL}			1.73	3.86	7.85	1.83	3.86	7.11	
Δt_{PLH}	XI	Y	153	200	337	151	200	307	ps/pF
Δt_{PHL}			124	240	325	124	240	300	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

series- or parallel-mode crystal operation

A series- or parallel-mode crystal can be used. See oscillators' general information for more detailed information on the selection of crystals. The capacitance loading the input and output should be larger at lower frequencies and smaller at higher frequencies to provide sufficient gain for oscillation yet insufficient gain to produce oscillation at unwanted overtone frequencies.

trial RC values recommended for use with fundamental crystals

FUNDAMENTAL FREQUENCY	R_{ext} (C_{in}‡ = C_{out}‡ = 30 pF)	R_{ext} (C_{in}‡ = C_{out}‡ = 64 pF)
20 MHz	0	0
16 MHz	220 Ω	0
12 MHz	470 Ω	220 Ω
8 MHz	1 kΩ	470 Ω
4 MHz	3.3 kΩ	1.5 kΩ
3 MHz	6.8 kΩ	3.3 kΩ
2 MHz	10 kΩ	4.7 kΩ
1 MHz	33 kΩ	15 kΩ

‡ C_{in} and C_{out} are the total capacitance of the circuit board and components, excluding the integrated circuit. Typical values range from 10 pF to 64 pF. For operation at lower frequencies, it is necessary to increase the size of C_{out} and/or R_{ext}.

Good design practices include:

- Placing the oscillator pins in the least "noisy" area of the package pins.
- Placing the oscillator on two adjacent pin locations.
- Placing the oscillator between a V_{CC} and ground pin utilizing primary or secondary power pin locations.
- Placing large outputs, especially those operating at data rates near the oscillator frequency, away from the oscillator pins.

D3030, APRIL 1988

INPUT BUFFER CELLS

The TSC500 Series CMOS standard cell provides the custom IC designer a wide selection of input buffers. For each input offered, both a CMOS and a TTL threshold input buffer version is available. The inputs can be used with an active pull-up or pull-down terminator. Use of a terminator ensures that the input will be driven to a high- or low-logic level thereby avoiding exposure to a high-impedance or floating condition. When used, the terminator is connected to the input node.

All input cells are designed to actively bypass and dissipate electrostatic discharges (ESD). Guard-ring structures, which provide current management techniques for the cell to recover from exposure to currents of up to 250 mA, are employed to negate most common sources that can produce a latch-up condition.

The following input cells are available in the TSC500 Series CMOS standard cell library:

INPUT BUFFERS FUNCTIONAL INDEX

DESCRIPTION	CELL NAME	OUTPUT DRIVE	COMMENTS	PAGE
Input buffers	IPI01LJ	1X	CMOS compatible	11-3
	IPI04LJ	1X	TTL compatible	11-5
	IPI07LJ	1X	CMOS compatible with hysteresis	11-7
	IPI09LJ	1X	TTL compatible with hysteresis	11-9
Input clock buffers	IPI11LJ	1X	CMOS compatible	11-11
	IPI14LJ	1X	TTL compatible	11-13

IPI01LJ
CMOS-COMPATIBLE INPUT BUFFER

D3030, APRIL 1988

INPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The IPI01LJ is an input buffer that interfaces CMOS input levels to CMOS internal voltage levels. A pull-up or pull-down terminator can be connected to the A node.

When the input buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IPI01LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

absolute maximum ratings and recommended operating conditions

These specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	TYP§	MAX	UNIT
V_T	Input threshold voltage			2.5		V
I_{CC}	Supply current	−55°C to 125°C	$V_I = V_{IH}$ or V_{IL}		4.72	mA
		0°C to 70°C			0.49	
I_I	Input current¶		$V_I = V_{CC}$ or 0		±1	µA
C_i	Intrinsic input capacitance#			4.41		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.97		pF

‡ For input voltages, V_{IH} or V_{IL}, see the TSC500 Series Data.
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Total current does not include pull-up or pull-down current source.
# Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y		0.56	0.9	1.5	0.59	0.9	1.42	ns
t_{PHL}				0.12	0.63	1.19	0.13	0.63	1.13	
Δt_{PLH}	A	Y		0.07	0.18	0.33	0.7	0.18	0.29	ns/pF
Δt_{PHL}				0.12	0.12	0.27	0.12	0.12	0.26	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IPI04LJ
TTL-COMPATIBLE INPUT BUFFER

D3030, APRIL 1988

INPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The IPI04LJ is an input buffer that interfaces TTL input levels to CMOS internal voltage levels. A pull-up or pull-down terminator can be connected to the A node.

When the input buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IPI04LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	TYP§	MAX	UNIT
V_T	Input threshold voltage			1.3		V
I_{CC}	Supply current	−55°C to 125°C	$V_I = V_{IH}$ or V_{IL}		3.57	mA
		0°C to 70°C			0.3	
I_I	Input current¶		$V_I = V_{CC}$ or 0		±1	µA
C_i	Intrinsic input capacitance#			4.41		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	2.82		pF

‡ For input voltages, V_{IH} or V_{IL}, see the TSC500 Series Data.
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Total current does not include pull-up or pull-down current source.
# Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y		0.79	1.41	2.23	0.82	1.41	2.14	ns
t_{PHL}				0.04	1.16	3.11	0.05	1.16	2.96	
Δt_{PLH}	A	Y		0.05	0.18	0.37	0.05	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.53	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IPI07LJ
CMOS-COMPATIBLE INPUT BUFFER WITH HYSTERESIS

D3030, APRIL 1988

INPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The IPI07LJ is an input buffer that interfaces CMOS input levels to CMOS internal voltage levels. A pull-up or pull-down terminator can be connected to the A node.

When the input buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IPI07LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	TYP§	MAX	UNIT
V_{T+}	Positive-going threshold voltage			3.35		V
V_{T-}	Negative-going threshold level			1.65		V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)			1.7		V
I_{CC}	Supply current	−55°C to 125°C	$V_I = V_{IH}$ or V_{IL}		0.82	mA
		0°C to 70°C			0.48	
I_I	Input current¶		$V_I = V_{CC}$ or 0		±1	µA
C_i	Intrinsic input capacitance#			4.17		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	4.53		pF

‡ For input voltages, V_{IH} or V_{IL}, see the TSC500 Series Data.
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Total current does not include pull-up or pull-down current source.
# Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y		1.2	1.62	2.27	1.24	1.62	2.18	ns
t_{PHL}				1.39	2.06	3.31	1.42	2.06	3.13	
Δt_{PLH}	A	Y		0.08	0.2	0.4	0.9	0.2	0.36	ns/pF
Δt_{PHL}				0.06	0.19	0.37	0.06	0.19	0.35	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IPI09LJ
TTL-COMPATIBLE INPUT BUFFER WITH HYSTERESIS

D3030, APRIL 1988

INPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The IPI09LJ is an input buffer that interfaces TTL input levels to CMOS internal voltage levels. A pull-up or pull-down terminator can be connected to the A node.

When the input buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IPI09LJ A,Y;

absolute maximum ratings and recommended operating conditions

These specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	TYP§	MAX	UNIT
V_{T+}	Positive-going threshold voltage			1.6		V
V_{T-}	Negative-going threshold level			1.2		V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)			0.4		V
I_{CC}	Supply current	−55°C to 125°C	$V_I = V_{IH}$ or V_{IL}		1.82	mA
		0°C to 70°C			0.28	
I_I	Input current¶		$V_I = V_{CC}$ or 0		±1	µA
C_i	Intrinsic input capacitance#			4.22		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	2.43		pF

‡ For input voltages, V_{IH} or V_{IL}, see the TSC500 Series Data.
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Total current does not include pull-up or pull-down current source.
# Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y		0.78	1.29	1.96	0.8	1.29	1.88	ns
t_{PHL}				0.2	1.77	5.06	0.22	1.77	4.79	
Δt_{PLH}	A	Y		0.05	0.18	0.35	0.06	0.18	0.31	ns/pF
Δt_{PHL}				0.04	0.25	0.61	0.04	0.25	0.58	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IPI11LJ CMOS-COMPATIBLE INPUT CLOCK BUFFER

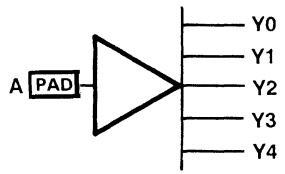
D3030, APRIL 1988

INPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Yn
L	L
H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Yn = A

description

The IPI11LJ is an input clock buffer that interfaces CMOS input levels to CMOS internal voltage levels. The buffer contains five internal clock-driver outputs that can be used to drive up to 3 pF (total) of interconnected loads each. A pull-up or pull-down terminator can be connected to the A node.

When the input clock buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IPI11LJ A,Y0,Y1,Y2,Y3,Y4;

absolute maximum ratings and recommended operating conditions

The maximum capacitive load permitted on each output is 3 pF.

Other ratings and conditions are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	TYP§	MAX	UNIT
V_T	Input threshold voltage			2.5		V
I_{CC}	Supply current	−55°C to 125°C	$V_I = V_{IH}$ or V_{IL}		5.97	mA
		0°C to 70°C			1.17	
I_I	Input current¶		$V_I = V_{CC}$ or 0		±1	µA
C_i	Intrinsic input capacitance#			5.87		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	12.7		pF

‡ For input voltages, V_{IH} or V_{IL}, see the TSC500 Series Data.
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Total current does not include pull-up or pull-down current source.
# Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Yn		0.75	1.55	2.65	0.79	1.55	2.5	ns
t_{PHL}				0.72	1.45	2.68	0.74	1.45	2.52	
Δt_{PLH}	A	Yn		0.09	0.15	0.34	0.09	0.15	0.33	ns/pF
Δt_{PHL}				0.1	0.19	0.32	0.11	0.19	0.32	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IPI14LJ
TTL-COMPATIBLE INPUT CLOCK BUFFER

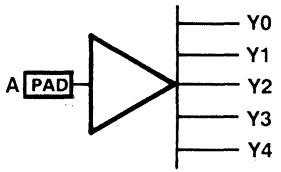
D3030, APRIL 1988

INPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Yn
L	L
H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Yn = A

description

The IPI14LJ is an input clock buffer that interfaces TTL input levels to CMOS internal voltage levels. The buffer contains five internal clock-driver outputs that can be used to drive up to 3 pF (total) of interconnected loads each. A pull-up or pull-down terminator can be connected to the A node.

When the input clock buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IPI14LJ A,Y0,Y1,Y2,Y3,Y4;

absolute maximum ratings and recommended operating conditions

The maximum capacitive load permitted on each output is 3 pF.

Other ratings and conditions are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡			TEST CONDITIONS	TYP§	MAX	UNIT
V_T	Input threshold voltage			1.3		V
I_{CC}	Supply current	−55°C to 125°C	$V_I = V_{IH}$ or V_{IL}		2.92	mA
		0°C to 70°C			0.3	
I_I	Input current¶		$V_I = V_{CC}$ or 0		±1	µA
C_i	Intrinsic input capacitance#			4.44		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	10.7		pF

‡ For input voltages, V_{IH} or V_{IL}, see the TSC500 Series Data.

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ Total current does not include pull-up or pull-down current source.

Total input capacitance is dependent on the package type and is equal to the sum of package capacitance and intrinsic input capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Yn		0.96	2.4	4.86	1.02	2.4	4.49	ns
t_{PHL}				0.85	2.21	4.85	0.91	2.21	4.43	
Δt_{PLH}	A	Yn		0.06	0.19	0.36	0.07	0.19	0.32	ns/pF
Δt_{PHL}				0.07	0.12	0.3	0.06	0.12	0.26	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

12 Bidirectional Buffers (I/O)

BIDIRECTIONAL INPUT/OUTPUT BUFFER CELLS

The TSC500 Series CMOS standard cell library provides the custom IC designer a selection of noninverting 3-state and open-drain input/output buffer cells that interface CMOS internal cells with TTL or CMOS bidirectional bus lines. The input buffer responds to either CMOS or TTL threshold logic levels imposed on the I/O bus regardless of the logic state of the 3-state output control, GZ.

Each bidirectional I/O buffer is offered in the following options with respect to di/dt circuitry:

CELL CLASS	RELATIVE di/dt	APPLICATION
IOIxxLJ	1	Critical path(s) only (least delay)
IOJxxLJ	0.5	Can reduce GND pins by up to 25%
IOKxxLJ	0.25	Can reduce GND pins by up to 45%
IOHxxLJ	0.125	Can reduce GND pins by up to 60% (most delay)

The cells are designed to actively bypass and dissipate electrostatic discharges (ESD). Guard-ring structures that provide current management techniques for the cell to recover from exposure to currents of up to 250 mA are employed, thereby negating the most common sources that can produce a latch-up condition.

The buffers can be used with an active pull-up or pull-down terminator. When used, the terminator is connected to the output node. Use of a terminator ensures that the I/O will be driven to a high- or low-logic level thereby avoiding exposure to a high-impedance or floating condition.

These output cells are designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current to flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

The dynamic-drive capability of each buffer is specified by the delta propagation delay time parameters included with the switching characteristics. The delta propagation delay times provide a means for making direct comparisons of the various output responses to changes in capacitive loading.

3-STATE AND OPEN-DRAIN INPUT/OUTPUT BUFFER CELLS GENERAL INFORMATION

D3030, APRIL 1988

The following input/output cells are available in the TSC500 Series CMOS standard cell library:

3-STATE INPUT/OUTPUT BUFFER CELL SELECTION TABLE

CELL NAME				OUTPUT CURRENT (mA)		INPUT THRESHOLD
di/dt = 1	di/dt = 0.5	di/dt = 0.25	di/dt = 0.125	SINK	SOURCE	
IOIA1LJ	IOJA1LJ	IOKA1LJ	IOHA1LJ	16	16	CMOS
IOIA4LJ	IOJA4LJ	IOKA4LJ	IOHA4LJ	16	16	TTL
IOIB1LJ	IOJB1LJ	IOKB1LJ	IOHB1LJ	24	16	CMOS
IOIB4LJ	IOJB4LJ	IOKB4LJ	IOHB4LJ	24	16	TTL
IOIE1LJ	IOJE1LJ	IOKE1LJ	IOHE1LJ	48	16	CMOS
IOIE4LJ	IOJE4LJ	IOKE4LJ	IOHE4LJ	48	16	TTL
IOIG1LJ	IOJG1LJ	IOKG1LJ	IOHG1LJ	64	16	CMOS
IOIG4LJ	IOJG4LJ	IOKG4LJ	IOHG4LJ	64	16	TTL
IOI01LJ	IOJ01LJ	IOK01LJ	IOH01LJ	10	10	CMOS
IOI04LJ	IOJ04LJ	IOK04LJ	IOH04LJ	10	10	TTL
IOI21LJ	IOJ21LJ	IOK21LJ	IOH21LJ	2	2	CMOS
IOI24LJ	IOJ24LJ	IOK24LJ	IOH24LJ	2	2	TTL
IOI41LJ	IOJ41LJ	IOK41LJ	IOH41LJ	4	4	CMOS
IOI44LJ	IOJ44LJ	IOK44LJ	IOH44LJ	4	4	TTL
IOI61LJ	IOJ61LJ	IOK61LJ	IOH61LJ	6	6	CMOS
IOI64LJ	IOJ64LJ	IOK64LJ	IOH64LJ	6	6	TTL

OPEN-DRAIN INPUT/OUTPUT BUFFER CELL SELECTION TABLE

CELL NAME				OUTPUT SINK CURRENT (mA)	INPUT THRESHOLD
di/dt = 1	di/dt = 0.5	di/dt = 0.25	di/dt = 0.125		
IOIEPLJ	IOJEPLJ	IOKEPLJ	IOHEPLJ	48	TTL

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IOIA1LJ
16-mA 3-STATE I/O BUFFER WITH CMOS INPUT AND CMOS/TTL OUTPUT

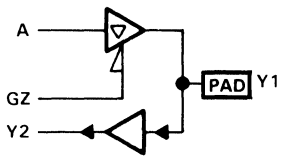
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOIA1LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOIA1LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −16 mA					3.7		V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 16 mA						0.5	V
			I_{OL} = 13.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.6			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		27.2			27.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.79	2.25	5.1	0.84	2.25	4.66	ns
t_{PHL}				1.01	2.7	5.88	1.09	2.7	5.35	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.78	2.49	5.79	0.83	2.49	5.3	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.97	2.58	5.58	1.04	2.58	5.08	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.94	2.68	6.13	0.99	2.68	5.6	ns
t_{PHL}				1.5	3.76	7.96	1.61	3.76	7.22	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.94	2.94	6.83	1.01	2.94	6.25	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.47	3.69	7.78	1.58	3.69	7.06	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.41			9.41		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.57			9.57		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		0	10	30	0	10	30	ps/pF
Δt_{PHL}				10	30	60	10	30	50	
Δt_{PZH}	GZ	Y1		0	10	30	0	10	30	ps/pF
Δt_{PZL}				10	30	60	20	30	60	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.92	2.6	5.8	0.97	2.6	5.3	ns
t_{PHL}				0.9	2.36	5.23	0.96	2.36	4.75	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.02	2.86	6.41	1.08	2.86	5.85	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.84	2.22	4.87	0.89	2.22	4.43	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.21	3.37	7.44	1.28	3.37	6.8	ns
t_{PHL}				1.22	3.11	6.75	1.3	3.11	6.12	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.32	3.64	8.09	1.4	3.64	7.39	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.19	3.01	6.51	1.27	3.01	5.91	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	50	10	20	40	ps/pF
Δt_{PHL}				10	20	40	10	20	40	
Δt_{PZH}	GZ	Y1		10	20	50	10	20	40	ps/pF
Δt_{PZL}				10	20	50	10	20	40	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.61	0.9	1.41	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.06	0.2	0.32	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOIA4LJ
16-mA 3-STATE I/O BUFFER WITH TTL INPUT AND CMOS/TTL OUTPUT

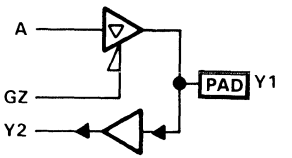
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOIA4LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOIA4LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 16 mA						0.5	V
			I_{OL} = 13.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		28.2			28.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.79	2.25	5.1	0.84	2.25	4.65	ns
t_{PHL}				1.01	2.7	5.87	1.08	2.7	5.34	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.78	2.49	5.78	0.83	2.49	5.29	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.97	2.57	5.57	1.03	2.57	5.07	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.94	2.68	6.13	0.99	2.68	5.59	ns
t_{PHL}				1.5	3.75	7.95	1.61	3.75	7.21	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.94	2.94	6.83	1	2.94	6.25	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.47	3.68	7.77	1.58	3.68	7.05	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.41			9.41		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.42			9.42		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		0	10	30	0	10	30	ps/pF
Δt_{PHL}				10	30	60	10	30	50	
Δt_{PZH}	GZ	Y1		0	10	30	0	10	30	ps/pF
Δt_{PZL}				10	30	60	20	30	60	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.92	2.6	5.79	0.97	2.6	5.3	ns
t_{PHL}				0.89	2.36	5.22	0.95	2.36	4.74	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.02	2.86	6.41	1.08	2.86	5.85	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.83	2.21	4.86	0.89	2.21	4.43	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.21	3.37	7.44	1.28	3.37	6.81	ns
t_{PHL}				1.22	3.1	6.74	1.3	3.1	6.12	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.32	3.65	8.09	1.4	3.65	7.39	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.19	3.01	6.5	1.27	3.01	5.9	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	50	10	20	40	ps/pF
Δt_{PHL}				10	20	40	10	20	40	
Δt_{PZH}	GZ	Y1		10	20	50	10	20	40	ps/pF
Δt_{PZL}				10	20	50	10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOIB1LJ
24-mA 3-STATE I/O BUFFER WITH CMOS INPUT AND CMOS/TTL OUTPUT

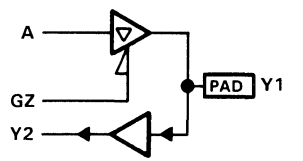
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOIB1LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOIB1LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 24 mA						0.5	V
			I_{OL} = 20.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.6			0.49	mA
C_i	Input capacitance	Y1			13.9			13.9		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		29.9			29.9		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.85	2.35	5.3	0.9	2.35	4.82	ns
t_{PHL}				0.91	2.48	5.48	0.98	2.48	4.99	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.79	2.51	5.84	0.84	2.51	5.34	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.85	2.37	5.2	0.91	2.37	4.74	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.98	2.75	6.26	1.04	2.75	5.71	ns
t_{PHL}				1.26	3.28	7.07	1.35	3.28	6.43	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.95	2.97	6.88	1.01	2.97	6.3	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.23	3.21	6.88	1.33	3.21	6.25	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.43			9.43		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.57			8.57		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		0	10	30	0	10	30	ps/pF
Δt_{PHL}				10	20	50	10	20	40	
Δt_{PZH}	GZ	Y1		0	10	30	0	10	30	ps/pF
Δt_{PZL}				10	20	50	10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	0.97	2.7	5.97	1.03	2.7	5.45	ns
t_{PHL}				0.81	2.21	4.95	0.87	2.21	4.5	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.03	2.88	6.46	1.09	2.88	5.9	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.77	2.08	4.62	0.82	2.08	4.21	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.24	3.44	7.56	1.32	3.44	6.91	ns
t_{PHL}				1.06	2.79	6.15	1.14	2.79	5.59	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.33	3.67	8.14	1.41	3.67	7.43	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.03	2.71	5.91	1.11	2.71	5.38	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
Δt_{PLH}	A	Y1		10	20	50	10	20	40	ps/pF
Δt_{PHL}				10	20	30	10	20	30	
Δt_{PZH}	GZ	Y1		10	20	50	10	20	40	ps/pF
Δt_{PZL}				10	20	40	10	20	30	

Input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ps/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOIB4LJ
24-mA 3-STATE I/O BUFFER WITH TTL INPUT AND CMOS/TTL OUTPUT

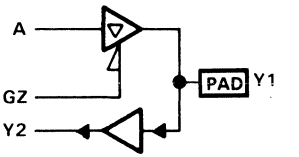
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOIB4LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOIB4LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −16 mA					3.7		V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 24 mA						0.5	V
			I_{OL} = 20.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.9			13.9		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		29.9			29.9		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.85	2.35	5.3	0.9	2.35	4.82	ns
t_{PHL}				0.91	2.48	5.48	0.97	2.48	4.99	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.79	2.51	5.84	0.84	2.51	5.34	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.85	2.37	5.19	0.91	2.37	4.73	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.98	2.75	6.25	1.04	2.75	5.7	ns
t_{PHL}				1.25	3.27	7.07	1.35	3.27	6.42	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.95	2.97	6.88	1.01	2.97	6.3	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.23	3.21	6.87	1.32	3.21	6.25	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.43			9.43		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.57			8.57		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		0	10	30	0	10	30	ps/pF
Δt_{PHL}				10	20	50	10	20	40	
Δt_{PZH}	GZ	Y1		0	10	30	0	10	30	ps/pF
Δt_{PZL}				10	20	50	10	20	40	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	3	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.53	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.97	2.7	5.97	1.03	2.7	5.45	ns
t_{PHL}				0.81	2.21	4.95	0.87	2.21	4.49	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.03	2.88	6.46	1.09	2.86	5.9	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.77	2.08	4.62	0.82	2.08	4.21	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.24	3.44	7.56	1.32	3.44	6.91	ns
t_{PHL}				1.06	2.79	6.15	1.14	2.79	5.59	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.33	3.67	8.14	1.41	3.67	7.43	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.03	2.71	5.91	1.11	2.71	5.37	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	50	10	20	40	ps/pF
Δt_{PHL}				10	20	30	10	20	30	
Δt_{PZH}	GZ	Y1		10	20	50	10	20	40	ps/pF
Δt_{PZL}				10	20	40	10	20	30	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOIEPLJ
48-mA OPEN-DRAIN I/O BUFFER WITH TTL INPUT WITH HYSTERESIS, AND CMOS/TTL OUTPUT

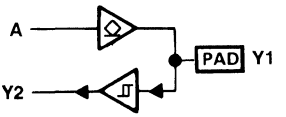
D3030, DECEMBER 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUTS	
A	Y1	Y1	Y2
L	L	L	L
H	H	H‡	H
H	L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A‡ Y2 = Y1

description

The IOIEPLJ is a noninverting open-drain input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip terminated bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus when the internal A node is at a high logic level. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOIEPLJ A,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_T	Input threshold voltage at A				2.2			2.2		V
V_{T+}	Positive-going threshold level at Y1				1.6			1.6		V
V_{T-}	Negative-going threshold level at Y1				1.2			1.2		V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$) at Y1				0.4			0.4		V
V_{OL}	Low-level output voltage		I_{OL} = 48 mA						0.5	V
			I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10			±5	μA
I_{CC}	Supply current		$V_I = V_{IH}$ or V_{IL}			6.6			1.14	mA
C_i	Input capacitance	A			0.59			0.59		pF
		Y1			11.2			11.2		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		10.4			10.4		pF

‡ With external pull-up resistor to Y2.

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y1	C_L = 15 pF	0.38	1.04	2.2	0.41	1.04	2.02	ns
			C_L = 50 pF	0.61	1.54	3.21	0.65	1.54	2.93	
t_{PLZ}	A	Y1			7.61			7.61		ns
Δt_{PZL}	A	Y1		10	10	30	10	10	30	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y1	C_L = 15 pF	0.34	0.87	1.85	0.36	0.87	1.7	ns
			C_L = 50 pF	0.52	1.25	2.64	0.55	1.25	2.41	
Δt_{PZL}	A	Y1		10	10	20	10	10	20	ps/pF

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2	C_L = 0	0.78	1.29	1.97	0.8	1.29	1.89	ns
t_{PHL}				0.21	1.79	5.05	0.22	1.79	4.83	
Δt_{PLH}	Y1	Y2		0.06	0.17	0.34	0.07	0.17	0.31	ns/pF
Δt_{PHL}				0.03	0.25	0.62	0.04	0.25	0.58	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOIE1LJ
48-mA 3-STATE I/O BUFFER WITH CMOS INPUT AND CMOS/TTL OUTPUT

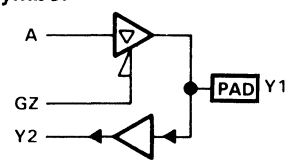
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOIE1LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOIE1LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −16 mA					3.7		V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 48 mA						0.5	V
			I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.6			0.49	mA
C_i	Input capacitance	Y1			15.4			15.4		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		44.3			44.3		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.98	2.77	6.26	1.04	2.77	5.68	ns
t_{PHL}				0.8	2.23	5.06	0.85	2.23	4.6	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.81	2.56	5.95	0.87	2.56	5.45	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.79	2.16	4.84	0.83	2.16	4.42	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.09	3.08	6.99	1.16	3.08	6.35	ns
t_{PHL}				0.99	2.71	6.02	1.05	2.71	5.47	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.97	3.01	6.99	1.03	3.01	6.4	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.98	2.65	5.82	1.04	2.65	5.31	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.55			9.55		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.62			9.62		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		0	10	20	0	10	20	ps/pF
Δt_{PHL}				10	10	30	10	10	20	
Δt_{PZH}	GZ	Y1		0	10	30	0	10	30	ps/pF
Δt_{PZL}				10	10	30	10	10	30	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.1	3.1	6.9	1.17	3.1	6.28	ns
t_{PHL}				0.75	2.05	4.68	0.79	2.05	4.26	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.05	2.94	6.6	1.11	2.94	6.02	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.72	1.97	4.44	0.76	1.97	4.05	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.36	3.76	8.28	1.45	3.76	7.55	ns
t_{PHL}				0.89	2.4	5.43	0.95	2.4	4.94	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.35	3.73	8.27	1.44	3.73	7.55	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.88	2.34	5.22	0.93	2.34	4.76	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	40	10	20	40	ps/pF
Δt_{PHL}				0	10	20	0	10	20	
Δt_{PZH}	GZ	Y1		10	20	50	10	20	40	ps/pF
Δt_{PZL}				0	10	20	0	10	20	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.53	0.6	0.9	1.41	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.33	0.07	0.2	0.32	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOIE4LJ
48-mA 3-STATE I/O BUFFER WITH TTL INPUT AND CMOS/TTL OUTPUT

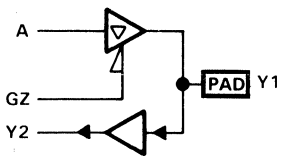
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOIE4LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOIE4LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 48 mA						0.5	V
			I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			15.4			15.4		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		45.2			45.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.98	2.77	6.26	1.04	2.77	5.68	ns
t_{PHL}				0.8	2.24	5.07	0.85	2.24	4.61	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.81	2.56	5.95	0.87	2.56	5.45	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.79	2.16	4.83	0.83	2.16	4.41	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.09	3.08	6.99	1.16	3.08	6.35	ns
t_{PHL}				0.99	2.7	6.01	1.05	2.7	5.47	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.97	3.01	6.99	1.03	3.01	6.4	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.98	2.65	5.81	1.04	2.65	5.3	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.55			9.55		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.62			9.62		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		0	10	20	0	10	20	ps/pF
Δt_{PHL}				10	10	30	10	10	20	
Δt_{PZH}	GZ	Y1		0	10	30	0	10	30	ps/pF
Δt_{PZL}				10	10	30	10	10	30	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.83	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	3	
Δt_{PLH}	Y1	Y2		0.05	0.18	0.37	0.05	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.53	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.1	3.1	6.9	1.17	3.1	6.27	ns
t_{PHL}				0.75	2.04	4.69	0.79	2.04	4.26	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.05	2.94	6.6	1.11	2.94	6.02	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.72	1.96	4.44	0.76	1.96	4.05	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.36	3.77	8.28	1.45	3.77	7.55	ns
t_{PHL}				0.89	2.4	5.43	0.95	2.4	4.94	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.35	3.73	8.27	1.44	3.73	7.55	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.88	2.34	5.22	0.93	2.34	4.75	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	40	10	20	40	ps/pF
Δt_{PHL}				0	10	20	0	10	20	
Δt_{PZH}	GZ	Y1		10	20	50	10	20	40	ps/pF
Δt_{PZL}				0	10	20	0	10	20	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOIG1LJ
64-mA 3-STATE I/O BUFFER WITH CMOS INPUT AND CMOS/TTL OUTPUT

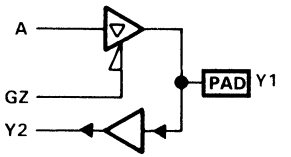
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOIG1LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOIG1LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 64 mA						0.5	V
			I_{OL} = 54.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.1			0.49	mA
C_i	Input capacitance	Y1			16.6			16.6		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		55.6			55.6		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.06	3.09	7.05	1.13	3.09	6.39	ns
t_{PHL}				0.79	2.21	5.06	0.84	2.21	4.6	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.83	2.6	6.03	0.88	2.6	5.52	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.78	2.16	4.85	0.82	2.16	4.43	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.18	3.38	7.7	1.26	3.38	7	ns
t_{PHL}				0.94	2.59	5.83	1	2.59	5.31	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.98	3.05	7.07	1.05	3.05	6.46	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.94	2.54	5.64	0.99	2.54	5.14	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.63			9.63		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10.17			10.17		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		0	10	20	0	10	20	ps/pF
Δt_{PHL}				0	10	20	0	10	20	
Δt_{PZH}	GZ	Y1		0	10	30	0	10	30	ps/pF
Δt_{PZL}				0	10	20	0	10	20	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

10IG1LJ
64-mA 3-STATE I/O BUFFER WITH CMOS INPUT AND CMOS/TTL OUTPUT

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.2	3.42	7.69	1.27	3.42	6.98	ns
t_{PHL}				0.74	2.05	4.73	0.78	2.05	4.3	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.07	2.98	6.69	1.13	2.98	6.11	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.72	1.98	4.51	0.76	1.98	4.11	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.45	4.06	8.99	1.54	4.06	8.19	ns
t_{PHL}				0.86	2.34	5.35	0.91	2.34	4.86	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.37	3.77	8.36	1.45	3.77	7.63	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.85	2.29	5.15	0.89	2.29	4.69	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	40	10	20	30	ps/pF
Δt_{PHL}				0	10	20	0	10	20	
Δt_{PZH}	GZ	Y1		10	20	50	10	20	40	ps/pF
Δt_{PZL}				0	10	20	0	10	20	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.57	0.91	1.53	0.6	0.91	1.42	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.07	0.19	0.32	0.08	0.19	0.3	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOIG4LJ
64-mA 3-STATE I/O BUFFER WITH TTL INPUT AND CMOS/TTL OUTPUT

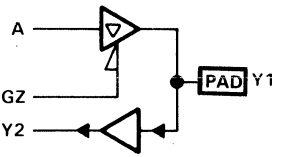
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOIG4LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOIG4LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −16 mA					3.7		V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 64 mA						0.5	V
			I_{OL} = 54.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			16.6			16.6		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		56.6			56.6		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.05	3.09	7.04	1.12	3.09	6.39	ns
t_{PHL}				0.79	2.22	5.07	0.84	2.22	4.61	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.82	2.6	6.03	0.88	2.6	5.52	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.78	2.15	4.86	0.82	2.15	4.43	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.17	3.38	7.7	1.25	3.38	7	ns
t_{PHL}				0.94	2.59	5.83	1	2.59	5.31	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.98	3.05	7.07	1.04	3.05	6.46	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.94	2.54	5.65	0.99	2.54	5.15	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.63			9.63		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10.17			10.17		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		0	10	20	0	10	20	ps/pF
Δt_{PHL}				0	10	20	0	10	20	
Δt_{PZH}	GZ	Y1		0	10	30	0	10	30	ps/pF
Δt_{PZL}				0	10	20	0	10	20	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.82	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	3	
Δt_{PLH}	Y1	Y2		0.05	0.18	0.37	0.05	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.53	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.18	3.42	7.69	1.26	3.42	6.98	ns
t_{PHL}				0.74	2.04	4.73	0.78	2.04	4.3	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.07	2.98	6.69	1.13	2.98	6.11	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.72	1.98	4.51	0.76	1.98	4.11	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.44	4.06	9	1.53	4.06	8.19	ns
t_{PHL}				0.86	2.34	5.34	0.91	2.34	4.86	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.37	3.77	8.36	1.45	3.77	7.63	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.85	2.29	5.15	0.9	2.29	4.68	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	40	10	20	30	ps/pF
Δt_{PHL}				0	10	20	0	10	20	
Δt_{PZH}	GZ	Y1		10	20	50	10	20	40	ps/pF
Δt_{PZL}				0	10	20	0	10	20	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOI01LJ
10-mA 3-STATE I/O BUFFER WITH CMOS INPUT AND CMOS/TTL OUTPUT

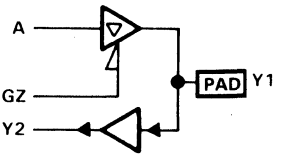
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOI01LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOI01LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −10 mA				3.7			V
			I_{OH} = −8.5 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 10 mA						0.5	V
			I_{OL} = 8.5 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.7			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		21.4			21.4		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.83	2.27	5.12	0.88	2.27	4.67	ns
t_{PHL}				1.23	3.15	6.76	1.31	3.15	6.14	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.83	2.53	5.82	0.88	2.53	5.33	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.2	3.08	6.61	1.28	3.08	6	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.04	2.9	6.59	1.1	2.9	6.02	ns
t_{PHL}				2	4.78	9.91	2.14	4.78	8.98	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.04	3.17	7.32	1.11	3.17	6.7	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.99	4.77	9.92	2.13	4.77	8.97	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.89			9.89		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.86			8.86		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	40	10	20	40	ps/pF
Δt_{PHL}				20	50	90	20	50	80	
Δt_{PZH}	GZ	Y1		10	20	40	10	20	40	ps/pF
Δt_{PZL}				20	50	90	20	50	80	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.01	2.77	6.08	1.07	2.77	5.56	ns
t_{PHL}				1.04	2.67	5.85	1.1	2.67	5.32	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.12	3.04	6.73	1.19	3.04	6.15	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1	2.57	5.6	1.06	2.57	5.1	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.46	3.94	8.56	1.56	3.94	7.83	ns
t_{PHL}				1.54	3.79	8.11	1.65	3.79	7.35	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.59	4.24	9.29	1.69	4.24	8.49	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.53	3.74	7.97	1.63	3.74	7.23	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	70	10	30	60	ps/pF
Δt_{PHL}				10	30	60	20	30	60	
Δt_{PZH}	GZ	Y1		10	30	70	10	30	70	ps/pF
Δt_{PZL}				10	30	70	20	30	60	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.61	0.9	1.41	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.06	0.2	0.32	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOI04LJ
10-mA 3-STATE I/O BUFFER WITH TTL INPUT AND CMOS/TTL OUTPUT

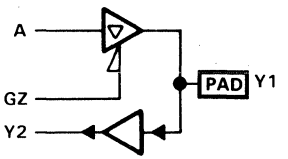
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOI04LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOI04LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −10 mA					3.7		V
			I_{OH} = −8.5 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 10 mA						0.5	V
			I_{OL} = 8.5 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		22.4			22.4		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted).

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.83	2.27	5.12	0.88	2.27	4.67	ns
t_{PHL}				1.22	3.14	6.75	1.31	3.14	6.13	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.83	2.53	5.82	0.88	2.53	5.33	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.19	3.07	6.6	1.28	3.07	5.99	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.04	2.9	6.59	1.1	2.9	6.02	ns
t_{PHL}				2	4.77	9.89	2.14	4.77	8.97	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.04	3.17	7.33	1.11	3.17	6.7	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.99	4.76	9.9	2.13	4.76	8.96	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.89			9.89		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.85			8.85		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	40	10	20	40	ps/pF
Δt_{PHL}				20	50	90	20	50	80	
Δt_{PZH}	GZ	Y1		10	20	40	10	20	40	ps/pF
Δt_{PZL}				20	50	90	20	50	80	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.82	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	3	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.06	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.53	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.01	2.77	6.08	1.07	2.77	5.56	ns
t_{PHL}				1.04	2.66	5.85	1.1	2.66	5.31	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.12	3.04	6.73	1.19	3.04	6.15	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1	2.56	5.6	1.06	2.56	5.09	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.47	3.95	8.56	1.56	3.95	7.84	ns
t_{PHL}				1.54	3.78	8.1	1.65	3.78	7.35	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.59	4.24	9.3	1.69	4.24	8.49	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.53	3.73	7.97	1.63	3.73	7.22	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	70	10	30	70	ps/pF
Δt_{PHL}				10	30	60	20	30	60	
Δt_{PZH}	GZ	Y1		10	30	70	10	30	70	ps/pF
Δt_{PZL}				10	30	70	20	30	60	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOI21LJ
2-mA 3-STATE I/O BUFFER WITH CMOS INPUT AND CMOS/TTL OUTPUT

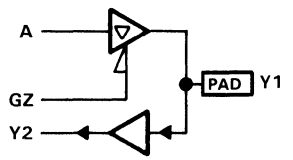
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOI21LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOI21LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −2 mA				3.7			V
			I_{OH} = −1.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 2 mA						0.5	V
			I_{OL} = 1.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.7			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.2			17.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.46	4.07	9.24	1.55	4.07	8.46	ns
t_{PHL}				3.58	8.34	16.93	3.86	8.34	15.32	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.47	4.43	10.47	1.56	4.43	9.54	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.7	9.15	20.4	3.99	9.15	18.01	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.41	6.98	15.99	2.56	6.98	14.66	ns
t_{PHL}				7.4	16.25	31.93	7.97	16.25	28.82	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.41	7.47	17.92	2.57	7.47	16.34	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	7.7	18.18	40.09	8.33	18.18	35.14	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		15.76			15.76		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		12.56			12.56		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		30	80	190	30	80	180	ps/pF
Δt_{PHL}				110	230	430	120	230	390	
Δt_{PZH}	GZ	Y1		30	90	210	30	90	190	ps/pF
Δt_{PZL}				110	260	560	120	260	490	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.4	6.23	13.26	2.55	6.23	12.15	ns
t_{PHL}				2.59	6.28	13.23	2.78	6.28	11.99	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.54	6.92	15.85	2.7	6.92	14.33	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.62	6.56	14.47	2.82	6.56	12.96	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	4.69	12.04	25.31	5	12.04	23.24	ns
t_{PHL}				5.01	11.48	23.48	5.4	11.48	21.21	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.86	13.31	30.59	5.19	13.31	27.61	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.11	12.19	26.45	5.51	12.19	23.55	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		70	170	340	70	170	320	ps/pF
Δt_{PHL}				70	150	290	70	150	260	
Δt_{PZH}	GZ	Y1		70	180	420	70	180	380	ps/pF
Δt_{PZL}				70	160	340	80	160	300	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.41	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.32	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOI24LJ
2-mA 3-STATE I/O BUFFER WITH TTL INPUT AND CMOS/TTL OUTPUT

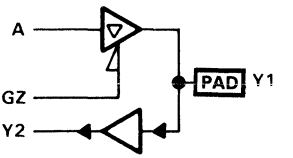
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOI24LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOI24LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −2 mA				3.7			V
			I_{OH} = −1.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 2 mA						0.5	V
			I_{OL} = 1.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.8			17.8		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.46	4.07	9.24	1.55	4.07	8.45	ns
t_{PHL}				3.57	8.3	16.84	3.84	8.3	15.24	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.47	4.43	10.47	1.56	4.43	9.54	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.68	9.1	20.27	3.98	9.1	17.89	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.41	6.98	15.99	2.56	6.98	14.66	ns
t_{PHL}				7.39	16.21	31.84	7.96	16.21	28.74	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.41	7.47	17.93	2.57	7.47	16.34	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	7.69	18.14	39.96	8.32	18.14	35.03	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		15.74			15.74		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		12.57			12.57		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		30	80	190	30	80	180	ps/pF
Δt_{PHL}				110	230	430	120	230	390	
Δt_{PZH}	GZ	Y1		30	90	210	30	90	190	ps/pF
Δt_{PZL}				110	260	560	120	260	490	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.41	6.25	13.3	2.57	6.25	12.19	ns
t_{PHL}				2.59	6.26	13.2	2.77	6.26	11.96	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.55	6.94	15.91	2.71	6.94	14.38	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.61	6.54	14.44	2.81	6.54	12.92	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	4.7	12.07	25.38	5.01	12.07	23.29	ns
t_{PHL}				5.01	11.46	23.45	5.39	11.46	21.18	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.87	13.34	30.66	5.2	13.34	27.68	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.11	12.17	26.41	5.51	12.17	23.51	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		70	170	350	70	170	320	ps/pF
Δt_{PHL}				70	150	290	70	150	260	
Δt_{PZH}	GZ	Y1		70	180	420	70	180	380	ps/pF
Δt_{PZL}				70	160	340	70	160	300	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOI41LJ
4-mA 3-STATE I/O BUFFER WITH CMOS INPUT AND CMOS/TTL OUTPUT

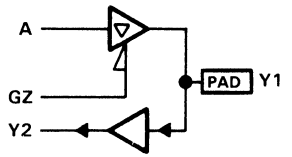
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOI41LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOI41LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −4 mA				3.7			V
			I_{OH} = −3.4 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 4 mA						0.5	V
			I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			11.3			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.6			17.6		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.06	2.88	6.47	1.12	2.88	5.91	ns
t_{PHL}				2.11	5.11	10.6	2.27	5.11	9.61	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.06	3.15	7.27	1.13	3.15	6.64	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.12	5.25	11.17	2.28	5.25	10.05	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.53	4.34	9.86	1.62	4.34	9.02	ns
t_{PHL}				4.02	9.06	18.11	4.32	9.06	16.37	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.54	4.65	10.82	1.64	4.65	9.89	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.08	9.46	19.6	4.39	9.46	17.54	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		11.65			11.65		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10.28			10.28		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	40	100	10	40	90	ps/pF
Δt_{PHL}				50	110	210	60	110	190	
Δt_{PZH}	GZ	Y1		10	40	100	10	40	90	ps/pF
Δt_{PZL}				60	120	240	60	120	210	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.51	3.98	8.54	1.6	3.98	7.82	ns
t_{PHL}				1.63	4.05	8.66	1.74	4.05	7.86	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.63	4.33	9.54	1.73	4.33	8.69	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.61	4.06	8.79	1.73	4.06	7.94	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.64	6.87	14.55	2.82	6.87	13.34	ns
t_{PHL}				2.85	6.67	13.86	3.05	6.67	12.54	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.79	7.37	16.12	2.97	7.37	14.69	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.85	6.79	14.36	3.06	6.79	12.92	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		30	80	170	30	80	160	ps/pF
Δt_{PHL}				30	80	150	40	80	130	
Δt_{PZH}	GZ	Y1		30	90	190	40	90	170	ps/pF
Δt_{PZL}				40	80	160	40	80	140	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOI44LJ
4-mA 3-STATE I/O BUFFER WITH TTL INPUT AND CMOS/TTL OUTPUT

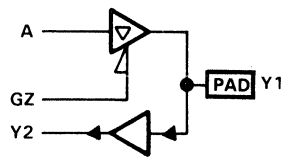
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOI44LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOI44LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −4 mA					3.7		V
			I_{OH} = −3.4 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 4 mA						0.5	V
			I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		18.3			18.3		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.06	2.88	6.47	1.12	2.88	5.91	ns
t_{PHL}				2.1	5.09	10.56	2.26	5.09	9.58	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.06	3.15	7.26	1.13	3.15	6.64	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.11	5.23	11.12	2.27	5.23	10.01	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.53	4.34	9.85	1.62	4.34	9.02	ns
t_{PHL}				4.01	9.04	18.07	4.32	9.04	16.34	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.54	4.65	10.82	1.64	4.65	9.89	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.07	9.44	19.55	4.39	9.44	17.49	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		11.65			11.65		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10.28			10.28		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	40	100	10	40	90	ps/pF
Δt_{PHL}				50	110	210	60	110	190	
Δt_{PZH}	GZ	Y1		10	40	100	10	40	90	ps/pF
Δt_{PZL}				60	120	240	60	120	210	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.51	3.99	8.55	1.61	3.99	7.83	ns
t_{PHL}				1.62	4.04	8.65	1.73	4.04	7.85	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.64	4.34	9.56	1.74	4.34	8.71	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.61	4.05	8.78	1.72	4.05	7.93	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.65	6.88	14.57	2.83	6.88	13.36	ns
t_{PHL}				2.84	6.67	13.84	3.05	6.67	12.53	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.79	7.38	16.15	2.97	7.38	14.71	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.85	6.79	14.34	3.06	6.79	12.91	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		30	80	170	30	80	160	ps/pF
Δt_{PHL}				30	80	150	40	80	130	
Δt_{PZH}	GZ	Y1		30	90	190	40	90	170	ps/pF
Δt_{PZL}				40	80	160	40	80	140	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOI61LJ
6-mA 3-STATE I/O BUFFER WITH CMOS INPUT AND CMOS/TTL OUTPUT

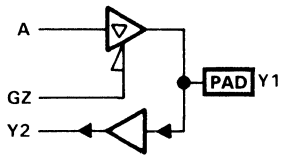
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOI61LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOI61LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −6 mA				3.7			V
			I_{OH} = −5.1 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 6 mA						0.5	V
			I_{OL} = 5.1 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.7			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		18.5			18.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.93	2.51	5.63	0.98	2.51	5.14	ns
t_{PHL}				1.62	4.01	8.43	1.73	4.01	7.65	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.93	2.77	6.36	0.99	2.77	5.81	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.61	4.02	8.53	1.72	4.02	7.72	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.25	3.5	7.94	1.32	3.5	7.26	ns
t_{PHL}				2.89	6.66	13.5	3.1	6.66	12.21	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.26	3.78	8.74	1.34	3.78	7.99	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.9	6.79	13.99	3.12	6.79	12.59	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		10.09			10.09		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.59			9.59		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	70	10	30	60	ps/pF
Δt_{PHL}				40	80	140	40	80	130	
Δt_{PZH}	GZ	Y1		10	30	70	10	30	60	ps/pF
Δt_{PZL}				40	80	160	40	80	140	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.22	3.27	7.07	1.3	3.27	6.47	ns
t_{PHL}				1.3	3.27	7.07	1.38	3.27	6.42	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.34	3.56	7.83	1.42	3.56	7.15	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.27	3.22	6.98	1.36	3.22	6.32	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.98	5.2	11.1	2.11	5.2	10.17	ns
t_{PHL}				2.12	5.05	10.62	2.27	5.05	9.62	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.11	5.56	12.1	2.24	5.56	11.05	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.11	5.06	10.7	2.26	5.06	9.66	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	60	120	20	60	110	ps/pF
Δt_{PHL}				20	50	100	30	50	90	
Δt_{PZH}	GZ	Y1		20	60	120	20	60	110	ps/pF
Δt_{PZL}				20	50	110	30	50	100	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOI64LJ
6-mA 3-STATE I/O BUFFER WITH TTL INPUT AND CMOS/TTL OUTPUT

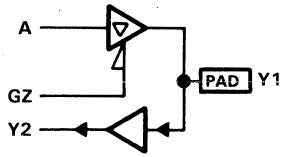
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOI64LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOI64LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −6 mA				3.7			V
			I_{OH} = −5.1 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 6 mA						0.5	V
			I_{OL} = 5.1 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		19.1			19.1		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	0.93	2.51	5.63	0.98	2.51	5.14	ns
t_{PHL}				1.61	4	8.41	1.72	4	7.64	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	0.93	2.77	6.36	0.99	2.77	5.81	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.6	4.01	8.51	1.71	4.01	7.7	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.25	3.5	7.93	1.32	3.5	7.26	ns
t_{PHL}				2.88	6.65	13.46	3.1	6.65	12.19	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.26	3.78	8.74	1.34	3.78	7.99	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.9	6.78	13.95	3.11	6.78	12.56	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		10.09			10.09		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.59			9.59		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	70	10	30	60	ps/pF
Δt_{PHL}				40	80	140	40	80	130	
Δt_{PZH}	GZ	Y1		10	30	70	10	30	60	ps/pF
Δt_{PZL}				40	80	160	40	80	140	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.23	3.27	7.08	1.3	3.27	6.47	ns
t_{PHL}				1.3	3.26	7.06	1.38	3.26	6.42	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.34	3.57	7.84	1.42	3.57	7.15	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.27	3.22	6.97	1.35	3.22	6.32	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.98	5.21	11.11	2.11	5.21	10.18	ns
t_{PHL}				2.12	5.05	10.61	2.26	5.05	9.61	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.11	5.57	12.12	2.25	5.57	11.06	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.11	5.06	10.69	2.26	5.06	9.66	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	60	120	20	60	110	ps/pF
Δt_{PHL}				20	50	100	30	50	90	
Δt_{PZH}	GZ	Y1		20	60	120	20	60	110	ps/pF
Δt_{PZL}				20	50	110	30	50	100	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJA1LJ
16-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

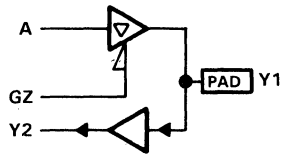
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOJA1LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJA1LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 16 mA						0.5	V
			I_{OL} = 13.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.6			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		20.8			20.8		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.29	3.64	8.29	1.36	3.64	7.56	ns
t_{PHL}				1.73	4.54	9.83	1.86	4.54	8.95	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.32	3.92	9.05	1.4	3.92	8.26	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.74	4.54	9.79	1.86	4.54	8.91	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.54	4.32	9.81	1.64	4.32	8.94	ns
t_{PHL}				2.37	5.92	12.52	2.55	5.92	11.38	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.57	4.6	10.57	1.68	4.6	9.64	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.38	5.93	12.5	2.55	5.93	11.35	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.3			9.3		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.34			9.34		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	40	10	20	40	ps/pF
Δt_{PHL}				20	40	80	20	40	70	
Δt_{PZH}	GZ	Y1		10	20	40	10	20	40	ps/pF
Δt_{PZL}				20	40	80	20	40	70	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJA1LJ
16-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.52	4.21	9.34	1.62	4.21	8.53	ns
t_{PHL}				1.52	4.04	8.92	1.62	4.04	8.12	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.67	4.51	10.06	1.78	4.51	9.16	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.52	4.01	8.8	1.62	4.01	8.01	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.94	5.24	11.5	2.07	5.24	10.49	ns
t_{PHL}				2	5.1	11.04	2.14	5.1	10.03	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.09	5.54	12.23	2.22	5.54	11.13	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2	5.08	10.93	2.14	5.08	9.94	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	60	10	30	60	ps/pF
Δt_{PHL}				10	30	60	10	30	50	
Δt_{PZH}	GZ	Y1		10	30	50	10	30	60	ps/pF
Δt_{PZL}				10	30	40	10	30	50	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJA4LJ
16-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

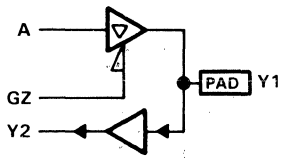
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOJA4LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJA4LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −16 mA					3.7		V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 16 mA						0.5	V
			I_{OL} = 13.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		22.5			22.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IOJA4LJ
16-mA 3-STATE I/O BUFFER
WITH 0.5 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.29	3.64	8.29	1.36	3.64	7.56	ns
t_{PHL}				1.73	4.53	9.83	1.85	4.53	8.94	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.32	3.92	9.05	1.41	3.92	8.26	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.73	4.53	9.77	1.86	4.53	8.89	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.54	4.32	9.8	1.64	4.32	8.94	ns
t_{PHL}				2.37	5.91	12.52	2.54	5.91	11.38	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.57	4.6	10.57	1.68	4.6	9.64	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.37	5.92	12.49	2.55	5.92	11.34	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.3			9.3		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.19			9.19		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	40	10	20	40	ps/pF
Δt_{PHL}				20	40	80	20	40	70	
Δt_{PZH}	GZ	Y1		10	20	40	10	20	40	ps/pF
Δt_{PZL}				20	40	80	20	40	70	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.52	4.21	9.34	1.62	4.21	8.53	ns
t_{PHL}				1.51	4.03	8.92	1.62	4.03	8.11	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.67	4.51	10.06	1.78	4.51	9.16	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.51	4.01	8.8	1.62	4.01	8.01	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.94	5.24	11.5	2.07	5.24	10.49	ns
t_{PHL}				1.99	5.09	11.04	2.14	5.09	10.03	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.09	5.54	12.23	2.23	5.54	11.15	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.99	5.07	10.93	2.14	5.07	9.93	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	60	10	30	60	ps/pF
Δt_{PHL}				10	30	60	20	30	50	
Δt_{PZH}	GZ	Y1		10	30	60	10	30	60	ps/pF
Δt_{PZL}				10	30	60	20	30	50	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJB1LJ
24-mA 3-STATE I/O BUFFER
WITH 0.5 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

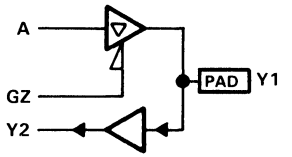
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOJB1LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJB1LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 24 mA						0.5	V
			I_{OL} = 20.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.6			0.49	mA
C_i	Input capacitance	Y1			13.9			13.9		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		22.5			22.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.29	3.65	8.31	1.37	3.65	7.58	ns
t_{PHL}				1.88	4.91	10.63	2.01	4.91	9.69	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.32	3.94	9.09	1.41	3.94	8.29	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.9	4.96	10.66	2.04	4.96	9.72	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.54	4.33	9.83	1.64	4.33	8.96	ns
t_{PHL}				2.43	6.11	12.95	2.61	6.11	11.79	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.58	4.62	10.62	1.69	4.62	9.68	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.46	6.15	12.98	2.64	6.15	11.81	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.31			9.31		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.27			8.27		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	40	10	20	40	ps/pF
Δt_{PHL}				20	30	70	20	30	60	
Δt_{PZH}	GZ	Y1		10	20	40	10	20	40	ps/pF
Δt_{PZL}				20	30	70	20	30	60	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJB1LJ
24-mA 3-STATE I/O BUFFER
WITH 0.5 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.52	4.21	9.36	1.62	4.21	8.55	ns
t_{PHL}				1.67	4.44	9.78	1.79	4.44	8.91	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.68	4.52	10.1	1.78	4.52	9.2	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.69	4.47	9.74	1.81	4.47	8.88	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.94	5.25	11.52	2.07	5.25	10.51	ns
t_{PHL}				2.1	5.39	11.67	2.25	5.39	10.62	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.09	5.56	12.27	2.23	5.56	11.17	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.12	5.41	11.63	2.27	5.41	10.59	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	60	10	30	60	ps/pF
Δt_{PHL}				10	30	50	10	30	50	
Δt_{PZH}	GZ	Y1		10	30	60	10	30	60	ps/pF
Δt_{PZL}				10	30	50	10	30	50	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJB4LJ
24-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

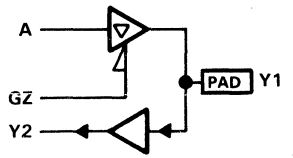
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOJB4LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJB4LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 24 mA						0.5	V
			I_{OL} = 20.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
ICC	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.49	mA
C_i	Input capacitance	Y1			13.9			13.9		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		24.7			24.7		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IOJB4LJ
24-mA 3-STATE I/O BUFFER
WITH 0.5 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.29	3.65	8.31	1.37	3.65	7.58	ns
t_{PHL}				1.88	4.91	10.62	2.01	4.91	9.68	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.32	3.94	9.09	1.41	3.94	8.29	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.9	4.96	10.64	2.04	4.96	9.7	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.54	4.33	9.83	1.64	4.33	8.96	ns
t_{PHL}				2.43	6.1	12.94	2.61	6.1	11.78	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.58	4.62	10.61	1.68	4.62	9.68	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.46	6.15	12.97	2.64	6.15	11.8	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.31			9.31		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.27			8.27		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	40	10	20	40	ps/pF
Δt_{PHL}				20	30	70	20	30	60	
Δt_{PZH}	GZ	Y1		10	20	40	10	20	40	ps/pF
Δt_{PZL}				20	30	70	20	30	60	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.52	4.22	9.36	1.62	4.22	8.55	ns
t_{PHL}				1.67	4.44	9.77	1.78	4.44	8.9	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.68	4.53	10.1	1.78	4.53	9.2	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.69	4.46	9.73	1.81	4.46	8.87	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.94	5.25	11.52	2.07	5.25	10.51	ns
t_{PHL}				2.1	5.39	11.66	2.25	5.39	10.61	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.1	5.56	12.27	2.23	5.56	11.17	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.12	5.41	11.63	2.27	5.41	10.58	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	60	10	30	60	ps/pF
Δt_{PHL}				10	30	50	10	30	50	
Δt_{PZH}	GZ	Y1		10	30	60	10	30	60	ps/pF
Δt_{PZL}				10	30	50	10	30	50	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJEPLJ
48-mA OPEN-DRAIN I/O BUFFER WITH 0.5 di/dt, TTL INPUT WITH HYSTERESIS, AND CMOS/TTL OUTPUT

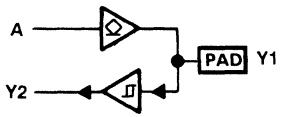
D3030, DECEMBER 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUTS	
A	Y1	Y1	Y2
L	L	L	L
H	H	H‡	H
H	L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A‡ Y2 = Y1

description

The IOJEPLJ is a noninverting open-drain input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip terminated bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus when the internal A node is at a high logic level. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJEPLJ A,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C MIN	TYP§	MAX	0°C to 70°C MIN	TYP§	MAX	UNIT
V_T	Input threshold voltage at A				2.2			2.2		V
V_{T+}	Positive-going threshold level at Y1				1.6			1.6		V
V_{T-}	Negative-going threshold level at Y1				1.2			1.2		V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$) at Y1				0.4			0.4		V
V_{OL}	Low-level output voltage		I_{OL} = 48 mA						0.5	V
			I_{OL} = 40.8 mA		0.5					
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0		±10			±5		μA
I_{CC}	Supply current		$V_I = V_{IH}$ or V_{IL}		3.84			1		mA
C_i	Input capacitance	A			0.59			0.59		pF
		Y1			11.2			11.2		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		9.52			9.52		pF

‡ With external pull-up resistor to Y2.

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y1	C_L = 15 pF	1.11	3.24	7.23	1.2	3.24	6.58	ns
			C_L = 50 pF	1.47	4.03	8.79	1.58	4.03	7.99	
t_{PLZ}	A	Y1			7.39			7.39		ns
Δt_{PZL}	A	Y1		10	20	40	10	20	40	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y1	C_L = 15 pF	0.99	2.91	6.61	1.06	2.91	6.01	ns
			C_L = 50 pF	1.27	3.55	7.91	1.36	3.55	7.19	
Δt_{PZL}	A	Y1		10	20	40	10	30	40	ps/pF

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2	C_L = 0	0.74	1.29	1.96	0.77	1.29	1.89	ns
t_{PHL}				0.21	1.79	5.09	0.22	1.79	4.83	
Δt_{PLH}	Y1	Y2		0.1	0.17	0.35	0.1	0.17	0.31	ns/pF
Δt_{PHL}				0.03	0.25	0.62	0.04	0.25	0.58	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJE1LJ
48-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

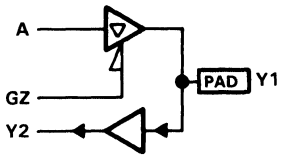
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOJE1LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJE1LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 48 mA						0.5	V
			I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.6			0.49	mA
C_i	Input capacitance	Y1			15.4			15.4		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		27.9			27.9		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.31	3.71	8.45	1.39	3.71	7.71	ns
t_{PHL}				1.71	4.59	10.15	1.82	4.59	9.24	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.34	3.99	9.21	1.43	3.99	8.41	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.73	4.64	10.15	1.85	4.64	9.25	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.56	4.38	9.95	1.66	4.38	9.07	ns
t_{PHL}				2.2	5.37	11.68	2.2	5.37	10.62	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.59	4.67	10.72	1.7	4.67	9.77	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.08	5.42	11.67	2.23	5.42	10.63	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.43			9.43		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.22			9.22		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	40	10	20	40	ps/pF
Δt_{PHL}				10	20	40	10	20	40	
Δt_{PZH}	GZ	Y1		10	20	40	10	20	40	ps/pF
Δt_{PZL}				10	20	40	10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.54	4.28	9.52	1.65	4.28	8.69	ns
t_{PHL}				1.56	4.24	9.5	1.66	4.24	8.65	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.7	4.59	10.24	1.81	4.59	9.33	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.59	4.27	9.46	1.69	4.27	8.62	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.96	5.3	11.66	2.1	5.3	10.63	ns
t_{PHL}				1.84	4.87	10.78	1.96	4.87	9.8	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.11	5.61	12.39	2.25	5.61	11.28	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.87	4.91	10.74	1.99	4.91	9.78	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	60	10	30	60	ps/pF
Δt_{PHL}				10	20	40	10	20	30	
Δt_{PZH}	GZ	Y1		10	30	60	10	20	60	ps/pF
Δt_{PZL}				10	20	40	10	20	30	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJE4LJ
48-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

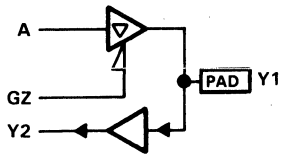
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOJE4LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJE4LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 48 mA						0.5	V
			I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}		3.45			0.3		mA
C_i	Input capacitance	Y1			15.4			15.4		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		29.9			29.9		pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJE4LJ
48-mA 3-STATE I/O BUFFER
WITH 0.5 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, ARPIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.31	3.71	8.45	1.39	3.71	7.71	ns
t_{PHL}				1.71	4.59	10.15	1.82	4.59	9.24	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.34	3.99	9.21	1.43	3.99	8.4	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.74	4.64	10.14	1.86	4.64	9.24	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.56	4.38	9.95	1.66	4.38	9.07	ns
t_{PHL}				2.06	5.37	11.68	2.2	5.37	10.62	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.59	4.67	10.72	1.7	4.67	9.77	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.09	5.42	11.67	2.24	5.42	10.62	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.43			9.43		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.22			9.22		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	40	10	20	40	ps/pF
Δt_{PHL}				10	20	40	10	20	40	
Δt_{PZH}	GZ	Y1		10	20	40	10	20	40	ps/pF
Δt_{PZL}				10	40	40	10	20	40	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.55	4.28	9.52	1.65	4.28	8.69	ns
t_{PHL}				1.56	4.23	9.5	1.66	4.23	8.64	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.7	4.59	10.24	1.81	4.59	9.33	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.58	4.27	9.41	1.69	4.27	8.61	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.96	5.31	11.66	2.1	5.31	10.63	ns
t_{PHL}				1.84	4.87	10.78	1.96	4.87	9.8	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.11	5.62	12.39	2.25	5.62	11.28	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.87	4.91	10.74	1.99	4.91	9.77	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	60	10	30	60	ps/pF
Δt_{PHL}				10	20	40	10	20	30	
Δt_{PZH}	GZ	Y1		10	30	60	10	30	60	ps/pF
Δt_{PZL}				10	20	40	10	20	30	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJG1LJ
64-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

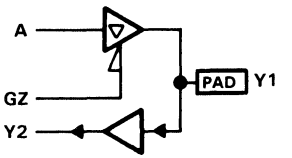
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOJG1LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJG1LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 64 mA						0.5	V
			I_{OL} = 54.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.1			0.49	mA
C_i	Input capacitance	Y1			16.6			16.6		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		31			31		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.34	3.77	8.58	1.42	3.77	7.82	ns
t_{PHL}				1.58	4.43	10.06	1.68	4.43	9.17	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.35	4.03	9.3	1.44	4.03	8.48	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.7	4.56	10.06	1.81	4.56	9.16	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.58	4.43	10.06	1.68	4.43	9.17	ns
t_{PHL}				1.95	5.17	11.38	2.08	5.17	10.34	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.6	4.69	10.78	1.71	4.69	9.83	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.98	5.21	11.35	2.12	5.21	10.33	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.52			9.52		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.7			9.7		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	40	10	20	40	ps/pF
Δt_{PHL}				10	20	40	10	20	30	
Δt_{PZH}	GZ	Y1		10	20	40	10	20	40	ps/pF
Δt_{PZL}				10	20	40	10	20	30	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJG1LJ
64-mA 3-STATE I/O BUFFER
WITH 0.5 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.57	4.35	9.66	1.68	4.35	8.81	ns
t_{PHL}				1.53	4.21	9.51	1.64	4.21	8.64	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.71	4.63	10.34	1.82	4.63	9.41	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.56	4.23	9.45	1.66	4.23	8.6	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.99	5.36	11.77	2.12	5.36	10.73	ns
t_{PHL}				1.76	4.74	10.59	1.88	4.74	9.62	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.12	5.65	12.47	2.27	5.65	11.35	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.79	4.77	10.53	1.91	4.77	9.58	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	60	10	30	50	ps/pF
Δt_{PHL}				10	20	30	10	20	30	
Δt_{PZH}	GZ	Y1		10	30	60	10	30	60	ps/pF
Δt_{PZL}				10	20	30	10	20	30	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJG4LJ
64-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

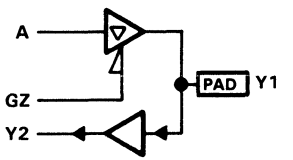
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOJG4LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJG4LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −16 mA					3.7		V
			I_{OH} = −13.6 mA		3.7					
V_{OL}	Low-level output voltage		I_{OL} = 64 mA						0.5	V
			I_{OL} = 54.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			16.6			16.6		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		32.5			32.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IOJG4LJ
64-mA 3-STATE I/O BUFFER
WITH 0.5 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.3	3.77	8.58	1.39	3.77	7.82	ns
t_{PHL}				1.66	4.53	10.08	1.78	4.53	9.17	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.35	4.03	9.29	1.44	4.03	8.48	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.7	4.56	10.06	1.81	4.56	9.16	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.54	4.43	10.06	1.65	4.43	9.16	ns
t_{PHL}				1.94	5.17	11.37	2.08	5.17	10.34	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.6	4.7	10.78	1.71	4.7	9.83	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.97	5.21	11.34	2.11	5.21	10.32	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.51			9.51		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.7			9.7		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	40	10	20	40	ps/pF
Δt_{PHL}				10	20	40	10	20	30	
Δt_{PZH}	GZ	Y1		10	20	40	10	20	40	ps/pF
Δt_{PZL}				10	20	40	10	20	30	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.54	4.35	9.66	1.65	4.35	8.81	ns
t_{PHL}				1.54	4.2	9.49	1.64	4.2	8.63	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.72	4.64	10.34	1.83	4.64	9.41	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.56	4.23	9.44	1.66	4.23	8.59	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.95	5.36	11.77	2.1	5.36	10.74	ns
t_{PHL}				1.76	4.74	10.59	1.88	4.74	9.62	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.13	5.65	12.47	2.27	5.65	11.35	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.79	4.77	10.53	1.91	4.77	9.58	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	60	10	30	60	ps/pF
Δt_{PHL}				10	20	30	10	20	30	
Δt_{PZH}	GZ	Y1		10	30	60	10	30	60	ps/pF
Δt_{PZL}				10	20	30	10	20	30	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJ01LJ
10-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

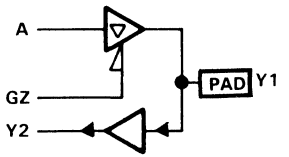
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOJ01LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJ01LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −10 mA				3.7			V
			I_{OH} = −8.5 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 10 mA						0.5	V
			I_{OL} = 8.5 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.7			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		18.7			18.7		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.34	3.75	8.51	1.42	3.75	7.75	ns
t_{PHL}				2.08	5.3	11.27	2.23	5.3	10.27	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.37	4.04	9.3	1.46	4.04	8.47	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.09	5.33	11.34	2.24	5.33	10.31	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.66	4.63	10.5	1.77	4.63	9.57	ns
t_{PHL}				3	7.26	15.07	3.23	7.26	13.69	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.7	4.93	11.31	1.81	4.93	10.3	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.02	7.31	15.23	3.24	7.31	13.8	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.77			9.77		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.62			8.62		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	60	10	30	50	ps/pF
Δt_{PHL}				30	60	110	30	60	100	
Δt_{PZH}	GZ	Y1		10	30	60	10	30	50	ps/pF
Δt_{PZL}				30	60	110	30	60	100	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJ01LJ
10-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.64	4.47	9.89	1.75	4.47	8.97	ns
t_{PHL}				1.78	4.63	10.07	1.91	4.63	9.17	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.79	4.78	10.62	1.91	4.78	9.66	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.78	4.62	10.01	1.91	4.62	9.1	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.22	5.88	12.81	2.37	5.88	11.68	ns
t_{PHL}				2.45	6.09	12.98	2.63	6.09	11.8	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.37	6.21	13.64	2.53	6.21	12.41	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.45	6.1	12.96	2.63	6.1	11.77	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	80	20	40	80	ps/pF
Δt_{PHL}				20	40	80	20	40	80	
Δt_{PZH}	GZ	Y1		20	40	90	20	40	80	ps/pF
Δt_{PZL}				20	40	80	20	40	80	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.41	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.32	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJ04LJ
10-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

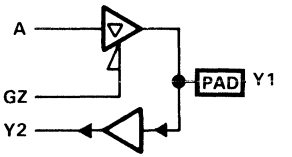
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOJ04LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJ04LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −10 mA				3.7			V
			I_{OH} = −8.5 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 10 mA						0.5	V
			I_{OL} = 8.5 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		19.9			19.9		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IOJ04LJ
10-mA 3-STATE I/O BUFFER
WITH 0.5 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.34	3.75	8.51	1.42	3.75	7.75	ns
t_{PHL}				2.08	5.29	11.25	2.23	5.29	10.25	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.37	4.03	9.29	1.46	4.03	8.47	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.09	5.32	11.32	2.24	5.32	10.29	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.66	4.63	10.5	1.77	4.63	9.56	ns
t_{PHL}				3	7.25	15.05	3.22	7.25	13.67	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.7	4.92	11.31	1.81	4.92	10.3	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.01	7.31	15.21	3.23	7.31	13.79	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.77			9.77		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.62			8.62		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
Δt_{PLH}	A	Y1		10	30	60	10	30	60	ps/pF
Δt_{PHL}				30	60	110	30	60	100	
Δt_{PZH}	GZ	Y1		10	30	60	10	30	50	ps/pF
Δt_{PZL}				30	60	110	30	60	100	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.65	4.47	9.84	1.75	4.47	8.97	ns
t_{PHL}				1.78	4.62	10.06	1.91	4.62	9.16	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.79	4.78	10.62	1.91	4.78	9.66	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.78	4.62	10	1.9	4.62	9.1	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.22	5.89	12.82	2.37	5.89	11.68	ns
t_{PHL}				2.45	6.09	12.97	2.63	6.09	11.79	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.37	6.22	13.65	2.53	6.22	12.42	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.45	6.09	12.96	2.63	6.09	11.76	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	90	20	40	80	ps/pF
Δt_{PHL}				20	40	80	20	40	80	
Δt_{PZH}	GZ	Y1		20	40	90	20	40	80	ps/pF
Δt_{PZL}				20	40	80	20	40	80	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJ21LJ
2-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

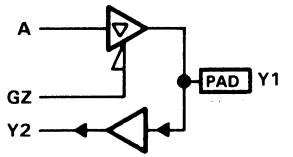
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOJ21LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJ21LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −2 mA				3.7			V
			I_{OH} = −1.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 2 mA						0.5	V
			I_{OL} = 1.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.7			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.2			17.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.34	6.41	14.51	2.5	6.41	13.22	ns
t_{PHL}				5.45	12.61	25.62	5.85	12.61	23.28	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.4	6.83	16.02	2.56	6.83	14.53	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.61	13.68	30.09	6.05	13.68	26.77	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.4	9.48	21.57	3.63	9.48	19.69	ns
t_{PHL}				9.34	20.73	41.1	10.06	20.73	37.22	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.44	10.02	23.66	3.68	10.02	21.49	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	9.66	22.79	49.74	10.44	22.79	43.94	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		15.58			15.58		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		12.31			12.31		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		30	90	200	30	90	180	ps/pF
Δt_{PHL}				110	230	440	120	230	400	
Δt_{PZH}	GZ	Y1		30	90	220	30	90	200	ps/pF
Δt_{PZL}				120	260	560	130	260	490	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.4	8.75	18.83	3.64	8.75	17.18	ns
t_{PHL}				4.31	10.29	21.5	4.62	10.29	19.55	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.59	9.54	21.79	3.83	9.54	19.65	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.38	10.76	23.46	4.7	10.76	21.11	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	5.73	14.63	31.03	6.13	14.63	28.38	ns
t_{PHL}				6.9	15.86	32.47	7.42	15.86	29.44	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	5.94	15.96	36.5	6.35	15.96	32.91	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	7.03	16.67	35.84	7.56	16.67	32.11	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		70	170	350	70	170	320	ps/pF
Δt_{PHL}				70	160	310	80	160	280	
Δt_{PZH}	GZ	Y1		70	180	420	70	180	380	ps/pF
Δt_{PZL}				80	170	350	80	170	310	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.41	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.32	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJ24LJ
2-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

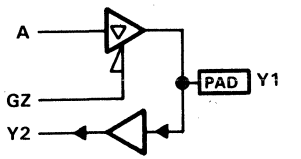
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOJ24LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJ24LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −2 mA				3.7			V
			I_{OH} = −1.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 2 mA						0.5	V
			I_{OL} = 1.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.7			17.7		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IOJ24LJ
2-mA 3-STATE I/O BUFFER
WITH 0.5 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.35	6.41	14.52	2.5	6.41	13.22	ns
t_{PHL}				5.43	12.57	25.52	5.84	12.57	23.19	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.4	6.84	16.02	2.56	6.84	14.53	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.59	13.63	29.94	6.03	13.63	26.65	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	3.4	9.49	21.58	3.64	9.49	19.69	ns
t_{PHL}				9.33	20.7	40.99	10.04	20.7	37.14	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.44	10.02	23.67	3.68	10.02	21.49	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	9.65	22.75	49.59	10.43	22.75	43.82	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		15.56			15.56		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		12.33			12.33		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
Δt_{PLH}	A	Y1		30	90	200	30	90	180	ps/pF
Δt_{PHL}				110	230	440	120	230	400	
Δt_{PZH}	GZ	Y1		30	90	220	30	90	200	ps/pF
Δt_{PZL}				120	260	560	130	260	490	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.41	8.78	18.87	3.65	8.78	17.22	ns
t_{PHL}				4.3	10.28	21.45	4.61	10.28	19.52	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.6	9.57	21.85	3.85	9.57	19.7	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.37	10.74	23.4	4.69	10.74	21.07	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	5.74	14.65	31.09	6.14	14.65	28.43	ns
t_{PHL}				6.9	15.85	32.42	7.41	15.85	29.41	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	5.95	15.98	36.56	6.36	15.98	32.97	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	7.02	16.66	35.78	7.55	16.66	32.07	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		70	170	350	70	170	320	ps/pF
Δt_{PHL}				70	160	310	80	160	280	
Δt_{PZH}	GZ	Y1		70	180	420	70	180	380	ps/pF
Δt_{PZL}				80	170	350	80	170	310	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJ41LJ
4-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

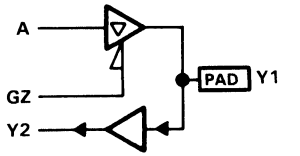
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOJ41LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJ41LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −4 mA				3.7			V
			I_{OH} = −3.4 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 4 mA						0.5	V
			I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			11.3			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.5			17.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.72	4.74	10.71	1.84	4.74	9.75	ns
t_{PHL}				3.35	8.05	16.62	3.6	8.05	15.12	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.77	5.06	11.68	1.89	5.06	10.62	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.39	8.3	17.6	3.65	8.3	15.89	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.33	6.44	14.58	2.49	6.44	13.29	ns
t_{PHL}				5.37	12.28	24.7	5.78	12.28	22.4	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.38	6.79	15.67	2.54	6.79	14.25	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.44	12.74	26.44	5.87	12.74	23.76	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		11.49			11.49		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10.02			10.02		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	50	110	20	50	100	ps/pF
Δt_{PHL}				60	120	230	60	120	210	
Δt_{PZH}	GZ	Y1		20	50	110	20	50	100	ps/pF
Δt_{PZL}				60	130	250	60	130	220	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJ41LJ
4-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.31	6.07	13.16	2.47	6.07	11.99	ns
t_{PHL}				2.74	6.76	14.33	2.94	6.76	13.03	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.48	6.49	14.41	2.65	6.49	13.06	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.75	6.86	14.75	2.95	6.86	13.36	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.53	9.11	19.48	3.77	9.11	17.79	ns
t_{PHL}				4.13	9.75	20.22	4.43	9.75	18.35	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.7	9.65	21.22	3.96	9.65	19.26	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.15	9.92	20.92	4.46	9.92	18.9	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		30	90	180	40	90	170	ps/pF
Δt_{PHL}				40	90	170	40	90	150	
Δt_{PZH}	GZ	Y1		30	90	190	40	90	180	ps/pF
Δt_{PZL}				40	90	180	40	90	160	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.58	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ps/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJ44LJ
4-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

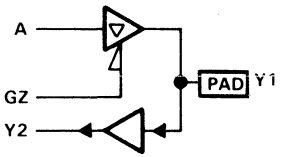
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOJ44LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJ44LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −4 mA				3.7			V
			I_{OH} = −3.4 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 4 mA						0.5	V
			I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.8			17.8		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IOJ44LJ
4-mA 3-STATE I/O BUFFER
WITH 0.5 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.72	4.73	10.71	1.84	4.73	9.75	ns
t_{PHL}				3.34	8.02	16.57	3.59	8.02	15.07	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.77	5.06	11.68	1.89	5.06	10.61	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.38	8.28	17.53	3.64	8.28	15.83	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.33	6.44	14.58	2.49	6.44	13.29	ns
t_{PHL}				5.37	12.26	24.65	5.77	12.26	22.36	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.38	6.79	15.67	2.54	6.79	14.25	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.44	12.72	26.38	5.86	12.72	23.71	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		11.49			11.49		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10.02			10.02		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	50	110	20	50	100	ps/pF
Δt_{PHL}				60	120	230	60	120	210	
Δt_{PZH}	GZ	Y1		20	50	110	20	50	100	ps/pF
Δt_{PZL}				60	130	250	60	130	230	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.32	6.07	13.18	2.48	6.07	12.01	ns
t_{PHL}				2.74	6.75	14.3	2.93	6.75	13.02	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.49	6.5	14.43	2.66	6.5	13.08	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.75	6.85	14.72	2.95	6.85	13.33	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.53	9.12	19.5	3.78	9.12	17.81	ns
t_{PHL}				4.12	9.74	20.2	4.43	9.74	18.33	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.71	9.66	21.24	3.96	9.66	19.28	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.15	9.92	20.9	4.46	9.92	18.88	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		30	90	180	40	90	170	ps/pF
Δt_{PHL}				40	90	170	40	90	150	
Δt_{PZH}	GZ	Y1		30	90	190	40	90	180	ps/pF
Δt_{PZL}				40	90	180	40	90	160	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJ61LJ
6-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

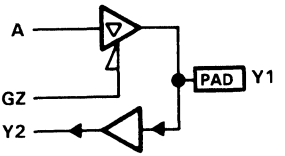
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOJ61LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJ61LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −6 mA				3.7			V
			I_{OH} = −5.1 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 6 mA						0.5	V
			I_{OL} = 5.1 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.7			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		18.5			18.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and cperating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.52	4.2	9.52	1.62	4.2	8.67	ns
t_{PHL}				2.66	6.55	13.7	2.85	6.55	12.46	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.57	4.51	10.38	1.67	4.51	9.44	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.68	6.65	14.09	2.88	6.65	12.76	

C_L = 50 pF

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.98	5.47	12.37	2.11	5.47	11.27	ns
t_{PHL}				4.07	9.52	19.4	4.37	9.52	17.6	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.02	5.78	13.27	2.16	5.78	12.08	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.1	9.7	20.07	4.41	9.7	18.13	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.94			9.94		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.34			9.34		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	40	80	10	40	70	ps/pF
Δt_{PHL}				40	80	160	40	80	150	
Δt_{PZH}	GZ	Y1		10	40	80	10	40	80	ps/pF
Δt_{PZL}				40	90	170	40	90	150	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJ61LJ
6-mA 3-STATE I/O BUFFER
WITH 0.5 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.96	5.21	11.37	2.09	5.21	10.36	ns
t_{PHL}				2.22	5.6	12	2.38	5.6	10.92	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.13	5.56	12.31	2.27	5.56	11.18	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.22	5.63	12.12	2.38	5.63	11	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.82	7.34	15.83	3.01	7.34	14.43	ns
t_{PHL}				3.21	7.75	16.25	3.45	7.75	14.76	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.99	7.75	16.96	3.19	7.75	15.41	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.22	7.81	16.48	3.45	7.81	14.92	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	60	130	30	60	120	ps/pF
Δt_{PHL}				30	60	120	30	60	110	
Δt_{PZH}	GZ	Y1		20	60	130	30	60	120	ps/pF
Δt_{PZL}				30	60	120	30	60	110	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOJ64LJ
6-mA 3-STATE I/O BUFFER WITH 0.5 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

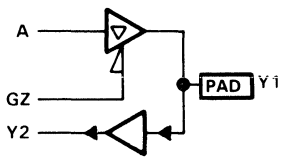
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOJ64LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOJ64LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −6 mA				3.7			V
			I_{OH} = −5.1 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 6 mA						0.5	V
			I_{OL} = 5.1 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		18.5			18.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.52	4.2	9.52	1.62	4.2	8.67	ns
t_{PHL}				2.65	6.53	13.67	2.85	6.53	12.44	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.57	4.51	10.38	1.67	4.51	9.44	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.67	6.64	14.05	2.87	6.64	12.73	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.98	5.46	12.37	2.11	5.46	11.26	ns
t_{PHL}				4.06	9.5	19.36	4.37	9.5	17.57	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.02	5.78	13.27	2.16	5.78	12.07	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.1	9.69	20.04	4.41	9.69	18.1	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.94			9.94		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.34			9.34		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	40	80	10	40	70	ps/pF
Δt_{PHL}				40	80	160	40	80	150	
Δt_{PZH}	GZ	Y1		10	40	80	10	40	80	ps/pF
Δt_{PZL}				40	90	170	40	90	150	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.96	5.21	11.38	2.1	5.21	10.36	ns
t_{PHL}				2.22	5.59	11.99	2.37	5.59	10.91	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.13	5.57	12.33	2.27	5.57	11.19	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.22	5.62	12.11	2.38	5.62	10.99	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.82	7.35	15.84	3.02	7.35	14.44	ns
t_{PHL}				3.21	7.74	16.23	3.44	7.74	14.75	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.99	7.75	16.97	3.19	7.75	15.42	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.22	7.8	16.47	3.45	7.8	14.91	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	60	130	30	60	120	ps/pF
Δt_{PHL}				30	60	120	30	60	110	
Δt_{PZH}	GZ	Y1		20	60	130	30	60	120	ps/pF
Δt_{PZL}				30	60	120	30	60	110	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOKA1LJ 16-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

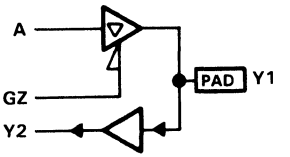
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOKA1LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOKA1LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 16 mA						0.5	V
			I_{OL} = 13.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.6			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		20.8			20.8		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.69	4.79	10.96	1.79	4.79	9.99	ns
t_{PHL}				2.46	6.29	13.53	2.64	6.29	12.33	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.74	5.09	11.79	1.85	5.09	10.74	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.47	6.32	13.6	2.65	6.32	12.37	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.02	5.68	12.96	2.15	5.68	11.79	ns
t_{PHL}				13.26	8.01	16.88	3.49	8.01	15.35	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.07	5.98	13.78	2.21	5.98	12.54	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.26	8.04	16.96	3.5	8.04	15.4	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.28			9.28		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.32			9.32		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	60	10	30	50	ps/pF
Δt_{PHL}				20	50	100	20	50	90	
Δt_{PZH}	GZ	Y1		10	30	60	10	30	50	ps/pF
Δt_{PZL}				20	50	100	20	50	90	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.02	5.56	12.37	2.16	5.56	11.27	ns
t_{PHL}				2.16	5.63	12.34	2.31	5.63	11.24	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.19	5.88	13.2	2.33	5.88	12	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.16	5.62	12.29	2.31	5.62	11.18	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.55	6.86	15.14	2.73	6.86	15.1	ns
t_{PHL}				2.77	6.98	15.05	2.96	6.98	13.69	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.72	7.18	15.92	2.9	7.18	14.47	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.77	6.97	15	2.96	6.97	13.63	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	80	20	40	70	ps/pF
Δt_{PHL}				20	40	80	20	40	70	
Δt_{PZH}	GZ	Y1		20	40	80	20	40	70	ps/pF
Δt_{PZL}				20	40	80	20	40	70	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOKA4LJ
16-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

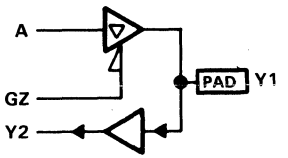
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOKA4LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOKA4LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 16 mA						0.5	V
			I_{OL} = 13.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		22.5			22.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.68	4.8	10.96	1.79	4.8	9.99	ns
t_{PHL}				2.45	6.29	13.51	2.63	6.29	12.31	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.74	5.09	11.79	1.86	5.09	10.73	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.46	6.31	13.58	2.64	6.31	12.35	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.02	5.68	12.95	2.15	5.68	11.79	ns
t_{PHL}				3.25	8	16.86	3.49	8	15.34	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.07	5.98	13.78	2.21	5.98	12.54	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.26	8.03	16.94	3.5	8.03	15.39	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.3			9.3		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.18			9.18		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	60	10	30	50	ps/pF
Δt_{PHL}				20	50	100	30	50	90	
Δt_{PZH}	GZ	Y1		10	30	60	10	30	50	ps/pF
Δt_{PZL}				20	50	100	30	50	90	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.02	5.57	12.38	2.16	5.57	11.28	ns
t_{PHL}				2.16	5.63	12.33	2.31	5.63	11.23	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.19	5.98	13.2	2.34	5.98	12	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.16	5.61	12.27	2.31	5.61	11.17	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.56	6.86	15.09	2.73	6.86	13.74	ns
t_{PHL}				2.76	6.98	15.04	2.96	6.98	13.68	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.72	7.19	15.93	2.91	7.19	14.47	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.76	6.96	14.99	2.96	6.96	13.63	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	80	20	40	70	ps/pF
Δt_{PHL}				20	40	80	20	40	70	
Δt_{PZH}	GZ	Y1		20	40	80	20	40	70	ps/pF
Δt_{PZL}				20	40	80	30	40	70	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOKB1LJ
24-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

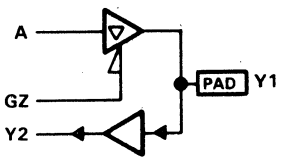
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOKB1LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOKB1LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −16 mA					3.7		V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 24 mA						0.5	V
			I_{OL} = 20.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.6			0.49	mA
C_i	Input capacitance	Y1			13.9			13.9		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		22.5			22.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.68	4.79	10.96	1.79	4.79	9.99	ns
t_{PHL}				2.87	7.19	15.3	3.08	7.19	13.96	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.74	5.1	11.83	1.86	5.1	10.77	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.91	7.29	15.47	3.12	7.29	14.11	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.02	5.68	12.96	2.15	5.68	11.8	ns
t_{PHL}				3.59	8.75	18.33	3.85	8.75	16.7	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.07	5.99	13.82	2.21	5.99	12.57	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.63	8.84	18.49	3.89	8.84	16.84	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.29			9.29		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.25			8.25		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	60	10	30	50	ps/pF
Δt_{PHL}				20	40	90	20	40	80	
Δt_{PZH}	GZ	Y1		10	30	60	10	30	60	ps/pF
Δt_{PZL}				20	40	90	20	40	80	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.02	5.56	12.37	2.16	5.56	11.28	ns
t_{PHL}				2.56	6.53	14.12	2.74	6.53	12.88	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.19	5.9	13.23	2.34	5.9	12.03	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.6	6.59	14.19	2.77	6.59	12.94	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.55	6.86	15.1	2.73	6.86	13.75	ns
t_{PHL}				3.12	7.78	16.63	3.34	7.78	15.16	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.73	7.2	15.95	2.91	7.2	14.5	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.15	7.84	16.69	3.37	7.84	15.21	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	80	20	40	70	ps/pF
Δt_{PHL}				20	40	70	20	40	70	
Δt_{PZH}	GZ	Y1		20	40	80	20	40	70	ps/pF
Δt_{PZL}				20	40	70	20	40	60	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ps/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOKB4LJ
24-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

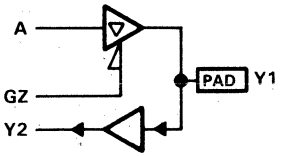
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOKB4LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOKB4LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 24 mA						0.5	V
			I_{OL} = 20.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.9			13.9		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		24.7			24.7		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IOKB4LJ
24-mA 3-STATE I/O BUFFER
WITH 0.25 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.68	4.79	10.96	1.79	4.79	9.99	ns
t_{PHL}				2.87	7.19	15.29	3.08	7.19	13.95	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.75	5.11	11.83	1.86	5.11	10.77	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.91	7.28	15.45	3.12	7.28	14.09	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.02	5.68	12.95	2.15	5.68	11.79	ns
t_{PHL}				3.59	8.74	18.32	3.85	8.74	16.69	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.07	5.99	13.82	2.22	5.99	12.57	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.63	8.83	18.47	3.89	8.83	16.82	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.3			9.3		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.25			8.25		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
Δt_{PLH}	A	Y1		10	30	60	10	30	50	ps/pF
Δt_{PHL}				20	40	90	20	40	80	
Δt_{PZH}	GZ	Y1		10	30	60	10	30	50	ps/pF
Δt_{PZL}				20	40	90	20	40	80	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.17	3.15	0.06	1.17	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0 54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.02	5.56	12.37	2.16	5.56	11.28	ns
t_{PHL}				2.56	6.52	14.12	2.65	6.52	12.88	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.2	5.91	13.24	2.34	5.91	12.03	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.59	6.58	14.18	2.77	6.58	12.93	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.55	6.86	15.1	2.73	6.86	13.75	ns
t_{PHL}				3.12	7.78	16.63	3.34	7.78	15.15	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.73	7.2	15.96	2.91	7.2	14.51	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.15	7.84	16.68	3.37	7.84	15.2	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	80	20	40	70	ps/pF
Δt_{PHL}				20	40	70	20	40	60	
Δt_{PZH}	GZ	Y1		20	40	80	20	40	70	ps/pF
Δt_{PZL}				20	40	70	20	40	60	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOKEPLJ
48-mA OPEN-DRAIN I/O BUFFER WITH 0.25 di/dt, TTL INPUT WITH HYSTERESIS, AND CMOS/TTL OUTPUT

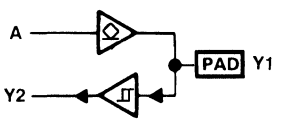
D3030, DECEMBER 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUTS	
A	Y1	Y1	Y2
L	L	L	L
H	H	H‡	H
H	L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A‡ Y2 = Y1

description

The IOKEPLJ is a noninverting open-drain input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip terminated bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus when the internal A node is at a high logic level. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOKEPLJ A,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_T	Input threshold voltage at A				2.2			2.2		V
V_{T+}	Positive-going threshold level at Y1				1.6			1.6		V
V_{T-}	Negative-going threshold level at Y1				1.2			1.2		V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$) at Y1				0.4			0.4		V
V_{OL}	Low-level output voltage		I_{OL} = 48 mA						0.5	V
			I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10			±5	μA
I_{CC}	Supply current		$V_I = V_{IH}$ or V_{IL}			3.16			0.88	mA
C_i	Input capacitance	A			0.59			0.59		pF
		Y1			11.2			11.2		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		9.52			9.52		pF

‡ With external pull-up resistor to Y2.

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y1	C_L = 15 pF	1.89	5.15	11.26	2.04	5.15	10.24	ns
			C_L = 50 pF	2.35	6.17	13.3	2.53	6.17	12.08	
t_{PLZ}	A	Y1			7.38			7.38		ns
Δt_{PZL}	A	Y1		10	30	60	20	30	50	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y1	C_L = 15 pF	1.69	4.68	10.4	1.82	4.68	9.45	ns
			C_L = 50 pF	2.05	5.52	12.12	2.21	5.52	11	
Δt_{PZL}	A	Y1		10	20	50	10	20	40	ps/pF

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2	C_L = 0	0.74	1.29	1.96	0.77	1.29	1.89	ns
t_{PHL}				0.21	1.79	5.09	0.22	1.79	4.83	
Δt_{PLH}	Y1	Y2		0.1	0.17	0.35	0.1	0.17	0.31	ns/pF
Δt_{PHL}				0.03	0.25	0.62	0.04	0.25	0.58	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOKE1LJ 48-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

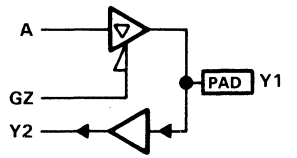
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOKE1LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOKE1LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 48 mA						0.5	V
			I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.6			0.49	mA
C_i	Input capacitance	Y1			15.4			15.4		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		27.9			27.9		pF

‡Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.71	4.86	11.12	1.82	4.86	10.13	ns
t_{PHL}				2.58	6.6	14.28	2.76	6.6	13.01	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.76	5.16	11.97	1.88	5.16	10.9	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.62	6.67	14.34	2.8	6.67	13.07	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.04	5.74	13.09	2.17	5.74	11.91	ns
t_{PHL}				3.03	7.62	16.3	3.25	7.62	14.84	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.09	6.04	13.93	2.23	6.04	12.67	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.07	7.68	16.34	3.29	7.68	14.88	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.41			9.41		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.2			9.2		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	60	10	30	50	ps/pF
Δt_{PHL}				10	30	60	10	30	50	
Δt_{PZH}	GZ	Y1		10	30	60	10	30	50	ps/pF
Δt_{PZL}				10	30	60	10	30	50	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.05	5.63	12.54	2.19	5.63	11.43	ns
t_{PHL}				2.36	6.11	13.39	2.52	6.11	12.2	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.22	5.97	13.4	2.37	5.97	12.18	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.39	6.15	13.39	2.55	6.15	12.2	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.58	6.92	15.24	2.75	6.92	13.88	ns
t_{PHL}				2.71	6.94	15.09	2.9	6.94	13.74	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.75	7.26	16.08	2.93	7.26	14.62	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.75	6.98	15.08	2.94	6.98	13.74	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	80	20	40	70	ps/pF
Δt_{PHL}				10	20	50	10	20	40	
Δt_{PZH}	GZ	Y1		20	40	80	20	40	70	ps/pF
Δt_{PZL}				10	20	50	10	20	40	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ps/pF
Δt_{PHL}				0.12	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOKE4LJ
48-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

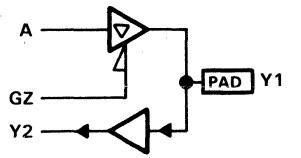
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOKE4LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOKE4LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 48 mA						0.5	V
			I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			15.4			15.4		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		29.9			29.9		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IOKE4LJ
48-mA 3-STATE I/O BUFFER
WITH 0.25 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	1.71	4.86	11.12	1.82	4.86	10.13	ns
t_{PHL}				2.58	6.6	14.27	2.76	6.6	13	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.76	5.16	11.97	1.88	5.16	10.89	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.61	6.66	14.33	2.8	6.66	13.06	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.04	5.74	13.08	2.17	5.74	11.91	ns
t_{PHL}				3.03	7.62	16.3	3.25	7.62	14.84	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.09	6.04	13.92	2.23	6.04	12.67	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.06	7.68	16.34	3.28	7.68	14.88	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.41			9.41		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.19			9.19		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
Δt_{PLH}	A	Y1		10	30	60	10	30	50	ps/pF
Δt_{PHL}				10	30	60	10	30	50	
Δt_{PZH}	GZ	Y1		10	30	60	10	30	50	ps/pF
Δt_{PZL}				10	30	60	10	30	50	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.05	5.64	12.55	2.19	5.64	11.43	ns
t_{PHL}				2.36	6.1	13.39	2.52	6.1	12.19	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.22	5.98	13.4	2.37	5.98	12.18	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.38	6.15	13.39	2.55	6.15	12.2	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.58	6.92	15.24	2.76	6.92	13.88	ns
t_{PHL}				2.71	6.94	15.09	2.9	6.94	13.73	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.75	7.26	16.09	2.93	7.26	14.62	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.74	6.98	15.08	2.93	6.98	13.73	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	80	20	40	70	ps/pF
Δt_{PHL}				10	20	50	10	20	40	
Δt_{PZH}	GZ	Y1		20	40	80	20	40	70	ps/pF
Δt_{PZL}				10	20	50	10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOKG1LJ
64-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

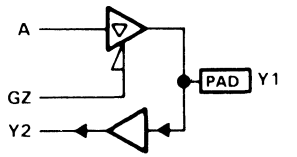
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOKG1LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOKG1LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 64 mA						0.5	V
			I_{OL} = 54.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.1			0.49	mA
C_i	Input capacitance	Y1			16.6			16.6		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		31			31		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.74	4.93	11.26	1.85	4.93	10.26	ns
t_{PHL}				2.5	6.43	14.01	2.67	6.43	12.75	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.77	5.2	12.06	1.89	5.2	10.98	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.44	6.47	13.72	2.61	6.47	12.49	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.07	5.79	13.22	2.2	5.79	12.03	ns
t_{PHL}				2.86	7.26	15.7	3.09	7.26	14.28	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.1	6.07	14	2.24	6.07	12.74	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.88	7.3	15.69	3.09	7.3	14.27	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.5			9.5		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.66			9.66		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	60	10	20	50	ps/pF
Δt_{PHL}				10	20	50	10	20	40	
Δt_{PZH}	GZ	Y1		10	20	60	10	20	50	ps/pF
Δt_{PZL}				10	20	50	10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOKG1LJ
64-mA 3-STATE I/O BUFFER
WITH 0.25 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.08	5.71	12.7	2.23	5.71	11.57	ns
t_{PHL}				2.3	5.98	13.21	2.45	5.98	12.02	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.24	6.02	13.5	2.39	6.02	12.27	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.32	6.01	13.17	2.48	6.01	11.99	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.61	6.98	15.39	2.79	6.98	14	ns
t_{PHL}				2.59	6.67	14.64	2.77	6.67	13.31	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.76	7.29	16.17	2.95	7.29	14.69	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.61	6.7	14.59	2.79	6.7	13.28	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	40	80	20	40	70	ps/pF
Δt_{PHL}				10	20	40	10	20	40	
Δt_{PZH}	GZ	Y1		10	40	80	20	40	70	ps/pF
Δt_{PZL}				10	20	40	10	20	40	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOKG4LJ
64-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

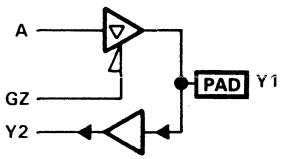
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOKG4LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOKG4LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −l6 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 64 mA						0.5	V
			I_{OL} = 54.4 mA			0.5				
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current		$V_I = V_{IH}$ or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			16.6			16.6		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		32.5			32.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOKG4LJ
64-mA 3-STATE I/O BUFFER
WITH 0.25 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.74	4.92	11.26	1.86	4.92	10.26	ns
t_{PHL}				2.5	6.43	14.01	2.67	6.43	12.75	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.78	5.2	12.05	1.9	5.2	10.98	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.52	6.47	14.01	2.7	6.47	12.75	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.07	5.79	13.21	2.2	5.79	12.02	ns
t_{PHL}				2.86	7.26	15.69	3.06	7.26	14.27	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.1	6.07	13.99	2.24	6.07	12.74	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.88	7.3	15.68	3.09	7.3	14.26	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.5			9.5		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.66			9.66		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	20	60	10	20	50	ps/pF
Δt_{PHL}				10	20	50	10	20	40	
Δt_{PZH}	GZ	Y1		10	20	60	10	20	50	ps/pF
Δt_{PZL}				10	20	50	10	20	40	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.09	5.71	12.7	2.23	5.71	11.57	ns
t_{PHL}				2.3	5.98	13.22	2.45	5.98	12.02	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.24	6.02	13.5	2.39	6.02	12.27	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.32	6.01	13.17	2.47	6.01	11.98	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.61	6.99	15.38	2.79	6.99	14	ns
t_{PHL}				2.59	6.67	14.64	2.76	6.67	13.31	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.76	7.3	16.17	2.95	7.3	14.7	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.61	6.7	14.59	2.79	6.7	13.27	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	40	80	20	40	70	ps/pF
Δt_{PHL}				10	20	40	10	20	40	
Δt_{PZH}	GZ	Y1		10	40	80	20	40	70	ps/pF
Δt_{PZL}				10	20	40	10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOK01LJ 10-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

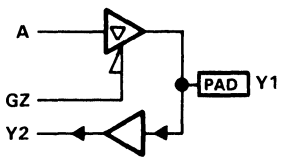
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOK01LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOK01LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −10 mA				3.7			V
			I_{OH} = −8.5 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 10 mA						0.5	V
			I_{OL} = 8.5 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.7			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		18.7			18.7		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.79	5.02	11.47	1.9	5.02	10.44	ns
t_{PHL}				2.93	7.34	15.56	3.15	7.34	14.18	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.83	5.33	12.35	1.96	5.33	11.23	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.95	7.42	15.82	3.16	7.42	14.37	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.21	6.15	14.01	2.35	6.15	12.75	ns
t_{PHL}				4.05	9.71	20.12	4.34	9.71	18.31	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.26	6.47	14.9	2.41	6.47	13.55	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.06	9.81	20.45	4.36	9.81	18.55	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.75			9.75		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.61			8.61		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	70	10	30	70	ps/pF
Δt_{PHL}				30	70	130	30	70	120	
Δt_{PZH}	GZ	Y1		10	30	70	10	30	70	ps/pF
Δt_{PZL}				30	70	130	30	70	120	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.21	5.97	13.21	2.36	5.97	12.03	ns
t_{PHL}				2.53	6.47	14.01	2.71	6.47	12.77	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.38	6.32	14.14	2.54	6.32	12.83	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.53	6.49	14.08	2.71	6.49	12.8	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.91	7.69	16.78	3.11	7.69	15.28	ns
t_{PHL}				3.37	8.31	17.64	3.6	8.31	16.06	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.08	8.05	17.75	3.29	8.05	16.12	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.37	8.33	17.73	3.61	8.33	16.11	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	50	100	20	50	90	ps/pF
Δt_{PHL}				20	50	100	30	50	90	
Δt_{PZH}	GZ	Y1		20	50	100	20	50	90	ps/pF
Δt_{PZL}				20	50	100	30	50	90	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.41	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOK04LJ
10-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

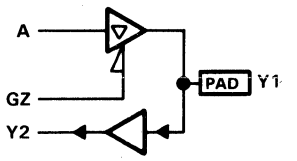
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOK04LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOK04LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −10 mA				3.7			V
			I_{OH} = −8.5 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 10 mA						0.5	V
			I_{OL} = 8.5 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		19.9			19.9		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOK04LJ
10-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	1.79	5.02	11.47	1.9	5.02	10.44	ns
t_{PHL}				2.93	7.33	15.54	3.14	7.33	14.16	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	1.83	5.33	12.35	1.96	5.33	11.23	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.94	7.41	15.79	3.16	7.41	14.35	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.21	6.15	14.01	2.35	6.15	12.75	ns
t_{PHL}				4.05	9.7	20.09	4.34	9.7	18.28	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.26	6.47	14.9	2.41	6.47	13.55	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.06	9.8	20.42	4.36	9.8	18.53	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.75			9.75		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.61			8.61		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	70	10	30	70	ps/pF
Δt_{PHL}				30	70	130	30	70	120	
Δt_{PZH}	GZ	Y1		10	30	70	10	30	70	ps/pF
Δt_{PZL}				30	70	130	30	70	120	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.21	5.97	13.22	2.36	5.97	12.03	ns
t_{PHL}				2.53	6.47	14	2.7	6.47	12.76	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.38	6.33	14.15	2.54	6.33	12.84	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.53	6.49	14.06	2.7	6.49	12.79	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.91	7.69	16.79	3.12	7.69	15.29	ns
t_{PHL}				3.36	8.3	17.63	3.6	8.3	16.05	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.09	8.05	17.76	3.3	8.05	16.13	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.36	8.33	17.71	3.6	8.33	16.1	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	50	100	20	50	90	ps/pF
Δt_{PHL}				20	50	100	30	50	90	
Δt_{PZH}	GZ	Y1		20	50	100	20	50	90	ps/pF
Δt_{PZL}				20	50	100	30	50	90	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOK21LJ
2-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

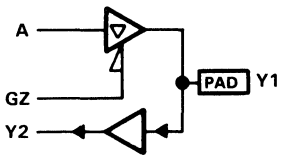
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOK21LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOK21LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −2 mA				3.7			V
			I_{OH} = −1.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 2 mA						0.5	V
			I_{OL} = 1.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.7			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.2			17.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.19	8.69	19.75	3.41	8.69	17.95	ns
t_{PHL}				7.3	16.86	34.45	7.84	16.86	31.35	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.25	9.2	21.64	3.48	9.2	19.57	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	7.54	18.35	40.63	8.12	18.35	36.2	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	4.44	12.14	27.53	4.75	12.14	25.06	ns
t_{PHL}				11.5	25.61	51.15	12.36	25.61	46.41	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.49	12.75	29.93	4.81	12.75	27.11	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	11.88	27.96	60.88	12.81	27.96	54.01	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		15.56			15.56		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		12.3			12.3		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		40	100	220	40	100	200	ps/pF
Δt_{PHL}				120	250	480	130	250	430	
Δt_{PZH}	GZ	Y1		40	100	240	40	100	220	ps/pF
Δt_{PZL}				120	270	580	130	270	510	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	4.45	11.38	24.62	4.77	11.38	22.41	ns
t_{PHL}				5.93	14.14	29.66	6.36	14.14	27.01	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.66	12.31	28.23	4.99	12.31	25.39	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	6.05	14.88	32.72	6.49	14.88	29.46	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	6.92	17.5	37.32	7.41	17.5	34.03	ns
t_{PHL}				8.88	20.44	42.03	9.54	20.44	38.18	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	7.14	18.92	43.19	7.65	18.92	38.88	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	9.05	21.47	46.25	9.72	21.47	41.55	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		70	170	360	80	170	330	ps/pF
Δt_{PHL}				80	180	350	90	180	320	
Δt_{PZH}	GZ	Y1		70	190	430	80	190	390	ps/pF
Δt_{PZL}				90	190	390	90	190	350	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.41	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOK24LJ
2-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

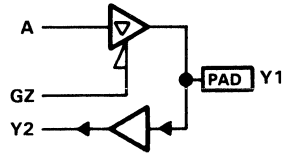
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOK24LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOK24LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −2 mA				3.7			V
			I_{OH} = −1.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 2 mA						0.5	V
			I_{OL} = 1.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.7			17.7		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.2	8.69	19.75	3.42	8.69	17.94	ns
t_{PHL}				7.29	16.82	34.35	7.82	16.82	31.26	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.25	9.2	21.65	3.48	9.2	19.57	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	7.53	18.3	40.5	8.11	18.3	36.09	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	4.44	12.15	27.54	4.76	12.15	25.07	ns
t_{PHL}				11.49	25.57	51.05	12.35	25.57	46.31	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.49	12.75	29.95	4.81	12.75	27.11	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	11.87	27.91	60.75	12.8	27.91	53.88	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		15.54			15.54		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		12.31			12.31		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		40	100	220	40	100	200	ps/pF
Δt_{PHL}				120	250	480	130	250	430	
Δt_{PZH}	GZ	Y1		40	100	240	40	100	220	ps/pF
Δt_{PZL}				120	270	580	130	270	510	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	4.47	11.4	24.69	4.79	11.4	22.44	ns
t_{PHL}				5.92	14.13	29.62	6.35	14.13	26.98	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.67	12.35	28.31	5	12.35	25.46	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	6.04	14.86	32.68	6.48	14.86	29.42	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	6.93	17.53	37.37	7.42	17.53	34.09	ns
t_{PHL}				8.88	20.42	41.98	9.53	20.42	38.14	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	7.15	18.95	43.27	7.66	18.95	38.94	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	9.04	21.45	46.19	9.72	21.45	41.48	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		70	180	360	80	180	330	ps/pF
Δt_{PHL}				80	180	350	90	180	320	
Δt_{PZH}	GZ	Y1		70	190	430	80	190	390	ps/pF
Δt_{PZL}				90	190	390	90	190	340	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOK41LJ
4-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

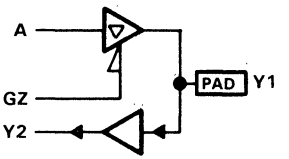
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOK41LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOK41LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −4 mA					3.7		V
			I_{OH} = −3.4 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 4 mA						0.5	V
			I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			11.3			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.5			17.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.35	6.47	14.7	2.51	6.47	13.36	ns
t_{PHL}				4.59	10.94	22.58	4.92	10.94	20.56	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.4	6.84	15.86	2.57	6.84	14.39	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.65	11.34	24.14	5	11.34	21.8	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.11	8.51	19.26	3.32	8.51	17.52	ns
t_{PHL}				6.86	15.69	31.68	7.37	15.69	28.76	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.16	8.91	20.53	3.38	8.91	18.63	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	6.95	16.27	33.87	7.48	16.27	30.5	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		11.47			11.47		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10.01			10.01		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	60	130	20	60	120	ps/pF
Δt_{PHL}				60	140	260	70	140	230	
Δt_{PZH}	GZ	Y1		20	60	130	20	60	120	ps/pF
Δt_{PZL}				70	140	280	70	140	250	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOK41LJ
4-mA 3-STATE I/O BUFFER
WITH 0.25 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.11	8.1	17.65	3.33	8.1	16.06	ns
t_{PHL}				3.81	9.36	19.8	4.08	9.36	18.04	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.29	8.61	19.22	3.52	8.61	17.4	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.83	9.55	20.6	4.11	9.55	18.67	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	4.48	11.47	24.62	4.8	11.47	22.42	ns
t_{PHL}				5.45	12.88	26.73	5.85	12.88	24.29	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.66	12.07	26.6	4.99	12.07	24.11	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.49	13.14	27.75	5.89	13.14	25.1	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		40	100	200	40	100	180	ps/pF
Δt_{PHL}				50	100	200	50	100	180	
Δt_{PZH}	GZ	Y1		40	100	210	40	100	190	ps/pF
Δt_{PZL}				50	100	200	50	100	180	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOK44LJ
4-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

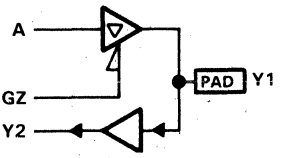
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOK44LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOK44LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −4 mA				3.7			V
			I_{OH} = −3.4 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 4 mA						0.5	V
			I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.8			17.8		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IOK44LJ
4-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.35	6.47	14.69	2.51	6.47	13.36	ns
t_{PHL}				4.58	10.91	22.52	4.91	10.91	20.51	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.4	6.84	15.86	2.57	6.84	14.34	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.64	11.32	24.05	4.99	11.32	21.73	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	3.11	8.51	19.26	3.32	8.51	17.52	ns
t_{PHL}				6.85	15.67	31.61	7.36	15.67	28.7	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.16	8.91	20.53	3.38	8.91	18.63	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	6.95	16.25	33.8	7.48	16.25	30.44	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		11.46			11.46		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10.01			10.01		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
Δt_{PLH}	A	Y1		20	60	130	20	60	120	ps/pF
Δt_{PHL}				60	140	260	70	140	230	
Δt_{PZH}	GZ	Y1		20	60	130	20	60	120	ps/pF
Δt_{PZL}				70	140	280	70	140	250	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.11	8.12	17.67	3.33	8.12	16.08	ns
t_{PHL}				3.81	9.35	19.77	4.08	9.35	18.02	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.3	8.62	19.24	3.53	8.62	17.41	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.83	9.54	20.56	4.11	9.54	18.64	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	4.49	11.48	24.64	4.8	11.48	22.45	ns
t_{PHL}				5.45	12.87	26.7	5.85	12.87	24.26	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.67	12.09	26.64	5	12.09	24.13	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.48	13.13	27.72	5.89	13.13	25.08	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		40	100	200	40	100	180	ps/pF
Δt_{PHL}				50	100	200	50	100	180	
Δt_{PZH}	GZ	Y1		40	100	210	40	100	190	ps/pF
Δt_{PZL}				50	100	200	50	100	180	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOK61LJ
6-mA 3-STATE I/O BUFFER
WITH 0.25 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

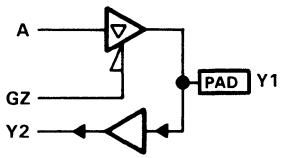
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOK61LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOK61LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −6 mA				3.7			V
			I_{OH} = −5.1 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 6 mA						0.5	V
			I_{OL} = 5.1 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.7			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		18.5			18.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.07	5.74	13.07	2.21	5.74	11.89	ns
t_{PHL}				3.7	9	18.78	3.97	9	17.11	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.11	6.08	14.07	2.26	6.08	12.77	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.73	9.2	19.51	4	9.2	17.68	

C_L = 50 pF

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.66	7.31	16.57	2.84	7.31	15.07	ns
t_{PHL}				5.33	12.44	25.39	5.73	12.44	23.07	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.7	7.65	17.60	2.89	7.65	15.98	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.37	12.71	26.36	5.78	12.71	23.84	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.92			9.92		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.33			9.33		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	100	20	40	90	ps/pF
Δt_{PHL}				50	100	190	50	100	170	
Δt_{PZH}	GZ	Y1		20	40	100	20	40	90	ps/pF
Δt_{PZL}				50	100	200	50	100	180	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOK61LJ
6-mA 3-STATE I/O BUFFER
WITH 0.25 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.66	7.02	15.39	2.84	7.02	14.01	ns
t_{PHL}				3.12	7.81	16.67	3.34	7.81	15.19	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.82	7.43	16.57	3.02	7.43	15.01	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.13	7.89	17.01	3.35	7.89	15.45	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.67	9.49	20.51	3.93	9.49	18.68	ns
t_{PHL}				4.32	10.41	21.8	4.63	10.41	19.82	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.84	9.94	21.84	4.11	9.94	19.81	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.33	10.52	22.23	4.65	10.52	20.16	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		30	70	150	30	70	130	ps/pF
Δt_{PHL}				30	70	150	40	50	130	
Δt_{PZH}	GZ	Y1		30	70	150	30	70	140	ps/pF
Δt_{PZL}				30	80	150	40	80	130	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ps/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOK64LJ
6-mA 3-STATE I/O BUFFER WITH 0.25 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

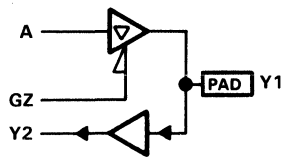
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOK64LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOK64LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −6 mA				3.7			V
			I_{OH} = −5.1 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 6 mA						0.5	V
			I_{OL} = 5.1 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		18.5			18.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IOK64LJ
6-mA 3-STATE I/O BUFFER
WITH 0.25 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.07	5.74	13.07	2.21	5.74	11.89	ns
t_{PHL}				3.69	8.98	18.74	3.96	8.98	17.07	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.12	6.08	14.06	2.26	6.08	12.77	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.72	9.18	19.46	4	9.18	17.64	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.65	7.32	16.57	2.83	7.32	15.07	ns
t_{PHL}				5.32	12.43	25.36	5.72	12.43	23.04	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.7	7.65	17.6	2.89	7.65	15.98	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.37	12.69	26.32	5.77	12.69	23.8	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.92			9.92		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.33			9.33		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	50	100	20	50	90	ps/pF
Δt_{PHL}				50	100	190	50	100	170	
Δt_{PZH}	GZ	Y1		20	50	100	20	50	90	ps/pF
Δt_{PZL}				50	100	200	50	100	180	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.66	7.03	15.41	2.85	7.03	14.02	ns
t_{PHL}				3.12	7.8	16.66	3.34	7.8	15.17	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.83	7.44	16.58	3.02	7.44	15.03	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.12	7.88	16.99	3.34	7.88	15.43	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.7	7.65	17.6	2.89	7.65	15.98	ns
t_{PHL}				5.37	12.69	26.32	5.77	12.69	23.8	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.67	9.51	20.53	3.93	9.51	18.69	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.32	10.41	21.79	4.63	10.41	19.81	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	50	100	20	50	90	ps/pF
Δt_{PHL}				50	100	200	50	100	180	
Δt_{PZH}	GZ	Y1		30	70	150	30	70	130	ps/pF
Δt_{PZL}				30	70	150	40	70	130	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOHA1LJ
16-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

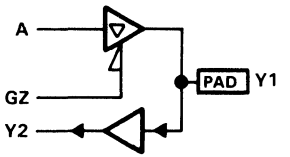
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOHA1LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOHA1LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 16 mA						0.5	V
			I_{OL} = 13.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.6			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		20.8			20.8		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.12	5.97	13.62	2.26	5.97	12.4	ns
t_{PHL}				3.29	8.22	17.52	3.52	8.22	15.96	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.18	6.29	14.54	2.33	6.29	13.23	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.31	8.28	17.71	3.54	8.28	16.1	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.52	7.04	16.03	2.69	7.04	14.59	ns
t_{PHL}				4.22	10.24	21.46	4.52	10.24	19.54	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.57	7.36	16.94	2.75	7.36	15.4	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.23	10.29	21.65	4.54	10.29	19.67	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.28			9.28		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.32			9.32		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	70	10	30	60	ps/pF
Δt_{PHL}				30	60	110	30	60	100	
Δt_{PZH}	GZ	Y1		10	30	70	10	30	60	ps/pF
Δt_{PZL}				30	60	110	30	60	100	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOHA1LJ
16-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.55	6.92	15.35	2.72	6.92	13.98	ns
t_{PHL}				2.91	7.4	16.06	3.11	7.4	14.63	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.72	7.28	16.32	2.91	7.28	14.82	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.91	7.4	16.08	3.11	7.4	14.63	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.18	8.46	18.6	3.4	8.46	16.93	ns
t_{PHL}				3.62	9.01	19.29	3.87	9.01	17.56	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.35	8.82	19.54	3.58	8.82	17.75	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.62	9.01	19.3	3.87	9.01	17.55	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	90	20	40	80	ps/pF
Δt_{PHL}				20	50	90	20	50	80	
Δt_{PZH}	GZ	Y1		20	40	90	20	40	80	ps/pF
Δt_{PZL}				20	50	90	20	50	80	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOHA4LJ
16-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

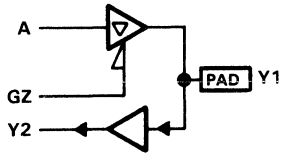
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOHA4LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOHA4LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 16 mA						0.5	V
			I_{OL} = 13.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		22.5			22.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOHA4LJ
16-mA 3-STATE I/O BUFFER
WITH 0.125 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.12	5.97	13.62	2.26	5.97	12.4	ns
t_{PHL}				3.29	8.21	17.49	3.52	8.21	15.94	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.18	6.28	14.54	2.33	6.28	13.23	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.3	8.27	17.69	3.54	8.27	16.08	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.52	7.04	16.01	2.69	7.04	14.57	ns
t_{PHL}				4.22	10.24	21.45	4.52	10.24	19.52	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.57	7.36	16.94	2.75	7.36	15.41	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.23	10.29	21.63	4.54	10.29	19.66	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.28			9.28		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.18			9.18		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	70	10	30	60	ps/pF
Δt_{PHL}				30	60	110	30	60	100	
Δt_{PZH}	GZ	Y1		10	30	70	10	30	60	ps/pF
Δt_{PZL}				30	60	110	30	60	100	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.55	6.92	15.36	2.73	6.92	13.99	ns
t_{PHL}				2.91	7.4	16.04	3.1	7.4	14.62	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.73	7.28	16.33	2.91	7.28	14.83	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.91	7.4	16.07	3.1	7.4	14.62	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.18	8.46	18.58	3.4	8.46	16.92	ns
t_{PHL}				3.62	9.01	19.29	3.87	9.01	17.55	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.36	8.82	19.56	3.59	8.82	17.76	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.62	9.01	19.3	3.87	9.01	17.55	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	90	20	40	80	ps/pF
Δt_{PHL}				20	50	90	20	50	80	
Δt_{PZH}	GZ	Y1		20	40	90	20	40	80	ps/pF
Δt_{PZL}				20	50	90	20	50	80	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOHB1LJ 24-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

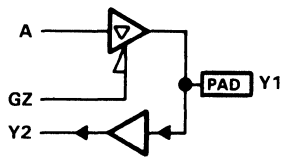
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOHB1LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOHB1LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 24 mA						0.5	V
			I_{OL} = 20.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.6			0.49	mA
C_i	Input capacitance	Y1			13.9			13.9		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		22.5			22.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.11	5.96	13.6	2.25	5.96	12.39	ns
t_{PHL}				4.08	9.83	20.55	4.37	9.83	18.76	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.18	6.3	14.58	2.33	6.3	13.26	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.14	9.98	20.89	4.43	9.98	19.05	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.51	7.03	16.01	2.68	7.03	14.57	ns
t_{PHL}				4.93	11.69	24.21	5.28	11.69	22.07	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.58	7.37	16.97	2.76	7.37	15.43	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.99	11.83	24.51	5.34	11.83	22.33	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.29			9.29		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.25			8.25		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	70	10	30	60	ps/pF
Δt_{PHL}				20	50	100	30	50	90	
Δt_{PZH}	GZ	Y1		10	30	70	10	30	60	ps/pF
Δt_{PZL}				20	50	100	30	50	90	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.54	6.91	15.33	2.71	6.91	13.96	ns
t_{PHL}				3.67	8.98	19.09	3.92	8.98	17.42	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.73	7.29	16.36	2.92	7.29	14.85	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.71	9.08	19.27	3.96	9.08	17.58	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.17	8.45	18.57	3.39	8.45	16.91	ns
t_{PHL}				4.34	10.5	22.14	4.64	10.5	20.18	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.36	8.83	19.57	3.59	8.83	17.78	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.38	10.59	22.29	4.68	10.59	20.32	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	90	20	40	80	ps/pF
Δt_{PHL}				20	40	90	20	40	80	
Δt_{PZH}	GZ	Y1		20	40	90	20	40	80	ps/pF
Δt_{PZL}				20	40	90	20	40	80	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOHB4LJ
24-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

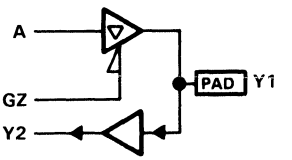
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOHB4LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOHB4LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −16 mA					3.7		V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 24 mA						0.5	V
			I_{OL} = 20.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
ICC	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.9			13.9		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		24.7			24.7		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IOHB4LJ
24-mA 3-STATE I/O BUFFER
WITH 0.125 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.11	5.96	13.6	2.25	5.96	12.38	ns
t_{PHL}				4.08	9.82	20.53	4.36	9.82	18.75	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.18	6.3	14.58	2.33	6.3	13.26	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.13	9.97	20.88	4.42	9.97	19.03	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.51	7.03	16.00	2.68	7.03	14.57	ns
t_{PHL}				4.93	11.68	24.18	5.28	11.68	22.06	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.58	7.37	16.97	2.76	7.37	15.44	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.98	11.82	24.49	5.34	11.82	22.31	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.29			9.29		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.25			8.25		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	70	10	30	60	ps/pF
Δt_{PHL}				20	50	100	30	50	90	
Δt_{PZH}	GZ	Y1		10	30	70	10	30	60	ps/pF
Δt_{PZL}				20	50	100	30	50	90	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.54	6.91	15.34	2.72	6.91	13.97	ns
t_{PHL}				3.67	8.98	19.08	3.92	8.98	17.41	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.73	7.3	16.36	2.92	7.3	14.86	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.71	9.08	19.26	3.96	9.08	17.57	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.17	8.45	18.57	3.39	8.45	16.91	ns
t_{PHL}				4.34	10.49	22.12	4.64	10.49	20.17	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.36	8.84	19.58	3.59	8.84	17.79	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.38	10.58	22.28	4.68	10.58	20.31	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	90	20	40	80	ps/pF
Δt_{PHL}				20	40	90	20	40	80	
Δt_{PZH}	GZ	Y1		20	40	90	20	40	80	ps/pF
Δt_{PZL}				20	40	90	20	40	80	

IOHEPLJ
48-mA OPEN-DRAIN I/O BUFFER WITH 0.125 di/dt, TTL INPUT WITH HYSTERESIS, AND CMOS/TTL OUTPUT

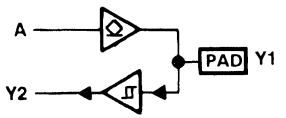
D3030, DECEMBER 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUTS	
A	Y1	Y1	Y2
L	L	L	L
H	H	H‡	H
H	L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A‡ Y2 = Y1

description

The IOHEPLJ is a noninverting open-drain input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip terminated bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus when the internal A node is at a high logic level. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOHEPLJ A,Y2,Y1;

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP§	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP§	0°C to 70°C MAX	UNIT
V_T	Input threshold voltage at A				2.2			2.2		V
V_{T+}	Positive-going threshold level at Y1				1.6			1.6		V
V_{T-}	Negative-going threshold level at Y1				1.2			1.2		V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$) at Y1				0.4			0.4		V
V_{OL}	Low-level output voltage		I_{OL} = 48 mA						0.5	V
			I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			2.61			0.78	mA
C_i	Input capacitance	A			0.59			0.59		pF
		Y1			11.2			11.2		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		9.52			9.52		pF

‡ With external pull-up resistor to Y2.

§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y1	C_L = 15 pF	2.87	7.37	15.8	3.09	7.37	14.36	ns
			C_L = 50 pF	3.4	8.59	18.25	3.66	8.59	16.57	
t_{PLZ}	A	Y1			7.38			7.38		ns
Δt_{PZL}	A	Y1		20	30	70	20	30	60	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y1	C_L = 15 pF	2.59	6.76	14.71	2.78	6.76	13.36	ns
			C_L = 50 pF	3.02	7.77	16.78	3.25	7.77	15.24	
Δt_{PZL}	A	Y1		10	30	60	10	30	50	ps/pF

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2	C_L = 0	0.74	1.29	1.96	0.77	1.29	1.89	ns
t_{PHL}				0.21	1.79	5.09	0.22	1.79	4.83	
Δt_{PLH}	Y1	Y2		0.1	0.17	0.35	0.1	0.17	0.31	ns/pF
Δt_{PHL}				0.03	0.25	0.62	0.04	0.25	0.58	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOHE1LJ 48-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

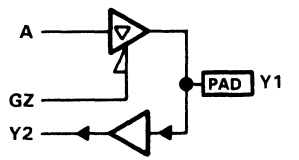
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOHE1LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOHE1LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 48 mA						0.5	V
			I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10			±5	μA
I_{CC}	Supply current		$V_I = V_{IH}$ or V_{IL}			10.6			0.49	mA
C_i	Input capacitance	Y1			15.4			15.4		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		27.9			27.9		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.13	6.03	13.79	2.27	6.03	12.55	ns
t_{PHL}				3.67	8.96	18.96	3.93	8.96	17.3	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.21	6.36	14.73	2.36	6.36	13.39	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.7	9.04	19.11	3.96	9.04	17.41	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.52	7.09	16.16	2.69	7.09	14.71	ns
t_{PHL}				4.21	10.18	21.43	4.5	10.18	19.52	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.6	7.42	17.1	2.78	7.42	15.54	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.23	10.25	21.55	4.54	10.25	19.61	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.41			9.41		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.18			9.18		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	70	10	30	60	ps/pF
Δt_{PHL}				20	30	70	20	30	60	
Δt_{PZH}	GZ	Y1		10	30	70	10	30	60	ps/pF
Δt_{PZL}				20	30	70	20	30	60	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.56	6.99	15.53	2.74	6.99	14.14	ns
t_{PHL}				3.36	8.32	17.85	3.59	8.32	16.28	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.76	7.37	16.53	2.95	7.37	15	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.38	8.36	17.91	3.61	8.36	16.31	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.19	8.52	18.74	3.41	8.52	17.05	ns
t_{PHL}				3.79	9.32	19.93	4.05	9.32	18.15	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.38	8.89	19.72	3.62	8.89	17.9	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.81	9.37	19.98	4.07	9.37	18.18	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	90	20	40	80	ps/pF
Δt_{PHL}				10	30	60	10	30	50	
Δt_{PZH}	GZ	Y1		20	40	90	20	40	80	ps/pF
Δt_{PZL}				10	30	60	10	30	50	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOHE4LJ
48-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

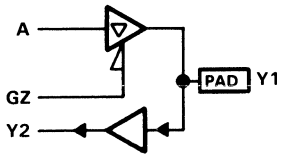
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOHE4LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOHE4LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 48 mA						0.5	V
			I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			15.4			15.4		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		29.9			29.9		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IOHE4LJ
48-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.13	6.03	13.78	2.27	6.03	12.55	ns
t_{PHL}				3.67	8.96	18.96	3.93	8.96	17.28	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.21	6.36	14.73	2.36	6.36	13.4	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.7	9.03	19.08	3.96	9.03	17.39	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.53	7.09	16.15	2.7	7.09	14.7	ns
t_{PHL}				4.2	10.18	21.42	4.5	10.18	21.42	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.6	7.42	17.09	2.78	7.42	15.53	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.23	10.25	21.52	4.53	10.25	19.59	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.41			9.41		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.18			9.18		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	70	10	30	60	ps/pF
Δt_{PHL}				20	30	70	20	30	60	
Δt_{PZH}	GZ	Y1		10	30	70	10	30	60	ps/pF
Δt_{PZL}				20	30	70	20	30	60	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.57	6.99	15.54	2.75	6.99	14.15	ns
t_{PHL}				3.36	8.32	17.85	3.58	8.32	16.27	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.77	7.37	16.54	2.95	7.37	15.02	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.38	8.36	17.89	3.61	8.36	16.3	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.19	8.52	18.73	3.41	8.52	17.05	ns
t_{PHL}				3.79	9.33	19.92	4.05	9.33	18.14	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.39	8.89	19.71	3.62	8.89	17.9	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.81	9.37	19.95	4.07	9.37	18.17	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	90	20	40	80	ps/pF
Δt_{PHL}				10	30	60	10	30	50	
Δt_{PZH}	GZ	Y1		20	40	90	20	40	80	ps/pF
Δt_{PZL}				10	30	60	10	30	50	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOHG1LJ 64-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

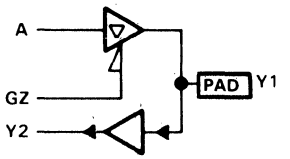
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOHG1LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOHG1LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −16 mA					3.7		V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 64 mA						0.5	V
			I_{OL} = 54.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.1			0.49	mA
C_i	Input capacitance	Y1			16.6			16.6		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		31			31		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.17	6.11	13.97	2.31	6.11	12.72	ns
t_{PHL}				3.53	8.62	18.37	3.77	8.62	16.73	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.22	6.41	14.83	2.37	6.41	13.49	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.54	8.65	18.39	3.78	8.65	16.74	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.55	7.16	16.31	2.73	7.16	14.84	ns
t_{PHL}				3.95	9.62	20.4	4.22	9.62	18.57	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.61	7.45	17.16	2.79	7.45	15.6	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.96	9.65	20.4	4.24	9.65	18.56	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.49			9.49		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.65			9.65		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	30	70	10	30	60	ps/pF
Δt_{PHL}				10	30	60	10	30	50	
Δt_{PZH}	GZ	Y1		10	30	70	10	30	60	ps/pF
Δt_{PZL}				10	30	60	10	30	50	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.6	7.08	15.73	2.78	7.08	14.32	ns
t_{PHL}				3.24	8.04	17.37	3.46	8.04	15.82	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.78	7.42	16.65	2.97	7.42	15.11	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.25	8.05	17.33	3.47	8.05	15.77	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.22	8.59	18.89	3.44	8.59	17.19	ns
t_{PHL}				3.59	8.87	19.1	3.83	8.87	17.38	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.4	8.93	19.79	3.63	8.93	17.98	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.6	8.88	19.04	3.84	8.88	17.33	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	90	20	40	80	ps/pF
Δt_{PHL}				10	20	50	10	20	40	
Δt_{PZH}	GZ	Y1		20	40	90	20	40	80	ps/pF
Δt_{PZL}				10	20	50	10	20	40	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOHG4LJ 64-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

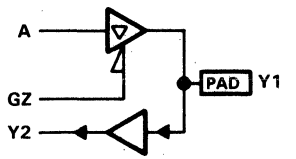
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOHG4LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOHG4LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 64 mA						0.5	V
			I_{OL} = 54.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			16.6			16.6		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		32.5			32.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.17	6.11	13.96	2.31	6.11	12.71	ns
t_{PHL}				3.52	8.61	18.35	3.77	8.61	16.72	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.23	6.4	14.83	2.38	6.4	13.48	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.54	8.64	18.37	3.78	8.64	16.73	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.55	7.16	16.31	2.73	7.16	14.84	ns
t_{PHL}				3.95	9.61	20.39	4.22	9.61	18.56	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.61	7.45	17.16	2.79	7.45	15.6	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.96	9.64	20.39	4.24	9.64	18.56	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.5			9.5		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.65			9.65		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
Δt_{PLH}	A	Y1		10	30	70	10	30	60	ps/pF
Δt_{PHL}				10	30	60	10	30	50	
Δt_{PZH}	GZ	Y1		10	30	70	10	30	60	ps/pF
Δt_{PZL}				10	30	60	10	30	50	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	3	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.53	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.61	7.08	15.73	2.79	7.08	14.32	ns
t_{PHL}				3.24	8.04	17.36	3.46	8.04	15.81	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.79	7.43	16.65	2.98	7.43	15.12	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.25	8.05	17.32	3.47	8.05	15.77	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.22	8.59	18.9	3.45	8.59	17.2	ns
t_{PHL}				3.59	8.87	19.09	3.83	8.87	17.37	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.4	8.93	19.8	3.64	8.93	17.99	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.6	8.88	19.04	3.84	8.88	17.32	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	40	90	20	40	80	ps/pF
Δt_{PHL}				10	20	50	10	20	40	
Δt_{PZH}	GZ	Y1		20	40	90	20	40	80	ps/pF
Δt_{PZL}				10	20	50	10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOH01LJ 10-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

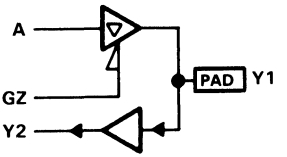
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOH01LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOH01LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −10 mA				3.7			V
			I_{OH} = −8.5 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 10 mA						0.5	V
			I_{OL} = 8.5 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.7			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		18.7			18.7		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.26	6.31	14.42	2.41	6.31	13.11	ns
t_{PHL}				3.88	9.54	20.09	4.16	9.54	18.32	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.3	6.64	15.39	2.46	6.64	13.98	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.9	9.68	20.57	4.18	9.68	18.69	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.77	7.67	17.43	2.96	7.67	15.85	ns
t_{PHL}				5.17	12.29	25.43	5.54	12.29	21.14	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.81	8	18.44	3.01	8	16.75	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.19	12.45	25.95	5.57	12.45	23.54	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.75			9.75		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.61			8.61		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	40	90	20	40	80	ps/pF
Δt_{PHL}				40	80	150	40	80	140	
Δt_{PZH}	GZ	Y1		10	40	90	20	40	80	ps/pF
Δt_{PZL}				40	80	150	40	80	140	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOH01LJ
10-mA 3-STATE I/O BUFFER
WITH 0.125 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.79	7.47	16.53	2.99	7.47	15.03	ns
t_{PHL}				3.37	8.48	18.22	3.61	8.48	16.62	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.95	7.86	17.61	3.16	7.86	15.97	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.37	8.54	18.42	3.61	8.54	16.75	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.62	9.48	20.69	3.87	9.48	18.82	ns
t_{PHL}				4.35	10.65	22.54	4.66	10.65	20.52	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.78	9.88	21.83	4.04	9.88	19.8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.35	10.7	22.75	4.66	10.7	20.66	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	60	120	30	60	110	ps/pF
Δt_{PHL}				30	60	110	30	60	110	
Δt_{PZH}	GZ	Y1		20	60	120	30	60	110	ps/pF
Δt_{PZL}				30	60	120	30	60	110	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.41	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.32	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOH04LJ
10-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

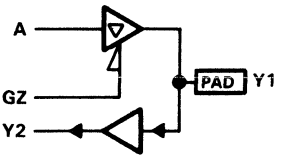
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOH04LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOH04LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −10 mA					3.7		V
			I_{OH} = −8.5 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 10 mA						0.5	V
			I_{OL} = 8.5 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		19.9			19.9		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IOH04LJ
10-mA 3-STATE I/O BUFFER
WITH 0.125 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.27	6.31	14.41	2.42	6.31	13.1	ns
t_{PHL}				3.87	9.53	20.06	4.15	9.53	18.29	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.3	6.64	15.4	2.46	6.64	13.98	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.9	9.66	20.52	4.18	9.66	18.65	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.77	7.67	17.44	2.96	7.67	15.85	ns
t_{PHL}				5.17	12.28	25.4	5.54	12.28	23.12	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.81	8.01	18.45	3.01	8.01	16.75	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.19	12.44	25.91	5.57	12.44	23.52	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.75			9.75		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.6			8.6		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		10	40	90	20	40	80	ps/pF
Δt_{PHL}				40	80	150	40	80	140	
Δt_{PZH}	GZ	Y1		10	40	90	20	40	80	ps/pF
Δt_{PZL}				40	80	150	40	80	140	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.8	7.48	16.53	3	7.48	15.04	ns
t_{PHL}				3.37	8.48	18.21	3.6	8.48	16.6	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.96	7.87	17.65	3.16	7.87	15.99	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.37	8.53	18.39	3.61	8.53	16.73	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.62	9.49	20.71	3.87	9.49	18.84	ns
t_{PHL}				4.35	10.64	22.52	4.66	10.64	20.5	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.78	9.89	21.85	4.05	9.89	19.81	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.35	10.7	22.73	4.66	10.7	20.66	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		20	60	120	30	60	110	ps/pF
Δt_{PHL}				30	60	120	30	60	110	
Δt_{PZH}	GZ	Y1		20	60	120	30	60	110	ps/pF
Δt_{PZL}				30	60	120	30	60	110	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOH21LJ 2-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

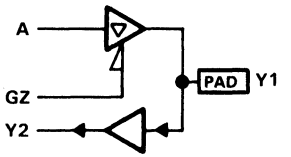
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOH21LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOH21LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −2 mA				3.7			V
			I_{OH} = −1.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 2 mA						0.5	V
			I_{OL} = 1.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.7			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.2			17.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	4.04	10.92	24.87	4.32	10.92	22.59	ns
t_{PHL}				9.18	21.21	43.41	9.84	21.21	39.56	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.1	11.53	27.27	4.4	11.53	24.61	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	9.51	23.23	51.77	10.23	23.23	46.14	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	5.47	14.8	33.56	5.86	14.8	30.5	ns
t_{PHL}				13.78	30.76	61.69	14.79	30.76	56.04	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	5.53	15.49	36.39	5.93	15.49	32.89	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	14.22	33.52	73.13	15.32	33.52	64.98	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		15.55			15.55		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		12.3			12.3		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		40	110	250	40	110	230	ps/pF
Δt_{PHL}				130	270	520	140	270	470	
Δt_{PZH}	GZ	Y1		40	110	260	40	110	240	ps/pF
Δt_{PZL}				130	290	610	150	290	540	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOH21LJ
2-mA 3-STATE I/O BUFFER
WITH 0.125 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	5.51	13.98	30.39	5.91	13.98	27.62	ns
t_{PHL}				7.58	18.08	37.93	8.11	18.08	34.58	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	5.73	15.11	34.89	6.15	15.11	31.3	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	7.74	19.13	42.33	8.3	19.13	38.11	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	8.17	20.5	43.91	8.75	20.5	39.96	ns
t_{PHL}				10.91	25.16	51.87	11.7	25.16	47.17	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	8.42	22.06	50.41	9.02	22.06	45.3	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	11.11	26.47	57.26	11.94	26.47	51.46	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		80	190	390	80	190	350	ps/pF
Δt_{PHL}				100	200	400	100	200	360	
Δt_{PZH}	GZ	Y1		80	200	440	80	200	400	ps/pF
Δt_{PZL}				100	210	430	100	210	380	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.41	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.32	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOH24LJ
2-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

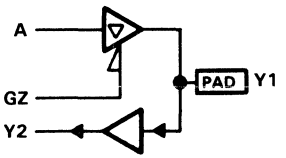
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOH24LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOH24LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −2 mA				3.7			V
			I_{OH} = −1.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 2 mA						0.5	V
			I_{OL} = 1.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.7			17.7		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	4.05	10.92	24.88	4.33	10.92	22.59	ns
t_{PHL}				9.16	21.17	43.3	9.82	21.17	39.46	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.1	11.54	27.27	4.4	11.54	24.61	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	9.49	23.16	51.59	10.21	23.16	45.99	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	5.48	14.8	33.57	5.87	14.8	30.5	ns
t_{PHL}				13.76	30.72	61.56	14.77	30.72	55.95	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	5.53	15.49	36.43	5.94	15.49	32.9	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	14.21	33.48	73.02	15.31	33.48	64.9	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		15.53			15.53		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		12.31			12.31		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		40	110	250	40	110	230	ps/pF
Δt_{PHL}				130	270	520	140	270	470	
Δt_{PZH}	GZ	Y1		40	110	260	40	110	240	ps/pF
Δt_{PZL}				130	290	610	150	290	540	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	3	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	5.53	14.01	30.46	5.92	14.01	27.67	ns
t_{PHL}				7.56	18.06	37.88	8.1	18.06	34.54	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	5.75	15.16	34.96	6.17	15.16	31.37	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	7.73	19.11	42.26	8.29	19.11	38.06	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	8.19	20.53	43.97	8.77	20.53	40.02	ns
t_{PHL}				10.89	25.15	51.8	11.68	25.15	47.14	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	8.42	22.09	50.51	9.03	22.09	45.38	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	11.11	26.45	57.2	11.93	26.45	51.43	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		80	190	390	80	190	350	ps/pF
Δt_{PHL}				100	200	400	100	200	360	
Δt_{PZH}	GZ	Y1		80	200	440	80	200	400	ps/pF
Δt_{PZL}				100	210	430	100	210	380	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOH41LJ 4-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

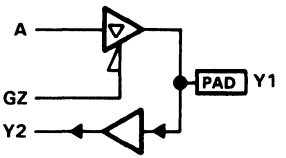
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOH41LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOH41LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −4 mA					3.7		V
			I_{OH} = −3.4 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 4 mA						0.5	V
			I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			11.3			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.5			17.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.99	8.19	18.6	3.19	8.19	16.9	ns
t_{PHL}				5.88	13.94	28.75	6.31	13.94	26.2	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.04	8.62	20.04	3.26	8.62	18.14	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.98	14.52	31	6.42	14.52	27.99	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.88	10.56	23.88	4.15	10.56	21.7	ns
t_{PHL}				8.43	19.26	39.02	9.05	19.26	35.45	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.93	11.01	25.4	4.22	11.01	23	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	8.56	20	41.81	9.21	20	37.68	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		11.46			11.46		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10.01			10.01		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		30	70	150	30	70	140	ps/pF
Δt_{PHL}				70	150	290	80	150	260	
Δt_{PZH}	GZ	Y1		30	70	150	30	70	140	ps/pF
Δt_{PZL}				70	160	310	80	160	280	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.91	10.12	22.09	4.18	10.12	20.07	ns
t_{PHL}				4.95	12.08	25.49	5.3	12.08	23.24	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.09	10.73	24.09	4.39	10.73	21.75	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.99	12.38	26.74	5.35	12.38	24.23	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	5.44	13.85	29.81	5.83	13.85	27.11	ns
t_{PHL}				6.83	16.12	33.51	7.33	16.12	30.47	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	5.64	14.55	32.16	6.05	14.55	29.07	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	6.89	16.48	34.94	7.4	16.48	31.61	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		40	110	220	50	110	200	ps/pF
Δt_{PHL}				50	120	230	60	120	210	
Δt_{PZH}	GZ	Y1		40	110	230	50	110	210	ps/pF
Δt_{PZL}				50	120	230	60	120	210	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOH44LJ
4-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

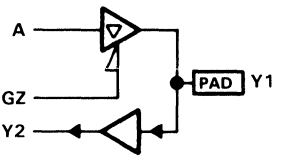
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOH44LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOH44LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −4 mA					3.7		V
			I_{OH} = −3.4 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 4 mA						0.5	V
			I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.8			17.8		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IOH44LJ
4-mA 3-STATE I/O BUFFER
WITH 0.125 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	2.99	8.19	18.62	3.19	8.19	16.91	ns
t_{PHL}				5.87	13.91	28.7	6.29	13.91	26.15	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.04	8.62	20.03	3.27	8.62	18.13	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.97	14.49	30.93	6.41	14.49	27.93	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.89	10.56	23.87	4.15	10.56	21.69	ns
t_{PHL}				8.42	19.24	38.96	9.04	19.24	35.4	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.93	11.01	25.41	4.22	11.01	23	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	8.55	19.97	41.75	9.19	19.97	37.63	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		11.46			11.46		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		10			10		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		30	70	150	30	70	140	ps/pF
Δt_{PHL}				70	150	290	80	150	260	
Δt_{PZH}	GZ	Y1		30	70	150	30	70	140	ps/pF
Δt_{PZL}				70	160	310	80	160	280	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	3	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.53	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.91	10.13	22.13	4.19	10.13	20.11	ns
t_{PHL}				4.94	12.07	25.49	5.29	12.07	23.23	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.1	10.74	24.12	4.4	10.74	21.77	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.98	12.36	26.72	5.34	12.36	24.21	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	5.46	13.87	29.82	5.85	13.87	27.13	ns
t_{PHL}				6.83	16.11	33.5	7.33	16.11	30.45	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	5.65	14.57	32.21	6.06	14.57	29.1	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	6.88	16.47	34.92	7.39	16.47	31.6	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		40	110	220	50	110	200	ps/pF
Δt_{PHL}				50	120	230	60	120	210	
Δt_{PZH}	GZ	Y1		40	110	230	50	110	210	ps/pF
Δt_{PZL}				50	120	230	60	120	210	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOH61LJ 6-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

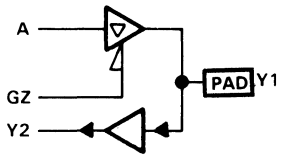
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOH61LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to CMOS threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOH61LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			2.5			2.5		
V_{OH}	High-level output voltage		I_{OH} = −6 mA				3.7			V
			I_{OH} = −5.1 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 6 mA						0.5	V
			I_{OL} = 5.1 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			10.7			0.49	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		18.5			18.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	55°C to 125°C MIN	55°C to 125°C TYP†	55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.64	7.28	16.57	2.82	7.28	15.06	ns
t_{PHL}				4.8	11.58	24.12	5.15	11.58	21.98	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.68	7.65	17.73	2.87	7.65	16.08	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.85	11.88	25.27	5.2	11.88	22.88	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	3.34	9.12	20.69	3.56	9.12	18.79	ns
t_{PHL}				6.67	15.51	31.7	7.16	15.51	28.8	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.37	9.51	21.88	3.62	9.51	19.84	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	6.73	15.87	33.04	7.23	15.87	29.88	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.92			9.92		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.33			9.33		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
Δt_{PLH}	A	Y1		20	50	120	20	50	110	ps/pF
Δt_{PHL}				50	110	220	60	110	190	
Δt_{PZH}	GZ	Y1		20	50	120	20	50	110	ps/pF
Δt_{PZL}				50	110	220	60	110	200	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOH61LJ
6-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, CMOS INPUT, AND CMOS/TTL OUTPUT

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.36	8.82	19.35	3.59	8.82	17.59	ns
t_{PHL}				4.1	10.15	21.6	4.39	10.15	19.69	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.53	9.3	20.8	3.78	9.3	18.83	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.11	10.29	22.21	4.4	10.29	20.16	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	4.53	11.62	25.18	4.85	11.62	22.89	ns
t_{PHL}				5.49	13.19	27.62	5.89	13.19	25.12	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.7	12.14	26.75	5.03	12.14	24.22	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.51	13.35	28.29	5.92	13.35	25.65	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		30	80	170	40	80	150	ps/pF
Δt_{PHL}				40	90	170	40	90	160	
Δt_{PZH}	GZ	Y1		30	80	170	40	80	150	ps/pF
Δt_{PZL}				40	90	170	40	90	160	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Y1	Y2		0.58	0.9	1.52	0.6	0.9	1.4	ns
t_{PHL}				0.12	0.63	1.21	0.13	0.63	1.16	
Δt_{PLH}	Y1	Y2		0.06	0.2	0.34	0.07	0.2	0.33	ns/pF
Δt_{PHL}				0.13	0.13	0.26	0.13	0.13	0.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

IOH64LJ
6-mA 3-STATE I/O BUFFER WITH 0.125 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

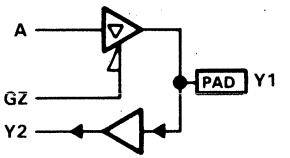
D3030, APRIL 1988

I/O BUFFER CELL

FUNCTION TABLE

INPUTS			OUTPUTS	
A	GZ	Y1	Y1	Y2
L	L	L	L	L
H	L	H	H	H
X	H	L	Z	L
X	H	H	Z	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATIONS: Y1 = A (if GZ is L) Y2 = Y1

description

The IOH64LJ cell is a noninverting 3-state input-output buffer that interfaces CMOS internal functions with TTL or CMOS off-chip bidirectional bus lines. The input buffer responds to TTL threshold levels imposed on the I/O bus regardless of the state of the output enable GZ. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: IOH64LJ A,GZ,Y2,Y1;

A pull-up or pull-down terminator can be connected to the Y1 node.

absolute maximum ratings and recommended operating conditions

These are specified as part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage	A, GZ			2.2			2.2		V
		Y1			1.3			1.3		
V_{OH}	High-level output voltage		I_{OH} = −6 mA				3.7			V
			I_{OH} = −5.1 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 6 mA						0.5	V
			I_{OL} = 5.1 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			3.45			0.3	mA
C_i	Input capacitance	Y1			13.8			13.8		pF
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		18.5			18.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

IOH64LJ
6-mA 3-STATE I/O BUFFER
WITH 0.125 di/dt, TTL INPUT, AND CMOS/TTL OUTPUT

D3030, ARPIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	2.64	7.28	16.57	2.82	7.28	15.06	ns
t_{PHL}				4.79	11.56	24.06	5.14	11.56	21.93	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	2.68	7.65	17.74	2.88	7.65	16.08	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.84	11.86	25.2	5.2	11.86	22.83	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	A	Y1	$R_L = \infty$	3.34	9.13	20.7	3.57	9.13	18.79	ns
t_{PHL}				6.66	15.49	31.65	7.15	15.49	28.78	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.38	9.51	21.89	3.62	9.51	19.84	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	6.72	15.86	32.99	7.23	15.86	29.84	
t_{PHZ}	GZ	Y1	R_L = 1 kΩ to GND		9.92			9.92		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.33			9.33		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
Δt_{PLH}	A	Y1		20	50	120	20	50	110	ps/pF
Δt_{PHL}				50	110	220	60	110	200	
Δt_{PZH}	GZ	Y1		20	50	120	20	50	110	ps/pF
Δt_{PZL}				50	110	220	60	110	200	

input switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP†	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP†	0°C to 70°C MAX	UNIT
t_{PLH}	Y1	Y2		0.79	1.43	2.26	0.81	1.43	2.16	ns
t_{PHL}				0.05	1.18	3.15	0.06	1.18	2.99	
Δt_{PLH}	Y1	Y2		0.06	0.18	0.37	0.07	0.18	0.32	ns/pF
Δt_{PHL}				0.03	0.24	0.58	0.04	0.24	0.54	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	3.37	8.83	19.37	3.6	8.83	17.61	ns
t_{PHL}				4.09	10.14	21.58	4.38	10.14	19.67	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	3.53	9.31	20.84	3.79	9.31	18.85	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.1	10.28	22.18	4.4	10.28	20.14	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y1	$R_L = \infty$	4.53	11.64	25.22	4.85	11.64	22.91	ns
t_{PHL}				5.49	13.18	27.6	5.89	13.18	25.11	
t_{PZH}	GZ	Y1	R_L = 1 kΩ to GND	4.7	12.15	26.79	5.04	12.15	24.24	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.51	13.34	28.27	5.91	13.34	25.63	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y1		30	80	170	40	80	150	ps/pF
Δt_{PHL}				40	90	170	40	90	160	
Δt_{PZH}	GZ	Y1		30	80	170	40	80	150	ps/pF
Δt_{PZL}				40	90	170	40	90	160	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

13 Output Buffers

D3030, APRIL 1988

OUTPUT MACROS

The TSC500 Series CMOS standard-cell library provides the custom IC designer a selection of output buffers. Each output is characterized for driving either CMOS or TTL loads. The buffers can be used with an active pull-up or pull-down terminator. When used, the terminator is connected to the output node. Use of a terminator, especially with an open-drain or 3-state output, ensures that the output will be driven to a high- or low-logic level thereby avoiding exposure to a high-impedance or floating condition.

Each output buffer is offered in the following options with respect to di/dt circuitry:

MACRO CLASS	RELATIVE di/dt	APPLICATION
OPIxxLJ	1	Critical path(s) only (least delay)
OPJxxLJ	0.5	Can reduce GND pins by up to 25%
OPKxxLJ	0.25	Can reduce GND pins by up to 45%
OPHxxLJ	0.125	Can reduce GND pins by up to 60% (most delay)

The TSC500 output cells are designed to actively bypass and dissipate electrostatic discharges (ESD). Guard-ring structures that provide current management techniques for the cell to recover from exposure to high currents of up to 400 mA are employed, thereby negating most common sources that can produce a latch-up condition.

These output macros are designed to provide low-impedance drive levels for both the high- and low-logic-level states. As a result, passive resistance has been omitted in series with the output transistors. Shorting a high-level output to ground or a low-level output to V_{CC} will cause current to flow in excess of that recommended for normal operation. Therefore, it is recommended that outputs not be shorted directly to ground or V_{CC}.

Dynamic-drive capability of the outputs is specified by the change in propagation delay time parameters included with the switching characteristics. The change in propagation delay times provides a means for making direct comparisons of the various output responses to changes in capacitive loading.

D3030, APRIL 1988

The following output cells are available in the TSC500 Series CMOS standard-cell library:

MACRO SELECTION TABLE

TTL-/CMOS COMPATIBLE OUTPUT BUFFER CELLS					
MACRO NAME				OUTPUT	
di/dt = 1	di/dt = 0.5	di/dt = 0.25	di/dt = 0.125	CURRENT	TYPE OF OUTPUT
OPIA0LJ	OPJA0LJ	OPKA0LJ	OPHA0LJ	16/16 mA	TOTEM-POLE
OPIA1LJ	OPJA1LJ	OPKA1LJ	OPHA1LJ	16 mA	OPEN-DRAIN
OPIA3LJ	OPJA3LJ	OPKA3LJ	OPHA3LJ	16/16 mA	3-STATE
OPIB0LJ	OPJB0LJ	OPKB0LJ	OPHB0LJ	24/16 mA	TOTEM-POLE
OPIB1LJ	OPJB1LJ	OPKB1LJ	OPHB1LJ	24 mA	OPEN-DRAIN
OPIB3LJ	OPJB3LJ	OPKB3LJ	OPHB3LJ	24/16 mA	3-STATE
OPIE0LJ	OPJE0LJ	OPKE0LJ	OPHE0LJ	48/16 mA	TOTEM-POLE
OPIE1LJ	OPJE1LJ	OPKE1LJ	OPHE1LJ	48 mA	OPEN-DRAIN
OPIE3LJ	OPJE3LJ	OPKE3LJ	OPHE3LJ	48/16 mA	3-STATE
OPIG0LJ	OPJG0LJ	OPKG0LJ	OPHG0LJ	64/16 mA	TOTEM-POLE
OPIG1LJ	OPJG1LJ	OPKG1LJ	OPHG1LJ	64 mA	OPEN-DRAIN
OPIG3LJ	OPJG3LJ	OPKG3LJ	OPHG3LJ	64/16 mA	3-STATE
OPI00LJ	OPJ00LJ	OPK00LJ	OPH00LJ	10/10 mA	TOTEM-POLE
OPI01LJ	OPJ01LJ	OPK01LJ	OPH01LJ	10 mA	OPEN-DRAIN
OPI03LJ	OPJ03LJ	OPK03LJ	OPH03LJ	10/10 mA	3-STATE
OPI20LJ	OPJ20LJ	OPK20LJ	OPH20LJ	2/2 mA	TOTEM-POLE
OPI21LJ	OPJ21LJ	OPK21LJ	OPH21LJ	2 mA	OPEN-DRAIN
OPI23LJ	OPJ23LJ	OPK23LJ	OPH23LJ	2/2 mA	3-STATE
OPI40LJ	OPJ40LJ	OPK40LJ	OPH40LJ	4/4 mA	TOTEM-POLE
OPI41LJ	OPJ41LJ	OPK41LJ	OPH41LJ	4 mA	OPEN-DRAIN
OPI43LJ	OPJ43LJ	OPK43LJ	OPH43LJ	4/4 mA	3-STATE
OPI60LJ	OPJ60LJ	OPK60LJ	OPH60LJ	6/6 mA	TOTEM-POLE
OPI61LJ	OPJ61LJ	OPK61LJ	OPH61LJ	6 mA	OPEN-DRAIN
OPI63LJ	OPJ63LJ	OPK63LJ	OPH63LJ	6/6 mA	3-STATE

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPIA0LJ 16-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPIA0LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist.

Label: OPIA0LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −16 mA				3.7			V
		I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 16 mA						0.5	V
		I_{OL} = 13.6 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			4.21			0.5	mA
C_i	Input capacitance			0.53			0.53		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		21.2			21.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	0.63	1.22	2.43	0.65	1.22	2.22	ns
t_{PHL}				0.76	1.83	3.81	0.81	1.83	3.47	
t_{PLH}	A	Y	C_L = 50 pF	0.75	1.64	3.43	0.79	1.64	3.13	ns
t_{PHL}				1.24	2.89	5.88	1.32	2.89	5.34	
Δt_{PLH}	A	Y		0	10	30	0	10	30	ps/pF
Δt_{PHL}				10	30	60	10	30	50	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	0.72	1.52	3.03	0.76	1.52	2.77	ns
t_{PHL}				0.66	1.54	3.24	0.7	1.54	2.95	
t_{PLH}	A	Y	C_L = 50 pF	1	2.28	4.66	1.06	2.28	4.27	ns
t_{PHL}				0.98	2.28	4.75	1.04	2.28	4.31	
Δt_{PLH}	A	Y		10	20	50	10	20	40	ps/pF
Δt_{PHL}				10	20	40	10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPIA1LJ
16-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPIA1LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPIA1LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA						0.5	V
		I_{OL} = 13.6 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			2.21			0.38	mA
C_i	Input capacitance			0.19			0.19		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		2.13			2.13		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	0.63	1.59	3.33	0.68	1.59	3.04	ns
t_{PZL}			C_L = 50 pF	1.15	2.72	5.57	1.23	2.72	5.05	
t_{PLZ}	A	Y			7.74			7.74		ns
Δt_{PZL}	A	Y		10	30	60	20	30	60	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	0.53	1.29	2.73	0.56	1.29	2.49	ns
t_{PZL}			C_L = 50 pF	0.9	2.11	4.4	0.95	2.11	4	
Δt_{PZL}	A	Y		10	20	50	10	20	40	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPIA3LJ
16-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

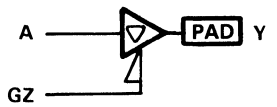
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPIA3LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPIA3LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 16 mA						0.5	V
			I_{OL} = 13.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		22.5			22.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.78	2.22	5.06	0.82	2.22	4.62	ns
t_{PHL}				1	2.63	5.73	1.06	2.63	5.2	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	0.77	2.47	5.75	0.82	2.47	5.26	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.94	2.49	5.39	1	2.49	4.91	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.93	2.67	6.11	0.98	2.67	5.58	ns
t_{PHL}				1.47	3.68	7.79	1.58	3.68	7.07	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	0.94	2.93	6.82	1	2.93	6.23	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.44	3.6	7.59	1.55	3.6	6.89	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.36			9.36		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.24			9.24		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	0	10	30	0	10	30	ps/pF
Δt_{PHL}				10	30	60	10	30	50	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	0	10	30	10	10	30	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	30	60	20	30	60	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPIA3LJ
16-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.9	2.56	5.74	0.95	2.56	5.25	ns
t_{PHL}				0.88	2.31	5.1	0.93	2.31	4.63	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.01	2.83	6.35	1.07	2.83	5.8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.81	2.14	4.71	0.87	2.14	4.29	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.19	3.34	7.4	1.27	3.34	6.77	ns
t_{PHL}				1.2	3.04	6.61	1.28	3.04	6	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.31	3.62	8.05	1.39	3.62	7.35	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.17	2.94	6.35	1.25	2.94	5.76	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	20	50	10	20	40	ps/pF
Δt_{PHL}				10	20	40	10	20	40	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	20	50	10	20	40	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	20	40	10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPIB0LJ 24-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPIB0LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist.

Label: OPIB0LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −16 mA				3.7			V
		I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 24 mA						0.5	V
		I_{OL} = 20.4 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			4.21			0.57	mA
C_i	Input capacitance			0.63			0.63		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		26			26		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	0.66	1.27	2.53	0.68	1.27	2.3	ns
t_{PHL}				0.65	1.58	3.27	0.69	1.58	2.99	
t_{PLH}	A	Y	C_L = 50 pF	0.78	1.67	3.48	0.81	1.67	3.17	ns
t_{PHL}				0.99	2.36	4.84	1.06	2.36	4.4	
Δt_{PLH}	A	Y		0	10	30	0	10	20	ps/pF
Δt_{PHL}				10	20	40	10	20	40	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	0.75	1.56	3.11	0.78	1.56	2.84	ns
t_{PHL}				0.56	1.33	2.8	0.59	1.33	2.55	
t_{PLH}	A	Y	C_L = 50 pF	1.02	2.31	4.7	1.08	2.31	4.3	ns
t_{PHL}				0.81	1.9	3.97	0.86	1.9	3.62	
Δt_{PLH}	A	Y		10	20	50	10	20	40	ps/pF
Δt_{PHL}				10	20	30	10	20	30	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPIB1LJ
24-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPIB1LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPIB1LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 24 mA						0.5	V
		I_{OL} = 20.4 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			3.31			0.57	mA
C_i	Input capacitance			0.27			0.27		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		3.44			3.44		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	0.53	1.32	2.77	0.56	1.32	2.53	ns
t_{PZL}			C_L = 50 pF	0.89	2.17	4.45	0.96	2.17	4.05	
t_{PLZ}	A	Y			6.79			6.69		ns
Δt_{PZL}	A	Y		10	20	50	10	20	40	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	0.44	1.08	2.28	0.47	1.08	2.09	ns
t_{PZL}			C_L = 50 pF	0.72	1.71	3.58	0.77	1.71	3.26	
Δt_{PZL}	A	Y		10	20	40	10	20	30	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPIB3LJ
24-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

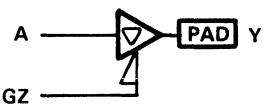
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPIB3LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPIB3LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 24 mA						0.5	V
			I_{OL} = 20.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		24.7			24.7		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPIB3LJ
24-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.83	2.31	5.22	0.88	2.31	4.76	ns
t_{PHL}				0.87	2.42	5.35	0.94	2.42	4.86	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	0.78	2.49	5.8	0.83	2.49	5.31	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.83	2.3	5.03	0.89	2.3	4.59	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.97	2.73	6.22	1.03	2.73	5.67	ns
t_{PHL}				1.23	3.21	6.93	1.32	3.21	6.3	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	0.95	2.96	6.87	1.01	2.96	6.28	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.21	3.15	6.72	1.3	3.15	6.11	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.37			9.37		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.29			8.29		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	0	10	30	0	10	30	ps/pF
Δt_{PHL}				10	20	50	10	20	40	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	0	10	30	10	10	30	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	20	50	10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.95	2.65	5.88	1.01	2.65	5.37	ns
t_{PHL}				0.8	2.16	4.83	0.85	2.16	4.39	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.02	2.85	6.4	1.08	2.85	5.85	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.74	2.02	4.48	0.79	2.02	4.08	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.23	3.4	7.5	1.3	3.4	6.86	ns
t_{PHL}				1.04	2.73	6.03	1.11	2.73	5.47	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.32	3.64	8.1	1.4	3.64	7.4	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.01	2.65	5.77	1.08	2.65	5.25	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	20	50	10	20	40	ps/pF
Δt_{PHL}				10	20	30	10	20	30	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	20	50	10	20	40	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	20	40	10	20	30	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPIE0LJ 48-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPIE0LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist.

Label: OPIE0LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −16 mA				3.7			V
		I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 48 mA						0.5	V
		I_{OL} = 40.8 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			6.6			1.15	mA
C_i	Input capacitance			0.92			0.92		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		36.5			36.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	0.7	1.36	2.74	0.73	1.36	2.48	ns
t_{PHL}				0.46	1.19	2.48	0.49	1.19	2.28	
t_{PLH}	A	Y	C_L = 50 pF	0.82	1.75	3.65	0.85	1.75	3.32	ns
t_{PHL}				0.67	1.64	3.4	0.71	1.64	3.11	
Δt_{PLH}	A	Y		0	10	30	0	10	20	ps/pF
Δt_{PHL}				10	10	30	10	10	20	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	0.79	1.68	3.36	0.83	1.68	3.07	ns
t_{PHL}				0.43	1	2.11	0.45	1	1.94	
t_{PLH}	A	Y	C_L = 50 pF	1.07	2.41	4.92	1.12	2.41	4.5	ns
t_{PHL}				0.57	1.35	2.83	0.61	1.35	2.59	
Δt_{PLH}	A	Y		10	20	40	10	20	40	ps/pF
Δt_{PHL}				0	10	20	0	10	20	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPIE1LJ
48-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPIE1LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPIE1LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 48 mA						0.5	V
		I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			6.6			1.14	mA
C_i	Input capacitance			0.55			0.55		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		7.12			7.12		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	0.35	0.99	2.07	0.38	0.99	1.91	ns
t_{PZL}			C_L = 50 pF	0.59	1.49	3.09	0.63	1.49	2.82	
t_{PLZ}	A	Y			7.2			7.2		ns
Δt_{PZL}	A	Y		10	10	30	10	10	30	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	0.32	0.82	1.74	0.34	0.82	1.6	ns
t_{PZL}			C_L = 50 pF	0.5	1.21	2.54	0.53	1.21	2.33	
Δt_{PZL}	A	Y		10	10	20	10	10	20	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPIE3LJ 48-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

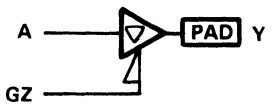
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPIE3LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPIE3LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 48 mA						0.5	V
			I_{OL} = 40.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		36.7			36.7		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.96	2.71	6.14	1.02	2.71	5.57	ns
t_{PHL}				0.79	2.19	4.97	0.84	2.19	4.53	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	0.81	2.55	5.92	0.86	2.55	5.42	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.77	2.11	4.72	0.8	2.11	4.31	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.08	3.04	6.89	1.14	3.04	6.26	ns
t_{PHL}				0.97	2.66	5.93	1.03	2.66	5.4	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	0.97	3.01	6.98	1.03	3.01	6.38	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.96	2.6	5.72	1.02	2.6	5.22	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.48			9.48		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.34			9.34		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	0	10	20	0	10	20	ps/pF
Δt_{PHL}				10	10	30	10	10	20	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	0	10	30	0	10	30	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	10	30	10	10	30	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPIE3LJ
48-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.08	3.03	6.75	1.15	3.03	6.14	ns
t_{PHL}				0.73	2	4.6	0.77	2	4.19	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.04	2.91	6.54	1.1	2.91	5.98	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.7	1.92	4.35	0.74	1.92	3.97	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.34	3.7	8.16	1.42	3.7	7.44	ns
t_{PHL}				0.87	2.37	5.35	0.93	2.37	4.87	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.34	3.7	8.23	1.43	3.7	7.52	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.86	2.3	5.13	0.91	2.3	4.68	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	20	40	10	20	40	ps/pF
Δt_{PHL}				0	10	20	0	10	20	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	20	50	10	20	40	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	0	10	20	0	10	20	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPIG0LJ
64-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPIG0LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist.

Label: OPIG0LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −16 mA				3.7			V
		I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 64 mA						0.5	V
		I_{OL} = 54.4 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			8.83			1.53	mA
C_i	Input capacitance			1.1			1.1		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		40.3			40.3		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	0.71	1.39	2.79	0.74	1.39	2.53	ns
t_{PHL}				0.4	1.04	2.17	0.43	1.04	1.99	
t_{PLH}	A	Y	C_L = 50 pF	0.83	1.77	3.7	0.86	1.77	3.37	ns
t_{PHL}				0.55	1.41	2.92	0.59	1.41	2.67	
Δt_{PLH}	A	Y		0	10	30	0	10	20	ps/pF
Δt_{PHL}				0	10	20	0	10	20	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	0.8	1.71	3.43	0.84	1.71	3.13	ns
t_{PHL}				0.36	0.88	1.86	0.38	0.88	1.71	
t_{PLH}	A	Y	C_L = 50 pF	1.08	2.44	4.99	1.14	2.44	4.56	ns
t_{PHL}				0.49	1.16	2.44	0.52	1.16	2.23	
Δt_{PLH}	A	Y		10	20	40	10	20	40	ps/pF
Δt_{PHL}				0	10	20	0	10	20	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPIG1LJ
64-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPIG1LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPIG1LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 64 mA						0.5	V
		I_{OL} = 54.4 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			8.83			1.53	mA
C_i	Input capacitance			0.71			0.71		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		9.41			9.41		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	0.33	.9	1.88	0.35	0.9	1.73	ns
t_{PZL}			C_L = 50 pF	0.5	1.3	2.7	0.53	1.3	2.48	
t_{PLZ}	A	Y			7.56			7.56		ns
Δt_{PZL}	A	Y		0	10	20	10	10	20	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	0.3	0.75	1.59	0.31	0.75	1.46	ns
t_{PZL}			C_L = 50 pF	0.44	1.07	2.24	0.46	1.07	2.05	
Δt_{PZL}	A	Y		0	10	20	0	10	20	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPIG3LJ
64-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

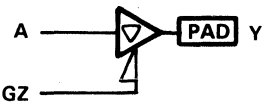
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPIG3LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPIG3LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 64 mA						0.5	V
			I_{OL} = 54.4 mA			0.5				
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current		$V_I = V_{IH}$ or V_{IL}		1.04			0.27		mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns		54.8			54.8		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPIG3LJ
64-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.03	3.03	6.9	1.1	3.03	6.25	ns
t_{PHL}				0.78	2.17	4.97	0.82	2.17	4.53	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	0.82	2.58	6	0.87	2.58	5.49	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.76	2.11	4.75	0.8	2.11	4.33	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.16	3.32	7.57	1.23	3.32	6.87	ns
t_{PHL}				0.92	2.55	5.74	0.98	2.55	5.22	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	0.98	3.04	7.05	1.04	3.04	6.45	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.91	2.5	5.55	0.97	2.5	5.06	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.56			9.56		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.88			9.88		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	0	10	20	0	10	20	ps/pF
Δt_{PHL}				0	10	20	0	10	20	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	0	10	30	0	10	30	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	0	10	20	0	10	20	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.16	3.34	7.51	1.23	3.34	6.82	ns
t_{PHL}				0.72	2.01	4.64	0.76	2.01	4.22	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.05	2.95	6.63	1.12	2.95	6.06	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.69	1.94	4.43	0.74	1.94	4.03	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.41	3.98	8.84	1.51	3.98	8.04	ns
t_{PHL}				0.84	2.3	5.26	0.89	2.3	4.78	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.36	3.74	8.32	1.44	3.74	7.6	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.83	2.25	5.07	0.88	2.25	4.61	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	20	40	10	20	30	ps/pF
Δt_{PHL}				0	10	20	0	10	20	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	20	50	10	20	40	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	0	10	20	0	10	20	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI00LJ 10-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI00LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist.

Label: OPI00LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −10 mA				3.7			V
		I_{OH} = −8.5 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 10 mA						0.5	V
		I_{OL} = 8.5 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			2.63			0.31	mA
C_i	Input capacitance			0.35			0.35		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		15.5			15.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	0.69	1.41	2.9	0.72	1.41	2.65	ns
t_{PHL}				0.95	2.28	4.72	1.02	2.28	4.3	
t_{PLH}	A	Y	C_L = 50 pF	0.89	2.04	4.37	0.93	2.04	4	ns
t_{PHL}				1.71	3.91	7.86	1.83	3.91	7.13	
Δt_{PLH}	A	Y		10	20	40	10	20	40	ps/pF
Δt_{PHL}				20	50	90	20	50	80	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	0.83	1.84	3.73	0.88	1.84	3.42	ns
t_{PHL}				0.8	1.87	3.94	0.84	1.87	3.58	
t_{PLH}	A	Y	C_L = 50 pF	1.28	3.01	6.21	1.36	3.01	5.69	ns
t_{PHL}				1.29	2.99	6.19	1.38	2.99	5.62	
Δt_{PLH}	A	Y		10	30	70	10	30	70	ps/pF
Δt_{PHL}				10	30	60	20	30	60	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI01LJ 10-mA N-CHANNEL OPEN-DRAIN OUTPUT BUFFER

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI01LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI01LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 10 mA						0.5	V
		I_{OL} = 8.5 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			1.37			0.24	mA
C_i	Input capacitance			0.13			0.13		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		1.36			1.36		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	0.85	2.07	4.34	0.9	2.07	3.95	ns
t_{PZL}			C_L = 50 pF	1.63	3.77	7.69	1.75	3.77	6.95	
t_{PLZ}	A	Y			8.01			8.01		ns
Δt_{PZL}	A	Y		20	50	100	20	50	90	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	0.69	1.65	3.51	0.73	1.65	3.2	ns
t_{PZL}			C_L = 50 pF	1.22	2.84	5.92	1.3	2.84	5.36	
Δt_{PZL}	A	Y		20	30	70	20	30	60	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI03LJ
10-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

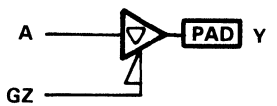
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPI03LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI03LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −10 mA				3.7			V
			I_{OH} = −8.5 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 10 mA						0.5	V
			I_{OL} = 8.5 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.8			17.8		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.82	2.23	5.04	0.86	2.23	4.61	ns
t_{PHL}				1.19	3.08	6.63	1.28	3.08	6.03	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	0.82	2.49	5.75	0.87	2.49	5.26	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.17	3.01	6.46	1.25	3.01	5.87	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.03	2.87	6.54	1.09	2.87	5.98	ns
t_{PHL}				1.97	4.71	9.78	2.11	4.71	8.86	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.03	3.14	7.27	1.1	3.14	6.65	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.95	4.7	9.77	2.1	4.7	8.84	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.83			9.83		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.74			8.74		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	20	40	10	20	40	ps/pF
Δt_{PHL}				20	50	90	20	50	80	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	20	40	10	20	40	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	20	50	90	20	50	90	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI03LJ
10-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.99	2.71	5.97	1.05	2.71	5.46	ns
t_{PHL}				1.02	2.62	5.76	1.08	2.62	5.23	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.1	2.98	6.62	1.17	2.98	6.05	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	0.98	2.52	5.49	1.04	2.52	5	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.44	3.89	8.46	1.54	3.89	7.74	ns
t_{PHL}				1.52	3.74	8.02	1.63	3.74	7.27	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.57	4.19	9.2	1.67	4.19	8.4	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.51	3.69	7.87	1.6	3.69	7.14	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	30	70	10	30	70	ps/pF
Δt_{PHL}				10	30	60	20	30	60	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	30	70	10	30	70	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	30	70	20	30	60	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI20LJ 2-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI20LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist.

Label: OPI20LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −2 mA				3.7			V
		I_{OH} = −1.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 2 mA						0.5	V
		I_{OL} = 1.6 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.53			0.06	mA
C_i	Input capacitance			0.09			0.09		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		8.22			8.22		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.26	3.13	6.93	1.33	3.13	6.35	ns
t_{PHL}				3.04	6.96	14.1	3.26	6.96	12.78	
t_{PLH}	A	Y	C_L = 50 pF	2.2	6.03	13.67	2.33	6.03	12.54	ns
t_{PHL}				6.84	14.83	27.05	7.37	14.83	24.98	
Δt_{PLH}	A	Y		30	80	190	30	80	180	ps/pF
Δt_{PHL}				110	220	370	120	220	350	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	2.03	4.94	10.3	2.16	4.94	9.44	ns
t_{PHL}				0.22	5.25	11.03	2.38	5.25	10.01	
t_{PLH}	A	Y	C_L = 50 pF	4.32	10.74	22.34	4.6	10.74	20.51	ns
t_{PHL}				4.64	10.43	19.27	5	10.43	17.97	
Δt_{PLH}	A	Y		70	170	340	70	170	320	ps/pF
Δt_{PHL}				70	150	240	70	150	230	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI21LJ
2-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI21LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI21LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA						0.5	V
		I_{OL} = 1.6 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.28			0.05	mA
C_i	Input capacitance			0.04			0.04		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		0.37			0.37		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.87	7	15.69	3.09	7	13.84	ns
t_{PZL}			C_L = 50 pF	6.87	16.01	35.21	7.43	16.01	30.84	
t_{PLZ}	A	Y			13.05			13.05		ns
Δt_{PZL}	A	Y		110	260	560	120	260	490	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.04	5	11.11	2.19	5	9.94	ns
t_{PZL}			C_L = 50 pF	4.54	10.61	23.01	4.89	10.61	20.47	
Δt_{PZL}	A	Y		70	160	340	80	160	300	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI23LJ
2-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

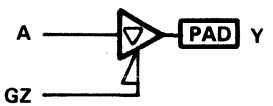
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPI23LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI23LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −2 mA				3.7			V
			I_{OH} = −1.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 2 mA						0.5	V
			I_{OL} = 1.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		11.8			11.8		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI23LJ
2-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.38	3.83	8.73	1.46	3.83	7.98	ns
t_{PHL}				3.45	8.19	16.83	3.73	8.19	15.23	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.38	4.18	9.91	1.47	4.18	9.04	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.56	8.96	20.14	3.85	8.96	17.8	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.32	6.73	15.47	2.47	6.73	14.18	ns
t_{PHL}				7.27	16.1	31.84	7.85	16.1	28.74	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.33	7.21	17.36	2.48	7.21	15.82	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	7.57	17.99	39.8	8.2	17.99	34.91	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		15.55			15.55		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		12.21			12.21		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	30	80	190	30	80	180	ps/pF
Δt_{PHL}				110	230	430	120	230	390	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	30	90	210	30	90	190	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	110	260	560	120	260	490	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.26	5.87	12.51	2.41	5.87	11.47	ns
t_{PHL}				2.52	6.25	13.34	2.71	6.25	12.09	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.4	6.52	14.97	2.55	6.52	13.53	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.55	6.52	14.56	2.75	6.52	13.04	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	4.55	11.67	24.55	4.86	11.67	22.53	ns
t_{PHL}				4.95	11.46	23.61	5.33	11.46	21.33	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	4.73	12.92	29.69	5.04	12.92	26.8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.04	12.15	26.53	5.45	12.15	23.64	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	70	170	340	70	170	320	ps/pF
Δt_{PHL}				70	150	290	70	150	260	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	70	180	420	70	180	380	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	70	160	340	80	160	300	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI40LJ 4-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI40LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist.

Label: OPI40LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −4 mA				3.7			V
		I_{OH} = −3.4 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 4 mA						0.5	V
		I_{OL} = 3.4 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			1.05			0.13	mA
C_i	Input capacitance			0.17			0.17		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		9.72			9.72		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	0.91	2.09	4.48	0.96	2.09	4.09	ns
t_{PHL}				1.74	4.07	8.3	1.86	4.07	7.54	
t_{PLH}	A	Y	C_L = 50 pF	1.38	3.55	7.87	1.46	3.55	7.21	ns
t_{PHL}				3.64	8.02	15.8	3.91	8.02	14.3	
Δt_{PLH}	A	Y		10	40	100	10	40	90	ps/pF
Δt_{PHL}				50	110	210	60	110	190	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.29	3.01	6.23	1.36	3.01	5.71	ns
t_{PHL}				1.35	3.18	6.67	1.43	3.18	6.06	
t_{PLH}	A	Y	C_L = 50 pF	2.42	5.9	12.24	2.57	5.9	11.23	ns
t_{PHL}				2.56	5.81	11.87	2.74	5.81	10.75	
Δt_{PLH}	A	Y		30	80	170	30	80	160	ps/pF
Δt_{PHL}				30	80	150	40	80	130	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI41LJ
4-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI41LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI41LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA						0.5	V
		I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.55			0.09	mA
C_i	Input capacitance			0.07			0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		0.62			0.62		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.6	3.86	8.2	1.72	3.86	7.37	ns
t_{PZL}			C_L = 50 pF	3.55	8.07	16.62	3.83	8.07	14.86	
t_{PLZ}	A	Y			9.77			9.77		ns
Δt_{PZL}	A	Y		60	120	240	60	120	210	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.22	2.93	6.3	1.3	2.93	5.69	ns
t_{PZL}			C_L = 50 pF	2.46	5.67	11.9	2.64	5.67	10.7	
Δt_{PZL}	A	Y		40	80	160	40	80	140	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI43LJ
4-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

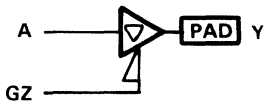
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPI43LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI43LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −4 mA				3.7			V
			I_{OH} = −3.4 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 4 mA						0.5	V
			I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		13.2			13.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.01	2.75	6.2	1.07	2.75	5.66	ns
t_{PHL}				2.03	4.98	10.4	2.18	4.98	9.43	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.02	3.02	6.99	1.08	3.02	6.38	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.03	5.11	10.93	2.19	5.11	9.83	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.48	4.21	9.59	1.57	4.21	8.78	ns
t_{PHL}				3.94	8.94	17.91	4.24	8.94	16.19	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.5	4.52	10.54	1.6	4.52	9.64	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.99	9.32	19.36	4.3	9.32	17.32	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		11.56			11.56		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.97			9.97		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	40	100	10	40	90	ps/pF
Δt_{PHL}				50	110	210	60	110	190	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	40	100	10	40	90	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	60	120	240	60	120	210	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.44	3.79	8.16	1.53	3.79	7.47	ns
t_{PHL}				1.58	3.98	8.56	1.69	3.98	7.77	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.56	4.14	9.14	1.66	4.14	8.32	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.56	3.99	8.67	1.67	3.99	7.84	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.57	6.68	14.16	2.74	6.68	12.99	ns
t_{PHL}				2.79	6.61	13.77	3	6.61	12.45	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.72	7.17	15.71	2.89	7.17	14.32	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.8	6.72	14.25	3.01	6.72	12.83	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	30	80	170	30	80	160	ps/pF
Δt_{PHL}				30	80	150	40	80	130	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	30	90	190	40	90	170	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	40	80	160	40	80	140	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI60LJ 6-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI60LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist.

Label: OPI60LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −6 mA				3.7			V
		I_{OH} = −5.1 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 6 mA						0.5	V
		I_{OL} = 5.1 mA			0.5				
I_{CC}	Supply current	V_I = V_{IH} or V_{IL}			1.58			0.19	mA
C_i	Input capacitance			0.24			0.24		pF
C_{pd}	Equivalent power dissipation capacitance	t_r = t_f = 1 ns		11.6			11.6		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	0.8	1.75	3.69	0.83	1.75	3.37	ns
t_{PHL}				1.31	3.08	6.33	1.4	3.08	5.76	
t_{PLH}	A	Y	C_L = 50 pF	1.12	2.74	6.01	1.17	2.74	5.5	ns
t_{PHL}				2.56	5.74	11.41	2.75	5.74	10.33	
Δt_{PLH}	A	Y		10	30	70	10	30	60	ps/pF
Δt_{PHL}				40	80	150	40	80	130	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.04	2.39	4.93	1.1	2.39	4.52	ns
t_{PHL}				1.04	2.46	5.17	1.11	2.46	4.7	
t_{PLH}	A	Y	C_L = 50 pF	1.79	4.32	8.96	1.9	4.32	8.22	ns
t_{PHL}				1.86	4.25	8.74	1.99	4.25	7.92	
Δt_{PLH}	A	Y		20	60	120	20	60	110	ps/pF
Δt_{PHL}				20	50	100	30	50	90	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI61LJ
6-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFER

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPI61LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI61LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 6 mA						0.5	V
		I_{OL} = 5.1 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.83			0.14	mA
C_i	Input capacitance			0.09			0.09		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		0.86			0.86		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.18	2.86	6.02	1.27	2.86	5.44	ns
t_{PZL}			C_L = 50 pF	2.47	5.64	11.49	2.66	5.64	10.34	
t_{PLZ}	A	Y			9.42			9.42		ns
Δt_{PZL}	A	Y		40	80	160	40	80	140	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	0.93	2.23	4.76	0.99	2.23	4.31	ns
t_{PZL}			C_L = 50 pF	1.77	4.08	8.53	1.89	4.08	7.7	
Δt_{PZL}	A	Y		20	50	110	30	50	100	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI63LJ
6-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

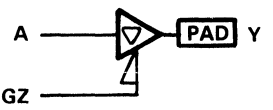
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPI63LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPI63LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −6 mA				3.7			V
			I_{OH} = −5.1 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 6 mA						0.5	V
			I_{OL} = 5.1 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}		1.04			0.27		mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		14.5			14.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPI63LJ
6-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH ACTIVE-LOW ENABLE

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.91	2.46	5.55	0.96	2.46	5.07	ns
t_{PHL}				1.56	3.91	8.27	1.67	3.91	7.51	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	0.91	2.72	6.28	0.96	2.72	5.74	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.54	3.92	8.35	1.65	3.92	7.55	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.22	3.45	7.88	1.3	3.45	7.2	ns
t_{PHL}				2.83	6.57	13.33	3.05	6.57	12.07	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.24	3.73	8.68	1.32	3.73	7.94	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.84	6.69	13.81	3.06	6.69	12.43	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		10.03			10.03		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.31			9.31		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	30	70	10	30	60	ps/pF
Δt_{PHL}				40	80	140	40	80	130	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	30	70	10	30	60	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	40	80	160	40	80	140	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.18	3.18	6.93	1.26	3.18	6.34	ns
t_{PHL}				1.27	3.22	6.97	1.35	3.22	6.33	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.3	3.47	7.69	1.38	3.47	7.01	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.24	3.16	6.86	1.32	3.16	6.22	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.94	5.11	10.96	2.07	5.11	10.04	ns
t_{PHL}				2.08	5	10.53	2.23	5	9.54	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.07	5.47	11.96	2.2	5.47	10.92	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.07	5.01	10.6	2.22	5.01	9.58	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	60	120	20	60	110	ps/pF
Δt_{PHL}				20	50	100	30	50	90	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	60	120	20	60	110	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	20	50	110	30	50	100	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJA0LJ
16-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPJA0LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJA0LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −16 mA				3.7			V
		I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 16 mA						0.5	V
		I_{OL} = 13.6 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			3.42			0.35	mA
C_i	Input capacitance			0.53			0.53		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		13.3			13.3		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	0.95	2.6	5.94	1.01	2.6	5.4	ns
t_{PHL}				1.31	3.48	7.48	1.4	3.48	6.83	
t_{PLH}	A	Y	C_L = 50 pF	1.22	3.32	7.55	1.3	3.32	6.86	ns
t_{PHL}				1.97	4.91	10.28	2.12	4.91	9.35	
Δt_{PLH}	A	Y		10	20	50	10	20	40	ps/pF
Δt_{PHL}				20	40	80	20	40	70	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.16	3.12	6.91	1.24	3.12	6.29	ns
t_{PHL}				1.13	3.04	6.67	1.21	3.04	6.08	
t_{PLH}	A	Y	C_L = 50 pF	1.6	4.2	9.17	1.71	4.2	8.34	ns
t_{PHL}				1.62	4.14	8.87	1.74	4.14	8.08	
Δt_{PLH}	A	Y		10	30	60	10	30	60	ps/pF
Δt_{PHL}				10	30	60	20	30	60	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJA1LJ
16-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPJA1LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJA1LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA						0.5	V
		I_{OL} = 13.6 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			1.38			0.35	mA
C_i	Input capacitance			0.19			0.19		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		1.96			1.96		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.21	3.28	7.19	1.29	3.28	6.53	ns
t_{PZL}			C_L = 50 pF	1.86	4.71	10	2	4.71	9.07	
t_{PLZ}	A	Y			7.53			7.53		ns
Δt_{PZL}	A	Y		20	40	80	20	40	70	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.03	2.84	6.34	1.1	2.84	5.77	ns
t_{PZL}			C_L = 50 pF	1.53	3.94	8.56	1.63	3.94	7.77	
Δt_{PZL}	A	Y		10	30	60	20	30	60	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJA3LJ
16-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt AND ACTIVE-LOW ENABLE

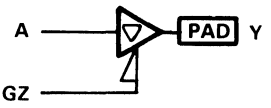
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPJA3LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJA3LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 16 mA						0.5	V
			I_{OL} = 13.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.3			17.3		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.28	3.62	8.22	1.35	3.62	7.5	ns
t_{PHL}				1.69	4.44	9.63	1.81	4.44	8.77	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.31	3.9	8.99	1.39	3.9	8.21	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.69	4.44	9.58	1.82	4.44	8.72	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.53	4.31	9.78	1.63	4.31	8.91	ns
t_{PHL}				2.33	5.83	12.34	2.51	5.83	11.22	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.57	4.59	10.55	1.67	4.59	9.62	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.34	5.84	12.32	2.51	5.84	11.19	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.24			9.24		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.04			9.04		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	20	40	10	20	40	ps/pF
Δt_{PHL}				20	40	80	20	40	70	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	20	40	10	20	40	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	20	40	80	20	40	70	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJA3LJ
16-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.5	4.17	9.26	1.6	4.17	8.45	ns
t_{PHL}				1.48	3.96	8.75	1.59	3.96	7.96	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.65	4.47	9.98	1.76	4.47	9.09	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.48	3.94	8.63	1.59	3.94	7.86	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.93	5.21	11.45	2.06	5.21	10.44	ns
t_{PHL}				1.97	5.03	10.89	2.11	5.03	9.9	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.08	5.52	12.18	2.21	5.52	11.09	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.97	5.01	10.78	2.1	5.01	9.8	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	30	60	10	30	60	ps/pF
Δt_{PHL}				10	30	60	10	30	60	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	30	60	10	30	60	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	30	60	10	30	60	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJB0LJ
24-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPJB0LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJB0LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −16 mA				3.7			V
		I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 24 mA						0.5	V
		I_{OL} = 20.4 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			3.42			0.5	mA
C_i	Input capacitance			0.63			0.63		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		14.8			14.8		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	0.95	2.6	5.93	1	2.6	5.39	ns
t_{PHL}				1.42	3.77	8.08	1.52	3.77	7.39	
t_{PLH}	A	Y	C_L = 50 pF	1.22	3.32	7.54	1.29	3.32	6.85	ns
t_{PHL}				1.99	5.02	10.51	2.14	5.02	9.58	
Δt_{PLH}	A	Y		10	20	50	10	20	40	ps/pF
Δt_{PHL}				20	40	70	20	40	60	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.16	3.11	6.9	1.23	3.11	6.28	ns
t_{PHL}				1.24	3.35	7.31	1.33	3.35	6.68	
t_{PLH}	A	Y	C_L = 50 pF	1.59	4.19	9.16	1.7	4.19	8.33	ns
t_{PHL}				1.68	4.34	9.29	1.8	4.34	8.47	
Δt_{PLH}	A	Y		10	30	60	10	30	60	ps/pF
Δt_{PHL}				10	30	60	10	30	50	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJB1LJ
24-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPJB1LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJB1LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 24 mA						0.5	V
		I_{OL} = 20.4 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			1.92			0.5	mA
C_i	Input capacitance			0.27			0.27		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		3.2			3.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.26	3.45	7.59	1.35	3.45	6.9	ns
t_{PZL}			C_L = 50 pF	1.81	4.66	9.95	1.94	4.66	9.04	
t_{PLZ}	A	Y			6.55			6.55		ns
Δt_{PZL}	A	Y		20	30	70	20	30	60	ps/pF

CMOS loads, R_L = 1 k to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.09	3.05	6.81	1.17	3.05	6.2	ns
t_{PZL}			C_L = 50 pF	1.52	4.01	8.74	1.63	4.01	7.94	
Δt_{PZL}	A	Y		10	30	60	10	30	50	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJB3LJ
24-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt AND ACTIVE-LOW ENABLE

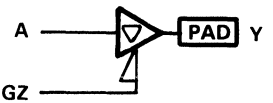
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPJB3LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJB3LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 24 mA						0.5	V
			I_{OL} = 20.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		19.2			19.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPJB3LJ
24-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.27	3.62	8.24	1.35	3.62	7.52	ns
t_{PHL}				1.84	4.83	10.48	1.97	4.83	9.55	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.31	3.91	9.02	1.4	3.91	8.23	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.87	4.88	10.51	2	4.88	9.57	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.53	4.31	9.8	1.63	4.31	8.93	ns
t_{PHL}				2.4	6.04	12.83	2.58	6.04	11.68	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.58	4.61	10.58	1.68	4.61	9.65	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.43	6.09	12.86	2.61	6.09	11.7	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.25			9.25		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.01			8.01		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	20	40	10	20	40	ps/pF
Δt_{PHL}				20	30	70	20	30	60	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	20	40	10	20	40	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	20	30	70	20	30	60	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.5	4.17	9.27	1.6	4.17	8.46	ns
t_{PHL}				1.64	4.38	9.65	1.76	4.38	8.79	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.66	4.48	10	1.77	4.48	9.11	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.66	4.4	9.62	1.78	4.4	8.76	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.93	5.22	11.47	2.06	5.22	10.46	ns
t_{PHL}				2.08	5.34	11.56	2.22	5.34	10.52	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.08	5.53	12.21	2.22	5.53	11.12	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.1	5.36	11.53	2.24	5.36	10.49	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	30	60	10	30	60	ps/pF
Δt_{PHL}				10	30	50	10	30	50	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	30	60	10	30	60	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	30	50	10	30	50	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJE0LJ
48-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPJE0LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJE0LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −16 mA				3.7			V
		I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 48 mA						0.5	V
		I_{OL} = 40.8 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			3.84			1	mA
C_i	Input capacitance			0.92			0.92		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		21.4			21.4		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	0.98	2.69	6.14	1.04	2.69	5.58	ns
t_{PHL}				1.2	3.35	7.29	1.29	3.35	6.66	
t_{PLH}	A	Y	C_L = 50 pF	1.24	3.38	7.7	1.32	3.38	7	ns
t_{PHL}				1.56	4.15	8.87	1.67	4.15	8.09	
Δt_{PLH}	A	Y		10	20	40	10	20	40	ps/pF
Δt_{PHL}				10	20	50	10	20	40	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.2	3.24	7.16	1.28	3.24	6.52	ns
t_{PHL}				1.07	3.02	6.68	1.14	3.02	6.1	
t_{PLH}	A	Y	C_L = 50 pF	1.63	4.28	9.36	1.74	4.28	8.51	ns
t_{PHL}				1.35	3.67	8	1.45	3.67	7.3	
Δt_{PLH}	A	Y		10	30	60	10	30	60	ps/pF
Δt_{PHL}				10	20	40	10	20	30	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJE1LJ
48-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT	OUTPUT
A	Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPJE1LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJE1LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 48 mA						0.5	V
		I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			3.84			1	mA
C_i	Input capacitance			0.55			0.55		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		6.61			6.61		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.12	3.26	7.26	1.21	3.26	6.6	ns
t_{PZL}			C_L = 50 pF	1.5	4.09	8.91	1.61	4.09	8.09	
t_{PLZ}	A	Y			6.96			6.96		ns
Δt_{PZL}	A	Y		10	20	50	10	20	40	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1	2.94	6.65	1.08	2.94	6.05	ns
t_{PZL}			C_L = 50 pF	1.3	3.62	8.04	1.4	3.62	7.3	
Δt_{PZL}	A	Y		10	20	40	10	20	40	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJE3LJ
48-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt AND ACTIVE-LOW ENABLE

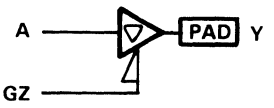
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPJE3LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJE3LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 48 mA						0.5	V
			I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		24.3			24.3		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.3	3.68	8.37	1.38	3.68	7.64	ns
t_{PHL}				1.68	4.53	10.03	1.8	4.53	9.13	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.33	3.96	9.15	1.42	3.96	8.34	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.71	4.58	10.03	1.83	4.58	9.14	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.55	4.36	9.92	1.65	4.36	9.04	ns
t_{PHL}				2.03	5.32	11.59	2.18	5.32	10.54	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.59	4.65	10.69	1.69	4.65	9.74	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.06	5.37	11.58	2.21	5.37	10.54	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.37			9.37		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.95			8.95		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	20	40	10	20	40	ps/pF
Δt_{PHL}				10	20	40	10	20	40	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	20	40	10	20	40	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	20	40	10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJE3LJ
48-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.53	4.24	9.42	1.63	4.24	8.6	ns
t_{PHL}				1.54	4.19	9.4	1.64	4.19	8.55	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.68	4.55	10.15	1.79	4.55	9.25	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.56	4.23	9.37	1.67	4.23	8.53	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.95	5.28	11.6	2.08	5.28	10.58	ns
t_{PHL}				1.82	4.83	10.7	1.94	4.83	9.73	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.1	5.59	12.34	2.24	5.59	11.23	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.85	4.87	10.66	1.97	4.87	9.7	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	30	60	10	30	60	ps/pF
Δt_{PHL}				10	20	40	10	20	30	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	30	60	10	30	60	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	20	40	10	20	30	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJG0LJ 64-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030. APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPJG0LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJG0LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −16 mA				3.7			V
		I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 64 mA						0.5	V
		I_{OL} = 54.4 mA			0.5				
I_{CC}	Supply current	V_I = V_{IH} or V_{IL}			5.13			1.34	mA
C_i	Input capacitance			1.1			1.1		pF
C_{pd}	Equivalent power dissipation capacitance	t_r = t_f = 1 ns		24.2			24.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	0.99	2.73	6.23	1.05	2.73	5.67	ns
t_{PHL}				1.11	3.18	6.97	1.19	3.18	6.37	
t_{PLH}	A	Y	C_L = 50 pF	1.25	3.42	7.77	1.33	3.42	7.07	ns
t_{PHL}				1.4	3.84	8.29	1.51	3.84	7.56	
Δt_{PLH}	A	Y		10	20	40	10	20	40	ps/pF
Δt_{PHL}				10	20	40	10	20	30	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.22	3.28	7.26	1.3	3.28	6.61	ns
t_{PHL}				1	2.88	6.42	1.07	2.88	5.86	
t_{PLH}	A	Y	C_L = 50 pF	1.64	4.32	9.44	1.75	4.32	8.59	ns
t_{PHL}				1.23	3.42	7.52	1.32	3.42	6.85	
Δt_{PLH}	A	Y		10	30	60	10	30	60	ps/pF
Δt_{PHL}				10	20	30	10	20	30	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJG1LJ
64-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPJG1LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJG1LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 64 mA						0.5	V
		I_{OL} = 54.4 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			5.13			1.34	mA
C_i	Input capacitance			0.71			0.71		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		8.63			8.63		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJG1LJ
64-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.08	3.19	7.15	1.17	3.19	6.51	ns
t_{PZL}			C_L = 50 pF	1.38	3.88	8.53	1.49	3.88	7.75	
t_{PLZ}	A	Y			7.35			7.35		ns
Δt_{PZL}	A	Y		10	20	40	10	20	40	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	0.97	2.89	6.59	1.04	2.89	5.99	ns
t_{PZL}			C_L = 50 pF	1.21	3.47	7.75	1.3	3.47	7.04	
Δt_{PZL}	A	Y		10	20	30	10	20	30	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPJG3LJ
64-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt AND ACTIVE-LOW ENABLE

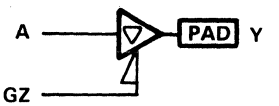
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPJG3LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJG3LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.4 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 64 mA						0.5	V
			I_{OL} = 54.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		27			27		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJG3LJ
64-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.33	3.73	8.5	1.41	3.73	7.75	ns
t_{PHL}				1.64	4.48	9.98	1.76	4.48	9.08	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.34	4	9.23	1.43	4	8.42	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.67	4.52	9.96	1.79	4.52	9.07	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.57	4.41	10.02	1.67	4.41	9.13	ns
t_{PHL}				1.92	5.13	11.29	2.06	5.13	10.26	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.6	4.68	10.75	1.7	4.68	9.8	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.96	5.17	11.26	2.1	5.17	10.25	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.45			9.45		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.43			9.43		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	20	40	10	20	40	ps/pF
Δt_{PHL}				10	20	40	10	20	30	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	20	40	10	20	40	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	20	40	10	20	30	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.55	4.3	9.55	1.66	4.3	8.72	ns
t_{PHL}				1.51	4.16	9.41	1.62	4.16	8.55	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.7	4.59	10.25	1.81	4.59	9.33	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.54	4.19	9.35	1.64	4.19	8.51	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.97	5.33	11.71	2.11	5.33	10.68	ns
t_{PHL}				1.74	4.7	10.51	1.86	4.7	9.55	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.11	5.62	12.41	2.25	5.62	11.3	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.77	4.73	10.46	1.89	4.73	9.51	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	30	60	10	30	60	ps/pF
Δt_{PHL}				10	20	30	10	20	30	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	30	60	10	30	60	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	20	30	10	20	30	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJ00LJ
10-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPJ00LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJ00LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −10 mA				3.7			V
		I_{OH} = −8.5 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 10 mA						0.5	V
		I_{OL} = 8.5 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			2.15			0.22	mA
C_i	Input capacitance			0.35			0.35		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		10.8			10.8		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.05	2.82	6.4	1.11	2.82	5.82	ns
t_{PHL}				1.64	4.19	8.88	1.76	4.19	8.1	
t_{PLH}	A	Y	C_L = 50 pF	1.4	3.75	8.5	1.48	3.75	7.73	ns
t_{PHL}				2.58	6.21	12.79	2.77	6.21	11.63	
Δt_{PLH}	A	Y		10	30	60	10	30	50	ps/pF
Δt_{PHL}				30	60	110	30	60	100	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.32	3.47	7.62	1.41	3.47	6.94	ns
t_{PHL}				1.39	3.61	7.82	1.48	3.61	7.13	
t_{PLH}	A	Y	C_L = 50 pF	1.92	4.94	10.7	2.05	4.94	9.74	ns
t_{PHL}				2.07	5.12	10.84	2.22	5.12	9.85	
Δt_{PLH}	A	Y		20	40	90	20	40	80	ps/pF
Δt_{PHL}				20	40	90	20	40	80	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJ01LJ
10-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPJ01LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJ01LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 10 mA						0.5	V
		I_{OL} = 8.5 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.85			0.22	mA
C_i	Input capacitance			0.13			0.13		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		1.26			1.26		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.51	3.96	8.57	1.62	3.96	7.78	ns
t_{PZL}			C_L = 50 pF	2.45	5.98	12.54	2.63	5.98	11.36	
t_{PLZ}	A	Y			7.8			7.8		ns
Δt_{PZL}	A	Y		30	60	110	30	60	100	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.27	3.37	7.45	1.36	3.37	6.76	ns
t_{PZL}			C_L = 50 pF	1.95	4.88	10.49	2.09	4.88	9.51	
Δt_{PZL}	A	Y		20	40	90	20	40	80	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJ03LJ
10-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt AND ACTIVE-LOW ENABLE

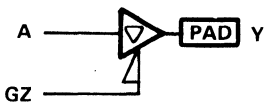
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPJ03LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJ03LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −10 mA				3.7			V
			I_{OH} = −8.5 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 10 mA						0.5	V
			I_{OL} = 8.5 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		14.9			14.9		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.32	3.69	8.39	1.4	3.69	7.65	ns
t_{PHL}				2.02	5.17	11.02	2.16	5.17	10.04	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.35	3.98	9.19	1.44	3.98	8.37	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.03	5.19	11.08	2.17	5.19	10.07	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.65	4.6	10.43	1.76	4.6	9.5	ns
t_{PHL}				2.95	7.14	14.83	3.16	7.14	13.48	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.69	4.89	11.24	1.8	4.89	10.24	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.95	7.19	14.98	3.17	7.19	13.58	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.7			9.7		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.51			8.51		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	30	60	10	30	50	ps/pF
Δt_{PHL}				30	60	110	30	60	100	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	30	60	10	30	50	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	30	60	110	30	60	100	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJ03LJ
10-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.61	4.39	9.69	1.72	4.39	8.84	ns
t_{PHL}				1.74	4.53	9.86	1.86	4.53	8.98	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.77	4.71	10.48	1.88	4.71	9.53	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	1.73	4.52	9.8	1.85	4.52	8.91	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.2	5.83	12.7	2.35	5.83	11.58	ns
t_{PHL}				2.41	6	12.8	2.58	6	11.63	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.35	6.16	13.54	2.51	6.16	12.32	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.41	6	12.77	2.58	6	11.59	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	40	90	20	40	80	ps/pF
Δt_{PHL}				20	40	80	20	40	80	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	40	90	20	40	80	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	20	40	80	20	40	80	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJ20LJ
2-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPJ20LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJ20LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −2 mA				3.7			V
		I_{OH} = −1.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 2 mA						0.5	V
		I_{OL} = 1.6 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.43			0.05	mA
C_i	Input capacitance			0.09			0.09		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		7.68			7.68		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.98	5.28	11.98	2.11	5.28	10.9	ns
t_{PHL}				4.73	11	22.41	5.08	11	20.41	
t_{PLH}	A	Y	C_L = 50 pF	3.06	8.41	19.14	3.27	8.41	17.46	ns
t_{PHL}				8.65	19.15	34.92	9.32	19.15	32.5	
Δt_{PLH}	A	Y		30	90	200	30	90	190	ps/pF
Δt_{PHL}				110	230	360	120	230	350	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	2.89	7.3	15.69	3.08	7.3	14.3	ns
t_{PHL}				3.77	9.03	18.88	4.03	9.03	17.22	
t_{PLH}	A	Y	C_L = 50 pF	5.23	13.2	27.94	5.59	13.2	25.54	ns
t_{PHL}				6.4	14.64	26.87	6.88	14.64	25.25	
Δt_{PLH}	A	Y		70	170	350	70	170	320	ps/pF
Δt_{PHL}				80	160	230	80	160	230	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJ21LJ
2-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPJ21LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJ21LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA						0.5	V
		I_{OL} = 1.6 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.17			0.04	mA
C_i	Input capacitance			0.04			0.04		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		0.35			0.35		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	4.37	10.81	24.06	4.71	10.81	21.41	ns
t_{PZL}			C_L = 50 pF	8.44	19.93	43.58	9.11	19.93	38.49	
t_{PLZ}	A	Y			12.79			12.79		ns
Δt_{PZL}	A	Y		120	260	560	130	260	490	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	3.4	8.49	18.8	3.65	8.49	16.92	ns
t_{PZL}			C_L = 50 pF	6.06	14.44	31.2	6.52	14.44	27.95	
Δt_{PZL}	A	Y		80	170	350	80	170	320	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJ23LJ
2-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt AND ACTIVE-LOW ENABLE

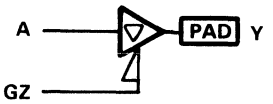
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPJ23LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJ23LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −2 mA				3.7			V
			I_{OH} = −1.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 2 mA						0.5	V
			I_{OL} = 1.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		11.4			11.4		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPJ23LJ
2-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.23	6.1	13.87	2.38	6.1	12.63	ns
t_{PHL}				5.3	12.39	25.41	5.7	12.39	23.09	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.27	6.52	15.33	2.43	6.52	13.91	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.46	13.42	29.71	5.89	13.42	26.45	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	3.29	9.19	20.94	3.52	9.19	19.12	ns
t_{PHL}				9.2	20.54	40.94	9.91	20.54	37.08	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.33	9.72	22.98	3.56	9.72	20.88	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	9.52	22.56	49.4	10.29	22.56	43.66	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		15.37			15.37		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		11.95			11.95		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	30	90	200	30	90	190	ps/pF
Δt_{PHL}				110	230	440	120	230	400	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	30	90	220	30	90	200	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	120	260	560	130	260	490	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	3.24	8.33	17.96	3.46	8.33	16.39	ns
t_{PHL}				4.22	10.19	21.49	4.53	10.19	19.55	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.42	9.09	20.8	3.65	9.09	18.76	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.29	10.65	23.41	4.61	10.65	21.07	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	5.58	14.21	30.16	5.96	14.21	27.58	ns
t_{PHL}				6.82	15.79	32.53	7.33	15.79	29.5	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	5.77	15.51	35.47	6.17	15.51	32	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	6.95	16.59	35.86	7.48	16.59	32.14	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	70	170	350	70	170	320	ps/pF
Δt_{PHL}				70	160	320	80	160	280	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	70	180	420	70	180	380	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	80	170	360	80	170	320	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPJ40LJ
4-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPJ40LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJ40LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −4 mA				3.7			V
		I_{OH} = −3.4 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 4 mA						0.5	V
		I_{OL} = 3.4 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.87			0.09	mA
C_i	Input capacitance			0.17			0.17		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		8.5			8.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.42	3.78	8.54	1.51	3.78	7.77	ns
t_{PHL}				2.83	6.81	14.05	3.04	6.81	12.8	
t_{PLH}	A	Y	C_L = 50 pF	2.05	5.53	12.52	2.18	5.53	11.4	ns
t_{PHL}				4.88	11.11	22.24	5.24	11.11	20.19	
Δt_{PLH}	A	Y		20	50	110	20	50	100	ps/pF
Δt_{PHL}				60	120	230	60	120	210	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.94	4.95	10.7	2.07	4.95	9.74	ns
t_{PHL}				2.31	5.7	12.06	2.47	5.7	10.99	
t_{PLH}	A	Y	C_L = 50 pF	3.17	8.03	17.11	3.38	8.03	15.61	ns
t_{PHL}				3.72	8.76	18.06	3.99	8.76	16.42	
Δt_{PLH}	A	Y		40	90	180	40	90	170	ps/pF
Δt_{PHL}				40	90	170	40	90	160	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJ41LJ
4-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPJ41LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJ41LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA						0.5	V
		I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.35			0.09	mA
C_i	Input capacitance			0.07			0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		0.58			0.58		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.6	6.48	13.94	2.8	6.48	12.56	ns
t_{PZL}			C_L = 50 pF	4.67	10.95	22.86	5.03	10.95	20.53	
t_{PLz}	A	Y			9.51			9.51		ns
Δt_{PZL}	A	Y		60	130	250	60	130	230	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.1	5.31	11.6	2.25	5.31	10.49	ns
t_{PZL}			C_L = 50 pF	3.51	8.42	17.89	3.77	8.42	16.15	
Δt_{PZL}	A	Y		40	90	180	40	90	160	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJ43LJ
4-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt AND ACTIVE-LOW ENABLE

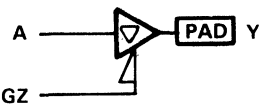
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPJ43LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJ43LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −4 mA				3.7			V
			I_{OH} = −3.4 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 4 mA						0.5	V
			I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		12.4			12.4		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.65	4.54	10.29	1.76	4.54	9.37	ns
t_{PHL}				3.27	7.91	16.42	3.51	7.91	14.93	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.7	4.87	11.26	1.81	4.87	10.24	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.31	8.15	17.36	3.56	8.15	15.68	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.26	6.26	14.18	2.41	6.26	12.93	ns
t_{PHL}				5.29	12.16	24.55	5.7	12.16	22.26	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.31	6.61	15.28	2.46	6.61	13.89	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.37	12.61	26.24	5.79	12.61	23.6	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		11.4			11.4		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.73			9.73		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	50	110	20	50	100	ps/pF
Δt_{PHL}				60	120	230	60	120	210	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	50	110	20	50	100	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	60	130	250	60	130	230	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJ43LJ
4-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.21	5.81	12.63	2.37	5.81	11.52	ns
t_{PHL}				2.69	6.68	14.23	2.88	6.68	12.94	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.39	6.23	13.86	2.55	6.23	12.57	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.7	6.78	14.63	2.9	6.78	13.26	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	3.43	8.86	18.97	3.67	8.86	17.32	ns
t_{PHL}				4.08	9.69	20.17	4.38	9.69	18.3	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.61	9.4	20.69	3.85	9.4	18.78	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.11	9.86	20.85	4.41	9.86	18.85	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	30	90	180	40	90	170	ps/pF
Δt_{PHL}				40	90	170	40	90	150	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	30	90	200	40	90	180	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	40	90	180	40	90	160	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJ60LJ
6-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPJ60LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJ60LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −6 mA				3.7			V
		I_{OH} = −5.1 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 6 mA						0.5	V
		I_{OL} = 5.1 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			1.29			0.13	mA
C_i	Input capacitance			0.24			0.24		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		9.3			9.3		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPJ60LJ
6-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.24	3.28	7.43	1.31	3.28	6.76	ns
t_{PHL}				2.18	5.39	11.24	2.34	5.39	10.24	
t_{PLH}	A	Y	C_L = 50 pF	1.71	4.59	10.4	1.82	4.59	9.46	ns
t_{PHL}				3.62	8.41	17.06	3.89	8.41	15.49	
Δt_{PLH}	A	Y		10	40	80	10	40	80	ps/pF
Δt_{PHL}				40	90	170	40	90	150	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.62	4.17	9.08	1.73	4.17	8.27	ns
t_{PHL}				1.81	4.57	9.75	1.94	4.57	8.89	
t_{PLH}	A	Y	C_L = 50 pF	2.49	6.35	13.65	2.66	6.35	12.44	ns
t_{PHL}				2.82	6.77	14.12	3.02	6.77	12.83	
Δt_{PLH}	A	Y		30	60	130	30	60	120	ps/pF
Δt_{PHL}				30	60	120	30	60	110	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJ61LJ
6-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPJ61LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJ61LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 6 mA						0.5	V
		I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.52			0.13	mA
C_i	Input capacitance			0.09			0.09		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		0.82			0.82		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPJ61LJ
6-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.01	5.09	10.94	2.16	5.09	9.9	ns
t_{PZL}			C_L = 50 pF	3.45	8.18	17.03	3.71	8.18	15.37	
t_{PLZ}	A	Y			9.19			9.19		ns
Δt_{PZL}	A	Y		40	90	170	40	90	160	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.65	4.25	9.31	1.77	4.25	8.44	ns
t_{PZL}			C_L = 50 pF	2.66	6.47	13.78	2.86	6.47	12.47	
Δt_{PZL}	A	Y		30	60	130	30	60	120	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJ63LJ
6-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt AND ACTIVE-LOW ENABLE

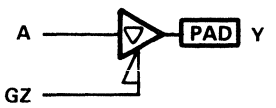
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPJ63LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPJ63LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −6 mA				3.7			V
			I_{OH} = −5.1 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 6 mA						0.5	V
			I_{OL} = 5.1 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		13.2			13.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPJ63LJ
6-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.5 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.47	4.08	9.27	1.56	4.08	8.44	ns
t_{PHL}				2.58	6.38	13.39	2.77	6.38	12.19	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.51	4.38	10.14	1.62	4.38	9.22	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.59	6.49	13.78	2.79	6.49	12.48	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.93	5.35	12.16	2.06	5.35	11.07	ns
t_{PHL}				3.99	9.37	19.12	4.29	9.37	17.35	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.97	5.67	13.06	2.11	5.67	11.89	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.02	9.55	19.79	4.33	9.55	17.88	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.88			9.88		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.07			9.07		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	40	80	10	40	80	ps/pF
Δt_{PHL}				40	90	160	40	90	150	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	40	80	10	40	80	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	40	90	170	40	90	150	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.89	5.04	11.04	2.02	5.04	10.07	ns
t_{PHL}				2.16	5.48	11.77	2.32	5.48	10.72	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.05	5.4	12	2.19	5.4	10.89	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.16	5.51	11.89	2.32	5.51	10.8	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.75	7.19	15.54	2.94	7.19	14.17	ns
t_{PHL}				3.16	7.64	16.05	3.39	7.64	14.58	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.92	7.59	16.66	3.12	7.59	15.15	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.16	7.7	16.28	3.39	7.7	14.75	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	60	130	20	60	130	ps/pF
Δt_{PHL}				30	60	120	30	60	110	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	60	130	30	60	120	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	30	60	130	30	60	110	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKA0LJ
16-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPKA0LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPKA0LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −16 mA				3.7			V
		I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 16 mA						0.5	V
		I_{OL} = 13.6 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			2.68			0.35	mA
C_i	Input capacitance			0.53			0.53		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		13.3			13.3		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.28	3.73	8.67	1.37	3.73	7.87	ns
t_{PHL}				1.91	5.1	10.95	2.06	5.1	9.99	
t_{PLH}	A	Y	C_L = 50 pF	1.63	4.68	10.79	1.75	4.68	9.79	ns
t_{PHL}				2.74	6.89	14.43	2.95	6.89	13.14	
Δt_{PLH}	A	Y		10	30	60	10	30	50	ps/pF
Δt_{PHL}				20	50	100	30	50	90	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.58	4.44	9.99	1.7	4.44	9.07	ns
t_{PHL}				1.65	4.51	9.88	1.77	4.51	9.01	
t_{PLH}	A	Y	C_L = 50 pF	2.14	5.81	12.85	2.3	5.81	11.67	ns
t_{PHL}				2.28	5.92	12.69	2.45	5.92	11.56	
Δt_{PLH}	A	Y		20	40	80	20	40	70	ps/pF
Δt_{PHL}				20	40	80	20	40	70	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKA1LJ
16-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPKA1LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPKA1LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA						0.5	V
		I_{OL} = 13.6 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			1.17			0.32	mA
C_i	Input capacitance			0.19			0.19		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		1.96			1.96		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.77	4.86	10.67	1.91	4.86	9.69	ns
t_{PZL}			C_L = 50 pF	2.59	6.64	14.18	2.79	6.64	12.86	
t_{PLZ}	A	Y			7.52			7.52		ns
Δt_{PZL}	A	Y		20	50	100	30	50	90	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.52	4.27	9.54	1.64	4.27	8.67	ns
t_{PZL}			C_L = 50 pF	2.15	5.67	12.39	2.31	5.67	11.24	
Δt_{PZL}	A	Y		20	40	80	20	40	70	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKA3LJ
16-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt AND ACTIVE-LOW ENABLE

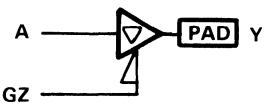
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPKA3LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPKA3LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 16 mA						0.5	V
			I_{OL} = 13.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.3			17.3		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.67	4.75	10.9	1.78	4.75	9.92	ns
t_{PHL}				2.4	6.18	13.3	2.58	6.18	12.12	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.72	5.05	11.7	1.84	5.05	10.65	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.41	6.21	13.36	2.59	6.21	12.16	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.01	5.66	12.89	2.14	5.66	11.74	ns
t_{PHL}				3.21	7.91	16.69	3.45	7.91	15.18	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.06	5.96	13.74	2.2	5.96	12.51	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.22	7.94	16.75	3.46	7.94	15.23	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.23			9.23		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.02			9.02		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	30	60	10	30	50	ps/pF
Δt_{PHL}				20	50	100	20	50	90	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	30	60	10	30	50	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	20	50	100	20	50	60	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKA3LJ
16-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2	5.5	12.28	2.14	5.5	11.18	ns
t_{PHL}				2.12	5.54	12.15	2.27	5.54	11.06	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.17	5.83	13.08	2.31	5.83	11.89	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.12	5.53	12.09	2.27	5.53	11.01	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.54	6.82	15.01	2.72	6.82	13.67	ns
t_{PHL}				2.73	6.9	14.89	2.92	6.9	13.54	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.71	7.15	15.86	2.89	7.15	14.41	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.73	6.89	14.83	2.92	6.89	13.49	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	40	80	20	40	70	ps/pF
Δt_{PHL}				20	40	80	20	40	70	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	40	80	20	40	70	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	20	40	80	20	40	70	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKB0LJ
24-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPKB0LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPKB0LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −16 mA				3.7			V
		I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 24 mA						0.5	V
		I_{OL} = 20.4 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			2.68			0.44	mA
C_i	Input capacitance			0.63			0.63		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		14.8			14.8		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKB0LJ
24-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.27	3.72	8.65	1.36	3.72	7.85	ns
t_{PHL}				2.29	5.86	12.37	2.46	5.86	11.31	
t_{PLH}	A	Y	C_L = 50 pF	1.63	4.66	10.77	1.74	4.66	9.77	ns
t_{PHL}				3.04	7.48	15.52	3.26	7.48	14.18	
Δt_{PLH}	A	Y		10	30	60	10	30	50	ps/pF
Δt_{PHL}				20	50	90	20	50	80	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.58	4.43	9.96	1.69	4.43	9.04	ns
t_{PHL}				2.02	5.27	11.3	2.16	5.27	10.33	
t_{PLH}	A	Y	C_L = 50 pF	2.14	5.79	12.83	2.29	5.79	11.65	ns
t_{PHL}				2.6	6.57	13.9	2.78	6.57	12.7	
Δt_{PLH}	A	Y		20	40	80	20	40	70	ps/pF
Δt_{PHL}				20	40	70	20	40	70	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKB1LJ
24-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPKB1LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPKB1LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 24 mA						0.5	V
		I_{OL} = 20.4 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			1.56			0.44	mA
C_i	Input capacitance			0.27			0.27		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		3.2			3.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKB1LJ
24-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D30, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.05	5.46	11.86	2.21	5.46	10.77	ns
t_{PZL}			C_L = 50 pF	2.76	7.02	14.93	2.97	7.02	13.55	
t_{PLZ}	A	Y			6.53			6.53		ns
Δt_{PZL}	A	Y		20	40	90	20	40	80	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.8	4.88	10.78	1.94	4.88	9.8	ns
t_{PZL}			C_L = 50 pF	2.35	6.14	13.33	2.53	6.14	12.10	
Δt_{PZL}	A	Y		20	40	70	20	40	70	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKB3LJ
24-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt AND ACTIVE-LOW ENABLE

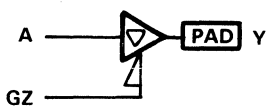
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPKB3LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPKB3LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 24 mA						0.5	V
			I_{OL} = 20.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		19.2			19.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKB3LJ
24-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.67	4.75	10.85	1.77	4.75	9.89	ns
t_{PHL}				2.83	7.1	15.12	3.03	7.1	13.8	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.73	5.06	11.73	1.84	5.06	10.68	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.87	7.19	15.29	3.07	7.19	13.93	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.01	5.66	12.89	2.14	5.66	11.74	ns
t_{PHL}				3.56	8.68	18.19	3.81	8.68	16.58	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.06	5.97	13.77	2.2	5.97	12.53	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.6	8.76	18.35	3.85	8.76	16.7	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.24			9.24		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		7.99			7.99		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	30	60	10	30	50	ps/pF
Δt_{PHL}				20	50	90	20	50	80	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	30	60	10	30	50	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	20	40	90	20	40	80	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.99	5.5	12.23	2.13	5.5	11.14	ns
t_{PHL}				2.53	6.46	13.98	2.71	6.46	12.75	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.17	5.84	13.11	2.32	5.84	11.92	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.56	6.51	14.05	2.74	6.51	12.8	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.54	6.82	15.01	2.71	6.82	13.67	ns
t_{PHL}				3.1	7.73	16.53	3.32	7.73	15.06	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.71	7.17	15.89	2.9	7.17	14.44	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.13	7.78	16.58	3.35	7.78	15.1	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	40	80	20	40	70	ps/pF
Δt_{PHL}				20	40	70	20	40	70	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	40	80	20	40	70	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	20	40	70	20	40	70	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKE0LJ
48-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPKE0LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPKE0LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −16 mA				3.7			V
		I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 48 mA						0.5	V
		I_{OL} = 40.8 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			3.16			0.88	mA
C_i	Input capacitance			0.92			0.92		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		21.4			21.4		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.32	3.84	8.93	1.41	3.84	8.11	ns
t_{PHL}				1.97	5.21	11.06	2.12	5.21	10.13	
t_{PLH}	A	Y	C_L = 50 pF	1.66	4.75	10.98	1.77	4.75	9.96	ns
t_{PHL}				2.43	6.25	13.15	2.62	6.25	12.01	
Δt_{PLH}	A	Y		10	30	60	10	30	50	ps/pF
Δt_{PHL}				10	30	60	10	30	50	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.64	4.58	10.3	1.76	4.58	9.36	ns
t_{PHL}				1.76	4.74	10.23	1.89	4.74	9.36	
t_{PLH}	A	Y	C_L = 50 pF	2.18	5.9	13.08	2.34	5.9	11.87	ns
t_{PHL}				2.13	5.6	11.98	2.29	5.6	10.93	
Δt_{PLH}	A	Y		20	40	80	20	40	70	ps/pF
Δt_{PHL}				10	20	50	10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKE1LJ
48-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPKE1LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPKE1LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 48 mA						0.5	V
		I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			3.16			0.88	mA
C_i	Input capacitance			0.55			0.55		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		6.61			6.61		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.89	5.16	11.27	2.04	5.16	10.25	ns
t_{PZL}			C_L = 50 pF	2.38	6.25	13.43	2.56	6.25	12.21	
t_{PLZ}	A	Y			6.95			6.95		ns
Δt_{PZL}	A	Y		10	30	60	10	30	60	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.7	4.71	10.43	1.83	4.71	9.48	ns
t_{PZL}			C_L = 50 pF	2.09	5.6	12.26	2.24	5.6	11.14	
Δt_{PZL}	A	Y		10	30	50	10	30	50	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKE3LJ
48-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt AND ACTIVE-LOW ENABLE

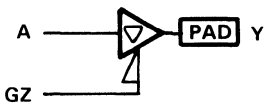
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPKE3LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPKE3LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 48 mA						0.5	V
			I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		24.3			24.3		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.69	4.81	11.01	1.8	4.81	10.03	ns
t_{PHL}				2.55	6.54	14.14	2.73	6.54	12.89	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.75	5.12	11.87	1.86	5.12	10.81	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.58	6.6	14.2	2.77	6.6	12.94	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.03	5.71	13.02	2.16	5.71	11.86	ns
t_{PHL}				3.01	7.57	16.19	3.22	7.57	14.74	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.08	6.02	13.88	2.22	6.02	12.63	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.04	7.63	16.24	3.26	7.63	14.79	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.35			9.35		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.92			8.92		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	30	60	10	30	50	ps/pF
Δt_{PHL}				10	30	60	10	30	50	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	30	60	10	30	50	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	30	60	10	30	50	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKE3LJ
48-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.02	5.57	12.4	2.16	5.57	11.3	ns
t_{PHL}				2.33	6.05	13.28	2.49	6.05	12.1	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.2	5.91	13.27	2.34	5.91	12.06	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.36	6.1	13.28	2.52	6.1	12.1	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.56	6.88	15.15	2.74	6.88	13.8	ns
t_{PHL}				2.7	6.9	15	2.88	6.9	13.65	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.73	7.22	16.01	2.92	7.22	14.56	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.72	6.94	15	2.91	6.94	13.65	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	40	80	20	40	70	ps/pF
Δt_{PHL}				10	20	50	10	20	40	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	40	80	20	40	70	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	20	50	10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKG0LJ
64-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPKG0LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPKG0LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −16 mA				3.7			V
		I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 64 mA						0.5	V
		I_{OL} = 54.4 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			4.23			1.18	mA
C_i	Input capacitance			1.1			1.1		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		24.2			24.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKG0LJ
64-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.34	3.9	9.07	1.43	3.9	8.23	ns
t_{PHL}				1.84	4.93	10.54	1.98	4.93	9.63	
t_{PLH}	A	Y	C_L = 50 pF	1.67	4.8	11.08	1.78	4.8	10.05	ns
t_{PHL}				2.21	5.78	12.26	2.37	5.78	11.19	
Δt_{PLH}	A	Y		10	30	60	10	30	50	ps/pF
Δt_{PHL}				10	20	50	10	20	40	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.66	4.65	10.45	1.78	4.65	9.48	ns
t_{PHL}				1.65	4.51	9.79	1.78	4.51	8.94	
t_{PLH}	A	Y	C_L = 50 pF	2.19	5.96	13.19	2.35	5.96	11.97	ns
t_{PHL}				1.95	5.21	11.24	2.1	5.21	10.25	
Δt_{PLH}	A	Y		20	40	80	20	40	70	ps/pF
Δt_{PHL}				10	20	40	10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKG1LJ
64-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPKG1LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPKG1LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 64 mA						0.5	V
		I_{OL} = 54.4 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			4.23			1.18	mA
C_i	Input capacitance			0.71			0.71		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		8.63			8.63		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPKG1LJ
64-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.83	5.02	11.01	1.97	5.02	10.01	ns
t_{PZL}			C_L = 50 pF	2.21	5.91	12.8	2.38	5.91	11.63	
t_{PLZ}	A	Y			7.35			7.35		ns
Δt_{PZL}	A	Y		10	30	50	10	30	50	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.65	4.61	10.25	1.78	4.61	9.3	ns
t_{PZL}			C_L = 50 pF	1.96	5.34	11.76	2.11	5.34	10.68	
Δt_{PZL}	A	Y		10	20	40	10	20	40	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPKG3LJ
64-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt AND ACTIVE-LOW ENABLE

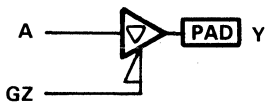
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPKG3LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPKG3LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 64 mA						0.5	V
			I_{OL} = 54.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		27			27		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPKG3LJ
64-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.72	4.88	11.15	1.83	4.88	10.16	ns
t_{PHL}				2.47	6.37	13.89	2.64	6.37	12.64	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.76	5.16	11.96	1.88	5.16	10.9	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.49	6.41	13.89	2.67	6.41	12.64	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.06	5.77	13.14	2.19	5.77	11.97	ns
t_{PHL}				2.83	7.22	15.6	3.04	7.22	14.19	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.09	6.05	13.95	2.23	6.05	12.69	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.86	7.26	15.59	3.06	7.26	14.18	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.43			9.43		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.39			9.39		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	30	60	10	30	50	ps/pF
Δt_{PHL}				10	20	50	10	20	40	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	30	60	10	30	50	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	20	50	10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.06	5.64	12.56	2.2	5.64	11.44	ns
t_{PHL}				2.28	5.94	13.12	2.43	5.94	11.93	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.21	5.96	13.38	2.36	5.96	12.16	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.3	5.96	13.07	2.45	5.96	11.9	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.59	6.94	15.28	2.77	6.94	13.92	ns
t_{PHL}				2.57	6.94	14.56	2.75	6.64	13.24	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.75	7.26	16.09	2.93	7.26	14.63	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.59	6.66	14.51	2.77	6.66	13.2	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	40	80	20	40	70	ps/pF
Δt_{PHL}				10	20	40	10	20	40	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	40	80	20	40	70	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	20	40	10	20	40	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK00LJ
10-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK00LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK00LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −10 mA				3.7			V
		I_{OH} = −8.5 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 10 mA						0.5	V
		I_{OL} = 8.5 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			1.68			0.2	mA
C_i	Input capacitance			0.35			0.35		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		10.8			10.8		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.41	4.03	9.35	1.51	4.03	8.48	ns
t_{PHL}				2.35	6.06	12.84	2.53	6.06	11.72	
t_{PLH}	A	Y	C_L = 50 pF	1.86	5.24	12.06	1.99	5.24	10.94	ns
t_{PHL}				3.5	8.51	17.55	3.77	8.51	15.99	
Δt_{PLH}	A	Y		10	30	80	10	30	70	ps/pF
Δt_{PHL}				30	70	130	40	70	120	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.8	4.91	10.96	1.93	4.91	9.95	ns
t_{PHL}				2	5.3	11.46	2.15	5.3	10.46	
t_{PLH}	A	Y	C_L = 50 pF	2.53	6.71	14.72	2.72	6.71	13.37	ns
t_{PHL}				2.86	7.19	15.21	3.08	7.19	13.87	
Δt_{PLH}	A	Y		20	50	110	20	50	100	ps/pF
Δt_{PHL}				20	50	110	30	50	100	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK01LJ
10-mA N-CHANNEL OPEN-DRAIN OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK01LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK01LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 10 mA						0.5	V
		I_{OL} = 8.5 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.73			0.2	mA
C_i	Input capacitance			0.13			0.13		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		1.26			1.26		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.18	5.78	12.58	2.35	5.78	11.4	ns
t_{PZL}			C_L = 50 pF	3.32	8.23	17.37	3.57	8.23	15.73	
t_{PLZ}	A	Y			7.78			7.78		ns
Δt_{PZL}	A	Y		30	70	140	30	70	120	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.84	5	11.09	1.98	5	10.07	ns
t_{PZL}			C_L = 50 pF	2.69	6.89	14.89	2.9	6.89	13.51	
Δt_{PZL}	A	Y		20	50	110	30	50	100	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK03LJ
10-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt AND ACTIVE-LOW ENABLE

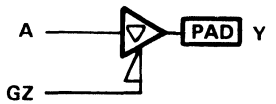
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPK03LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK03LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −10 mA				3.7			V
			I_{OH} = −8.5 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 10 mA						0.5	V
			I_{OL} = 8.5 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		14.9			14.9		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.76	4.95	11.31	1.87	4.95	10.32	ns
t_{PHL}				2.86	7.17	15.22	3.06	7.17	13.87	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	1.81	5.26	12.21	1.93	5.26	11.11	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.87	7.25	15.46	3.08	7.25	14.05	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.19	6.11	13.91	2.34	6.11	12.66	ns
t_{PHL}				3.98	9.56	19.82	4.27	9.56	18.04	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.24	6.43	14.82	2.4	6.43	13.48	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.99	9.65	20.12	4.29	9.65	18.26	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.68			9.68		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.5			8.5		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	30	70	10	30	70	ps/pF
Δt_{PHL}				30	70	130	30	70	120	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	30	70	10	30	70	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	30	70	130	30	70	120	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.17	5.88	13.01	2.32	5.88	11.87	ns
t_{PHL}				2.47	6.34	13.74	2.64	6.34	12.52	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.34	6.23	13.96	2.5	6.23	12.67	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.47	6.35	13.78	2.64	6.35	12.54	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.89	7.62	16.65	3.09	7.62	15.16	ns
t_{PHL}				3.31	8.19	17.39	3.54	8.19	15.83	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.06	7.99	17.64	3.27	7.99	16.02	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.31	8.21	17.47	3.54	8.21	15.87	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	50	100	20	50	90	ps/pF
Δt_{PHL}				20	50	100	30	50	90	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	50	110	20	50	100	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	20	50	110	30	50	100	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK20LJ
2-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK20LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK20LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −2 mA				3.7			V
		I_{OH} = −1.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 2 mA						0.5	V
		I_{OL} = 1.6 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.34			0.04	mA
C_i	Input capacitance			0.09			0.09		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		7.68			7.68		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK20LJ
2-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	2.68	7.36	16.88	2.87	7.36	15.33	ns
t_{PHL}				6.43	15	30.66	6.9	15	27.97	
t_{PLH}	A	Y	C_L = 50 pF	3.98	10.92	24.91	4.26	10.92	22.65	ns
t_{PHL}				10.71	23.84	42.61	11.52	23.84	40.08	
Δt_{PLH}	A	Y		40	100	230	40	100	210	ps/pF
Δt_{PHL}				120	250	340	130	250	350	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	3.79	9.73	21.17	4.06	9.73	19.24	ns
t_{PHL}				5.25	12.64	26.49	5.62	12.64	24.19	
t_{PLH}	A	Y	C_L = 50 pF	6.3	15.94	34.06	6.75	15.94	31.03	ns
t_{PHL}				8.29	19.01	33.75	8.9	19.01	32.18	
Δt_{PLH}	A	Y		70	180	370	80	180	340	ps/pF
Δt_{PHL}				90	180	210	90	180	230	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK21LJ
2-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK21LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK21LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA						0.5	V
		I_{OL} = 1.6 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.15			0.04	mA
C_i	Input capacitance			0.04			0.04		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		0.35			0.35		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK21LJ
2-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	5.95	14.81	33.24	6.41	14.81	29.58	ns
t_{PZL}			C_L = 50 pF	10.31	24.46	53.49	11.13	24.46	47.39	
t_{PLZ}	A	Y			12.74			12.74		ns
Δt_{PZL}	A	Y		120	280	580	130	280	280	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	1.88	4.48	9.83	2.02	4.48	8.78	ns
t_{PZL}			C_L = 50 pF	4.37	10.1	21.77	4.71	10.1	19.33	
Δt_{PZL}	A	Y		90	190	390	90	190	350	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK23LJ
2-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt AND ACTIVE-LOW ENABLE

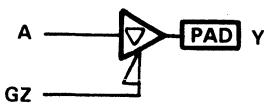
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPK23LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK23LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High level output voltage		I_{OH} = −2 mA				3.7			V
			I_{OH} = −1.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 2 mA						0.5	V
			I_{OL} = 1.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		11.4			11.4		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPK23LJ
2-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	3.05	8.29	18.91	3.25	8.29	17.19	ns
t_{PHL}				7.14	16.6	34.13	7.66	16.6	31.06	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.1	8.8	20.74	3.32	8.8	18.77	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	7.38	18.05	40.14	7.94	18.05	35.8	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	4.31	11.77	26.72	4.6	11.77	24.33	ns
t_{PHL}				11.36	25.41	50.96	12.22	25.41	46.24	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	4.35	12.37	29.08	4.66	12.37	26.35	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	11.73	27.72	60.58	12.65	27.72	53.76	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		15.35			15.35		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		11.93			11.93		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	40	100	220	40	100	200	ps/pF
Δt_{PHL}				120	250	480	130	250	430	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	40	100	240	40	100	220	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	120	280	580	130	280	510	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	4.25	10.87	23.57	4.55	10.87	21.44	ns
t_{PHL}				5.83	14.01	29.56	6.25	14.01	26.93	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	4.45	11.78	27.04	4.77	11.78	24.33	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.95	14.74	32.58	6.39	14.74	29.34	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	6.74	17.01	36.29	7.21	17.01	33.1	ns
t_{PHL}				8.8	20.35	42.04	9.45	20.35	38.2	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	6.95	18.4	42.02	7.44	18.4	37.82	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	8.97	21.37	46.24	9.64	21.37	41.54	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	70	180	360	80	180	330	ps/pF
Δt_{PHL}				80	180	360	90	180	320	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	70	190	430	80	190	390	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	90	190	390	90	190	350	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK40LJ
4-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK40LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK40LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −4 mA				3.7			V
		I_{OH} = −3.4 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 4 mA						0.5	V
		I_{OL} = 3.4 mA			0.4				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.68			0.08	mA
C_i	Input capacitance			0.17			0.17		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		8.5			8.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.92	5.35	12.29	2.05	5.35	11.16	ns
t_{PHL}				3.94	9.49	19.58	4.23	9.49	17.87	
t_{PLH}	A	Y	C_L = 50 pF	2.71	7.48	17.05	2.9	7.48	15.49	ns
t_{PHL}				6.26	14.38	28.84	6.73	14.38	26.27	
Δt_{PLH}	A	Y		20	60	140	20	60	120	ps/pF
Δt_{PHL}				70	140	260	70	140	240	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	2.59	6.81	14.94	2.78	6.81	13.58	ns
t_{PHL}				3.26	8.12	17.14	3.5	8.12	15.66	
t_{PLH}	A	Y	C_L = 50 pF	4	10.26	22.09	4.28	10.26	20.1	ns
t_{PHL}				4.94	11.75	24.19	5.3	11.75	22.07	
Δt_{PLH}	A	Y		40	100	200	40	100	190	ps/pF
Δt_{PHL}				50	100	200	50	100	180	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK41LJ
4-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK41LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK41LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA						0.5	V
		I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.29			0.08	mA
C_i	Input capacitance			0.07			0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		0.58			0.58		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	3.63	9.11	19.74	3.91	9.11	17.79	ns
t_{PZL}			C_L = 50 pF	5.96	14.13	29.64	6.42	14.13	26.67	
t_{PLz}	A	Y			9.5			9.5		ns
Δt_{PZL}	A	Y		70	140	280	70	140	250	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.97	7.64	16.8	3.19	7.64	15.2	ns
t_{PZL}			C_L = 50 pF	4.65	11.31	24.12	5	11.31	21.8	
Δt_{PZL}	A	Y		50	100	210	50	100	190	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPK43LJ
4-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt AND ACTIVE-LOW ENABLE

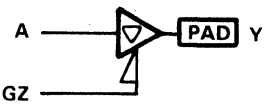
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPK43LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK43LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −4 mA				3.7			V
			I_{OH} = −3.4 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 4 mA						0.5	V
			I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		12.4			12.4		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.25	6.2	14.10	2.4	6.2	12.83	ns
t_{PHL}				4.49	10.77	22.3	4.82	10.77	20.31	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.3	6.58	15.27	2.46	6.58	13.86	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.56	11.16	23.82	4.9	11.16	21.53	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	3.01	8.26	18.68	3.21	8.26	17.02	ns
t_{PHL}				6.77	15.56	31.48	7.28	15.56	28.58	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.06	8.66	19.98	3.27	8.66	18.14	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	6.88	16.13	33.63	7.4	16.13	30.3	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		11.38			11.38		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.72			9.72		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	60	130	20	60	120	ps/pF
Δt_{PHL}				70	140	260	70	140	240	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	60	130	20	60	120	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	70	140	280	70	140	250	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK43LJ
4-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.98	7.77	16.94	3.18	7.77	15.42	ns
t_{PHL}				3.75	9.26	19.64	4.02	9.26	17.9	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.16	8.27	18.5	3.37	8.27	16.75	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.78	9.45	20.43	4.05	9.45	18.53	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	4.35	11.15	23.93	4.66	11.15	21.81	ns
t_{PHL}				5.4	12.81	26.64	5.79	12.81	24.21	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	4.54	11.75	25.92	4.85	11.75	23.49	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.44	13.07	27.65	5.84	13.07	25.02	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	40	100	200	40	100	180	ps/pF
Δt_{PHL}				50	100	200	50	100	180	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	40	100	210	40	100	190	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	50	100	210	50	100	190	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK60LJ
6-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK60LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK60LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −6 mA				3.7			V
		I_{OH} = −5.1 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 6 mA						0.5	V
		I_{OL} = 5.1 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			1.01			0.12	mA
C_i	Input capacitance			0.24			0.24		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		9.3			9.3		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPK60LJ
6-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.66	4.68	10.8	1.78	4.68	9.8	ns
t_{PHL}				3.08	7.64	15.94	3.31	7.64	14.54	
t_{PLH}	A	Y	C_L = 50 pF	2.27	6.31	14.45	2.43	6.31	13.12	ns
t_{PHL}				4.76	11.18	22.74	5.12	11.18	20.68	
Δt_{PLH}	A	Y		20	50	100	20	50	90	ps/pF
Δt_{PHL}				50	100	190	50	100	180	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	2.18	5.83	12.91	2.34	5.83	11.72	ns
t_{PHL}				2.58	6.59	14.08	2.76	6.59	12.84	
t_{PLH}	A	Y	C_L = 50 pF	3.22	8.37	18.18	3.46	8.37	16.53	ns
t_{PHL}				3.82	9.28	19.37	4.1	9.28	17.64	
Δt_{PLH}	A	Y		30	70	150	30	70	140	ps/pF
Δt_{PHL}				40	80	150	40	80	140	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK61LJ
6-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPK61LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK61LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 6 mA						0.5	V
		I_{OL} = 5.1 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.44			0.12	mA
C_i	Input capacitance			0.09			0.09		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		0.82			0.82		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK61LJ
6-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.85	7.3	15.78	3.07	7.3	14.28	ns
t_{PZL}			C_L = 50 pF	4.52	10.9	22.81	4.87	10.9	20.6	
t_{PLZ}	A	Y			9.17			9.17		ns
Δt_{PZL}	A	Y		50	100	200	50	100	180	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.36	6.21	13.68	2.54	6.21	12.4	ns
t_{PZL}			C_L = 50 pF	3.59	8.92	19.07	3.86	8.92	17.27	
Δt_{PZL}	A	Y		40	80	150	40	80	140	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK63LJ
6-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt AND ACTIVE-LOW ENABLE

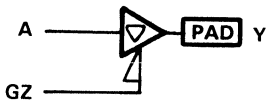
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPK63LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPK63LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −6 mA				3.7			V
			I_{OH} = −5.1 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 6 mA						0.5	V
			I_{OL} = 5.1 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}		1.04			0.27		mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		13.2			13.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPK63LJ
6-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.25 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	1.99	5.54	12.65	2.13	5.54	11.51	ns
t_{PHL}				3.59	8.79	18.38	3.86	8.79	16.74	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.04	5.88	13.65	2.18	5.88	12.4	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.62	8.98	19.08	3.89	8.98	17.31	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.58	7.12	16.18	2.75	7.12	14.73	ns
t_{PHL}				5.24	12.26	25.04	5.63	12.26	22.75	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.62	7.47	17.22	2.8	7.47	15.65	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.28	12.52	26.01	5.68	12.52	23.52	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.86			9.86		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.06			9.06		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	50	100	20	50	90	ps/pF
Δt_{PHL}				50	100	190	50	100	170	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	50	100	20	50	90	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	50	100	200	50	100	180	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.56	6.77	14.89	2.73	6.77	13.56	ns
t_{PHL}				3.04	7.65	16.36	3.26	7.65	14.91	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.72	7.19	16.06	2.91	7.19	14.56	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.05	7.73	16.69	3.27	7.73	15.16	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	3.57	9.26	20.04	3.82	9.26	18.26	ns
t_{PHL}				4.25	10.27	21.53	4.56	10.27	19.58	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.74	9.71	21.37	4	9.71	19.4	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.26	10.38	21.97	4.58	10.38	19.92	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	30	70	150	30	70	130	ps/pF
Δt_{PHL}				30	70	150	40	70	130	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	30	70	150	30	70	140	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	30	80	150	40	80	140	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHA0LJ
16-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPHA0LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPHA0LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −16 mA				3.7			V
		I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 16 mA						0.5	V
		I_{OL} = 13.6 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			2.68			0.32	mA
C_i	Input capacitance			0.53			0.53		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		13.3			13.3		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.65	4.88	11.43	1.77	4.88	10.36	ns
t_{PHL}				2.62	6.86	14.62	2.82	6.86	13.35	
t_{PLH}	A	Y	C_L = 50 pF	2.08	6.02	13.99	2.23	6.02	12.68	ns
t_{PHL}				3.59	8.98	18.72	3.86	8.98	17.07	
Δt_{PLH}	A	Y		10	30	70	10	30	70	ps/pF
Δt_{PHL}				30	60	120	30	60	110	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	2.05	5.76	13.05	2.2	5.76	11.83	ns
t_{PHL}				2.28	6.13	13.31	2.46	6.13	12.15	
t_{PLH}	A	Y	C_L = 50 pF	2.71	7.39	16.46	2.91	7.39	14.94	ns
t_{PHL}				3.02	7.81	16.65	3.25	7.81	15.19	
Δt_{PLH}	A	Y		20	50	100	20	50	90	ps/pF
Δt_{PHL}				20	50	100	20	50	90	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHA1LJ
16-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPHA1LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPHA1LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA						0.5	V
		I_{OL} = 13.6 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			1.03			0.29	mA
C_i	Input capacitance			0.19			0.19		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		1.96			1.96		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.47	6.64	14.51	2.67	6.64	13.17	ns
t_{PZL}			C_L = 50 pF	3.43	8.74	18.66	3.69	8.74	16.91	
t_{PLZ}	A	Y			7.52			7.52		ns
Δt_{PZL}	A	Y		30	60	120	30	60	110	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.15	5.89	13.1	2.31	5.89	11.89	ns
t_{PZL}			C_L = 50 pF	2.88	7.57	16.51	3.1	7.57	14.97	
Δt_{PZL}	A	Y		20	50	100	20	50	90	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHA3LJ
16-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt AND ACTIVE-LOW ENABLE

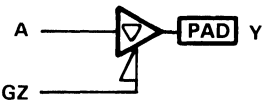
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPHA3LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPHA3LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 16 mA						0.5	V
			I_{OL} = 13.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		17.3			17.3		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.1	5.91	13.47	2.24	5.91	12.27	ns
t_{PHL}				3.24	8.11	17.31	3.47	8.11	15.77	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.16	6.24	14.43	2.31	6.24	13.12	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.25	8.16	17.49	3.49	8.16	15.9	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.51	7.01	15.95	2.68	7.01	14.51	ns
t_{PHL}				4.18	10.15	21.3	4.48	10.15	19.39	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.56	7.33	16.88	2.74	7.33	15.35	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.19	10.21	21.46	4.5	10.21	19.51	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.23			9.23		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.02			9.02		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	30	70	10	30	60	ps/pF
Δt_{PHL}				30	60	110	30	60	100	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	30	70	10	30	60	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	30	60	110	30	60	100	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHA3LJ
16-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.52	6.84	15.17	2.69	6.84	13.82	ns
t_{PHL}				2.87	7.32	15.9	3.07	7.32	14.48	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.7	7.21	16.17	2.88	7.21	14.68	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	2.87	7.32	15.91	3.07	7.32	14.48	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	3.16	8.41	18.49	3.38	8.41	16.83	ns
t_{PHL}				3.59	8.94	19.17	3.84	8.94	17.45	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.34	8.78	19.45	3.57	8.78	17.67	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.59	8.94	19.16	3.84	8.94	17.43	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	40	90	20	40	90	ps/pF
Δt_{PHL}				20	50	90	20	50	80	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	40	90	20	40	90	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	20	50	90	20	50	80	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHB0LJ
24-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPHB0LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPHB0LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −16 mA				3.7			V
		I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 24 mA						0.5	V
		I_{OL} = 20.4 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			2.18			0.39	mA
C_i	Input capacitance			0.63			0.63		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		14.8			14.8		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHB0LJ
24-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.64	4.85	11.38	1.76	4.85	10.32	ns
t_{PHL}				3.34	8.22	16.96	3.58	8.22	15.55	
t_{PLH}	A	Y	C_L = 50 pF	2.07	6	13.95	2.22	6	12.65	ns
t_{PHL}				4.22	10.17	20.81	4.53	10.17	19.04	
Δt_{PLH}	A	Y		10	30	70	10	30	70	ps/pF
Δt_{PHL}				30	60	110	30	60	100	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	2.04	5.74	13	2.19	5.74	11.79	ns
t_{PHL}				2.97	7.46	15.63	3.18	7.46	14.33	
t_{PLH}	A	Y	C_L = 50 pF	2.7	7.37	16.42	2.9	7.37	14.9	ns
t_{PHL}				3.66	9.04	18.83	3.93	9.04	17.23	
Δt_{PLH}	A	Y		20	50	100	20	50	90	ps/pF
Δt_{PHL}				20	50	90	20	50	80	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHB1LJ
24-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPHB1LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPHB1LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 24 mA						0.5	V
		I_{OL} = 20.4 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			1.31			0.39	mA
C_i	Input capacitance			0.27			0.27		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		3.2			3.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	3.08	7.84	16.76	3.31	7.84	15.23	ns
t_{PZL}			C_L = 50 pF	3.93	9.71	20.46	4.22	9.71	18.57	
t_{PLZ}	A	Y			6.53			6.53		ns
Δt_{PZL}	A	Y		20	50	110	30	50	100	ps/pF

CMOS loads, R_L = 1 k to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.74	7.1	15.4	2.94	7.1	14	ns
t_{PZL}			C_L = 50 pF	3.41	8.62	18.49	3.66	8.62	16.79	
Δt_{PZL}	A	Y		20	40	90	20	40	80	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHB3LJ
24-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt AND ACTIVE-LOW ENABLE

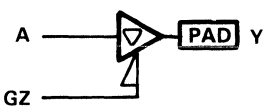
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPHB3LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPHB3LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 24 mA						0.5	V
			I_{OL} = 20.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		19.2			19.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHB3LJ
24-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.09	5.9	13.46	2.22	5.9	12.26	ns
t_{PHL}				4.03	9.73	20.35	4.31	9.73	18.58	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.17	6.25	14.46	2.31	6.25	13.15	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.09	9.87	20.7	4.38	9.87	18.87	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.5	7	15.92	2.67	7	14.49	ns
t_{PHL}				4.9	11.61	24.06	5.24	11.61	21.94	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.57	7.35	16.91	2.75	7.35	15.38	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.95	11.75	24.36	5.3	11.75	22.19	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.23			9.23		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		7.98			7.98		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	30	70	10	30	60	ps/pF
Δt_{PHL}				20	50	110	30	50	100	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	30	70	10	30	60	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	20	50	100	30	50	90	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.5	6.83	15.16	2.68	6.83	13.81	ns
t_{PHL}				3.64	8.91	18.93	3.88	8.91	17.28	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.7	7.22	16.2	2.89	7.22	14.71	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.68	9	19.13	3.93	9	17.44	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	3.15	8.4	18.45	3.37	8.4	16.8	ns
t_{PHL}				4.32	10.44	22.01	4.61	10.44	20.08	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.34	8.79	19.49	3.57	8.79	17.7	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.36	10.53	22.17	4.65	10.53	20.21	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	40	90	20	40	90	ps/pF
Δt_{PHL}				20	40	90	20	40	80	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	40	90	20	40	90	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	20	40	90	20	40	80	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHE0LJ
48-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPHE0LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPHE0LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −16 mA				3.7			V
		I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 48 mA						0.5	V
		I_{OL} = 40.8 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			2.61			0.78	mA
C_i	Input capacitance			0.92			0.92		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		21.4			21.4		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.69	5.01	11.73	1.82	5.01	10.63	ns
t_{PHL}				2.93	7.33	15.16	3.15	7.33	13.91	
t_{PLH}	A	Y	C_L = 50 pF	2.1	6.1	14.19	2.25	6.1	12.86	ns
t_{PHL}				3.47	8.59	17.71	3.73	8.59	16.22	
Δt_{PLH}	A	Y		10	30	70	10	30	60	ps/pF
Δt_{PHL}				20	40	70	20	40	70	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	2.11	5.92	13.41	2.27	5.92	12.16	ns
t_{PHL}				2.64	6.72	14.11	2.83	6.72	12.94	
t_{PLH}	A	Y	C_L = 50 pF	2.75	7.49	16.7	2.95	7.49	15.16	ns
t_{PHL}				3.08	7.76	16.26	3.3	7.76	14.89	
Δt_{PLH}	A	Y		20	40	90	20	40	90	ps/pF
Δt_{PHL}				10	30	60	10	30	60	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHE1LJ
48-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPHE1LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPHE1LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 48 mA						0.5	V
		I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			2.61			0.78	mA
C_i	Input capacitance			0.55			0.55		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		6.61			6.61		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.89	7.42	15.88	3.11	7.42	14.44	ns
t_{PZL}			C_L = 50 pF	3.46	8.72	18.51	3.72	8.72	16.81	
t_{PLZ}	A	Y			6.95			6.95		ns
Δt_{PZL}	A	Y		20	40	80	20	40	70	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.62	6.82	14.81	2.81	6.82	13.47	ns
t_{PZL}			C_L = 50 pF	3.08	7.91	17.05	3.31	7.91	15.49	
Δt_{PZL}	A	Y		10	30	60	10	30	60	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPHE3LJ
48-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt AND ACTIVE-LOW ENABLE

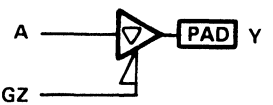
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPHE3LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPHE3LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 48 mA						0.5	V
			I_{OL} = 40.8 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		24.3			24.3		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.11	5.97	13.63	2.25	5.97	12.42	ns
t_{PHL}				3.64	8.88	18.8	3.9	8.88	17.15	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.19	6.31	14.61	2.34	6.31	13.29	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.67	8.96	18.93	3.93	8.96	17.26	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.52	7.06	16.06	2.69	7.06	14.61	ns
t_{PHL}				4.18	10.12	21.3	4.48	10.12	19.4	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.59	7.39	17.02	2.77	7.39	15.48	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.21	10.19	21.41	4.51	10.19	19.49	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.36			9.36		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.91			8.91		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	30	70	10	30	60	ps/pF
Δt_{PHL}				20	40	70	20	40	60	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	30	70	10	30	60	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	20	40	70	20	40	60	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHE3LJ
48-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.53	6.91	15.35	2.71	6.91	13.98	ns
t_{PHL}				3.33	8.26	17.72	3.56	8.26	16.15	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.74	7.3	16.38	2.92	7.3	14.87	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.36	8.31	17.76	3.59	8.31	16.19	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	3.17	8.47	18.6	3.39	8.47	16.93	ns
t_{PHL}				3.77	9.28	19.82	4.03	9.28	18.05	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.37	8.85	19.62	3.6	8.85	17.82	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.79	9.32	19.86	4.06	9.32	18.08	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	40	90	20	40	80	ps/pF
Δt_{PHL}				10	30	60	10	30	50	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	40	90	20	40	80	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	30	60	10	30	50	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHG0LJ
64-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPHG0LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPHG0LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −16 mA				3.7			V
		I_{OH} = −13.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 64 mA						0.5	V
		I_{OL} = 54.4 mA			0.5				
I_{CC}	Supply current	V_I = V_{IH} or V_{IL}			3.5			1.04	mA
C_i	Input capacitance			1.1			1.1		pF
C_{pd}	Equivalent power dissipation capacitance	t_r = t_f = 1 ns		24.2			24.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHG0LJ
64-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.72	5.08	11.91	1.84	5.08	10.79	ns
t_{PHL}				2.73	6.91	14.32	2.94	6.91	13.15	
t_{PLH}	A	Y	C_L = 50 pF	2.12	6.17	14.33	2.28	6.17	12.99	ns
t_{PHL}				3.17	7.93	16.48	3.41	7.93	15.06	
Δt_{PLH}	A	Y		10	30	70	10	30	60	ps/pF
Δt_{PHL}				10	30	60	10	30	50	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	2.13	6.01	13.6	2.3	6.01	12.33	ns
t_{PHL}				2.47	6.36	13.37	2.65	6.36	12.28	
t_{PLH}	A	Y	C_L = 50 pF	2.77	7.56	16.85	2.98	7.56	15.29	ns
t_{PHL}				2.83	7.21	15.21	3.04	7.21	13.9	
Δt_{PLH}	A	Y		20	40	90	20	40	80	ps/pF
Δt_{PHL}				10	20	50	10	20	50	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHG1LJ
64-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPHG1LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPHG1LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 64 mA						0.5	V
		I_{OL} = 54.4 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			3.5			1.04	mA
C_i	Input capacitance			0.71			0.71		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		8.63			8.63		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHG1LJ
64-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.76	7.13	15.33	2.97	7.13	13.94	ns
t_{PZL}			C_L = 50 pF	3.21	8.19	17.49	3.46	8.19	15.88	
t_{PLZ}	A	Y			7.34			7.34		ns
Δt_{PZL}	A	Y		10	30	60	10	30	60	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.5	6.59	14.36	2.69	6.59	13.05	ns
t_{PZL}			C_L = 50 pF	2.88	7.47	16.2	3.09	7.47	14.71	
Δt_{PZL}	A	Y		10	30	50	10	30	50	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHG3LJ
64-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt AND ACTIVE-LOW ENABLE

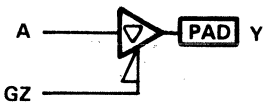
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPHG3LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPHG3LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −16 mA				3.7			V
			I_{OH} = −13.4 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 64 mA						0.5	V
			I_{OL} = 54.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		27			27		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPHG3LJ
64-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.14	6.05	13.81	2.29	6.05	12.58	ns
t_{PHL}				3.49	8.55	18.24	3.73	8.55	16.61	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.2	6.35	14.71	2.35	6.35	13.38	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.5	8.59	18.25	3.75	8.59	16.62	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.54	7.12	16.2	2.71	7.12	14.75	ns
t_{PHL}				3.92	9.57	20.3	4.19	9.57	18.47	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.6	7.42	17.11	2.78	7.42	15.55	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.93	9.59	20.29	4.21	9.59	18.47	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.43			9.43		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.38			9.38		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	30	70	10	30	60	ps/pF
Δt_{PHL}				10	30	60	10	30	50	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	30	70	10	30	60	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	30	60	10	30	50	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.57	7	15.54	2.75	7	14.15	ns
t_{PHL}				3.21	7.99	17.26	3.43	7.99	15.72	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.76	7.35	16.5	2.94	7.35	14.98	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.22	8	17.21	3.44	8	15.67	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	3.2	8.53	18.75	3.43	8.53	17.08	ns
t_{PHL}				3.56	8.83	19.01	3.81	8.83	17.29	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.38	8.89	19.72	3.61	8.89	17.91	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.57	8.84	18.95	3.82	8.84	17.25	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	40	90	20	40	80	ps/pF
Δt_{PHL}				10	20	50	10	20	40	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	40	90	20	40	80	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	10	20	50	10	20	50	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPH00LJ
10-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPH00LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPH00LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −10 mA				3.7			V
		I_{OH} = −8.5 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 10 mA						0.5	V
		I_{OL} = 8.5 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			1.34			0.18	mA
C_i	Input capacitance			0.35			0.35		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		10.8			10.8		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	1.81	5.27	12.34	1.94	5.27	11.17	ns
t_{PHL}				3.17	8.07	17.01	3.41	8.07	15.54	
t_{PLH}	A	Y	C_L = 50 pF	2.34	6.72	15.57	2.51	6.72	14.11	ns
t_{PHL}				4.5	10.93	22.57	4.84	10.93	20.56	
Δt_{PLH}	A	Y		20	40	90	20	40	80	ps/pF
Δt_{PHL}				40	80	160	40	80	140	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	2.29	6.34	14.3	2.46	6.34	12.96	ns
t_{PHL}				2.73	7.13	15.34	2.93	7.13	14.01	
t_{PLH}	A	Y	C_L = 50 pF	3.16	8.46	18.71	3.39	8.46	16.97	ns
t_{PHL}				3.73	9.38	19.84	4.01	9.38	18.08	
Δt_{PLH}	A	Y		20	60	130	30	60	110	ps/pF
Δt_{PHL}				30	60	130	30	60	120	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPH01LJ 10-mA N-CHANNEL OPEN-DRAIN OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPH01LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPH01LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 10 mA						0.5	V
		I_{OL} = 8.5 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.64			0.18	mA
C_i	Input capacitance			0.13			0.13		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		1.26			1.26		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.97	7.78	16.93	3.2	7.78	15.34	ns
t_{PZL}			C_L = 50 pF	4.29	10.63	22.49	4.63	10.63	20.37	
t_{PLZ}	A	Y			7.78			7.78		ns
Δt_{PZL}	A	Y		40	80	160	40	80	140	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	2.54	6.82	15.09	2.73	6.82	13.69	ns
t_{PZL}			C_L = 50 pF	3.54	9.05	19.58	3.81	9.05	17.76	
Δt_{PZL}	A	Y		30	60	130	30	60	120	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPH03LJ
10-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt AND ACTIVE-LOW ENABLE

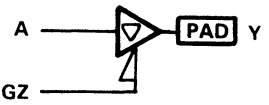
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPH03LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPH03LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −10 mA				3.7			V
			I_{OH} = −8.5 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 10 mA						0.5	V
			I_{OL} = 8.5 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	μA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		14.9			14.9		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.24	6.23	14.2	2.39	6.23	12.93	ns
t_{PHL}				3.79	9.35	19.71	4.06	9.35	17.98	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.27	6.57	15.23	2.43	6.57	13.84	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.81	9.49	20.19	4.08	9.49	18.34	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.75	7.62	17.32	2.94	7.62	15.75	ns
t_{PHL}				5.09	12.13	25.1	5.46	12.13	22.84	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.79	7.96	18.34	2.99	7.96	16.66	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.11	12.28	25.59	5.48	12.28	23.23	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.68			9.68		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		8.5			8.5		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	10	40	90	20	40	80	ps/pF
Δt_{PHL}				40	80	150	40	80	140	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	10	40	90	20	40	80	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	40	80	150	40	80	140	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPH03LJ
10-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.76	7.37	16.27	2.95	7.37	14.81	ns
t_{PHL}				3.3	8.34	17.92	3.54	8.34	16.34	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.92	7.76	17.41	3.12	7.76	15.79	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	3.3	8.39	18.12	3.53	8.39	16.47	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	3.59	9.41	20.54	3.85	9.41	18.69	ns
t_{PHL}				4.29	10.52	22.27	4.59	10.52	20.28	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.76	9.82	21.69	4.02	9.82	19.68	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.29	10.58	22.46	4.59	10.58	20.41	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	60	120	30	60	110	ps/pF
Δt_{PHL}				30	60	120	30	60	110	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	60	120	30	60	110	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	30	60	120	30	60	110	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPH20LJ
2-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPH20LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPH20LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −2 mA				3.7			V
		I_{OH} = −1.6 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 2 mA						0.5	V
		I_{OL} = 1.6 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.28			0.04	mA
C_i	Input capacitance			0.09			0.09		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		7.68			7.68		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPH20LJ
2-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	3.39	9.42	21.73	3.63	9.42	19.7	ns
t_{PHL}				8.14	19	38.81	8.72	19	35.48	
t_{PLH}	A	Y	C_L = 50 pF	4.88	13.44	30.78	5.24	13.44	27.92	ns
t_{PHL}				12.85	28.69	49	13.81	28.69	46.95	
Δt_{PLH}	A	Y		40	110	260	50	110	230	ps/pF
Δt_{PHL}				130	280	290	150	280	330	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	4.69	12.14	26.65	5.04	12.14	24.18	ns
t_{PHL}				6.74	16.26	33.97	7.21	16.26	31.11	
t_{PLH}	A	Y	C_L = 50 pF	7.42	18.79	40.48	7.96	18.79	36.79	ns
t_{PHL}				10.18	23.43	38.77	10.93	23.43	38	
Δt_{PLH}	A	Y		80	190	400	80	190	360	ps/pF
Δt_{PHL}				100	200	140	110	200	200	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPH21LJ
2-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT	OUTPUT
A	Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPH21LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPH21LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA						0.5	V
		I_{OL} = 1.6 mA			0.5				
I_{OZ}	Off-state output current	$V_{(}$ = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current	V = V_{IH} or V_{IL}			0.13			0.04	mA
C_i	Input capacitance			0.04			0.04		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		0.35			0.35		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPH21LJ
2-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	7.61	18.99	43.07	8.2	18.99	38.3	ns
t_{PZL}			C_L = 50 pF	12.38	29.39	64.43	13.34	29.39	57.21	
t_{PLZ}	A	Y			12.78			12.78		ns
Δt_{PZL}	A	Y		140	300	610	150	300	540	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	6.19	15.66	35.33	6.64	15.66	31.73	ns
t_{PZL}			C_L = 50 pF	9.6	23.09	50.33	10.32	23.09	45.18	
Δt_{PZL}	A	Y		100	210	430	110	210	380	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPH23LJ
2-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt AND ACTIVE-LOW ENABLE

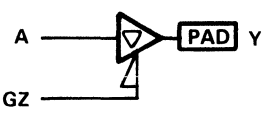
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPH23LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPH23LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High level output voltage		I_{OH} = −2 mA				3.7			V
			I_{OH} = −1.6 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 2 mA						0.5	V
			I_{OL} = 1.6 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		11.4			11.4		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPH23LJ
2-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	3.85	10.46	23.85	4.12	10.46	21.66	ns
t_{PHL}				9	20.89	42.98	9.65	20.89	39.17	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.91	11.07	26.21	4.2	11.07	23.66	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	9.32	22.85	51.21	10.02	22.85	45.63	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	5.3	14.37	32.55	5.68	14.37	29.61	ns
t_{PHL}				13.62	30.52	61.4	14.62	30.52	55.82	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	5.36	15.06	35.4	5.75	15.06	32	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	14.07	33.24	72.57	15.15	33.24	64.57	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		15.34			15.34		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		11.94			11.94		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	40	110	250	40	110	230	ps/pF
Δt_{PHL}				130	280	530	140	280	480	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	40	110	260	40	110	240	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	140	300	610	150	300	540	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	5.27	13.39	29.14	5.64	13.39	26.48	ns
t_{PHL}				7.46	17.89	37.72	7.99	17.89	34.41	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	5.49	14.51	33.5	5.89	14.51	30.07	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	7.63	18.93	42.1	8.18	18.93	37.89	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	7.95	19.94	42.65	8.51	19.94	38.85	ns
t_{PHL}				10.82	25.04	51.79	11.59	25.04	47.14	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	8.18	21.48	49.09	8.77	21.48	44.11	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	11.03	26.33	57.04	11.84	26.33	51.32	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	80	190	390	80	190	350	ps/pF
Δt_{PHL}				100	200	400	100	200	360	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	80	200	450	80	200	400	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	100	210	430	100	210	380	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPH40LJ
4-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPH40LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPH40LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −4 mA				3.7			V
		I_{OH} = −3.4 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 4 mA						0.5	V
		I_{OL} = 3.4 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.56			0.07	mA
C_i	Input capacitance			0.17			0.17		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		8.5			8.5		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	2.44	6.92	16.03	2.61	6.92	14.52	ns
t_{PHL}				5.08	12.26	25.3	5.46	12.26	23.09	
t_{PLH}	A	Y	C_L = 50 pF	3.36	9.39	21.56	3.61	9.39	19.54	ns
t_{PHL}				7.71	17.76	35.56	8.29	17.76	32.48	
Δt_{PLH}	A	Y		30	70	160	30	70	140	ps/pF
Δt_{PHL}				80	160	290	80	160	270	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	3.25	8.66	19.18	3.49	8.66	17.39	ns
t_{PHL}				4.27	10.62	22.41	4.57	10.62	20.47	
t_{PLH}	A	Y	C_L = 50 pF	4.85	12.5	27.16	5.2	12.5	24.65	ns
t_{PHL}				6.22	14.81	30.35	6.67	14.81	27.78	
Δt_{PLH}	A	Y		50	110	230	50	110	210	ps/pF
Δt_{PHL}				60	120	230	60	120	210	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPH41LJ
4-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPH41LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPH41LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA						0.5	V
		I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.26			0.07	mA
C_i	Input capacitance			0.07			0.07		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		0.58			0.58		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	4.75	11.92	25.94	5.11	11.92	23.37	ns
t_{PZL}			C_L = 50 pF	7.37	17.54	36.97	7.94	17.54	33.28	
t_{PLZ}	A	Y			9.5			9.5		ns
Δt_{PZL}	A	Y		70	160	320	80	160	280	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	3.94	10.14	22.35	4.24	10.14	20.21	ns
t_{PZL}			C_L = 50 pF	5.88	14.36	30.76	6.32	14.36	27.8	
Δt_{PZL}	A	Y		60	120	240	60	120	220	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPH43LJ
4-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt AND ACTIVE-LOW ENABLE

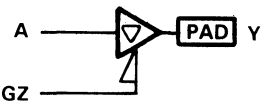
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPH43LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPH43LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High level output voltage		I_{OH} = −4 mA				3.7			V
			I_{OH} = −3.4 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 4 mA						0.5	V
			I_{OL} = 3.4 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		12.4			12.4		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.86	7.85	17.86	3.06	7.85	16.24	ns
t_{PHL}				5.76	13.73	28.45	6.19	13.73	25.9	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.91	8.28	19.28	3.13	8.28	17.46	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.86	14.31	30.63	6.3	14.31	27.68	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	3.75	10.24	22.92	4.01	10.24	20.94	ns
t_{PHL}				8.34	19.11	38.82	8.96	19.11	35.25	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.81	10.69	24.71	4.09	10.69	22.38	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	8.47	19.84	41.56	9.11	19.84	37.46	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		11.38			11.38		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.71			9.71		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	30	70	140	30	70	130	ps/pF
Δt_{PHL}				70	150	300	80	150	270	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	30	70	160	30	70	140	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	70	160	310	80	160	280	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPH43LJ
4-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	3.74	9.71	21.21	4	9.71	19.29	ns
t_{PHL}				4.87	11.95	25.32	5.22	11.95	23.07	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.93	10.31	23.19	4.21	10.31	20.94	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.91	12.25	26.53	5.27	12.25	24.05	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	5.29	13.46	28.75	5.66	13.46	26.25	ns
t_{PHL}				6.77	16.04	33.43	7.27	16.04	30.38	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	5.48	14.15	31.33	5.88	14.15	28.32	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	6.83	16.39	34.83	7.34	16.39	31.52	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	40	110	220	50	110	200	ps/pF
Δt_{PHL}				50	120	230	60	120	210	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	40	110	230	50	110	210	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	50	120	240	60	120	210	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPH60LJ
6-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPH60LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPH60LJ A,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OH}	High-level output voltage	I_{OH} = −6 mA				3.7			V
		I_{OH} = −5.1 mA	3.7						
V_{OL}	Low-level output voltage	I_{OL} = 6 mA						0.5	V
		I_{OL} = 5.1 mA			0.5				
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.82			0.11	mA
C_i	Input capacitance			0.24			0.24		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		9.3			9.3		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPH60LJ
6-mA TOTEM-POLE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	2.11	6.08	14.15	2.27	6.08	12.82	ns
t_{PHL}				4.04	9.98	20.75	4.35	9.98	18.96	
t_{PLH}	A	Y	C_L = 50 pF	2.84	8.01	18.48	3.05	8.01	16.73	ns
t_{PHL}				5.97	14.05	28.59	6.42	14.05	26.04	
Δt_{PLH}	A	Y		20	60	120	20	60	110	ps/pF
Δt_{PHL}				60	120	220	60	120	200	

CMOS loads, $R_L = \infty$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	C_L = 15 pF	2.76	7.47	16.68	2.97	7.47	15.12	ns
t_{PHL}				3.43	8.72	18.52	3.68	8.72	16.93	
t_{PLH}	A	Y	C_L = 50 pF	3.96	10.39	22.75	4.26	10.39	20.63	ns
t_{PHL}				4.87	11.87	24.75	5.23	11.87	22.56	
Δt_{PLH}	A	Y		30	80	170	40	80	160	ps/pF
Δt_{PHL}				40	90	180	40	90	160	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPH61LJ
6-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt

D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	H

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A

description

The OPH61LJ cell is a noninverting output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPH61LJ A,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage			2.2			2.2		V
V_{OL}	Low-level output voltage	I_{OL} = 6 mA						0.5	V
		I_{OL} = 5.1 mA			0.5				
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±5	µA
I_{CC}	Supply current	$V_I = V_{IH}$ or V_{IL}			0.39			0.11	mA
C_i	Input capacitance			0.09			0.09		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns		0.82			0.82		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPH61LJ
6-mA N-CHANNEL OPEN-DRAIN CMOS/TTL OUTPUT BUFFER WITH 0.125 dt/dt

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TTL loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	3.79	9.67	20.99	4.09	9.67	18.97	ns
t_{PZL}			C_L = 50 pF	5.71	13.78	28.99	6.15	13.78	26.18	
t_{PLZ}	A	Y			9.17			9.17		ns
Δt_{PZL}	A	Y		50	120	230	60	120	210	ps/pF

CMOS loads, R_L = 1 kΩ to V_{CC}

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PZL}	A	Y	C_L = 15 pF	3.19	8.35	18.4	3.43	8.35	16.67	ns
t_{PZL}			C_L = 50 pF	4.62	11.51	24.68	4.97	11.51	22.35	
Δt_{PZL}	A	Y		40	90	180	40	90	160	ps/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

OPH63LJ
6-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt AND ACTIVE-LOW ENABLE

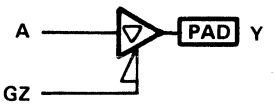
D3030, APRIL 1988

OUTPUT BUFFER CELL

FUNCTION TABLE

INPUTS		OUTPUT
GZ	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

POSITIVE LOGIC EQUATION: Y = A (if GZ is L)

description

The OPH63LJ is a noninverting 3-state output buffer that interfaces internal cells with TTL or CMOS external loads. The buffer incorporates di/dt circuitry designed to reduce the effects of impedance mismatch. When the output buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: OPH63LJ A,GZ,Y;

A pull-up or pull-down terminator can be connected to the Y node.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_T	Input threshold voltage				2.2			2.2		V
V_{OH}	High-level output voltage		I_{OH} = −6 mA				3.7			V
			I_{OH} = −5.1 mA	3.7						
V_{OL}	Low-level output voltage		I_{OL} = 6 mA						0.5	V
			I_{OL} = 5.1 mA			0.5				
I_{OZ}	Off-state output current		V_O = V_{CC} or 0			±10			±5	µA
I_{CC}	Supply current		V_I = V_{IH} or V_{IL}			1.04			0.27	mA
C_i	Input capacitance	A			0.18			0.18		pF
		GZ			0.15			0.15		
C_{pd}	Equivalent power dissipation capacitance		t_r = t_f = 1 ns		13.2			13.2		pF

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OPH63LJ
6-mA 3-STATE CMOS/TTL OUTPUT BUFFER WITH 0.125 di/dt AND ACTIVE-LOW ENABLE

D3030, APRIL 1988

TTL SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	2.54	7.01	15.98	2.17	7.01	14.54	ns
t_{PHL}				4.68	11.35	23.66	5.03	11.35	21.56	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	2.57	7.39	17.17	2.76	7.39	15.58	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.73	11.64	24.78	5.08	11.64	22.46	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	3.24	8.88	20.15	3.46	8.88	18.31	ns
t_{PHL}				6.57	15.31	31.33	7.06	15.31	28.47	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.27	9.26	21.36	3.51	9.26	19.37	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	6.63	15.67	32.66	7.13	15.67	29.52	
t_{PHZ}	GZ	Y	R_L = 1 kΩ to GND		9.86			9.86		ns
t_{PLZ}			R_L = 1 kΩ to V_{CC}		9.06			9.06		

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	20	50	120	20	50	110	ps/pF
Δt_{PHL}				50	110	220	60	110	200	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	20	50	120	20	50	110	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	50	120	230	60	120	200	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

CMOS SWITCHING CHARACTERISTICS

output switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

C_L = 15 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	3.23	8.49	18.67	3.46	8.49	16.99	ns
t_{PHL}				4.01	9.98	21.25	4.3	9.98	19.37	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	3.39	8.98	20.14	3.64	8.98	18.23	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	4.02	10.12	21.85	4.31	10.12	19.84	

C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	4.4	11.33	24.55	4.71	11.33	22.32	ns
t_{PHL}				5.42	13.04	27.34	5.82	13.04	24.86	
t_{PZH}	GZ	Y	R_L = 1 kΩ to GND	4.57	11.84	26.14	4.9	11.84	23.67	ns
t_{PZL}			R_L = 1 kΩ to V_{CC}	5.44	13.2	28.01	5.84	13.2	25.38	

change in propagation delay time with load capacitance over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Δt_{PLH}	A	Y	$R_L = \infty$	30	80	170	40	80	150	ps/pF
Δt_{PHL}				40	90	170	40	90	160	
Δt_{PZH}	GZ	Y	R_L = 1 kΩ to GND	30	80	170	40	80	160	ps/pF
Δt_{PZL}			R_L = 1 kΩ to V_{CC}	40	90	180	40	90	160	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

14 Arithmetic Functions

D3030, APRIL 1988

MAGNITUDE COMPARATORS AND ARITHMETIC FUNCTIONS (SOFTWARE)

DESCRIPTION		CELL NAME	OUTPUT DRIVE	COMMENTS	EQUIVALENT NA210s	PAGE
4-Bit	Magnitude Comparator (P = Q, P < Q, P > Q)	S085LJ	2X	Expandable to N-bit words	50	14-3
4-Bit	ALU Uses Either Active-low or Active-high Data	S181LJ	1X	16 arithmetic operations with ripple and look-ahead carry, also performs 16 logic operations	89	14-8
9-Bit	Parity Generator/ Checker	S280LJ	2X	Odd and even parity outputs	54	14-18
4-Bit	Binary Full Adder	S283LJ	2X	With full carry look-ahead	66.25	14-22
8-Bit	Magnitude Comparator (P = Q, P > Q)	S686LJ	2X	Expandable to N-bit words, each output has an enable input (L)	75.25	14-28
8-Bit	Identity Comparator (P = Q)	S688LJ	2X	Expandable to N-bit words, output has enable input (L)	28.25	14-34

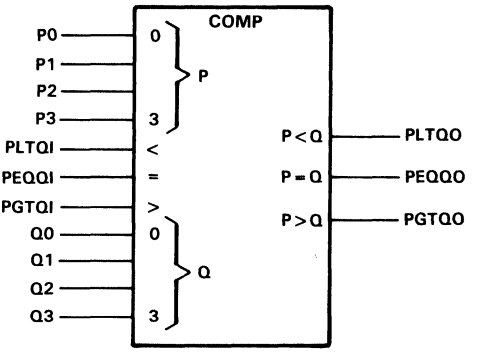
S085LJ
4-BIT MAGNITUDE COMPARATOR

D3030, APRIL 1988

SOFTWARE MACRO

- **Performs Magnitude Comparison of Binary, BCD, and Monotonic Codes**
- **Weighted Cascading Inputs Accomodate Both Serial and Parallel Expansion**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S085LJ software macro implements a 4-bit expandable magnitude comparator. The 4-bit magnitude comparator macro performs comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (P, Q) are made and are available at three outputs. These devices are fully expandable to any number of bits without additional gates. Words of greater length may be compared by connecting comparators in cascade. The PGTQO, PLTQO, and PEQQO outputs of a stage handling less significant bits are connected to the corresponding PGTQI, PLTQI, and PEQQI inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the PEQQI input. The cascading path of the S085LJ is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

The S085LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AO221LJ	1.75	4	7	0.88
IV120LJ	1	3	3	0.93
NA210LJ	1	6	6	1.14
NA310LJ	1.25	2	2.5	0.38
NA410LJ	1.5	2	3	0.38
NA510LJ	3	7	21	6.16
NA810LJ	3.75	2	7.5	1.82
TOTALS		26	50	11.69

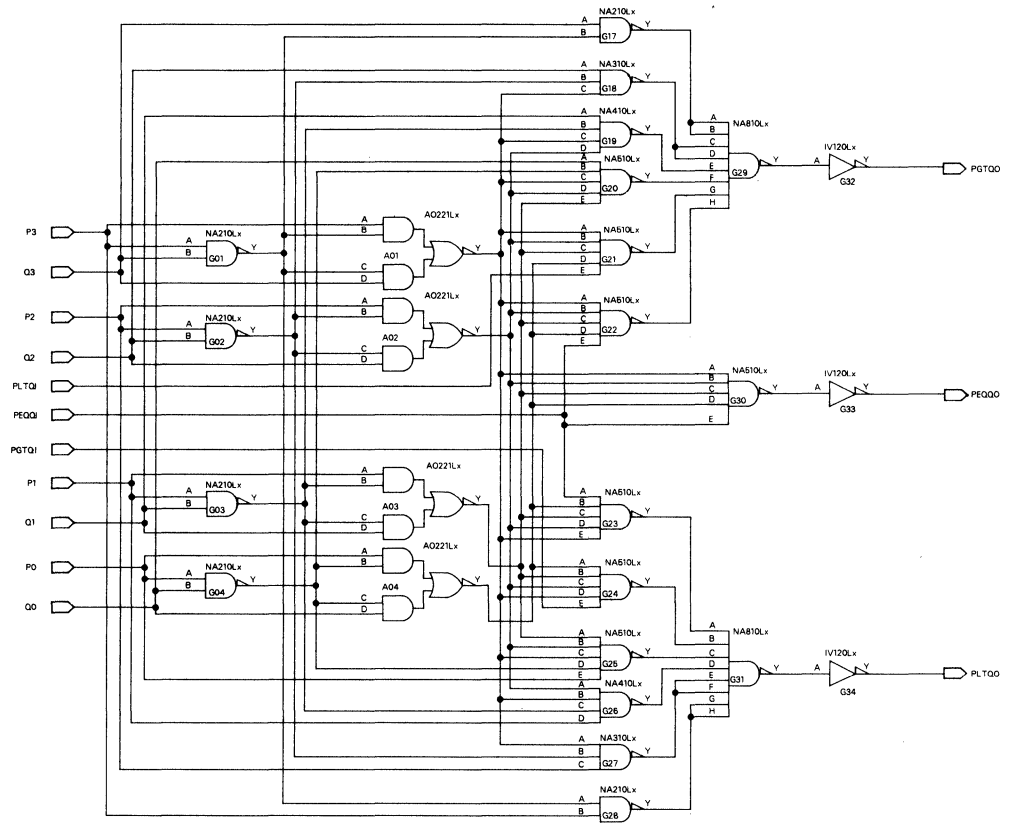
When the comparator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S085LJ P3,P2,P1,P0,Q3,Q2,Q1,Q0,PGTQI,PLTQI,PEQQI,PGTQO,PLTQO,PEQQO;

FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
P3, Q3	P2, Q2	P1, Q1	P0, Q0	PGTQI	PLTQI	PEQQI	PGTQO	PLTQO	PEQQO
P3 > Q3	X	X	X	X	X	X	H	L	L
P3 < Q3	X	X	X	X	X	X	L	H	L
P3 = Q3	P2 > Q2	X	X	X	X	X	H	L	L
P3 = Q3	P2 < Q2	X	X	X	X	X	L	H	L
P3 = Q3	P2 = Q2	P1 > Q1	X	X	X	X	H	L	L
P3 = Q3	P2 = Q2	P1 < Q1	X	X	X	X	L	H	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 > Q0	X	X	X	H	L	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 < Q0	X	X	X	L	H	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	H	L	L	H	L	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	L	H	L	L	H	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	X	X	H	L	L	H
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	H	H	L	L	L	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	L	L	L	H	H	L

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	PEQQI		0.18		pF
		PGTQI, PLTQI		0.06		
		All others		0.18		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	11.69		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Pn, Qn	PGTQO,PLTQO		4.6	9.6		4.6	6.8	ns
t_{PHL}				5.6	12.2		5.6	8.6	
t_{PLH}	Pn, Qn	PEQQO		4.6	9.8		4.6	7.4	ns
t_{PHL}				2.9	5.8		2.9	4.3	
t_{PLH}	PLTQI,PEQQI	PLTQO		2.3	5.3		2.3	2.8	ns
t_{PHL}				2.4	5		2.4	2.7	
t_{PLH}	PGTQI,PEQQI	PGTQO		2.3	4.8		2.3	2.6	ns
t_{PHL}				2.4	3.8		2.4	2.7	
t_{PLH}	PEQQI	PEQQO		1.4	2.7		1.4	1.5	ns
t_{PHL}				1.1	2.3		1.1	1.3	
Δt_{PLH}	Any	Any	0.24	0.52	1.1	0.26	0.52	1	ns/pF
Δt_{PHL}			0.28	0.42	0.68	0.28	0.42	0.62	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE†

```
BLOCK S085LJ;
P3      @INPUT;
P2      @INPUT;
P1      @INPUT;
P0      @INPUT;
Q3      @INPUT;
Q2      @INPUT;
Q1      @INPUT;
Q0      @INPUT;
PGTQI   @INPUT;
PLTQI   @INPUT;
PEQQI   @INPUT;
PGTQO   @OUTPUT;
PLTQO   @OUTPUT;
PEQQO   @OUTPUT;
STRUCTURE
AO1     :AO221LJ  P3,G1O,G1O,Q3,AO1O;
AO2     :AO221LJ  P2,G2O,G2O,Q2,AO2O;
AO3     :AO221LJ  P1,G3O,G3O,Q1,AO3O;
AO4     :AO221LJ  P0,G4O,G4O,Q0,AO4O;
G01     :NA210LJ  P3,Q3,G1O;
G02     :NA210LJ  P2,Q2,G2O;
G03     :NA210LJ  P1,Q1,G3O;
G04     :NA210LJ  P0,Q0,G4O;
G17     :NA210LJ  Q3,G1O,G17O;
G18     :NA310LJ  Q2,G2O,AO1O,G18O;
G19     :NA410LJ  Q1,G3O,AO1O,AO2O,G19O;
G20     :NA510LJ  Q0,G4O,AO1O,AO2O,AO3O,G20O;
G21     :NA510LJ  AO1O,AO2O,AO3O,AO4O,PLTQI,G21O;
G22     :NA510LJ  AO1O,AO2O,AO3O,AO4O,PEQQI,G22O;
G23     :NA510LJ  PEQQI,AO4O,AO3O,AO2O,AO1O,G23O;
G24     :NA510LJ  AO4O,AO3O,AO2O,AO1O,PGTQI,G24O;
G25     :NA510LJ  AO3O,AO2O,AO1O,G4O,P0,G25O;
G26     :NA410LJ  AO2O,AO1O,G3O,P1,G26O;
G27     :NA310LJ  AO1O,G2O,P2,G27O;
G28     :NA210LJ  G1O,P3,G28O;
G29     :NA810LJ  G17O,G17O,G18O,G18O,G19O,G20O,G21O,
                  G22O,G29O;
G30     :NA510LJ  AO1O,AO2O,AO3O,AO4O,PEQQI,G30O;
G31     :NA810LJ  G23O,G24O,G25O,G26O,G27O,G27O,G28O,
                  G28O,G31O;
G32     :IV120LJ  G29O,PGTQO;
G33     :IV120LJ  G30O,PEQQO;
G34     :IV120LJ  G31O,PLTQO;
END S085LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

S181LJ
ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

D3030, APRIL 1988

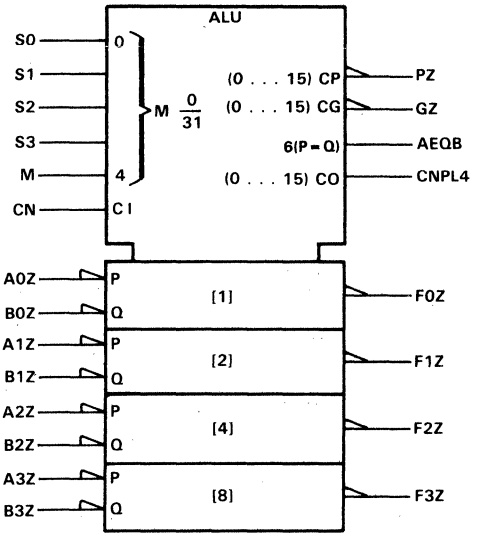
SOFTWARE MACRO

- Performs Full 16-Function Arithmetic or Boolean Combinations of Two Variables
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
  - Exclusive-OR
  - Comparator
  - AND,NAND,OR,NOR
  - Plus Ten Other Logic Operations

description

The S181LJ software macro implements a 4-bit arithmetic logic unit. The S181LJ performs 16 arithmetic or Boolean operations on two 4-bit binary words as shown in function Tables 1 and 2. Choice between the two operating modes is established by the mode control, M, and selection of one-of-sixteen operations is accomplished at the select inputs, S3,S2,S1, and S0.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

The S181LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN210LJ	1.5	9	13.5	2.97
AN310LJ	1.75	9	15.75	3.42
AN420LJ	2.25	1	2.25	0.6
EX210LJ	1.75	4	7	1.44
EX220LJ	2	4	8	2.12
IV110LJ	0.75	8	6	1.28
IV120LJ	1	1	1	0.31
NA210LJ	1	4	4	0.76
NA220LJ	1.5	1	1.5	0.38
NA310LJ	1.25	4	5	0.76
NA410LJ	1.5	6	9	1.14
NA510LJ	3	2	6	1.76
NO210LJ	1	5	5	0.6
NO310LJ	1.25	4	5	0.52
TOTALS		62	89	18.06

When the arithmetic logic unit/function generator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S181LJ A3Z,A2Z,A1Z,A0Z,B3Z,B2Z,B1Z,B0Z,CN,M,S3,S2,S1,
S0,F3Z,F2Z,F1Z,F0Z,AEQB,GZ,PZ,CNPL4;

When the mode control input is low, the 16 arithmetic operations are accessible via the four select inputs. The 4-bit full adder incorporates both ripple and look-ahead carry circuitry providing the capability to extend either technique across expanded word widths when multiple S181LJs are used in parallel.

The S181LJ accomodates both active-high and active-low data simply by redefining the designations used to describe the data inputs and outputs. For use with active-low data, use Table 1 and the input/output designations provided for the label developed above. For use with active-high data, use Table 2.

Note that only the relationship of A, B, and F data with respect to the carry and look-ahead circuitry are affected.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B. Arithmetic operations with and without carry are shown in Tables 1 and 2.

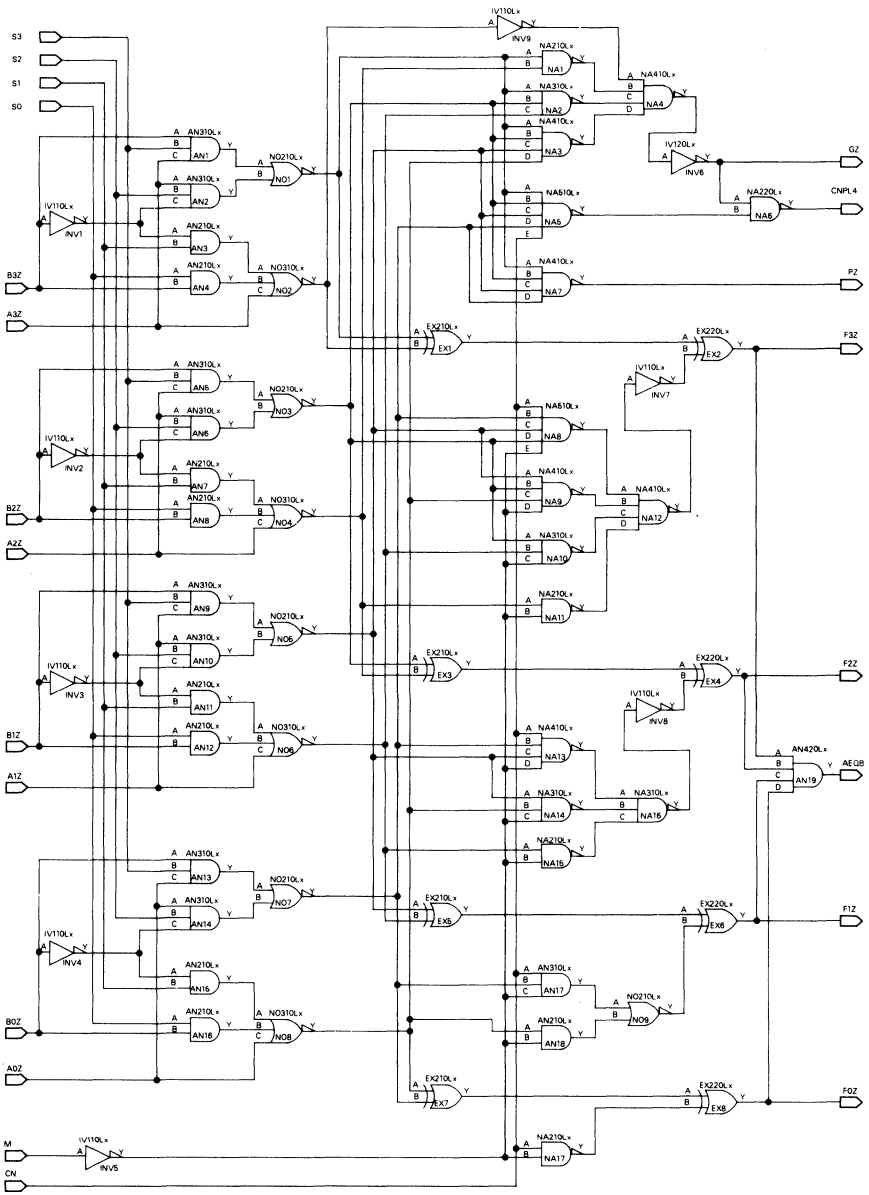
The S181LJ also performs a comparison of the A and B operands. The AEQB output is decoded from the function outputs (F3, F2, F1, and F0) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with CN = H when performing this comparison. The AEQB output can be AND or NAND gated to perform comparisons over expanded ALUs. The CNPL4 carry output can also be used to supply relative magnitude information. Again, the ALU must be in the subtract mode by having the select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT CN	OUTPUT CNPL4	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	A>B	A<B
H	L	A<B	A>B
L	H	A>B	A<B
L	L	A<B	A>B

S181LJ
ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

D3030, APRIL 1988

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

signal designations

The polarity indicators (open arrowheads) in both Figures 1 and 2 indicate that the associated input or output is active-low with respect to the function shown inside the symbol, and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations used in Figure 2 accommodate the logic functions and arithmetic operations for the active-high data given in Table 2.

FIGURE 1

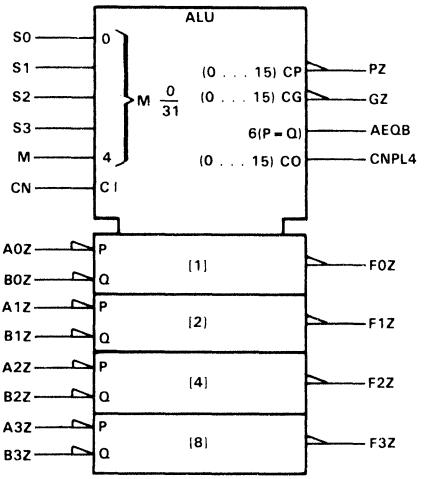
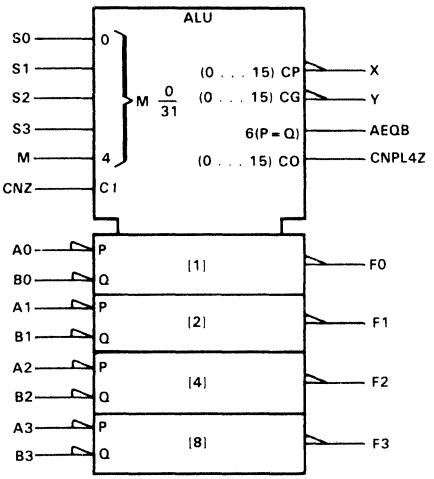


FIGURE 2



D3030, APRIL 1988

TABLE 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	CN = L (no carry)	CN = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A$\oplus$B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

*Each bit is shifted to the next more significant position.

TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	CNZ = H (no carry)	CNZ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A + B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A + B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	A = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

*Each bit is shifted to the next more significant position.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	An, Bn		0.16		pF
		CN		0.27		
		M		0.05		
		Sn		0.2		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	18.1		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CN	CNPL4		1.5	2.8		1.5	2.7	ns
t_{PHL}				1.2	2.4		1.2	2.1	
t_{PLH}	AnZ or BnZ	CNPL4 SUM		4.2	8.9		4.2	8.4	ns
t_{PHL}				4.3	8.9		4.3	8.1	
t_{PLH}	CN	Fn‡		2.8	6.1		2.8	5.4	ns
t_{PHL}				2.8	6.4		2.8	5.7	
t_{PLH}	AnZ or BnZ	GZ SUM		4	8.3		4	7.7	ns
t_{PHL}				4.5	9.5		4.5	8.9	
t_{PLH}	AnZ or BnZ	PZ SUM		2.5	5		2.5	4.6	ns
t_{PHL}				3.5	7.4		3.5	6.8	
t_{PLH}	AiZ or BnZ	FiZ SUM		4.5	9.9		4.5	9.1	ns
t_{PHL}				4.8	10.8		4.8	9.8	
t_{PLH}	AnZ or BnZ	AEQB DIFF		5.3	11.3		5.3	10.3	ns
t_{PHL}				4.6	10.9		4.6	10	
Δt_{PLH}	Any	CNPL4	0.22	0.5	1.08	0.24	0.5	1	ns/pF
Δt_{PHL}			0.28	0.48	1.02	0.28	0.48	0.9	
Δt_{PLH}	AnZ or BnZ	GZ	0.24	0.52	1.1	0.26	0.52	1	ns/pF
Δt_{PHL}			0.28	0.42	0.68	0.28	0.42	0.62	
Δt_{PLH}	AnZ or BnZ	PZ	0.4	1.88	3.96	0.44	1.88	3.64	ns/pF
Δt_{PHL}			0.52	1.64	3.84	0.56	1.64	3.46	
Δt_{PLH}	Any	FiZ	0.2	0.52	1.14	0.22	0.52	1.04	ns/pF
Δt_{PHL}			0.2	0.6	1.36	0.24	0.6	1.24	
Δt_{PLH}	Any	AEQB	0.18	0.58	1.26	0.2	0.58	1.16	ns/pF
Δt_{PHL}			0.16	0.38	0.78	0.18	0.38	0.7	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The test mode is SUM or DIFF.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE†

```
BLOCK S181LJ;
A3Z       @INPUT;
A2Z       @INPUT;
A1Z       @INPUT;
A0Z       @INPUT;
B3Z       @INPUT;
B2Z       @INPUT;
B1Z       @INPUT;
B0Z       @INPUT;
CN        @INPUT;
M         @INPUT;
S3        @INPUT;
S2        @INPUT;
S1        @INPUT;
S0        @INPUT;
F3Z       @OUTPUT;
F2Z       @OUTPUT;
F1Z       @OUTPUT;
F0Z       @OUTPUT;
AEQB      @OUTPUT;
GZ        @OUTPUT;
PZ        @OUTPUT;
CNPL4     @OUTPUT;

STRUCTURE
AN1       :AN310LJ  B3Z,S3,A3Z,AN1O;
AN10      :AN310LJ  A1Z,S2,INV3O,AN10O;
AN11      :AN210LJ  INV3O,S1,AN11O;
AN12      :AN210LJ  S0,B1Z,AN12O;
AN13      :AN310LJ  B0Z,S3,A0Z,AN13O;
AN14      :AN310LJ  A0Z,S2,INV4O,AN14O;
AN15      :AN210LJ  INV4O,S1,AN15O;
AN16      :AN210LJ  S0,B0Z,AN16O;
AN17      :AN310LJ  CN,NO7O,INV5O,AN17O;
AN18      :AN210LJ  NO8O,INV5O,AN18O;
AN19      :AN420LJ  F3Z,F2Z,F1Z,F0Z,AEQB;
AN2       :AN310LJ  A3Z,S2,INV1O,AN2O;
AN3       :AN210LJ  INV1O,S1,AN3O;
AN4       :AN210LJ  S0,B3Z,AN4O;
AN5       :AN310LJ  B2Z,S3,A2Z,AN5O;
AN6       :AN310LJ  A2Z,S2,INV2O,AN6O;
AN7       :AN210LJ  INV2O,S1,AN7O;
AN8       :AN210LJ  S0,B2Z,AN8O;
AN9       :AN310LJ  B1Z,S3,A1Z,AN9O;
EX1       :EX210LJ  NO1O,NO2O,EX1O;
EX2       :EX220LJ  EX1O,INV7O,F3Z;
EX3       :EX210LJ  NO3O,NO4O,EX3O;
EX4       :EX220LJ  EX3O,INV8O,F2Z;
EX5       :EX210LJ  NO5O,NO6O,EX5O;
EX6       :EX220LJ  EX5O,NO9O,F1Z;
EX7       :EX210LJ  NO8O,NO7O,EX7O;
EX8       :EX220LJ  EX7O,NA17O,F0Z;
INV1      :IV110LJ  B3Z,INV1O;
INV2      :IV110LJ  B2Z,INV2O;
INV3      :IV110LJ  B1Z,INV3O;
INV4      :IV110LJ  B0Z,INV4O;
INV5      :IV110LJ  M,INV5O;
INV6      :IV120LJ  NA4O,GZ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

HDL FILE† (Continued)

```
INV7        :IV110LJ    NA12O,INV7O;
INV8        :IV110LJ    NA16O,INV8O;
INV9        :IV110LJ    NO2O,INV9O;
NA1         :NA210LJ    NO1O,NO4O,NA1O;
NA10        :NA310LJ    NO3O,NO6O,INV5O,NA10O;
NA11        :NA210LJ    NO4O,INV5O,NA11O;
NA12        :NA410LJ    NA8O,NA9O,NA10O,NA11O,NA12O;
NA13        :NA410LJ    CN,NO7O,NO5O,INV5O,NA13O;
NA14        :NA310LJ    NO5O,NO8O,INV5O,NA14O;
NA15        :NA210LJ    NO6O,INV5O,NA15O;
NA16        :NA310LJ    NA13O,NA14O,NA15O,NA16O;
NA17        :NA210LJ    CN,INV5O,NA17O;
NA2         :NA310LJ    NO1O,NO3O,NO6O,NA2O;
NA3         :NA410LJ    NO1O,NO3O,NO5O,NO8O,NA3O;
NA4         :NA410LJ    INV9O,NA1O,NA2O,NA3O,NA4O;
NA5         :NA510LJ    NO1O,NO3O,NO5O,NO7O,CN,NA5O;
NA6         :NA220LJ    GZ,NA5O,CNPL4;
NA7         :NA410LJ    NO1O,NO3O,NO5O,NO7O,PZ;
NA8         :NA510LJ    CN,NO7O,NO5O,NO3O,INV5O,NA8O;
NA9         :NA410LJ    NO5O,NO3O,NO8O,INV5O,NA9O;
NO1         :NO210LJ    AN1O,AN2O,NO1O;
NO2         :NO310LJ    AN3O,AN4O,A3Z,NO2O;
NO3         :NO210LJ    AN5O,AN6O,NO3O;
NO4         :NO310LJ    AN7O,AN8O,A2Z,NO4O;
NO5         :NO210LJ    AN9O,AN10O,NO5O;
NO6         :NO310LJ    AN11O,AN12O,A1Z,NO6O;
NO7         :NO210LJ    AN13O,AN14O,NO7O;
NO8         :NO310LJ    AN15O,AN16O,A0Z,NO8O;
NO9         :NO210LJ    AN17O,AN18O,NO9O;
END S181LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

S280LJ
9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

D3030, APRIL 1988

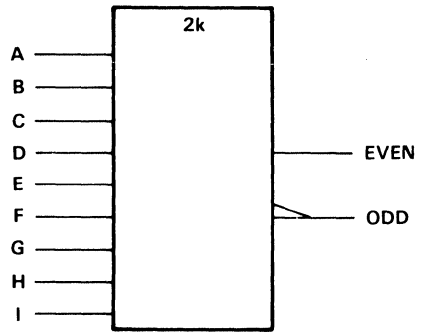
SOFTWARE MACRO

- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bits**

description

The S280LJ software macro implements a parallel 9-bit parity generator. The 9-bit configuration simplifies construction of large parity generators. These universal 9-bit parity generator/checker macros feature odd and even outputs to facilitate operation in either odd- or even-parity applications. The word-length capability is easily expanded by cascading. The S280LJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	EVEN	ODD
0,2,4,6,8	H	L
1,3,5,7,9	L	H

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV110LJ	0.75	18	13.5	2.88
IV120LJ	1	5	5	1.55
NA310LJ	1.25	20	25	3.8
NA410LJ	1.5	2	3	0.38
NA420LJ	2.5	3	7.5	1.17
TOTALS		48	54	9.78

When the parity generator/checker is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

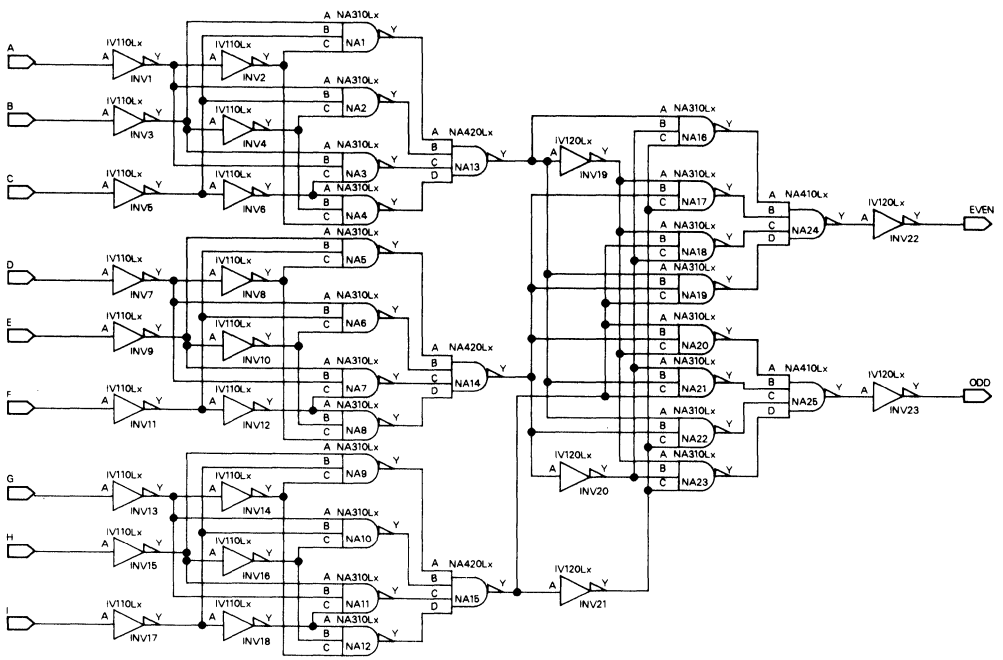
Label: S280LJ A,B,C,D,E,G,H,I,EVEN,ODD;

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S280LJ
9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

D3030, APRIL 1988

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	Any input		0.05		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	9.8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any	EVEN		4.5	8.8		4.5	8.2	ns
t_{PHL}				4.3	8.7		4.3	7.8	
t_{PLH}	Any	ODD		4.8	9.4		4.8	8.7	ns
t_{PHL}				4.8	9.8		4.8	9.2	
Δt_{PLH}	Any	Any	0.24	0.52	1.1	0.26	0.52	1	ns/pF
Δt_{PHL}			0.28	0.42	0.68	0.28	0.42	0.62	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE‡

```
BLOCK S280LJ;                  STRUCTURE
A          @INPUT;             INV1     :IV110LJ   A,INV1O;
B          @INPUT;             INV10    :IV110LJ   INV9O,INV10O;
C          @INPUT;             INV11    :IV110LJ   F,INV11O;
D          @INPUT;             INV12    :IV110LJ   INV11O,INV12O;
E          @INPUT;             INV13    :IV110LJ   G,INV13O;
F          @INPUT;             INV14    :IV110LJ   INV13O,INV14O;
G          @INPUT;             INV15    :IV110LJ   H,INV15O;
H          @INPUT;             INV16    :IV110LJ   INV15O,INV16O;
I          @INPUT;             INV17    :IV110LJ   I,INV17O;
EVEN       @OUTPUT;            INV18    :IV110LJ   INV17O,INV18O;
ODD        @OUTPUT;            INV19    :IV120LJ   SNA13,SIV19;
                               INV2     :IV110LJ   INV1O,INV2O;
                               INV20    :IV120LJ   SNA14,SIV20;
                               INV21    :IV120LJ   SNA15,SIV21;
                               INV22    :IV120LJ   SNA24,EVEN;
                               INV23    :IV120LJ   SNA25,ODD;
                               INV3     :IV110LJ   B,INV3O;
                               INV4     :IV110LJ   INV3O,INV4O;
                               INV5     :IV110LJ   C,INV5O;
                               INV6     :IV110LJ   INV5O,INV6O;
                               INV7     :IV110LJ   D,INV7O;
```

‡ The HDL netlist format requires the "STRUCTURE" program lines to follow the"BLOCK" I/O program lines.

HDL FILE† (Continued)

```
INV8      :IV110LJ    INV7O,INV8O;
INV9      :IV110LJ    E,INV9O;
NA1       :NA310LJ    INV3O,INV5O,INV2O,SNA1;
NA10      :NA310LJ    INV13O,INV17O,INV16O,SNA10;
NA11      :NA310LJ    INV15O,INV13O,INV18O,SNA11;
NA12      :NA310LJ    INV18O,INV16O,INV14O,SNA12;
NA13      :NA420LJ    SNA1,SNA2,SNA3,SNA4,SNA13;
NA14      :NA420LJ    SNA5,SNA6,SNA7,SNA8,SNA14;
NA15      :NA420LJ    SNA9,SNA10,SNA11,SNA12,SNA15;
NA16      :NA310LJ    SNA13,SIV20,SIV21,SNA16;
NA17      :NA310LJ    SIV19,SNA14,SIV21,SNA17;
NA18      :NA310LJ    SIV19,SNA15,SIV20,SNA18;
NA19      :NA310LJ    SNA13,SNA14,SNA15,SNA19;
NA2       :NA310LJ    INV1O,INV5O,INV4O,SNA2;
NA20      :NA310LJ    SNA15,SNA14,SIV19,SNA20;
NA21      :NA310LJ    SIV20,SNA13,SNA15,SNA21;
NA22      :NA310LJ    SNA13,SNA14,SIV21,SNA22;
NA23      :NA310LJ    SIV19,SIV20,SIV21,SNA23;
NA24      :NA410LJ    SNA16,SNA17,SNA18,SNA19,SNA24;
NA25      :NA410LJ    SNA20,SNA21,SNA22,SNA23,SNA25;
NA3       :NA310LJ    INV3O,INV1O,INV6O,SNA3;
NA4       :NA310LJ    INV6O,INV4O,INV2O,SNA4;
NA5       :NA310LJ    INV9O,INV11O,INV8O,SNA5;
NA6       :NA310LJ    INV7O,INV11O,INV10O,SNA6;
NA7       :NA310LJ    INV9O,INV7O,INV12O,SNA7;
NA8       :NA310LJ    INV12O,INV10O,INV8O,SNA8;
NA9       :NA310LJ    INV15O,INV17O,INV14O,SNA9;
END S280LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

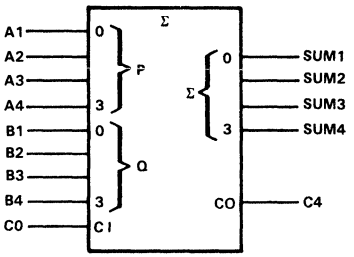
S283LJ
4-BIT BINARY FULL ADDER WITH FAST CARRY

D3030, APRIL 1988

SOFTWARE MACRO

- **Full-Carry Look-Ahead Across the Four Bits**
- **Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S283LJ software macro implements a parallel 4-bit binary full adder. The 4-bit configuration provides a fully designed, fast-carry adder and simplifies construction of large adders. These full adders perform the addition of two 4-bit binary words. The sum outputs are provided for each bit and the resultant carry (C4) is generated in parallel from the four bits. These adders feature full-carry look-ahead across all four bits, providing the system designer with built-in partial look-ahead. The adder logic, including the carry, is implemented in its true form. End around carry can be accomplished without the need for logic or level inversion. The S283LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN220LJ	1.75	5	8.75	2.35
EX220LJ	2	4	8	2.12
IV110LJ	0.75	10	7.5	1.6
IV120LJ	1	2	2	0.62
NA220LJ	1.5	7	10.5	2.66
NA320LJ	2	4	8	1.48
NA420LJ	2.5	3	7.5	1.17
NA520LJ	3.25	2	6.5	2.1
NO220LJ	1.5	5	7.5	1.15
TOTALS		42	66.25	15.25

When the full adder is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S283LJ A4,A3,A2,A1,B4,B3,B2,B1,C0,SUM4,SUM3,SUM2,SUM1,C4;

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S283LJ
4-BIT BINARY FULL ADDER WITH FAST CARRY

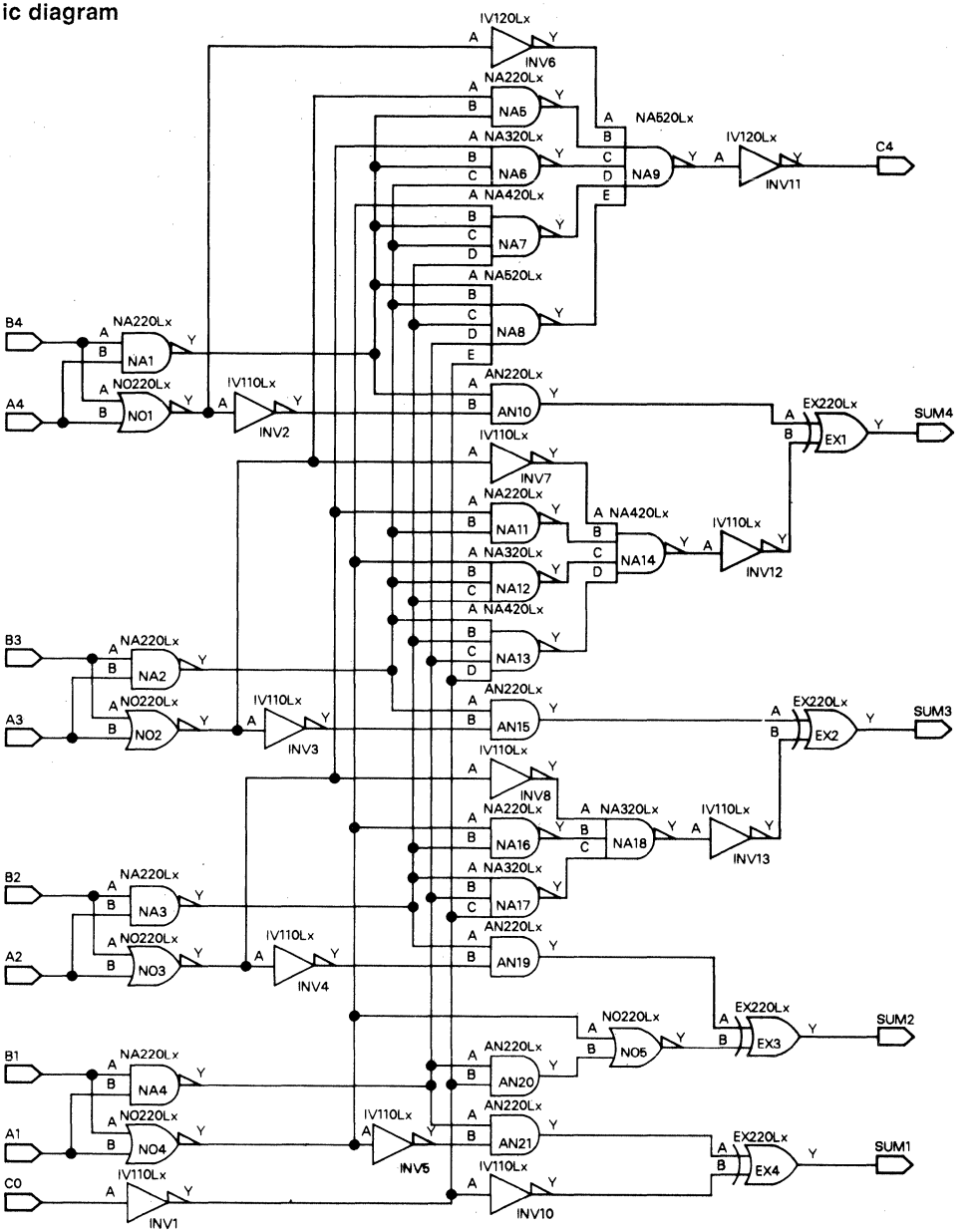
D3030, APRIL 1988

FUNCTION TABLE

INPUTS				OUTPUTS					
				WHEN C0 = L			WHEN C0 = H		
				WHEN C2 = L			WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	SUM1 / SUM3	SUM2 / SUM4	C2 / C4	SUM1 / SUM3	SUM2 / SUM4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs SUM1 and SUM2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs SUM3, SUM4, and C4.

logic diagram



S283LJ
4-BIT BINARY FULL ADDER WITH FAST CARRY

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	An, Bn		0.23		pF
		C0		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	15.3		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	C0	SUMn		2.7	6		2.7	3.4	ns
t_{PHL}				2.8	5.9		2.8	3.4	
t_{PLH}	An, Bn	SUMn		2.2	5.7		2.2	4.1	ns
t_{PHL}				2.8	5.7		2.8	5.2	
t_{PLH}	C0	C4		3	5.9		3	5.5	ns
t_{PHL}				3.1	6.6		3.1	6.2	
t_{PLH}	An, Bn	C4		3.1	6		3.1	5.4	ns
t_{PHL}				3	5		3	4.7	
Δt_{PLH}	Any	C4	0.24	0.52	1.1	0.26	0.52	1	ns/pF
Δt_{PHL}			0.28	0.42	0.68	0.28	0.42	0.62	
Δt_{PLH}	Any	SUMn	0.2	0.52	1.14	0.22	0.52	1.04	ns/pF
Δt_{PHL}			0.2	0.6	1.36	0.24	0.6	1.24	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE†

```
BLOCK S283LJ;
A4      @INPUT;
A3      @INPUT;
A2      @INPUT;
A1      @INPUT;
B4      @INPUT;
B3      @INPUT;
B2      @INPUT;
B1      @INPUT;
C0      @INPUT;
SUM4    @OUTPUT;
SUM3    @OUTPUT;
SUM2    @OUTPUT;
SUM1    @OUTPUT;
C4      @OUTPUT;

STRUCTURE
EX1     :EX220LJ  AN10O,INV12O,SUM4;
EX2     :EX220LJ  AN15O,INV13O,SUM3;
EX3     :EX220LJ  AN19O,NO5O,SUM2;
EX4     :EX220LJ  AN21O,INV10O,SUM1;
INV1    :IV110LJ  C0,INV1O;
INV10   :IV110LJ  INV1O,INV10O;
INV11   :IV120LJ  NA9O,C4;
INV12   :IV110LJ  NA14O,INV12O;
INV13   :IV110LJ  NA18O,INV13O;
INV2    :IV110LJ  NO1O,INV2O;
INV3    :IV110LJ  NO2O,INV3O;
INV4    :IV110LJ  NO3O,INV4O;
INV5    :IV110LJ  NO4O,INV5O;
INV6    :IV120LJ  NO1O,INV6O;
INV7    :IV110LJ  NO2O,INV7O;
INV8    :IV110LJ  NO3O,INV8O;
NA1     :NA220LJ  B4,A4,NA1O;
AN10    :AN220LJ  NA1O,INV2O,AN10O;
NA11    :NA220LJ  NO3O,NA2O,NA11O;
NA12    :NA320LJ  NO4O,NA2O,NA3O,NA12O;
NA13    :NA420LJ  NA2O,NA3O,NA4O,INV1O,NA13O;
NA14    :NA420LJ  INV7O,NA11O,NA12O,NA13O,NA14O;
AN15    :AN220LJ  NA2O,INV3O,AN15O;
NA16    :NA220LJ  NO4O,NA3O,NA16O;
NA17    :NA320LJ  NA3O,NA4O,INV1O,NA17O;
NA18    :NA320LJ  INV8O,NA16O,NA17O,NA18O;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

HDL FILE† (Continued)

```
AN19      :AN220LJ   NA3O,INV4O,AN19O;
NA2       :NA220LJ   B3,A3,NA2O;
AN20      :AN220LJ   NA4O,INV1O,AN20O;
AN21      :AN220LJ   NA4O,INV5O,AN21O;
NA3       :NA220LJ   B2,A2,NA3O;
NA4       :NA220LJ   B1,A1,NA4O;
NA5       :NA220LJ   NO2O,NA1O,NA5O;
NA6       :NA320LJ   NO3O,NA1O,NA2O,NA6O;
NA7       :NA420LJ   NO4O,NA1O,NA2O,NA3O,NA7O;
NA8       :NA520LJ   NA1O,NA2O,NA3O,NA4O,INV1O,NA8O;
NA9       :NA520LJ   INV6O,NA5O,NA6O,NA7O,NA8O,NA9O;
NO1       :NO220LJ   B4,A4,NO1O;
NO2       :NO220LJ   B3,A3,NO2O;
NO3       :NO220LJ   B2,A2,NO3O;
NO4       :NO220LJ   B1,A1,NO4O;
NO5       :NO220LJ   NO4O,AN20O,NO5O;
END S283LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

S686LJ
8-BIT MAGNITUDE COMPARATOR

D3030, APRIL 1988

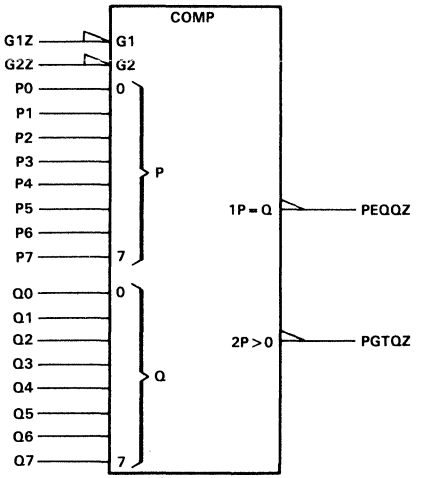
SOFTWARE MACRO

- **Performs Magnitude Comparison of Binary, BCD, and Monotonic Codes**
- **Weighted Cascading Inputs Accomodate Both Serial and Parallel Expansion**

description

The S686LJ software macro implements an 8-bit expandable magnitude comparator. The 8-bit configuration simplifies construction of wider comparators. These 8-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Two fully decoded decisions, P > Q or P = Q, about two eight-bit words (P,Q) are made and are externally available at two outputs that can be decoded with a NAND gate to provide the P < Q decision. These devices are fully expandable to any number of bits. Words of greater length may be compared by connecting comparators in cascade. The PEQQZ and PGTQZ outputs of a stage handling less-significant bits are connected to the corresponding G1Z and G2Z inputs of the next stage handling more-significant bits.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

The S686LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN210LJ	1.5	4	6	1.32
AN310LJ	1.75	7	12.25	2.66
AN410LJ	2	6	12	2.52
EX210LJ	1.75	8	14	2.88
IV110LJ	0.75	13	9.75	2.08
IV120LJ	1	5	5	1.55
NA210LJ	1	4	4	0.76
NA310LJ	1.25	3	3.75	0.57
NA410LJ	1.5	3	4.5	0.57
NA420LJ	2.5	1	2.5	0.39
NO220LJ	1.5	1	1.5	0.23
TOTALS		55	75.25	15.53

When the magnitude comparator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S686LJ P0,P1,P2,P3,P4,P5,P6,P7,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7,G1Z,G2Z,PEQQZ, PGTQZ;

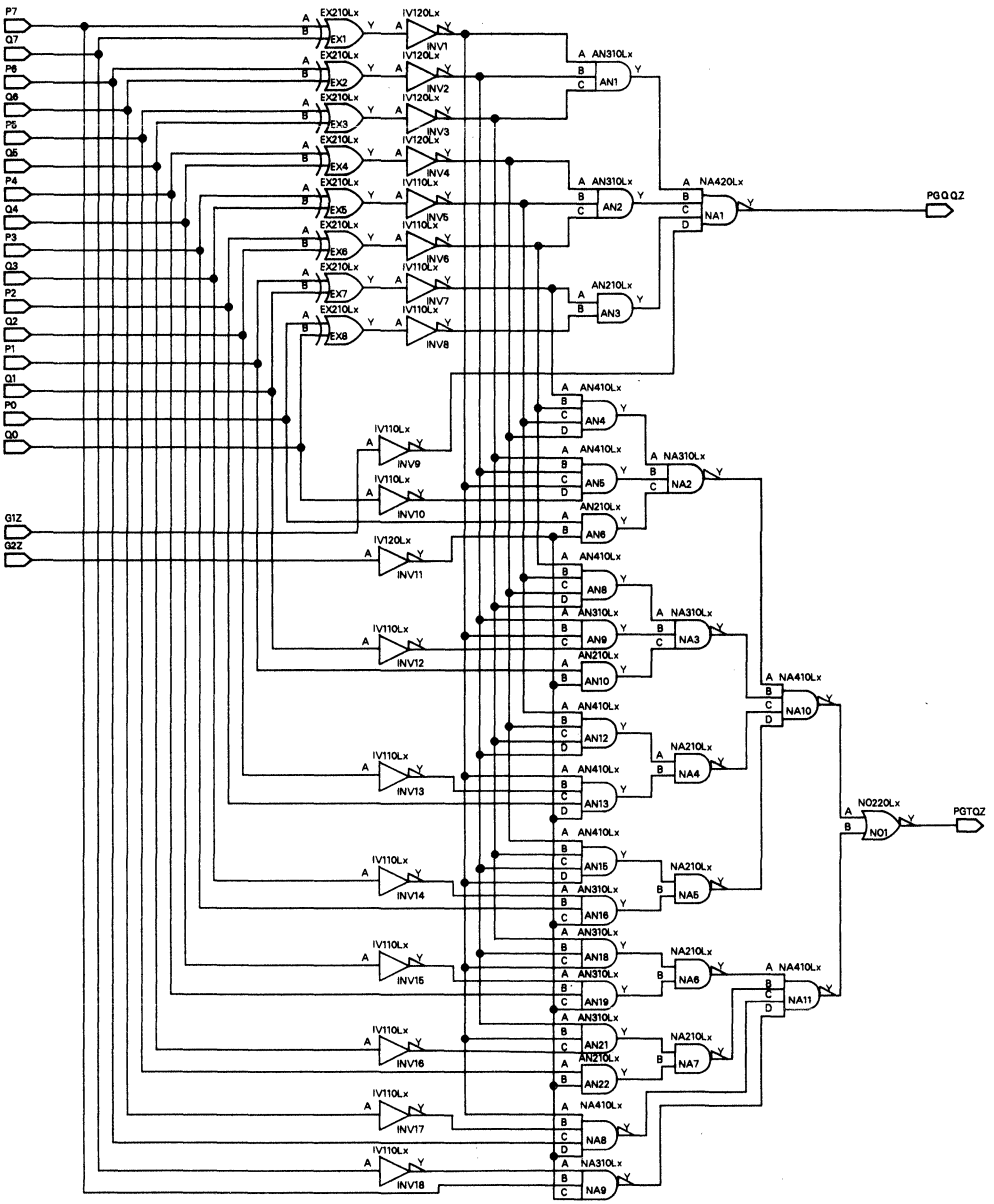
FUNCTION TABLE

INPUTS			OUTPUTS‡	
DATA	ENABLES†		PEQQZ	PGTQZ
Pn, Qn	G1Z	G2Z		
P = Q	L	X	L	H
P > Q	X	L	H	L
P < Q	X	X	H	H
P = Q	H	X	H	H
P > Q	X	H	H	H
X	H	H	H	H

† G1Z enables PEQQZ, and G2Z enables PGTQZ.

‡ The P < Q function can be generated by applying the PEQQZ and PGTQZ outputs to a 2-input NAND gate.

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	G1Z		0.05		pF
		G2Z		0.11		
		Any P or Q		0.13		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	15		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Pn, Qn	Any		2.6	6		2.6	5.6	ns
t_{PHL}				2.9	8.2		2.9	7.6	
t_{PLH}	G1Z, G2Z	Any		2	5.9		2	5.5	ns
t_{PHL}				2.1	6.3		2.1	5.9	
Δt_{PLH}	Any	Any	0.22	0.98	2.22	0.24	0.98	2.04	ns/pF
Δt_{PHL}			0.26	0.78	1.82	0.28	0.78	1.62	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE†

```
BLOCK S686LJ;
P0      @INPUT;
P1      @INPUT;
P2      @INPUT;
P3      @INPUT;
P4      @INPUT;
P5      @INPUT;
P6      @INPUT;
P7      @INPUT;
Q0      @INPUT;
Q1      @INPUT;
Q2      @INPUT;
Q3      @INPUT;
Q4      @INPUT;
Q5      @INPUT;
Q6      @INPUT;
Q7      @INPUT;
G1Z     @INPUT;
G2Z     @INPUT;
PEQQZ   @OUTPUT;
PGTQZ   @OUTPUT;
STRUCTURE
AN1     :AN310LJ  INV1O,INV2O,INV3O,AN1O;
AN10    :AN210LJ  P1,INV11O,AN10O;
AN12    :AN410LJ  INV5O,INV4O,INV3O,INV2O,AN12O;
AN13    :AN410LJ  INV1O,INV13O,P2,INV11O,AN13O;
AN15    :AN410LJ  INV4O,INV3O,INV2O,INV1O,AN15O;
AN16    :AN310LJ  INV14O,P3,INV11O,AN16O;
AN18    :AN310LJ  INV3O,INV2O,INV1O,AN18O;
AN19    :AN310LJ  INV15O,P4,INV11O,AN19O;
AN2     :AN310LJ  INV4O,INV5O,INV6O,AN2O;
AN21    :AN310LJ  INV2O,INV1O,INV16O,AN21O;
AN22    :AN210LJ  P5,INV11O,AN22O;
AN3     :AN210LJ  INV7O,INV8O,AN3O;
AN4     :AN410LJ  INV7O,INV6O,INV5O,INV4O,AN4O;
AN5     :AN410LJ  INV3O,INV2O,INV1O,INV10O,AN5O;
AN6     :AN210LJ  P0,INV11O,AN6O;
AN8     :AN410LJ  INV6O,INV5O,INV4O,INV3O,AN8O;
AN9     :AN310LJ  INV2O,INV1O,INV12O,AN9O;
EX1     :EX210LJ  P7,Q7,EX1O;
EX2     :EX210LJ  P6,Q6,EX2O;
EX3     :EX210LJ  P5,Q5,EX3O;
EX4     :EX210LJ  P4,Q4,EX4O;
EX5     :EX210LJ  P3,Q3,EX5O;
EX6     :EX210LJ  P2,Q2,EX6O;
EX7     :EX210LJ  P1,Q1,EX7O;
EX8     :EX210LJ  P0,Q0,EX8O;
INV1    :IV120LJ  EX1O,INV1O;
INV10   :IV110LJ  Q0,INV10O;
INV11   :IV120LJ  G2Z,INV11O;
IV12    :IV110LJ  Q1,INV12O;
INV13   :IV110LJ  Q2,INV13O;
INV14   :IV110LJ  Q3,INV14O;
INV15   :IV110LJ  Q4,INV15O;
INV16   :IV110LJ  Q5,INV16O;
INV17   :IV110LJ  Q6,INV17O;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

HDL FILE† (Continued)

```
INV18     :IV110LJ    Q7,INV18O;
INV2      :IV120LJ    EX2O,INV2O;
INV3      :IV120LJ    EX3O,INV3O;
INV4      :IV120LJ    EX4O,INV4O;
INV5      :IV110LJ    EX5O,INV5O;
INV6      :IV110LJ    EX6O,INV6O;
INV7      :IV110LJ    EX7O,INV7O;
INV8      :IV110LJ    EX8O,INV8O;
INV9      :IV110LJ    G1Z,INV9O;
NA1       :NA420LJ    AN1O,AN2O,AN3O,INV9O,PEQQZ;
NA10      :NA410LJ    NA2O,NA3O,NA4O,NA5O,NA10O;
NA11      :NA410LJ    NA6O,NA7O,NA8O,NA9O,NA11O;
NA2       :NA310LJ    AN4O,AN5O,AN6O,NA2O;
NA3       :NA310LJ    AN8O,AN9O,AN10O,NA3O;
NA4       :NA210LJ    AN12O,AN13O,NA4O;
NA5       :NA210LJ    AN15O,AN16O,NA5O;
NA6       :NA210LJ    AN18O,AN19O,NA6O;
NA7       :NA210LJ    AN21O,AN22O,NA7O;
NA8       :NA410LJ    INV1O,INV17O,P6,INV11O,NA8O;
NA9       :NA310LJ    INV18O,P7,INV11O,NA9O;
NO1       :NO220LJ    NA10O,NA11O,PGTQZ;
END S686LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

S688LJ
8-BIT IDENTITY COMPARATOR

D3030, APRIL 1988

SOFTWARE MACRO

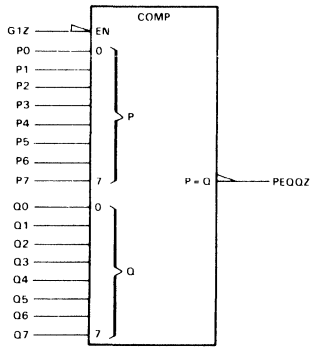
- **Performs Identity Comparison of Binary, BCD, and Monotonic Codes**
- **Cascading Input Accomodates Expansion**

description

The S688LJ software macro implements an 8-bit expandable identity comparator. The 8-bit configuration simplifies construction of wider comparators. These 8-bit identity comparators perform bit-by-bit comparison of binary, straight BCD (8-4-2-1), or random codes. The fully decoded equality decision (P = Q?) on 8-bit words (P,Q) is made. These devices are expandable to any number of bits. Words of greater length may be compared by connecting comparators in cascade. The PEQQZ output of a stage handling less significant bits is connected to the corresponding G1Z input of the next stage handling more-significant bits.

The S688LJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS		OUTPUT
DATA Pn, Qn	ENABLE G1Z	PEQQZ
P=Q	L	L
P>Q	X	H
P<Q	X	H
X	H	H

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN210LJ	1.5	1	1.5	0.33
AN310LJ	1.75	2	3.5	0.76
EX210LJ	1.75	8	14	2.88
IV110LJ	0.75	9	6.75	1.44
NA420LJ	2.5	1	2.5	0.39
TOTALS		21	28.25	5.8

When the identity comparator is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

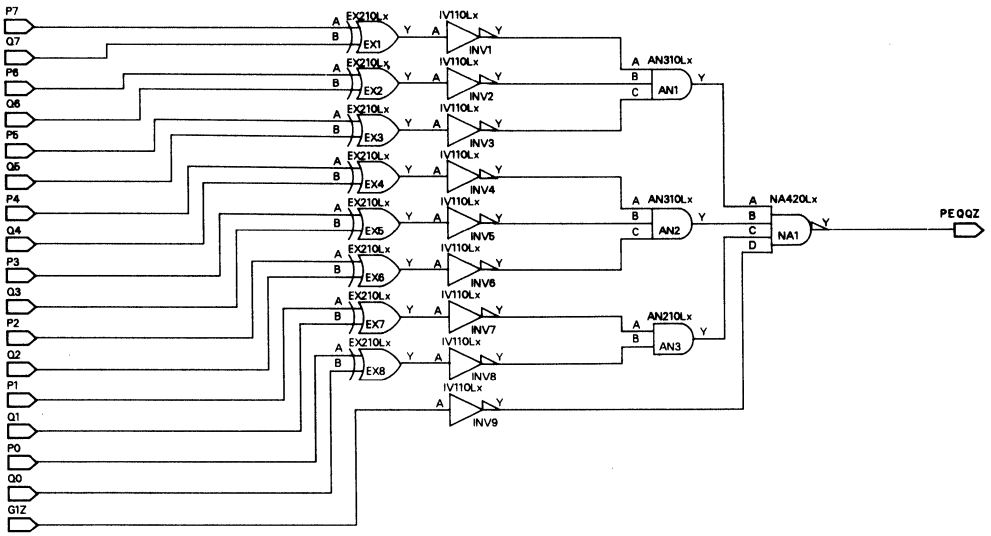
Label: S688LJ P0,P1,P2,P3,P4,P5,P6,P7,Q0,Q1,Q2,Q3,Q4,Q5,Q6, Q7,G1Z,PEQQZ;

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S688LJ
8-BIT IDENTITY COMPARATOR

D3030, APRIL 1988

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	G1Z		0.05		pF
		Any P or Q		0.08		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	5.8		pF

D3030, APRIL 1988

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Pn, Qn	PEQQZ		2.4	4.3		2.4	3.9	ns
t_{PHL}				2.5	5.1		2.5	4.8	
t_{PLH}	G1Z	PEQQZ		0.9	1.5		0.9	1.4	ns
t_{PHL}				0.9	1.8		0.9	1.6	
Δt_{PLH}	Any	PEQQZ	0.22	0.68	1.46	0.24	0.68	1.34	ns/pF
Δt_{PHL}			0.26	0.78	1.82	0.28	0.78	1.62	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE‡

```
BLOCK S688LJ;                    STRUCTURE
P0          @INPUT;              AN1     :AN310LJ  INV1O,INV2O,INV3O,AN1O;
P1          @INPUT;              AN2     :AN310LJ  INV4O,INV5O,INV6O,AN2O;
P2          @INPUT;              AN3     :AN210LJ  INV7O,INV8O,AN3O;
P3          @INPUT;              EX1     :EX210LJ  P7,Q7,EX1O;
P4          @INPUT;              EX2     :EX210LJ  P6,Q6,EX2O;
P5          @INPUT               EX3     :EX210LJ  P5,Q5,EX3O;
P6          @INPUT;              EX4     :EX210LJ  P4,Q4,EX4O;
P7          @INPUT;              EX5     :EX210LJ  P3,Q3,EX5O;
Q0          @INPUT;              EX6     :EX210LJ  P2,Q2,EX6O;
Q1          @INPUT;              EX7     :EX210LJ  P1,Q1,EX7O;
Q2          @INPUT;              EX8     :EX210LJ  P0,Q0,EX8O;
Q3          @INPUT;              INV1    :IV110LJ  EX1O,INV1O;
Q4          @INPUT;              INV2    :IV110LJ  EX2O,INV2O;
Q5          @INPUT;              INV3    :IV110LJ  EX3O,INV3O;
Q6          @INPUT;              INV4    :IV110LJ  EX4O,INV4O;
Q7          @INPUT;              INV5    :IV110LJ  EX5O,INV5O;
G1Z         @INPUT;              INV6    :IV110LJ  EX6O,INV6O;
PEQQZ       @OUTPUT;             INV7    :IV110LJ  EX7O,INV7O;
                                 INV8    :IV110LJ  EX8O,INV8O;
                                 INV9    :IV110LJ  G1Z,INV9O;
                                 NA1     :NA420LJ  AN1O,AN2O,AN3O,INV9O,PEQQZ;
                                 END S688LJ;
```

‡ The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

15 Counters

COUNTERS
FUNCTIONAL INDEX

D3030, APRIL 1988

COUNTERS – POSITIVE-EDGE-TRIGGERED

DESCRIPTION	f_{clock} (MHz)	CELL NAME	OUTPUT DRIVE	COMMENTS	EQUIVALENT NA210s	PAGE
4-Bit Ripple Binary	185	R2408LJ	1X	Async clear (L)	23.5	15-3

COUNTERS (SOFTWARE) – POSITIVE-EDGE-TRIGGERED

DESCRIPTION	CELL NAME	LOAD	OUTPUT DRIVE	COMMENTS	EQUIVALENT NA210s	PAGE
4-Bit Binary	S161ALJ	Sync	1X	Async clear (L)	63	15-5
4-Bit Binary	S163ALJ	Sync	1X	Sync clear (L)	65.25	15-11
4-Bit Ripple Binary	S177LJ		1X	Async clear (L)	47.5	15-17
4-Bit Up/Down Binary	S191LJ	Async	1X	No clear (use load)	80.5	15-22
4-Bit Up/Down	S193LJ	Async	1X	Async clear (H) dual clock	73	15-30
Dual 4-Bit Ripple Binary	S393LJ		1X	Async clear (H)	50	15-36
8-Bit Binary	S590LJ	None	1X	Async clear (L) 3-state outputs	130	15-40
8-Bit Binary	S593XLJ	Sync	1X	Async clear (L) 3-state outputs	179	15-46
4-Bit Up/Down Binary	S669LJ	Sync	1X	No clear (use load)	69	15-53

R2408LJ
4-BIT RIPPLE COUNTER

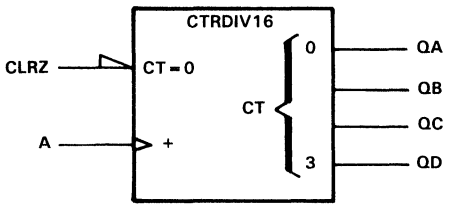
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUTS			
CLRZ	A	QD	QC	QB	QA
L	X	L	L	L	L
H	↑	L	L	L	H
H	↑	L	L	H	H
H	↑	L	L	H	L
H	↑	L	H	L	L
H	↑	L	H	L	H
H	↑	L	H	H	L
H	↑	L	H	H	H
H	↑	H	L	L	L
H	↑	H	L	L	H
H	↑	H	L	H	L
H	↑	H	L	H	H
H	↑	H	H	L	L
H	↑	H	H	L	H
H	↑	H	H	H	L
H	↑	H	H	H	H
H	↑	L	L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The R2408LJ cell implements a 4-bit binary counter. The 4-bit length means that larger blocks of custom logic can be handled efficiently to construct large counters. The clock input, A, triggers on the positive-going edge, and the clear input is active low.

The counter contains an embedded clock driver that buffers the clock input to a single 2-line input. This further simplifies implementation of longer counters, as standard library buffers can be used to drive multiple clock inputs that are used in the longer counters. When the counter is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: R2408LJ CLRZ,A,QA,QB,QC,QD;

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	185	MHz
t_w	Pulse duration	CLRZ low	3		ns
		A high or low	2.7		
t_{su}	Setup time before clock	CLRZ inactive	0		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLRZ		0.47		pF
		A		0.11		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	2.62		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	QA	0.5	1.43	3.24	0.52	1.43	2.95	ns
t_{PHL}			0.5	1.42	3.23	0.52	1.42	2.97	
t_{PLH}	A	QB	0.87	2.62	6.21	0.92	2.62	5.66	ns
t_{PHL}			0.73	2.32	5.5	0.77	2.32	5.04	
t_{PLH}	A	QC	1.09	3.56	8.48	1.18	3.56	7.73	ns
t_{PHL}			0.96	3.25	7.77	1.04	3.25	7.08	
t_{PLH}	A	QD	1.25	4.34	10.42	1.34	4.34	9.49	ns
t_{PHL}			1.12	4.05	9.75	1.21	4.05	8.89	
t_{PHL}	CLRZ	Qn	0.29	0.91	2	0.32	0.91	1.84	ns
Δt_{PLH}	A	Qn	0.2	0.62	1.34	0.2	0.62	1.24	ns/pF
Δt_{PHL}			0.16	0.46	0.98	0.16	0.46	0.88	
Δt_{PHL}	CLRZ	Qn	0.18	0.46	0.98	0.18	0.46	0.88	ns/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

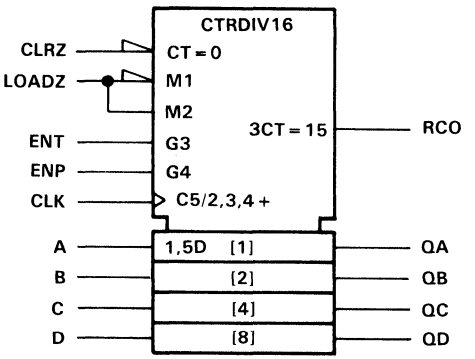
S161ALJ
SYNCHRONOUS 4-BIT BINARY COUNTER WITH DIRECT CLEAR

D3030, APRIL 1988

SOFTWARE MACRO

- **Internal Look-Ahead Enhances Performance of Cascaded Counters**
- **Asynchronous Clear Initializes Sequence Regardless of Mode**
- **Parallel Synchronously Presettable for Full-Cycle Modulo-N Sequences**
- **Gated Enables and RCO Implement Local and Global Carry Status**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S161ALJ software macro implements a synchronous 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the count-enable inputs and other gating. This mode of operation eliminates output counting spikes associated with asynchronous (ripple) counters. The clear and load inputs are buffered to enhance performance. Clocking of the register occurs on the rising (positive-going) edge of the clock waveform. The S161ALJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN320LJ	2	1	2	0.55
IV110LJ	0.75	4	3	0.64
IV120LJ	1	4	4	1.24
IV140LJ	1.5	2	3	1.26
NA210LJ	1	6	6	1.14
NA310LJ	1.25	10	12.5	1.9
NA410LJ	1.5	2	3	0.38
NA510LJ	3	2	6	1.76
R2406LJ	23.5	1	23.5	5.16
TOTALS		32	63	14.03

When the counter is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S161ALJ D,C,B,A,CLK,CLRZ,ENP,ENT,LOADZ,QD,QC,QB,QA,RCO;

These counters are fully programmable; that is, they may be preset to any number between 0 and 15. Since presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

Clearing is asynchronous. A low level at the clear input sets all outputs low regardless of the levels of the clock, load, or enable.

The carry look-ahead circuitry provides for cascading counters in n-bit synchronous applications without additional gating. Instrumental in achieving this are two count-enable inputs and a ripple-carry output. Both count-enable inputs (ENP and ENT) must be high to count. ENP enables the local 4-bits and the ENT is fed forward to globally extend the enable/disable of previous/next 4-bit cascaded counters. The ripple-carry out (RCO), when locally and globally enabled, will output a high-level pulse at maximum count that is used to enable successive stages.

These counters feature a fully independent clock. Changes at control inputs other than the clear will have no effect on the counter until clocking occurs. The functions of the counter are dictated solely by conditions meeting setup, hold, and duration recommendations.

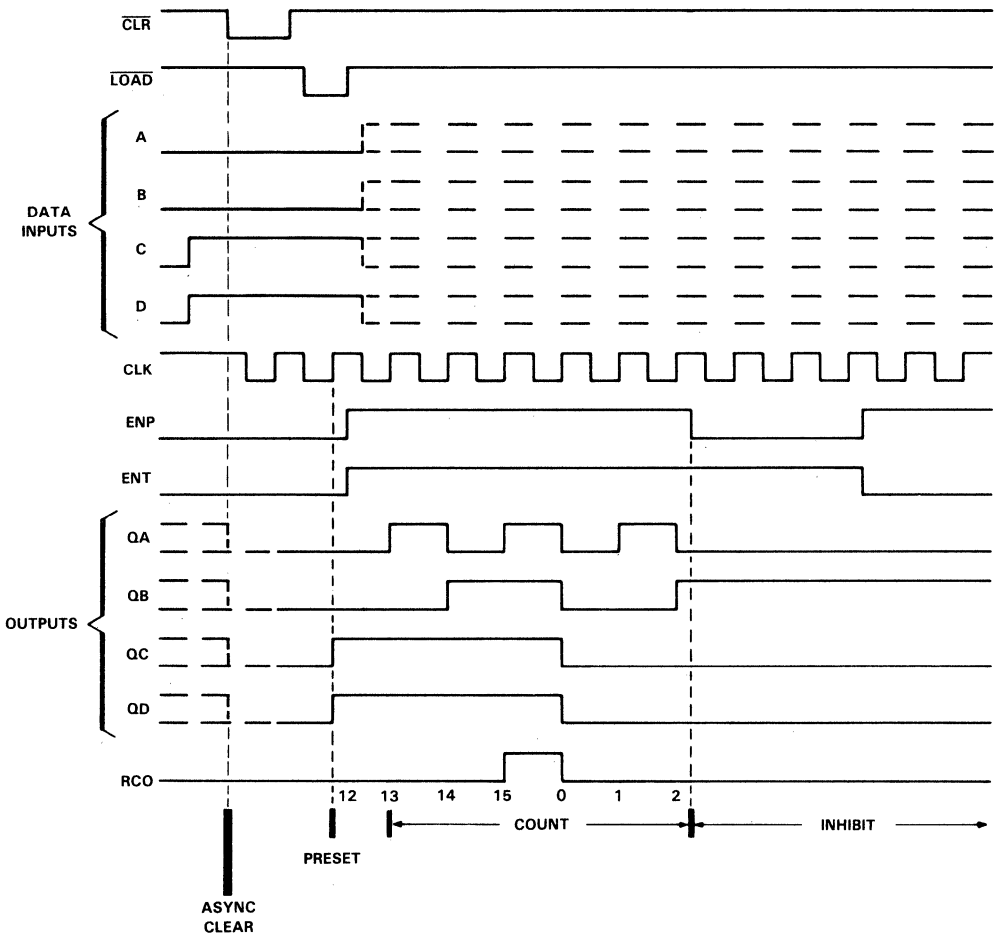
S161ALJ
SYNCHRONOUS 4-BIT BINARY COUNTER WITH DIRECT CLEAR

D3030, APRIL 1988

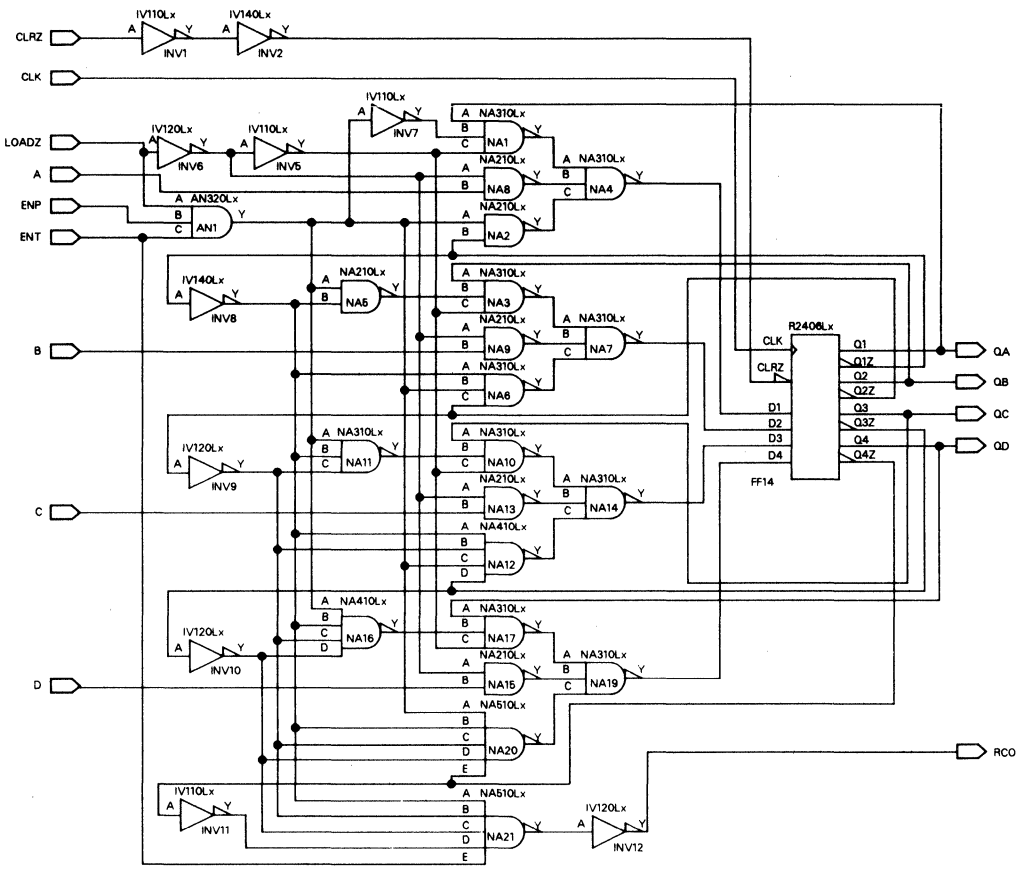
S161ALJ output sequence

Illustrated below is the following sequence:

1. Asynchronously clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit.



logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

S161ALJ
SYNCHRONOUS 4-BIT BINARY COUNTER WITH DIRECT CLEAR

D3030, APRIL 1988

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A, B, C, D		0.06		pF
		CLK		0.11		
		CLRZ		0.05		
		ENP		0.05		
		ENT		0.05		
		LOADZ		0.16		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	14.1		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	RCO		3.7	8		3.7	7.4	ns
t_{PHL}				3.7	7.9		3.7	7	
t_{PLH}	CLK	Any Q		1.5	3.2		1.5	3	ns
t_{PHL}				1.6	3.7		1.6	3.4	
t_{PLH}	ENT	RCO		1.4	2.7		1.4	2.6	ns
t_{PHL}				1.1	2.3		1.1	2.1	
t_{PHL}	CLRZ	Any Q		1.6	3.2		1.6	3	ns
t_{PLH}	CLRZ	RCO		3	5.8		3	5.2	
Δt_{PLH}	Any	Any Q	0.42	1.12	2.32	0.44	1.12	2.12	ns/pF
Δt_{PHL}			0.34	0.76	1.54	0.36	0.76	1.4	
Δt_{PLH}	Any	RCO	0.24	0.52	1.1	0.26	0.52	1	ns/pF
Δt_{PHL}			0.28	0.42	0.68	0.28	0.42	0.62	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

S161ALJ
SYNCHONOUS 4-BIT BINARY COUNTER WITH DIRECT CLEAR

D3030, APRIL 1988

HDL FILE†

```
BLOCK     S161ALJ;
D         @INPUT;
C         @INPUT;
B         @INPUT;
A         @INPUT;
CLK       @INPUT;
CLRZ      @INPUT;
ENP       @INPUT;
ENT       @INPUT;
LOADZ     @INPUT;
QD        @OUTPUT;
QC        @OUTPUT;
QB        @OUTPUT;
QA        @OUTPUT;
RCO       @OUTPUT;
STRUCTURE
AN1       :AN320LJ  LOADZ,ENP,ENT,AN1O;
FF14      :R2406LJ  INV2O,NA4O,NA7O,NA14O,
                    NA19O,CLK,QA,FFA__QZ,QB,
                    FFB__QZ,QC,FFC__QZ,QD,
                    FFD__QZ;
INV1      :IV110LJ  CLRZ,INV1O;
INV10     :IV120LJ  FFC__QZ,INV10O;
INV11     :IV110LJ  FFD__QZ,INV11O;
INV12     :IV120LJ  NA21O,RCO;
INV2      :IV140LJ  INV1O,INV2O;
INV5      :IV110LJ  INV6O,INV5O;
INV6      :IV120LJ  LOADZ,INV6O;
INV7      :IV110LJ  AN1O,INV7O;
INV8      :IV140LJ  FFA__QZ,INV8O;
INV9      :IV120LJ  FFB__QZ,INV9O;
NA1       :NA310LJ  QA,INV7O,INV5O,NA1O;
NA10      :NA310LJ  QC,NA11O,INV5O,NA10O;
NA11      :NA310LJ  AN1O,INV8O,INV9O,NA11O;
NA12      :NA410LJ  INV8O,INV9O,AN1O,FFC__QZ,NA12O;
NA13      :NA210LJ  INV6O,C,NA13O;
NA14      :NA310LJ  NA10O,NA13O,NA12O,NA14O;
NA15      :NA210LJ  INV6O,D,NA15O;
NA16      :NA410LJ  AN1O,INV8O,INV9O,INV10O,NA16O;
NA17      :NA310LJ  QD,NA16O,INV5O,NA17O;
NA19      :NA310LJ  NA17O,NA15O,NA20O,NA19O;
NA2       :NA210LJ  AN1O,FFA__QZ,NA2O;
NA20      :NA510LJ  AN1O,INV8O,INV9O,INV10O,FFD__QZ,NA20O;
NA21      :NA510LJ  INV8O,INV9O,INV10O,INV11O,ENT,NA21O;
NA3       :NA310LJ  QB,NA5O,INV5O,NA3O;
NA4       :NA310LJ  NA1O,NA8O,NA2O,NA4O;
NA5       :NA210LJ  AN1O,INV8O,NA5O;
NA6       :NA310LJ  INV8O,AN1O,FFB__QZ,NA6O;
NA7       :NA310LJ  NA3O,NA9O,NA6O,NA7O;
NA8       :NA210LJ  INV6O,A,NA8O;
NA9       :NA210LJ  INV6O,B,NA9O;
END S161ALJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

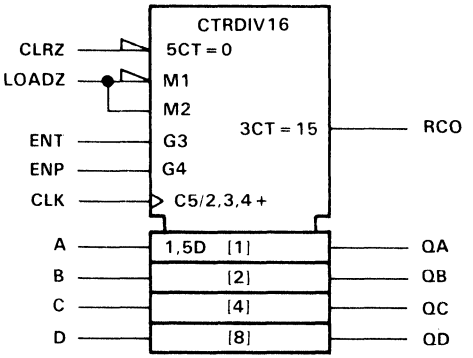
S163ALJ
SYNCHRONOUS 4-BIT BINARY COUNTER

D3030, APRIL 1988

SOFTWARE MACRO

- **Internal Look-Ahead Enhances Performance of Cascaded Counters**
- **Synchronous Clear Initializes Sequence Regardless of Mode**
- **Parallel Synchronously Presettable for Full-Cycle Modulo-N Sequences**
- **Gated Enables and RCO Implement Local and Global Carry Status**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S163ALJ software macro implements a synchronous 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the count-enable inputs and other gating. This mode of operation eliminates output counting spikes associated with asynchronous (ripple) counters. The clear and load inputs are buffered to enhance performance, and clocking of the register occurs on the rising (positive-going) edge of the clock waveform.

D3030, APRIL 1988

The S163ALJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN410LJ	2	1	2	0.42
IV110LJ	0.75	3	2.25	0.48
IV120LJ	1	3	3	0.93
IV140LJ	1.5	1	1.5	0.63
NA210LJ	1	6	6	1.14
NA310LJ	1.25	10	12.5	1.9
NA410LJ	1.5	2	3	0.38
NA510LJ	3	2	6	2.64
NO220LJ	1.5	1	1.5	0.23
NO240LJ	2.5	1	2.5	0.44
R2406LJ	23.5	1	23.5	5.16
TO010LJ	1.5	1	1.5	Nil
TOTALS		32	65.25	14.35

When the counter is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S163ALJ D,C,B,A,CLK,CLRZ,ENP,ENT,LOADZ,QD,QC,QB,QA,RCO;

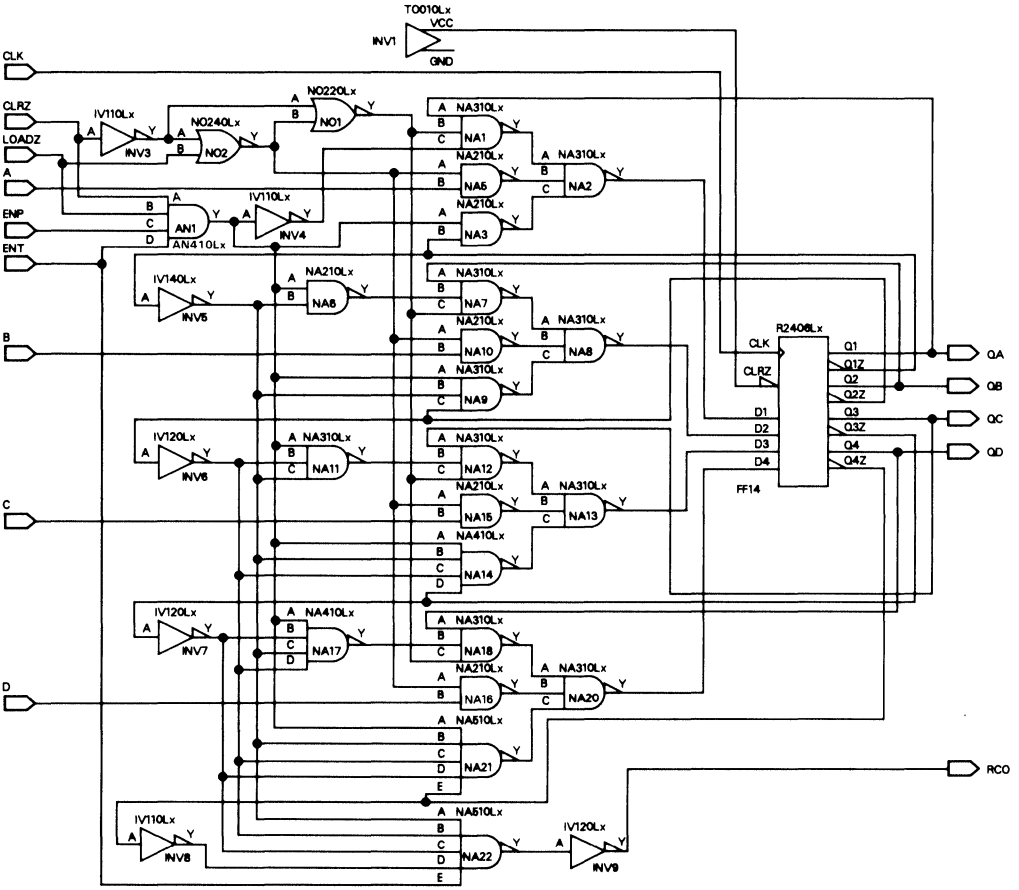
These counters are fully programmable; that is, they may be preset to any number between 0 and 15. Since presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

Clearing is synchronous. A low level at the clear input will set all outputs low on the next positive transition of the clock.

The carry look-ahead circuitry provides for cascading counters in n-bit synchronous applications without additional gating. Instrumental in achieving this are two count-enable inputs and a ripple-carry output. Both count-enable inputs (ENP and ENT) must be high to count. ENP enables the local 4-bits and the ENT is fed forward to globally extend the enable/disable of previous/next 4-bit cascaded counters. The ripple-carry out (RCO), when locally and globally enabled, will output a high-level pulse that is used to enable successive stages.

These counters feature a fully independent clock. Changes at control inputs, including clear, will have no effect on the counter until clocking occurs. The functions of the counter are dictated solely by conditions meeting setup, hold, and duration recommendations.

logic diagram

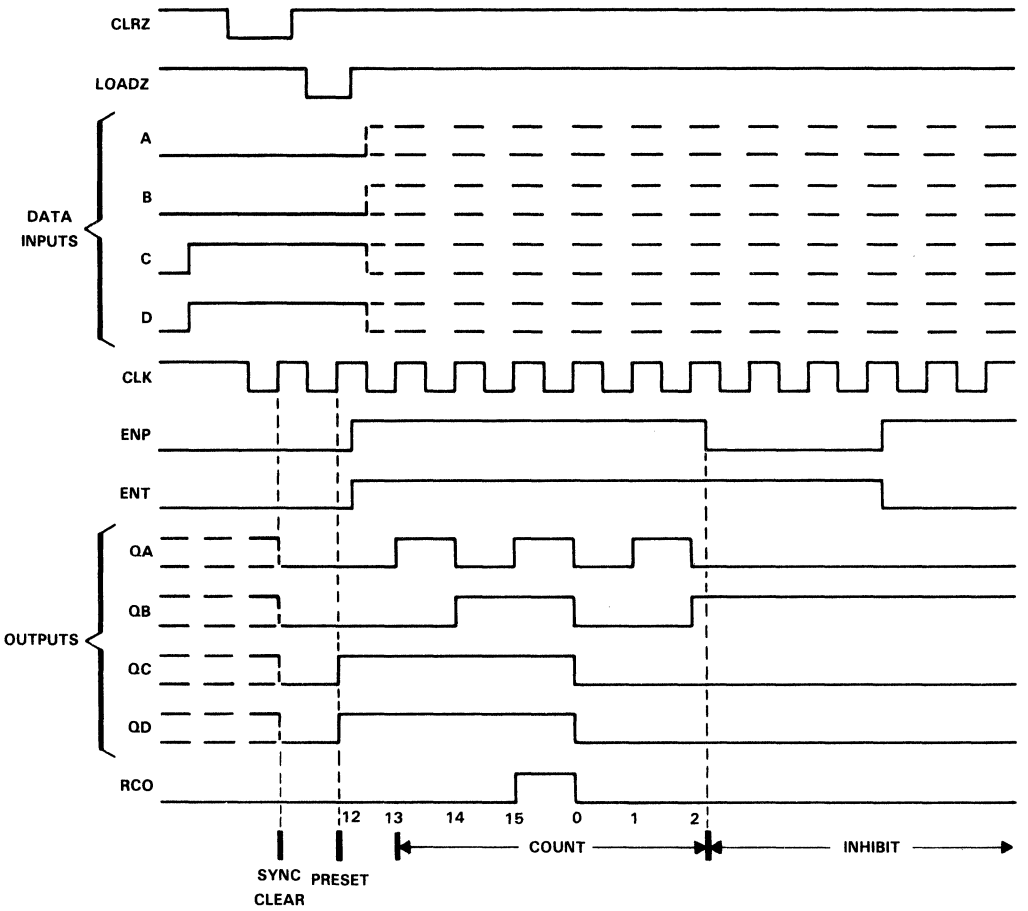


D3030, APRIL 1988

S163ALJ output sequence

Illustrated below is the following sequence:

1. Synchronously clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit.



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A, B, C, D		0.06		pF
		CLK		0.11		
		CLRZ		0.1		
		ENP		0.05		
		ENT		0.11		
		LOADZ		0.27		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	14.35		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	RCO		3.7	8		3.7	7.4	ns
t_{PHL}				3.7	7.9		3.7	7	
t_{PLH}	CLK	Any Q		1.5	3.2		1.5	3	ns
t_{PHL}				1.6	3.7		1.6	3.4	
t_{PLH}	ENT	RCO		1.4	2.7		1.4	2.6	ns
t_{PHL}				1.1	2.3		1.1	2.1	
Δt_{PLH}	Any	Any Q	0.42	1.12	2.32	0.44	1.12	2.12	ns/pF
Δt_{PHL}			0.34	0.76	1.54	0.36	0.76	1.4	
Δt_{PLH}	Any	RCO	0.24	0.52	1.1	0.26	0.52	1	ns/pF
Δt_{PHL}			0.28	0.42	0.68	0.28	0.42	0.62	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

D3030, APRIL 1988

HDL FILE†

```
BLOCK S163ALJ;
D                @INPUT;
C                @INPUT;
B                @INPUT;
A                @INPUT;
CLK              @INPUT;
CLRZ             @INPUT;
ENP              @INPUT;
ENT              @INPUT;
LOADZ            @INPUT;
QD               @OUTPUT;
QC               @OUTPUT;
QB               @OUTPUT;
QA               @OUTPUT;
RCO              @OUTPUT;
STRUCTURE
AN1      :AN410LJ   CLRZ,LOADZ,ENP,ENT,AN1O;
FF14     :R2406LJ   ICLRZ,NA2O,NA8O,NA13O,NA20O,
                    CLK,QA,QAZ,QB,QBZ,QC,QCZ,QD,
                    QDZ;
INV1     :TO010LJ   DUM,CLRZ;
INV3     :IV110LJ   CLRZ,INV3O;
INV4     :IV110LJ   AN1O,INV4O;
INV5     :IV140LJ   QAZ,INV5O;
INV6     :IV120LJ   QBZ,INV6O;
INV7     :IV120LJ   QCZ,INV7O;
INV8     :IV110LJ   QDZ,INV8O;
INV9     :IV120LJ   NA22O,RCO;
NA1      :NA310LJ   QA,NO1O,INV4O,NA1O;
NA10     :NA210LJ   NO2O,B,NA10O;
NA11     :NA310LJ   AN1O,INV6O,INV5O,NA11O;
NA12     :NA310LJ   QC,NA11O,NO1O,NA12O;
NA13     :NA310LJ   NA12O,NA15O,NA14O,NA13O;
NA14     :NA410LJ   AN1O,INV5O,INV6O,QCZ,NA14O;
NA15     :NA210LJ   NO2O,C,NA15O;
NA16     :NA210LJ   NO2O,D,NA16O;
NA17     :NA410LJ   AN1O,INV7O,INV5O,INV6O,NA17O;
NA18     :NA310LJ   QD,NA17O,NO1O,NA18O;
NA2      :NA310LJ   NA1O,NA5O,NA3O,NA2O;
NA20     :NA310LJ   NA18O,NA16O,NA21O,NA20O;
NA21     :NA510LJ   AN1O,INV5O,INV6O,INV7O,QDZ,NA21O;
NA22     :NA510LJ   INV5O,INV6O,INV7O,INV8O,ENT,NA22O;
NA3      :NA210LJ   AN1O,QAZ,NA3O;
NA5      :NA210LJ   NO2O,A,NA5O;
NA6      :NA210LJ   AN1O,INV5O,NA6O;
NA7      :NA310LJ   QB,NA6O,NO1O,NA7O;
NA8      :NA310LJ   NA7O,NA10O,NA9O,NA8O;
NA9      :NA310LJ   AN1O,INV5O,QBZ,NA9O;
NO1      :NO220LJ   INV3O,NO2O,NO1O;
NO2      :NO240LJ   INV3O,LOADZ,NO2O;
END S163ALJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

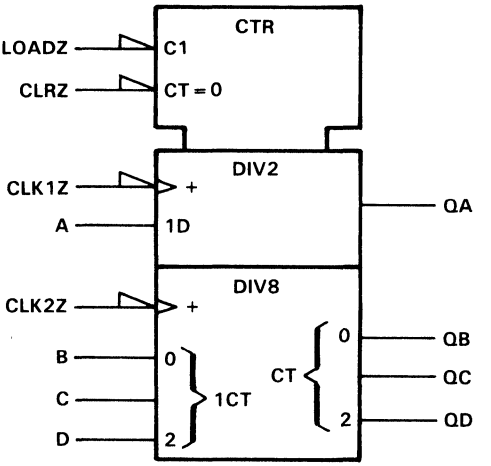
S177LJ
1-BIT AND 3-BIT BINARY RIPPLE COUNTER

D3030, APRIL 1988

SOFTWARE MACRO

- **Individual 1-Bit and 3-Bit Counters for Implementing Custom Count Sequences**
- **Asynchronous Clear Initializes Sequence Regardless of Mode**
- **Parallel Asynchronously Presettable for Modulo-N Sequences**
- **Performs Ripple-Count or Simple Latching Functions**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S177LJ software macro implements a 1-bit and 3-bit ripple counter element. The overall 4-bit configuration provides a multifunction counter/latch whose 4-bit length simplifies construction of large counters. These ripple counters consist of four D-type flip-flops that are interconnected to provide a divide-by-two and a divide-by-eight counter. A divide-by-16 sequence is obtained by connecting the QA output to the CLK2Z input. During the count operation, transfer of information to the outputs occur on the negative-going edge of the clock pulse. The S177LJ implements the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
DFB20LJ	7.25	4	29	7.12
IV110LJ	0.75	2	1.5	0.32
IV120LJ	1	4	4	1.24
NA310LJ	1.25	4	5	0.76
NO210LJ	1	8	8	0.96
TOTALS		22	47.5	10.4

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S177LJ A,B,C,D,LOADZ,CLRZ,CLK1Z,CLK2Z,QA,QB,QC,QD;

The counter is fully programmable; that is, it may be preset to any number between 0 and 15. As presetting is asynchronous, a low level at the load input disables the counter and causes the outputs to agree with the setup data independent of the level of the clock input. These counters may be used as 4-bit latches by using the LOADZ input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when LOADZ is low, but will remain unchanged when LOADZ is high and the clock inputs are inactive.

Clearing is asynchronous. A low level at the clear input sets all outputs low regardless of the levels of the clocks or LOADZ.

FUNCTION TABLE
(See Note 1)

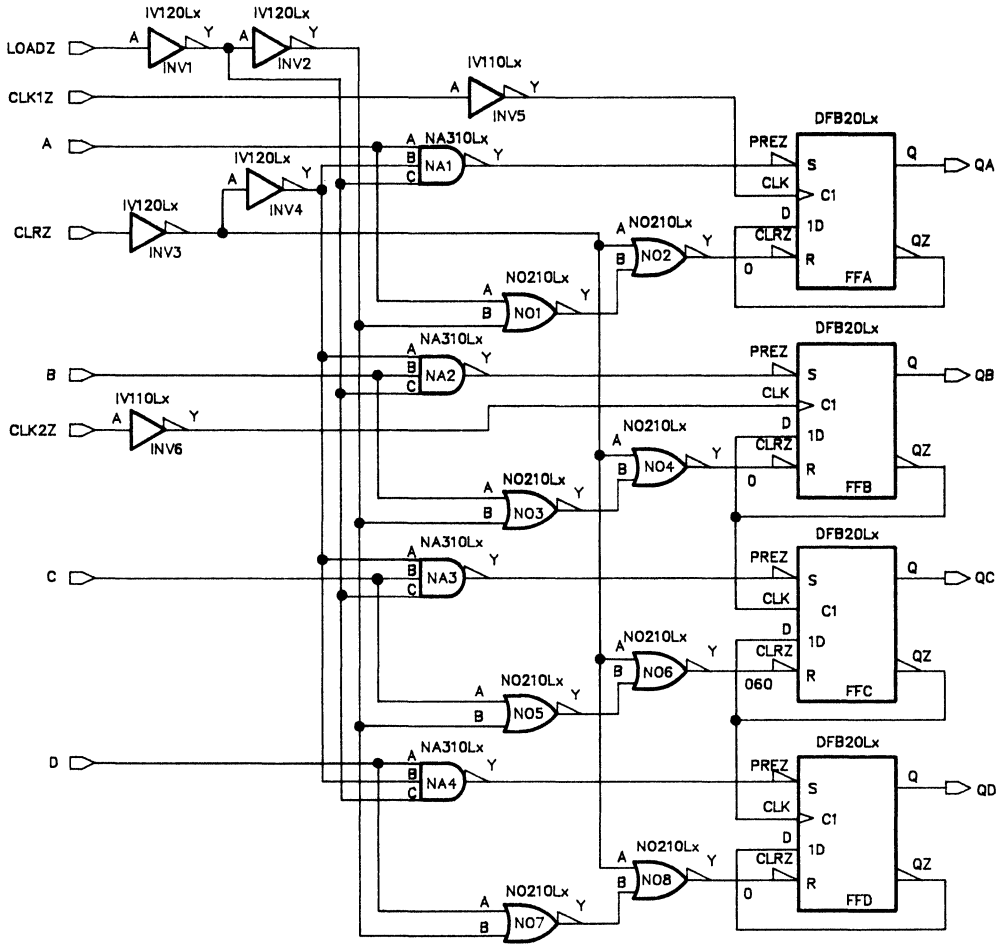
INPUTS							OUTPUTS			
CLRZ	LOADZ	D	C	B	A	CLK1Z	QD	QC	QB	QA
L	H	X	X	X	X	X	L	L	L	L
H	L	d	c	b	a	X	d	c	b	a
H	H	X	X	X	X	↓	L	L	L	H
H	H	X	X	X	X	↓	L	L	H	L
H	H	X	X	X	X	↓	L	L	H	H
H	H	X	X	X	X	↓	L	H	L	L
H	H	X	X	X	X	↓	L	H	L	H
H	H	X	X	X	X	↓	L	H	H	L
H	H	X	X	X	X	↓	L	H	H	H
H	H	X	X	X	X	↓	H	L	L	L
H	H	X	X	X	X	↓	H	L	L	H
H	H	X	X	X	X	↓	H	L	H	L
H	H	X	X	X	X	↓	H	L	H	H
H	H	X	X	X	X	↓	H	H	L	L
H	H	X	X	X	X	↓	H	H	L	H
H	H	X	X	X	X	↓	H	H	H	L
H	H	X	X	X	X	↓	H	H	H	H
H	H	X	X	X	X	↓	L	L	L	L
H	H	X	X	X	X	↓	Qo	Qo	Qo	Qo

See Explanation of Function Tables in Section 1.
NOTE 1: Table applies with output QA connected to CLK2Z input.

S177LJ
1-BIT AND 3-BIT BINARY RIPPLE COUNTER

D3030, APRIL 1988

logic diagram



D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLRZ		0.06		pF
		LOADZ		0.11		
		All other inputs		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	10.4		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (See Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK1Z	QA		2.4	5.6		2.4	5.1	ns
t_{PHL}				1.8	4.1		1.8	3.7	
t_{PLH}		QB		2.4	5.6		2.4	5.1	ns
t_{PHL}				1.8	4.1		1.8	3.7	
t_{PLH}	CLK2Z	QC		4.5	10.5		4.5	9.6	ns
t_{PHL}				3.9	9		3.9	8.2	
t_{PLH}		QD		6.6	15.4		6.6	14.1	ns
t_{PHL}				6	14		6	12.8	
t_{PLH}	A,B,C,D	Any		1.5	3.1		1.5	2.8	ns
t_{PHL}				2.2	4.6		2.2	4.3	
t_{PLH}	LOADZ	Any		2.4	5.4		2.4	5	ns
t_{PHL}				2.5	5		2.5	4.8	
t_{PHL}	CLRZ	Any Q		4.1	8.5		4.1	8	ns
Δt_{PLH}	Any	Any	0.16	0.56	1.18	0.2	0.56	1.1	ns/pF
Δt_{PHL}			0.14	0.36	0.78	0.16	0.36	0.7	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S177LJ
1-BIT AND 3-BIT BINARY RIPPLE COUNTER

HDL FILE†

```
BLOCK S177LJ;
A          @INPUT;
B          @INPUT;
C          @INPUT;
D          @INPUT;
LOADZ      @INPUT;
CLRZ       @INPUT;
CLK1Z      @INPUT;
CLK2Z      @INPUT;
QA         @OUTPUT;
QB         @OUTPUT;
QC         @OUTPUT;
QD         @OUTPUT;
STRUCTURE
INV1       :IV120LJ    LOADZ,LD;
INV2       :IV120LJ    LD,LDZ;
INV3       :IV120LJ    CLRZ,CLEAR;
INV4       :IV120LJ    CLEAR,CLEARZ;
FFA        :DFB20LJ    NO2O,NA1O,FFAQZ,CLK1,QA,FFAQZ;
FFB        :DFB20LJ    NO4O,NA2O,FFBQZ,CLK2,QB,FFBQZ;
FFC        :DFB20LJ    NO6O,NA3O,FFCQZ,FFBQZ,QC,FFCQZ;
FFD        :DFB20LJ    NO8O,NA4O,FFDQZ,FFCQZ,QD,FFDQZ;
INV5       :IV110LJ    CLK1Z,CLK1;
INV6       :IV110LJ    CLK2Z,CLK2;
NA1        :NA310LJ    A,CLEARZ,LD,NA1O;
NO1        :NO210LJ    A,LDZ,NO1O;
NO2        :NO210LJ    CLEAR,NO1O,NO2O;
NA2        :NA310LJ    B,CLEARZ,LD,NA2O;
NO3        :NO210LJ    B,LDZ,NO3O;
NO4        :NO210LJ    CLEAR,NO3O,NO4O;
NA3        :NA310LJ    C,CLEARZ,LD,NA3O;
NO5        :NO210LJ    C,LDZ,NO5O;
NO6        :NO210LJ    CLEAR,NO5O,NO6O;
NA4        :NA310LJ    D,CLEARZ,LD,NA4O;
NO7        :NO210LJ    D,LDZ,NO7O;
NO8        :NO210LJ    CLEAR,NO7O,NO8O;
END S177LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

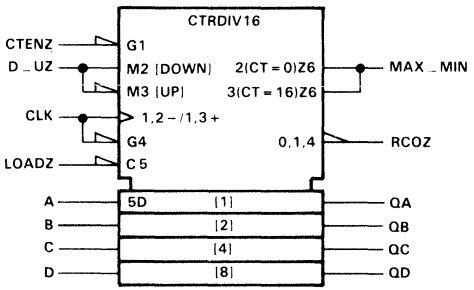
S191LJ
SYNCHRONOUS UP/DOWN BINARY COUNTER WITH DOWN/UP MODE CONTROL

D3030, APRIL 1988

SOFTWARE MACRO

- **Single Down/Up Control Line**
- **Look-Ahead Circuitry Enhances Performance of Cascaded Counters**
- **Fully Synchronous in Count Mode**
- **Parallel Asynchronous Load for Modulo-N Count Sequences**
- **Count Enable Input for Setting Sequence Start and Stop**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S191LJ software macro implements a synchronous, reversible up/down 4-bit binary counter. A synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates output counting spikes normally associated with asynchronous (ripple clock) counters.

The S191LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
DFB20LJ	7.25	4	29	7.12
IV110LJ	0.75	13	9.75	2.08
IV120LJ	1	1	1	0.31
NA210LJ	1	26	26	4.94
NA310LJ	1.25	3	3.75	0.57
NA410LJ	1.5	2	3	0.38
NA510LJ	3	2	6	1.76
NO210LJ	1	2	2	0.24
TOTALS		53	80.5	17.4

When the counter is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S191LJ D,C,B,A,CLK,D__UZ,CTENZ,LOADZ,QD,QC,QB,QA,RCOZ,MAX__MIN;

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S191LJ
SYNCHRONOUS UP/DOWN BINARY COUNTER WITH DOWN/UP MODE CONTROL

D3030, APRIL 1988

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input (CTENZ) is low. A high at CTENZ inhibits counting. The direction of the count is determined by the level of the down/up (D__UZ) input. When D__UZ is low, the counter counts up and when the D__UZ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs (CTENZ and D__UZ) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

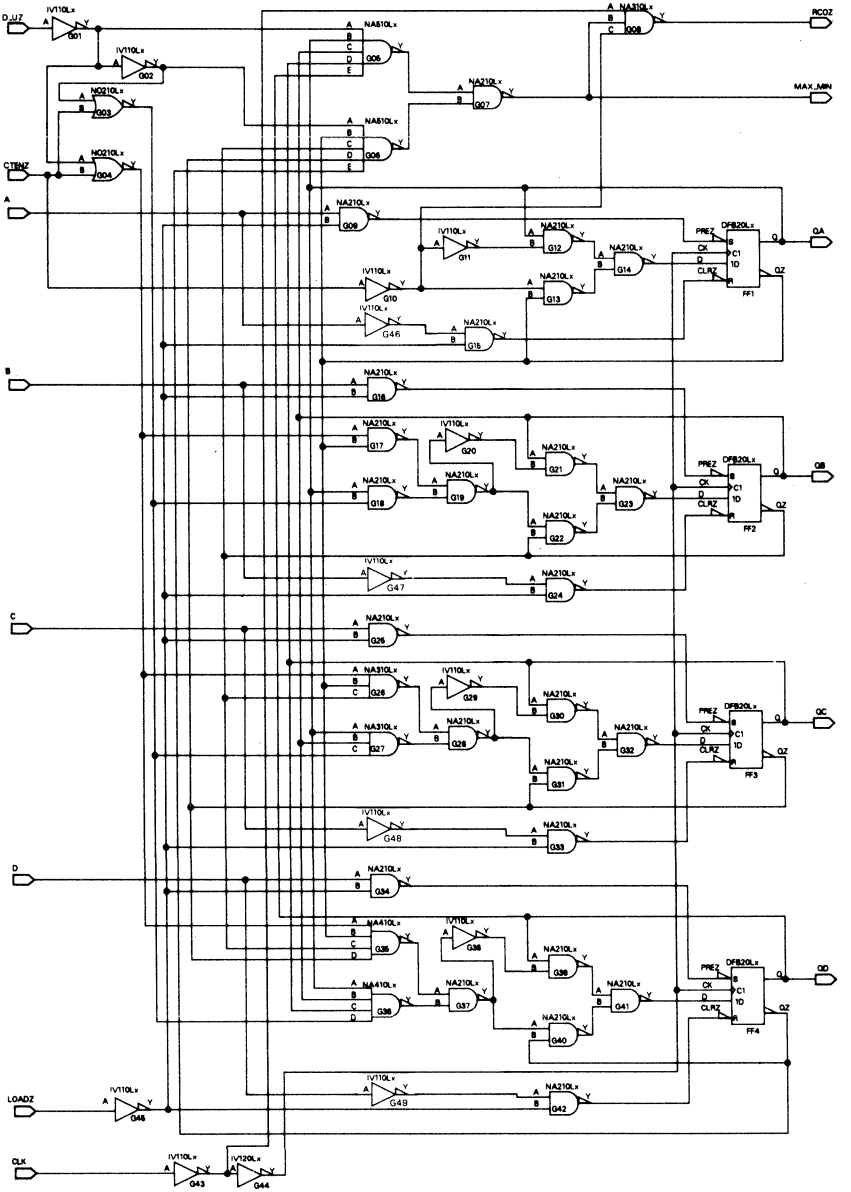
These counters are fully programmable; that is, they may be preset to any number between 0 and 15 by placing a low on the load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple and maximum/minimum count. The latter output (MAX__MIN) produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (all outputs high) counting up. The ripple clock output (RCOZ) produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple-clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

S191LJ
SYNCHRONOUS UP/DOWN BINARY COUNTER WITH DOWN/UP MODE CONTROL

D3030, APRIL 1988

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

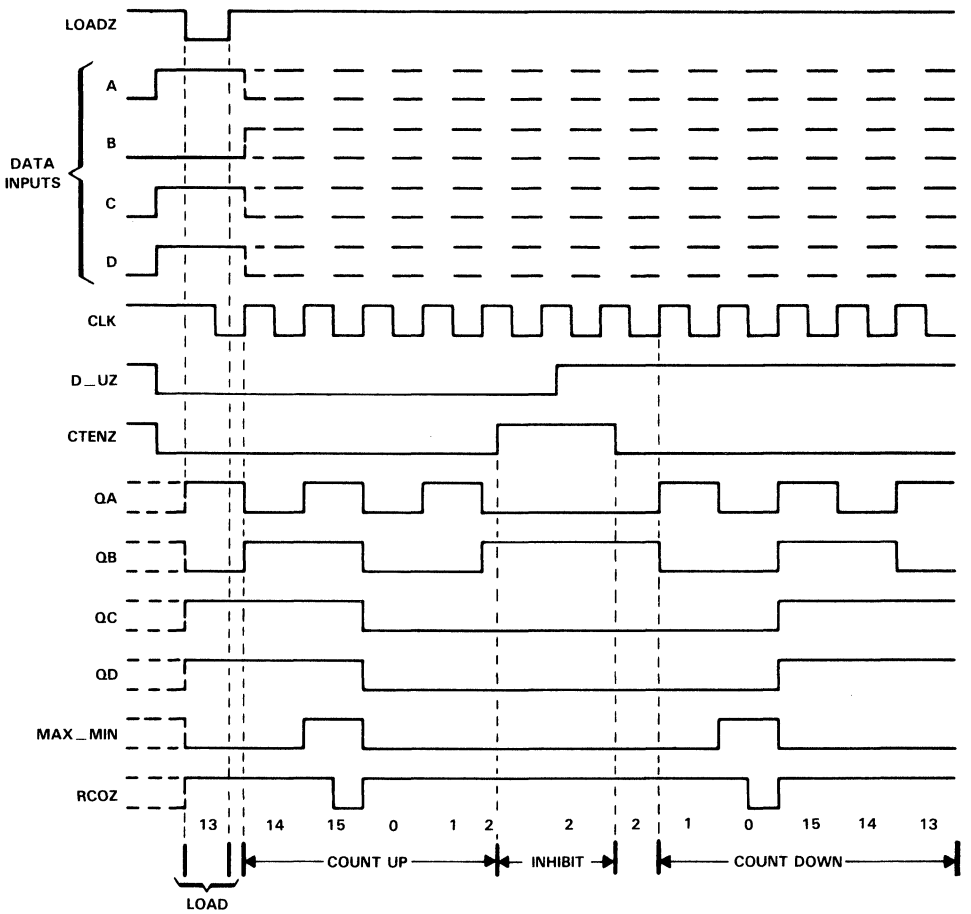
S191LJ
SYNCHRONOUS UP/DOWN BINARY COUNTER WITH DOWN/UP MODE CONTROL

D3030, APRIL 1988

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CTENZ		0.15		pF
		All other inputs		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	16.8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	LOADZ	Any Q		2.6	5.2		2.6	4.9	ns
t_{PHL}				2.6	5.2		2.6	5	
t_{PLH}	A,B,C,D	Any Q		1.5	3		1.5	2.7	ns
t_{PHL}				2.3	4.5		2.3	4.2	
t_{PLH}	CLK	RCOZ		0.9	1.4		0.9	1.4	ns
t_{PHL}				0.9	1.7		0.9	1.6	
t_{PLH}	CLK	Any Q		3.2	6.9		3.2	6.4	ns
t_{PHL}				2.6	5.3		2.6	4.9	
t_{PLH}	CLK	MAX_MIN		4.9	10.4		4.9	9.4	ns
t_{PHL}				3.7	7.5		3.7	7.1	
t_{PLH}	D_UZ	RCOZ		2.7	5.3		2.7	4.8	ns
t_{PHL}				2.4	4.9		2.4	3.9	
t_{PLH}	D_UZ	MAX_MIN		2.1	4.3		2.1	4.5	ns
t_{PHL}				2.4	4.7		2.4	4.2	
t_{PLH}	CTENZ	RCOZ		1	1.7		1	1.5	ns
t_{PHL}				1	1.9		1	1.7	
Δt_{PLH}	Any	Any Q	0.2	0.56	1.18	0.2	0.56	1.1	ns/pF
Δt_{PHL}			0.18	0.36	0.78	0.18	0.36	0.7	
Δt_{PLH}	Any	RCOZ	0.42	1.29	3.26	0.44	1.29	3	ns/pF
Δt_{PHL}			0.46	1.32	3.04	0.48	1.32	2.74	
Δt_{PLH}	Any	MAX_MIN	0.38	1.14	2.66	0.4	1.14	2.46	ns/pF
Δt_{PHL}			0.4	0.99	2.2	0.42	0.99	1.98	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

S191LJ SYNCHRONOUS UP/DOWN BINARY COUNTER WITH DOWN/UP MODE CONTROL

D3030, APRIL 1988

HDL FILE†

```
BLOCK S191LJ;
D          @INPUT;
C          @INPUT;
B          @INPUT;
A          @INPUT;
CLK        @INPUT;
D_UZ       @INPUT;
CTENZ      @INPUT;
LOADZ      @INPUT;
QD         @OUTPUT;
QC         @OUTPUT;
QB         @OUTPUT;
QA         @OUTPUT;
RCOZ       @OUTPUT;
MAX_MIN    @OUTPUT;
STRUCTURE
FF1        :DFB20LJ   G15O,G09O,G14O,G44O,QA,FF1QZ;
FF2        :DFB20LJ   G24O,G16O,G23O,G44O,QB,FF2QZ;
FF3        :DFB20LJ   G33O,G25O,G32O,G44O,QC,FF3QZ;
FF4        :DFB20LJ   G42O,G34O,G41O,G44O,QD,FF4QZ;
G01        :IV110LJ   D_UZ,G01O;
G02        :IV110LJ   G01O,G02O;
G03        :NO210LJ   G02O,CTENZ,G03O;
G04        :NO210LJ   G01O,CTENZ,G04O;
G05        :NA510LJ   G01O,QA,QB,QC,QD,G05O;
G06        :NA510LJ   G02O,FF1QZ,FF2QZ,FF3QZ,FF4QZ,G06O;
G07        :NA210LJ   G05O,G06O,MAX_MIN;
G08        :NA310LJ   G43O,MAX_MIN,G10O,RCOZ;
G09        :NA210LJ   A,G45O,G09O;
G10        :IV110LJ   CTENZ,G10O;
G11        :IV110LJ   G10O,G11O;
G12        :NA210LJ   QA,G11O,G12O;
G13        :NA210LJ   G10O,FF1QZ,G13O;
G14        :NA210LJ   G12O,G13O,G14O;
G15        :NA210LJ   G46O,G45O,G15O;
G16        :NA210LJ   B,G45O,G16O;
G17        :NA210LJ   G04O,FF1QZ,G17O;
G18        :NA210LJ   QA,G03O,G18O;
G19        :NA210LJ   G17O,G18O,G19O;
G20        :IV110LJ   G19O,G20O;
G21        :NA210LJ   QB,G20O,G21O;
G22        :NA210LJ   G19O,FF2QZ,G22O;
G23        :NA210LJ   G21O,G22O,G23O;
G24        :NA210LJ   G47O,G45O,G24O;
G25        :NA210LJ   C,G45O,G25O;
G26        :NA310LJ   G04O,FF1QZ,FF2QZ,G26O;
G27        :NA310LJ   QA,QB,G03O,G27O;
G28        :NA210LJ   G26O,G27O,G28O;
G29        :IV110LJ   G28O,G29O;
G30        :NA210LJ   QC,G29O,G30O;
G31        :NA210LJ   G28O,FF3QZ,G31O;
G32        :NA210LJ   G30O,G31O,G32O;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

HDL FILE† - Continued

```
G33     :NA210LJ   G48O,G45O,G33O;
G34     :NA210LJ   D,G45O,G34O;
G35     :NA410LJ   G04O,FF1QZ,FF2QZ,FF3QZ,G35O;
G36     :NA410LJ   QA,QB,QC,G03O,G36O;
G37     :NA210LJ   G35O,G36O,G37O;
G38     :IV110LJ   G37O,G38O;
G39     :NA210LJ   QD,G38O,G39O;
G40     :NA210LJ   G37O,FF4QZ,G40O;
G41     :NA210LJ   G39O,G40O,G41O;
G42     :NA210LJ   G49O,G45O,G42O;
G43     :IV110LJ   CLK,G43O;
G44     :IV120LJ   G43O,G44O;
G45     :IV110LJ   LOADZ,G45O;
G46     :IV110LJ   A,G46O;
G47     :IV110LJ   B,G47O;
G48     :IV110LJ   C,G48O;
G49     :IV110LJ   D,G49O;
END S191LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

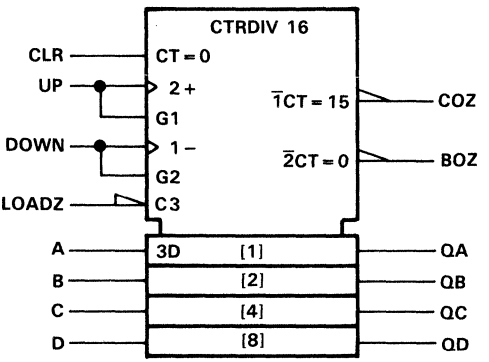
S193LJ
SYNCHRONOUS 4-BIT UP/DOWN COUNTER WITH DUAL CLOCK AND CLEAR

D3030, APRIL 1988

SOFTWARE MACRO

- Dual Clock Inputs for Sourcing Count Direction
- Fully Synchronous in Count Modes
- Parallel Asynchronous Load for Modulo-N Count Sequences
- Asynchronous Clear
- Look-Ahead Circuitry Enhances Performance of Cascaded Counters

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S193LJ software macro implements a synchronous, reversible up/down, 4-bit binary counter with dual clock inputs and a separate clear input. Its 4-bit length means that testability is simplified when constructing large counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters. The S193LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN210LJ	1.5	6	9	1.98
AN310LJ	1.75	2	3.5	0.76
AN410LJ	2	2	4	0.84
IV110LJ	0.75	4	3	0.64
IV120LJ	1	4	4	1.24
NA210LJ	1	4	4	0.76
NA310LJ	1.25	4	5	0.76
NA520LJ	3.25	2	6.5	2.1
NO210LJ	1	4	4	0.48
TAB20LJ	7.5	4	30	6.44
TOTALS		36	73	16

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S193LJ
SYNCHRONOUS 4-BIT UP/DOWN COUNTER WITH DUAL CLOCK AND CLEAR

D3030, APRIL 1988

When the counter is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S193LJ A,B,C,D,UP,DOWN,LOADZ,CLR,BOZ,COZ,QA,QB,QC,QD;

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (UP or DOWN). The direction of counting is determined by which count input is pulsed while the other count input is high. These counters are fully programmable; that is, they may be preset to any number between 0 and 15 by placing a low on the load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

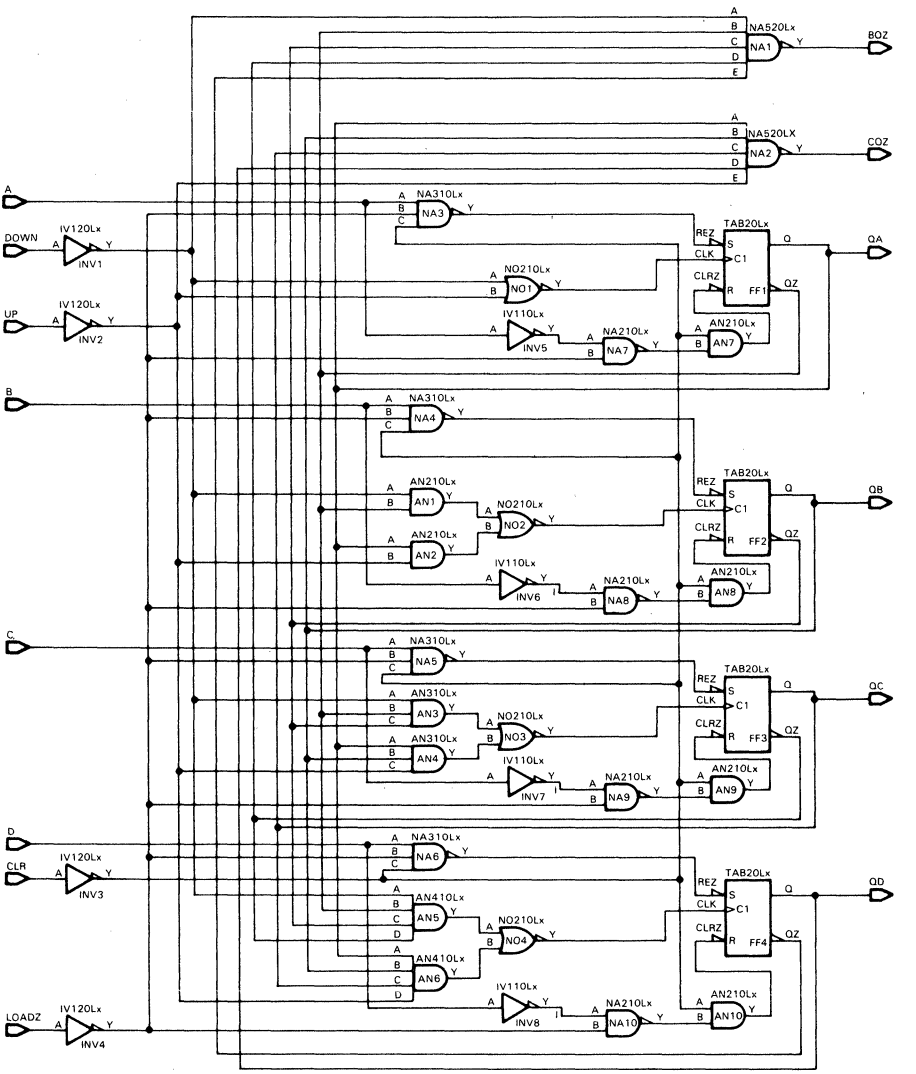
A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters are designed to be cascaded without the need for additional circuitry. The borrow output (BOZ) produces a low-level pulse while the count is zero (all outputs low) and the count-down is low. Similarly, the carry output (COZ) produces a low-level pulse while the count is maximum (all outputs high) and the count-up input is low. The counters are cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

S193LJ
SYNCHRONOUS 4-BIT UP/DOWN COUNTER WITH DUAL CLOCK AND CLEAR

D3030, APRIL 1988

logic diagram

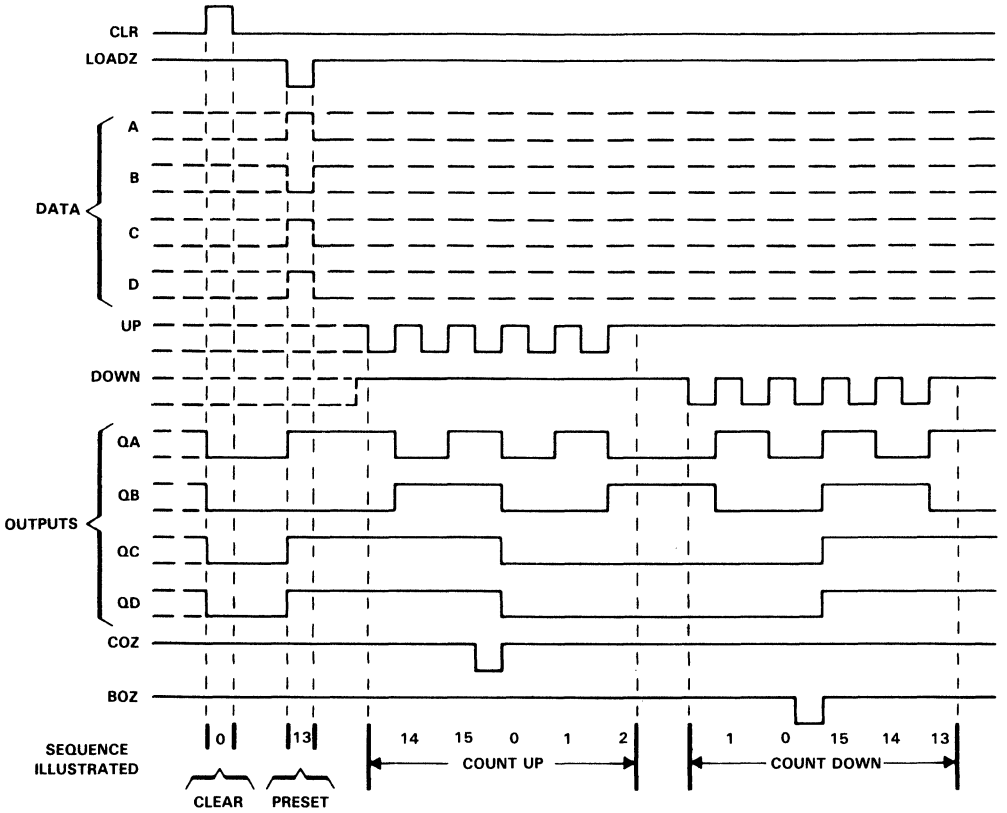


TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

typical clear, load, and count sequences (see Notes A and B)

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Load (preset) to binary thirteen
3. Count up to fourteen, fifteen (carry), zero, one, and two
4. Count down to one, zero (borrow), fifteen, fourteen and thirteen.



NOTES: A. Clear overrides load, data and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A, B, C, D		0.05		pF
		All other inputs		0.11		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	15.4		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	UP	COZ		1.1	2.2		1.1	2.1	ns
t_{PHL}				1.6	3.3		1.6	3.1	
t_{PLH}	DOWN	BOZ		1.1	2.4		1.1	2.1	ns
t_{PHL}				1.6	3.5		1.6	3.2	
t_{PLH}	DOWN,UP	Any Q		4.2	9.5		4.2	8.7	ns
t_{PHL}				3.5	7.8		3.5	7.1	
t_{PLH}	LOADZ	Any Q		3	6		3	5.5	ns
t_{PHL}				2.7	5.7		2.7	5.3	
t_{PHL}	CLR	Any Q		2.1	4.3		2.1	4	ns
Δt_{PLH}	Any	Any Q	0.2	0.56	1.24	0.22	0.56	1.14	ns/pF
Δt_{PHL}			0.16	0.38	0.82	0.16	0.38	0.74	
Δt_{PLH}	Any	BOZ,COZ	0.16	0.46	0.96	0.18	0.46	0.88	ns/pF
Δt_{PHL}			0.14	0.36	0.76	0.16	0.36	0.68	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

S193LJ
SYNCHRONOUS 4-BIT UP/DOWN COUNTER WITH DUAL CLOCK AND CLEAR

D3030, APRIL 1988

HDL FILE†

```
BLOCK S193LJ;
A          @INPUT;
B          @INPUT;
C          @INPUT;
D          @INPUT;
UP         @INPUT;
DOWN       @INPUT;
LOADZ      @INPUT;
CLR        @INPUT;
BOZ        @OUTPUT;
COZ        @OUTPUT;
QA         @OUTPUT;
QB         @OUTPUT;
QC         @OUTPUT;
QD         @OUTPUT;
STRUCTURE
AN1        :AN210LJ   INV1S,FF1S,AN1S;
AN10       :AN210LJ   INV3S,NA10S,AN10S;
AN2        :AN210LJ   QA,INV2S,AN2S;
AN3        :AN310LJ   INV1S,FF1S,FF2S,AN3S;
AN4        :AN310LJ   QA,QB,INV2S,AN4S;
AN5        :AN410LJ   INV1S,FF1S,FF2S,FF3S,AN5S;
AN6        :AN410LJ   QA,QB,QC,INV2S,AN6S;
AN7        :AN210LJ   INV3S,NA7S,AN7S;
AN8        :AN210LJ   INV3S,NA8S,AN8S;
AN9        :AN210LJ   INV3S,NA9S,AN9S;
FF1        :TAB20LJ   AN7S,NA3S,NO1S,QA,FF1S;
FF2        :TAB20LJ   AN8S,NA4S,NO2S,QB,FF2S;
FF3        :TAB20LJ   AN9S,NA5S,NO3S,QC,FF3S;
FF4        :TAB20LJ   AN10S,NA6S,NO4S,QD,FF4S;
INV1       :IV120LJ   DOWN,INV1S;
INV2       :IV120LJ   UP,INV2S;
INV3       :IV120LJ   CLR,INV3S;
INV4       :IV120LJ   LOADZ,INV4S;
INV5       :IV110LJ   A,INV5S;
INV6       :IV110LJ   B,INV6S;
INV7       :IV110LJ   C,INV7S;
INV8       :IV110LJ   D,INV8S;
NA1        :NA520LJ   INV1S,FF1S,FF2S,FF3S,FF4S,BOZ;
NA10       :NA210LJ   INV8S,INV4S,NA10S;
NA2        :NA520LJ   QA,QB,QC,QD,INV2S,COZ;
NA3        :NA310LJ   A,INV4S,INV3S,NA3S;
NA4        :NA310LJ   B,INV4S,INV3S,NA4S;
NA5        :NA310LJ   C,INV4S,INV3S,NA5S;
NA6        :NA310LJ   D,INV4S,INV3S,NA6S;
NA7        :NA210LJ   INV5S,INV4S,NA7S;
NA8        ;NA210LJ   INV6S,INV4S,NA8S;
NA9        :NA210LJ   INV7S,INV4S,NA9S;
NO1        :NO210LJ   INV1S,INV2S,NO1S;
NO2        :NO210LJ   AN1S,AN2S,NO2S;
NO3        :NO210LJ   AN3S,AN4S,NO3S;
NO4        :NO210LJ   AN5S,AN6S,NO4S;
END S193LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

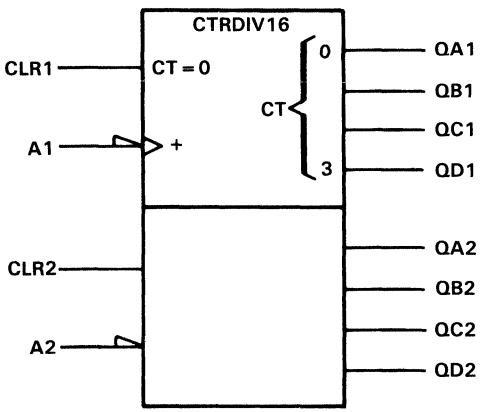
S393LJ
DUAL FOUR-BIT RIPPLE COUNTER

D3030, APRIL 1988

SOFTWARE MACRO

- **Software Dual Four-Bit Counter for Custom IC Applications**
- **Direct Clear Input Simplifies Initialization or Cycle Length**
- **Embedded Clock Drivers Provide Symmetrical Performance Across Long Counters**
- **Cascadable and Expandable for Full Customization**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S393LJ software macro implements dual 4-bit binary counter elements. The dual 4-bit configuration simplifies construction of large counters. This software macro reduces input loading for implementation of larger counters, when standard library buffer cells are used to buffer each clock and clear input to further enhance the performance across long counters. The S393LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV110LJ	0.75	4	3	0.64
R2408LJ	23.5	2	47	5.24
TOTALS		6	50	5.88

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S393LJ A1,CLR1,A2,CLR2,QA1,QB1,QC1,QD1,QA2,QB2,QC2,QD2;

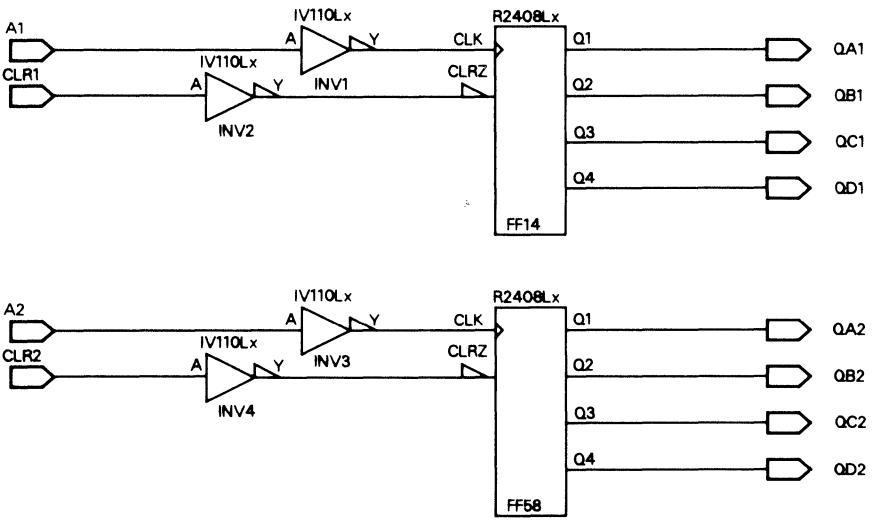
S393LJ
DUAL FOUR-BIT RIPPLE COUNTER

D3030, APRIL 1988

FUNCTION TABLE
(EACH COUNTER)

INPUTS		OUTPUTS			
CLRn	An	QDn	QCn	QBn	QAn
H	X	L	L	L	L
L	↓	L	L	L	H
L	↓	L	L	H	L
L	↓	L	L	H	H
L	↓	L	H	L	L
L	↓	L	H	L	H
L	↓	L	H	H	L
L	↓	L	H	H	H
L	↓	H	L	L	L
L	↓	H	L	L	H
L	↓	H	L	H	L
L	↓	H	L	H	H
L	↓	H	H	L	L
L	↓	H	H	L	H
L	↓	H	H	H	L
L	↓	H	H	H	H
L	↓	L	L	L	L

logic diagram



D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These aare specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	An		0.05		pF
		CLRn		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	5.9		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	An	QAn		1.9	4.2		1.9	3.8	ns
t_{PHL}				1.9	4.2		1.9	3.9	
t_{PLH}	An	QDn		4.8	11.4		4.8	8.6	ns
t_{PHL}				4.5	10.7		4.5	9.8	
t_{PHL}	CLRn	Any Q		1.7	3.4		1.7	3.1	ns
Δt_{PLH}	An	Any Q	0.2	0.62	1.34	0.2	0.62	1.24	ns/pF
Δt_{PHL}			0.16	0.46	0.98	0.16	0.46	0.88	
Δt_{PHL}	CLRn	Any Q	0.18	0.46	0.98	0.18	0.46	0.88	ns/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

HDL FILE†

```
BLOCK S393LJ;
A1          @INPUT;
CLR1        @INPUT;
A2          @INPUT;
CLR2        @INPUT;
QA1         @OUTPUT;
QB1         @OUTPUT;
QC1         @OUTPUT;
QD1         @OUTPUT;
QA2         @OUTPUT;
QB2         @OUTPUT;
QC2         @OUTPUT;
QD2         @OUTPUT;

STRUCTURE
INV1        :IV110LJ    A1,INV1O;
INV2        :IV110LJ    CLR1,INV2O;
INV3        :IV110LJ    A2,INV3O;
INV4        :IV110LJ    CLR2,INV4O;
FF14        :R2408LJ    INV1O,INV2O,QA1,QB1,QC1,QD1;
FF58        :R2408LJ    INV3O,INV4O,QA2,QB2,QC2,QD2;
END S393LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

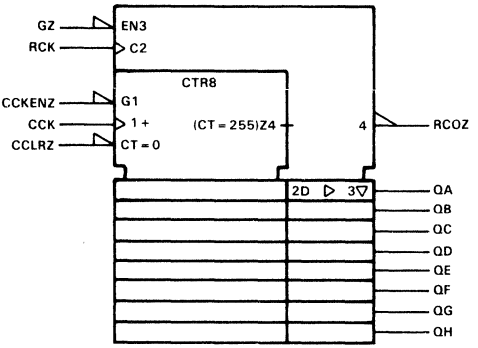
S590LJ
8-BIT BINARY COUNTER
WITH 3-STATE OUTPUT REGISTERS

D3030, APRIL 1988

SOFTWARE MACRO

- **8-Bit Counter with Register**
- **Individual Positive-Edge Triggered Clocks for Counter and Register**
- **3-State Output Register Provides Parallel Bus Interface**
- **Counter Has Direct Clear and Clock Enable**
- **Ripple-Carry Output Simplifies Expansion**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S590LJ software macro implements a synchronous 8-bit binary counter element. The 8-bit configuration simplifies construction of large counters. The S590LJ 8-bit binary counter feeds an 8-bit storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input, CCLRZ, and a count enable input, CCKENZ. For cascading, a ripple-carry output, RCOZ, is provided. Expansion is easily accomplished by tying RCOZ of the lower stage to CCKENZ of the higher stage, etc.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S590LJ
8-BIT BINARY COUNTER
WITH 3-STATE OUTPUT REGISTERS

D3030, APRIL 1988

The S590LJ is implemented with the standard cell functions indicated:

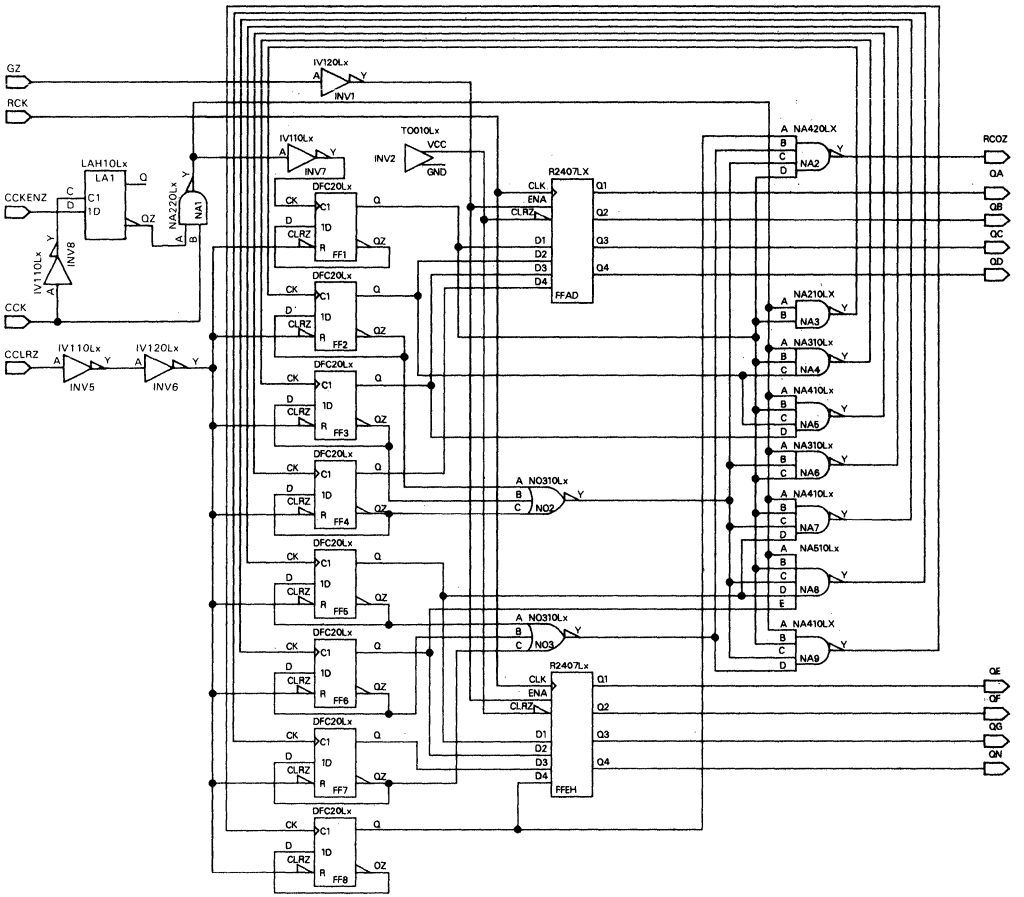
CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
DFC20LJ	6.75	8	54	15.04
IV110LJ	0.75	3	2.25	0.48
IV120LJ	1	2	2	0.62
LAH10LJ	3.75	1	3.75	0.75
NA210LJ	1	1	1	0.19
NA220LJ	1.5	1	1.5	0.38
NA310LJ	1.25	2	2.5	0.38
NA410LJ	1.5	3	4.5	0.57
NA420LJ	2.5	1	2.5	0.39
NA510LJ	3	1	3	0.88
NO310LJ	1.25	2	2.5	0.26
R2407LJ	24.5	2	49	9.92
TO010LJ	1.5	1	1.5	NIL
TOTALS		28	130	29.86

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S590LJ CCK,CCKENZ,RCK,CCLRZ,GZ,QA,QB,QC,QD,QE,QF,QG,QH,RCOZ;

Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CCK		0.12		pF
		CCKENZ		0.06		
		CCLRZ		0.05		
		GZ		0.11		
		RCK		0.22		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f = 1$ ns	29.14		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Notes 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CCK	RCOZ		3	6.1		3	5.6	ns
t_{PHL}				4	8.4		4	7.6	
t_{PLH}	CCLRZ	RCOZ		4.4	4.7		4.4	4.5	ns
t_{PLH}	RCK	Qn		1.6	3.5		1.6	3.2	ns
t_{PHL}	GZ	Qn		1.7	3.9		1.7	3.6	ns
t_{PZH}				1	1.9		1	1.9	
t_{PZL}				0.9	1.6		0.9	1.6	
Δt_{PLH}	RCK	Qn	0.77	2.14	4.64	0.82	2.14	4.27	ns/pF
Δt_{PHL}			0.51	1.33	2.76	0.55	1.33	2.54	
Δt_{PLH}	CCLRZ	RCOZ	0.22	0.68	1.46	0.24	0.68	1.34	ns/pF
Δt_{PHL}			0.26	0.78	1.82	0.28	0.78	1.62	
Δt_{PZH}	GZ	Qn	0.77	2.2	4.93	0.82	2.2	4.51	ns/pF
Δt_{PZL}			0.54	1.38	3.23	0.57	1.38	2.88	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance.

2. Enable and delta-enable times are measured using the conditions specified for the R2407LJ.

S590LJ
8-BIT BINARY COUNTER WITH 3-STATE OUTPUT REGISTERS

D3030, APRIL 1988

HDL FILE†

```
BLOCK S590LJ;
CCK        @INPUT;
CCKENZ     @INPUT;
RCK        @INPUT;
CCLRZ      @INPUT;
GZ         @INPUT;
QA         @OUTPUT;
QB         @OUTPUT;
QC         @OUTPUT;
QD         @OUTPUT;
QE         @OUTPUT;
QF         @OUTPUT;
QG         @OUTPUT;
QH         @OUTPUT;
RCOZ       @OUTPUT;
STRUCTURE
FF1        :DFC20LJ   INV6O,FF1QZ,INV70,FF1Q,FF1QZ;
FF2        :DFC20LJ   INV6O,FF2QZ,NA3O,FF2Q,FF2QZ;
FF3        :DFC20LJ   INV6O,FF3QZ,NA4O,FF3Q,FF3QZ;
FF4        :DFC20LJ   INV6O,FF4QZ,NA5O,FF4Q,FF4QZ;
FF5        :DFC20LJ   INV6O,FF5QZ,NA6O,FF5Q,FF5QZ;
FF6        :DFC20LJ   INV6O,FF6QZ,NA7O,FF6Q,FF6QZ;
FF7        :DFC20LJ   INV6O,FF7QZ,NA8O,FF7Q,FF7QZ;
FF8        :DFC20LJ   INV6O,FF8QZ,NA9O,FF8Q,FF8QZ;
INV1       :IV120LJ   GZ,INV1O;
INV2       :TO010LJ   TIELO,TIEHI;
INV5       :IV110LJ   CCLRZ,INV5O;
INV6       :IV120LJ   INV5O,INV6O;
INV7       :IV110LJ   NA1O,INV7O;
INV8       :IV110LJ   CCK,INV8O;
NA1        :NA220LJ   LA1O,CCK,NA1O;
LA1        :LAH10LJ   CCKENZ,INV80,DUM,LA1O;
NA2        :NA420LJ   FF8Q,NO3O,NO2O,FF1Q,RCOZ;
NA3        :NA210LJ   NA1O,FF1Q,NA3O;
NA4        :NA310LJ   NA1O,FF1Q,FF2Q,NA4O;
NA5        :NA410LJ   NA1O,FF1Q,FF2Q,FF3Q,NA5O;
NA6        :NA310LJ   NA1O,NO2O,FF1Q,NA6O;
NA7        :NA410LJ   NA1O,FF1Q,NO2O,FF5Q,NA7O;
NA8        :NA510LJ   NA1O,FF1Q,NO2O,FF5Q,FF6Q,NA8O;
NA9        :NA410LJ   NA1O,FF1Q,NO2O,NO3O,NA9O;
NO2        :NO310LJ   FF2QZ,FF3QZ,FF4QZ,NO2O;
NO3        :NO310LJ   FF5QZ,FF6QZ,FF7QZ,NO3O;
FFAD       :R2407LJ   TIEHI,FF1Q,FF2Q,FF3Q,FF4Q,RCK,INV1O,QA,
                      QB,QC,QD;
FFEH       :R2407LJ   TIEHI,FF5Q,FF6Q,FF7Q,FF8Q,RCK,INV10,QE,
                      QF,QG,QH;
END S590LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

S593XLJ
8-BIT BINARY COUNTER WITH INPUT REGISTERS

D3030, APRIL 1988

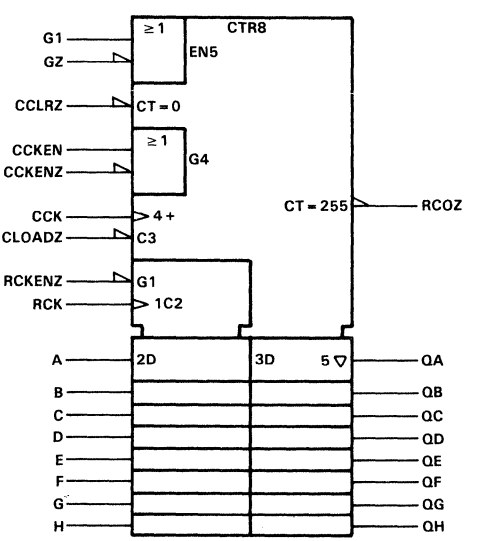
SOFTWARE MACRO

- **8-Bit Counter with Input Registers**
- **Individual Positive-Edge-Triggered Clocks for Counter and Register**
- **3-State Counter Outputs Provide Parallel Bus Interface**
- **Counter Has Direct Clear and Clock Enable**
- **Ripple-Carry Output Simplifies Expansion**

description

The S593XLJ software macro implements a synchronous 8-bit binary counter element. The 8-bit length simplifies construction of large counters. The common data I/O port implemented on the packaged counter has been separated to provide individual data inputs to the register and individual 3-state outputs from the S593XLJ counter. The S593XLJ implements an 8-bit storage register that feeds an 8-bit binary counter. The counter has parallel 3-state outputs. Separate clocks are provided for both the binary counter and storage register.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S593XLJ
8-BIT BINARY COUNTER WITH INPUT REGISTERS

D3030, APRIL 1988

The S593XLJ is implemented with the standard cell functions indicated:

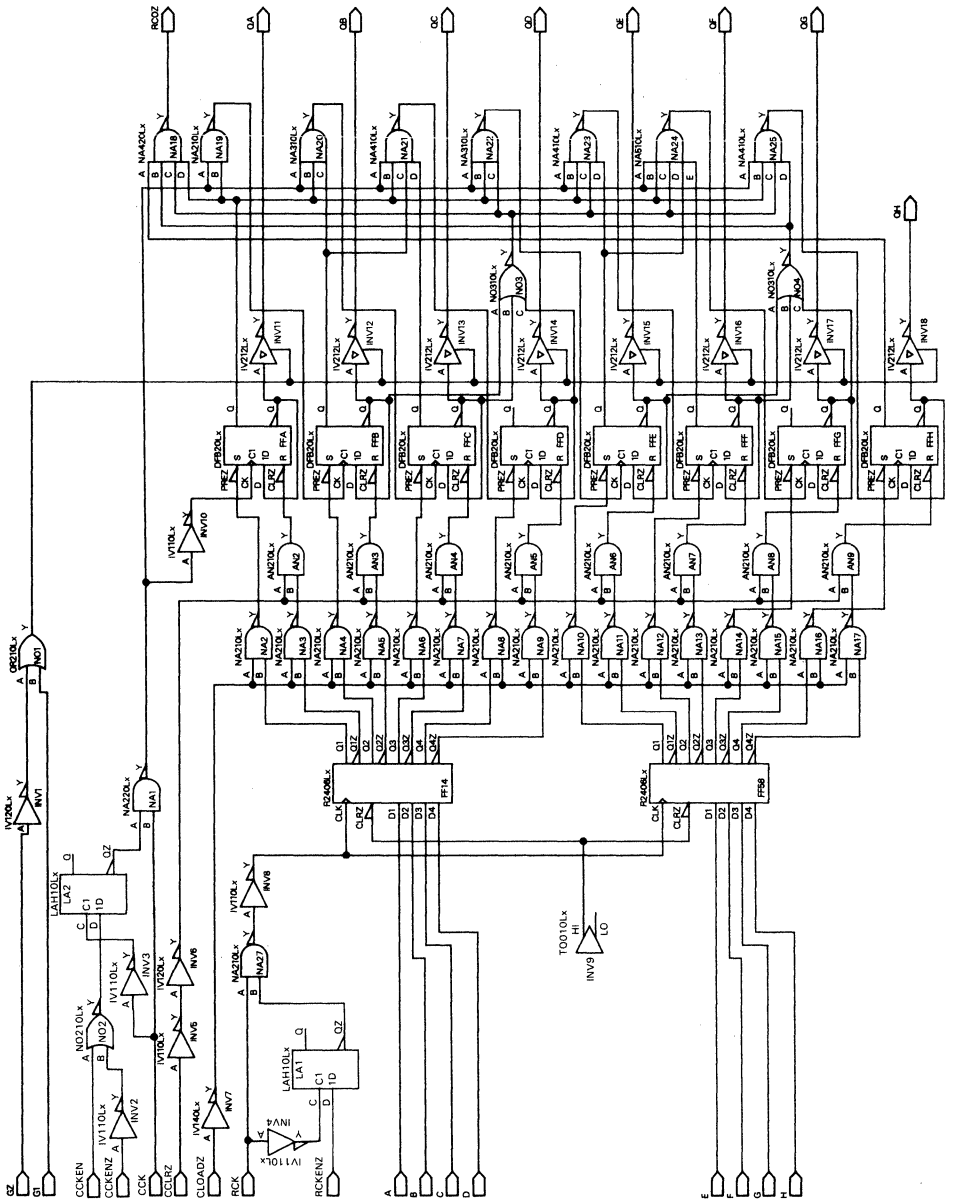
CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN210LJ	1.5	8	12	2.64
DFB20LJ	7.25	8	58	14.24
IV110LJ	0.75	6	4.5	0.96
IV120LJ	1	2	2	0.62
IV140LJ	1.5	1	1.5	0.63
IV212LJ	1.25	8	10	1.44
LAH10LJ	3.75	2	7.5	0.78
NA210LJ	1	17	17	3.23
NA220LJ	1.5	1	1.5	0.38
NA310LJ	1.25	2	2.5	0.38
NA410LJ	1.5	3	4.5	0.57
NA420LJ	2.5	1	2.5	0.39
NA510LJ	3	1	3	0.88
NO210LJ	1	1	1	0.12
NO310LJ	1.25	2	2.5	0.26
OR210LJ	1.25	1	1.25	0.37
R2406LJ	23.5	2	47	10.32
TO010LJ	0.75	1	0.75	NIL
TOTALS		67	179	38.21

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S593XLJ A,B,C,D,E,F,G,H,CCK,CCKEN,CCKENZ,RCK,RCKENZ, CCLRZ,CLOADZ, G1,GZ,QA,QB,QC,QD,QE,QF,QG,QH,RCOZ;

The binary counter features a direct clear input, CCLRZ, and a count enable input, CCKENZ. For cascading, a ripple-carry output, RCOZ, is provided. Expansion is easily accomplished by tying RCOZ of the lower stage to CCKENZ of the higher stage, etc. Both the counter and register clocks are positive-edge-triggered. If the user wishes to connect both clocks together, the counter state will equal the previous register contents plus one. Internal circuitry prevents clocking from the clock enable.

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A thru H		0.06		pF
		CCK		0.12		
		CLOADZ		0.23		
		G1		0.05		
		Z		0.11		
		All other inputs		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	37.56		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Notes 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CCKZ	RCOZ		3.2	6.8		3.2	6	ns
t_{PHL}				4	8.7		4	7.8	
t_{PLH}	CCLRZ	RCOZ		3	5.8		3	5.4	ns
t_{PHL}	CCLRZ	Qn		3.7	7.9		3.7	7.3	
t_{PLH}	CCK	Qn		3.4	7.6		3.4	6.3	ns
t_{PHL}				3.9	8.2		3.9	7.3	
t_{PLH}	CLOADZ	Qn		2.4	5		2.4	4.6	ns
t_{PHL}				3.8	8.4		3.8	7.5	
t_{PLH}	CLOADZ	RCOZ		5.8	6		5.8	5.7	ns
t_{PHL}				4.8	10		4.8	8.9	
t_{PZH}	GZ	Qn		2	4.3		2	3.8	ns
t_{PZL}				2	3.6		2	3.6	
t_{PZH}	G1	Qn		1.8	3.8		1.8	3.4	ns
t_{PZL}				1.8	3.6		1.8	3.2	
Δt_{PLH}	Any	Qn	0.7	2.08	4.52	0.76	2.08	4.16	ns/pF
Δt_{PHL}			0.48	1.22	2.7	0.52	1.22	2.42	
Δt_{PLH}	Any	RCOZ	0.22	0.68	1.46	0.24	0.68	1.34	ns/pF
Δt_{PHL}			0.26	0.78	1.82	0.28	0.78	1.62	
Δt_{PZH}	Any	Qn	0.76	2.14	4.8	0.8	2.14	4.38	ns/pF
Δt_{PZL}			0.52	1.26	2.88	0.56	1.26	2.56	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance.

2. Enable and delta-enable times are measured using the conditions specified for the IV212LJ.

S593XLJ
8-BIT BINARY COUNTER WITH INPUT REGISTERS

D3030, APRIL 1988

HDL FILE†

```
BLOCK S593XLJ;
A       @INPUT;
B       @INPUT;
C       @INPUT;
D       @INPUT;
E       @INPUT;
F       @INPUT;
G       @INPUT;
H       @INPUT;
CCK     @INPUT;
CCKEN   @INPUT;
CCKENZ  @INPUT;
RCK     @INPUT;
RCKENZ  @INPUT;
CCLRZ   @INPUT;
CLOADZ  @INPUT;
G1      @INPUT;
GZ      @INPUT;
QA      @OUTPUT;
QB      @OUTPUT;
QC      @OUTPUT;
QD      @OUTPUT;
QE      @OUTPUT;
QF      @OUTPUT;
QG      @OUTPUT;
QH      @OUTPUT;
RCOZ    @OUTPUT;

STRUCTURE
AN2     :AN210LJ   INV6O,NA3O,AN2O;
AN3     :AN210LJ   INV6O,NA5O,AN3O;
AN4     :AN210LJ   INV6O,NA7O,AN4O;
AN5     :AN210LJ   INV6O,NA9O,AN5O;
AN6     :AN210LJ   INV6O,NA11O,AN6O;
AN7     :AN210LJ   INV6O,NA13O,AN7O;
AN8     :AN210LJ   INV6O,NA15O,AN8O;
AN9     :AN210LJ   INV6O,NA17O,AN9O;
FFA     :DFB20LJ   AN2O,NA2O,FFAQZ,INV10O,FFAQ,FFAQZ;
FFB     :DFB20LJ   AN3O,NA4O,FFBQZ,NA19O,FFBQ,FFBQZ;
FFC     :DFB20LJ   AN4O,NA6O,FFCQZ,NA20O,FFCQ,FFCQZ;
FFD     :DFB20LJ   AN5O,NA8O,FFDQZ,NA21O,DUM,FFDQZ;
FFE     :DFB20LJ   AN6O,NA10O,FFEQZ,NA22O,FFEQ,FFEQZ;
FFF     :DFB20LJ   AN7O,NA12O,FFFQZ,NA23O,FFFQ,FFFQZ;
FFG     :DFB20LJ   AN8O,NA14O,FFGQZ,NA24O,DUM,FFGQZ;
FFH     :DFB20LJ   AN9O,NA16O,FFHQZ,NA25O,FFHQ,FFHQZ;
FF14    :R2406LJ   TIEHI,A,B,C,D,RCFQZ,F1Q,F1QZ,
                   F2Q,F2QZ,F3Q,F3QZ,FQ4,F4QZ;
FF58    :R2406LJ   TIEHI,E,F,G,H,RCFQZ,F1Q,F1QZ,
                   F6Q,F6QZ,F7Q,F7QZ,F8Q,F8QZ;
INV1    :IV120LJ   GZ,INV1O;
INV2    :IV110LJ   CCKENZ,INV2O;
INV3    :IV110LJ   CCK,INV3O;
INV4    :IV110LJ   RCK,INV4O;
INV5    :IV11OLJ   CCLRZ,INV5O;
INV6    :IV120LJ   INV5O,INV6O;
INV7    :IV140LJ   CLOADZ,INV7O;
INV8    :IV110LJ   NA27O,RCFQZ;
INV9    :TO010LJ   TIELO,TIEHI;
INV10   :IV110LJ   NA1O,INV10O;
INV11   :IV212LJ   FFAQZ,NO1O,QA;
INV12   :IV212LJ   FFBQZ,NO1O,QB;
INV13   :IV212LJ   FFCQZ,NO1O,QC;
INV14   :IV212LJ   FFDQZ,NO1O,QD;
INV15   :IV212LJ   FFEQZ,NO1O,QE;
INV16   :IV212LJ   FFFQZ,NO1O,QF;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

HDL FILE† - Continued

```
INV17     :IV212LJ    FFGQZ,NO1O,QG;
INV18     :IV212LJ    FFHQZ,NO1O,QH;
LA1       :LAH10LJ    RCKENZ,INV4O,DUM,LA1O;
LA2       :LAH10LJ    N02O,INV3O,DUM,LA2O;
NA1       :NA220LJ    LA2O,CCK,NA1O;
NA2       :NA210LJ    INV7O,F1Q,NA2O;
NA3       :NA210LJ    INV7O,F1QZ,NA3O;
NA4       :NA210LJ    INV7O,F2Q,NA4O;
NA5       :NA210LJ    INV7O,F2QZ,NA5O;
NA6       :NA210LJ    INV7O,F3Q,NA6O;
NA7       :NA210LJ    INV7O,F3QZ,NA7O;
NA8       :NA210LJ    F4Q,INV7O,NA8O;
NA9       :NA210LJ    INV7O,F4QZ,NA9O;
NA10      :NA210LJ    INV7O,F5Q,NA10O;
NA11      :NA210LJ    INV7O,F5QZ,NA11O;
NA12      :NA210LJ    INV7O,F6Q,NA12O;
NA13      :NA210LJ    INV7O,F6QZ,NA13O;
NA14      :NA210LJ    INV7O,F7Q,NA14O;
NA15      :NA210LJ    INV7O,F7QZ,NA15O;
NA16      :NA210LJ    F8Q,INV7O,NA16O;
NA17      :NA210LJ    INV7O,F8QZ,NA17O;
NA18      :NA420LJ    FFHQ,NO4O,NO3O,FFAQ,RCOZ;
NA19      :NA210LJ    NA1O,FFAQ,NA19O;
NA20      :NA310LJ    NA1O,FFAQ,FFBQ,NA20O;
NA21      :NA410LJ    NA1O,FFAQ,FFBQ,FFCQ,NA21O;
NA22      :NA310LJ    NA1O,FFAQ,NO3O,NA22O;
NA23      :NA410LJ    NA1O,FFAQ,NO3O,FFEQ,NA23O;
NA24      :NA510LJ    NA1O,FFAQ,NO3O,FFEQ,FFFQ,NA24O;
NA25      :NA410LJ    NA1O,FFAQ,NO3O,NO4O,NA25O;
NA27      :NA210LJ    RCK,LA1O,NA27O;
NO1       :OR210LJ    INV1O,G1,NO1O;
NO2       :NO21OLJ    CCKEN,INV2O,NO2O;
NO3       :NO310LJ    FFBQZ,FFCQZ,FFDQZ,NO3O;
NO4       :NO310LJ    FFEQZ,FFFQZ,FFGQZ,NO4O;
END S593XLJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

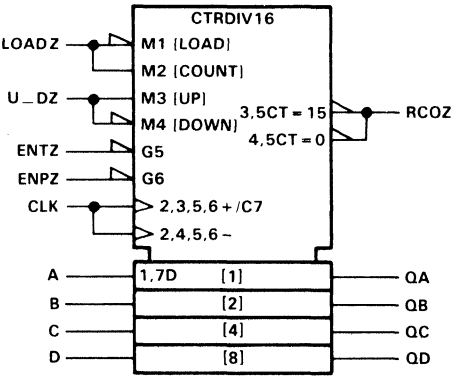
S669LJ
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTER WITH LOOK-AHEAD

D3030, APRIL 1988

SOFTWARE MACRO

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**
- **Buffered Outputs**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S669LJ software macro implements a synchronous 4-bit up-down binary counter. The 4-bit length simplifies construction of large counters. These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally assoicated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

The S669LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN320LJ	2	1	2	0.35
AO221LJ	1.75	4	7	0.88
IV110LJ	0.75	7	5.25	1.12
IV120LJ	1	3	3	0.93
NA210LJ	1	6	6	1.14
NA310LJ	1.25	10	12.5	1.9
NA410LJ	1.5	2	3	0.38
NA510LJ	3	2	6	1.76
R2406LJ	23.5	1	23.5	5.16
TO010LJ	0.75	1	0.75	NIL
TOTALS		37	69	13.82

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S669LJ D,C,B,A,CLK,U_DZ,ENPZ,ENTZ,LOADZ,QD,QC,QB,QA,RCOZ;

These counters are fully programmable; that is, they may be preset to any number between 0 and 15. As loading is synchronous, setting up a low level at the load input disables the counter and causes the output to agree with the data inputs after the next clock pulse.

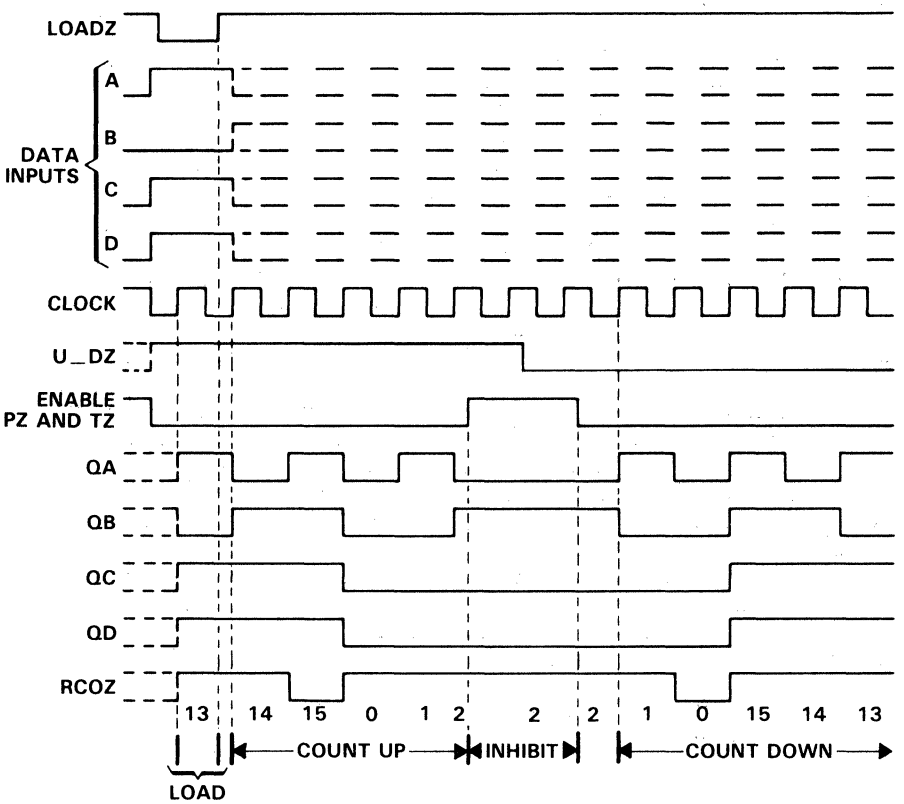
The carry look-ahead circuitry provides for cascading counters in n-bit synchronous applications without additional gating. Instrumental in achieving this are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENPZ and ENTZ) must be low to count. ENPZ enables the local 4-bits and the ENTZ is fed forward to globally extend the enable/disable of previous/next 4-bit cascaded counters. The ripple-carry out RCOZ, when locally and globally enabled, will output a low-level pulse that is used to enable successive stages. Transitions at the ENPZ and ENTZ inputs are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENPZ, ENTZ, LOADZ, U_DZ) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enable, disable, load, or count) will be dictated solely by the conditions meeting the setup and hold times.

typical load, count, and inhibit sequences

This sequence shows the following characteristics:

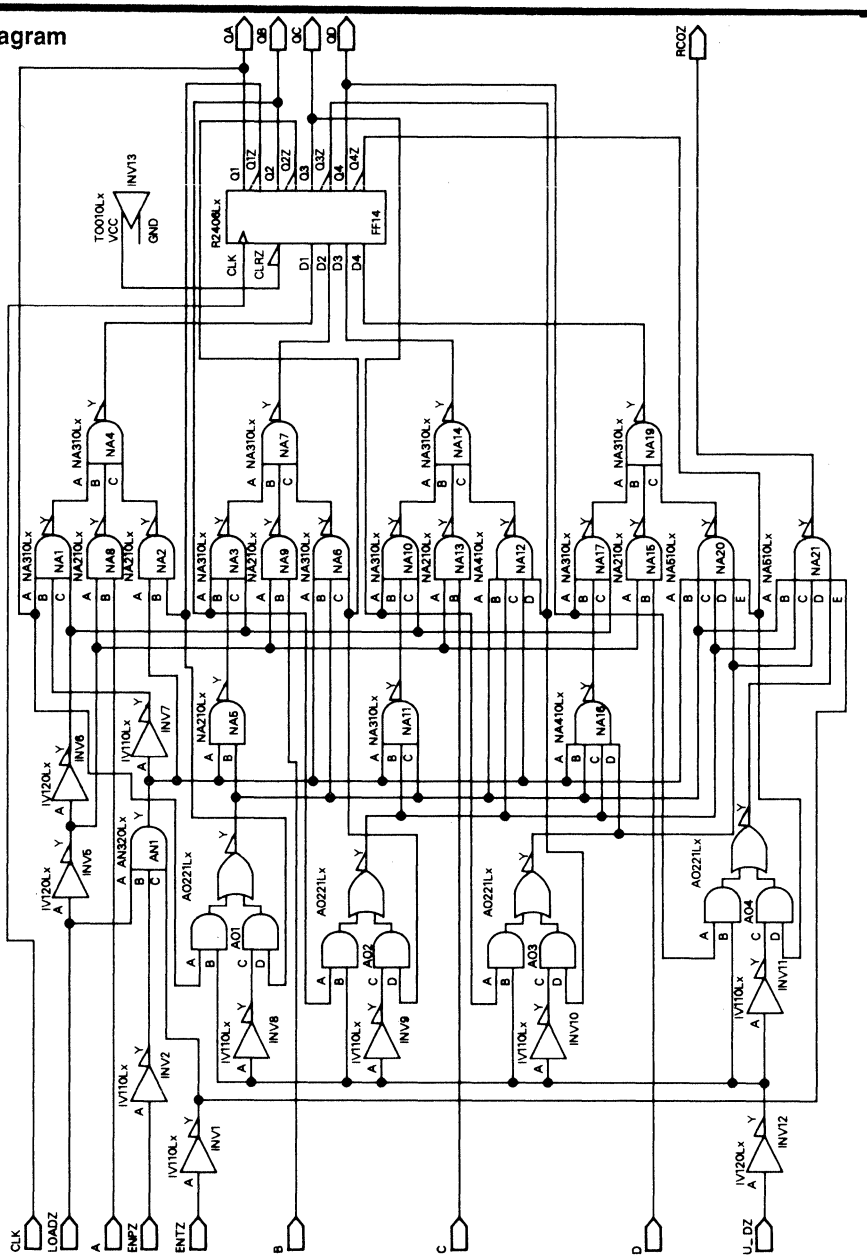
1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, two, and
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



S669LJ
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTER WITH LOOK-AHEAD

D3030, APRIL 1988

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S669LJ
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTER WITH LOOK-AHEAD

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK, U_DZ		0.11		pF
		LOADZ		0.16		
		All other inputs		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	13.82		pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Notes 1 and 2)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	RCOZ		2.7	5.9		2.7	5.4	ns
t_{PHL}				4.5	10.2		4.5	9.4	
t_{PLH}	CLK	Qn		1.5	3.4		1.5	3	ns
t_{PHL}				1.7	3.8		1.7	3.5	
t_{PLH}	ENTZ	RCOZ		1.1	2.2		1.1	2	ns
t_{PHL}				1.5	3.1		1.5	3	
t_{PLH}	U_DZ	RCOZ		1.8	3.7		1.8	3.4	ns
t_{PHL}				3.8	8.1		3.8	7.1	
Δt_{PLH}	Any	Qn	0.42	1.12	2.32	0.44	1.12	2.12	ns/pF
Δt_{PHL}			0.34	0.76	1.54	0.36	0.76	1.4	
Δt_{PLH}	Any	RCOZ	0.36	0.92	1.92	0.38	0.92	1.76	ns/pF
Δt_{PHL}			0.24	0.56	1.14	0.24	0.56	1.02	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switcing characteristics are simullations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

S669LJ SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTER WITH LOOK-AHEAD

D3030, APRIL 1988

HDL FILE†

```
BLOCK S669LJ;
D          @INPUT;
C          @INPUT;
B          @INPUT;
A          @INPUT;
CLK        @INPUT;
U__DZ      @INPUT;
ENPZ       @INPUT;
ENTZ       @INPUT;
LOADZ      @INPUT;
QD         @OUTPUT;
QC         @OUTPUT;
QB         @OUTPUT;
QA         @OUTPUT;
RCOZ       @OUTPUT;
STRUCTURE
AN1        :AN320LJ   LOADZ,INV2O,INV1O,AN1O;
AO12       :AO221LJ   QA,INV12O,INV8O,FFAQZ,AO1O;
AO2        :AO221LJ   QB,INV12O,INV9O,FFBQZ,AO2O;
AO3        :AO221LJ   QC,INV12O,INV10O,FFCQZ,AO3O;
AO4        :AO221LJ   QD,INV12O,INV11O,FFDQZ,AO4O;
INV1       :IV110LJ   ENTZ,INV1O;
INV10      :IV110LJ   INV12O,INV10O;
INV11      :IV110LJ   INV12O,INV11O;
INV12      :IV120LJ   U__DZ,INV12O;
INV13      :TO010LJ   DUM,CLRZ;
INV2       :IV110LJ   ENPZ,INV2O;
INV5       :IV120LJ   LOADZ,INV5O;
INV6       :IV120LJ   INV5O,INV6O;
INV7       :IV110LJ   AN1O,INV7O;
INV8       :IV110LJ   INV12O,INV8O;
INV9       :IV110LJ   INV12O,INV9O;
NA1        :NA310LJ   QA,INV7O,INV6O,NA1O;
NA10       :NA310LJ   QC,NA11O,INV6O,NA10O;
NA11       :NA310LJ   AN1O,AO2O,AO1O,NA11O;
NA12       :NA410LJ   AO1O,AO2O,AN1O,FFCQZ,NA12O;
NA13       :NA210LJ   INV5O,C,NA13O;
NA14       :NA310LJ   NA10O,NA13O,NA12O,NA14O;
NA15       :NA210LJ   INV5O,D,NA15O;
NA16       :NA410LJ   AN1O,AO1O,AO2O,AO3O,NA16O;
NA17       :NA310LJ   QD,NA16O,INV6O,NA17O;
NA19       :NA310LJ   NA17O,NA15O,NA20O,NA19O;
NA2        :NA210LJ   AN1O,FFAQZ,NA2O;
NA20       :NA510LJ   AN1O,AO1O,AO2O,AO3O,FFDQZ,NA20O;
NA21       :NA510LJ   AO1O,AO2O,AO3O,AO4O,INV1O,RCOZ;
NA3        :NA310LJ   QB,NA5O,INV6O,NA3O;
NA4        :NA310LJ   NA1O,NA8O,NA2O,NA4O;
NA5        :NA210LJ   AN1O,AO1O,NA5O;
NA6        :NA310LJ   AN1O,AO1O,FFBQZ,NA6O;
NA7        :NA310LJ   NA3O,NA9O,NA6O,NA7O;
NA8        :NA210LJ   INV5O,A,NA8O;
NA9        :NA210LJ   INV5O,B,NA9O;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

HDL FILE† - Continued

```
FF14          :R2406LJ   CLRZ,NA4O,NA7O,NA14O,NA19O,CLK,QA,
                         FFAQZ,QB,FFBQZ,QC,FFCQZ,QD,FFDQZ;

END S669LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

16 Demultiplexers

DEMULTIPLEXERS
FUNCTIONAL INDEX

D3030, APRIL 1988

DECODERS/DEMULTIPLEXERS (HARDWIRED)

DESCRIPTION	CELL NAME	OUTPUT DRIVE	COMMENTS	EQUIVALENT NA210s	PAGE
2-to-4	DE210LJ	1X		4	16-3
2-to-4	DE212LJ	1X	Active H output enable	4	16-4

DECODERS/DEMULTIPLEXERS (SOFTWARE)

DESCRIPTION	MACRO NAME	OUTPUT DRIVE	COMMENTS	EQUIVALENT NA210s	PAGE
3-to-8	S137LJ	1X	Transparent or latched select inputs, active H or L enables for cascading	40.25	16-6
3-to-8	S138LJ	1X	Active L,L, or H cascading enables	29.5	16-11
Dual 2-to-4	S139LJ	1X	Separate active L output enables	24	16-15
Dual 2-to-4	S155LJ	1X	Separate data and enable inputs	23.75	16-19

DE210LJ
2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

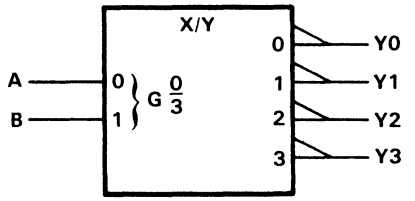
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUTS			
A	B	Y0	Y1	Y2	Y3
L	L	L	H	H	H
H	L	H	L	H	H
L	H	H	H	L	H
H	H	H	H	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DE210LJ cell is an internal 2-line to 4-line decoder/demultiplexer. When the decoder is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DE210LJ A,B,Y0,Y1,Y2,Y3;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.18		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	1.13		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Any	0.2	0.41	1.1	0.2	0.41	1.03	ns
t_{PHL}			0.2	0.46	1.26	0.21	0.46	1.15	
Δt_{PLH}	A, B	Any	0.36	1.08	2.62	0.4	1.08	2.42	ns/pF
Δt_{PHL}			0.36	0.94	2.18	0.38	0.94	1.98	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DE212LJ
2-LINE TO 4-LINE DECODER/DEMULTIPLEXER WITH ACTIVE-HIGH ENABLE

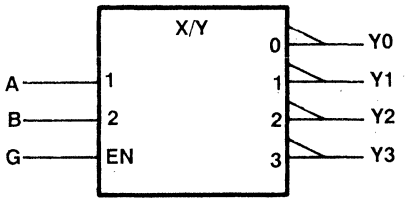
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUTS			
A	B	G	Y0	Y1	Y2	Y3
X	X	L	H	H	H	H
L	L	H	L	H	H	H
H	L	H	H	L	H	H
L	H	H	H	H	L	H
H	H	H	H	H	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The DE212LJ cell is an internal 2-line to 4-line decoder/demultiplexer featuring active-high enable for expandability. When the decoder is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: DE212LJ A,B,G,Y0,Y1,Y2,Y3;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A, B		0.18		pF
		G		0.23		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.12		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A, B	Y	0.22	0.45	1.13	0.22	0.45	1.05	ns
t_{PHL}			0.22	0.52	1.45	0.23	0.52	1.34	
t_{PLH}	G	Y	0.21	0.36	0.68	0.21	0.36	0.63	ns
t_{PHL}			0.21	0.37	0.73	0.2	0.37	0.67	
Δt_{PLH}	A, B	Y	0.42	1.22	3.06	0.44	1.22	2.82	ns/pF
Δt_{PHL}			0.44	1.31	3.08	0.48	1.31	2.78	
Δt_{PLH}	G	Y	0.38	1.06	2.3	0.44	1.06	2.12	ns/pF
Δt_{PHL}			0.44	1.31	3.1	0.48	1.31	2.78	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

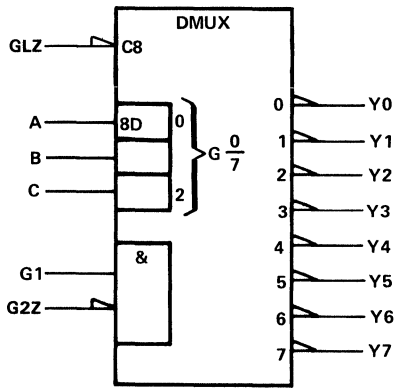
S137LJ
3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

D3030, APRIL 1988

SOFTWARE MACRO

- **Latched Address Lines Ensure Stable Bus Interface**
- **Expandable Select Width**
- **Parallel Decoders for Multiple-Bit Words**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S137LJ software macro implements a 3-line to 8-line decoder/demultiplexer. The S137LJ incorporates a 3-bit latch on the three address inputs to simplify system design, as the data selected is stored and is available until replaced by another selection. When the latch-enable input (GLZ) is low, the S137LJ acts as a decoder/demultiplexer. When GLZ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as GLZ remains high. This latching capability makes the S137LJ ideally suited for implementing stable decoders for strobed (stored-address) applications in bus-oriented systems.

Also provided in the macro are output controls, G1 and G2Z, that enable and disable the outputs. When enabled (G1 is high and G2Z is low), the selected output is low. When disabled (G1 is low or G2Z is high), all outputs are high. These controls permit the macro to be cascaded to accommodate wider multiplexers, as only the anbled 8-bit field will contain an active-low data bit. The S137LJ is implemented with standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN210LJ	1.5	6	9	1.98
IV110LJ	0.75	5	3.75	0.8
NA420LJ	2.5	8	20	3.12
NO210LJ	1	6	6	0.72
NO220LJ	1.5	1	1.5	0.23
TOTALS		26	40.25	6.85

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S137LJ C,B,A,GLZ,G2Z,G1,Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7;

S137LJ
3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

D3030, APRIL 1988

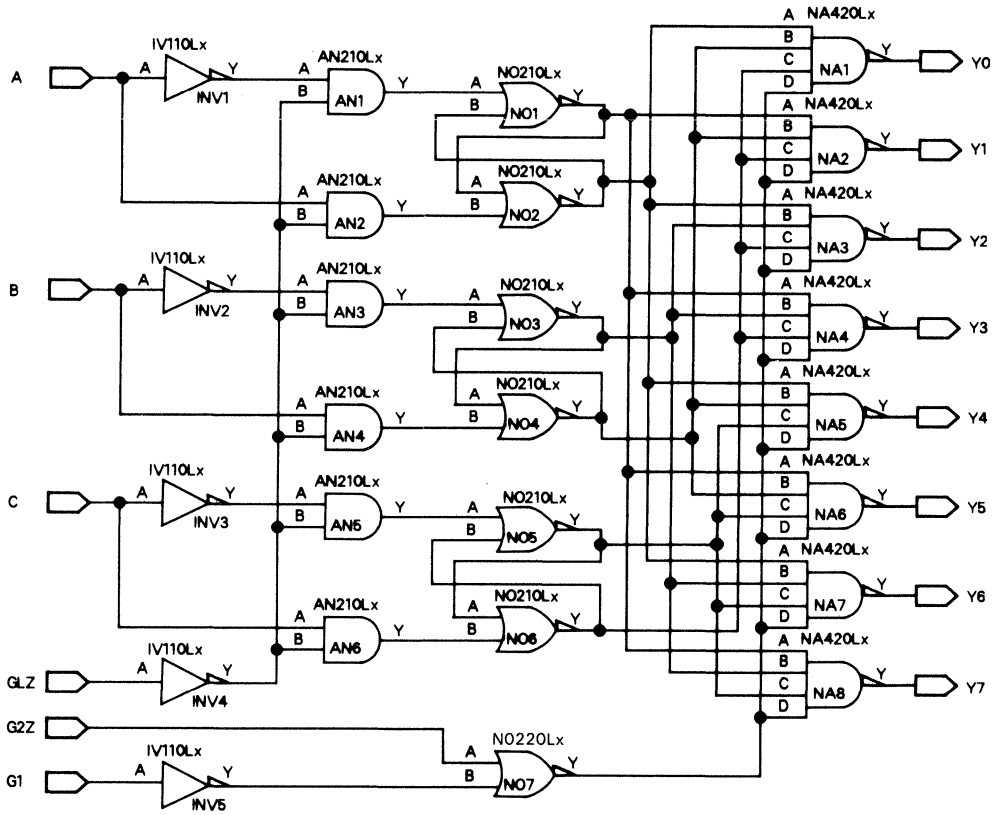
FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
GLZ	G1	G2Z	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address = L All others = H							

S137LJ
3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

D3030, APRIL 1988

logic diagram



S137LJ
3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A, B, C		0.1		pF
		GLZ, G1Z, G2Z		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	6.85		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (See Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A, B, C, GLZ	Any		2.9	6.2		2.9	5.9	ns
t_{PHL}				4.9	10.6		4.9	9.9	
t_{PLH}	G1 or G2Z	Any		2.4	5.1		2.4	4.7	ns
t_{PHL}				3.7	8		3.7	7.3	
Δt_{PLH}	Any	Any	0.22	0.68	1.46	0.24	0.68	1.34	ns/pF
Δt_{PHL}			0.26	0.78	1.82	0.28	0.78	1.62	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE†

```
BLOCK S137LJ;
C       @INPUT;
B       @INPUT;
A       @INPUT;
GLZ     @INPUT;
G2Z     @INPUT;
G1      @INPUT;
Y0      @OUTPUT;
Y1      @OUTPUT;
Y2      @OUTPUT;
Y3      @OUTPUT;
Y4      @OUTPUT;
Y5      @OUTPUT;
Y6      @OUTPUT;
Y7      @OUTPUT;

STRUCTURE
AN1     :AN210LJ  AN,GLP,LIAP;
AN2     :AN210LJ  A,GLP,LIAN;
AN3     :AN210LJ  BN,GLP,LIBP;
AN4     :AN210LJ  B,GLP,LIBN;
AN5     :AN210LJ  CN,GLP,LICP;
AN6     :AN210LJ  C,GLP,LICN;
INV1    :IV110LJ  A,AN;
INV2    :IV110LJ  B,BN;
INV3    :IV110LJ  C,CN;
INV4    :IV110LJ  GLZ,GLP;
INV5    :IV110LJ  G1,IV5O;
NA1     :NA420LJ  LOAN,LOBN,LOCN,OC,Y0;
NA2     :NA420LJ  LOAP,LOBN,LOCN,OC,Y1;
NA3     :NA420LJ  LOAN,LOBP,LOCN,OC,Y2;
NA4     :NA420LJ  LOAP,LOBP,LOCN,OC,Y3;
NA5     :NA420LJ  LOAN,LOBN,LOCP,OC,Y4;
NA6     :NA420LJ  LOAP,LOBN,LOCP,OC,Y5;
NA7     :NA420LJ  LOAN,LOBP,LOCP,OC,Y6;
NA8     :NA420LJ  LOAP,LOBP,LOCP,OC,Y7;
NO1     :NO210LJ  LIAP,LOAN,LOAP;
NO2     :NO210LJ  LOAP,LIAN,LOAN;
NO3     :NO210LJ  LIBP,LOBN,LOBP;
NO4     :NO210LJ  LOBP,LIBN,LOBN;
NO5     :NO210LJ  LICP,LOCN,LOCP;
NO6     :NO210LJ  LOCP,LICN,LOCN;
NO7     :NO220LJ  G2Z,IV5O,OC;
END S137LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

S138LJ
3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

D3030, APRIL 1988

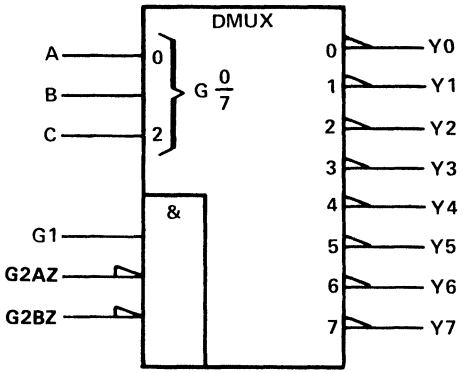
SOFTWARE MACRO

- **Three Enable Inputs for Expandability**
- **Choice of an Active-High or Two Active-Low Enables**
- **Parallel Decoders for Multiple Bit Words**

description

The S138LJ software macro implements a 3-line to 8-line decoder/demultiplexer. Also provided in the macro are strobe inputs, G1, G2AZ, and G2BZ, which enable and disable the outputs. All of the outputs are high when disabled. They are enabled when G1 is high and both G2AZ and G2BZ are low. This condition enables the selected output and it goes to a low logic level. These enables also permit the S138LJ to be cascaded to accommodate wider multiplexers, because only the enabled 8-bit field will contain an active data bit. The S138LJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV110LJ	0.75	1	0.75	0.16
IV120LJ	1	6	6	1.86
NA420LJ	2.5	8	20	3.12
NO330LJ	2.75	1	2.75	0.35
TOTALS		16	29.5	5.49

When the decoder/demultiplexer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

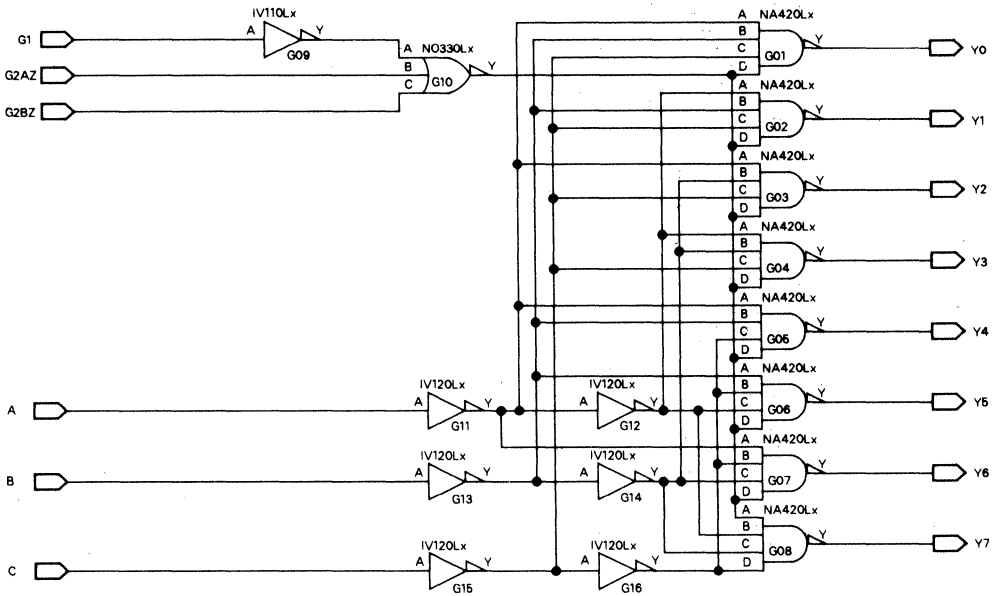
Label: S138LJ G1,G2AZ,G2BZ,A,B,C,Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7;

D3030, APRIL 1988

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	G2AZ	G2BZ	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

logic diagram



Lx = LH for 2-μm standard cells.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A, B, C		0.11		pF
		G2AZ, G2BZ		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	5.49		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A, B, C	Any		1.1	2.9		1.1	2.6	ns
t_{PHL}				1.6	2.9		1.6	2.6	
t_{PLH}	G1, G2AZ, or G2BZ	Any		1.6	3.5		1.6	3.2	ns
t_{PHL}				2.3	5.4		2.3	5	
Δt_{PLH}	Any	Any	0.22	0.63	1.46	0.24	0.63	1.34	ns/pF
Δt_{PHL}			0.26	0.77	1.82	0.28	0.77	1.62	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for a gate array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

D3030, APRIL 1988

HDL FILE†

```
BLOCK S138LJ;                    STRUCTURE
G1          @INPUT;              G01     :NA420LJ  G11O,G13O,G15O,G10O,Y0;
G2AZ        @INPUT;              G02     :NA420LJ  G12O,G13O,G15O,G10O,Y1;
G2BZ        @INPUT;              G03     :NA420LJ  G11O,G14O,G15O,G10O,Y2;
A           @INPUT;              G04     :NA420LJ  G12O,G14O,G15O,G10O,Y3;
B           @INPUT;              G05     :NA420LJ  G11O,G13O,G16O,G10O,Y4;
C           @INPUT;              G86     :NA420LJ  G13O,G16O,G12O,G10O,Y5;
Y0          @OUTPUT;             G07     :NA420LJ  G11O,G16O,G14O,G10O,Y6;
Y1          @OUTPUT;             G08     :NA420LJ  G10O,G12O,G14O,G16O,Y7;
Y2          @OUTPUT;             G09     :IV110LJ  G1,G09O;
Y3          @OUTPUT;             G10     :NO330LJ  G09O,G2AZ,G2BZ,G10O;
Y4          @OUTPUT;             G11     :IV120LJ  A,G11O;
Y5          @OUTPUT;             G12     :IV120LJ  G11O,G12O;
Y6          @OUTPUT;             G13     :IV120LJ  B,G13O;
Y7          @OUTPUT;             G14     :IV120LJ  G13O,G14O;
                                 G15     :IV120LJ  C,G15O;
                                 G16     :IV120LJ  G15O,G16O;
                                 END S138LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

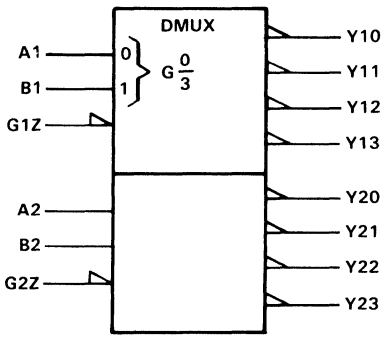
S139LJ
DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

D3030, APRIL 1988

SOFTWARE MACRO

- **Enable Input Permits Expansion of Each Decoder**
- **Parallel Decoders for Multiple Bit Words**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S139LJ software macro implements a dual 2-line to 4-line decoder/demultiplexer. Also provided in the macro are two strobe inputs G1Z and G2Z that enable and disable the outputs. The four outputs of a decoder are high when its corresponding strobe is high. When the strobe is low, the selected output is low. These strobes, G1Z for decoder 1 and G2Z for decoder 2, permit the S139LJ decoders to be cascaded to accommodate wider multiplexers, since only the enabled 4-bit field will contain an active-low data bit. The S139LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV110LJ	0.75	8	6	1.28
IV120LJ	1	2	2	0.62
NA320LJ	2	8	16	2.96
TOTALS		18	24	4.86

When the decoder/demultiplexer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

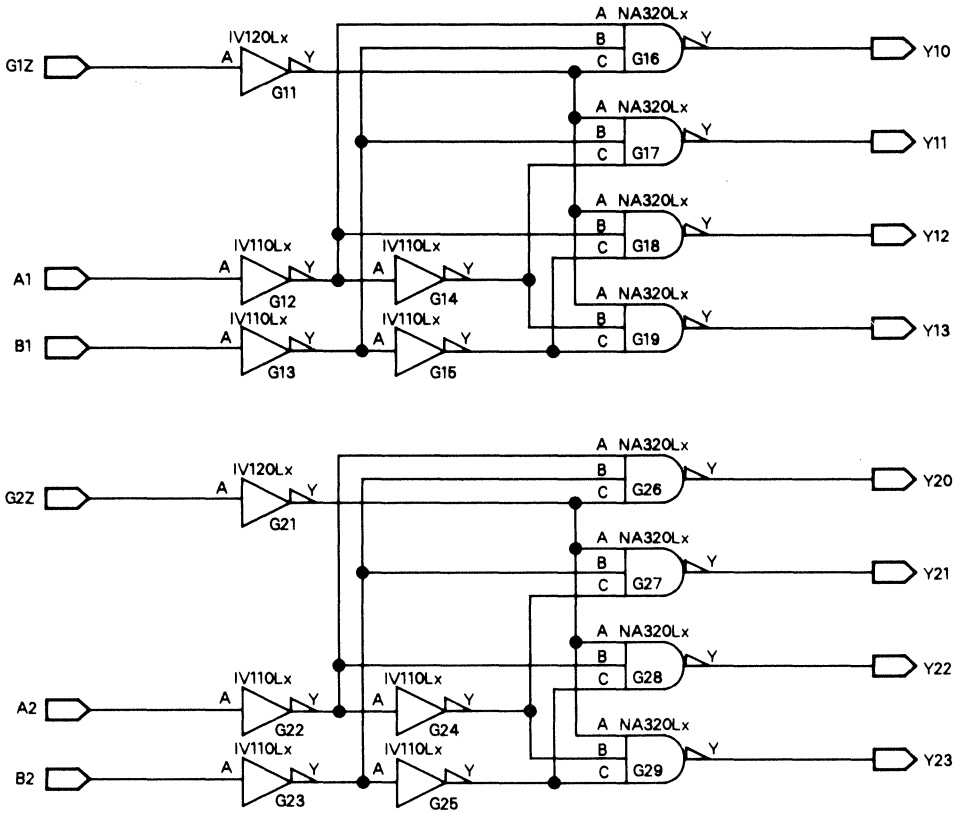
Label: S139LJ A1,B1,G1Z,A2,B2,G2Z,Y10,Y11,Y12,Y13,Y20,Y21,Y22,Y23;

D3030, APRIL 1988

FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
GnZ	Bn	An	Yn0	Yn1	Yn2	Yn3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	An, Bn		0.05		pF
		GnZ		0.11		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	4.9		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	An or Bn	Any		1.7	3		1.7	2.9	ns
t_{PHL}				1.7	3		1.7	2.8	
t_{PLH}	GnZ	Any		0.8	1.4		0.8	1.4	ns
t_{PHL}				0.9	1.7		0.9	1.5	
Δt_{PLH}	Any	Any	0.22	0.58	1.24	0.24	0.58	1.14	ns/pF
Δt_{PHL}			0.26	0.62	1.42	0.26	0.62	1.28	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

D3030, APRIL 1988

HDL FILE†

```
BLOCK S139LJ;
A1          @INPUT;
B1          @INPUT;
G1Z         @INPUT;
A2          @INPUT;
B2          @INPUT;
G2Z         @INPUT;
Y10         @OUTPUT;
Y11         @OUTPUT;
Y12         @OUTPUT;
Y13         @OUTPUT;
Y20         @OUTPUT;
Y21         @OUTPUT;
Y22         @OUTPUT;
Y23         @OUTPUT;
STRUCTURE
G11         :IV120LJ    G1Z,G11O;
G12         :IV110LJ    A1,G12O;
G13         :IV110LJ    B1,G13O;
G14         :IV110LJ    G12O,G14O;
G15         :IV110LJ    G13O,G15O;
G16         :NA320LJ    G12O,G13O,G11O,Y10;
G17         :NA320LJ    G11O,G13O,G14O,Y11;
G18         :NA320LJ    G11O,G12O,G15O,Y12;
G19         :NA320LJ    G11O,G14O,G15O,Y13;
G21         :IV120LJ    G2Z,G21O;
G22         :IV110LJ    A2,G22O;
G23         :IV110LJ    B2,G23O;
G24         :IV110LJ    G22O,G24O;
G25         :IV110LJ    G23O,G25O;
G26         :NA320LJ    G22O,G23O,G21O,Y20;
G27         :NA320LJ    G21O,G23O,G24O,Y21;
G28         :NA320LJ    G21O,G22O,G25O,Y22;
G29         :NA320LJ    G21O,G24O,G25O,Y23;
END S139LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

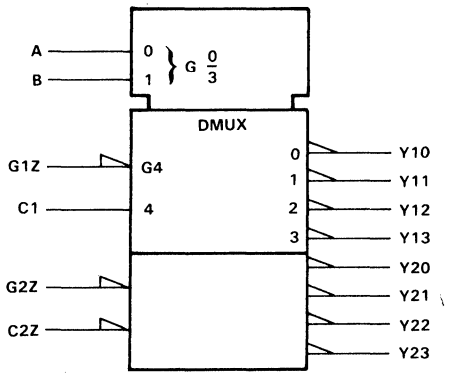
S155LJ
DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER WITH DATA AND ENABLE LINES

D3030, APRIL 1988

SOFTWARE MACRO

- **Enable Input Permits Expansion of Each Decoder**
- **Individual Data Input to Each 4-Line Decoder**
- **Parallel Decoders for Multiple Bit Words**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S155LJ software macro implements an 8-line or dual 4-line decoder/demultiplexer. The A and B inputs are common to the two sections of the macro and select one of the four outputs in each section. Each section has a C input ANDed with a G input and for 4-line demultiplexer applications, a choice can be made in the use of these inputs as strobe and data inputs. In section 1, when C1 is high, the selected output assumes the level of G1Z, or to view this another way, when G1Z is low the selected output assumes the complement of the level of C1. In section 2, C2Z and G2Z are interchangeable. When both are low, the selected output is low. When one of them is high, all outputs are high. When a 3-line to 8-line decoder or a 1-line to 8-line demultiplexer is required, C1 and C2Z are connected together to act as a third select line (Cn) with lines A and B. G1Z and G2Z are also connected together to act as an active-low strobe or data line for this application. The S155LJ is implemented with standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV110LJ	0.75	1	0.75	0.16
IV120LJ	1	4	4	1.24
NA320LJ	2	8	16	2.96
NO220LJ	1.5	2	3	0.46
TOTALS		15	23.75	4.82

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S155LJ C1,G1Z,C2Z,G2Z,A,B,Y10,Y11,Y12,Y13,Y20,Y21,Y22,Y23;

FUNCTION TABLE
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	G1Z	C1	Y10	Y11	Y12	Y13
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	G2Z	C2Z	Y20	Y21	Y22	Y23
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

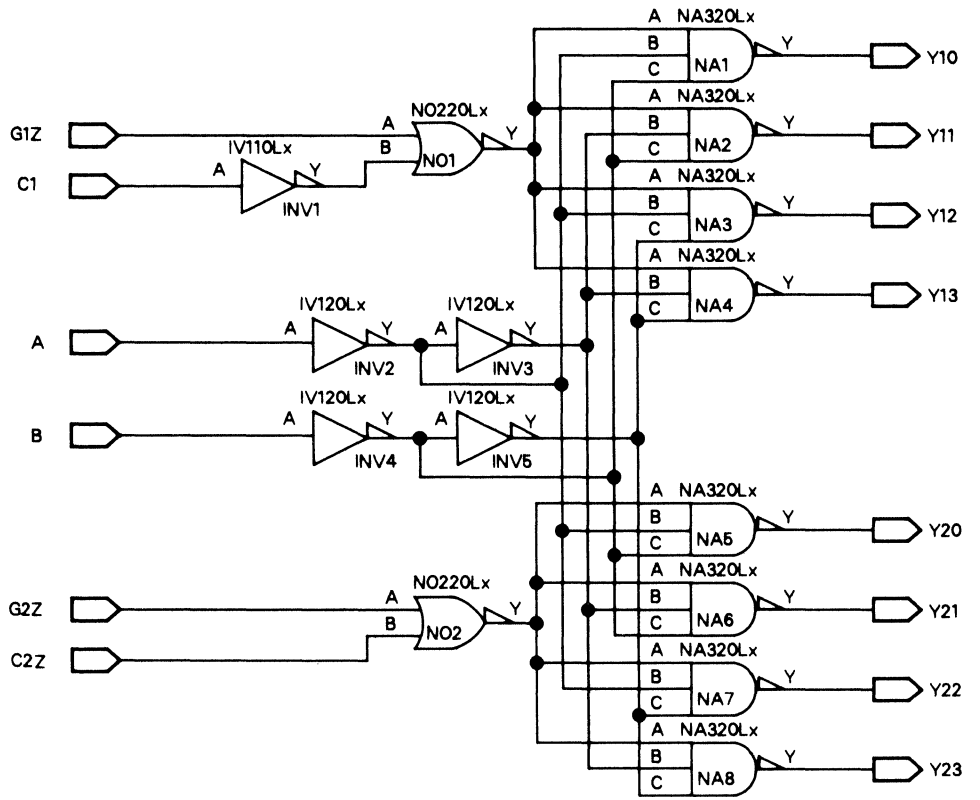
INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
Cn†	B	A	GnZ‡	Y20	Y21	Y22	Y23	Y10	Y11	Y12	Y13
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

† C = inputs C1 and C2Z connected together
‡ G = inputs G1Z and G2Z connected together

S155LJ
DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER WITH DATA AND ENABLE LINES

D3030, APRIL 1988

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLRZ		0.11		pF
		PREZ		0.05		
		D		0.11		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	4.9		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (See Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B	Any		0.9	1.5		0.9	1.4	ns
t_{PHL}				1.5	2.7		1.5	2.4	
t_{PLH}	G1Z or C1	Y1n		1.1	2.7		1.1	2.5	ns
t_{PHL}				1.5	3.5		1.5	3.3	
t_{PLH}	G2Z or C2Z	Y2n		1.1	2.7		1.1	2.5	ns
t_{PHL}				1.5	3.5		1.5	3.3	
Δt_{PLH}	Any	Any	0.22	0.58	1.24	0.24	0.58	1.14	ns/pF
Δt_{PHL}			0.26	0.62	1.42	0.26	0.62	1.28	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for a gate array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

S155LJ
DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER WITH DATA AND ENABLE LINES

D3030, APRIL 1988

HDL FILE†

```
BLOCK S155LJ;
C1      @INPUT;
G2Z     @INPUT;
A       @INPUT;
B       @INPUT;
Y10     @OUTPUT;
Y11     @OUTPUT;
Y12     @OUTPUT;
Y13     @OUTPUT;
Y20     @OUTPUT;
Y21     @OUTPUT;
Y22     @OUTPUT;
Y23     @OUTPUT;
STRUCTURE
INV1    :IV110LJ  C1,INV1O;
INV2    :IV120LJ  A,INV2O;
INV3    :IV120LJ  INV2O,INV3O;
INV4    :IV120LJ  B,INV4O;
INV5    :IV120LJ  INV4O,INV5O;
NA1     :NA320LJ  NO1O,INV2O,INV4O,Y10;
NA2     :NA320LJ  NO1O,INV3O,INV4O,Y11;
NA3     :NA320LJ  NO1O,INV2O,INV5O,Y12;
NA4     :NA320LJ  NO1O,INV3O,INV5O,Y13;
NA5     :NA320LJ  NO2O,INV2O,INV4O,Y20;
NA6     :NA320LJ  NO2O,INV3O,INV4O,Y21;
NA7     :NA320LJ  NO2O,INV2O,INV5O,Y22;
NA8     :NA320LJ  NO2O,INV3O,INV5O,Y23;
NO1     :NO220LJ  G1Z,INV1O,NO1O;
NO2     :NO220LJ  G2Z,C2Z,NO2O;
END S155LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

17 Multiplexers

MULTIPLEXERS
FUNCTIONAL INDEX

D3030, APRIL 1988

MULTIPLEXERS (HARDWIRED)

DESCRIPTION	CELL NAME	OUTPUT DRIVE	COMMENTS	EQUIVALENT NA210s	PAGE
2-to-1 with 3-State Output	MU110LJ	1X	Active L enable	3.5	17-3
2-to-1	MU111LJ	1X		2.25	17-5
4-to-1	MU210LJ	1X		5	17-6
8-to-1 with 3-State Output	MU310LJ	1X	Active L enable	14.75	17-7
8-to-1	MU320LJ	2X		11.25	17-9

MULTIPLEXERS (SOFTWARE)

DESCRIPTION	MACRO NAME	OUTPUT DRIVE	COMMENTS	EQUIVALENT NA210s	PAGE
8-to-1 with Complementary Outputs	S151LJ	1X	Active L enable	35	17-11
Dual 4-to-1	S153LJ	1X	Separate active L enables	21.5	17-15
Quad 2-to-1 Noninverting	S157LJ	1X	Active L enable	17	17-19
Quad 2-to-1 Inverting	S158LJ	1X	Active L enable	20	17-23
8-to-1 3-State Complementary Outputs	S251LJ	1X	Active L enable	24.5	17-27
Quad 2-to-1 Noninverting 3-State Outputs	S257ALJ	1X	Active L enable	21	17-31
Quad 2-to-1 Inverting 3-State Outputs	S258ALJ	1X	Active L enable	15	17-35
Quad 2-to-1 Storage	S298LJ	1X	Negative edge-triggered register	37	17-39
Quad 2-to-1 Storage, Complementary Outputs	S398LJ	1X	Positive edge-triggered register	39	17-43
Quad 2-to-1 Storage	S399LJ	1X	Positive edge-triggered register	36	17-47

MU110LJ
2-LINE TO 1-LINE MULTIPLEXER WITH 3-STATE OUTPUT

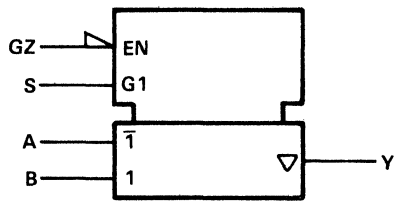
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
S	GZ	Y
X	H	Z
L	L	A
H	L	B

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The MU110LJ cell is an internal 2-line to 1-line multiplexer that interfaces directly with internal three-state bus lines. When the multiplexer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: MU110LJ A,B,S,GZ,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A		0.08		pF
		S		0.09		
		GZ		0.1		
C_o	Output capacitance			0.06		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.38		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B	Y	$R_L = \infty$	0.23	0.7	1.62	0.23	0.7	1.49	ns
t_{PHL}				0.23	0.6	1.32	0.26	0.6	1.2	
t_{PLH}	S	Y		0.32	0.94	2.04	0.37	0.94	1.88	ns
t_{PHL}				0.37	0.87	1.79	0.37	0.87	1.66	
t_{PZH}	GZ	Y	R_L = 40 kΩ to GND	0.07	0.18	0.33	0.06	0.18	0.32	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.2	0.39	0.69	0.19	0.39	0.64	
t_{PHZ}	GZ	Y	R_L = 40 kΩ to GND		3.51			3.51		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		2.1			2.1		
Δt_{PLH}	A or B	Y		0.7	2	4.36	0.74	2	4	ns/pF
Δt_{PHL}				0.36	0.86	1.88	0.36	0.86	1.7	
Δt_{PLH}	S	Y		0.7	2	4.34	0.74	2	4	ns/pF
Δt_{PHL}				0.32	0.86	1.9	0.36	0.86	1.7	
Δt_{PZH}	GZ	Y		0.74	2.04	4.6	0.78	2.04	4.2	ns/pF
Δt_{PZL}				0.24	0.86	2.3	0.28	0.86	2.08	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

MU111LJ
2-LINE TO 1-LINE MULTIPLEXER

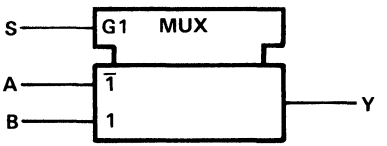
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUT S	OUTPUT Y
L	A
H	B

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The MU111LJ cell is an internal 2-line to 1-line multiplexer. When the multiplexer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: MU111LJ A,B,S,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A, B		0.05		pF
		S		0.11		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.41		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	0.27	0.65	1.37	0.29	0.65	1.23	ns
t_{PHL}			0.27	0.77	1.82	0.28	0.77	1.67	
t_{PLH}	S	Y	0.26	0.62	1.22	0.28	0.62	1.12	ns
t_{PHL}			0.27	0.63	1.33	0.28	0.63	1.25	
Δt_{PLH}	A or B	Y	0.42	1.07	2.26	0.44	1.07	2.1	ns/pF
Δt_{PHL}			0.3	0.65	1.34	0.32	0.65	1.2	
Δt_{PLH}	S	Y	0.42	1.08	2.26	0.44	1.08	2.08	ns/pF
Δt_{PHL}			0.3	0.66	1.34	0.32	0.66	1.18	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

MU210LJ
4-LINE TO 1-LINE MULTIPLEXER

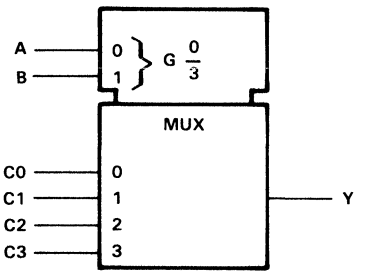
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS		OUTPUT
B	A	Y
L	L	C0
L	H	C1
H	L	C2
H	H	C3

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The MU210LJ cell is an internal 4-line to 1-line multiplexer. When the multiplexer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: MU210LJ C0,C1,C2,C3,A,B,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A, B		0.13		pF
		Any C		0.08		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.52		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A, B	Y	0.15	0.71	2.02	0.17	0.71	1.86	ns
t_{PHL}			0.27	0.87	2.46	0.28	0.87	2.28	
t_{PLH}	Any C	Y	0.29	0.73	1.56	0.31	0.73	1.43	ns
t_{PHL}			0.33	0.83	1.84	0.34	0.83	1.7	
Δt_{PLH}	A, B	Y	0.42	1.08	2.26	0.44	1.08	2.08	ns/pF
Δt_{PHL}			0.28	0.65	1.36	0.3	0.65	1.22	
Δt_{PLH}	Any C	Y	0.4	1.07	2.28	0.44	1.07	2.08	ns/pF
Δt_{PHL}			0.28	0.67	1.38	0.32	0.67	1.24	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

MU310LJ
8-LINE TO 1-LINE MULTIPLEXER WITH 3-STATE OUTPUT

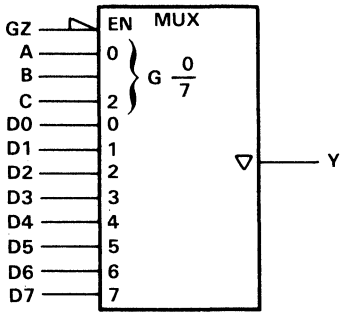
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS				OUTPUT
C	B	A	GZ	Y
X	X	X	H	Z
L	L	L	L	D0
L	L	H	L	D1
L	H	L	L	D2
L	H	H	L	D3
H	L	L	L	D4
H	L	H	L	D5
H	H	L	L	D6
H	H	H	L	D7

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The MU310LJ cell is an internal 8-line to 1-line multiplexer that interfaces directly with internal three-state bus lines. When the multiplexer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: MU310LJ D0,D1,D2,D3,D4,D5,D6,D7,A,B,C,GZ,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	D0 thru D7		0.08		pF
		A or C		0.12		
		B		0.06		
		GZ		0.1		
C_o	Output capacitance			0.07		pF
C_{pd}	dissipation capacitance		$t_r = t_f$ = 1 ns	0.66		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	D0 thru D7	Y	$R_L = \infty$	0.44	1.13	2.54	0.46	1.13	2.31	ns
t_{PHL}				0.43	1.26	3	0.45	1.26	2.74	
t_{PLH}	A, B, or C	Y		0.19	1.15	3.45	0.21	1.15	3.16	ns
t_{PHL}				0.31	1.3	3.99	0.33	1.3	3.63	
t_{PZH}	GZ	Y	R_L = 40 kΩ to GND	0.03	0.23	0.6	0.04	0.23	0.55	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.2	0.37	0.72	0.21	0.37	0.67	
t_{PHZ}	GZ	Y	R_L = 40 kΩ to GND		3.86			3.86		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		2.2			2.2		
Δt_{PLH}	D0 thru D7	Y		0.7	2.06	4.48	0.76	2.06	4.12	ns/pF
Δt_{PHL}				0.4	1.08	2.4	0.42	1.08	2.18	
Δt_{PLH}	A, B, or C	Y		0.72	2.06	4.48	0.76	2.06	4.12	ns/pF
Δt_{PHL}				0.4	1.07	2.38	0.42	1.07	2.16	
Δt_{PZH}	GZ	Y		0.74	2.12	4.72	0.78	2.12	4.32	ns/pF
Δt_{PZL}				0.26	0.96	2.46	0.28	0.96	2.22	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

MU320LJ
8-LINE TO 1-LINE MULTIPLEXER WITH 2X OUTPUT

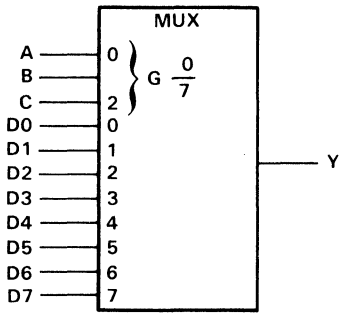
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUT
C	B	A	Y
X	X	X	L
L	L	L	D0
L	L	H	D1
L	H	L	D2
L	H	H	D3
H	L	L	D4
H	L	H	D5
H	H	L	D6
H	H	H	D7

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The MU320LJ cell is an internal 8-line to 1-line multiplexer with a 2X output to enhance capacitive drive capability and fanout. When the multiplexer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: MU320LJ D0,D1,D2,D3,D4,D5,D6,D7,A,B,C,Y;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	D0 thru D7		0.05		pF
		A, B, or C		0.11		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.28		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	D0 thru D7	Y	$R_L = \infty$	0.53	1.62	3.9	0.56	1.62	3.54	ns
t_{PHL}				0.57	1.89	4.71	0.61	1.89	4.29	
t_{PLH}	A, B, or C	Y		0.25	1.42	5.03	0.28	1.42	4.59	ns
t_{PHL}				0.33	1.61	5.74	0.35	1.61	5.24	
Δt_{PLH}	D0 thru D7	Y		0.2	0.55	1.18	0.2	0.55	1.1	ns/pF
Δt_{PHL}				0.14	0.44	0.92	0.16	0.44	0.84	
Δt_{PLH}	A, B, or C	Y		0.18	0.55	1.18	0.2	0.55	1.08	ns/pF
Δt_{PHL}				0.16	0.44	0.92	0.16	0.44	0.84	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S151LJ
8-LINE TO 1-LINE MULTIPLEXER

D3030, APRIL 1988

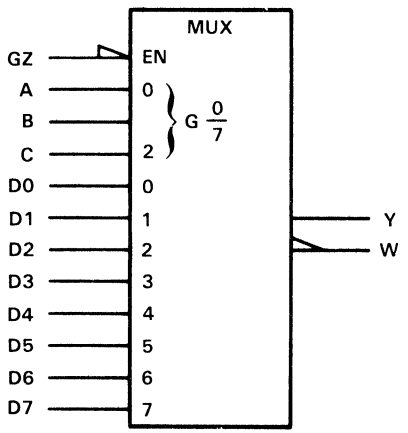
SOFTWARE MACRO

- **Active-Low Strobe for Expandability**
- **Use Parallel Multiplexers for Multiple-Bit Words**

description

The S151LJ software macro implements an 8-line to 1-line multiplexer. The macro has a strobe input, GZ, that enables and disables the inputs. The Y output is low and the W output is high when GZ is high. When GZ is low, the Y output assumes the level of the selected input and the W output assumes the complement of that level. This strobe permits the macro to be employed for designing wider multiplexers, since only the enabled 8-bit field will output an active data bit. The S151LJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV110LJ	0.75	3	2.25	0.48
IV120LJ	1	5	5	1.55
NA510LJ	3	8	24	7.04
NA810LJ	3.75	1	3.75	0.91
TOTALS		17	35	9.98

When the multiplexer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

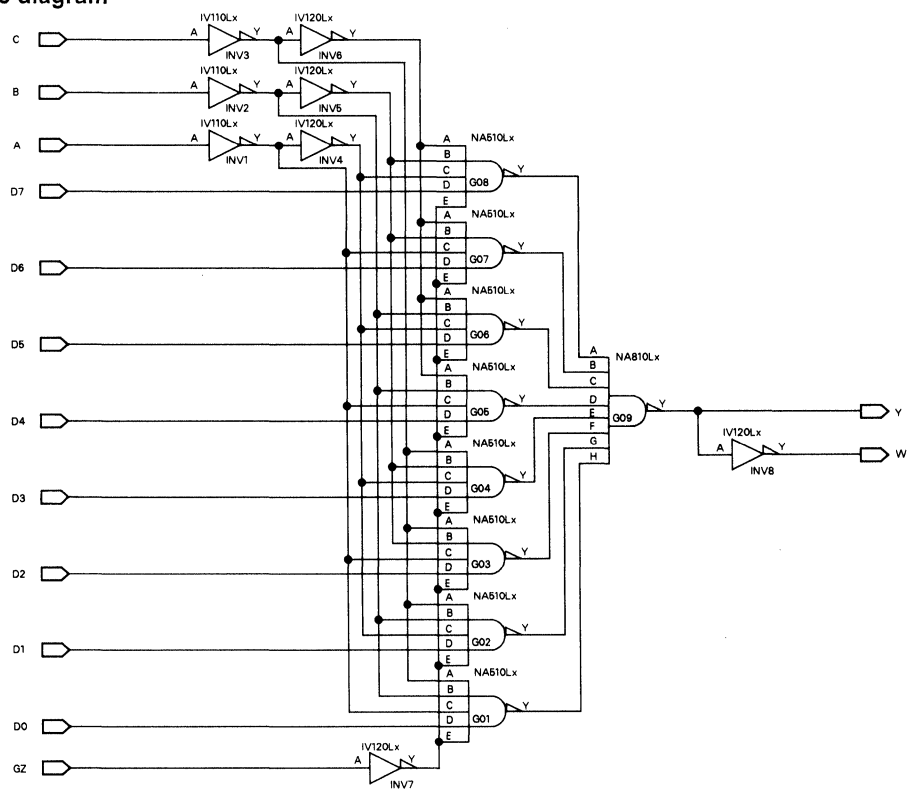
Label: S151LJ GZ,A,B,C,D0,D1,D2,D3,D4,D5,D6,D7,Y,W;

FUNCTION TABLE

INPUTS				OUTPUTS	
C	B	A	GZ	Y	W
X	X	X	H	L	H
L	L	L	L	D0	D0
L	L	H	L	D1	D1
L	H	L	L	D2	D2
L	H	H	L	D3	D3
H	L	L	L	D4	D4
H	L	H	L	D5	D5
H	H	L	L	D6	D6
H	H	H	L	D7	D7

D0, D1...D7 = the level of the respective D input.

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	GZ		0.11		pF
		All other inputs		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	10		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A, B, or C	Y		2.9	6.3		2.9	5.7	ns
t_{PHL}				2.9	5.8		2.9	5.4	
t_{PLH}		W		3.1	6.1		3.1	5.7	ns
t_{PHL}				3.1	6.7		3.1	6.1	
t_{PLH}	Any D	Y		2	4.3		2	3.9	ns
t_{PHL}				2.1	4.7		2.1	4.3	
t_{PLH}		W		2.3	5		2.3	4.6	ns
t_{PHL}				2.2	4.7		2.2	4.3	
t_{PLH}	GZ	Y		2.6	5.5		2.6	5.1	ns
t_{PHL}				2.7	5.7		2.7	5.1	
t_{PLH}		W		2.9	6		2.9	5.4	ns
t_{PHL}				2.8	5.9		2.8	5.5	
Δt_{PLH}	Any	Y	0.34	0.92	1.92	0.36	0.92	1.76	ns/pF
Δt_{PHL}			0.24	0.56	1.14	0.26	0.56	1.02	
Δt_{PLH}	Any	W	0.24	0.52	1.1	0.26	0.52	1	ns/pF
Δt_{PHL}			0.28	0.42	0.68	0.28	0.42	0.62	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

D3030, APRIL 1988

HDL FILE†

```
BLOCK S151LJ;
GZ          @INPUT;
A           @INPUT;
B           @INPUT;
C           @INPUT;
D0          @INPUT;
D1          @INPUT;
D2          @INPUT;
D3          @INPUT;
D4          @INPUT;
D5          @INPUT;
D6          @INPUT;
D7          @INPUT;
Y           @OUTPUT;
W           @OUTPUT;
STRUCTURE
G01         :NA510LJ    CZ,BZ,AZ,D0,INV7O,U0;
G02         :NA510LJ    CZ,BZ,AT,D1,INV7O,U1;
G03         :NA510LJ    CZ,BT,AZ,D2,INV7O,U2;
G04         :NA510LJ    CZ,BT,AT,D3,INV7O,U3;
G05         :NA510LJ    CT,BZ,AZ,D4,INV7O,U4;
G06         :NA510LJ    CT,BZ,AT,D5,INV7O,U5;
G07         :NA510LJ    CT,BT,AZ,D6,INV7O,U6;
G08         :NA510LJ    CT,BT,AT,D7,INV7O,U7;
G09         :NA810LJ    U7,U6,U5,U4,U3,U2,U1,U0,Y;
INV1        :IV110LJ    A,AZ;
INV2        :IV110LJ    B,BZ;
INV3        :IV110LJ    C,CZ;
INV4        :IV120LJ    AZ,AT;
INV5        :IV120LJ    BZ,BT;
INV6        :IV120LJ    CZ,CT;
INV7        :IV120LJ    GZ,INV7O;
INV8        :IV120LJ    Y,W;
END S151LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S153LJ
DUAL 4-LINE TO 1-LINE MULTIPLEXER

D3030, APRIL 1988

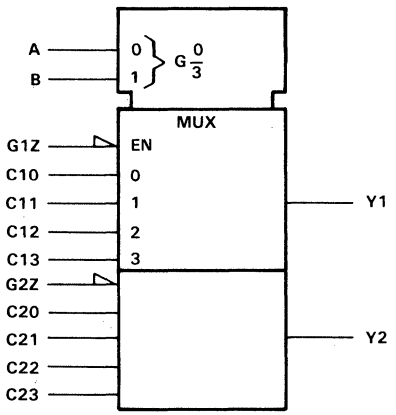
SOFTWARE MACRO

- **Active-Low Strobe for Expandability**
- **Use Parallel Multiplexers for Multiple-Bit Words**

description

The S153LJ software macro implements a dual 4-line to 1-line multiplexer. Each 4-bit half of the macro has a strobe input that enables and disables its associated outputs. The Yn output is low when GnZ is high. When GnZ is low, the output assumes the level of the selected input. These strobes permit the macro to be employed for designing wider multiplexers, since only the enabled 4-bit field will output an active data bit. The S153LJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV110LJ	0.75	6	4.5	0.96
NA410LJ	1.5	8	12	1.52
NA420LJ	2.5	2	5	0.78
TOTALS		16	21.5	3.26

When the multiplexer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

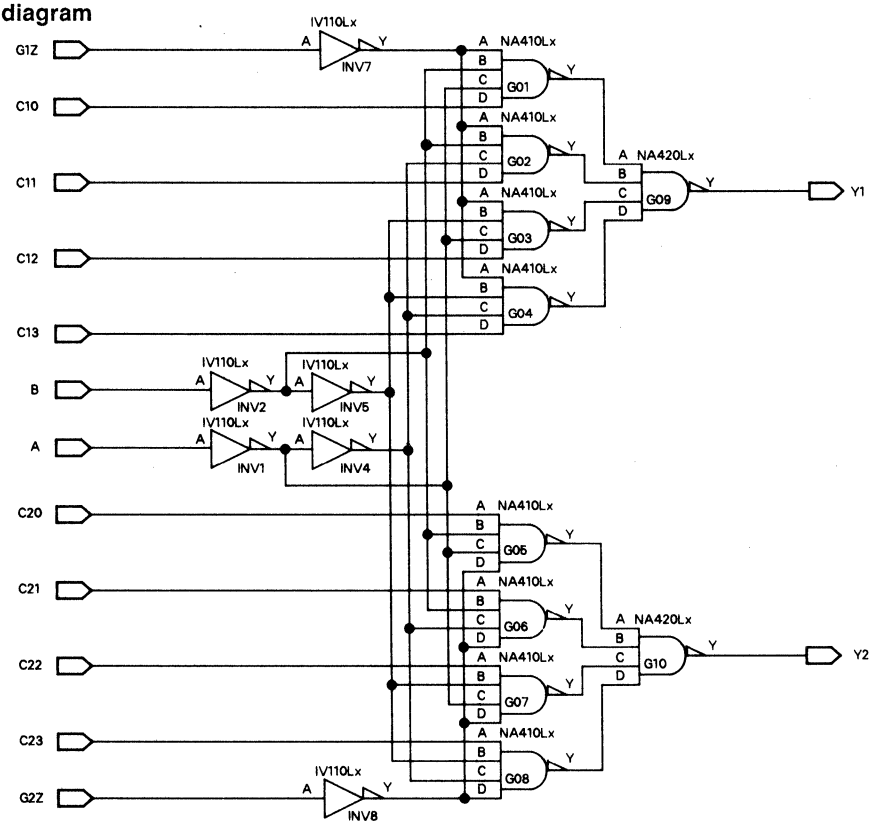
Label: S153LJ G1Z,G2Z,A,B,C10,C11,C12,C13,C20,C21,C22,C23,Y1,Y2;

D3030, APRIL 1988

FUNCTION TABLE

INPUTS						STROBE GnZ	OUTPUT Y
SELECT		DATA					
B	A	Cn0	Cn1	Cn2	Cn3		
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S153LJ
DUAL 4-LINE TO 1-LINE MULTIPLEXER

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage		2.2		V
C_i	Input capacitance		0.05		pF
C_{pd}	Equivalent power dissipation capacitance	$t_r = t_f$ = 1 ns	3.3		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B	Y		2.7	5.2		2.7	4.8	ns
t_{PHL}				1.9	5.4		1.9	3.6	
t_{PLH}	Any C	Y		1.3	2.7		1.3	2.5	ns
t_{PHL}				1.2	2.6		1.2	2.5	
t_{PLH}	G1Z or G2Z	Y		2	4.1		2	3.8	ns
t_{PHL}				1.8	3.7		1.8	3.5	
Δt_{PLH}	Any	Y	0.22	0.68	1.46	0.24	0.68	1.34	ns/pF
Δt_{PHL}			0.26	0.78	1.82	0.28	0.78	1.62	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

D3030, APRIL 1988

HDL FILE†

```
BLOCK S153LJ;                    STRUCTURE
G1Z       @INPUT;                G01     :NA410LJ   STB1Z,BZ,AZ,C10,U10;
G2Z       @INPUT;                G02     :NA410LJ   STB1Z,BZ,AT,C11,U11;
A         @INPUT;                G03     :NA410LJ   STB1Z,BT,AZ,C12,U12;
B         @INPUT;                G04     :NA410LJ   STB1Z,BT,AT,C13,U13;
C10       @INPUT;                G05     :NA410LJ   C20,BZ,AZ,STB2Z,U20;
C11       @INPUT;                G06     :NA410LJ   C21,BZ,AT,STB2Z,U21;
C12       @INPUT;                G07     :NA410LJ   C22,BT,AZ,STB2Z,U22;
C13       @INPUT;                G08     :NA410LJ   C23,BT,AT,STB2Z,U23;
C20       @INPUT;                G09     :NA420LJ   U10,U11,U12,U13,Y1;
C21       @INPUT;                G10     :NA420LJ   U20,U21,U22,U23,Y2;
C22       @INPUT;                INV1    :IV110LJ   A,AZ;
C23       @INPUT;                INV2    :IV110LJ   B,BZ;
Y1        @OUTPUT;               INV4    :IV110LJ   AZ,AT;
Y2        @OUTPUT;               INV5    :IV110LJ   BZ,BT;
                                 INV7    :IV110LJ   G1Z,STB1Z;
                                 INV8    :IV110LJ   G2Z,STB2Z;
                                 END S153LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S157LJ
QUADRUPLE 2-LINE TO 1-LINE NONINVERTING MULTIPLEXER

D3030, APRIL 1988

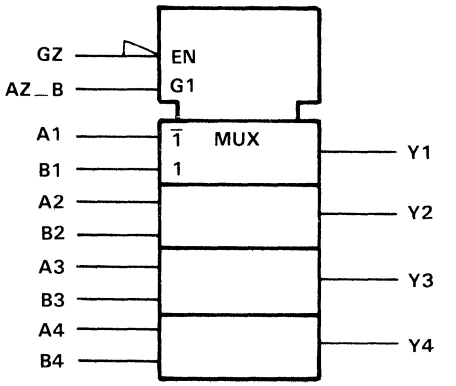
SOFTWARE MACRO

- **Active-Low Strobe for Expandability**
- **Use Parallel Multiplexers for Multiple-Bit Words**

description

The S157LJ software macro implements four 2-line to 1-line noninverting multiplexers. The macro has a strobe input, GZ, that enables and disables the outputs. The Y outputs are forced low when GZ is high. When GZ is low, the outputs assume the level of the selected inputs. This strobe permits the macro to be employed for designing wider multiplexers, since only the enabled 4-bit field will output an active data bit. The S157LJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN220LJ	1.75	2	3.5	0.94
IV110LJ	0.75	2	1.5	0.32
NA210LJ	1	12	12	2.28
TOTALS		16	17	3.54

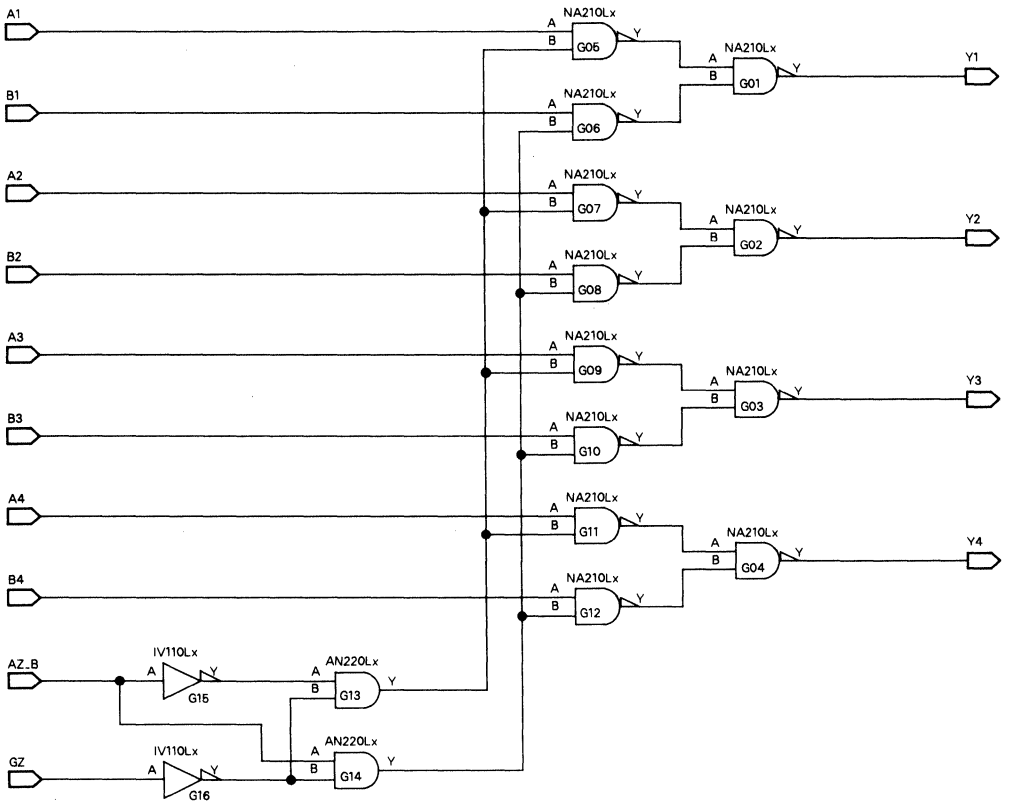
When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S157LJ A1,A2,A3,A4,B1,B2,B3,B4,AZ_B,GZ,Y1,Y2,Y3,Y4;

FUNCTION TABLE

INPUTS				OUTPUT
STROBE	SELECT	DATA		
GZ	AZ_B	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

logic diagram



S157LJ
QUADRUPLE 2-LINE TO 1-LINE NONINVERTING MULTIPLEXER

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	AZ_B		0.11		pF
		All other inputs		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	3.6		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A or B	Y		0.8	1.5		0.8	1.3	ns
t_{PHL}				0.9	1.5		0.9	1.5	
t_{PLH}	GZ or AZ_B	Y		2.2	4.2		2.2	3.9	ns
t_{PHL}				2.2	4.1		2.2	3.7	
Δt_{PLH}	Any	Y	0.38	1.26	2.66	0.4	1.26	2.46	ns/pF
Δt_{PHL}			0.4	1	2.2	0.42	1	1.98	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE†

```
BLOCK S157LJ;                    STRUCTURE
A1          @INPUT;      G01     :NA210LJ   G05O,G06O,Y1;
A2          @INPUT;      G02     :NA210LJ   G07O,G08O,Y2;
A3          @INPUT;      G03     :NA210LJ   G09O,G10O,Y3;
A4          @INPUT;      G04     :NA210LJ   G11O,G12O,Y4;
B1          @INPUT;      G05     :NA210LJ   A1,G13O,G05O;
B2          @INPUT;      G06     :NA210LJ   B1,G14O,G06O;
B3          @INPUT;      G07     :NA210LJ   A2,G13O,G07O;
B4          @INPUT;      G08     :NA210LJ   B2,G14O,G08O;
AZ__B       @INPUT;      G09     :NA210LJ   A3,G13O,G09O;
GZ          @INPUT;      G10     :NA210LJ   B3,G14O,G10O;
Y1          @OUTPUT;     G11     :NA210LJ   A4,G13O,G11O;
Y2          @OUTPUT;     G12     :NA210LJ   B4,G14O,G12O;
Y3          @OUTPUT;     G13     :AN220LJ   G15O,G16O,G13O;
Y4          @OUTPUT;     G14     :AN220LJ   AZ__B,G16O,G14O;
                         G15     :IV110LJ   AZ__B,G15O;
                         G16     :IV110LJ   GZ,G16O;
                         END S157LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

S158LJ
QUADRUPLE 2-LINE TO 1-LINE INVERTING MULTIPLEXER

D3030 APRIL 1988

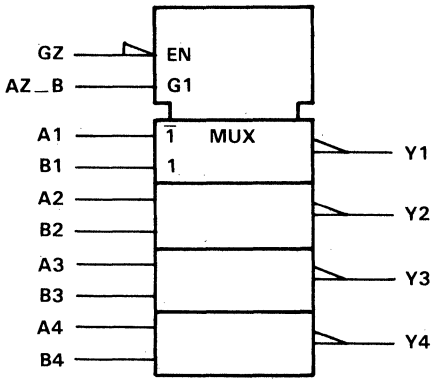
SOFTWARE MACRO

- **Active-Low Strobe for Expandability**
- **Use Parallel Multiplexers for Multiple-Bit Words**

description

The S158LJ software macro implements four 2-line to 1-line multiplexers. The macro has a strobe input, GZ, that enables and disables the outputs. The Y outputs are forced high when GZ is high. When GZ is low, the outputs assume the complement of the level of the selected bit. This strobe permits the macro to be employed for designing wider multiplexers because only the enabled 4-bit field will output an active data bit. The S158LJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN220LJ	1.75	6	10.5	2.82
IV110LJ	0.75	2	1.5	0.32
NA210LJ	1	8	8	1.52
TOTALS		16	20	4.66

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S158LJ A1,A2,A3,A4,B1,B2,B3,B4,AZ_B,GZ,Y1,Y2,Y3,Y4;

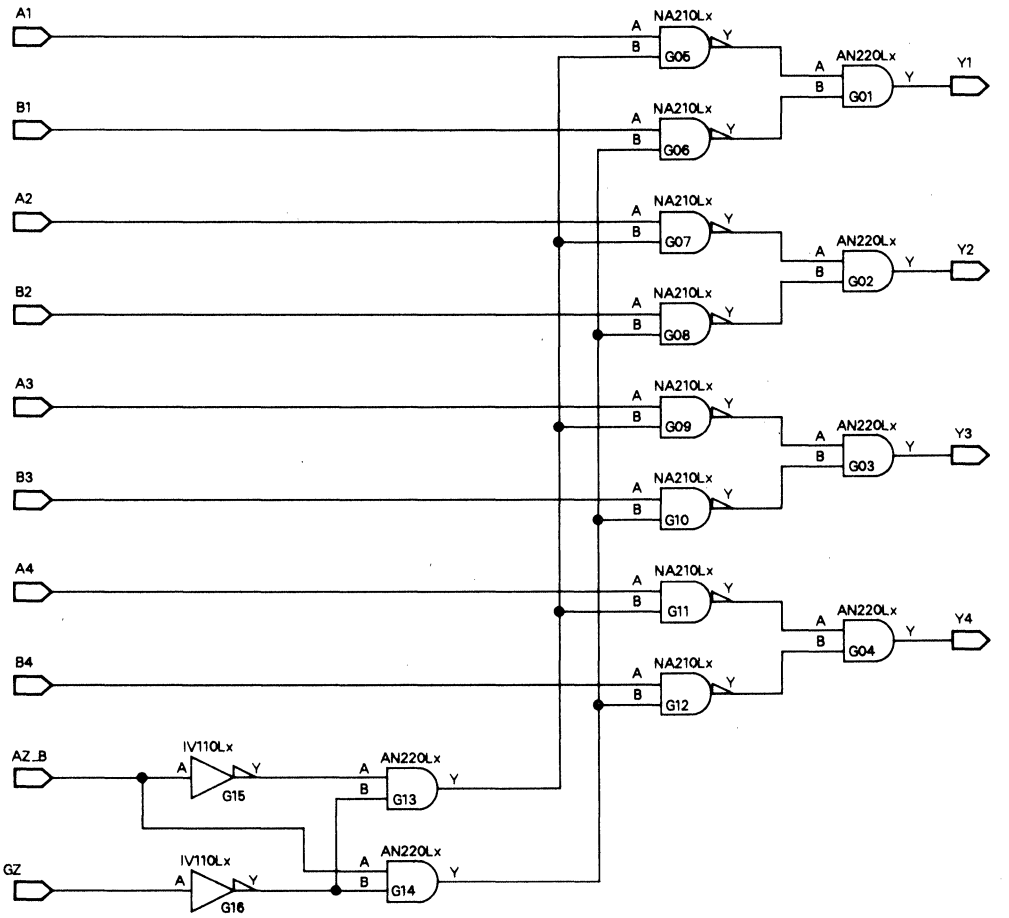
S158LJ
QUADRUPLE 2-LINE TO 1-LINE INVERTING MULTIPLEXER

D3030, APRIL 1988

FUNCTION TABLE

INPUTS				OUTPUT
STROBE	SELECT	DATA		
GZ	AZ_B	A	B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S158LJ
QUADRUPLE 2-LINE TO 1-LINE INVERTING MULTIPLEXER

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	AZ_B		0.11		pF
		All other inputs		0.05		
C_{pd}	dissipation capacitance		$t_r = t_f$ = 1 ns	4.7		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (See Note 1)

PARA-METER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any Z or B	Y		1.2	2.1		1.2	2	ns
t_{PHL}				1.1	2.2		1.1	2	
t_{PLH}	GZ or AZ_B	Y		2.5	4.7		2.5	4.2	ns
t_{PHL}				2.5	4.9		2.5	4.6	
Δt_{PLH}	Any	Y	0.2	0.56	1.16	0.2	0.56	1.06	ns/pF
Δt_{PHL}			0.14	0.36	0.72	0.16	0.36	0.64	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE†

```
BLOCK S158LJ;
A1          @INPUT;
A2          @INPUT;
A3          @INPUT;
A4          @INPUT;
B1          @INPUT;
B2          @INPUT;
B3          @INPUT;
B4          @INPUT;
AZ_B        @INPUT;
GZ          @INPUT;
Y1          @OUTPUT;
Y2          @OUTPUT;
Y3          @OUTPUT;
Y4          @OUTPUT;
STRUCTURE
G01         :AN220LJ    G05O,G06O,Y1;
G02         :AN220LJ    G07O,G08O,Y2;
G03         :AN220LJ    G09O,G10O,Y3;
G04         :AN220LJ    G11O,G12O,Y4;
G05         :NA210LJ    A1,G13O,G05O;
G06         :NA210LJ    B1,G14O,G06O;
G07         :NA210LJ    A2,G13O,G07O;
G08         :NA210LJ    B2,G14O,G08O;
G09         :NA210LJ    A3,G13O,G09O;
G10         :NA210LJ    B3,G14O,G10O;
G11         :NA210LJ    A4,G13O,G11O;
G12         :NA210LJ    B4,G14O,G12O;
G13         :AN220LJ    G15O,G16O,G13O;
G14         :AN220LJ    AZ_B,G16O,G14O;
G15         :IV110LJ    AZ_B,G15O;
G16         :IV110LJ    GZ,G16O;
END S158LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S251LJ
8-LINE TO 1-LINE MULTIPLEXER WITH 3-STATE OUTPUTS

D3030, APRIL 1988

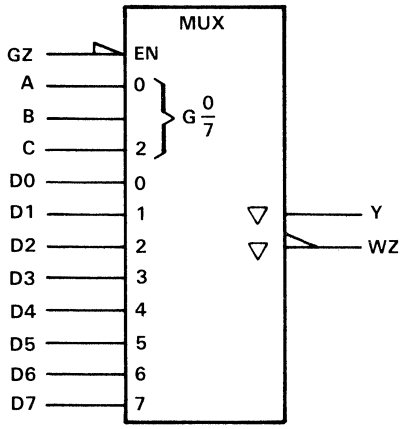
SOFTWARE MACRO

- **3-State Outputs Interface Internal Data Buses Directly**
- **Active-Low Strobe for Expandability**
- **Use Parallel Multiplexers for Multiple-Bit Words**

description

The S251LJ software macro implements an 8-line to 1-line multiplexer. The macro has a strobe input GZ, that enables and disables the 3-state outputs to facilitate interfacing the multiplexer directly with internal control or data buses. The Y output and the WZ output are in a high-impedance state when GZ is high. When GZ is low, the Y output assumes the level of the selected input and the WZ output is the complement of that level. This strobe permits the macro to also be employed for designing wider multiplexers, because only the enabled 8-bit field will output an active data bit. The S251LJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV110LJ	0.75	3	2.25	0.48
IV120LJ	1	4	4	1.24
IV212LJ	1.25	2	2.5	0.36
NA410LJ	1.5	8	12	1.52
NA810LJ	3.75	1	3.75	0.91
TOTALS		18	24.5	4.51

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S251LJ GZ,A,B,C,D0,D1,D2,D3,D4,D5,D6,D7,Y,WZ;

S251LJ
8-LINE TO 1-LINE MULTIPLEXER WITH 3-STATE OUTPUTS

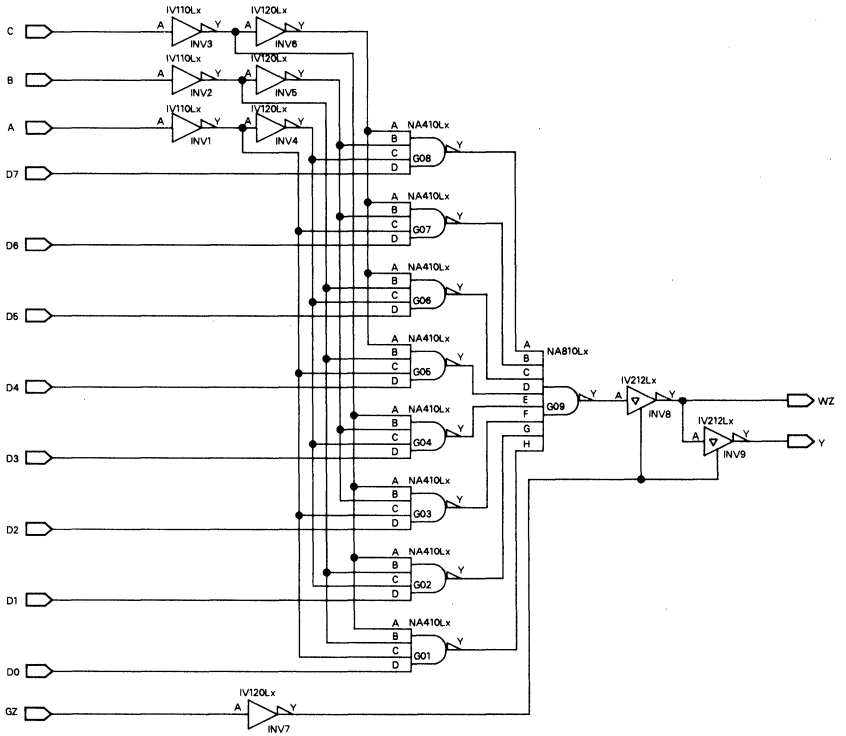
D3030, APRIL 1988

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	WZ
C	B	A	GZ		
X	X	X	H	Z	Z
L	L	L	L	D0	D0
L	L	H	L	D1	D1
L	H	L	L	D2	D2
L	H	H	L	D3	D3
H	L	L	L	D4	D4
H	L	H	L	D5	D5
H	H	L	L	D6	D6
H	H	H	L	D7	D7

D0,D1 . . . D7 = the level of the respective D input.

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S251LJ
8-LINE TO 1-LINE MULTIPLEXER WITH 3-STATE OUTPUTS

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	GZ		0.11		pF
		All other inputs		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	4.6		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (See Notes 1 and 2)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A, B, or C	Y		3.5	7.8		3.5	6.9	ns
t_{PHL}				3.6	8.9		3.6	8.2	
t_{PLH}		WZ		3.2	8.2		3.2	7.6	ns
t_{PHL}				3.2	6.8		3.2	6.2	
t_{PLH}	Any D	Y		2.5	5.6		2.5	5.1	ns
t_{PHL}				2.6	6.2		2.6	5.6	
t_{PLH}		WZ		2.2	5.6		2.2	5	ns
t_{PHL}				2.3	4.8		2.3	4.4	
t_{PZH}	GZ	Y		1.1	2.2		1.1	1.9	ns
t_{PZL}				0.7	1.2		0.7	1	
t_{PZH}		WZ		0.8	1.7		0.8	1.5	ns
t_{PZL}				0.8	1.4		0.8	1.2	
Δt_{PLH}	Any	Y, WZ	0.7	2.08	4.52	0.76	2.08	4.16	ns/pF
Δt_{PHL}			0.48	1.22	2.7	0.52	1.22	2.42	
Δt_{PZH}	Any	Y, WZ	0.76	2.14	4.8	0.8	2.14	4.38	ns/pF
Δt_{PZL}			0.52	1.26	2.88	0.56	1.26	2.56	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

2. Enable and delta-enable times are measured using the conditions specified for the IV212LJ.

HDL FILE†

```
BLOCK S251LJ;                    STRUCTURE
GZ          @INPUT;              G01     :NA410LJ  CZ,BZ,AZ,D0,U0;
A           @INPUT;              G02     :NA410LJ  CZ,BZ,AT,D1,U1;
B           @INPUT;              G03     :NA410LJ  CZ,BT,AZ,D2,U2;
C           @INPUT;              G04     :NA410LJ  CZ,BT,AT,D3,U3;
D0          @INPUT;              G05     :NA410LJ  CT,BZ,AZ,D4,U4;
D1          @INPUT;              G06     :NA410LJ  CT,BZ,AT,D5,U5;
D2          @INPUT;              G07     :NA410LJ  CT,BT,AZ,D6,U6;
D3          @INPUT;              G08     :NA410LJ  CT,BT,AT,D7,U7;
D4          @INPUT;              G09     :NA810LJ  U7,U6,U5,U4,U3,U2,U1,U0,YINT;
D5          @INPUT;              INV1    :IV110LJ  A,AZ;
D6          @INPUT;              INV2    :IV110LJ  B,BZ;
D7          @INPUT;              INV3    :IV110LJ  C,CZ;
Y           @OUTPUT;             INV4    :IV120LJ  AZ,AT;
WZ          @OUTPUT;             INV5    :IV120LJ  BZ,BT;
                                 INV6    :IV120LJ  CZ,CT;
                                 INV7    :IV120LJ  GZ,INV7O;
                                 INV8    :IV212LJ  YINT,INV7O,WZ;
                                 INV9    :IV212LJ  WZ,INV7O,Y;
                                 END S251LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S257ALJ
QUADRUPLE 2-LINE TO 1-LINE MULTIPLEXER WITH 3-STATE OUTPUTS

D3030 APRIL 1988

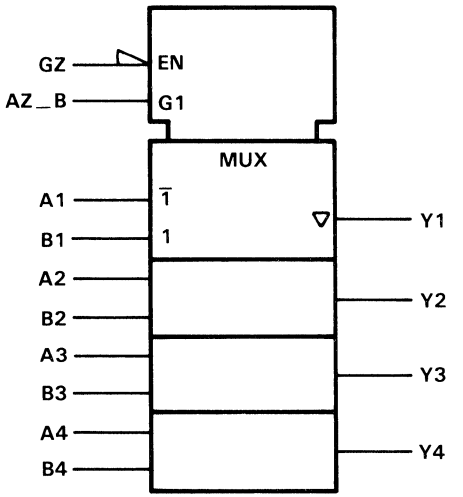
SOFTWARE MACRO

- **3-State Outputs Interface with Internal Data Buses Directly**
- **Active-Low Enable for Expandability**
- **Use Parallel Multiplexers for Multiple-Bit Words**

description

The S257ALJ software macro implements four 2-line to 1-line multiplexers. The macro has an enable input, GZ, that enables and disables the 3-state outputs to facilitate interfacing the multiplexers directly with internal control or data buses. The Y outputs are in a high-impedance state when GZ is high. When GZ is low, the outputs assume the levels of the selected inputs. This enable permits the macro to also be employed for designing wider multiplexers, because only the enabled 4-bit field will output an active data bit. The S257ALJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN220LJ	1.75	2	3.5	0.94
IV110LJ	0.75	10	7.5	1.6
IV212LJ	1.25	8	10	1.44
TOTALS		20	21	3.98

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S257ALJ A1,A2,A3,A4,B1,B2,B3,B4,GZ,AZ_B,Y1,Y2,Y3,Y4;

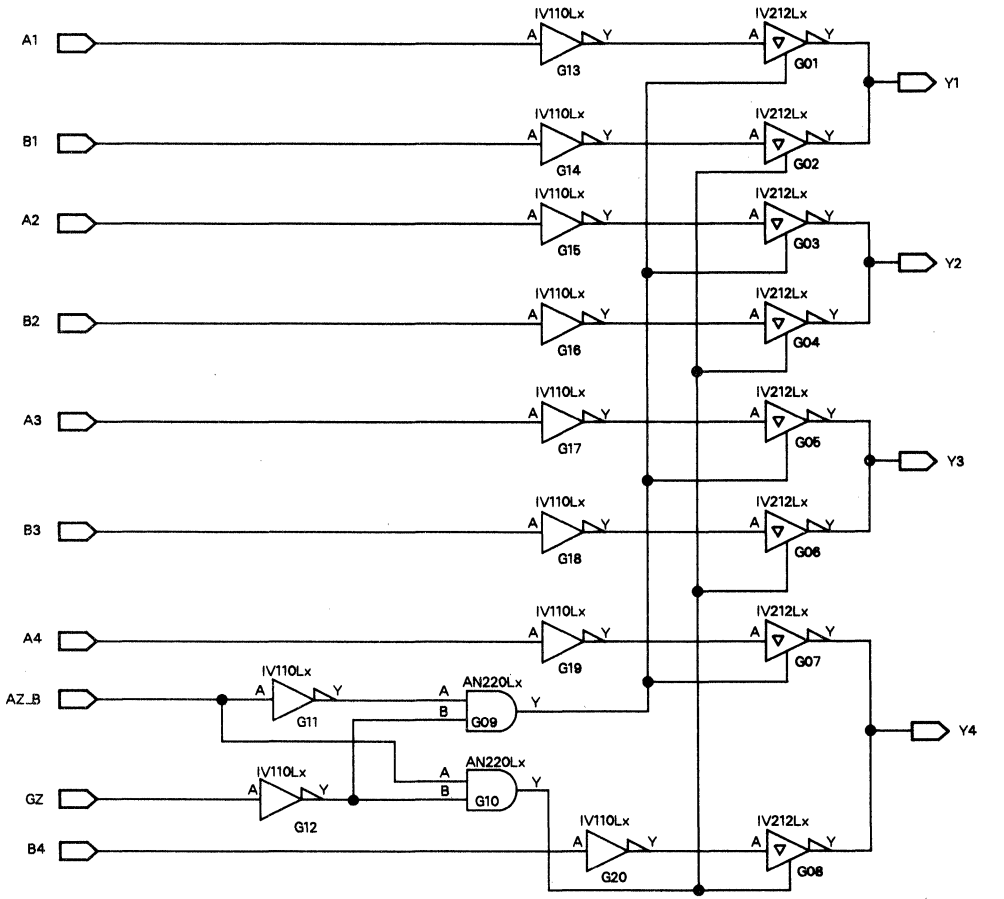
S257ALJ
QUADRUPLE 2-LINE TO 1-LINE MULTIPLEXER WITH 3-STATE OUTPUTS

D3030, APRIL 1988

FUNCTION TABLE

INPUTS				OUTPUT
ENABLE	SELECT	DATA		
GZ	AZ_B	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

logic diagram



S257ALJ
QUADRUPLE 2-LINE TO 1-LINE MULTIPLEXER WITH 3-STATE OUTPUTS

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	AZ__B		0.11		pF
		All other inputs		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	4		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A or B	Yn		0.9	1.9		0.9	1.7	ns
t_{PHL}				0.9	1.7		0.9	1.5	
t_{PLH}	AZ__B	Yn		1.9	3		1.9	2.8	ns
t_{PHL}				2.9	4		2.9	3.7	
t_{PZH}	GZ	Yn		1.8	3.7		1.8	3.5	ns
t_{PZL}				1.8	3.4		1.8	3.2	
Δt_{PLH}	Any	Yn	0.7	2.08	4.52	0.76	2.08	4.16	ns/pF
Δt_{PHL}			0.48	1.22	2.7	0.52	1.22	2.42	
Δt_{PZH}	Any	Yn	0.76	2.14	4.8	0.8	2.14	4.38	ns/pF
Δt_{PZL}			0.52	1.26	2.88	0.56	1.26	2.56	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

S257ALJ
QUADRUPLE 2-LINE TO 1-LINE MULTIPLEXER WITH 3-STATE OUTPUTS

D3030, APRIL 1988

HDL FILE†

```
BLOCK S257ALJ;
A1          @INPUT;
A2          @INPUT;
A3          @INPUT;
A4          @INPUT;
B1          @INPUT;
B2          @INPUT;
B3          @INPUT;
B4          @INPUT;
GZ          @INPUT;
AZ_B        @INPUT;
Y1          @OUTPUT;
Y2          @OUTPUT;
Y3          @OUTPUT;
Y4          @OUTPUT;
STRUCTURE
G01         :IV212LJ    G13O,G09O,Y1;
G02         :IV212LJ    G14O,G10O,Y1;
G03         :IV212LJ    G15O,G09O,Y2;
G04         :IV212LJ    G16O,G10O,Y2;
G05         :IV212LJ    G17O,G09O,Y3;
G06         :IV212LJ    G18O,G10O,Y3;
G07         :IV212LJ    G19O,G09O,Y4;
G08         :IV212LJ    G20O,G10O,Y4;
G09         :AN220LJ    G11O,G12O,G09O;
G10         :AN220LJ    AZ_B,G12O,G10O;
G11         :IV110LJ    AZ_B,G11O;
G12         :IV110LJ    GZ,G12O;
G13         :IV110LJ    A1,G13O;
G14         :IV110LJ    B1,G14O;
G15         :IV110LJ    A2,G15O;
G16         :IV110LJ    B2,G16O;
G17         :IV110LJ    A3,G17O;
G18         :IV110LJ    B3,G18O;
G19         :IV110LJ    A4,G19O;
G20         :IV110LJ    B4,G20O;
END S257ALJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S258ALJ
QUADRUPLE 2-LINE TO 1-LINE INVERTING MULTIPLEXER WITH 3-STATE OUTPUTS

D3030, APRIL 1988

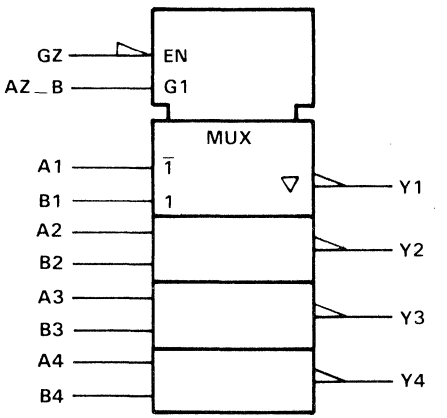
SOFTWARE MACRO

- **3-State Outputs Interface with Internal Data Buses Directly**
- **Active-Low Enable for Expandability**
- **Use Parallel Multiplexers for Multiple-Bit Words**

description

The S258ALJ software macro implements four 2-line to 1-line multiplexers. The macro has an enable input, GZ, that enables and disables the 3-state outputs to facilitate interfacing the multiplexers directly with internal control or data buses. The Y outputs are in a high-impedance state when GZ is high. When GZ is low, the outputs assume the complement of the level of the selected input. This enable permits the macro to also be employed for designing wider multiplexers, because only the enabled 4-bit field will output an active data bit. The S258ALJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN220LJ	1.75	2	3.5	0.94
IV110LJ	0.75	2	1.5	0.32
IV212LJ	1.25	8	10	1.44
TOTALS		12	15	2.7

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S258ALJ A1,A2,A3,A4,B1,B2,B3,B4,GZ,AZ_B,Y1,Y2,Y3,Y4;

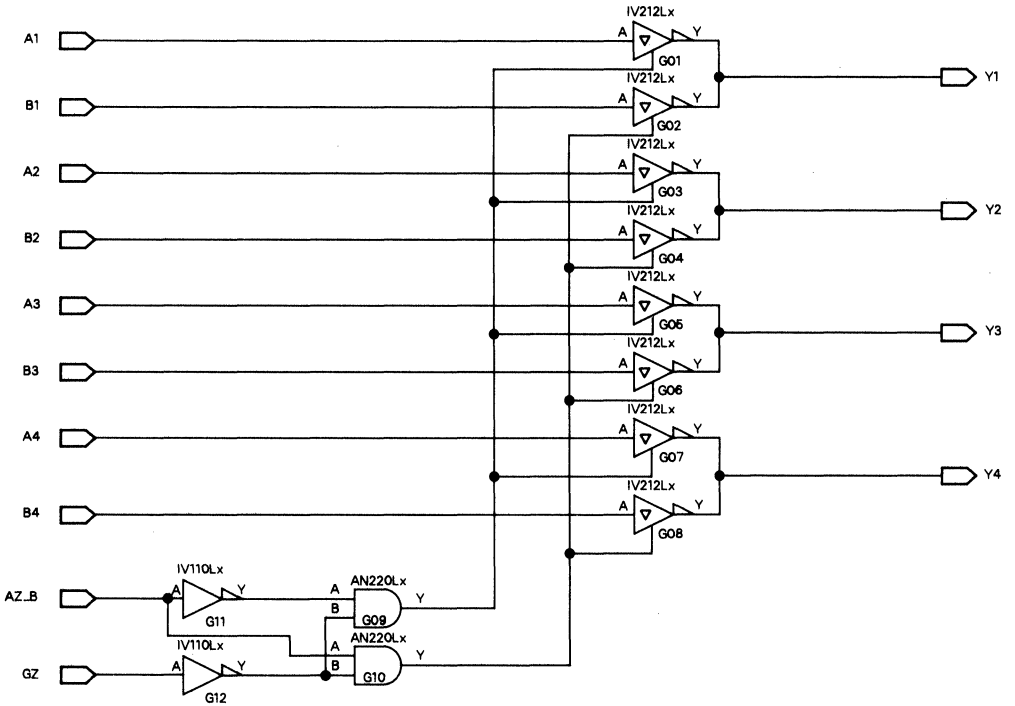
S258ALJ
QUADRUPLE 2-LINE TO 1-LINE INVERTING MULTIPLEXER WITH 3-STATE OUTPUTS

D3030, APRIL 1988

FUNCTION TABLE

INPUTS				OUTPUT
ENABLE	SELECT	DATA		
GZ	AZ_B	A	B	Y
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S258ALJ
QUADRUPLE 2-LINE TO 1-LINE INVERTING MULTIPLEXER WITH 3-STATE OUTPUTS

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	AZ__B		0.11		pF
		GZ		0.05		
		All other inputs		0.11		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	2.7		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Notes 1 and 2)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Any A or B	Yn		0.8	1.9		0.8	1.7	ns
t_{PHL}				0.6	1.2		0.6	1.2	
t_{PLH}	AZ__B	Yn		1.9	3.6		1.9	3.3	ns
t_{PHL}				2.9	4		2.9	3.7	
t_{PZH}	GZ	Yn		2.2	4.6		2.2	4.3	ns
t_{PZL}				2	3.9		2	3.6	
Δt_{PLH}	Any	Yn	0.7	2.08	4.52	0.76	2.08	4.16	ns/pF
Δt_{PHL}			0.48	1.22	2.7	0.52	1.22	2.42	
Δt_{PZH}	Any	Yn	0.76	2.14	4.8	0.8	2.14	4.38	ns/pF
Δt_{PZL}			0.52	1.26	2.88	0.56	1.26	2.56	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

2. Enable and delta-enable times are measured using the conditions specified for the IV212LH.

HDL FILE†

```
BLOCK S258ALJ;                  STRUCTURE
A1          @INPUT;             G01         :IV212LJ    A1,G09O,Y1;
A2          @INPUT;             G02         :IV212LJ    B1,G10O,Y1;
A3          @INPUT;             G03         :IV212LJ    A2,G09O,Y2;
A4          @INPUT;             G04         :IV212LJ    B2,G10O,Y2;
B1          @INPUT;             G05         :IV212LJ    A3,G09O,Y3;
B2          @INPUT;             G06         :IV212LJ    B3,G10O,Y3;
B3          @INPUT;             G07         :IV212LJ    A4,G09O,Y4;
B4          @INPUT;             G08         :IV212LJ    B4,G10O,Y4;
GZ          @INPUT;             G09         :AN220LJ    G11O,G12O,G09O;
AZ__B       @INPUT;             G10         :AN220LJ    AZ__B,G12O,G10O;
Y1          @OUTPUT;            G11         :IV110LJ    AZ__B,G11O;
Y2          @OUTPUT;            G12         :IV110LJ    GZ,G12O;
Y3          @OUTPUT;            END S258ALJ;
Y4          @OUTPUT;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

S298LJ
QUADRUPLE 2-INPUT MULTIPLEXER WITH NEGATIVE-EDGE-TRIGGERED REGISTER

D3030, APRIL 1988

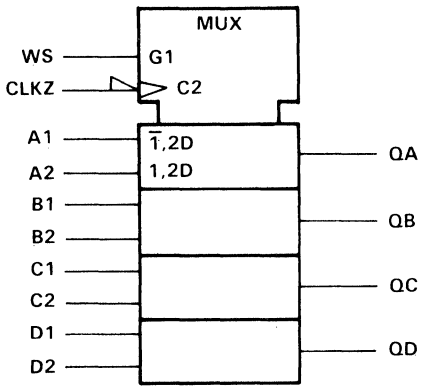
SOFTWARE MACRO

- **Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock**
- **Storage Register Loads New Data on Negative-Going Transition**
- **Implements Hexadecimal/BCD Shifter**
- **Parallel Multiplexers for Wider Words**

description

The S298LJ software macro implements a 4-bit 2-line to 1-line multiplexer with storage. When the Word-Select (WS) input is low, word one (A1, B1, C1, D1) is applied to the flip-flops. A high WS input causes word two (A2, B2, C2, D2) to be selected. The selected word is clocked to the outputs on the negative-going edge of the clock pulse. The S298LJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV120LJ	1	3	3	0.93
NA210LJ	1	12	12	2.28
R2405LJ	20.5	1	20.5	4.62
TO010LJ	1.5	1	1.5	NIL
TOTALS		17	37	7.83

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S298LJ A1,A2,B1,B2,C1,C2,D1,D2,CLKZ,WS,QA,QB,QC,QD;

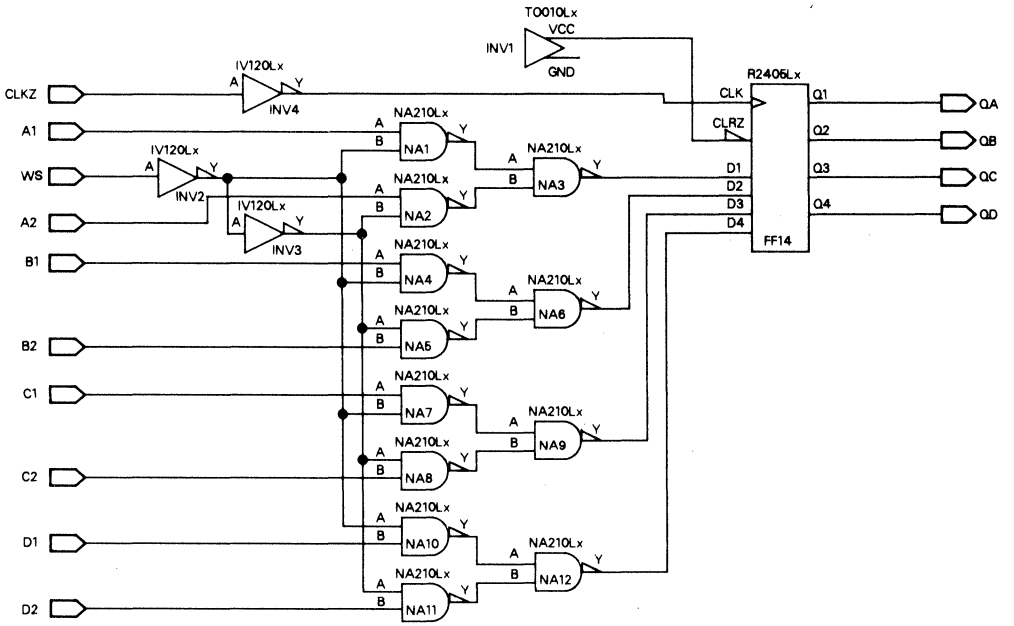
S298LJ
QUADRUPLE 2-INPUT MULTIPLEXER WITH NEGATIVE-EDGE-TRIGGERED REGISTER

D3030, APRIL 1988

FUNCTION TABLE

INPUTS		OUTPUTS			
WS	CLKZ	QA	QB	QC	QD
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	QA_0	QB_0	QC_0	QD_0

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S298LJ
QUADRUPLE 2-INPUT MULTIPLEXER WITH NEGATIVE-EDGE-TRIGGERED REGISTER

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLRZ		0.11		pF
		WS		0.11		
		All other inputs		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	7.83		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLKZ	Qn		1.8	3.7		1.8	3.5	ns
t_{PHL}				2	4.2		2	3.9	
Δt_{PLH}	Any	Qn	0.42	1.06	2.24	0.44	1.06	2.04	ns/pF
Δt_{PHL}			0.34	0.78	1.58	0.36	0.78	1.4	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

S298LJ
QUADRUPLE 2-INPUT MULTIPLEXER WITH NEGATIVE-EDGE-TRIGGERED REGISTER

D3030, APRIL 1988

HDL FILE†

```
BLOCK S298LJ;
A1      @INPUT;
A2      @INPUT;
B1      @INPUT;
B2      @INPUT;
C1      @INPUT;
C2      @INPUT;
D1      @INPUT;
D2      @INPUT;
CLKZ    @INPUT;
WS      @INPUT;
QA      @OUTPUT;
QB      @OUTPUT;
QC      @OUTPUT;
QD      @OUTPUT;
STRUCTURE
FF14    :R2405LJ    INV1O,NA3O,NA6O,NA9O,
                    NA12O,INV4O,QA,QB,QC,QD;
INV1    :TO010LJ    DUM,INV1O;
INV2    :IV120LJ    WS,INV2O;
INV3    :IV120LJ    INV2O,INV3O;
INV4    :IV120LJ    CLKZ,INV4O;
NA1     :NA210LJ    A1,INV2O,NA1O;
NA10    :NA210LJ    INV2O,D1,NA10O;
NA11    :NA210LJ    INV3O,D2,NA11O;
NA12    :NA210LJ    NA10O,NA11O,NA12O;
NA2     :NA210LJ    A2,INV3O,NA2O;
NA3     :NA210LJ    NA1O,NA2O,NA3O;
NA4     :NA210LJ    B1,INV2O,NA4O;
NA5     :NA210LJ    INV3O,B2,NA5O;
NA6     :NA210LJ    NA4O,NA5O,NA6O;
NA7     :NA210LJ    C1,INV2O,NA7O;
NA8     :NA210LJ    INV3O,C2,NA8O;
NA9     :NA210LJ    NA7O,NA8O,NA9O;
END S298LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S398LJ QUADRUPLE 2-INPUT MULTIPLEXER WITH POSITIVE-EDGE-TRIGGERED COMPLEMENTARY OUTPUT REGISTER

D3030, APRIL 1988

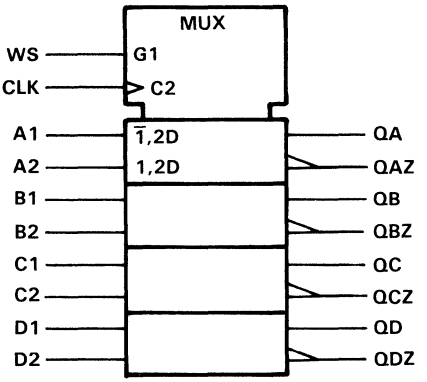
SOFTWARE MACRO

- Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock
- Storage Register Loads New Data on Positive-Going Transition
- Implements Hexadecimal/BCD Shifter
- Use Parallel Multiplexers for Multiple-Bit Words

description

The S398LJ software macro implements four 2-line to 1-line multiplexers with storage. When the world-select (WS) input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high WS input causes word 2 (A2, B2, C2, D2) to be selected. The selected word is clocked to the outputs on the positive-going edge of the clock pulse. The S398LJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS		OUTPUTS‡			
WORD SELECT	CLK	QA	QB	QC	QD
L	↑	a1	b1	c1	d1
H	↑	a2	b2	c2	d2
X	L	QA_0	QB_0	QC_0	QD_0

‡ Corresponding QnZ output is the complement of (shown).

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV120LJ	1	2	2	0.62
NA210LJ	1	12	12	2.28
R2406LJ	23.5	1	23.5	5.16
TO010LJ	1.5	1	1.5	NIL
TOTALS		16	39	8.06

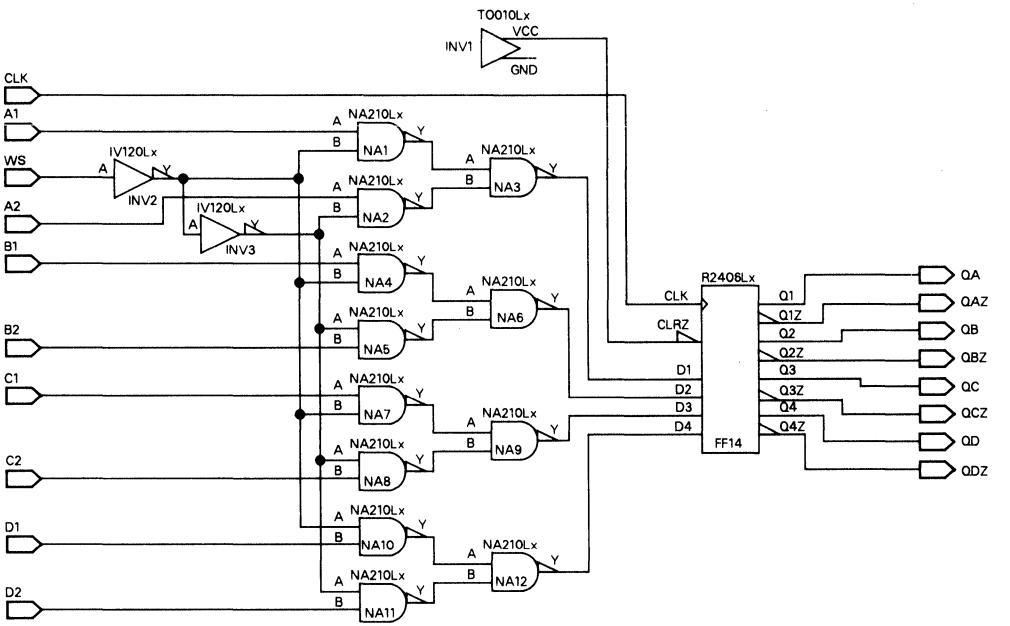
When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S398LJ A1,A2,B1,B2,C1,C2,D1,D2,CLK,WS,QA,QAZ,QB,QBZ,QC,QCZ,QD,QDZ;

S398LJ
QUADRUPLE 2-INPUT MULTIPLEXER WITH POSITIVE-EDGE-TRIGGERED COMPLEMENTARY OUTPUT REGISTER

D3030, APRIL 1988

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

QUADRUPLE 2-INPUT MULTIPLEXER WITH POSITIVE-EDGE-TRIGGERED COMPLEMENTARY OUTPUT REGISTER

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.11		pF
		WS		0.11		
		All other inputs		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	8.06		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(see Note 1), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Qn		1.4	3.1		1.4	2.8	ns
t_{PHL}				1.6	3.6		1.6	3.3	
t_{PLH}	CLK	QnZ		1.8	3.9		1.8	3.5	ns
t_{PHL}				1.7	3.8		1.7	3.5	
Δt_{PLH}	Any	Qn	0.42	1.12	2.32	0.44	1.12	2.12	ns/pF
Δt_{PHL}			0.26	0.76	1.54	0.28	0.76	1.4	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE†

```
BLOCK S398LJ;                    STRUCTURE
A1          @INPUT;              FF14        :R2406LJ   INV1O,NA3O,NA6O,NA9O,
A2          @INPUT;                                     NA12O,CLK,QA,QAZ,
B1          @INPUT;                                     QB,QBZ,QC,QCZ,QD,QDZ;
B2          @INPUT;              INV1        :TO010LJ   DUM,INV1O;
C1          @INPUT;              INV2        :IV120LJ   WS,INV2O;
C2          @INPUT;              INV3        :IV120LJ   INV2O,INV3O;
D1          @INPUT;              NA1         :NA210LJ   A1,INV2O,NA1O;
D2          @INPUT;              NA10        :NA210LJ   INV2O,D1,NA10O;
CLK         @INPUT;              NA11        :NA210LJ   INV3O,D2,NA11O;
WS          @INPUT;              NA12        :NA210LJ   NA10O,NA11O,NA12O;
QA          @OUTPUT;             NA2         :NA210LJ   A2,INV3O,NA2O;
QAZ         @OUTPUT;             NA3         :NA210LJ   NA1O,NA2O,NA3O;
QB          @OUTPUT;             NA4         :NA210LJ   B1,INV2O,NA4O;
QBZ         @OUTPUT;             NA5         :NA210LJ   INV3O,B2,NA5O;
QC          @OUTPUT;             NA6         :NA210LJ   NA4O,NA5O,NA6O;
QCZ         @OUTPUT;             NA7         :NA210LJ   C1,INV2O,NA7O;
QD          @OUTPUT;             NA8         :NA210LJ   INV3O,C2,NA8O;
QDZ         @OUTPUT;             NA9         :NA210LJ   NA7O,NA8O,NA9O;
                                 END S398LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

S399LJ
QUADRUPLE 2-INPUT MULTIPLEXER WITH POSITIVE-EDGE-TRIGGERED REGISTER

D3030, APRIL 1988

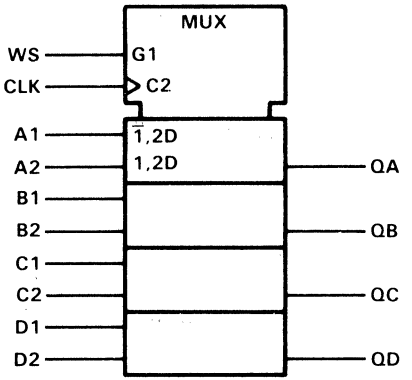
SOFTWARE MACRO

- **Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock**
- **Storage Register Loads New Data on Positive-Going Transition**
- **Implements Hexadecimal/BCD Shifter**
- **Use Parallel Multiplexers for Multiple-Bit Words**

description

The S399LJ software macro implements four 2-line to 1-line multiplexers with storage. When the word-select (WS) input is low, word one (A1, B1, C1, D1) is applied to the flip-flops. A high WS input causes word two (A2, B2, C2, D2) to be selected. The selected word is clocked to the outputs on the positive-going edge of the clock pulse. The S399LJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV120LJ	1	2	2	0.62
NA210LJ	1	12	12	2.28
R2405LJ	20.5	1	20.5	4.62
TO010LJ	1.5	1	1.5	NIL
TOTALS		16	36	7.52

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S399LJ A1,A2,B1,B2,C1,C2,D1,D2,CLK,WS,QA,QB,QC,QD;

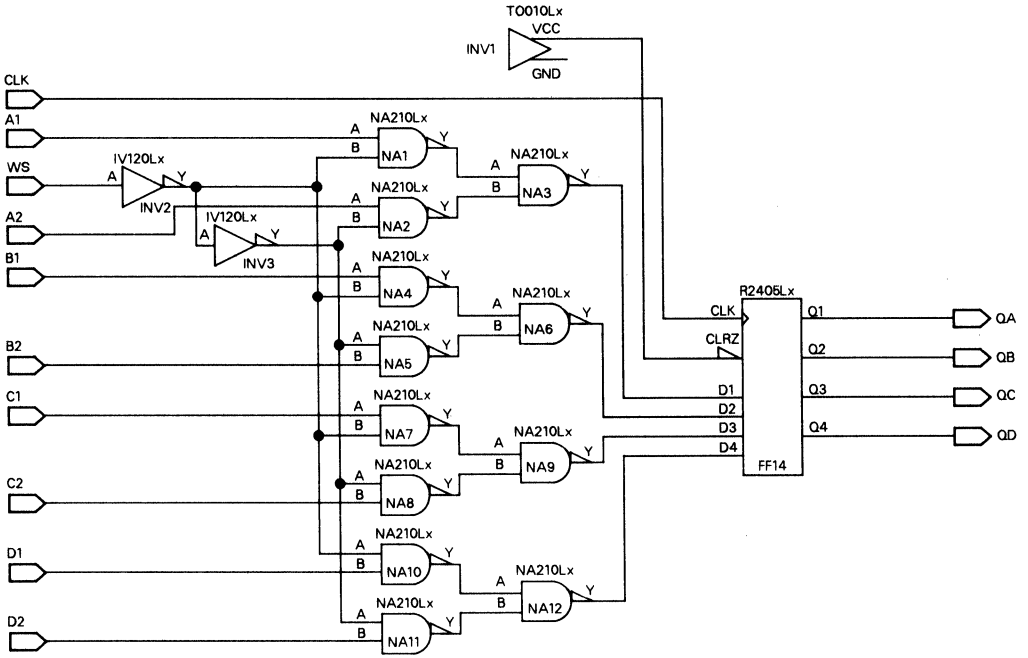
S399LJ
QUADRUPLE 2-INPUT MULTIPLEXER WITH POSITIVE-EDGE-TRIGGERED REGISTER

D3030, APRIL 1988

FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLK	QA	QB	QC	QD
L	↑	a1	b1	c1	d1
H	↑	a2	b2	c2	d2
X	L	QA_0	QB_0	QC_0	QD_0

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S399LJ
QUADRUPLE 2-INPUT MULTIPLEXER WITH POSITIVE-EDGE-TRIGGERED REGISTER

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance;	CLK		0.11		pF
		WS		0.11		
		All other inputs		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	7.52		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Qn		1.4	3.1		1.4	2.9	ns
t_{PHL}				1.6	3.6		1.6	3.3	
Δt_{PLH}	CLK	Qn	0.42	1.06	2.24	0.44	1.06	2.04	ns/pF
Δt_{PHL}			0.34	0.78	1.58	0.36	0.78	1.4	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE†

```
BLOCK S399LJ;
A1          @INPUT;
A2          @INPUT;
B1          @INPUT;
B2          @INPUT;
C1          @INPUT;
C2          @INPUT;
D1          @INPUT;
D2          @INPUT;
CLK         @INPUT;
WS          @INPUT;
QA          @OUTPUT;
QB          @OUTPUT;
QC          @OUTPUT;
QD          @OUTPUT;

STRUCTURE
FF14        :R2405LJ    INV1O,NA3O,NA6O,NA9O,
                        NA12O,CLK,QA,QB,
                        QC,QD;
INV1        :TO010LJ    DUM,INV1O;
INV2        :IV120LJ    WS,INV2O;
INV3        :IV120LJ    INV2O,INV3O;
NA1         :NA210LJ    A1,INV2O,NA1O;
NA10        :NA210LJ    INV2O,D1,NA10O;
NA11        :NA210LJ    INV3O,D2,NA11O;
NA12        :NA210LJ    NA10O,NA11O,NA12O;
NA2         :NA210LJ    A2,INV3O,NA2O;
NA3         :NA210LJ    NA1O,NA2O,NA3O;
NA4         :NA210LJ    B1,INV2O,NA4O;
NA5         :NA210LJ    INV3O,B2,NA5O;
NA6         :NA210LJ    NA4O,NA5O,NA6O;
NA7         :NA210LJ    C1,INV2O,NA7O;
NA8         :NA210LJ    INV3O,C2,NA8O;
NA9         :NA210LJ    NA7O,NA8O,NA9O;
END S399LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

18 Registers

D3030, APRIL 1988

REGISTERS – POSITIVE-EDGE-TRIGGERED

DESCRIPTION	f_{clock} (MHz)	CELL NAME	OUTPUT DRIVE	COMMENTS	EQUIVALENT NA210s	PAGE
4-Bit SIPO	175	R2401LJ	1X	Async clear (L)	23.5	18-3
4-Bit SIPO Comp Outputs	175	R2402LJ	1X	Async clear (L)	25.5	18-5
4-Bit SIPO/PIPO	170	R2403LJ	1X	Parallel load (L)	29.5	18-7
4-Bit SIPO/PIPO Comp Outputs	170	R2404LJ	1X	Parallel load (L)	31.5	18-9
4-Bit PIPO	150	R2405LJ	1X	Async clear (L)	20.5	18-11
4-Bit PIPO Comp Outputs	150	R2406LJ	1X	Async clear (L)	23.5	18-13
4-Bit PIPO 3-State Outputs	150	R2407LJ	1X	Async clear (L)	24.5	18-15

REGISTERS (SOFTWARE)

DESCRIPTION	CELL NAME	OUTPUT DRIVE	COMMENTS	EQUIVALENT NA210s	PAGE
8-Bit SIPO with AND Gate Input	S164LJ	2X	Async clear (L)	50.75	18-17
8-Bit PISO and Complementary MSB Outputs	S165ALJ	1X	Parallel load (L) and clock inhibit input	85.5	18-22
8-Bit SISO/PISO	S166LJ	1X	Parallel load (L), Clock inhibit, and async clear (L)	66.5	18-28
4-Bit PIPO Bidirectional Shift	S194ALJ	1X	Parallel load, shift right, shift left, do nothing, and async clear (L)	52.75	18-34
4-Bit PIPO with J-KZ Serial Inputs and Complementary MSB Outputs	S195ALJ	1X	Parallel, load, serial shift, and async clear (L)	41.5	18-40
8-Bit PIPO Bidirectional Shift with 3-State Inputs/Outputs	S299LJ	1X	Parallel load, shift right, shift left, do nothing, and async clear (L)	127	18-46
8-Bit PIPO Bidirectional Shift	S299XLJ	1X	Parallel load, shift right, shift left, do nothing, and async clear (L)	101.25	18-53
8-Bit SIPO with 3-State Outputs	S595LJ	1X	Separate clocks for shift and output register, and async S/R clear (L)	99.5	18-59

REGISTERS (SOFTWARE) (Continued)

DESCRIPTION	CELL NAME	OUTPUT DRIVE	COMMENTS	EQUIVALENT NA210s	PAGE
8-Bit SIPO with PI Input Register and 3-State S/R Outputs	S598XLJ	1X	Parallel load from input registers, multiplexed dual serial inputs, separate reg and S/R clocks, and async S/R clear (L)	160.25	18-63
8-Bit PIPO Bidirectional Transceiver	S651LJ	1X	Sources real time or stored data, independent clocks, inverting data paths	172.5	18-69
8-Bit PIPO Bidirectional Transcseiver	S652LJ	1X	Sources real time or stored data, independent clocks, noninverting data paths	196.5	18-77

R2401LJ
4-BIT REGISTER
WITH SERIAL INPUT AND ASYNCHRONOUS CLEAR

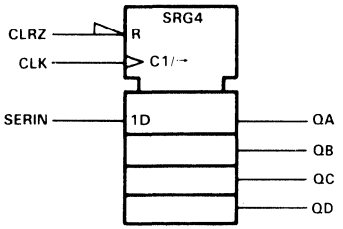
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUTS			
CLRZ	CLK	SERIN	QA	QB	QC	QD
L	X	X	L	L	L	L
H	↑	H	H	QA_n	QB_n	QC_n
H	↑	L	L	QA_n	QB_n	QC_n
H	L	X	Q_0	Q_0	Q_0	Q_0

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The R2401LJ cell implements a 4-bit serial-input shift register with true outputs. Its four-bit length simplifies design of large registers.

The register contains an embedded clock driver that buffers the clock input to a single 2-line input. This feature simplifies implementing longer registers because standard library buffers can be used to drive multiple clock inputs, which are used in the longer registers. When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: R2401LJ CLRZ,SERIN,CLK,QA,QB,QC,QD;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	175	MHz
t_w	Pulse duration	CLRZ low	2		ns
		CLK high	2.9		
		CLK low	2.9		
t_{su}	Setup time before clock	SERIN (H or L)	2		ns
		CLRZ inactive (H)	0		
t_h	Hold time after clock	SERIN (H or L)	0		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.11		pF
		CLRZ		0.47		
		SERIN		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	4.53		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.55	1.51	3.25	0.60	1.51	2.97	ns
t_{PHL}			0.54	1.64	3.59	0.57	1.64	3.31	
t_{PHL}	CLRZ	Q	0.27	0.67	1.36	0.29	0.67	1.25	ns
Δt_{PLH}	CLK	Q	0.22	0.62	1.32	0.24	0.62	1.22	ns/pF
Δt_{PHL}			0.18	0.42	0.88	0.2	0.42	0.78	
Δt_{PHL}	CLRZ	Q	0.18	0.4	0.86	0.2	0.4	0.78	ns/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

R2402LJ
4-BIT SHIFT REGISTER
WITH SERIAL INPUT AND COMPLEMENTARY OUTPUTS

D3030, APRIL 1988

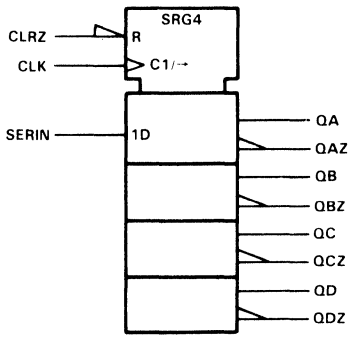
INTERNAL CELL

FUNCTION TABLE

INPUTS			OUTPUTS			
CLRZ	CLK	SERIN	QA*	QB*	QC*	QD*
L	X	X	L	L	L	L
H	↑	H	H	QA_n	QB_n	QC_n
H	↑	L	L	QA_n	QB_n	QC_n
H	L	X	Q_0	Q_0	Q_0	Q_0

*The QXZ output is the complement of QX.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The R2402LJ cell implements a 4-bit serial-input shift register with complementary outputs. Its four-bit length simplifies design of large registers.

The register contains an embedded clock driver that buffers the clock input to a single 2-line input. This feature simplifies implementing longer registers because standard library buffers can be used to drive multiple clock inputs, which are used in the longer registers. When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: R2402LJ CLRZ,SERIN,CLK,QA,QAZ,QB,QBZ,QC,QCZ,QD,QDZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	175	MHz
t_w	Pulse duration	CLRZ low	2		ns
		CLK high	2.9		
		CLK low	2.9		
t_{su}	Setup time before clock	SERIN (H or L)	2		ns
		CLRZ inactive (H)	0		
t_h	Hold time after clock	SERIN (H or L)	0		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.11		pF
		CLRZ		0.47		
		SERIN		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	5.08		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.58	1.62	3.5	0.63	1.62	3.21	ns
t_{PHL}			0.55	1.71	3.79	0.6	1.71	3.46	
t_{PLH}	CLK	QZ	0.63	1.83	4.04	0.68	1.83	3.71	ns
t_{PHL}			0.59	1.7	3.74	0.63	1.7	3.41	
t_{PLH}	CLRZ	QZ	0.33	0.85	1.8	0.36	0.85	1.65	ns
t_{PHL}	CLRZ	Q	0.29	0.74	1.53	0.3	0.74	1.4	
Δt_{PLH}	CLK	Q	0.24	0.6	1.28	0.24	0.6	1.18	ns/pF
Δt_{PHL}			0.2	0.4	0.8	0.2	0.4	0.74	
Δt_{PLH}	CLK	QZ	0.38	1.02	2.16	0.42	1.02	1.98	ns/pF
Δt_{PHL}			0.46	1.2	2.58	0.5	1.2	2.38	
Δt_{PLH}	CLRZ	QZ	0.42	1.02	2.14	0.44	1.02	1.96	ns/pF
Δt_{PHL}	CLRZ	Q	0.16	0.38	0.78	0.18	0.38	0.7	ns/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

R2403LJ
4-BIT SHIFT REGISTER
WITH SERIAL AND PARALLEL INPUTS

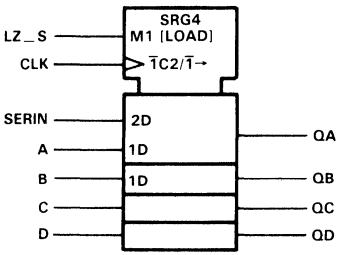
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE

INPUTS							OUTPUTS			
			DATA							
LZ_S	CLK	SERIN	A	B	C	D	QA	QB	QC	QD
L	↑	X	a	b	c	d	a	b	c	d
H	↑	H	X	X	X	X	H	QA_n	QB_n	QC_n
H	↑	L	X	X	X	X	L	QA_n	QB_n	QC_n
X	L	X	X	X	X	X	Q_0	Q_0	Q_0	Q_0

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The R2403LJ cell implements a 4-bit serial-input or parallel-input shift register with true outputs. The four-bit length simplifies design of large registers.

The register contains an embedded clock driver that buffers the clock input to a single 2-line input. This feature simplifies implementing longer registers because standard library buffers can be used to drive multiple clock inputs, which are used in the longer registers. When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: R2403LJ SERIN,LZ_S,CLK,A,B,C,D,QA,QB,QC,QD;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	170	MHz
t_w	Pulse duration	CLK high	2.9		ns
		CLK low	2.9		
t_{su}	Setup time before clock	SERIN (H or L)	2		ns
		LZ_S (H or L)	0		
		A..D (H or L)	2		
t_h	Hold time after clock	SERIN (H or L)	0		ns
		LZ_S (H or L)	0		
		A..D (H or L)	0		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.11		pF
		Dn		0.07		
		LZ_S		0.35		
		SERIN		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	5.18		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.53	1.38	2.94	0.57	1.38	2.69	ns
t_{PHL}			0.55	1.6	3.53	0.6	1.6	3.22	
Δt_{PLH}	CLK	Q	0.2	0.6	1.28	0.22	0.6	1.16	ns/pF
Δt_{PHL}			0.2	0.42	0.82	0.18	0.42	0.76	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

R2404LJ
4-BIT SHIFT REGISTER WITH SERIAL/ PARALLEL INPUTS AND COMPLEMENTARY OUTPUTS

D3030, APRIL 1988

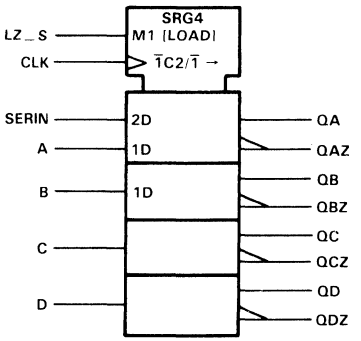
INTERNAL CELL

FUNCTION TABLE

INPUTS							OUTPUTS			
			DATA							
LZ_S	CLK	SERIN	A	B	C	D	QA*	QB*	QC*	QD*
L	↑	X	a	b	c	d	a	b	c	d
H	↑	H	X	X	X	X	H	QA_n	QB_n	QC_n
H	↑	L	X	X	X	X	L	QA_n	QB_n	QC_n
X	L	X	X	X	X	X	Q_0	Q_0	Q_0	Q_0

*The QXZ output is the complement of QX.

logic†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The R2404LJ cell implements a 4-bit serial-input or parallel-input shift register with complementary outputs. The four-bit length simplifies design of large registers.

The register contains an embedded clock driver that buffers the clock input to a single 2-line input. This feature simplifies implementing longer registers because standard library buffers can be used to drive multiple clock inputs, which are used in the longer registers. When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: R2404LJ SERIN,LZ_S,CLK,A,B,C,D,QA,QAZ,QB,QBZ,QC,QCZ,QD,QDZ;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	170	MHz
t_w	Pulse duration	CLK high	2.9		ns
		CLK low	2.9		
t_{su}	Setup time before clock	SERIN (H or L)	2		ns
		LZ_S (H or L)	0		
		A..D (H or L)	2		
t_h	Hold time after clock	SERIN (H or L)	0		ns
		LZ_S (H or L)	0		
		A..D (H or L)	0		

R2404LJ
4-BIT SHIFT REGISTER WITH SERIAL/ PARALLEL INPUTS AND COMPLEMENTARY OUTPUTS

D3030, APRIL 1988

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.11		pF
		Dn		0.07		
		LZ_S		0.34		
		SERIN		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	4.92		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Q	0.56	1.47	3.16	0.59	1.47	2.88	ns
t_{PHL}			0.56	1.68	3.68	0.61	1.68	3.37	
t_{PLH}	CLK	QZ	0.64	1.78	3.92	0.67	1.78	3.6	ns
t_{PHL}			0.59	1.55	3.38	0.62	1.55	3.1	
Δt_{PLH}	CLK	Q	0.22	0.6	1.26	0.22	0.6	1.16	ns/pF
Δt_{PHL}			0.2	0.38	0.78	0.2	0.38	0.7	
Δt_{PLH}	CLK	QZ	0.36	1.02	2.16	0.4	1.02	1.96	ns/pF
Δt_{PHL}			0.46	1.22	2.56	0.48	1.22	2.34	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

R2405LJ
4-BIT FLIP-FLOPS/REGISTER WITH ASYNCHRONOUS CLEAR

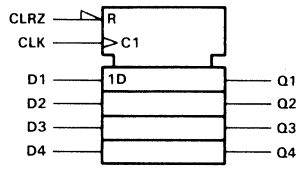
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLRZ	CLK	Dn	Qn
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	$\overline{Q}_0$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The R2405LJ cell implements four D-type flip-flops or 4-bit parallel-input register element with true outputs. Its four-bit length simplifies design of large registers.

The flip-flops/register contains an embedded clock driver that buffers the clock input. This feature simplifies implementing longer registers because standard library buffers can be used to drive multiple clock inputs that are used in the longer registers. When the flip-flops/register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: R2405LJ CLRZ,D1,D2,D3,D4,CLK,Q1,Q2,Q3,Q4;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	150	MHz
t_w	Pulse duration	CLRZ low	2		ns
		CLK high or low	3.3		
t_{su}	Setup time before clock	Dn (high or low)	2		ns
		CLRZ inactive (high)	0		
t_h	Hold time after clock	Dn (high or low)	0		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.11		pF
		CLRZ		0.47		
		Dn		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	4.62		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Qn	0.55	1.45	3.14	0.59	1.45	2.88	ns
t_{PHL}			0.53	1.62	3.61	0.58	1.62	3.31	
t_{PLH}	CLRZ	Qn	0.28	0.66	1.35	0.28	0.66	1.23	ns
Δt_{PLH}	CLK	Qn	0.42	1.06	2.24	0.44	1.06	2.04	ns/pF
Δt_{PHL}	CLRZ	Qn	0.34	0.78	1.58	0.36	0.78	0.7	ns/pF
Δt_{PHL}			0.34	0.76	1.54	0.36	0.76	1.4	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

R2406LJ
4-BIT FLIP-FLOPS/REGISTER WITH COMPLEMENTARY OUTPUTS

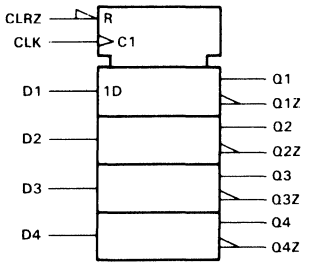
D3030, APRIL 1988

INTERNAL CELL

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLRZ	CLK	Dn	Qn	QZn
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The R2406LJ cell implements a 4-bit D-type flip-flop/register element with asynchronous clear and complementary outputs. Its four-bit length simplifies design of large registers.

The flip-flops/register contains an embedded clock driver that buffers the clock input. This feature simplifies implementing longer registers because standard library buffers can be used to drive multiple clock inputs that are used in the longer registers. When the flip-flops/register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: R2406LJ CLRZ,D1,D2,D3,D4,CLK,Q1,Q1Z,Q2,Q2Z,Q3,Q3Z,Q4,Q4Z;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	150	MHz
t_w	Pulse duration	CLRZ low	2		ns
		CLK high or low	3.3		
t_{su}	Setup time before clock	Dn (high or low)	2		ns
		CLRZ inactive (high)	0		
t_h	Hold time after clock	Dn (high or low)	0		ns

R2406LJ
4-BIT FLIP-FLOPS/REGISTER WITH COMPLEMENTARY OUTPUTS

D3030, APRIL 1988

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.11		pF
		CLRZ		0.47		
		Dn		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	5.16		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Qn	0.57	1.43	3.13	0.59	1.43	2.87	ns
t_{PHL}			0.56	1.64	3.63	0.59	1.64	3.33	
t_{PLH}	CLK	QZn	0.61	1.76	3.89	0.65	1.76	3.54	ns
t_{PHL}			0.68	1.76	3.84	0.71	1.76	3.51	
t_{PLH}	CLRZ	QZn	0.39	0.9	1.89	0.41	0.9	1.72	ns
t_{PHL}	CLRZ	Qn	0.28	0.65	1.33	0.29	0.65	1.22	
Δt_{PLH}	CLK	Qn	0.42	1.12	2.32	0.44	1.12	2.12	ns/pF
Δt_{PHL}			0.34	0.76	1.54	0.36	0.76	1.4	
Δt_{PLH}	CLK	QZn	0.42	1.08	2.26	0.44	1.08	2.08	ns/pF
Δt_{PHL}			0.26	0.6	1.18	0.28	0.6	1.06	
Δt_{PLH}	CLRZ	QZn	0.4	1.08	2.26	0.42	1.08	2.08	ns/pF
Δt_{PHL}		Qn	0.34	0.76	1.54	0.36	0.76	1.4	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

R2407LJ
4-BIT FLIP-FLOPS/REGISTER WITH 3-STATE OUTPUTS

D3030, APRIL 1988

INTERNAL CELL

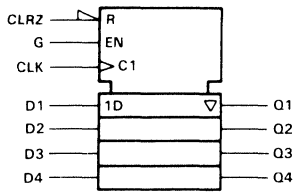
FUNCTION TABLE
(EACH FLIP-FLOP) (see Note 1)

INPUTS				OUTPUT
G	CLRZ	CLK	Dn	Qn
H	L	X	X	L
H	H	↑	H	H
H	H	↑	L	L
H	H	L	X	Q_0
L	X	X	X	Z

Q_0 = level of Q before the indicated steady-state input conditions were established.

NOTE 1: When G is low, the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The R2407LJ cell implements a four D-type flip-flops or a 4-bit parallel-input register element with three-state outputs. Its four-bit length simplifies design of large registers.

The flip-flops/register contains an embedded clock driver that buffers the clock input. This feature simplifies implementing longer registers because standard library buffers can be used to drive multiple clock inputs that are used in the longer registers. When the flip-flops/register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: R2407LJ CLRZ,D1,D2,D3,D4,CLK,G,Q1,Q2,Q3,Q4;

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	150	MHz
t_w	Pulse duration	CLRZ low	2		ns
		CLK high or low	3.3		
t_{su}	Setup time before clock	Dn (high or low)	2		ns
		CLRZ inactive (high)	0		
t_h	Hold time after clock	Dn (high or low)	0		ns

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP†	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.11		pF
		CLRZ		0.46		
		Dn		0.06		
		G		0.32		
C_o	Output capacitance			0.06		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	4.96		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Qn		0.59	1.59	3.52	0.62	1.59	3.22	ns
t_{PHL}				0.59	1.72	3.94	0.64	1.72	3.57	
t_{PHL}	CLRZ	Qn		0.33	0.79	2.7	0.34	0.79	2.25	ns
t_{PZH}	G	Y	R_L = 40 kΩ to GND	0.11	0.35	0.73	0.12	0.35	0.67	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.16	0.29	0.44	0.17	0.29	0.42	
t_{PHZ}	G	Y	R_L = 40 kΩ to GND	1.96	2.1	2.36	1.9	2.1	2.4	ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}	0.8	0.91	1.06	0.77	0.91	1.08	
Δt_{PLH}	CLK	Qn		0.77	2.14	4.64	0.82	2.14	4.27	ns/pF
Δt_{PHL}				0.51	1.33	2.76	0.55	1.33	2.54	
Δt_{PHL}	CLRZ	Qn		0.53	1.25	0.47	0.58	1.25	0.9	ns/pF
Δt_{PZH}	G	Qn		0.77	2.2	4.93	0.82	2.2	4.51	ns/pF
Δt_{PZL}				0.54	1.38	3.23	0.57	1.38	2.88	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

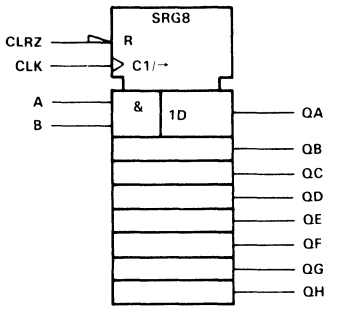
S164LJ 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

D3030, APRIL 1988

SOFTWARE MACRO

- **AND-Gated (Enable/Disable) Serial Inputs**
- **Buffered Clear and Serial Inputs**
- **Direct Clear**
- **Embedded Clock Drivers Provide Clock Buffering**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S164LJ software macro implements an 8-bit parallel-out shift register. These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data. Low level inputs inhibit entry of new data and reset the first flip-flop to a low level at the next clock pulse. A high level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock input.

The S164LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN210LJ	1.5	1	1.5	0.33
IV110LJ	0.75	1	0.75	0.16
IV140LJ	1.5	1	1.5	0.63
R2401LJ	23.5	2	47	9.06
TOTALS		5	50.75	10.18

When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

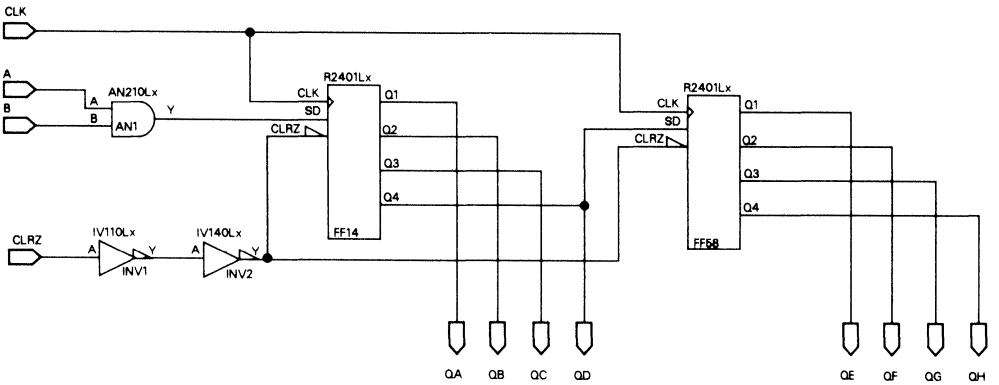
Label: S164LJ A,B,CLK,CLRZ,QA,QB,QC,QD,QE,QF,QG,QH;

D3030, APRIL 1988

FUNCTION TABLE

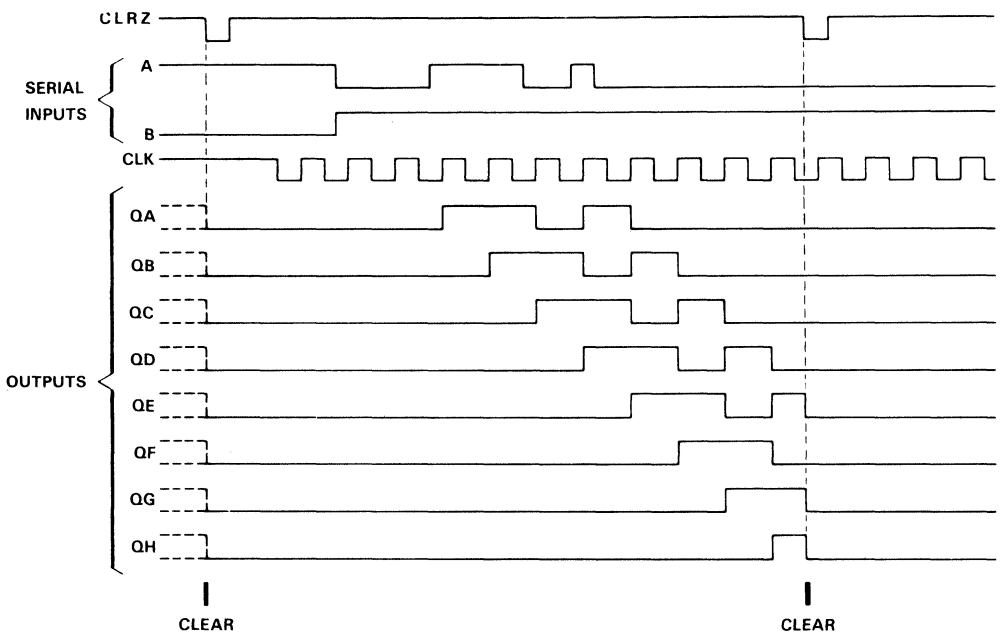
INPUTS				OUTPUTS		
CLR	CLK	A	B	QA	QB. . .QH	
L	X	X	X	L	L	L
H	L	X	X	QA_0	QB_0	QH_0
H	↑	H	H	H	QA_n	QG_n
H	↑	L	X	L	QA_n	QG_n
H	↑	X	L	L	QA_n	QG_n

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

typical clear, shift, and clear sequences



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	GZ		0.06		pF
		CLK		0.22		
		CLRZ		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	10.2		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Qn		1.5	3.3		1.5	3	ns
t_{PHL}				1.6	3.7		1.6	3.3	
t_{PHL}	CLRZ	Qn		1.5	3.3		1.5	3.1	ns
Δt_{PLH}	CLK	Qn	0.22	0.62	1.32	0.24	0.62	1.22	ns/pF
Δt_{PHL}			0.18	0.42	0.88	0.2	0.42	0.78	
Δt_{PHL}	CLRZ	Qn	0.18	0.4	0.86	0.2	0.4	0.78	ns/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

S164LJ
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

D3030, APRIL 1988

HDL FILE†

```
BLOCK S164LJ;
A       @INPUT;
B       @INPUT;
CLK     @INPUT;
CLRZ    @INPUT;
QA      @OUTPUT;
QB      @OUTPUT;
QC      @OUTPUT;
QD      @OUTPUT;
QE      @OUTPUT;
QF      @OUTPUT;
QG      @OUTPUT;
QH      @OUTPUT;

STRUCTURE
AN1     :AN210LJ   A,B,AN1O;
INV1    :IV110LJ   CLRZ,INV1O;
INV2    :IV140LJ   INV1O,INV2O;
FF14    :R2401LJ   INV2O,AN1O,CLK,QA,QB,QC,QD;
FF58    :R2401LJ   INV2O,QD,CLK,QE,QF,QG,QH;
END S164LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

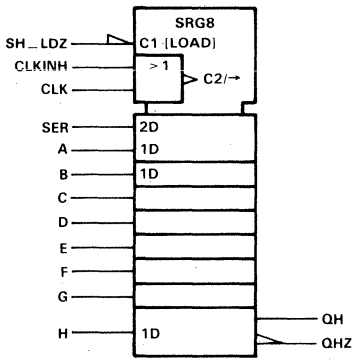
S165ALJ
PARALLEL-LOAD 8-BIT SHIFT REGISTER

D3030, APRIL 1988

SOFTWARE MACRO

- **Gated (Enable/Inhibit) Clock Inputs**
- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Clock Driver Provides Clock Buffering**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S165ALJ software macro implements an 8-bit parallel-in shift register. The S165ALJ is an 8-bit serial shift register that, when clocked, shifts the data toward serial output QH. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH_LDZ input. The S165ALJ also features a clock inhibit function and a complementary serial output QHZ. The S165ALJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
DFB20LJ	7.25	8	58	14.24
IV110LJ	1	8	6	1.68
IV140LJ	1.5	1	1.5	0.63
NA210LJ	1	16	16	3.04
OR240LJ	4	1	4	1.16
TOTALS		34	85.5	20.75

When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S165ALJ A,B,C,D,E,F,G,H,CLK,CLKINH,SH_LDZ,SER,QH,QHZ;

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

Clocking is accomplished by a low-to-high transition of the CLK input while SH_LDZ is held high and CLKINH is held low. The functions of the CLK and CLKINH (clock inhibit) inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLKINH will also accomplish clocking, CLKINH should be changed to the high level only while the CLK input is high. Parallel loading is inhibited when SH_LDZ is held high. The parallel inputs to the register are enabled while SH_LDZ is low independently of the levels of CLK, CLKINH, or SER inputs.

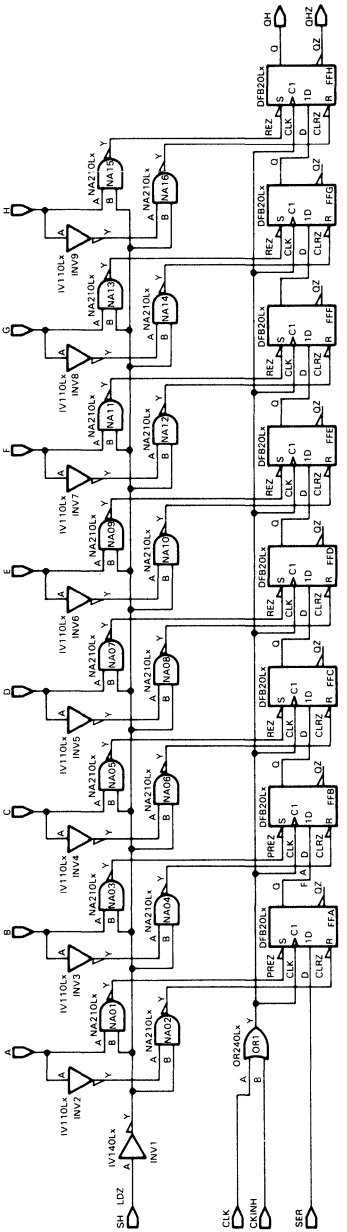
FUNCTION TABLE

INPUTS			FUNCTION
SH_LDZ	CLK	CLKINH	
L	X	X	Parallel load A thru H
H	H	X	No change
H	X	H	No change
H	L	↑	Shift
H	↑	L	Shift

Shift = Content of each internal register shifts toward serial output QH. Data at serial input is shifted into first register.

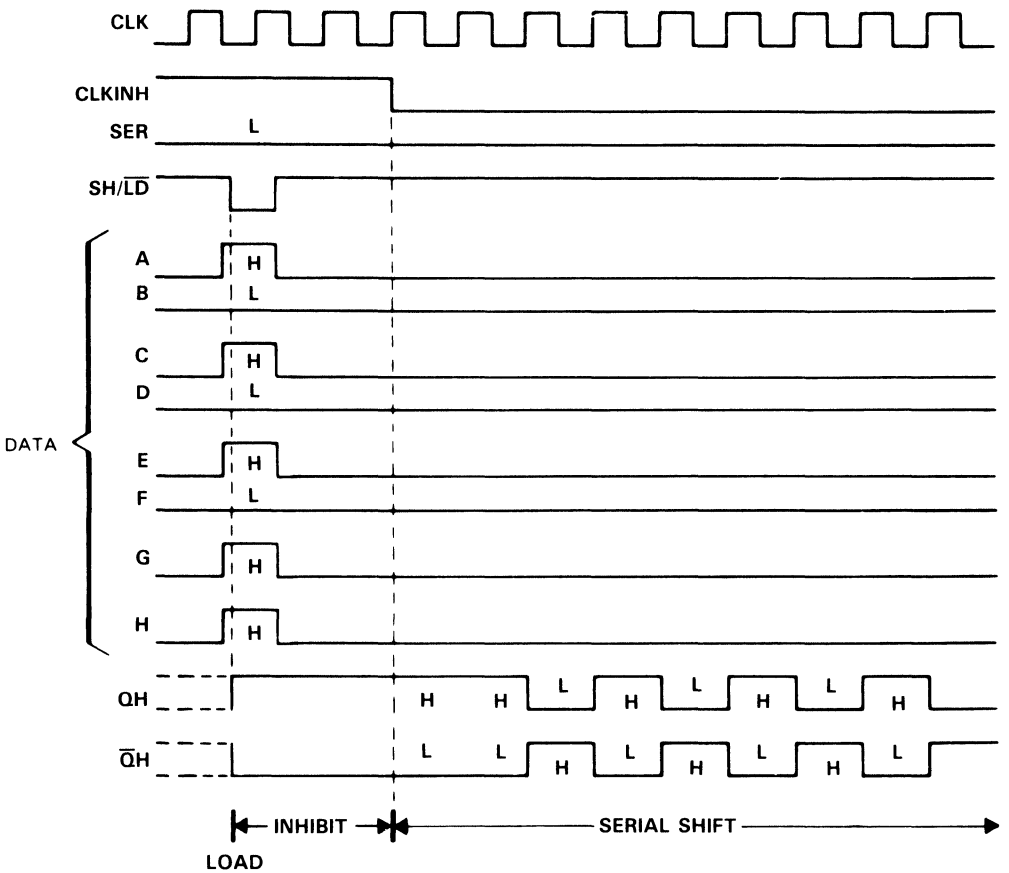
D3030, APRIL 1988

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

typical shift, load, and inhibit sequences



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A thru H		0.05		pF
		CLK, CLKINH		0.06		
		SER		0.05		
		SH_LDZ		0.35		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	18.8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	SH_LDZ	QH,QHZ		2.5	5.8		2.5	5.4	ns
t_{PHL}				2.1	3.9		2.1	3.7	
t_{PLH}	CLK	QH,QHZ		2.7	6.3		2.7	5.8	ns
t_{PHL}				2.1	4.8		2.1	4.4	
t_{PLH}	H	QH,QHZ		1.5	3		1.5	2.7	ns
t_{PHL}				1.5	3		1.5	2.7	
Δt_{PLH}	Any	Qn	0.16	0.56	1.18	0.2	0.56	1.1	ns/pF
Δt_{PHL}			0.14	0.36	0.78	0.16	0.36	0.7	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE†

```
BLOCK S165ALJ;
A          @INPUT;
B          @INPUT;
C          @INPUT;
D          @INPUT;
E          @INPUT;
F          @INPUT;
G          @INPUT;
H          @INPUT;
CLK        @INPUT;
CLKINH     @INPUT;
SH_LDZ     @INPUT;
SER        @INPUT;
QH         @OUTPUT;
QHZ        @OUTPUT;
STRUCTURE
FFA        :DFB20LJ   NA02O,NA01O,SER,OR1O,FFAQ,DUM;
FFB        :DFB20LJ   NA04O,NA03O,FFAQ,OR1O,FFBQ,DUM;
FFC        :DFB20LJ   NA06O,NA05O,FFBQ,OR1O,FFCQ,DUM;
FFD        :DFB20LJ   NA08O,NA07O,FFCQ,OR1O,FFDQ,DUM;
FFE        :DFB20LJ   NA10O,NA09O,FFDQ,OR1O,FFEQ,DUM;
FFF        :DFB20LJ   NA12O,NA11O,FFEQ,OR1O,FFFQ,DUM;
FFG        :DFB20LJ   NA14O,NA13O,FFFQ,OR1O,FFGQ,DUM;
FFH        :DFB20LJ   NA16O,NA15O,FFGQ,OR1O,QH,QHZ;
INV1       :IV140LJ   SH_LDZ,INV1O;
INV2       :IV110LJ;  A,INV2O;
INV3       :IV110LJ   B,INV3O;
INV4       :IV110LJ   C,INV4O;
INV5       :IV110LJ   D,INV5O;
INV6       :IV110LJ   E,INV6O;
INV7       :IV110LJ   F,INV7O;
INV8       :IV110LJ   G,INV8O;
INV9       :IV110LJ   H,INV9O;
NA01       :NA210LJ   A,INV1O,NA01O;
NA02       :NA210LJ   INV2O,INV1O,NA02O;
NA03       :NA210LJ   B,INV1O,NA03O;
NA04       :NA210LJ   INV3O,INV1O,NA04O;
NA05       :NA210LJ   C,INV1O,NA05O;
NA06       :NA210LJ   INV4O,INV1O,NA06O;
NA07       NA210LJ    D,INV1O,NA07O;
NA08       :NA210LJ   INV5O,INV1O,NA08O;
NA09       :NA210LJ   E,INV1O,NA09O;
NA10       :NA210LJ   INV6O,INV1O,NA10O;
NA11       :NA210LJ   F,INV1O,NA11O;
NA12       :NA210LJ   INV7O,INV1O,NA12O;
NA13       :NA210LJ   G,INV1O,NA13O;
NA14       :NA210LJ   INV8O,INV1O,NA14O;
NA15       :NA210LJ   H,INV10,NA15O;
NA16       :NA210LJ   INV9O,INV1O,NA16O;
OR1        :OR240LJ   CLK,CLKINH,OR1O:
END S165ALJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

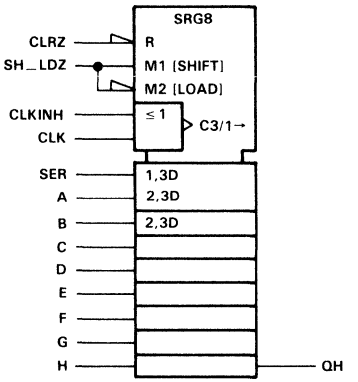
S166LJ
PARALLEL-LOAD 8-BIT SHIFT REGISTER WITH DIRECT CLEAR

D3030, APRIL 1988

SOFTWARE MACRO

- **Synchronous Parallel Load**
- **Direct Overriding Clear**
- **Parallel-to-Serial Conversion**
- **Direct Clear**
- **Embedded Clock Drivers Provide Clock Buffering**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S166LJ software macro implements an 8-bit parallel-in shift register. The S166LJ is an 8-bit serial shift register that, when clocked, shifts the data toward serial output QH. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH_LDZ input. The S166LJ also features a clock inhibit function and a direct clear input. The S166LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AO221LJ	1.75	8	14	1.76
IV110LJ	0.75	9	6.75	1.44
IV120LJ	1	2	2	0.62
IV140LJ	1.5	1	1.5	0.63
OR210LJ	1.25	1	1.25	0.37
R2405LJ	20.5	2	41	9.24
TOTALS		23	66.5	14.06

When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S166LJ A,B,C,D,E,F,G,H,CLK,CLKINH,SER,SH_LDZ,CLRZ,QH;

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S166LJ
PARALLEL-LOAD 8-BIT SHIFT REGISTER WITH DIRECT CLEAR

D3030, ARPIL 1988

The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse input. When the shift-load input is low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse input. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate that permits one input to perform as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A direct clear input, when taken low, overrides all other inputs, including the clock, and resets all flip-flops to zero.

FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLRZ	SH_LDZ	CLKINH	CLK	SER	A. . .H	QA	QB	QH
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	QA_0	QB_0	QH_0
H	L	L	↑	X	a. . .h	a	b	h
H	H	L	↑	H	X	H	QA_n	QG_n
H	H	L	↑	L	X	L	QA_n	QG_n
H	X	H	↑	X	X	QA_0	QB_0	QH_0

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

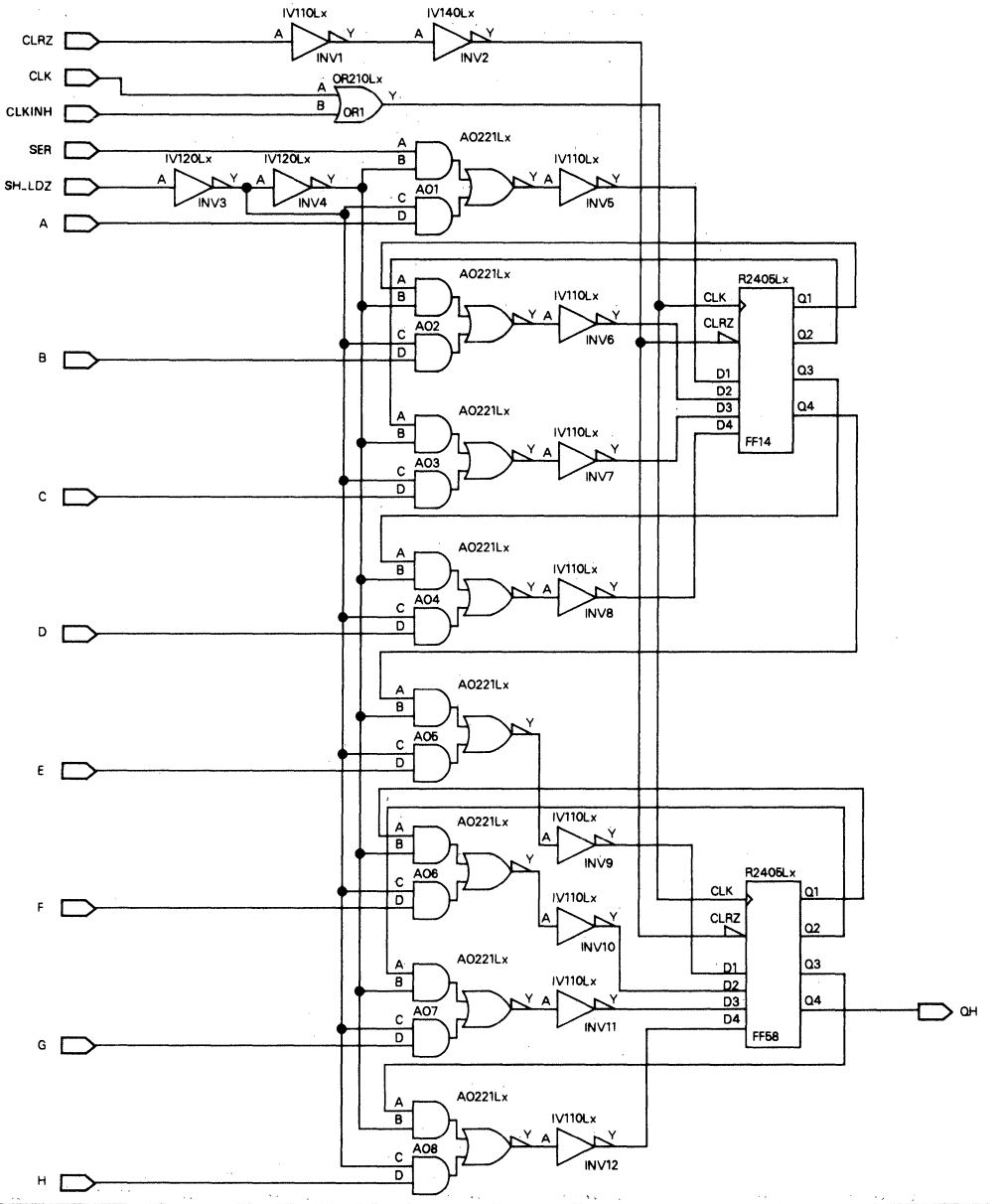
timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

S166LJ
PARALLEL-LOAD 8-BIT SHIFT REGISTER WITH DIRECT CLEAR

D3030, APRIL 1988

logic diagram

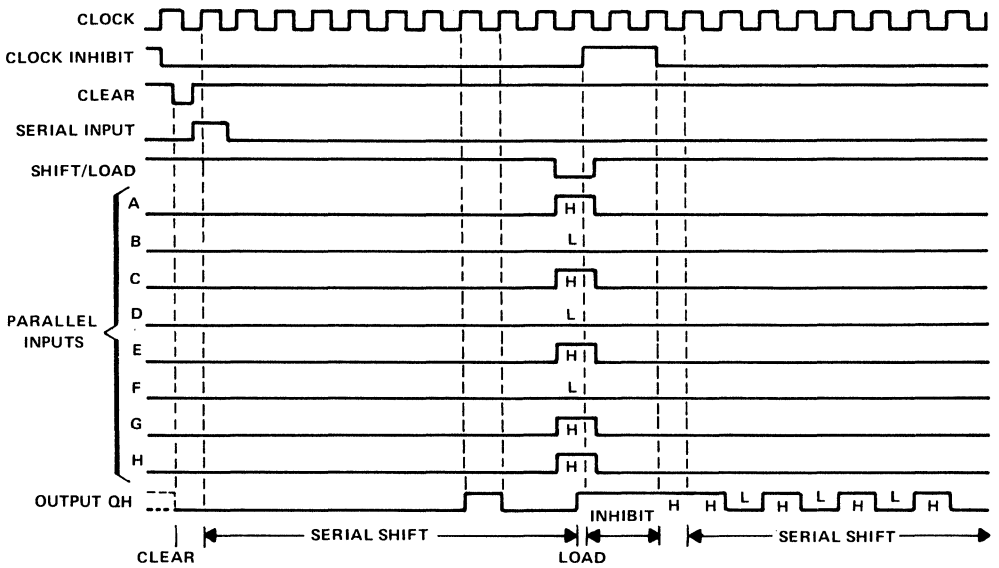


TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S166LJ
PARALLEL-LOAD 8-BIT SHIFT REGISTER WITH DIRECT CLEAR

D3030, APRIL 1988

typical shift, load, and inhibit sequences



electrical characateristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A thru H		0.06		pF
		CLK, CLKINH		0.06		
		SER		0.06		
		SH_LDZ		0.11		
		CLRZ		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	14.1		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	QH		2.3	5		2.3	4.6	ns
t_{PHL}				2.5	5.5		2.5	5	
t_{PHL}	CLRZ	QH		1.7	3.2		1.7	3.1	ns
Δt_{PLH}	Any	QH	0.42	1.06	2.24	0.44	1.06	2.04	ns/pF
Δt_{PHL}			0.34	0.78	1.58	0.36	0.78	1.4	
Δt_{PHL}	CLRZ	QH	0.34	0.76	1.54	0.36	0.76	1.4	ns/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S166LJ
PARALLEL-LOAD 8-BIT SHIFT REGISTER WITH DIRECT CLEAR

D3030, APRIL 1988

HDL FILE†

```
BLOCK S166LJ;
A          @INPUT;
B          @INPUT;
C          @INPUT;
D          @INPUT;
E          @INPUT;
F          @INPUT;
G          @INPUT;
H          @INPUT;
CLK        @INPUT;
CLKINH     @INPUT;
SER        @INPUT;
SH_LDZ     @INPUT;
CLRZ       @INPUT;
QH         @OUTPUT;
STRUCTURE
AO1        :AO221LJ   SER,INV4O,INV3O,A,AO1O;
AO2        :AO221LJ   QA,INV4O,INV3O,B,AO2O;
AO3        :AO221LJ   QB,INV4O,INV3O,C,AO3O;
AO4        :AO221LJ   QC,INV4O,INV3O,D,AO4O;
AO5        :AO221LJ   QD,INV4O,INV3O,E,AO5O;
AO6        :AO221LJ   QE,INV4O,INV3O,F,AO6O;
AO7        :AO221LJ   QF,INV4O,INV3O,G,AO7O;
AO8        :AO221LJ   QG,INV4O,INV3O,H,AO8O;
FF14       :R2405LJ   INV2O,INV5O,INV6O,INV7O,
                      INV8O,OR1O,QA,QB,QC,QD;
FF58       :R2405LJ   INV2O,INV9O,INV10O,INV11O,
                      INV12O,OR1O,QE,QF,QG,QH;
INV1       :IV110LJ   CLRZ,INV1O;
INV10      :IV110LJ   AO6O,INV10O;
INV11      :IV110LJ   AO7O,INV11O;
INV12      :IV110LJ   AO8O,INV12O;
INV2       :IV140LJ   INV1O,INV2O;
INV3       :IV120LJ   SH_LDZ,INV3O;
INV4       :IV120LJ   INV3O,INV4O;
INV5       :IV110LJ   AO1O,INV5O;
INV6       :IV110LJ   AO2O,INV6O;
INV7       :IV110LJ   AO3O,INV7O;
INV8       :IV110LJ   AO4O,INV8O;
INV9       :IV110LJ   AO5O,INV9O;
OR1        :OR210LJ   CLK,CLKINH,OR1O;
END S166LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

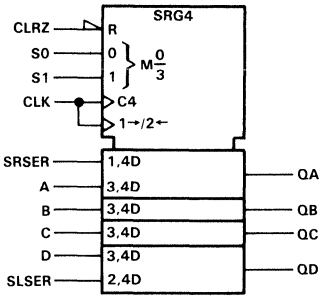
S194ALJ
BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

D3030, APRIL 1988

SOFTWARE MACRO

- **Parallel Inputs and Outputs**
- **Four Operating Modes:**
  - **Synchronous Parallel Load**
  - **Right Shift**
  - **Left Shift**
  - **Do Nothing**
- **Positive Edge-Triggered Clocking**
- **Embedded Clock Drivers Provide Clock Buffering**
- **Direct Overriding Clear**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S194ALJ software macro implements a 4-bit parallel-in/parallel-out bidirectional, universal shift register. The 4-bit length simplifies construction of large registers. These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit features parallel inputs, parallel outputs, right-shift and left-shift inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation:

Inhibit clocking (do nothing)
Shift right (in the direction QA toward QD)
Shift left (in the direction QD toward QA)
Parallel loading

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. When both mode control inputs are low, a free-running clock will reload the present state of each flip-flop on each clock transition to implement the do-nothing mode.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S194ALJ
BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

The S194ALJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV110LJ	0.75	1	0.75	0.16
IV120LJ	1	4	4	1.24
IV140LJ	1.5	1	1.5	0.63
NA310LJ	1.25	16	20	3.04
NA410LJ	1.5	4	6	0.76
R2405LJ	20.5	1	20.5	4.62
TOTALS		27	52.75	10.45

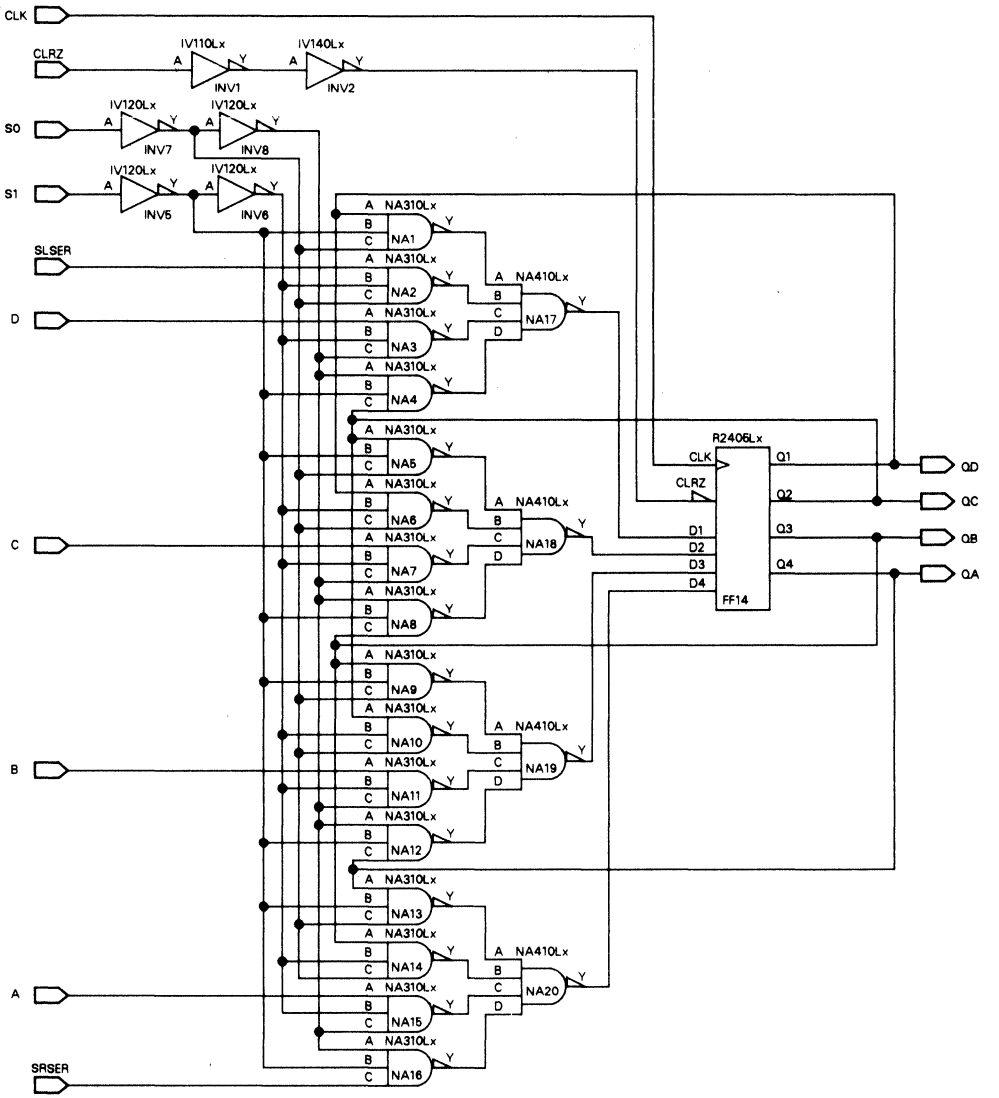
When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S194ALJ A,B,C,D,SRSER,SLSER,CLK,CLRZ,S1,S0,QA,QB,QC,QD;

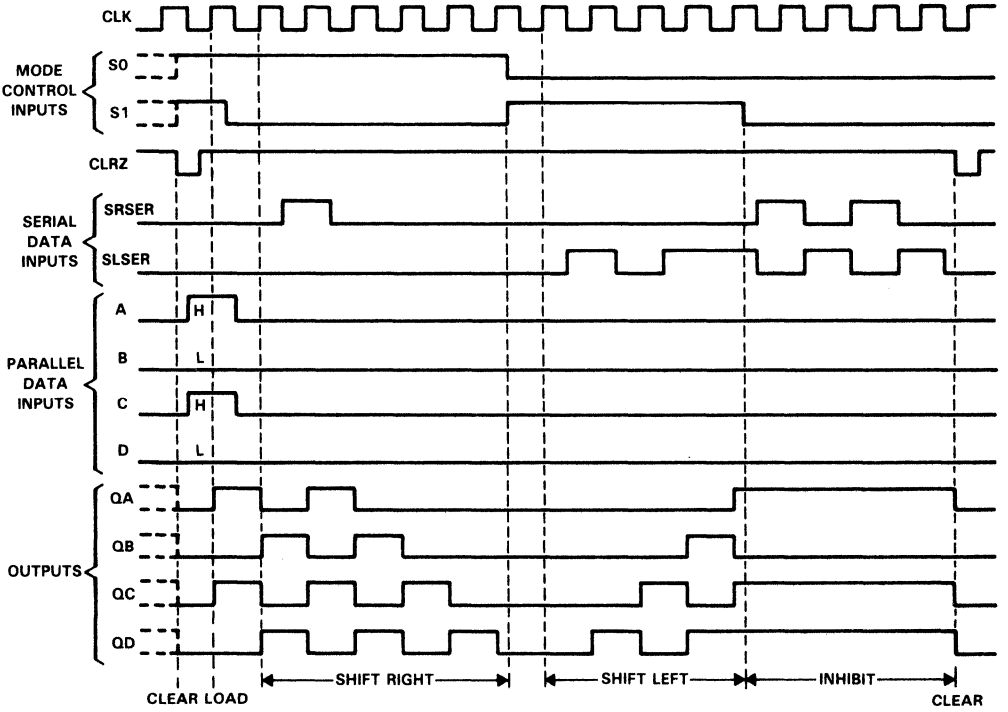
FUNCTION TABLE

INPUTS										OUTPUTS			
	MODE			SERIAL		PARALLEL							
CLRZ	S1	S0	CLK	SLSER	SRSER	A	B	C	D	QA	QB	QC	QD
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	QA_0	QB_0	QC_0	QD_0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QA_n	QB_n	QC_n
H	L	H	↑	X	L	X	X	X	X	L	QA_n	QB_n	QC_n
H	H	L	↑	H	X	X	X	X	X	QB_n	QC_n	QD_n	H
H	H	L	↑	L	X	X	X	X	X	QB_n	QC_n	QD_n	L
H	L	L	X	X	X	X	X	X	X	QA_0	QB_0	QC_0	QD_0

logic diagram



typical clear, load, right-shift, left-shift, inhibit, and clear sequences



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK, S0, S1		0.11		pF
		All other inputs		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	10.5		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Qn		1.6	3.4		1.6	3.2	ns
t_{PHL}				1.7	3.8		1.7	3.5	
t_{PHL}	CLRZ	Qn		1.8	3.3		1.8	3.1	ns
Δt_{PLH}	CLK	Qn	0.42	1.06	2.24	0.44	1.06	2.04	ns/pF
Δt_{PHL}			0.34	0.78	1.58	0.36	0.78	1.4	
Δt_{PHL}	CLRZ	Qn	0.34	0.76	1.54	0.36	0.76	1.4	ns/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S194ALJ
BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

D3030, APRIL 1988

HDL FILE†

```
BLOCK S194ALJ;
A          @INPUT;
B          @INPUT;
C          @INPUT;
D          @INPUT;
SRSER      @INPUT;
SLSER      @INPUT;
CLK        @INPUT;
CLRZ       @INPUT;
S1         @INPUT;
S0         @INPUT;
QA         @OUTPUT;
QB         @OUTPUT;
QC         @OUTPUT;
QD         @OUTPUT;
STRUCTURE
FF14       :R2405LJ   INV2O,NA17O,NA18O,NA19O,
                      NA20O,CLK,QD,QC,QB,QA;
INV1       :IV110LJ   CLRZ,INV1O;
INV2       :IV140LJ   INV1O,INV2O;
INV5       :IV120LJ   S1,INV5O;
INV6       :IV120LJ   INV5O,INV6O;
INV7       :IV120LJ   S0,INV7O;
INV8       :IV120LJ   INV7O,INV8O;
NA1        :NA310LJ   QD,INV5O,INV7O,NA1O;
NA10       :NA310LJ   QC,INV6O,INV7O,NA10O;
NA11       :NA310LJ   B,INV6O,INV8O,NA11O;
NA12       :NA310LJ   INV8O,INV5O,QA,NA12O;
NA13       :NA310LJ   QA,INV5O,INV7O,NA13O;
NA14       :NA310LJ   QB,INV6O,INV7O,NA14O;
NA15       :NA310LJ   A,INV6O,INV8O,NA15O;
NA16       :NA310LJ   INV8O,INV5O,SRSER,NA16O;
NA17       :NA410LJ   NA1O,NA2O,NA3O,NA4O,NA17O;
NA18       :NA410LJ   NA5O,NA6O,NA7O,NA8O,NA18O;
NA19       :NA410LJ   NA9O,NA10O,NA11O,NA12O,NA19O;
NA2        :NA310LJ   SLSER,INV6O,INV7O,NA2O;
NA20       :NA410LJ   NA13O,NA14O,NA15O,NA16O,NA20O;
NA3        :NA310LJ   D,INV6O,INV8O,NA3O;
NA4        :NA310LJ   INV8O,INV5O,QC,NA4O;
NA5        :NA310LJ   QC,INV5O,INV7O,NA5O;
NA6        :NA310LJ   QD,INV6O,INV7O,NA6O;
NA7        :NA310LJ   C,INV6O,INV8O,NA7O;
NA8        :NA310LJ   INV8O,INV5O,QB,NA8O;
NA9        :NA310LJ   QB,INV5O,INV7O,NA9O;
End S194ALJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

S195ALJ
4-BIT PARALLEL-ACCESS SHIFT REGISTER

D3030, APRIL 1988

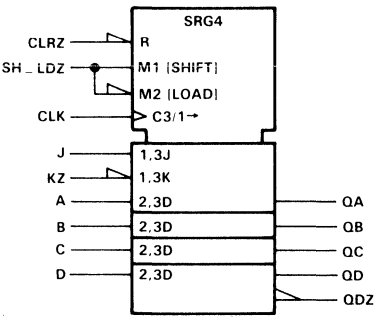
SOFTWARE MACRO

- **Synchronous Parallel Load**
- **Positive-Edge-Triggered Clocking**
- **J and KZ Inputs to First Stage**
- **Complementary Outputs from Last Stage**
- **Embedded Clock Drivers Provide Clock Buffering**

description

The S195ALJ software macro implements a 4-bit parallel-out shift register. These 4-bit registers feature parallel inputs, parallel outputs, J-KZ serial inputs, shift-load control input, and a direct overriding clear. The registers have two modes of operation: parallel load and shift (in the direction QA toward QD). The S195ALJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV110LJ	0.75	1	0.75	0.16
IV120LJ	1	2	2	0.62
IV140LJ	1.5	1	1.5	0.63
NA210LJ	1	10	10	1.9
NA310LJ	1.25	3	3.75	0.57
R2406LJ	23.5	1	23.5	5.16
TOTALS		18	41.5	9.04

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

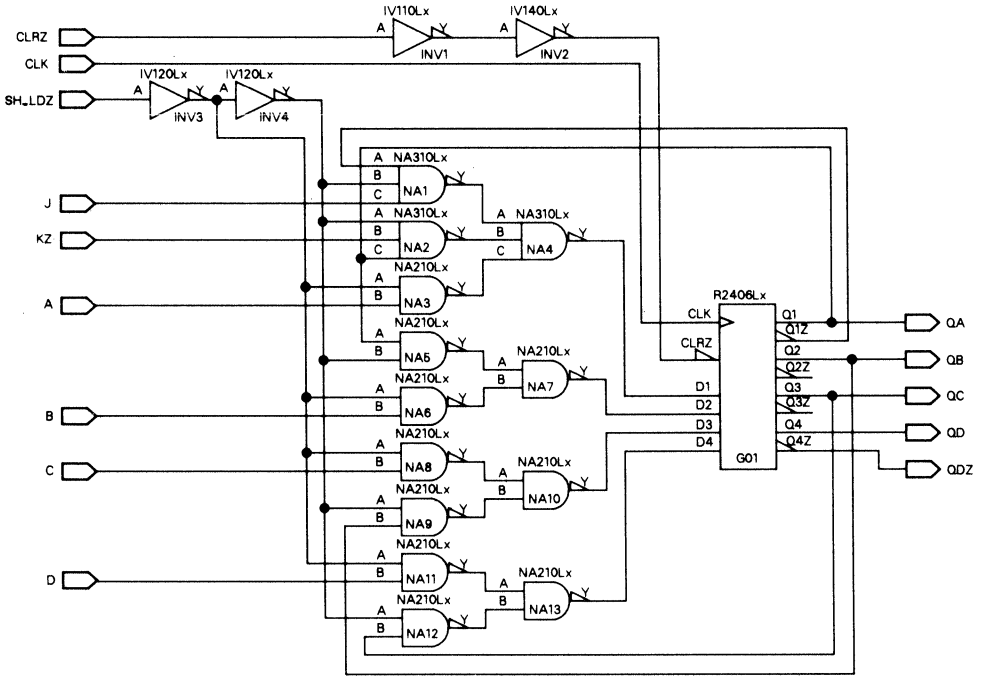
When the register is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S195ALJ CLRZ,CLK,SH_LDZ,J,KZ,A,B,C,D,QA,QB,QC,QD,QDZ;

Parallel loading is accomplished by applying the four bits of data and taking the shift-load control (SH_LDZ) input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock (CLK) input. During loading, serial data flow is inhibited. Shifting is accomplished synchronously when the shift-load control input is high. Serial data for this mode is entered at the J-KZ inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

D3030, APRIL 1988

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

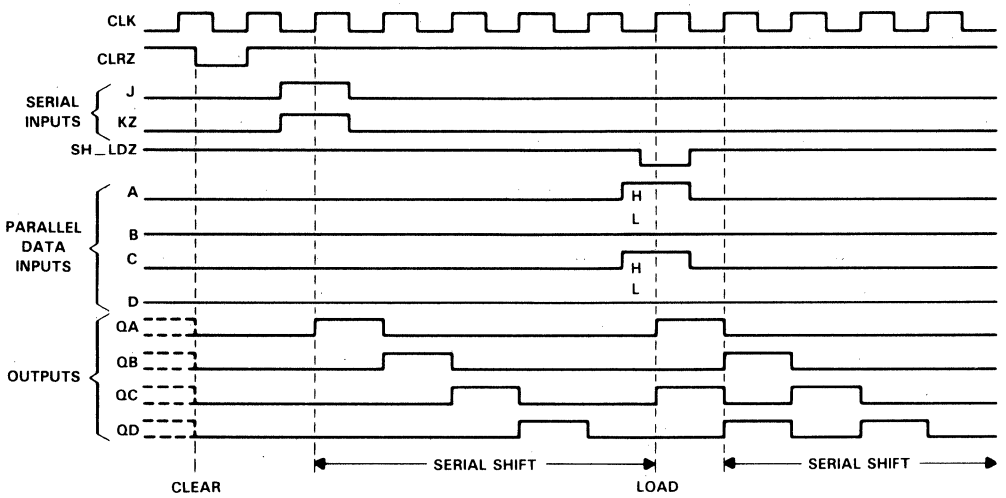
S195ALJ
4-BIT PARALLEL-ACCESS SHIFT REGISTER

D3030, ARPIL 1988

FUNCTION TABLE

INPUTS									OUTPUTS				
			SERIAL		PARALLEL								
CLRZ	SH_LDZ	CLK	J	KZ	A	B	C	D	QA	QB	QC	QD	QDZ
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	d
H	H	L	X	X	X	X	X	X	QA_0	QB_0	QC_0	QD_0	QD_0
H	H	↑	L	H	X	X	X	X	QA_0	QA_0	QB_n	QC_n	QC_n
H	H	↑	L	L	X	X	X	X	L	QA_n	QB_n	QC_n	QC_n
H	H	↑	H	H	X	X	X	X	H	QA_n	QB_n	QC_n	QC_n
H	H	↑	H	L	X	X	X	X	QA_n	QA_n	QB_n	QC_n	QC_n

typical clear, shift, and load sequences



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK, SH_LDZ		0.11		pF
		All other inputs		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	9.04		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Qn		1.5	3.3		1.5	3	ns
t_{PHL}				1.7	3.5		1.7	3.4	
t_{PLH}	CLK	QDZ		1.8	3.9		1.8	3.5	ns
t_{PHL}				1.7	3.8		1.7	3.5	
t_{PHL}	CLRZ	Qn		1.7	3.3		1.7	3	ns
t_{PLH}	CLRZ	QDZ		1	1.8		1	1.7	ns
Δt_{PLH}	Any	Qn,QDZ	0.4	1.12	2.32	0.42	1.12	2.12	ns/pF
Δt_{PHL}			0.28	0.76	1.54	0.3	0.76	1.4	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

S195ALJ
4-BIT PARALLEL-ACCESS SHIFT REGISTER

HDL FILE†

```
BLOCK S195ALJ;
CLRZ        @INPUT;
CLK         @INPUT;
SH_LDZ      @INPUT;
J           @INPUT;
KZ          @INPUT;
A           @INPUT;
B           @INPUT;
C           @INPUT;
D           @INPUT;
QA          @OUTPUT;
QB          @OUTPUT;
QC          @OUTPUT;
QD          @OUTPUT;
QDZ         @OUTPUT;

STRUCTURE
INV1        :IV110LJ    CLRZ,CLR;
INV2        :IV140LJ    CLR,CLRZ1;
INV3        :IV120LJ    SH_LDZ,SHLDZ;
INV4        :IV120LJ    SHLDZ,SHLD1;
NA1         :NA310LJ    QAZ,SHLD1,J,S1;
NA10        :NA210LJ    S8,S9,S10;
NA11        :NA210LJ    SHLDZ,D,S11;
NA12        :NA210LJ    SHLD1,QC,S12;
NA13        :NA210LJ    S11,S12,S13;
NA2         :NA310LJ    SHLD1,KZ,QA,S2;
NA3         :NA210LJ    SHLDZ,A,S3;
NA4         :NA310LJ    S1,S2,S3,S4;
NA5         :NA210LJ    QA,SHLD1,S5;
NA6         :NA210LJ    SHLDZ,B,S6;
NA7         :NA210LJ    S5,S6,S7;
NA8         :NA210LJ    SHLDZ,C,S8;
NA9         :NA210LJ    SHLD1,QB,S9;
G01         :R2406LJ    CLRZ1,S4,S7,S10,S13,CLK,QA,QAZ,QB,DUM,
                        QC,DUM,QD,QDZ;
END S195ALJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

S299LJ
8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTER

D3030, APRIL 1988

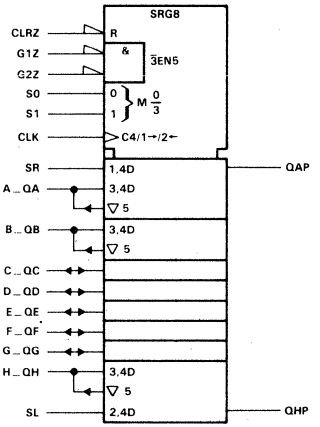
SOFTWARE MACRO

- Ported 3-State Inputs/Outputs Simplify Implementation of:
  - Single/Multiple Push/Pop Stack
  - Multiple/Supplementary Accumulator
  - Bus Storage/Shift Register
- Four Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Left Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Embedded Clock Drivers Provide Clock Buffering

description

The S299LJ software macro implements an 8-bit parallel-in/parallel-out bidirectional, universal shift/storage register. The 8-bit length simplifies construction of large registers. These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit features parallel inputs, parallel outputs, right-shift and left-shift inputs, operating-mode-control inputs, and a direct overriding clear line.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S299LJ
8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTER

D3030, APRIL 1988

The S299LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN210LJ	1.5	1	1.5	0.33
IV110LJ	0.75	2	1.5	0.32
IV140LJ	1.5	4	6	2.52
IV222LJ	2	8	16	3.04
NA310LJ	1.25	32	40	6.08
NA410LJ	1.5	8	12	1.52
NO330LJ	3	1	3	0.35
R2406LJ	24.5	2	47	10.32
TOTALS		58	127	24.48

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S299LJ S0,S1,G1Z,G2Z,SL,SR,CLK,CLRZ,QAP,QHP,
A_QA,B_QB,C_QC,D_QD,E_QE,F_QF,G_QG,H_QH;

The S299LJ register has four distinct modes of operation;

Parallel loading
Shift right (in the direction QA toward QH)
Shift left (in the direction QH toward QA)
Inhibit clocking (do nothing)

Synchronous parallel loading is accomplished by taking either output control input, G1Z or G2Z, high and applying the eight bits of data while both mode-control inputs, S0 and S1, are high. The data are loaded into the associated flip-flops on the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the right-shift data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. When both mode-control inputs are low, a free-running clock will reload the present state of each flip-flop on each clock transition to implement the do-nothing mode.

S299LJ
8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTER

D3030, APRIL 1988

FUNCTION TABLE

INPUTS								I/O PORTS								OUTPUTS	
	MODE		OUTPUT CONTROLS			SERIAL											
CLRZ	S1	S0	G1Z†	G2Z†	CLK	SL	SR	AQA	BQB	CQC	DQD	EQE	FQF	GQG	HQH	QAP	QHP
L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
H	L	L	L	L	X	X	X	QA_0	QB_0	QC_0	QD_0	QE_0	QF_0	QG_0	QH_0	QA_0	QH_0
H	X	X	L	L	L	X	X	QA_0	QB_0	QC_0	QD_0	QE_0	QF_0	QG_0	QH_0	QA_0	QH_0
H	L	H	L	L	↑	X	H	H	QA_n	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	H	QG_n
H	L	H	L	L	↑	X	L	L	QA_n	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	L	QG_n
H	H	L	L	L	↑	H	X	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	QH_n	H	QB_n	H
H	H	L	L	L	↑	L	X	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	QH_n	L	QB_n	L
H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

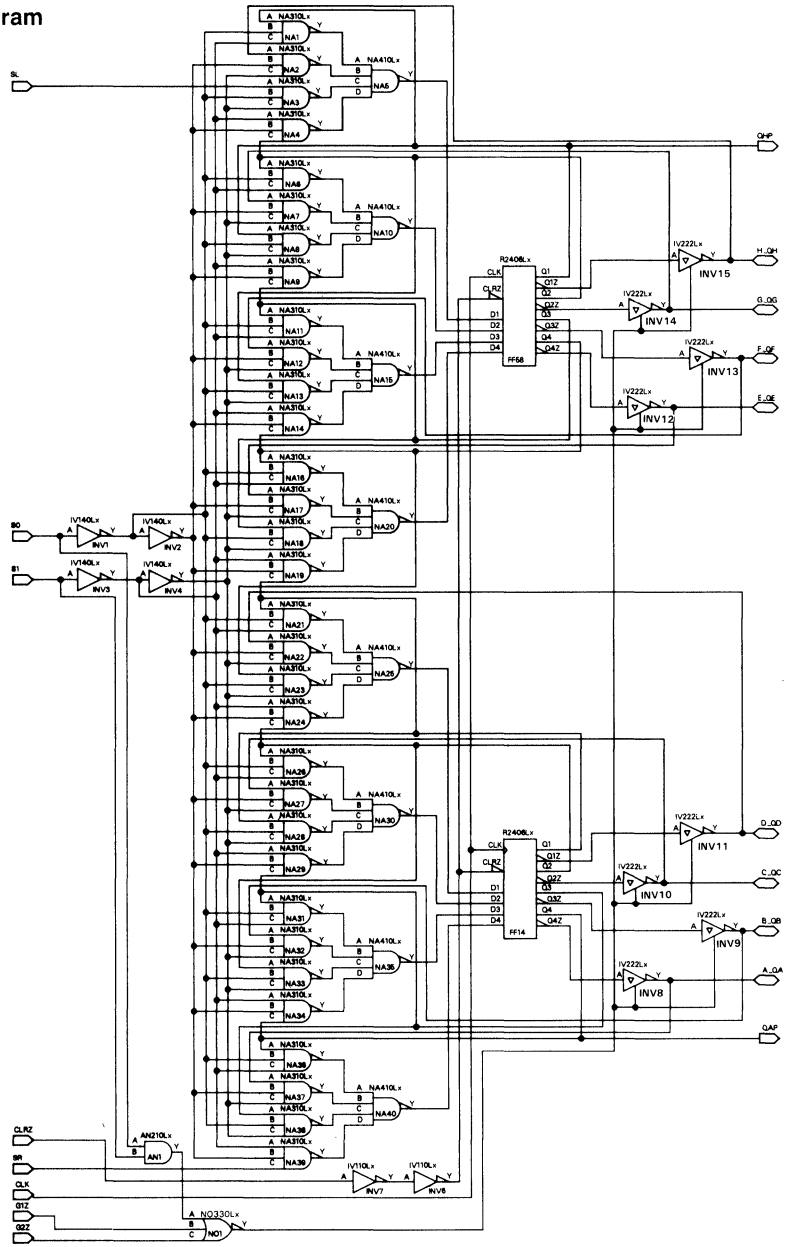
† When one or both output controls are high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. a. . .h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S299LJ
8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTER

D3030, APRIL 1988

logic diagram



S299LJ
8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTER

D3030, APRIL 1988

absolute maximum ratings and recommended conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.22		pF
		G1Z, G2Z		0.11		
		S0, S1		0.28		
		A_QA. .H_QH		0.05		
		All other inputs		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	24.48		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Notes 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Qn		2.3	5		2.3	4.6	ns
t_{PHL}				2.4	5.3		2.4	4.7	
t_{PHL}	CLRZ	Qn		2.4	4.3		2.4	3.9	ns
t_{PLH}	CLK	QAP,QHP		1.5	3.3		1.5	3	ns
t_{PHL}				1.7	3.8		1.7	3.4	
t_{PHL}	CLRZ	QAP,QHP		2.3	4.3		2.3	4	ns
t_{PZH}	GnZ	Qn		3.3	5.3		3.3	4.9	ns
t_{PZL}				3.1	5		3.1	4.6	
Δt_{PLH}	Any	Any	0.34	1	2.22	0.34	1	2.06	ns/pF
Δt_{PHL}			0.26	0.6	1.34	0.28	0.6	1.2	
Δt_{PZH}	GnZ	Qn	0.34	1.02	2.26	0.38	1.02	2.08	ns/pF
Δt_{PZL}			0.38	0.64	1.36	0.38	0.64	1.2	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

2. Enable and delta-enable times are measured using the conditions specified for the S2406LJ.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S299LJ
8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTER

D3030, APRIL 1988

HDL FILE†

```
BLOCK S299LJ;
S0          @INPUT;
S1          @INPUT;
G1Z         @INPUT;
G2Z         @INPUT;
SL          @INPUT;
SR          @INPUT;
CLK         @INPUT;
CLRZ        @INPUT;
QAP         @OUTPUT;
QHP         @OUTPUT;
A_QA        @INOUT;
B_QB        @INOUT;
C_QC        @INOUT;
D_QD        @INOUT;
E_QE        @INOUT;
F_QF        @INOUT;
G_QG        @INOUT;
H_QH        @INOUT;

STRUCTURE
AN1         :AN210LJ    S0,S1,AN1O;
INV1        :IV140LJ    S0,INV1O;
INV10       :IV222LJ    CN,NO1O,C_QC;
INV11       :IV222LJ    DN,NO1O,D_QD;
INV12       :IV222LJ    EN,NO1O,E_QE;
INV13       :IV222LJ    FN,NO1O,F_QF;
INV14       :IV222LJ    GN,NO1O,G_QG;
INV15       :IV222LJ    HN,NO1O,H_QH;
INV2        :IV140LJ    INV1O,INV2O;
INV3        :IV140LJ    S1,INV3O;
INV4        :IV140LJ    INV3O,INV4O;
INV6        :IV110LJ    INV7O,INV6O;
INV7        :IV110LJ    CLRZ,INV7O;
INV8        :IV222LJ    AN,NO1O,A_QA;
INV9        :IV222LJ    BN,NO1O,B_QB;
NA1         :NA310LJ    QHP,INV1O,INV3O,NA1O;
NA10        :NA410LJ    NA6O,NA7O,NA8O,NA9O,NA10O;
NA11        :NA310LJ    FP,INV1O,INV3O,NA11O;
NA12        :NA310LJ    F_QF,INV2O,INV4O,NA12O;
NA13        :NA310LJ    GP,INV1O,INV4O,NA13O;
NA14        :NA310LJ    INV3O,INV2O,EP,NA14O;
NA15        :NA410LJ    NA11O,NA12O,NA13O,NA14O,NA15O;
NA16        :NA310LJ    EP,INV1O,INV3O,NA16O;
NA17        :NA310LJ    E_QE,INV2O,INV4O,NA17O;
NA18        :NA310LJ    FP,INV1O,INV4O,NA18O;
NA19        :NA310LJ    INV3O,INV2O,DP,NA19O;
NA2         :NA310LJ    H_QH,INV2O,INV4O,NA2O;
NA20        :NA410LJ    NA16O,NA17O,NA18O,NA19O,NA20O;
NA21        :NA310LJ    DP,INV1O,INV3O,NA21O;
NA22        :NA310LJ    D_QD,INV2O,INV4O,NA22O;
NA23        :NA310LJ    EP,INV1O,INV4O,NA23O;
NA24        :NA310LJ    INV3O,INV2O,CP,NA24O;
NA25        :NA410LJ    NA21O,NA22O,NA23O,NA24O,NA25O;
NA26        :NA310LJ    CP,INV1O,INV3O,NA26O;
NA27        :NA310LJ    C_QC,INV2O,INV4O,NA27O;
NA28        :NA310LJ    DP,INV1O,INV4O,NA28O;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

HDL FILE† - Continued

```
NA29      :NA310LJ  INV3O,INV2O,BP,NA29O;
NA3       :NA310LJ  SL,INV1O,INV4O,NA3O;
NA30      :NA410LJ  NA26O,NA27O,NA28O,NA29O,NA30O;
NA31      :NA310LJ  BP,INV1O,INV3O,NA31O;
NA32      :NA310LJ  B_QB,INV2O,INV4O,NA32O;
NA33      :NA310LJ  CP,INV1O,INV4O,NA33O;
NA34      :NA310LJ  INV3O,INV2O,QAP,NA34O;
NA35      :NA410LJ  NA31O,NA32O,NA33O,NA34O,NA35O;
NA36      :NA310LJ  QAP,INV1O,INV3O,NA36O;
NA37      :NA310LJ  A_QA,INV2O,INV4O,NA37O;
NA38      :NA310LJ  BP,INV1O,INV4O,NA38O;
NA39      :NA310LJ  INV3O,INV2O,SR,NA39O;
NA4       :NA310LJ  INV3O,INV2O,GP,NA4O;
NA40      :NA410LJ  NA36O,NA37O,NA38O,NA39O,NA40O;
NA5       :NA410LJ  NA1O,NA2O,NA3O,NA4O,NA5O;
NA6       :NA310LJ  GP,INV1O,INV3O,NA6O;
NA7       :NA310LJ  G_QG,INV2O,INV4O,NA7O;
NA8       :NA310LJ  QHP,INV1O,INV4O,NA8O;
NA9       :NA310LJ  INV3O,INV2O,FP,NA9O;
NO1       :NO330LJ  AN1O,G1Z,G2Z,NO1O;
FF14      :R2406LJ  INV6O,NA25O,NA30O,NA35O,NA40O,CLK,
                    DP,DN,CP,CN,BP,BN,QAP,AN;
FF58      :R2406LJ  INV6O,NA5O,NA10O,NA15O,NA20O,
                    CLK,QHP,HN,GP,GN,FP,FN,EP,EN;
END S299LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

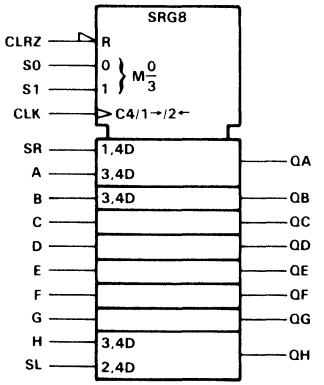
S299XLJ
8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

D3030, APRIL 1988

SOFTWARE MACRO

- **Parallel Inputs and Outputs**
- **Four Operating Modes:**
  Synchronous Parallel Load
  Right Shift
  Left Shift
  Do Nothing
- **Positive Edge-Triggered Clocking**
- **Embedded Clock Drivers Provide Clock Buffering**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S299XLJ software macro implements an 8-bit parallel-in/parallel-out bidirectional, universal shift register. The 8-bit length simplifies construction of large registers. The common data I/O port implemented in the packaged shift register has been separated to provide individual data inputs to the register and individual bistate outputs from the S299XLJ register. These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit features parallel inputs, parallel outputs, right-shift and left-shift inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation:

Parallel loading
Shift right (in the direction QA toward QH)
Shift left (in the direction QH toward QA)
Inhibit clocking (do nothing)

D3030, APRIL 1988

The S299XLJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV110LJ	0.75	1	0.75	0.16
IV140LJ	1.5	5	7.5	3.15
NA310LJ	1.25	32	40	6.08
NA410LJ	1.5	8	12	1.52
R2405LJ	20.5	2	41	9.24
TOTALS		48	101.25	20.15

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S299XLJ A,B,C,D,E,F,G,H,S0,S1,SL,SR,CLK,CLRZ,
QA,QB,QC,QD,QE,QF,QG,QH;

Synchronous parallel loading is accomplished by applying the eight bits of data and taking both mode-control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. When both mode-control inputs are low, a free-running clock will reload the present state of each flip-flop on each clock transition to implement the do-nothing mode.

FUNCTION TABLE

INPUTS													OUTPUTS							
	MODE			SERIAL		PARALLEL														
CLRZ	S1	S0	CLK	SL	SR	A	B	C	D	E	F	G	H	QA	QB	QC	QD	QE	QF	QG	QH
L	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L	L	L	L	L	L	L
H	X	X	L	X	X	X	X	X	X	X	X	X	X	QA_0	QB_0	QC_0	QD_0	QE_0	QF_0	QG_0	QH_0
H	H	H	↑	X	X	a	b	c	d	e	f	g	h	a	b	c	d	e	f	g	h
H	L	H	↑	X	H	X	X	X	X	X	X	X	X	H	QA_n	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n
H	L	H	↑	X	L	X	X	X	X	X	X	X	X	L	QA_n	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n
H	H	L	↑	H	X	X	X	X	X	X	X	X	X	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	QH_n	H
H	H	L	↑	L	X	X	X	X	X	X	X	X	X	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	QH_n	L
H	L	L	X	X	X	X	X	X	X	X	X	X	X	QA_0	QB_0	QC_0	QD_0	QE_0	QF_0	QG_0	QH_0

typical clear, load, right-shift, left-shift, inhibit, and clear sequences

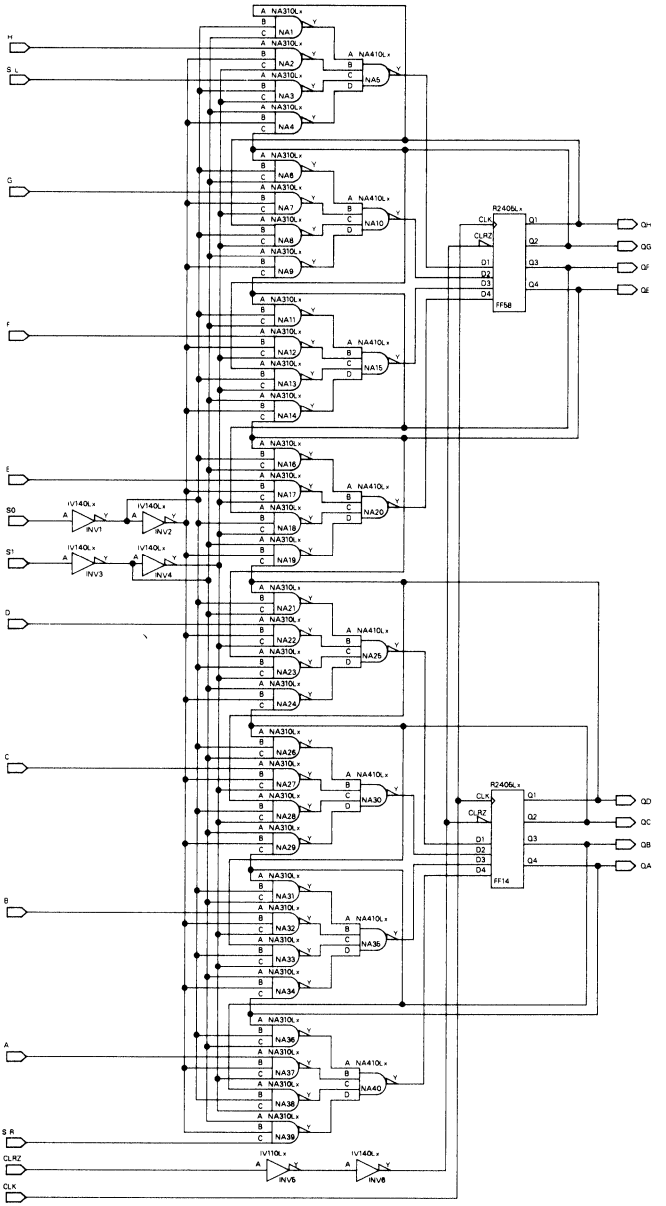
The 4-bit sequences illustrated on the S194LJ data sheet are applicable for similar 8-bit functions performed by the S299XLJ.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S299XLJ
8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

D3030, APRIL 1988

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.16		pF
		S0, S1		0.15		
		All other inputs		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	20.2		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CLK	Qn		1.6	3.4		1.6	3.2	ns
t_{PHL}				1.7	3.8		1.7	3.5	
t_{PHL}	CLRZ	Qn		1.9	3.4		1.9	3.3	ns
Δt_{PLH}	CLK	Qn	0.42	1.06	2.24	0.44	1.06	2.04	ns/pF
Δt_{PHL}			0.34	0.78	1.58	0.36	0.78	1.4	
Δt_{PHL}	CLRZ	Qn	0.34	0.76	1.54	0.36	0.76	1.4	ns/pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

HDL FILE†

```
BLOCK S299XLJ;
A       @INPUT;
B       @INPUT;
C       @INPUT;
D       @INPUT;
E       @INPUT;
F       @INPUT;
G       @INPUT;
H       @INPUT;
S0      @INPUT;
S1      @INPUT;
SL      @INPUT;
SR      @INPUT;
CLK     @INPUT;
CLRZ    @INPUT;
QA      @OUTPUT;
QB      @OUTPUT;
QC      @OUTPUT;
QD      @OUTPUT;
QE      @OUTPUT;
QF      @OUTPUT;
QG      @OUTPUT;
QH      @OUTPUT;
STRUCTURE
INV1    :IV140LJ    S0,INV1O;
INV2    :IV140LJ    INV1O,INV2O;
INV3    :IV140LJ    S1,INV3O;
INV4    :IV140LJ    INV3O,INV4O;
INV5    :IV110LJ    CLRZ,INV5O;
INV6    :IV140LJ    INV5O,INV6O;
NA1     :NA310LJ    QH,INV1O,INV3O,NA1O;
NA10    :NA410LJ    NA6O,NA7O,NA8O,NA9O,NA10O;
NA11    :NA310LJ    QF,INV1O,INV3O,NA11O;
NA12    :NA310LJ    F,INV2O,INV4O,NA12O;
NA13    :NA310LJ    QG,INV1O,INV4O,NA13O;
NA14    :NA310LJ    INV3O,INV2O,QE,NA14O;
NA15    :NA410LJ    NA11O,NA12O,NA13O,NA14O,NA15O;
NA16    :NA310LJ    QE,INV1O,INV3O,NA16O;
NA17I   :NA310LJ    E,INV2O,INV4O,NA17O;
NA18    :NA310LJ    QF,INV1O,INV4O,NA18O;
NA19    :NA310LJ    INV3O,INV2O,QD,NA19O;
NA2     :NA310LJ    H,INV2O,INV4O,NA2O;
NA20    :NA410LJ    NA16O,NA17O,NA18O,NA19O,NA20O;
NA21    :NA310LJ    QD,INV1O,INV3O,NA21O;
NA22    :NA310LJ    D,INV2O,INV4O,NA22O;
NA23    :NA310LJ    QE,INV1O,INV4O,NA23O;
NA24    :NA310LJ    INV3O,INV2O,QC,NA24O;
NA25    :NA410LJ    NA21O,NA22O,NA23O,NA24O,NA25O;
NA26    :NA310LJ    QC,INV1O,INV3O,NA26O;
NA27    :NA310LJ    C,INV2O,INV4O,NA27O;
NA28    :NA310LJ    QD,INV1O,INV4O,NA28O;
NA29    :NA310LJ    INV3O,INV2O,QB,NA29O;
NA3     :NA310LJ    SL,INV1O,INV4O,NA3O;
NA30    :NA410LJ    NA26O,NA27O,NA28O,NA29O,NA30O;
NA31    :NA310LJ    QB,INV1O,INV3O,NA31O;
NA32    :NA310LJ    B,INV2O,INV4O,NA32O;
NA33    :NA310LJ    QC,INV1O,INV4O,NA33O;
NA34    :NA310LJ    INV3O,INV2O,QA,NA34O;
NA35    :NA410LJ    NA31O,NA32O,NA33O,NA34O,NA35O;
NA36    :NA310LJ    QA,INV1O,INV3O,NA36O;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

HDL FILE† - Continued

```
NA37      :NA310LJ   A,INV2O,INV4O,NA37O;
NA38      :NA310LJ   QB,INV1O,INV4O,NA38O;
NA39      :NA310LJ   INV3O,INV2O,SR,NA39O;
NA4       :NA310LJ   INV3O,INV2O,QG,NA4O;
NA40      :NA410LJ   NA36O,NA37O,NA38O,NA39O,NA40O;
NA5       :NA410LJ   NA1O,NA2O,NA3O,NA4O,NA5O;
NA6       :NA310LJ   QG,INV1O,INV3O,NA6O;
NA7       :NA310LJ   G,INV2O,INV4O,NA7O;
NA8       :NA310LJ   QH,INV1O,INV4O,NA8O;
NA9       :NA310LJ   INV3O,INV2O,QF,NA9O;
FF14      :R2405LJ   INV6O,NA25O,NA30O,NA35O,NA40O,
                     CLK,QD,QC,QB,QA;
FF58      :R2405LJ   INV6O,NA5O,NA10O,NA15O,NA20O,
                     CLK,QH,QG,QF,QE;
END S299XLJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

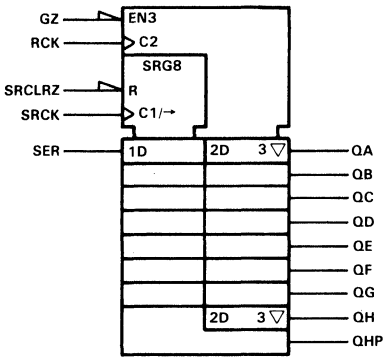
S595LJ
8-BIT SHIFT REGISTER WITH 3-STATE OUTPUT REGISTERS

D3030, APRIL 1988

SOFTWARE MACRO

- 8-Bit Serial-In, Parallel-Out Shift Registers with Output Storage
- Buffered Clear and Output-Enable Inputs
- Shift Register has Direct Clear
- Embedded Clock Drivers Provide Clock Buffering
- Dependable Texas Instruments Quality and Reliability

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The S595LJ software macro implements an 8-bit parallel-out shift register with output storage registers. The 8-bit length simplifies construction of large registers. These macros each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial outputs for cascading. Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift-register state will always be one clock pulse ahead of the storage register. The S595LJ is implemented with the standard cell functions indicated:

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV110LJ	0.75	1	0.75	0.16
IV120LJ	1	2	2	0.62
R2401LJ	23.5	2	47	9.06
R2407LJ	24.5	2	49	9.92
TO010LJ	0.75	1	0.75	NIL
TOTALS		8	99.5	19.76

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S595LJ SER,SRCK,SRCLRZ,RCK,GZ,QA,QB,QC,QD,QE,QF,QG,QH,QHP;

S595LJ
8-BIT SHIFT REGISTER WITH 3-STATE OUTPUT REGISTERS

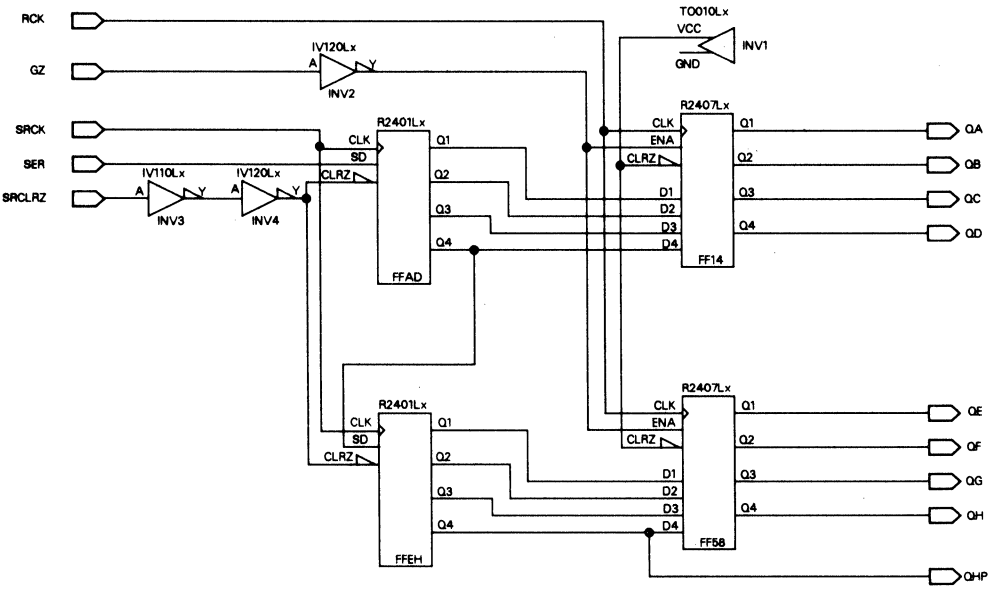
D3030, APRIL 1988

FUNCTION TABLE

SHIFT REGISTER							OUTPUT REGISTER				
INPUTS				OUTPUTS			INPUTS		OUTPUTS		
SRCLRZ	SRCK	SER	sQA	sQB . .	sQH	sQHP	RCK	GZ	QA	QB . . .	QH
X	X	X	X	X	X	X	X	H	Z	Z	Z
X	X	X	X	X	X	X	L	L	QA_0	QB_0	QH_0
L	X	X	L	L	L	L	↑	L	L	L	L
H	↑	H	H	sQA_n	sQG_n	sQG_n	L	L	rQA_0	rQB_0	rQH_0
H	↑	L	L	sQA_n	sQG_n	sQG_n	L	L	rQA_0	rQB_0	rQH_0
H	↑	H	H	sQA_n	sQG_n	sQG_n	↑	L	sQA	sQB	sQH
H	↑	L	L	sQA_n	sQG_n	sQG_n	↑	L	sQA	sQB	sQH
H	L	X	sQA_0	sQB_0	sQH_0	sQH_0	↑	L	sQA	sQB	sQH

H = high level(steady state)
L = low level (steady state)
sQ = shift register output
X = irrelevant(any input, including transitions)
Z = high impedance (off state)
↑ = transition from low to high level
QA_0, QB_0, QH_0 = the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.
QAn, QGn = the level of QA or QG before the most-recent ↑ transition of the clock; indicates a one-bit shift.
NOTE: When GZ is high, the output is disabled to the high-impedance state.

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S595LJ
8-BIT SHIFT REGISTER
WITH 3-STATE OUTPUT REGISTERS

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	GZ		0.11		pF
		RCK, SRCK		0.22		
		SER		0.06		
		SRCLRZ		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	19.76		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Notes 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	SRCK	QHP		1.5	3.3		1.5	3	ns
t_{PHL}				1.6	3.7		1.6	3.3	
t_{PLH}	RCK	Qn		1.6	3.5		1.6	3.2	ns
t_{PHL}				1.7	3.9		1.7	3.6	
t_{PHL}	SRCLRZ	QHP		1.9	3.8		1.9	3.2	ns
t_{PZH}	GZ	Qn		1.1	1.9		1.1	1.9	ns
t_{PZL}				1	1.6		1	1.6	
Δt_{PLH}	RCK	Qn	0.77	2.14	4.64	0.82	2.14	4.27	ns/pF
Δt_{PHL}			0.51	1.33	2.76	0.55	1.33	2.54	
Δt_{PZH}	GZ	Qn	0.77	2.2	4.93	0.82	2.2	4.51	ns/pF
Δt_{PZL}			0.54	1.38	3.23	0.57	1.38	2.88	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance.

2. Enable and delta-enable times are measured using the conditions specified for the S2407LJ.

HDL†

```
BLOCK S595LJ;
SER         @INPUT;
SRCK        @INPUT;
SRCLRZ      @INPUT;
RCK         @INPUT;
GZ          @INPUT;
QA          @OUTPUT;
QB          @OUTPUT;
QC          @OUTPUT;
QD          @OUTPUT;
QE          @OUTPUT;
QF          @OUTPUT;
QG          @OUTPUT;
QH          @OUTPUT;
QHP         @OUTPUT;

STRUCTURE
INV1        :TO010LJ    DUM,INV1O;
INV2        :IV120LJ    GZ,INV2O;
INV3        :IV110LJ    SRCLRZ,INV3O;
INV4        :IV120LJ    INV3O,INV4O;
FF14        :R2407LJ    INV1O,FFAQ,FFBQ,FFCQ,FFDQ,
                        RCK,INV2O,QA,QB,QC,QD;
FF58        :R2407LJ    INV1O,FFEQ,FFFQ,FFGQ,QHP,
                        RCK,INV2O,QE,QF,QG,QH;
FFAD        :R2401LJ    INV4O,SER,SRCK,FFAQ,FFBQ,FFCQ,FFDQ;
FFEH        :R2401LJ    INV4O,FFDQ,SRCK,FFEQ,FFFQ,FFGQ,QHP;
END S595LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S598XLJ 8-BIT SHIFT REGISTER WITH INPUT REGISTERS

D3030, APRIL 1988

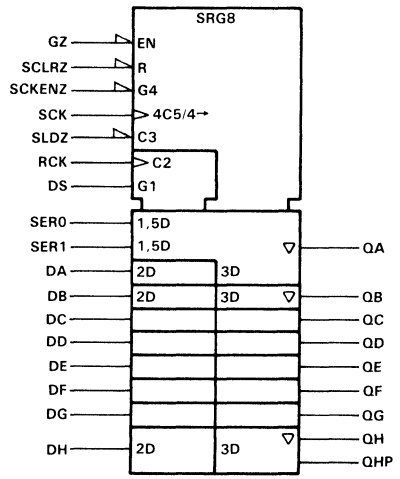
SOFTWARE MACRO

- **8-Bit Serial-In, Parallel-Out Shift Registers with Output Storage**
- **Buffered Clear and Output-Enable Inputs**
- **Shift Register has Direct Clear**
- **Embedded Clock Drivers Provide Clock Buffering**

description

The S598XLJ software macro implements an 8-bit parallel-out shift register with input storage registers. The 8-bit length simplifies construction of large registers. The common data I/O port implemented on the packaged shift register has been separated to provide individual data inputs to the register and individual 3-state outputs from the S598XLJ counter. The S598XLJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
AN210LJ	1.5	10	15	3.3
DFB20LJ	7.25	8	58	14.24
IV110LJ	0.75	4	3	0.64
IV120LJ	1	4	4	1.24
IV140LJ	1.5	1	1.5	0.63
IV212LJ	1.25	8	10	1.44
LAH10LJ	3.75	1	3.75	0.78
NA210LJ	1	16	16	3.04
OR210LJ	1.25	1	1.25	0.37
R2406LJ	23.5	2	47	10.32
TO010LJ	0.75	1	0.75	NIL
TOTALS		56	160.25	36

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S598XLJ DA,DB,DC,DD,DE,DF,DG,DH,RCK,SCK,SCKENZ,SLDZ,SCLRZ, SER0,SER1,DS,GZ,QA,QB,QC,QD,QE,QF,QG,QH,QHP;

These macros each contain an 8-bit serial-in, parallel-out shift register fed by an 8-bit D-type input register. The shift register has parallel 3-state outputs. Separate clocks are provided for the shift register and the input register. The shift register has a direct-overriding clear, multiplexed dual serial inputs, and dual serial outputs to simplify cascading. Both the shift-register and input-register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift-register output will be equal to one-half or double the previous value of the storage register. The shift-register clock is implemented with an associated clock enable that contains internal circuitry to prevent it from triggering the clock.

FUNCTION TABLE

INPUT REGISTER					SHIFT REGISTER											
					INPUTS								OUTPUTS			
RCK	INPUTS		OUTPUTS		SCLRZ	GZ	CLOCK		LOAD	SERIAL						
	DA. . .DH		RA. . .RH				SCKENZ	SCK	SLDZ	DS	SER0	SER1	QA	QB. . .QH		QHP
X	X	X	X	X	X	H	X	X	X	X	X	X	Z	Z	Z	QH
X	X	X	X	X	L	L	X	X	X	X	X	X	L	L	L	L
↑	a	h	a	h	H	L	H	X	X	X	X	X	QA_0	QB_0	QH_0	QH_0
L	X	X	RA_0	RH_0	H	L	L	↑	L	X	X	X	RA	RB	RH	RH
↑	a	h	a	h	H	L	L	↑	H	L	H	X	H	QA_n	QG_n	QG_n
X	X	X	X	X	H	L	L	↑	H	L	H	X	H	QA_n	QG_n	QG_n
X	X	X	X	X	H	L	L	↑	H	L	L	X	L	QA_n	QG_n	QG_n
X	X	X	X	X	H	L	L	↑	H	H	X	H	H	QA_n	QG_n	QG_n
X	X	X	X	X	H	L	L	↑	H	H	X	L	L	QA_n	QG_n	QG_n
X	X	X	X	X	H	L	X	L	X	X	X	X	QA_0	QB_0	QH_0	QH_0

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

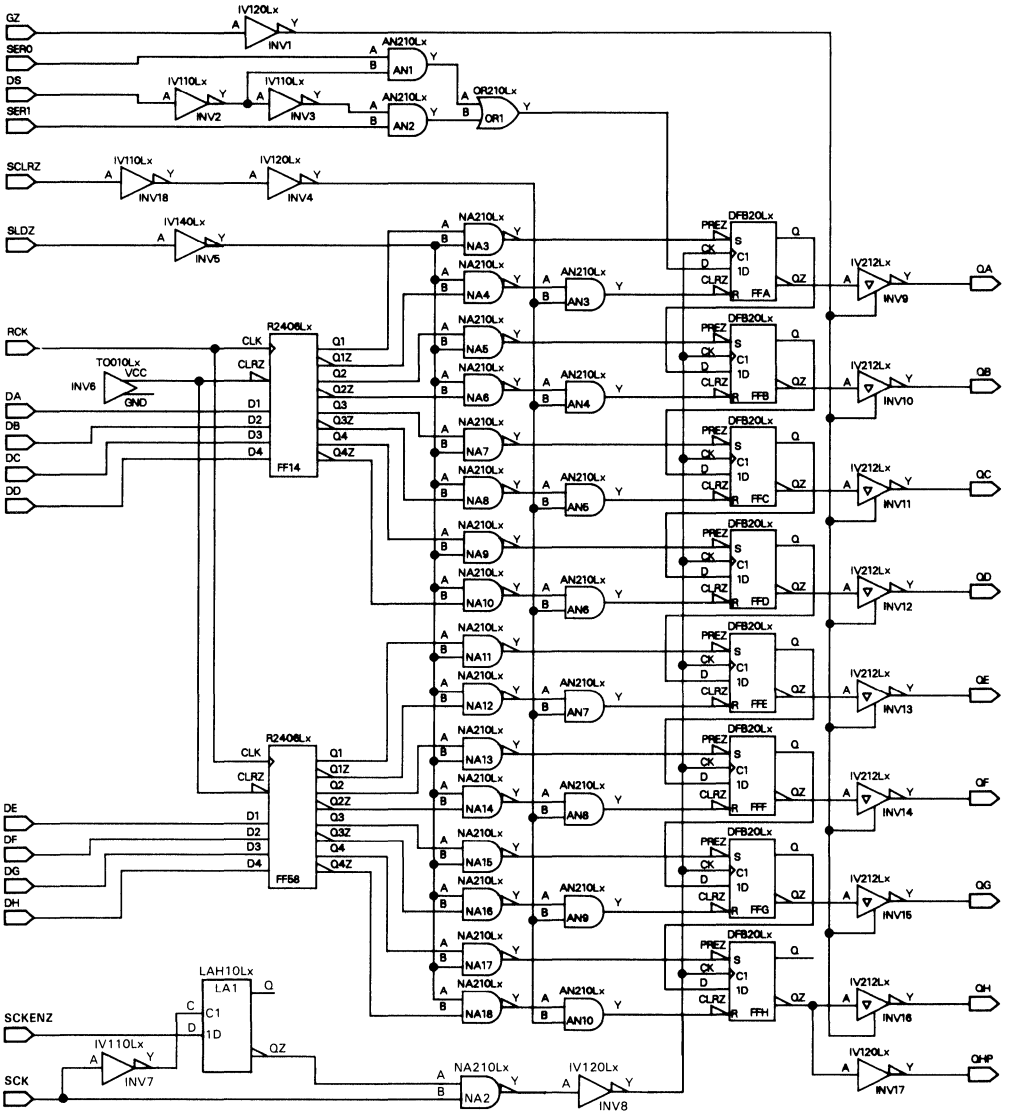
timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

S598XLJ
8-BIT SHIFT REGISTER WITH INPUT REGISTERS

D3030, APRIL 1988

logic diagram



electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	Dn SERn		0.06		pF
		GZ		0.11		
		RDK, SLDZ		0.23		
		Any other input		0.06		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	36		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Notes 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	SCK	QHP		2.3	6.5		2.3	6	ns
t_{PHL}				3.7	8.1		3.7	7.5	
t_{PHL}	SCLRZ	QHP		3.7	6.1		3.7	5.7	ns
t_{PHL}	SCLRZ	Qn		3.1	7.9		3.1	7.3	ns
t_{PLH}	SCK	Qn		3.1	6.9		3.1	6.4	ns
t_{PHL}				3.7	8.3		3.7	7.6	
t_{PLH}	SLDZ	QHP		2.3	4.8		2.3	4.3	ns
t_{PHL}				3.1	6.1		3.1	5.7	
t_{PLH}	SSLDZ	Qn		2.4	5		2.4	4.7	ns
t_{PHL}				3.7	7.9		3.7	7.3	
t_{PZH}	GZ	Qn		1	2		1	1.8	ns
t_{PZL}				1	1.8		1	1.6	
Δt_{PLH}	Any	Qn	0.7	2.08	4.52	0.76	2.08	4.16	ns/pF
Δt_{PHL}			0.48	1.22	2.7	0.52	1.22	2.42	
Δt_{PZH}	GZ	Qn	0.76	2.14	4.8	0.8	2.14	4.38	ns/pF
Δt_{PZL}			0.52	1.26	2.88	0.56	1.26	2.56	
Δt_{PLH}	Any	QHP	0.24	0.52	1.1	0.26	0.52	1	ns/pF
Δt_{PHL}			0.28	0.42	0.68	0.28	0.42	0.62	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Actual performance can be evaluated at post-layout simulation.

2. Enable and delta-enable times are measured using the conditions specified for the IV212LJ.

HDL FILE†

```
BLOCK S598XLJ;
DA          @INPUT;
DB          @INPUT;
DC          @INPUT;
DD          @INPUT;
DE          @INPUT;
DF          @INPUT;
DG          @INPUT;
DH          @INPUT;
RCK         @INPUT;
SCK         @INPUT;
SCKENZ      @INPUT;
SLDZ        @INPUT;
SCLRZ       @INPUT;
SER0        @INPUT;
SER1        @INPUT;
DS          @INPUT;
GZ          @INPUT;
QA          @OUTPUT;
QB          @OUTPUT;
QC          @OUTPUT;
QD          @OUTPUT;
QE          @OUTPUT;
QF          @OUTPUT;
QG          @OUTPUT;
QH          @OUTPUT;
QHP         @OUTPUT;

STRUCTURE
AN1         :AN210LJ    SER0,INV2O,AN1O;
AN2         :AN210LJ    INV3O,SER1,AN2O;
AN3         :AN210LJ    NA4O,INV4O,AN3O;
AN4         :AN210LJ    NA6O,INV4O,AN4O;
AN5         :AN210LJ    NA8O,INV4O,AN5O;
AN6         :AN210LJ    NA10O,INV4O,AN6O;
AN7         :AN210LJ    NA12O,INV4O,AN7O;
AN8         :AN210LJ    NA14O,INV4O,AN8O;
AN9         :AN210LJ    NA16O,INV4O,AN9O;
AN10        :AN210LJ    NA18O,INV4O,AN10O;
FFA         :DFB20LJ    AN3O,NA3O,OR1O,INV8O,FFAQ,FFAQZ;
FFB         :DFB20LJ    AN4O,NA5O,FFAQ,INV8O,FFBQ,FFBQZ;
FFC         :DFB20LJ    AN5O,NA7O,FFBQ,INV8O,FFCQ,FFCQZ;
FFD         :DFB20LJ    AN6O,NA9O,FFCQ,INV8O,FFDQ,FFDQZ;
FFE         :DFB20LJ    AN7O,NA11O,FFDQ,INV8O,FFEQ,FFEQZ;
FFF         :DFB20LJ    AN8O,NA13O,FFEQ,INV8O,FFFQ,FFFQZ;
FFG         :DFB20LJ    AN9O,NA15O,FFFQ,INV8O,FFGQ,FFGQZ;
FFH         :DFB20LJ    AN10O,NA17O,FFGQ,INV8O,DUM,FFHQZ;
FF14        :R2406LJ    TIEHI,DA,DB,DC,DD,RCK,FF1Q,FF1QZ,
                        FF2Q,FF2QZ,FF3Q,FF3QZ,FF4Q,FF4QZ;
F58         :R2406LJ    TIEHI,DE,DF,DG,DH,RCK,FF5Q,FF5QZ,
                        FF6Q,FF6QZ,FF7Q,FF7QZ,FF8Q,FF8QZ;
INV1        :IV120LJ    GZ,INV1O;
INV2        :IV110LJ    DS,INV2O;
INV3        :IV110LJ    INV2O,INV3O;
INV4        :IV120LJ    INV18O,INV4O;
INV5        :IV140LJ    SLDZ, INV50;
INV6        :TO010LJ    TIELO,TIEHI;
INV7        :IV110LJ    SCK,INV7O;
INV8        :IV120LJ    NA2O,INV8O;
INV9        :IV212LJ    FFAQZ,INV1O,QA;
INV10       :IV212LJ    FFBQZ,INV1O,QB;
INV11       :IV212LJ    FFCQZ,INV1O,QC;
INV12       :IV212LJ    FFDQZ,INV1O,QD;
INV13       :IV212LJ    FFEQZ,INV1O,QE;
INV14       :IV212LJ    FFFQZ,INV1O,QF;
```

† The HDL netlist format requires the "STRUCTURE" program line sto follow the "BLOCK" I/O program lines.

HDL FILE† - Continued

```
INV15     :IV212LJ   FFGQZ,INV1O,QG;
INV16     :IV212LJ   FFHQZ,INV1O,QH;
INV17     :IV120LJ   FFHQZ,QHP;
INV18     :IV110LJ   SCLRZ,INV18O;
LA1       :LAH10LJ   SCKENZ,INV7O,DUM1,LA1O;
NA2       :NA210LJ   LA1O,SCK,NA2O;
NA3       :NA210LJ   FF1Q,INV5O,NA3O;
NA4       :NA210LJ   INV5O,FF1QZ,NA4O;
NA5       :NA210LJ   FF2Q,INV5O,NA5O;
NA6       :NA210LJ   INV5O,FF2QZ,NA6O;
NA7       :NA210LJ   FF3Q,INV5O,NA7O;
NA8       :NA210LJ   INV5O,FF3QZ,NA8O;
NA9       :NA210LJ   FF4Q,INV5O,NA9O;
NA10      :NA210LJ   INV5O,FF4QZ,NA10O;
NA11      :NA210LJ   FF5Q,INV5O,NA11O;
NA12      :NA210LJ   INV5O,FF5QZ,NA12O;
NA13      :NA210LJ   FF6Q,INV5O,NA13O;
NA14      :NA210LJ   INV5O,FF6QZ,NA14O;
NA15      :NA210LJ   FF7Q,INV5O,NA15O;
NA16      :NA210LJ   INV5O,FF7QZ,NA16O;
NA17      :NA210LJ   FF8Q,INV5O,NA17O;
NA18      :NA210LJ   INV5O,FF8QZ,NA18O;
OR1       :OR210LJ   AN1O,AN2O,OR1O;
END S598XLJ;
```

† The HDL netlist format requires the "STRUCTURE" program line sto follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S651LJ
8-BIT BIDIRECTIONAL UNIVERSAL TRANSCEIVER REGISTER WITH INVERTING DATA PATHS

D3030, APRIL 1988

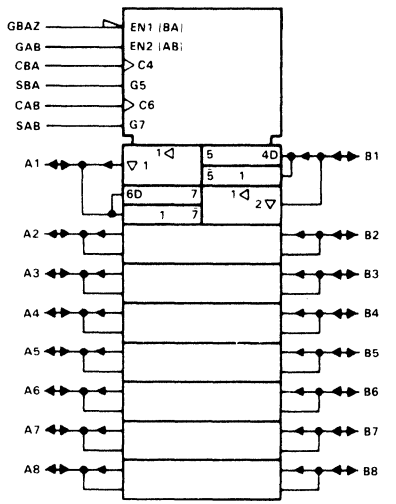
SOFTWARE MACRO

- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Inverting Data Paths**
- **Positive Edge-Triggered Clocking**
- **Embedded Clock Drivers Provide Clock Buffering**

description

The S651LJ software macro implements an 8-bit parallel-in/parallel-out bidirectional, universal transceiver register. The 8-bit length simplifies construction of large registers. These bidirectional transceivers are designed to incorporate virtually all of the features a system designer may want in a transceiver. The circuit features parallel inputs, parallel outputs, direction control, and source-control inputs. The S651LJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV110LJ	0.75	1	0.75	0.16
IV140LJ	1.5	6	9	3.78
IV222LJ	2	16	32	6.08
NA210LJ	1	48	48	9.12
R2405LJ	20.5	4	82	18.48
TO010LJ	0.75	1	0.75	NIL
TOTALS		76	172.5	37.62

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S651LJ GBAZ,GAB,SBA,SAB,CBA,CAB,A1,A2,A3,A4, A5,A6,A7,A8,B1,B2,B3,B4,B5,B6,B7,B8;

The S651LJ consists of bus interface circuits, D-type registers, and control circuitry arranged for multiplexed transmission of data directly to or from an internal data bus or from the embedded storage registers. Enable GAB and GBAZ are provided to control the transceiver functions. SAB and SBA control inputs are provided to select whether real-time or stored data are transferred. A low input level selects real-time data, and a high selects stored data. The examples on the following page demonstrate the four fundamental bus-management functions that can be performed with the S651LJ.

Data on the A or B data bus, or both, can be stored in the internal D registers by low-to-high transitions at the appropriate clock inputs (CAB and CBA) regardless of the select or enable control inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type registers by simultaneously enabling GAB and GBAZ. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at a high impedance, each set of bus lines will remain at its last state.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
GAB	GBAZ	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	see Note 1	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	see Note 1	Input	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Sotred A Data to B Bus and Stored A Data to A Bus

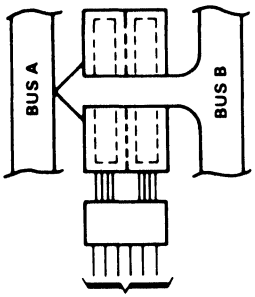
† The data output functions may be enabled or disabled by various signals at the GAB and GBAZ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every low-to- high transition on the clock inputs.

NOTE 1: This input combination is not specified.

S651LJ
8-BIT BIDIRECTIONAL UNIVERSAL TRANSCEIVER REGISTER WITH INVERTING DATA PATHS

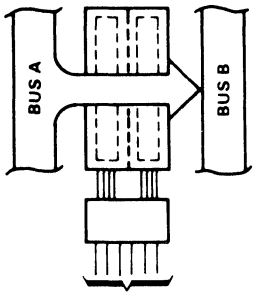
D3030, APRIL 1988

typical bus management functions



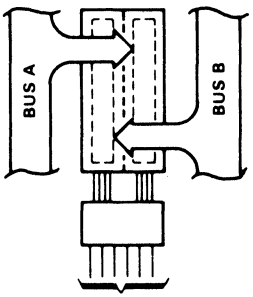
GAB	GBAZ	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



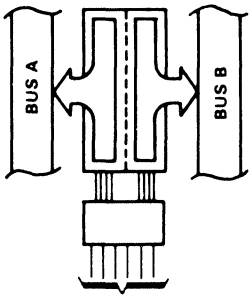
GAB	GBAZ	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



GAB	GBAZ	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

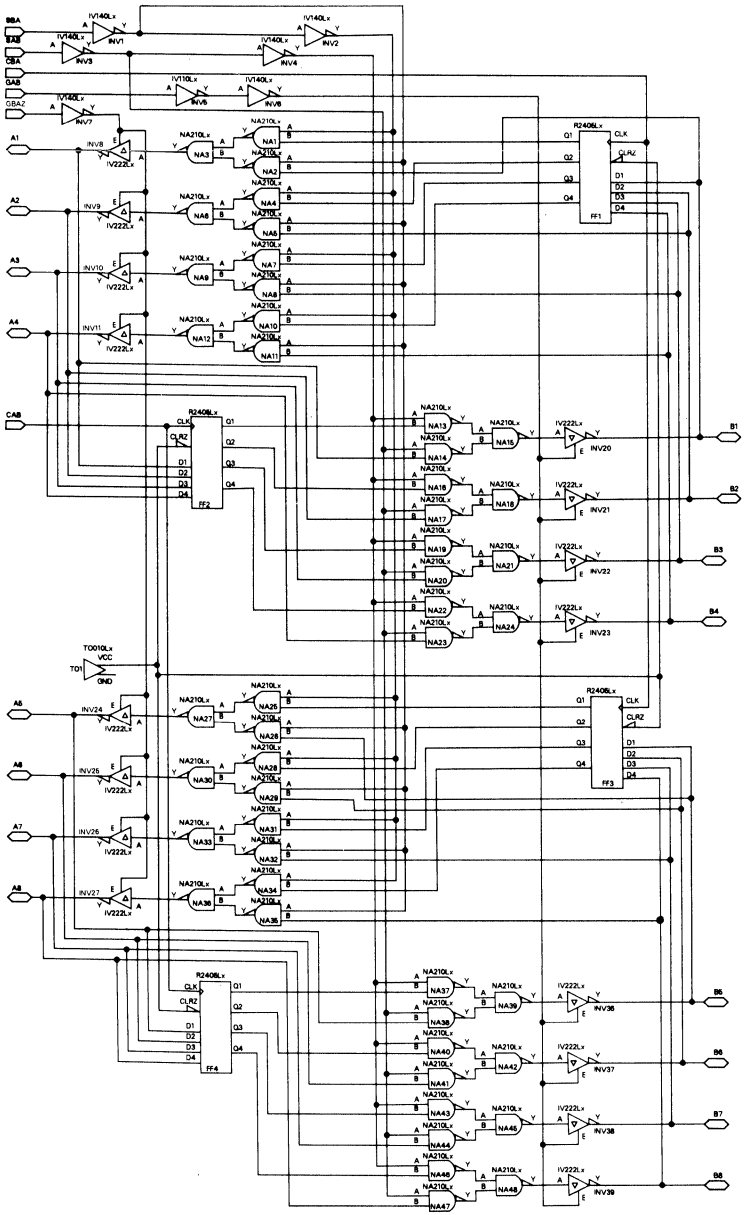
STORAGE FROM
A AND/OR B



GAB	GBAZ	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER
STORED DATA
TO A AND/OR B

logic diagram



absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	An or Bn		0.12		pF
		CAB, CBA		0.22		
		GAB		0.05		
		GBAZ, SAB, SBA		0.23		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	37.62		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Notes 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CAB,CBA	A,B		3.5	7.3		3.5	6.5	ns
t_{PHL}				3.2	6.6		3.2	6.1	
t_{PLH}	A,B	B,A		1.7	3.3		1.7	3	ns
t_{PHL}				1.5	3.9		1.5	2.7	
t_{PLH}	SAB,SBA	A,B		2.2	3.9		2.2	3.7	ns
t_{PHL}				2.2	3.9		2.2	3.4	
t_{PZH}	GAB,GBAZ	A,B		1.4	2.9		1.4	2.8	ns
t_{PZL}				1.3	2.5		1.3	2.3	
Δt_{PLH}	Any	Any	0.34	1	2.22	0.34	1	2.06	ns/pF
Δt_{PHL}			0.26	0.6	1.34	0.28	0.6	1.2	
Δt_{PZH}	GAB,GBAZ	Any	0.34	1.02	2.26	0.38	1.02	2.08	ns/pF
Δt_{PZL}			0.38	0.64	1.36	0.38	0.64	1.2	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

2. Enable and delta-enable times are measured using the conditions specified for the IV222LJ.

S651LJ
8-BIT BIDIRECTIONAL UNIVERSAL TRANSCEIVER REGISTER WITH INVERTING DATA PATHS

D3030, APRIL 1988

HDL FILE†

```
BLOCK S651LJ;
GBAZ        @INPUT;
GAB         @INPUT;
SBA         @INPUT;
SAB         @INPUT;
CBA         @INPUT;
CAB         @INPUT;
A1          @INOUT;
A2          @INOUT;
A3          @INOUT;
A4          @INOUT;
A5          @INOUT;
A6          @INOUT;
A7          @INOUT;
A8          @INOUT;
B1          @INOUT;
B2          @INOUT;
B3          @INOUT;
B4          @INOUT;
B5          @INOUT;
B6          @INOUT;
B7          @INOUT;
B8          @INOUT;
STRUCTURE
INV1        :IV140LJ    SBA,SBAZ;
INV10       :IV222LJ    SNA9,GBA,A3;
INV11       :IV222LJ    SNA12,GBA,A4;
INV2        :IV140LJ    SBAZ,SBA1;
INV20       :IV222LJ    SNA15,GAB1,B1;
INV21       :IV222LJ    SNA18,GAB1,B2;
INV22       :IV222LJ    SNA21,GAB1,B3;
INV23       :IV222LJ    SNA24,GAB1,B4;
INV24       :IV222LJ    SNA27,GBA,A5;
INV25       :IV222LJ    SNA30,GBA,A6;
INV26       :IV222LJ    SNA33,GBA,A7;
INV27       :IV222LJ    SNA36,GBA,A8;
INV3        :IV140LJ    SAB,SABZ;
INV36       :IV222LJ    SNA39,GAB1,B5;
INV37       :IV222LJ    SNA42,GAB1,B6;
INV38       :IV222LJ    SNA45,GAB1,B7;
INV39       :IV222LJ    SNA48,GAB1,B8;
INV4        :IV140LJ    SABZ,SAB1;
INV5        :IV110LJ    GAB,GABZ;
INV6        :IV140LJ    GABZ,GAB1;
INV7        :IV140LJ    GBAZ,GBA;
INV8        :IV222LJ    SNA3,GBA,A1;
INV9        :IV222LJ    SNA6,GBA,A2;
NA1         :NA210LJ    SBA1,FF1A,SNA1;
NA10        :NA210LJ    SBA1,FF1D,SNA10;
NA11        :NA210LJ    SBAZ,B4,SNA11;
NA12        :NA210LJ    SNA10,SNA11,SNA12;
NA13        :NA210LJ    SAB1,FF2A,SNA13;
NA14        :NA210LJ    SABZ,A1,SNA14;
NA15        :NA210LJ    SNA13,SNA14,SNA15;
NA16        :NA210LJ    SAB1,FF2B,SNA16;
NA17        :NA210LJ    SABZ,A2,SNA17;
NA18        :NA210LJ    SNA16,SNA17,SNA18;
NA19        :NA210LJ    SAB1,FF2C,SNA19;
NA2         :NA210LJ    SBAZ,B1,SNA2;
NA20        :NA210LJ    SABZ,A3,SNA20;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

HDL FILE† - Continued

```
NA21    :NA210LJ   SNA19,SNA20,SNA21;
NA22    :NA210LJ   SAB1,FF2D,SNA22;
NA23    :NA210LJ   SABZ,A4,SNA23;
NA24    :NA210LJ   SNA22,SNA23,SNA24;
NA25    :NA210LJ   SBA1,FF3A,SNA25;
NA26    :NA210LJ   SBAZ,B5,SNA26;
NA27    :NA210LJ   SNA25,SNA26,SNA27;
NA28    :NA210LJ   SBA1,FF3B,SNA28;
NA29    :NA210LJ   SBAZ,B6,SNA29;
NA3     :NA210LJ   SNA1,SNA2,SNA3;
NA30    :NA210LJ   SNA28,SNA29,SNA30;
NA31    :NA210LJ   SBA1,FF3C,SNA31;
NA32    :NA210LJ   SBAZ,B7,SNA32;
NA33    :NA210LJ   SNA31,SNA32,SNA33;
NA34    :NA210LJ   SBA1,FF3D,SNA34;
NA35    :NA210LJ   SBAZ,B8,SNA35;
NA36    :NA210LJ   SNA34,SNA35,SNA36;
NA37    :NA210LJ   SAB1,FF4A,SNA37;
NA38    :NA210LJ   SABZ,A5,SNA38;
NA39    :NA210LJ   SNA37,SNA38,SNA39;
NA4     :NA210LJ   SBA1,FF1B,SNA4;
NA40    :NA210LJ   SAB1,FF4B,SNA40;
NA41    :NA210LJ   SABZ,A6,SNA41;
NA42    :NA210LJ   SNA40,SNA41,SNA42;
NA43    :NA210LJ   SAB1,FF4C,SNA43;
NA44    :NA210LJ   SABZ,A7,SNA44;
NA45    :NA210LJ   SNA43,SNA44,SNA45;
NA46    :NA210LJ   SAB1,FF4D,SNA46;
NA47    :NA210LJ   SABZ,A8,SNA47;
NA48    :NA210LJ   SNA46,SNA47,SNA48;
NA5     :NA210LJ   SBAZ,B2,SNA5;
NA6     :NA210LJ   SNA4,SNA5,SNA6;
NA7     :NA210LJ   SBA1,FF1C,SNA7;
NA8     :NA210LJ   SBAZ,B3,SNA8;
NA9     :NA210LJ   SNA7,SNA8,SNA9;
TO1     :TO010LJ   DUM,STO1:
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

HDL FILE† - Continued

```
FF1         :R2405LJ   STO1,B1,B2,B3,B4,CBA,FF1A,
                       FF1B,FF1C,FF1D;
FF2         :R2405LJ   STO1,A1,A2,A3,A4,CAB,FF2A,
                       FF2B,FF2C,FF2D;
FF3         :R2405LJ   STO1,B5,B6,B7,B8,CBA,
                       FF3A,FF3B,FF3C,FF3D;
FF4         :R2405LJ   STO1,A5,A6,A7,A8,CAB,FF4A,
                       FF4B,FF4C,FF4D;
END S651LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the "BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S652LJ
8-BIT BIDIRECTIONAL UNIVERSAL TRANSCEIVER REGISTER WITH NONINVERTING DATA PATHS

D3030, APRIL 1988

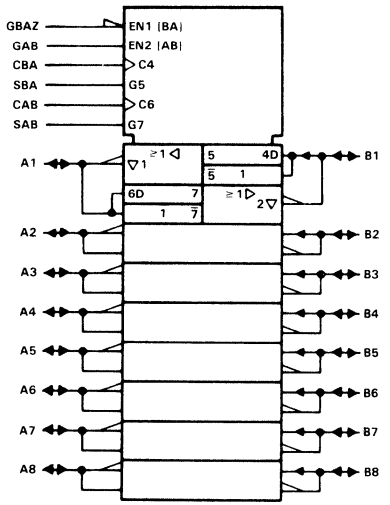
SOFTWARE MACRO

- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Noninverting Data Paths**
- **Edge-Triggered Clocking**
- **Embedded Clock Drivers Provide Clock Buffering**

description

The S652LJ software macro implements an 8-bit parallel-in/parallel-out bidirectional, universal transceiver register. The 8-bit length simplifies construction of large registers. These bidirectional transceivers are designed to incorporate virtually all of the features a system designer may want in a transceiver. The circuit features parallel inputs, parallel outputs, direction control, and source-control inputs. The S652LJ is implemented with the standard cell functions indicated:

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CELL NAME	EQUIVALENT NUMBER OF NA210LJs	TOTAL NO. USED	TOTAL EQUIVALENT NA210LJs	TOTAL C_{pd} (pF)
IV110LJ	0.75	17	12.75	2.72
IV140LJ	1.5	6	9	3.78
IV222LJ	2	16	32	6.08
NA210LJ	1	48	48	9.12
R2406LJ	23.5	4	94	20.64
TO010LJ	0.75	1	0.75	NIL
TOTALS		92	196.5	42.34

When the macro is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: S651LJ GBAZ,GAB,SBA,SAB,CBA,CAB,A1,A2,A3,A4,
A5,A6,A7,A8,B1,B2,B3,B4,B5,B6,B7,B8;

The S652LJ consists of bus interface circuits, D-type registers, and control circuitry arranged for multiplexed transmission of data directly to or from an internal data bus or from the embedded storage registers. Enable GAB and GBAZ are provided to control the transceiver functions. SAB and SBA control inputs are provided to select whether real-time or stored data are transferred. A low input level selects real-time data, and a high selects stored data. The examples on the following page demonstrate the four fundamental bus-management functions that can be performed with the S652LJ.

Data on the A or B data bus, or both, can be stored in the internal D registers by low-to-high transitions at the appropriate clock inputs (CAB and CBA) regardless of the select or enable control inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type registers by simultaneously enabling GAB and GBAZ. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at a high impedance, each set of bus lines will remain at its last state.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
GAB	GBAZ	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Sotred A Data to B Bus and Stored B Data to A Bus

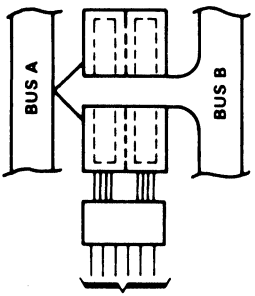
† The data output functions may be enabled or disabled by various signals at the GAB and GBAZ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every low-to- high transition on the clock inputs.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S652LJ
8-BIT BIDIRECTIONAL UNIVERSAL TRANSCEIVER REGISTER WITH NONINVERTING DATA PATHS

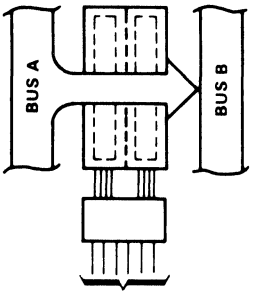
D3030, APRIL 1988

typical bus management functions



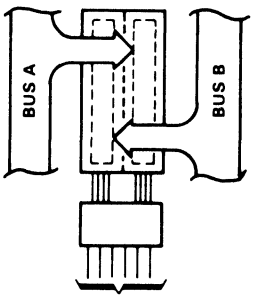
GAB	GBAZ	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



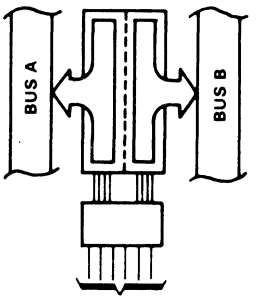
GAB	GBAZ	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



GAB	GBAZ	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A AND/OR B



GAB	GBAZ	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

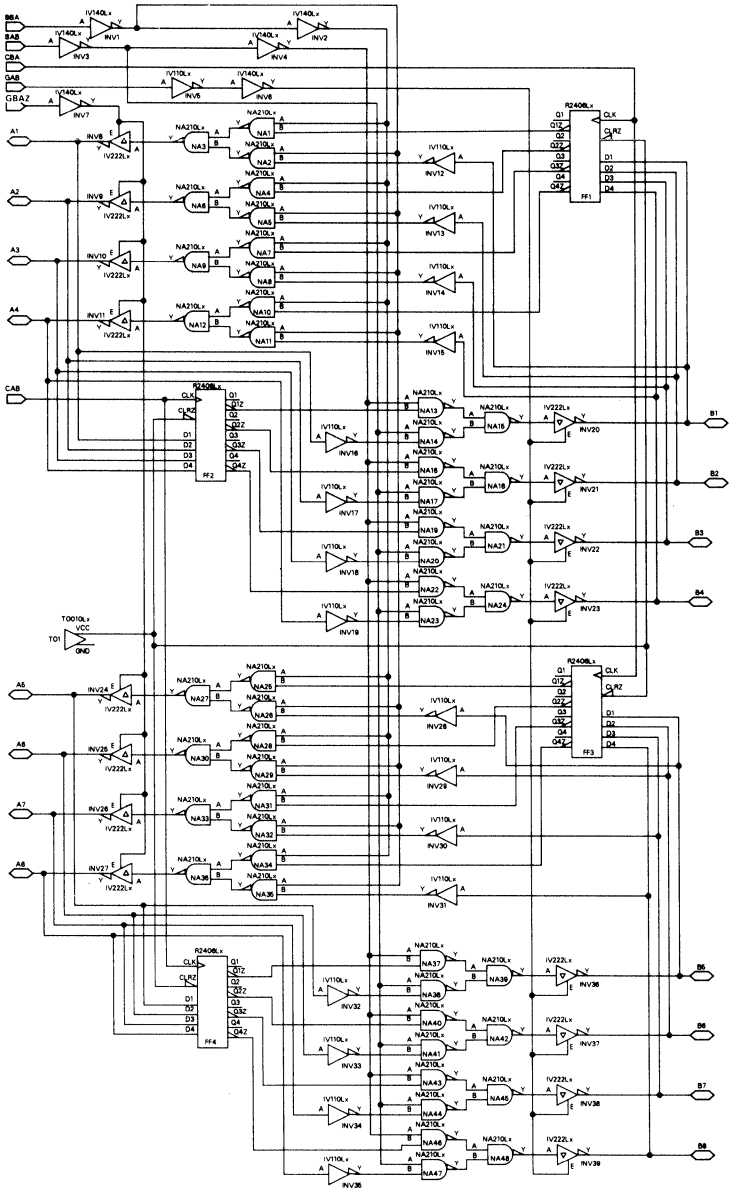
TRANSFER
STORED DATA
TO A AND/OR B

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S652LJ
8-BIT BIDIRECTIONAL UNIVERSAL TRANSCEIVER REGISTER WITH NONINVERTING DATA PATHS

D3030, APRIL 1988

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

S652LJ
8-BIT BIDIRECTIONAL UNIVERSAL TRANSCEIVER REGISTER WITH NONINVERTING DATA PATHS

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements

Specific timing data regarding pulse duration, setup time, and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked cells embedded in the software macros. Evaluations of timing requirements made during pre-layout simulation produce workstation output used to identify and resolve each specific timing need.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	An or Bn		0.11		pF
		CAB, CBA		0.22		
		GAB		0.05		
		GBAZ, SAB, SBA		0.23		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	42.34		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (see Notes 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CAB,CBA	A,B		3.5	7.3		3.5	6.7	ns
t_{PHL}				3.6	7.3		3.6	6.7	
t_{PLH}	A,B	B,A		2.2	4		2.2	3.7	ns
t_{PHL}				2	3.9		2	3.5	
t_{PLH}	SAB,SBA	A,B		2.2	4.5		2.2	4.3	ns
t_{PHL}				2.1	3.9		2.1	4	
t_{PZH}	GAB,GBAZ	A,B		1.5	2.9		1.5	2.7	ns
t_{PZL}				1.4	2.5		1.4	2.3	
Δt_{PLH}	Any	Any	0.34	1	2.22	0.34	1	2.06	ns/pF
Δt_{PHL}			0.26	0.6	1.34	0.28	0.6	1.2	
Δt_{PZH}	GAB,GBAZ	Any	0.34	1.02	2.26	0.38	1.02	2.08	ns/pF
Δt_{PZL}			0.38	0.64	1.36	0.38	0.64	1.2	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. These switching characteristics are simulations of the software macro using interconnect capacitance values for an array design having 4000 gates. Post-layout simulation uses actual interconnect capacitance values.

2. Enable and delta-enable times are measured using the conditions specified for the IV222LJ.

HDL FILE†

```
BLOCK S652LJ;
GBAZ        @INPUT;
GAB         @INPUT;
SBA         @INPUT;
SAB         @INPUT;
CBA         @INPUT;
CAB         @INPUT;
A1          @INOUT;
A2          @INOUT;
A3          @INOUT;
A4          @INOUT;
A5          @INOUT;
A6          @INOUT;
A7          @INOUT;
A8          @INOUT;
B1          @INOUT;
B2          @INOUT;
B3          @INOUT;
B4          @INOUT;
B5          @INOUT;
B6          @INOUT;
B7          @INOUT;
B8          @INOUT;
STRUCTURE
INV1        :IV140LJ    SBA,SBAZ;
INV10       :IV222LJ    SNA9,GBA,A3;
INV11       :IV222LJ    SNA12,GBA,A4;
INV12       :IV110LJ    B1,SIV12;
INV13       :IV110LJ    B2,SIV13;
INV14       :IV110LJ    B3,SIV14;
INV15       :IV110LJ    B4,SIV15;
INV16       :IV110LJ    A1,SIV16;
INV17       :IV110LJ    A2,SIV17;
INV18       :IV110LJ    A3,SIV18;
INV19       :IV110LJ    A4,SIV19;
INV2        :IV140LJ    SBAZ,SBA1;
INV20       :IV222LJ    SNA15,GAB1,B1;
INV21       :IV222LJ    SNA18,GAB1,B2;
INV22       :IV222LJ    SNA21,GAB1,B3;
INV23       :IV222LJ    SNA24,GAB1,B4;
INV24       :IV222LJ    SNA27,GBA,A5;
INV25       :IV222LJ    SNA30,GBA,A6;
INV26       :IV222LJ    SNA33,GBA,A7;
INV27       :IV222LJ    SNA36,GBA,A8;
INV28       :IV110LJ    B5,SIV28;
INV29       :IV110LJ    B6,SIV29;
INV3        :IV140LJ    SAB,SABZ;
INV30       :IV110LJ    B7,SIV30;
INV31       :IV110LJ    B8,SIV31;
INV32       :IV110LJ    A5,SIV32;
INV33       :IV110LJ    A6,SIV33;
INV34       :IV110LJ    A7,SIV34;
INV35       :IV110LJ    A8,SIV35;
INV36       :IV222LJ    SNA39,GAB1,B5;
INV37       :IV222LJ    SNA42,GAB1,B6;
INV38       :IV222LJ    SNA45,GAB1,B7;
INV39       :IV222LJ    SNA48,GAB1,B8;
INV4        :IV140LJ    SABZ,SAB1;
INV5        :IV110LJ    GAB,GABZ;
INV6        :IV140LJ    GABZ,GAB1;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the BLOCK" I/O program lines.

HDL FILE† - Continued

```
INV7    :IV140LJ    GBAZ,GBA;
INV8    :IV222LJ    SNA3,GBA,A1;
INV9    :IV222LJ    SNA6,GBA,A2;
NA1     :NA210LJ    SBA1,FF1AZ,SNA1;
NA10    :NA210LJ    SBA1,FF1DZ,SNA10;
NA11    :NA210LJ    SBAZ,SIV15,SNA11;
NA12    :NA210LJ    SNA10,SNA11,SNA12;
NA13    :NA210LJ    SAB1,FF2AZ,SNA13;
NA14    :NA210LJ    SABZ,SIV16,SNA14;
NA15    :NA210LJ    SNA13,SNA14,SNA15;
NA16    :NA210LJ    SAB1,FF2BZ,SNA16;
NA17    :NA210LJ    SABZ,SIV17,SNA17;
NA18    :NA210LJ    SNA16,SNA17,SNA18;
NA19    :NA210LJ    SAB1,FF2CZ,SNA19;
NA2     :NA210LJ    SBAZ,SIV12,SNA2;
NA20    :NA210LJ    SABZ,SIV18,SNA20;
NA21    :NA210LJ    SNA19,SNA20,SNA21;
NA22    :NA210LJ    SAB1,FF2DZ,SNA22;
NA23    :NA210LJ    SABZ,SIV19,SNA23;
NA24    :NA210LJ    SNA22,SNA23,SNA24;
NA25    :NA210LJ    SBA1,FF3AZ,SNA25;
NA26    :NA210LJ    SBAZ,SIV28,SNA26;
NA27    :NA210LJ    SNA25,SNA26,SNA27;
NA28    :NA210LJ    SBA1,FF3BZ,SNA28;
NA29    :NA210LJ    SBAZ,SIV29,SNA29;
NA3     :NA210LJ    SNA1,SNA2,SNA3;
NA30    :NA210LJ    SNA28,SNA29,SNA30;
NA31    :NA210LJ    SBA1,FF3CZ,SNA31;
NA32    :NA210LJ    SBAZ,SIV30,SNA32;
NA33    :NA210LJ    SNA31,SNA32,SNA33;
NA34    :NA210LJ    SBA1,FF3DZ,SNA34;
NA35    :NA210LJ    SBAZ,SIV31,SNA35;
NA36    :NA210LJ    SNA34,SNA35,SNA36;
NA37    :NA210LJ    SAB1,FF4AZ,SNA37;
NA38    :NA210LJ    SABZ,SIV32,SNA38;
NA39    :NA210LJ    SNA37,SNA38,SNA39;
NA4     :NA210LJ    SBA1,FF1BZ,SNA4;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the BLOCK" I/O program lines.

HDL FILE† - Continued

```
NA40      :NA210LJ   SAB1,FF4BZ,SNA40;
:NA41     :NA210LJ   SABZ,SIV33,SNA41;
NA42      :NA210LJ   SNA40,SNA41,SNA42;
NA43      :NA210LJ   SAB1,FF4CZ,SNA43;
NA44      :NA210LJ   SABZ,SIV34,SNA44;
NA45      :NA210LJ   SNA43,SNA44,SNA45;
NA46      :NA210LJ   SAB1,FF4DZ,SNA46;
NA47      :NA210LJ   SABZ,SIV35,SNA47;
NA48      :NA210LJ   SNA46,SNA47,SNA48;
NA5       :NA210LJ   SBAZ,SIV13,SNA5;
NA6       :NA210LJ   SNA4,SNA5,SNA6;
NA7       :NA210LJ   SBA1,FF1CZ,SNA7;
NA8       :NA210LJ   SBAZ,SIV14,SNA8;
NA9       :NA210LJ   SNA7,SNA8,SNA9;
TO1       :TO010LJ   DUM,STO1;
FF1       :R2406LJ   STO1,B1,B2,B3,B4,CBA,DUM,
                     FF1AZ,DUM,FF1BZ,DUM,
                     FF1CZ,DUM,FF1DZ;
FF2       :R2406LJ   STO1,A1,A2,A3,A4,CAB,DUM,
                     FF2AZ,DUM,FF2BZ,DUM,
                     FF2CZ,DUM,FF2DZ;
FF3       :R2406LJ   STO1,B5,B6,B7,B8,CBA,DUM,
                     FF3AZ,DUM,FF3BZ,DUM,
                     FF3CZ,DUM,FF3DZ;
FF4       :R2406LJ   STO1,A5,A6,A7,A8,CAB,DUM,
                     FF4AZ,DUM,FF4BZ,DUM,
                     FF4CZ,DUM,FF4DZ;
END S652LJ;
```

† The HDL netlist format requires the "STRUCTURE" program lines to follow the BLOCK" I/O program lines.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

Testability Functions

19

TESTABILITY FUNCTIONS
FUNCTIONAL INDEX

D3030, JANUARY 1989

TEST PORT CONTROLLERS

DESCRIPTION	CELL NAME	OUTPUT DRIVE	COMMENTS	PAGE
Parallel Test Port Controller	TP000LJ	1X	Implements module selection	19-3
Global Enable and Clock Controller	TP006LJ	4X	Implements global and latch enable	19-6
Inverting Parallel Module Test Output Buffer	TP008LJ	4X	Implements a test-mode output selector using two output buffers	19-9
Inverting Parallel Module Test Input Buffer	TP009LJ	4X	Implements a test-mode input selector using two input buffers	19-12
Inverting Parallel Module Test Output Buffer	TP010LJ	4X	Implements a test-mode output selector	19-15

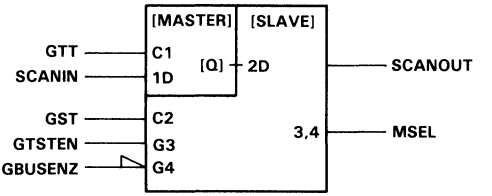
TP000LJ
PARALLEL TEST PORT CONTROLLER WITH 1X OUTPUTS

D3030, JANUARY 1989

INTERNAL CONTROLLER CELL

- **Implements Module Selection in Parallel MegaModule™ Testing (PMT) Scheme**
- **PMT Requires One Dedicated Test-Mode External Package Pin**
- **Full Parallel Input/Output PMT Ports Overlay Normal Inputs/ Outputs**
- **All PMT Inputs, Outputs, and Module Selected are Latched During Test**
- **A Single, Cascadable Parallel Test Port Controller is Required for Each MegaModule™ in the Package**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TP000LJ cell contains a master/slave shift register latch, a 3-input NOR gate, and 2 inverters. It implements a test-port controller for use in parallel module test (PMT) schemes. The parallel module test scheme is used on TSC500 Series MegaModule™ functions to provide complete testability for all MegaModules™ used in an ASIC design. The PMT scheme enables each MegaModule™, individually, and ports its inputs and outputs directly to existing package pins for testing purposes. Receiving test-mode enable signals (GTSTEN and GBUSENZ) from the package-test controller and test-sequence instructions at the SCANIN, the TP000LJ shift register latch output in combination with the NOR gate asserts the module select (MSEL) command for the MegaModule™ that it controls. Upon completion of module select, the shift register latch transfers control to the next module controller. When the controller is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TP000LJ SCANIN,GTT,GST,GTSTEN,GBUSENZ,SCANOUT,MSEL;

MegaModule is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE

INPUTS						OUTPUTS		FUNCTION
GBUSENZ	GTSTEN	MASTER			SLAVE	SCANOUT	MSEL	
		GTT†	SCANIN	OUT Q	GST†			
H	X	H	d	d	L	$SCANOUT_O$	L	Load master latch and disable module test mode
H	X	L	X	Q_O	H	Q_O	L	Load slave latch and disable module test mode
X	L	H	d	d	L	$SCANOUT_O$	L	Load master latch disable module test mode
X	L	L	X	Q_O	H	Q_O	L	Load slave latch disable module test mode
X	X	H	H	H	L	$SCANOUT_O$	X	Load H into master latch
H	X	L	X	H	H	H	L	Load H into slave latch
L	H	X	X	X	L	H	H	Enable module test mode

† GTT and GST must not be high simultaneously.

SIGNAL DESCRIPTIONS

NAME	TITLE
GBUSENZ	Global bus enable. Active when low. When high, forces MSEL low. This is done while shifting data from the master to the slave latch.
GST	Slave latch enable. When high, data is entered into the slave from the master.
GTSTEN	Global test enable. Active when high. When low, forces MSEL low.
GTT	Global test true (master latch enable). When high, data is entered into the master from SCANIN.
MSEL	Module select output. Active when high.
SCANIN	Master latch data input
SCANOUT	Slave latch output

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
t_w	Pulse duration	GST high	2.25		ns
		GTT high	2		
t_{su}	Setup time	GTT low before GST↑	1.3		ns
		SCANIN before GTT↓	2.5		
t_h	Hold time	SCANIN after GTT low	0		ns

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	GBUSENZ		0.04		pF
		GST		0.03		
		GTSTEN		0.05		
		GTT		0.04		
		SCANIN		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.7		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	GBUSENZ	MSEL	0.18	0.27	0.48	0.18	0.27	0.45	ns
t_{PHL}			0.3	0.41	0.6	0.3	0.41	0.57	
t_{PLH}	GST	SCANOUT	0.46	1	2.09	0.46	1	1.95	ns
t_{PHL}			0.16	0.79	1.91	0.18	0.79	1.75	
t_{PLH}	GTSTEN	MSEL	0.2	0.68	1.54	0.21	0.68	1.41	ns
t_{PHL}			0.25	0.54	1.08	0.26	0.54	1	
t_{PLH}	GST	MSEL	0.52	1.24	2.67	0.54	1.24	2.48	ns
t_{PHL}			0.22	0.95	2.28	0.24	0.95	2.09	
Δt_{PLH}	GBUSENZ	MSEL	1.03	3.08	6.84	1.1	3.08	6.29	ns/pF
Δt_{PHL}			0.72	1.62	3.28	0.78	1.62	2.96	
Δt_{PLH}	GST	SCANOUT	0.43	1.1	2.29	0.46	1.1	2.11	ns/pF
Δt_{PHL}			0.35	0.76	1.51	0.37	0.76	1.36	
Δt_{PLH}	GTSTEN	MSEL	1.08	3.11	6.85	1.16	3.11	6.29	ns/pF
Δt_{PHL}			0.48	1.04	2.08	0.51	1.04	1.87	
Δt_{PLH}	GST	MSEL	1.08	3.11	6.79	1.16	3.11	6.27	ns/pF
Δt_{PHL}			0.57	1.23	2.46	0.62	1.23	2.22	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

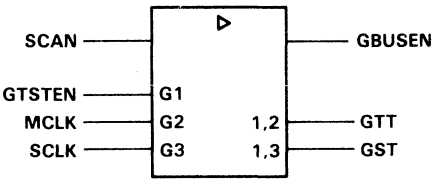
TP006LJ GLOBAL ENABLE AND TEST PORT CLOCK CONTROLLER WITH 4X OUTPUTS

D3030, JANUARY 1989

INTERNAL CONTROLLER CELL

- **Implements Global Test Bus and Latch Enable In Parallel MegaModule™ Testing (PMT) Scheme**
- **PMT Scheme Requires One Dedicated Test-Mode External Package Pin**
- **Full Parallel Input/Output PMT Ports Overlay Normal Inputs/ Outputs**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TP006LJ cell contains a buffer with 4X output drive and two 3-input AND gates with 4X output drive. It implements a global bus enable and test-port latch controller for use in parallel module test (PMT) schemes. The parallel module test scheme is used on TSC500 Series MegaModule™ functions to provide complete testability for all MegaModules™ used in an ASIC design. The PMT scheme enables each MegaModule™, individually, and ports its inputs and outputs directly to existing package pins for testing purposes. When an off-chip test-mode enable signal (SCAN) is received, the on-chip global bus enable (GBUSEN) output is asserted. After this, an off-chip global test enable (GTSTEN) signal will condition the two AND gates to pass both off-chip master clock (MCLK) and slave clock (SCLK) to all on-chip parallel test port controller (TP000LJ) latches. Each MegaModule™ is then sequentially selected and enabled for test through its associated parallel test port controller. The off-chip test-mode enable and global test enable signals are normally generated by the device test program. When the controller is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TP006LJ SCAN,MCLK,SCLK,GTSTEN,GBUSEN,GTT,GST;

MegaModule is a trademark of Texas Instruments Incorporated.

TP006LJ GLOBAL ENABLE AND TEST PORT CLOCK CONTROLLER WITH 4X OUTPUTS

D3030, JANUARY 1989

FUNCTION TABLE

INPUTS				OUTPUTS			FUNCTION
SCAN	GTSTEN	MCLK	SCLK	GBUSEN	GTT†	GST†	
L	X	X	X	L	L	L	Disable test mode
H	L	X	X	H	L	L	Disable global latch strobes GTT and GST
H	H	H	L	H	H	L	Enable global test bus and nonoverlapping latch strobes GTT and GST
H	H	L	H	H	L	H	

† GTT and GST must not be high simultaneously.

SIGNAL DESCRIPTIONS

NAME	TITLE
SCAN	Test mode select input
GTSTEN	Global latch strobe enable output. Active when high.
MCLK	Master latch strobe input
SCLK	Slave latch strobe input
GBUSEN	Global bus enable output. Active when high.
GTT	Master latch strobe output (global test true). Active when high.
GST	Slave latch strobe output. Active when high.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
t_w	Pulse duration	SCLK high	2.25		ns
		MCLK high	2		
t_{su}	Setup time	MCLK low before SCLK↑	1.3		ns
		SCAN high before MCLK↓	4.5		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	GTSTEN		0.12		pF
		MCLK		0.05		
		SCAN		0.06		
		SCLK		0.05		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	3.28		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	GTSTEN	GTT	0.32	0.86	1.95	0.34	0.86	1.76	ns
t_{PHL}			0.29	0.8	1.73	0.3	0.8	1.59	
t_{PLH}	GTSTEN	GST	0.32	0.86	1.95	0.34	0.86	1.76	ns
t_{PHL}			0.29	0.8	1.73	0.3	0.8	1.59	
t_{PLH}	MCLK	GTT	0.31	0.85	1.89	0.33	0.85	1.72	ns
t_{PHL}			0.31	0.81	1.8	0.33	0.81	1.64	
t_{PLH}	SCLK	GST	0.31	0.85	1.89	0.33	0.85	1.72	ns
t_{PHL}			0.31	0.81	1.8	0.33	0.81	1.64	
t_{PLH}	SCAN	GBUSEN	0.26	0.6	1.14	0.29	0.6	1.05	ns
t_{PHL}			0.3	0.72	1.49	0.32	0.72	1.36	
t_{PLH}	SCAN	GTT	0.47	1.32	2.92	0.51	1.32	2.65	ns
t_{PHL}			0.5	1.49	3.37	0.54	1.49	3.08	
t_{PLH}	SCAN	GST	0.47	1.32	2.92	0.51	1.32	2.65	ns
t_{PHL}			0.5	1.49	3.37	0.54	1.49	3.08	
Δt_{PLH}	GTSTEN	GTT	0.12	0.3	0.69	0.13	0.3	0.63	ns/pF
Δt_{PHL}			0.13	0.24	0.52	0.14	0.24	0.48	
Δt_{PLH}	GTSTEN	GST	0.12	0.3	0.69	0.13	0.3	0.63	ns/pF
Δt_{PHL}			0.13	0.24	0.52	0.14	0.24	0.48	
Δt_{PLH}	MCLK	GTT	0.13	0.3	0.69	0.13	0.3	0.63	ns/pF
Δt_{PHL}			0.13	0.26	0.53	0.13	0.26	0.49	
Δt_{PLH}	SCLK	GST	0.13	0.3	0.69	0.13	0.3	0.63	ns/pF
Δt_{PHL}			0.13	0.26	0.53	0.13	0.26	0.49	
Δt_{PLH}	SCAN	GBUSEN	0.1	0.27	0.56	0.1	0.27	0.52	ns/pF
Δt_{PHL}			0.11	0.24	0.5	0.11	0.24	0.46	
Δt_{PLH}	SCAN	GTT	0.24	0.69	1.56	0.26	0.69	1.43	ns/pF
Δt_{PHL}			0.25	0.54	1.16	0.25	0.54	1.06	
Δt_{PLH}	SCAN	GST	0.24	0.69	1.56	0.26	0.69	1.43	ns/pF
Δt_{PHL}			0.25	0.54	1.16	0.25	0.54	1.06	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

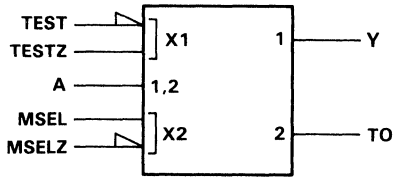
TP008LJ
INVERTING PARALLEL MODULE TEST OUTPUT BUFFER WITH 4X OUTPUTS

D3030, JANUARY 1989

INTERNAL BUFFER CELL

- **Implements Output Buffer for Use in Parallel MegaModule™ Testing (PMT) Scheme**
- **PMT Scheme Requires One Dedicated Test-Mode External Package Pin**
- **Full Parallel Input/Output PMT Ports Overlay Normal Inputs/ Outputs**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TP008LJ cell contains two internal inverting output buffers. It implements a test-mode output selector for use in parallel module test (PMT) schemes. The parallel module test scheme can be used on TSC500 Series designs to provide increased levels of testability. The PMT scheme selectively enables and disables modules used in the design and ports inputs and outputs directly to existing package pins for testing purposes. The TP008LJ buffers incorporate two transmission gates that route an internal output from the A input to one of two outputs. The data path A to Y is active when TEST and MSEL are low and TESTZ and MSELZ are high. The test path A to TO is active when logic levels at TEST/TESTZ and MSEL/MSELZ are reversed. The test output buffer is designed for TEST/TESTZ and MSEL/MSELZ pairs to be driven with complementary logic levels. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TP008LJ A,TEST,TESTZ,MSEL,MSELZ,TO,Y;

MegaModule is a trademark of Texas Instruments Incorporated.

TP008LJ
INVERTING PARALLEL MODULE TEST OUTPUT BUFFER WITH 4X OUTPUTS

D3030, JANUARY 1989

FUNCTION TABLE

INPUTS					OUTPUTS		FUNCTION
A	TEST	TESTZ	MSEL	MSELZ	Y	TO	
a†	L	L	L	L	(ā)‡	(ā)‡	Not recommended
a†	L	H	L	H	ā‡	Z	Normal mode
a†	H	L	H	L	Z	ā	Test mode
a†	H	H	H	H	(ā)‡	(ā)‡	Not recommended

† a = Logic level H or L.
‡ (a) = Weak logic level H or L resulting from activation of only one half of a CMOS transmission gate.

SIGNAL DESCRIPTIONS

NAME	TITLE
A	Data input
TEST, TESTZ	Complementary data-path select inputs
MSEL, MSELZ	Complementary test-path select inputs
TO	Test internal output
Y	Data internal output

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A		0.23		pF
		TEST		0.09		
		TESTZ		0.05		
		MSEL		0.07		
		MSELZ		0.06		
C_o	Output capacitance	Y		0.11		pF
		TO		0.07		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1.08		pF

TP008LJ
INVERTING PARALLEL MODULE TEST OUTPUT BUFFER WITH 4X OUTPUTS

D3030, JANUARY 1989

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.19	0.33	0.58	0.2	0.33	0.55	ns
t_{PHL}				0.13	0.33	0.59	0.14	0.33	0.57	
t_{PLH}	A	TO	$R_L = \infty$	0.19	0.33	0.58	0.2	0.33	0.55	ns
t_{PHL}				0.13	0.33	0.59	0.14	0.33	0.57	
t_{PZH}	TEST	Y	R_L = 40 kΩ to GND	0	0.15	0.28	0	0.15	0.29	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0	0.03	0.25	0	0.03	0.24	
t_{PHZ}	TEST	Y	R_L = 40 kΩ to GND		4.42			4.42		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		2.26			2.26		
t_{PZH}	TESTZ	Y	R_L = 40 kΩ to GND	0	0.15	0.28	0	0.15	0.29	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0	0.03	0.25	0	0.03	0.24	
t_{PHZ}	TESTZ	Y	R_L = 40 kΩ to GND		4.42			4.42		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		2.26			2.26		
t_{PZH}	MSEL	TO	R_L = 40 kΩ to GND	0.08	0.3	0.42	0.09	0.3	0.44	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0	0.18	0.4	0	0.18	0.39	
t_{PHZ}	MSEL	TO	R_L = 40 kΩ to GND		4.28			4.28		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		2.11			2.11		
t_{PZH}	MSELZ	TO	R_L = 40 kΩ to GND	0.08	0.3	0.42	0.09	0.3	0.44	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0	0.18	0.4	0	0.18	0.39	
t_{PHZ}	MSELZ	TO	R_L = 40 kΩ to GND		4.28			4.28		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		2.11			2.11		
Δt_{PLH}	A	Y	$R_L = \infty$	0.14	0.37	0.81	0.15	0.37	0.74	ns/pF
Δt_{PHL}				0.2	0.34	0.68	0.2	0.34	0.61	
Δt_{PLH}	A	TO	$R_L = \infty$	0.14	0.37	0.81	0.15	0.37	0.74	ns/pF
Δt_{PHL}				0.2	0.34	0.68	0.2	0.34	0.61	
Δt_{PZH}	TEST	Y	R_L = 40 kΩ to GND	0.27	0.35	0.67	0.27	0.35	0.6	ns/pF
Δt_{PZL}			R_L = 20 kΩ to V_{CC}	0.32	0.42	0.65	0.32	0.42	0.59	
Δt_{PZH}	TESTZ	Y	R_L = 40 kΩ to GND	0.27	0.35	0.67	0.27	0.35	0.6	ns/pF
Δt_{PZL}			R_L = 20 kΩ to V_{CC}	0.32	0.42	0.65	0.32	0.42	0.59	
Δt_{PZH}	MSEL	TO	R_L = 40 kΩ to GND	0.27	0.35	0.66	0.27	0.35	0.59	ns/pF
Δt_{PZL}			R_L = 20 kΩ to V_{CC}	0.32	0.42	0.65	0.33	0.42	0.59	
Δt_{PZH}	MSELZ	TO	R_L = 40 kΩ to GND	0.27	0.35	0.66	0.27	0.35	0.59	ns/pF
Δt_{PZL}			R_L = 20 kΩ to V_{CC}	0.32	0.42	0.65	0.33	0.42	0.59	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

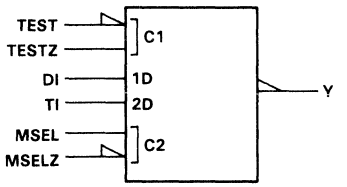
TP009LJ INVERTING PARALLEL MODULE TEST INPUT BUFFER WITH 4X OUTPUTS

D3030, JANUARY 1989

INTERNAL BUFFER CELL

- **Implements Input Buffer for Use in Parallel MegaModule™ Testing (PMT) Scheme**
- **PMT Scheme Requires One Dedicated Test-Mode External Package Pin**
- **Full Parallel Input/Output PMT Ports Overlay Normal Inputs/ Outputs**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TP009LJ cell contains two internal inverting input buffers. It implements a test-mode input selector for use in parallel module test (PMT) schemes. The test input buffer is designed for TEST/TESTZ and MSEL/MSELZ pairs to be driven with complementary logic levels. The parallel module test scheme can be used on TSC500 Series designs to provide increased levels of testability. The PMT scheme selectively enables and disables modules used in the design and ports inputs and outputs directly to existing package pins for testing purposes. The TP009LJ buffers incorporate two transmission gates that select activation of a data input, DI, or test input, TI, that is then latched into a bus holder. The data path DI to Y is active when TEST and MSEL are low and TESTZ and MSELZ are high. The test input is active when logic levels at TEST/TESTZ and MSEL/MSELZ are reversed. The test input buffer is designed for TEST/TESTZ and MSEL/MSELZ pairs to be driven with complementary logic levels. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TP009LJ DI,TI,TEST,TESTZ,MSEL,MSELZ,Y;

MegaModule is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TP009LJ INVERTING PARALLEL MODULE TEST INPUT BUFFER

D3030, JANUARY 1989

FUNCTION TABLE

INPUTS†						OUTPUT	FUNCTION
DI	TEST	TESTZ	TI	MSEL	MSELZ	Y	
X	L	L	X	L	L	?	Not recommended
a‡	L	H	X	L	H	$\overline{a}$	Normal mode
X	H	L	a‡	H	L	$\overline{a}$	Test mode
X	H	L	X	L	H	Y_0	Not selected (hold)
X	H	H	X	H	H	?	Not recommended

† Input combinations not shown are not recommended.
‡ a = Logic level H or L at input.

SIGNAL DESCRIPTIONS

NAME	TITLE
DI	Data input
TI	Test input
TEST, TESTZ	Complementary data-path select inputs
MSEL, MSELZ	Complementary test-path select inputs
Y	Data/test internal output

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	DI		0.11		pF
		TI		0.1		
		TEST		0.08		
		TESTZ		0.05		
		MSEL		0.07		
		MSELZ		0.05		
C_o	Output capacitance	Y		0.23		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	0.8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	DI	Y	0.26	0.47	0.85	0.27	0.47	0.79	ns
t_{PHL}			0.25	0.46	0.76	0.26	0.46	0.71	
t_{PLH}	TI	Y	0.29	0.51	0.95	0.3	0.51	0.89	ns
t_{PHL}			0.22	0.44	0.73	0.24	0.44	0.69	
t_{PLH}	MSEL, MSELZ	Y	0.24	0.37	0.35	0.25	0.37	0.36	ns
t_{PLH}			0.02	0.3	0.49	0.04	0.3	0.48	
t_{PLH}	TEST, TESTZ	Y	0.05	0.22	0.24	0.05	0.22	0.25	ns
t_{PHL}			0	0.13	0.32	0	0.13	0.31	
Δt_{PLH}	DI	Y	0.22	0.59	1.31	0.23	0.59	1.2	ns/pF
Δt_{PHL}			0.23	0.45	0.96	0.24	0.45	0.86	
Δt_{PLH}	TI	Y	0.26	0.73	1.59	0.28	0.73	1.46	ns/pF
Δt_{PHL}			0.24	0.47	1.01	0.24	0.47	0.9	
Δt_{PLH}	MSEL, MSELZ	Y	0.22	0.58	1.56	0.22	0.58	1.41	ns/pF
Δt_{PHL}			0.34	0.47	0.98	0.34	0.47	0.88	
Δt_{PLH}	TEST,TESTZ	Y	0.22	0.45	1.21	0.23	0.45	1.09	ns/pF
Δt_{PHL}			0.33	0.46	0.94	0.33	0.46	0.84	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

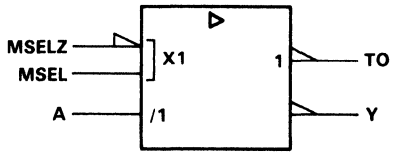
TP010LJ
INVERTING PARALLEL MODULE TEST OUTPUT BUFFER WITH 4X OUTPUTS

D3030, JANUARY 1989

INTERNAL BUFFER CELL

- **Implements Internal Output Buffer for Use in Parallel MegaModule™ Testing (PMT) Scheme**
- **PMT Scheme Requires One Dedicated Test-Mode External Package Pin**
- **Full Parallel Input/Output PMT Ports Overlay Normal Inputs/ Outputs**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The TP010LJ cell contains an inverting buffer with 4X output drive. It implements an internal test-mode output selector for use in parallel module test (PMT) schemes. The parallel module test scheme can be used on TSC500 Series designs to provide increased levels of testability. The PMT scheme selectively enables and disables modules used in the design and ports inputs and outputs directly to existing package pins for testing purposes. The TP010LJ buffer incorporates a transmission gate to select activation of the test output. The inverting data path, A to Y, is active continuously while the test output is active only when MSEL is high and MSELZ is low. The test output buffer is designed for MSEL and MSELZ to be driven with complementary logic levels. When the buffer is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: TP010LJ A,MSEL,MSELZ,TO,Y;

MegaModule is a trademark of Texas Instruments Incorporated.

TP010LJ
INVERTING PARALLEL MODULE TEST OUTPUT BUFFER WITH 4X OUTPUTS

D3030, JANUARY 1989

FUNCTION TABLE

INPUTS			OUTPUTS		FUNCTION
A	MSEL	MSELZ	Y	TO	
a†	L	L	$\bar{a}$	$(\bar{a})$‡	Not recommended
a†	L	H	$\bar{a}$	Z	Normal mode
a†	H	L	$\bar{a}$	$\bar{a}$	Test mode
a†	H	H	$\bar{a}$	$(\bar{a})$‡	Not recommended

† a = Logic level H or L.
‡ (a) = Weak logic level H or L resulting from activation of only one half of a CMOS transmission gate.

SIGNAL DESCRIPTIONS

NAME	TITLE
A	Data path input
MSEL, MSELZ	Complementary mode-select inputs
Y	Data path output
TO	Test output

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	A		0.23		pF
		MSEL		0.09		
		MSELZ		0.06		
C_o	Output capacitance	TO		0.07		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	1		pF

TP010LJ
INVERTING PARALLEL MODULE TEST OUTPUT BUFFER WITH 4X OUTPUTS

D3030, JANUARY 1989

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y	$R_L = \infty$	0.14	0.23	0.39	0.14	0.23	0.38	ns
t_{PHL}				0.08	0.22	0.42	0.08	0.22	0.41	
t_{PLH}	A	TO	$R_L = \infty$	0.23	0.46	0.84	0.25	0.46	0.78	ns
t_{PHL}				0.2	0.46	0.77	0.22	0.46	0.73	
t_{PZH}	MSEL	TO	R_L = 40 kΩ to GND	0.05	0.28	0.44	0.07	0.28	0.44	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0	0.13	0.38	0	0.13	0.37	
t_{PHZ}	MSEL	TO	R_L = 40 kΩ to GND		4.46			4.46		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		2.18			2.18		
t_{PZH}	MSELZ	TO	R_L = 40 kΩ to GND	0.05	0.28	0.44	0.07	0.28	0.44	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0	0.13	0.38	0	0.13	0.37	
t_{PHZ}	MSELZ	TO	R_L = 40 kΩ to GND		4.46			4.46		ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}		2.18			2.18		
Δt_{PLH}	A	Y	$R_L = \infty$	0.13	0.29	0.52	0.14	0.29	0.47	ns/pF
Δt_{PHL}				0.14	0.25	0.35	0.17	0.25	0.32	
Δt_{PLH}	A	TO	$R_L = \infty$	0.15	0.35	0.76	0.15	0.35	0.7	ns/pF
Δt_{PHL}				0.18	0.29	0.62	0.18	0.29	0.56	
Δt_{PZH}	MSEL	TO	R_L = 40 kΩ to GND	0.26	0.32	0.55	0.26	0.32	0.49	ns/pF
Δt_{PZL}			R_L = 20 kΩ to V_{CC}	0.3	0.41	0.57	0.31	0.41	0.52	
Δt_{PZH}	MSELZ	TO	R_L = 40 kΩ to GND	0.26	0.32	0.55	0.26	0.32	0.49	ns/pF
Δt_{PZL}			R_L = 20 kΩ to V_{CC}	0.3	0.41	0.57	0.31	0.41	0.52	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

Random Access Memories 20

STATIC RANDOM-ACCESS MEMORIES
GENERAL INFORMATION

D3030, APRIL 1988

The static random-access memory (RAM) is implemented in TI's 1-μm CMOS technology and is intended for use in designs using the TSC500 Series standard cell library. Full parallel access with separate inputs and 3-state outputs is provided. Power is reduced to a standby level in the power-down mode. A parallel testability scheme is included in the RAM with test mode selection for accessing inputs and outputs through use of the parallel test-port controller cell, TP000LJ, and the global-test enable/controller cell, TP006LJ. Write cycle times of 25, 27, 30, and 31 ns are available in this RAM series.

An independant output enable, GZ, is provided for the 3-state outputs to interface the memory directly with internal data buses. A separate enable input, EZ, is provided for enabling or disabling the entire memory. When disabled, the memory assumes a powered-down state. An individual write input, WZ, enters new data into the addressed word location when taken low. The memory contains embedded buffers to reduce input loading.

Common characteristics for all RAM types in this series are included in the following tables. Logic symbols and unique electrical and switching characteristics for individual RAM cells are provided on subsequent pages. Twelve different RAM cells are provided and structured as shown in the table below:

RAM CELL FUNCTIONAL INDEX

CELL NAME	ORGANIZATION		RELATIVE CELL AREA TO NA210LJ	PAGE
	WORDS	WORD LENGTH		
RH000LJ	64	4	3866	20-9
RH001LJ	64	8	3866	20-11
RH002LJ	128	4	5855	20-13
RH003LJ	128	8	5855	20-15
RH004LJ	256	4	9834	20-17
RH005LJ	256	8	9834	20-19
RH006LJ	512	4	6526	20-21
RH007LJ	512	8	6526	20-23
RH008LJ	1024	4	5564	20-25
RH009LJ	1024	8	8209	20-27
RH010LJ	2048	4	12114	20-29
RH011LJ	2048	8	12114	20-31

D3030, APRIL 1988

FUNCTION TABLES

TABLE 1. NORMAL-MODE FUNCTION TABLE (ALL RAM TYPES)

INPUTS						OUTPUTS	MEMORY MODE
	ENABLE			ADDRESS	DATA	DATA	
TEST	EZ	GZ	WZ	A0 THRU An	D0 THRU Dn	Q0 THRU Qn	
L	H	X	X	X	X	Hi-Z	Power-down
L	L	L	H	Valid address	X	Data out	Read
L	L	L	L	Valid address	Valid data	Hi-Z	Write
L	L	H	L	Valid address	Valid data	Hi-Z	Write
L	L	H	H	X	X	Hi-Z	–
H	X	X	X	X	X	Hi-Z	Test (See Note 1)

NOTE 1: Data written in the normal mode is retained when the RAM module is placed in the test mode.

TABLE 2. TEST-MODE FUNCTION TABLE (ALL RAM TYPES)

INPUTS					OUTPUTS	MEMORY MODE
			ADDRESS	DATA	DATA	
TEST	MSEL	TIn	TIn THRU TIn	TI0 THRU TIn	TO0 THRU TOn	
H	L	X	X	X	Hi-Z	Power-down
H	H	H	Valid address	X	Data out	Test read
H	H	L	Valid address	Valid data	H	Test write
L	X	X	X	X	Hi-Z	Normal (See Note 2)

NOTE 2: Data written in the test mode is retained when the RAM module is returned to the normal mode.

NORMAL-MODE SIGNAL DESCRIPTIONS

NAME(S)	TITLE	FUNCTION
TEST	Test Enable	When low, the normal mode is enabled and the signals in this table are used. When high, the test mode is enabled and the other signals in this table are disabled. See Note 1.
A0 - An	Address	Address inputs
D0 - Dn	Data In	Data inputs
EZ	Memory Enable	When low, the memory is enabled. When high, the memory is disabled to a power-down mode and the Q outputs are in a high-impedance state. Data is retained during power-down.
GZ	Output Enable	When low, data appears at the memory output. When high, the Q outputs are in a high-impedance state (data is retained).
Q0 - Qn	Data Out	Data outputs
WZ	Read/Write	When low, data is written into the addressed locations and the Q outputs are in a high-impedance state. When high, writing is inhibited and data from the addressed word is present at the Q outputs. See Note 3.

NOTES: 1. Data written in the normal mode is retained when the RAM module is placed in the test mode.
3. WZ or EZ must be high while changing addresses to prevent erroneously writing data into a memory location.

TEST-MODE SIGNAL DESCRIPTIONS

NAME(S)	TITLE	FUNCTION
TEST	Test Enable	When high, the test mode is enabled. When low, the other signals described in this table are disabled.
MSEL	Memory Select	When high, the memory module is enabled for testing. When low, the memory is disabled to a powered-down mode and the test outputs are in a high-impedance state. Test data is retained during power-down. See Note 4.
TIn - TIn	Test Address	Test address inputs
TI0 - TIn	Test Data In	Test data inputs
TO0 - TOn	Test Data Out	Test data outputs
TIn	Test Write	When low, data is written into the test-address locations and the test outputs are in a high-impedance state. When high, test-writing is inhibited and data from the addressed word is present at the TO outputs. See Note 4.

NOTE 4: MSEL must be low or TIn must be high while changing test addresses to prevent erroneously writing data into a memory test location.

D3030, APRIL 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(see Note 5)

PARAMETER		RH0nnLJ					UNIT	FIG
		00 THRU 07	08	09	10	11		
			MIN					
$t_{su(AE)}$	Address setup time before enable	0	0	0	0	0	ns	2
$t_{h(EA)}$	Address hold time after enable	5	5	5	5	5	ns	2
$t_{su(AW)}$	Address setup time before write	0	0	0	0	0	ns	1
$t_{h(WA)}$	Address hold time after write	5	5	5	5	5	ns	1
$t_{su(E)}$	Memory enable setup time (See Note 6)	25	27	27	30	31	ns	1,2
$t_{su(D)}$	Data setup time (See Note 6)	10	10	10	10	10	ns	1,2
$t_{h(D)}$	Data hold time (See Note 6)	5	5	5	5	5	ns	1,2
$t_{su(WL)}$	Write-low setup time (See Note 6)	15	15	15	15	15	ns	1,2
$t_{su(WH)}$	Write-high setup time before read	0	0	0	0	0	ns	3
$t_{h(WH)}$	Write-high hold time after read							3
$t_{c(W)}$	Write cycle time	30	32	32	35	36	ns	1,2

NOTES: 5. Timing requirements for the test-mode inputs and outputs are generally the same as the normal mode. The requirements are not specified because the test mode normally operates at speeds less than 1 MHz.

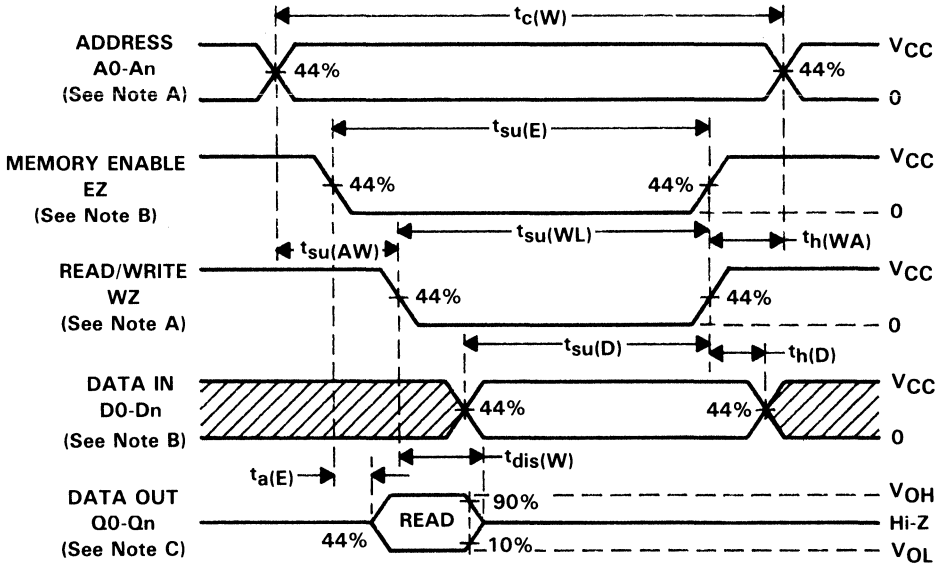
6. Memory enable setup time $t_{su(E)}$, data setup time $t_{su(D)}$, data hold time $t_{h(D)}$, and write-low setup time $t_{su(WL)}$ are all with respect to the rise of $\overline{EZ}$ or $\overline{WZ}$, whichever occurs first.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{dis(E)}$	EZ	Any Q		6.7			6.7		ns
$t_{en(G)}$	GZ	Any Q	0.7	1.3	3	0.8	1.3	2.8	ns
$t_{dis(G)}$				5.9			5.9		
$t_{en(W)}$	WZ	Any Q	0.8	2.5	5	0.8	2.5	5	ns
$t_{dis(W)}$				6.3			6.3		
$\Delta t_{a(A)}$	Any A	Any Q	0.2	1	2.3	0.2	1	2.1	ns/pF
$\Delta t_{a(E)}$	EZ	Any Q	0.2	1	2.3	0.2	1	2.1	ns/pF
$\Delta t_{en(G)}$	GZ	Any Q	0.2	1	2.3	0.2	1	2.1	ns/pF
$\Delta t_{en(W)}$	WZ	Any Q	0.2	1	2.3	0.2	1	2.1	ns/pF

† For $t_{a(A)}$ and $t_{a(E)}$ see individual data sheet.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. EZ or WZ must be high during address transitions.

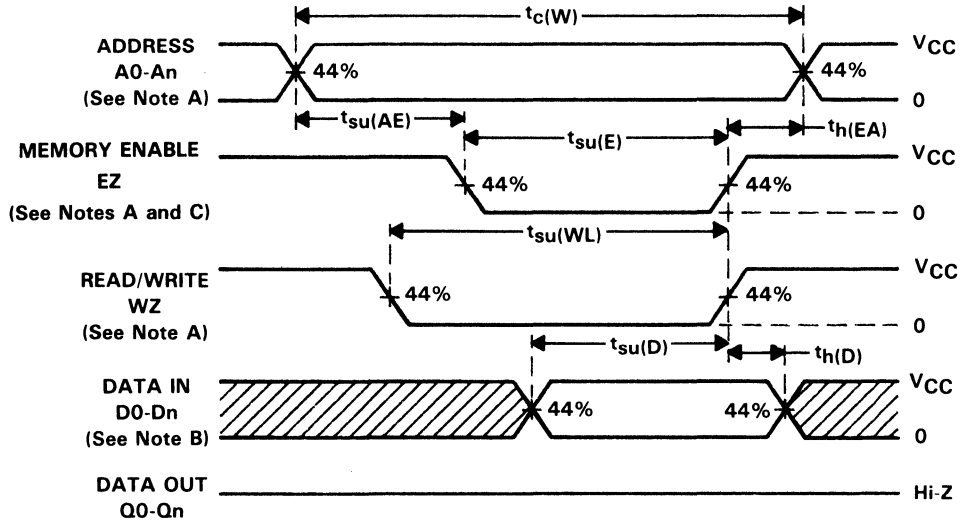
B. Memory enable setup time $t_{su(E)}$, data setup time $t_{su(D)}$, data hold time $t_{h(D)}$, and write-low setup time $t_{su(WL)}$ are all with respect to the rise of EZ or WZ, whichever occurs first.

C. This write cycle is used if output enable (GZ) is low.

FIGURE 1. WRITE CYCLE 1

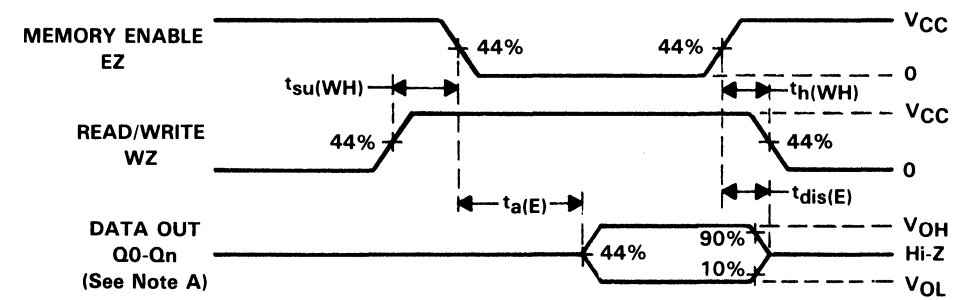
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



NOTES: A. EZ or WZ must be high during address transitions.
B. Memory enable setup time $t_{su(E)}$, data setup time $t_{su(D)}$, data hold time $t_{h(D)}$, and write-low setup time $t_{su(WL)}$ are all with respect to the rise of EZ or WZ, whichever occurs first.
C. This write cycle is used if output enable (GZ) is high.

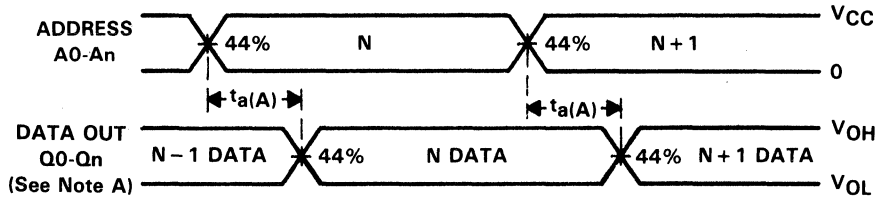
FIGURE 2. WRITE CYCLE 2



NOTE A: GZ is low and address is valid.

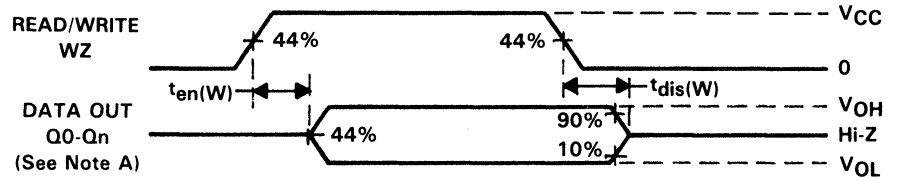
FIGURE 3. MEMORY-ENABLE ACCESS TIME

PARAMETER MEASUREMENT INFORMATION



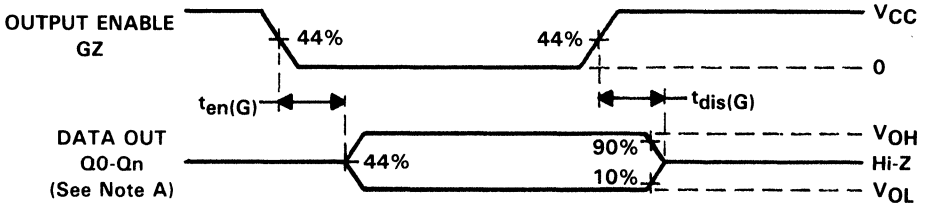
NOTE A: EZ and GZ are low and WZ is high.

FIGURE 4. ADDRESS ACCESS TIME



NOTE A: EZ and GZ are low and address is valid.

FIGURE 5. OUTPUT ENABLE AND DISABLE FROM READ/WRITE



NOTE A: EZ is low, WZ is high and address is valid.

FIGURE 6. OUTPUT ENABLE AND DISABLE FROM OUTPUT ENABLE

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

RH000LJ 64-WORD BY 4-BIT STATIC RANDOM-ACCESS MEMORY WITH 3-STATE OUTPUTS

D3030, APRIL 1988

RANDOM-ACCESS MEMORY CELL

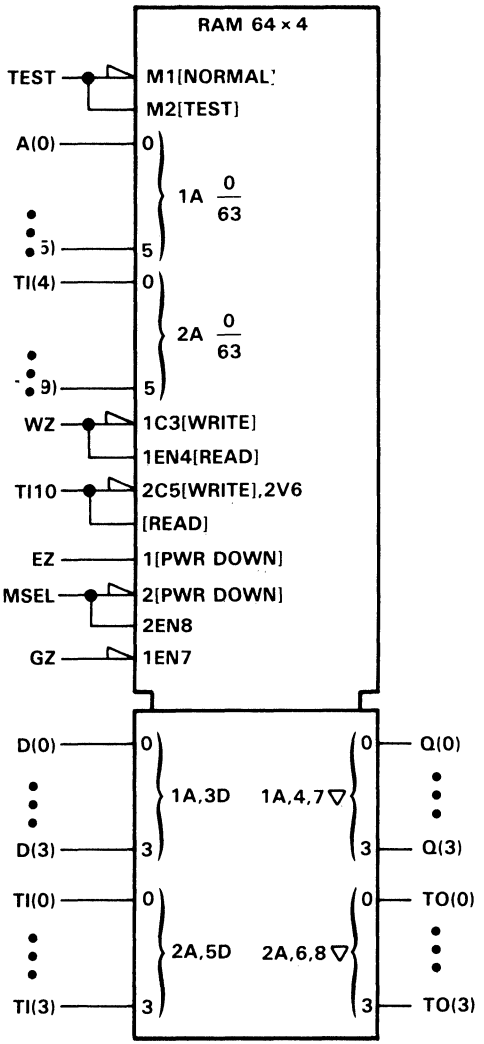
description

The RH000LJ cell is a dedicated 64-word by 4-bit static random-access memory (RAM). A parallel testability scheme is implemented in the RAM with test-mode selection for accessing inputs and outputs through use of the parallel test-port controller cell, TP000LJ, and the global test enable/ controller cell, TP006LJ.

When the RAM is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: RH000LJ D0,D1,D2,D3,TI0,TI1, TI2,TI3,A0,A1,A2,A3,A4,A5,TI4,TI5, TI6,TI7,TI8,TI9,TI10,TEST,EZ,WZ, GZ,MSEL,Q0,Q1,Q2,Q3,TO0,TO1, TO2,TO3;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TYP†	MAX	UNIT
V_T	Input threshold voltage				2.2		V
I_{CC}	Supply current	EZ = H		$V_I = V_{CC}$ or 0		10	µA
		EZ = L	−55°C to 125°C			22.5	mA
			0°C to 70°C			21	
C_i	Input capacitance	Any A, GZ, WZ			0.11		pF
		Any D			0.1		
		EZ			0.18		
C_{pd}	Equivalent power dissipation capacitance			$t_r = t_f = 1$ ns	120		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Any A	Any Q	2.6	7.6	20	2.9	7.6	18.2	ns
$t_{a(E)}$	EZ	Any Q	2.6	7.6	20	2.9	7.6	18.2	ns

† Typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.

RH001LJ 64-WORD BY 8-BIT STATIC RANDOM-ACCESS MEMORY WITH 3-STATE OUTPUTS

D3030, APRIL 1988

RANDOM-ACCESS MEMORY CELL

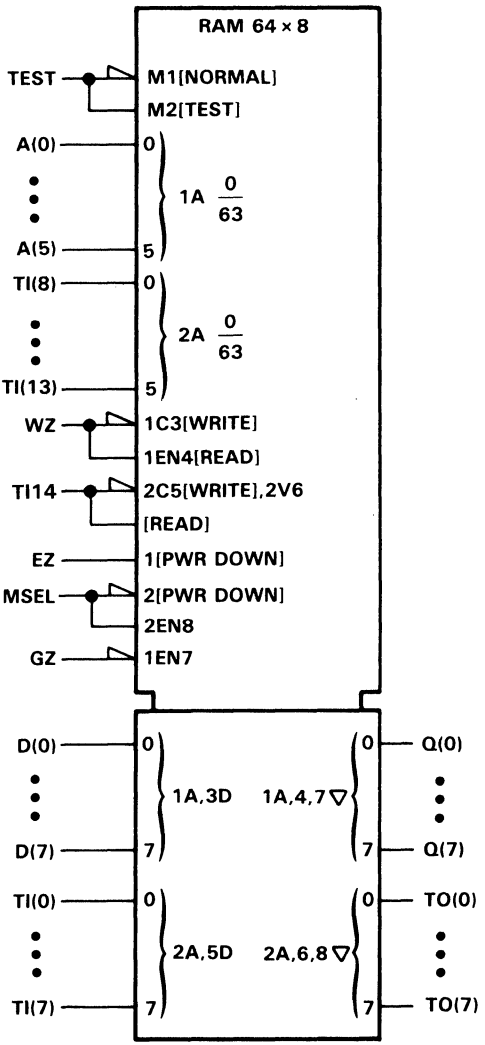
description

The RH001LJ cell is a dedicated 64-word by 8-bit static random-access memory (RAM). A parallel testability scheme is implemented in the RAM with test-mode selection for accessing inputs and outputs through use of the parallel test-port controller cell, TP000LJ, and the global test enable/ controller cell, TP006LJ.

When the RAM is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: RH001LJ D0,D1,D2,D3,D3,D4, D5,D6,D7,TI0,TI1,TI2,TI3,TI4,TI5,TI6, TI7,A0 A1,A2,A3,A4,A5,TI8,TI9,TI10, TI11,TI12,TI13,TI14,TEST,EZ,WZ, GZ,MSEL,Q0,Q1,Q2,Q3,Q4,Q5,Q6, Q7,TO0,TO1,TO2,TO3,TO4,TO5, TO6,TO7;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TYP†	MAX	UNIT
V_T	Input threshold voltage				2.2		V
I_{CC}	Supply current	EZ = H		$V_I = V_{CC}$ or 0		10	µA
		EZ = L	−55°C to 125°C		45.1		mA
			0°C to 70°C			42	
C_i	Input capacitance	Any A, GZ, WZ			0.11		pF
		Any D			0.1		
		EZ			0.18		
C_{pd}	Equivalent power dissipation capacitance			$t_r = t_f = 1$ ns	240		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Any A	Any Q	2.7	7.7	20.1	2.9	7.7	18.3	ns
$t_{a(E)}$	EZ	Any Q	2.7	7.7	20.1	2.9	7.7	18.3	ns

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

RH002LJ
128-WORD BY 4-BIT STATIC RANDOM-ACCESS MEMORY WITH 3-STATE OUTPUTS

D3030, APRIL 1988

RANDOM-ACCESS MEMORY CELL

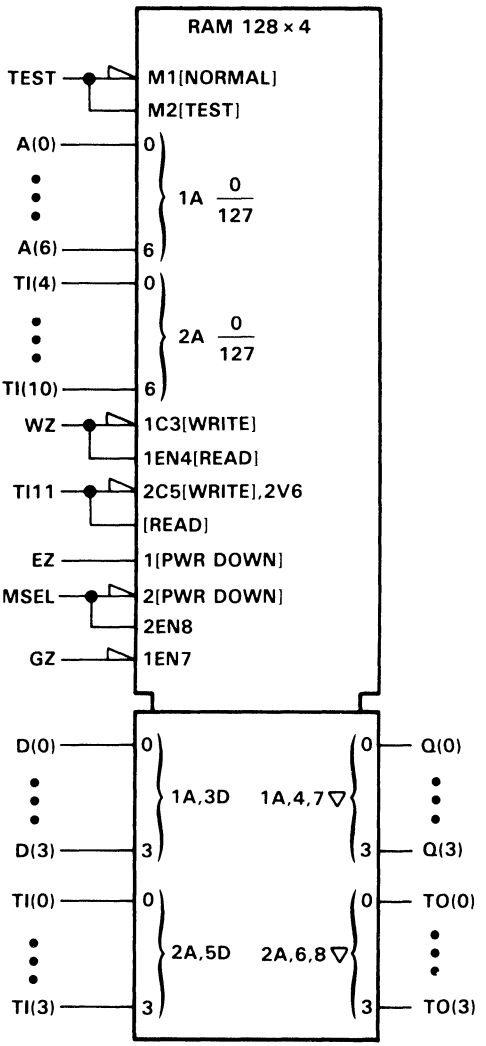
description

The RH002LJ cell is a dedicated 128-word by 4-bit static random-access memory (RAM). A parallel testability scheme is implemented in the RAM with test-mode selection for accessing inputs and outputs through use of the parallel test-port controller cell, TP000LJ, and the global test enable/controller cell, TP006LJ.

When the RAM is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: RH002LJ D0,D1,D2,D3,TI0,TI1, TI2,TI3,A0,A1,A2,A3,A4,A5,A6,TI4, TI5,TI6,TI7,TI8,TI9,TI10,TEST,EZ, WZ,GZ,MSEL,TI11,Q0,Q1,Q2,Q3, TO0,TO1,TO2,TO3;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TYP†	MAX	UNIT
V_T	Input threshold voltage				2.2		V
I_{CC}	Supply current	EZ = H		$V_I = V_{CC}$ or 0		10	µA
		EZ = L	−55°C to 125°C			22.5	mA
			0°C to 70°C			21	
C_i	Input capacitance	Any A, GZ, WZ			0.11		pF
		Any D			0.1		
		EZ			0.18		
C_{pd}	Equivalent power dissipation capacitance			$t_r = t_f = 1$ ns	120		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Any A	Any Q	2.8	8.3	21.5	3.1	8.3	19.5	ns
$t_{a(E)}$	EZ	Any Q	2.8	8.3	21.5	3.1	8.3	19.5	ns

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

RH003LJ
128-WORD BY 8-BIT STATIC RANDOM-ACCESS MEMORY WITH 3-STATE OUTPUTS

D3030, APRIL 1988

RANDOM-ACCESS MEMORY CELL

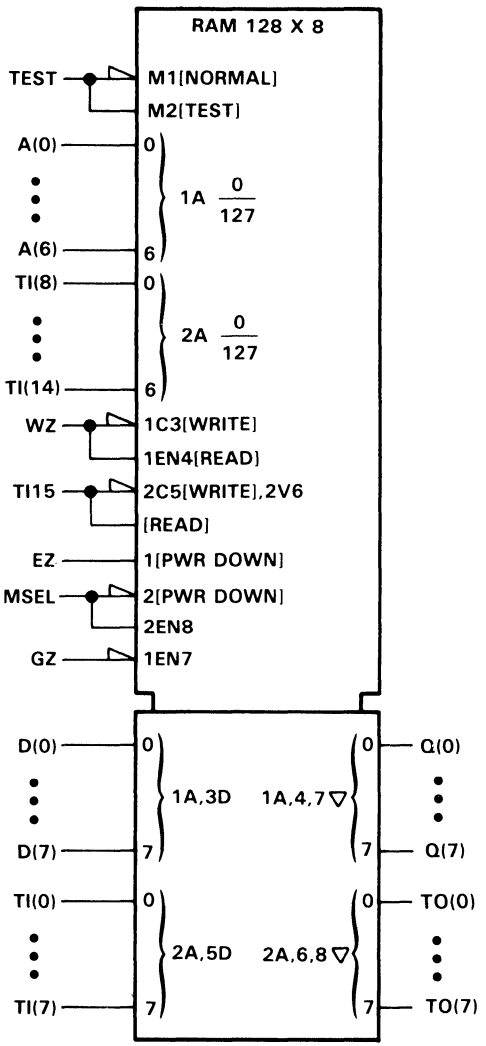
description

The RH003LJ cell is a dedicated128-word by 8-bit static random-access memory (RAM). A parallel testability scheme is implemented in the RAM with test-mode selection for accessing inputs and outputs through use of the parallel test-port controller cell, TP000LJ, and the global test enable/ controller cell, TP006LJ.

When the RAM is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: RH0u3LJ D0,D1,D2,D3,D3,D4, D5,D6,D7,TI0,TI1,TI2,TI3,TI4,TI5,TI6, TI7,A0,A1,A2,A3,A4,A5,A6,TI8,TI9, TI10,TI11,TI12,TI13,TI14,TI15,TEST, EZ,WZ,GZ,MSEL,Q0,Q1,Q2,Q3,Q4, Q5,Q6,Q7,TO0,TO1,TO2,TO3,TO4, TO5,TO6,TO7;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TYP†	MAX	UNIT
V_T	Input threshold voltage				2.2		V
I_{CC}	Supply current	EZ = H		$V_I = V_{CC}$ or 0		10	µA
		EZ = L	−55°C to 125°C			45.1	mA
			0°C to 70°C			42	
C_i	Input capacitance	Any A, GZ, WZ			0.11		pF
		Any D			0.1		
		EZ			0.18		
C_{pd}	Equivalent power dissipation capacitance			$t_r = t_f = 1$ ns	240		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Any A	Any Q	2.8	8.3	21.5	3.1	8.3	19.5	ns
$t_{a(E)}$	EZ	Any Q	2.8	8.3	21.5	3.1	8.3	19.5	ns

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

RH004LJ
256-WORD BY 4-BIT STATIC RANDOM-ACCESS MEMORY WITH 3-STATE OUTPUTS

D3030, APRIL 1988

RANDOM-ACCESS MEMORY CELL

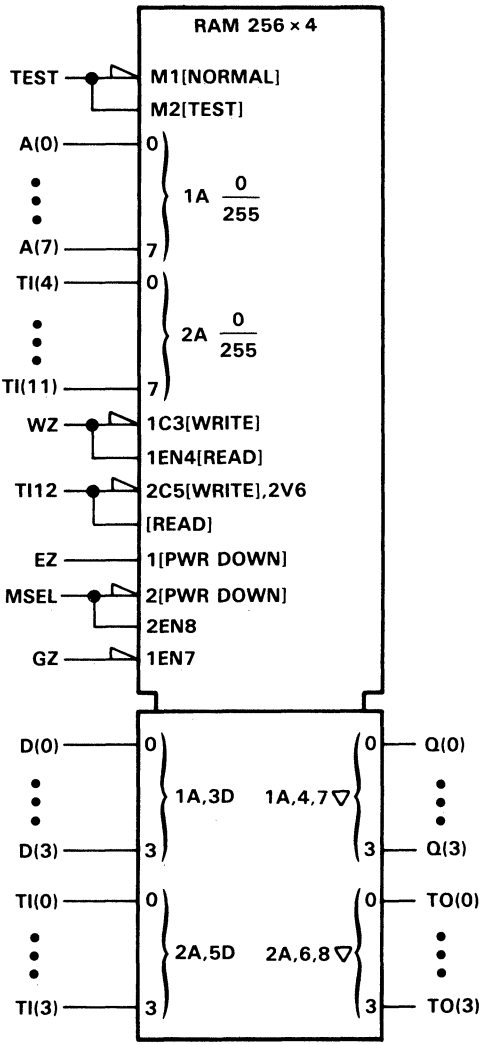
description

The RH004LJ cell is a dedicated 256-word by 4-bit static random-access memory (RAM). A parallel testability scheme is implemented in the RAM with test-mode selection for accessing inputs and outputs through use of the parallel test-port controller cell, TP000LJ, and the global test enable/ controller cell, TP006LJ.

When the RAM is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: RH004LJ D0,D1,D2,D3,TI0,TI1, TI2,TI3,A0,A1,A2,A3,A4,A5,A6,A7, TI4,TI5,TI6,TI7,TI8,TI9,TI10,TI11, TI12,TEST,EZ,WZ,GZ,MSEL,Q0,Q1, Q2,Q3,TO0,TO1,TO2,TO3;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TYP†	MAX	UNIT
V_T	Input threshold voltage				2.2		V
I_{CC}	Supply current	EZ = H		$V_I = V_{CC}$ or 0		10	μA
		EZ = L	−55°C to 125°C			22.5	mA
			0°C to 70°C			21	
C_i	Input capacitance	Any A, GZ, WZ			0.11		pF
		Any D			0.1		
		EZ			0.18		
C_{pd}	Equivalent power dissipation capacitance			$t_r = t_f = 1$ ns	120		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Any A	Any Q	3.2	9.3	24	3.5	9.3	21.8	ns
$t_{a(E)}$	EZ	Any Q	3.2	9.3	24	3.5	9.3	21.8	ns

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

RH005LJ
256-WORD BY 8-BIT STATIC RANDOM-ACCESS MEMORY WITH 3-STATE OUTPUTS

D3030, APRIL 1988

RANDOM-ACCESS MEMORY CELL

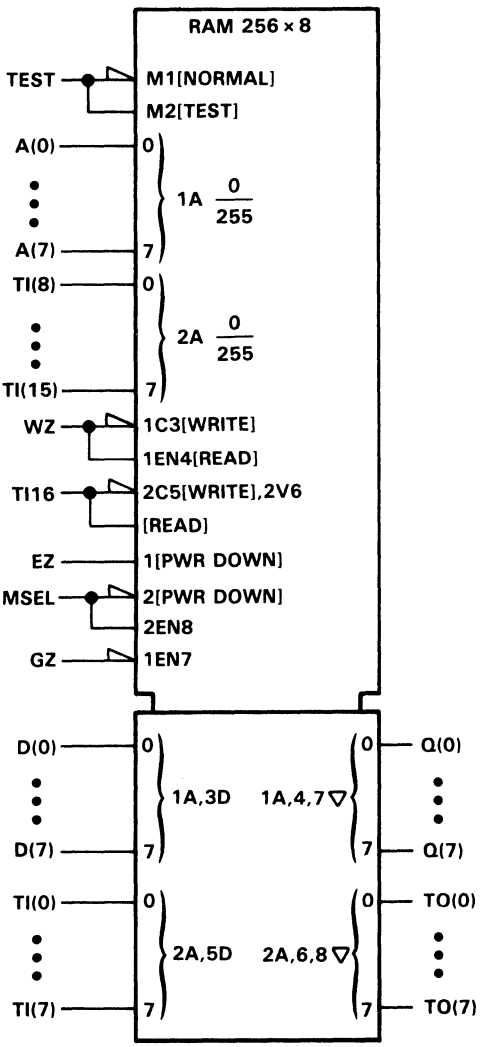
description

The RH005LJ cell is a dedicated 256-word by 8-bit static random-access memory (RAM). A parallel testability scheme is implemented in the RAM with test-mode selection for accessing inputs and outputs through use of the parallel test-port controller cell, TP000LJ, and the global test enable/ controller cell, TP006LJ.

When the RAM is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: RH005LJ D0,D1,D2,D3,D3,D4, D5,D6,D7,TI0,TI1,TI2,TI3,TI4,TI5,TI6, TI7,A0, A1,A2,A3,A4,A5,A6,A7,TI8, TI9,TI10,TI11,TI12,TI13,TI14,TI15, TI16,TEST,EZ,WZ,GZ,MSEL,Q0,Q1, Q2,Q3,Q4,Q5,Q6,Q7,TO0,TO1,TO2, TO3,TO4,TO5,TO6,TO7;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TYP†	MAX	UNIT
V_T	Input threshold voltage				2.2		V
I_{CC}	Supply current	EZ = H		$V_I = V_{CC}$ or 0		10	μA
		EZ = L	−55°C to 125°C			45.1	mA
			0°C to 70°C			42	
C_i	Input capacitance	Any A, GZ, WZ			0.11		pF
		Any D			0.1		
		EZ			0.18		
C_{pd}	Equivalent power dissipation capacitance			$t_r = t_f = 1$ ns	240		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Any A	Any Q	3.2	9.4	24.1	3.5	9.4	21.9	ns
$t_{a(E)}$	EZ	Any Q	3.2	9.4	24.1	3.5	9.4	21.9	ns

† Typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

RH006LJ
512-WORD BY 4-BIT STATIC RANDOM-ACCESS MEMORY WITH 3-STATE OUTPUTS

D3030, APRIL 1988

RANDOM-ACCESS MEMORY CELL

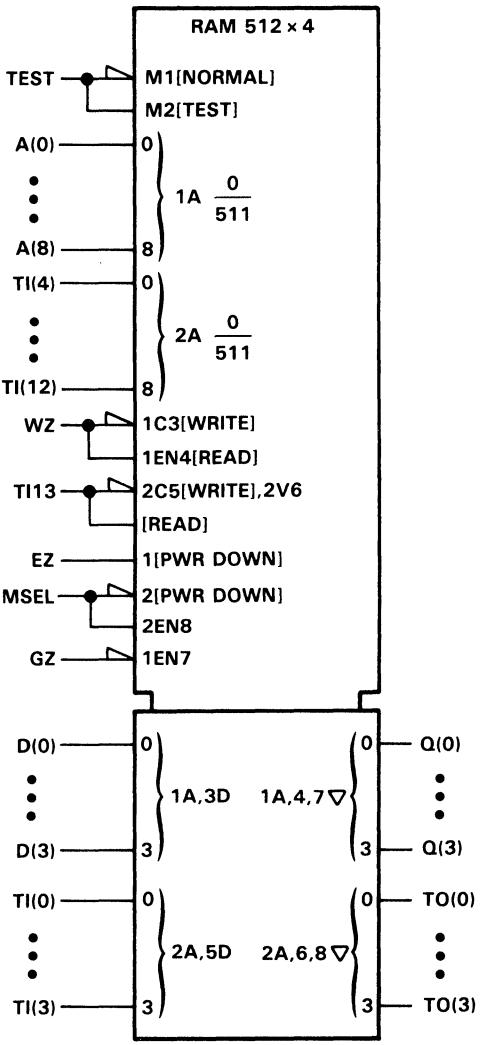
description

The RH006LJ cell is a dedicated 512-word by 4-bit static random-access memory (RAM). A parallel testability scheme is implemented in the RAM with test-mode selection for accessing inputs and outputs through use of the parallel test-port controller cell, TP000LJ, and the global test enable/ controller cell, TP006LJ.

When the RAM is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: RH006LJ D0,D1,D2,D3,TI0,TI1, TI2,TI3,A0,A1,A2,A3,A4,A5,A6,A7, A8,TI4,TI5,TI6,TI7,TI8,TI9,TI10,TI11, TI12,TI13,TEST,EZ,WZ,GZ,MSEL, Q0,Q1,Q2,Q3,TO0,TO1,TO2,TO3;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TYP†	MAX	UNIT
V_T	Input threshold voltage				2.2		V
I_{CC}	Supply current	EZ = H		$V_I = V_{CC}$ or 0		10	µA
		EZ = L	−55°C to 125°C			43.3	mA
			0°C to 70°C			40.3	
C_i	Input capacitance	Any A, GZ, WZ			0.11		pF
		Any D			0.1		
		EZ			0.18		
C_{pd}	Equivalent power dissipation capacitance			$t_r = t_f = 1$ ns	120		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Any A	Any Q	3.2	9.2	23.6	3.3	9.2	21.5	ns
$t_{a(E)}$	EZ	Any Q	3.2	9.2	23.6	3.3	9.2	21.5	ns

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

RH007LJ
512-WORD BY 8-BIT STATIC RANDOM-ACCESS MEMORY WITH 3-STATE OUTPUTS

D3030, APRIL 1988

RANDOM-ACCESS MEMORY CELL

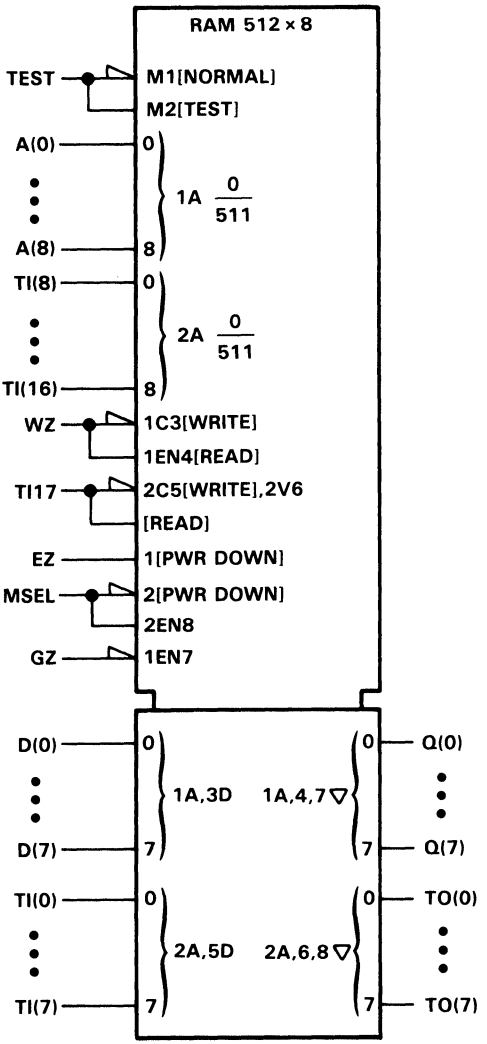
description

The RH007LJ cell is a dedicated 512-word by 8-bit static random-access memory (RAM). A parallel testability scheme is implemented in the RAM with test-mode selection for accessing inputs and outputs through use of the parallel test-port controller cell, TP000LJ, and the global test enable/ controller cell TP006LJ.

When the RAM is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: RH007LJ D0,D1,D2,D3,D3,D4, D5,D6,D7,TI0,TI1,TI2,TI3,TI4,TI5,TI6, TI7,A0,A1,A2,A3,A4,A5,A6,A7,A8, TI8,TI9,TI10,TI11,TI12,TI13,TI14, TI15,TI16,TI17,TEST,EZ,WZ,GZ, MSEL,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7, TO0,TO1,TO2,TO3,TO4,TO5,TO6, TO7;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TYP†	MAX	UNIT
V_T	Input threshold voltage				2.2		V
I_{CC}	Supply current	EZ = H		$V_I = V_{CC}$ or 0		10	µA
		EZ = L	−55°C to 125°C			86.6	mA
			0°C to 70°C			80.6	
C_i	Input capacitance	Any A, GZ, WZ			0.11		pF
		Any D			0.1		
		EZ			0.18		
C_{pd}	Equivalent power dissipation capacitance			$t_r = t_f = 1$ ns	240		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Any A	Any Q	3.3	9.5	24.1	3.5	9.5	22	ns
$t_{a(E)}$	EZ	Any Q	3.3	9.5	24.1	3.5	9.5	22	ns

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

RH008LJ
1024-WORD BY 4-BIT STATIC RANDOM-ACCESS MEMORY WITH 3-STATE OUTPUTS

D3030, APRIL 1988

RANDOM-ACCESS MEMORY CELL

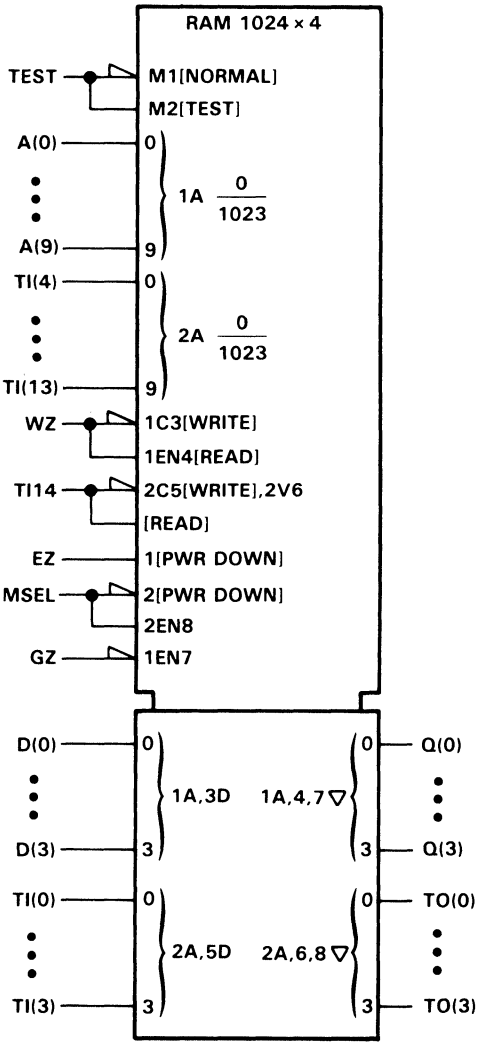
description

The RH008LJ cell is a dedicated 1024-word by 4-bit static random-access memory (RAM). A parallel testability scheme is implemented in the RAM with test-mode selection for accessing inputs and outputs through use of the parallel test-port controller cell, TP000LJ, and the global test enable/controller cell, TP006LJ.

When the RAM is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: RH008LJ D0,D1,D2,D3,TI0,TI1, TI2,TI3,A0,A1,A2,A3,A4,A5,A6,A7, A8,A9,TI4,TI5,TI6,TI7,TI8,TI9,TI10, TI11,TI12,TI13,TI14,TEST,EZ,WZ, GZ,MSEL,Q0,Q1,Q2,Q3,TO0,TO1, TO2,TO3;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TYP†	MAX	UNIT
V_T	Input threshold voltage				2.2		V
I_{CC}	Supply current	EZ = H		$V_I = V_{CC}$ or 0		10	µA
		EZ = L	−55°C to 125°C			43.3	mA
			0°C to 70°C			40.3	
C_i	Input capacitance	Any A, GZ, WZ			0.11		pF
		Any D			0.1		
		EZ			0.18		
C_{pd}	Equivalent power dissipation capacitance			$t_r = t_f = 1$ ns	120		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Any A	Any Q	3.8	10.4	26.6	4	10.4	23.9	ns
$t_{a(E)}$	EZ	Any Q	3.8	10.4	26.6	4	10.4	23.9	ns

† Typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.

RH009LJ
1024-WORD BY 8-BIT STATIC RANDOM-ACCESS MEMORY WITH 3-STATE OUTPUTS

D3030, APRIL 1988

RANDOM-ACCESS MEMORY CELL

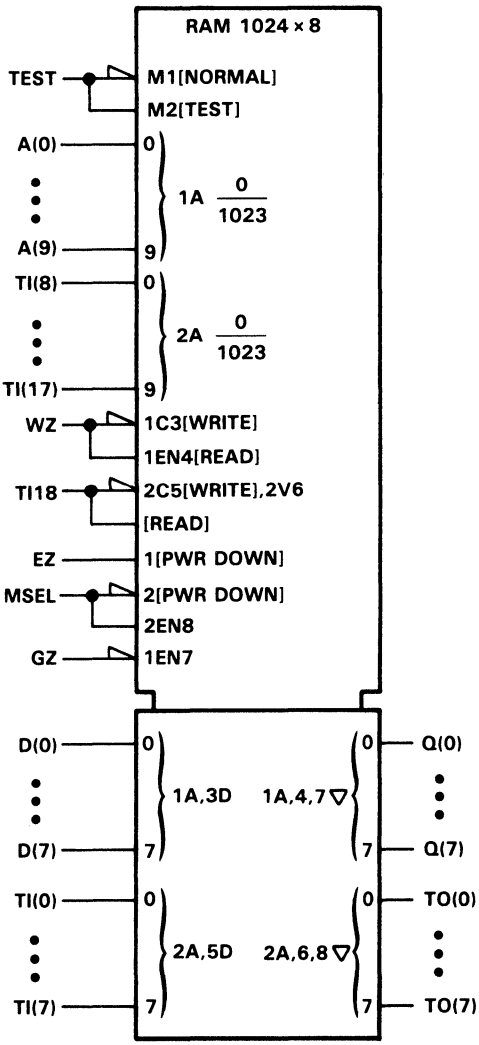
description

The RH009LJ cell is a dedicated 1024-word by 8-bit static random-access memory (RAM). A parallel testability scheme is implemented in the RAM with test-mode selection for accessing inputs and outputs through use of the parallel test-port controller cell, TP000LJ, and the global test enable/controller cell, TP006LJ.

When the RAM is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: RH009LJ D0,D1,D2,D3,D3,D4, D5,D6,D7,TI0,TI1,TI2,TI3,TI4,TI5,TI6, TI7,A0,A1,A2,A3,A4,A5,A6,A7,A8,A9, TI8,TI9,TI10,TI11,TI12,TI13,TI14, TI15,TI16,TI17,TI18,TEST,EZ,WZ, GZ,MSEL,Q0,Q1,Q2,Q3,Q4,Q5,Q6, Q7,TO0,TO1,TO2,TO3,TO4,TO5, TO6,TO7;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TYP†	MAX	UNIT
V_T	Input threshold voltage				2.2		V
I_{CC}	Supply current	EZ = L		$V_I = V_{CC}$ or 0		10	µA
		EZ = L	−55°C to 125°C			86.6	mA
			0°C to 70°C			80.6	
C_i	Input capacitance	Any A, GZ, WZ			0.11		pF
		Any D			0.1		
		EZ			0.18		
C_{pd}	Equivalent power dissipation capacitance			$t_r = t_f = 1$ ns	240		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Any A	Any Q	3.9	10.8	27	4.2	10.8	24.4	ns
$t_{a(E)}$	EZ	Any Q	3.9	10.8	27	4.2	10.8	24.4	ns

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

RH010LJ
2048-WORD BY 4-BIT STATIC RANDOM-ACCESS MEMORY WITH 3-STATE OUTPUTS

D3030, APRIL 1988

RANDOM-ACCESS MEMORY CELL

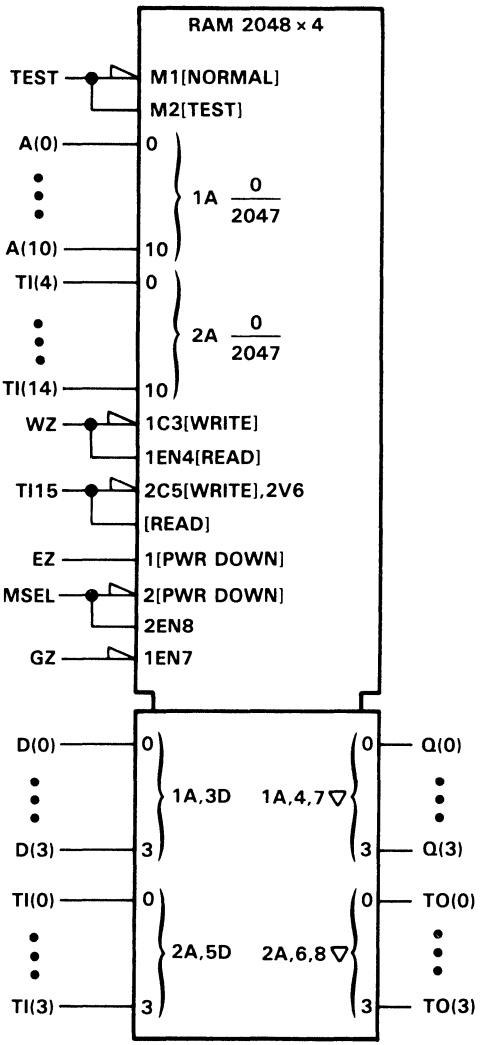
description

The RH010LJ cell is a dedicated 2048-word by 4-bit static random-access memory (RAM). A parallel testability scheme is implemented in the RAM with test-mode selection for accessing inputs and outputs through use of the parallel test-port controller cell, TP000LJ, and the global test enable/controller cell, TP006LJ.

When the RAM is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: RH010LJ D0,D1,D2,D3,TI0,TI1, TI2,TI3,A0,A1,A2,A3,A4,A5,A6,A7, A8,A9,A10,TI4,TI5,TI6,TI7,TI8,TI9, TI10,TI11,TI12,TI13,TI14,TI15,TEST, EZ,WZ,GZ,MSEL,Q0,Q1,Q2,Q3, TO0,TO1,TO2,TO3;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TYP†	MAX	UNIT
V_T	Input threshold voltage				2.2		V
I_{CC}	Supply current	EZ = H		$V_I = V_{CC}$ or 0		10	µA
		EZ = L	−55°C to 125°C			70.9	mA
			0°C to 70°C			66	
C_i	Input capacitance	Any A, GZ, WZ			0.11		pF
		Any D			0.1		
		EZ			0.18		
C_{pd}	Equivalent power dissipation capacitance			$t_r = t_f = 1$ ns	120		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Any A	Any Q	4.5	11.9	29.5	4.9	11.9	26.7	ns
$t_{a(E)}$	EZ	Any Q	4.5	11.9	29.5	4.9	11.9	26.7	ns

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

RH011LJ
2048-WORD BY 8-BIT STATIC RANDOM-ACCESS MEMORY WITH 3-STATE OUTPUTS

D3030, APRIL 1988

RANDOM-ACCESS MEMORY CELL

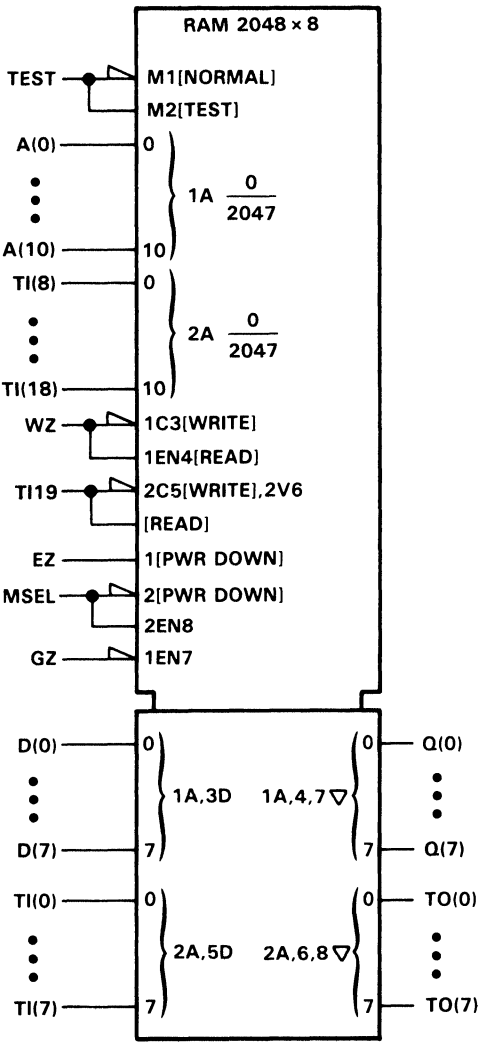
description

The RH011LJ cell is a dedicated 2048-word by 8-bit static random-access memory (RAM). A parallel testability scheme is implemented in the RAM with test-mode selection for accessing inputs and outputs through use of the parallel test-port controller cell, TP000LJ, and the global test enable/controller cell, TP006LJ.

When the RAM is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: RH011LJ D0,D1,D2,D3,D3,D4, D5,D6,D7,TI0,TI1,TI2,TI3,TI4,TI5,TI6, TI7,A0, A1,A2,A3,A4,A5,A6,A7,A8, A9,A10,TI8,TI9,TI10,TI11,TI12,TI13, TI14,TI15,TI16,TI17,TI18,TI19,TEST, EZ,WZ,GZ,MSEL,Q0,Q1,Q2,Q3,Q4, Q5,Q6,Q7,TO0,TO1,TO2,TO3,TO4, TO5,TO6,TO7;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TYP†	MAX	UNIT
V_T	Input threshold voltage				2.2		V
I_{CC}	Supply current	EZ = H		$V_I = V_{CC}$ or 0		10	µA
		EZ = L	−55°C to 125°C			141.9	mA
			0°C to 70°C			132	
C_i	Input capacitance	Any A, GZ, WZ			0.11		pF
		Any D			0.1		
		EZ			0.18		
C_{pd}	Equivalent power dissipation capacitance			$t_r = t_f = 1$ ns	240		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), $C_L = 0$

PARAM-ETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C			0°C to 70°C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Any A	Any Q	4.9	12.6	30.5	5.3	12.6	27.7	ns
$t_{a(E)}$	EZ	Any Q	4.9	12.6	30.5	5.3	12.6	27.7	ns

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

TSC500 SERIES
MegaModule™

GENERAL DATA FIFO MEMORIES WITH 3-STATE OUTPUTS AND ENHANCED STATUS FLAGS

D3030, DECEMBER 1988

- **Choice of 32-, 64-, or 128-Word Depths by 9 Bits Wide**
- **"Latch-and-Go" Input Port**
- **Data Retention at V_{CC} > 2 V**
- **Status Flags for**
  - **Full**
  - **Almost Full (Programmable Assertion Number)**
  - **Half Full**
  - **Empty**
  - **Almost Empty (Programmable Assertion Number)**
- **Full Parallel Module Testability (PMT) Incorporated with Parallel Test Inputs and Outputs**

FIFO SUMMARY

CELL NAME	WORD DEPTH	BIT WIDTH	DATA RATES		PAGE
			READ	WRITE	
FI503LJ	32	9	45 MHz	40 MHz	21-13
FI603LJ	64	9	45 MHz	40 MHz	21-19
FI703LJ	128	9	40 MHz	39 MHz	21-25

description

The 1-µm MegaModule™ standard cells are dedicated hardwired macros implementing first-in first-out (FIFO) memories. Three depths are offered, 32-, 64-, and 128-words, to provide buffered data transfer between high-performance systems and peripherals. Multiple FIFOs can be paralleled to implement wide-word buffer memories. The 9-bit organizations simplify implementation of data paths requiring parity or additional control bits. The FIFO macros contain embedded buffers that reduce input loading, which simplifies implementing larger FIFOs.

A parallel testability scheme is included in the FIFOs with test-mode selection for accessing inputs and outputs through use of the parallel test-port controller cell, TP000LJ, and the global-test enable/controller cell, TP006LJ.

reset input (RSTZ)

When low, the reset input RSTZ resets the write and read address stack pointers to zero count, sets the empty status flag EFZ and the almost-empty status flag AEZ to a low logic level, sets the status flags AFZ, HFZ, and FFZ to a high logic level, and inhibits the internal effects of the read clock (READCLK) until a write operation is performed. Since the outputs are not set to specific logic levels, the data outputs are not valid until a write operation is performed.

data inputs (D0 thru D8)

Data is written into the memory on a low-to-high transition of the write clock input WRCLK after a specified setup time. This latches the input data to permit the write data input to change without loss of data. The status output EFZ goes high after the first word is stored.

data outputs (Q0 thru Q8)

After resetting or an empty condition, the first data word written into the memory appears (noninverted) at the outputs and output EFZ goes high. When the number of words clocked in exceeds the number of words clocked out by 32, 64, or 128 (maximum capacity), the memory is full and FFZ goes low. At this time, write clock WRCLK has no effect on the data residing in memory.

Each successive memory location written with a data word is accessed by a low-to-high transition of the read clock input READCLK. After resetting or when all written locations are accessed using the read clock READCLK, the EFZ output goes low indicating the memory is empty. Once the last word is read from the FIFO additional read clocks have no effect on the data outputs, however a write clock will cause the outputs to reflect the new word entered.

Each 3-state netlist bus employed in a CMOS design utilizing parallel module testing (PMT) should be controlled with a bus-holder latch (LH110LJ) to retain high- or low-logic level data on the bus. The controlled logic levels prevent ambiguous states from occuring internal to the IC.

empty flag output (EFZ)

The empty flag output EFZ is asserted (low) when the FIFO is empty. The FIFO is empty after the reset input RSTZ goes low or after asserting the read clock READCLK when there is only one word stored in the FIFO.

almost-empty assertion inputs (AEn)

The almost-empty assertion number AE, determined by the programmable assertion inputs AEn, is equal to the number of words above empty contained in the FIFO when the almost-empty flag output AEZ is asserted. A function table, provided on each FIFO data sheet, enumerates the AEn input conditions necessary for generating the AE value.

almost-empty flag output (AEZ)

The almost-empty flag output AEZ is asserted (low) when the number of words contained in the FIFO is less than or equal to the almost-empty assertion number AE determined by the AEn inputs. The assertion number is 1 through 4 for FI503LJ and 1 through 8 for FI603LJ and FI703LJ. The code is straight positive-logic binary except that the highest assertion number (4 or 8) is represented by all AEn inputs being low.

almost-full assertion inputs (AFn)

The almost-full assertion number AF, determined by the programmable assertion inputs AFn, is equal to the number of words below the full capacity of the FIFO when the almost-full flag output AFZ is asserted. A function table, provided on each FIFO data sheet, enumerates the AFn input conditions necessary for generating the AF value.

almost-full flag output (AFZ)

The almost-full flag output AFZ is asserted (low) when the number of words contained in the FIFO is greater than or equal to the capacity of the FIFO minus the almost-full assertion number AF, determined by the AFn inputs. The assertion number is 1 through 4 for FI503LJ and 1 through 8 for FI603LJ and FI703LJ. The code is straight positive-logic binary except that the highest assertion number (4 or 8) is represented by all AFn inputs being low.

full-flag output (FFZ)

The full-flag output FFZ is asserted (low) when the FIFO is full. The FIFO is full after writing the 32nd, 64th, or 128th word into the FIFO (depending on the capacity of the FIFO) in excess of the number of words read out. Data at the output (first word) is valid.

half-flag output (HFZ)

The half-flag output HFZ is asserted (low) when the number of words contained in the FIFO is greater than or equal to 1/2 the capacity of the FIFO.

3-state output control (OEZ)

When output control input OEZ is low, stored data appears at the Qn outputs. When OEZ is high, the 3-state outputs are in the high-impedance state.The output control does not affect the internal operation of the FIFOs.

parallel module test

To test the FIFO MegaModule™, the TEST pin is held high and the FIFO is enabled or disabled for test with the module select MSEL pin. Under these conditions the FIFO is controlled and written by the test input TIxx pins and observed at the test output TOxx pins. When more than one MegaModule™ is present in a design, they will share a common test bus but only the MSEL pin of the MegaModule™ currently being tested should be high (enabled).

PARALLEL MODULE TEST MODE SUMMARY TABLE

INPUTS		FIFO MODE
TEST	MSEL	
L	L	NORMAL OPERATION (TEST PINS Txxx DISABLED)
L	H	NOT PERMITTED
H	L	TEST MODE BUT NOT ACTIVE FOR TEST (DISABLED)
H	H	TEST MODE AND ACTIVE FOR TESTING (ENABLED)

CMOS designs employing parallel module test must have each normal output controlled with an LH110LJ bus-holder latch to prevent ambiguous states from occurring internal to the IC.

MegaModule is a trademark of Texas Instruments Incorporated.

Timing requirements associated with the test inputs and outputs are generally the same as the normal FIFO function. The test requirements are not specified because the test mode normally operates at speeds less than 1 MHz. Texas Instruments generates the functional FIFO test patterns.

absolute maximum ratings

These are specified as a part of the applicable cell library. Data and status stored in the FIFO are retained if the supply voltage is not permitted to go below 2 V minimum. Functional characteristics other than data and status retention are not specified when V_{CC} = 2 V to 4.5 V.

MegaModule is a trademark of Texas Instruments Incorporated.

NORMAL-MODE SIGNAL DESCRIPTIONS

NODE		FUNCTION
NAME(S)	TITLE	
TEST	Test Enable	When low, the normal mode is enabled and the signals in this table are used. When high, the test mode is enabled and the other signals described in this table are disabled.
AEZ	Almost-Empty Flag	Low when the FIFO is within AE words of being empty, where AE is the almost-empty assertion number.
AE0, AE1 of FI503LJ or AE0, AE1, AE2 of FI603LJ and FI703LJ	Almost-Empty Assertion Number	Inputs that set the maximum number of words in the FIFO above empty when the almost-empty flag output AEZ is asserted. The assertion number AE is 1 through 4 for FI503LJ and 1 through 8 for FI603LJ and FI703LJ. The code is straight positive-logic binary except that the highest assertion number (4 or 8) is represented by all AEn inputs being low.
AFZ	Almost-Full Flag	Low when the FIFO is within AF words of being full, where AF is the almost-full assertion number.
AF0, AF1 of FI503LJ or AF0, AF1, AF2 of FI603LJ and FI703LJ	Almost-Full Assertion Number	Inputs that set the minimum number of words in the FIFO above empty when the almost-full status flag output AFZ is asserted. The assertion number AF is 1 through 4 for FI503LJ and 1 through 8 for FI603LJ and FI703LJ. The code is straight positive-logic binary except that the highest assertion number (4 or 8) is represented by all AFn inputs being low.
D0-D8	Data Input	Data inputs
EFZ	Empty Flag	Low when FIFO is empty.
FFZ	Full Flag	Low when FIFO is full.
HFZ	Half-Full Flag	Low when the FIFO contains one-half or more words than full capacity.
OEZ	Output Enable	When low, data appears at the FIFO outputs. When high, the Q outputs are in a high-impedance state (data is retained).
Q0-Q8	Data Output	Data outputs
READCLK	Read Clock	Low-to-high transition reads (unloads) data words from FIFO.
RSTZ	Reset	When low, write and read addresses go to zero, EFZ and AEZ go low, AFZ, FFZ, and HFZ go high, and READCLK effects are inhibited. Data out is not valid.
WRCLK	Write Clock	Low-to-high transition latches input data into FIFO.

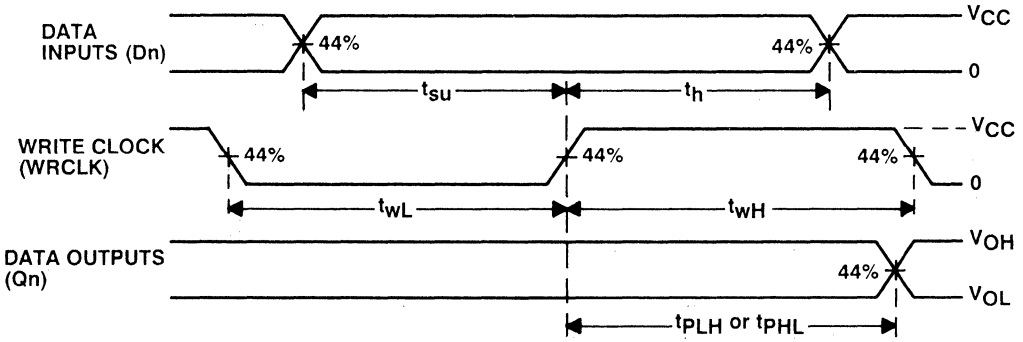
TEST-MODE SIGNAL DESCRIPTIONS

NODE		FUNCTION
NAME(S)	TITLE	
TEST	Test Enable	When high, the test mode is enabled. When low, the other signals described in this table are disabled.
MSEL	Module Select for Test	When high, the FIFO module is enabled for testing. When low, the FIFO module is disabled.
TO10 (AEZ)	Almost-Empty Test Flag	Low when the FIFO is within AE words of being empty, where AE is the almost-empty assertion number.
TI12,TI13 of FI503LJ or TI12, TI13, and TI14 of FI603LJ and FI703LJ (AE0, AE1, or AE2)	Almost-Empty Test Assertion Number	Inputs that set the maximum number of words in the FIFO above empty when the almost-empty flag output TO10(AEZ) is asserted. The assertion number AE is 1 through 4 for FI503LJ and 1 through 8 for the FI603LJ and FI703LJ. The code is straight positive-logic binary except that the highest assertion number (4 or 8) is represented by all AEn inputs being low.
TO11(AFZ)	Almost-Full Test Flag	Low when the FIFO is within AF words of being full, where AF is the almost-full assertion number.
TI14,TI15 of FI503LJ or TI15, TI16, and TI17 of FI603LJ and FI703LJ (AF0, AF1, or AF2)	Almost-Full Test Assertion Number	Inputs that set the minimum number of words in the FIFO above empty when the almost-full status flag output TO11(AFZ) is asserted. The assertion number AF is 1 through 4 for FI503LJ and 1 through 8 for the FI603LJ and FI703LJ. The code is straight positive-logic binary except that the highest assertion number (4 or 8) is represented by all AFn inputs being low.
TI0-TI8(D0-D8)	Test Data In	Data inputs
TO13 (EFZ)	Test Empty Flag	Low when FIFO is empty.
TO12 (FFZ)	Test Full Flag	Low when FIFO is full.
TO9 (HFZ)	Test Half-Full Flag	Low when the FIFO contains one-half or more words than full capacity.
TI16 (FI503LJ) TI18 (FI603LJ and FI703LJ0 (OEZ)	Test Output Enable	When low, data appears at the FIFO outputs. When high, the Q outputs are in a high-impedance state (data is retained).
TO0-TO8(Q0-Q8)	Test Data Out	Data outputs
TI11 (READCLK)	Test Read Clock	Low-to-high transition reads (unloads) data words from FIFO.
TI10 (RSTZ)	Test Reset	When low, write and read addresses go to zero, TO13(EFZ) and TO10(AEZ) go low, TO11(AFZ), TO12(FFZ), and TO9(HFZ) go high, and READCLK effects are inhibited. Data out is not valid.
TI9 (WRCLK)	Test Write Clock	Low-to-high transition latches input data into FIFO.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
$V_{CC(DR)}$	Supply voltage for data retention		2			V
T_A	Operating free-air temperature	Military	−55		125	°C
		Commercial	0		70	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. After writing (loading) begins, FIFO data output is valid.
B. After reading (unloading) empties FIFO, additional read clock cycles are inhibited and a write loads new data.
C. After reset, FIFO data output is not valid.

FIGURE 1. WRITE TIMING DIAGRAM

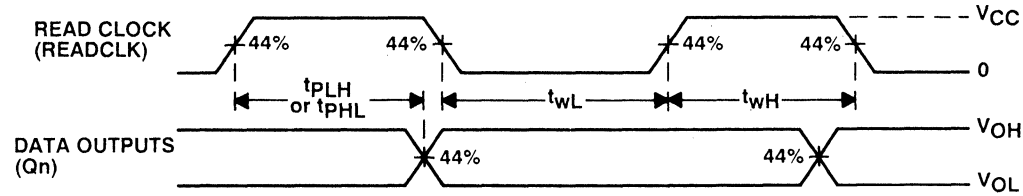


FIGURE 2. READ TIMING DIAGRAM

MegaModule is a trademark of Texas Instruments Incorporated.

PARAMETER MEASUREMENT INFORMATION

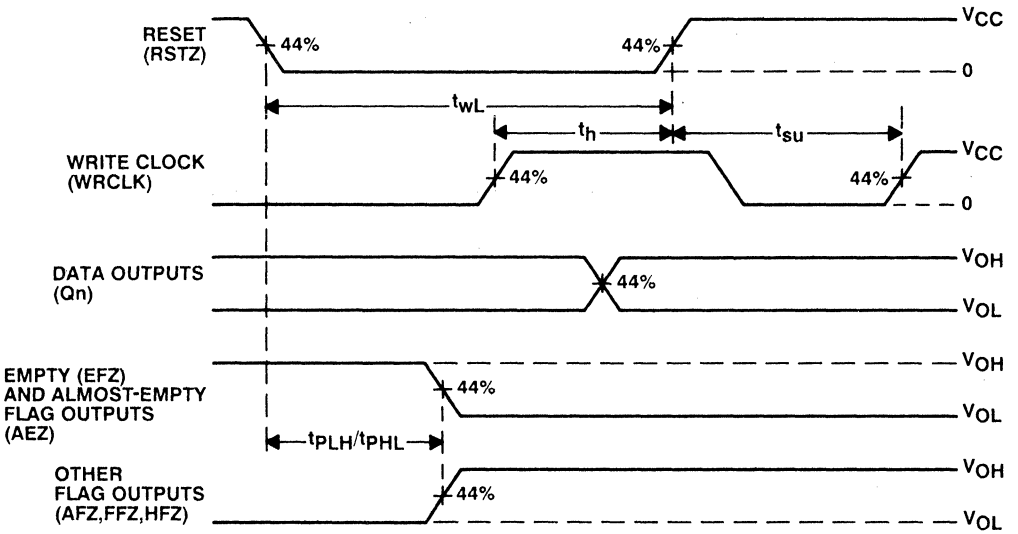


FIGURE 3. RESET TIMING DIAGRAM

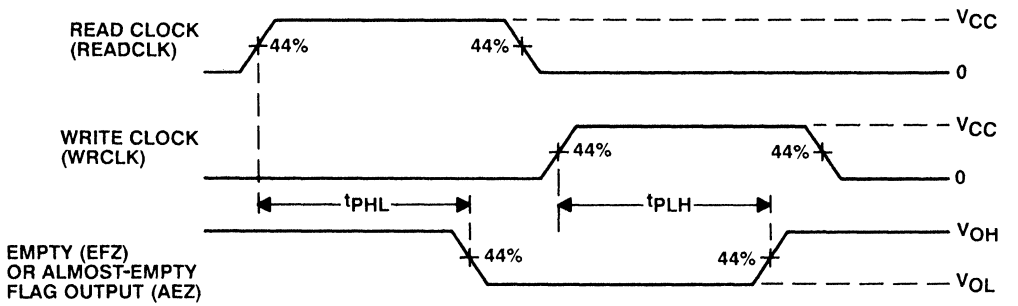


FIGURE 4. EMPTY OR ALMOST-EMPTY FLAG TIMING DIAGRAM

MegaModule is a trademark of Texas Instruments Incorporated.

PARAMETER MEASUREMENT INFORMATION

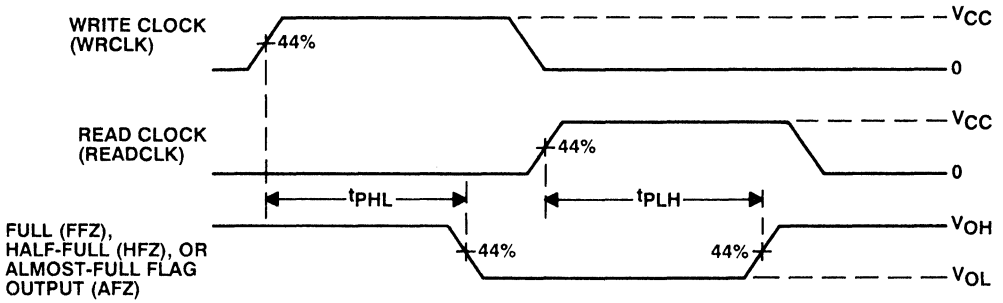


FIGURE 5. FULL, HALF-FULL, ALMOST-FULL FLAG TIMING DIAGRAM

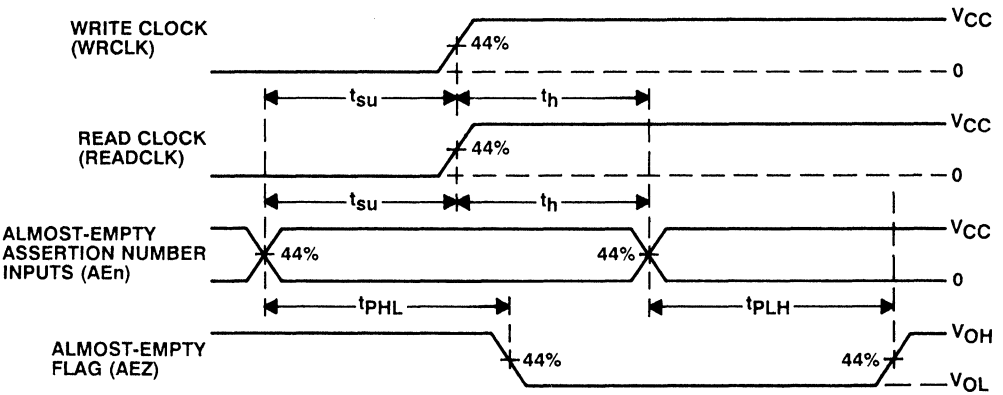


FIGURE 6. ALMOST-EMPTY ASSERTION NUMBER TIMING DIAGRAM

MegaModule is a trademark of Texas Instruments Incorporated.

PARAMETER MEASUREMENT INFORMATION

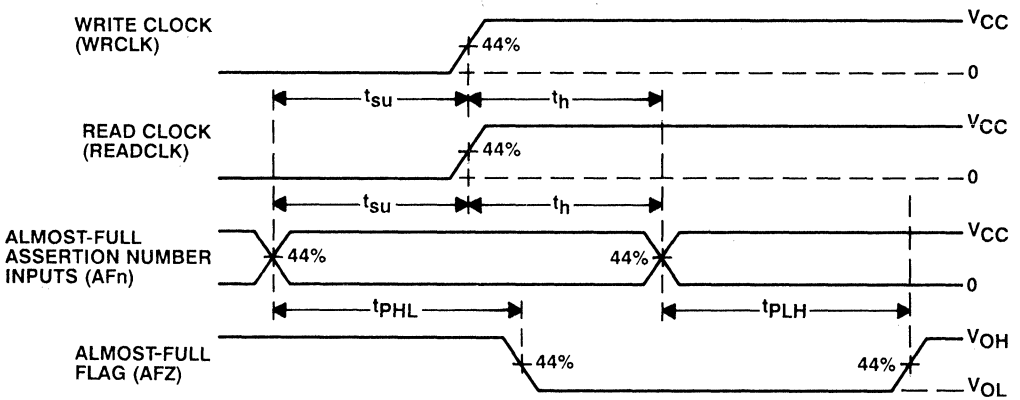


FIGURE 7. ALMOST-FULL ASSERTION NUMBER TIMING DIAGRAM

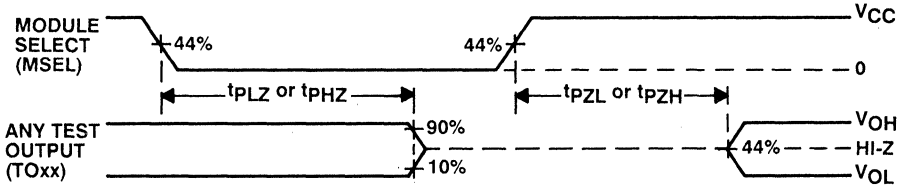


FIGURE 8. MODULE SELECT TIMING DIAGRAM

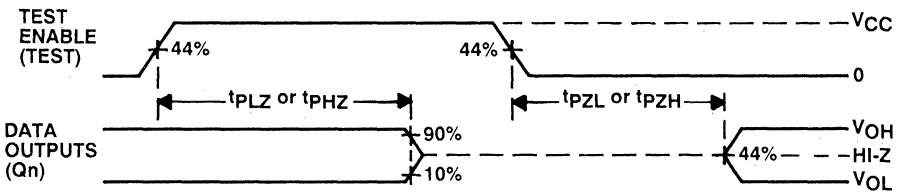


FIGURE 9. TEST TIMING DIAGRAM

MegaModule is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

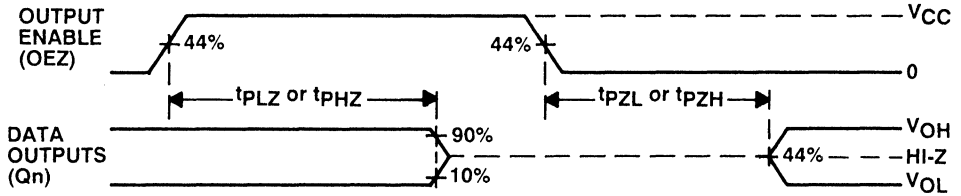


FIGURE 10. OUTPUT ENABLE TIMING DIAGRAM

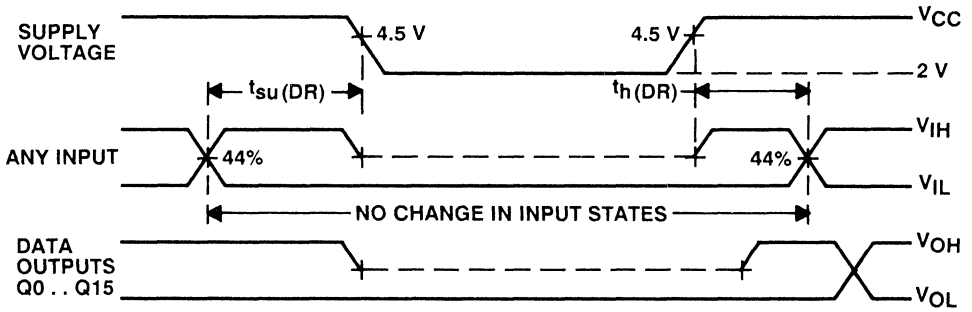


FIGURE 11. DATA RETENTION VOLTAGE WAVEFORMS

MegaModule is a trademark of Texas Instruments Incorporated.

TSC500 SERIES
MegaModule™

FI503LJ
32-WORD BY 9-BIT FIFO MEMORIES WITH 3-STATE OUTPUTS AND EXPANDED STATUS FLAGS

D3030, DECEMBER 1988

- **32-Words Deep by 9 Bits Wide**
- **Expanded Status Flags:**
  - **Full**
  - **Almost Full**
  - **Half Full**
  - **Empty**
  - **Almost Empty**
- **Data Retention at V_{CC} > 2 V**
- **Full Parallel Module Testability (PMT) Incorporated with Parallel Test Inputs and Outputs**

description

This 1-μm MegaModule™ standard cell is a dedicated hardwired macro implementing a 32-word by 9-bit first-in first-out memory (FIFO) with 3-state outputs, expanded status indicators, and parallel module test control circuitry. When the MegaModule™ is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: FI503LJ MSEL,TEST,WRCLK,READCLK,RSTZ,TI9,TI11,TI10,OEZ,TI16,AE0,AE1, AF0,AF1,TI12,TI13,TI14,TI15,D0,D1,D2,D3,D4,D5,D6,D7,D8,TI0,TI1,TI2,TI3,TI4, TI5,TI6,TI7,TI8,AEZ,AFZ,HFZ,FFZ,EFZ,TO10,TO11,TO9,TO12,TO13,Q0,Q1,Q2, Q3,Q4,Q5,Q6,Q7,Q8,TO0,TO1,TO2,TO3,TO4,TO5,TO6,TO7,TO8;

CMOS designs employing parallel module test must have each normal output controlled with an LH110LJ bus-holder latch to prevent ambiguous states from occurring internal to the IC during testing.

almost-empty flag (AEZ)

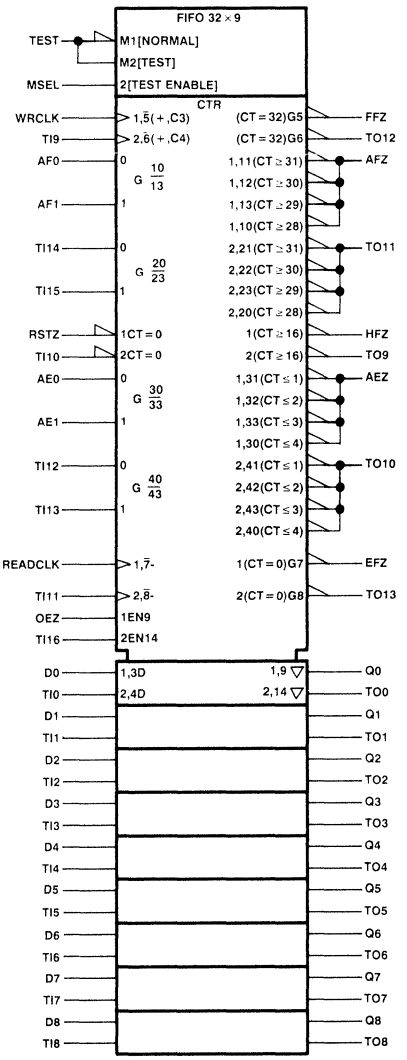
The almost-empty flag (AEZ) is asserted (low) when the number of words in the FIFO is equal to or less than the programmed threshold determined by the AEn bits. The almost-empty flag thresholds and corresponding AEn bit combinations are given in the table at the right.

AEZ PROGRAMMING TABLE

AE1	AE0	AEZ FLAG ASSERTED LOW (WORDS IN FIFO)
L	H	1 OR LESS
H	L	2 OR LESS
H	H	3 OR LESS
L	L	4 OR LESS

MegaModule is a trademark of Texas Instruments Incorporated.

logic symbol†



† The logic symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12. The symbol is functionally correct but does not show the details of implementation. This symbol represents the memories as if they were controlled by a single counter containing the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

MegaModule is a trademark of Texas Instruments Incorporated.

almost-full flag (AFZ)

The almost-full flag (AFZ) is asserted (low) when the number of words in the FIFO buffer is equal to or greater than the programmed threshold determined by the AFn bits. The almost-full flag thresholds and corresponding AFn bit combinations are given in the table at the right.

AFZ PROGRAMMING TABLE

AF1	AF0	AFZ FLAG ASSERTED (WORDS IN FIFO)
L	H	31 OR MORE
H	L	30 OR MORE
H	H	29 OR MORE
L	L	28 OR MORE

Values of the AEn or AFn bits may be applied by tie-off cells, latches, or dynamically during operation.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the applicable cell library. Data and status stored in the FIFO are retained if the supply voltage is not permitted to go below 2 V minimum. Functional characteristics other than data and status retention are not specified when V_{CC} = 2 V to 4.5 V.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			FIGURE†	MIN MAX	UNIT
f_{clock}	Clock frequency	READCLK		45	MHz
		WRCLK		40	
t_w	Pulse duration	READCLK high	2	10	ns
		READCLK low	2	12	
		RSTZ low	3	6	
		WRCLK high	1	12.5	
		WRCLK low	1	12	
t_{su}	Setup time	AEn or AFn before READCLK↑	6,7	1	ns
		AEn or AFn before WRCLK↑	6,6	1	
		Data before WRCLK↑	1	4	
		RSTZ inactive before WRCLK↑	1	3	
$t_{su(DR)}$	Setup time for data retention	All inputs before V_{CC} falls below 4.5 V	11	27.6	ns
t_h	Hold time	AEn or AFn after READCLK↑	6,7	4.1	ns
		AEn or AFn after WRCLK↑	6,7	4.5	
		Data after WRCLK↑	1	0	
		RSTZ active after WRCLK↑	3	11	
$t_{h(DR)}$	Hold time for data retention	All inputs after V_{CC} reaches 4.5 V	11	27.6	ns

† Figures referenced are in the FIFO general data.

MegaModule is a trademark of Texas Instruments Incorporated.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	AE0,AE1,AF0,AF1		0.31		pF
		Dn		0.35		
		MSEL		0.25		
		OEZ		0.24		
		READCLK		0.26		
		RSTZ		0.48		
		TEST		0.31		
		WRCLK		0.28		
C_i	Test input capacitance	TI12 to TI15		0.38		pF
		TI0 to TI8		0.42		
		TI16		0.36		
		TI9		0.36		
		TI10		0.36		
		TI11		0.32		
C_o	Output capacitance	Qn		0.35		pF
		TO0 to TO8		0.39		
		TO9 TO TO13		0.41		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	207		pF

MegaModule is a trademark of Texas Instruments Incorporated.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FIG†	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	AEn	AEZ	6		1.6	5.2	12.2	1.8	5.2	11	ns
t_{PHL}					1.7	4.8	11.1	1.8	4.8	10.1	
t_{PLH}	AFn	AFZ	7		1.6	5.2	12.2	1.8	5.2	11	ns
t_{PHL}					1.7	4.8	11.1	1.8	4.8	10.1	
t_{PLH}	READCLK	AFZ	5		4	11.7	26.3	4.3	11.7	24.2	ns
t_{PLH}		HFZ	5		4	11.7	26.3	4.3	11.7	24.2	
t_{PLH}		FFZ	5		1.5	4.5	10.5	1.6	4.5	9.5	
t_{PLH}		Qn	2		3.7	11	25.8	3.9	11	23.5	
t_{PHL}		Qn	2		3.7	11	25.1	3.9	11	22.9	
t_{PHL}		AEZ	4		4.2	12	27.3	4.5	12	24.9	
t_{PHL}		EFZ	4		2.6	7.9	18.3	2.8	7.9	16.6	
t_{PLH}	RSTZ	AFZ	3		3.5	10.9	25.5	3.7	10.9	23.2	ns
t_{PLH}		FFZ	3		1.3	3.9	8.8	1.4	3.9	8	
t_{PLH}		HFZ	3		3.5	10.9	25.5	3.7	10.9	23.2	
t_{PHL}		AEZ	3		3.4	10.7	25.2	3.7	10.7	22.9	
t_{PHL}		EFZ	3		1.47	4.6	10.7	1.6	4.6	9.7	
t_{PLH}	WRCLK	AEZ	4		3.9	12	27.1	4.2	12	24.9	ns
t_{PLH}		EFZ	4		1.4	4.5	10.6	1.5	4.5	9.6	
t_{PLH}		Qn	1		2.2	7.2	17.1	2.4	7.2	15.6	
t_{PHL}		Qn	1		2.4	7.5	17.5	2.5	7.5	16	
t_{PHL}		AFZ	5		4.1	12.2	27.6	4.4	12.2	25.4	
t_{PHL}		FFZ	5		2.8	8.7	20.5	3	8.7	18.6	
t_{PHL}		HFZ	5		4.1	12.2	27.6	4.4	12.2	25.4	
t_{PZH}	MSEL	Any TOn	8	C_L = 1 pF, R_L = 40 kΩ to GND	0.82	1.9	3.92	0.86	1.9	3.63	ns
t_{PZL}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}	0.72	1.5	3.07	0.74	1.5	2.85	
t_{PHZ}	MSEL	Any TOn	8	C_L = 1 pF, R_L = 40 kΩ to GND		9			9		ns
t_{PLZ}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}		3.54			3.54		

† Figures referenced are in the FIFO general data.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

MegaModule is a trademark of Texas Instruments Incorporated.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FIG†	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PZH}	OEZ	Qn	10	C_L = 1 pF, R_L = 40 kΩ to GND	0.99	3.03	7.26	1.04	3.03	6.54	ns
t_{PZL}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}	0.72	2.2	5.31	0.76	2.2	4.76	
t_{PHZ}	OEZ	Qn	10	C_L = 1 pF, R_L = 40 kΩ to GND		16.57			16.57		ns
t_{PLZ}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}		7.9			7.9		
t_{PZH}	TEST	Any	9	C_L = 1 pF, R_L = 40 kΩ to GND	0.98	1.95	3.85	1.01	1.95	3.57	ns
t_{PZL}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}	0.95	2.03	3.98	1	2.03	3.68	
t_{PHZ}	TEST	Any	9	C_L = 1 pF, R_L = 40 kΩ to GND		7.35			7.35		ns
t_{PLZ}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}		4.16			4.16		
Δt_{PZH}	MSEL	Any TOn	8		0.33	0.87	1.84	0.36	0.87	1.67	ns/pF
Δt_{PZL}					0.32	0.81	1.79	0.33	0.81	1.61	
Δt_{PZH}	OEZ	Qn	10		0.24	0.69	1.56	0.26	0.69	1.42	ns/pF
Δt_{PZL}					0.18	0.47	1.05	0.19	0.47	0.95	
Δt_{PZH}	TEST	Qn	9		0.37	1.1	2.34	0.41	1.1	2.14	ns/pF
Δt_{PZL}					0.29	0.67	1.5	0.3	0.67	1.35	
Δt_{PLH}	Any other	Any other	1-7		0.2	0.7	1.62	0.22	0.7	1.46	ns/pF
Δt_{PHL}					0.16	0.5	1.08	0.17	0.5	0.96	

† Figures referenced are in the FIFO general data.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

MegaModule is a trademark of Texas Instruments Incorporated.

TSC500 SERIES MegaModule™

FI603LJ 64-WORD BY 9-BIT FIFO MEMORIES WITH 3-STATE OUTPUTS AND EXPANDED STATUS FLAGS

D3030, DECEMBER 1988

- **64-Words Deep by 9 Bits Wide**
- **Expanded Status Flags:**
  - **Full**
  - **Almost Full**
  - **Half Full**
  - **Empty**
  - **Almost Empty**
- **Data Retention at V_{CC} > 2 V**
- **Full Parallel Module Testability (PMT) Incorporated with Parallel Test Inputs and Outputs**

description

This 1-µm MegaModule™ standard cell is a dedicated hardwired macro implementing a 64-word by 9-bit first-in first-out memory (FIFO) with 3-state outputs, expanded status indicators, and parallel module test control circuitry. When the MegaModule™ is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: FI603LJ MSEL,TEST,WRCLK,READCLK,RSTZ,TI9,TI11,TI10,OEZ,TI18,AE0,AE1, AE2,AF0,AF1,AF2,TI12,TI13,TI14,TI15,TI16,TI17,D0,D1,D2,D3,D4,D5,D6,D7,D8, TI0,TI1,TI2,TI3,TI4,TI5,TI6,TI7,TI8,AEZ,AFZ,HFZ,FFZ,EFZ,TO10,TO11,TO9,TO12, TO13,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8,TO0,TO1,TO2,TO3,TO4,TO5,TO6,TO7, TO8;

CMOS designs employing parallel module test must have each normal output controlled with an LH110LJ bus-holder latch to prevent ambiguous states from occurring internal to the IC during testing.

almost-empty flag (AEZ)

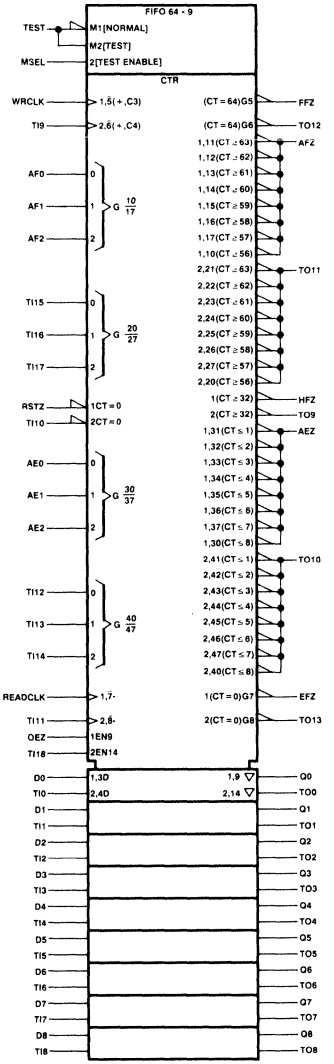
The almost-empty flag (AEZ) is asserted (low) when the number of words in the FIFO is equal to or less than the programmed threshold determined by the AEn bits. The almost-empty flag thresholds and corresponding AEn bit combinations are given in the table at the right.

AEZ PROGRAMMING TABLE

AE2	AE1	AE0	AEZ FLAG ASSERTED LOW (WORDS IN FIFO)
L	L	H	1 OR LESS
L	H	L	2 OR LESS
L	H	H	3 OR LESS
H	L	L	4 OR LESS
H	L	H	5 OR LESS
H	H	L	6 OR LESS
H	H	H	7 OR LESS
L	L	L	8 OR LESS

MegaModule is a trademark of Texas Instruments Incorporated.

logic symbol†



† The logic symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12. The symbol is functionally correct but does not show the details of implementation. This symbol represents the memories as if they were controlled by a single counter containing the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

MegaModule is a trademark of Texas Instruments Incorporated.

FI603LJ
64-WORD BY 9-BIT FIFO MEMORIES WITH 3-STATE OUTPUTS AND EXPANDED STATUS FLAGS

D3030, DECEMBER 1988

almost-full flag (AFZ)

The almost-full flag (AFZ) is asserted (low) when the number of words in the FIFO buffer is equal to or greater than the programmed threshold determined by the AFn bits. The almost-full flag thresholds and corresponding AFn bit combinations are given in the table at the right.

Values of the AEn or AFn bits may be applied by tie-off cells, latches, or dynamically during operation.

AFZ PROGRAMMING TABLE

AF2	AF1	AF0	AFZ FLAG ASSERTED LOW (WORDS IN FIFO)
L	L	H	63 OR MORE
L	H	L	62 OR MORE
L	H	H	61 OR MORE
H	L	L	60 OR MORE
H	L	H	59 OR MORE
H	H	L	58 OR MORE
H	H	H	57 OR MORE
L	L	L	56 OR MORE

absolute maximum ratings and recommended operating conditions

These are specified as a part of the applicable cell library. Data and status stored in the FIFO are retained if the supply voltage is not permitted to go below 2 V minimum. Functional characteristics other than data and status retention are not specified when V_{CC} = 2 V to 4.5 V.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			FIGURE†	MIN	MAX	UNIT
f_{clock}	Clock frequency	READCLK			45	MHz
		WRCLK			40	
t_w	Pulse duration	READCLK high	2	12		ns
		READCLK low	2	10		
		RSTZ low	3	6		
		WRCLK high	1	12.5		
		WRCLK low	1	12.5		
t_{su}	Setup time	AEn or AFn before READCLK↑	6,7	7		ns
		AEn or AFn before WRCLK↑	6,6	6		
		Data before WRCLK↑	1	4		
		RSTZ inactive before WRCLK↑	1	3		
$t_{su(DR)}$	Setup time for data retention	All inputs before V_{CC} falls below 4.5 V	11	39.17		ns
t_h	Hold time	AEn or AFn after READCLK↑	6,7	0		ns
		AEn or AFn after WRCLK↑	6,7	0		
		Data after WRCLK↑	1	0		
		RSTZ active after WRCLK↑	3	13		
$t_{h(DR)}$	Hold time for data retention	All inputs after V_{CC} reaches 4.5 V	11	39.17		ns

† Figures referenced are in the FIFO general data.

MegaModule is a trademark of Texas Instruments Incorporated.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	AEn,AFn		0.35		pF
		Dn		0.42		
		MSEL		0.21		
		OEZ		0.36		
		READCLK		0.32		
		RSTZ		0.38		
		TEST		0.43		
		WRCLK		0.18		
C_i	Test input capacitance	TI12 to TI17		0.41		pF
		TI0 to TI8		0.34		
		TI18		0.36		
		TI9		0.41		
		TI10		0.27		
		TI11		0.37		
C_o	Output capacitance	Qn		0.37		pF
		TO0 to TO8		0.39		
		TO9 TO TO13		0.22		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	194		pF

MegaModule is a trademark of Texas Instruments Incorporated.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FIG†	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	AEn	AEZ	6		3.11	9.48	22.3	3.32	9.48	20.18	ns
t_{PHL}					3.01	8.55	19.49	3.21	8.55	17.77	
t_{PLH}	AFn	AFZ	7		3.11	9.48	22.3	3.32	9.48	20.18	ns
t_{PHL}					3.01	8.55	19.49	3.21	8.55	17.77	
t_{PLH}	READCLK	AFZ	5		4.8	13.89	31.56	5.14	13.89	28.75	ns
t_{PLH}		HFZ	5		4.8	13.89	31.56	5.14	13.89	28.75	
t_{PLH}		FFZ	5		2.05	5.74	12.93	2.19	5.74	11.75	
t_{PLH}		Qn	2		4.29	12.64	28.98	4.6	12.64	26.4	
t_{PHL}		Qn	2		4.38	12.62	28.79	4.69	12.62	26.18	
t_{PHL}		AEZ	4		4.76	13.85	31.48	5.11	13.58	28.68	
t_{PHL}		EFZ	4		3.09	9.05	21.03	3.32	9.05	19.03	
t_{PLH}	RSTZ	AFZ	3		5.58	16.39	38.2	5.94	16.39	34.6	ns
t_{PLH}		FFZ	3		1.69	4.58	10.12	1.81	4.85	9.28	
t_{PLH}		HFZ	3		5.58	16.39	38.2	5.94	16.39	34.6	
t_{PHL}		AEZ	3		5.74	16.79	39.17	6.12	16.79	35.47	
t_{PHL}		EFZ	3		1.66	4.74	10.84	1.76	4.74	9.85	
t_{PLH}	WRCLK	AEZ	4		5.6	17.14	40.15	6	17.14	36.42	ns
t_{PLH}		EFZ	4		1.74	5.17	11.88	1.87	5.17	10.8	
t_{PLH}		Qn	1		3.41	10.32	23.88	3.65	10.32	21.76	
t_{PHL}		Qn	1		3.16	9.75	22.71	3.4	9.75	20.63	
t_{PHL}		AFZ	5		5.72	17.57	41.15	6.13	17.57	37.31	
t_{PHL}		FFZ	5		3.61	10.79	25.25	3.86	10.79	22.82	
t_{PHL}		HFZ	5		5.72	17.57	41.15	6.13	17.57	37.31	
t_{PZH}	MSEL	Any TOn	8	C_L = 1 pF, R_L = 40 kΩ to GND	0.98	2.19	4.44	1.02	2.19	4.13	ns
t_{PZL}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}	0.86	1.89	3.73	0.9	1.89	3.47	
t_{PHZ}	MSEL	Any TOn	8	C_L = 1 pF, R_L = 40 kΩ to GND		7.94			7.94		ns
t_{PLZ}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}		3.86			3.86		

† Figures referenced are in the FIFO general data.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

MegaModule is a trademark of Texas Instruments Incorporated.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FIG†	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PZH}	OEZ	Qn	10	C_L = 1 pF, R_L = 40 kΩ to GND	0.99	3.03	7.26	1.04	3.03	6.54	ns
t_{PZL}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}	0.72	2.2	5.31	0.76	2.2	4.76	
t_{PHZ}	OEZ	Qn	10	C_L = 1 pF, R_L = 40 kΩ to GND		16.57			16.57		ns
t_{PLZ}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}		7.9			7.9		
t_{PZH}	TEST	Any	9	C_L = 1 pF, R_L = 40 kΩ to GND	0.98	1.95	3.85	1.01	1.95	3.57	ns
t_{PZL}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}	0.95	2.03	3.98	1	2.03	3.68	
t_{PHZ}	TEST	Any	9	C_L = 1 pF, R_L = 40 kΩ to GND		7.35			7.35		ns
t_{PLZ}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}		4.16			4.16		
Δt_{PZH}	MSEL	Any TOn	8		0.33	0.87	1.84	0.36	0.87	1.67	ns/pF
Δt_{PZL}					0.32	0.81	1.79	0.33	0.81	1.61	
Δt_{PZH}	OEZ	Qn	10		0.24	0.69	1.56	0.26	0.69	1.42	ns/pF
Δt_{PZL}					0.18	0.47	1.05	0.19	0.47	0.95	
Δt_{PZH}	TEST	Qn	9		0.37	1.1	2.34	0.41	1.1	2.14	ns/pF
Δt_{PZL}					0.29	0.67	1.5	0.3	0.67	1.35	
Δt_{PLH}	Any other	Any other	1-7		0.2	0.7	1.62	0.22	0.7	1.46	ns/pF
Δt_{PHL}					0.16	0.5	1.08	0.17	0.5	0.96	

† Figures referenced are in the FIFO general data.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

MegaModule is a trademark of Texas Instruments Incorporated.

TSC500 SERIES
MegaModule™

FI703LJ
128-WORD BY 9-BIT FIFO MEMORIES WITH 3-STATE OUTPUTS AND EXPANDED STATUS FLAGS

D3030, DECEMBER 1988

- **128-Words Deep by 9 Bits Wide**
- **Expanded Status Flags:**
  - **Full**
  - **Almost Full**
  - **Half Full**
  - **Empty**
  - **Almost Empty**
- **Data Retention at V_{CC} > 2 V**
- **Full Parallel Module Testability (PMT) Incorporated with Parallel Test Inputs and Outputs**

description

This 1-µm MegaModule™ standard cell is a dedicated hardwired macro implementing a 128-word by 9-bit first-in first-out memory (FIFO) with 3-state outputs, expanded status indicators, and parallel module test control circuitry. When the MegaModule™ is called from the engineering workstation input, the following label format is developed and will be captured in the design netlist:

Label: FI703LJ MSEL,TEST,WRCLK,READCLK,RSTZ,TI9,TI11,TI10,OEZ,TI18,AE0,AE1, AE2,AF0,AF1,AF2,TI12,TI13,TI14,TI15,TI16,TI17,D0,D1,D2,D3,D4,D5,D6,D7,D8, TI0,TI1,TI2,TI3,TI4,TI5,TI6,TI7,TI8,AEZ,AFZ,HFZ,FFZ,EFZ,TO10,TO11,TO9,TO12, TO13,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8,TO0,TO1,TO2,TO3,TO4,TO5,TO6,TO7, TO8;

CMOS designs employing parallel module test must have each normal output controlled with an LH110LJ bus-holder latch to prevent ambiguous states from occurring internal to the IC during testing.

almost-empty flag (AEZ)

The almost-empty flag (AEZ) is asserted (low) when the number of words in the FIFO is equal to or less than the programmed threshold determined by the AEn bits. The almost-empty flag thresholds and corresponding AEn bit combinations are given in the table at the right.

AEZ PROGRAMMING TABLE

AE2	AE1	AE0	AEZ FLAG ASSERTED LOW (WORDS IN FIFO)
L	L	H	1 OR LESS
L	H	L	2 OR LESS
L	H	H	3 OR LESS
H	L	L	4 OR LESS
H	L	H	5 OR LESS
H	H	L	6 OR LESS
H	H	H	7 OR LESS
L	L	L	8 OR LESS

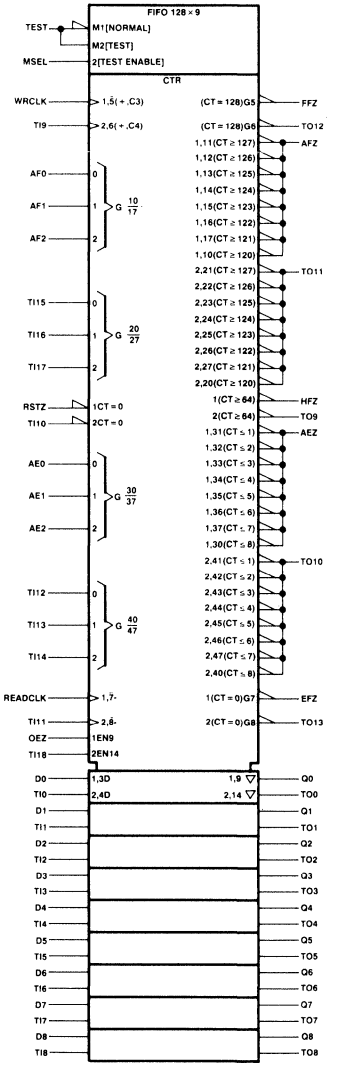
MegaModule is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

FI703LJ
128-WORD BY 9-BIT FIFO MEMORIES WITH 3-STATE OUTPUTS AND EXPANDED STATUS FLAGS

D3030, DECEMBER 1988

logic symbol†



† The logic symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12. The symbol is functionally correct but does not show the details of implementation. This symbol represents the memories as if they were controlled by a single counter containing the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

MegaModule is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

almost-full flag (AFZ)

The almost-full flag (AFZ) is asserted (low) when the number of words in the FIFO buffer is equal to or greater than the programmed threshold determined by the AFn bits. The almost-full flag thresholds and corresponding AFn bit combinations are given in the table at the right.

Values of the AEn or AFn bits may be applied by tie-off cells, latches, or dynamically during operation.

AFZ PROGRAMMING TABLE

AF2	AF1	AF0	AFZ FLAG ASSERTED LOW (WORDS IN FIFO)
L	L	H	127 OR MORE
L	H	L	126 OR MORE
L	H	H	125 OR MORE
H	L	L	124 OR MORE
H	L	H	123 OR MORE
H	H	L	122 OR MORE
H	H	H	121 OR MORE
L	L	L	120 OR MORE

absolute maximum ratings and recommended operating conditions

These are specified as a part of the applicable cell library. Data and status stored in the FIFO are retained if the supply voltage is not permitted to go below 2 V minimum. Functional characteristics other than data and status retention are not specified when V_{CC} = 2 V to 4.5 V.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			FIGURE†	MIN	MAX	UNIT
f_{clock}	Clock frequency	READCLK			40	MHz
		WRCLK			39	
t_w	Pulse duration	READCLK high	2	12.5		ns
		READCLK low	2	12		
		RSTZ low	3	7		
		WRCLK high	1	13		
		WRCLK low	1	12.5		
t_{su}	Setup time	AEn or AFn before READCLK↑	6,7	6.5		ns
		AEn or AFn before WRCLK↑	6,6	5.5		
		Data before WRCLK↑	1	7		
		RSTZ inactive before WRCLK↑	1	6		
$t_{su(DR)}$	Setup time for data retention	All inputs before V_{CC} falls below 4.5 V	11	34.32		ns
t_h	Hold time	AEn or AFn after READCLK↑	6,7	0		ns
		AEn or AFn after WRCLK↑	6,7	0		
		Data after WRCLK↑	1	0		
		RSTZ active after WRCLK↑	3	12		
$t_{h(DR)}$	Hold time for data retention	All inputs after V_{CC} reaches 4.5 V	11	34.32		ns

† Figures referenced are in the FIFO general data.

MegaModule is a trademark of Texas Instruments Incorporated.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	AEn,AFn		0.62		pF
		Dn		0.67		
		MSEL		0.51		
		OEZ		0.89		
		READCLK		0.66		
		RSTZ		0.7		
		TEST		0.54		
		WRCLK		0.71		
C_i	Test input capacitance	TI12 to TI17		0.83		pF
		TI0 to TI8		0.97		
		TI18		0.88		
		TI9		0.71		
		TI10		0.65		
		TI11		0.65		
C_o	Output capacitance	Qn		1.18		pF
		TO0 to TO8		1.16		
		TO9 TO TO13		1.03		
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	268		pF

MegaModule is a trademark of Texas Instruments Incorporated.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FIG†	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	AEn	AEZ	6		3.07	8.99	20.92	3.27	8.99	18.92	ns
t_{PHL}					3.03	8.63	19.67	3.21	8.63	17.91	
t_{PLH}	AFn	AFZ	7		3.07	8.99	20.92	3.27	8.99	18.92	ns
t_{PHL}					3.03	8.63	19.67	3.21	8.63	17.91	
t_{PLH}	READCLK	AFZ	5		4.67	12.95	29.11	4.97	12.95	26.57	ns
t_{PLH}		HFZ	5		4.67	12.95	29.11	4.97	12.95	26.57	
t_{PLH}		FFZ	5		2.21	6.15	13.7	2.37	6.15	12.49	
t_{PLH}		Qn	2		5.37	14.94	33.67	5.71	14.94	30.65	
t_{PHL}		Qn	2		5.36	15.08	34.15	5.69	15.08	31.13	
t_{PHL}		AEZ	4		4.63	12.9	29.02	4.93	12.9	26.51	
t_{PHL}		EFZ	4		3.45	9.72	22.66	3.67	9.72	20.4	
t_{PLH}	RSTZ	AFZ	3		6.13	15.21	33.51	6.41	15.21	30.55	ns
t_{PLH}		FFZ	3		1.81	4.93	10.97	1.93	4.93	10.03	
t_{PLH}		HFZ	3		6.13	15.21	33.51	6.41	15.21	30.55	
t_{PHL}		AEZ	3		6.3	15.64	34.54	6.6	15.64	31.49	
t_{PHL}		EFZ	3		2.08	5.8	13.31	2.21	5.8	12.09	
t_{PLH}	WRCLK	AEZ	4		4.93	14.32	33.29	5.2	14.32	30.22	ns
t_{PLH}		EFZ	4		2.29	6.08	13.28	2.42	6.08	12.38	
t_{PLH}		Qn	1		3.83	10.86	24.69	4.06	10.86	22.53	
t_{PHL}		Qn	1		4.13	11.63	26.4	4.38	11.63	24.07	
t_{PHL}		AFZ	5		5.01	14.75	34.32	5.33	14.75	31.15	
t_{PHL}		FFZ	5		3.7	10.33	23.99	3.91	10.33	21.67	
t_{PHL}		HFZ	5		5.01	14.75	34.32	5.33	14.75	31.15	
t_{PZH}	MSEL	Any TOn	8	C_L = 1 pF, R_L = 40 kΩ to GND	2.18	4.14	7.77	2.25	4.14	7.21	ns
t_{PZL}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}	2.19	4.12	7.7	2.26	4.12	7.14	
t_{PHZ}	MSEL	Any TOn	8	C_L = 1 pF, R_L = 40 kΩ to GND		14.95			14.95		ns
t_{PLZ}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}		9.79			9.79		

† Figures referenced are in the FIFO general data.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

MegaModule is a trademark of Texas Instruments Incorporated.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0 (Continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FIG†	TEST CONDITIONS	−55°C to 125°C MIN	−55°C to 125°C TYP‡	−55°C to 125°C MAX	0°C to 70°C MIN	0°C to 70°C TYP‡	0°C to 70°C MAX	UNIT
t_{PZH}	OEZ	Qn	10	C_L = 1 pF, R_L = 40 kΩ to GND	1.01	2.59	5.73	1.04	2.59	5.25	ns
t_{PZL}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}	1.01	2.55	5.64	1.06	2.55	5.16	
t_{PHZ}	OEZ	Qn	10	C_L = 1 pF, R_L = 40 kΩ to GND		13.03			13.03		ns
t_{PLZ}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}		7.75			7.75		
t_{PZH}	TEST	Any	9	C_L = 1 pF, R_L = 40 kΩ to GND	3.76	6.09	10.57	3.84	6.09	9.87	ns
t_{PZL}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}	3.76	6.05	10.53	3.84	6.05	9.75	
t_{PHZ}	TEST	Any	9	C_L = 1 pF, R_L = 40 kΩ to GND		16.42			16.42		ns
t_{PLZ}				C_L = 1 pF, R_L = 20 kΩ to V_{CC}		11.21			11.21		
Δt_{PZH}	MSEL	Any TOn	8		0.15	0.39	0.85	0.16	0.39	0.78	ns/pF
Δt_{PZL}					0.15	0.35	0.73	0.16	0.35	0.66	
Δt_{PZH}	OEZ	Qn	10		0.14	0.37	0.82	0.15	0.37	0.75	ns/pF
Δt_{PZL}					0.14	0.34	0.72	0.15	0.34	0.65	
Δt_{PZH}	TEST	Qn	9		0.05	0.15	0.34	0.05	0.15	0.32	ns/pF
Δt_{PZL}					0.14	0.32	0.68	0.15	0.32	0.62	
Δt_{PLH}	Any other	Any other	1-7		0.07	0.36	0.84	0.08	0.36	0.76	ns/pF
Δt_{PHL}					0.11	0.38	0.92	0.12	0.38	0.84	

† Figures referenced are in the FIFO general data.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

MegaModule is a trademark of Texas Instruments Incorporated.

D3030, DECEMBER 1988

- **Full Parallel Access with One Independent Write Port and Two Independent Read Ports**
- **Use Register Files in Parallel for Multiple Word Lengths**
- **Data Retention at V_{CC} > 2 V**

3-PORT REGISTER FILE SUMMARY

CELL NAME	WORD DEPTH	BIT WIDTH	AVERAGE READ ACCESS TIME (ns)	PAGE
RF400LJ	16	8	5.2	22-7
RF402LJ	16	9	5.2	22-15
RF403LJ	16	12	6.6	22-19
RF600LJ	64	8	5.5	22-23
RF602LJ	64	9	5.6	22-31

description

Each 3-port register file is provided with an independently addressed data input port and two independently addressed read ports. Because the read mode is asynchronous, data entry and data retrieval can occur simultaneously.

The write enable input, WEZ, provides a simple implementation of the write cycle. When high, the write enable input inhibits new data entry; when low, the write function is enabled and a positive transition at the clock input will store data present at the data inputs in the addressed register word.

Two output enables provide 3-state control for the data outputs:

- G1Z controls output data lines Q10 – Q1n, which are addressed by address lines RA10 – RA1n.
- G2Z controls output data lines Q20 – Q2n, which are addressed by address lines RA20 – RA2n.

When high, an output enable places its associated output lines in a high-impedence state; when low, the register word that is addressed is available at the data output port associated with the read address port.

MegaModule is a trademark of Texas Instruments Incorporated.

PARAMETER MEASUREMENT INFORMATION

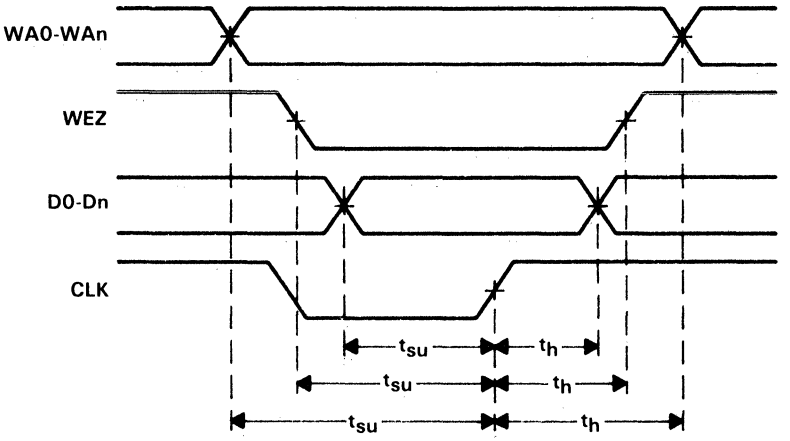
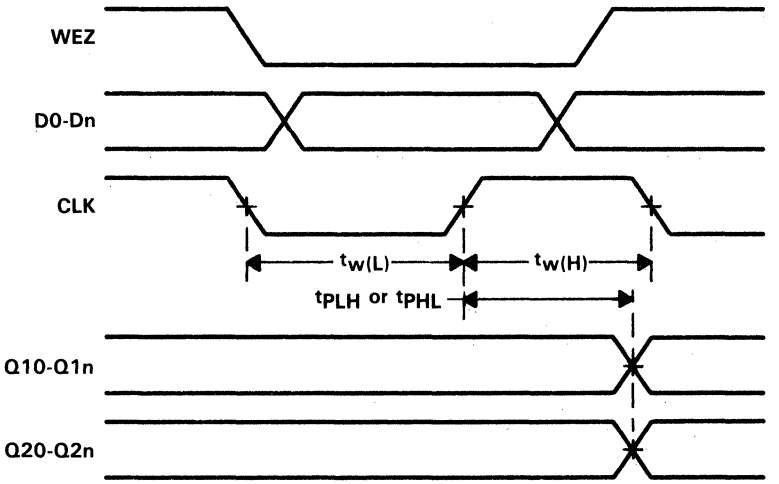


FIGURE 1. SETUP AND HOLD TIMES



NOTE A: Addresses for write and both reads are the same.

FIGURE 2. CLOCK PULSE DURATION, PROPAGATION DELAY TIMES FROM CLOCK

MegaModule is a trademark of Texas Instruments Incorporated.

PARAMETER MEASUREMENT INFORMATION (Continued)

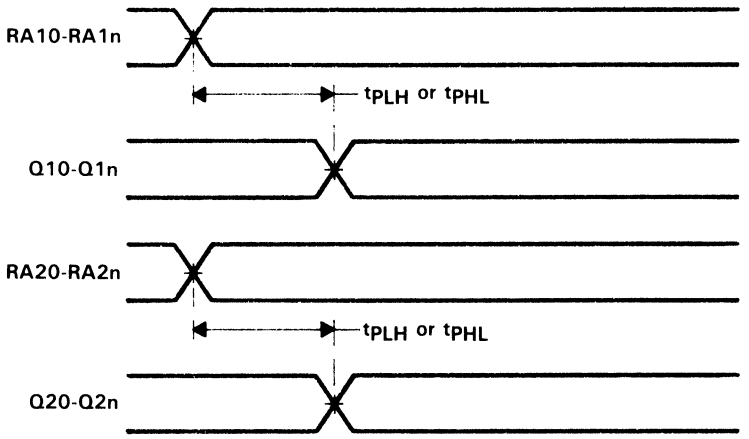


FIGURE 3. PROPAGATION DELAY TIMES FROM READ ADDRESS LOAD

MegaModule is a trademark of Texas Instruments Incorporated.

D3030, DECEMBER 1988

- **Full Parallel Access with Two Independent Write Ports and Two Independent Read Ports**
- **Use Register Files in Parallel for 16-, 32-, or 64-Bit Word Lengths**
- **Data Retention at V_{CC} > 2 V**

4-PORT REGISTER FILE SUMMARY

CELL NAME	WORD DEPTH	BIT WIDTH	AVERAGE READ ACCESS TIME (ns)	PAGE
RF401LJ	16	8	5.3	22-11
RF601LJ	64	8	5.5	22-27

description

Each 4-port register-file is provided with two independently addressed data input ports and two independently addressed read ports. Because the read mode is asynchronous, data entry and data retrieval can occur simultaneously.

Two write enables provide control for permitting data to be written into the addressed location:

- WE1Z controls data lines D10 – D17, which are addressed by address lines WA10 – WA1n.
- WE2Z control data lines D20 – D27, which are addressed by address lines WA20 – WA2n.

When high, the write enable input inhibits new data entry; when low, the write function is enabled. A positive transition at the clock input, combined with a low write enable, stores data applied at the associated data input port; data is stored in the register word that is addressed by the associated write-address inputs. If both write ports are attempting a write to the same register word, data applied at data lines D10 – D17 has priority.

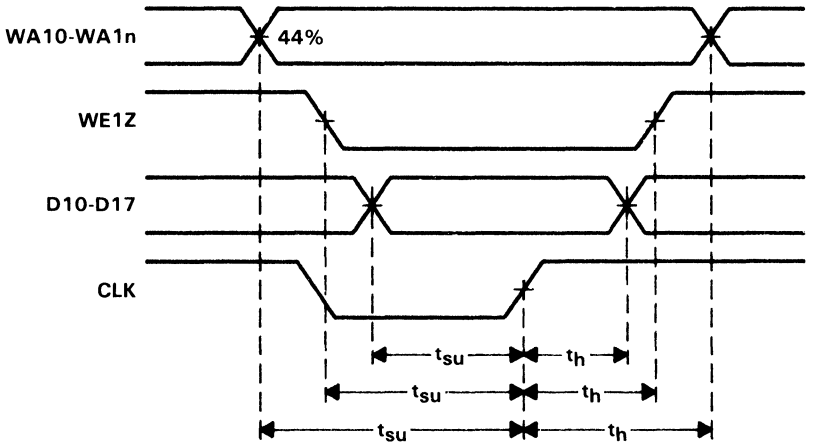
Two output enables provide 3-state control for the data outputs:

- G1Z controls output data lines Q10 – Q17, which are addressed by address lines RA10 – RA1n.
- G2Z controls output data lines Q20 – Q27, which are addressed by address lines RA20 – RA2n.

When high, an output enable places its associated output lines in a high-impedence state; when low, the register word that is addressed is available at the data output port associated with the read-address port.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



NOTE A: One set of ports is shown, the other set functions identically.

FIGURE 1. SETUP AND HOLD TIMES

MegaModule is a trademark of Texas Instruments Incorporated.

PARAMETER MEASUREMENT INFORMATION (Continued)

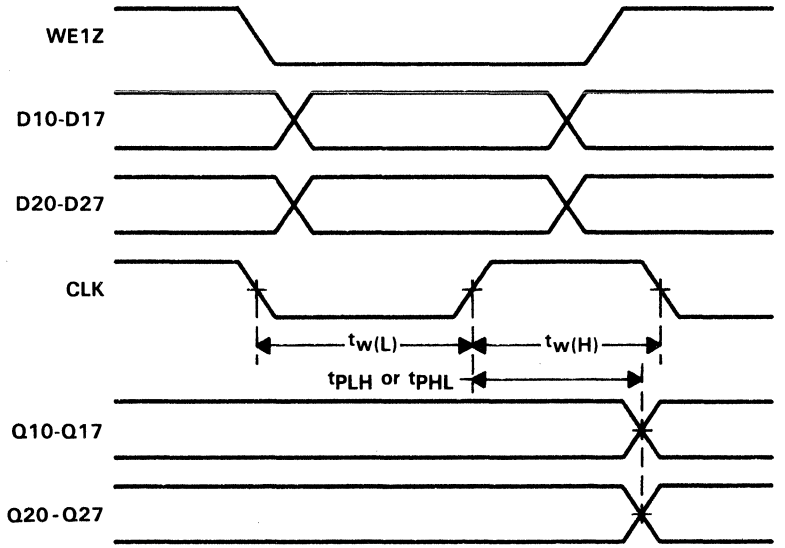


FIGURE 2. CLOCK PULSE DURATION, PROPAGATION DELAY TIMES FROM CLOCK

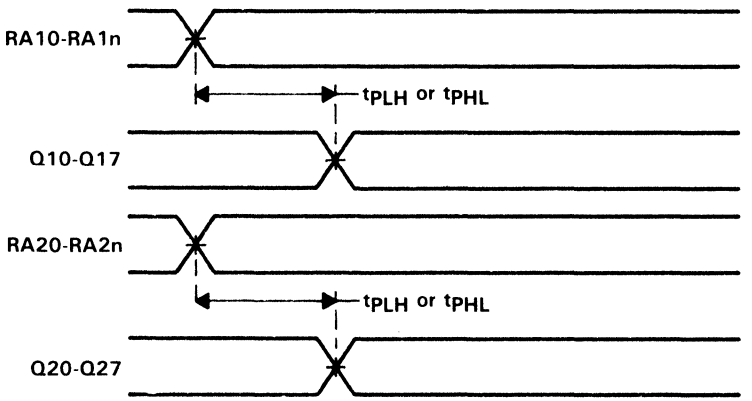


FIGURE 3. PROPAGATION DELAY TIMES FROM READ ADDRESS

MegaModule is a trademark of Texas Instruments Incorporated.

TSC500 SERIES MegaModule™

RF400LJ 16-WORD BY 8-BIT EDGE-TRIGGERED 3-PORT REGISTER FILE WITH 3-STATE OUTPUTS

D3030, DECEMBER 1988

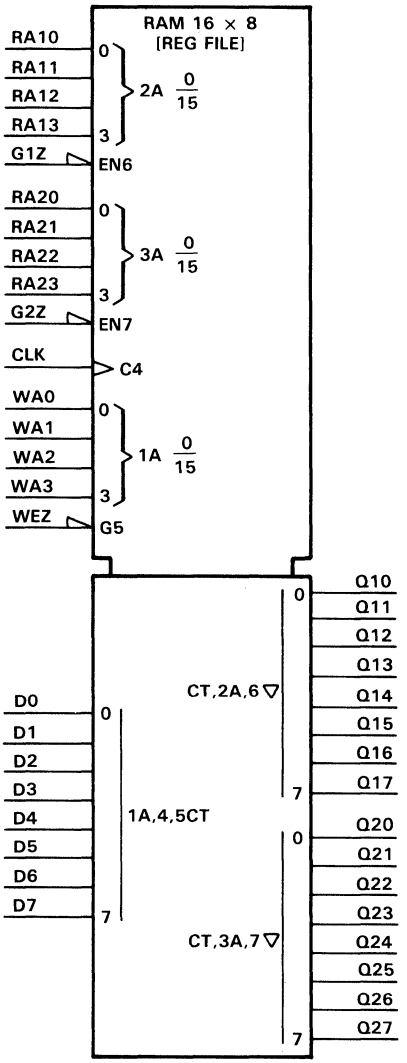
- **Full Parallel Access with One Independent Write Port and Two Independent Read Ports**
- **Use Register Files in Parallel for 16-Bit, 32-Bit, or 64-Bit Word Lengths**
- **Data Retention at V_{CC} > 2 V**

description

The RF400LJ hardwired standard cell MegaModule™ implements a 16-word by 8-bit, 3-port, high-speed register file. When the macro is called from the engineering workstation input, the following label format is developed and captured in the design netlist:

Label: RF400LJ CLK,WEZ,WA0,WA1, WA2,WA3,RA10,RA11,RA12,RA13, RA20,RA21,RA22,RA23,D0,D1,D2, D3,D4,D5,D6,D7,G1Z,G2Z,Q10, Q11,Q12,Q13,Q14,Q15,Q16,Q17, Q20,Q21,Q22,Q23,Q24,Q25,Q26, Q27;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MegaModule is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE

INPUTS				FUNCTION
CLK	WEZ	G1Z	G2Z	
↑	L	X	X	Store data from D0-D7 in location determined by WA0-WA3.
L	X	X	X	No change in stored data
X	H	X	X	No change in stored data
X	X	L	X	Output data through Q10-Q17 from location determined by RA10-RA13.
X	X	X	L	Output data through Q20-Q27 from location determined by RA20-RA23.
X	X	H	X	Outputs Q10-Q17 are in high-impedance state.
X	X	X	H	Outputs Q20-Q27 are in high-impedance state.

SIGNAL DESCRIPTION

NAME	FUNCTION
CLK	Clock input. When WEZ is low, data present at the data input port is stored in the addressed location during a low-to-high transition at the clock input. The clock is inactive while at the high or low level.
D0-D7	8-bit data input port
G1Z	Output enable for output port Q10-Q17; active when low
G2Z	Output enable for output port Q20-Q27; active when low
Q10-Q17 Q20-Q27	Two 8-bit data output ports
RA10-RA13	Read address for output port Q10-Q17
RA20-RA23	Read address for output port Q20-Q27
WA0-WA3	Write address
WEZ	Write enable, active when low

MegaModule is a trademark of Texas Instruments Incorporated.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

Data stored in the register are retained if the supply voltage is not permitted to go below 2 V minimum and remains quiescent until power up. Functional characteristics other than data retention are not specified when V_{CC} = 2 V to 4.5 V.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
t_w	Clock pulse duration	High	3		ns
		Low	3		
t_{su}	Setup time before CLK↑	Write address	4		ns
		Data	1		
		Write enable	5		
t_h	Hold time after CLK↑	Write address	0		ns
		Data	1		
		Write enable	0		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.09		pF
		Dn		0.07		
		GnZ		0.09		
		RBn		0.07		
		WAn		0.06		
		WEZ		0.09		
C_o	Output capacitance			0.22		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	50		pF

MegaModule is a trademark of Texas Instruments Incorporated.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	RAn	Any	$R_L = \infty$	1.72	4.92	11.38	1.82	4.92	10.36	ns
t_{PHL}				1.95	5.31	11.72	2.09	5.31	10.68	
t_{PLH}	CLK	Any	$R_L = \infty$	1.32	4.28	10.16	1.42	4.28	9.28	ns
t_{PHL}				1.5	4.65	10.91	1.6	4.65	9.95	
t_{PZH}	GnZ	Qn	R_L = 40 kΩ to GND	0.47	1.33	3.14	0.49	1.33	2.85	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.27	0.76	1.74	0.29	0.76	1.6	
t_{PHZ}	GnZ	Qn	R_L = 40 kΩ to GND	5.74	6.84	8.56	5.77	6.84	8.31	ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}	2.27	2.76	3.38	2.3	2.75	3.29	
Δt_{PLH}	RAn	Any		0.2	0.6	1.3	0.21	0.6	1.2	ns/pF
Δt_{PHL}				0.14	0.33	0.74	0.15	0.33	0.66	
Δt_{PLH}	CLK	Any		0.21	0.59	1.28	0.22	0.59	1.18	ns/pF
Δt_{PHL}				0.1	0.33	0.72	0.12	0.33	0.64	
Δt_{PZH}	GnZ	Qn		0.23	0.61	1.32	0.24	0.61	1.21	ns/pF
Δt_{PZL}				0.19	0.48	1.06	0.2	0.48	0.96	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

MegaModule is a trademark of Texas Instruments Incorporated.

TSC500 SERIES MegaModule™

RF401LJ 16-WORD BY 8-BIT EDGE-TRIGGERED 4-PORT REGISTER FILE WITH 3-STATE OUTPUTS

D3030, DECEMBER 1988

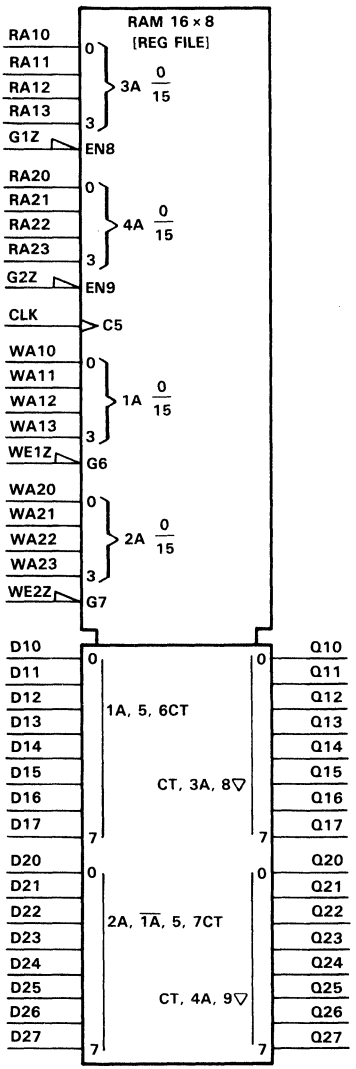
- **Full Parallel Access with Two Independent Write Ports and Two Independent Read Ports**
- **Use Register Files in Parallel for 16-Bit, 32-Bit, or 64-Bit Word Lengths**
- **Data Retention at V_{CC} > 2 V**

description

The RF401LJ hardwired standard cell MegaModule™ implements a 16-word by 8-bit, 4-port, high-speed register file. When the macro is called from the engineering workstation input, the following label format is developed and captured in the design netlist:

Label: RF401LJ CLK,WE1Z,WA10, WA11,WA12,WA13,WE2Z,WA20, WA21,WA22,WA23,RA10,RA11, RA12,RA13,RA20,RA21,RA22,RA23, D10,D11,D12,D13,D14,D15,D16, D17,D20,D21,D22,D23,D24,D25, D26,D27,G1Z,G2Z,Q10,Q11,Q12, Q13,Q14,Q15,Q16,Q17,Q20,Q21, Q22,Q23,Q24,Q25,Q26,Q27;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MegaModule is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

RF401LJ
16-WORD BY 8-BIT EDGE-TRIGGERED 4-PORT REGISTER FILE WITH 3-STATE OUTPUTS

D3030, DECEMBER 1988

FUNCTION TABLE

INPUTS					FUNCTION
CLK	WE1Z	WE2Z	G1Z	G2Z	
↑	L	H	X	X	Store data from D10-D17 in location determined by WA10-WA13.
↑	H	L	X	X	Store data from D20-D27 in location determined by WA20-WA23.
↑	L	L	X	X	Store data from D10-D17 in location determined by WA10-WA13 and store data from D20-D27 in location determined by WA20-WA23. If the addresses are the same, only data from D10-D17 is stored.
L	X	X	X	X	No change in stored data
X	H	H	X	X	No change in stored data
X	X	X	L	X	Output data through Q10-Q17 from location determined by RA10-RA13.
X	X	X	X	L	Output data through Q20-Q27 from location determined by RA20-RA23.
X	X	X	H	X	Outputs Q10-Q17 are in high-impedance state.
X	X	X	X	H	Outputs Q20-Q27 are in high-impedance state.

SIGNAL DESCRIPTION

NAME	FUNCTION
CLK	Clock input. When WEZ is low, data present at the enabled data input port is stored in the addressed location during a low-to-high transition at the clock input. The clock is inactive while at the high or low level.
D10-D17 D20-D27	Two 8-bit data input ports
G1Z	Output enable for output port Q10-Q17; active when low
G2Z	Output enable for output port Q20-Q27; active when low
Q10-Q17 Q20-Q27	Two 8-bit data output ports
RA10-RA13	Read address for output port Q10-Q17
RA20-RA23	Read address for output port Q20-Q27
WA10-WA13	Write address for input port D10-D17
WA20-WA23	Write address for input port D20-D27
WE1Z	Write enable for input port D10-D17; active when low
WE2Z	Write enable for input port D20-D27; active when low

MegaModule is a trademark of Texas Instruments Incorporated.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

Data stored in the register are retained if the supply voltage is not permitted to go below 2 V minimum and remains quiescent until power up. Functional characteristics other than data retention are not specified when V_{CC} = 2 V to 4.5 V.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
t_w	Clock pulse duration	High	3		ns
		Low	3		
t_{su}	Setup time before CLK↑	Write address	6		ns
		Data	2		
		Write enable	6		
t_h	Hold time after CLK↑	Write address	0		ns
		Data	1		
		Write enable	0		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.12		pF
		Dn		0.08		
		GnZ		0.12		
		RAn		0.11		
		WAn		0.08		
		WEnZ		0.12		
C_o	Output capacitance			0.22		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	71		pF

MegaModule is a trademark of Texas Instruments Incorporated.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	RAn	Any	$R_L = \infty$	1.81	5.11	11.74	1.91	5.11	10.7	ns
t_{PHL}				2.08	5.48	11.96	2.21	5.48	10.92	
t_{PLH}	CLK	Any	$R_L = \infty$	1.42	4.49	10.67	1.51	4.49	9.73	ns
t_{PHL}				1.5	4.81	11.33	1.61	4.81	10.32	
t_{PZH}	GnZ	Qn	R_L = 40 kΩ to GND	0.47	1.33	3.14	0.49	1.33	2.85	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.27	0.76	1.74	0.29	0.76	1.6	
t_{PHZ}	GnZ	Qn	R_L = 40 kΩ to GND	5.74	6.84	8.56	5.77	6.84	8.31	ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}	2.27	2.76	3.38	2.3	2.76	3.29	
Δt_{PLH}	CLK	Any		0.19	0.6	1.3	0.21	0.6	1.22	ns/pF
Δt_{PHL}				0.15	0.34	0.72	0.15	0.34	0.66	
Δt_{PLH}	RAn	Any		0.18	0.6	1.32	0.2	0.6	1.22	ns/pF
Δt_{PHL}				0.11	0.32	0.74	0.12	0.32	0.66	
Δt_{PZH}	GnZ	Qn		0.23	0.61	1.32	0.24	0.61	1.21	ns/pF
Δt_{PZL}				0.19	0.48	1.06	0.2	0.48	0.96	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

See general data on 4-port register files.

MegaModule is a trademark of Texas Instruments Incorporated.

TSC500 SERIES MegaModule™

RF402LJ 16-WORD BY 9-BIT EDGE-TRIGGERED 3-PORT REGISTER FILE WITH 3-STATE OUTPUTS

D3030, DECEMBER 1988

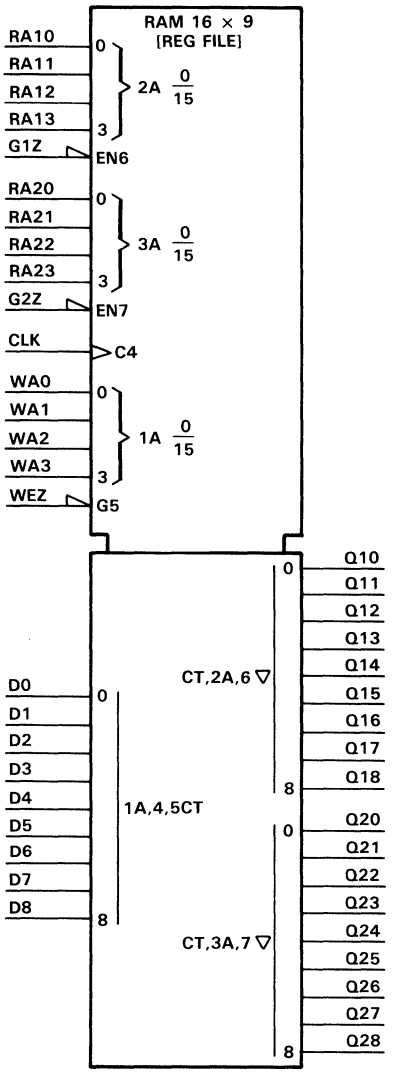
- **Full Parallel Access with One Independent Write Port and Two Independent Read Ports**
- **Use Register Files in Parallel for 18-Bit, 36-Bit, or 72-Bit Word Lengths**
- **Data Retention at V_{CC} > 2 V**

description

The RF402LJ hardwired standard cell MegaModule™ implements a 16-word by 9-bit, 3-port, high-speed register file. The 9-bit organization simplifies implementation of data-paths requiring parity or additional control bits. When the macro is called from the engineering workstation input, the following label format is developed and captured in the design netlist:

Label: RF402LJ CLK,WEZ,WA0,WA1, WA2,WA3,RA10,RA11,RA12,RA13, RA20,RA21,RA22,RA23,D0,D1,D2, D3,D4,D5,D6,D7,G1Z,G2Z,Q10, Q11,Q12,Q13,Q14,Q15,Q16,Q17, Q18,Q20,Q21,Q22,Q23,Q24,Q25, Q26,Q27,Q28;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MegaModule is a trademark of Texas Instruments Incorporated.

RF402LJ
16-WORD BY 9-BIT EDGE-TRIGGERED 3-PORT REGISTER FILE WITH 3-STATE OUTPUTS

D3030, DECEMBER 1988

FUNCTION TABLE

INPUTS				FUNCTION
CLK	WEZ	G1Z	G2Z	
↑	L	X	X	Store data from D0-D8 in location determined by WA0-WA3.
L	X	X	X	No change in stored data
X	H	X	X	No change in stored data
X	X	L	X	Output data through Q10-Q18 from location determined by RA10-RA13.
X	X	X	L	Output data through Q20-Q28 from location determined by RA20-RA23.
X	X	H	X	Outputs Q10-Q18 are in high-impedance state.
X	X	X	H	Outputs Q20-Q28 are in high-impedance state.

SIGNAL DESCRIPTION

NAME	FUNCTION
CLK	Clock input. When WEZ is low, data present at the enabled data input port is stored in the addressed location during a low-to-high transition at the clock input. The clock is inactive while at the high or low level.
D0-D8	9-bit data input port
G1Z	Output enable for output port Q10-Q18; active when low
G2Z	Output enable for output port Q20-Q28; active when low
Q10-Q18 Q20-Q28	Two 9-bit data output ports
RA10-RA13	Read address for output port Q10-Q18
RA20-RA23	Read address for output port Q20-Q28
WA0-WA3	Write address
WEZ	Write enable, active when low

MegaModule is a trademark of Texas Instruments Incorporated.

RF402LJ
16-WORD BY 9-BIT EDGE-TRIGGERED 3-PORT REGISTER FILE WITH 3-STATE OUTPUTS

D3030, DECEMBER 1988

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

Data stored in the register are retained if the supply voltage is not permitted to go below 2 V minimum and remains quiescent until power up. Functional characteristics other than data retention are not specified when V_{CC} = 2 V to 4.5 V.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
t_w	Clock pulse duration	High	3		ns
		Low	3		
t_{su}	Setup time before CLK↑	Write address	5		ns
		Data	1		
		Write enable	5		
t_h	Hold time after CLK↑	Write address	0		ns
		Data	1		
		Write enable	0		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.09		pF
		Dn		0.07		
		GnZ		0.09		
		RAn		0.07		
		WAn		0.06		
		WEZ		0.09		
C_o	Output capacitance			0.22		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	53		pF

MegaModule is a trademark of Texas Instruments Incorporated.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	RAn	Any	$R_L = \infty$	1.71	5	11.57	1.82	5	10.53	ns
t_{PHL}				1.98	5.39	11.87	2.11	5.39	10.84	
t_{PLH}	CLK	Any	$R_L = \infty$	1.38	4.37	10.33	1.47	4.37	9.43	ns
t_{PHL}				1.51	4.72	11.07	1.62	4.72	10.12	
t_{PZH}	GnZ	Qn	R_L = 40 kΩ to GND	0.47	1.33	3.14	0.49	1.33	2.85	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.27	0.76	1.74	0.29	0.76	1.6	
t_{PHZ}	GnZ	Qn	R_L = 40 kΩ to GND	5.74	6.84	8.56	5.77	6.84	8.31	ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}	2.27	2.76	3.38	2.3	2.76	3.29	
Δt_{PLH}	CLK	Any		0.18	0.59	1.3	0.2	0.59	1.2	ns/pF
Δt_{PHL}				0.11	0.33	0.74	0.13	0.33	0.66	
Δt_{PLH}	RAn	Any		0.21	0.6	1.3	0.22	0.6	1.2	ns/pF
Δt_{PHL}				0.13	0.33	0.74	0.13	0.33	0.66	
Δt_{PZH}	GnZ	Qn		0.23	0.61	1.32	0.24	0.61	1.21	ns/pF
Δt_{PZL}				0.19	0.48	1.06	0.2	0.48	0.96	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

See general data on 3-port register files.

MegaModule is a trademark of Texas Instruments Incorporated.

TSC500 SERIES MegaModule™

RF403LJ 16-WORD BY 12-BIT EDGE-TRIGGERED 3-PORT REGISTER FILE WITH 3-STATE OUTPUTS

D3030, DECEMBER 1988

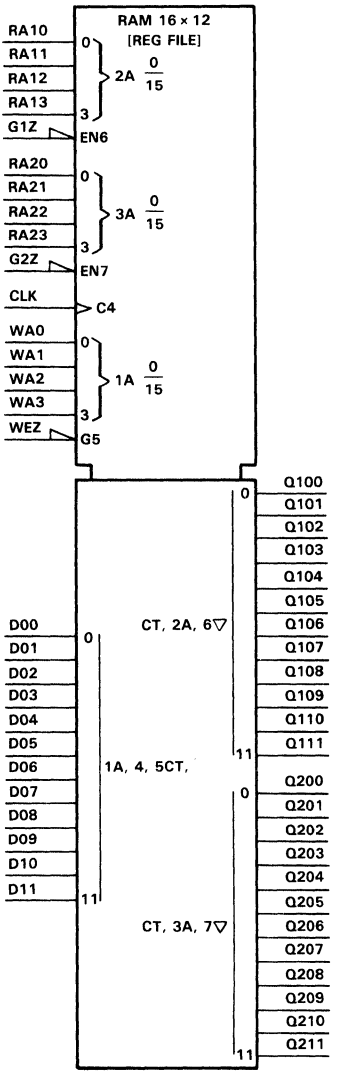
- **Full Parallel Access with One Independent Write Port and Two Independent Read Ports**
- **Use Register Files in Parallel for 24-Bit, 48-Bit, or 96-Bit Word Lengths**
- **Data Retention at V_{CC} > 2 V**

description

The RF403LJ hardwired standard cell MegaModule™ implements a 16-word by 12-bit, 3-port, high-speed register file. The 12-bit organization simplifies implementation of data-paths requiring parity and/or additional control bits. When the macro is called from the engineering workstation input, the following label format is developed and captured in the design netlist:

Label: RF403LJ CLK,WEZ,WA0,WA1, WA2,WA3,RA10,RA11,RA12,RA13, RA20,RA21,RA22,RA23,D00,D01, D02,D03,D04,D05,D06,D07,D08, D09,D10,D11,G1Z,G2Z,Q100,Q101, Q102,Q103,Q104,Q105,Q106,Q107, Q108,Q109,Q110,Q111,Q200, Q201,Q202,Q203,Q204,Q205,Q206, Q207,Q208,Q209,Q210,Q211;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MegaModule is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

RF403LJ
16-WORD BY 12-BIT EDGE-TRIGGERED 3-PORT REGISTER FILE WITH 3-STATE OUTPUTS

TSC500 SERIES
MegaModule™

D3030, DECEMBER 1988

FUNCTION TABLE

INPUTS				FUNCTION
CLK	WEZ	G1Z	G2Z	
↑	L	X	X	Store data from D0-D11 in location determined by WA0-WA3.
L	X	X	X	No change in stored data
X	H	X	X	No change in stored data
X	X	L	X	Output data through Q100-Q111 from location determined by RA10-RA13.
X	X	X	L	Output data through Q200-Q211 from location determined by RA20-RA23.
X	X	H	X	Outputs Q100-Q111 are in high-impedance state.
X	X	X	H	Outputs Q200-Q211 are in high-impedance state.

SIGNAL DESCRIPTION

NAME	FUNCTION
CLK	Clock input. When WEZ is low, data present at the enabled data input port is stored in the addressed location during a low-to-high transition at the clock input. The clock is inactive while at the high or low level.
D00-D11	12-bit data input port
G1Z	Output enable for output port Q100-Q111; active when low
G2Z	Output enable for output port Q200-Q211 active when low
Q100-Q111 Q200-Q211	Two 9-bit data output ports
RA10-RA13	Read address for output port Q100-Q111
RA20-RA23	Read address for output port Q200-Q211
WA0-WA3	Write address
WEZ	Write enable, active when low

MegaModule is a trademark of Texas Instruments Incorporated.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

Data stored in the register are retained if the supply voltage is not permitted to go below 2 V minimum and remains quiescent until power up. Functional characteristics other than data retention are not specified when V_{CC} = 2 V to 4.5 V.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
t_w	Clock pulse duration	High	3		ns
		Low	3		
t_{su}	Setup time before CLK↑	Write address	7.4		ns
		Data	2.6		
		Write enable	6		
t_h	Hold time after CLK↑	Write address	0		ns
		Data	1.7		
		Write enable	0		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.09		pF
		Dn		0.07		
		GnZ		0.09		
		RAn		0.07		
		WAn		0.06		
		WEZ		0.09		
C_o	Output capacitance			0.22		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	53		pF

MegaModule is a trademark of Texas Instruments Incorporated.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	RAn	Any	$R_L = \infty$	2.13	6.3	14.63	2.29	6.3	13.31	ns
t_{PHL}				2.59	6.91	14.8	2.78	6.91	13.54	
t_{PLH}	CLK	Any	$R_L = \infty$	1.87	5.86	13.64	2	5.86	12.48	ns
t_{PHL}				2.14	6.35	14.4	2.29	6.35	13.15	
t_{PZH}	GnZ	Qn	R_L = 40 kΩ to GND	0.52	1.7	4.14	0.55	1.7	3.77	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.29	0.88	2.1	0.3	0.88	1.92	
t_{PHZ}	GnZ	Qn	R_L = 40 kΩ to GND	5.79	7.24	9.7	5.83	7.24	9.31	ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}	2.34	2.87	3.67	2.35	2.87	3.57	
Δt_{PLH}	CLK	Any		0.15	0.4	0.92	0.16	0.4	0.84	ns/pF
Δt_{PHL}				0.07	0.18	0.34	0.08	0.18	0.32	
Δt_{PLH}	RAn	Any		0.16	0.37	0.82	0.15	0.37	0.78	ns/pF
Δt_{PHL}				0.08	0.14	0.3	0.08	0.14	0.28	
Δt_{PZH}	GnZ	Qn		0.25	0.65	1.4	0.26	0.65	1.28	ns/pF
Δt_{PZL}				0.2	0.53	1.2	0.21	0.53	1.09	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

See general data on 3-port register files.

MegaModule is a trademark of Texas Instruments Incorporated.

TSC500 SERIES MegaModule™

RF600LJ 64-WORD BY 8-BIT EDGE-TRIGGERED 3-PORT REGISTER FILE WITH 3-STATE OUTPUTS

D3030, DECEMBER 1988

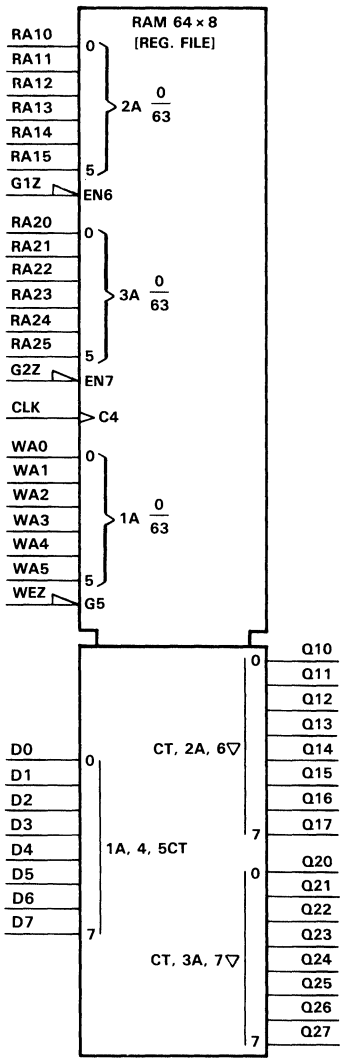
- **Full Parallel Access with One Independent Write Port and Two Independent Read Ports**
- **Use Register Files in Parallel for 16-Bit, 32-Bit, or 64-Bit Word Lengths**
- **Data Retention at V_{CC} > 2 V**

description

The RF600LJ hardwired standard cell MegaModule™ implements a 64-word by 8-bit, 3-port, high-speed register file. When the macro is called from the engineering workstation input, the following label format is developed and captured in the design netlist:

Label: RF600LJ CLK,WEZ,WA0,WA1, WA2,WA3,WA4,WA5,RA10,RA11, RA12,RA13,RA14,RA15,RA20,RA21, RA22,RA23,RA24,RA25,D0,D1,D2, D3,D4,D5,D6,D7,G1Z,G2Z,Q10, Q11,Q12,Q13,Q14,Q15,Q16,Q17, Q20,Q21,Q22,Q23,Q24,Q25,Q26, Q27;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MegaModule is a trademark of Texas Instruments Incorporated.

RF600LJ
64-WORD BY 8-BIT EDGE-TRIGGERED 3-PORT REGISTER FILE WITH 3-STATE OUTPUTS

D3030, DECEMBER 1988

FUNCTION TABLE

INPUTS				FUNCTION
CLK	WEZ	G1Z	G2Z	
↑	L	X	X	Store data from D0-D7 in location determined by WA0-WA3.
L	X	X	X	No change in stored data
X	H	X	X	No change in stored data
X	X	L	X	Output data through Q10-Q17 from location determined by RA10-RA15.
X	X	X	L	Output data through Q20-Q27 from location determined by RA20-RA25.
X	X	H	X	Outputs Q10-Q17 are in high-impedance state.
X	X	X	H	Outputs Q20-Q27 are in high-impedance state.

SIGNAL DESCRIPTION

NAME	FUNCTION
CLK	Clock input. When WEZ is low, data present at the enabled data input port is stored in the addressed location during a low-to-high transition at the clock input. The clock is inactive while at the high or low level.
D0-D7	8-bit data input port
G1Z	Output enable for output port Q10-Q17; active when low
G2Z	Output enable for output port Q20-Q27; active when low
Q10-Q17 Q20-Q27	Two 8-bit data output ports
RA10-RA15	Read address for output port Q10-Q17
RA20-RA25	Read address for output port Q20-Q27
WA0-WA5	Write address
WEZ	Write enable, active when low

MegaModule is a trademark of Texas Instruments Incorporated.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

Data stored in the register are retained if the supply voltage is not permitted to go below 2 V minimum and remains quiescent until power up. Functional characteristics other than data retention are not specified when V_{CC} = 2 V to 4.5 V.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
t_w	Clock pulse duration	High	3		ns
		Low	3		
t_{su}	Setup time before CLK↑	Write address	5		ns
		Data	2		
		Write enable	4		
t_h	Hold time after CLK↑	Write address	0		ns
		Data	0		
		Write enable	0		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.38		pF
		Dn		0.09		
		GnZ		0.13		
		RAn		0.34		
		WAn		0.34		
		WEZ		0.13		
C_o	Output capacitance			0.22		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	60		pF

MegaModule is a trademark of Texas Instruments Incorporated.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	RAn	Any	$R_L = \infty$	1.74	4.95	11.25	1.85	4.95	10.28	ns
t_{PHL}				2.21	6	13.43	2.35	6	12.24	
t_{PLH}	CLK	Any	$R_L = \infty$	2.23	6.76	15.56	2.38	6.76	14.21	ns
t_{PHL}				1.99	6.13	14.19	2.13	6.13	12.93	
t_{PZH}	GnZ	Qn	R_L = 40 kΩ to GND	0.56	1.59	3.8	0.58	1.59	3.43	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.33	0.89	2.16	0.34	0.89	1.93	
t_{PHZ}	GnZ	Qn	R_L = 40 kΩ to GND	6.78	7.91	9.66	6.82	7.91	9.38	ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}	2.75	3.23	3.95	2.77	3.23	3.83	
Δt_{PLH}	Any	Any		0.2	0.65	1.42	0.22	0.65	1.3	ns/pF
Δt_{PHL}				0.12	0.31	0.62	0.12	0.31	0.56	
Δt_{PZH}	GnZ	Qn		0.22	0.59	1.28	0.23	0.59	1.18	ns/pF
Δt_{PZL}				0.19	0.51	1.08	0.2	0.51	1.01	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

See general data on 3-port register files.

MegaModule is a trademark of Texas Instruments Incorporated.

TSC500 SERIES
MegaModule™

RF601LJ
64-WORD BY 8-BIT EDGE-TRIGGERED 4-PORT REGISTER FILE WITH 3-STATE OUTPUTS

D3030, DECEMBER 1988

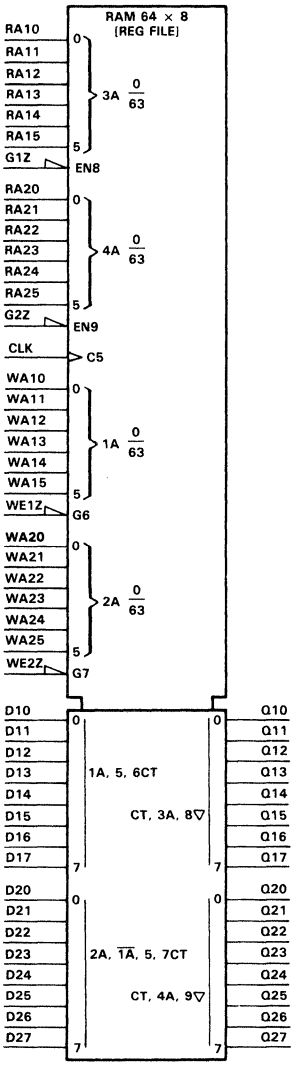
- **Full Parallel Access with Two Independent Write Ports and Two Independent Read Ports**
- **Use Register Files in Parallel for 16-Bit, 32-Bit, or 64-Bit Word Lengths**
- **Data Retention at V_{CC} > 2 V**

description

The RF601LJ hardwired standard cell MegaModule™ implements a 64-word by 8-bit, 4-port, high-speed register file. When the macro is called from the engineering workstation input, the following label format is developed and captured in the design netlist:

Label: RF601LJ CLK,WE1Z,WA10, WA11,WA12,WA13,WA14,WA15, WE2Z,WA20,WA21,WA22,WA23, WA24,WA25,RA10,RA11,RA12,RA13, RA14,RA15,RA20,RA21,RA22,RA23, RA24,RA25,D10,D11,D12,D13,D14, D15,D16,D17,D20,D21,D22,D23, D24,D25,D26,D27,G1Z,G2Z,Q10, Q11,Q12,Q13,Q14,Q15,Q16,Q17, Q20,Q21,Q22,Q23,Q24,;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MegaModule is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

FUNCTION TABLE

INPUTS					FUNCTION
CLK	WE1Z	WE2Z	G1Z	G2Z	
↑	L	H	X	X	Store data from D10-D17 in location determined by WA10-WA15.
↑	H	L	X	X	Store data from D20-D27 in location determined by WA20-WA25.
↑	L	L	X	X	Store data from D10-D17 in location determined by WA10-WA15 and store data from D20-D27 in location determined by WA20-WA25. If the addresses are the same, only data from D10-D17 is stored.
L	X	X	X	X	No change in stored data
X	H	H	X	X	No change in stored data
X	X	X	L	X	Output data through Q10-Q17 from location determined by RA10-RA15.
X	X	X	X	L	Output data through Q20-Q27 from location determined by RA20-RA25.
X	X	X	H	X	Outputs Q10-Q17 are in high-impedance state.
X	X	X	X	H	Outputs Q20-Q27 are in high-impedance state.

SIGNAL DESCRIPTION

NAME	FUNCTION
CLK	Clock input. When WEZ is low, data present at the enabled data input port is stored in the addressed location during a low-to-high transition at the clock input. The clock is inactive while at the high or low level.
D10-D17 D20-D27	Two 8-bit data input ports
G1Z	Output enable for output port Q10-Q17; active when low
G2Z	Output enable for output port Q20-Q27; active when low
Q10-Q17 Q20-Q27	Two 8-bit data output ports
RA10-RA15	Read address for output port Q10-Q17
RA20-RA25	Read address for output port Q20-Q27
WA10-WA15	Write address for input port D10-D17
WA20-WA25	Write address for input port D20-D27
WE1Z	Write enable for input port D10-D17; active when low
WE2Z	Write enable for input port D20-D27; active when low

MegaModule is a trademark of Texas Instruments Incorporated.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

Data stored in the register are retained if the supply voltage is not permitted to go below 2 V minimum and remains quiescent until power up. Functional characteristics other than data retention are not specified when V_{CC} = 2 V to 4.5 V.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
t_w	Clock pulse duration	High	3		ns
		Low	3		
t_{su}	Setup time before CLK↑	Write address	5		ns
		Data	2		
		Write enable	4		
t_h	Hold time after CLK↑	Write address	0		ns
		Data	0		
		Write enable	0		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.38		pF
		Dn		0.09		
		GnZ		0.13		
		RAn		0.34		
		WAn		0.34		
		WEnZ		0.13		
C_o	Output capacitance			0.22		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	101		pF

MegaModule is a trademark of Texas Instruments Incorporated.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	RAn	Any	$R_L = \infty$	1.76	4.99	11.35	1.88	4.99	10.36	ns
t_{PHL}				2.19	6.06	13.66	2.34	6.06	12.43	
t_{PLH}	CLK	Any	$R_L = \infty$	2.41	7.36	16.97	2.58	7.36	15.47	ns
t_{PHL}				2.26	6.91	16.03	2.42	6.91	14.59	
t_{PZH}	GnZ	Qn	R_L = 40 kΩ to GND	0.56	1.59	3.8	0.58	1.59	3.43	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.33	0.89	2.16	0.34	0.89	1.93	
t_{PHZ}	GnZ	Qn	R_L = 40 kΩ to GND	6.78	7.91	9.66	6.82	7.91	9.38	ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}	2.75	3.23	3.95	2.77	3.23	3.83	
Δt_{PLH}	CLK	Any		0.22	0.65	1.42	0.23	0.65	1.32	ns/pF
Δt_{PHL}				0.12	0.32	0.66	0.13	0.32	0.6	
Δt_{PLH}	RAn	Any		0.25	0.66	1.42	0.26	0.66	1.3	ns/pF
Δt_{PHL}				0.15	0.3	0.74	0.15	0.3	0.5	
Δt_{PZH}	GnZ	Qn		0.22	0.59	1.28	0.23	0.59	1.18	ns/pF
Δt_{PZL}				0.19	0.51	1.08	0.2	0.51	1.01	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

See general data on 4-port register files.

TSC500 SERIES MegaModule™

RF602LJ 64-WORD BY 9-BIT EDGE-TRIGGERED 3-PORT REGISTER FILE WITH 3-STATE OUTPUTS

D3030, DECEMBER 1988

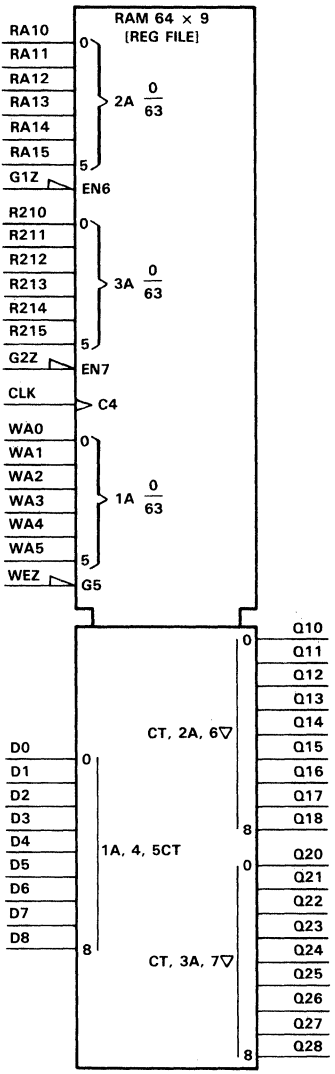
- **Full Parallel Access with One Independent Write Port and Two Independent Read Ports**
- **Use Register Files in Parallel for 18-Bit, 36-Bit, or 72-Bit Word Lengths**
- **Data Retention at V_{CC} > 2 V**

description

The RF602LJ hardwired standard cell MegaModule™ implements a 64-word by 9-bit, 3-port, high-speed register file. The 9-bit organization simplifies implementation of data-paths requiring parity or additional control bits. When the macro is called from the engineering workstation input, the following label format is developed and captured in the design netlist:

Label: RF602LJ CLK,WEZ,WA0,WA1, WA2,WA3,WA4,WA5,RA10,RA11, RA12,RA13,RA14,RA15,RA20,RA21, RA22,RA23,RA24,RA25,D0,D1,D2, D3,D4,D5,D6,D7,G1Z,G2Z,Q10, Q11,Q12,Q13,Q14,Q15,Q16,Q17, Q20,Q21,Q22,Q23,Q24,Q25,Q26, Q27,Q28;

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MegaModule is a trademark of Texas Instruments Incorporated.

RF602LJ
64-WORD BY 9-BIT EDGE-TRIGGERED 3-PORT REGISTER FILE WITH 3-STATE OUTPUTS

TSC500 SERIES
MegaModule™

D3030, DECEMBER 1988

FUNCTION TABLE

INPUTS				FUNCTION
CLK	WEZ	G1Z	G2Z	
↑	L	X	X	Store data from D0-D8 in location determined by WA0-WA5.
L	X	X	X	No change in stored data
X	H	X	X	No change in stored data
X	X	L	X	Output data through Q10-Q18 from location determined by RA10-RA15.
X	X	X	L	Output data through Q20-Q28 from location determined by RA20-RA25.
X	X	H	X	Outputs Q10-Q18 are in high-impedance state.
X	X	X	H	Outputs Q20-Q28 are in high-impedance state.

SIGNAL DESCRIPTION

NAME	FUNCTION
CLK	Clock input. When WEZ is low, data present at the enabled data input port is stored in the addressed location during a low-to-high transition at the clock input. The clock is inactive while at the high or low level.
D0-D8	9-bit data input port
G1Z	Output enable for output port Q10-Q18; active when low
G2Z	Output enable for output port Q20-Q28; active when low
Q10-Q18 Q20-Q28	Two 9-bit data output ports
RA10-RA15	Read address for output port Q10-Q18
RA20-RA25	Read address for output port Q20-Q28
WA0-WA5	Write address
WEZ	Write enable, active when low

MegaModule is a trademark of Texas Instruments Incorporated.

absolute maximum ratings and recommended operating conditions

These are specified as a part of the TSC500 Series Data.

Data stored in the register are retained if the supply voltage is not permitted to go below 2 V minimum and remains quiescent until power up. Functional characteristics other than data retention are not specified when V_{CC} = 2 V to 4.5 V.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
t_w	Clock pulse duration	High	3		ns
		Low	3		
t_{su}	Setup time before CLK↑	Write address	5		ns
		Data	2		
		Write enable	4		
t_h	Hold time after CLK↑	Write address	0		ns
		Data	0		
		Write enable	0		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	MAX	UNIT
V_T	Input threshold voltage			2.2		V
C_i	Input capacitance	CLK		0.38		pF
		Dn		0.09		
		GnZ		0.13		
		RAn		0.34		
		WAn		0.34		
		WEnZ		0.13		
C_o	Output capacitance			0.22		pF
C_{pd}	Equivalent power dissipation capacitance		$t_r = t_f$ = 1 ns	74		pF

MegaModule is a trademark of Texas Instruments Incorporated.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), C_L = 0

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−55°C to 125°C			0°C to 70°C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	RAn	Any	$R_L = \infty$	1.81	5.04	11.41	1.92	5.04	10.41	ns
t_{PHL}				2.23	6.14	13.71	2.38	6.14	12.5	
t_{PLH}	CLK	Any	$R_L = \infty$	2.25	6.83	15.69	2.4	6.83	14.33	ns
t_{PHL}				2.01	6.19	14.32	2.16	6.19	13.04	
t_{PZH}	GnZ	Qn	R_L = 40 kΩ to GND	0.56	1.59	3.8	0.58	1.59	3.43	ns
t_{PZL}			R_L = 20 kΩ to V_{CC}	0.33	0.89	2.16	0.34	0.89	1.93	
t_{PHZ}	GnZ	Qn	R_L = 40 kΩ to GND	6.78	7.91	9.66	6.82	7.91	9.38	ns
t_{PLZ}			R_L = 20 kΩ to V_{CC}	2.75	3.23	3.95	2.77	3.23	3.83	
Δt_{PLH}	Any	Any		0.2	0.63	1.42	0.22	0.63	1.3	ns/pF
Δt_{PHL}				0.11	0.29	0.62	0.13	0.29	0.58	
Δt_{PLH}	GnZ	Qn		0.22	0.59	1.28	0.23	0.59	1.18	ns/pF
Δt_{PHL}				0.19	0.51	1.08	0.2	0.51	1.01	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

See general data on 3-port register files.

MegaModule is a trademark of Texas Instruments Incorporated.

TI Sales Offices

ALABAMA: Huntsville (205) 837-7530.

ARIZONA: Phoenix (602) 995-1007;
Tucson (602) 292-2640.

CALIFORNIA: Irvine (714) 660-1200;
Roseville (916) 786-9208;
San Diego (619) 278-9601;
Santa Clara (408) 980-9000;
Torrance (213) 217-7010;
Woodland Hills (818) 704-7759.

COLORADO: Aurora (303) 368-8000.

CONNECTICUT: Wallingford (203) 269-0074.

FLORIDA: Altamonte Springs (305) 260-2116;
Ft. Lauderdale (305) 973-8502;
Tampa (813) 885-7411.

GEORGIA: Norcross (404) 662-7900.

ILLINOIS: Arlington Heights (312) 640-2925.

INDIANA: Carmel (317) 573-6400;
Ft. Wayne (219) 424-5174.

IOWA: Cedar Rapids (319) 395-9550.

KANSAS: Overland Park (913) 451-4511.

MARYLAND: Columbia (301) 964-2003.

MASSACHUSETTS: Waltham (617) 895-9100.

MICHIGAN: Farmington Hills (313) 553-1569;
Grand Rapids (616) 957-4200.

MINNESOTA: Eden Prairie (612) 828-9300.

MISSOURI: St. Louis (314) 569-7600.

NEW JERSEY: Iselin (201) 750-1050.

NEW MEXICO: Albuquerque (505) 345-2555.

NEW YORK: East Syracuse (315) 463-9291;
Melville (516) 454-6600;
Pittsford (716) 385-6770;
Poughkeepsie (914) 473-2900.

NORTH CAROLINA: Charlotte (704) 527-0933;
Raleigh (919) 876-2725.

OHIO: Beachwood (216) 464-6100;
Beaver Creek (513) 427-6200.

OREGON: Beaverton (503) 643-6758.

PENNSYLVANIA: Blue Bell (215) 825-9500.

PUERTO RICO: Hato Rey (809) 753-8700.

TENNESSEE: Johnson City (615) 461-2192.

TEXAS: Austin (512) 250-7655;
Houston (713) 778-6592;
Richardson (214) 680-5082;
San Antonio (512) 496-1779.

UTAH: Murray (801) 266-8972.

WASHINGTON: Redmond (206) 881-3080.

WISCONSIN: Brookfield (414) 782-2899.

CANADA: Nepean, Ontario (613) 726-1970;
Richmond Hill, Ontario (416) 884-9181;
St. Laurent, Quebec (514) 336-1860.

TI Regional Technology Centers

CALIFORNIA: Irvine (714) 660-8105;
Santa Clara (408) 748-2220;

GEORGIA: Norcross (404) 662-7945.

ILLINOIS Arlington Heights (312) 640-2909.

MASSACHUSETTS: Waltham (617) 895-9196.

TEXAS: Richardson (214) 680-5066.

CANADA: Nepean, Ontario (613) 726-1970.

TI Distributors

TI AUTHORIZED DISTRIBUTORS
Arrow/Kierulff Electronics Group
Arrow (Canada)
Future Electronics (Canada)
GRS Electronics Co., Inc.
Hall-Mark Electronics
Marshall Industries
Newark Electronics
Schweber Electronics
Time Electronics
Wyle Laboratories
Zeus Components

–OBSOLETE PRODUCT ONLY–
Rochester Electronics, Inc.
Newburyport, Massachusetts
(508) 462-9332

ALABAMA: Arrow/Kierulff (205) 837-6955;
Hall-Mark (205) 837-8700; Marshall (205) 881-9235;
Schweber (205) 895-0480.

ARIZONA: Arrow/Kierulff (602) 437-0750;
Hall-Mark (602) 437-1200; Marshall (602) 496-0290;
Schweber (602) 431-0030; Wyle (602) 866-2888.

CALIFORNIA: Los Angeles/Orange County:
Arrow/Kierulff (818) 701-7500, (714) 838-5422;
Hall-Mark (818) 773-4500, (714) 669-4100;
Marshall (818) 407-0101, (818) 459-5500,
(714) 458-5395; Schweber (818) 880-9686;
(714) 863-0200, (213) 320-8090; Wyle (818) 880-9000,
(714) 863-9953; Zeus (714) 921-9000; (818) 889-3838;
Sacramento: Hall-Mark (916) 624-9781;
Marshall (916) 635-9700; Schweber (916) 364-0222;
Wyle (916) 638-5282;
San Diego: Arrow/Kierulff (619) 565-4800;
Hall-Mark (619) 268-1201; Marshall (619) 578-9600;
Schweber (619) 450-0454; Wyle (619) 565-9171;
San Francisco Bay Area: Arrow/Kierulff (408) 745-6600,
Hall-Mark (408) 432-0900; Marshall (408) 942-4600;
Schweber (408) 432-7171; Wyle (408) 727-2500;
Zeus (408) 998-5121.

COLORADO: Arrow/Kierulff (303) 790-4444;
Hall-Mark (303) 790-1662; Marshall (303) 451-8383;
Schweber (303) 799-0258; Wyle (303) 457-9953.

CONNETICUT: Arrow/Kierulff (203) 265-7741;
Hall-Mark (203) 271-2844; Marshall (203) 265-3822;
Schweber (203) 264-4700.

FLORIDA: Ft. Lauderdale:
Arrow/Kierulff (305) 429-8200; Hall-Mark (305) 971-9280;
Marshall (305) 977-4880; Schweber (305) 977-7511;
Orlando: Arrow/Kierulff (407) 323-0252;
Hall-Mark (407) 830-5855; Marshall (407) 767-8585;
Schweber (407) 331-7555; Zeus (407) 365-3000;
Tampa: Hall-Mark (813) 530-4543;
Marshall (813) 576-1399; Schweber (813) 541-5100.

GEORGIA: Arrow/Kierulff (404) 449-8252;
Hall-Mark (404) 447-8000; Marshall (404) 923-5750;
Schweber (404) 449-9170.

ILLINOIS: Arrow/Kierulff (312) 250-0500;
Hall-Mark (312) 860-3800; Marshall (312) 490-0155;
Newark (312) 784-5100; Schweber (312) 364-3750.

INDIANA: Indianapolis: Arrow/Kierulff (317) 243-9353;
Hall-Mark (317) 872-8875; Marshall (317) 297-0483;
Schweber (317) 843-1050.

IOWA: Arrow/Kierulff (319) 395-7230;
Schweber (319) 373-1417.

KANSAS: Kansas City: Arrow/Kierulff (913) 541-9542;
Hall-Mark (913) 888-4747; Marshall (913) 492-3121;
Schweber (913) 492-2922.

TEXAS INSTRUMENTS

MARYLAND: Arrow/Kierulff (301) 995-6002;
Hall-Mark (301) 988-9800; Marshall (301) 235-9464;
Schweber (301) 840-5900; Zeus (301) 997-1118.

MASSACHUSETTS Arrow/Kierulff (508) 658-0900;
Hall-Mark (508) 667-0902; Marshall (508) 658-0810;
Schweber (617) 275-5100; Time (617) 532-6200;
Wyle (617) 273-7300; Zeus (617) 863-8800.

MICHIGAN: Detroit: Arrow/Kierulff (313) 462-2290;
Hall-Mark (313) 462-1205; Marshall (313) 525-5850;
Newark (313) 967-0600; Schweber (313) 525-8100;
Grand Rapids: Arrow/Kierulff (616) 243-0912.

MINNESOTA: Arrow/Kierulff (612) 830-1800;
Hall-Mark (612) 941-2600; Marshall (612) 559-2211;
Schweber (612) 941-5280.

MISSOURI: St. Louis: Arrow/Kierulff (314) 567-6888;
Hall-Mark (314) 291-5350; Marshall (314) 291-4650;
Schweber (314) 739-0526.

NEW HAMPSHIRE: Arrow/Kierulff (603) 668-6968;
Schweber (603) 625-2250.

NEW JERSEY: Arrow/Kierulff (201) 538-0900,
(609) 596-8000; GRS Electronics (609) 964-8560;
Hall-Mark (201) 575-4415, (201) 882-9773,
(609) 235-1900; Marshall (201) 882-0320,
(609) 234-9100; Schweber (201) 227-7880.

NEW MEXICO: Arrow/Kierulff (505) 243-4566.

NEW YORK: Long Island:
Arrow/Kierulff (516) 231-1009; Hall-Mark (516) 737-0600;
Marshall (516) 273-2424; Schweber (516) 334-7474;
Zeus (914) 937-7400;
Rochester: Arrow/Kierulff (716) 427-0300;
Hall-Mark (716) 425-3300; Marshall (716) 235-7620;
Schweber (716) 424-2222;
Syracuse: Marshall (607) 798-1611.

NORTH CAROLINA: Arrow/Kierulff (919) 876-3132,
(919) 725-8711; Hall-Mark (919) 872-0712;
Marshall (919) 878-9882; Schweber (919) 876-0000.

OHIO: Cleveland: Arrow/Kierulff (216) 248-3990;
Hall-Mark (216) 349-4632; Marshall (216) 248-1788;
Schweber (216) 464-2970;
Columbus: Hall-Mark (614) 888-3313;
Dayton: Arrow/Kierulff (513) 435-5563;
Marshall (513) 898-4480; Schweber (513) 439-1800.

OKLAHOMA: Arrow/Kierulff (918) 252-7537;
Schweber (918) 622-8003.

OREGON: Arrow/Kierulff (503) 645-6456;
Marshall (503) 644-5050; Wyle (503) 640-6000.

PENNSYLVANIA: Arrow/Kierulff (412) 856-7000,
(215) 928-1800; GRS Electronics (215) 922-7037;
Marshall (412) 963-0441; Schweber (215) 441-0600,
(412) 963-6804.

TEXAS: Austin: Arrow/Kierulff (512) 835-4180;
Hall-Mark (512) 258-8848; Marshall (512) 837-1991;
Schweber (512) 339-0088; Wyle (512) 834-9957;
Dallas: Arrow/Kierulff (214) 380-6464;
Hall-Mark (214) 553-4300; Marshall (214) 233-5200;
Schweber (214) 661-5010; Wyle (214) 235-9953;
Zeus (214) 783-7010;
El Paso: Marshall (915) 593-0706;
Houston: Arrow/Kierulff (713) 530-4700;
Hall-Mark (713) 781-6100; Marshall (713) 895-9200;
Schweber (713) 784-3600; Wyle (713) 879-9953.

UTAH: Arrow/Kierulff (801) 973-6913;
Hall-Mark (801) 972-1008; Marshall (801) 485-1551;
Wyle (801) 974-9953.

WASHINGTON: Arrow/Kierulff (206) 575-4420;
Marshall (206) 486-5747; Wyle (206) 881-1150.

WISCONSIN: Arrow/Kierulff (414) 792-0150;
Hall-Mark (414) 797-7844; Marshall (414) 797-8400;
Schweber (414) 784-9020.

CANADA: Calgary: Future (403) 235-5325;
Edmonton: Future (403) 438-2858;
Montreal: Arrow Canada (514) 735-5511;
Future (514) 694-7710;
Ottawa: Arrow Canada (613) 226-6903;
Future (613) 820-8313;
Quebec City: Arrow Canada (418) 871-7500;
Toronto: Arrow Canada (416) 672-7769;
Future (416) 638-4771; Marshall (416) 674-2161;
Vancouver: Arrow Canada (604) 291-2986;
Future (604) 294-1166.

Customer Response Center

TOLL FREE: (800) 232-3200

OUTSIDE USA: (214) 995-6611
(8:00 a.m. – 5:00 p.m. CST)

TI Worldwide Sales Offices

ALABAMA: Huntsville: 500 Wynn Drive, Suite 514, Huntsville, AL 35805, (205) 837-7530.

ARIZONA: Phoenix: 8825 N. 23rd Ave., Phoenix, AZ 85021, (602) 995-1007; **TUCSON:** 818 W. Miracle Mile, Suite 43, Tucson, AZ 85705, (602) 292-2640.

CALIFORNIA: Irvine: 17891 Cartwright Dr., Irvine, CA 92714, (714) 660-1200; **Roseville:** 1 Sierra Gate Plaza, Roseville, CA 95678, (916) 786-9208; **San Diego:** 4333 View Ridge Ave., Suite 100, San Diego, CA 92123, (619) 278-9601; **Santa Clara:** 5353 Betsy Ross Dr., Santa Clara, CA 95054, (408) 980-9000; **Torrance:** 690 Knox St., Torrance, CA 90502, (213) 217-7010; **Woodland Hills:** 21220 Erwin St., Woodland Hills, CA 91367, (818) 704-7759.

COLORADO: Aurora: 1400 S. Potomac Ave., Suite 101, Aurora, CO 80012, (303) 368-8000.

CONNECTICUT: Wallingford: 9 Barnes Industrial Park Rd., Barnes Industrial Park, Wallingford, CT 06492, (203) 269-0074.

FLORIDA: Altamonte Springs: 370 S. North Lake Blvd, Altamonte Springs, FL 32701, (305) 260-2116; **Ft. Lauderdale:** 2950 N.W. 62nd St., Ft. Lauderdale, FL 33309, (305) 973-8502; **Tampa:** 4803 George Rd., Suite 390, Tampa, FL 33634, (813) 885-7411.

GEORGIA: Norcross: 5515 Spalding Drive, Norcross, GA 30092, (404) 662-7900

ILLINOIS: Arlington Heights: 515 W. Algonquin, Arlington Heights, IL 60005, (312) 640-2925.

INDIANA: Ft. Wayne: 2020 Inwood Dr., Ft. Wayne, IN 46815, (219) 424-5174; **Carmel:** 550 Congressional Dr., Carmel, IN 46032, (317) 573-6400.

IOWA: Cedar Rapids: 373 Collins Rd. NE, Suite 201, Cedar Rapids, IA 52402, (319) 395-9550.

KANSAS: Overland Park: 7300 College Blvd., Lighton Plaza, Overland Park, KS 66210, (913) 451-4511.

MARYLAND: Columbia: 8815 Centre Park Dr., Columbia MD 21045, (301) 964-2003.

MASSACHUSETTS: Waltham: 950 Winter St., Waltham, MA 02154, (617) 895-9100.

MICHIGAN: Farmington Hills: 33737 W. 12 Mile Rd., Farmington Hills, MI 48018, (313) 553-1569. **Grand Rapids:** 3075 Orchard Vista Dr. S.E., Grand Rapids, MI 49506, (616) 957-4200.

MINNESOTA: Eden Prairie: 11000 W. 78th St., Eden Prairie, MN 55344 (612) 828-9300.

MISSOURI: St. Louis: 11816 Borman Drive, St. Louis, MO 63146, (314) 569-7600.

NEW JERSEY: Iselin: 485E U.S. Route 1 South, Parkway Towers, Iselin, NJ 08830 (201) 750-1050.

NEW MEXICO: Albuquerque: 2820-D Broadbent Pkwy NE, Albuquerque, NM 87107, (505) 345-2555.

NEW YORK: East Syracuse: 6365 Collamer Dr., East Syracuse, NY 13057, (315) 463-9291; **Melville:** 1895 Walt Whitman Rd., P.O. Box 2936, Melville, NY 11747, (516) 454-6600; **Pittsford:** 2851 Clover St., Pittsford, NY 14534, (716) 385-6770; **Poughkeepsie:** 385 South Rd., Poughkeepsie, NY 12601, (914) 473-2900.

NORTH CAROLINA: Charlotte: 8 Woodlawn Green, Woodlawn Rd., Charlotte, NC 28210, (704) 527-0933; **Raleigh:** 2809 Highwoods Blvd., Suite 100, Raleigh, NC 27625, (919) 876-2725.

OHIO: Beachwood: 23775 Commerce Park Rd., Beachwood, OH 44122, (216) 464-6100; **Beavercreek:** 4200 Colonel Glenn Hwy., Beavercreek, OH 45431, (513) 427-6200.

OREGON: Beaverton: 6700 SW 105th St., Suite 110, Beaverton, OR 97005, (503) 643-6758.

PENNSYLVANIA: Blue Bell: 670 Sentry Pkwy, Blue Bell, PA 19422, (215) 825-9500.

PUERTO RICO: Hato Rey: Mercantil Plaza Bldg., Suite 505, Hato Rey, PR 00918, (809) 753-8700.

TENNESSEE: Johnson City: Erwin Hwy, P.O. Drawer 1255, Johnson City, TN 37605 (615) 461-2192.

TEXAS: Austin: 12501 Research Blvd., Austin, TX 78759, (512) 250-7655; **Richardson:** 1001 E. Campbell Rd., Richardson, TX 75081, (214) 680-5082; **Houston:** 9100 Southwest Frwy., Suite 250, Houston, TX 77074, (713) 778-6592; **San Antonio:** 1000 Central Parkway South, San Antonio, TX 78232, (512) 496-1779.

UTAH: Murray: 5201 South Green St., Suite 200, Murray, UT 84123, (801) 266-8972.

WASHINGTON: Redmond: 5010 148th NE, Bldg B, Suite 107, Redmond, WA 98052, (206) 881-3080.

WISCONSIN: Brookfield: 450 N. Sunny Slope, Suite 150, Brookfield, WI 53005, (414) 782-2899.

CANADA: Nepean: 301 Moodie Drive, Mallorn Center, Nepean, Ontario, Canada, K2H9C4, (613) 726-1970. **Richmond Hill:** 280 Centre St. E., Richmond Hill L4C1B1, Ontario, Canada (416) 884-9181; **St. Laurent:** Ville St. Laurent Quebec, 9480 Trans Canada Hwy., St. Laurent, Quebec, Canada H4S1R7, (514) 336-1860.

ARGENTINA: Texas Instruments Argentina Viamonte 1119, 1053 Capital Federal, Buenos Aires, Argentina, 541/748-3699

AUSTRALIA (& NEW ZEALAND): Texas Instruments Australia Ltd.: 6-10 Talavera Rd., North Ryde (Sydney), New South Wales, Australia 2113, 2 + 887-1122; 5th Floor, 418 St. Kilda Road, Melbourne, Victoria, Australia 3004, 3 + 267-4677; 171 Philip Highway, Elizabeth, South Australia 5112, 8 + 255-2066.

AUSTRIA: Texas Instruments Ges.m.b.H.: Industriestrabe B/16, A-2345 Brunn/Gebirge, 2236-846210.

BELGIUM: Texas Instruments N.V. Belgium S.A.: 11, Avenue Jules Bondetlaan 11, 1140 Brusseis, Belgium, (02) 242-3080.

BRAZIL: Texas Instruments Electronicos do Brasil Ltda.: Rua Paes Leme, 524-7 Andar Pinheiros, 05424 Sao Paulo, Brazil, 0815-6166.

DENMARK: Texas Instruments A/S, Mairelundvej 46E, 2730 Herlev, Denmark, 2 - 91 74 00.

FINLAND: Texas Instruments Finland OY: Ahertajantie 3, P.O. Box 81, ESP00, Finland, (90) 0-461-422.

FRANCE: Texas Instruments France: Paris Office, BP 67 8-10 Avenue Morane-Saulnier, 78141 Velizy-Villacoublay cedex (1) 30 70 1003.

GERMANY (Fed. Republic of Germany): Texas Instruments Deutschland GmbH: Haggertystrasse 1, 8050 Freising, 8161 + 80-4591; Kurfuerstendamm 195/196, 1000 Berlin 15, 30 + 882-7365; III, Hagen 43/Kibbelstrasse, .19, 4300 Essen, 201-24250; Kirchhorsterstrasse 2, 3000 Hannover 51, 511 + 648021; Maybachstrabe 11, 7302 Ostfildern 2-Nelingen, 711 + 34030.

TEXAS INSTRUMENTS

HONG KONG: Texas Instruments Hong Kong Ltd., 8th Floor, World Shipping Ctr., 7 Canton Rd., Kowloon, Hong Kong, (852) 3-7351223.

IRELAND: Texas Instruments (Ireland) Limited: 7/8 Harcourt Street, Stillorgan, County Dublin, Eire, 1 781677.

ITALY: Texas Instruments Italia S.p.A. Divisione Semiconduttori: Viale Europa, 40, 20093 Cologne Monzese (Milano), (02) 253001; Via Castello della Magliana, 38, 00148 Roma, (06) 5222651; Via Amendola, 17, 40100 Bologna, (051) 554004.

JAPAN: Tokyo Marketing/Sales (Headquarters): Texas Instruments Japan Ltd., MS Shibaura Bldg., 9F, 4-13-23 Shibaura, Minato-ku, Tokyo 108, Japan, 03-769-8700. Texas Instruments Japan Ltd.: Nisshoiwai Bldg. 5F, 30 Imabashi 3-chome, Higashi-ku, Osaka 541, Japan, 06-294-1881; Daini Toyota West Bldg. 7F, 10-27 Meieki 4-chome, Nakamura-ku, Nagoya 450, 052-583-8691; Daiichi Seimei Bldg. 6F, 3-10 Oyama-cho, Kanazawa 920, Ishikawa-ken, 0762-23-5471; Daiichi Olympic Tachikawa Bldg. 6F, 1-25-12 Akebono-cho, Tachikawa 190, Tokyo, 0425-27-6426; Matsumoto Showa Bldg. 6F, 2-11 Fukashi 1-chome, Matsumoto 390, Nagano-ken, 0263-33-1060; Yokohama Nishiguchi KN Bldg. 6F, 2-8-4 Kita-Saiwai-cho, Nishi-ku, Yokohama 220, 045-322-6741; Nihon Seimei Kyoto Yasaka Bldg. 5F, 843-2 Higashi Shiokohjidori, Nishinotoh-in Higashi-iru, Shiokouji, Shimogyo-ku, Kyoto 600, 075-341-7713; 2597-1, Aza Harudai, Oaza Yasaka, Kitsuki 873, Oitaken, 09786-3-3211; Miho Plant, 2350 Kihara Mihomura, Inashiki-gun 300-04, Ibaragi-ken, 0298-85-2541.

KOREA: Texas Instruments Korea Ltd., 28th Fl., Trade Tower, #159, Samsung-Dong, Kangnam-ku, Seoul, Korea 2 + 551-2810.

MEXICO: Texas Instruments de Mexico S.A.: Alfonso Reyes—115, Col. Hipodromo Condesa, Mexico, D.F., Mexico 06120, 525/525-3860.

MIDDLE EAST: Texas Instruments: No. 13, 1st Floor Mannai Bldg., Diplomatic Area, P.O. Box 26335, Manama Bahrain, Arabian Gulf, 973 + 274681.

NETHERLANDS: Texas Instruments Holland B.V., 19 Hogehilweg, 1100 AZ Amsterdam—Zuidoost, Holland 20 + 5602911.

NORWAY: Texas Instruments Norway A/S: PB106, Refstad 0585, Oslo 5, Norway, (2) 155090.

PEOPLES REPUBLIC OF CHINA: Texas Instruments China Inc., Beijing Representative Office, 7-05 Citic Bldg., 19 Jianguomenwai Daije, Beijing, China, (861) 5002255, Ext. 3750.

PHILIPPINES: Texas Instruments Asia Ltd.: 14th Floor, Ba- Lepanto Bldg., Paseo de Roxas, Makati, Metro Manila, Philippines, 817-60-31.

PORTUGAL: Texas Instruments Equipamento Electronico (Portugal), Lda.: Rua Eng. Frederico Ulrich, 2650 Moreira Da Maia, 4470 Maia, Portugal, 2-948-1003.

SINGAPORE (+ INDIA, INDONESIA, MALAYSIA, THAILAND): Texas Instruments Singapore (PTE) Ltd., Asia Pacific Division, 101 Thompson Rd. #23-01, United Square, Singapore 1130, 350-8100.

SPAIN: Texas Instruments Espana, S.A.: C/Jose Lazaro Galdiano No. 6, Madrid 28036, 1/458.14.58.

SWEDEN: Texas Instruments International Trade Corporation (Sverigefilialen): S-164-93, Stockholm, Sweden, 8 - 752-5800.

SWITZERLAND: Texas Instruments, Inc., Reidstrasse 6, CH-8953 Dietikon (Zuerich) Switzerland, 1-740 2220.

TAIWAN: Texas Instruments Supply Co., 9th Floor Bank Tower, 205 Tun Hwa N. Rd., Taipei, Taiwan, Republic of China, 2 + 713-9311.

UNITED KINGDOM: Texas Instruments Limited: Manton Lane, Bedford, MK41 7PA, England, 0234 270111.

TEXAS INSTRUMENTS

Printed in U.S.A.
689—5

SRSS034