TEXAS INSTRUMENTS

Advanced Logic and Bus Interface Logic

Data Book

Data Book

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1991

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INTRODUCTION

The new advanced logic and bus interface logic solutions from Texas Instruments can help you design today's high-performance, low-power bus interface while addressing important design issues such as enhancing speed and conserving board space.

Solutions include:

- ACL LSI for high-speed, low-power logic requirements
- ACL Widebus™ Series doubles I/O count in the same board area
- BiCMOS and submicron BiCMOS bus-interface logic families offering drivers, transceivers, latches, registers, and registered and latched transceivers
- Bus-termination arrays for an effective termination solution
- Clock drivers minimize skew
- ECL translators for fast, low-power ECL/TTL translations
- FIFOs help accelerate overall system performance
- Futurebus+ transceivers with logic voltage levels selected to optimize bus performance
- Low-impedance line drivers with speed and power characteristics similar to those of BCT octals and drive capability of 188 mA
- SCOPE™ products providing on-chip testability
- 64 Series BiCMOS designed for the telecommunications-or industrial-equipment market to withstand extended temperature ranges and hot-card insertion

This book provides pertinent technical information on available and planned advanced logic and bus interface logic devices. Additionally, the General Information Section contains an alphanumerical index, functional index, and other useful information.

For more information on Texas Instruments advanced logic and bus interface logic products, please contact your local TI field sales office or authorized distributor, or call Texas Instruments at 1-800-232-3200.

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_I **Input capacitance**
The internal capacitance at an input of the device.

C_O **Output capacitance**
The internal capacitance at an output of the device.

C_{pd} **Power dissipation capacitance**
Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.

ΔI_{CC} **Supply current change (ACT devices only)**
The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OZ} **Off-state (high-impedance-state) output current (of a three-state output)**
The current flowing into* an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output.

*Current out of a terminal is given as a negative value.

t_a **Access time**
The time interval between the application of a specified input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a three-state or open-collector output)**
The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs will change only if they are low at the time of disabling so $t_{dis} = t_{PLH}$.

t_{en} **Enable time (of a three-state or open-collector output)**
The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{G}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL}. Open-collector outputs will change only if they are responding to data that would cause the output to go low so, for them, $t_{en} = t_{PHL}$.

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ($t_{pd} = t_{PHL}$ or t_{PLH}).

t_{PHL} **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

V_{T+} **Positive-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} **Negative-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

The following symbols are used in function tables on TI data sheets:

H = high level (steady state)

L = low level (steady state)

↑ = transition from low to high level

↓ = transition from high to low level

→ = value/level or resulting value/level is routed to indicated destination

↶ = value/level is re-entered

X = irrelevant (any input, including transitions)

Z = off (high-impedance) state of a 3-state-output

a..h = the level of steady-state inputs at inputs A through H respectively

Q_0 = level of Q before the indicated steady-state input conditions were established

$\overline{Q}_0$ = complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established

Q_n = level of Q before the most recent active transition indicated by ↓ or ↑

⎍ = one high-level pulse

⎏ = one low-level pulse

TOGGLE = each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎏, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is not at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

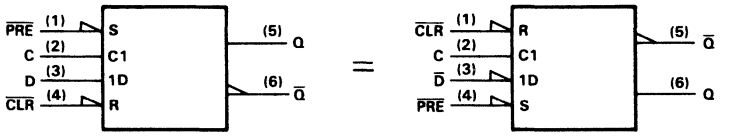
The function table functional tests do not reflect all possible combinations or sequential modes.

D flip-flop and latch signal conventions

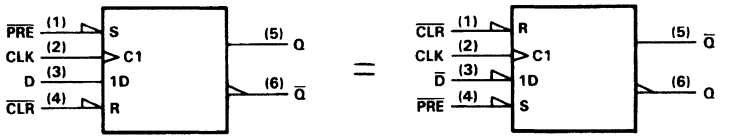
It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active-low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown in parentheses.



LATCH LATCH



FLIP-FLOP FLIP-FLOP

The figures show that when Q and $\overline{Q}$ exchange names, the Preset and Clear pins also exchange names. The polarity indicators (◺) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active-low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

In digital system design, consideration must be given to thermal management of components. The small size of the "small outline" package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the EPIC™ ACL family. In general, the junction temperature for any device can be calculated using Equation 1.

$$T_J = R_{\theta JA} \times P_T + T_A \qquad (1)$$

where

T_J = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to free air
P_T = total power dissipation of the device
T_A = free-air temperature

The total power consumption can be determined from Equation 2 for an AC device and Equation 3 for an ACT device.

JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
AIR VELOCITY

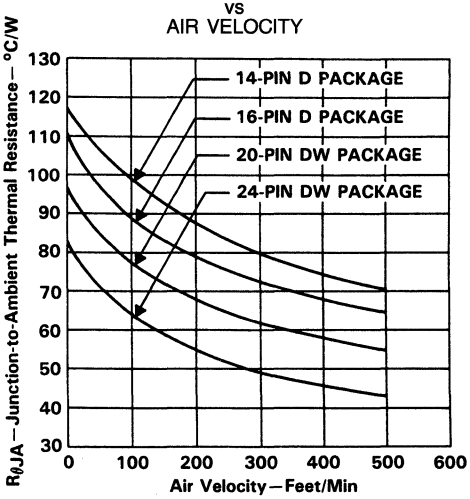


FIGURE 1

$$P_T = V_{CC} \times I_{CC} + (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o) \qquad (2)$$

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o) \qquad (3)$$

where

V_{CC} = supply voltage (5 V for typical, 5.5 V for maximum) see Note 1
I_{CC} = quiescent supply current (specified on device data sheet)
C_{pd} = Power dissipation capacitance (from the device data sheet)
f_i = input frequency
C_L = output load capacitance
f_o = output frequency
N = number of inputs driven by a TTL device
dc = duty cycle
ΔI_{CC} = increase in supply current (specified on device data sheet)

NOTE 1: In system applications I_{CC} can be minimized by keeping input voltage levels less than 1 V for V_{IL} and greater than $V_{CC} - 1$ V for V_{IH} and input rise and fall times less than 15 ns.

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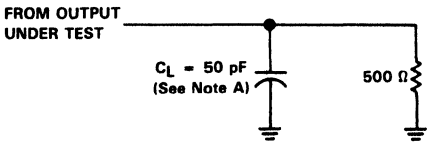
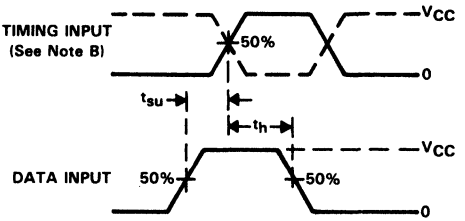
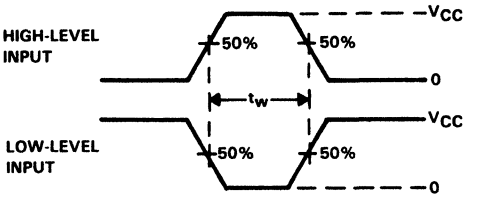
SERIES 54AC11XXX AND 74AC11XXX DEVICES
SERIES 54AC16XXX AND 74AC16XXX DEVICES



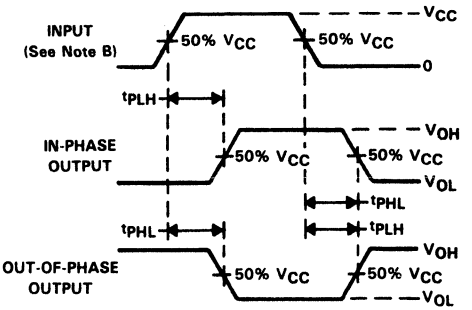
LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS



SETUP AND HOLD TIMES



PULSE DURATION

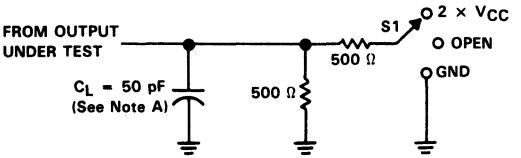


PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns. Pulse polarity can be either a high-to-low-to-high or low-to-high-to-low.
C. The outputs are measured one at a time with one input transition per measurement.

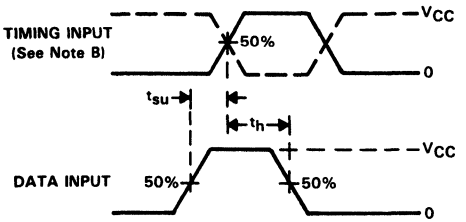
SERIES 54AC11XXX AND 74AC11XXX DEVICES

SERIES 54AC11XXX AND 74AC11XXX DEVICES

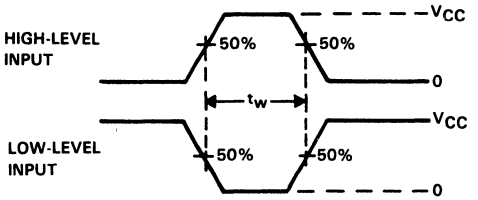


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND

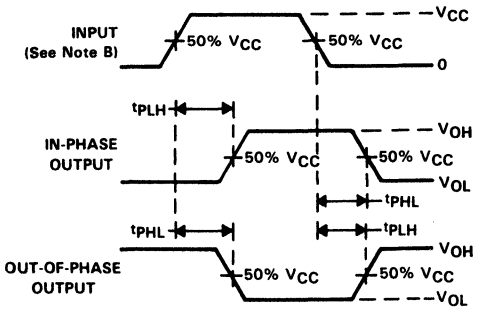
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



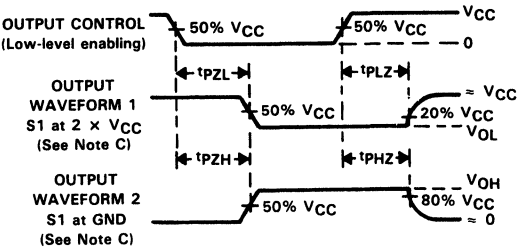
SETUP AND HOLD TIMES



PULSE DURATION



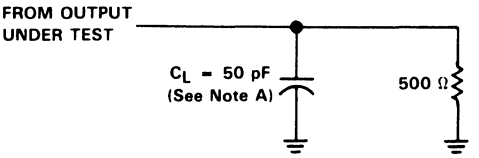
PROPAGATION DELAY TIMES



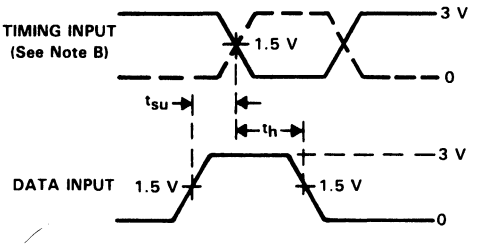
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns. Pulse polarity can be either a high-to-low-to-high or low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

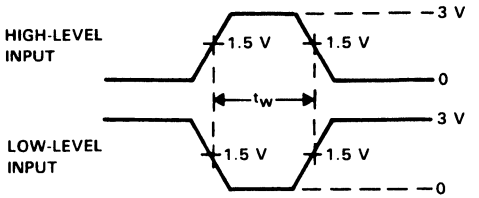
SERIES 54ACT11XXX AND 74ACT11XXX DEVICES
SERIES 54ACT16XXX AND 74ACT16XXX DEVICES



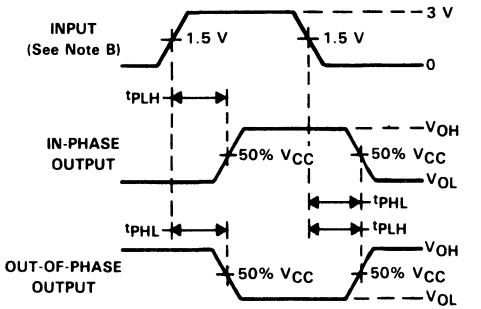
LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS



SETUP AND HOLD TIMES



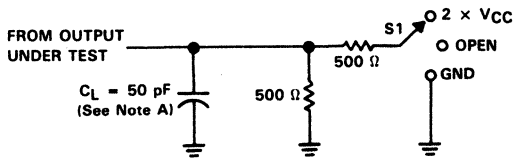
PULSE DURATION



PROPAGATION DELAY TIMES

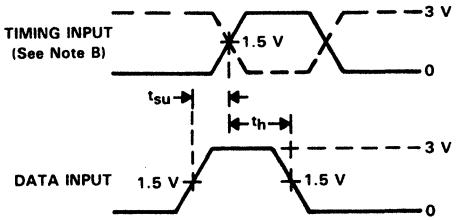
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns. Pulse polarity can be either a high-to-low-to-high or low-to-high-to-low.
C. The outputs are measured one at a time with one input transition per measurement.

SERIES 54ACT11XXX AND 74ACT11XXX DEVICES
SERIES 54ACT16XXX AND 74ACT16XXX DEVICES

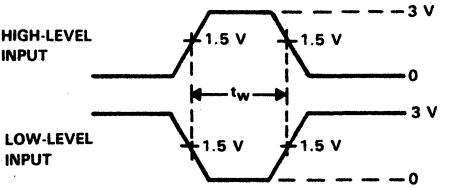


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

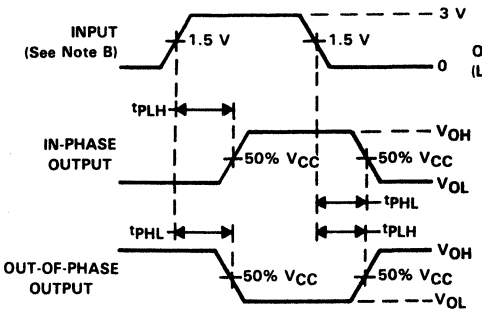
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



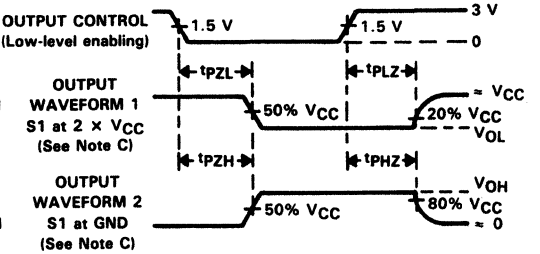
SETUP AND HOLD TIMES



PULSE DURATION



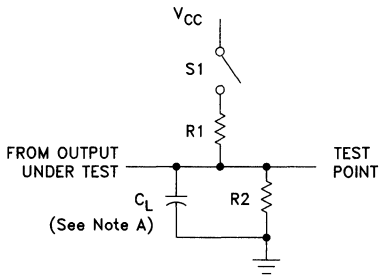
PROPAGATION DELAY TIMES



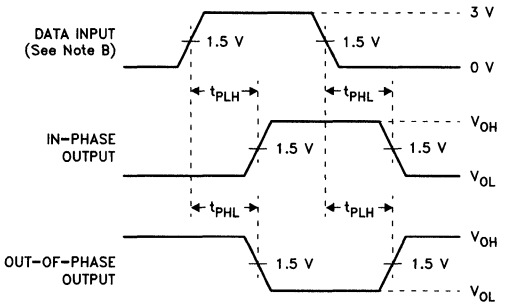
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns. Pulse polarity may be either a high-to-low-to-high or low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

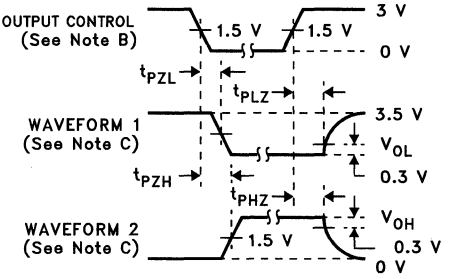
SERIES SN54BCT25XXX AND SN74BCT25XXX DEVICES



LOAD CIRCUIT



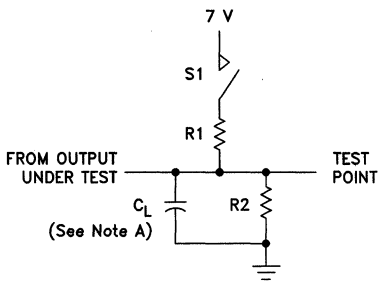
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



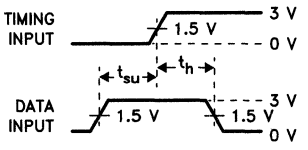
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 1 to 3 ns. For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns. Pulse polarity can be either a high-to-low-to-high or low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

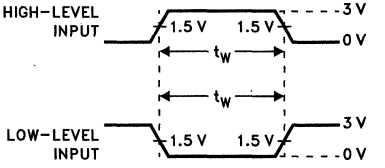
SERIES SN54BCT8XXX AND SN74BCT8XXX DEVICES



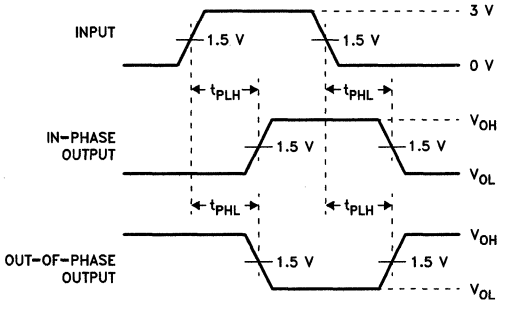
LOAD CIRCUIT 1 ALL OUTPUTS EXCEPT FOR ERROR FLAG



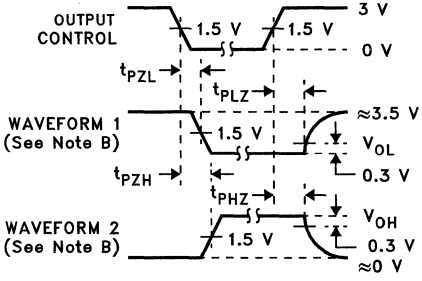
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



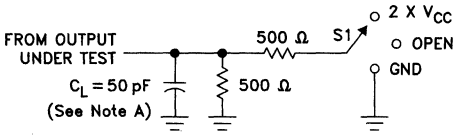
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

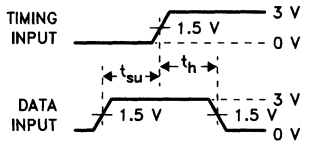
SERIES SN54ACT8XXX AND SN74ACT8XXX DEVICES

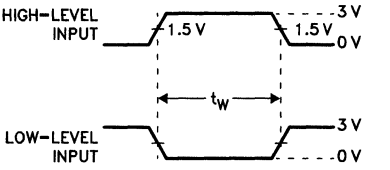


LOAD CIRCUIT

SWITCH POSITION TABLE

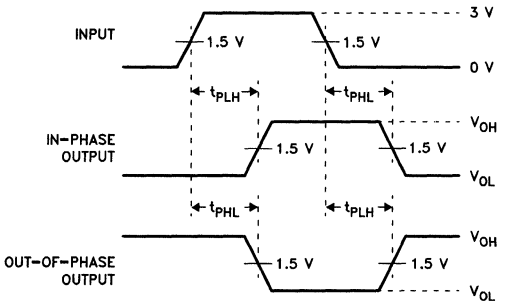
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND



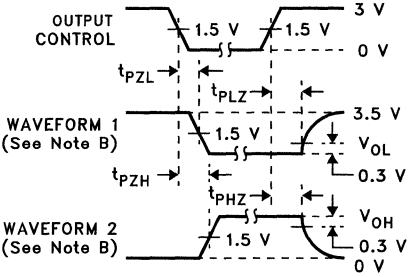


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS



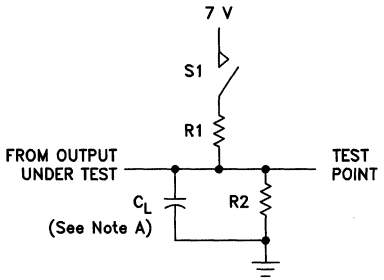
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



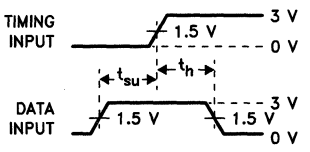
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

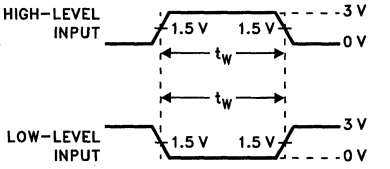
SERIES SN64BCT8XXX DEVICES



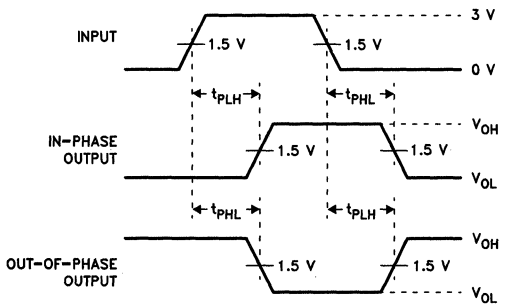
LOAD CIRCUIT 1 ALL OUTPUTS EXCEPT FOR ERROR FLAG



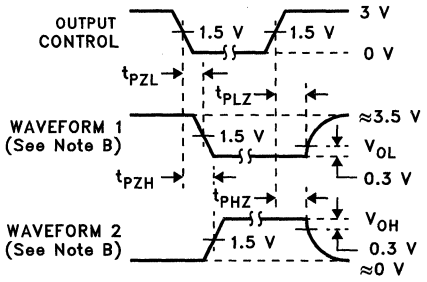
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

SERIES SN54FXXX AND SN74FXXX DEVICES

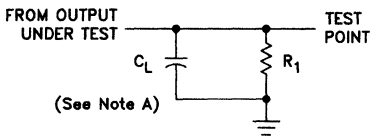


FIGURE 1. LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

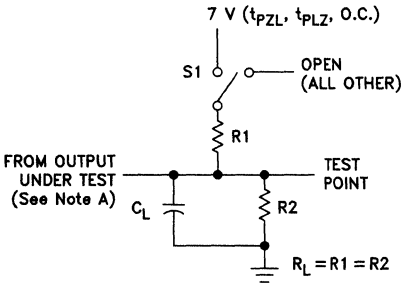
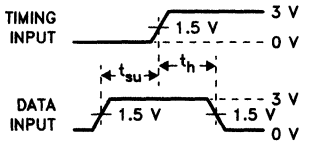
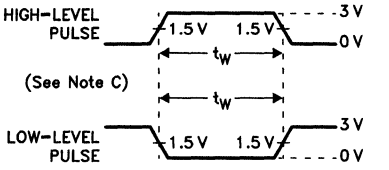


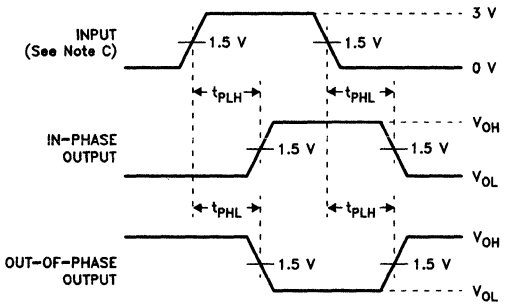
FIGURE 2. LOAD CIRCUIT FOR THREE STATE AND OPEN-COLLECTOR OUTPUTS



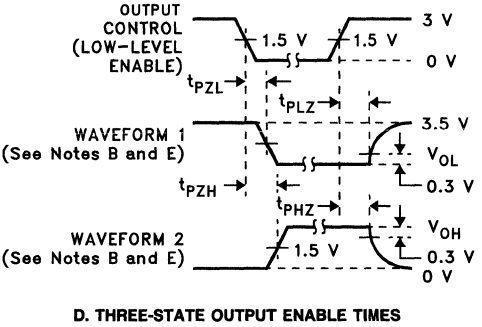
A. SETUP AND HOLD TIMES



B. PULSE WIDTHS



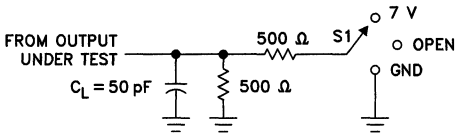
C. PROPAGATION DELAY TIMES



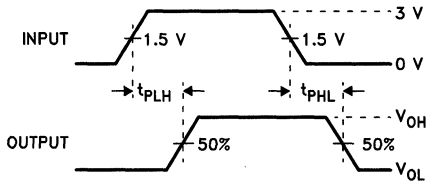
D. THREE-STATE OUTPUT ENABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics; PRR = 1 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
D. When measuring propagation delay times of three-state outputs, switch S1 is open.
E. The outputs are measured one at a time with one input transition per measurement.

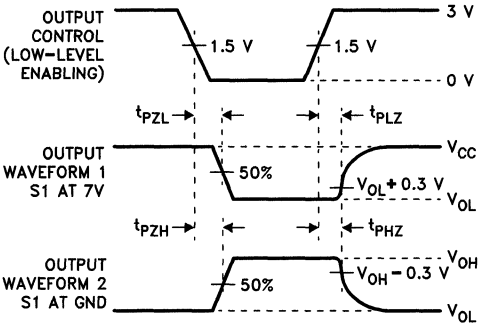
SERIES SN54BCTXXX AND SN74BCTXXX DEVICES



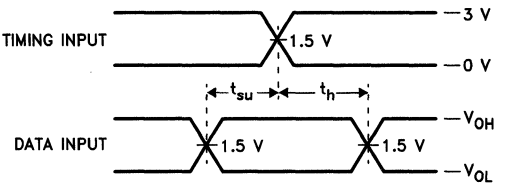
LOAD CIRCUIT FOR OUTPUTS



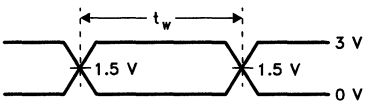
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



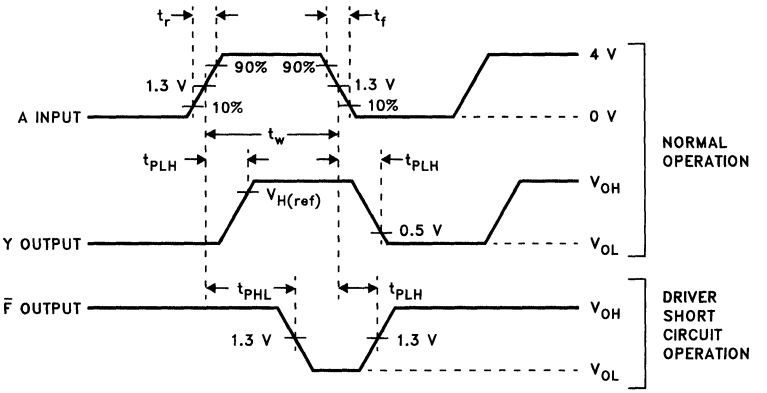
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



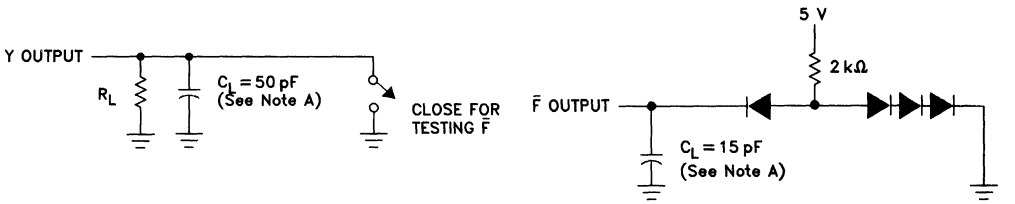
VOLTAGE WAVEFORMS
PULSE DURATION

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 2.5 ns, t_f = 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

SERIES SN55ALSXXX AND SN75ALSXXX DEVICES

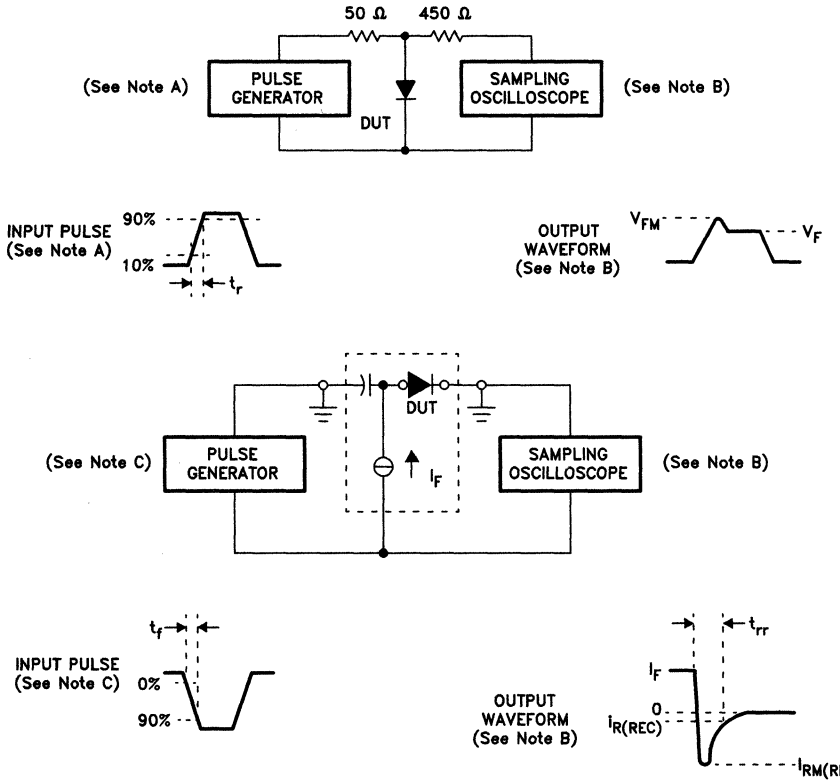


NOTE: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_{out} = 50\ \Omega$.



NOTE: A. C_L includes probe and stray capacitance.

SERIES SN54S10XX AND SN74S10XX DEVICES

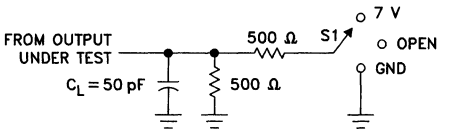


NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: t_r = 20 ns, Z_{out} = 50 Ω, f_{PR} = 500 Hz, duty cycle = 0.01.

B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \leq$ 350 ps, R_{in} = 50 Ω, $C_{in} = \leq$5 pF.

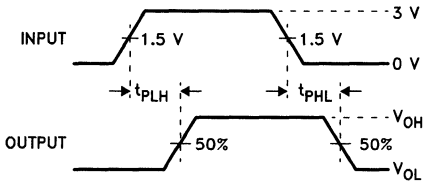
C. The input pulse is supplied by a pulse generator having the following characteristics: t_f = 0.5 ns, Z_{out} = 50 Ω, $t_w = \leq$ 50 ns, duty cylce ≤0.01.

SERIES SN54ABTXXX AND SN74ABTXXX DEVICES

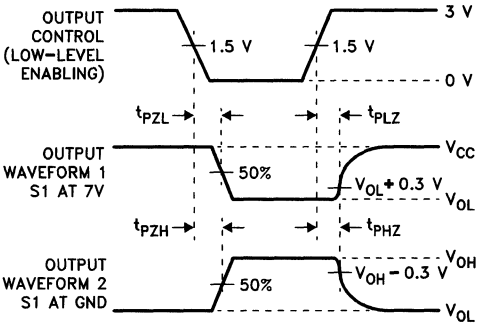


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

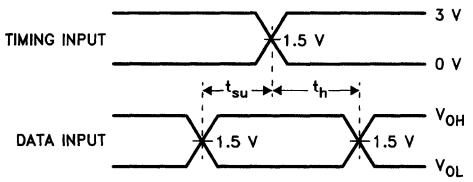
LOAD CIRCUIT FOR OUTPUTS



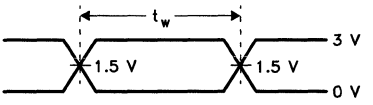
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES



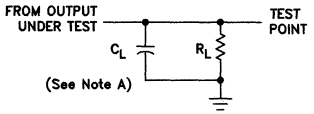
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



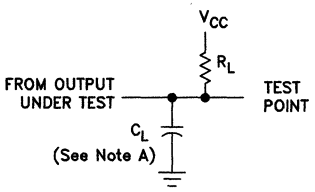
VOLTAGE WAVEFORMS PULSE DURATION

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 2.5 ns, t_f = 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

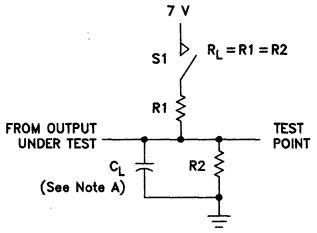
SERIES SN54ASXXX AND SN74ASXXX DEVICES



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

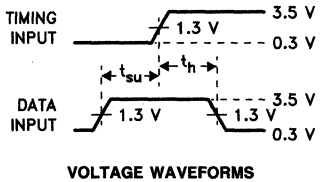


LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

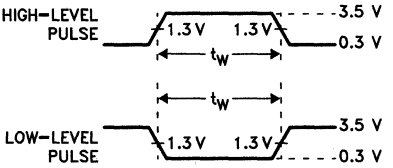


LOAD CIRCUIT FOR THREE-STATE OUTPUTS

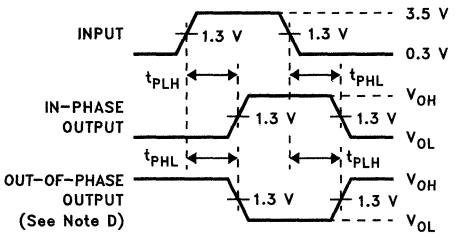
NOTE: A. C_L includes probe and jig capacitance.



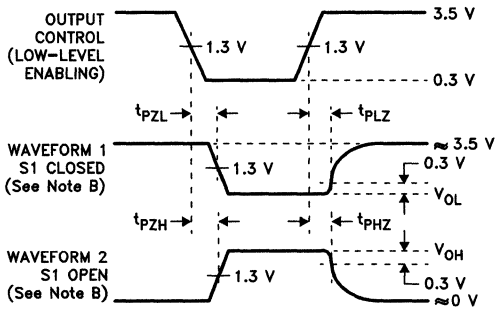
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



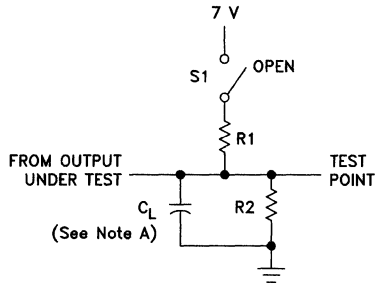
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay items of 3-state outputs, switch S1 is open.
E. The outputs are measured one at a time with one input transition per measurement.

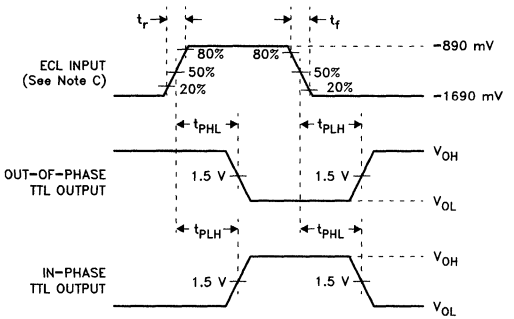
SERIES SN10KHT ECL-TO-TTL TRANSLATOR



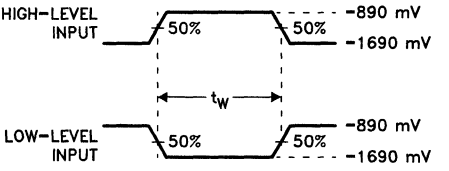
LOAD CIRCUIT

SWITCH POSITION TABLE

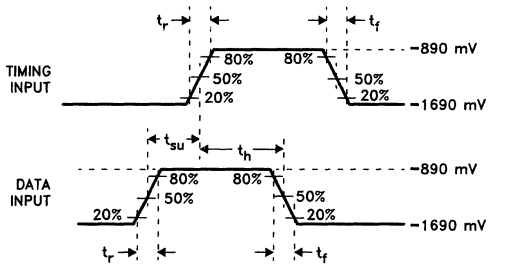
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



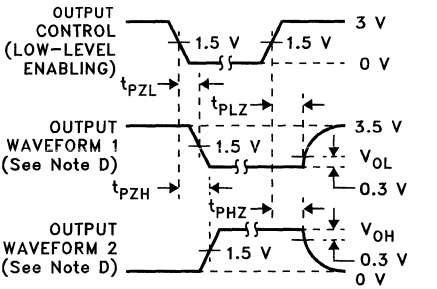
VOLTAGE WAVEFORMS
ECL-INPUT PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



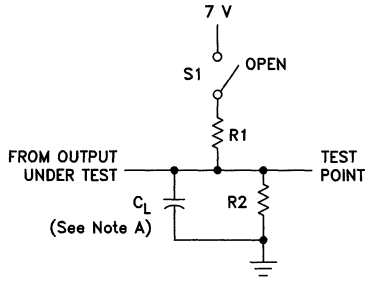
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
TTL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 1.5 ns, t_f ≤ 1.5 ns.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. The outputs are measured one at a time with one transition per measurement.

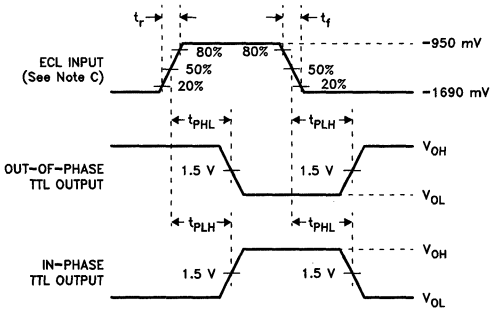
SERIES SN100KT ECL-TO-TTL TRANSLATOR



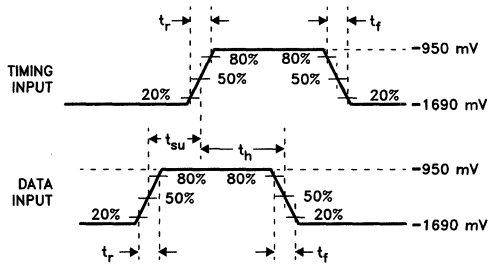
LOAD CIRCUIT

SWITCH POSITION TABLE

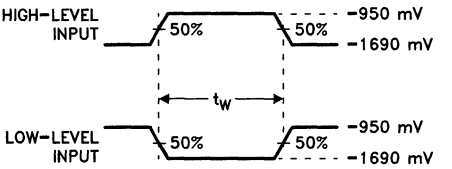
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



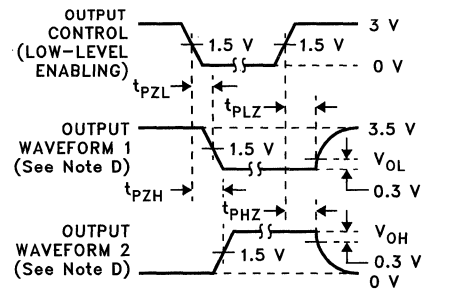
VOLTAGE WAVEFORMS
ECL-INPUT PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



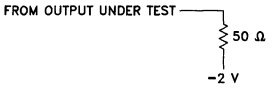
VOLTAGE WAVEFORMS
PULSE DURATION



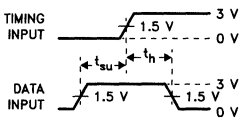
VOLTAGE WAVEFORMS
TTL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 0.7 ns, t_f ≤ 0.7 ns.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. The outputs are measured one at a time with one transition per measurement.

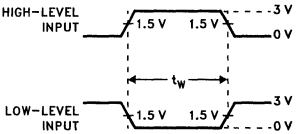
SERIES SN100KT TTL-TO-ECL TRANSLATOR



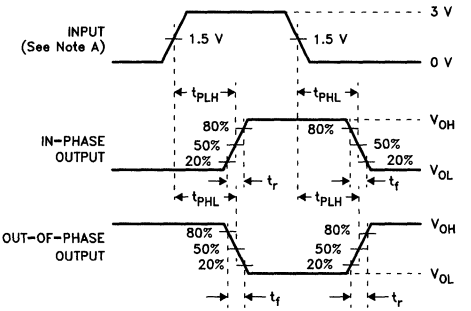
OUTPUT LOAD CIRCUIT



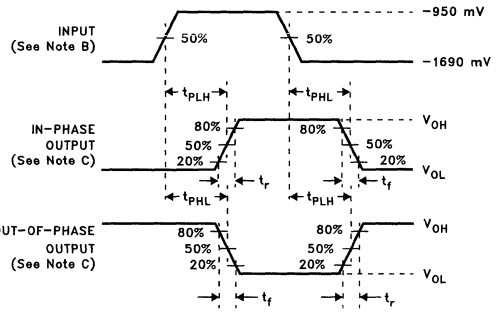
SETUP AND HOLD TIMES



PULSE DURATION



TTL-INPUT PROPAGATION DELAY TIMES



ECL-INPUT PROPAGATION DELAY TIMES

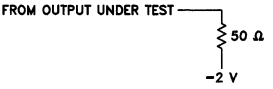
NOTES: A. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

B. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 0.7 ns, t_f ≤ 0.7 ns.

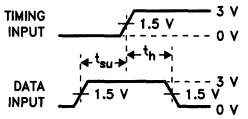
C. Waveform 1 is for an output with internal conditions such that the output is high except when disabled by $\overline{OE}$.

D. The outputs are measured one at a time with one input transition per measurement.

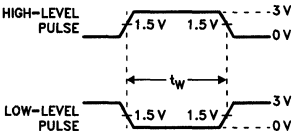
SERIES SN10KHT OCTAL TTL-TO-ECL TRANSLATOR



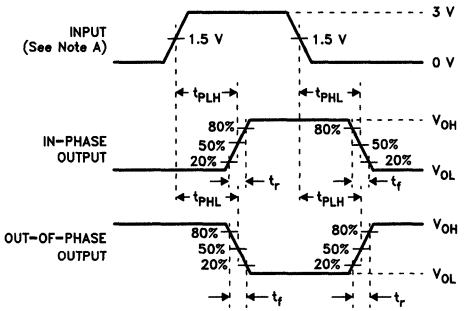
OUTPUT LOAD CIRCUIT



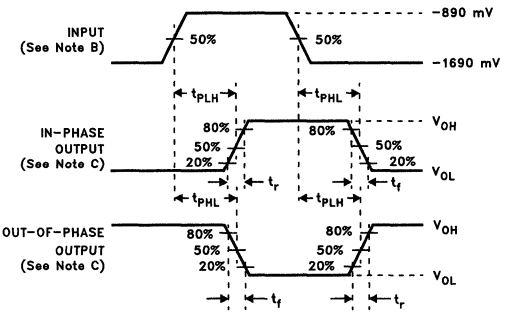
SETUP AND HOLD TIMES



PULSE DURATION



TTL-INPUT PROPAGATION DELAY TIMES



ECL-INPUT PROPAGATION DELAY TIMES

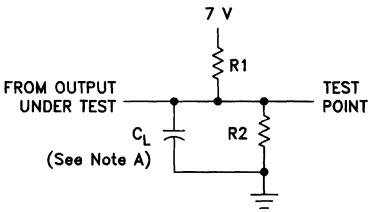
NOTES: A. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

B. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 1.5 ns, t_f ≤ 1.5 ns.

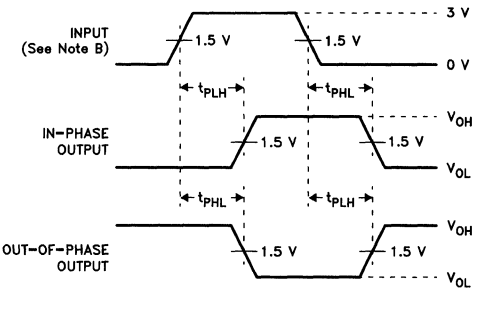
C. Waveform 1 is for an output with internal conditions such that the output is high except when disabled by $\overline{OE}$.

D. The outputs are measured one at a time with one input transition per measurement.

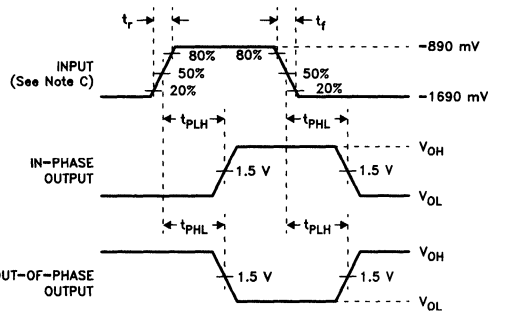
SERIES SN10KHT ECL-TO-TTL TRANSLATORS WITH OPEN-COLLECTOR OUTPUTS



LOAD CIRCUIT



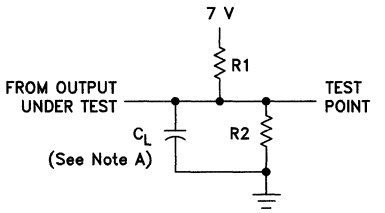
TTL-INPUT PROPAGATION DELAY TIMES



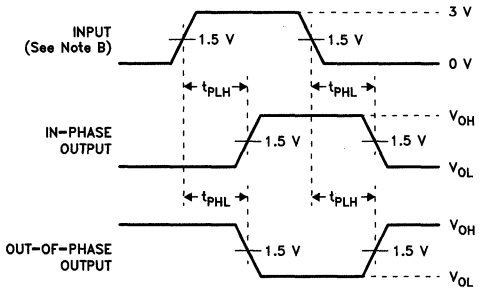
ECL-INPUT PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 1.5 ns, t_f ≤ 1.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

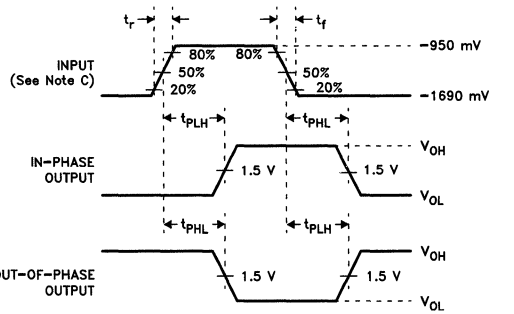
SERIES SN10KT ECL-TO-TTL TRANSLATORS WITH OPEN-COLLECTOR OUTPUTS



LOAD CIRCUIT



VOLTAGE WAVEFORMS
TTL-INPUT PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ECL-INPUT PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 0.7 ns, t_f ≤ 0.7 ns.
D. The outputs are measured one at a time with one transition per measurement.

The following tables outline the logic functions Texas Instruments offers in a variety of technologies. The tables are organized by function type, and list all options available or planned of that function. The technology columns identify the appropriate family and identify a particular data book, where more information can be found. The applicable literature number, composed of either seven or eight digits, can be found on the back cover at the lower right-hand corner of each publication.

List of Applicable Data Books:

AC and ACT Devices	Advanced CMOS Logic Data Book	SCAD001B
Advanced Logic Devices	Advanced Logic and Bus Interface Logic Data Book	SCYD001
AS and ALS Devices	ALS/AS Logic Data Book	SDAD001B
BCT Devices	BiCMOS Bus Interface Logic Data Book	SCBD001A
F Devices	F Logic (54/75F) Data Book	SDFD001A
HC and HCT Devices	High-Speed CMOS Logic Data Book	SCLD001C
Std TTL, LS, and S Devices	Standard TTL Logic Data Book	SDLD001A

Contents

Contents (continued)

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

GATES

Positive-NAND Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
8-Input		'30	●	●	●	●					
		'11030						●	●		
13-Input		'133	●			●					
Dual 2-Input		'8003	●								
Dual 4-Input		'11013					●		▲		
		'20	●	●	●	●					
		'40	●		●						
		'1020	●								
		'11020						●	●		
Triple 3-Input		'10	●	●	●	●					
		'1010	●								
		'11010						●	●		
Quad 2-Input		'00	●	●	●	●	●				
		'11000						●	●		
		'37	●		●						
	OC	'38	●		●						
		'132				●					
		'11132						▲	▲		
		'1000	●	●							
Hex 2-Input		'804	●	●							
		'1804	●	●							
Dual 4-Input	OC	'22	●								
Triple 3-Input	OC	'12	●								
Quad 2-Input	OC	'01	●			●					
	OC	'03	●			●					
	OC	'1003	●								

NOTES:
● Product available in technology indicated
▲ New Product planned in technology indicated

GATES (continued)

Positive-AND Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Triple 3-Input	OC	'15	•								
Quad 2-Input	OC	'09	•		•	•					
		'7001				•					
Dual 4-Input		'21	•	•	•	•					
		'11021						•	•		
Triple 3-Input		'11	•	•	•	•					
		'11011						•	•		
Quad 2-Input		'08	•	•	•	•	•				
		'1008	•	•							
		'11008						•	•		
Hex 2-Input		'808	•	•		•					
		'1808	•	•							

Positive-OR/NOR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Triple 3-Input		'4075				•					
Quad 2-Input		'32	•	•	•	•	•				
		'1032	•	•							
		'11032						•	•		
Quad 2-Input		'7032				•					
Hex 2-Input		'832	•	•		•					
		'1832	•	•							
Dual 4-Input		'4002				•					
Dual 5-Input		'260			•						
Triple 3-Input		'27	•	•	•	•					
		'11027						•	•		
Quad 2-Input		'02	•	•	•	•	•				
		'28	•								
	OC	'33	•								
		'36			•	•					
		'1002	•								
		'1036		•							
		'7002				•					
		'11002						•	•		
Hex 2-Input		'805	•	•		•					
		'1805	•	•							

NOTES:
• Product available in technology indicated
▲ New Product planned in technology indicated

GATES (continued)

OR/NOR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
8-Input		'4078				•					
Quad 2-Input		'86	•	•	•	•					
Exclusive OR Gates with		'11086						•	•		
Toten-Pole Outputs		'386				•					
Quad 2-Input Exclusive OR Gates	OC	'136	•	•							
Quad 2-Input		'810	•	•							
Exclusive-NOR Gates		'7266				•					
Quad 2-Input Exclusive-NOR Gates	OC	'811	•	•							

AND-NOR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Wide 4-2-3-2		'64			•						
Input		'11064						▲	▲		
Dual 2-Wide		'51			•	•					
2-Input, 3-Input		'11051						▲	▲		

INVERTING/NONINVERTING BUFFERS

Hex Inverters/Noninverters

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY									
			ALS	AS	F	HC	HCT	HCU	AC	ACT	BCT	ABT
Hex Inverters		'04	•	•	•	•	•	•				
		'11004							•	•		
	OC	'05	•			•						
		'14				•						
		'11014							▲	▲		
		'1004	•	•								
		'1005	•									
Hex Noninverters		'34	•	•								
		'11034							•	•		
	OC	'35	•									
		'1034	•	•								
	OC	'1035	•									

NOTES:
- • Product available in technology indicated
- ▲ New Product planned in technology indicated

BUFFER/DRIVERS AND BUS TRANSCEIVERS

Drivers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Quad Buffers/	3S	'125			●	●				●	
Drivers	3S	'126			●	●				●	
Noninverting Hex	3S	'365				●					
Buffers/Drivers	3S	'367				●					
Inverting Hex	3S	'366				●					
Buffers/Drivers	3S	'368				●					
Noninverting	3S	'241	●	●	●	●	●			●	▲
Octal		'11241						●	●		
Buffers/Drivers		'25241								▲	
		'244	●	●	●	●	●			●	▲
		'11244						●	●		
		'1244	●								
		'25244								▲	
		'465	●								
		'541	●		●	●	●			●	▲
	OC	'757	●	●						●	
		'760	●	●						●	
		'25760								▲	
Inverting Octal	3S	'240	●	●	●	●	●			●	▲
Buffers/Drivers		'11240						●	●		
		'1240	●								
		'25240								▲	
		'466	●								
		'540	●		●	●	●			●	▲
	OC	'756	●	●						▲	
		'763	●	●							
Inverting and	3S	'230		●							
Noninverting Octal	OC	'762		●							
Buffers/Drivers											
Noninverting 10-Bit	3S	'11827						●	●		
Buffers/Drivers		'29827	●							●	▲
Inverting 10-Bit	3S	'11828						●	●		
Buffers/Drivers		'29828	●							●	
Noninverting 16-bit Buffers/Drivers	3S	'16244						▲	●		
Inverting 16-bit Buffers/Drivers	3S	'16240						▲	●		
Noninverting 18-bit Buffers/Drivers	3S	'16825						▲	▲		
Inverting 18-bit Buffers/Drivers	3S	'16826						▲	▲		
Noninverting 20-bit Buffers/Drivers	3S	'16827						▲	▲		
Inverting 20-bit Buffers/Drivers	3S	'16828						▲	▲		

NOTES:
- ● Product available in technology indicated
- ▲ New Product planned in technology indicated

BUFFER/DRIVERS AND BUS TRANSCEIVERS (continued)

Drivers (continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Octal Buffers/ Drivers with Input Pull-up Resistors		'746	●								
		'747	●								

Bus Transceivers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Noninverting Quad Transceivers	OC	'759		●							
	3S	'243	●	●	●		●				
Inverting Quad Transceivers	OC	'758	●								
	3S	'242	●	●	●		●				
Noninverting Octal Transceivers	3S	'245	●	●	●	●	●			●	▲
		'1245	●								
		'11245						●	●		
		'25245								●	
	OC	'621	●		●						
	3S	'623	●	●	●	●	●			●	▲
		'11623						●	●		
	OC/3S	'639	●	●							
	OC	'641	●	●							
	3S	'645	●	●		●	●				
	3S	'1640	●								
		'1645	●								
Inverting Octal Transceivers	3S	'620	●	●	●					●	▲
		'11620						●	●		
		'25620								▲	
	OC	'622	●		●						
	OC/3S	'638	●	●							
	3S	'640	●	●		●	●			●	▲
		'11640						●	●		
		'25640								▲	
	OC	'642	●	●						▲	
		'25642								●	
True and Inverting Octal Transceivers	3S	'643	●	●			●				
		'11643						●	●		
	OC	'644		●							
Noninverting 9-Bit Transceivers	3S	'11863						▲	▲		
		'29863	●							●	
Inverting 9-Bit Transceivers	3S	'11864						▲	▲		
		'29864	●							●	
Noninverting 10-Bit Transceivers	3S	'11861						▲	▲		
		'29861	●							●	
Inverting 10-Bit Transceivers	3S	'11862						▲	▲		
		'29862	●							●	
Noninverting 16-Bit Transceivers	3S	'16245						●	●		
		'16623						▲	▲		

NOTES:
● Product available in technology indicated
▲ New Product planned in technology indicated

BUFFER/DRIVERS AND BUS TRANSCEIVERS (continued)

Bus Transceivers (continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Inverting 16-Bit Transceivers	3S	'16640						▲	●		
		'16620						●	▲		
Noninverting 18-Bit Transceivers	3S	'16863						▲	▲		
Inverting 18-Bit Transceivers	3S	'16864						▲	▲		
Noninverting 20-Bit Transceivers	3S	'16861						▲	▲		
Inverting 20-Bit Transceivers	3S	'16862						▲	▲		
Noninverting Octal Registered Transceivers	3S	'543			▲					●	▲
		'11543						▲	▲		
		'646	●	●		●	●			●	▲
		'11646						●	●		
		'25646								▲	
	OC	'647	●								
	3S	'652	●	●		●	●			●	▲
		'11652						●	●		
		'25652								▲	
	OC/3S	'653	●								
		'654	●								
	3S	'2952								▲	▲
Inverting Octal Registered Transceivers	3S	'544			▲					●	▲
		'11544						▲	▲		
		'648	●	●		●	●			▲	▲
		'11648						●	●		
		'651	●	●		●	●			▲	▲
		'11651						▲	▲		
		'2953								▲	▲
Noninverting 16-Bit Registered Transceivers	3S	'16470						▲	▲		
		'16543						▲	●		
		'16646						▲	●		
		'16652						▲	●		
		'16952						▲	▲		
Inverting 16-Bit Registered Transceivers	3S	'16471						▲	▲		
		'16544						▲	●		
		'16648						▲	▲		
		'16651						▲	▲		
		'16953						▲	▲		
Noninverting 18-Bit Registered Transceivers	3S	'16472						▲	▲		
		'16474						▲	▲		
Inverting 18-Bit Registered Transceivers	3S	'16473						▲	▲		
		'16475						▲	▲		

NOTES:
- ● Product available in technology indicated
- ▲ New Product planned in technology indicated

BUFFER/DRIVERS AND BUS TRANSCEIVERS (continued)

Bus Transceivers (continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
8-/9-Bit Bus Transceivers with Parity Checker/ Generator	3S	'657			▲					▲	▲
		'11657						▲	▲		
		'658				●	●				
		'659				●	●				
		'664					●				
		'665					●				
	3S/OC	'11833						▲	▲		
		'29833	●							●	
		'11834						▲	▲		
		'29834								●	
		'11853						▲	▲		
		'29853	●							●	
		'11854						▲	▲		
		'29854	●							●	
Universal Transceivers/ Port Controllers	3S	'11852						▲	▲		
		'856		●							
		'877		●							

MOS Memory Drivers/Transceivers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Octal Transceivers w/ Series Resistors on Output	3S	'2623		●							
		'2640		●							
		'2645		●							
Octal Buffers/ Drivers w/ Series Resistors on Output	3S	'2240	●							●	
		'2241								●	
		'2244	●							●	
		'2540	●								
		'2541	●								
Octal Bidirectional Transceiver w/ Series Resistors on A-port	3S	'2245								▲	
Octal Latch w/ Series Resistors on Output	3S	'2574								▲	
10-Bit Buffers/ Drivers w/ Series Resistors	3S	'2827								●	
		'2828								●	
11-Bit Buffers/ Drivers w/ Series Resistors	3S	'2410								▲	
		'2411								▲	

NOTES:
● Product available in technology indicated
▲ New Product planned in technology indicated

TESTABILITY BUS INTERFACE CIRCUITS

SCOPE™ Testability Circuits (3-State Output)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Octal Buffer/ Driver	3S	'8244								●	
Octal Transceiver	3S	'8245								●	
Octal Transparent Latch	3S	'8373								●	
Octal Flip-Flop	3S	'8374								●	

FLIP-FLOPS/LATCHES

Flip-Flops

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Dual J-K Edge Triggered		'73				●					
		'76				●					
		'107				●					
		'109	●	●	●	●					
		'11109						●	●		
		'112	●		●	●					
		'11112						●	●		
		'113	●		●	●					
		'114	●		●						
Dual D-Type		'74	●	●	●	●	●				
		'11074						●	●		
Dual D-Type with 2-Input NAND/NOR Gates		'7074				●					
		'7075				●					
		'7076				●					
Dual 4-Bit D-Type Edge-Triggered		'874	●	●							
		'11874						●	●		
		'876	●	●							
	3S	'878	●	●							
		'879	●	●							
Quad D-Type		'173				●					
		'175	●	●	●	●					
		'11175						●	●		
		'379			●	●					
		'11379						●	▲		
Hex D-Type		'174	●	●	▲	●					
		'11174						▲	▲		
		'378			▲	●					
		'11378						▲	▲		
Octal D-Type True Data	3-S	'374	●	●	●	●	●			●	▲
		'11374						●	●		
		'574	●	●	▲	●	●			▲	▲

NOTES:
● Product available in technology indicated
▲ New Product planned in technology indicated

FLIP-FLOPS/LATCHES (continued)

Flip-Flops (continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Octal D-Type True Data with Clear		'273	●		▲	●	●				
		'11273						▲	▲		
	3-S	'575	●	●							
		'874	●	●							
		'878	●	●							
Octal D-Type True Data with Enable		'377			●	●	●				▲
		'11377						●	●		
Octal D-Type Inverting	3-S	'534	●	●	●	●	●			●	▲
		'11534						●	●		
		'564	●		●	●	●			▲	
		'576	●	●							
		'826		●							
		'11826						▲	▲		
		'29826	●							▲	
Octal Dual Ranked True Data	3-S	'4374		●							
		'11478						▲	▲		
Octal Inverting with Clear	3-S	'577	●	●							
		'879	●	●							
Octal Inverting with Preset	3-S	'876	●	●							
Octal True Data	3-S	'825		●							
		'11825						▲	▲		
		'29825	▲							▲	
9-Bit True Data	3-S	'823		●							▲
		'11823						▲	▲		
		'29823	●							●	
9-Bit Inverting	3-S	'824		●							
		'11824						▲	▲		
		'29824	●							▲	
10-Bit True Data	3-S	'821		●							▲
		'11821						▲	▲		
		'29821	●							●	
10-Bit Inverting	3-S	'822		●							
		'11822						●	●		
8-Bit Diagnostic Pipeline Register		'29818	●								
16-Bit Noninverting	3-S	'16374						▲	●		
16-Bit Inverting	3-S	'16534						▲	▲		
18-Bit Noninverting	3-S	'16823						▲	▲		
18-Bit Inverting	3-S	'16824						▲	▲		
20-Bit Noninverting	3-S	'16821						▲	▲		
20-Bit Inverting	3-S	'16822						▲	▲		

NOTES:
● Product available in technology indicated
▲ New Product planned in technology indicated

FLIP-FLOPS/LATCHES (continued)

Latches

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY								
				ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Bistable	4-Bit		'75				●					
			'375				●					
D-Type Edge-Triggered Inverting and Noninverting	Octal		'996	●								
D-Type Transparent Readback Latch True	Octal	3S	'990	●								
	9-Bit	3S	'992	●								
	10-Bit	3S	'994	●								
D-Type Transparent Readback Latch Inverting	Octal	3S	'991	●								
	9-Bit	3S	'993	●								
D-Type Transparent with Clear True Outputs	Octal	3S	'666	●								
D-Type Transparent with Clear Inverting Outputs	Octal		'667	●								
D-Type Transparent True	Octal	3-S	'373	●	●	●	●	●			●	▲
			'11373						●	●		
			'573	●	●	●	●	●			▲	▲
	16-Bit	3S	'16373						▲	●		
D-Type Dual 4-Bit Transparent True	Octal	3-S	'873	●	●							
			'11873						●	●		

NOTES:
● Product available in technology indicated
▲ New Product planned in technology indicated

FLIP-FLOPS/LATCHES (continued)

Latches (continued)

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY								
				ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
D-Type Transparent Inverting	Octal	3-S	'533	●	●	●	●				▲	
			'11533						●	●		
			'563	●		●	●	●			▲	
			'580	●	●							
	16-Bit	3S	'16533						▲	▲		
Dual 4-Bit Transparent Inverting	Octal	3-S	'880	●	●							
2-Input Multiplexed	Octal	3-S	'604				●					
Addressable	Octal	2-S	'259	●			●					
		Q	'4724				●					
D-Type True Inputs	10-Bit	3-S	'841	●	●							▲
			'11841						▲	▲		
			'29841	●							▲	
	9-Bit	3-S	'843	●	●							▲
			'11843						▲	▲		
			'29843	●							●	
	Octal	3-S	'845	●	●							▲
			'11845						▲	▲		
			'29845	●							▲	
	18-Bit	3S	'16843						▲	▲		
	20-Bit	3S	'16841						▲	▲		
D-Type Inverting Inputs	10-Bit	3-S	'842	●	●							
			'11842						▲	▲		
			'29842	●							▲	
	9-Bit	3-S	'844	●	●							
			'11844						▲	▲		
			'29844	●							▲	
	Octal	3-S	'846	●								
			'11846						▲	▲		
			'29846	●							●	
	18-Bit	3S	'16844						▲	▲		
	20-Bit	3S	'16842						▲	▲		

NOTES:
● Product available in technology indicated
▲ New Product planned in technology indicated

REGISTERS

Shift Registers

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY								
				ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Parallel-In Parallel-Out	4		'194		●		●					
			'11194						●	▲		
Bidirection	8		'198									
			'299	●		●	●				▲	
			'11299						▲	▲		
			'323	●		●					▲	
			'11323						▲	▲		
Parallel-In Parallel-Out	4		'195		●		●					
Serial-In Parallel-Out	8		'164	●			●					
Parallel-In Serial-Out	8		'165	●			●					
			'166	●			●					
Serial-In Parallel-Out with Output Latches	8	3-S	'594				●					
			'595				●					

Register Files

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Dual 16 Word x 4 Bits	3-S	'870	●	●							
		'11870						▲	▲		
		'871		●							

NOTES:
● Product available in technology indicated
▲ New Product planned in technology indicated

COUNTERS

Synchronous Counters—Positive-Edge Triggered

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY							
			ALS	AS	F	HC	HCT	AC	ACT	BCT
4-Bit Decade	Sync	'160	●	●	●	●				
		'11160						●	▲	
		'162	●	●	●					
		'11162						●	▲	
		'560	●							
4-Bit Decade Up/ Down	Sync	'168	●		●					
		'11168						▲	▲	
	Async	'190	●		▲	●				
		'11190						▲	▲	
		'192	●		▲	●				
		'11192						▲	▲	
	Sync	'568	●		●					
		'11568						▲	▲	
4-Bit Binary	Sync	'161	●	●	●	●				
		'11161						▲	▲	
		'163	●	●	●	●				
		'11163						▲	▲	
		'561	●							
8-Bit Binary	Sync	'11579						▲	▲	
4-Bit Binary Up/Down	Async	'191	●		▲	●				
		'11191						▲	▲	
		'193	●		▲	●				
		'11193						▲	▲	
	Sync	'169	●	●	●					
		'11169						▲	▲	
		'569	●		●					
		'11569						▲	▲	
		'8169	●							
8-Bit Up/Down	Async CLR	'867	●	●						
		'11867						▲	▲	
	Sync CLR	'869	●	●						
		'11869						▲	▲	
Divide-by-10 Counter	Sync	'4017				●				

NOTES:
● Product available in technology indicated
▲ New Product planned in technology indicated

COUNTERS (continued)

Asynchronous Counters (Ripple Clock)—Negative-Edge Triggered

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY							
			ALS	AS	F	HC	HCT	AC	ACT	BCT
Dual 4-Bit Decade	None	'390				•				
	Set-to-9	'490				•				
Dual 4-Bit Binary	None	'393				•				
7-Bit Binary	Sync	'4024				•				
12-Bit Binary	Sync	'4040				•				
14-Bit Binary	Sync	'4020				•				
		'4060				•				
		'4061				•				

8-Bit Binary Counters with Registers

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY							
			ALS	AS	F	HC	HCT	AC	ACT	BCT
Parallel	3-State	'590				•				
Register Outputs		'11590						▲	▲	
Parallel Register Inputs	2-State	'11592						▲	▲	
Parallel I/O	3-State	'11593						▲	▲	

NOTES:
• Product available in technology indicated
▲ New Product planned in technology indicated

DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS

Encoders/Data Selectors/Multiplexers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Quad 2-to-1		'157	●	●	●	●					
		'11157						▲	▲		
		'158	●	●	●	●					
		'11158						●	▲		
		'298		●		●					
	3-S	'257	●	●	●	●					
		'11257						●	●		
		'258	●	●	●	●					
		'11258						●	●		
Dual 4-to-1		'153	●	●	●	●					
		'11153						▲	▲		
	3-S	'253	●	●	●	●					
		'11253						●	●		
		'352	●	●	●	●					
		'11352						▲	▲		
	3-S	'353	●	●	●	●					
		'11353						●	●		
Hex 2-to-1 Universal Multiplexer	3-S	'857	●	●							
8-to-1		'151	●	●	●	●					
		'11151						●	●		
	3-S	'251	●		●	●					
		'11251						●	●		
		'354				●					
16-to-1		'11150						▲	▲		
	3-S	'250		●							
		'11250						▲	▲		
		'850		●							
		'851		●							
Full BCD		'147				●					
Cascadable Octal		'148				●					

NOTES:
● Product available in technology indicated
▲ New Product planned in technology indicated

DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS (continued)

Decoders/Demultiplexers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Dual 2-to-4		'239				●					
		'11239						●	▲		
		'139	●		▲	●	●				
		'11139						●	▲		
		'155	●								
	OC	'156	●								
3-to-8		'138	●	●	●	●	●				
		'11138						●	●		
3-to-8		'237				●	●				
		'238				●	●				
		'11238						●	●		
3-to-8 with Address Registers		'131	●	●							
		'137	●	●		●	●				
4-to-10 BCD-to-Decimal		'42				●					
4-to-16		'154	●								
		'11154						▲	▲		
4-to-16 with Address Latches		'4514				●					
		'4515				●					
Dual 2-to-4 for Battery Backed-Up Memories		'2414								▲	

NOTES:
● Product available in technology indicated
▲ New Product planned in technology indicated

Shifters

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Bit Shifter	3-S	'350			●						

COMPARATORS AND PARITY GENERATOR/CHECKERS

Comparators

DESCRIPTION								TYPE	TECHNOLOGY							
INPUT	P = Q	$\overline{P = Q}$	P>Q	$\overline{P>Q}$	P<Q	OUTPUT	ENABLE		ALS	AS	F	HC	HCT	AC	ACT	BCT
4-Bit/ 8-Bit	Yes		Yes	No		2-S	No	'85				•				
20 kΩ	Yes	No	No	No	No	OC	Yes	'518	•		•					
Pull-up	No	Yes	No	No	No	2-S	Yes	'520	•		•					
								'11520						•	•	
	No	Yes	No	No	No	OC	Yes	'522	•							
	No	Yes	No	Yes	No	2-S	No	'682				•				
Standard	Yes	No	No	No	No	OC	Yes	'519	•		•					
	No	Yes	No	No	No	2-S	Yes	'521	•		•					
								'11521						•	•	
	No	Yes	No	Yes	No	2-S	No	'684				•				
	No	Yes	No	No	No	2-S	Yes	'688	•			•				
	No	Yes	No	No	No	OC	Yes	'689	•							
Latched P	No	No	Yes	No	Yes	2-S	Yes	'885		•						
Latched P and Q	Yes	No	Yes	No	Yes	L	Yes	'866		•						

COMPARATORS AND PARITY GENERATOR/CHECKERS

Address Comparators

DESCRIPTION	OUTPUT ENABLE	LATCHED ENABLE	TYPE	TECHNOLOGY							
				ALS	AS	F	HC	HCT	AC	ACT	BCT
16-Bit to 4-Bit	Yes		'677	•							
			'11677						▲	▲	
		Yes	'11678						▲	▲	
12-Bit to 4-Bit	Yes		'679	•			•				
		Yes	'680	•							

Parity Generators/Checkers

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY								
				ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Odd/Even Generators/ Checkers	9		'280	•	•	•	•					
			'11280						•	•		
			'286		•							
			'11286						•	•		

Fuse-Programmable Comparators

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
16-Bit Identity Comparator		'526	•								
12-Bit Identity Comparator		'528	•								
8-Bit Identity Comparator and 4-Bit Comparator		'527	•								

NOTES:
• Product available in technology indicated
▲ New Product planned in technology indicated

ARITHMETIC CIRCUITS AND FIFO MEMORIES

Parallel Binary Adders

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Bit		'283			●	●					

Accumulators, Arithmetic Logic Units, Look-Ahead Carry Generators

DESCRIPTION		OUTPUT	TYPE	TECHNOLOGY								
				ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Bit Arithmetic Logic Units: Function Generators			'181		●							
			'11181						●	●		
			'381			●						
			'881		●							
			'11881						▲	▲		
4-Bit Arithmetic Logic Unit With Ripple Carry			'382			●						
Look Ahead Carry Generators	32-Bit		'882		●							
			'11882						▲	▲		

First-In First-Out Memories (FIFOs)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY									
			LS	S	ALS	AS	F	HC	HCT	AC	ACT	BCT
16 Words x 4 Bits	3-S	'222	●									
	3-S	'224	●									
	3-S	'232			●							
	OC	'227	●									
	OC	'228	●									
16 Words x 5 Bits	3-S	'225		●								
	3-S	'229B			●							
	3-S	'233B			●							
64 Words x 4 Bits	3-S	'236			●							
	3-S	'234			●							
64 Words x 5 Bits	3-S	'235			●							
64 Words x 8 Bits	3-S	'2232A			●							
64 Words x 9 Bits	3-S	'2233A			●							
32 Words x 9 Bits Bidirectional	3-S	'2238			●							
1k Words x 18 Bits		'7801									●	
		'7802									▲	
1k Words x 9 Bits Bidirectional		'2235									▲	

NOTES:
● Product available in technology indicated
▲ New Product planned in technology indicated

CLOCK DRIVER CIRCUITS

Clock Driver

DESCRIPTION	TYPE	TECHNOLOGY							
		ALS	AS	F	HC	HCT	AC	ACT	BCT
Hex Inverting Clock Drivers/Buffers	'11204						•		
Dual 1-to-4 Clock Drivers/Buffers	'11208						•	•	
Triple 4-Input AND/NAND Clock Drivers	'11800						▲	▲	
Triple 4-Input OR/NOR Clock Drivers	'11802						▲	▲	
Octal Divide-by-2 Clock Drivers (6 Invert, 9 Noninvert)	'303		•						
Octal Divide-by-2 Clock Drivers (8 Noninvert)	'305		•						
Octal Divide-by-2 Clock Drivers (4 Invert, 4 Noninvert)	'304		▲						

NOTES:
• Product available in technology indicated
▲ New Product planned in technology indicated

ECL TRANSLATORS

ECL-to-TTL or TTL-to-ECL Translators

DESCRIPTION	LEVEL TRANSLATION	OUTPUT	TYPE	AVAILABILITY
Octal Bus Driver Inverting	ECL-to-TTL	OC	10KHT5538	•
			100KT5538	•
		3S	10KHT5540	•
			100KT5540	•
	TTL-to-ECL	OE	10KHT5542	•
			100KT5542	•
Octal Bus Driver Noninverting	ECL-to-TTL	OC	10KHT5539	•
			100KT5539	•
		3S	10KHT5541	•
			100KT5541	•
	TTL-to-ECL	OE	10KHT5543	•
			100KT5543	•
Octal Bus Transceiver Inverting	ECL-to-TTL TTL-to-ECL	OE/3S	10KHT5563	▲
			100KT5563	▲
			10KHT5562	▲
			100KT5562	▲
Octal Bus Transceiver Noninverting	ECL-to-TTL TTL-to-ECL	OE/3S	10KHT5564	▲
			100KT5564	▲
			10KHT5565	▲
			100KT5565	▲

ECL TRANSLATORS (continued)

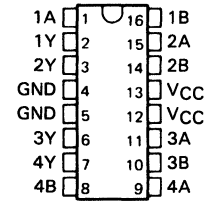
ECL-to-TTL or TTL-to-ECL Translators (continued)

DESCRIPTION	LEVEL TRANSLATION	OUTPUT	TYPE	AVAILABILITY
Octal D-Type Latch Inverting	ECL-to-TTL	3S	10KHT5575	▲
			100KT5575	▲
	TTL-to-ECL	OE	10KHT5579	▲
			100KT5579	▲
Octal D-Type Latch True	ECL-to-TTL	3S	10KHT5573	▲
			100KT5573	▲
	TTL-to-ECL	OE	10KHT5577	▲
			100KT5577	▲
Octal D-type Flip-Flop Inverting	ECL-to-TTL	3S	10KHT5576	▲
			100KT5576	▲
	TTL-to-ECL	OE	10KHT5580	▲
			100KT5580	▲
Octal D-Type Flip-Flop True	ECL-to-TTL	3S	10KHT5574	●
			100KT5574	●
	TTL-to-ECL	OE	10KHT5578	●
			100KT5578	●
Octal Registered Transceiver Inverting	ECL-to-TTL	OE/3S	10KHT5591	▲
			100KT5591	▲
			10KHT5593	▲
			100KT5593	▲
			10KHT5648	▲
			100KT5648	▲
Octal Registered Transceiver Noninverting	ECL-to-TTL	OE/3S	10KHT5590	▲
			100KT5590	▲
			10KHT5592	▲
			100KT5592	▲
			10KHT5646	▲
			100KT5646	▲

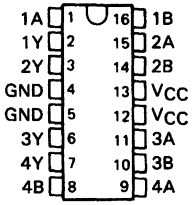
NOTES:
- ● Product available in technology indicated
- ▲ New Product planned in technology indicated

EPIC™ ACL PINOUTS

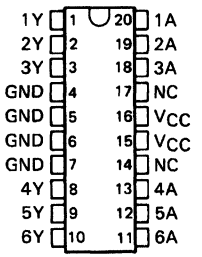
'AC11000, 'ACT11000
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
(TOP VIEW)



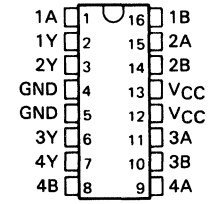
'AC11002, 'ACT11002
QUADRUPLE 2-INPUT
POSITIVE-NOR GATES
(TOP VIEW)



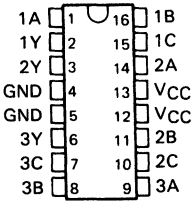
'AC11004, 'ACT11004
HEX INVERTERS
(TOP VIEW)



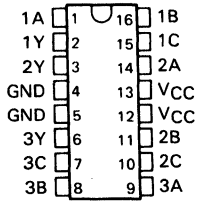
'AC11008, 'ACT11008
QUADRUPLE 2-INPUT
POSITIVE-AND GATES
(TOP VIEW)



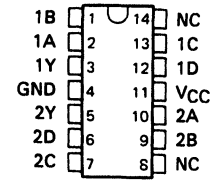
'AC11010, 'ACT11010
TRIPLE 3-INPUT
POSITIVE-NAND GATES
(TOP VIEW)



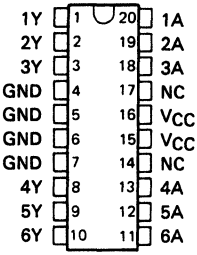
'AC11011, 'ACT11011
TRIPLE 3-INPUT
POSITIVE-AND GATES
(TOP VIEW)



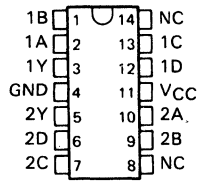
'AC11013, 'ACT11013
DUAL 4-INPUT GATES
(TOP VIEW)



'AC11014, 'ACT11014
HEX INVERTERS
(TOP VIEW)



'AC11020, 'ACT11020
DUAL 4-INPUT
POSITIVE-NAND GATES
(TOP VIEW)



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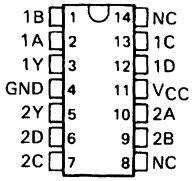
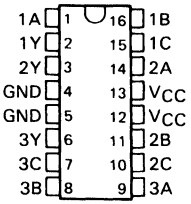
EPIC™ ACL PINOUTS (continued)

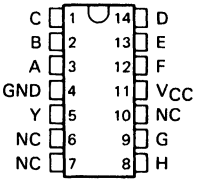
'AC11021, 'ACT11021
DUAL 4-INPUT
POSITIVE-AND GATES
(TOP VIEW)



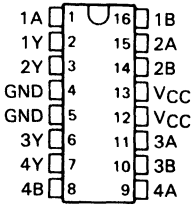
'AC11027, 'ACT11027
TRIPLE 3-INPUT
POSITIVE-NOR GATES
(TOP VIEW)



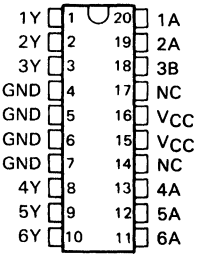
'AC11030, 'ACT11030
8-INPUT POSITIVE-NAND GATES
(TOP VIEW)



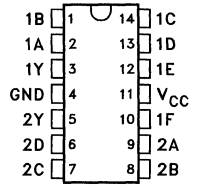
'AC11032, 'ACT11032
QUADRUPLE 2-INPUT
POSITIVE-OR GATES
(TOP VIEW)



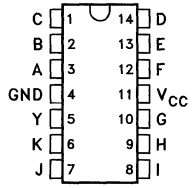
'AC11034, 'ACT11034
HEX NONINVERTERS
(TOP VIEW)



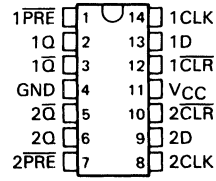
'AC11051, 'ACT11051
DUAL 2-INPUT AND-OR GATE
(TOP VIEW)



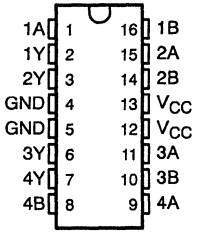
'AC11064, 'ACT11064
QUAD 4-2-3-2-INPUT AND-OR GATE
(TOP VIEW)



'AC11074, 'ACT11074
DUAL D-TYPE POSITIVE-EDGE
TRIGGERED FLIP-FLOPS WITH
CLEAR AND PRESET
(TOP VIEW)

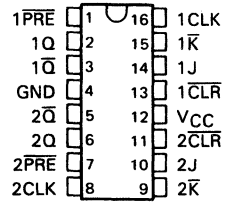


'AC11086, 'ACT11086
QUAD 2-INPUT EXCLUSIVE-OR GATE
(TOP VIEW)

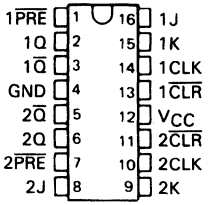


EPIC™ ACL PINOUTS (continued)

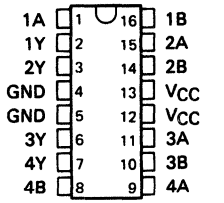
'AC11109, 'ACT11109
DUAL J-K
POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET
(TOP VIEW)



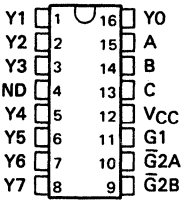
'AC11112, 'ACT11112
DUAL J-K NEGATIVE
EDGE-TRIGGERED FLIP-FLOPS
WITH CLEAR AND PRESET
(TOP VIEW)



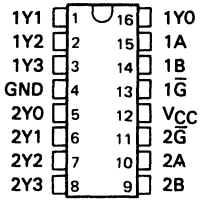
'AC11132, 'ACT11132
QUADRUPLE 2-INPUT
POSITIVE-NAND SCHMITT TRIGGERS
(TOP VIEW)



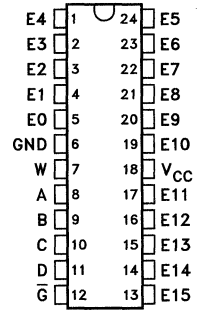
'AC11138, 'ACT11138
3-LINE TO 8-LINE
DECODERS/DEMULTIPLEXERS
(TOP VIEW)



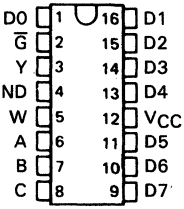
'AC11139, 'ACT11139
DUAL 2-LINE TO 4-LINE
DECODERS/DEMULTIPLEXERS
(TOP VIEW)



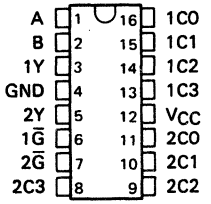
'AC11150, 'ACT11150
1-OF-16 DATA
GENERATOR/MULTIPLEXERS
(TOP VIEW)



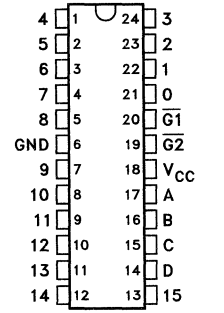
'AC11151, 'ACT11151
1 OF 8 DATA
SELECTORS/MULTIPLEXERS
(TOP VIEW)



'AC11153, 'ACT11153
DUAL 4-LINE TO 1-LINE DATA
SELECTORS/MULTIPLEXERS
(TOP VIEW)

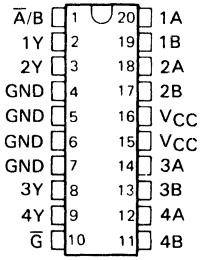


'AC11154, 'ACT11154
4-TO-16 LINE
DECODER/DEMULTIPLEXER
(TOP VIEW)

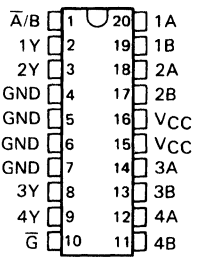


EPIC™ ACL PINOUTS (continued)

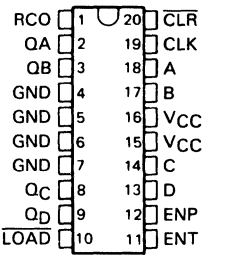
'AC11157, 'ACT11157
QUADRUPLE 1 OF 2
DATA SELECTORS/MULTIPLEXERS
(TOP VIEW)



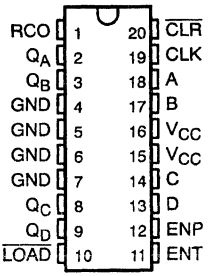
'AC11158, 'ACT11158
QUADRUPLE 1 OF 2 DATA
SELECTORS/MULTIPLEXERS
(TOP VIEW)



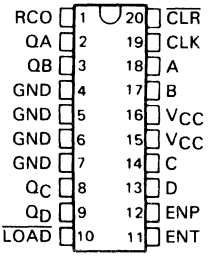
'AC11160, 'ACT11160
SYNCHRONOUS 4-BIT
DECADE COUNTERS
(TOP VIEW)



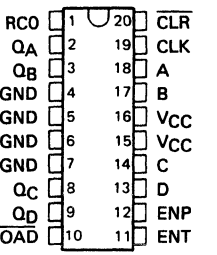
'AC11161, 'ACT11161
SYNCHRONOUS 4-BIT
BINARY COUNTERS
(TOP VIEW)



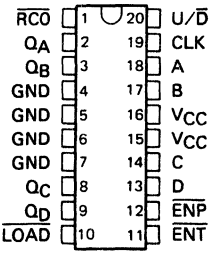
'AC11162, 'ACT11162
SYNCHRONOUS 4-BIT
DECADE COUNTERS
(TOP VIEW)



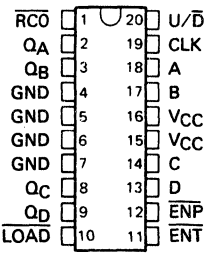
'AC11163, 'ACT11163
SYNCHRONOUS 4-BIT
BINARY COUNTERS
(TOP VIEW)



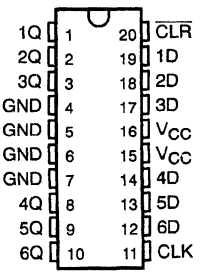
'AC11168, 'ACT11168
SYNCHRONOUS 4-BIT UP/DOWN
DECADE COUNTERS
(TOP VIEW)



'AC11169, 'ACT11169
SYNCHRONOUS 4-BIT UP/DOWN
BINARY COUNTERS
(TOP VIEW)

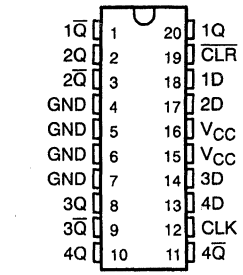


'AC11174, 'ACT11174
HEX D-TYPE
FLIP-FLOPS WITH CLEAR
(TOP VIEW)

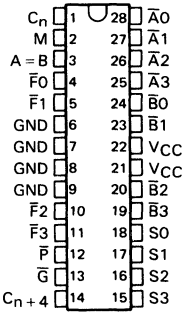


EPIC™ ACL PINOUTS (continued)

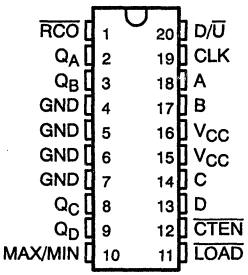
'AC11175, 'ACT11175
QUADRUPLE D-TYPE
FLIP-FLOPS WITH CLEAR
(TOP VIEW)



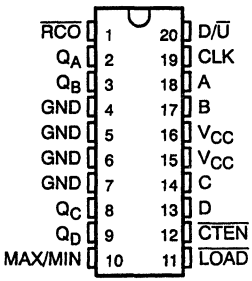
'AC11181, 'ACT11181
ARITHMETIC LOGIC UNITS/
FUNCTION GENERATORS
(TOP VIEW)



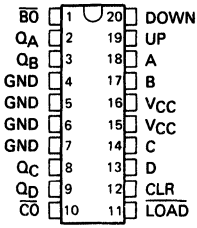
'AC11190, 'ACT11190
SYNCHRONOUS 4-BIT UP/DOWN
DECADE COUNTERS
(TOP VIEW)



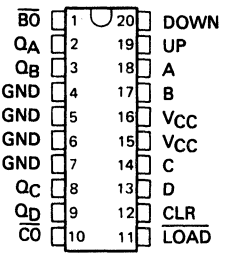
'AC11191, 'ACT11191
SYNCHRONOUS 4-BIT UP/DOWN
BINARY COUNTERS
(TOP VIEW)



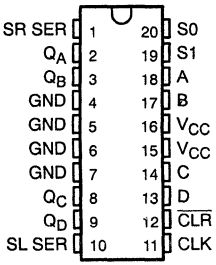
'AC11192, 'ACT11192
SYNCHRONOUS 4-BIT UP/DOWN DECADE
COUNTERS (DUAL CLOCK WITH CLEAR)
(TOP VIEW)



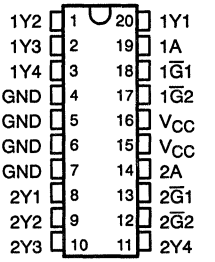
'AC11193, 'ACT11193
SYNCHRONOUS 4-BIT UP/DOWN BINARY
COUNTERS (DUAL CLOCK WITH CLEAR)
(TOP VIEW)



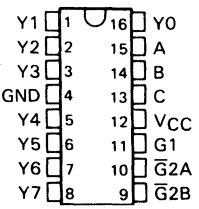
'AC11194, 'ACT11194
4-BIT BIDIRECTIONAL UNIVERSAL
SHIFT REGISTERS
(TOP VIEW)



'AC11208, 'ACT11208
DUAL 1-TO-4 CLOCK DRIVER
(TOP VIEW)

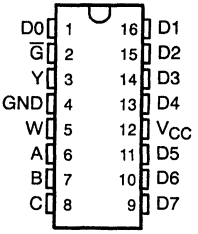


'AC11238, 'ACT11238
3-LINE TO 8-LINE
DECODERS/DEMULTIPLEXERS
(TOP VIEW)

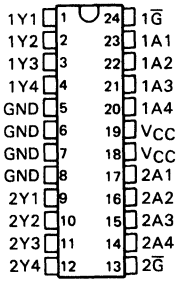


EPIC™ ACL PINOUTS (continued)

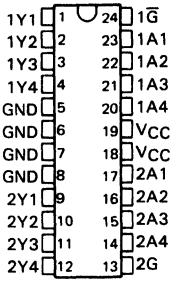
'AC11239, 'ACT11239
DUAL 2-LINE TO 4-LINE
DECODERS/DEMULTIPLEXERS
(TOP VIEW)



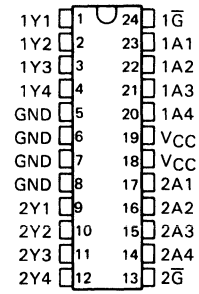
'AC11240, 'ACT11240
OCTAL BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS
(TOP VIEW)



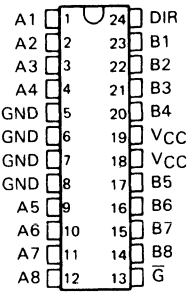
'AC11241, 'ACT11241
OCTAL BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS
(TOP VIEW)



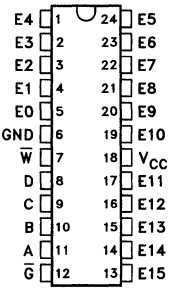
'AC11244, 'ACT11244
OCTAL BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS
(TOP VIEW)



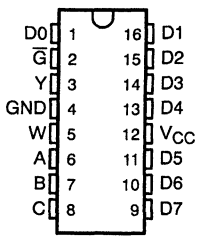
'AC11245, 'ACT11245
OCTAL BUS TRANSCEIVERS WITH
3-STATE OUTPUTS
(TOP VIEW)



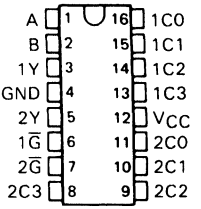
'AC11250, 'ACT11250
1-OF-16 DATA
GENERATOR/MULTIPLEXER
(TOP VIEW)



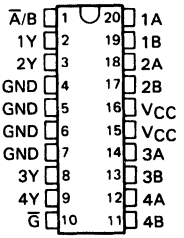
'AC11251, 'ACT11251
1 OF 8 DATA SELECTORS/
MULTIPLEXERS WITH 3-STATE OUTPUTS
(TOP VIEW)



'AC11253, 'ACT11253
DUAL 4-LINE TO 1-LINE DATA
SELECTORS/MULTIPLEXERS
WITH 3-STATE OUTPUTS
(TOP VIEW)

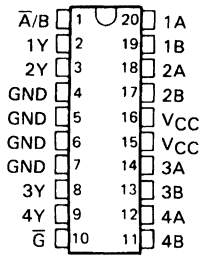


'AC11257, 'ACT11257
QUADRUPLE 1 OF 2 DATA
SELECTORS/MULTIPLEXERS WITH
3-STATE OUTPUTS
(TOP VIEW)

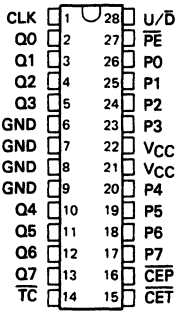


EPIC™ ACL PINOUTS (continued)

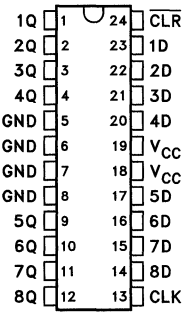
'AC11258, 'ACT11258
QUADRUPLE 1 OF 2 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS
(TOP VIEW)



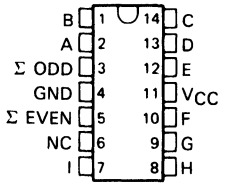
'AC11269, 'ACT11269
8-BIT BIDIRECTIONAL BINARY COUNTER
(TOP VIEW)



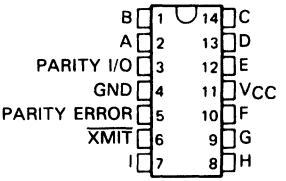
'AC11273, 'ACT11273
OCTAL D-TYPE FLIP-FLOP
(TOP VIEW)



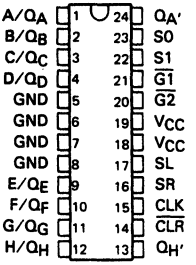
'AC11280, 'ACT11280
9-BIT PARITY GENERATORS/CHECKERS
(TOP VIEW)



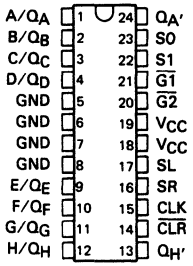
'AC11286, 'ACT11286
9-BIT PARITY GENERATORS/CHECKERS WITH BUS DRIVER PARITY I/O PORT
(TOP VIEW)



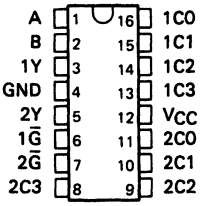
'AC11299, 'ACT11299
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS
(TOP VIEW)



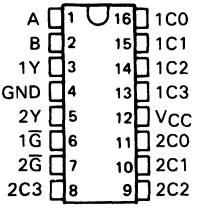
'AC11323, 'ACT11323
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS
(TOP VIEW)



'AC11352, 'ACT11352
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS
(TOP VIEW)

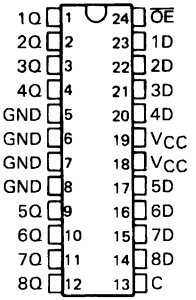


'AC11353, 'ACT11353
DUAL 1 OF 4 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS
(TOP VIEW)

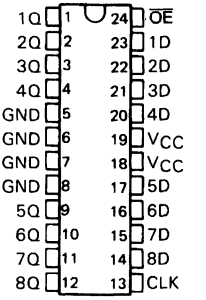


EPIC™ ACL PINOUTS (continued)

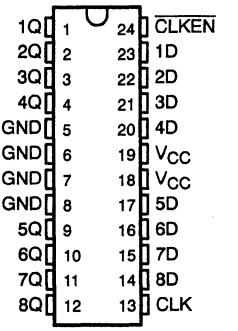
'AC11373, 'ACT11373
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



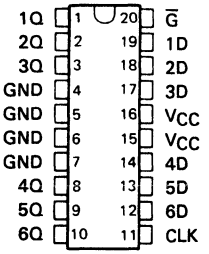
'AC11374, 'ACT11374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
(TOP VIEW)



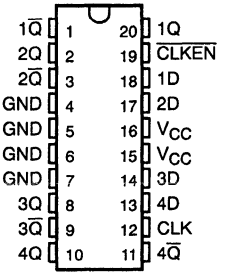
'AC11377, 'ACT11377
OCTAL D-TYPE FLIP-FLOP
(TOP VIEW)



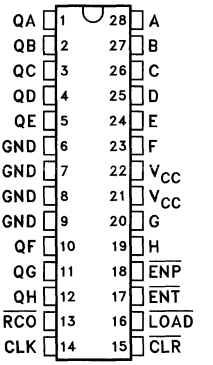
'AC11378, 'ACT11378
HEX D-TYPE FLIP-FLOPS WITH CLOCK ENABLE
(TOP VIEW)



'AC11379, 'ACT11379
QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR
(TOP VIEW)

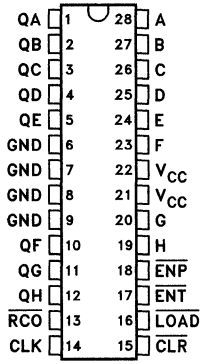


'AC11461
'ACT11461
8-BIT SYNCHRONOUS BINARY COUNTER
(TOP VIEW)

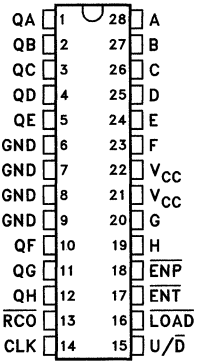


EPIC™ ACL PINOUTS (continued)

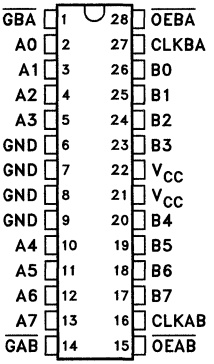
'AC11463
'ACT11463
8-BIT SYNCHRONOUS
BINARY COUNTER
(TOP VIEW)



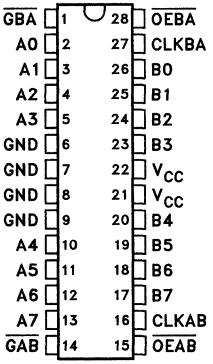
'AC11469
'ACT11469
8-BIT SYNCHRONOUS
UP/DOWN COUNTER
(TOP VIEW)



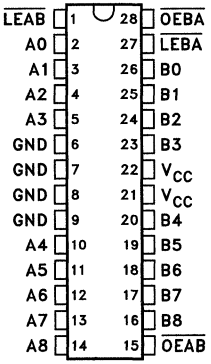
'AC11470
'ACT11470
OCTAL BUS
TRANSCEIVER
(TOP VIEW)



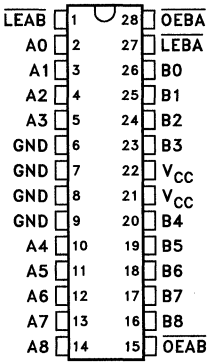
'AC11471
'ACT11471
OCTAL BUS
TRANSCEIVER
(TOP VIEW)



'AC11472
'ACT11472
9-BIT BUS
TRANSCEIVER
(TOP VIEW)



'AC11473
'ACT11473
9-BIT BUS
TRANSCEIVER
(TOP VIEW)



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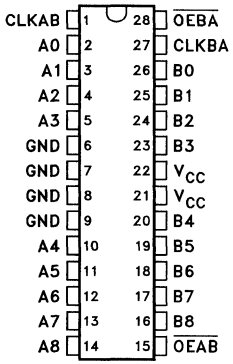
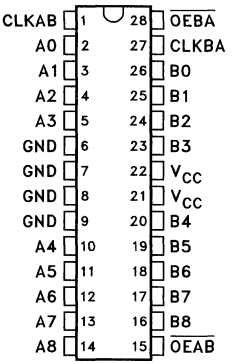
EPIC™ ACL PINOUTS (continued)

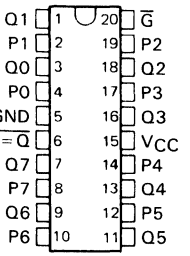
AC11474
ACT11474
9-BIT BUS TRANSCEIVER
(TOP VIEW)



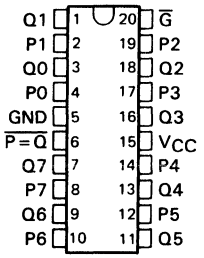
'AC11475
'ACT11475
9-BIT BUS TRANSCEIVER
(TOP VIEW)



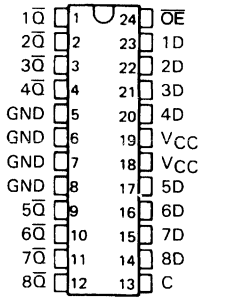
'AC11520, 'ACT11520
8-BIT IDENTITY COMPARATOR
(TOP VIEW)



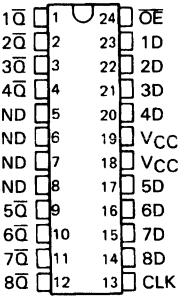
'AC11521, 'ACT11521
8-BIT IDENTITY COMPARATOR
(TOP VIEW)



'AC11533, 'ACT11533
OCTAL D-TYPE TRANSPARENT
LATCHES WITH 3-STATE OUTPUT
(TOP VIEW)

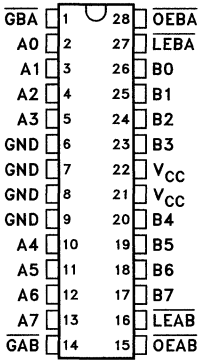


'AC11534, 'ACT11534
OCTAL D-TYPE EDGE-TRIGGERED
FLIP-FLOPS WITH 3-STATE OUTPUT
(TOP VIEW)

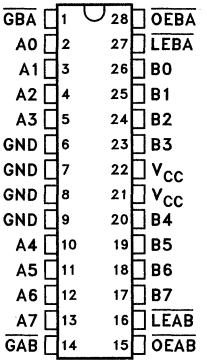


EPIC™ ACL PINOUTS (continued)

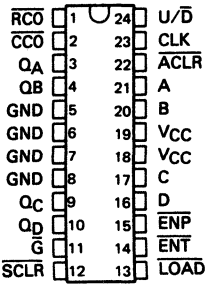
'AC111543, 'ACT11543
OCTAL REGISTERED TRANSCEIVER
(TOP VIEW)



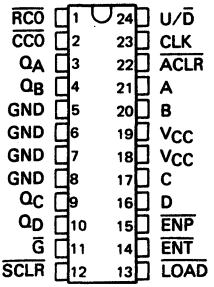
'AC11544, 'ACT11544
OCTAL REGISTERED TRANSCEIVER
(TOP VIEW)



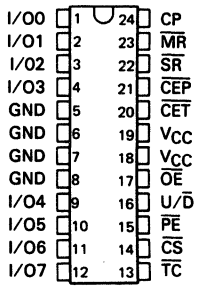
'AC11568, 'ACT11568
SYNCHRONOUS 4-BIT UP/DOWN
DECADE COUNTERS WITH
3-STATE OUTPUTS
(TOP VIEW)



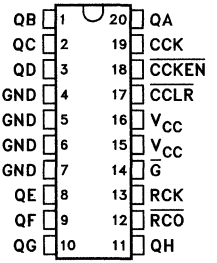
'AC11569, 'ACT11569
SYNCHRONOUS 4-BIT UP/DOWN
BINARY COUNTERS WITH
3-STATE OUTPUTS
(TOP VIEW)



'AC11579, 'ACT11579
8-BIT BIDIRECTIONAL BINARY
COUNTER WITH 3-STATE OUTPUTS
(TOP VIEW)

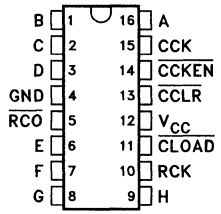


'AC11590, 'ACT11590
8-BIT REGISTERED BINARY COUNTER
(TOP VIEW)

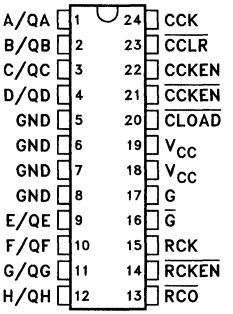


EPIC™ ACL PINOUTS (continued)

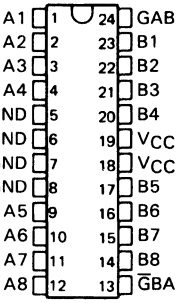
'AC11592, 'ACT11592
8-BIT REGISTERED BINARY COUNTER
(TOP VIEW)



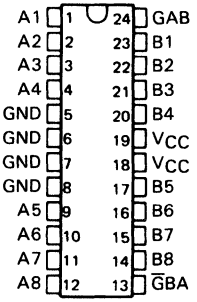
'AC11593, 'ACT11593
8-BIT REGISTERED BINARY COUNTER
(TOP VIEW)



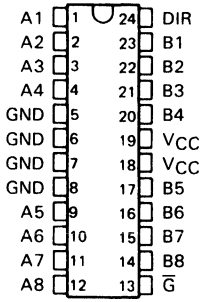
'AC11620, 'ACT11620
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTUTS
(TOP VIEW)



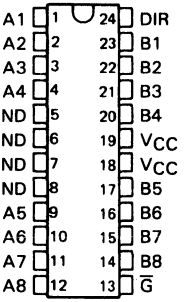
'AC11623, 'ACT11623
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
(TOP VIEW)



'AC11640, 'ACT11640
OCTAL BUS TRANSCEIVERS
(TOP VIEW)

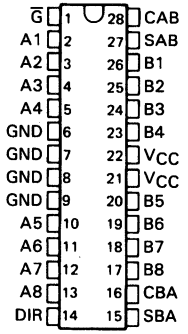


'AC11643, 'ACT11643
OCTAL BUS TRANSCEIVERS
(TOP VIEW)

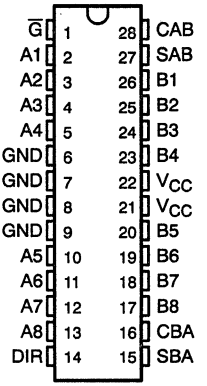


EPIC™ ACL PINOUTS (continued)

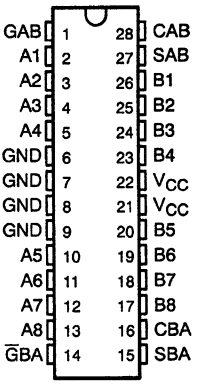
'AC11646, 'ACT11646
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS
(TOP VIEW)



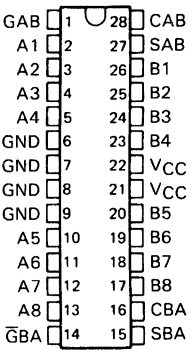
'AC11648, 'ACT11648
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS
(TOP VIEW)



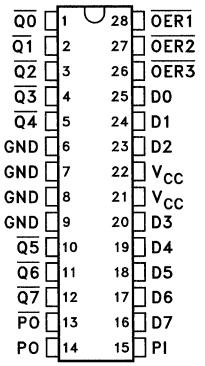
'AC11651, 'ACT11651
OCTAL BUS TRANSCEIVERS AND REGISTERS
(TOP VIEW)



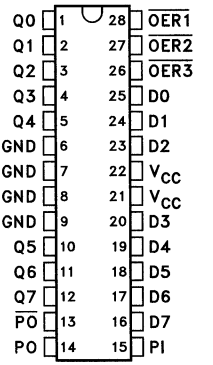
'AC11652, 'ACT11652
OCTAL BUS TRANSCEIVERS AND REGISTERS
(TOP VIEW)



'AC11655, 'ACT11655
OCTAL BUS DRIVER WITH PARITY
(TOP VIEW)

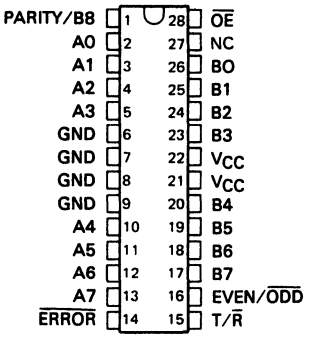


'AC11656, 'ACT11656
OCTAL BUS DRIVER WITH PARITY
(TOP VIEW)

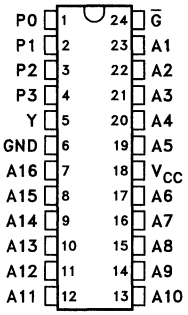


EPIC™ ACL PINOUTS (continued)

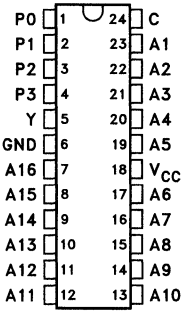
'AC11657, 'ACT11657
OCTAL BIDIRECTIONAL TRANSCEIVERS WITH 8-BIT PARITY GENERATOR/ CHECKER AND 3-STATE OUTPUTS
(TOP VIEW)



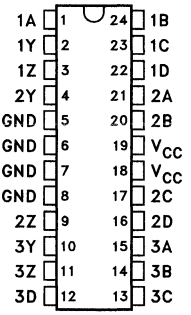
'AC11677, 'ACT11677
16-BIT ADDRESS COMPARATOR
(TOP VIEW)



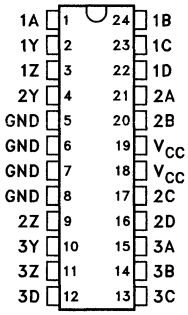
'AC11678, 'ACT11678
16-BIT LATCHED ADDRESS COMPARATOR
(TOP VIEW)



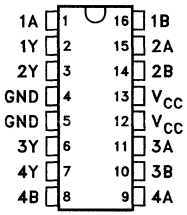
'AC11800, 'ACT11800
TRIPLE 4-INPUT AND/NAND DRIVER
(TOP VIEW)



'AC11802, 'ACT11802
TRIPLE 4-INPUT OR/NOR DRIVER
(TOP VIEW)

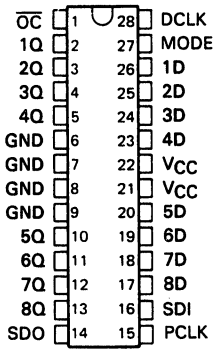


'AC11810, 'ACT11810
QUAD 2-INPUT EXCLUSIVE NOR GATE
(TOP VIEW)

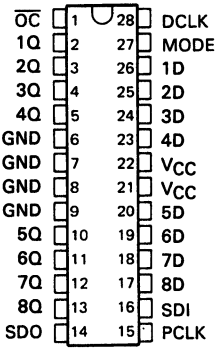


EPIC™ ACL PINOUTS (continued)

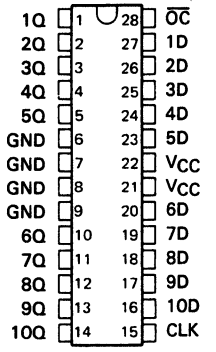
'AC11818, 'ACT11818
DIAGNOSTIC/PIPELINE REGISTER
(TOP VIEW)



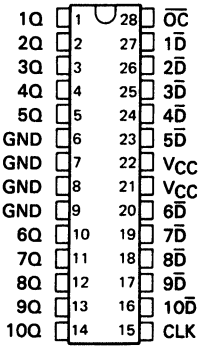
'AC11819, 'ACT11819
DIAGNOSTIC/PIPELINE REGISTER
(TOP VIEW)



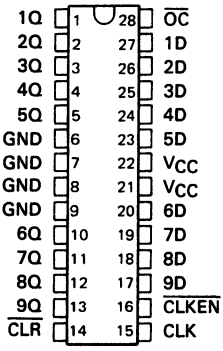
'AC11821, 'ACT11821
10-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS
(TOP VIEW)



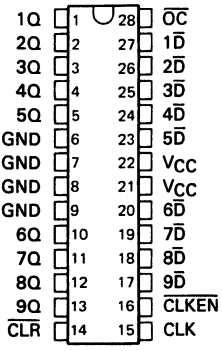
'AC11822, 'ACT11822
10-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS
(TOP VIEW)



'AC11823, 'ACT11823
9-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS
(TOP VIEW)



'AC11824, 'ACT11824
9-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS
(TOP VIEW)



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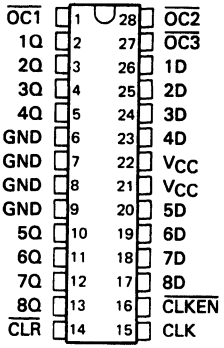
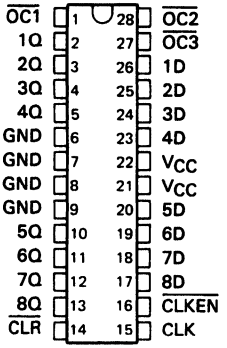
EPIC™ ACL PINOUTS (continued)

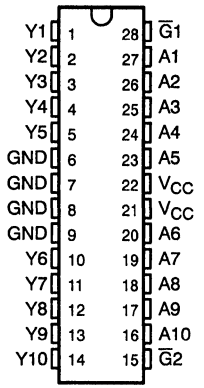
'AC11825, 'ACT11825
8-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS
(TOP VIEW)



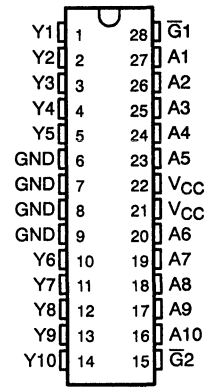
'AC11826, 'ACT11826
8-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS
(TOP VIEW)



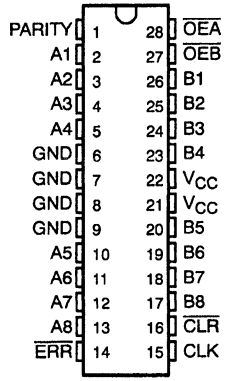
'AC11827, 'ACT11827
10-BIT BUFFERS WITH
3-STATE OUTPUTS
(TOP VIEW)



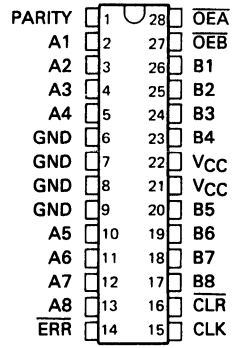
'AC11828, 'ACT11828
10-BIT BUFFERS WITH
3-STATE OUTPUTS
(TOP VIEW)



'AC11833, 'ACT11833
PARITY BUS TRANSCEIVERS
(TOP VIEW)

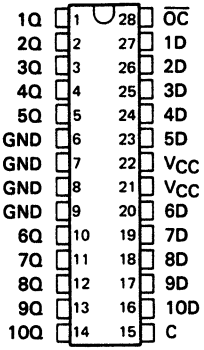


'AC11834, 'ACT11834
PARITY BUS TRANSCEIVERS
(TOP VIEW)

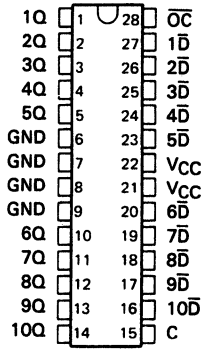


EPIC™ ACL PINOUTS (continued)

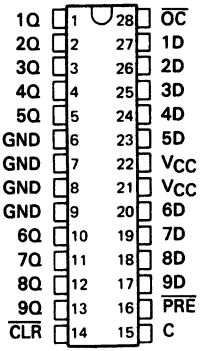
'AC11841, 'ACT11841
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



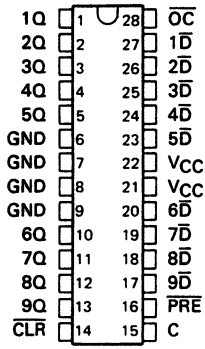
'AC11842, 'ACT11842
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



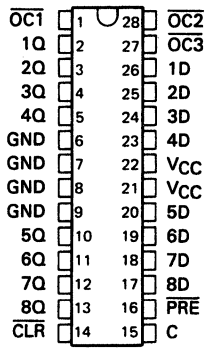
'AC11843, 'ACT11843
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



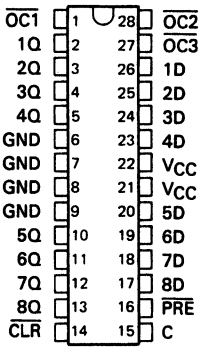
'AC11844, 'ACT11844
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



'AC11845, 'ACT11845
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)

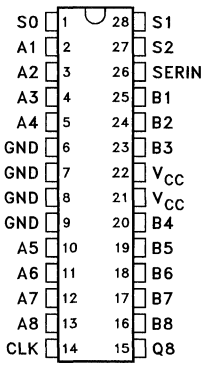


'AC11846, 'ACT11846
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)

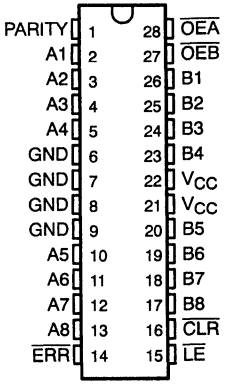


EPIC™ ACL PINOUTS (continued)

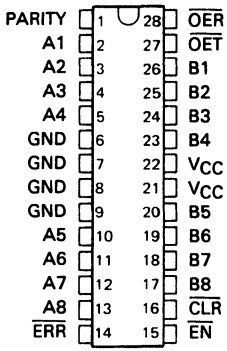
'AC11852, 'ACT11852
8-BIT UNIVERSAL
PORT CONTROLLER
(TOP VIEW)



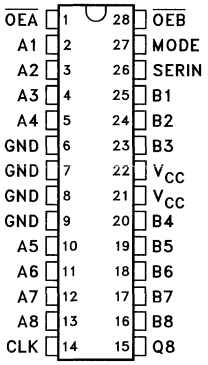
'AC11853, 'ACT11853
PARITY BUS TRANSCEIVERS
(TOP VIEW)



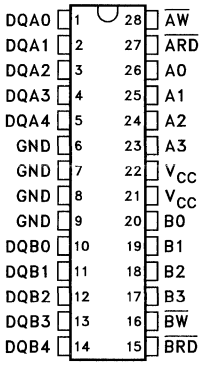
'AC11854, 'ACT11854
PARITY BUS TRANSCEIVERS
(TOP VIEW)



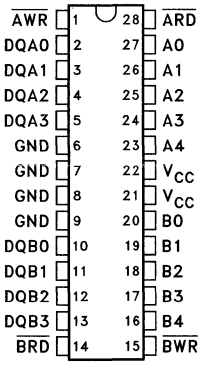
'AC11856, 'ACT11856
8-BIT UNIVERSAL
PORT CONTROLLER
(TOP VIEW)



'AC11858, 'ACT11858
DUAL PORT
16 x 5 REGISTER FILE
(TOP VIEW)

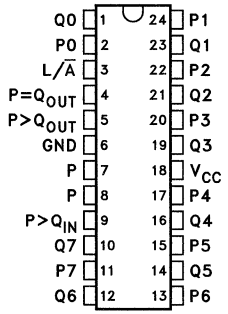


'AC11859, 'ACT11859
DUAL PORT
32 x 4 REGISTER FILE
(TOP VIEW)

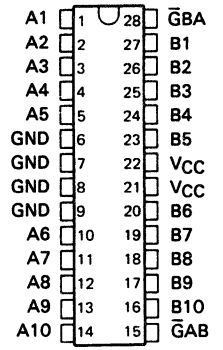


EPIC™ ACL PINOUTS (continued)

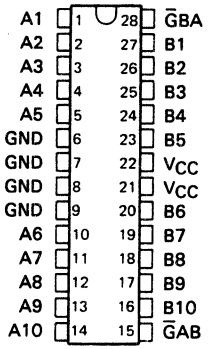
'AC11860, 'ACT11860
8-BIT MAGITUDE COMPARATOR
(TOP VIEW)



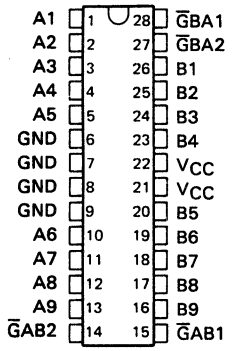
'AC11861, 'ACT11861
10-BIT BUS TRANSCEIVERS WITH
3-STATE OUTPUTS
(TOP VIEW)



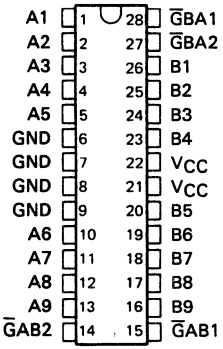
'AC11862, 'ACT11862
10-BIT BUS TRANSCEIVERS WITH
3-STATE OUTPUTS
(TOP VIEW)



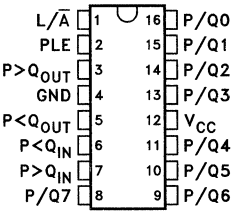
'AC11863, 'ACT11863
9-BIT BUS TRANSCEIVERS WITH
3-STATE OUTPUTS
(TOP VIEW)



'AC11864, 'ACT11864
9-BIT BUS TRANSCEIVERS WITH
3-STATE OUTPUTS
(TOP VIEW)



'AC11865, 'ACT11865
8-BIT MAGNITUDE COMPARATOR
(TOP VIEW)



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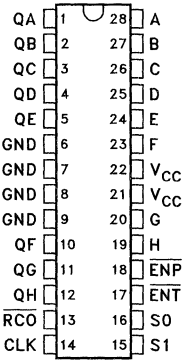
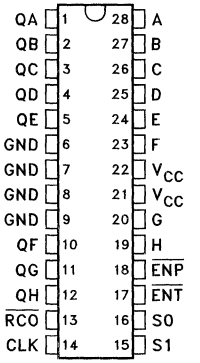
EPIC™ ACL PINOUTS (continued)

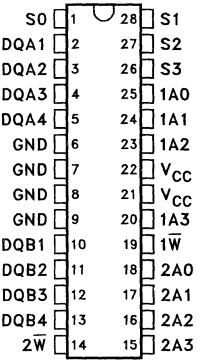
'AC11867, 'ACT11867
8-BIT SYNCHRONOUS
UP/DOWN COUNTER
(TOP VIEW)



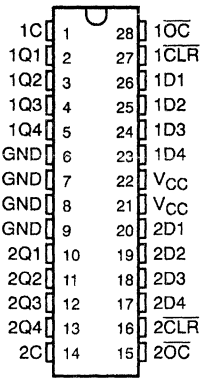
'AC11869, 'ACT11869
8-BIT SYNCHRONOUS
UP/DOWN COUNTER
(TOP VIEW)



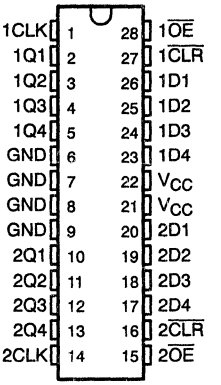
'AC11870, 'ACT11870
DUAL PORT
16 x 4 REGISTER FILE
(TOP VIEW)



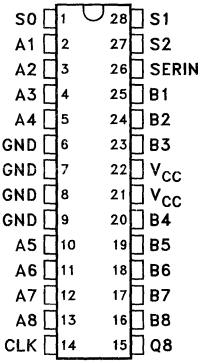
'AC11873, 'ACT11873
DUAL 4-BIT D-TYPE LATCHES
WITH 3-STATE OUTPUTS
(TOP VIEW)



'AC11874, 'ACT11874
DUAL 4-BIT D-TYPE EDGE-TRIGGERED
FLIP-FLOPS
(TOP VIEW)

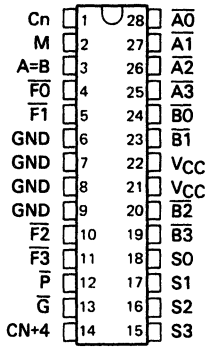


'AC11877, 'ACT11877
8-BIT UNIVERSAL
PORT CONTROLLER
(TOP VIEW)

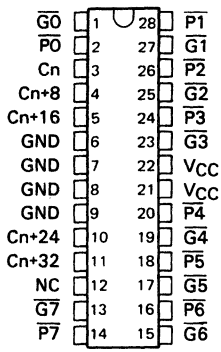


EPIC™ ACL PINOUTS (continued)

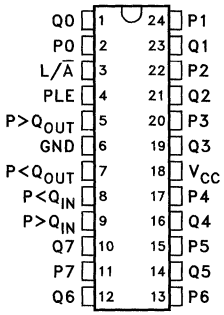
'AC11881, 'ACT11881
ARITHMETIC LOGIC UNITS/
FUNCTION GENERATORS
(TOP VIEW)



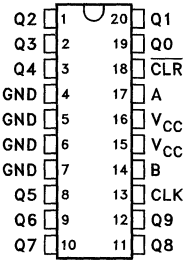
'AC11882, 'ACT11882
32-BIT LOOK-AHEAD
CARRY GENERATORS
(TOP VIEW)



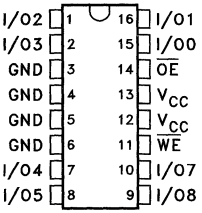
'AC11885, 'ACT11885
8-BIT MAGNITUDE COMPARATOR
(TOP VIEW)



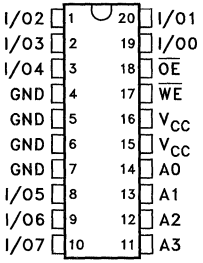
'AC11898, 'ACT11898
10-BIT SHIFT REGISTER
(TOP VIEW)



'AC11979, 'ACT11979
8-BIT MULTIPLEXED I/O
READ-BACK REGISTER
(TOP VIEW)



'AC11980, 'ACT11980
16 x 8 MULTIPLEXED I/O
READ-BACK REGISTER
(TOP VIEW)



TEXAS INSTRUMENTS
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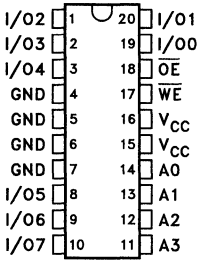
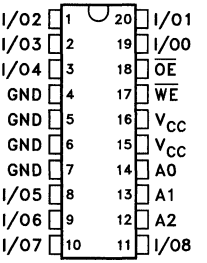
EPIC™ ACL PINOUTS (continued)

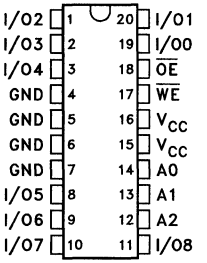
'AC11981, 'ACT11981
16 x 8 MULTIPLEXED I/O
READ-BACK REGISTER
(TOP VIEW)



'AC11987, 'ACT11987
8 x 9 MULTIPLEXED I/O
READ-BACK REGISTER
(TOP VIEW)

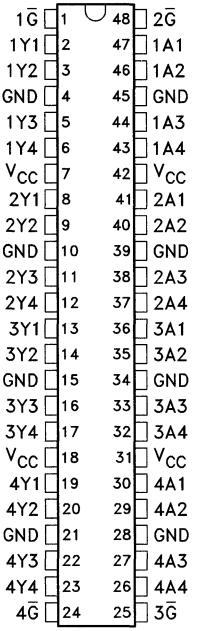


'AC11988, 'ACT11988
8 x 9 MULTIPLEXED I/O
READ-BACK REGISTER
(TOP VIEW)

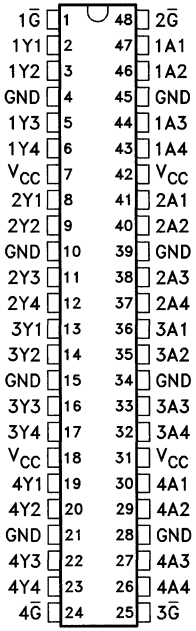


WIDE BUS™ PINOUTS

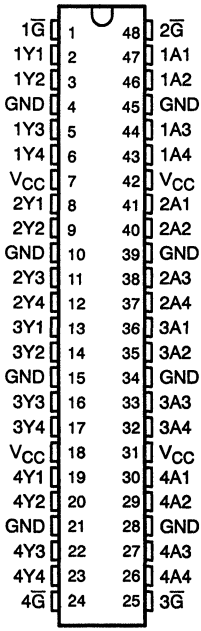
54AC16240 ... WD PACKAGE
74AC16240 ... DL PACKAGE
16-BIT BUS DRIVERS
(TOP VIEW)



54ACT16240 ... WD PACKAGE
74ACT16240 ... DL PACKAGE
16-BIT BUS DRIVERS
(TOP VIEW)



54AC/ACT16241 ... WD PACKAGE
74AC/ACT16241 ... DL PACKAGE
16-BIT BUS DRIVERS
(TOP VIEW)



TEXAS INSTRUMENTS
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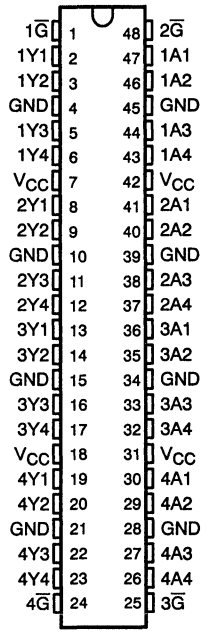
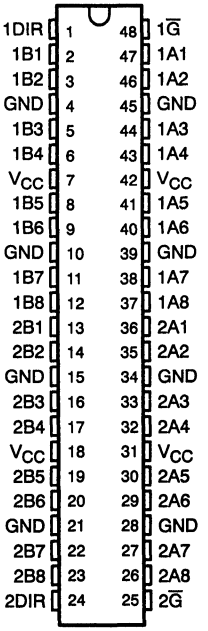
WIDE BUS™ PINOUTS (continued)

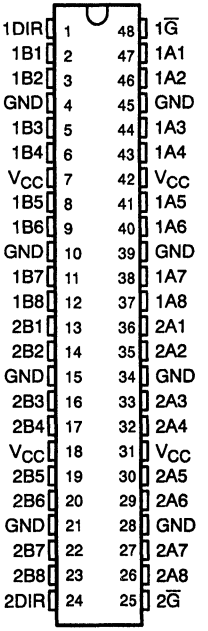
54AC16244 ... WD PACKAGE
74AC16244 ... DL PACKAGE
54ACT16244 ... WD PACKAGE
74ACT16244 ... DL PACKAGE
16-BIT BUS DRIVERS
(TOP VIEW)



54AC16245 ... WD PACKAGE
74AC16245 ... DL PACKAGE
16-BIT BUS TRANSCEIVERS
(TOP VIEW)

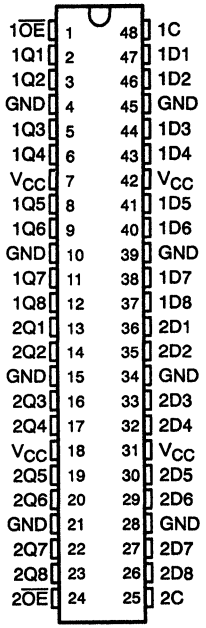


54ACT16245 ... WD PACKAGE
74ACT16245 ... DL PACKAGE
16-BIT BUS TRANSCEIVERS
(TOP VIEW)

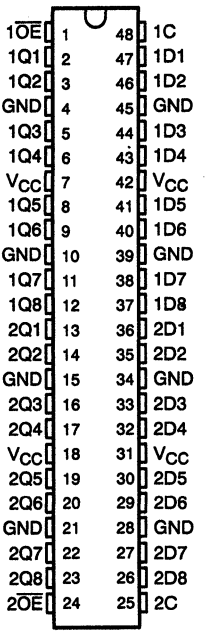


WIDE BUS™ PINOUTS (continued)

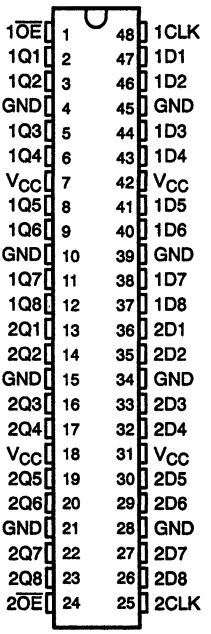
54AC16373 ... WD PACKAGE
74AC16373 ... DL PACKAGE
16-BIT D-TYPE LATCHES
(TOP VIEW)



54ACT16373 ... WD PACKAGE
74ACT16373 ... DL PACKAGE
16-BIT D-TYPE LATCHES
(TOP VIEW)



54AC16374 ... WD PACKAGE
74AC16374 ... DL PACKAGE
16-BIT D-TYPE FLIP-FLOPS
(TOP VIEW)



TEXAS INSTRUMENTS
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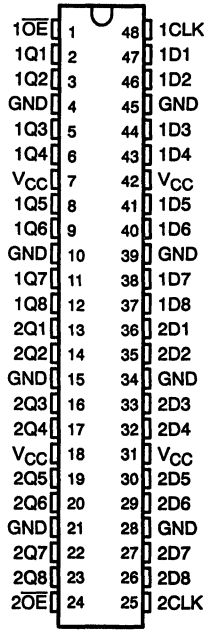
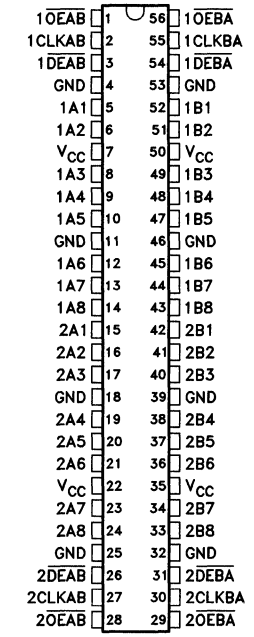
WIDE BUS™ PINOUTS (continued)

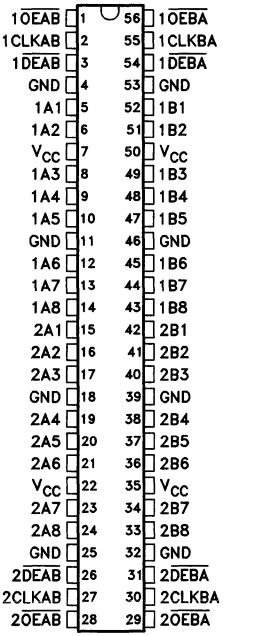
54ACT16374 ... WD PACKAGE
74ACT16374 ... DL PACKAGE
16-BIT D-TYPE FLIP-FLOPS
(TOP VIEW)



54AC16470, 54ACT16470 ...
WD PACKAGE
74AC16470, 74ACT16470 ...
DL PACKAGE
16-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)

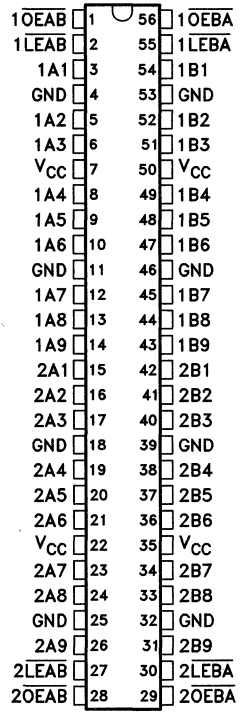


54AC16471, 54ACT16471 ...
WD PACKAGE
74AC16471, 74ACT16471 ...
DL PACKAGE
16-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)

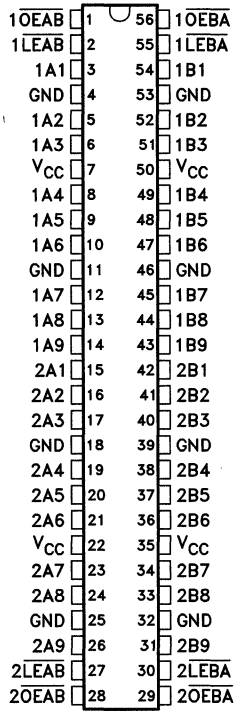


WIDE BUS™ PINOUTS (continued)

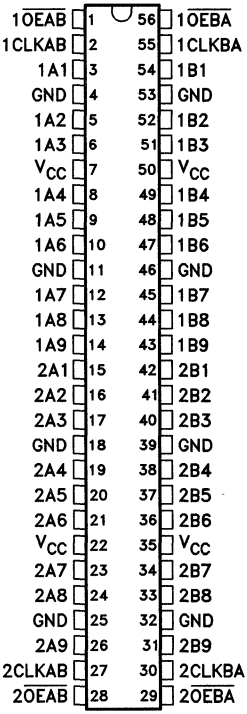
54AC16472, 54ACT16472 ...
WD PACKAGE
74AC16472, 74ACT16472 ...
DL PACKAGE
18-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)



54AC16473, 54ACT16473 ...
WD PACKAGE
74AC16473, 74ACT16473 ...
DL PACKAGE
18-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)

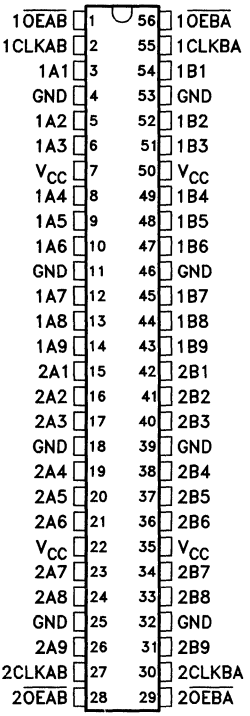


54AC16474, 54ACT16474 ...
WD PACKAGE
74AC16474, 74ACT16474 ...
DL PACKAGE
18-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)

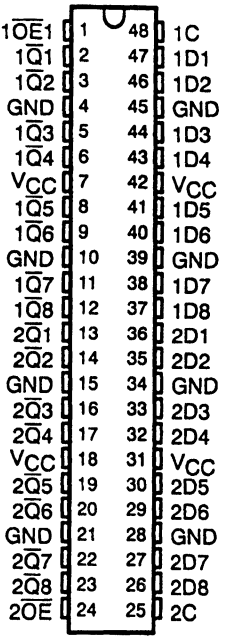


WIDE BUS™ PINOUTS (continued)

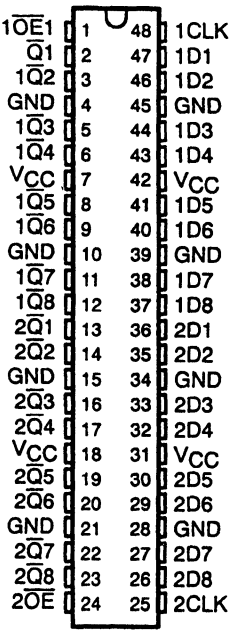
54AC16475, 54ACT16475 ...
WD PACKAGE
74AC16475, 74ACT16475 ...
DL PACKAGE
18-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)



'AC16533, 'ACT16533
16-BIT D-TYPE LATCHES
(TOP VIEW)

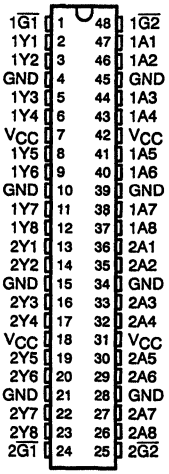


'AC16534, 'ACT16534
16-BIT D-TYPE FLIP-FLOPS
(TOP VIEW)

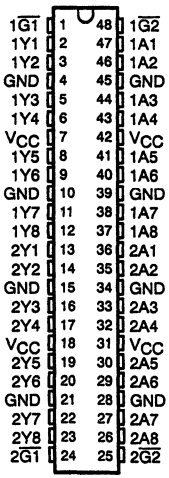


WIDE BUS™ PINOUTS (continued)

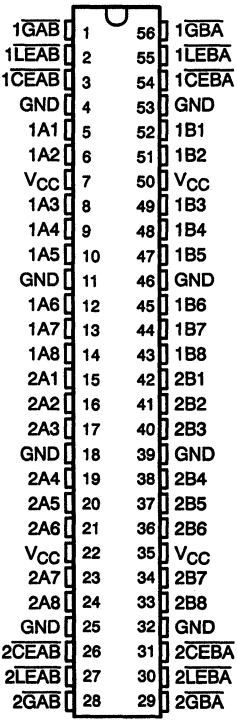
'AC16540, 'ACT16540
16-BIT BUS DRIVERS
(TOP VIEW)



'AC16541, 'ACT16541
16-BIT BUS DRIVERS
(TOP VIEW)



54AC16543 . . . WD PACKAGE
74AC16543 . . . DL PACKAGE
16-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)



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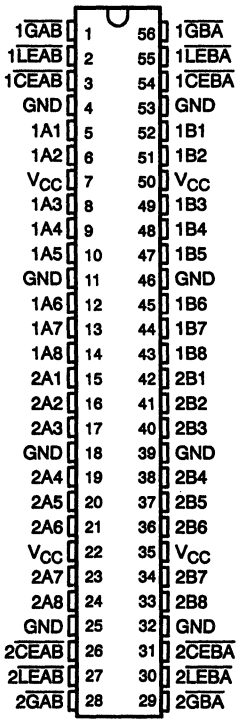
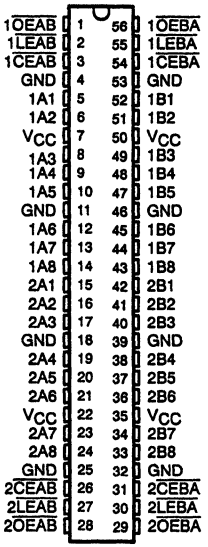
WIDE BUS™ PINOUTS (continued)

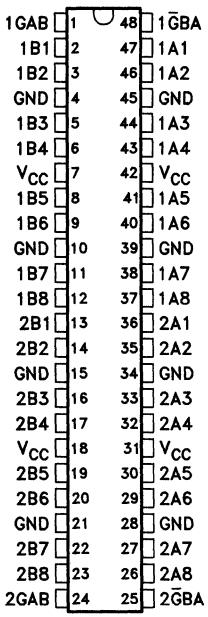
54ACT16543 ... WD PACKAGE
74ACT16543 ... DL PACKAGE
16-BIT REGISTERED TRANSSCEIVERS
(TOP VIEW)



'AC16544, 'ACT16544
16-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)

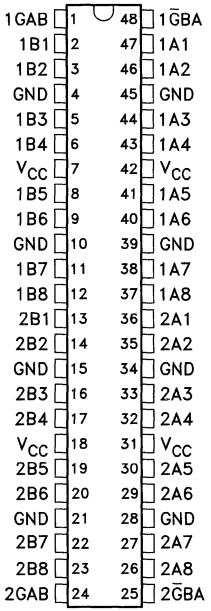


54ACT16620 ... WD PACKAGE
74ACT16620 ... DL PACKAGE
16-BIT BUS TRANSCEIVERS
(TOP VIEW)

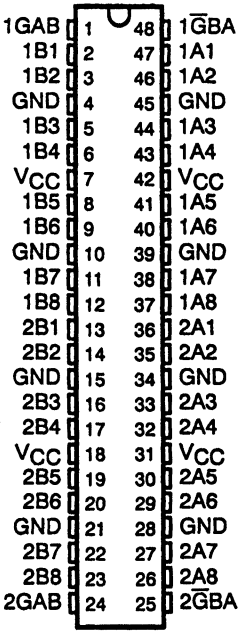


WIDE BUS™ PINOUTS (continued)

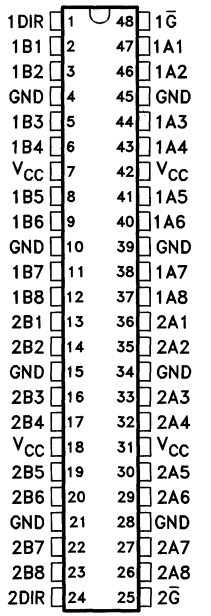
54AC16620 ... WD PACKAGE
74AC16620 ... DL PACKAGE
16-BIT BUS TRANSCEIVERS
(TOP VIEW)



'AC16623, 'ACT16623
16-BIT BUS TRANSCEIVERS
(TOP VIEW)



54AC16640 ... WD PACKAGE
74AC16640 ... DL PACKAGE
16-BIT BUS TRANSCEIVERS
(TOP VIEW)



TEXAS INSTRUMENTS
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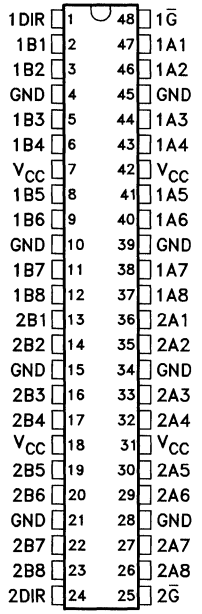
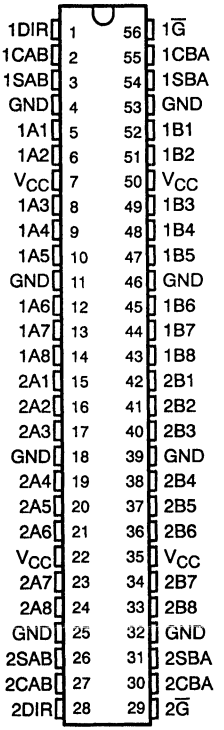
WIDE BUS™ PINOUTS (continued)

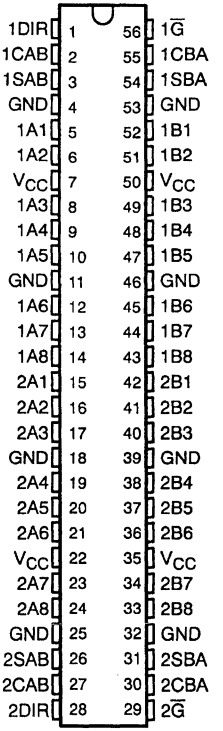
54ACT16640 ... WD PACKAGE
74ACT16640 ... DL PACKAGE
16-BIT BUS TRANSCEIVERS
(TOP VIEW)



54AC16646 ... WD PACKAGE
74AC16646 ... DL PACKAGE
16-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)

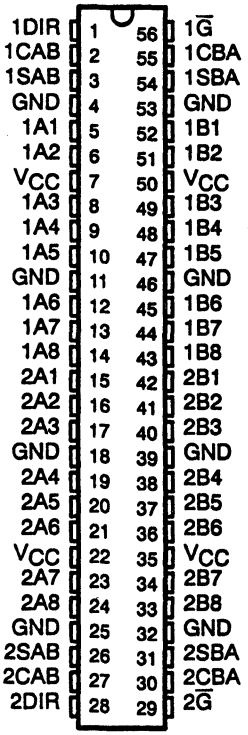


54ACT16646 ... WD PACKAGE
74ACT16646 ... DL PACKAGE
16-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)

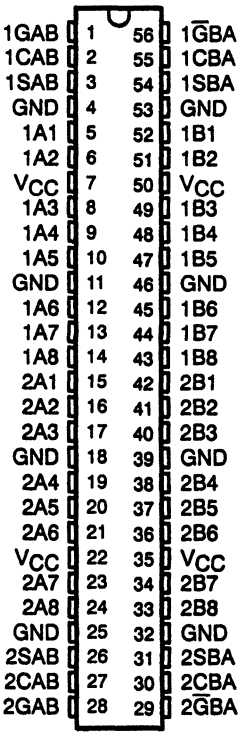


WIDE BUS™ PINOUTS (continued)

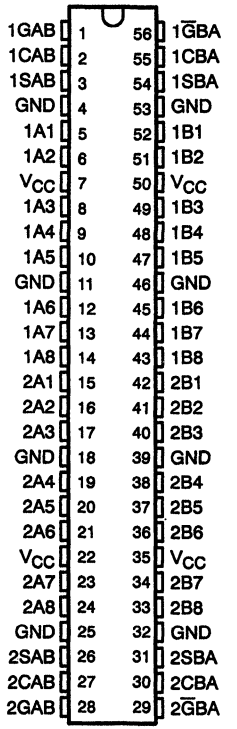
'AC16648, 'ACT16648
16-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)



'AC16651, 'ACT16651
16-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)



54AC16652 ... WD PACKAGE
74AC16652 ... DL PACKAGE
16-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)



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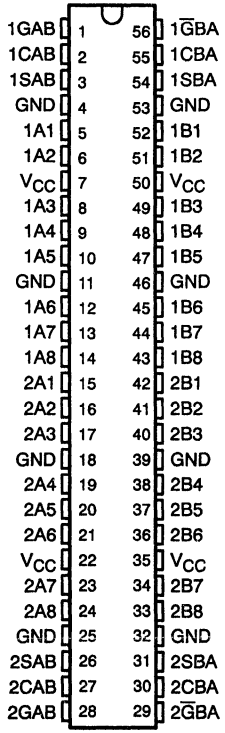
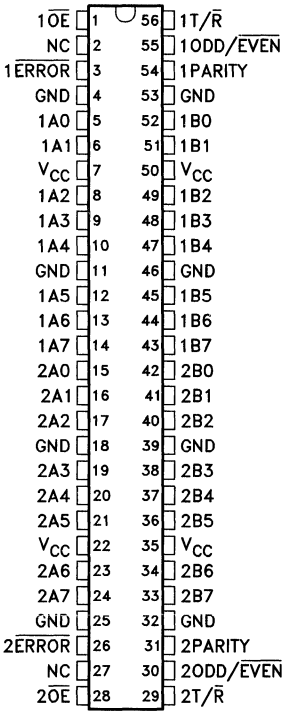
WIDE BUS™ PINOUTS (continued)

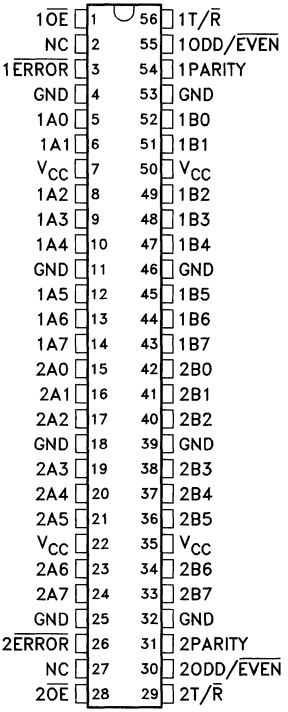
54ACT16652 ... WD PACKAGE
74ACT16652 ... DL PACKAGE
16-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)



54AC16657 ... WD PACKAGE
74AC16657 ... DL PACKAGE
16-BIT BUS TRANSCEIVERS
WITH PARITY
(TOP VIEW)

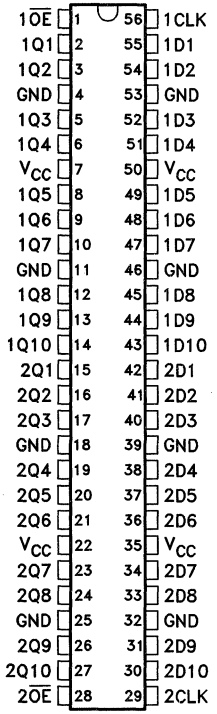


54ACT16657 ... WD PACKAGE
74ACT16657 ... DL PACKAGE
16-BIT BUS TRANSCEIVERS
WITH PARITY
(TOP VIEW)

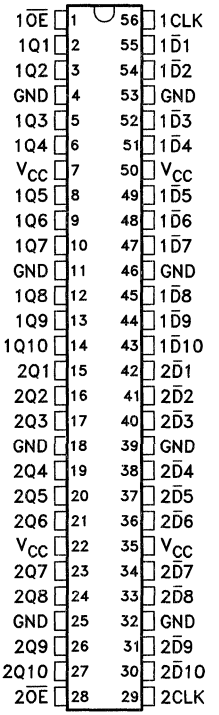


WIDE BUS™ PINOUTS (continued)

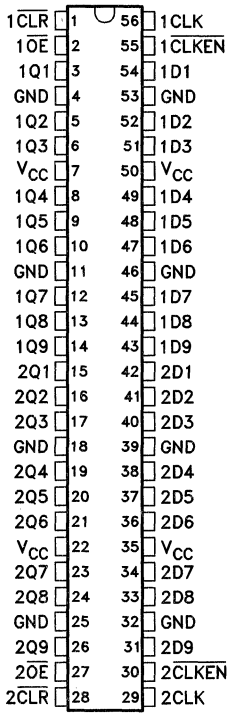
54AC16821, 54ACT16821 ...
WD PACKAGE
74AC16821, 74ACT16821 ...
DL PACKAGE
20-BIT D-TYPE FLIP-FLOPS
(TOP VIEW)



54AC16822, 54ACT16822 ...
WD PACKAGE
74AC16822, 74ACT16822 ...
DL PACKAGE
20-BIT D-TYPE FLIP-FLOPS
(TOP VIEW)

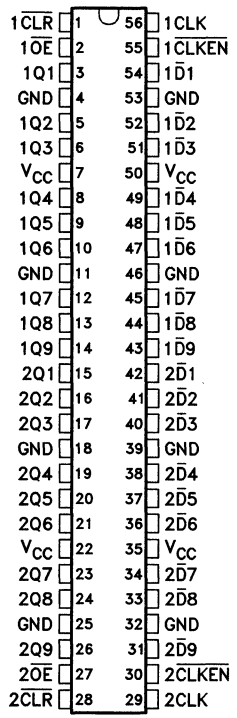


54AC16823, 54ACT16823 ...
WD PACKAGE
74AC16823, 74ACT16823 ...
DL PACKAGE
18-BIT D-TYPE FLIP-FLOPS
(TOP VIEW)

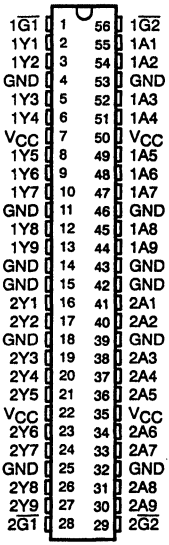


WIDE BUS™ PINOUTS (continued)

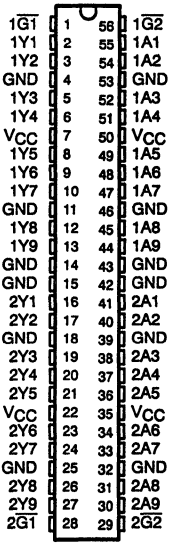
54AC16824, 54ACT16824 ...
WD PACKAGE
74AC16824, 74ACT16824 ...
DL PACKAGE
18-BIT D-TYPE FLIP-FLOPS
(TOP VIEW)



'AC16825, 'ACT16825
18-BIT BUS DRIVERS
(TOP VIEW)

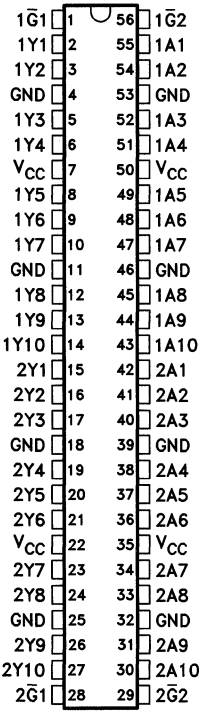


'AC16826, 'ACT16826
18-BIT BUS DRIVERS
(TOP VIEW)

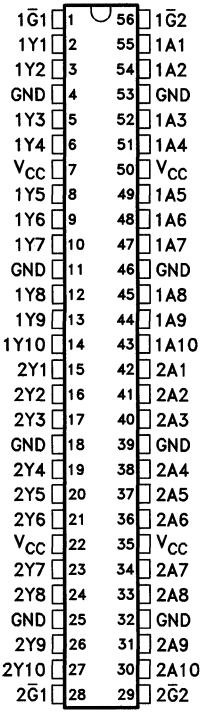


WIDE BUS™ PINOUTS (continued)

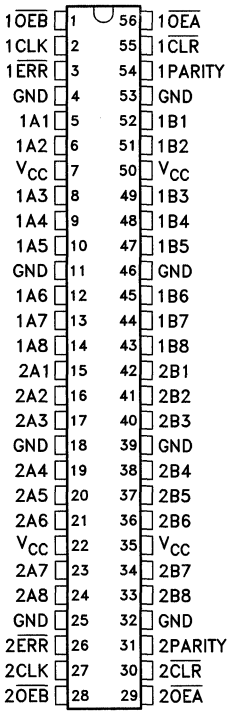
74AC/ACT16827 ... DL PACKAGE
54AC/ACT16827 ... WD PACKAGE
20-BIT BUS DRIVERS
(TOP VIEW)



74AC/ACT16828 ... DL PACKAGE
54AC/ACT16828 ... WD PACKAGE
20-BIT BUS DRIVERS
(TOP VIEW)

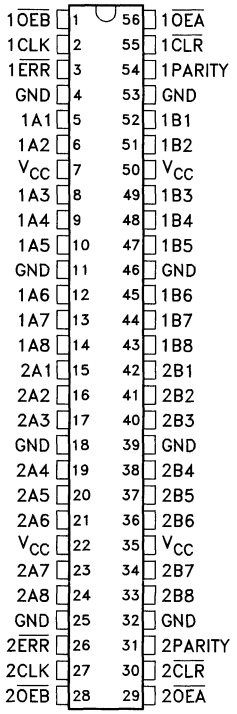


54AC16833, 54ACT16833 ...
WD PACKAGE
74AC16833, 74ACT16833 ...
DL PACKAGE
16-BIT BUS TRANSCEIVERS
WITH PARITY
(TOP VIEW)

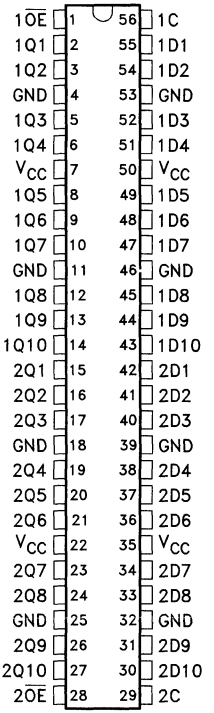


WIDE BUS™ PINOUTS (continued)

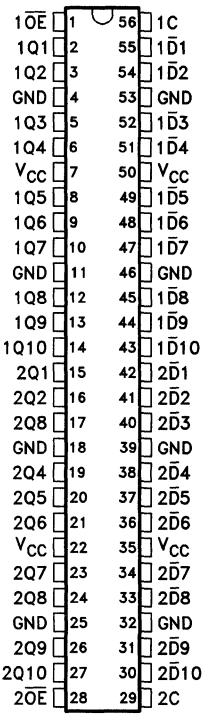
54AC16834, 54ACT16834 ...
WD PACKAGE
74AC16834, 74ACT16834 ...
DL PACKAGE
16-BIT BUS TRANSCEIVERS WITH PARITY
(TOP VIEW)



74AC/ACT16841 ... DL PACKAGE
54AC/ACT16841 ... WD PACKAGE
20-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)

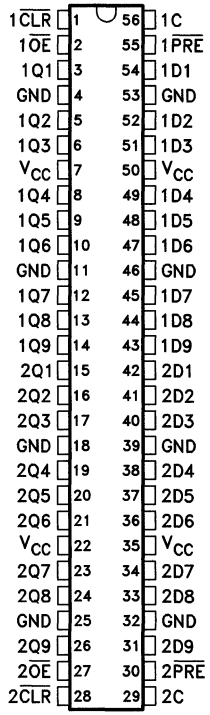


74AC/ACT16842 ... DL PACKAGE
54AC/ACT16842 ... WD PACKAGE
20-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)

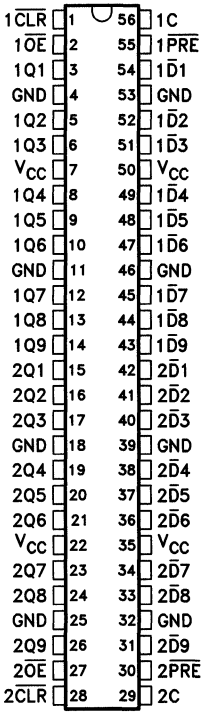


WIDE BUS™ PINOUTS (continued)

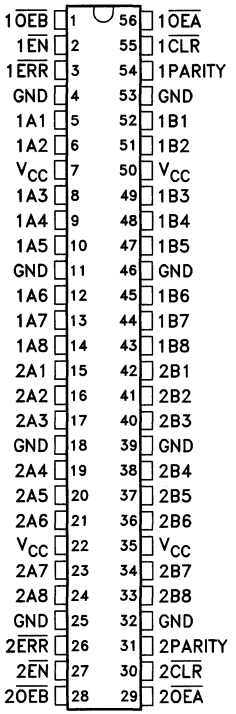
74AC/ACT16843 ... DL PACKAGE
54AC/ACT16843 ... WD PACKAGE
18-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



74AC/ACT16844 ... DL PACKAGE
54AC/ACT16844 ... WD PACKAGE
18-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)

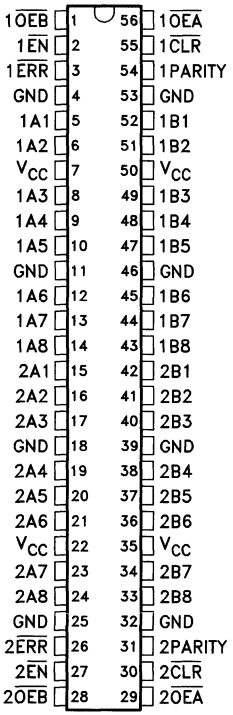


54AC16853, 54ACT16853 ...
WD PACKAGE
74AC16853, 74ACT16853 ...
DL PACKAGE
DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS
(TOP VIEW)

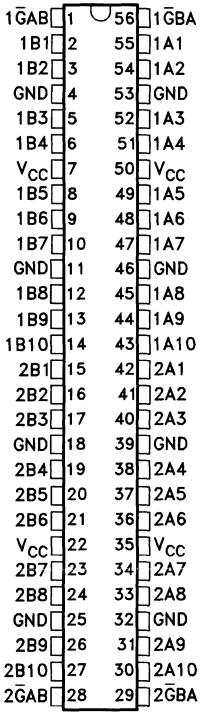


WIDE BUS™ PINOUTS (continued)

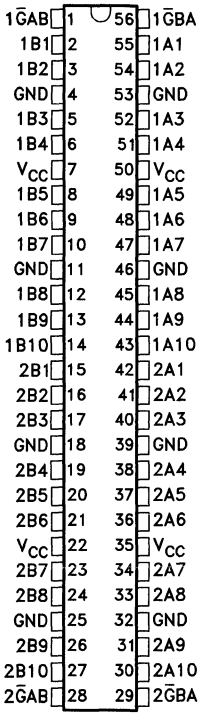
74AC/ACT16854 ... DL PACKAGE
54AC/ACT16854 ... WD PACKAGE
DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS
(TOP VIEW)



54AC16861, 54ACT16861 ...
WD PACKAGE
74AC16861, 74ACT16861 ...
DL PACKAGE
20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)

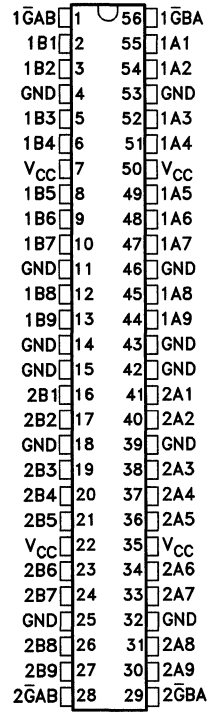


54AC16862, 54ACT16862 ...
WD PACKAGE
74AC16862, 74ACT16862 ...
DL PACKAGE
20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)

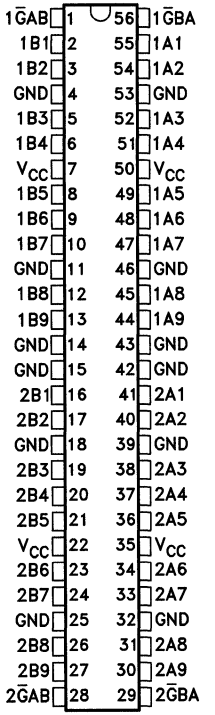


WIDE BUS™ PINOUTS (continued)

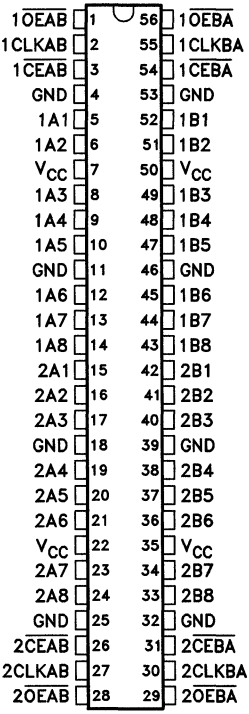
54AC16863, 54ACT16863 ...
WD PACKAGE
74AC16863, 74ACT16863 ...
DL PACKAGE
18-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



54AC16864, 54ACT16864 ...
WD PACKAGE
74AC16864, 74ACT16864 ...
DL PACKAGE
18-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)

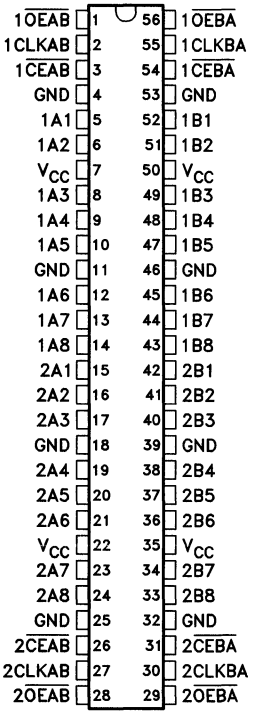


54AC16952, 54ACT16952 ...
WD PACKAGE
74AC16952, 74ACT16952 ...
DL PACKAGE
16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



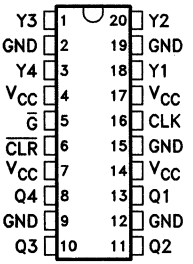
WIDE BUS™ PINOUTS (continued)

54AC16953, 54ACT16953 ...
WD PACKAGE
74AC16953, 74ACT16953 ...
DL PACKAGE
16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)

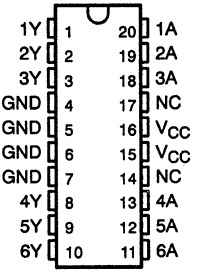


CLOCK DRIVERS

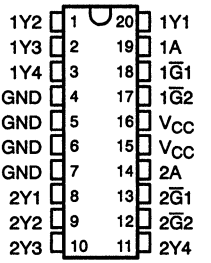
SN74ABT3337 ... DW OR N PACKAGE
CLOCK DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



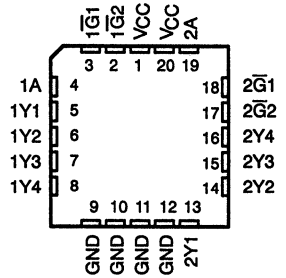
74AC11204 ... DW OR N PACKAGE
HEX INVERTERS/CLOCK DRIVERS
(TOP VIEW)



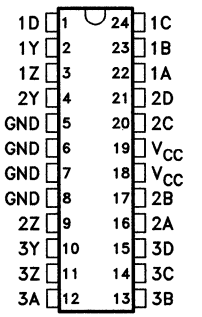
54AC/ACT11208 ... J PACKAGE
74AC/ACT11208 ... DW OR N PACKAGE
DUAL 1-LINE TO 4-LINE CLOCK DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



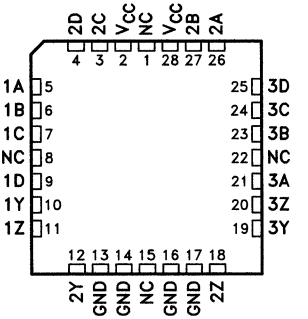
54AC/ACT11208 ... FK PACKAGE
DUAL 1-LINE TO 4-LINE CLOCK DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



54AC/ACT11800 ... JT PACKAGE
74AC/ACT11800 ... DW OR NT PACKAGE
TRIPLE 4-INPUT AND/NAND CLOCK DRIVERS
(TOP VIEW)



54AC/ACT11800 ... FK PACKAGE
TRIPLE 4-INPUT AND/NAND CLOCK DRIVERS
(TOP VIEW)



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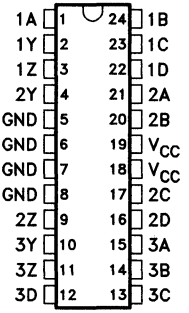
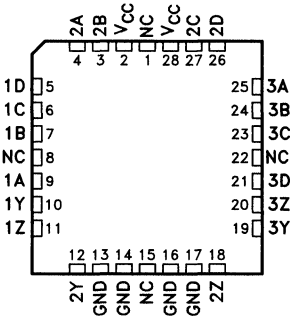
CLOCK DRIVERS (continued)

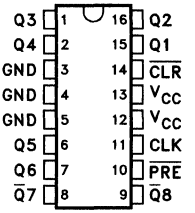
54AC/ACT11802 ... JT PACKAGE
74AC/ACT11802 ... DW OR NT PACKAGE
TRIPLE 4-INPUT OR/NOR CLOCK DRIVERS
(TOP VIEW)



54AC/ACT11802 ... FK PACKAGE
TRIPLE 4-INPUT OR/NOR CLOCK DRIVERS
(TOP VIEW)

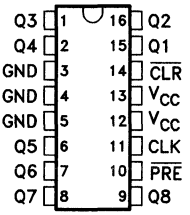


74AS303 ... D† OR N PACKAGE
OCTAL DIVIDE-BY-2 CIRCUITS/CLOCK DRIVERS
(TOP VIEW)

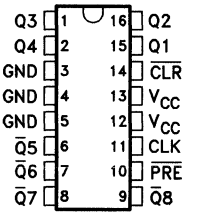


†CONTACT FACTORY FOR INFORMATION ON AVAILABILITY OF S.O. PACKAGE.

SN74AS304 ... D OR N PACKAGE
OCTAL DIVIDE-BY-2 CIRCUITS/CLOCK DRIVERS
(TOP VIEW)

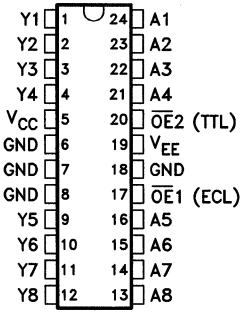


74AS305 ... D OR N PACKAGE
OCTAL DIVIDE-BY-2 CIRCUITS/CLOCK DRIVERS
(TOP VIEW)

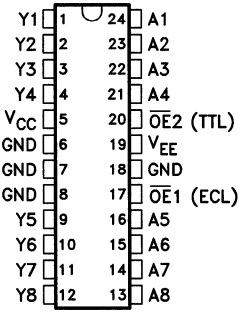


ECL

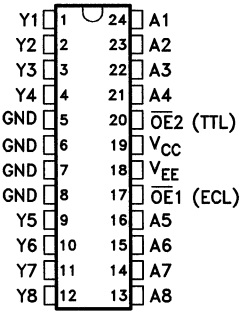
SN10KHT5538 ... DW OR NT PACKAGE
SN100KT5538 ... DW OR NT PACKAGE
OCTAL ECL-TO-TTL TRANSLATORS
WITH OPEN-COLLECTOR OUTPUTS
(TOP VIEW)



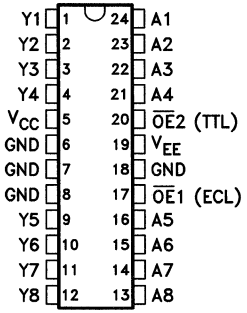
SN10KHT5539 ... DW OR NT PACKAGE
SN100KT5539 ... DW OR NT PACKAGE
OCTAL ECL-TO-TTL TRANSLATORS
WITH OPEN COLLECTOR OUTPUTS
(TOP VIEW)



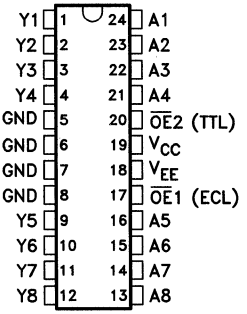
SN10KHT5540 ... DW OR NT PACKAGE
SN100KT5540 ... DW OR NT PACKAGE
OCTAL ECL-TO-TTL TRANSLATOR
WITH 3-STATE OUTPUTS
(TOP VIEW)



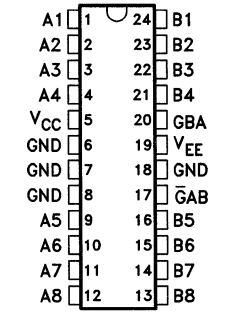
SN10KHT5541 ... DW OR NT PACKAGE
SN100KT5541 ... DW OR NT PACKAGE
OCTAL ECL-TO-TTL TRANSLATOR
WITH 3-STATE OUTPUTS
(TOP VIEW)



SN10KHT5542, SN10KHT5543 ...
DW OR NT PACKAGE
SN100KT5542, SN100KT5543 ...
DW OR NT PACKAGE
OCTAL TTL-TO-ECL TRANSLATORS
WITH OUTPUT ENABLE
(TOP VIEW)



SN10KHT5562, SN100KT5562 ...
DW OR NT PACKAGE
OCTAL TTL/ECL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
(TOP VIEW)



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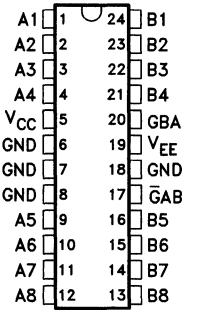
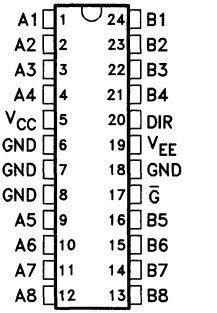
ECL (continued)

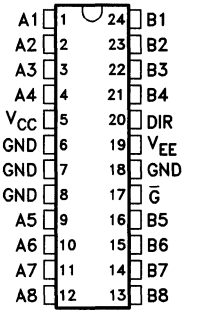
SN10KHT5563, SN100KT5563 ...
DW OR NT PACKAGE
OCTAL TTL/ECL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



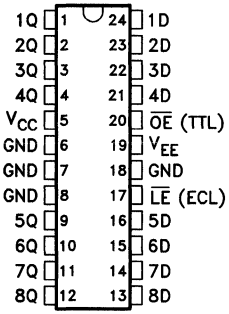
SN10KHT5564, SN100KT5564 ...
DW OR NT PACKAGE
OCTAL TTL/ECL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



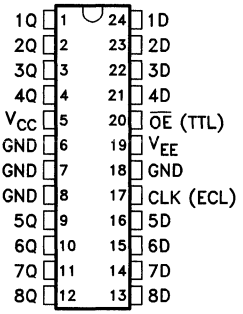
SN10KHT5565, SN100KT5565 ...
DW OR NT PACKAGE
OCTAL TTL/ECL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



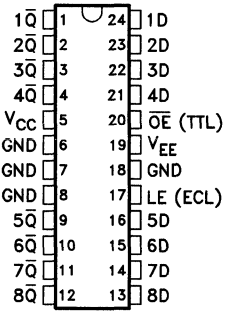
SN10KHT5573, SN100KT5573 ...
DW OR NT PACKAGE
OCTAL ECL-TO-TTL TRANSLATORS WITH D-TYPE TRANSPARENT LATCHES AND 3-STATE OUTPUTS
(TOP VIEW)



SN10KHT5574, SN100KT5574 ...
DW OR NT PACKAGE
OCTAL ECL-TO-TTL TRANSLATORS WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS
(TOP VIEW)

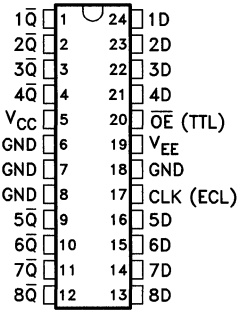


SN10KHT5575, SN100KT5575 ...
DW OR NT PACKAGE
OCTAL ECL-TO-TTL TRANSLATORS WITH D-TYPE TRANSPARENT LATCHES AND 3-STATE OUTPUTS
(TOP VIEW)

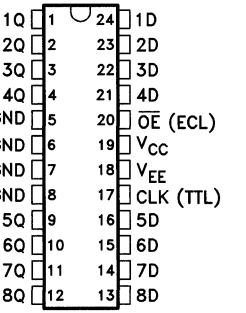


ECL (continued)

SN10KHT5576, SN100KT5576 ...
DW OR NT PACKAGE
OCTAL ECL-TO-TTL TRANSLATORS
WITH D-TYPE TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS
(TOP VIEW)

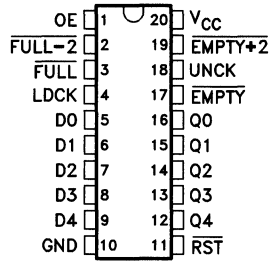


SN10KHT5578, SN100KT5578 ...
DW OR NT PACKAGE
OCTAL TTL-TO-ECL TRANSLATORS
WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND OUTPUT ENABLE
(TOP VIEW)

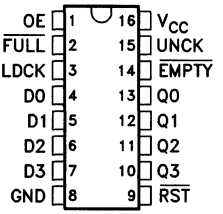


FIFO

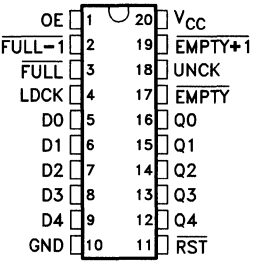
SN74ALS229B ... DW OR N PACKAGE
16 x 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES
(TOP VIEW)



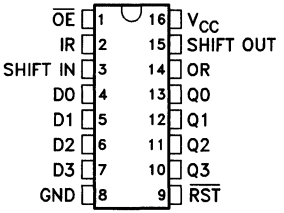
SN74ALS232B ... DW OR N PACKAGE
16 x 4 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY
(TOP VIEW)



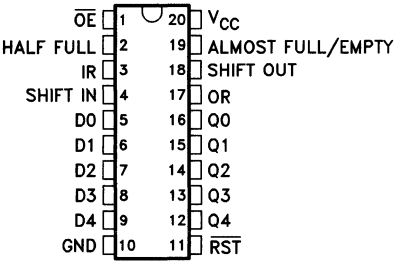
SN74ALS233B ... DW OR N PACKAGE
16 x 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES
(TOP VIEW)



SN54ALS234 ... J PACKAGE
SN74ALS234 ... DW OR N PACKAGE
64 x 4 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY
(TOP VIEW)

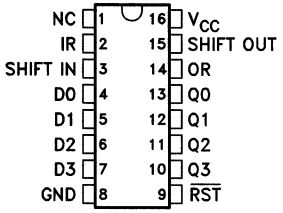


SN54ALS235 ... J PACKAGE
SN74ALS235 ... DW OR N PACKAGE
64 x 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY
(TOP VIEW)

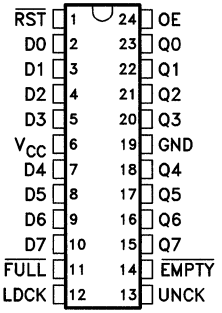


FIFO (continued)

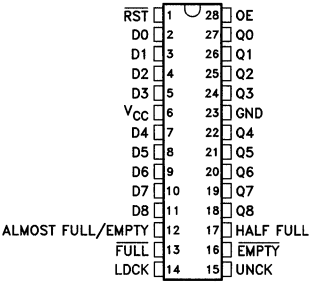
SN54ALS236 ... J PACKAGE
SN74ALS236 ... DW OR N PACKAGE
64 x 4 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY
(TOP VIEW)



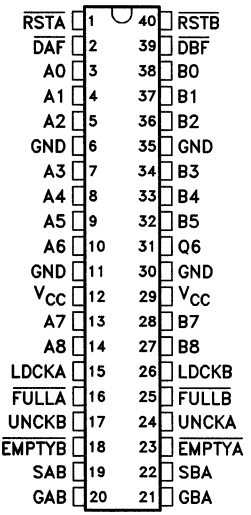
SN74ALS2232A ... NT PACKAGE
64 x 8 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY
(TOP VIEW)



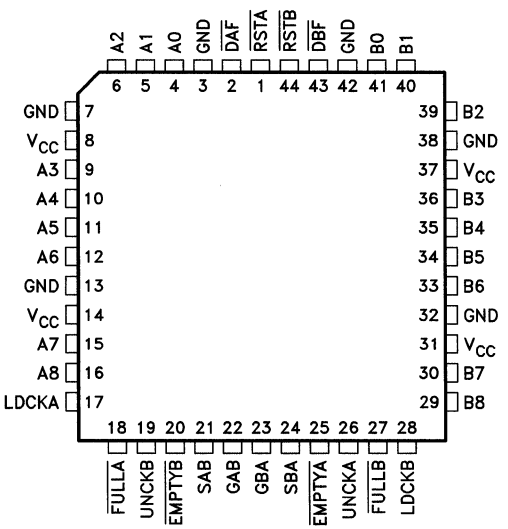
SN74ALS2233A ... N PACKAGE
64 x 9 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY
(TOP VIEW)



SN74ALS2238 ... N PACKAGE
32 x 9 x 2 ASYNCHRONOUS BIDIRECTIONAL FIRST-IN FIRST-OUT MEMORY
(TOP VIEW)

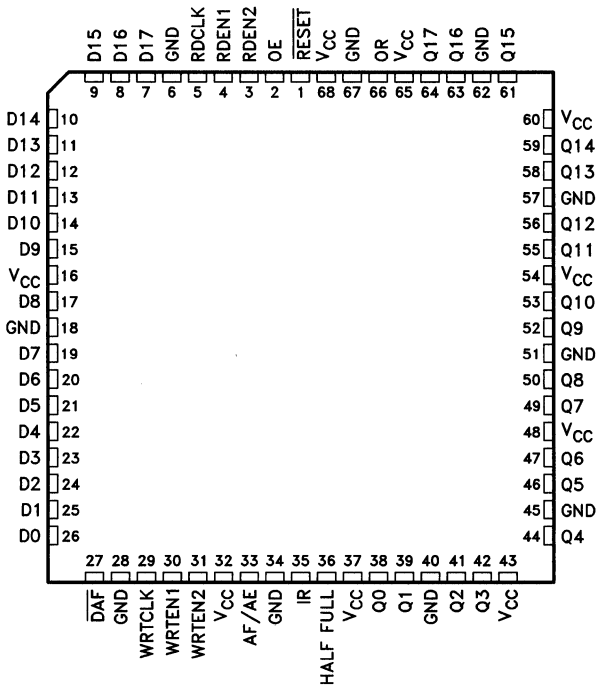


SN74ALS2238 ... FN PACKAGE
32 x 9 x 2 ASYNCHRONOUS BIDIRECTIONAL FIRST-IN FIRST-OUT MEMORY
(TOP VIEW)



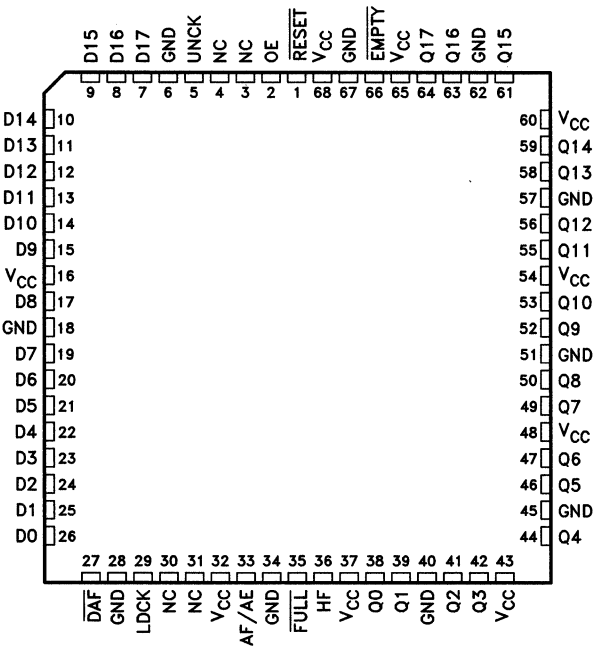
FIFO (continued)

SN74ACT7801 . . . FN PACKAGE
1024 x 18 ASYNCHRONOUS FIRST-IN-FIRST-OUT MEMORY
(TOP VIEW)



FIFO (continued)

SN74ACT7802 ... FN PACKAGE
1024 x 18 ASYNCHRONOUS FIRST-IN-FIRST-OUT MEMORY
(TOP VIEW)



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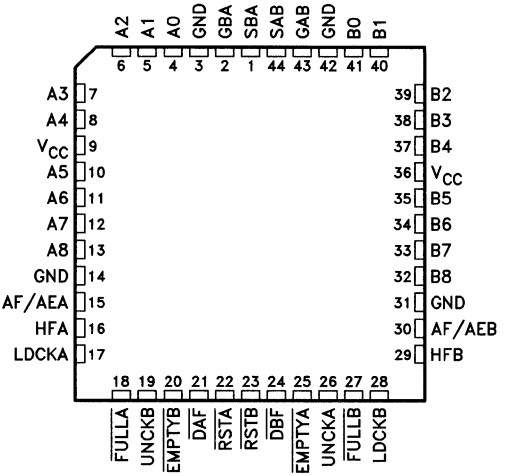
FIFO (continued)

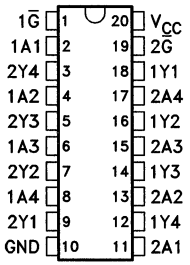
SN74ACT2235 ... FN PACKAGE
1024 x 9 x 2 ASYNCHRONOUS FIRST-IN-FIRST-OUT MEMORY
(TOP VIEW)



MEMORY DRIVERS

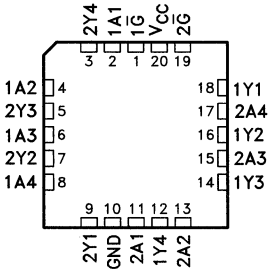
SN54ALS2240 ... J PACKAGE
SN74ALS2240 ... DW OR N PACKAGE

SN54ALS2241 ... J PACKAGE
SN74ALS2241 ... DW OR N PACKAGE
OCTAL BUFFERS AND LINE DRIVERS/ MOS DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)

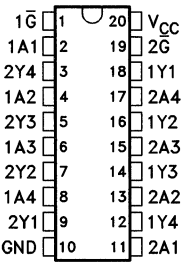


SN54ALS2240 ... FK PACKAGE

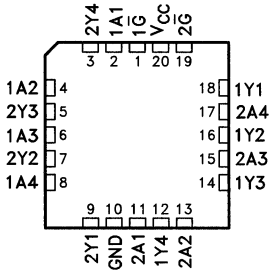
SN54ALS2241 ... J PACKAGE
SN74ALS2241 ... DW OR N PACKAGE
OCTAL BUFFERS AND LINE DRIVERS/ MOS DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



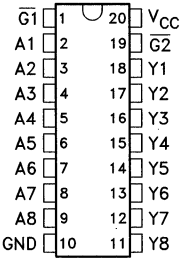
SN54ALS2244 ... J PACKAGE
SN74ALS2244 ... DW OR N PACKAGE
OCTAL BUFFERS AND LINE DRIVERS/ MOS DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



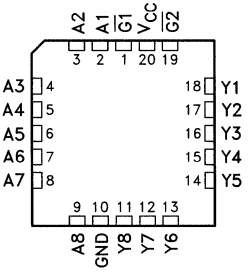
SN54ALS2244 ... FK PACKAGE
OCTAL BUFFERS AND LINE DRIVERS/ MOS DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



SN54ALS2540, SN54ALS2541 ... J PACKAGE
SN74ALS2540, SN74ALS2541 ... DW OR N PACKAGE
(TOP VIEW)



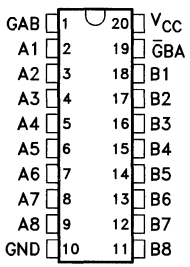
SN54ALS2540, SN54ALS2541 ... FK PACKAGE
(TOP VIEW)



MEMORY DRIVERS (continued)

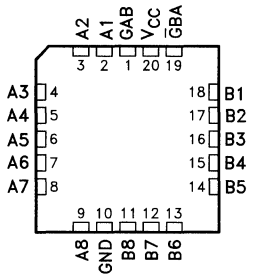
SN54AS2620, SN74AS2620
SN54AS2623, SN74AS2623
OCTAL BUS TRANSCEIVERS/MOS DRIVERS

SN54AS' ... J PACKAGE
SN74AS' ... DW OR N PACKAGE
(TOP VIEW)



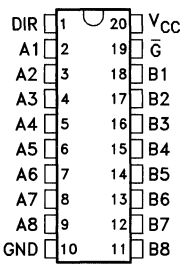
SN54AS2620, SN74AS2620
SN54AS2623, SN74AS2623
OCTAL BUS TRANSCEIVERS/MOS DRIVERS

SN54AS' ... FK PACKAGE
(TOP VIEW)



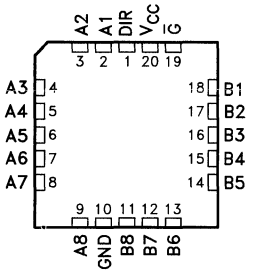
SN54AS2640, SN74AS2640
SN54AS2645, SN74AS2645
OCTAL BUS TRANSCEIVER/MOS DRIVER

SN54AS' ... J PACKAGE
SN74AS' ... DW OR N PACKAGE
(TOP VIEW)

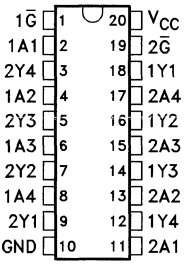


SN54AS2640, SN74AS2640
SN54AS2645, SN74AS2645
OCTAL BUS TRANSCEIVER/MOS DRIVER

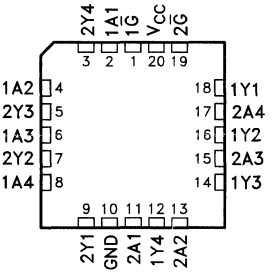
SN54AS' ... FK PACKAGE
(TOP VIEW)



SN54BCT2240 ... J PACKAGE
SN74BCT2240 ... DW OR N PACKAGE
OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)

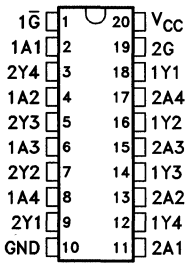


SN54BCT2240 ... FK PACKAGE
OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)

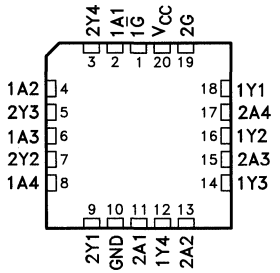


MEMORY DRIVERS (continued)

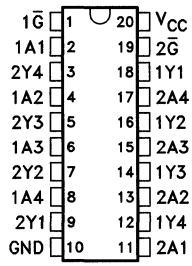
SN54BCT2241 ... J PACKAGE
SN74BCT2241 ... DW OR N PACKAGE
OCTAL BUFFERS AND LINE DRIVERS/ MOS DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



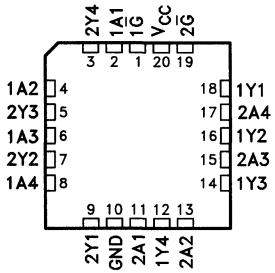
SN54BCT2241 ... FK PACKAGE
OCTAL BUFFERS AND LINE DRIVERS/ MOS DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



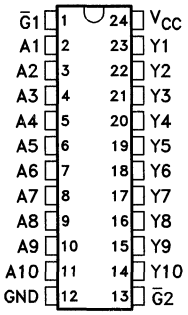
SN54BCT2244 ... J PACKAGE
SN74BCT2244 ... DW OR N PACKAGE
OCTAL BUFFERS AND LINE DRIVERS/ MOS DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



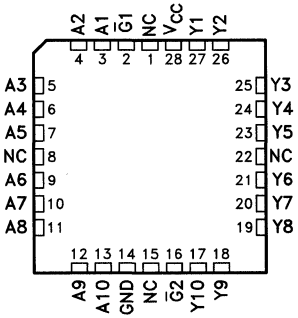
SN54BCT2244 ... FK PACKAGE
OCTAL BUFFERS AND LINE DRIVERS/ MOS DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



SN54BCT2827A, SN54BCT2828A ... JT PACKAGE
SN74BCT2827A, SN74BCT2828A ... DW OR N PACKAGE
8-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)

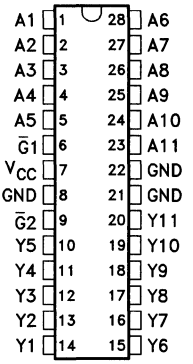


SN54BCT2827A, SN54BCT2828A ... FK PACKAGE
8-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)

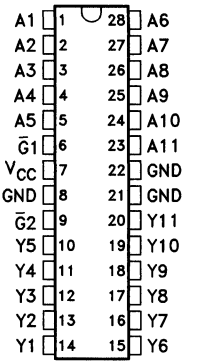


MEMORY DRIVERS (continued)

SN54BCT2410 ... JT PACKAGE
SN74BCT2410 ... NT PACKAGE
11-BIT MOS MEMORY DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)

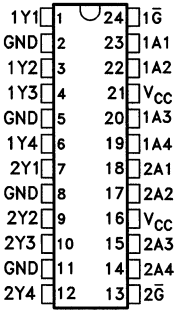


SN54BCT2411 ... JT PACKAGE
SN74BCT2411 ... NT PACKAGE
11-BIT MOS MEMORY DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)

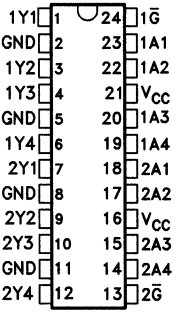


25-OHM LOW-IMPACT

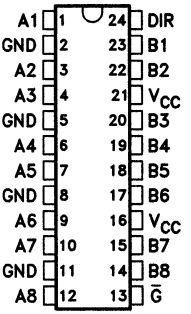
SN54BCT25240 ... JT PACKAGE
SN74BCT25240 ... NT PACKAGE
OCTAL 25-OHM LINE DRIVERS
WITH 3-STATE OUTPUTS
(TOP VIEW)



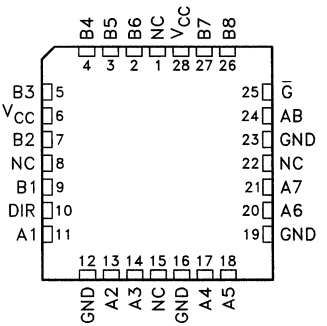
SN54BCT25244 ... JT PACKAGE
SN74BCT25244 ... NT PACKAGE
OCTAL 25-OHM LINE DRIVERS
WITH 3-STATE OUTPUTS
(TOP VIEW)



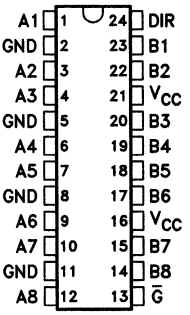
SN54BCT25245 ... JT PACKAGE
SN74BCT25245 ... DW or NT PACKAGE
25-OHM OCTAL BUS TRANSCEIVERS
(TOP VIEW)



SN54BCT25245 ... FK PACKAGE
25-OHM OCTAL BUS TRANSCEIVERS
(TOP VIEW)

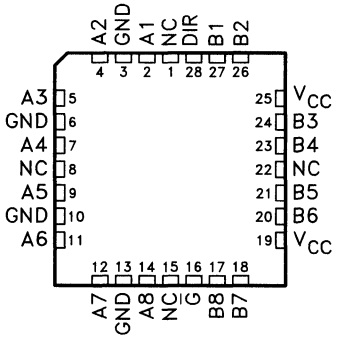


SN54BCT25641 ... JT PACKAGE
SN74BCT25641 ... DW OR NT PACKAGE
25-OHM OCTAL BUS TRANSCEIVERS
(TOP VIEW)

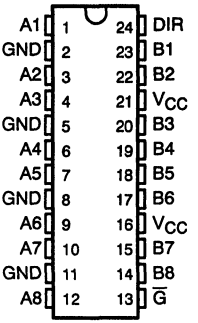


25-OHM LOW-IMPACT (continued)

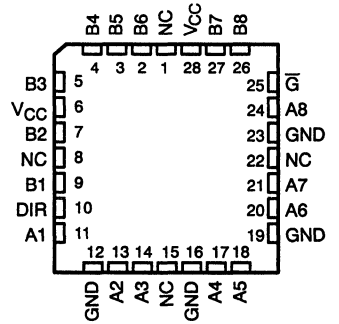
SN54BCT25641 ... FK PACKAGE
25-OHM OCTAL BUS TRANSCEIVERS
(TOP VIEW)



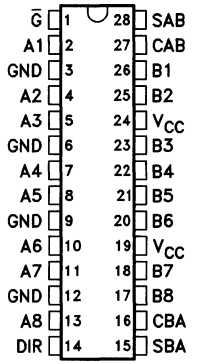
SN54BCT25642 ... JT PACKAGE
SN74BCT25642 ... DW OR NT PACKAGE
25-OHM OCTAL BUS TRANSCEIVERS
(TOP VIEW)



SN54BCT25642 ... FK PACKAGE
25-OHM OCTAL BUS TRANSCEIVERS
(TOP VIEW)

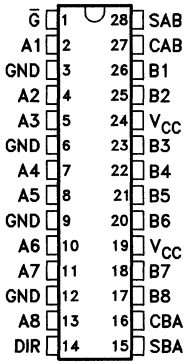


SN54BCT25646 ... JT PACKAGE
SN74BCT25646 ... NT PACKAGE
OCTAL 25-OHM REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)

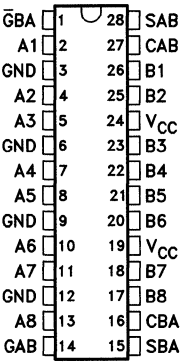


25-OHM LOW-IMPACT (continued)

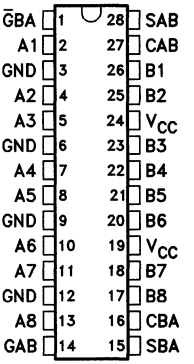
SN54BCT25648 ... JT PACKAGE
SN74BCT25648 ... NT PACKAGE
OCTAL 25-OHM REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



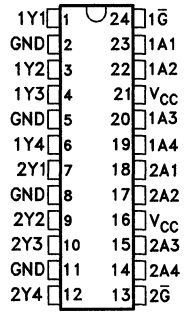
SN54BCT25651 ... JT PACKAGE
SN74BCT25651 ... NT PACKAGE
OCTAL 25-OHM REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



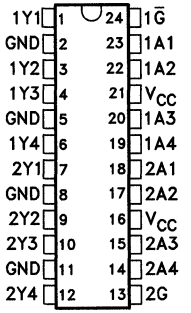
SN54BCT25652 ... JT PACKAGE
SN74BCT25652 ... NT PACKAGE
OCTAL 25-OHM REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



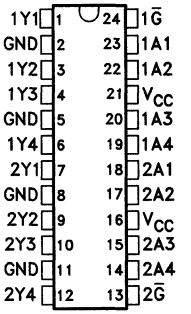
SN54BCT25756 ... JT PACKAGE
SN74BCT25756 ... NT PACKAGE
OCTAL 25-OHM LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS
(TOP VIEW)



SN54BCT25757 ... JT PACKAGE
SN74BCT25757 ... NT PACKAGE
OCTAL 25-OHM LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS
(TOP VIEW)



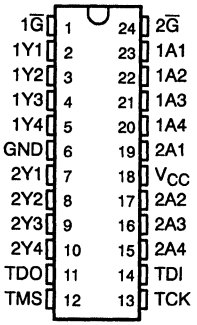
SN54BCT25760 ... JT PACKAGE
SN74BCT25760 ... NT PACKAGE
OCTAL 25-OHM LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS
(TOP VIEW)



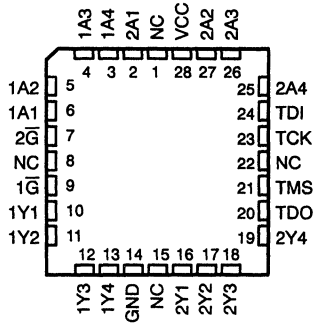
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SCOPE

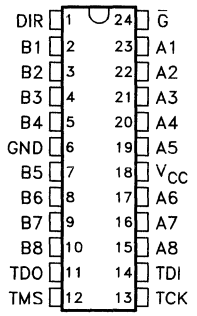
SN54BCT8244 ... JT PACKAGE
SN74BCT8244 ... DW OR NT PACKAGE
SCAN TEST DEVICE WITH OCTAL BUFFER
(TOP VIEW)



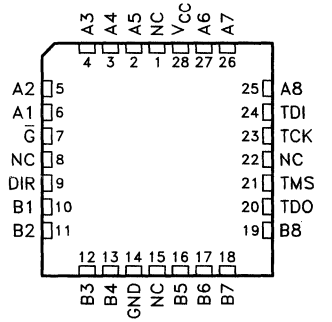
SN54BCT8244 ... FK PACKAGE
SCAN TEST DEVICE WITH OCTAL BUFFER
(TOP VIEW)



SN54BCT8245 ... JT PACKAGE
SN74BCT8245 ... DW OR NT PACKAGE
SCAN TEST DEVICE WITH OCTAL BUS TRANSCEIVER
(TOP VIEW)

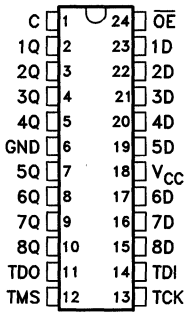


SN54BCT8245 ... FK PACKAGE
SCAN TEST DEVICE WITH OCTAL BUS TRANSCEIVER
(TOP VIEW)

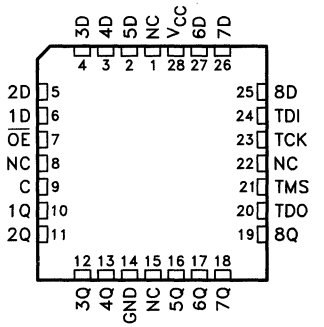


SCOPE (continued)

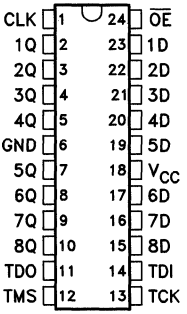
SN54BCT8373 ... JT PACKAGE
SN74BCT8373 ... DW OR NT PACKAGE
SCAN TEST DEVICES WITH OCTAL D-TYPE LATCHES
(TOP VIEW)



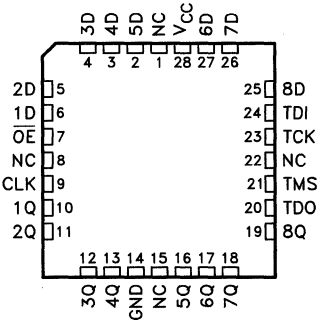
SN54BCT8373 ... FK PACKAGE
SCAN TEST DEVICES WITH OCTAL D-TYPE LATCHES
(TOP VIEW)



SN54BCT8374 ... JT PACKAGE
SN74BCT8374 ... DW OR NT PACKAGE
SCAN TEST DEVICES WITH OCTAL
D-TYPE EDGE-TRIGGERED FLIP-FLOPS
(TOP VIEW)

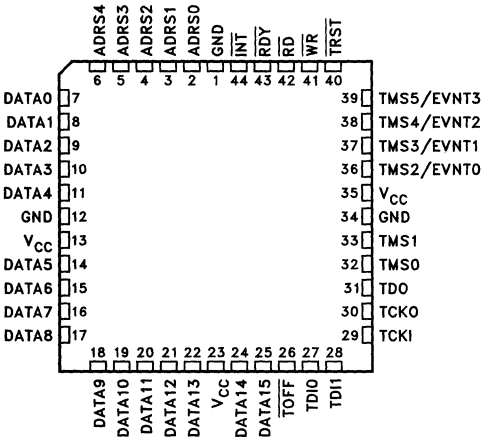


SN54BCT8374 ... FK PACKAGE
SCAN TEST DEVICES WITH OCTAL
D-TYPE EDGE-TRIGGERED FLIP-FLOPS
(TOP VIEW)

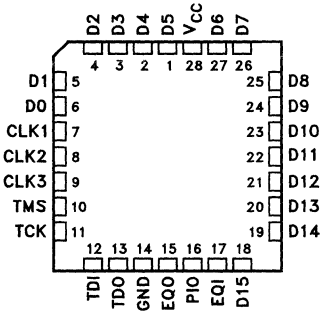


SCOPE (continued)

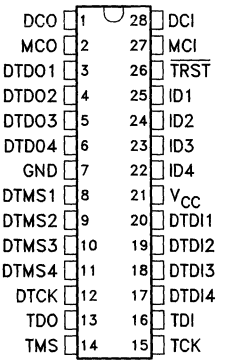
54ACT8990 ... FJ PACKAGE
74ACT8990 ... FN PACKAGE
TEST BUS CONTROLLERS
(TOP VIEW)



SN54ACT8994 ... FK PACKAGE
SN74ACT8994 ... FN PACKAGE
DIGITAL BUS MONITORS
(TOP VIEW)

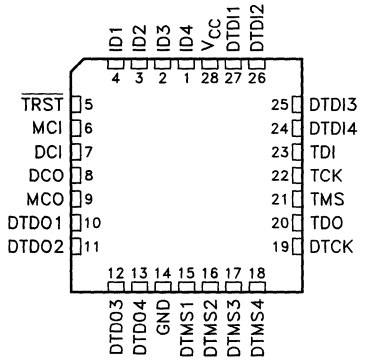


54ACT8997 ... JT PACKAGE
74ACT8997 ... DW OR NT PACKAGE
SCAN PATH LINKER WITH 4-BIT IDENTIFICATION BUSES
(TOP VIEW)

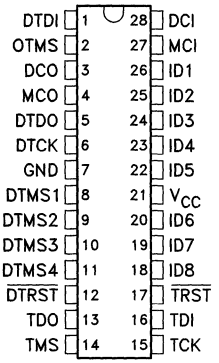


SCOPE (continued)

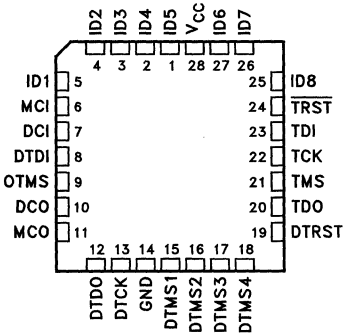
54ACT8997 ... FK PACKAGE
SCAN PATH LINKER WITH 4-BIT IDENTIFICATION BUSES
(TOP VIEW)



54ACT8999 ... JT PACKAGE
74ACT899 ... DW OR NT PACKAGE
SCAN PATH SELECTORS WITH 8-BIT BIDIRECTIONAL DATA BUS
(TOP VIEW)



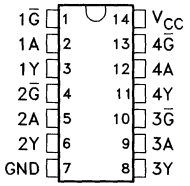
54ACT8999 ... FK PACKAGE
SCAN PATH SELECTORS WITH 8-BIT BIDIRECTIONAL DATA BUSES
(TOP VIEW)



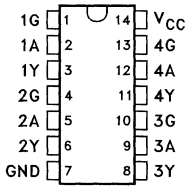
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

64BCT

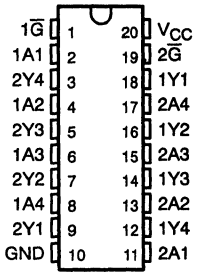
SN64BCT125 ... D or N PACKAGE
QUADRUPLE BUS BUFFER GATES
WITH 3-STATE OUTPUTS
(TOP VIEW)



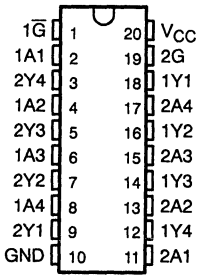
SN64BCT126 ... D or N PACKAGE
QUADRUPLE BUS BUFFER GATES
WITH 3-STATE OUTPUTS
(TOP VIEW)



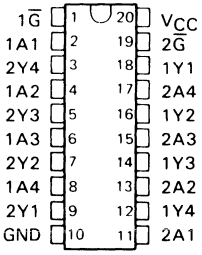
SN64BCT240 ... DW OR N PACKAGE
OCTAL BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS
(TOP VIEW)



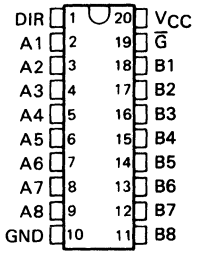
SN64BCT241 ... DW OR N PACKAGE
OCTAL BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS
(TOP VIEW)



SN64BCT244 ... DW OR N PACKAGE
OCTAL BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS
(TOP VIEW)

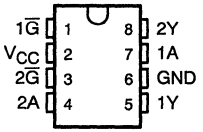


SN64BCT245 ... DW OR N PACKAGE
OCTAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
(TOP VIEW)

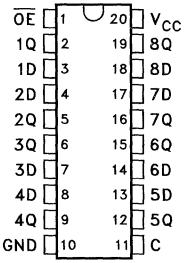


64BCT (continued)

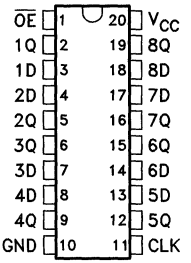
SN64BCT306 ... D OR P PACKAGE
DUAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



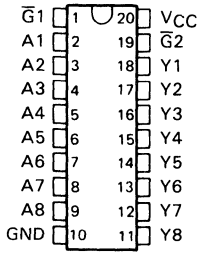
SN64BCT373 ... DW OR N PACKAGE
OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUTS
(TOP VIEW)



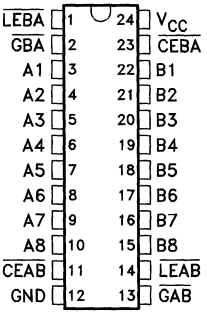
SN64BCT374 ... DW OR N PACKAGE
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUTS
(TOP VIEW)



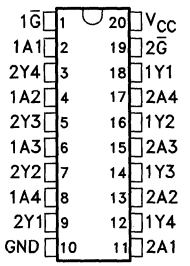
SN64BCT541 ... DW OR N PACKAGE
OCTAL BUFFER AND LINE DRIVER WITH 3-STATE OUTPUTS
(TOP VIEW)



SN64BCT543 ... JT OR NT PACKAGE
OCTAL REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS
(TOP VIEW)

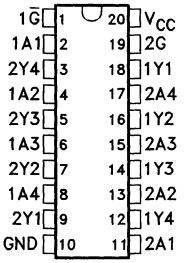


SN64BCT2240 ... DW OR N PACKAGE
OCTAL BUFFER/MOS DRIVER WITH 3-STATE OUTPUTS
(TOP VIEW)

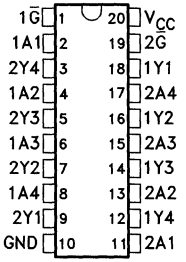


64BCT (continued)

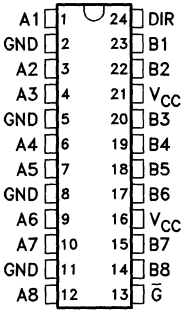
SN64BCT2241 ... DW OR N PACKAGE
OCTAL BUFFER/MOS DRIVER
WITH 3-STATE OUTPUTS
(TOP VIEW)



SN64BCT2244 ... J OR N PACKAGE
OCTAL BUFFER/MOS DRIVER
WITH 3-STATE OUTPUTS
(TOP VIEW)

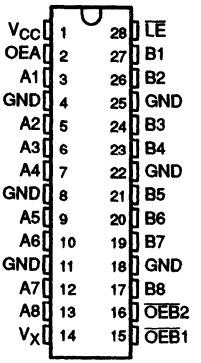


SN64BCT25245 ... DW or NT PACKAGE
25-OHM OCTAL BUS TRANSCEIVER
(TOP VIEW)

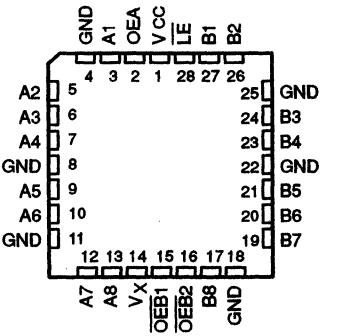


BTL TRANSCEIVERS

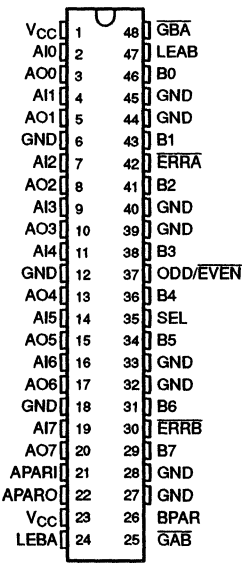
SN54F776 ... JT PACKAGE
SN74F776 ... DW OR NT PACKAGE
PI-BUS OCTAL BIDIRECTIONAL LATCHED TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS
(TOP VIEW)



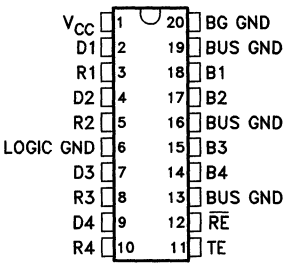
SN54F776 ... FK PACKAGE
PI-BUS OCTAL BIDIRECTIONAL LATCHED TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS
(TOP VIEW)



SN54BCT979 ... WD PACKAGE
SN74BCT979 ... DL PACKAGE
9-BIT REGISTERED BTL TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS
(TOP VIEW)



SN75ALS053 ... N PACKAGE
QUAD FUTUREBUS TRANSCEIVER
(TOP VIEW)



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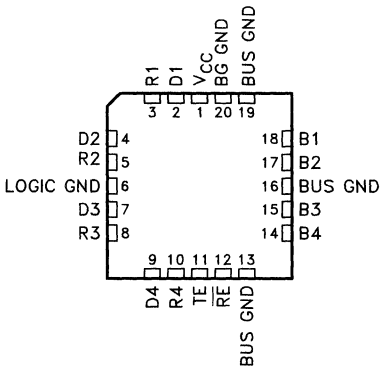
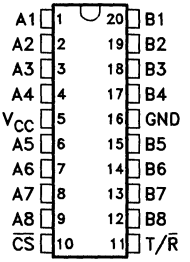
BTL TRANSCEIVERS (continued)

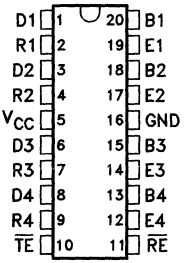
SN75ALS053 ... FN CHIP CARRIER PACKAGE
QUAD FUTUREBUS TRANSCEIVER
(TOP VIEW)



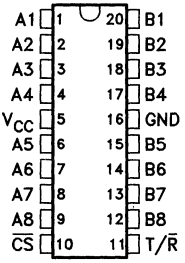
SN75ALS056 ... DW OR N PACKAGE
TRAPEZOIDAL-WAVEFORM INTERFACE
BUS TRANSCEIVERS
(TOP VIEW)



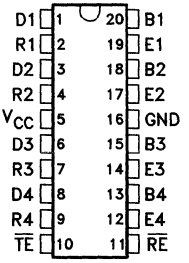
SN75ALS057 ... DW OR N PACKAGE
TRAPEZOIDAL-WAVEFORM INTERFACE
BUS TRANSCEIVERS
(TOP VIEW)



SN55ALS056 ... J OR W PACKAGE
TRAPEZOIDAL-WAVEFORM INTERFACE
BUS TRANSCEIVERS
(TOP VIEW)

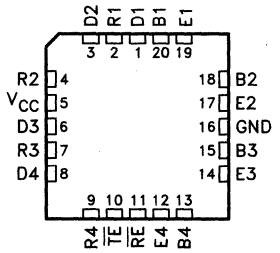


SN55ALS057 ... J OR W PACKAGE
TRAPEZOIDAL-WAVEFORM INTERFACE
BUS TRANSCEIVERS
(TOP VIEW)

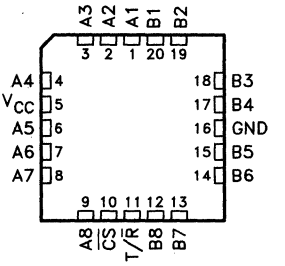


BTL TRANSCEIVERS (continued)

SN55ALS056 ... FK PACKAGE
TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVERS
(TOP VIEW)

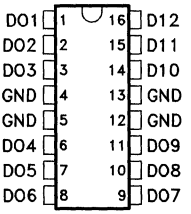


SN55ALS057 ... FK PACKAGE
TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVERS
(TOP VIEW)

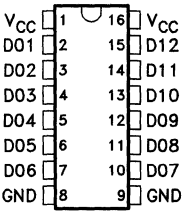


BTA

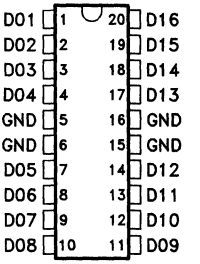
SN74S1050 ... D OR N PACKAGE
12-BIT SCHOTTKY BARRIER DIODE
BUS TERMINATION ARRAY
(TOP VIEW)



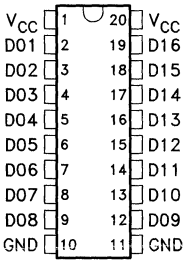
SN74S1051 ... D OR N PACKAGE
12-BIT SCHOTTKY BARRIER DIODE
BUS TERMINATION ARRAYS
(TOP VIEW)



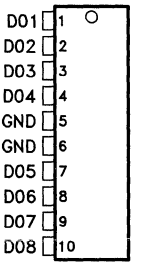
SN74S1052 ... DW OR N PACKAGE
16-BIT SCHOTTKY BARRIER DIODE
BUS TERMINATION ARRAY
(TOP VIEW)



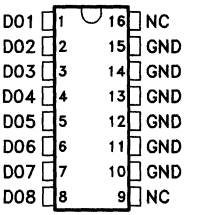
SN74S1053 ... DW OR N PACKAGE
16-BIT SCHOTTKY BARRIER DIODE
BUS TERMINATION ARRAYS
(TOP VIEW)



SN74S1056 ... SC PACKAGE
8-BIT SCHOTTKY BARRIER DIODE BUS
TERMINATION ARRAYS
(TOP VIEW)



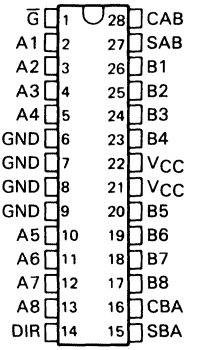
SN74S1056 ... D PACKAGE
8-BIT SCHOTTKY BARRIER DIODE BUS
TERMINATION ARRAYS
(TOP VIEW)



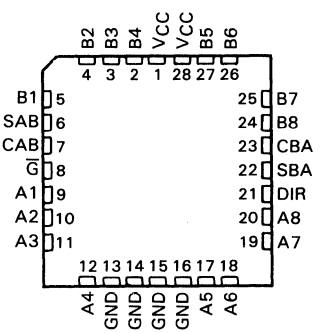
2 ACL LSI Products

- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic DIPs**

54AC11646 . . . JT PACKAGE
74AC11646 . . . DW OR NW PACKAGE
(TOP VIEW)



54AC11646 . . . FK PACKAGE
(TOP VIEW)



description

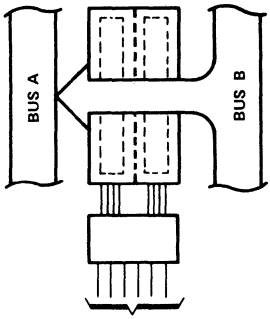
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry with 3-state outputs arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

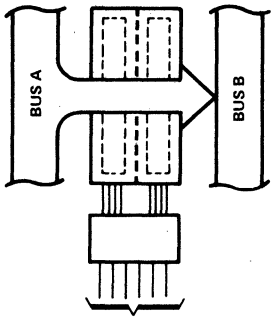
The 54AC11646 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11646 is characterized for operation from −40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.



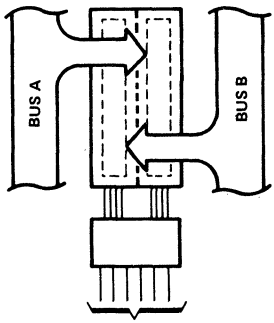
1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



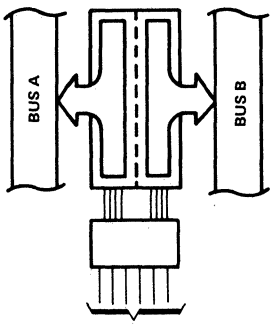
1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	HorL	X	H
L	H	HorL	X	H	X

TRANSFER
STORED DATA
TO A OR B

Pin numbers shown are for DW, JT, and NW packages.

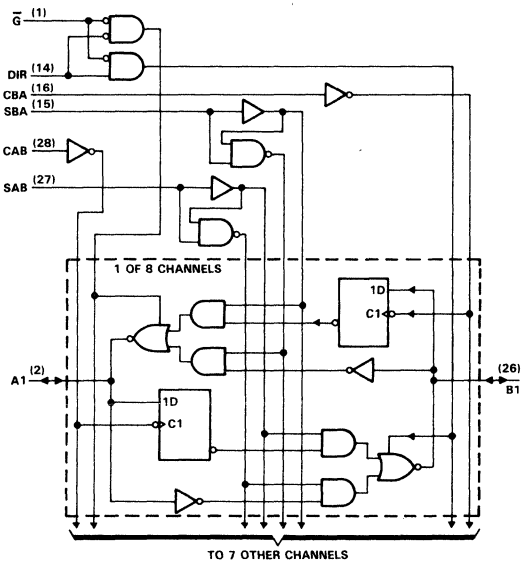
FIGURE 1. BUS-MANAGEMENT FUNCTIONS

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

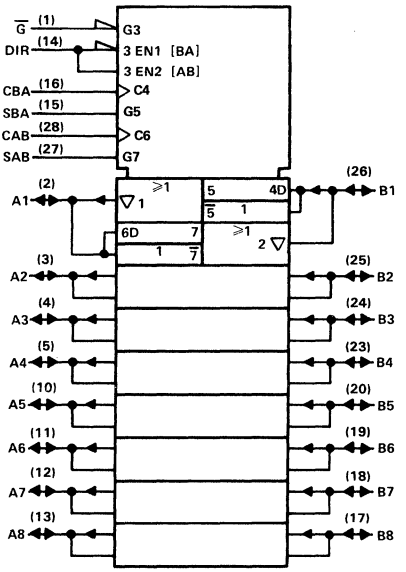
† The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagram (positive logic)



Pin numbers shown are for DW, JT, and NW packages.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11646			74AC11646			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Input voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11646		74AC11646		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	A or B ports	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	Control pins	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	$\overline{G}$ or DIR	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements, V_{CC} = 3.3 V ± 0.3 V (see Note 2)

		T_A = 25°C		54AC11646		74AC11646		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	65	0	65	0	65	MHz
t_w	Pulse duration, CAB or CBA high or low	7.7		7.7		7.7		ns
t_{su}	Setup time, A before CABt or B before CBAt	6.5		6.5		6.5		ns
t_h	Hold time, A after CABt or B after CBAt	1		1		1		ns

timing requirements, V_{CC} = 5 V ± 0.5 V (see Note 2)

		T_A = 25°C		54AC11646		74AC11646		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	100	0	100	0	100	MHz
t_w	Pulse duration, CAB or CBA high or low	5		5		5		ns
t_{su}	Setup time, A before CABt or B before CBAt	4.5		4.5		4.5		ns
t_h	Hold time, A after CABt or B after CBAt	1		1		1		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics, V_{CC} = 3.3 V ± 0.3 V (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11646		74AC11646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			65			65		65		MHz
t_{PLH}	A or B	B or A	1.5	9.1	12.1	1.5	14.9	1.5	13.8	ns
t_{PHL}			1.5	10.7	13.4	1.5	15.3	1.5	14.5	
t_{PZH}	$\overline{G}$	A or B	1.5	13	16.4	1.5	20.2	1.5	18.7	ns
t_{PZL}			1.5	16.1	20.4	1.5	22.2	1.5	21.8	
t_{PHZ}	$\overline{G}$	A or B	1.5	7.9	9.6	1.5	10.8	1.5	10.3	ns
t_{PLZ}			1.5	7.2	8.9	1.5	10.1	1.5	9.6	
t_{PLH}	CBA or CAB	A or B	1.5	11.8	15	1.5	18.4	1.5	17	ns
t_{PHL}			1.5	13.7	16.8	1.5	19.4	1.5	18.3	
t_{PLH}	SBA or SAB† (A or B high)	A or B	1.5	9.8	12.9	1.5	15.6	1.5	14.4	ns
t_{PHL}			1.5	12	14.5	1.5	16.7	1.5	15.8	
t_{PLH}	SBA or SAB† (A or B low)	A or B	1.5	10.7	13.8	1.5	16.6	1.5	15.4	ns
t_{PHL}			1.5	12.4	15	1.5	17.3	1.5	16.4	
t_{PZH}	DIR	A or B	1.5	13.7	17.1	1.5	21	1.5	19.4	ns
t_{PZL}			1.5	16.8	21	1.5	25.3	1.5	23.6	
t_{PHZ}	DIR	A or B	1.5	7.9	9.7	1.5	11	1.5	10.5	ns
t_{PLZ}			1.5	7.3	9.1	1.5	10.4	1.5	9.9	

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics, V_{CC} = 5 V ± 0.5 V (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11646		74AC11646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100			100		100		MHz
t_{PLH}	A or B	B or A	1.5	5.5	7.9	1.5	9.5	1.5	8.8	ns
t_{PHL}			1.5	6.3	8.9	1.5	10.3	1.5	9.8	
t_{PZH}	$\overline{G}$	A or B	1.5	7.8	10.7	1.5	13	1.5	12	ns
t_{PZL}			1.5	8.5	11.9	1.5	14	1.5	13.1	
t_{PHZ}	$\overline{G}$	A or B	1.5	5.9	8.4	1.5	9.3	1.5	8.9	ns
t_{PLZ}			1.5	5.9	7.7	1.5	8.7	1.5	8.3	
t_{PLH}	CBA or CAB	A or B	1.5	7	9.7	1.5	11.9	1.5	11	ns
t_{PHL}			1.5	8.2	11	1.5	13	1.5	12.2	
t_{PLH}	SBA or SAB† (A or B high)	A or B	1.5	5.9	8.4	1.5	10.1	1.5	9.4	ns
t_{PHL}			1.5	7.2	9.8	1.5	11.4	1.5	10.7	
t_{PLH}	SBA or SAB† (A or B low)	A or B	1.5	6.3	8.9	1.5	10.7	1.5	9.9	ns
t_{PHL}			1.5	7.3	9.9	1.5	11.7	1.5	11	
t_{PZH}	DIR	A or B	1.5	8.4	11.2	1.5	13.6	1.5	12.6	ns
t_{PZL}			1.5	9.1	12.3	1.5	14.6	1.5	13.7	
t_{PHZ}	DIR	A or B	1.5	6.3	8.2	1.5	9.1	1.5	8.7	ns
t_{PLZ}			1.5	5.7	7.5	1.5	8.5	1.5	8.1	

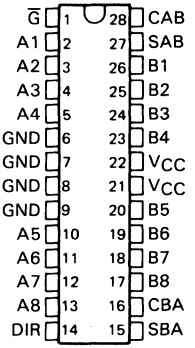
†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

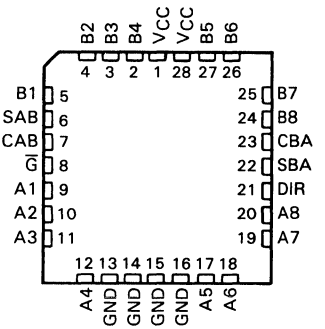
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	59	pF
		Outputs disabled		15	

- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic DIPs**

54ACT11646 . . . JT PACKAGE
74ACT11646 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11646 . . . FK PACKAGE
(TOP VIEW)



description

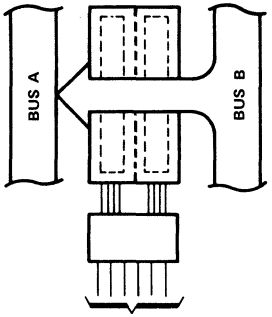
These devices consist of bus transceiver circuits, 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

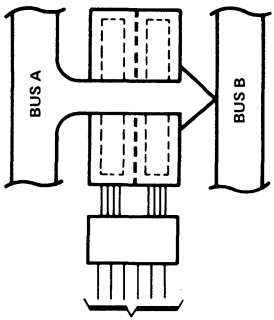
The 54ACT11646 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11646 is characterized for operation from −40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.



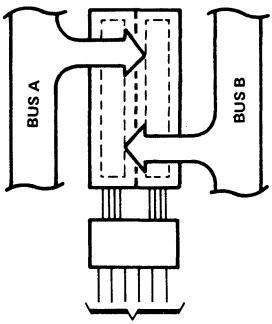
1 $\overline{G}$	14 DIR	28 CAB	16 CBA	27 SAB	15 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



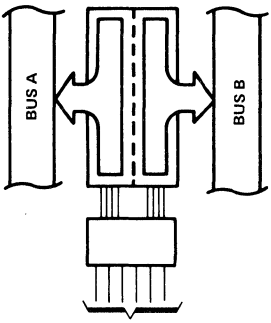
1 $\overline{G}$	14 DIR	28 CAB	16 CBA	27 SAB	15 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



1 $\overline{G}$	14 DIR	28 CAB	16 CBA	27 SAB	15 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



1 $\overline{G}$	14 DIR	28 CAB	16 CBA	27 SAB	15 SBA
L	L	X	HorL	X	H
L	H	HorL	X	H	X

TRANSFER STORED DATA
TO A OR B

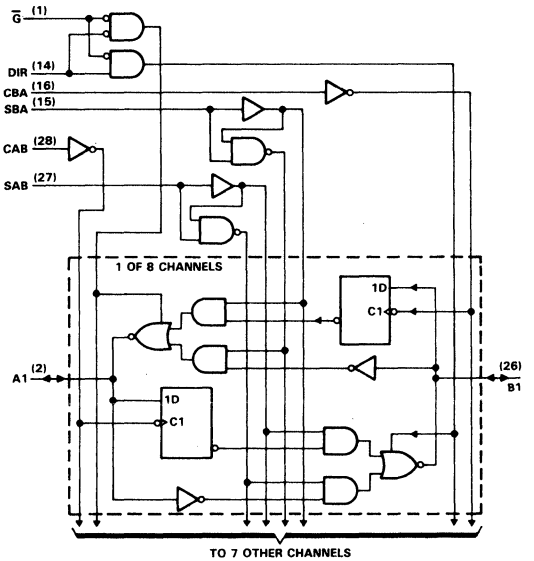
FIGURE 1. BUS-MANAGEMENT FUNCTIONS

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

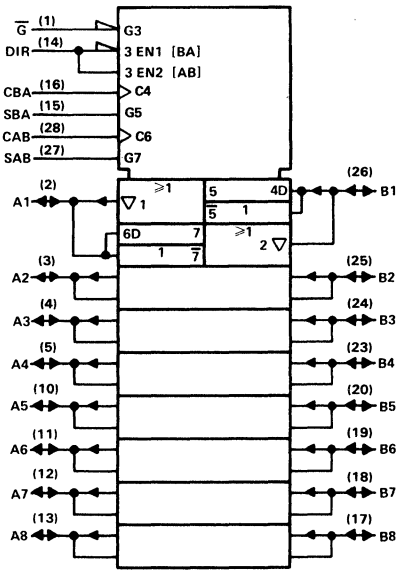
† The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11646		74ACT11646		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11646		74ACT11646		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	A or B ports‡	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	$\overline{G}$ or DIR	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i		V_I = V_{CC} or GND	5 V		4.5						pF
C_o		V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements, V_{CC} = 5 ± 0.5 V (see Note 2)

		T_A = 25°C		54ACT11646		74ACT11646		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	105	0	105	0	105	MHz
t_w	Pulse duration, CAB or CBA high or low	4.8		4.8		4.8		ns
t_{su}	Setup time, A before CLK↑ or B before CBA↑	4.5		4.5		4.5		ns
t_h	Hold time, A after CAB↑ or B after CBA↑	2.5		2.5		2.5		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics, V_{CC} = 5 V ± 0.5 V (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11646		74ACT11646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			105			105		105		MHz
t_{PLH}	A or B	B or A	1.5	7.3	10.1	1.5	12.5	1.5	11.5	ns
t_{PHL}			1.5	7.2	11	1.5	12.9	1.5	12	
t_{PZH}	$\overline{G}$	A or B	1.5	7.7	12.8	1.5	15.5	1.5	14.4	ns
t_{PZL}			1.5	9.2	13.8	1.5	16.7	1.5	15.3	
t_{PHZ}	$\overline{G}$	A or B	1.5	8.6	10.7	1.5	12.3	1.5	11.6	ns
t_{PLZ}			1.5	7.8	9.7	1.5	11.2	1.5	10.6	
t_{PLH}	CBA or CAB	A or B	1.5	8.8	11.9	1.5	14.7	1.5	13.5	ns
t_{PHL}			1.5	10	13.4	1.5	15.9	1.5	14.9	
t_{PZH}	DIR	A or B	1.5	10.2	13.7	1.5	16.7	1.5	15.3	ns
t_{PZL}			1.5	10.9	14.8	1.5	18	1.5	16.5	
t_{PHZ}	DIR	A or B	1.5	7.9	10.5	1.5	11.8	1.5	11.3	ns
t_{PLZ}			1.5	7.3	9.5	1.5	10.7	1.5	10.3	
t_{PLH}	SBA or SAB (A or B high)	A or B	1.5	6.7	10.3	1.5	12.4	1.5	11.5	ns
t_{PHL}			1.5	9.1	12.1	1.5	14.5	1.5	13.5	
t_{PLH}	SBA or SAB (A or B low)	A or B	1.5	8	10.9	1.5	13.6	1.5	12.4	ns
t_{PHL}			1.5	8.1	11.9	1.5	14	1.5	13.1	

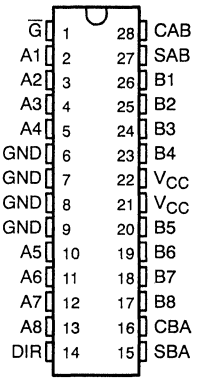
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

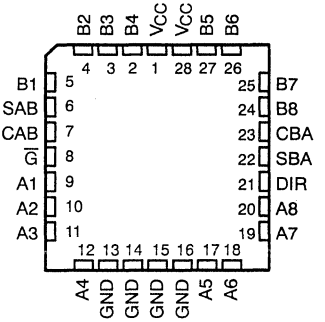
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	63	pF
		Outputs disabled		14	

- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Inverting Data Paths**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11648 . . . JT PACKAGE
74AC11648 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11648 . . . FK PACKAGE
(TOP VIEW)



description

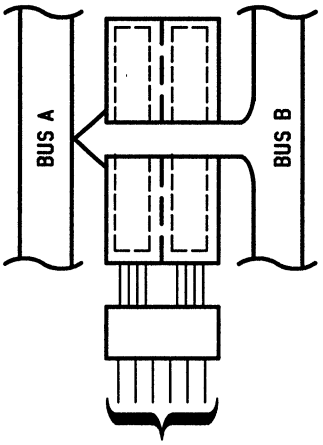
These devices consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

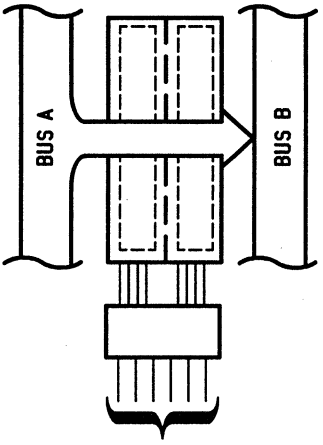
The 54AC11648 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11648 is characterized for operation from – 40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.



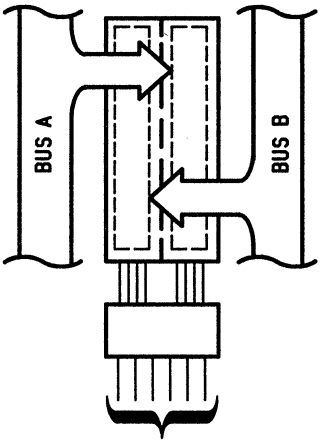
1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



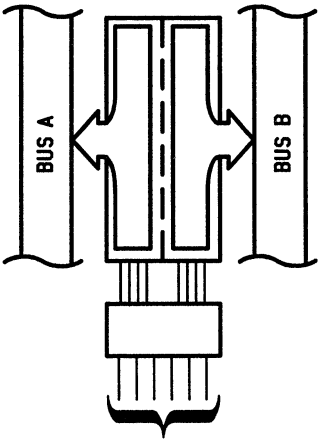
1	14	28	26	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B, OR A AND B



1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA TO A OR B

FIGURE 1. BUS-MANAGEMENT FUNCTIONS

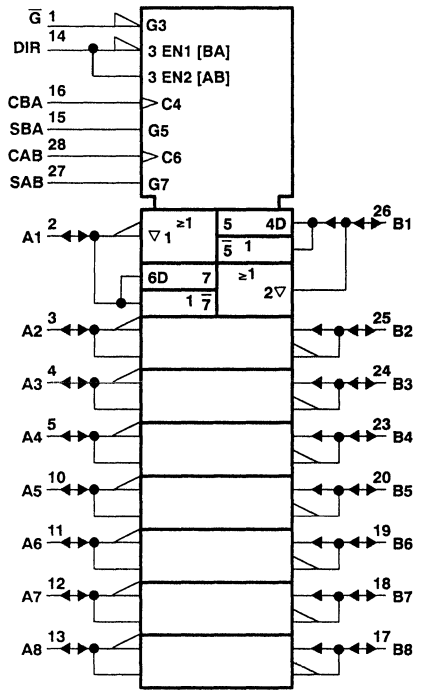
Pin numbers shown are for DW, JD, and NW packages.

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	BI THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X	Input	Output	Store $\overline{A}$ Data to B Bus

† The data output functions may be enabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

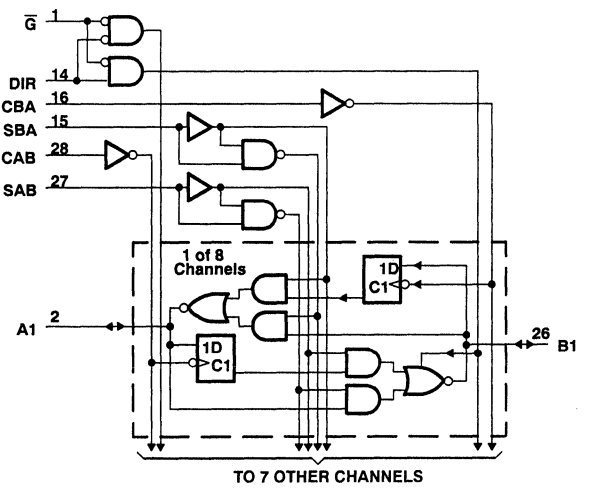
logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, or NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND pins ..... ± 200 mA
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11648			74AC11648			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			– 4			– 4	mA
		V_{CC} = 4.5 V			– 24			– 24	
		V_{CC} = 5.5 V			– 24			– 24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		– 55		125	– 40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11648		74AC11648		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = – 50 μA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = – 4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = – 50 mA†	5.5 V				3.85				
		I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	A or B ports‡	$V_I = V_{CC}$ or GND	5.5 V			± 0.5		± 10		± 5	μA
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_o	A or B ports	$V_I = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (see Note 2)

		T_A = 25°C		54AC11648		74AC11648		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	40	0	40	0	40	MHz
t_w	Pulse duration, CAB or CBA high or low	12.5		12.5		12.5		ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	6.5		6.5		6.5		ns
t_h	Hold time, A before CAB↑ or B after CBA↑	0		0		0		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (see Note 2)

		T_A = 25°C		54AC11648		74AC11648		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	90	0	90	0	90	MHz
t_w	Pulse duration, CAB or CBA high or low	5.6		5.6		5.6		ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	4.5		4.5		4.5		ns
t_h	Hold time, A before CAB↑ or B after CBA↑	0		0		0		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11648		74AC11648		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			40			40		40		MHz
t_{PLH}	A or B	B or A	3	8.7	12.6	3	15.6	3	14.3	ns
t_{PHL}			3.8	9.3	14.4	3.8	17	3.8	15.9	
t_{PZH}	$\overline{G}$	A or B	5	11.1	17.2	5	21	5	19.4	ns
t_{PZL}			5.2	12.8	20.5	5.2	24.7	5.2	23	
t_{PHZ}	$\overline{G}$	A or B	4.1	7.2	9.9	4.1	11.2	4.1	10.6	ns
t_{PLZ}			3.7	6.5	9.1	3.7	10.2	3.7	9.7	
t_{PLH}	CBA or CAB	A or B	4.3	10.1	15.6	4.3	19.2	4.3	17.6	ns
t_{PHL}			5.2	11.5	17.6	5.2	20.5	5.2	19.4	
t_{PLH}	SAB or SBA† (with A or B high)	A or B	3.7	9.1	14.1	3.7	17.2	3.7	15.8	ns
t_{PHL}			4.5	10.3	15.9	4.5	18.5	4.5	17.4	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	3.2	8.6	13.6	3.2	16.6	3.2	15.3	ns
t_{PHL}			4.6	10.3	15.6	4.6	18.2	4.6	17.1	
t_{PZH}	DIR	A or B	4.9	11.6	18.2	4.9	22.4	4.9	20.6	ns
t_{PZL}			5.2	14.2	21.6	5.2	24.9	5.2	24.3	
t_{PHZ}	DIR	A or B	3.8	7.1	10.1	3.8	11.4	3.8	10.9	ns
t_{PLZ}			3.5	6.5	9.3	3.5	10.6	3.5	10.1	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11648		74AC11648		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			90			90		90		MHz
t_{PLH}	A or B	B or A	2.6	5.6	8.3	2.6	10.3	2.6	9.5	ns
t_{PHL}			3.2	6.4	9.4	3.2	11.4	3.2	10.6	
t_{PZH}	$\overline{G}$	A or B	4.2	7.8	11.3	4.2	13.8	4.2	12.8	ns
t_{PZL}			4.1	8.1	12	4.1	14.7	4.1	13.6	
t_{PHZ}	$\overline{G}$	A or B	3.8	6.3	8.6	3.8	9.6	3.8	9.2	ns
t_{PLZ}			3.5	5.7	7.8	3.5	8.8	3.5	8.4	
t_{PLH}	CBA or CAB	A or B	3.6	6.9	10	3.6	12.4	3.6	11.4	ns
t_{PHL}			4.3	8	11.4	4.3	13.8	4.3	12.8	
t_{PLH}	SAB or SBA† (with A or B high)	A or B	3.1	6.2	9.2	3.1	11.3	3.1	10.4	ns
t_{PHL}			3.8	7.6	10.4	3.8	12.5	3.8	11.6	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	2.8	6.1	8.9	2.8	10.9	2.8	10.1	ns
t_{PHL}			3.8	7.3	10.4	3.8	12.5	3.8	11.6	
t_{PZH}	DIR	A or B	4	8	11.9	4	14.5	4	13.4	ns
t_{PZL}			4.1	8.4	12.7	4.1	15.5	4.1	14.4	
t_{PHZ}	DIR	A or B	3.5	6.1	8.5	3.5	9.5	3.5	9.1	ns
t_{PLZ}			3.4	5.9	7.8	3.4	8.7	3.4	8.4	

† These parameters are measured with the internal output state of the storageregister opposite to that of the bus input.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceivers	Outputs enabled	C_L = 50 pF, f = 1 MHz	66	pF
		Outputs disabled		17	

- **Inputs are TTL-Voltage Compatible**
- **Independent Registers for A and B Buses**
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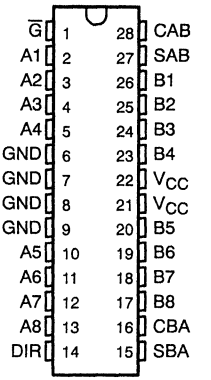
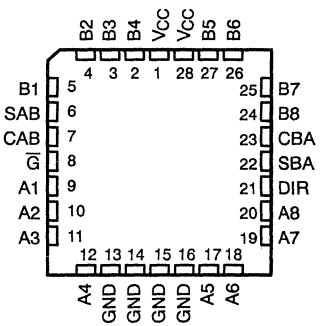


54ACT11648 . . . FK PACKAGE
(TOP VIEW)



description

These devices consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

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When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

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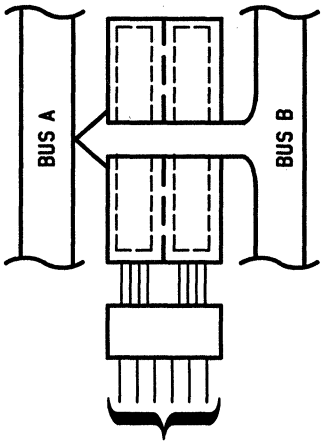
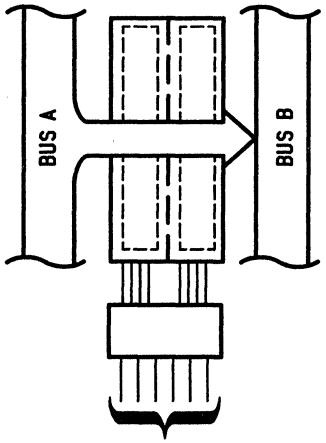


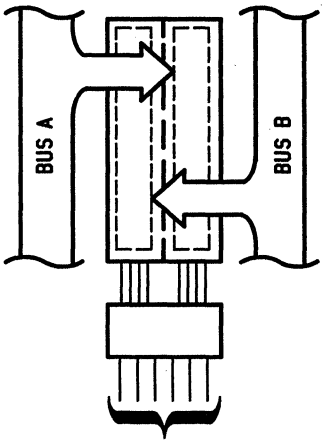
1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



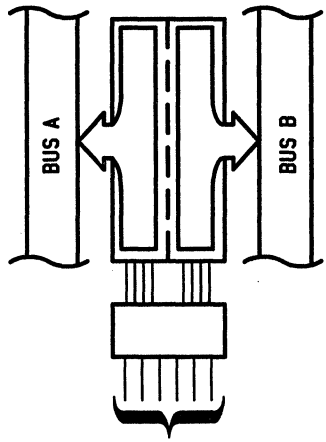
1	14	28	26	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B, OR A AND B



1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA TO A OR B

FIGURE 1. BUS-MANAGEMENT FUNCTIONS

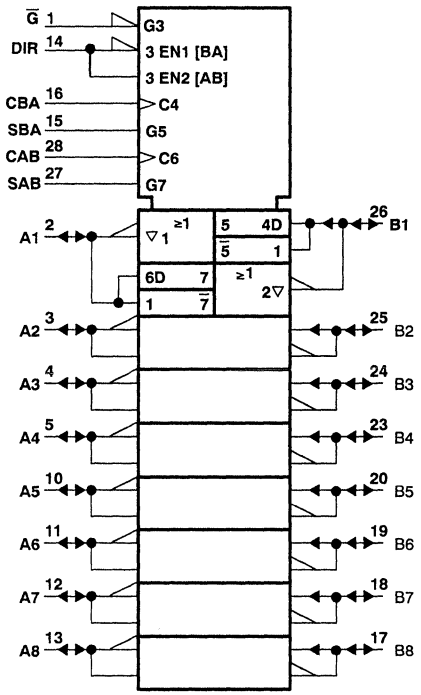
Pin numbers shown are for DW, JT, and NT packages.

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	BI THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X	Input	Output	Store $\overline{A}$ Data to B Bus

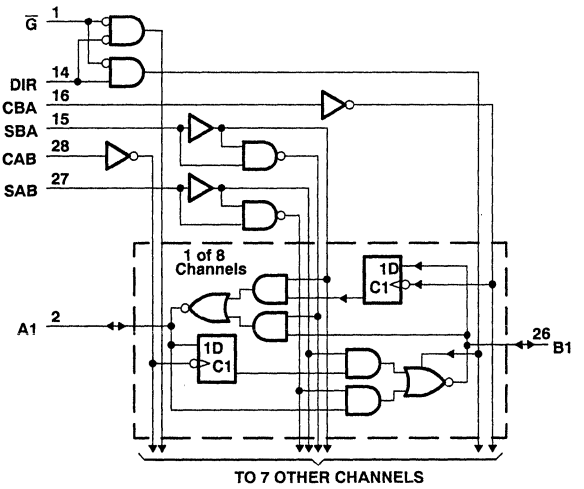
† The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, or NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND pins ..... ± 200 mA
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11648			74ACT11648			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			– 24			– 24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	– 55		125	– 40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11648		74ACT11648		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = – 50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = – 50 mA†	5.5 V				3.85				
		I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control Inputs	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{OZ}	A or B ports‡	$V_I = V_{CC}$ or GND	5.5 V			± 0.5		± 10		± 5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}	A or B ports	$V_I = V_{CC}$ or GND	5 V		12						

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage currrent.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements, V_{CC} = 5 V ± 0.5 V (see Note 2)

		T_A = 25°C		54ACT11648		74ACT11648		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	75	0	75	0	75	MHz
t_w	Pulse duration, CAB or CBA high or low	6.7		6.7		6.7		ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	5		5		5		ns
t_h	Hold time, A after CAB↑ or B after CBA↑	2		2		2		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11648		74ACT11648		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			75			75		75		MHz
t_{PLH}	A or B	B or A	2.4	6.5	9.5	2.4	11.6	2.4	10.7	ns
t_{PHL}			4.4	8.5	11.3	4.4	13.8	4.4	12.7	
t_{PZH}	$\overline{G}$	A or B	4.2	9.2	13	4.2	15.8	4.2	14.6	ns
t_{PZL}			4.3	9.8	13.9	4.3	16.9	4.3	15.6	
t_{PHZ}	$\overline{G}$	A or B	5.7	8.7	11.3	5.7	12.9	5.7	12.2	ns
t_{PLZ}			5.3	8.1	10.5	5.3	12.1	5.3	11.4	
t_{PLH}	CBA or CAB	A or B	5.2	9.4	12	5.2	14.9	5.2	13.7	ns
t_{PHL}			6	10.5	13.5	6	16.3	6	15.2	
t_{PLH}	SAB or SBA† (with A or B high)	A or B	4.7	8.6	11.3	4.7	14	4.7	12.9	ns
t_{PHL}			3.8	8.6	12	3.8	14.3	3.8	13.4	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	2.6	7.1	10.2	2.6	12.5	2.6	11.5	ns
t_{PHL}			5.4	9.7	12.6	5.4	15.2	5.4	14.1	
t_{PZH}	DIR	A or B	3.9	9.8	14.9	3.9	18.4	3.9	16.9	ns
t_{PZL}			3.9	10.8	15.1	3.9	18.7	3.9	17.2	
t_{PHZ}	DIR	A or B	4.5	8.2	10.6	4.5	12	4.5	11.5	ns
t_{PLZ}			3.9	7.3	9.6	3.9	11.9	3.9	11.3	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

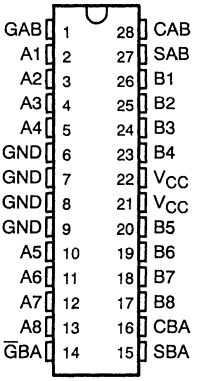
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceivers	Outputs enabled	C_L = 50 pF,	f = 1 MHz	61	pF
		Outputs disabled			15	

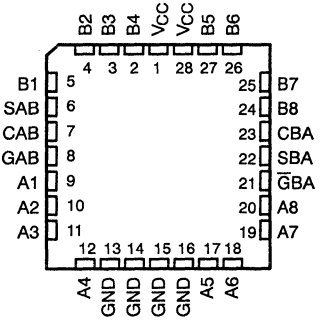
D3444, MARCH 1990–REVISED OCTOBER 1990

- **Bus Transceivers/Registers**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Inverting Data Paths**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11651 . . . JT PACKAGE
74AC11651 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11651 . . . FK PACKAGE
(TOP VIEW)



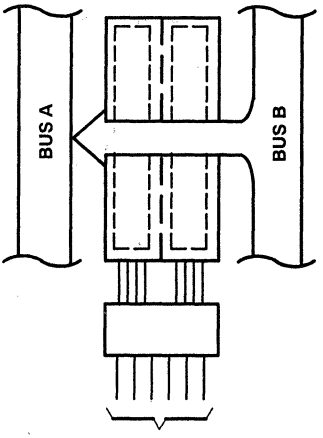
description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enables GAB and $\overline{G}$BA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}$BA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

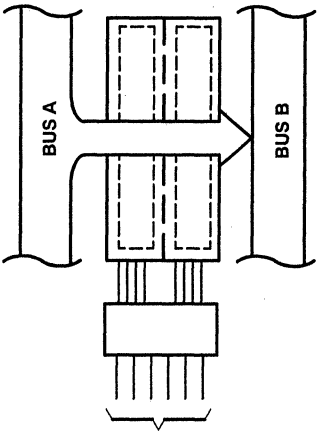
The 54AC11651 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74AC11651 is characterized for operation from – 40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.



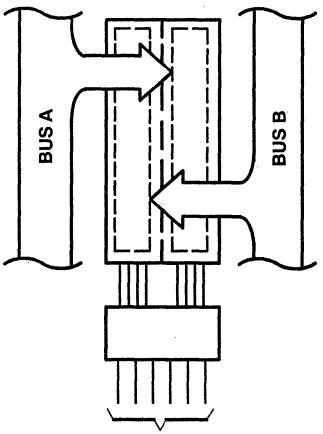
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



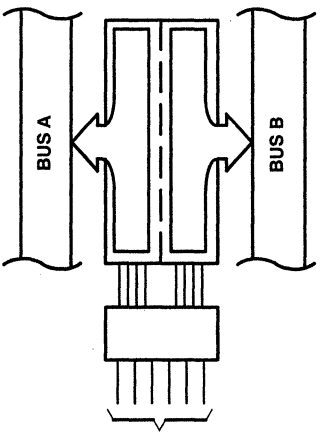
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A AND/OR B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA TO A AND/OR B

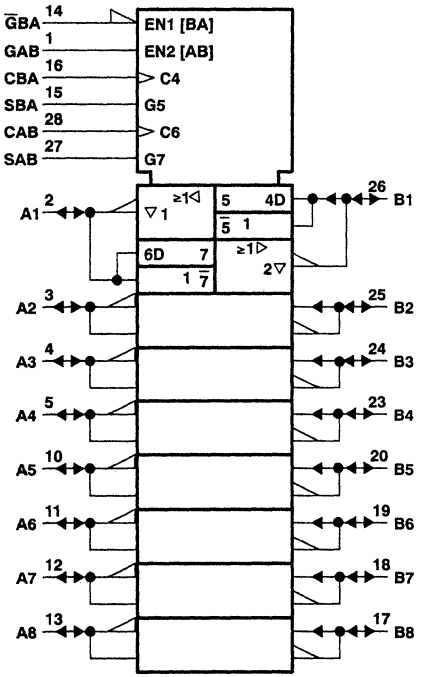
Figure 1. Bus Transfer Diagram

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified†	Store A, Hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified†	Input	Hold A, Store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus

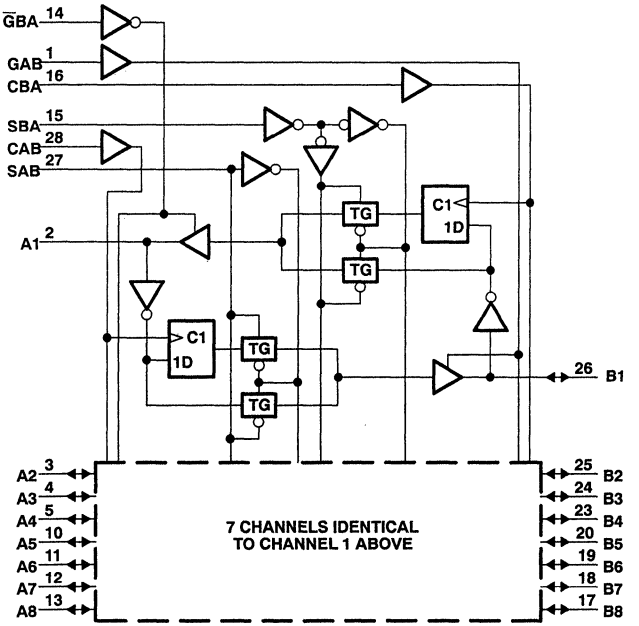
† The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
‡ Select control = L: clocks can occur simultaneously. Select control = H: clocks must be staggered in order to load both registers.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, or NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, or NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND pins ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11651			74AC11651			
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			– 4			– 4	mA
		V_{CC} = 4.5 V			– 24			– 24	
		V_{CC} = 5.5 V			– 24			– 24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		– 55		125	– 40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11651		74AC11651		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = – 50 μA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = – 4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = – 50 mA†	5.5 V				3.85				
		I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	A or B ports‡	$V_I = V_{CC}$ or GND	5.5 V			± 0.5		± 10		± 5	μA
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}	A or B ports	$V_I = V_{CC}$ or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 2)

		T_A = 25°C		54AC11651		74AC11651		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	45	0	45	0	45	MHz
t_w	Pulse duration, CAB or CBA high or low	10		10		10		ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	6.5		6.5		6.5		ns
t_h	Hold time, A after CAB↑ or B after CBA↑	0		0		0		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

		T_A = 25°C		54AC11651		74AC11651		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	90	0	90	0	90	MHz
t_w	Pulse duration, CAB or CBA high or low	5.5		5.5		5.5		ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	4.5		4.5		4.5		ns
t_h	Hold time, A after CAB↑ or B after CBA↑	0.5		0.5		0.5		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11651		74AC11651		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			45			45		45		MHz
t_{PLH}	A or B	B or A	3.2	7.7	12.1	3.2	15.4	3.2	14	ns
t_{PHL}			4.3	9.5	14.6	4.3	17.2	4.3	16.1	
t_{PLH}	CBA or CAB	A or B	4.6	9.8	15	4.6	15.8	4.6	17.2	ns
t_{PHL}			5.4	11.5	17.5	5.4	20.5	5.4	19.2	
t_{PLH}	SBA or SAB† with A or B high	A or B	3.8	8.6	13.3	3.8	16.9	3.8	15.3	ns
t_{PHL}			4.8	10.2	15.5	4.8	18.2	4.8	17.1	
t_{PLH}	SBA or SAB† with A or B low	A or B	3.4	8.1	12.7	3.4	16	3.4	14.6	ns
t_{PHL}			5	10.3	15.5	5	18.2	5	17.1	
t_{PZH}	$\overline{G}$BA	A	4.6	9.8	14.9	4.6	18.4	4.6	16.9	ns
t_{PZL}			5.3	12.1	18.9	5.3	23.2	5.3	21.3	
t_{PHZ}	$\overline{G}$BA	A	4.4	6.6	8.8	4.4	9.5	4.4	9.2	ns
t_{PLZ}			3.8	5.8	7.8	3.8	8.3	3.8	8.1	
t_{PZH}	GAB	B	4.9	10.2	15.5	4.9	19.2	4.9	17.6	ns
t_{PZL}			5.5	12.2	18.8	5.5	22.9	5.5	21.2	
t_{PHZ}	GAB	B	4.4	6.7	8.9	4.4	9.6	4.4	9.3	ns
t_{PLZ}			3.5	5.7	7.8	3.5	8.2	3.5	8	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11651		74AC11651		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			90			90		90		MHz
t_{PLH}	A or B	B or A	2.6	5.3	8	2.6	9.9	2.6	9.1	ns
t_{PHL}			3.5	6.5	9.4	3.5	11.3	3.5	10.5	
t_{PLH}	CBA or CAB	A or B	3.8	6.8	10	3.8	12.4	3.8	11.4	ns
t_{PHL}			4.7	8.1	11.5	4.7	13.8	4.7	12.8	
t_{PLH}	SAB or SBA† with A or B high	A or B	3.2	6	8.8	3.2	11	3.2	10.1	ns
t_{PHL}			3.9	7	10.1	3.9	12	3.9	11.2	
t_{PLH}	SAB or SBA† with A or B low	A or B	2.9	5.7	8.5	2.9	10.4	2.9	9.5	ns
t_{PHL}			4.1	7.2	10.3	4.1	12.3	4.1	11.4	
t_{PZH}	$\overline{G}$BA	A	3.9	6.9	9.8	3.9	12	3.9	11.1	ns
t_{PZL}			4.2	7.6	11	4.2	13.7	4.2	12.5	
t_{PHZ}	$\overline{G}$BA	A	4.1	5.9	7.6	4.1	8.2	4.1	8	ns
t_{PLZ}			3.5	5.2	6.8	3.5	7.4	3.5	7.1	
t_{PZH}	GAB	B	4.2	5.9	10.4	4.2	12.9	4.2	11.8	ns
t_{PZL}			4.5	8	11.4	4.5	14	4.5	12.9	
t_{PHZ}	GAB	B	4.2	6	7.8	4.2	8.4	4.2	8.2	ns
t_{PLZ}			3.3	5.1	6.9	3.3	7.3	3.3	7.2	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	64	pF
		Outputs disabled		14	

D3445, MARCH 1990–REVISED OCTOBER 1990

- **Inputs are TTL-Voltage Compatible**
- **Bus Transceivers/Registers**
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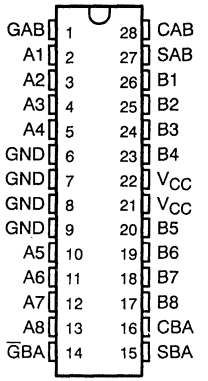
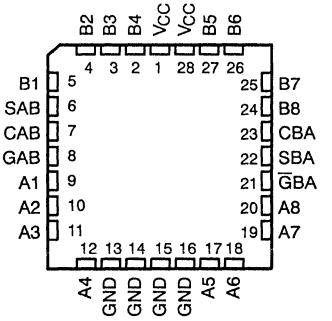
- **Inverting Data Paths**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11651 . . . JT PACKAGE
74ACT11651 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11651 . . . FK PACKAGE
(TOP VIEW)



description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enables GAB and $\overline{G}$BA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data.

A low input level selects real-time data and a high selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers. Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}$BA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The 54ACT11651 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT11651 is characterized for operation from – 40°C to 85°C.

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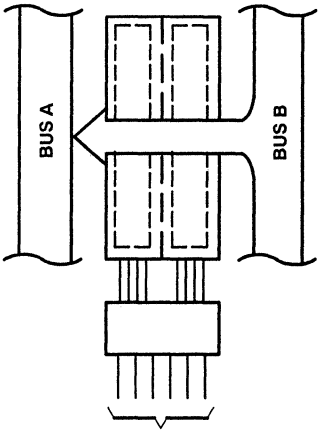
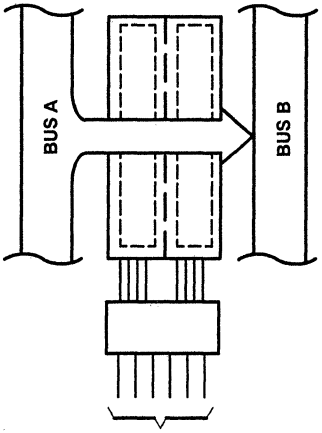


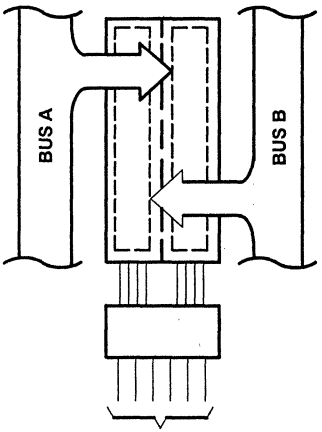
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



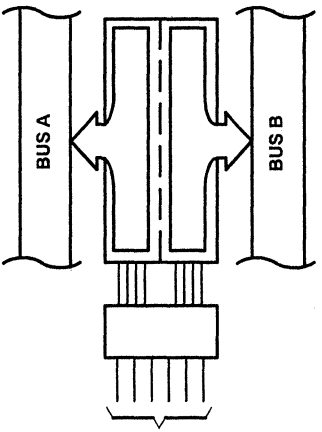
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A AND/OR B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA TO A AND/OR B

Figure 1. Bus Transfer Diagram

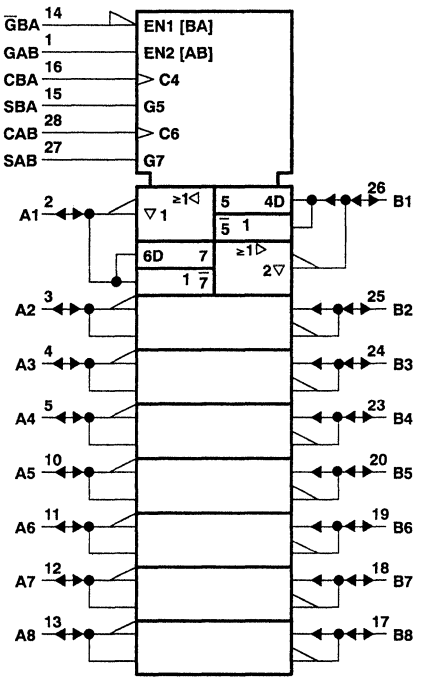
FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified†	Store A, Hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified†	Input	Hold A, Store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus

† The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

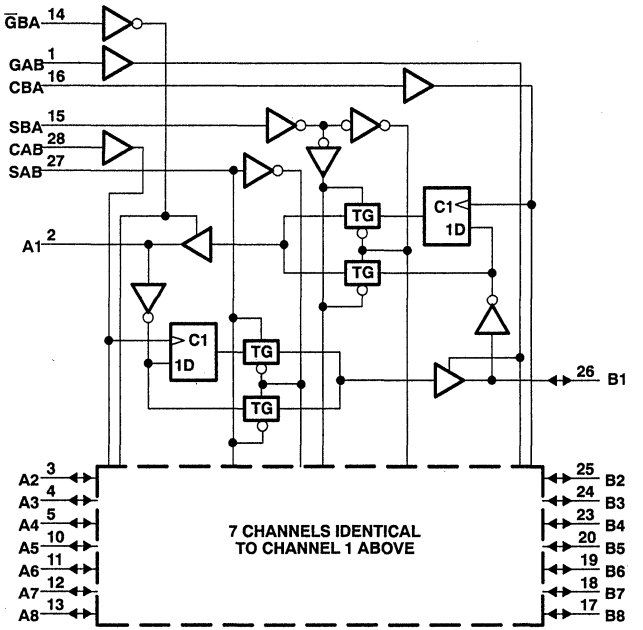
‡ Select control = L: clocks can occur simultaneously. Select control = H: clocks must be staggered in order to load both registers.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, or NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND pins ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		SN54ACT11651			SN74ACT11651			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11651		74ACT11651		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	A or B ports§	V_I = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	Control Inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡		V_I = V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports	V_I = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

		T_A = 25°C		54ACT11651		74ACT11651		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	90	0	90	0	90	MHz
t_w	Pulse duration, CAB or CBA high or low	5.5		5.5		5.5		ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	4.5		4.5		4.5		ns
t_h	Hold time, A after CAB↑ or B after CBA↑	2		2		2		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11651		74ACT11651		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			90			90		90		MHz
t_{PLH}	A or B	B or A	2.6	5.6	8.9	2.6	10.7	2.6	9.9	ns
t_{PHL}			4.7	7.7	10.7	4.7	12.8	4.7	11.9	
t_{PLH}	CBA or CAB	A or B	5.5	8.4	11.2	5.5	13.8	5.5	12.7	ns
t_{PHL}			6.3	9.5	12.7	6.3	15.3	6.3	14.1	
t_{PLH}	SBA or SAB† with A or B high	A or B	4.8	7.6	10.4	4.8	12.9	4.8	11.8	ns
t_{PHL}			4.1	7.7	11.2	4.1	13.3	4.1	12.4	
t_{PLH}	SBA or SAB† with A or B low	A or B	3	6.2	9.3	3	11.3	3	10.4	ns
t_{PHL}			5.6	8.7	11.7	5.6	14.1	5.6	13	
t_{PZH}	$\overline{G}$BA	A	4	7.4	10.7	4	12.9	4	11.9	ns
t_{PZL}			4.3	8.2	11.9	4.3	14.5	4.3	13.3	
t_{PHZ}	$\overline{G}$BA	A	5.9	7.7	9.5	5.9	10.4	5.9	10	ns
t_{PLZ}			5.1	6.9	8.7	5.1	9.6	5.1	9.2	
t_{PZH}	GAB	B	5.9	9	12.1	5.9	15.1	5.9	13.7	ns
t_{PZL}			6.4	9.8	13.2	6.4	16.3	6.4	14.9	
t_{PHZ}	GAB	B	4.7	7.1	9.5	4.7	10.7	4.7	10	ns
t_{PLZ}			3.8	6.1	8.4	3.8	9.1	3.8	8.8	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	Outputs enabled	C_L = 50 pF,	f = 1 MHz	61	pF
		Outputs disabled			15	

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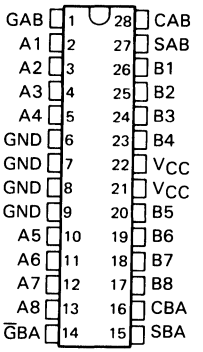
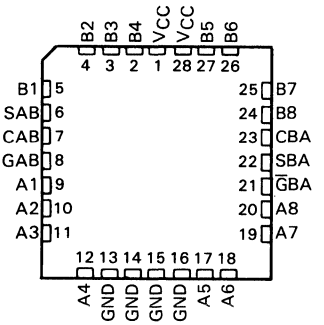


54AC11652 . . . FK PACKAGE
(TOP VIEW)



description

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Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}$BA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

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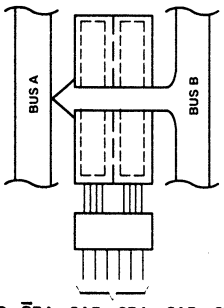
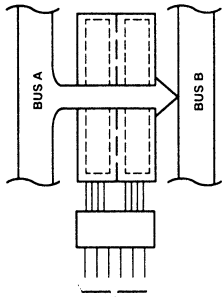


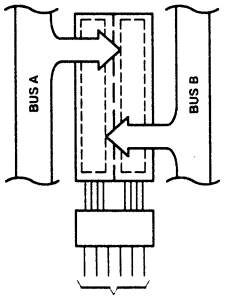
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



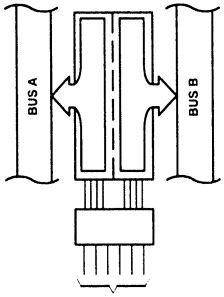
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A AND/OR B/



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA
TO A AND/OR B

FIGURE 1. BUS TRANSFER DIAGRAM

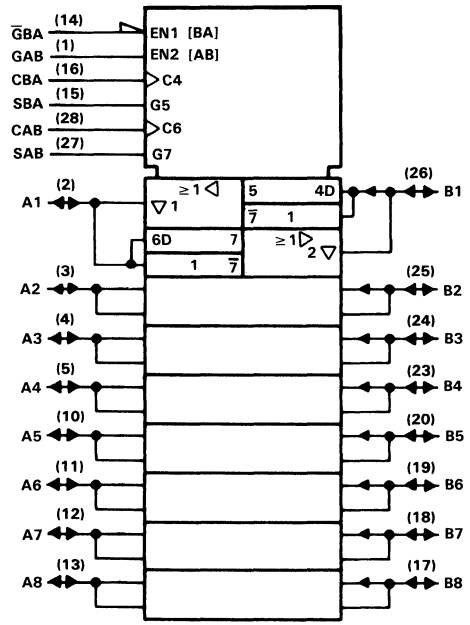
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified†	Store A, Hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified†	Input	Hold A, Store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored B Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

† The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

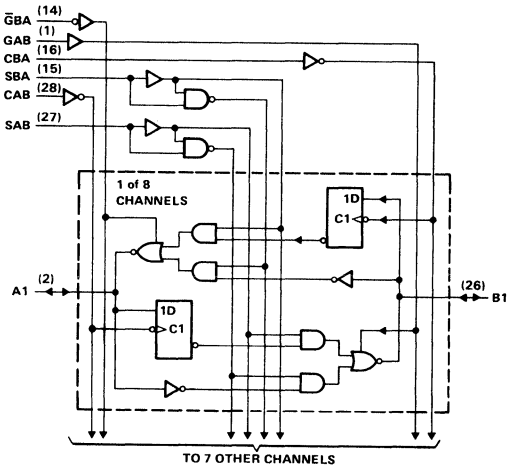
‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

			54AC11652			74AC11652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 v			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Control pins	0		5	0		5	ns/V
		Data	0		10	0		10	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11652		74AC11652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 µA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 µA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}‡	A or B ports	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	µA
I_I	Control pins	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	µA
C_i	Control pins	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 2)

PARAMETER		T_A = 25°C		54AC11652		74AC11652		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	65	0	65	0	65	MHz
t_w	Pulse duration, CAB or CBA high or low	7.7		7.7		7.7		ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	6		6		6		ns
t_h	Hold time, A after CAB↑ or B after CBA↑	1		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER		T_A = 25°C		54AC11652		74AC11652		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	105	0	105	1	105	MHz
t_w	Pulse duration, CAB or CBA high or low	4.8		4.8		4.8		ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	4.5		4.5		4.5		ns
t_h	Hold time, A after CAB↑ or B after CBA↑	1		1		1		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11652		74AC11652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			65			65		65		MHz
t_{PLH}	A or B	B or A	2.9	8.5	11.1	2.9	13.9	2.9	12.9	ns
t_{PHL}			3.9	10.3	12.9	3.9	14.9	3.9	14.2	
t_{PLH}	CBA or CAB	A or B	4.3	11.2	14.3	4.3	17.6	4.3	16.2	ns
t_{PHL}			5.3	13.1	16.2	5.3	18.7	5.3	17.8	
t_{PLH}	SBA or SAB† with A or B high	A or B	3.4	9.4	12	3.4	14.7	3.4	13.7	ns
t_{PHL}			4.7	11.5	14.3	4.7	16.5	4.7	15.6	
t_{PLH}	SBA or SAB† with A or B low	A or B	3.9	10.5	13.3	3.9	16.1	3.9	14.9	ns
t_{PHL}			4.8	12.1	16.3	4.8	18.5	4.8	17.7	
t_{PZH}	$\overline{G}$BA	A	4.3	11.1	14.5	4.3	17.8	4.3	16.5	ns
t_{PZL}			5.2	14.4	19.8	5.2	23.4	5.2	22	
t_{PHZ}	$\overline{G}$BA	A	3.7	6.4	8.1	3.7	8.7	3.7	8.5	ns
t_{PLZ}			3.5	6	7.8	3.5	8.4	3.5	8.2	
t_{PZH}	GAB	B	4.7	11.6	15	4.7	18.3	4.7	16.9	ns
t_{PZL}			5.6	14.8	19.9	5.6	23.4	5.6	21.9	
t_{PHZ}	GAB	B	4	6.6	8.2	4	8.8	4	8.6	ns
t_{PLZ}			3.5	6.1	7.7	3.5	8.2	3.5	8	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11652		74AC11652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			105			105		105		MHz
t_{PLH}	A or B	B or A	2.4	5.2	7.6	2.4	9.2	2.4	8.6	ns
t_{PHL}			3.1	6	8.7	3.1	10.1	3.1	9.6	
t_{PLH}	CBA or CAB	A or B	3.6	6.7	9.5	3.6	11.5	3.6	10.7	ns
t_{PHL}			4.4	7.8	10.8	4.4	12.8	4.4	12	
t_{PLH}	SBA or SAB† with A or B high	A or B	2.9	5.6	8.1	2.9	9.7	2.9	9.1	ns
t_{PHL}			3.8	6.9	9.6	3.8	11.4	3.8	10.7	
t_{PLH}	SBA or SAB† with A or B low	A or B	3.3	6.2	8.8	3.3	10.5	3.3	9.9	ns
t_{PHL}			4	7.1	9.9	4	11.5	4	10.9	
t_{PZH}	$\overline{G}$BA	A	3.3	6.6	9.6	3.3	11.6	3.3	10.9	ns
t_{PZL}			4.2	7.4	10.9	4.2	13	4.2	12.2	
t_{PHZ}	$\overline{G}$BA	A	3.6	5.5	7.2	3.6	7.8	3.6	7.6	ns
t_{PLZ}			3.3	5	6.7	3.3	7.2	3.3	7.1	
t_{PZH}	GAB	B	4.1	7.2	10.1	4.1	12.2	4.1	11.3	ns
t_{PZL}			4.6	7.9	11.1	4.6	13.2	4.6	12.3	
t_{PHZ}	GAB	B	3.9	5.6	7.3	3.9	7.8	3.9	7.6	ns
t_{PLZ}			3.4	5.2	6.8	3.4	7.4	3.4	7.2	

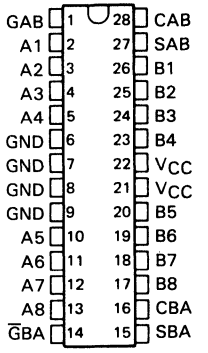
† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

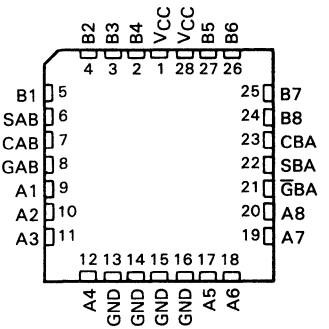
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	60	pF
		Outputs disabled		14	

- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic DIPs

54ACT11652 . . . JT PACKAGE
74ACT11652 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11652 . . . FK PACKAGE
(TOP VIEW)



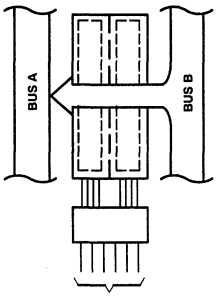
description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enables GAB and $\overline{G}$BA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}$BA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

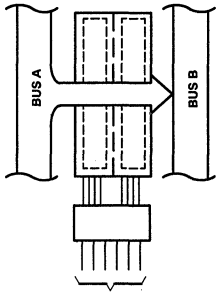
The 54ACT11652 is characterized for operation over the full military temperature range of – 55°C to 125°C.The 74ACT11652 is characterized for operation from – 40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.



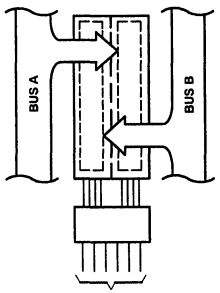
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



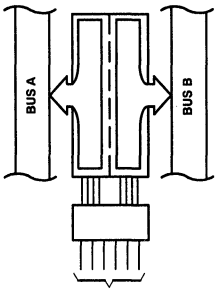
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A AND/OR B



GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA
TO A AND/OR B

FIGURE 1. BUS TRANSFER DIAGRAM

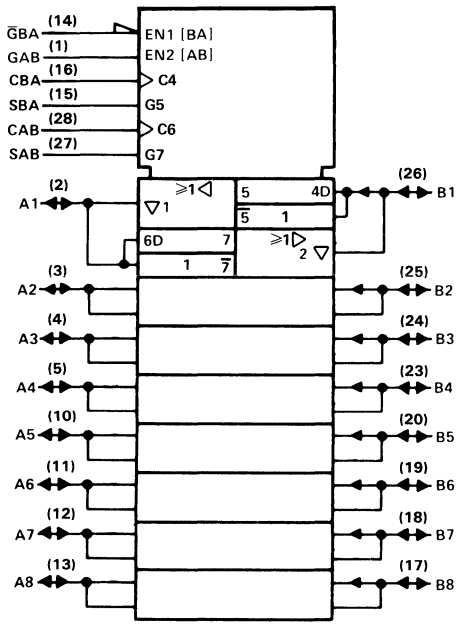
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified†	Store A, Hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified†	Input	Hold A, Store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

† The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

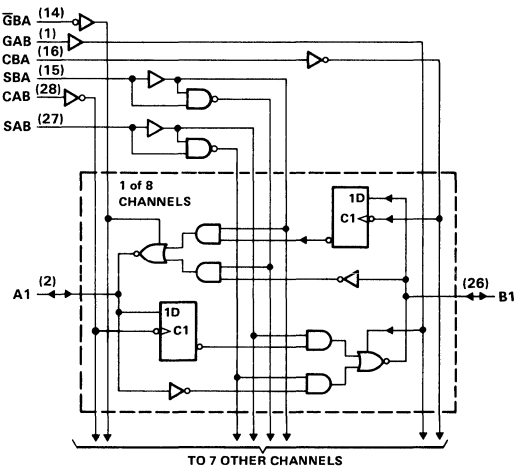
logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		54ACT11652		74ACT11652		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11652		74ACT11652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 µA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	A or B ports‡	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	µA
I_I	GAB or $\overline{G}$BA	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	µA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	GAB or $\overline{G}$BA	V_I = V_{CC} or GND	5 V		4.5						pF
C_o	A or B ports	V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements, V_{CC} = 5 V ± 0.5 V (see Note 2)

PARAMETER		T_A = 25°C		54ACT11652		74ACT11652		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	105	0	105	0	105	MHz
t_w	Pulse duration, CAB or CBA high or low	4.8		4.8		4.8		ns
t_{su}	Setup time, A before CLK↑ or B before CBA↑	4		4		4		ns
t_h	Hold time, A after CAB↑ or B after CBA↑	2.5		2.5		2.5		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11652		74ACT11652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			105			105		105		MHz
t_{PLH}	A or B	B or A	3.8	7	9.9	3.8	11.9	3.8	11.1	ns
t_{PHL}			3.4	6.7	10.7	3.4	12.2	3.4	11.6	
t_{PLH}	CBA or CAB	A or B	5.4	8.4	11.8	5.4	14.1	5.4	13.1	ns
t_{PHL}			6.1	9.4	13.1	6.1	15.3	6.1	14.4	
t_{PLH}	SBA or SAB† with A or B high	A or B	2.8	6.2	10.1	2.8	11.8	2.8	11	ns
t_{PHL}			5.5	8.7	12.1	5.5	14.1	5.5	13.3	
t_{PLH}	SBA or SAB† with A or B low	A or B	4.9	7.8	11	4.9	13.2	4.9	12.2	ns
t_{PHL}			3.9	7.5	11.6	3.9	13.3	3.9	12.6	
t_{PZH}	$\overline{G}$BA	A	3.3	7.2	11.4	3.3	13.5	3.3	12.6	ns
t_{PZL}			4.1	7.8	12.6	4.1	14.7	4.1	13.8	
t_{PHZ}	$\overline{G}$BA	A	5.2	7.2	9.3	5.2	10.4	5.2	9.9	ns
t_{PLZ}			4.8	6.7	8.6	4.8	9.7	4.8	9.3	
t_{PZH}	GAB	B	5.1	9.1	13.4	5.1	16.7	5.1	15.2	ns
t_{PZL}			5.8	9.7	14.2	5.8	17.6	5.8	16.1	
t_{PHZ}	GAB	B	3.4	6.8	9.7	3.4	10.8	3.4	10.3	ns
t_{PLZ}			3.1	6	8.8	3.1	9.7	3.1	9.3	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

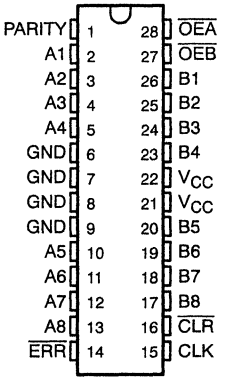
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	59	pF
		Outputs disabled		14	

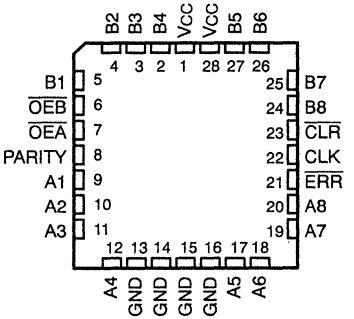
D3448, MARCH 1990–REVISED OCTOBER 1990

- **High-Speed Bus Transceivers With Parity Generator/Checker**
- **Parity-Error-Flag Open-Drain Output**
- **Register for Storage of the Parity-Error Flag**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11833 . . . JT PACKAGE
74AC11833 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11833 . . . FK PACKAGE
(TOP VIEW)



description

The 'AC11833 is an 8-bit to 9-bit parity transceiver designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the $\overline{ERR}$ output will indicate whether or not an error in the B data has occurred. The output enable inputs $\overline{OEA}$ and $\overline{OEB}$ can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd output (PARITY) and monitors the parity of the I/O ports with an open-drain parity error flag ($\overline{ERR}$). $\overline{ERR}$ is clocked into the register on the rising edge of the CLK input. The error flag register is cleared with a low pulse on the $\overline{CLR}$ input. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The 54AC11833 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11833 is characterized for operation from – 40°C to 85°C.

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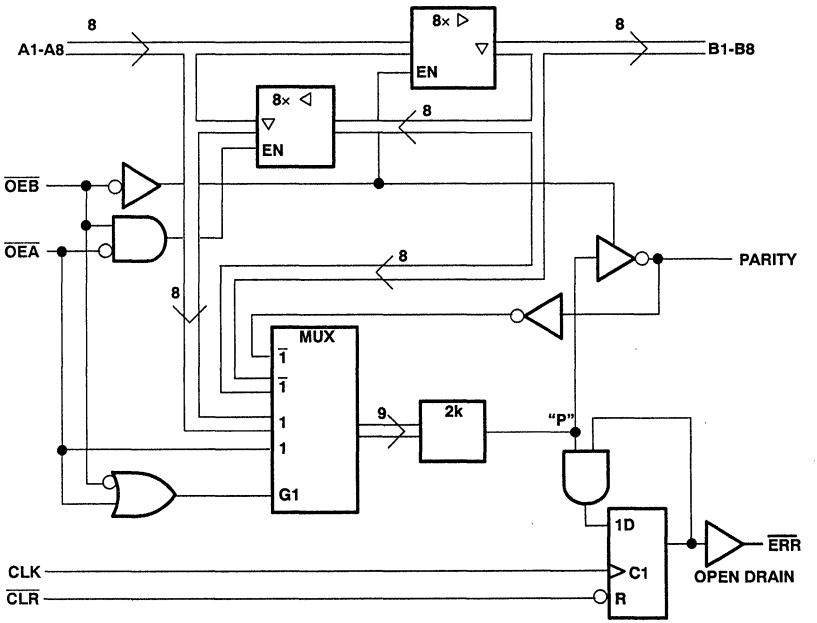
PRODUCT PREVIEW

Function Table

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	Ai Σ of H's	Bi† Σ of H's	A	B	PARITY	$\overline{ERR}$	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and Generate Parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B Data to A Bus and Check Parity
X	X	L	X	X	X	X	NA	NA	H	Clear Error Flag Register
H	H	H L H H	No↑ No↑ ↑ ↑	X X Odd Even	X	Z	Z	Z	NC H H L	Isolation‡
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ In this mode, the $\overline{ERR}$ output, when clocked, shows inverted parity of the A bus.

logic diagram (positive logic)



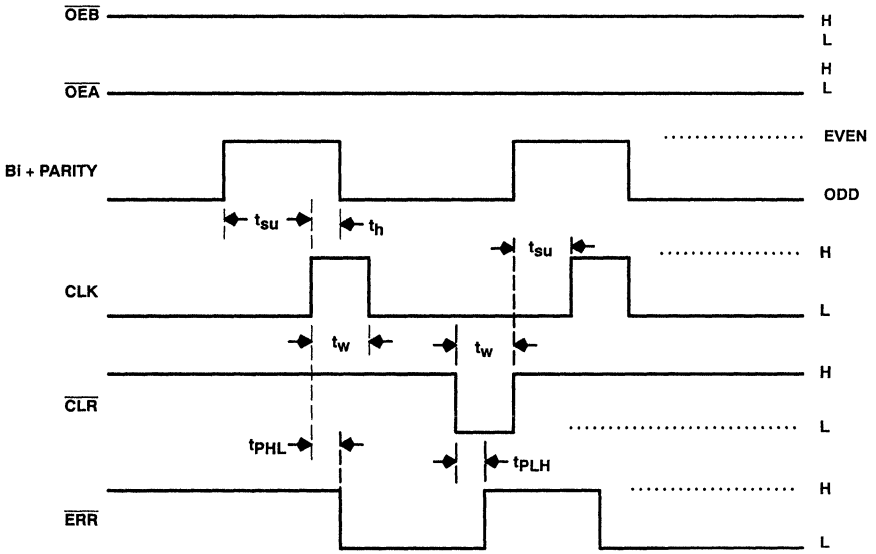
PRODUCT PREVIEW

Error-Flag Function Table

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION
$\overline{CLR}$	CLK	POINT "P"	$\overline{ERR}$ n-1	$\overline{ERR}$	
H	↑	H	H	H	Sample
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

$\overline{ERR}$ n-1 represents the state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, CLK, or point "P".

error-flag waveforms



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±225 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11833			74AC11833			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11833		74AC11833		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	$\overline{ERR}$	$V_O = V_{CC}$	5.5 V			0.5		10		5	µA
V_{OH}	All outputs except $\overline{ERR}$	I_{OH} = – 50 µA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = – 4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = – 50 mA†	5.5 V				3.85				
		I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 µA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	A or B ports, PARITY	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 10		± 5	µA
I_I	$\overline{OEA}$, $\overline{OEB}$, CLK, and $\overline{CLR}$	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	µA
C_i	$\overline{OEA}$, $\overline{OEB}$, CLK, and $\overline{CLR}$	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}	A or B ports, PARITY	$V_O = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 2)

			T_A = 25°C		54AC11833		74AC11833		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high	5		5		5		ns
		CLK low	5		5		5		
		$\overline{CLR}$ low	5		5		5		
t_{su}	Setup time before CLK↑	Bi and PARITY	14		14		14		ns
		$\overline{CLR}$ inactive	2		2		2		
t_h	Hold time after CLK ↑, Bi and PARITY		0		0		0		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

			T_A = 25°C		54AC11833		74AC11833		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high	5		5		5		ns
		CLK low	5		5		5		
		$\overline{CLR}$ low	5		5		5		
t_{su}	Setup time before CLK↑	Bi and PARITY	14		14		14		ns
		$\overline{CLR}$ inactive	2		2		2		
t_h	Hold time after CLK ↑, Bi and PARITY		0		0		0		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

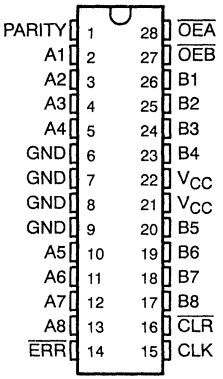
PARAMETER				TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	A to B	C_L = 50 pF, f = 1 MHz	87	pF
			B to A		60	
		Outputs disabled	A to B	C_L = 50 pF, f = 1 MHz	28	pF
			B to A		8	

PRODUCT PREVIEW

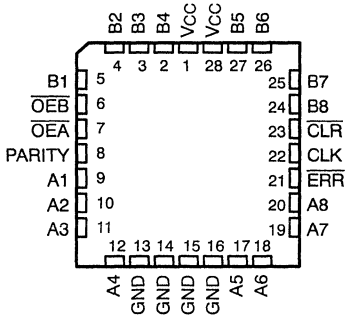
D3449, MARCH 1990–REVISED OCTOBER 1990

- **Inputs are TTL-Voltage Compatible**
- **High-Speed Bus Transceivers With Parity Generator/Checker**
- **Parity-Error-Flag Open-Drain Output**
- **Register for Storage of the Parity-Error Flag**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11833 . . . JT PACKAGE
74ACT11833 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11833 . . . FK PACKAGE
(TOP VIEW)



description

The 'ACT11833 is an 8-bit to 9-bit parity transceiver designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the $\overline{ERR}$ output will indicate whether or not an error in the B data has occurred. The output enable inputs $\overline{OEA}$ and $\overline{OEB}$ can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd output (PARITY) and monitors the parity of the I/O ports with an open-drain parity error flag ($\overline{ERR}$). $\overline{ERR}$ is clocked into the register on the rising edge of the CLK input. The error flag register is cleared with a low pulse on the $\overline{CLR}$ input. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The 54ACT11833 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11833 is characterized for operation from – 40°C to 85°C.

PRODUCT PREVIEW

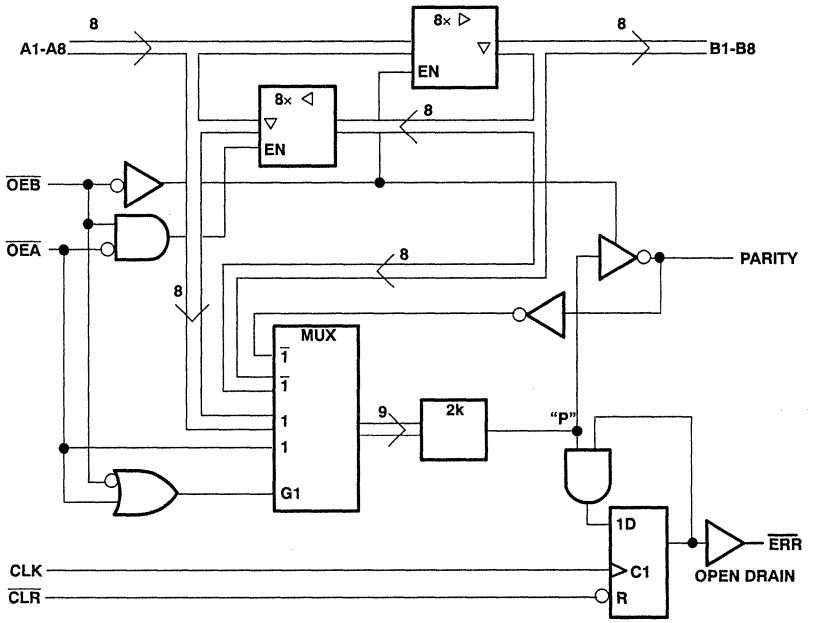
EPIC is a trademark of Texas Instruments Incorporated.

Function Table

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	Ai Σ of H's	BI† Σ of H's	A	B	PARITY	$\overline{ERR}$	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and Generate Parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B Data to A Bus and Check Parity
X	X	L	X	X	X	X	NA	NA	H	Clear Error Flag Register
H	H	H L H H	No↑ No↑ ↑ ↑	X X Odd Even	X	Z	Z	Z	NC H H L	Isolation‡
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ In this mode, the $\overline{ERR}$ output, when clocked, shows inverted parity of the A bus.

logic diagram (positive logic)



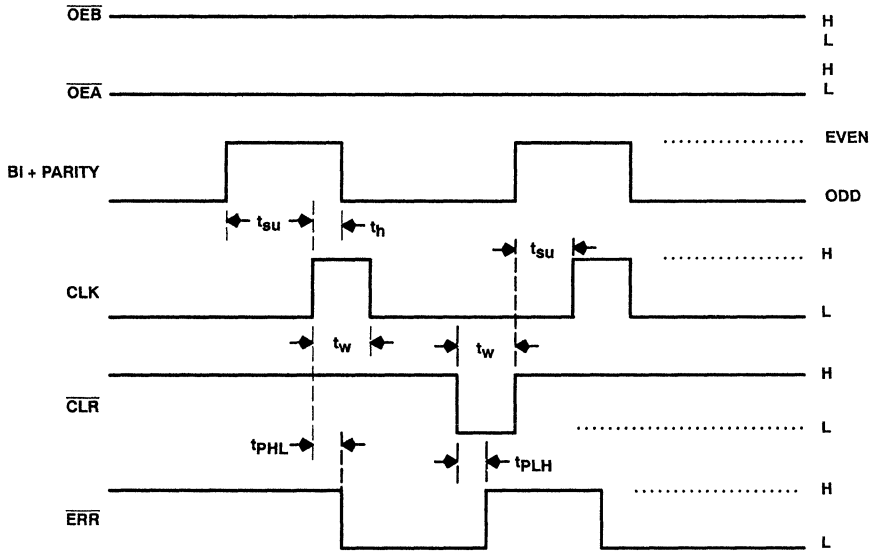
PRODUCT PREVIEW

Error-Flag Function Table

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION
$\overline{CLR}$	CLK	POINT "P"	$\overline{ERR}$ n-1	$\overline{ERR}$	
H	↑	H	H	H	Sample
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

$\overline{ERR}$ n-1 represents the state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, CLK, or point "P".

error-flag waveforms



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±225 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11833			74ACT11833			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11833		74ACT11833		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	All outputs except $\overline{ERR}$	I_{OH} = – 50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = – 50 mA†	5.5 V				3.85				
		I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	$\overline{OEA}$, $\overline{OEB}$, CLK, and $\overline{CLR}$	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{OZ}	A or B ports, PARITY‡	V_O = V_{CC} or GND	5.5 V			± 0.5		± 10		± 5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$\overline{OEA}$, $\overline{OEB}$, CLK, and $\overline{CLR}$	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports, PARITY	V_O = V_{CC} or GND	5 V		12						

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

			T_A = 25°C		54ACT11833		74ACT11833		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high	5		5		5		ns
		CLK low	5		5		5		
		$\overline{CLR}$ low	5		5		5		
t_{su}	Setup time before CLK↑	Bi and PARITY	14		14		14		ns
		$\overline{CLR}$ inactive	2		2		2		
t_h	Hold time after CLK ↑, Bi and PARITY		0		0		0		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

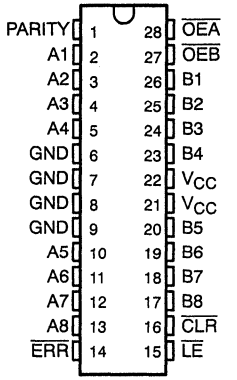
PARAMETER				TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	A to B	C_L = 50 pF,	f = 1 MHz	87	pF
			B to A			60	
		Outputs disabled	A to B	C_L = 50 pF,	f = 1 MHz	28	pF
			B to A			8	

PRODUCT PREVIEW

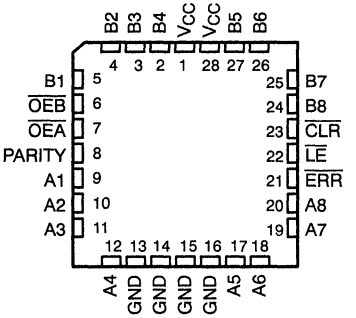
D3473, MARCH 1990

- **High-Speed Bus Transceivers With Parity Generator/Checker**
- **Parity-Error-Flag Open-Drain Output**
- **Register for Storage of the Parity-Error Flag**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11853 . . . JT PACKAGE
74AC11853 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11853 . . . FK PACKAGE
(TOP VIEW)



description

The 'AC11853 is an 8-bit to 9-bit parity transceiver designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the $\overline{ERR}$ output will indicate whether or not an error in the B data has occurred. The output-enable inputs $\overline{OEA}$ and $\overline{OEB}$ can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd output (PARITY) and monitors the parity of the I/O ports with an open-drain parity-error flag ($\overline{ERR}$). $\overline{ERR}$ can be either passed, sampled, stored, or cleared from the latch using the $\overline{LE}$ and $\overline{CLR}$ control inputs. The error flag register is cleared with a low pulse on the $\overline{CLR}$ input. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

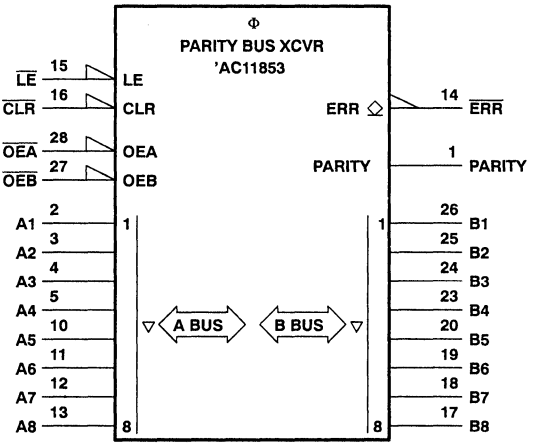
The 54AC11853 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11853 is characterized for operation from – 40°C to 85°C.

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic symbol†

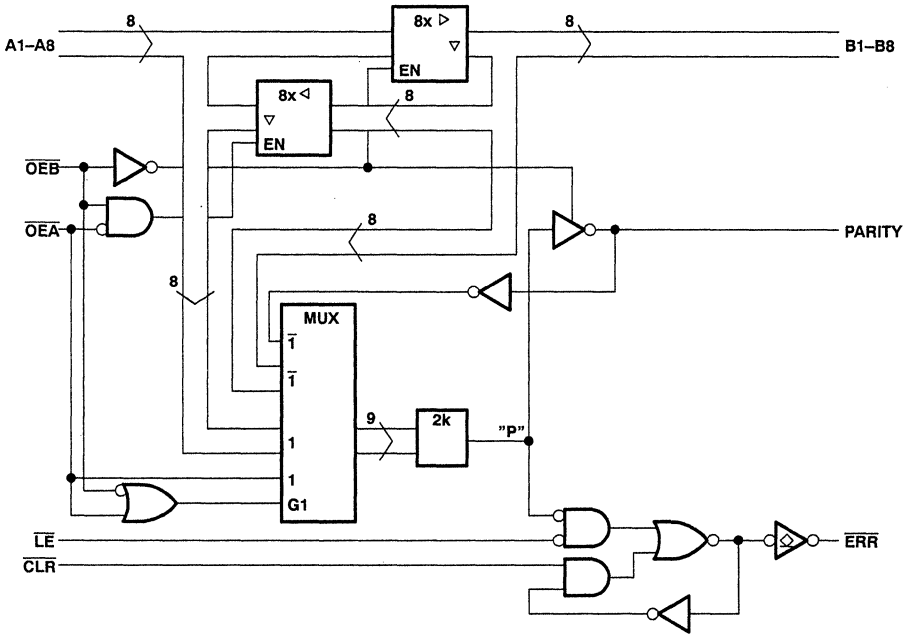


† This symbol is in accordance with ANSI/IEEE Std 91-1984.
Pin numbers shown are for DW, JT, and NT packages.

PRODUCT PREVIEW

D3473, MARCH 1990

logic diagram (positive logic)



FUNCTION TABLE

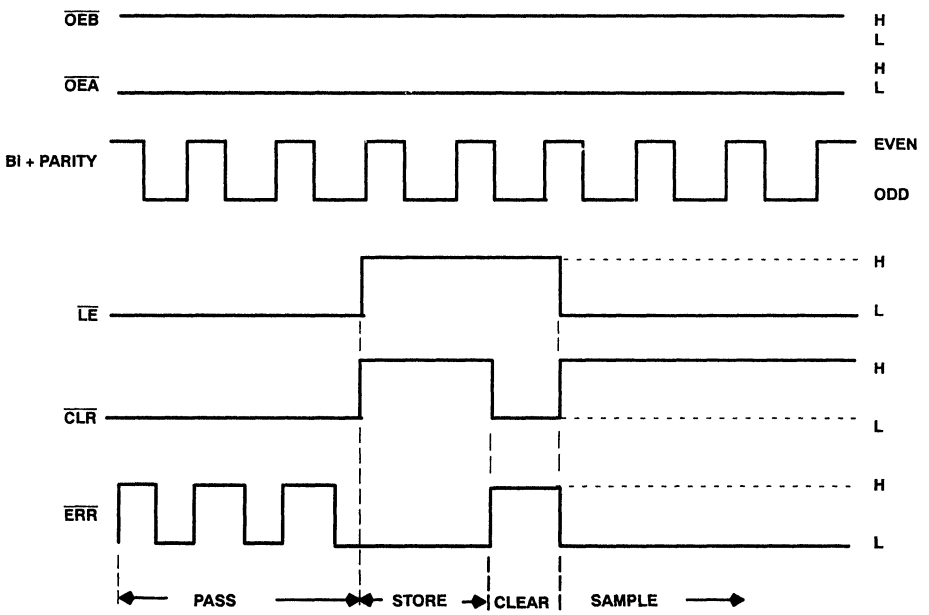
INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	$\overline{LE}$	AI Σ of H's	BI† Σ of H's	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and Generate Parity
H	L	X	L	NA	Odd Even	B	NA	NA	H L	B Data to A Bus and Check Parity
H	L	H	H	NA	X	X	NA	NA	NC	Store Error Flag
X	X	L	H	X	X	X	NA	NA	H	Clear Error Flag Register
H	H	H L X X	H H L L	X X L Odd H Even	X	Z	Z	Z	NC H H L	Isolation§ (Parity check)
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume the $\overline{ERR}$ output was previously high.
§ In this mode, the $\overline{ERR}$ output, when enabled, shows inverted parity of the A bus.

PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

error-flag waveforms



ERROR FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION
$\overline{LE}$	$\overline{CLR}$	POINT "P"	$\overline{ERR}_{n-1}$ †	$\overline{ERR}$	
L	L	L H	X	L H	PASS
L	H	L X H	X L H	L L H	SAMPLE
H	L	X	X	H	CLEAR
H	H	X	L H	L H	STORE

† ERRn-1 represents the state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, $\overline{LE}$, or point P.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND pins ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11853			74AC11853			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11853		74AC11853		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	$\overline{ERR}$	$V_O = V_{CC}$	5.5 V			0.5		10		5	μA
V_{OH}	All outputs except $\overline{ERR}$	$I_{OH} = -50$ μA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		$I_{OH} = -4$ mA	3 V	2.58			2.4		2.48		
		$I_{OH} = -24$ mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		$I_{OH} = -50$ mA†	5.5 V				3.85				
		$I_{OH} = -75$ mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	A or B ports, PARITY	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 10		± 5	μA
I_I	$\overline{OEA}$, $\overline{OEB}$, $\overline{LE}$, and $\overline{CLR}$	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μA
C_i	$\overline{OEA}$, $\overline{OEB}$, $\overline{LE}$, and $\overline{CLR}$	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}	A or B ports, PARITY	$V_O = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 2)

			T_A = 25°C		54AC11853		74AC11853		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{LE}$ high	5		5		5		ns
		$\overline{LE}$ low	5		5		5		
		$\overline{CLR}$ low	5		5		5		
t_{su}	Setup time before $\overline{LE}$↑	Bi and PARITY	14		14		14		ns
		$\overline{CLR}$ inactive	2		2		2		
t_h	Hold time, Bi and PARITY after $\overline{LE}$↑		0		0		0		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

			T_A = 25°C		54AC11853		74AC11853		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{LE}$ high	5		5		5		ns
		$\overline{LE}$ low	5		5		5		
		$\overline{CLR}$ low	5		5		5		
t_{su}	Setup time, before $\overline{LE}$↓	Bi and PARITY	14		14		14		ns
		$\overline{CLR}$ inactive	2		2		2		
t_h	Hold time, Bi and PARITY after $\overline{LE}$↓		0		0		0		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

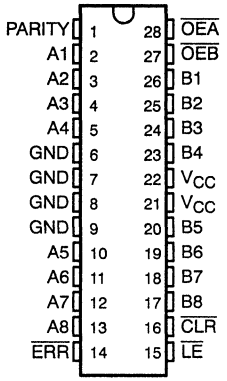
PARAMETER		TEST CONDITIONS			TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	A to B	C_L = 50 pF, f = 1 MHz	87	pF
			B to A		60	
		Outputs disabled	A to B		28	
			B to A		8	

PRODUCT PREVIEW

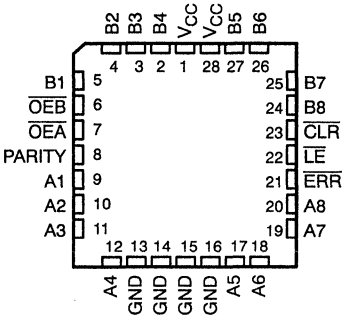
D3474, MARCH 1990–REVISED OCTOBER 1990

- **High-Speed Bus Transceivers With Parity Generator/Checker**
- **Parity-Error-Flag Open-Drain Output**
- **Register for Storage of the Parity-Error Flag**
- **Inputs are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11853 . . . JT PACKAGE
74ACT11853 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11853 . . . FK PACKAGE
(TOP VIEW)



description

The 'ACT11853 is an 8-bit to 9-bit parity transceiver designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the $\overline{ERR}$ output will indicate whether or not an error in the B data has occurred. The output-enable inputs $\overline{OEA}$ and $\overline{OEB}$ can be used to disable the device so that the buses are effectively isolated.

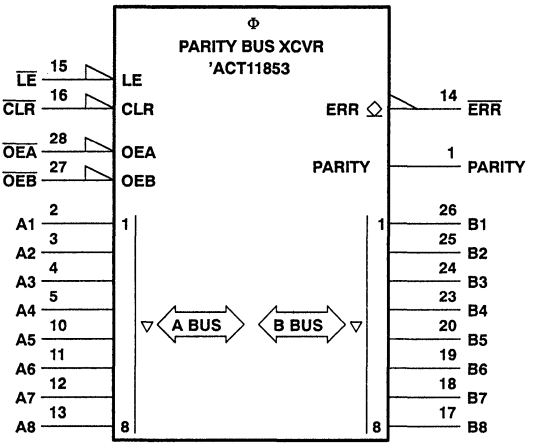
A 9-bit parity generator/checker generates a parity-odd output (PARITY) and monitors the parity of the I/O ports with an open-drain parity-error flag ($\overline{ERR}$). $\overline{ERR}$ can be either passed, sampled, stored, or cleared from the latch using the $\overline{LE}$ and $\overline{CLR}$ control inputs. The error flag register is cleared with a low pulse on the $\overline{CLR}$ input. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The 54ACT11853 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11853 is characterized for operation from – 40°C to 85°C.

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

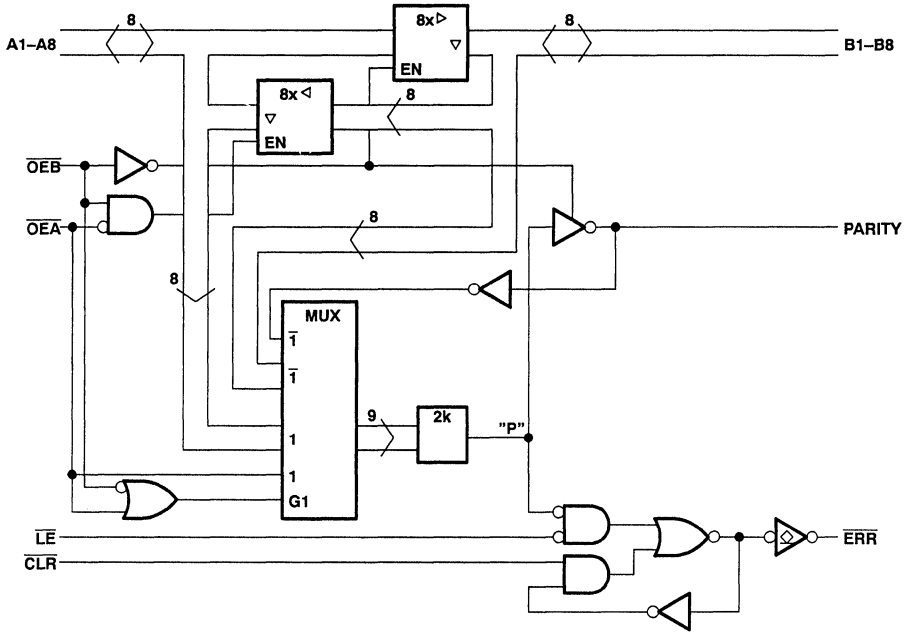
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.
Pin numbers shown are for DW, JT, and NT packages.

PRODUCT PREVIEW

logic diagram (positive logic)



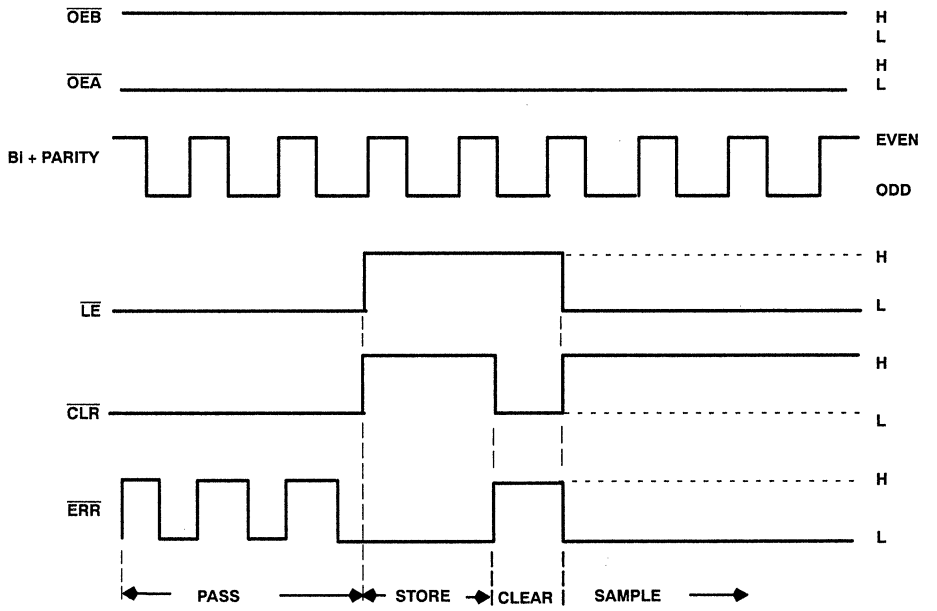
FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	$\overline{LE}$	AI Σ of H's	BI† Σ of H's	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and Generate Parity
H	L	X	L	NA	Odd Even	B	NA	NA	H L	B Data to A Bus and Check Parity
H	L	H	H	NA	X	X	NA	NA	NC	Store Error Flag
X	X	L	H	X	X	X	NA	NA	H	Clear Error Flag Register
H	H	H L X X	H H L L	X X L Odd H Even	X	Z	Z	Z	NC H H L	Isolation§ (Parity check)
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume the $\overline{ERR}$ output was previously high.
§ In this mode, the $\overline{ERR}$ output, when enabled, shows inverted parity of the A bus.

PRODUCT PREVIEW

error-flag waveforms



ERROR FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION
$\overline{LE}$	$\overline{CLR}$	POINT "P"	$\overline{ERR}_{n-1}$ †	$\overline{ERR}$	
L	L	L H	X	L H	PASS
L	H	L X H	X L H	L L H	SAMPLE
H	L	X	X	H	CLEAR
H	H	X	L H	L H	STORE

† ERRn-1 represents the state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, $\overline{LE}$, or point P.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND pins ..... ± 200 mA
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11853			74ACT11853			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			– 24			– 24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	– 55		125	– 40		85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11853		74ACT11853		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	All outputs except $\overline{ERR}$	I_{OH} = – 50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = – 50 mA†	5.5 V				3.85				
		I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	$\overline{OEA}$, $\overline{OEB}$, $\overline{LE}$, and $\overline{CLR}$	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{OZ}	A or B ports, PARITY‡	V_O = V_{CC} or GND	5.5 V			± 0.5		± 10		± 5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$\overline{OEA}$, $\overline{OEB}$, $\overline{LE}$, and $\overline{CLR}$	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports, PARITY	V_O = V_{CC} or GND	5 V		12						

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

			T_A = 25°C		54ACT11853		74ACT11853		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{LE}$ high	5		5		5		ns
		$\overline{LE}$ low	5		5		5		
		$\overline{CLR}$ low	5		5		5		
t_{su}	Setup time, before $\overline{LE}$↓	Bi and PARITY	14		14		14		ns
		$\overline{CLR}$ inactive	2		2		2		
t_h	Hold time, Bi and PARITY after $\overline{LE}$↓		0		0		0		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

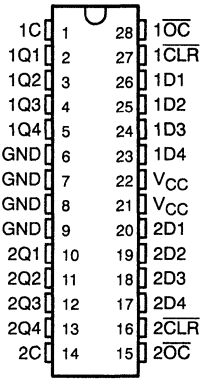
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	A to B	C_L = 50 pF, f = 1 MHz	87	pF
			B to A		60	
		Outputs disabled	A to B		28	
			B to A		8	

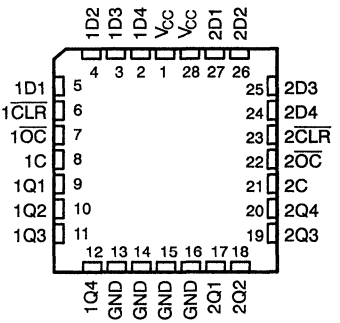
PRODUCT PREVIEW

- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11873 . . . JT PACKAGE
74AC11873 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11873 . . . FK PACKAGE
(TOP VIEW)



description

These dual 4-bit registers feature 3-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The dual 4-bit latches are transparent D-type. When the latch enable input (1C or 2C) is high, the (Q) outputs will follow the data (D) inputs in true form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When $\overline{CLR}$ goes low, the Q outputs go low independently of enable C. The outputs are in a high-impedance state when $\overline{OC}$ (output control) is at a high logic level.

The 54AC11873 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11873 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	C	D	Q
L	L	X	X	L
L	H	H	H	H
L	H	H	L	L
L	H	L	X	Q_0
H	X	X	X	Z

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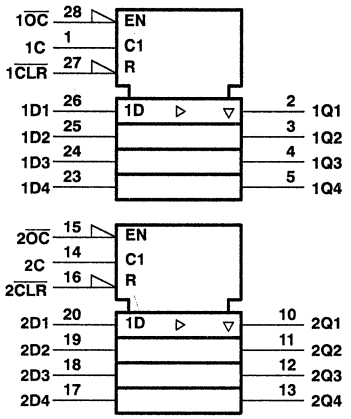
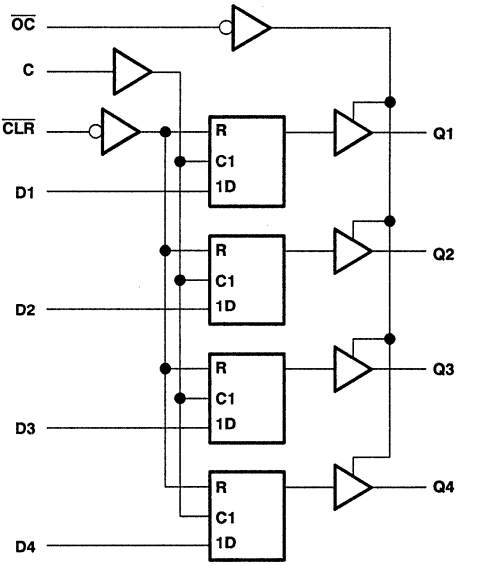
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, or NT packages.

logic diagram, each quad latch (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND pins ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11873			74AC11873			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			– 4			– 4	mA
		V_{CC} = 4.5 V			– 24			– 24	
		V_{CC} = 5.5 V			– 24			– 24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		– 55		125	– 40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11873		74AC11873		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 µA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OH} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			± 0.5		± 10		± 5	µA
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	µA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF
C_o	V_I = V_{CC} or GND	5 V		13.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 2)

PARAMETER			T_A = 25°C		54AC11873		74AC11873		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	5		5		5		ns
		C high	5		5		5		
t_{su}	Setup time, data before C↓	Data high	3		3		3		ns
		Data low	4		4		4		
t_h	Hold time, data after C↓	Data high	1		1		1		ns
		Data low	1		1		1		

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER			T_A = 25°C		54AC11873		74AC11873		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	5		5		5		ns
		C high	5		5		5		
t_{su}	Setup time, data before C↓	Data high	2		2		2		ns
		Data low	3		3		3		
t_h	Hold time, data after C↓	Data high	1		1		1		ns
		Data low	1		1		1		

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11873		74AC11873		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2.8	8.8	11.2	2.8	14.1	2.8	13	ns
t_{PHL}			2.8	9	11.2	2.8	13.6	2.8	12.7	
t_{PLH}	C	Q	3	9.4	11.8	3	14.9	3	13.6	ns
t_{PHL}			2.9	9.4	11.7	2.9	14.2	2.9	13.2	
t_{PHL}	$\overline{CLR}$	Q	2.3	8.2	10.3	2.3	12.2	2.3	11.5	ns
t_{PZH}	$\overline{OC}$	Q	1.8	6.4	8.4	1.8	10.5	1.8	9.7	ns
t_{PZL}			2.7	9.9	12.5	2.7	15.7	2.7	14.4	
t_{PHZ}	$\overline{OC}$	Q	3.8	6.8	8.4	3.8	9.4	3.8	9	ns
t_{PLZ}			3.5	6.8	8.5	3.5	9.5	3.5	9.1	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11873		74ACT11873		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2.2	5.5	7.3	2.2	9.2	2.2	8.4	ns
t_{PHL}			2.1	5.5	7.2	2.1	8.9	2.1	8.2	
t_{PLH}	C	Q	2.4	5.9	7.8	2.4	9.7	2.4	8.9	ns
t_{PHL}			2.2	5.8	7.6	2.2	9.4	2.2	8.7	
t_{PHL}	$\overline{CLR}$	Q	1.7	5.1	6.8	1.7	8.2	1.7	7.6	ns
t_{PZH}	$\overline{OC}$	Q	1.2	4.1	5.6	1.2	7	1.2	6.4	ns
t_{PZL}			1.9	5.5	7.3	1.9	9.2	1.9	8.5	
t_{PHZ}	$\overline{OC}$	Q	3.5	5.9	7.4	3.5	8.2	3.5	7.9	ns
t_{PLZ}			3.3	5.5	7	3.3	7.9	3.3	7.6	

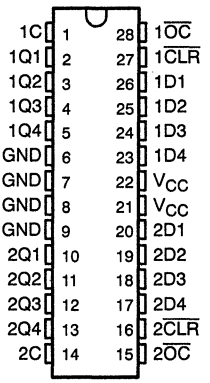
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

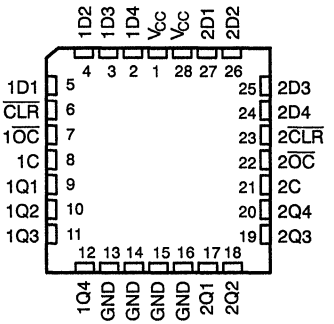
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	43	pF
		Outputs disabled		9	

- **Inputs are TTL-Voltage Compatible**
- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11873 . . . JT PACKAGE
74ACT11873 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11873 . . . FK PACKAGE
(TOP VIEW)



description

These dual 4-bit registers feature 3-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The dual 4-bit latches are transparent D-type. When the latch enable input (1C or 2C) is high, the (Q) outputs will follow the data (D) inputs in true form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When $\overline{CLR}$ goes low, the Q outputs go low independently of enable C. The outputs are in a high-impedance state when $\overline{OC}$ (output control) is at a high logic level.

The 54ACT11873 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11873 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	C	D	Q
L	L	X	X	L
L	H	H	H	H
L	H	H	L	L
L	H	L	X	Q_0
H	X	X	X	Z

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TEXAS INSTRUMENTS
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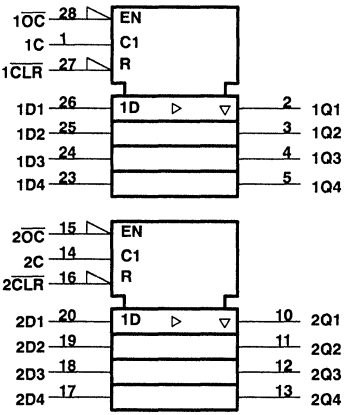
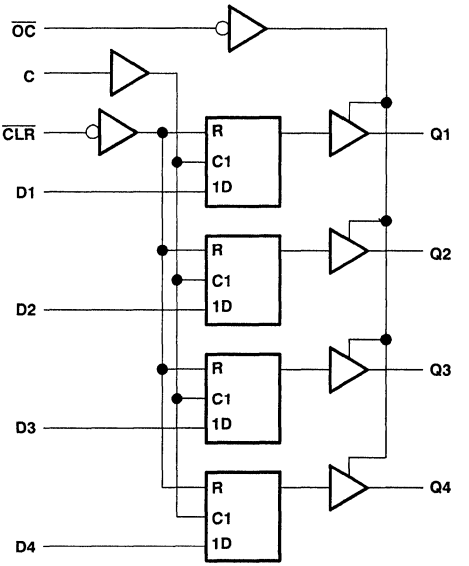
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, or NT packages.

logic diagram (positive logic)

each quad latch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND pins ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11873		74ACT11873		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		– 24		– 24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	– 55	125	– 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11873		74ACT11873		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 10		± 5	µA
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	µA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_o	$V_O = V_{CC}$ or GND	5 V		13.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER			T_A = 25°C		54ACT11873		74ACT11873		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	5		5		5		ns
		Enable C high	5		5		5		
t_{su}	Setup time, data before C↓	Data high	6		6		6		ns
		Data low	3		3		3		
t_h	Hold time, data after C↓	Data high	0		0		0		ns
		Data low	0		0		0		

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11873		74ACT11873		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	4.4	7.2	8.8	4.4	10.9	4.4	10	ns
t_{PHL}			3	6.6	9.1	3	10.9	3	10.2	
t_{PLH}	C	Q	4.7	8.1	10	4.7	12.3	4.7	11.3	ns
t_{PHL}			5.2	8.9	10.9	5.2	13.3	5.2	12.3	
t_{PHL}	$\overline{CLR}$	Q	2.9	6.5	9	2.9	10.7	2.9	10	ns
t_{PZH}	$\overline{OC}$	Q	1.9	4.9	7.1	1.9	8.5	1.9	8	ns
t_{PZL}			2.7	6.4	9.1	2.7	11.1	2.7	10.3	
t_{PHZ}	$\overline{OC}$	Q	5.7	8	9.5	5.7	10.6	5.7	10.2	ns
t_{PLZ}			5.2	7.8	9.1	5.2	10.2	5.2	9.8	

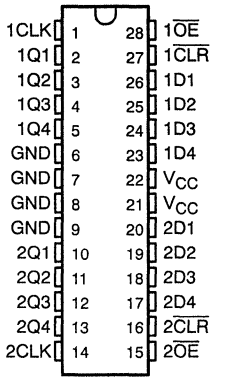
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

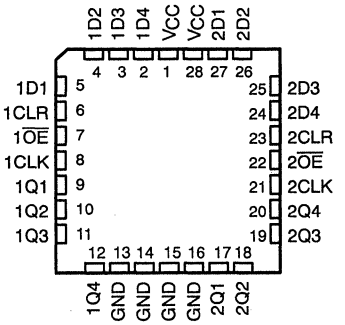
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	40	pF
		Outputs disabled		7	

- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Asynchronous Clear**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11874 . . . JT PACKAGE
74AC11874 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11874 . . . FK PACKAGE
(TOP VIEW)



description

The 54AC11874 and 74AC11874 contain dual 4-bit registers featuring 3-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, and working registers.

The edge-triggered flip-flops enter data on the low-to-high transition of the clock. The 'AC11874 has $\overline{CLR}$ inputs and noninverting outputs. Taking this input ($\overline{CLR}$) low causes the four Q outputs to go low independently of the clock.

The 54AC11874 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74AC11874 is characterized for operation from –40°C to 85°C.

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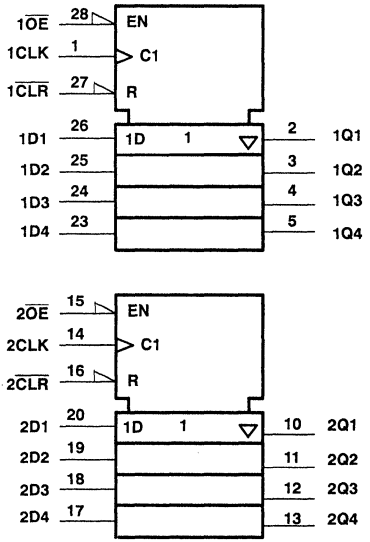
FUNCTION TABLE
(each flip-flop)

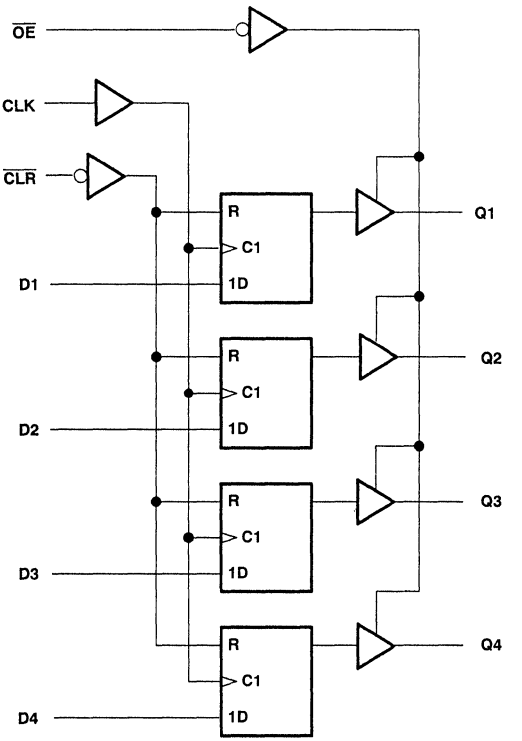
INPUTS				OUTPUT
$\overline{OE}$	$\overline{CLR}$	CLK	D	Q
L	L	X	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_O
H	X	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±200 mA
Storage temperature range ..... −55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11874			74AC11874			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11874		74AC11874		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			± 0.5		± 10		± 5	μA
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF
C_o	V_O = V_{CC} or GND	5 V		13.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 2)

PARAMETER			T_A = 25°C		54AC11874		74AC11874		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	60	0	60	0	60	MHz
t_w	Pulse duration	$\overline{CLR}$ low	4		4		4		ns
		CLK high or low	8.3		8.3		8.3		
t_{su}	Setup time before CLK↑	Data	3		3		3		ns
		$\overline{CLR}$ inactive	1.5		1.5		1.5		
t_h	Hold time after CLK↑	Data	1		1		1		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER			T_A = 25°C		54AC11874		74AC11874		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	125	0	125	0	125	MHz
t_w	Pulse duration	$\overline{CLR}$ low	4		4		4		ns
		CLK high or low	4		4		4		
t_{su}	Setup time before CLK↑	Data	2		2		2		ns
		$\overline{CLR}$ inactive	1.5		1.5		1.5		
t_h	Hold time after CLK↑	Data	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3 V ± 0.3 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11874		74AC11874		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			60			60		60		MHz
t_{PLH}	CLK	Any Q	2.9	7.3	11	2.9	13.5	2.9	12.5	ns
t_{PHL}			3.7	8.8	13.1	3.7	15.6	3.7	14.6	
t_{PHL}	$\overline{CLR}$	Any Q	3.9	9.3	14	3.9	16.8	3.9	15.7	ns
t_{PZH}	$\overline{OE}$	Any Q	2.1	5.6	8.7	2.1	10.7	2.1	9.8	ns
t_{PZL}			3.1	8.4	13.1	3.1	16	3.1	14.9	
t_{PHZ}	$\overline{OE}$	Any Q	4	6.2	8.2	4	8.9	4	8.7	ns
t_{PLZ}			3.9	6.3	8.5	3.9	9.3	3.9	9	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11874		74AC11874		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125			125		125		MHz
t_{PLH}	CLK	Any Q	2.3	5.2	7.4	2.3	9	2.3	8.3	ns
t_{PHL}			2.9	6.1	8.6	2.9	10.3	2.9	9.6	
t_{PHL}	$\overline{CLR}$	Any Q	2.9	6.3	8.9	2.9	10.7	2.9	10	ns
t_{PZH}	$\overline{OE}$	Any Q	1.5	4	5.9	1.5	7.1	1.5	6.6	ns
t_{PZL}			2.3	5.4	7.8	2.3	9.5	2.3	8.8	
t_{PHZ}	$\overline{OE}$	Any Q	3.8	5.7	7.3	3.8	8	3.8	7.7	ns
t_{PLZ}			3.7	5.5	7.1	3.7	7.8	3.7	7.5	

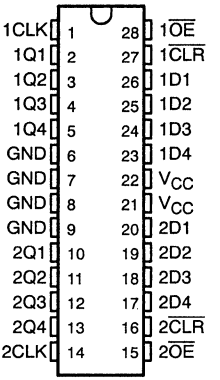
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

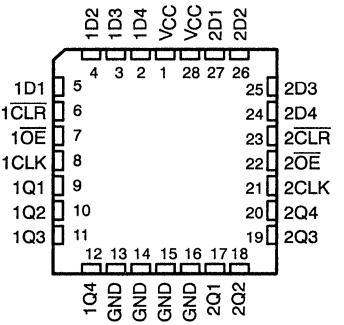
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF,	f = 1 MHz	31	pF
		Outputs disabled			13	

- **Inputs are TTL-Voltage Compatible**
- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Asynchronous Clear**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11874 . . . JT PACKAGE
74ACT11874 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11874 . . . FK PACKAGE
(TOP VIEW)



description

The 54ACT11874 and 74ACT11874 contain dual 4-bit registers featuring 3-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, and working registers.

The edge-triggered flip-flops enter data on the low-to-high transition of the clock. The 'ACT11874 has $\overline{CLR}$ inputs and noninverting outputs. Taking $\overline{CLR}$ low causes the four Q outputs to go low independently of the clock.

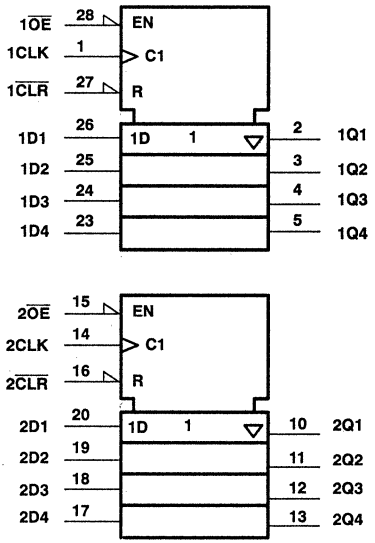
The 54ACT11874 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11874 is characterized for operation from – 40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each flip-flop)

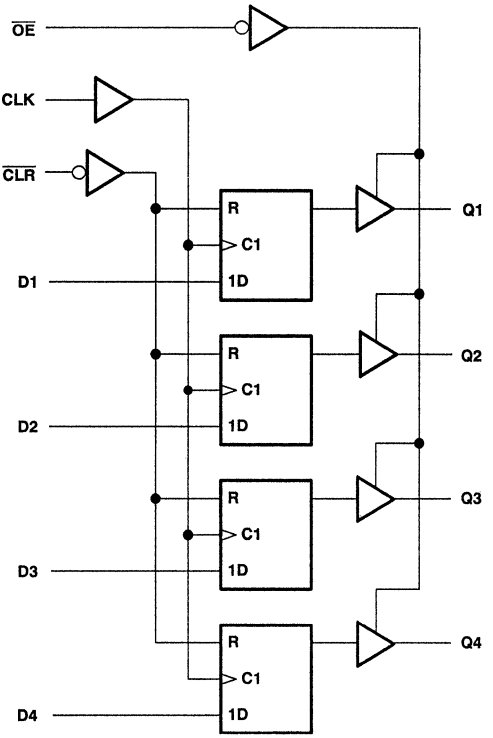
INPUTS				OUTPUT
$\overline{OE}$	$\overline{CLR}$	CLK	D	Q
L	L	X	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, V_I (see Note 1) ..... -0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1) ..... -0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND pins ..... ± 200 mA
Storage temperature range ..... $-55°C$ to $150°C$

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11874		74ACT11874		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			54ACT11874		74ACT11874		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50$ μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24$ mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50$ mA‡	5.5 V				3.85				
	$I_{OH} = -75$ mA‡	5.5 V						3.85		
V_{OL}	$I_{OL} = 50$ μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	$I_{OL} = 24$ mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	$I_{OL} = 50$ mA‡	5.5 V					1.65			
	$I_{OL} = 75$ mA‡	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_o	$V_O = V_{CC}$ or GND	5 V		13.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER			T_A = 25°C		54ACT11874		74ACT11874		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	125	0	125	0	125	MHz
t_w	Pulse duration	$\overline{CLR}$ low	4		4		4		ns
		CLK high or low	4		4		4		
t_{su}	Setup time before CLK↑	Data	5		5		5		ns
		$\overline{CLR}$ low	2		2		2		
t_h	Hold time after CLK↑	Data	1		1		1		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11874		74ACT11874		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125			125		125		MHz
t_{PLH}	CLK	Any Q	3.7	6.6	8.4	3.7	10.2	3.7	9.4	ns
t_{PHL}			4.1	7.6	9.5	4.1	11.3	4.1	10.6	
t_{PHL}	$\overline{CLR}$	Any Q	3.5	7.8	10.5	3.5	12.7	3.5	11.8	ns
t_{PZH}	$\overline{OE}$	Any Q	1.6	4.6	6.7	1.6	7.9	1.6	7.4	ns
t_{PZL}			2.4	6	8.6	2.4	10.2	2.4	9.5	
t_{PHZ}	$\overline{OE}$	Any Q	5.4	7.4	8.9	5.4	9.7	5.4	9.4	ns
t_{PLZ}			4.9	7.1	8.5	4.9	9.5	4.9	9.1	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

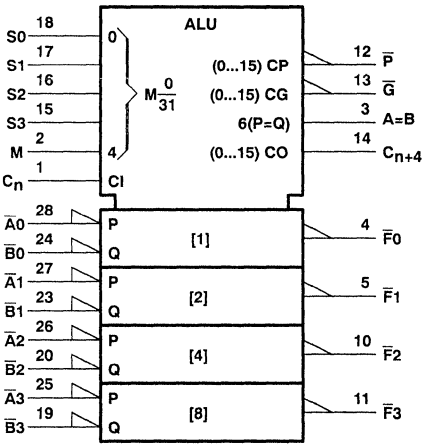
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF,	f = 1 MHz	35	pF
		Outputs disabled			17	

D3479, MARCH 1990

- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes: Addition, Subtraction, Shift Operand A One Position, Magnitude Comparison, Plus Twelve Other Arithmetic Operations
- Logic Function Modes Exclusive-OR, Comparator, AND, NAND, OR, NOR, Plus Ten Other Logic Operations
- Provides Status Register Checks
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

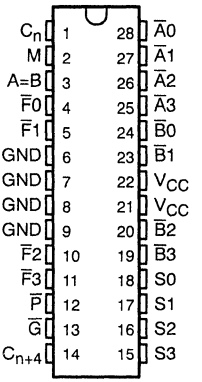
logic symbol†



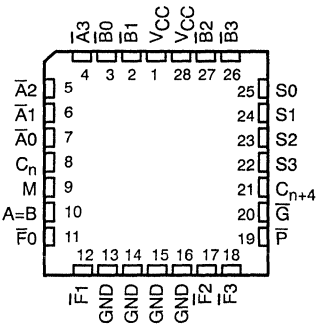
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

EPIC is a trademark of Texas Instruments Incorporated.

54AC11881 . . . JT PACKAGE
74AC11881 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11881 . . . FK PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

signal designations

In both Figures 1 and 2, the polarity indicators (▷) indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2.

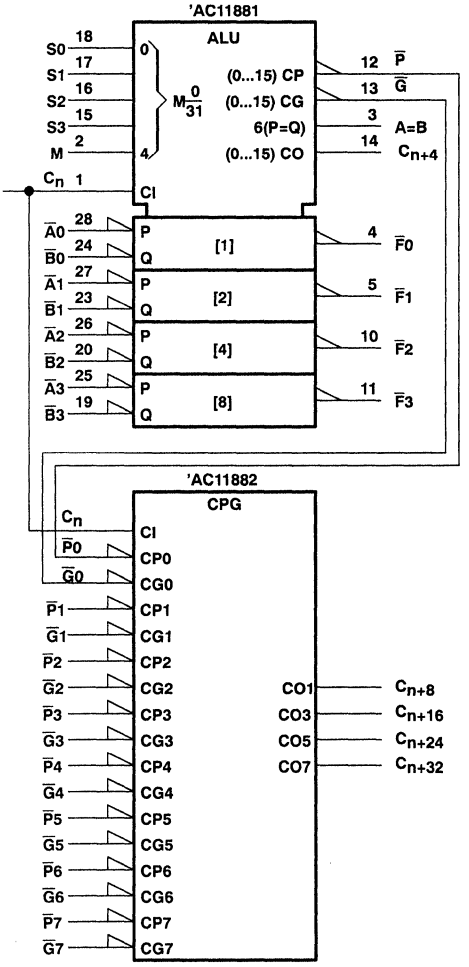


FIGURE 1
(USE WITH TABLE 1)

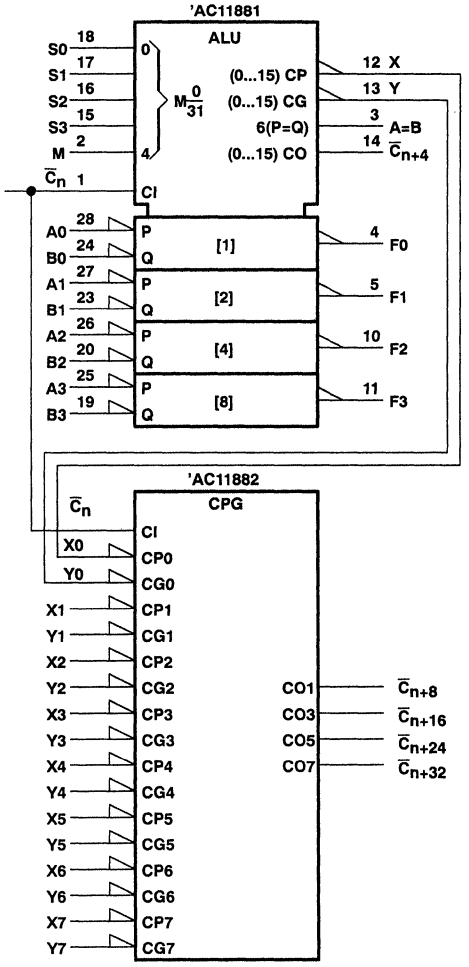


FIGURE 2
(USE WITH TABLE 2)

Pin numbers shown are for DW, JT, and NT packages.

PRODUCT PREVIEW

description

The 'AC11881 arithmetic logic units (ALU)/function generators have a complexity of 77 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs, $\overline{G}$ and $\overline{P}$, for the four bits in the package. When used in conjunction with the 54AC11882 or 74AC11882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AC11882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without enternal circuitry.

The 'AC11881 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	28	24	27	23	26	20	25	19	4	5	10	11	1	14	12	13
Active-low data (Table 1)	$\overline{A}0$	$\overline{B}0$	$\overline{A}1$	$\overline{B}1$	$\overline{A}2$	$\overline{B}2$	$\overline{A}3$	$\overline{B}3$	$\overline{F}0$	$\overline{F}1$	$\overline{F}2$	$\overline{F}3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition, where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

The 'AC11881 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2,F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU must be in the subtract mode with C_n=H when performing this comparison. The A=B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	$A \geq B$	$A \leq B$
H	L	$A < B$	$A > B$
L	H	$A > B$	$A < B$
L	L	$A \leq B$	$A \geq B$

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

The 'AC11881 has the same pinout and same functionality as the 'AC11181 except for the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs when the device is in the logic mode (M = H).

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description (continued)

In the logic mode, the 'ACT11881 provides the user with a status check on the input words A and B and the output word F. While in the logic mode, the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs supply status information based upon the following logical combinations:

$\overline{P} = F0 + F1 + F2 + F3$
$\overline{G} = H$
$C_{n+4} = PC_n$.

Function Tables for Input Bits Equal/Not Equal

S0 = S3 = H, S1 = S2 = L, AND M = H

C_n	DATA INPUTS				OUTPUTS		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$\overline{A}0 = \overline{B}0$	$\overline{A}1 = \overline{B}1$	$\overline{A}2 = \overline{B}2$	$\overline{A}3 = \overline{B}3$	H	L	H
L	$\overline{A}0 = \overline{B}0$	$\overline{A}1 = \overline{B}1$	$\overline{A}2 = \overline{B}2$	$\overline{A}3 = \overline{B}3$	H	L	L
X	$\overline{A}0 \neq \overline{B}0$	X	X	X	H	H	L
X	X	$\overline{A}1 \neq \overline{B}1$	X	X	H	H	L
X	X	X	$\overline{A}2 \neq \overline{B}2$	X	H	H	L
X	X	X	X	$\overline{A}3 \neq \overline{B}3$	H	H	L

S0 = S1 = S3 = L, S2 = H, AND M = H

C_n	DATA INPUTS				OUTPUTS		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$\overline{A}0$ or $\overline{B}0$ = L	$\overline{A}1$ or $\overline{B}1$ = L	$\overline{A}2$ or $\overline{B}2$ = L	$\overline{A}3$ or $\overline{B}3$ = L	H	L	H
L	$\overline{A}0$ or $\overline{B}0$ = L	$\overline{A}1$ or $\overline{B}1$ = L	$\overline{A}2$ or $\overline{B}2$ = L	$\overline{A}3$ or $\overline{B}3$ = L	H	L	L
X	$\overline{A}0 = \overline{B}0$ = H	X	X	X	H	H	L
X	X	$\overline{A}1 = \overline{B}1$ = H	X	X	H	H	L
X	X	X	$\overline{A}2 = \overline{B}2$ = H	X	H	H	L
X	X	X	X	$\overline{A}3 = \overline{B}3$ = H	H	H	L

The combination of signals on the S3 through S0 control lines determine the operation performed on the data words to generate the output bits $\overline{F}i$. By monitoring the $\overline{P}$ and C_{n+4} outputs, the user can determine if all pairs of input bits are equal (see table above) or if any pair of inputs are both high (see table above). The 'ACT11881 has the unique feature of providing an A = B status while the exclusive-OR ($\oplus$) function is being utilized. When the control inputs (S3, S2, S1, S0) equal H, L, L, H; a status check is generated to determine whether all pairs ($\overline{A}i$, $\overline{B}i$) are equal in the following manner: $\overline{P}$ = (A0 $\oplus$ B0) + (A1 $\oplus$ B1) + (A2 $\oplus$ B2) + (A3 $\oplus$ B3). This unique bit-by-bit comparison of the data words, which is available on the totem-pole $\overline{P}$ output, is particularly useful when cascading 'ACT11881s. As the A = B condition is sensed in the first stage, the signal is propagated through the same ports used for carry generation in the arithmetic mode ($\overline{P}$ and $\overline{G}$). Thus, the A = B status is transmitted to the second stage more quickly without the need for external multiplexing logic. The A = B open-drain output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs ($\overline{A}i$, $\overline{B}i$) being high, it is necessary to set the control lines (S3, S2, S1, S0) to L, H, L, L. The data pairs will then be ANDed together and the results ORed in the following manner: $\overline{P} = \overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$.

S3	S2	S1	S0	M	$\overline{P} = F0 + F1 + F2 + F3$
L	H	L	L	H	$\overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$
H	L	L	H	H	(A0 $\oplus$ B0) + (A1 $\oplus$ B1) + (A2 $\oplus$ B2) + (A3 $\oplus$ B3)

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Table 1. Logic Functions and Arithmetic Operations (Active-Low)

SELECTION				ACTIVE-LOW DATA		
S3	S2	S1	S0	M = H	M = L; ARITHMETIC OPERATIONS	
				LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \overline{A} + B$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	$F = \overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A + \overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	$F = \overline{A}B$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

Table 2. Logic Functions and Arithmetic Operations (Active-High)

SELECTION				ACTIVE-HIGH DATA		
S3	S2	S1	S0	M = H	M = L; ARITHMETIC OPERATIONS	
				LOGIC FUNCTIONS	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	$F = \overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	$F = \overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	H	L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

† Each bit is shifted to the next more significant position.

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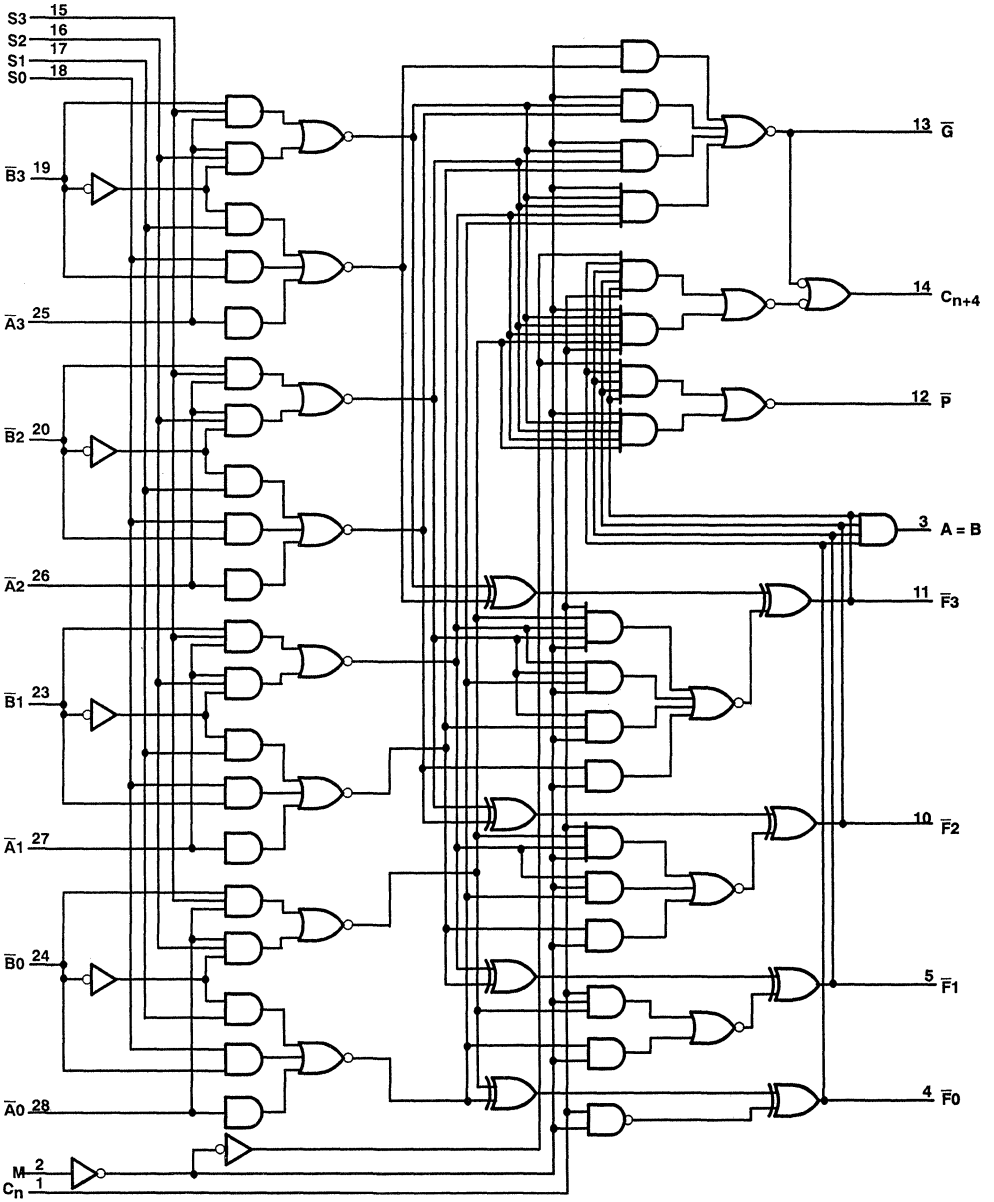
logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

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TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±200mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11881			74AC11881			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current, All outputs except A=B	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11881		74AC11881		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	A = B	$V_O = V_{CC}$	5.5 V			0.5		10		5	μA
V_{OH}		$I_{OH} = -50$ μA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		$I_{OH} = -4$ mA	3 V	2.58			2.4		2.48		
		$I_{OH} = -24$ mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		$I_{OH} = -50$ mA†	5.5 V				3.85				
		$I_{OH} = -75$ mA†	5.5 V						3.85		
V_{OL}		$I_{OL} = 50$ μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		$I_{OL} = 12$ mA	3 V			0.36		0.5		0.44	
		$I_{OL} = 24$ mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		$I_{OL} = 50$ mA†	5.5 V					1.65			
		$I_{OL} = 75$ mA†	5.5 V							1.65	
I_I		$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μA
C_i		$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_o	A = B	$V_O = V_{CC}$ or GND	5 V		11						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	161	pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

DIFF Mode Test Table

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 2)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PLH}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

DIFF Mode Test Table

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 2)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	In-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	In-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH}	$\overline{A}i$	None	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PLH}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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PARAMETER MEASUREMENT INFORMATION

DIFF Mode Test Table (Continued)

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 2)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or Any $\overline{F}$	In-Phase
t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or Any $\overline{F}$	In-Phase
t_{PLH}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	In-Phase
t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	In-Phase

Logic Mode Test Table

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 2)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$, and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$, and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$, and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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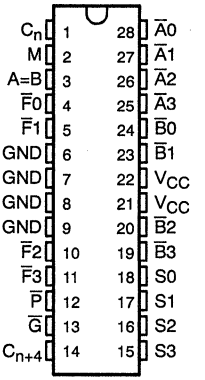
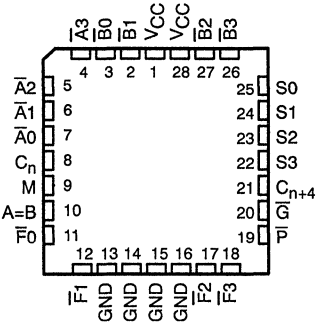
- Inputs are TTL-Voltage Compatible
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes: Addition, Subtraction, Shift Operand A One Position, Magnitude Comparison, Plus Twelve Other Arithmetic Operations
- Logic Function Modes Exclusive-OR, Comparator, AND, NAND, OR, NOR, Plus Ten Other Logic Operations
- Provides Status Register Checks
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

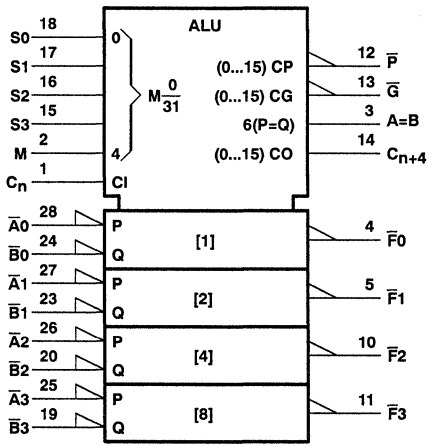
54ACT11881 . . . JT OR JW PACKAGE
74ACT11881 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11881 . . . FK PACKAGE
(TOP VIEW)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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signal designations

In both Figures 1 and 2, the polarity indicators (▷) indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2.

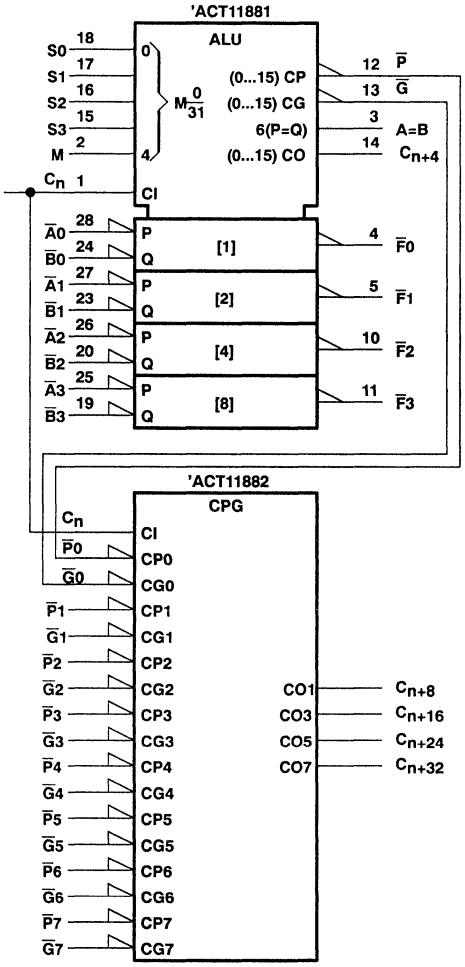

FIGURE 1
(USE WITH TABLE 1)

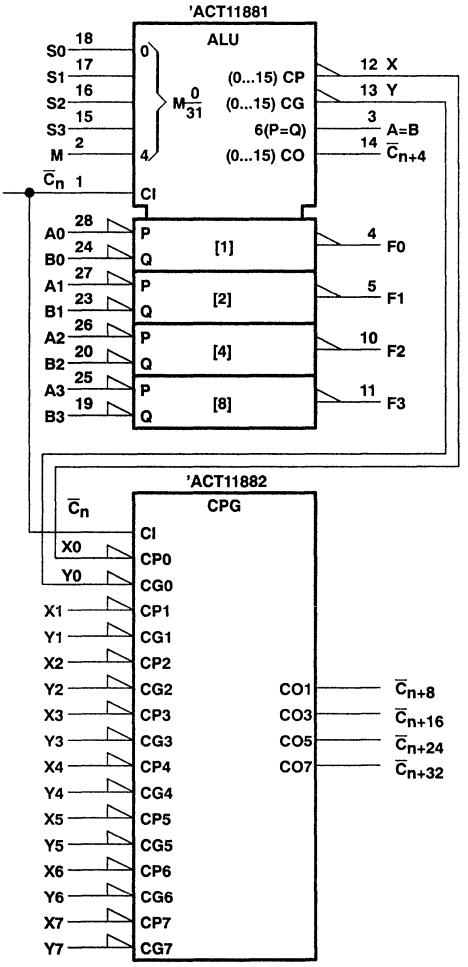

FIGURE 2
(USE WITH TABLE 2)

Pin numbers shown are for DW, JT, and NT packages.

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description

The 'ACT11881 arithmetic logic units (ALU)/function generators have a complexity of 77 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs, $\overline{G}$ and $\overline{P}$, for the four bits in the package. When used in conjunction with the 54ACT11882 or 74ACT11882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'ACT11882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without enternal circuitry.

The 'ACT11881 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	28	24	27	23	26	20	25	19	4	5	10	11	1	14	12	13
Active-low data (Table 1)	$\overline{A}0$	$\overline{B}0$	$\overline{A}1$	$\overline{B}1$	$\overline{A}2$	$\overline{B}2$	$\overline{A}3$	$\overline{B}3$	$\overline{F}0$	$\overline{F}1$	$\overline{F}2$	$\overline{F}3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition, where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

The 'ACT11881 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2,F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU must be in the subtract mode with C_n=H when performing this comparison. The A=B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

The 'ACT11881 has the same pinout and same functionality as the 'ACT11181 except for the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs when the device is in the logic mode (M = H).

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description (continued)

In the logic mode, the 'ACT11881 provides the user with a status check on the input words A and B and the output word F. While in the logic mode, the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs supply status information based upon the following logical combinations:

$\overline{P} = F0 + F1 + F2 + F3$
$\overline{G} = H$
$C_{n+4} = PC_n$.

Function Tables for Input Bits Equal/Not Equal

S0 = S3 = H, S1 = S2 = L, AND M = H

C_n	DATA INPUTS				OUTPUTS		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$\overline{A}0 = \overline{B}0$	$\overline{A}1 = \overline{B}1$	$\overline{A}2 = \overline{B}2$	$\overline{A}3 = \overline{B}3$	H	L	H
L	$\overline{A}0 = \overline{B}0$	$\overline{A}1 = \overline{B}1$	$\overline{A}2 = \overline{B}2$	$\overline{A}3 = \overline{B}3$	H	L	L
X	$\overline{A}0 \neq \overline{B}0$	X	X	X	H	H	L
X	X	$\overline{A}1 \neq \overline{B}1$	X	X	H	H	L
X	X	X	$\overline{A}2 \neq \overline{B}2$	X	H	H	L
X	X	X	X	$\overline{A}3 \neq \overline{B}3$	H	H	L

S0 = S1 = S3 = L, S2 = H, AND M = H

C_n	DATA INPUTS				OUTPUTS		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$\overline{A}0$ or $\overline{B}0$ = L	$\overline{A}1$ or $\overline{B}1$ = L	$\overline{A}2$ or $\overline{B}2$ = L	$\overline{A}3$ or $\overline{B}3$ = L	H	L	H
L	$\overline{A}0$ or $\overline{B}0$ = L	$\overline{A}1$ or $\overline{B}1$ = L	$\overline{A}2$ or $\overline{B}2$ = L	$\overline{A}3$ or $\overline{B}3$ = L	H	L	L
X	$\overline{A}0 = \overline{B}0$ = H	X	X	X	H	H	L
X	X	$\overline{A}1 = \overline{B}1$ = H	X	X	H	H	L
X	X	X	$\overline{A}2 = \overline{B}2$ = H	X	H	H	L
X	X	X	X	$\overline{A}3 = \overline{B}3$ = H	H	H	L

The combination of signals on the S3 through S0 control lines determine the operation performed on the data words to generate the output bits $\overline{F}i$. By monitoring the $\overline{P}$ and C_{n+4} outputs, the user can determine if all pairs of input bits are equal (see table above) or if any pair of inputs are both high (see table above). The 'ACT11881 has the unique feature of providing an A = B status while the exclusive-OR ($\oplus$) function is being utilized. When the control inputs (S3, S2, S1, S0) equal H, L, L, H; a status check is generated to determine whether all pairs ($\overline{A}i$, $\overline{B}i$) are equal in the following manner: $\overline{P} = (A0 \oplus B0) + (A1 \oplus B1) + (A2 \oplus B2) + (A3 \oplus B3)$. This unique bit-by-bit comparison of the data words, which is available on the totem-pole $\overline{P}$ output, is particularly useful when cascading 'ACT11881s. As the A = B condition is sensed in the first stage, the signal is propagated through the same ports used for carry generation in the arithmetic mode ($\overline{P}$ and $\overline{G}$). Thus, the A = B status is transmitted to the second stage more quickly without the need for external multiplexing logic. The A = B open-drain output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs ($\overline{A}i$, $\overline{B}i$) being high, it is necessary to set the control lines (S3, S2, S1, S0) to L, H, L, L. The data pairs will then be ANDed together and the results ORed in the following manner: $\overline{P} = \overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$.

S3	S2	S1	S0	M	$\overline{P} = F0 + F1 + F2 + F3$
L	H	L	L	H	$\overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$
H	L	L	H	H	$(A0 \oplus B0) + (A1 \oplus B1) + (A2 \oplus B2) + (A3 \oplus B3)$

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Table 1

SELECTION				ACTIVE-LOW DATA		
S3	S2	S1	S0	M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS C_n = L (no carry)	 C_n = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \overline{A} + B$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{A + B}$	F = A PLUS $(A + \overline{B})$	F = A PLUS $(A + \overline{B})$ PLUS 1
L	H	L	H	$F = \overline{B}$	F = AB PLUS $(A + \overline{B})$	F = AB PLUS $(A + \overline{B})$ PLUS 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A + \overline{B}$	$F = A + \overline{B}$	F = $(A + \overline{B})$ PLUS 1
H	L	L	L	$F = \overline{A}B$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	$F = A\overline{B}$ PLUS (A + B)	$F = A\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	$F = A\overline{B}$ PLUS A	$F = A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

Table 2

SELECTION				ACTIVE-HIGH DATA		
S3	S2	S1	S0	M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS $\overline{C}_n$ = H (no carry)	 $\overline{C}_n$ = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	$F = \overline{A}B$	$F = A + \overline{B}$	F = $(A + \overline{B})$ PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{AB}$	$F = A$ PLUS $A\overline{B}$	$F = A$ PLUS $A\overline{B}$ PLUS 1
L	H	L	H	$F = \overline{B}$	F = (A + B) PLUS $A\overline{B}$	$F = A$ PLUS $A\overline{B}$ PLUS 1
L	H	H	L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A\overline{B}$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = $(A + \overline{B})$ PLUS AB	F = $(A + \overline{B})$ PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	$F = A + \overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = $(A + \overline{B})$ PLUS A	F = $(A + \overline{B})$ PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

† Each bit is shifted to the next more significant position.

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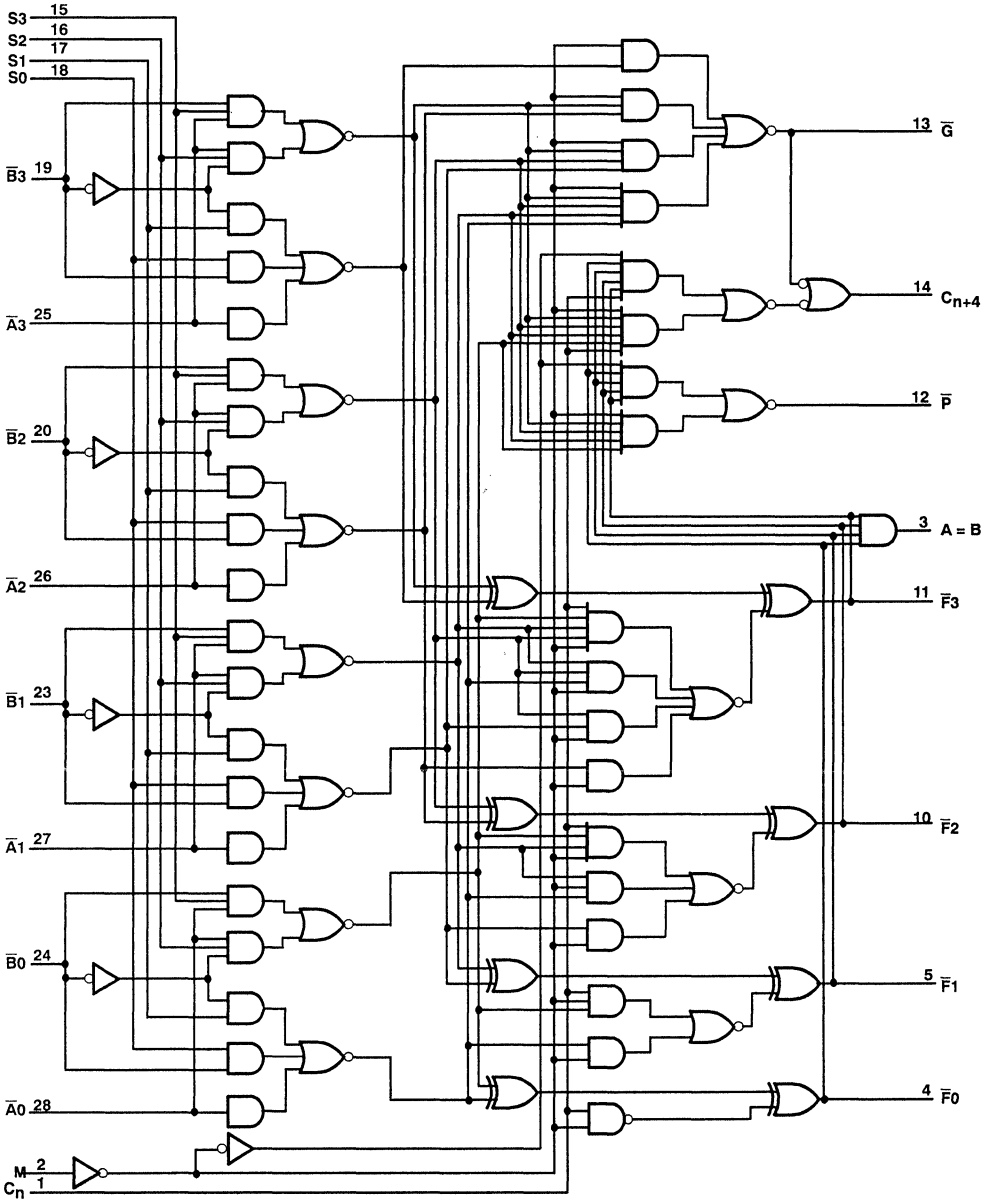
logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ± 200mA
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11881		74ACT11881		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		– 24		– 24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	– 55	125	– 40	85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11881		74ACT11881		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	A = B	$V_O = V_{CC}$	5.5 V			0.5		10		5	μA
V_{OH}		$I_{OH} = -50$ μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		$I_{OH} = -24$ mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		$I_{OH} = -50$ mA†	5.5 V				3.85				
		$I_{OH} = -75$ mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I		$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}‡		$V_I = V_{CC}$ or GND	5.5 V			0.9		1		1	mA
C_i		$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_o	A = B	$V_O = V_{CC}$ or GND	5 V		11						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	170	pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

SUM Mode Test Table

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 2)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PLH}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

DIFF Mode Test Table

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 2)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	In-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	In-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH}	$\overline{A}i$	None	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PLH}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase
t_{PLH}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or Any $\overline{F}$	In-Phase
t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or Any $\overline{F}$	In-Phase
t_{PLH}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	In-Phase
t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	In-Phase

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

Logic Mode Test Table

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE 2)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$, and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$, and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$, and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

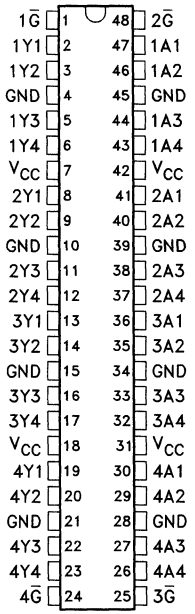
PRODUCT PREVIEW

ACL Widebus™ Products

TI0281—D3605, JULY 1990—REVISED NOVEMBER 1990

- **Members of the Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16240 ... WD PACKAGE
74AC16240 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16240 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical $\overline{G}$ (active-low output enable) inputs. The 'AC16240 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 54AC16240 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC16240 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE, EACH SECTION

INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	L
L	L	H
H	X	Z

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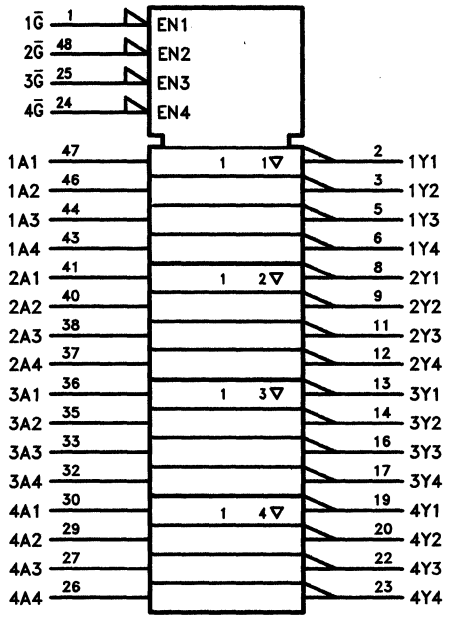
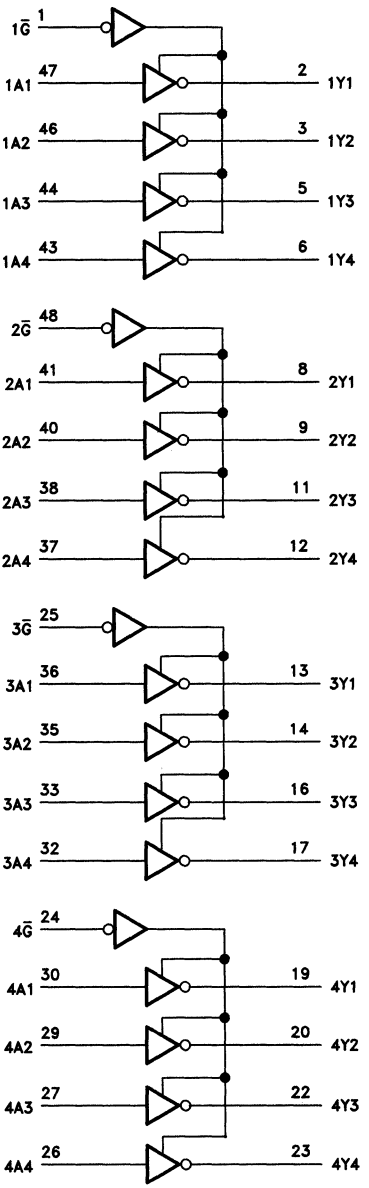
D3605, JULY 1990—REVISED NOVEMBER 1990—TI0281

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC16240			74AC16240			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage power supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16240		74AC16240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF
C_o	V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ±0.3 V (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16240		74AC16240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.8	5.4	7.5	1.8	8.9	1.8	8.3	ns
t_{PHL}			2.5	7	9.3	2.5	10.8	2.5	10.2	
t_{PZH}	$\overline{G}$	Y	2.1	6.1	8.5	2.1	10.2	2.1	9.5	ns
t_{PZL}			2.9	8.4	11.3	2.9	13.5	2.9	12.6	
t_{PHZ}	$\overline{G}$	Y	4.3	6.2	8.3	4.3	9	4.3	8.7	ns
t_{PLZ}			3.6	6	7.8	3.6	8.5	3.6	8.4	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16240		74AC16240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.3	3.3	5.3	1.3	6.2	1.3	5.8	ns
t_{PHL}			1.9	4.3	6.5	1.9	7.6	1.9	7.1	
t_{PZH}	$\overline{G}$	Y	1.6	3.8	5.9	1.6	7	1.6	6.6	ns
t_{PZL}			3.2	4.7	7.2	2.2	8.7	2.2	8.1	
t_{PHZ}	$\overline{G}$	Y	4.2	6	7.7	4.2	8.4	4.2	8.1	ns
t_{PLZ}			3.4	5.1	6.9	3.4	7.5	3.4	7.3	

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

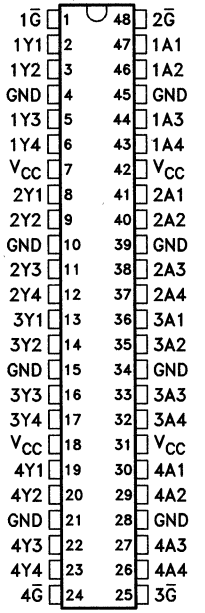
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	42	pF
		Outputs disabled		6	

TI0282—D3606, JULY 1990

- **Members of the Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16240 . . . WD PACKAGE
74ACT16240 . . . DL PACKAGE
(TOP VIEW)



description

The 'ACT16240 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical $\overline{G}$ (active-low output enable) inputs. The 'ACT16240 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 54ACT16240 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT16240 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE, EACH SECTION

INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	L
L	L	H
H	X	Z

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TEXAS INSTRUMENTS
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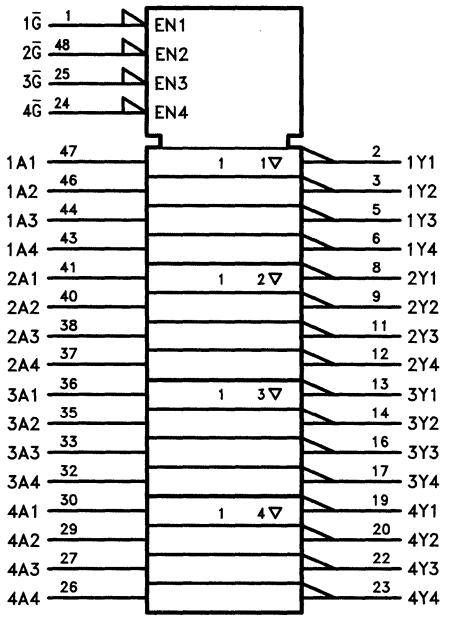
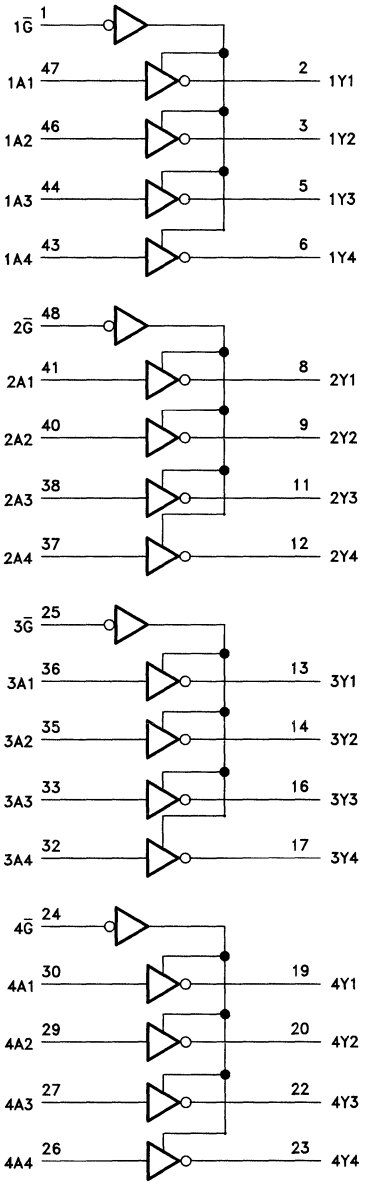
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT16240		74ACT16240		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater.
3. All V_{CC} and GND pins must be connected to the proper voltage power supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16240		74ACT16240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.94		3.8		
		5.5 V	4.94			4.94		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	Other inputs at One input at 3.4 V, GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF
C_o	V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16240		74ACT16240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2.3	5	7.7	2.3	9	2.3	8.5	ns
t_{PHL}			4.1	6.7	9.2	4.1	11.1	4.1	10.2	
t_{PZH}	$\overline{G}$	Y	2.6	5.6	8.5	2.6	10.1	2.6	9.4	ns
t_{PZL}			3.3	6.7	10.2	3.3	12.2	3.3	11.4	
t_{PHZ}	$\overline{G}$	Y	5.9	8.3	11	5.9	12.7	5.9	12	ns
t_{PLZ}			5.1	7.4	9.9	5.1	11.3	5.1	10.7	

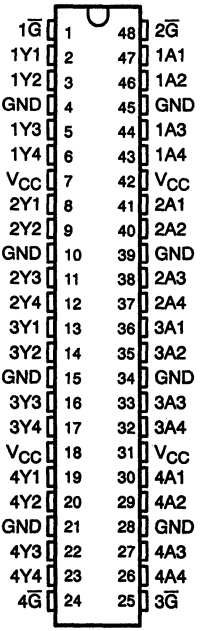
NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	38	pF
		Outputs disabled		9	

- **Member of the Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16244 ... WD PACKAGE
74AC16244 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16244 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical $\overline{G}$ (active-low) output-enable inputs.

The 74AC16244 is packaged in the TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54AC16244 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC16244 is characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

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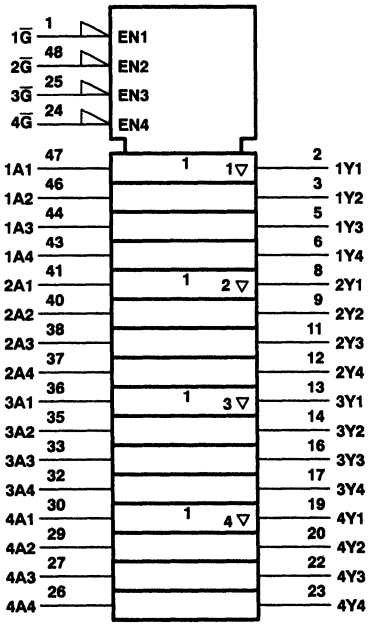
FUNCTION TABLE
(each driver)

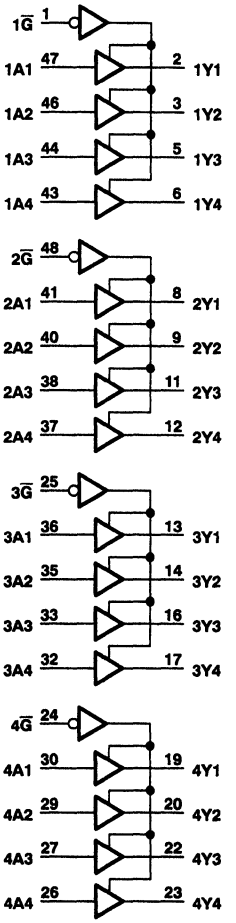
INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC16244			74AC16244			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

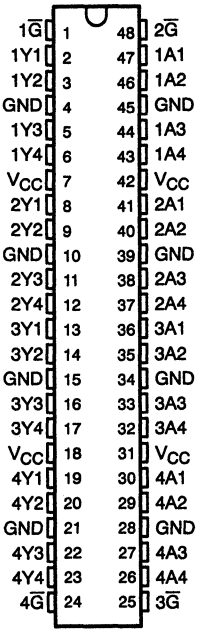
PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16244		74AC16244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_I = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF
C_o	V_I = V_{CC} or GND	5 V		12						

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

PRODUCT PREVIEW

- **Members of the Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-To-Center Pin Spacings**
- **Inputs are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16244 ... WD PACKAGE
74ACT16244 ... DL PACKAGE
(TOP VIEW)



description

The 'ACT16244 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical $\overline{G}$ (active-low) output-enable inputs.

The 74ACT16244 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16244 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT16244 is characterized for operation from −40°C to 85°C.

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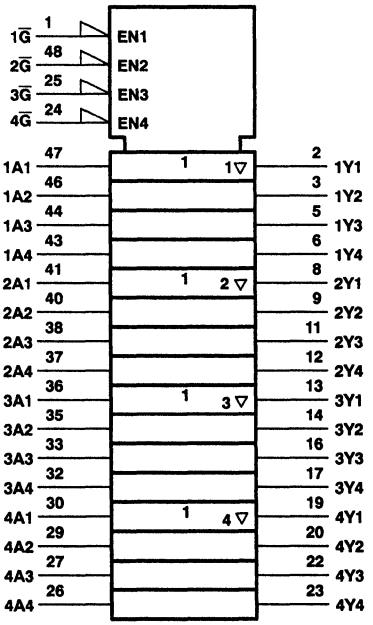
FUNCTION TABLE
(each driver)

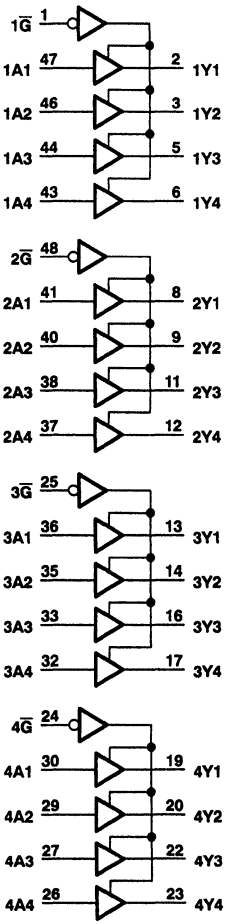
INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT16244		74ACT16244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater.
3. All V_{CC} and GND pins must be connected to the proper voltage supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16244		74ACT16244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_I = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF
C_o	V_I = V_{CC} or GND	5 V		13.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16244		74ACT16244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	4	6.5	8.5	4	10.3	4	9.4	ns
t_{PHL}			3.4	6.3	8.7	3.4	10.1	3.4	9.5	
t_{PZH}	$\overline{G}$	Y	3	5.8	8.1	3	9.5	3	8.9	ns
t_{PZL}			3.7	6.7	9.3	3.7	11	3.7	10.3	
t_{PHZ}	$\overline{G}$	Y	5.4	8.1	10.3	5.4	12	5.4	11.3	ns
t_{PHL}			5	7.5	9.5	5	10.9	5	10.3	

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	39	pF
		Outputs disabled		11	

TI0173—D3451, MARCH 1990

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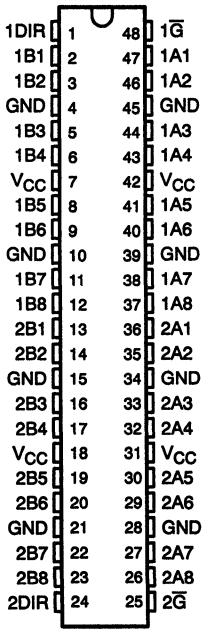
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16245 ... WD PACKAGE
74AC16245 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction control inputs (DIR). The enable inputs ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The 74AC16245 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16245 is characterized over the full military temperature range of −55°C to 125°C. The 74AC16245 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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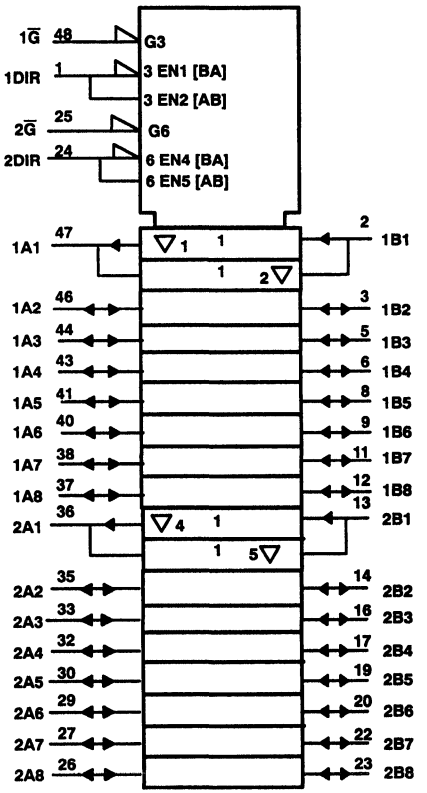
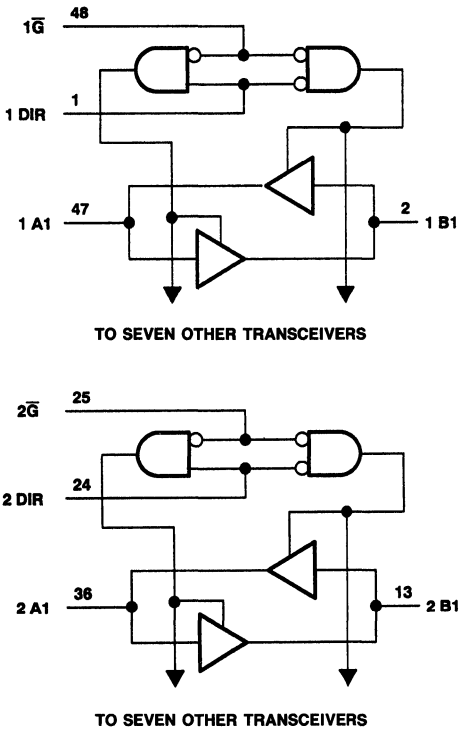
logic symbol†



logic diagrams (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC16245			74AC16245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16245		74AC16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports‡	V_I = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports	V_I = V_{CC} or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16245		74AC16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.5	7.6	10.4	2.5	12.8	2.5	11.9	ns
t_{PHL}			3.1	9	12.3	3.1	14.3	3.1	13.5	
t_{PZH}	$\overline{G}$	A or B	2.8	8.6	11.8	2.8	14.4	2.8	13.2	ns
t_{PZL}			3.9	12	16.2	3.9	19.3	3.9	18	
t_{PHZ}	$\overline{G}$	A or B	5.3	8.4	10.4	5.3	11.6	5.3	11.2	ns
t_{PLZ}			4.4	7.7	9.7	4.4	10.6	4.4	10.3	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16245		74AC16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	4.6	6.9	2	8.5	2	7.9	ns
t_{PHL}			2.5	5.2	7.9	2.5	9.5	2.5	8.9	
t_{PZH}	$\overline{G}$	A or B	2.3	4.9	7.5	2.3	9.3	2.3	8.6	ns
t_{PZL}			3	6.2	9.5	3	11.6	3	10.7	
t_{PHZ}	$\overline{G}$	A or B	5	7.2	9.1	5	10.2	5	9.8	ns
t_{PLZ}			4.2	6.2	8.1	4.2	9	4.2	8.7	

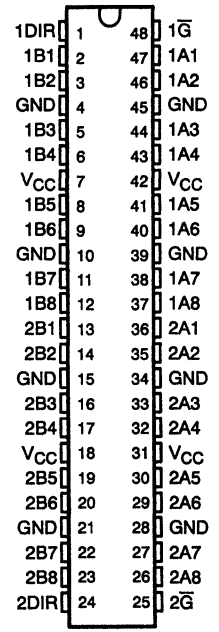
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	43	pF
		Outputs disabled		8	

TI0182—D3402, DECEMBER 1989—REVISED MARCH 1990

- **Members of the Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16245 . . . WD PACKAGE
74ACT16245 . . . DL PACKAGE
(TOP VIEW)



description

The 'ACT16245 is a 16-bit bus transceiver organized as a dual-octal noninverting 3-state transceiver and is designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The 74ACT16245 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16245 is characterized over the full military temperature range of −55°C to 125°C. The 74ACT16245 is characterized for operation from −40°C to 85°C.

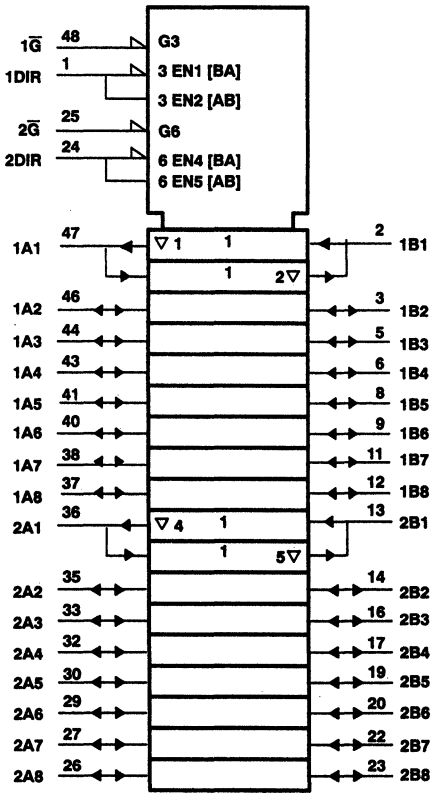
FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

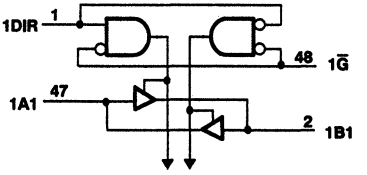
D3402, DECEMBER 1989—REVISED MARCH 1990—TI0182

logic symbol†

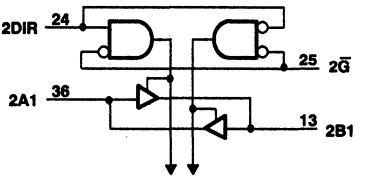


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



TO SEVEN OTHER TRANSCEIVERS



TO SEVEN OTHER TRANSCEIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT16245		74ACT16245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater.
3. All V_{CC} and GND pins must be connected to the proper voltage supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16245		74ACT16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.94		3.8		
			5.5 V	4.94			4.94		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports‡	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current I_I.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16245		74ACT16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3.2	6.9	9.3	3.2	11.5	3.2	10.5	ns
t_{PHL}			2.6	6.4	9.2	2.6	11.1	2.6	10.2	
t_{PZH}	$\overline{G}$	B or A	2.7	6.4	9.1	2.7	10.9	2.7	10	ns
t_{PZL}			3.4	7.4	10.5	3.4	12.6	3.4	11.6	
t_{PHZ}	$\overline{G}$	B or A	5.8	9.2	11.6	5.8	13.4	5.8	12.6	ns
t_{PLZ}			5.5	8.5	10.8	5.5	12.7	5.5	11.8	

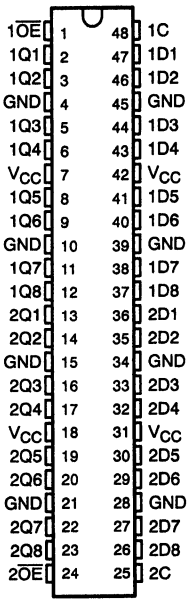
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	52	pF
		Outputs disabled		10	

TI0154—D3467, MARCH 1990

- **Member of the Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Distributed Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16373 ... WD PACKAGE
74AC16373 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16373 is a 16-bit D-type transparent latch with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit latches or one 16-bit latch. The Q outputs of the latches will follow the D inputs if enable C is taken high. When C is taken low, the Q outputs will be latched at the levels set up at the D inputs.

A buffered output-enable input $\overline{OE}$ can be used to place the outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control $\overline{OE}$ does not affect the internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74AC16373 is packaged in TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54AC16373 is characterized over the full military temperature range of −55°C to 125°C. The 74AC16373 is characterized for operation from −40°C to 85°C.

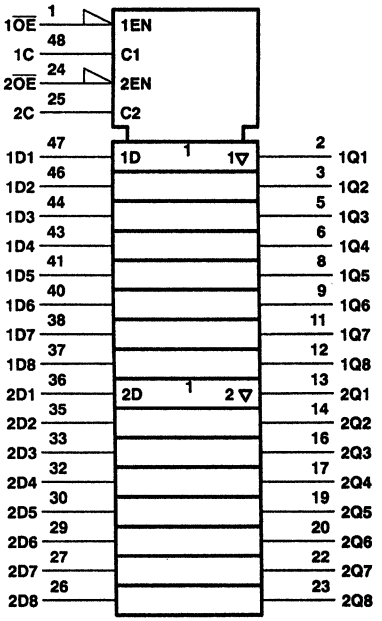
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE

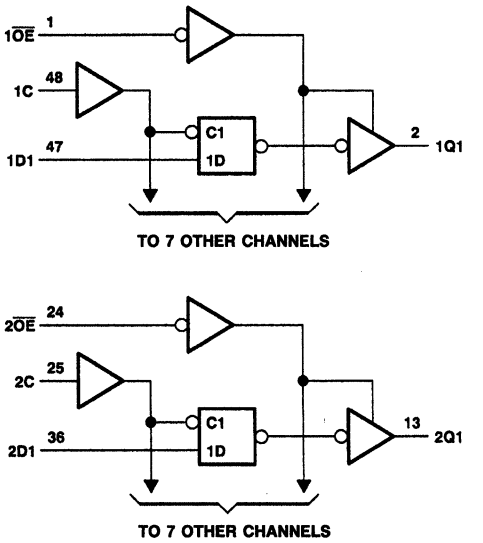
INPUTS			OUTPUT
$\overline{OE}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

			54AC16373			74AC16373			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 3)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater.
3. All V_{CC} and GND pins must be connected to the proper voltage supply.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16373		74AC16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_I = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF
C_o	V_I = V_{CC} or GND	5 V		12						pF

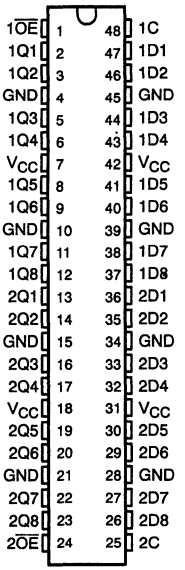
† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

PRODUCT PREVIEW

TI0150—D3468, MARCH 1990—REVISED JUNE 1990

- **Members of the Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL-Voltage Compatible**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16373 ... WD PACKAGE
74ACT16373 ... DL PACKAGE
(TOP VIEW)



description

The 'ACT16373 is a 16-bit D-type transparent latch with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads.

It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The device can be used as two 8-bit latches or one 16-bit latch. The Q outputs of the latches will follow the D inputs if enable C is taken high. When C is taken low, the Q outputs will be latched at the levels set up at the D inputs.

A buffered output-enable input $\overline{OE}$ can be used to place the outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pullup components. The output enable $\overline{OE}$ does not affect the internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT16373 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

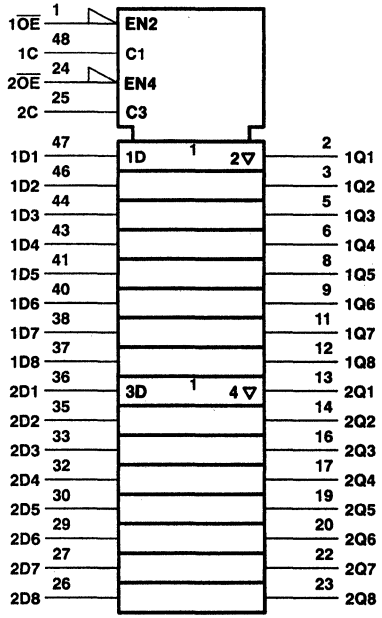
The 54ACT16373 is characterized over the full military temperature range of −55°C to 125°C. The 74ACT16373 is characterized for operation from −40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE
(each section)

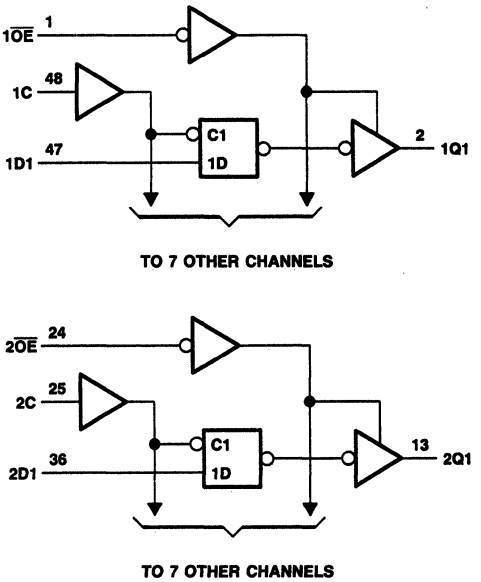
INPUTS			OUTPUT
$\overline{OE}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT16373		74ACT16373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater.
3. All V_{CC} and GND pins must be connected to the proper voltage supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16373		74ACT16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF
C_o	V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at one time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (see Figure 1)

		T_A = 25°C		54ACT16373		74ACT16373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, C high	4		4		4		ns
t_{su}	Setup time, data before C ↓	1		1		1		ns
t_h	Hold time, data after C ↓	5		5		5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

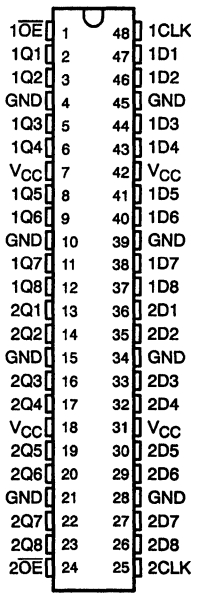
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16373		74ACT16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3.8	7.9	9.4	3.8	11.8	3.8	11.1	ns
t_{PHL}			3.1	8.2	9.7	3.1	13	3.1	12.3	
t_{PLH}	C	Q	4.6	9.3	10.8	4.6	13.7	4.6	12.8	ns
t_{PHL}			4.5	9.1	10.5	4.5	13	4.5	12.2	
t_{PZH}	$\overline{OE}$	Q	3.1	8	9.5	3.1	13	3.1	12.1	ns
t_{PZL}			3.8	9.4	11.1	3.8	15.1	3.8	14.2	
t_{PHZ}	$\overline{OE}$	Q	5.3	8.6	9.9	5.3	11	5.3	10.7	ns
t_{PLZ}			4.3	7.4	8.7	4.3	9.8	4.3	9.4	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	43	pF
		Outputs disabled		4.5	

- **Member of the Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Distributed Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16374 . . . WD PACKAGE
74AC16374 . . . DL PACKAGE
(TOP VIEW)



description

The 'AC16374 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of CLK, the Q outputs of the flip-flop are set to the logic levels set up at the D inputs.

An output enable input $\overline{OE}$ can be used to place the outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state provides the capability to drive the bus lines in a bus-organized system without need for interface or pullup components. The output enable $\overline{OE}$ does not affect the internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74AC16374 is packaged in TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54AC16374 is characterized over the full military temperature range of −55°C to 125°C. The 74AC16374 is characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

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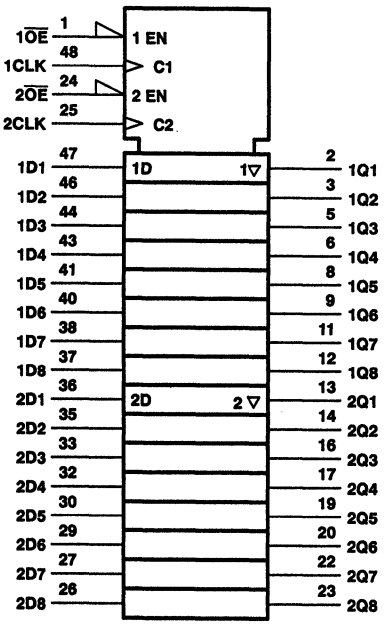
FUNCTION TABLE

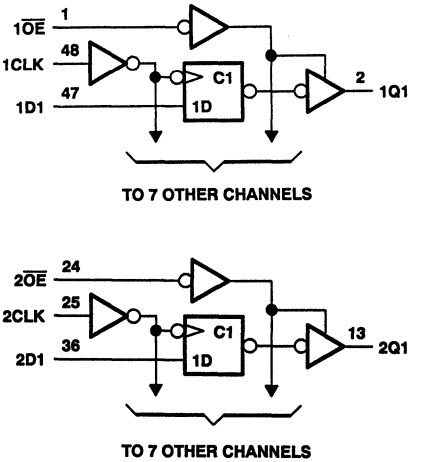
INPUTS			OUTPUT
$\overline{OE}$	C	D	Q
L	↑	H	H
L	↑	L	L
L	X	X	Q_O
L	↓	X	Q_O
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC16374			74AC16374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16374		74AC16374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF
C_o	V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 3)

			T_A = 25°C		54AC16374		74AC16374		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency								MHz
t_W	Pulse duration	CLK low							ns
		CLK high							
t_{SU}	Setup time, data before C↑								ns
t_h	Hold time, data after C↑								ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 3)

			T_A = 25°C		54AC16374		74AC16374		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK low							ns
		CLK high							
t_{su}	Setup time, data before C↑								ns
t_h	Hold time, data after C↑								ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16374		74AC16374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}										MHz
t_{PLH}	CLK	Q								ns
t_{PHL}										
t_{PZH}	$\overline{OE}$	Q								ns
t_{PZL}										
t_{PHZ}	$\overline{OE}$	Q								ns
t_{PLZ}										

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16374		74AC16374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}										MHz
t_{PLH}	CLK	Q								ns
t_{PHL}										
t_{PZH}	$\overline{OE}$	Q								ns
t_{PZL}										
t_{PHZ}	$\overline{OE}$	Q								ns
t_{PLZ}										

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

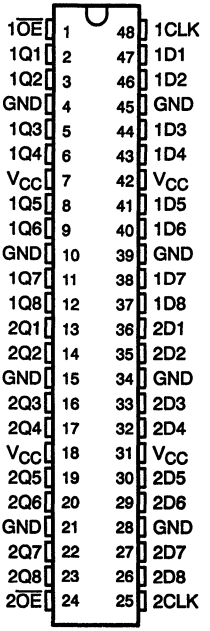
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz		pF
		Outputs disabled			

PRODUCT PREVIEW

TI0195—D3469, MARCH 1990—REVISED JUNE 1990

- **Members of the Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL-Voltage Compatible**
- **3-State Bus-Driving True Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed Center-Pin V_{CC} and GND Pin Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16374 ... WD PACKAGE
74ACT16374 ... DL PACKAGE
(TOP VIEW)



description

The 'ACT16374 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of CLK, the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

An output-enable input $\overline{OE}$ can be used to place the outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state provides the capability to drive the bus lines in a bus-organized system without need for interface or pullup components. The output-enable $\overline{OE}$ does not affect the internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT16374 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16374 is characterized over the full military temperature range of −55°C to 125°C. The 74ACT16374 is characterized for operation from −40°C to 85°C.

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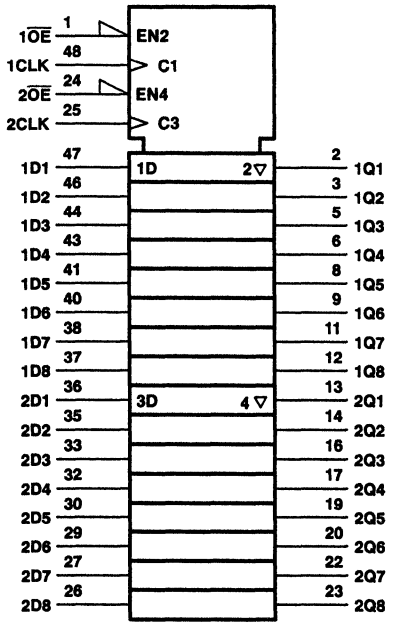
FUNCTION TABLE
(each section)

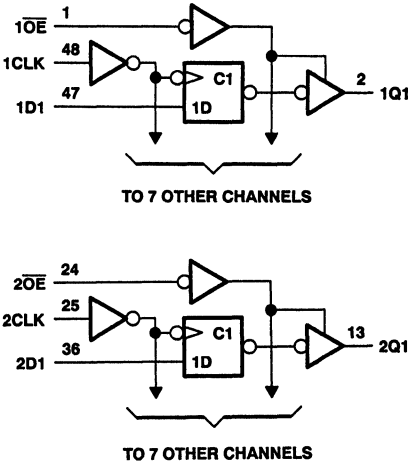
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_O
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT16374			74ACT16374			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16374		74ACT16374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.94		3.8		
		5.5 V	4.94			4.94		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF
C_o	V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V

			T_A = 25°C		54ACT16374		74ACT16374		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	65	0	65	0	65	MHz
t_w	Pulse duration	CLK low	7.5		7.5		7.5		ns
		CLK high	4.5		4.5		4.5		
t_{su}	Setup time, data before C ↑		6.5		6.5		6.5		ns
t_h	Hold time, data before C ↑		1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16374		74ACT16374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			65			65		65		MHz
t_{PLH}	CLK	Q	5.1	8.8	10.9	5.1	13.2	5.1	12.4	ns
t_{PHL}			5.3	8.8	10.9	5.3	13.1	5.3	12.2	
t_{PZH}	$\overline{OE}$	Q	3.7	8.4	10.5	3.7	12.7	3.7	11.9	ns
t_{PZL}			4.4	9.7	11.9	4.4	14.3	4.4	13.4	
t_{PHZ}	$\overline{OE}$	Q	5.4	7.9	9.8	5.4	10.9	5.4	10.4	ns
t_{PLZ}			4.9	7.2	9.1	4.9	10.2	4.9	9.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

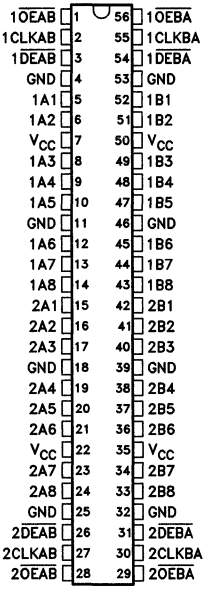
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	52	pF
		Outputs disabled		38	

16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0246—D3569, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16470, 54ACT16470 ... WD PACKAGE
74AC16470, 74ACT16470 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16470 and 'ACT16470 are noninverting 16-bit registered bus transceivers composed of two 8-bit sections with separate control signals. For either 8-bit transceiver section, data flow in the A-to-B mode is controlled by output enable (1$\overline{OEAB}$ or 2$\overline{OEAB}$), direction enable (1$\overline{DEAB}$ or 2$\overline{DEAB}$), and clock (1CLKAB or 2CLKAB) inputs.

When 1$\overline{DEAB}$ (or 2$\overline{DEAB}$) is high, storage of the current A-bus data is inhibited and the corresponding B outputs are in the high-impedance state. When 1$\overline{DEAB}$ (or 2$\overline{DEAB}$) is low, the register contents and the output buffers are controlled by 1CLKAB (or 2CLKAB) and 1$\overline{OEAB}$ (or 2$\overline{OEAB}$). A low level on 1CLKAB (or 2CLKAB) inhibits register loading; a low-to-high transition on 1CLKAB (or 2CLKAB) causes loading of the corresponding registers with the current A-bus data. If 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is low, the corresponding B outputs reflect the contents of the registers. A high level on 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) causes the B outputs to be in the high-impedance state.

FUNCTION TABLE, EACH SECTION†

INPUTS			LATCH DATA	B OUTPUTS
$\overline{DEAB}$	CLKAB	$\overline{OEAB}$		
H	X	X	Previous A Data	Z
L	L	H	Previous A Data	Z
L	L	L	Previous A Data	Previous A Data
L	↑	H	Current A Data	Z
L	↑	L	Current A Data	Current A Data

† A-to-B data flow is shown. B-to-A data flow is controlled analogously by $\overline{DEBA}$, CLKBA, and $\overline{OEBA}$.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

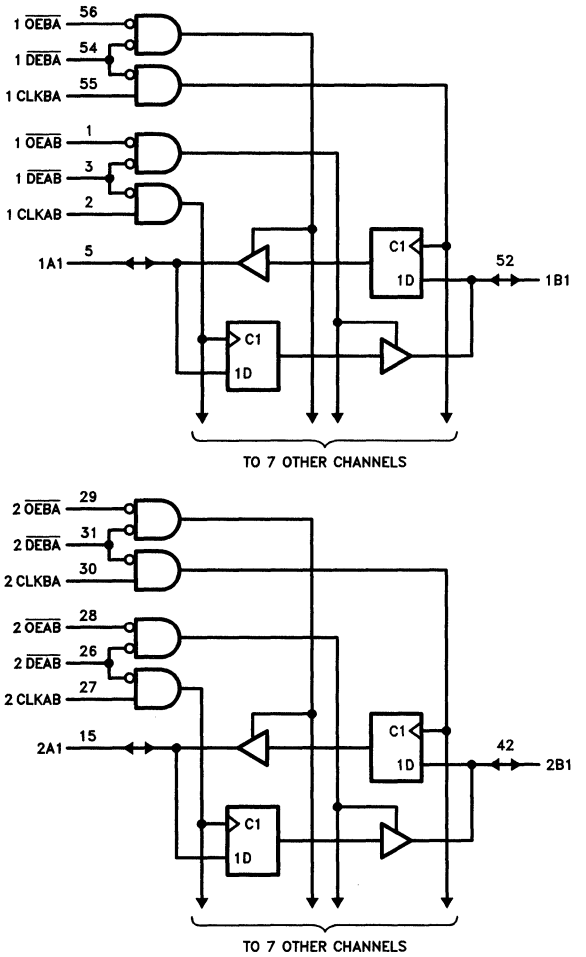
Data flow from B to A is similar, but uses 1$\overline{\text{OEBA}}$ and/or 2$\overline{\text{OEBA}}$, 1$\overline{\text{DEBA}}$ and/or 2$\overline{\text{DEBA}}$, and 1CLKBA and/or 2CLKBA.

The 74AC16470 and 74ACT16470 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16470 has CMOS-compatible input thresholds. The 'ACT16470 has TTL-compatible input thresholds.

The 54AC16470 and 54ACT16470 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16470 and 74ACT16470 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)



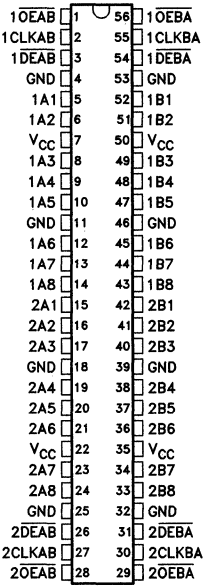
PRODUCT PREVIEW

16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0247—D3570, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16471, 54ACT16471 ... WD PACKAGE
74AC16471, 74ACT16471 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16471 and 'ACT16471 are inverting 16-bit registered bus transceivers composed of two 8-bit sections with separate control signals. For either 8-bit transceiver section, data flow in the A-to-B mode is controlled by output-enable (1$\overline{OEAB}$ or 2$\overline{OEAB}$), direction-enable (1$\overline{DEAB}$ or 2$\overline{DEAB}$), and clock (1CLKAB or 2CLKAB) inputs.

When 1$\overline{DEAB}$ (or 2$\overline{DEAB}$) is high, storage of the current A-bus data is inhibited and the corresponding B outputs are in the high-impedance state. When 1$\overline{DEAB}$ (or 2$\overline{DEAB}$) is low, the register contents and the output buffers are controlled by 1CLKAB (or 2CLKAB) and 1$\overline{OEAB}$ (or 2$\overline{OEAB}$). A low level on 1CLKAB (or 2CLKAB) inhibits loading of the registers with the current A-bus data; a low-to-high transition on 1CLKAB (or 2CLKAB) causes the corresponding registers to be loaded with the current A-bus data. If 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is low, the corresponding B outputs reflect the inverse of the register contents. A high level on 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) causes the B outputs to be in the high-impedance state.

FUNCTION TABLE, EACH SECTION†

INPUTS			LATCH DATA	B OUTPUTS
$\overline{DEAB}$	CLKAB	$\overline{OEAB}$		
H	X	X	Previous A Data	Z
L	L	H	Previous A Data	Z
L	L	L	Previous A Data	Inverse of Previous A Data
L	↑	H	Current A Data	Z
L	↑	L	Current A Data	Inverse of Current A Data

† A-to-B data flow is shown. B-to-A data flow is controlled analogously by $\overline{DEBA}$, CLKBA, and $\overline{OEBA}$.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

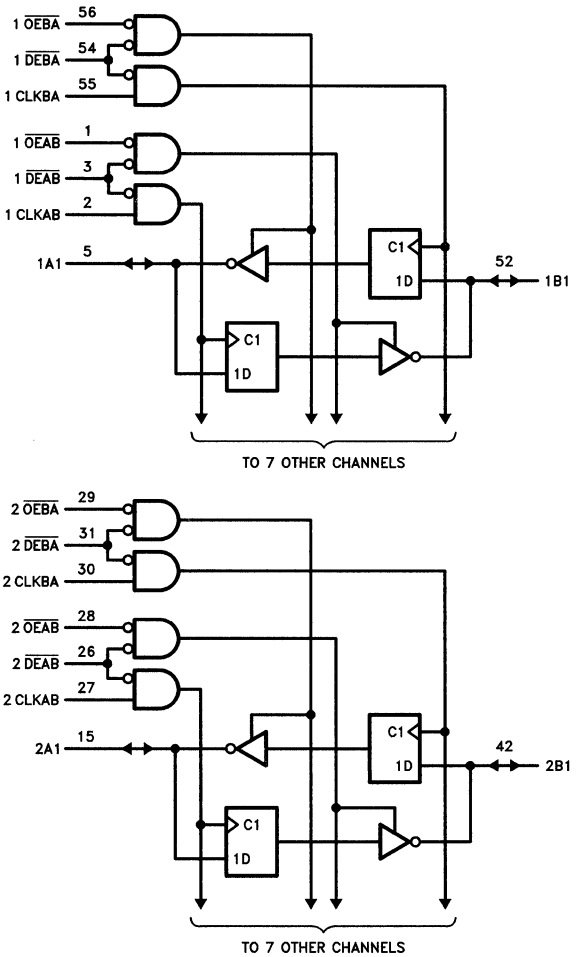
Data flow from B to A is similar, but uses 1$\overline{\text{OEBA}}$ and/or 2$\overline{\text{OEBA}}$, 1$\overline{\text{DEBA}}$ and/or 2$\overline{\text{DEBA}}$, and 1CLKBA and/or 2CLKBA.

The 74AC16471 and 74ACT16471 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16471 has CMOS-compatible input thresholds. The 'ACT16471 has TTL-compatible input thresholds.

The 54AC16471 and 54ACT16471 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16471 and 74ACT16471 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)



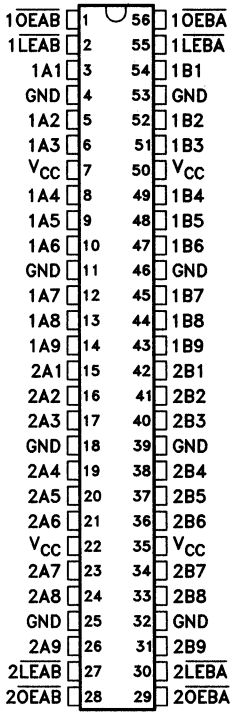
PRODUCT PREVIEW

18-BIT LATCHED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0248—D3571, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Package (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16472, 54ACT16472 ... WD PACKAGE
74AC16472, 74ACT16472 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16472 and 'ACT16472 are noninverting 18-bit latched bus transceivers composed of two 9-bit sections with separate control signals. For either 9-bit transceiver section, data flow in the A-to-B mode is controlled by output enable (1$\overline{OEAB}$ or 2$\overline{OEAB}$) and latch enable (1$\overline{LEAB}$ or 2$\overline{LEAB}$) inputs. When 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is low, the corresponding B outputs are active (high or low logic levels). When 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is high, the corresponding B outputs are in the high-impedance state. The latches retain their prior states when 1$\overline{LEAB}$ (or 2$\overline{LEAB}$) is high and reflect the states of the corresponding A inputs when 1$\overline{LEAB}$ (or 2$\overline{LEAB}$) is low.

FUNCTION TABLE, EACH SECTION†

INPUTS		LATCH DATA	B OUTPUTS
$\overline{LEAB}$	$\overline{OEAB}$		
L	L	Current A Data	Current A Data
H	L	Previous A Data	Previous A Data
L	H	Current A Data	Z
H	H	Previous A Data	Z

† A-to-B data flow is shown. B-to-A data flow is controlled analogously by $\overline{OEBA}$ and $\overline{LEBA}$.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

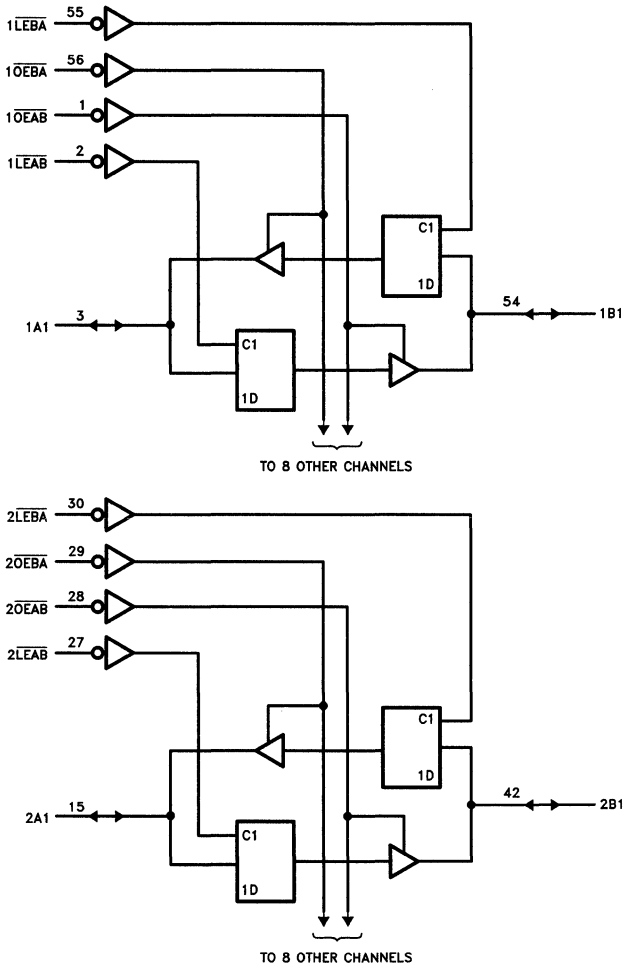
Data flow from B to A is similar, but uses $1\overline{OEBA}$ and/or $2\overline{OEBA}$ and $1\overline{LEBA}$ and/or $2\overline{LEBA}$.

The 74AC16472 and 74ACT16472 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16472 has CMOS-compatible input thresholds. The 'ACT16472 has TTL-compatible input thresholds.

The 54AC16472 and 54ACT16472 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16472 and 74ACT16472 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)



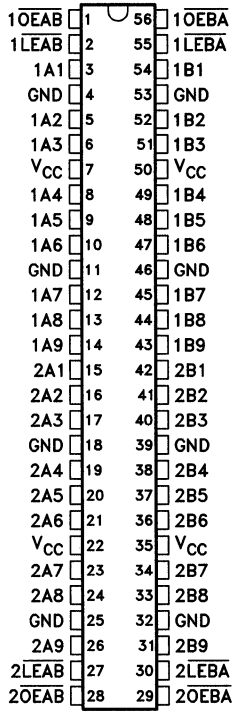
PRODUCT PREVIEW

18-BIT LATCHED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0249—D3572, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16473, 54ACT16473 . . . WD PACKAGE
74AC16473, 74ACT16473 . . . DL PACKAGE
(TOP VIEW)



description

The 'AC16473 and 'ACT16473 are inverting 18-bit latched bus transceivers composed of two 9-bit sections with separate control signals. For either 9-bit transceiver section, data flow in the A-to-B mode is controlled by output enable (1$\overline{OEAB}$ or 2$\overline{OEAB}$) and latch enable (1$\overline{LEAB}$ or 2$\overline{LEAB}$) inputs. When 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is low, the corresponding B outputs are active (high or low logic levels). When 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is high, the corresponding B outputs are in the high-impedance state. The latches retain their prior states when 1$\overline{LEAB}$ (or 2$\overline{LEAB}$) is high and reflect the states of the corresponding A inputs when 1$\overline{LEAB}$ (or 2$\overline{LEAB}$) is low.

FUNCTION TABLE, EACH SECTION†

INPUTS		LATCH DATA	B OUTPUTS
$\overline{LEAB}$	$\overline{OEAB}$		
L	L	Current A Data	Inverse of Current A Data
H	L	Previous A Data	Inverse of Previous A Data
L	H	Current A Data	Z
H	H	Previous A Data	Z

† A-to-B data flow is shown. B-to-A data flow is controlled analogously by $\overline{OEBA}$ and $\overline{LEBA}$.

PRODUCT PREVIEW

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TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

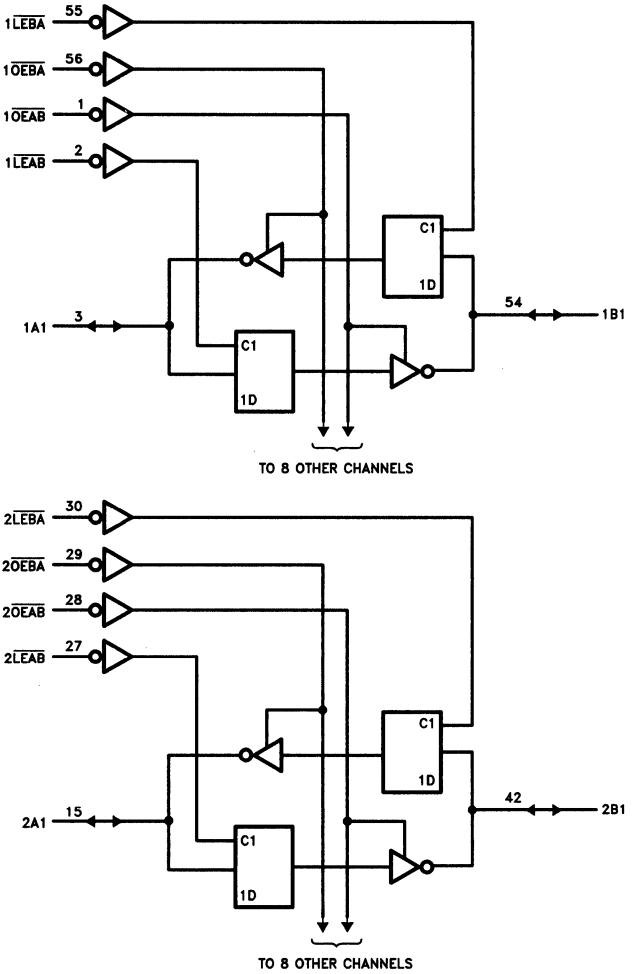
Data flow from B to A is similar, but uses $1\overline{OEBA}$ and/or $2\overline{OEBA}$ and $1\overline{LEBA}$ and/or $2\overline{LEBA}$.

The 74AC16473 and 74ACT16473 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16473 has CMOS-compatible input thresholds. The 'ACT16473 has TTL-compatible input thresholds.

The 54AC16473 and 54ACT16473 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16473 and 74ACT16473 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)



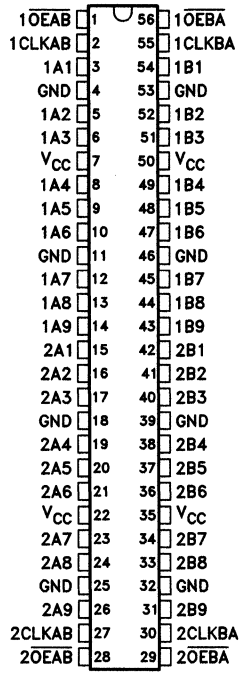
PRODUCT PREVIEW

18-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0250—D3573, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16474, 54ACT16474 ... WD PACKAGE
74AC16474, 74ACT16474 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16474 and 'ACT16474 are noninverting 18-bit registered bus transceivers composed of two 9-bit sections with separate control signals. For either 9-bit transceiver section, data flow in the A-to-B mode is controlled by output-enable (1$\overline{OEAB}$ or 2$\overline{OEAB}$) and clock (1CLKAB or 2CLKAB) inputs. When 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is low, the corresponding B outputs are active (high or low logic levels) and take on either the current A-bus data on a low-to-high transition of 1CLKAB (or 2CLKAB) or the previously stored A-bus data if 1CLKAB (or 2CLKAB) is low.

When 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is high, the corresponding B outputs are in the high-impedance state. 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) does not affect the operation of the internal registers. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Data flow from B to A is similar, but uses 1$\overline{OEBA}$ and/or 2$\overline{OEBA}$ and 1CLKBA and/or 2CLKBA.

FUNCTION TABLE, EACH SECTION†

INPUTS		LATCH DATA	B OUTPUTS
CLKAB	$\overline{OEAB}$		
L	L	Previous A Data	Previous A Data
L	H	Previous A Data	Z
↑	L	Current A Data	Current A Data
↑	H	Current A Data	Z

† A-to-B data flow is shown. B-to-A data flow is controlled analogously by CLKBA and $\overline{OEBA}$.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

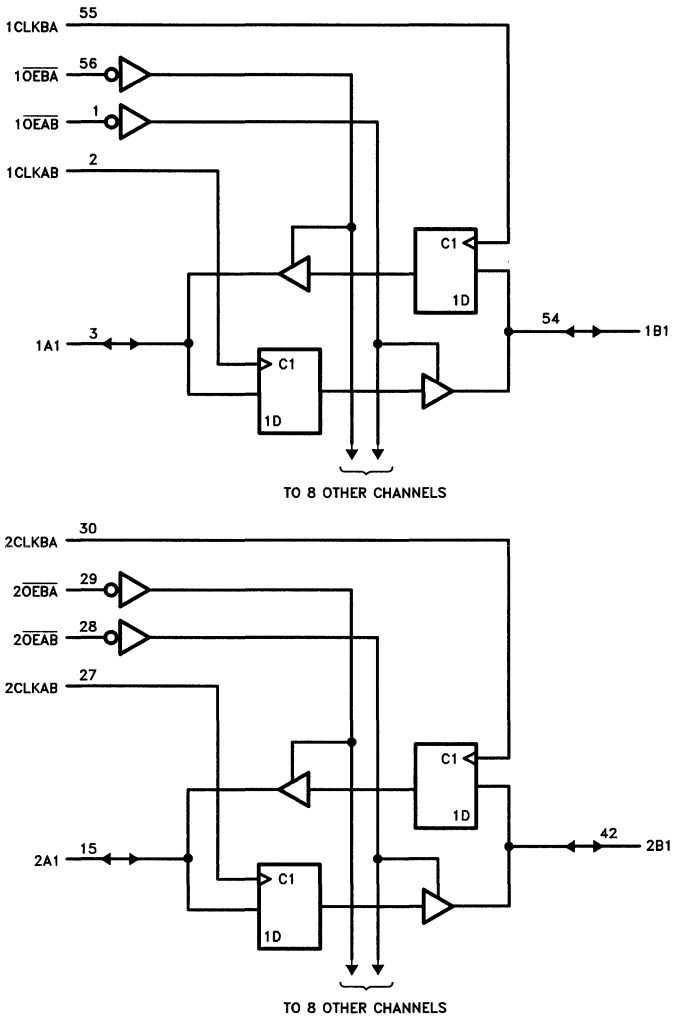
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

The 74AC16474 and 74ACT16474 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16474 has CMOS-compatible input thresholds. The 'ACT16474 has TTL-compatible input thresholds.

The 54AC16474 and 54ACT16474 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16474 and 74ACT16474 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)



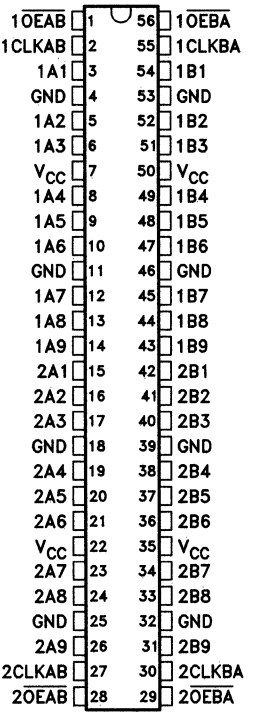
PRODUCT PREVIEW

18-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0251—D3574, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16475, 54ACT16475 ... WD PACKAGE
74AC16475, 74ACT16475 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16475 and 'ACT16475 are inverting 18-bit registered bus transceivers composed of two 9-bit sections with separate control signals. For either 9-bit transceiver section, data flow in the A-to-B mode is controlled by output-enable ($1\overline{OEAB}$ or $2\overline{OEAB}$) and clock (1CLKAB or 2CLKAB) inputs. When $1\overline{OEAB}$ (or $2\overline{OEAB}$) is low, the corresponding B outputs are active (high or low logic levels) and take on either the inverse of the current A-bus data on a low-to-high transition of 1CLKAB (or 2CLKAB) or the inverse of the previously stored A-bus data if 1CLKAB (or 2CLKAB) is low.

When $1\overline{OEAB}$ (or $2\overline{OEAB}$) is high, the corresponding B outputs are in the high-impedance state. $1\overline{OEAB}$ (or $2\overline{OEAB}$) does not affect the operation of the internal registers. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE, EACH SECTION†

INPUTS		LATCH DATA	B OUTPUTS
CLKAB	$\overline{OEAB}$		
L	L	Previous A Data	Inverse of Previous A Data
L	H	Previous A Data	Z
↑	L	Current A Data	Inverse of Current A Data
↑	H	Current A Data	Z

† A-to-B data flow is shown. B-to-A data flow is controlled analogously by CLKBA and $\overline{OEBA}$.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

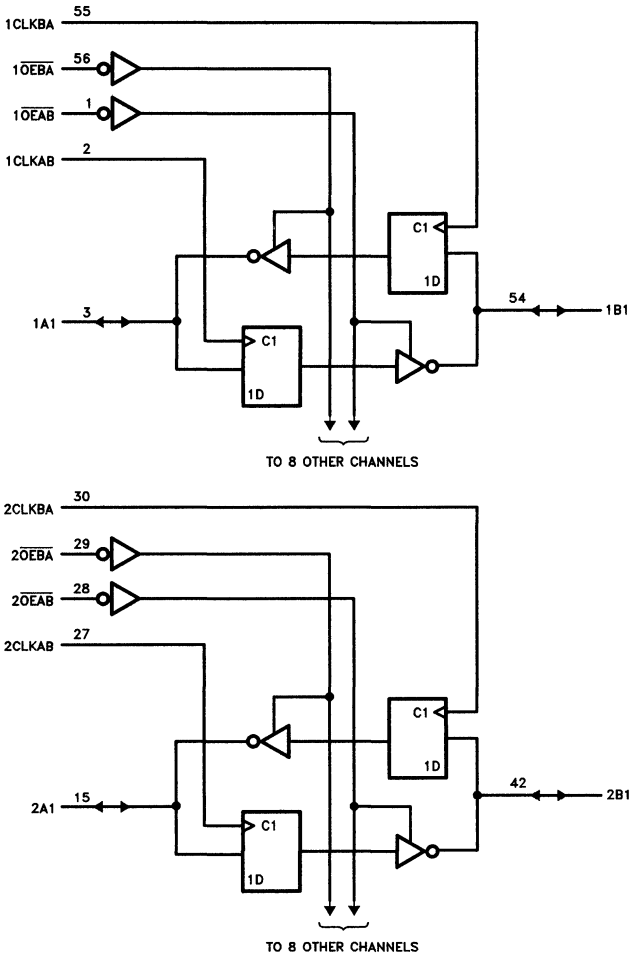
Data flow from B to A is similar, but uses $1\overline{OEBA}$ and/or $2\overline{OEBA}$ and 1CLKBA and/or 2CLKBA.

The 74AC16475 and 74ACT16475 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16475 has CMOS-compatible input thresholds. The 'ACT16475 has TTL-compatible input thresholds.

The 54AC16475 and 54ACT16475 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16475 and 74ACT16475 are characterized for operation from −40°C to 85°C.

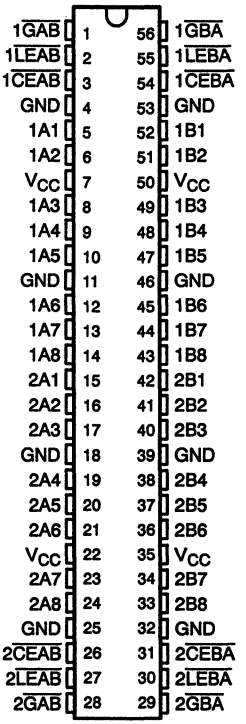
logic diagram (positive logic)



PRODUCT PREVIEW

- **Members of the Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **3-State True Outputs**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16543 . . . WD PACKAGE
74AC16543 . . . DL PACKAGE
(TOP VIEW)



description

The 'AC16543 is a 16-bit registered transceiver and contains two sets of D-type latches for temporary storage of data flowing in either direction. The 'AC16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate Latch Enable ($\overline{LEAB}$ or $\overline{LEBA}$) and Output Enable ($\overline{GAB}$ or $\overline{GBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B Enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data to B. Having ($\overline{CEAB}$) low and ($\overline{LEAB}$) low makes the A-to-B latches transparent; a subsequent low-to-high transition ($\overline{LEAB}$) puts the A latches in the storage mode. Data flow from B-to-A is similar, but requires using the ($\overline{CEBA}$), ($\overline{LEBA}$), and ($\overline{GBA}$) inputs.

The 74AC16543 is packaged in TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54AC16543 is characterized over the full military temperature range of −55°C to 125°C. The 74AC16543 is characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

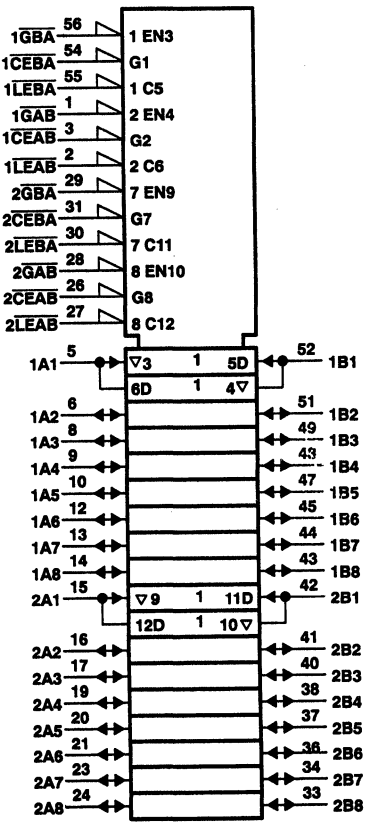
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE (each octal register)

INPUTS			LATCH STATUS A TO B†	OUTPUT BUFFERS B1 THRU B8
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{GAB}$		
H	X	X	Storing	High Z
X	H		Storing	
X		H		High Z
L	L	L	Transparent	Current A Data
L	H	L	Storing	Previous‡ A Data

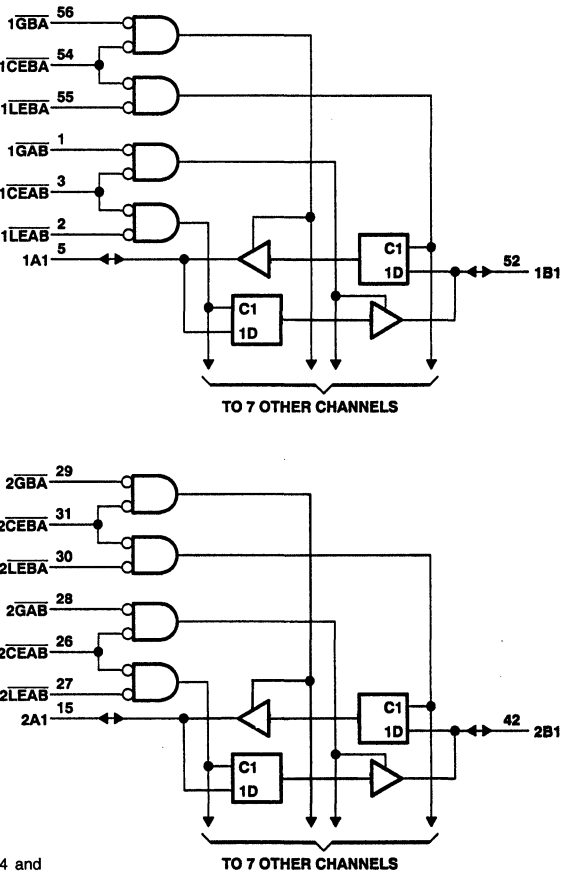
† A-to-B data flow is shown: B-to-A flow control is the same except uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$.
‡ Data present before low-to-high transition of $\overline{LEAB}$

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC16543			74AC16543			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

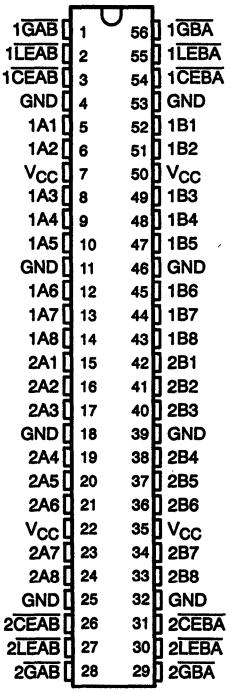
PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16543		74AC16543		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports‡	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- **Members of the Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL-Voltage Compatible**
- **3-State True Outputs**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16543 ... WD PACKAGE
74ACT16543 ... DL PACKAGE
(TOP VIEW)



description

The 'ACT16543 is a 16-bit registered transceiver and contains two sets of D-type latches for temporary storage of data flowing in either direction. The 'ACT16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output enable ($\overline{GAB}$ or $\overline{GBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B Enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data to B. Having $\overline{CEAB}$ low and $\overline{LEAB}$ low makes the A-to-B latches transparent; a subsequent low-to-high transition ($\overline{LEAB}$) puts the A latches in the storage mode. Data flow from B-to-A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$ inputs.

The 74ACT16543 is packaged in TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54ACT16543 is characterized over the full military temperature range of −55°C to 125°C. The 74ACT16543 is characterized for operation from −40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

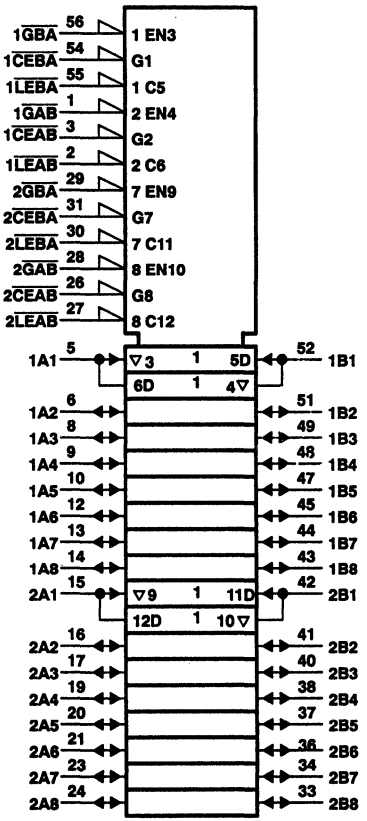
Function Table (each octal register)

INPUTS			LATCH STATUS A TO B†	OUTPUT BUFFERS B1 THRU B8
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{GAB}$		
H	X	X	Storing	Z
X	H	X	Storing	
X	X	H		Z
L	L	L	Transparent	Current A Data
L	H	L	Storing	Previous‡ A Data

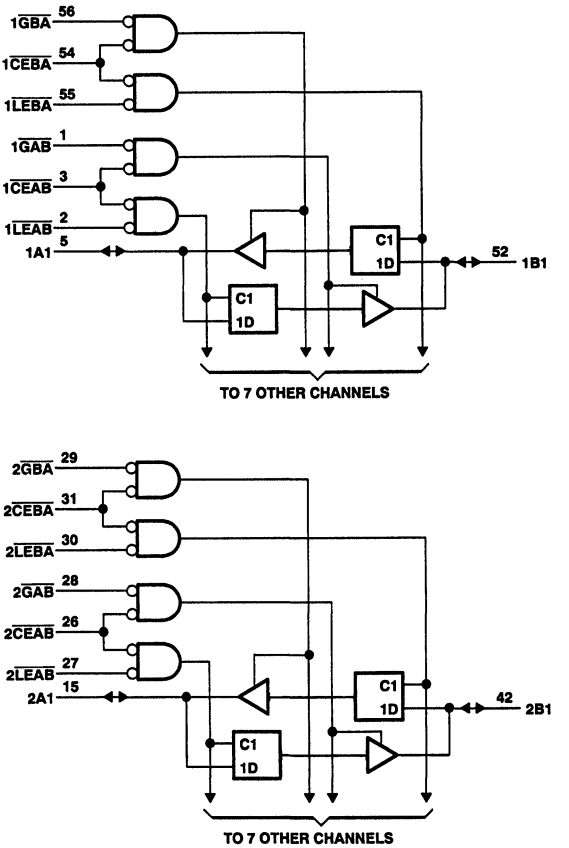
† A-to-B data flow is shown: B-to-A flow control is the same except it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$.

‡ Data present before low-to-high transition of $\overline{LEAB}$ occurring while $\overline{CEAB}$ is low.

logic symbol§



logic diagram (positive logic)



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT16543			74ACT16543			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16543		74ACT16543		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control Inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B Ports‡	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports	V_I = V_{CC} or GND	5 V		12						

† Not more than one output should be tested at one time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (unless otherwise noted) (see Note 3)

		T_A = 25°C		54ACT16543		74ACT16543		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low	7.5		7.5		7.5		ns
t_{su}	Setup time, data before $\overline{LEAB}$ or $\overline{LEBA}$ ↑	2.5		2.5		2.5		ns
t_h	Hold time, data after $\overline{LEAB}$ or $\overline{LEBA}$ ↑	4		4		4		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16543		74ACT16543		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	A or B	3.5	6.9	9.5	3.5	11.3	3.5	10.5	ns
t_{PHL}			3.1	7.3	10.7	3.1	13.1	3.1	11.6	
t_{PLH}	$\overline{LEAB}$ or $\overline{LEBA}$	A or B	3.9	8.6	12.3	3.9	15.1	3.9	13.8	ns
t_{PHL}			3.9	8.7	12.2	3.9	14.6	3.9	13.5	
t_{PZH}	$\overline{GAB}$ or $\overline{GBA}$	A or B	2.6	7.1	10.3	2.6	12.6	2.6	11.4	ns
t_{PZL}			3.5	8.3	11.9	3.5	14.4	3.5	13.2	
t_{PHZ}	$\overline{GAB}$ or $\overline{GBA}$	A or B	4.1	8.2	10.5	4.1	11.3	4.1	11.1	ns
t_{PLZ}			5	7.3	9.3	5	10.4	5	9.6	
t_{PZH}	$\overline{CEAB}$ or $\overline{CEBA}$	A or B	3.1	7.3	10.7	3.1	12.9	3.1	11.7	ns
t_{PZL}			3.9	8.5	12.2	3.9	14.8	3.9	13.5	
t_{PHZ}	$\overline{CEAB}$ or $\overline{CEBA}$	A or B	4.6	8.5	11	4.6	11.9	4.6	11.6	ns
t_{PLZ}			5.2	7.4	9.7	5.2	10.8	5.2	10.5	

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

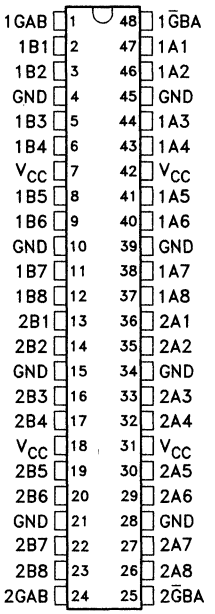
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	45	pF
		Outputs disabled		12	

TI0289—D3600, JULY 1990—REVISE OCTOBER 1990

- **Members of the Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16620 ... WD PACKAGE
74AC16620 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16620 is an inverting 16-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the complementary enable inputs (1$\overline{G}$BA, 1GAB, 2$\overline{G}$BA, and 2GAB). The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the bus transceiver the capability to store data by simultaneous enabling of 1$\overline{G}$BA and 1GAB (and/or 2$\overline{G}$BA and 2GAB). Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, the bus lines remain at their last states.

The 74AC16620 is packaged in TI's shrink small-outline packages (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16620 is characterized over the full military temperature range of −55°C to 125°C. The 74AC16620 is characterized for operation from − 40°C to 85°C.

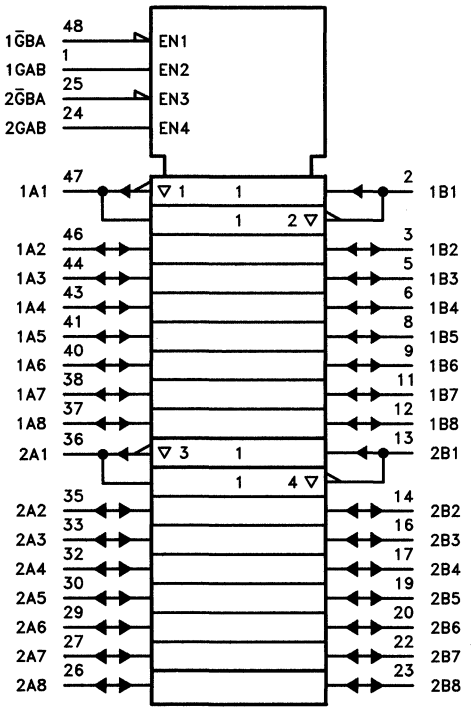
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

D3600, JULY 1990—REVISE OCTOBER 1990—TI0289

FUNCTION TABLE, EACH SECTION

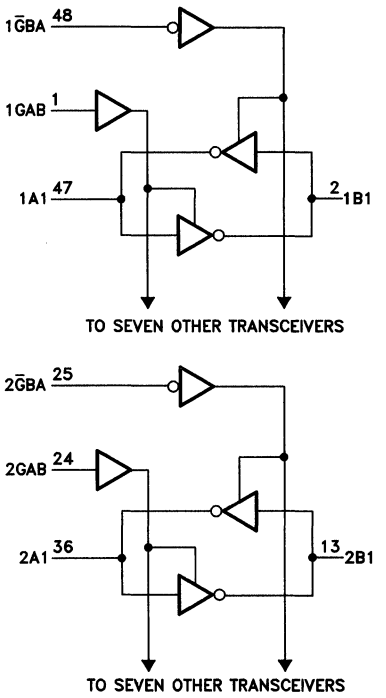
ENABLE INPUTS		OPERATION
$\overline{G}BA$	GAB	
L	L	$\overline{B}$ data to A bus
H	H	$\overline{A}$ data to B bus
H	L	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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TI0289—D3600, JULY 1990—REVISE OCTOBER 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... − 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... − 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... − 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC16620			74AC16620			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			− 4			− 4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16620		74AC16620		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports‡	V_I = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports	V_I = V_{CC} or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16620		74AC16620		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.7	6.1	8.7	2.7	10.3	2.7	9.7	ns
t_{PHL}			3.9	7.9	10.6	3.9	12.3	3.9	11.7	
t_{PZH}	$\overline{G}$BA	A	3.2	7.1	10	3.2	11.8	3.2	11.2	ns
t_{PZL}			4.5	11.1	13.5	4.5	15.8	4.5	15	
t_{PHZ}	$\overline{G}$BA	A	5.3	7.4	9.5	5.3	10.6	5.3	10.2	ns
t_{PLZ}			4.6	7	9.2	4.6	10.1	4.6	9.8	
t_{PZH}	GAB	B	3.1	6.7	9.5	3.1	11.3	3.1	10.7	ns
t_{PZL}			4.4	9.6	13	4.4	15.2	4.4	14.5	
t_{PHZ}	GAB	B	5	7.1	9.3	5	10.1	5	9.8	ns
t_{PLZ}			4.4	6.8	8.9	4.4	9.7	4.4	9.4	

NOTE 3: For load circuit and voltage waveforms, see Section 1.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16620		74AC16620		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.1	3.9	6.1	2.1	7.2	2.1	6.8	ns
t_{PHL}			3.1	4.9	7.3	3.1	8.7	3.1	8.2	
t_{PZH}	$\overline{G}$BA	A	2.2	4.3	6.8	2.2	8	2.2	7.6	ns
t_{PZL}			3.3	5.5	8.4	3.3	9.9	3.3	9.4	
t_{PHZ}	$\overline{G}$BA	A	4.9	6.6	8.6	4.9	9.5	4.9	9.2	ns
t_{PLZ}			4.1	5.8	7.8	4.1	8.6	4.1	8.3	
t_{PZH}	GAB	B	2.2	4.2	6.5	2.2	7.7	2.2	7.3	ns
t_{PZL}			3.4	5.4	8.1	3.4	9.6	3.4	9.1	
t_{PHZ}	GAB	B	4.6	6.4	8.5	4.6	9.4	4.6	9	ns
t_{PLZ}			4.1	5.6	7.6	4.1	8.3	4.1	8	

NOTE 3: For load circuit and voltage waveforms, see Section 1.

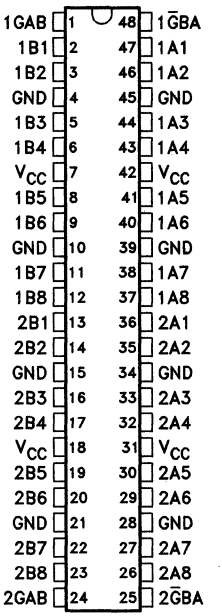
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	49	pF
		Outputs disabled		6	

TI0243—D3584, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16620 ... WD PACKAGE
74ACT16620 ... DL PACKAGE
(TOP VIEW)



description

The 'ACT16620 is an inverting 16-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the complementary enable inputs (1$\overline{G}$BA, 1GAB, 2$\overline{G}$BA, and 2GAB). The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the bus transceiver the capability to store data by simultaneous enabling of 1$\overline{G}$BA (or 2$\overline{G}$BA) and 1GAB (or 2GAB). Each output reinforces its input in this transceiver configuration. Thus, when both output-enable inputs are active and all other sources to the two sets of bus lines are high impedance, the bus lines remain at their last states.

The 'ACT16620 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 54ACT16620 is characterized over the full military temperature range of −55°C to 125°C. The 74ACT16620 is characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

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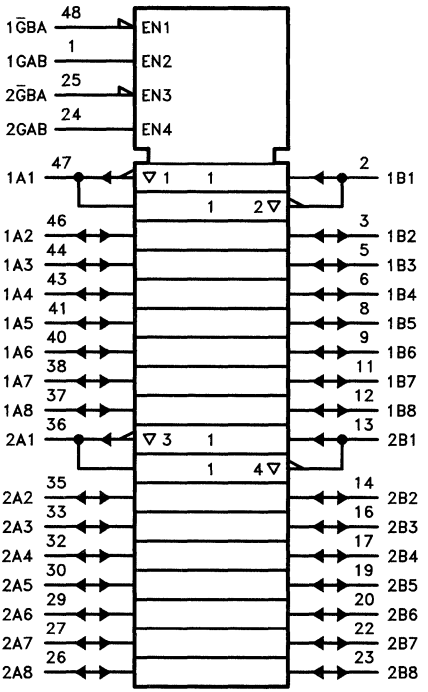
TI0243—D3584, JUNE 1990

FUNCTION TABLE, EACH SECTION

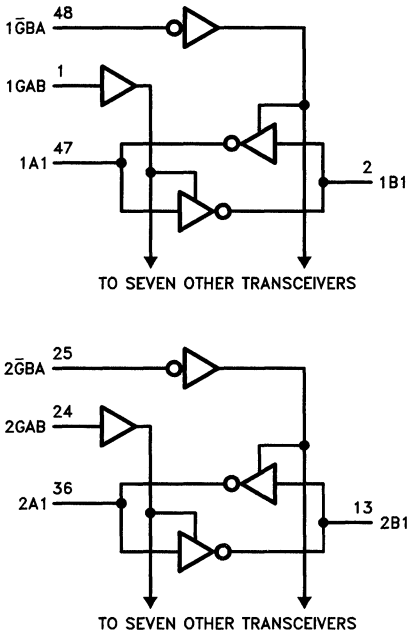
ENABLE INPUTS		OPERATION
$\overline{G}BA$	GAB	
L	L	$\overline{B}$ data to A bus
H	H	$\overline{A}$ data to B bus
H	L	Bus Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

D3584, JUNE 1990—TI0243

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT16620		74ACT16620		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater.

3. All V_{CC} and GND pins must be connected to the proper voltage power supply.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16620		74ACT16620		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.94		3.8		
			5.5 V	4.94			4.94		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OH} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports‡	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B Ports	V_O = V_{CC} or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16620		74ACT16620		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A								ns
t_{PHL}										
t_{PZH}	$\overline{G}$BA	A								ns
t_{PZL}										
t_{PHZ}	$\overline{G}$BA	A								ns
t_{PLZ}										
t_{PZH}	GAB	B								ns
t_{PZL}										
t_{PHZ}	GAB	B								ns
t_{PLZ}										

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

D3584, JUNE 1990—TI0243

operating characteristics, V_{CC} = 5 V, T_A = 25°C

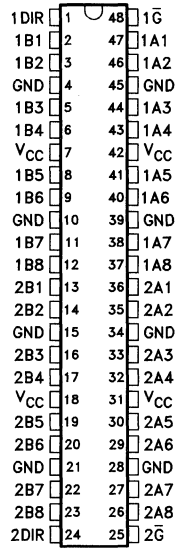
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz		pF
		Outputs disabled			

PRODUCT PREVIEW

TI0284—D3607, JULY 1990—REVISED OCTOBER 1990

- **Members of the Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Flow-Through Architecture Optimize PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16640 ... WD PACKAGE
74AC16640 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16640 is an inverting 16-bit transceiver designed for asynchronous communication between data buses.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the direction control inputs (1DIR and 2DIR).

The enable inputs ($1\overline{G}$ and $2\overline{G}$) can be used to disable the device so that the buses are effectively isolated. The 'AC16640 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 54AC16640 is characterized over the full military temperature range of −55°C to 125°C. The 74AC16640 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE, EACH SECTION

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	$\overline{B}$ Data to A Bus
L	H	$\overline{A}$ Data to B Bus
H	X	Bus Isolation

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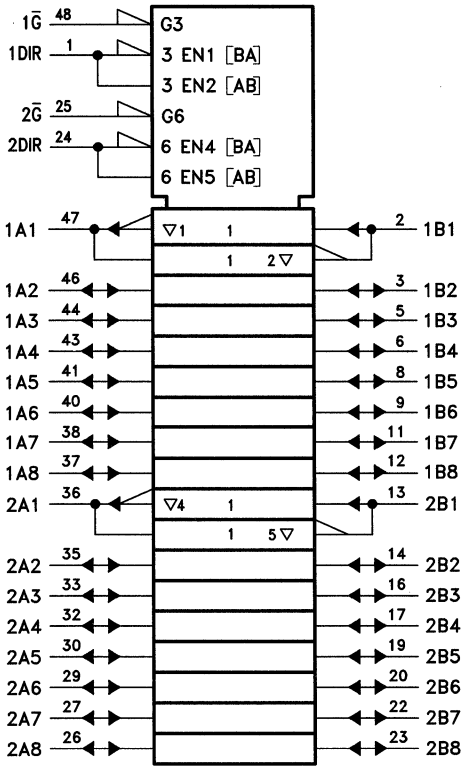
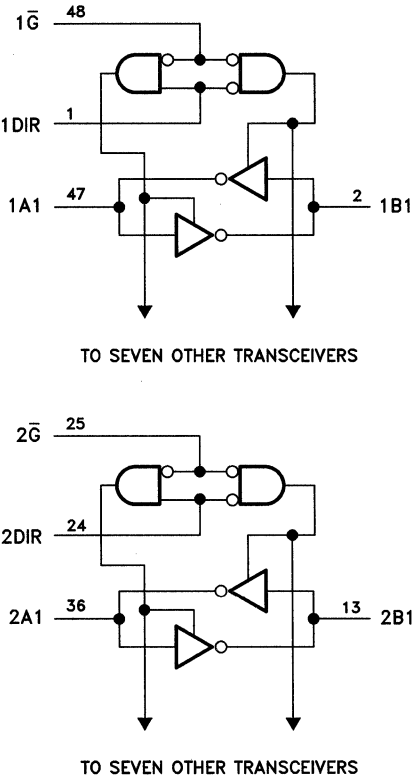
D3607, JULY 1990—REVISED OCTOBER 1990—TI0284

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC16640			74AC16640			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.

D3607, JULY 1990—REVISED OCTOBER 1990—TI0284

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16640		74AC16640		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		16						pF

† Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16640		74AC16640		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.2	6.9	9.1	2.2	10.7	2.2	10	ns
t_{PHL}			3	8.5	11	3	12.6	3	11.9	
t_{PZH}	$\overline{G}$	A or B	3	8.2	11	3	13.2	3	12.3	ns
t_{PZL}			3.9	10.9	14	3.9	16.8	3.9	15.5	
t_{PHZ}	$\overline{G}$	A or B	5.1	8.3	10.6	5.1	11.7	5.1	11.2	ns
t_{PLZ}			4.3	7.8	10.1	4.3	11	4.3	10.6	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16640		74AC16640		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.8	4.7		1.8	8	1.8	7.3	ns
t_{PHL}			2.6	5.7		2.6	9.2	2.6	8.6	
t_{PZH}	$\overline{G}$	A or B	2.4	5.6		2.4	8.5	2.4	8	ns
t_{PZL}			3	6.6		3	10.7	3	9.9	
t_{PHZ}	$\overline{G}$	A or B	5	7.5		5	10.4	5	9.9	ns
t_{PLZ}			4.1	6.5		4.1	9.3	4.1	9	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

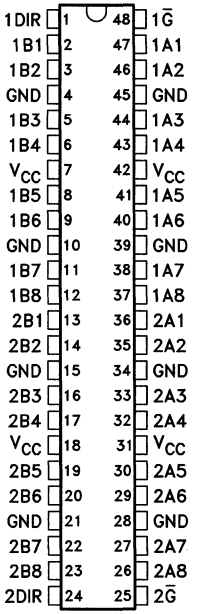
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	55	pF
		Outputs disabled		8	

TI0244—D3585, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16640 ... WD PACKAGE
74ACT16640 ... DL PACKAGE
(TOP VIEW)



description

The 'ACT16640 is an inverting 16-bit transceiver designed for asynchronous communication between data buses.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the direction control inputs (1DIR and 2DIR). The enable inputs ($1\overline{G}$ and $2\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The 'ACT16640 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 54ACT16640 is characterized over the full military temperture range of −55°C to 125°C. The 74ACT16640 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE, EACH SECTION

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Bus Isolation

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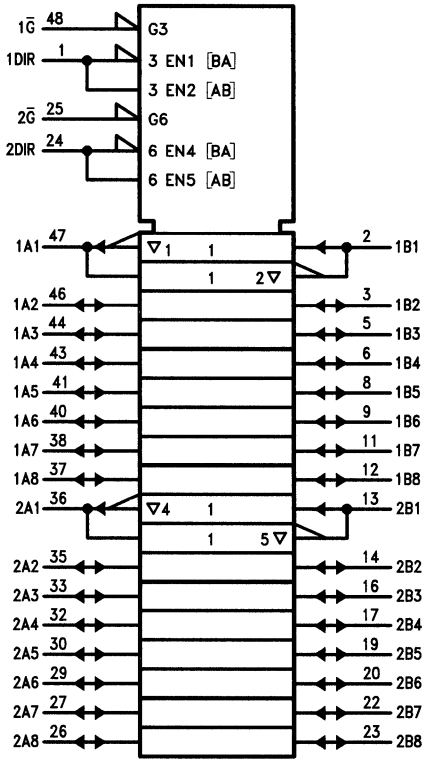
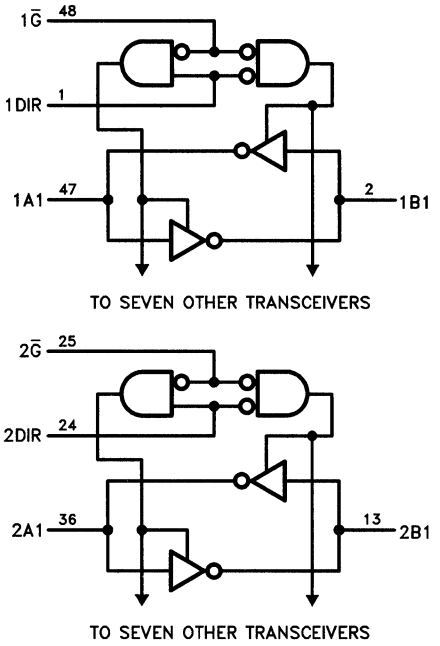
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Inut voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT16640		74ACT16640		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater.
3. All V_{CC} and GND pins must be connected to the proper voltage power supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16640		74ACT16640		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.94		3.8		
			5.5 V	4.94			4.94		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports‡	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B Ports	V_O = V_{CC} or GND	5 V		16						pF

† Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16640		74ACT16640		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.2	6	8.3	2.2	9.6	2.2	9.1	ns
t_{PHL}			4.1	7.6	9.3	4.1	11.3	4.1	10.5	
t_{PZH}	$\overline{G}$	A or B	2.7	6.9	8.9	2.7	10.4	2.7	9.8	ns
t_{PZL}			3.5	8.2	10.4	3.5	12.1	3.5	11.5	
t_{PHZ}	$\overline{G}$	A or B	6.1	9.4	11.4	6.1	13.1	6.1	12.5	ns
t_{PLZ}			5.5	8.7	10.3	5.5	11.5	5.5	11	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	52	pF
		Outputs disabled		9	

- **Member of the Texas Instruments Widebus™ Family**
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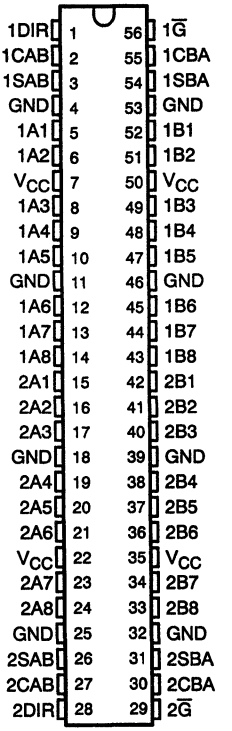
54AC16646 ... WD PACKAGE
74AC16646 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16646 is a 16-bit bus transceiver, which consists of D-type flip-flops and control circuitry with 3-state outputs arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock input (CAB or CBA). Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable ($\overline{G}$) and direction (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus receives data when $\overline{G}$ is active (low). In the isolation mode ($\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The 74AC16646 is packaged in the TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54AC16646 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC16646 is characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

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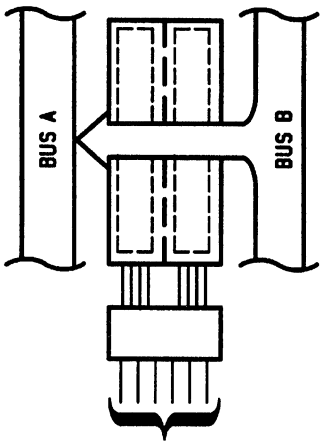
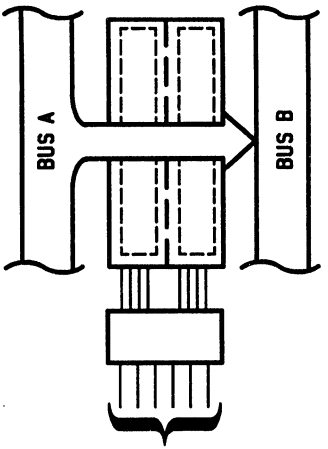


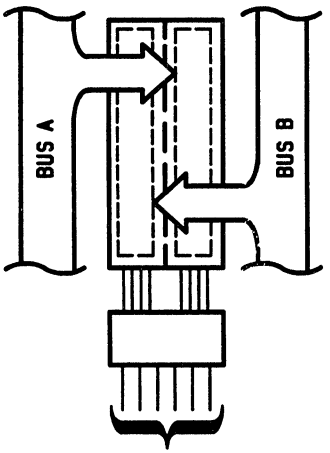
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



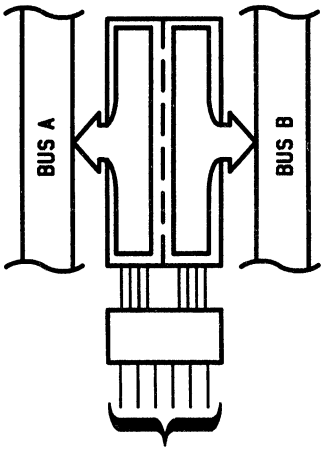
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



$\overline{G}$	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B OR A AND B



$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA TO A OR B

FIGURE 1. BUS TRANSFER DIAGRAM

PRODUCT PREVIEW

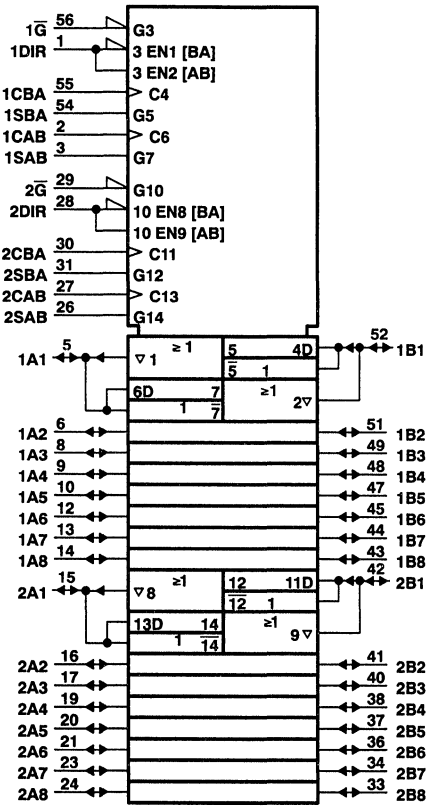
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus

† The data output functions may be enabled or disabled by various signals at the $\overline{G}$ or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

PRODUCT PREVIEW

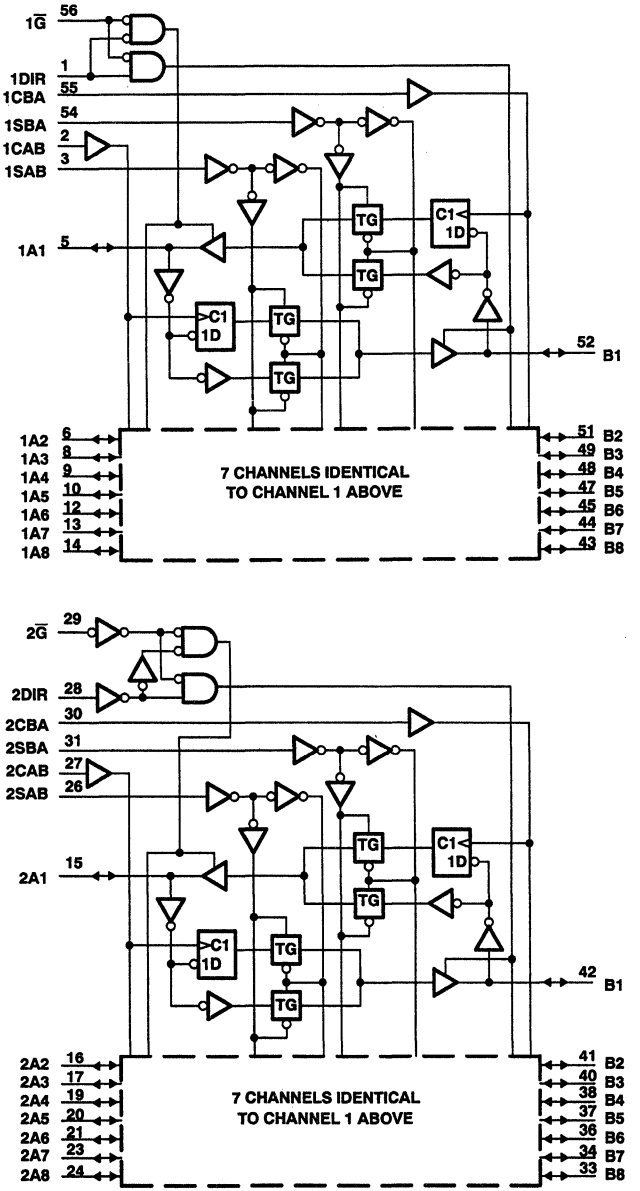
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagrams (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC16646			74AC16646			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16646		74AC16646		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports‡	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

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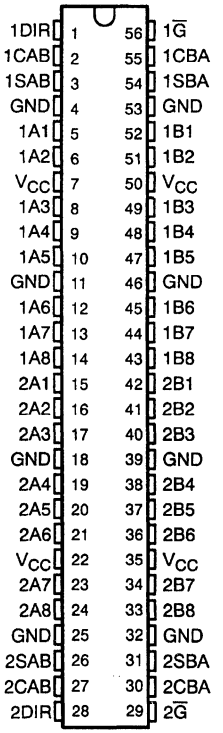
54ACT16646 ... WD PACKAGE
74ACT16646 ... DL PACKAGE
(TOP VIEW)



description

The 'ACT16646 is a 16-bit bus transceiver, which consists of D-type flip-flops and control circuitry with 3-state outputs arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock input (CAB or CBA). Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable ($\overline{G}$) and direction (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus receivers data when $\overline{G}$ is low. In the isolation mode ($\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

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The 54ACT16646 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11646 is characterized for operation from −40°C to 85°C.

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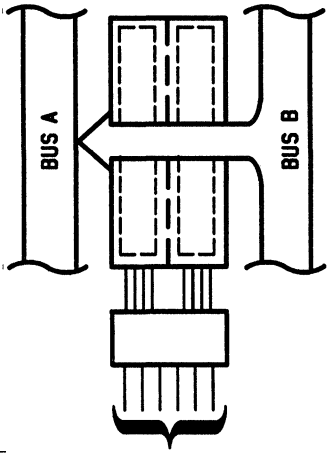
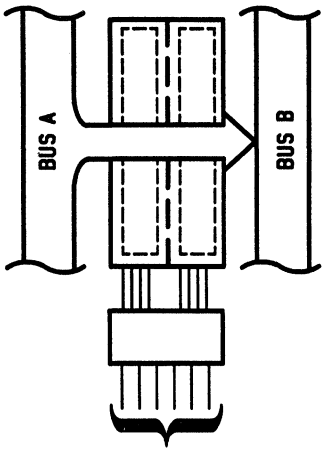


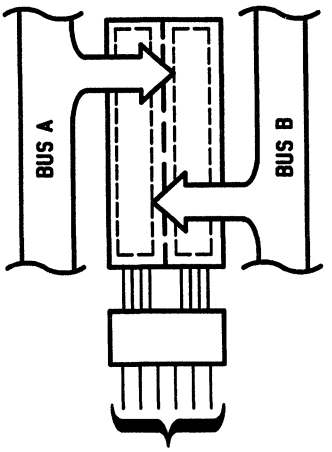
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



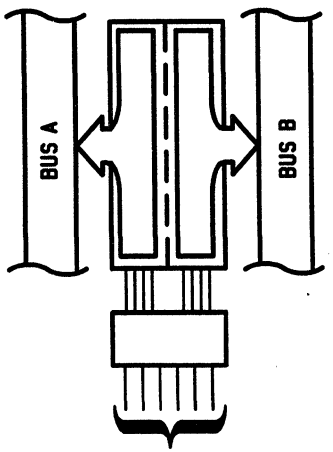
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



$\overline{G}$	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B OR A AND B



$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	H or L	X	X
L	H	H or L	X	H	X

TRANSFER STORED DATA TO A OR B

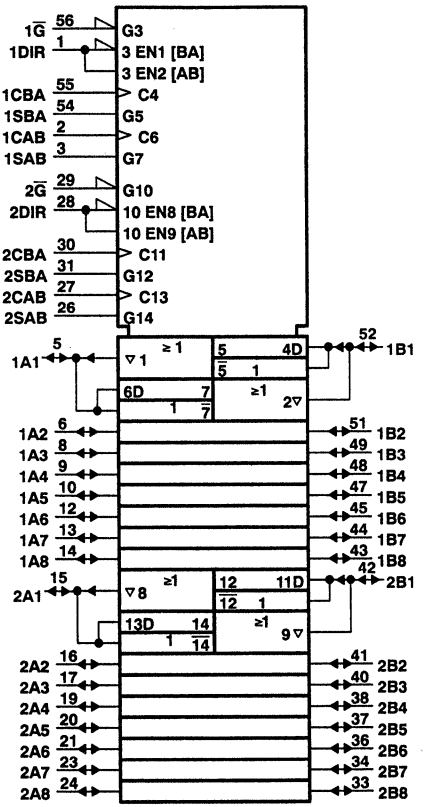
FIGURE 1. BUS TRANSFER DIAGRAM

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus

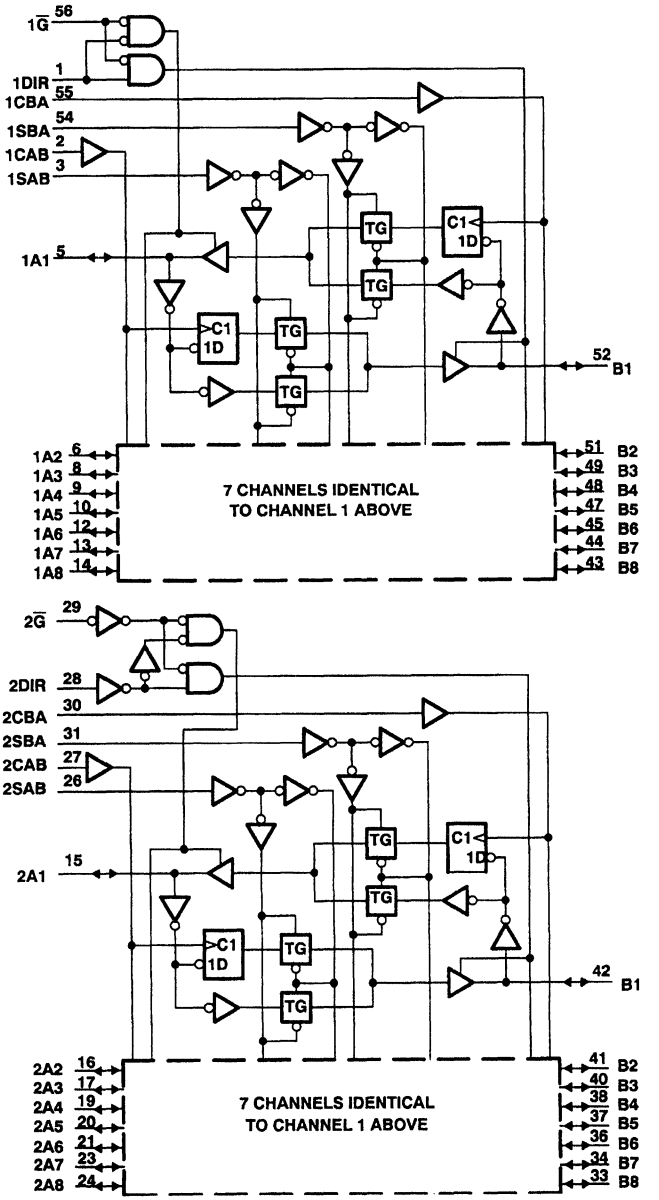
† The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT16646		74ACT16646		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTES: 2. All V_{CC} and GND pins must be connected to the proper voltage supply.
3. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of 5 kΩ or greater.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16646		74AC16646		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.94		3.8		
			5.5 V	4.94			4.94		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports‡	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (unless otherwise noted) (see Note 3)

			T_A = 25°C		54ACT16646		74ACT16646		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	90	0	90	0	90	MHz
t_w	Pulse duration, CAB or CBA high or low		5.5		5.5		5.5		ns
t_{su}	Setup time, A before CAB ↑ or B before CBA ↑	Data high	4		4		4		ns
		Data low	6		6		6		
t_h	Hold time, A after CAB ↑ or B after CBA ↑		1.5		1.5		1.5		ns

NOTE: 3. Load circuits and voltage waveforms are shown in Section 1 of *Advanced CMOS Logic Data Book, 1990.*

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16646		74ACT16646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			90			90		90		MHz
t_{PLH}	A or B	B or A	3.9	7.5	9.4	3.9	11.5	3.9	10.6	ns
t_{PHL}			3.4	7.6	10.8	3.4	12.2	3.4	11.4	
t_{PZH}	$\overline{G}$	A or B	3.2	7.7	10.8	3.2	12.9	3.2	11.9	ns
t_{PZL}			4.2	9.0	12.2	4.2	14.6	4.2	13.5	
t_{PHZ}	$\overline{G}$	A or B	5.3	7.7	9.6	5.3	10.4	5.3	10.2	ns
t_{PLZL}			4.9	7.3	9.2	4.9	10.3	4.9	9.9	
t_{PLH}	CBA or CAB	A or B	4.9	8.9	11.1	4.9	13.1	4.9	12.2	ns
t_{PHL}			5.1	9.0	11.0	5.1	13.1	5.1	12.3	
t_{PLH}	SAB or SBA† (with A or B high)	A or B	5.2	10.3	13.8	5.2	17.2	5.2	15.6	ns
t_{PHL}			4.9	8.2	10.6	4.9	12.5	4.9	11.7	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	4.3	7.8	9.9	4.3	12.1	4.3	11.1	ns
t_{PHL}			5.9	11.2	14.9	5.9	18.2	5.9	16.7	
t_{PZH}	DIR	A or B	4.5	9.5	13.8	4.5	18.2	4.5	15.2	ns
t_{PZL}			4.3	9.2	11.8	4.3	14.2	4.3	13.1	
t_{PHZ}	DIR	A or B	4.5	7.9	10.2	4.5	11.2	4.5	10.8	ns
t_{PLZ}			4.4	7.5	9.8	4.4	10.8	4.4	10.4	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE: 3. Load circuits and voltage waveforms are shown in Section 1 of *Advanced CMOS Logic Data Book, 1990.*

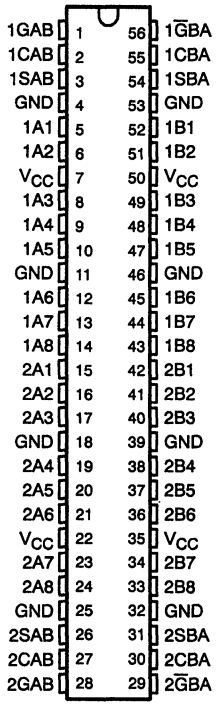
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per tranceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	58	pF
		Outputs disabled		13	

TI0190—D3463, MARCH 1990

- **Member of the Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Bus Transceivers/Registers**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16652 ... WD PACKAGE
74AC16652 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16652 is a 16-bit bus transceiver which consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Enable GAB and $\overline{G}$BA are provided to control the transceiver functions, SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}$BA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The 74AC16652 is packaged in the TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54AC16652 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC16652 is characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

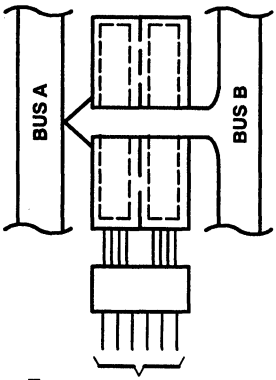
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified	Input	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

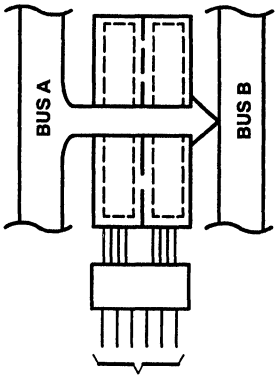
† The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

PRODUCT PREVIEW



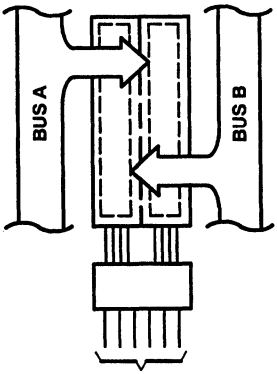
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



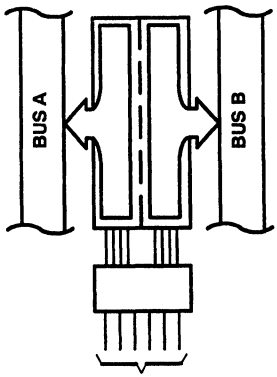
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A, B OR A AND B



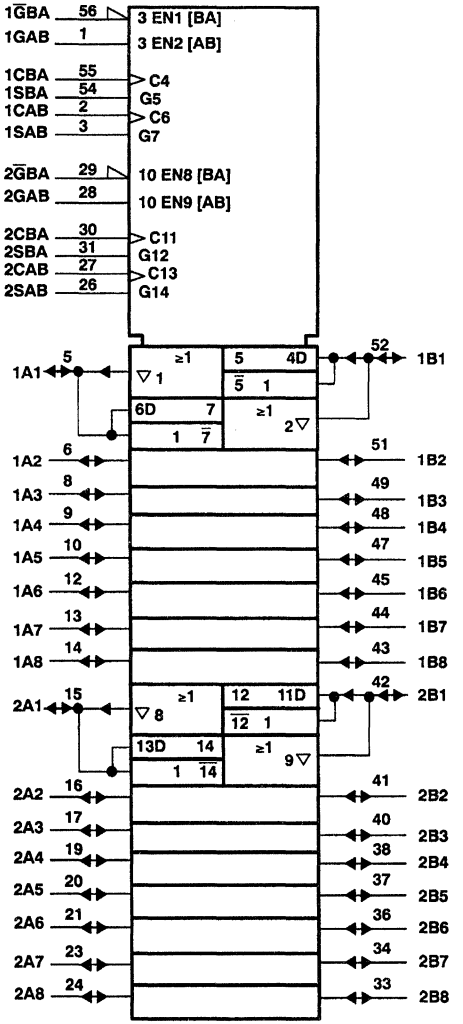
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA TO A OR B

FIGURE 1. BUS TRANSFER DIAGRAM

PRODUCT PREVIEW

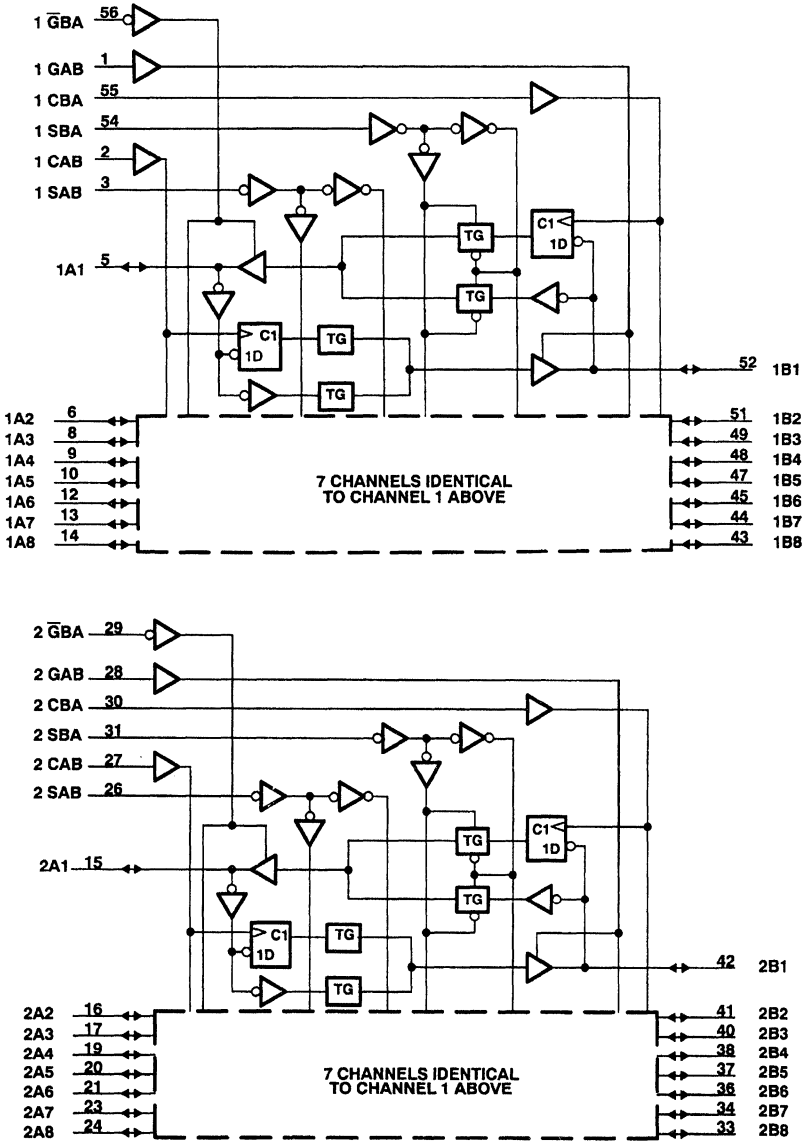
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC16652			74AC16652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16652		74AC16652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports‡	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		16						pF

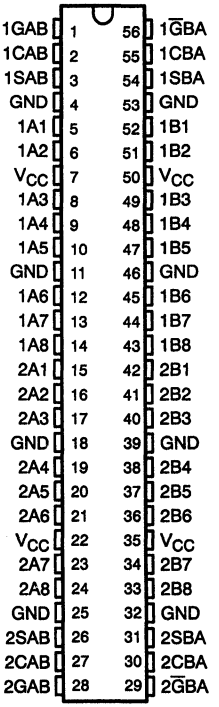
† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

TI0191—D3464, MARCH 1990

- **Member of the Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL-Voltage Compatible**
- **Bus Transceivers/Registers**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16652 . . . WD PACKAGE
74ACT16652 . . . DL PACKAGE
(TOP VIEW)



description

The 'ACT16652 is a 16-bit bus transceiver which consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Enable GAB and $\overline{G}$BA are provided to control the transceiver functions, SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}$BA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The 74ACT16652 is packaged in the TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54ACT16652 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT16652 is characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

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TEXAS INSTRUMENTS
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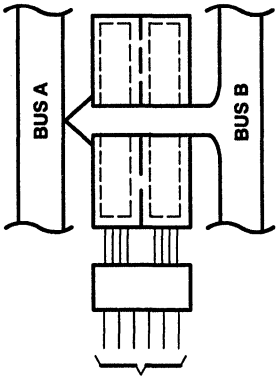
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified	Input	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored B Data to A Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

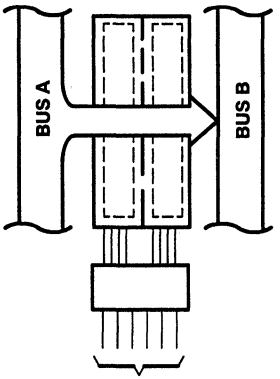
† The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

PRODUCT PREVIEW



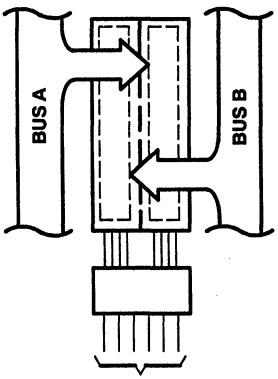
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



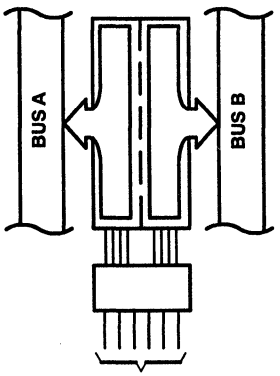
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A, B OR A AND B



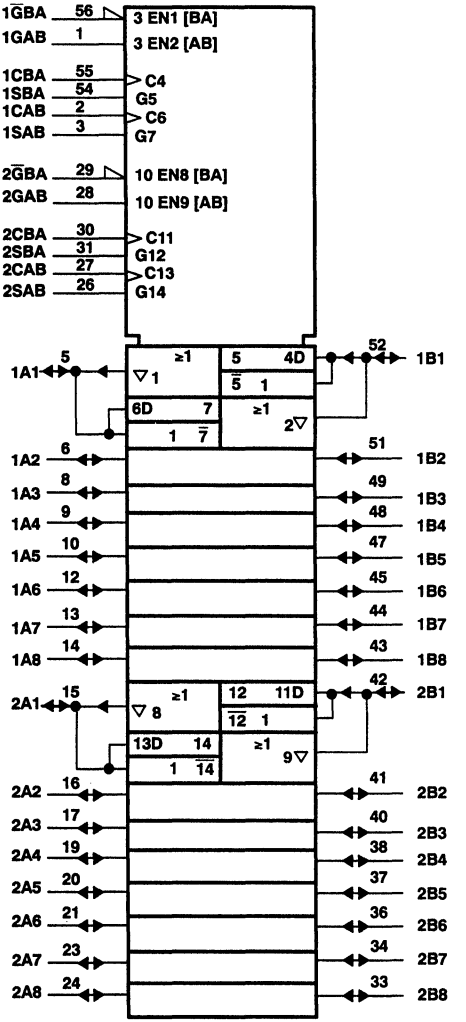
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA TO A OR B

FIGURE 1. BUS TRANSFER DIAGRAM

PRODUCT PREVIEW

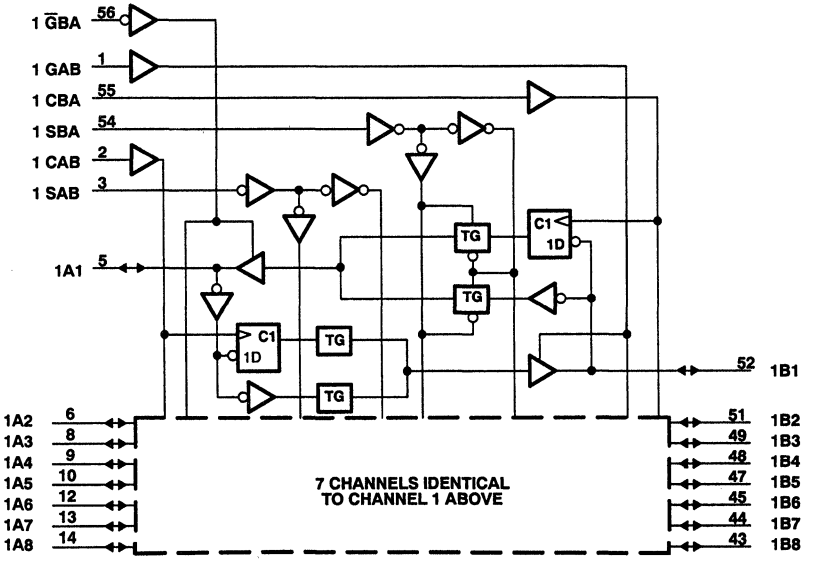
logic symbol†

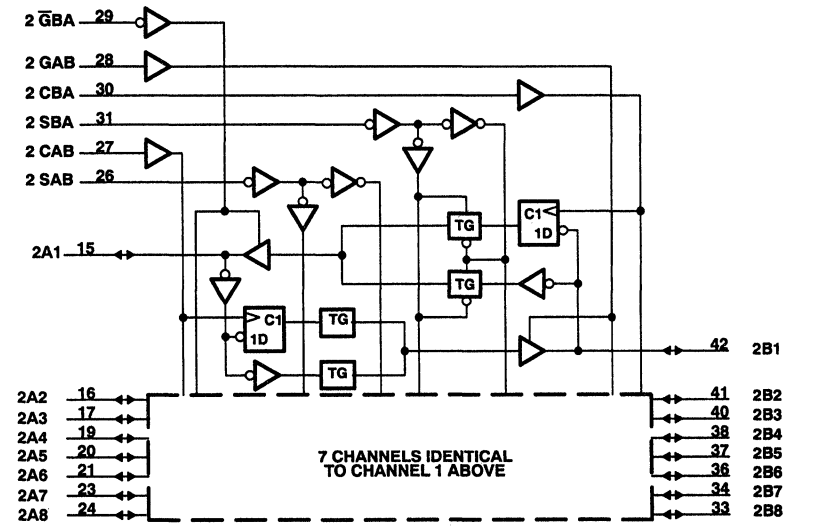


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagrams (positive logic)





PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT16652			74ACT16652			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

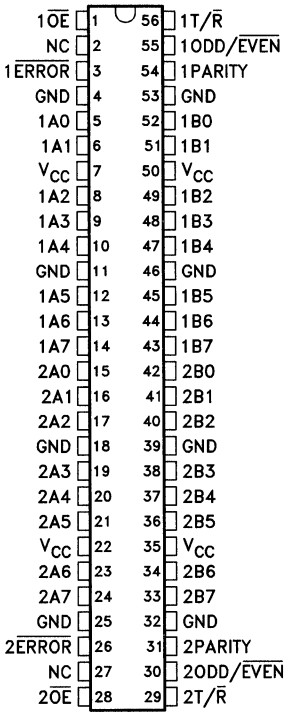
PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16652		74ACT16652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.94		3.8		
			5.5 V	4.94			4.94		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

PRODUCT PREVIEW

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16657 ... WD PACKAGE
74AC16657 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16657 contains two noninverting octal transceiver sections with separate parity generator/checker circuits and control signals. For either section, the transmit/receive input (1T/$\overline{R}$ or 2T/$\overline{R}$) determines the direction of data flow. When 1T/$\overline{R}$ (or 2T/$\overline{R}$) is high, data flows from the 1A (or 2A) port to the 1B (or 2B) port (transmit mode); when 1T/$\overline{R}$ (or 2T/$\overline{R}$) is low, data flows from the 1B (or 2B) port to the 1A (or 2A) port (receive mode). When the output-enable input 1$\overline{OE}$ (or 2$\overline{OE}$) is high, both the 1A (or 2A) and 1B (or 2B) ports are in the high-impedance state.

Odd or even parity is selected by a logic high or low level, respectively, on the 1ODD/$\overline{EVEN}$ (or 2ODD/$\overline{EVEN}$) input. 1PARITY (or 2PARITY) carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

In the transmit mode, after the 1A (or 2A) bus is polled to determine the number of high bits, 1PARITY (or 2PARITY) is set to the logic level that maintains the parity sense selected by the level at the 1ODD/$\overline{EVEN}$ (or 2ODD/$\overline{EVEN}$) input. For example, if 1ODD/$\overline{EVEN}$ is low (even parity selected) and there are five high bits on the 1A bus, then 1PARITY is set to the logic high level so that an even number of the nine total bits (eight 1A-bus bits plus parity bit) are high.

In the receive mode, after the 1B (or 2B) bus is polled to determine the number of high bits, the 1$\overline{ERROR}$ (or 2$\overline{ERROR}$) output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if 1ODD/$\overline{EVEN}$ is high (odd parity selected), 1PARITY is high, and there are three high bits on the 1B bus, then 1$\overline{ERROR}$ is low, indicating a parity error.

PRODUCT PREVIEW

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The 'AC16657 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board.

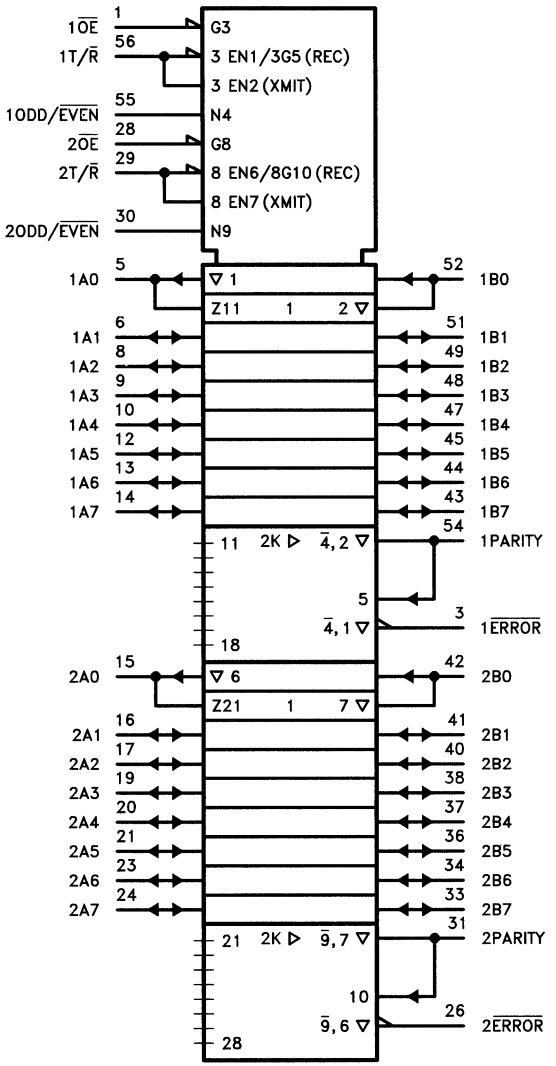
The 54AC16657 is characterized over the full military temperature range of −55°C to 125°C. The 74AC16657 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE, EACH SECTION

NUMBER OF A OR B	INPUTS			INPUT/OUTPUT	OUTPUTS	
INPUTS THAT ARE HIGH	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	PARITY	$\overline{ERROR}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
DON'T CARE	H	X	X	Z	Z	Z

PRODUCT PREVIEW

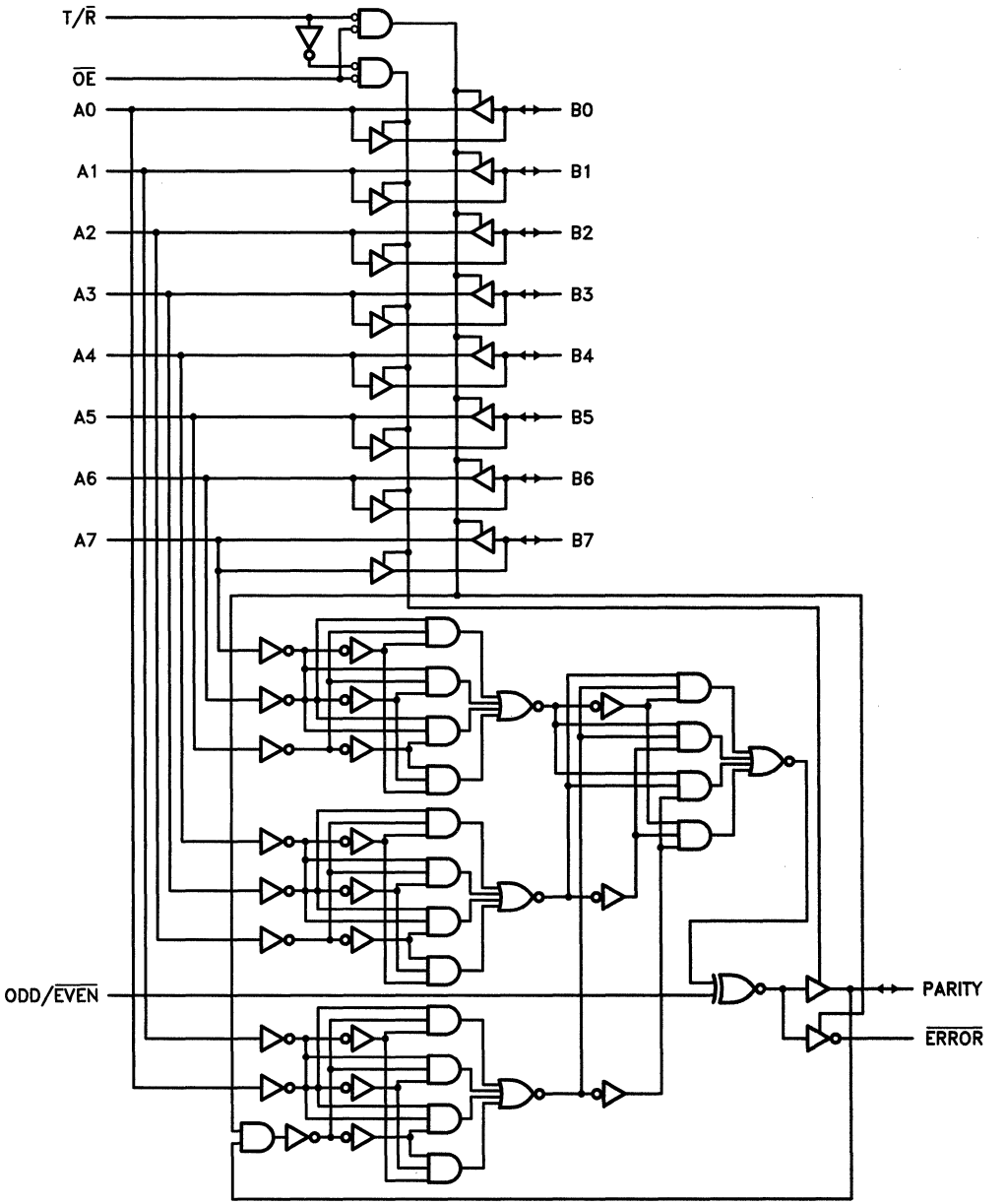
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram, each transceiver (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±500 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC16657			74AC16657			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage power supply.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16657		74AC16657		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports‡	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16657		74AC16657		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A								ns
t_{PHL}										
t_{PLH}	A_n	PARITY								ns
t_{PHL}										
t_{PLH}	ODD/$\overline{EVEN}$	PARITY,$\overline{ERROR}$								ns
t_{PHL}										
t_{PLH}	B_n	$\overline{ERROR}$								ns
t_{PHL}										
t_{PLH}	PARITY	$\overline{ERROR}$								ns
t_{PHL}										
t_{PZH}	$\overline{OE}$	A_n, B_n, PARITY or $\overline{ERROR}$								ns
t_{PZL}										
t_{PHZ}	$\overline{OE}$	A_n, B_n, PARITY or $\overline{ERROR}$								ns
t_{PLZ}										

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16657		74AC16657		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A								ns
t_{PHL}										
t_{PLH}	A_n	PARITY								ns
t_{PHL}										
t_{PLH}	ODD/$\overline{EVEN}$	PARITY,$\overline{ERROR}$								ns
t_{PHL}										
t_{PLH}	B_n	$\overline{ERROR}$								ns
t_{PHL}										
t_{PLH}	PARITY	$\overline{ERROR}$								ns
t_{PHL}										
t_{PZH}	$\overline{OE}$	A_n, B_n, PARITY or $\overline{ERROR}$								ns
t_{PZL}										
t_{PHZ}	$\overline{OE}$	A_n, B_n, PARITY or $\overline{ERROR}$								ns
t_{PLZ}										

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

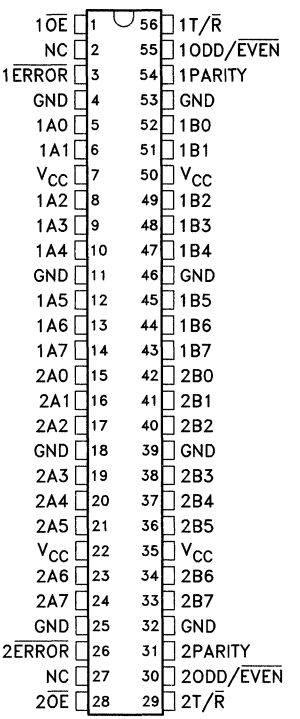
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz		pF
		Outputs disabled			

PRODUCT PREVIEW

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **3-State Outputs Drive Bus Lines Directly**
- **Inputs are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16657 ... WD PACKAGE
74ACT16657 ... DL PACKAGE
(TOP VIEW)



description

The 'ACT16657 contains two noninverting octal transceiver sections with separate parity generator/checker circuits and control signals. For either section, the transmit/receive input (1T/$\overline{R}$ or 2T/$\overline{R}$) determines the direction of data flow. When 1T/$\overline{R}$ (or 2T/$\overline{R}$) is high, data flows from the 1A (or 2A) port to the 1B (or 2B) port (transmit mode); when 1T/$\overline{R}$ (or 2T/$\overline{R}$) is low, data flows from the 1B (or 2B) port to the 1A (or 2A) port (receive mode). When the output-enable input 1$\overline{OE}$ (or 2$\overline{OE}$) is high, both the 1A (or 2A) and 1B (or 2B) ports are in the high-impedance state.

Odd or even parity is selected by a logic high or low level, respectively, on the 1ODD/$\overline{EVEN}$ (or 2ODD/$\overline{EVEN}$) input. 1PARITY (or 2PARITY) carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

In the transmit mode, after the 1A (or 2A) bus is polled to determine the number of high bits, 1PARITY (or 2PARITY) is set to the logic level that maintains the parity sense selected by the level at the 1ODD/$\overline{EVEN}$ (or 2ODD/$\overline{EVEN}$) input. For example, if 1ODD/$\overline{EVEN}$ is low (even parity selected) and there are five high bits on the 1A bus, then 1PARITY is set to the logic high level so that an even number of the nine total bits (eight 1A-bus bits plus parity bit) are high.

In the receive mode, after the 1B (or 2B) bus is polled to determine the number of high bits, the 1$\overline{ERROR}$ (or 2$\overline{ERROR}$) output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if 1ODD/$\overline{EVEN}$ is high (odd parity selected), 1PARITY is high, and there are three high bits on the 1B bus, then 1$\overline{ERROR}$ is low, indicating a parity error.

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PRODUCT PREVIEW

description (continued)

The 'ACT16657 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board.

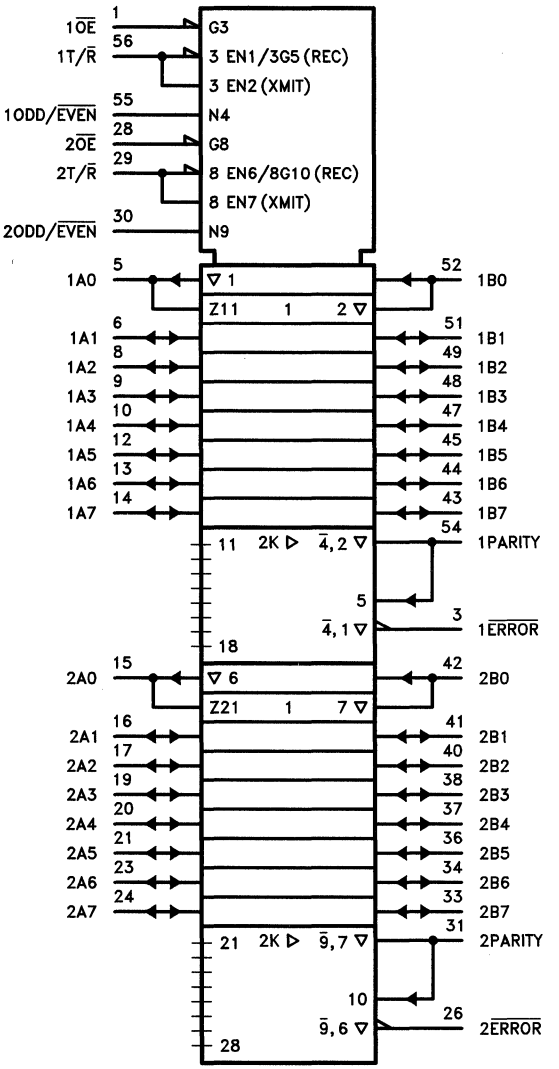
The 54ACT16657 is characterized over the full military temperature range of −55°C to 125°C. The 74ACT16657 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE, EACH SECTION

NUMBER OF A OR B	INPUTS			INPUT/OUTPUT	OUTPUTS	
INPUTS THAT ARE HIGH	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	PARITY	$\overline{ERROR}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
DON'T CARE	H	X	X	Z	Z	Z

PRODUCT PREVIEW

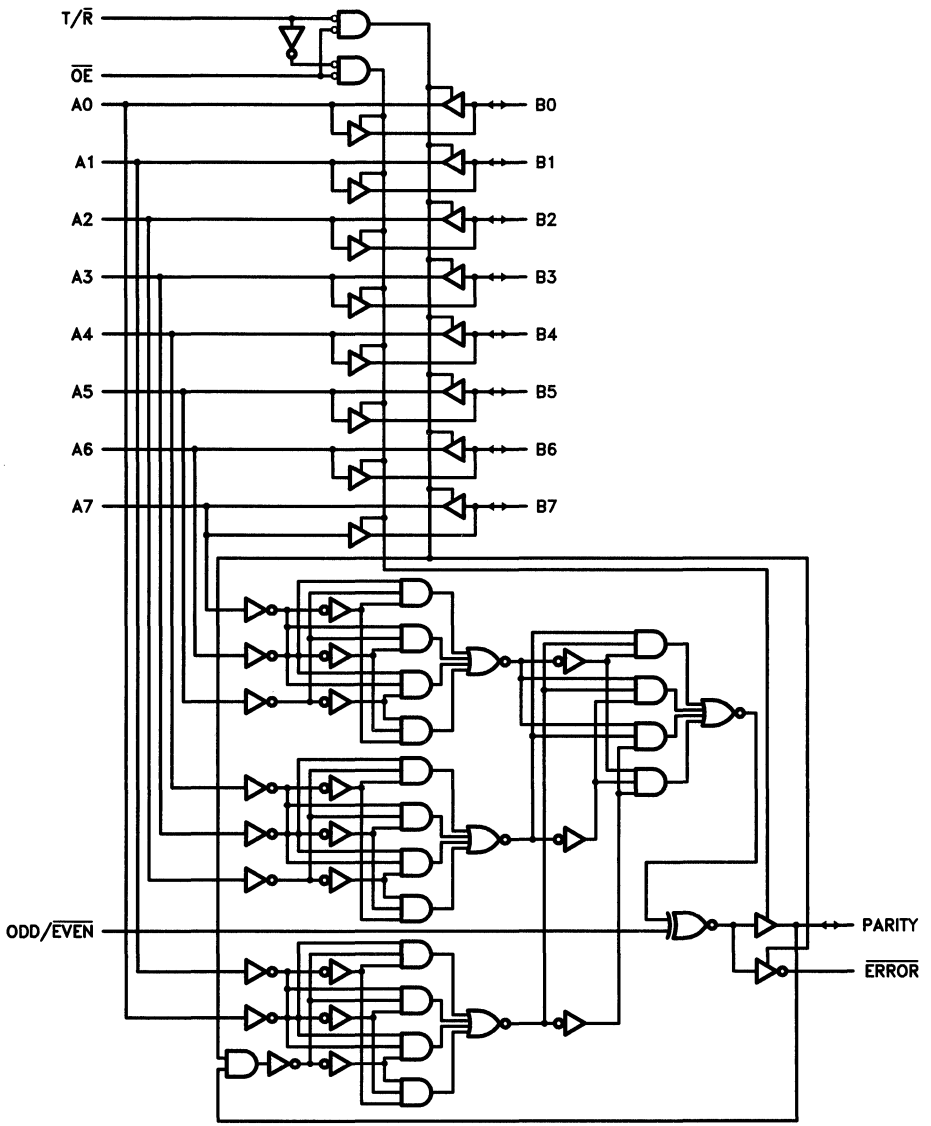
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram, each transceiver (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±500 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54ACT16657			74ACT16657			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage power supply.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16657		74ACT16657		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports‡	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16657		74ACT16657		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A								ns
t_{PHL}										
t_{PLH}	A_n	PARITY								ns
t_{PHL}										
t_{PLH}	ODD/$\overline{EVEN}$	PARITY,$\overline{ERROR}$								ns
t_{PHL}										
t_{PLH}	B_n	$\overline{ERROR}$								ns
t_{PHL}										
t_{PLH}	PARITY	$\overline{ERROR}$								ns
t_{PHL}										
t_{PZH}	$\overline{OE}$	A_n, B_n, PARITY or $\overline{ERROR}$								ns
t_{PZL}										
t_{PHZ}	$\overline{OE}$	A_n, B_n, PARITY or $\overline{ERROR}$								ns
t_{PLZ}										

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16657		74ACT16657		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A								ns
t_{PHL}										
t_{PLH}	A_n	PARITY								ns
t_{PHL}										
t_{PLH}	ODD/$\overline{EVEN}$	PARITY,$\overline{ERROR}$								ns
t_{PHL}										
t_{PLH}	B_n	$\overline{ERROR}$								ns
t_{PHL}										
t_{PLH}	PARITY	$\overline{ERROR}$								ns
t_{PHL}										
t_{PZH}	$\overline{OE}$	A_n, B_n, PARITY or $\overline{ERROR}$								ns
t_{PZL}										
t_{PHZ}	$\overline{OE}$	A_n, B_n, PARITY or $\overline{ERROR}$								ns
t_{PLZ}										

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz		pF
		Outputs disabled			

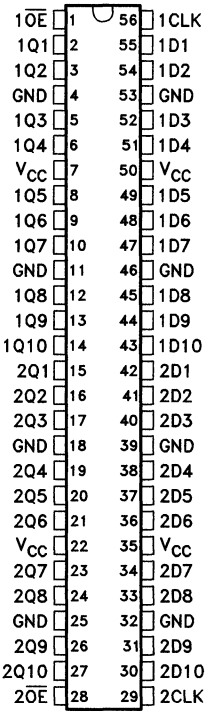
PRODUCT PREVIEW

20-BIT D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

TI0252—D3575, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16821, 54ACT16821 ... WD PACKAGE
74AC16821, 74ACT16821 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16821 and 'ACT16821 are noninverting 20-bit D-type flip-flops composed of two 10-bit sections with separate control signals. For either 10-bit flip-flop section, the data present at the corresponding D inputs is stored in the flip-flops on the rising edge of the clock input (1CLK or 2CLK) and appears on the appropriate Q outputs if the output enable $1\overline{OE}$ (or $2\overline{OE}$) is low. If $1\overline{OE}$ (or $2\overline{OE}$) is high, the outputs are in the high-impedance state. $1\overline{OE}$ (or $2\overline{OE}$) does not affect the operation of the flip-flops. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE, EACH SECTION

INPUTS		FLIP-FLOP DATA	Q OUTPUTS
CLK	$\overline{OE}$		
↑	H	Current D Data	Z
L	H	Previous D Data	Z
↑	L	Current D Data	Current D Data
L	L	Previous D Data	Previous D Data

PRODUCT PREVIEW

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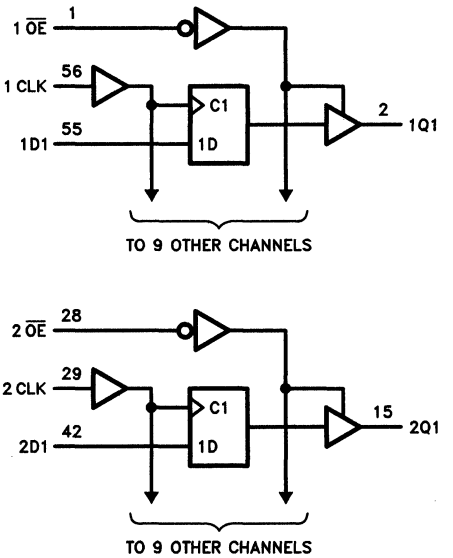
The 74AC16821 and 74ACT16821 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16821 has CMOS-compatible input thresholds. The 'ACT16821 has TTL-compatible input thresholds.

The 54AC16821 and 54ACT16821 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16821 and 74ACT16821 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)



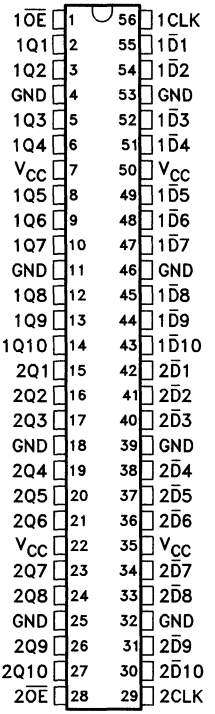
PRODUCT PREVIEW

20-BIT D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

TI0253—D3576, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16822, 54ACT16822 ... WD PACKAGE
74AC16822, 74ACT16822 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16822 and 'ACT16822 are inverting 20-bit D-type flip-flops composed of two 10-bit sections with separate control signals. For either 10-bit flip-flop section, the inverse of the data present at the corresponding D inputs is stored in the flip-flops on the rising edge of the clock input (1CLK or 2CLK) and appears on the appropriate Q outputs if the output enable $1\overline{OE}$ (or $2\overline{OE}$) is low. If $1\overline{OE}$ (or $2\overline{OE}$) is high, the outputs are in the high-impedance state. $1\overline{OE}$ (or $2\overline{OE}$) does not affect the operation of the flip-flops. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE, EACH SECTION

INPUTS		FLIP-FLOP DATA	Q OUTPUTS
CLK	$\overline{OE}$		
↑	H	Current $\overline{D}$ Data	Z
L	H	Previous $\overline{D}$ Data	Z
↑	L	Current $\overline{D}$ Data	Inverse of Current $\overline{D}$ Data
L	L	Previous $\overline{D}$ Data	Inverse of Previous $\overline{D}$ Data

PRODUCT PREVIEW

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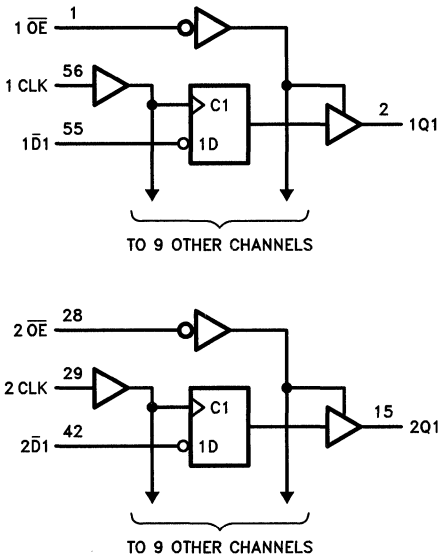
The 74AC16822 and 74ACT16822 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16822 has CMOS-compatible input thresholds. The 'ACT16822 has TTL-compatible input thresholds.

The 54AC16822 and 54ACT16822 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16822 and 74ACT16822 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)



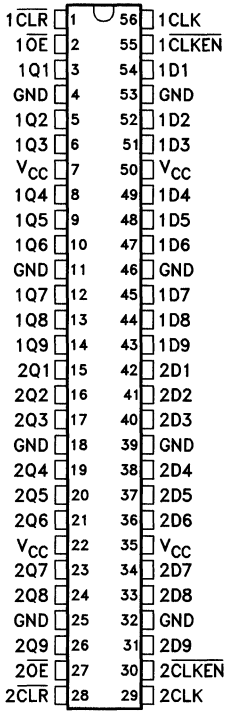
PRODUCT PREVIEW

18-BIT D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

TI0254—D3577, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16823, 54ACT16823 ... WD PACKAGE
74AC16823, 74ACT16823 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16823 and 'ACT16823 are noninverting 18-bit D-type flip-flops composed of two 9-bit sections with separate control signals. For either 9-bit flip-flop section, if the clock enable (1$\overline{\text{CLKEN}}$ or 2$\overline{\text{CLKEN}}$) is low, the data present at the corresponding D inputs is stored in the flip-flops on the rising edge of 1CLK (or 2CLK). When 1$\overline{\text{CLKEN}}$ (or 2$\overline{\text{CLKEN}}$) is high, the flip-flops retain their previously stored values. Taking 1$\overline{\text{CLR}}$ (or 2$\overline{\text{CLR}}$) low asynchronously clears the corresponding flip-flops.

When the output enable (1$\overline{\text{OE}}$ or 2$\overline{\text{OE}}$) is low, the corresponding Q outputs are active (high or low logic levels). When 1$\overline{\text{OE}}$ (or 2$\overline{\text{OE}}$) is high, the corresponding outputs are in the high-impedance state. 1$\overline{\text{OE}}$ (or 2$\overline{\text{OE}}$) does not affect the internal operation of the flip-flops: previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE, EACH SECTION

INPUTS				FLIP-FLOP DATA	Q OUTPUTS
$\overline{\text{CLR}}$	$\overline{\text{CLKEN}}$	CLK	$\overline{\text{OE}}$		
L	X	X	L	L	L
H	H	X	L	Previous D Data	Previous D Data
H	X	L	L	Previous D Data	Previous D Data
H	L	↑	L	Current D Data	Current D Data
H	H	X	H	Previous D Data	Z
H	X	L	H	Previous D Data	Z
H	L	↑	H	Current D Data	Z

PRODUCT PREVIEW

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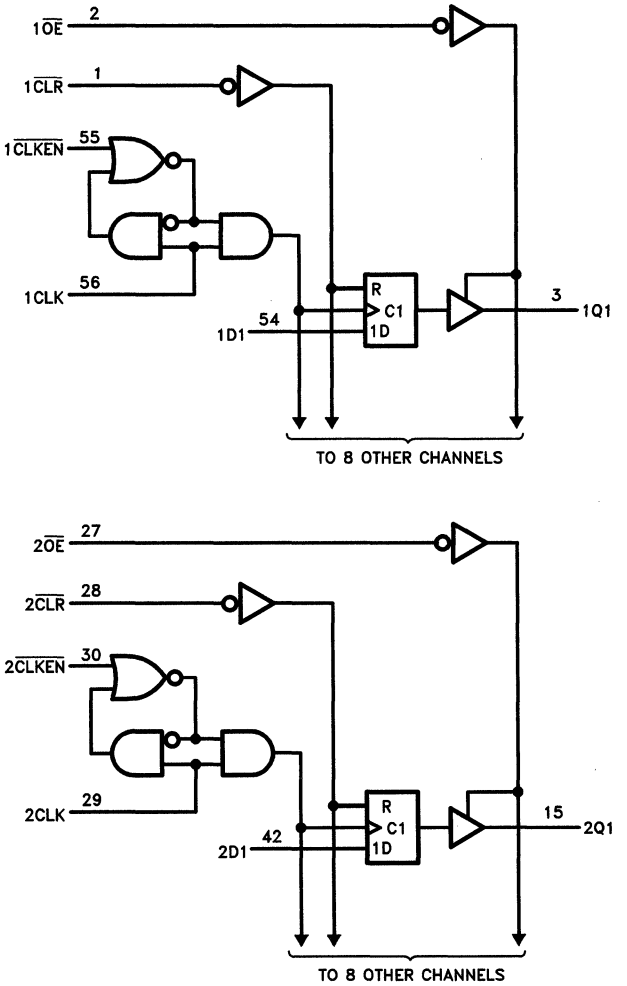
The 74AC16823 and 74ACT16823 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16823 has CMOS-compatible input thresholds. The 'ACT16823 has TTL-compatible input thresholds.

The 54AC16823 and 54ACT16823 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16823 and 74ACT16823 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)



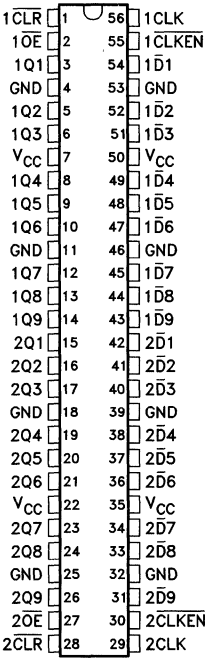
PRODUCT PREVIEW

18-BIT D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

TI0255—D3578, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16824, 54ACT16824 ... WD PACKAGE
74AC16824, 74ACT16824 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16824 and 'ACT16824 are inverting 18-bit D-type flip-flops composed of two 9-bit sections with separate control signals. For either 9-bit flip-flop section, if the clock enable (1$\overline{\text{CLKEN}}$ or 2$\overline{\text{CLKEN}}$) is low, the inverse of the data present at the corresponding D inputs is stored in the flip-flops on the rising edge of 1CLK (or 2CLK). When 1$\overline{\text{CLKEN}}$ (or 2$\overline{\text{CLKEN}}$) is high, the flip-flops retain their previously stored values. Taking 1$\overline{\text{CLR}}$ (or 2$\overline{\text{CLR}}$) low asynchronously clears the corresponding flip-flops.

When the output enable (1$\overline{\text{OE}}$ or 2$\overline{\text{OE}}$) is low, the corresponding Q outputs are active (high or low logic levels). When 1$\overline{\text{OE}}$ (or 2$\overline{\text{OE}}$) is high, the corresponding outputs are in the high-impedance state. 1$\overline{\text{OE}}$ (or 2$\overline{\text{OE}}$) does not affect the internal operation of the flip-flops: previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE, EACH SECTION

INPUTS				FLIP-FLOP DATA	Q OUTPUTS
$\overline{\text{CLR}}$	$\overline{\text{CLKEN}}$	CLK	$\overline{\text{OE}}$		
L	X	X	L	L	L
H	H	X	L	Previous $\overline{\text{D}}$ Data	Inverse of Previous $\overline{\text{D}}$ Data
H	X	L	L	Previous $\overline{\text{D}}$ Data	Inverse of Previous $\overline{\text{D}}$ Data
H	L	↑	L	Current $\overline{\text{D}}$ Data	Inverse of Current $\overline{\text{D}}$ Data
H	H	X	H	Previous $\overline{\text{D}}$ Data	Z
H	X	L	H	Previous $\overline{\text{D}}$ Data	Z
H	L	↑	H	Current $\overline{\text{D}}$ Data	Z

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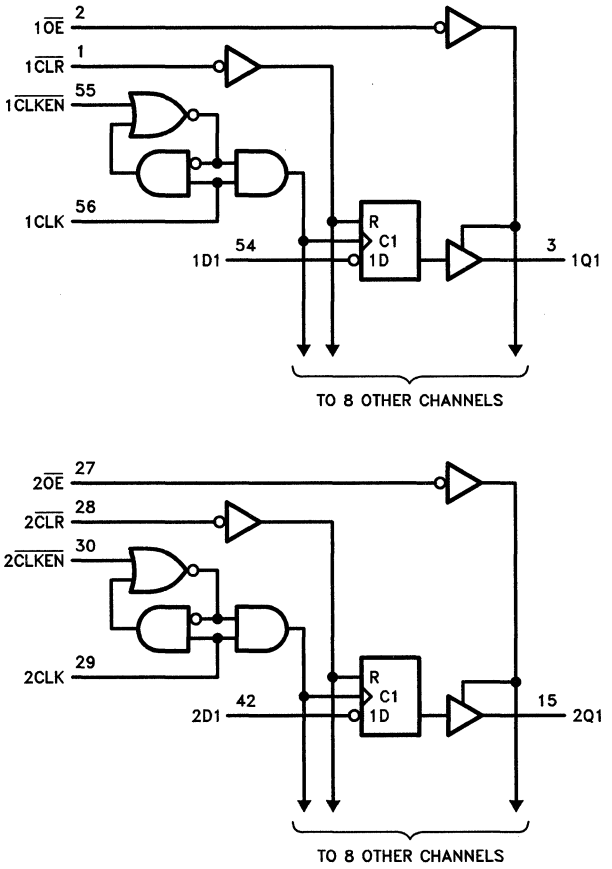
PRODUCT PREVIEW

The 74AC16824 and 74ACT16824 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16824 has CMOS-compatible input thresholds. The 'ACT16824 has TTL-compatible input thresholds.

The 54AC16824 and 54ACT16824 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16824 and 74ACT16824 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)



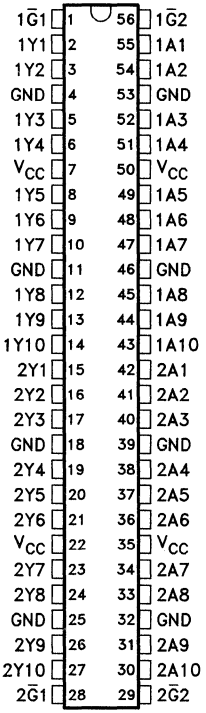
PRODUCT PREVIEW

20-BIT BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

TI0268—D3544, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16827, 54ACT16827 ... WD PACKAGE
74AC16827, 74ACT16827 ... DL PACKAGE
(TOP VIEW)



description

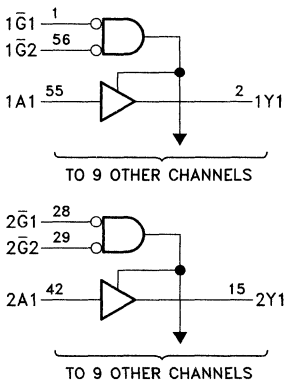
The 'AC16827 and 'ACT16827 are noninverting 20-bit buffers composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output enable inputs ($1\overline{G}1$ and $1\overline{G}2$ or $2\overline{G}1$ and $2\overline{G}2$) must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

The 74AC16827 and 74ACT16827 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16827 has CMOS-compatible input thresholds. The 'ACT16827 has TTL-compatible input thresholds.

The 54AC16827 and 54ACT16827 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16827 and 74ACT16827 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)



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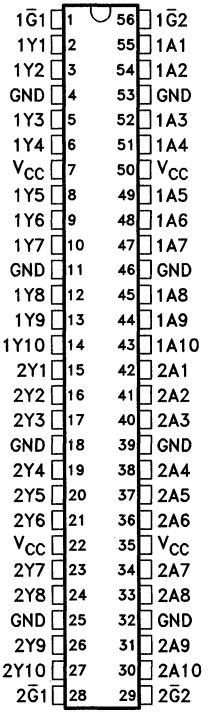
PRODUCT PREVIEW

20-BIT BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

TI0269—D3545, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16828, 54ACT16828 ... WD PACKAGE
74AC16828, 74ACT16828 ... DL PACKAGE
(TOP VIEW)



description

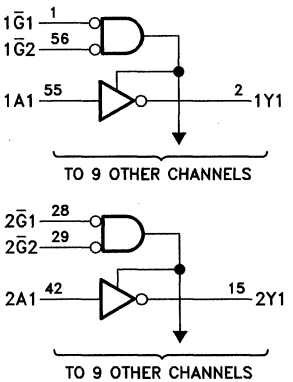
The 'AC16828 and 'ACT16828 are inverting 20-bit buffers composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output enable inputs ($1\overline{G}1$ and $1\overline{G}2$ or $2\overline{G}1$ and $2\overline{G}2$) must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are placed into the high-impedance state.

The 74AC16828 and 74ACT16828 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16828 has CMOS-compatible input thresholds. The 'ACT16828 has TTL-compatible input thresholds.

The 54AC16828 and 54ACT16828 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16828 and 74ACT16828 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)



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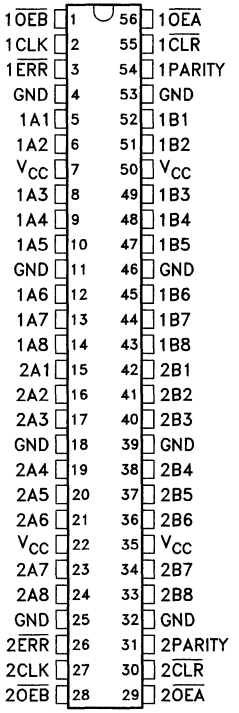
PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TI0270—D3546, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-up Immunity at 125°C**

54AC16833, 54ACT16833 ... WD PACKAGE
74AC16833, 74ACT16833 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16833 and 'ACT16833 contain two noninverting 8-bit to 9-bit parity bus transceivers. For each transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B input data to generate an active-low error flag if odd parity is not detected.

The error output ($1\overline{ERR}$ or $2\overline{ERR}$) is configured as an open-collector output. The B-to-A parity error flag is clocked into $1\overline{ERR}$ (or $2\overline{ERR}$) on the low-to-high transition of 1CLK (or 2CLK). $1\overline{ERR}$ (or $2\overline{ERR}$) is cleared (set high) by taking the clear input $1\overline{CLR}$ (or $2\overline{CLR}$) low.

The 74AC16833 and 74ACT16833 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16833 has CMOS-compatible input thresholds. The 'ACT16833 has TTL-compatible input thresholds.

The 54AC16833 and 54ACT16833 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16833 and 74ACT16833 are characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

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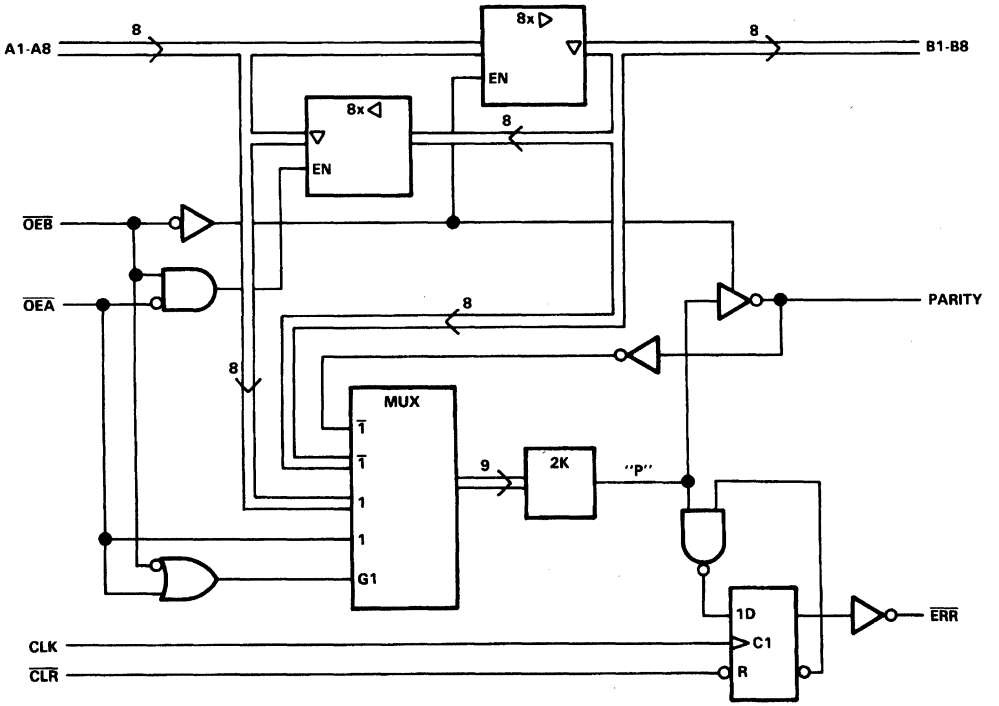
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic diagram, each transceiver (positive logic)

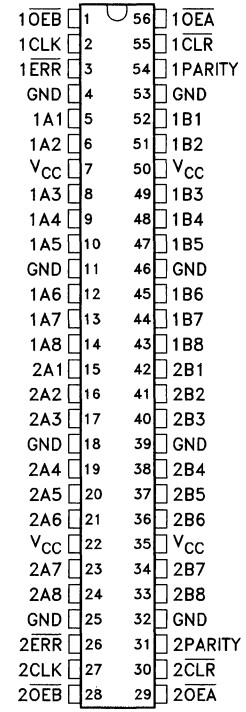


PRODUCT PREVIEW

TI0271—D3547, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16834, 54ACT16834 ... WD PACKAGE
74AC16834, 74ACT16834 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16834 and 'ACT16834 contain two inverting 8-bit to 9-bit parity bus transceivers. For each transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B input data to generate an active-low error flag if odd parity is not detected.

The error output (1$\overline{ERR}$ or 2$\overline{ERR}$) is configured as an open-collector output. The B-to-A parity error flag is clocked into 1$\overline{ERR}$ (or 2$\overline{ERR}$) on the low-to-high transition of 1CLK (or 2CLK). 1$\overline{ERR}$ (or 2$\overline{ERR}$) is cleared (set high) by taking the clear input 1$\overline{CLR}$ (or 2$\overline{CLR}$) low.

The 74AC16834 and 74ACT16834 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16834 has CMOS-compatible input thresholds. The 'ACT16834 has TTL-compatible input thresholds.

The 54AC16834 and 54ACT16834 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16834 and 74ACT16834 are characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

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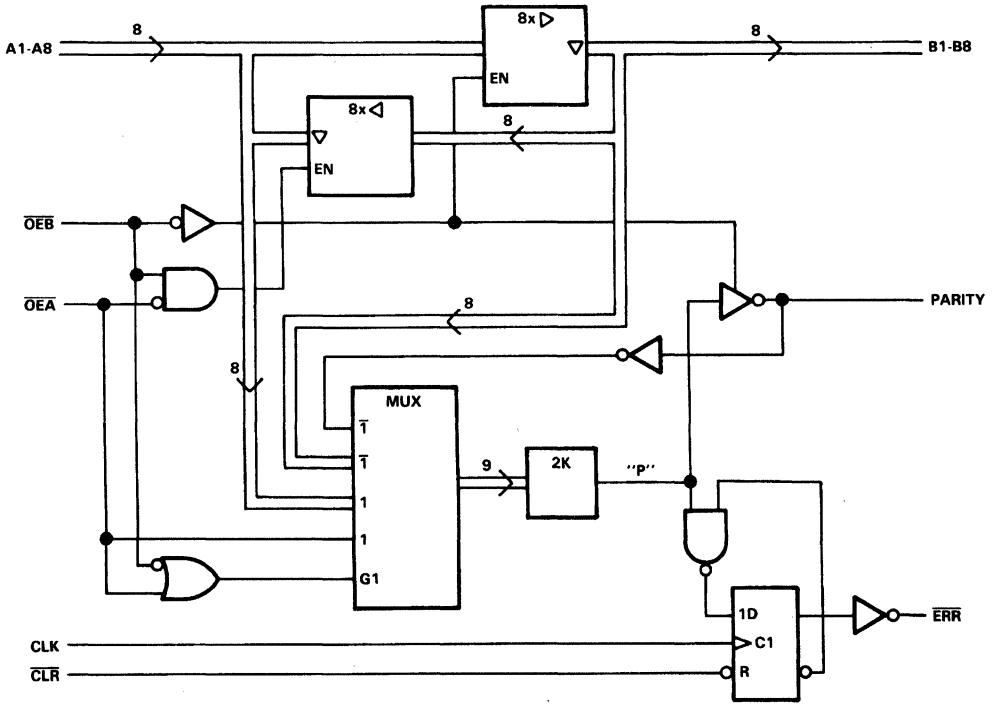
logic diagram, each transceiver (positive logic)

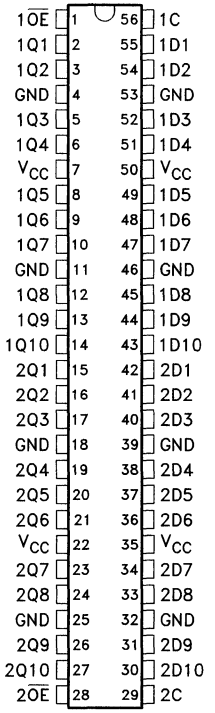


PRODUCT PREVIEW

TI0272—D3548, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

74AC/ACT16841 ... DL PACKAGE
54AC/ACT16841 ... WD PACKAGE
(TOP VIEW)



description

The 54AC/ACT16841 and 74AC/ACT16841 are noninverting 20-bit D-type latches composed of two 10-bit sections. Separate control signals are provided for each 10-bit section.

For each 10-bit section, when the enable input (1C or 2C) is low, the latches are placed into the storage mode. In contrast, when (1C or 2C) is high, the latches are transparent. In this mode, the data present at the 1D (or 2D) inputs is transmitted to the 1Q (or 2Q) outputs if $1\overline{OE}$ (or $2\overline{OE}$) is low. If $1\overline{OE}$ (or $2\overline{OE}$) is high, the corresponding outputs are in the high-impedance state.

The 74AC16841 and 74ACT16841 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16841 has CMOS-compatible input thresholds. The 'ACT16841 has TTL-compatible input thresholds.

The 54AC/ACT16841 is characterized over the full military temperature range of −55°C to 125°C. The 74AC/ACT16841 is characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

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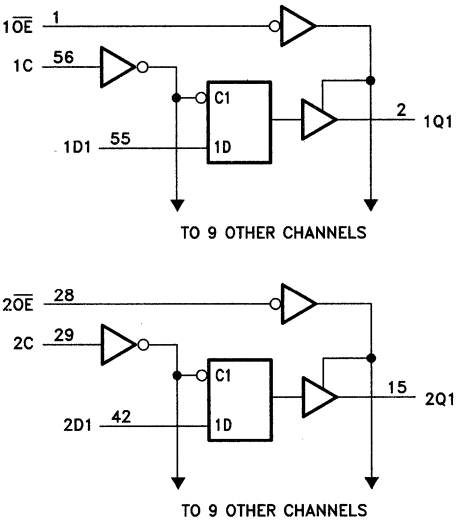
D3548, JUNE 1990—TI0272

logic diagram (positive logic)

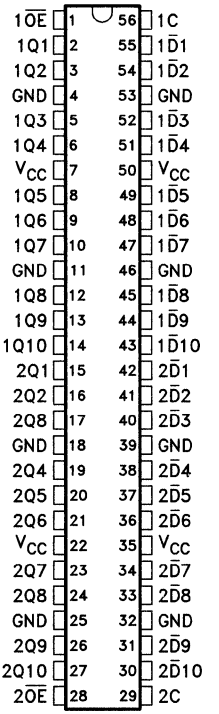


PRODUCT PREVIEW

TI0273—D3549, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16842, 54ACT16842 ... WD PACKAGE
74AC16842, 74ACT16842 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16842 and 'ACT16842 are inverting 20-bit D-type latches composed of two 10-bit sections with separate control signals. For each 10-bit section, when the enable input 1C (or 2C) is low, the latches are in the storage mode. In contrast, when 1C (or 2C) is high, the latches are transparent. In this mode, the inverse of the data present at the 1D (or 2D) inputs is transmitted to the 1Q (or 2Q) outputs if $1\overline{OE}$ (or $2\overline{OE}$) is low. If $1\overline{OE}$ (or $2\overline{OE}$) is high, the corresponding outputs are in the high-impedance state.

The 74AC16842 and 74ACT16842 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16842 has CMOS-compatible input thresholds. The 'ACT16842 has TTL-compatible input thresholds.

The 54AC16842 and 54ACT16842 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16842 and 74ACT16842 are characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

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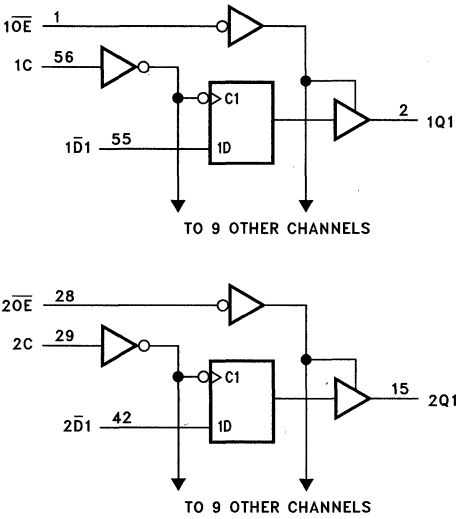
logic diagram (positive logic)

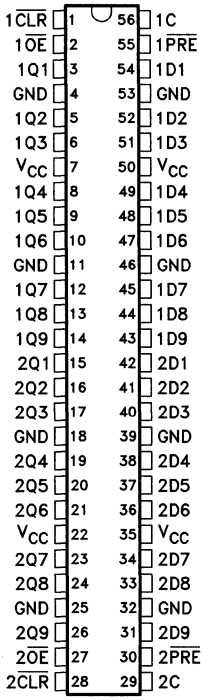


PRODUCT PREVIEW

TI0274—D3550, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16843, 54ACT16843 . . . WD PACKAGE
74AC16843, 74ACT16843 . . . DL PACKAGE
(TOP VIEW)



description

The 'AC16843 and 'ACT16843 are noninverting 18-bit D-type latches composed of two 9-bit sections with separate control signals. For each 9-bit section, when the enable input 1C (or 2C) is low, the latches are in the storage mode. In contrast, when 1C (or 2C) is high, the latches are transparent. In this mode, data present at the 1D (or 2D) inputs is transmitted to the 1Q (or 2Q) outputs if $1\overline{OE}$ (or $2\overline{OE}$) is low. If $1\overline{OE}$ (or $2\overline{OE}$) is high, the corresponding outputs are in the high-impedance state.

Preset ($1\overline{PRE}$ and $2\overline{PRE}$) and clear ($1\overline{CLR}$ and $2\overline{CLR}$) inputs are provided to set the corresponding Q outputs asynchronously to a high or low logic level. Taking $1\overline{PRE}$ (or $2\overline{PRE}$) low sets the corresponding outputs high. If $1\overline{PRE}$ (or $2\overline{PRE}$) is high, taking $1\overline{CLR}$ (or $2\overline{CLR}$) low sets the corresponding outputs low.

The 74AC16843 and 74ACT16843 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16843 has CMOS-compatible input thresholds. The 'ACT16843 has TTL-compatible input thresholds.

The 54AC16843 and 54ACT16843 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16843 and 74ACT16843 are characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

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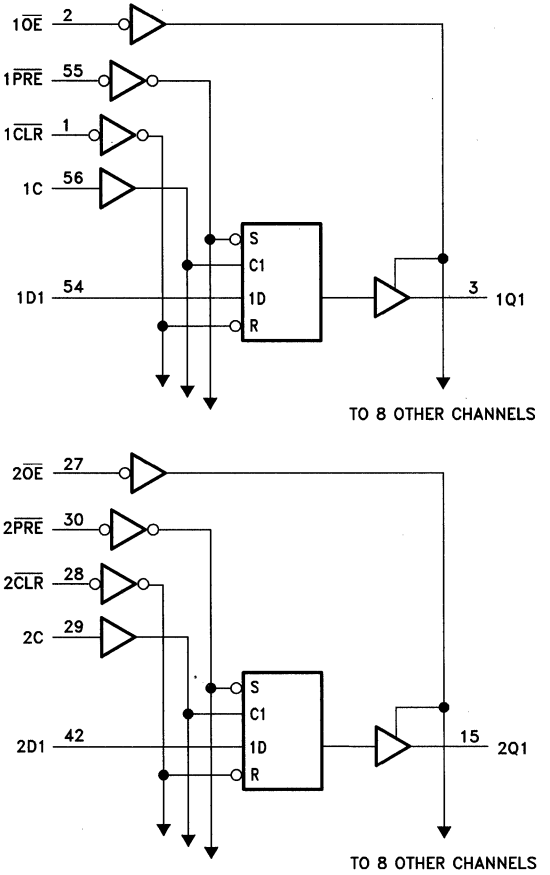
logic diagram (positive logic)

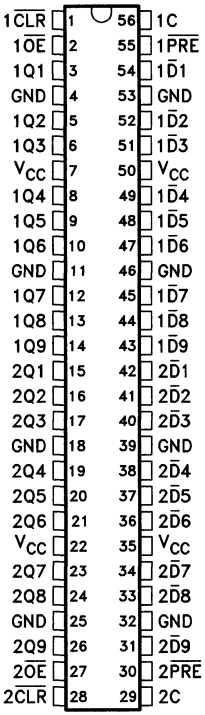


PRODUCT PREVIEW

TI0275—D3551, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

SN54AC/ACT16844 . . . WD PACKAGE
SN74AC/ACT16844 . . . DL PACKAGE
(TOP VIEW)



description

The 54AC/ACT16844 and 74AC/ACT16844 are inverting 18-bit D-type latches composed of two 9-bit sections. Separate control signals are provided for each 9-bit section.

For each 9-bit section, when the enable input 1C (or 2C) is low, the latches are placed into the storage mode. In contrast, when 1C (or 2C) is high, the latches are transparent. In this mode, the inverse of the data present at the 1$\overline{D}$ (or 2$\overline{D}$) inputs is transmitted to the 1Q (or 2Q) outputs if 1$\overline{OE}$ (or 2$\overline{OE}$) is low. If 1$\overline{OE}$ (or 2$\overline{OE}$) is high, the corresponding outputs are in the high-impedance state.

Preset (1$\overline{PRE}$ and 2$\overline{PRE}$) and clear (1$\overline{CLR}$ and 2$\overline{CLR}$) inputs are provided to set the corresponding Q outputs asynchronously to a high or low logic level. Taking 1$\overline{PRE}$ (or 2$\overline{PRE}$) low sets the corresponding outputs high. If 1$\overline{PRE}$ (or 2$\overline{PRE}$) is high, taking 1$\overline{CLR}$ (or 2$\overline{CLR}$) low sets the corresponding outputs low.

The 74AC16844 and 74ACT16844 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16844 has CMOS-compatible input thresholds. The 'ACT16844 has TTL-compatible input thresholds.

The 54AC/ACT16844 is characterized over the full military temperature range of −55°C to 125°C. The 74AC/ACT16844 is characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

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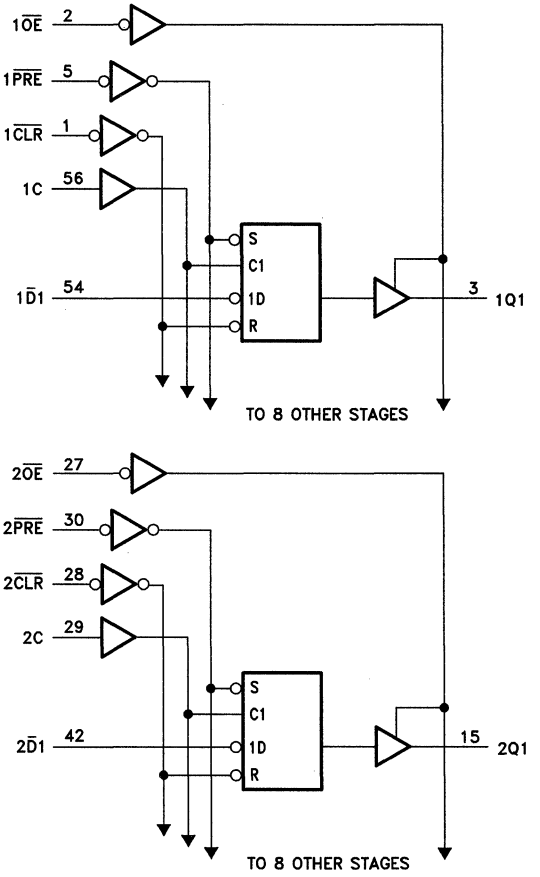
D3551, JUNE 1990—TI0275

logic diagram (positive logic)



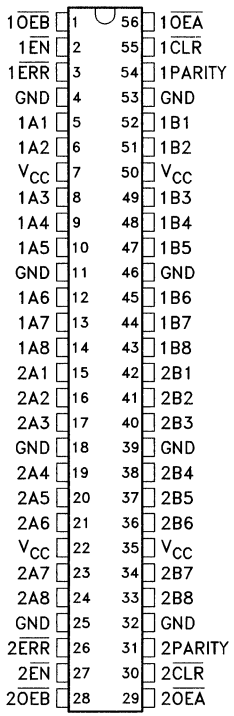
PRODUCT PREVIEW

DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

TI0276—D3552, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16853, 54ACT16853 ... WD PACKAGE
74AC16853, 74ACT16853 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16853 and 'ACT16853 contain two noninverting 8-bit to 9-bit parity bus transceivers. For either transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B input data to generate an active-low error flag if odd parity is not detected.

The error output (1$\overline{\text{ERR}}$ or 2$\overline{\text{ERR}}$) is an open-collector output. 1$\overline{\text{ERR}}$ (or 2$\overline{\text{ERR}}$) can be passed, sampled, stored, and cleared from the latch using the latch enable (1$\overline{\text{EN}}$ and 2$\overline{\text{EN}}$) and clear (1$\overline{\text{CLR}}$ and 2$\overline{\text{CLR}}$) inputs.

The 74AC16853 and 74ACT16853 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

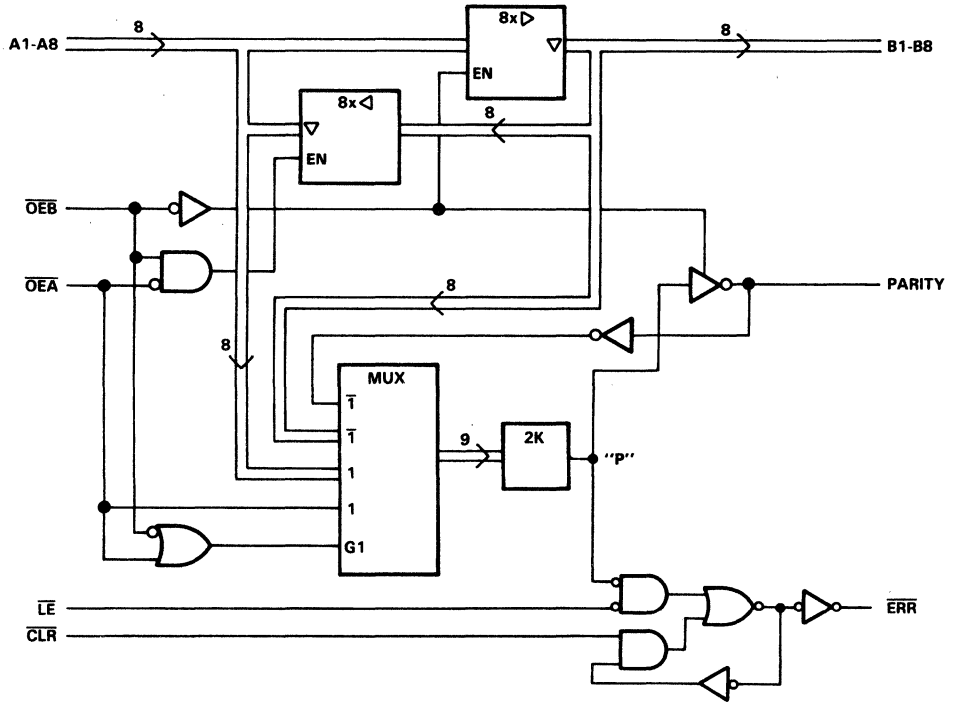
The 'AC16853 has CMOS-compatible input thresholds. The 'ACT16853 has TTL-compatible input thresholds.

The 54AC16853 and 54ACT16853 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16853 and 74ACT16853 are characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic diagram, each transceiver (positive logic)

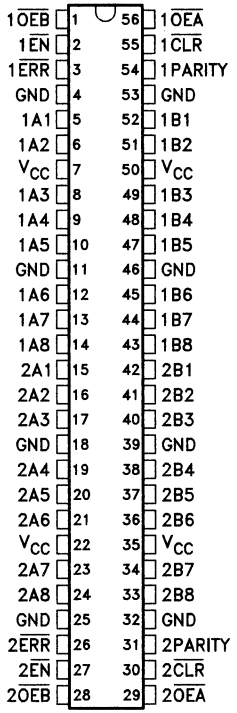


PRODUCT PREVIEW

TI0277—D3553, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16854, 54ACT16854 ... WD PACKAGE
74AC16854, 74ACT16854 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16854 and 'ACT16854 contain two inverting 8-bit to 9-bit parity bus transceivers. For either transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B input data to generate an active-low error flag if odd parity is not detected.

The error output (1$\overline{ERR}$ or 2$\overline{ERR}$) is an open-collector output. 1$\overline{ERR}$ (or 2$\overline{ERR}$) can be passed, sampled, stored, and cleared from the latch using the latch enable (1$\overline{EN}$ and 2$\overline{EN}$) and clear (1$\overline{CLR}$ and 2$\overline{CLR}$) inputs.

The 74AC16854 and 74ACT16854 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

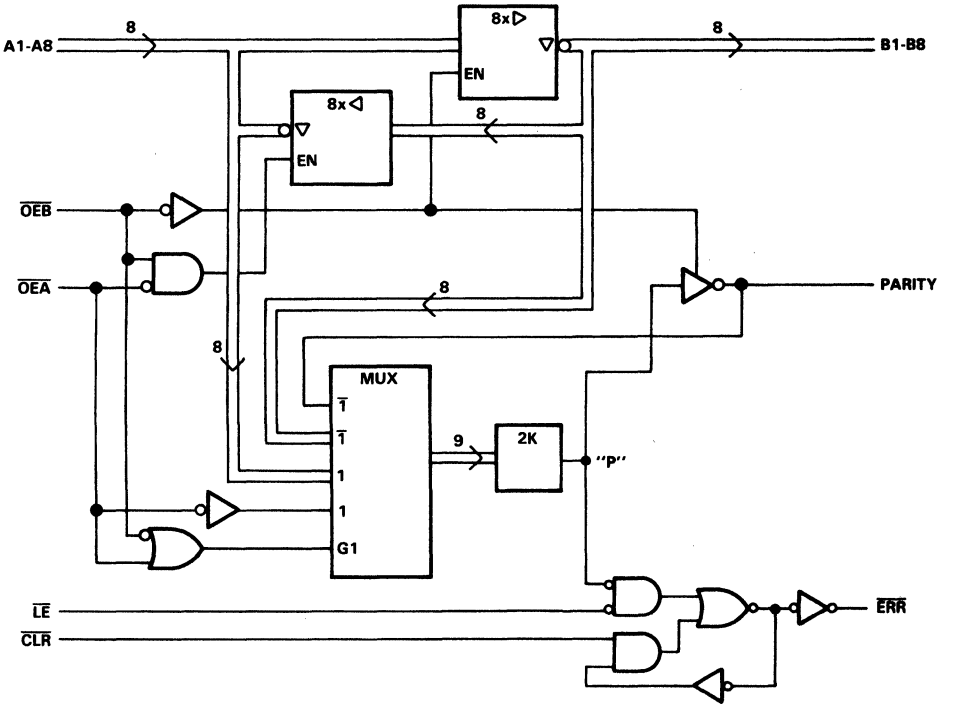
The 'AC16854 has CMOS-compatible input thresholds. The 'ACT16854 has TTL-compatible input thresholds.

The 54AC16854 and 54ACT16854 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16854 and 74ACT16854 are characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic diagram, each transceiver (positive logic)

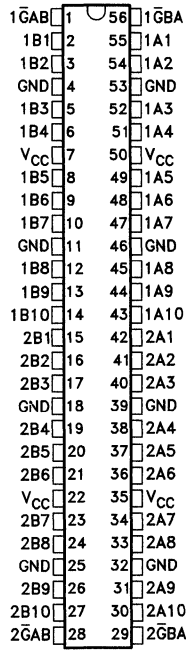


PRODUCT PREVIEW

TI0234—D3556, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16861, 54ACT16861 . . . WD PACKAGE
74AC16861, 74ACT16861 . . . DL PACKAGE
(TOP VIEW)



description

The 'AC16861 and 'ACT16861 are noninverting 20-bit bus transceivers composed of two 10-bit transceiver sections with separate control signals. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the levels present at the output-enable inputs (1$\overline{G}$AB, 2$\overline{G}$AB, 1$\overline{G}$BA, and 2$\overline{G}$BA). The control logic also allows for isolation and latching.

The 74AC16861 and 74ACT16861 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16861 has CMOS-compatible input thresholds. The 'ACT16861 has TTL-compatible input thresholds.

The 54AC16861 and 54ACT16861 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16861 and 74ACT16861 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE, EACH SECTION

INPUTS		OPERATION
$\overline{G}$AB	$\overline{G}$BA	
L	H	A to B
H	L	B to A
H	H	Isolation
L	L	Latch A and B (A = B)

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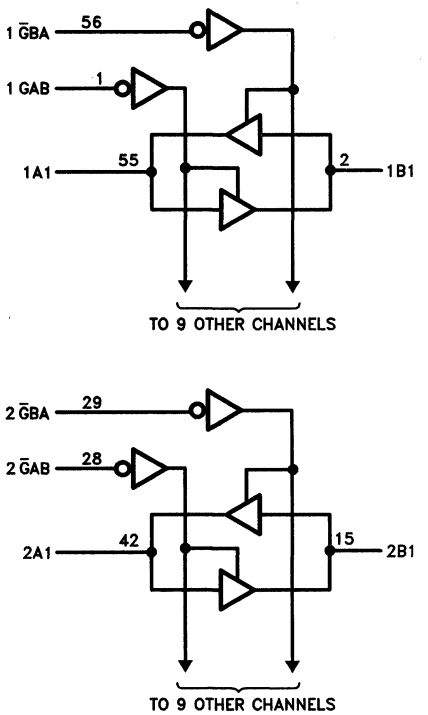
PRODUCT PREVIEW

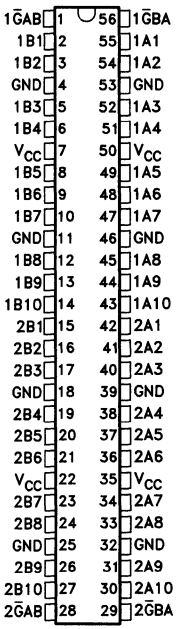
logic diagram (positive logic)



PRODUCT PREVIEW

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16862, 54ACT16862 ... WD PACKAGE
74AC16862, 74ACT16862 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16862 and 'ACT16862 are inverting 20-bit bus transceivers composed of two 10-bit transceiver sections with separate control signals. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the levels present at the output-enable inputs ($1\overline{G}AB$, $2\overline{G}AB$, $1\overline{G}BA$, and $2\overline{G}BA$). The control logic also allows for isolation and latching.

The 74AC16862 and 74ACT16862 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16862 has CMOS-compatible input thresholds. The 'ACT16862 has TTL-compatible input thresholds.

The 54AC16862 and 54ACT16862 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16862 and 74ACT16862 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE, EACH SECTION

INPUTS		OPERATION
$\overline{G}AB$	$\overline{G}BA$	
L	H	$\overline{A}$ to B
H	L	$\overline{B}$ to A
H	H	Isolation
L	L	Latch A and B ($A = \overline{B}$)

PRODUCT PREVIEW

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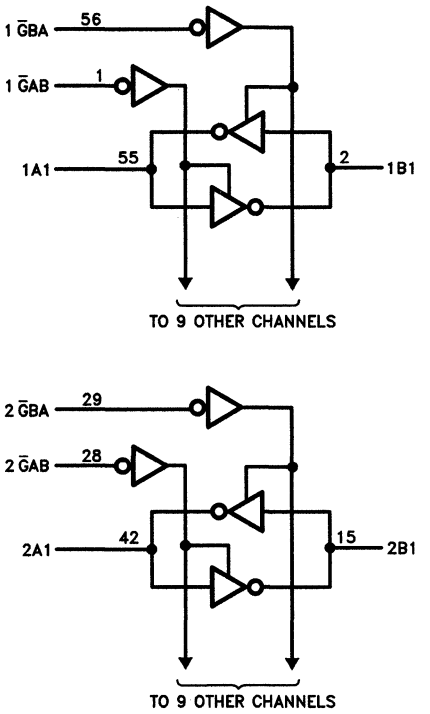
logic diagram (positive logic)

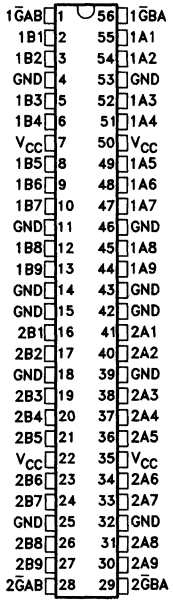


PRODUCT PREVIEW

TI0236—D3558, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16863, 54ACT16863 ... WD PACKAGE
74AC16863, 74ACT16863 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16863 and 'ACT16863 are noninverting 18-bit bus transceivers composed of two 9-bit transceiver sections with separate control signals. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the levels present at the output-enable inputs ($1\overline{G}AB$, $2\overline{G}AB$, $1\overline{G}BA$, and $2\overline{G}BA$). The control logic also allows for isolation and latching.

The 74AC16863 and 74ACT16863 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16863 has CMOS-compatible input thresholds. The 'ACT16863 has TTL-compatible input thresholds.

The 54AC16863 and 54ACT16863 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16863 and 74ACT16863 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE, EACH SECTION

INPUTS		OPERATION
$\overline{G}AB$	$\overline{G}BA$	
L	H	A to B
H	L	B to A
H	H	Isolation
L	L	Latch A and B (A = B)

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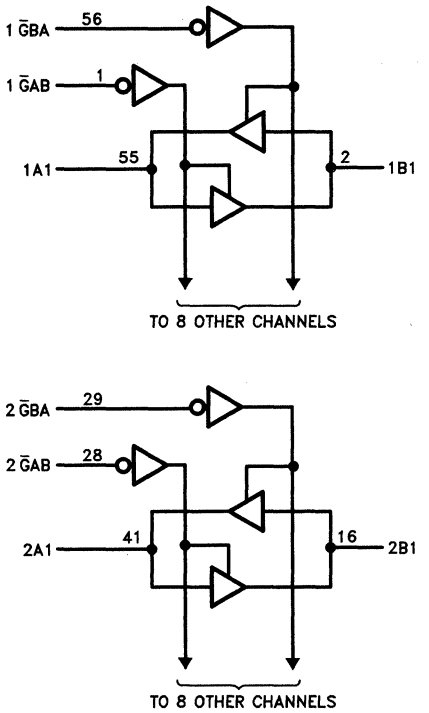
PRODUCT PREVIEW

logic diagram (positive logic)

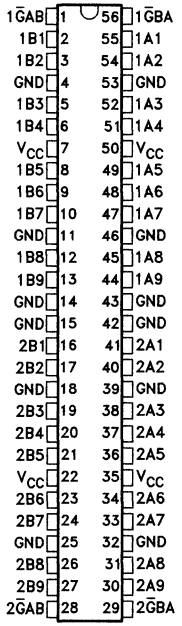


PRODUCT PREVIEW

TI0237—D3559, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16864, 54ACT16864 ... WD PACKAGE
74AC16864, 74ACT16864 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16864 and 'ACT16864 are inverting 18-bit bus transceivers composed of two 9-bit transceiver sections with separate control signals. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the levels present at the output-enable inputs ($1\overline{G}AB$, $2\overline{G}AB$, $1\overline{G}BA$, and $2\overline{G}BA$). The control logic also allows for isolation and latching.

The 74AC16864 and 74ACT16864 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16864 has CMOS-compatible input thresholds. The 'ACT16864 has TTL-compatible input thresholds.

The 54AC16864 and 54ACT16864 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16864 and 74ACT16864 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE, EACH SECTION

INPUTS		OPERATION
$\overline{G}AB$	$\overline{G}BA$	
L	H	$\overline{A}$ to B
H	L	$\overline{B}$ to A
H	H	Isolation
L	L	Latch A and B ($A = \overline{B}$)

PRODUCT PREVIEW

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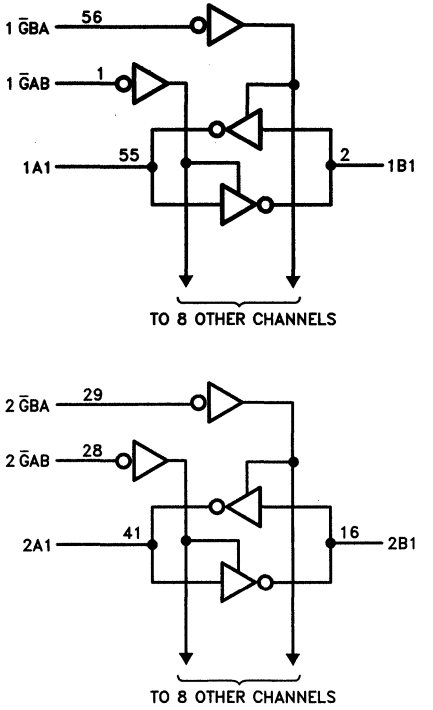
logic diagram (positive logic)



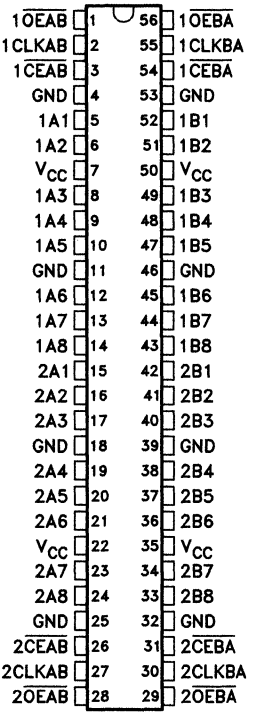
PRODUCT PREVIEW

16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0238—D3560, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16952, 54ACT16952 ... WD PACKAGE
74AC16952, 74ACT16952 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16952 and 'ACT16952 are noninverting 16-bit registered bus transceivers composed of two 8-bit transceiver sections with separate control signals.

Data flow in the A-to-B mode is controlled by output-enable (1$\overline{OEAB}$ and 2$\overline{OEAB}$), clock-enable (1$\overline{CEAB}$ and 2$\overline{CEAB}$), and clock (1CLKAB and 2CLKAB) inputs. When 1$\overline{CEAB}$ (or 2$\overline{CEAB}$) is high, data storage is inhibited and the registers retain their previous states. When 1$\overline{CEAB}$ (or 2$\overline{CEAB}$) is low, the data present at the corresponding A inputs is stored in the device on a low-to-high transition of 1CLKAB (or 2CLKAB). If 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is also low, this stored data appears on the corresponding B outputs; if 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is high, the corresponding B outputs are in the high-impedance state. 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) does not affect the operation of the internal registers. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Data flow from B to A is controlled by 1$\overline{OEBA}$ and 2$\overline{OEBA}$, 1$\overline{CEBA}$ and 2$\overline{CEBA}$, and 1CLKBA and 2CLKBA in a manner analogous to that described above for A-to-B data flow.

PRODUCT PREVIEW

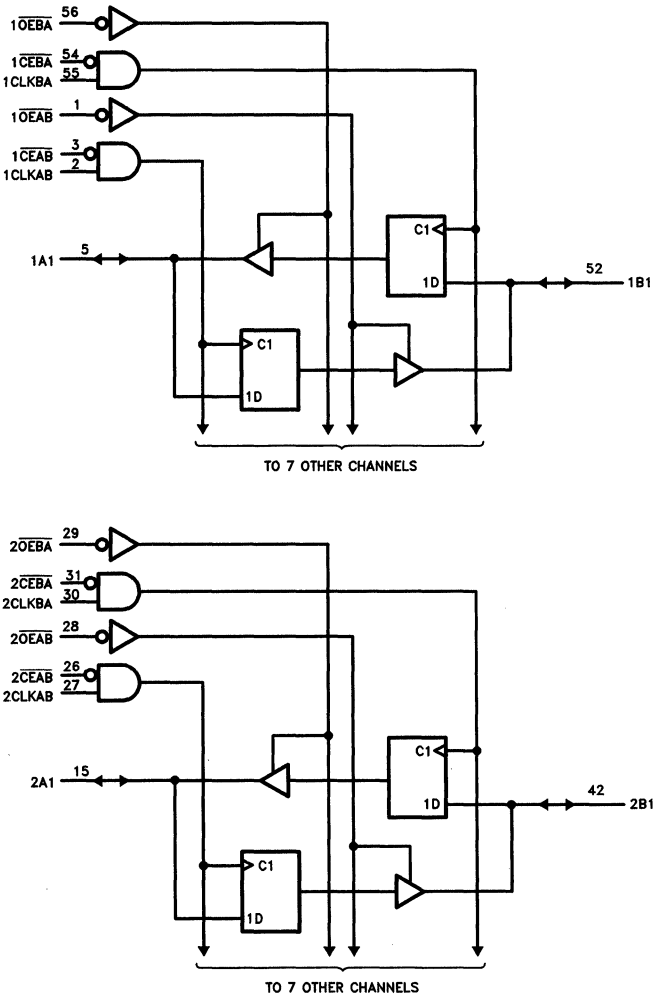
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

The 74AC16952 and 74ACT16952 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16952 has CMOS-compatible input thresholds. The 'ACT16952 has TTL-compatible input thresholds.

The 54AC16952 and 54ACT16952 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16952 and 74ACT16952 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)



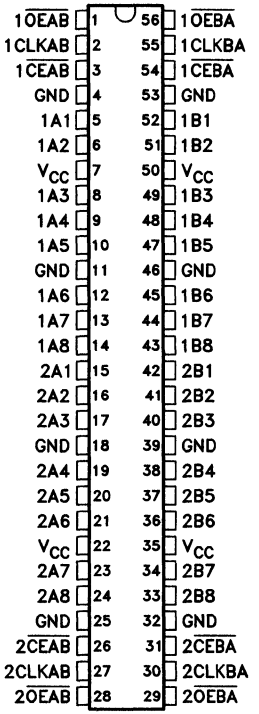
PRODUCT PREVIEW

16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0239—D3561, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16953, 54ACT16953 . . . WD PACKAGE
74AC16953, 74ACT16953 . . . DL PACKAGE
(TOP VIEW)



description

The 'AC16953 and 'ACT16953 are inverting 16-bit registered bus transceivers composed of two 8-bit transceiver sections with separate control signals.

Data flow in the A-to-B mode is controlled by output-enable (1$\overline{OEAB}$ and 2$\overline{OEAB}$), clock-enable (1$\overline{CEAB}$ and 2$\overline{CEAB}$), and clock (1CLKAB and 2CLKAB) inputs. When 1$\overline{CEAB}$ (or 2$\overline{CEAB}$) is high, data storage is inhibited and the registers retain their previous states. When 1$\overline{CEAB}$ (or 2$\overline{CEAB}$) is low, the inverse of the data present at the corresponding A inputs is stored in the device on a low-to-high transition of 1CLKAB (or 2CLKAB). If 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is also low, this stored data appears on the corresponding B outputs; if 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is high, the corresponding B outputs are in the high-impedance state. 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) does not affect the operation of the internal registers. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Data flow from B to A is controlled by 1$\overline{OEBA}$ and 2$\overline{OEBA}$, 1$\overline{CEBA}$ and 2$\overline{CEBA}$, and 1CLKBA and 2CLKBA in a manner analogous to that described above for A-to-B data flow.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

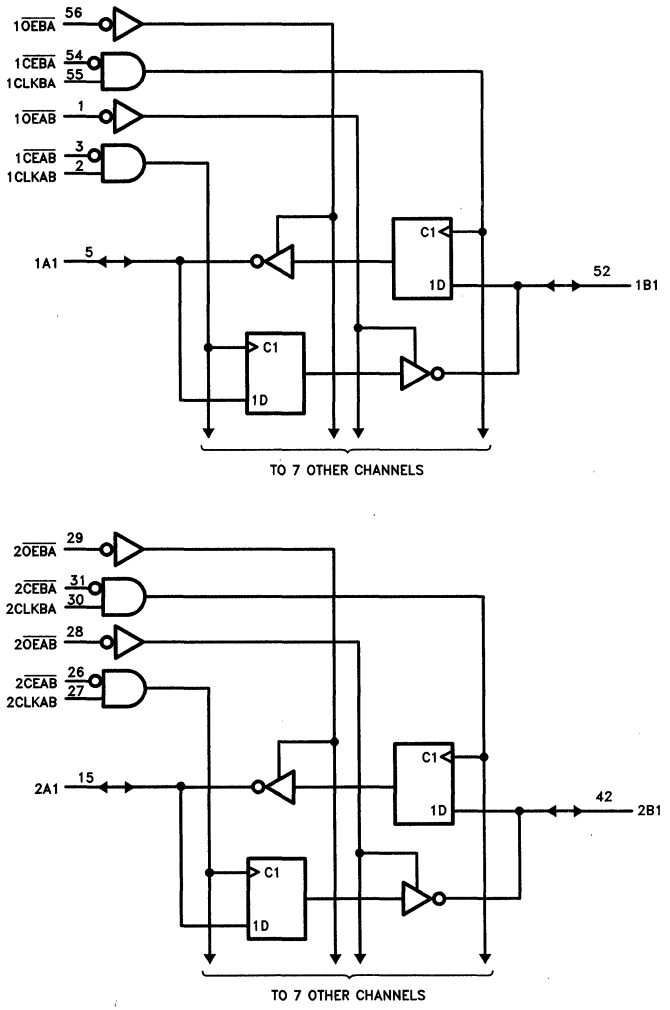
PRODUCT PREVIEW

The 74AC16953 and 74ACT16953 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16953 has CMOS-compatible input thresholds. The 'ACT16953 has TTL-compatible input thresholds.

The 54AC16953 and 54ACT16953 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16953 and 74ACT16953 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)



PRODUCT PREVIEW

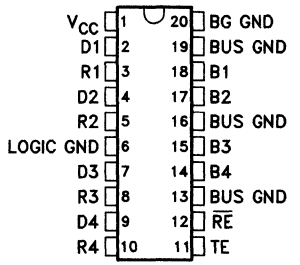
4

BTL Transceiver Products

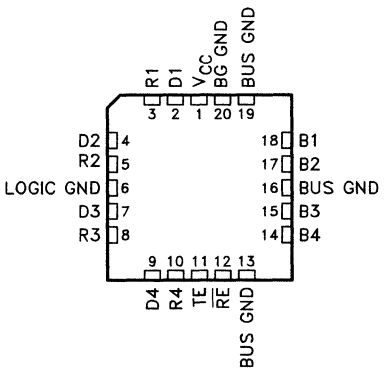
TI0267—D3077, JANUARY 1988—REVISED SEPTEMBER 1989

- **High Speed Quad Transceiver**
- **Fully Compatible with IEEE Standard 896.1-1987 Futurebus Requirements**
- **Drives Load Impedances as Low as 10 Ω**
- **High-Speed Advanced Low-Power Schottky Circuits**
- **Low Power Dissipation . . . 81 mW Max per Channel**
- **High-Impedance P-N-P Inputs**
- **BTL™ Logic Level 1-V Bus Swing Reduces Power Consumption**
- **Low Bus-Port Capacitance**
- **Power-Up/Power-Down Protection (Glitch-Free)**
- **Open-Collector Driver Outputs Allows Wired-OR Connections**
- **Multiple Bus Channel Ground Returns to Reduce Channel Noise Interference**
- **Designed to Be a Faster, Lower Power Functional Equivalent of National DS3893**

N PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The SN75ALS053 is a four-channel, monolithic, high-speed, advanced low-power Schottky device designed for two-way data communication in a densely populated backplane. The SN75ALS053 has independent driver input (Dn) and receiver output (Rn) pins and separate driver and receiver disables. This transceiver is designed for use in high-speed bus systems and is similar to the SN75ALS057 transceiver except that the trapezoidal feature has been eliminated to speed up the propagation delays.

These transceivers feature open-collector driver outputs, each with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pullup on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs are capable of driving an equivalent dc load of as low as 10 Ω.

The receivers have a precision threshold set by an internal bandgap reference to give accurate input thresholds over V_{CC} and temperature variations.

These transceivers are compatible with Backplane Transceiver Logic (BTL™) technology at significantly reduced power dissipation per channel.

The SN75ALS053 is characterized for operation from 0°C to 70°C.

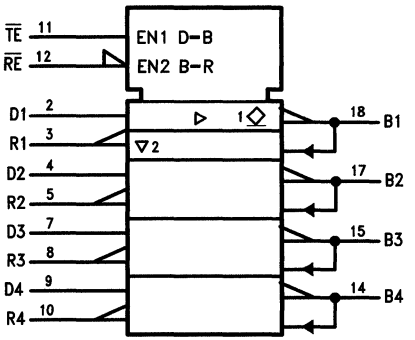
BTL is a trademark of National Semiconductor Corporation.

FUNCTION TABLE
TRANSMIT/RECEIVE

CONTROLS		CHANNELS	
TE	$\overline{RE}$	D → B	B → R
L	L	D	R
L	H	D	D
H	L	T	R
H	H	T	D

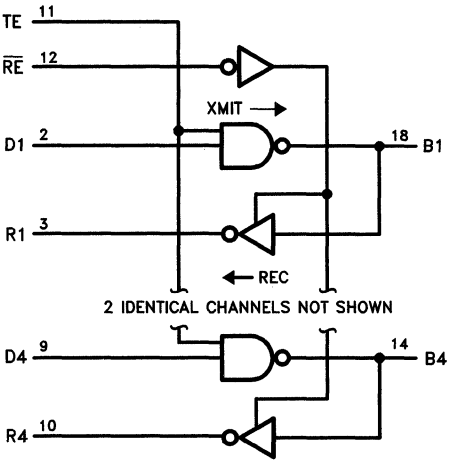
H = high level, L = low level, R = receive, T = transmit, D = disable
Direction of data transmission is from Dn to Bn, direction of data reception is from Bn to Rn.

logic symbol†

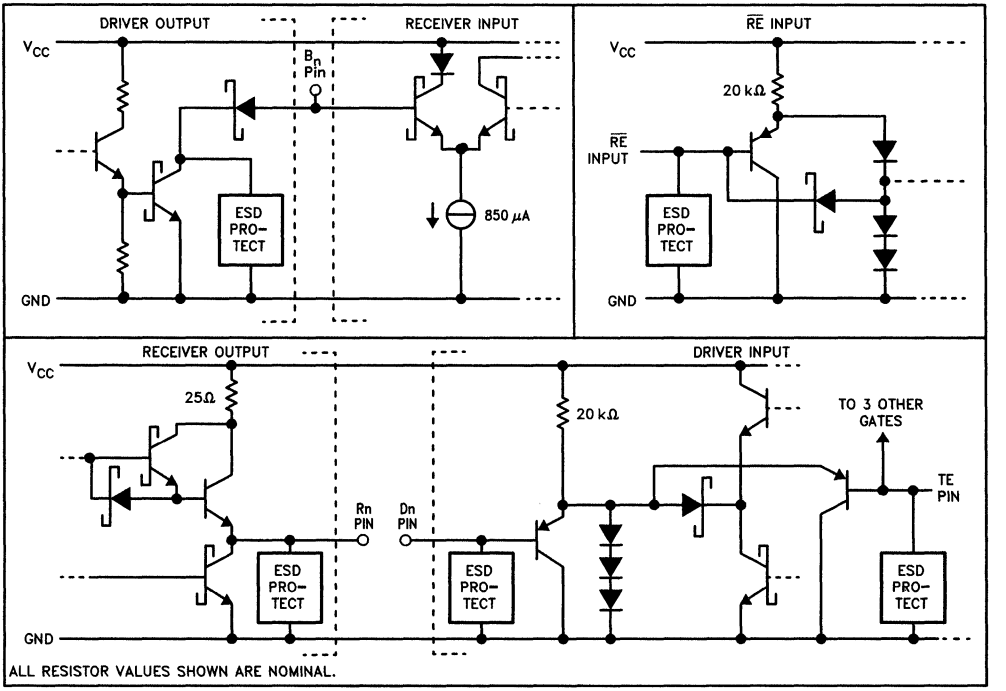


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	6 V
Control input voltage	5.5 V
Driver input voltage	5.5 V
Driver output voltage	2.5 V
Receiver input voltage	2.5 V
Receiver output voltage	5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6mm (1/16 in.) from case for 10 seconds: N package	260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
FN	1400 mW	11.2 mW/°C	896 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level driver and control input voltage	2			V
V_{IL}	Low-level driver and control input voltage			0.8	V
	Bus termination voltage	1.9		2.1	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage at Dn, DE, or $\overline{RE}$		$I_I = -18$ mA			−1.5	V
V_T	Receiver input threshold at Bn			1.426		1.674	V
V_{OH}	High-level output voltage at Rn		Bn at 1.2 V, $\overline{RE}$ at 0.8 V, $I_{OH} = -1$ mA	2.5			V
V_{OL}	Low-level output voltage	Rn	Bn at 2 V, $\overline{RE}$ at 0.8 V, $I_{OL} = 20$ mA			0.5	V
		Bn	Dn at 2.4 V, TE at 2.4 V, $V_L = 2$ V, $R_L = 10\ \Omega$, See Figure 1	0.75		1.2	
I_{IH}	High-level input current	Dn, TE or $\overline{RE}$	$V_I = V_{CC}$			40	μA
		Bn	$V_I = 2$ V, $V_{CC} = 0$ or 5.25 V, Dn at 0.8 V, TE at 0.8 V,			100	
I_{IL}	Low-level input current at Dn, TE or $\overline{RE}$		$V_I = 0.4$ V			−400	μA
I_{OS}	Short-circuit output current at Rn		Rn at 0 V, Bn at 1.2 V, $\overline{RE}$ at 0.8 V	−70		−200	mA
I_{CC}	Supply curent					65	mA
$C_{o(B)}$	Driver output capacitance		$V_{CC} = 5$ V, $T_A = 25°C$		6.5		pF

switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Dn	Bn	TE at 3 V, V_L = 2 V, See Figure 2	2	7	ns
t_{PHL}	Propagation delay time high-to-low-level output				2	7	
t_{PLH}	Propagation delay time, low-to-high-level output	Dn	Bn	Dn at 3 V, V_L = 2 V, See Figure 2	2	7	ns
t_{PHL}	Propagation delay time high-to-low-level output				2	7	
t_{TLH}	Transition time, low-to-high-level output	Dn	Bn	TE at 3 V, V_L = 2 V, See Figure 2	0.5	5	ns
t_{THL}	Transition time, high-to-low-level output				0.5	5	
	Skew between driver channels†	Dn	Bn	TE at 3 V, V_L = 2 V		1	ns

receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Bn	Rn	$\overline{RE}$ at 0.3 V, TE at 0.3 V, See Figure 3	2	8	ns
t_{PHL}	Propagation delay time high-to-low-level output				2	8	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	Rn	Bn at 2 V, TE at 0.3 V, V_L = 5 V, C_L = 5 pF, R_{L1} = 500 Ω, See Figure 4		6	ns
t_{PZL}	Output enable time to low level	$\overline{RE}$	Rn	Bn at 2 V, TE at 0.3 V, V_L = 5 V, C_L = 5 pF, R_{L1} = 500 Ω, See Figure 4		12	ns
t_{PHZ}	Output disable time from high level	$\overline{RE}$	Rn	Bn at 1 V, TE at 0.3 V, V_L = 0, C_L = 5 pF, R_{L1} = 500 Ω, See Figure 4		6	ns
t_{PZH}	Output enable time to high level	$\overline{RE}$	Rn	Bn at 1 V, TE at 0.3 V, V_L = 0, C_L = 5 pF, R_{L1} = 500 Ω, See Figure 4		12	ns
	Skew between receiver channels†	Bn	Rn	$\overline{RE}$ at 0.3 V, TE at 0.3 V		1	ns

† Skew is the difference between the propagation delay time (t_{PLH} or t_{PHL}) of one receiver channel and that same propagation delay time of any other receiver channel. It applies for both t_{PLH} and t_{PHL}.

PARAMETER MEASUREMENT INFORMATION

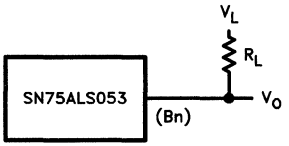
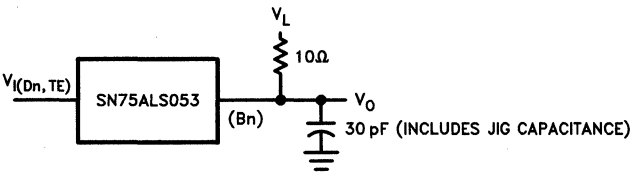
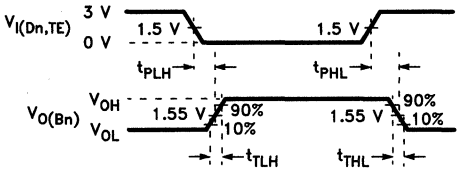


FIGURE 1. DRIVER LOW-LEVEL-OUTPUT-VOLTAGE TEST CIRCUIT



TEST CIRCUIT

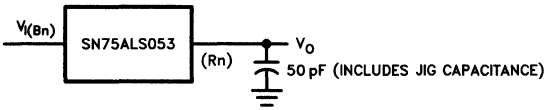


VOLTAGE WAVEFORMS

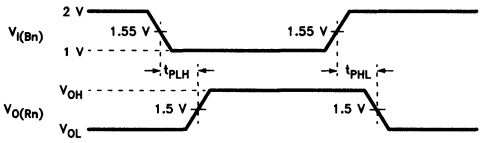
NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 2. DRIVER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



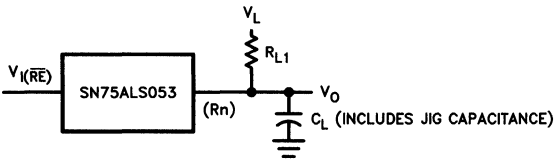
TEST CIRCUIT



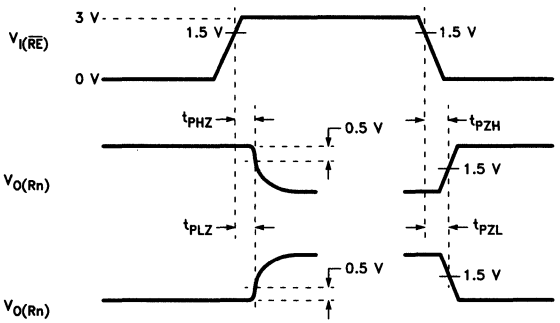
VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 10$ ns from 10% to 90%

FIGURE 3. RECEIVER PROPAGATION DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

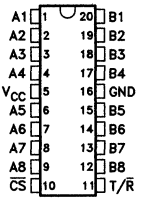
NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 4. PROPAGATION DELAY FROM $\overline{RE}$ TO Rn

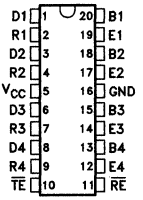
SDAS171—TI0265—D3275, APRIL 1989

- **Suitable for IEEE Standard 896 Applications†**
- **SN55ALS056 is an Octal Transceiver**
- **SN55ALS057 is a Quad Transceiver**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low Power Dissipation . . . 60 mW/Channel Max**
- **High-Impedance P-N-P Inputs**
- **BTL™ Logic Level 1-V Bus Swing Reduces Power Consumption**
- **Trapezoidal Bus Output Waveform Reduces Noise Coupling to Adjacent Lines**
- **Power-Up/Down Protection (Glitch-Free)**
- **Open-Collector Driver Outputs Allow Wired-OR Connections**

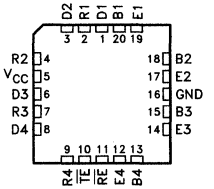
SN55ALS056 . . . J OR W PACKAGE
(TOP VIEW)



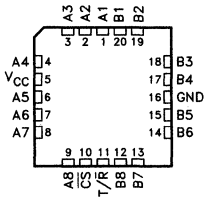
SN55ALS057 . . . J OR W PACKAGE
(TOP VIEW)



SN55ALS056 . . . FK PACKAGE
(TOP VIEW)



SN55ALS057 . . . FK PACKAGE
(TOP VIEW)



description

The SN55ALS056 is an 8-channel, monolithic, high-speed, Advanced Low-Power Schottky device designed for 2-way data communication in a densely populated backplane. The SN55ALS057 is a 4-channel version with independent driver input (Dn) and receiver output (Rn) pins and a separate driver disable for each driver (En). Both are compatible with Backplane Transceiver Logic (BTL™) technology at significantly reduced power dissipation per channel.

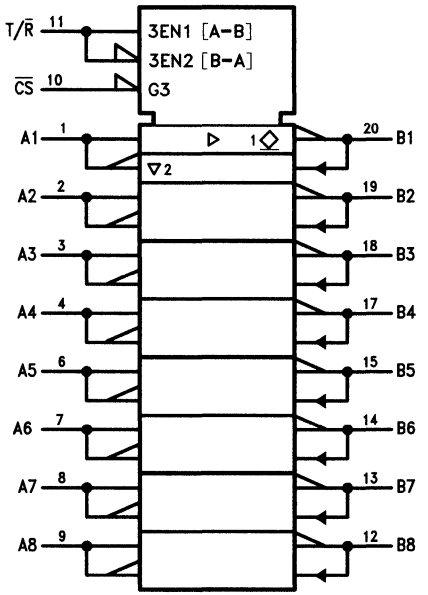
These transceivers feature open-collector driver outputs with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pull-up termination on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs generate trapezoidal waveforms that reduce crosstalk between channels. The drivers are capable of driving an equivalent dc load as low as 18.5 Ω. The receivers have internal low-pass filters to further improve noise immunity.

The SN55ALS056 and SN55ALS057 are characterized for operation from −55°C to 125°C.

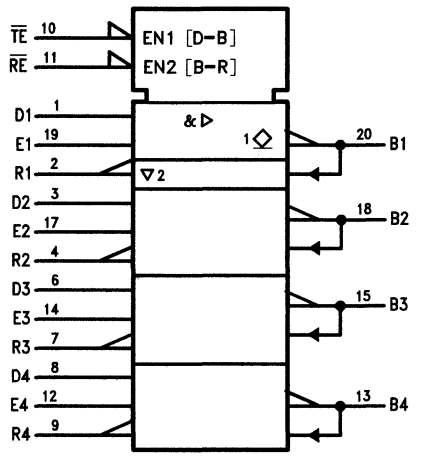
† The transceivers are suitable for IEEE Standard 896 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range.
BTL is a trademark of National Semiconductor Corporation.

logic symbols†

SN55ALS056

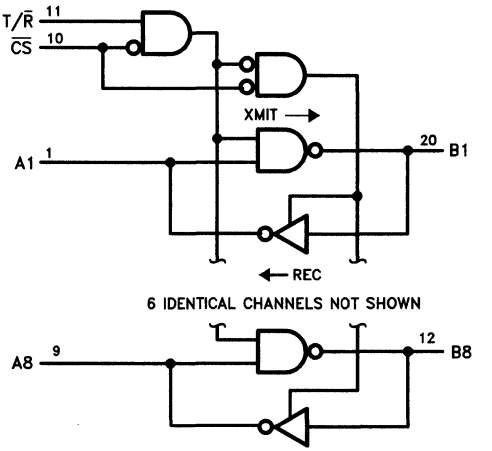


SN55ALS057

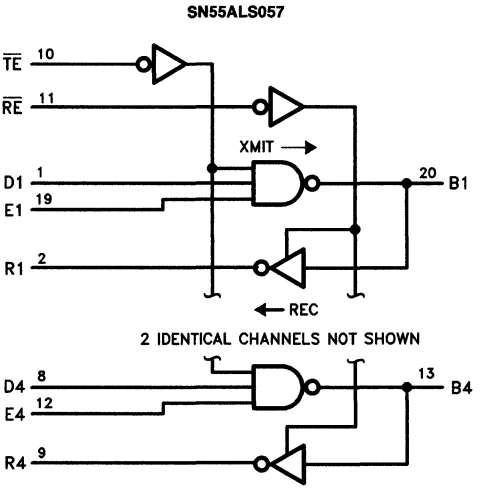


logic diagrams (positive logic)

SN55ALS056



SN55ALS057



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

D3275, APRIL 1989—TI0265—SDAS171

SN55ALS056
FUNCTION TABLE
TRANSMIT/RECEIVE

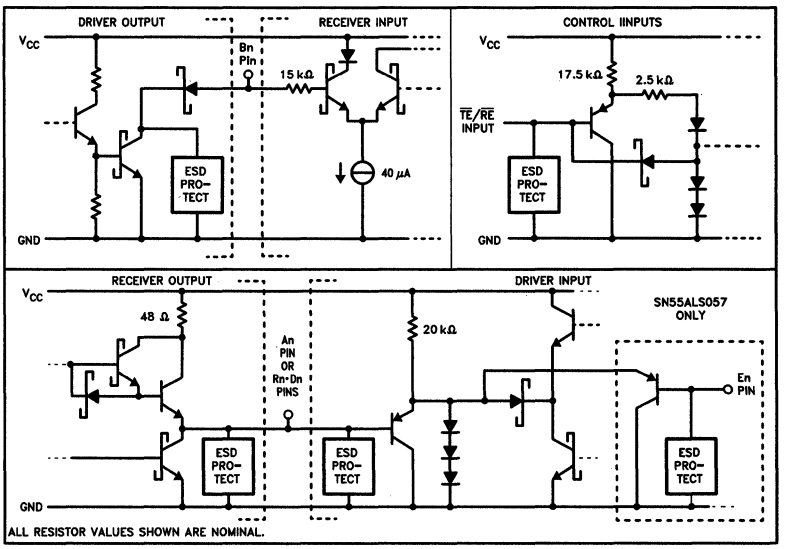
CONTROLS		CHANNELS
$\overline{CS}$	T/$\overline{R}$	A ⟷ B
L	H	T (A → B)
L	L	R (B → A)
H	X	D

SN55ALS057
FUNCTION TABLE
TRANSMIT/RECEIVE

CONTROLS			CHANNELS	
$\overline{TE}$	$\overline{RE}$	En	D → B	B → R
L	L	L	D	R
L	L	H	T	R
L	H	L	D	D
L	H	H	T	D
H	L	X	D	R
H	H	X	D	D

H = high level, L = low-level, R = receive, T = transmit, D = disable, X = irrelevant
Direction of data transmission is from An to Bn for the SN55ALS056 and from Dn to Bn for the SN55ALS057.
Direction of data reception is from Bn to An for the SN55ALS056 and from Bn to Rn for the SN55ALS057.
Data transfer is inverting in both directions.

schematics of inputs and outputs



† Additional ESD protection is on the SN55ALS057, which has separate receiver output and driver input pins.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 6 V
Control input voltage ..... 5.5 V
Driver input voltage ..... 5.5 V
Driver output voltage ..... 2.5 V
Receiver input voltage ..... 2.5 V
Receiver output voltage ..... 5.5 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 1375 mW
Operating free-air temperature range ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm ($1/16$ inch) from case for 60 seconds ..... 300°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate to 275 mW at 125°C at the rate of 11.0 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level driver and control input voltage	2			V
V_{IL}	Low-level driver and control input voltage			0.8	V
	Bus termination voltage	1.9		2.1	V
T_A	Operating free-air temperature	−55		125	°C

SN55ALS056 electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at An, T/$\overline{R}$, or $\overline{CS}$		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_T	Receiver input threshold at Bn		V_{CC} = 5 V,	T_A = 25°C	1.45		1.65	V
			V_{CC} = 5 V,	T_A = −55°C to 125°C	1.4		1.7	
V_{OH}	High-level output voltage at An		V_{CC} = 4.5 V, $\overline{CS}$ at 0.8 V, I_{OH} = −400 μA	Bn at 1.2 V, T/$\overline{R}$ at 0.8 V,	2.4			V
V_{OL}	Low-level output voltage	An	V_{CC} = 4.5 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V,	Bn at 2V, T/$\overline{R}$ at 0.8 V, I_{OL} = 16 mA			0.5	V
		Bn	V_{CC} = 4.5 V, $\overline{CS}$ at 0.8 V, See Figure 1	An at 2 V, T/$\overline{R}$ at 2 V,	0.75		1.2	
I_{IH}	High-level input current	An, T/$\overline{R}$, or $\overline{CS}$	V_I = V_{CC} = 5.5 V				40	μA
		Bn	V_{CC} = 5.5 V, An at 0.8 V,	V_I = 2 V, T/$\overline{R}$ at 0.8 V			100	
I_{IL}	Low-level input current at An, T/$\overline{R}$, or $\overline{CS}$		V_{CC} = 5.5 V,	V_I = 0.4 V			−400	μA
I_{OS}	Short-circuit output current at An		V_{CC} = 5.5 V, Bn at 1.2 V, T/$\overline{R}$ at 0.8 V	An at 0 V, $\overline{CS}$ at 0.8 V,	−35		−125	μA
I_{CC}	Supply current		V_{CC} = 5.5 V				85	mA
$C_{o(B)}$	Driver output capacitance					4.5		pF

SN55ALS057 electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at Dn, En, $\overline{TE}$, or $\overline{RE}$		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_T	Receiver input threshold at Bn		V_{CC} = 5 V,	T_A = 25°C	1.45		1.65	V
			V_{CC} = 5 V,	T_A = −55°C to 125°C	1.4		1.7	
V_{OH}	High-level output voltage at Rn		V_{CC} = 4.5 V, $\overline{RE}$ at 0.8 V,	Bn at 1.2 V, I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	Rn	V_{CC} = 4.5 V, $\overline{RE}$ at 0.8 V,	Bn at 2 V, I_{OL} = 16 mA			0.5	V
		Bn	V_{CC} = 4.5 V, En at 2 V, See Figure 1	Dn at 2 V, $\overline{TE}$ at 0.8 V	0.75		1.2	
I_{IH}	High-level input current	Dn, En, $\overline{TE}$, or $\overline{RE}$	V_I = V_{CC} = 5.5 V				40	μA
		Bn	V_{CC} = 5.5 V, Dn at 0.8 V, $\overline{TE}$ at 0.8 V	V_I = 2 V, En at 0.8 V,			100	
I_{IL}	Low-level input current at Dn, En, $\overline{TE}$, or $\overline{RE}$		V_{CC} = 5.5 V,	V_I = 0.4 V			−400	μA
I_{OS}	Short-circuit output current at Rn		V_{CC} = 5.5 V, Bn at 1.2 V,	Rn at 0 V, $\overline{RE}$ at 0.8 V	−35		−125	μA
I_{CC}	Supply current		V_{CC} = 5.5 V				85	mA
$C_{o(B)}$	Driver output capacitance					4.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Bn	An	$\overline{CS}$ at 0.8 V, V_L = 5 V, See Figure 4	T/$\overline{R}$ at 0.8 V, S1 closed,	25°C			20	ns
						Full range			22	
t_{PHL}	Propagation delay time, high- to low-level output					25°C			18	
						Full range			20	
t_{PLZ}	Output disable time from low level	$\overline{CS}$	An	Bn at 2 V, V_L = 5 V, See Figure 5	T/$\overline{R}$ at 0.8 V, S1 closed,	25°C			20	ns
						Full range			22	
t_{PZL}	Output enable time to low level					25°C			13	
						Full range			14	
t_{PHZ}	Output disable time from high level	$\overline{CS}$	An	Bn at 0.8 V, V_L = 0, S1 closed,	T/$\overline{R}$ at 0.8 V, See Figure 5	25°C			12	ns
						Full range			13	
t_{PZH}	Output enable time to high-level			Bn at 0.8 V, S1 open,	T/$\overline{R}$ at 0.8 V, See Figure 5	25°C			14	
						Full range			22	
t_{PLZ}	Output disable time from low level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8V, V_L = 5 V, See Figure 5	VC at 2 V, S1 closed,	25°C			17	ns
						Full range			20	
t_{PZL}	Output enable time to low level					25°C			25	
						Full range			40	
t_{PHZ}	Output disable time from high level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, S1 closed,	V_L = 0 See Figure 5	25°			12	ns
						Full range			13	
t_{PZH}	Output enable time to high level			$\overline{CS}$ at 0.8 V, See Figure 5	S1 open,	25°C			15	
						Full range			22	
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	An or Rn	V_L = 5 V, See Figure 6	S1 closed,	25°C	4			ns
						Full range	2			

driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		T_A†	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	An	Bn	$\overline{CS}$ at 0.8 V, V_L = 2 V,	T/$\overline{R}$ at 2 V, See Figure 2	25°C			10	ns
						Full range			40	
t_{PHL}	Propagation delay time, high- to low-level output					25°C			12	
						Full range			15	
t_{PLH}	Propagation delay time, low- to high-level output	$\overline{CS}$	Bn	An and T/$\overline{R}$ at 2 V, See Figure 2	V_L = 2 V,	25°C			18	ns
						Full range			30	
t_{PHL}	Propagation delay time, high- to low-level output					25°C			20	
						Full range			22	
t_{PLH}	Propagation delay time, low- to high-level output	T/$\overline{R}$	Bn	$\overline{CS}$ at 0.8 V, See Figure 3	V_L = 2 V,	25°C			18	ns
						Full range			37	
t_{PHL}	Propagation delay time, high- to low-level output					25°C			18	
						Full range			21	
t_{TLH}	Transition time, low- to high-level output	An	Bn	$\overline{CS}$ at 0.8 V, V_L = 2 V,	T/$\overline{R}$ at 2 V, See Figure 2	25°C	1	3	8	ns
						Full range	1		33	
t_{THL}	Transition time, high- to low-level output					25°C	1	3	10	
						Full range	1		13	

† Full range is −55°C to 125°C.
‡ Typical values are at V_{CC} = 5 V.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Bn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 2 V, V_L = 5 V, S1 closed, See Figure 4	25°C		20	ns
					Full range		22	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		18	
					Full range		20	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	Rn	Bn at 2 V, $\overline{TE}$ at 2 V, V_L = 5 V, S1 closed, See Figure 5	25°C		15	ns
					Full range		17	
t_{PZL}	Output enable time to low level				25°C		13	
					Full range		14	
t_{PHZ}	Output disable time from high level	$\overline{RE}$	Rn	Bn at 0.8 V, $\overline{TE}$ at 2 V, V_L = 0, S1 closed, See Figure 5	25°C		12	ns
					Full range		13	
t_{PZH}	Output enable time to high-level			Bn at 0.8 V, $\overline{TE}$ at 2 V, S1 closed, See Figure 5	25°C		14	
					Full range		15	
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	Rn	V_L = 5 V, S1 closed, See Figure 6	25°C	4		ns
					Full range	2		

driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Dn or En	Bn	$\overline{TE}$ at 0.8 V, $\overline{RE}$ at 2 V, V_L = 2 V, See Figure 2	25°C			10	ns
					Full range			27	
t_{PHL}	Propagation delay time, high- to low-level output				25°C			12	
					Full range			15	
t_{PLH}	Propagation delay time, low- to high-level output	TE	Bn	Dn, En, $\overline{RE}$ at 2 V, V_L = 2 V, See Figure 2	25°C			10	ns
					Full range			27	
t_{PHL}	Propagation delay time, high- to low-level output				25°C			17	
					Full range			19	
t_{TLH}	Transition time, low- to high-level output	Dn or En	Bn	$\overline{RE}$ at 2 V, V_L = 2 V, See Figure 2	25°C	1	3	8	ns
					Full range	1		33	
t_{THL}	Transition time, high- to low-level output				25°C	1	3	10	
					Full range	1		13	

‡ Typical values are at V_{CC} = 5 V.

driver plus receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Dn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 0.8 V, V_L = 2 V, See Figure 7 (Both loads are used)	25°C		25	ns
					Full range		35	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		25	
					Full range		35	

‡ Full range is −55°C to 125°C.

PARAMETER MEASUREMENT INFORMATION

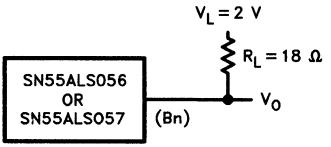
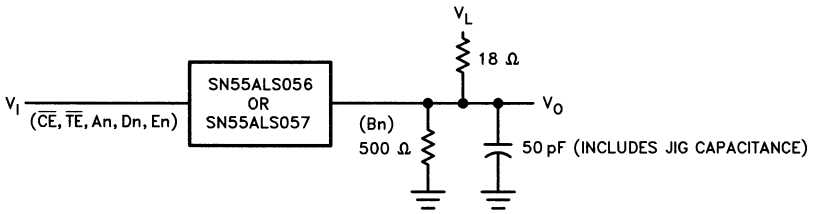
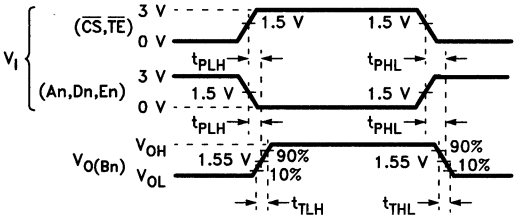


FIGURE 1. TEST CIRCUIT FOR DRIVER LOW-LEVEL OUTPUT VOLTAGE



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%.

FIGURE 2. DRIVER PROPAGATION DELAY TIMES

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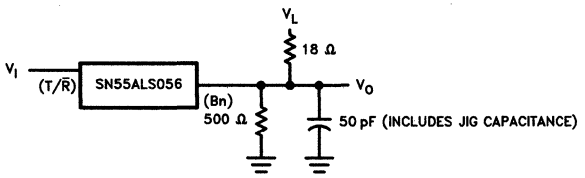
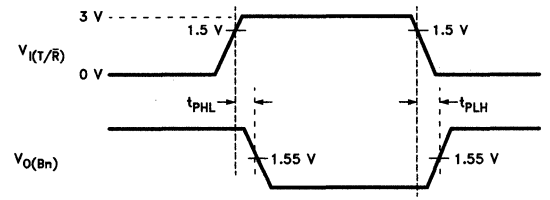
PARAMETER MEASUREMENT INFORMATION



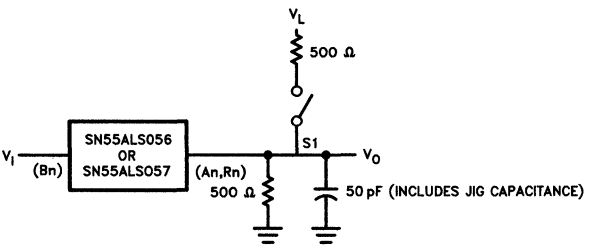
TEST CIRCUIT



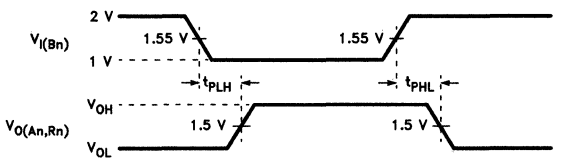
VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%.

FIGURE 3. PROPAGATION DELAY FROM T/$\overline{R}$ TO Bn



TEST CIRCUIT

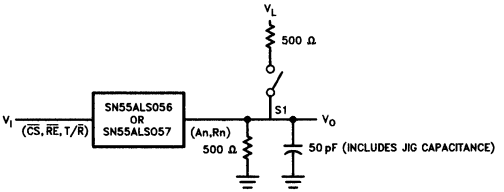


VOLTAGE WAVEFORMS

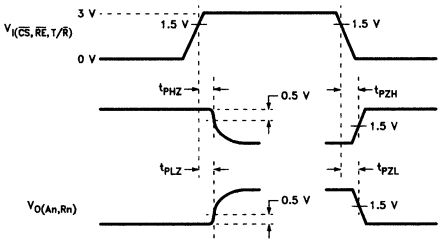
NOTE: $t_r = t_f \leq 10$ ns from 10% to 90%.

FIGURE 4. RECEIVER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



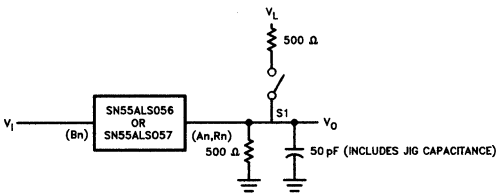
TEST CIRCUIT



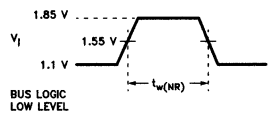
VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%.

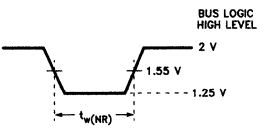
FIGURE 5. PROPAGATION DELAY FROM $\overline{CS}$ OR T/$\overline{R}$ TO An OR FROM $\overline{RE}$ TO Rn



TEST CIRCUIT



t_W is increased until the output voltage fall just reaches 2.0 V.



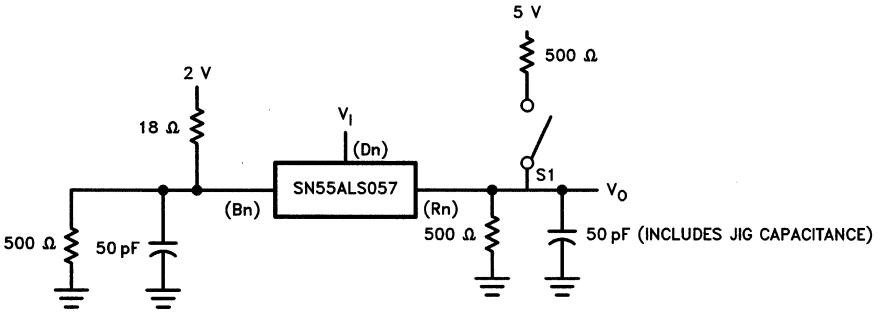
t_W is increased until the output voltage rise just reaches 0.8 V.

VOLTAGE WAVEFORMS

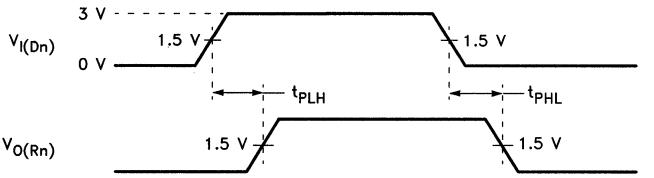
NOTE: $t_r = t_f \leq 2$ ns from 10% to 90%.

FIGURE 6. RECEIVER NOISE IMMUNITY

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%.

FIGURE 7. DRIVER PLUS RECEIVER DELAY TIMES

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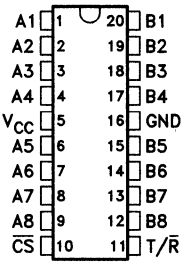
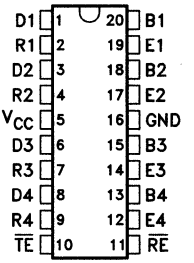
- **SN75ALS056 is an Octal Transceiver**
- **SN75ALS057 is a Quad Transceiver**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low Power Dissipation . . . 52.5 mW/Channel Max**
- **High-Impedance P-N-P Inputs**
- **Logic Level 1-V Bus Swing Reduces Power Consumption**
- **Trapezoidal Bus Output Waveform Reduces Noise Coupling to Adjacent Lines**
- **Power-Up/Down Protection (Glitch Free)**
- **Open-Collector Driver Outputs Allow Wired-OR Connections**
- **Designed to Be a Faster, Lower Power Functional Equivalent of National DS3896, DS3897**

SN75ALS056
DW OR N PACKAGE
(TOP VIEW)



SN75ALS057
DW OR N PACKAGE
(TOP VIEW)



description

The SN75ALS056 is an 8-channel, monolithic, high-speed, advanced low-power Schottky device designed for 2-way data communication in a densely populated backplane. The SN75ALS057 is a 4-channel version with independent driver input (Dn) and receiver output (Rn) pins and a separate driver disable for each driver (En).

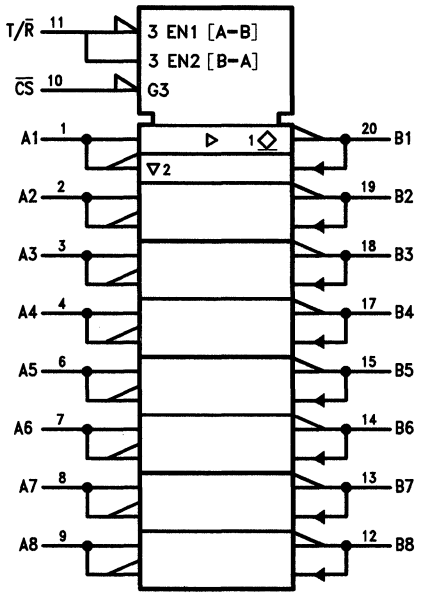
These transceivers feature open-collector driver outputs with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pull-up termination on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs generate trapezoidal waveforms that reduce crosstalk between channels. The drivers are capable of driving an equivalent dc load as low as 18.5 Ω.

The receivers have internal low-pass filters to further improve noise immunity.

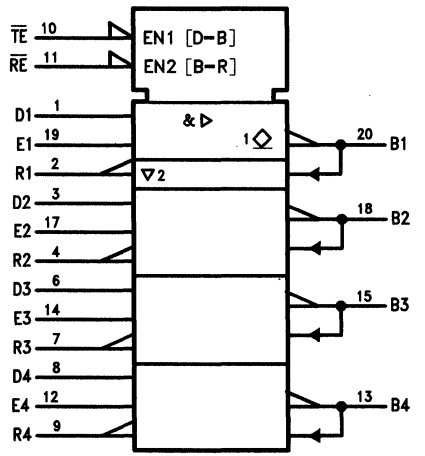
The SN75ALS056 and SN75ALS057 are characterized for operation from 0°C to 70°C.

logic symbols†

SN75ALS056

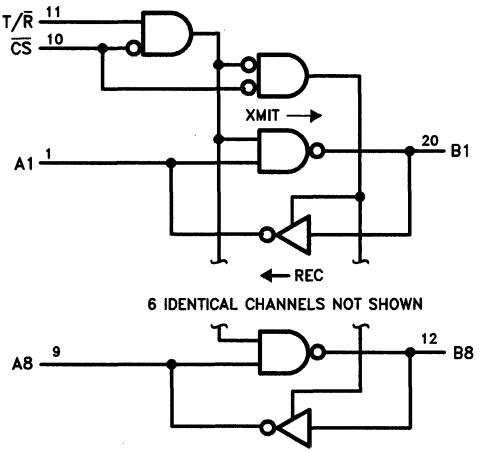


SN75ALS057

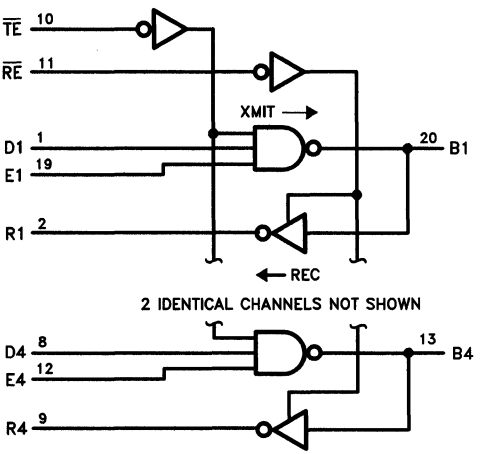


logic diagrams (positive logic)

SN75ALS056



SN75ALS057



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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SN75ALS056
FUNCTION TABLE
TRANSMIT/RECEIVE

CONTROLS		CHANNELS
$\overline{CS}$	T/$\overline{R}$	A ⟷ B
L	H	T (A → B)
L	L	R (B → A)
H	X	D

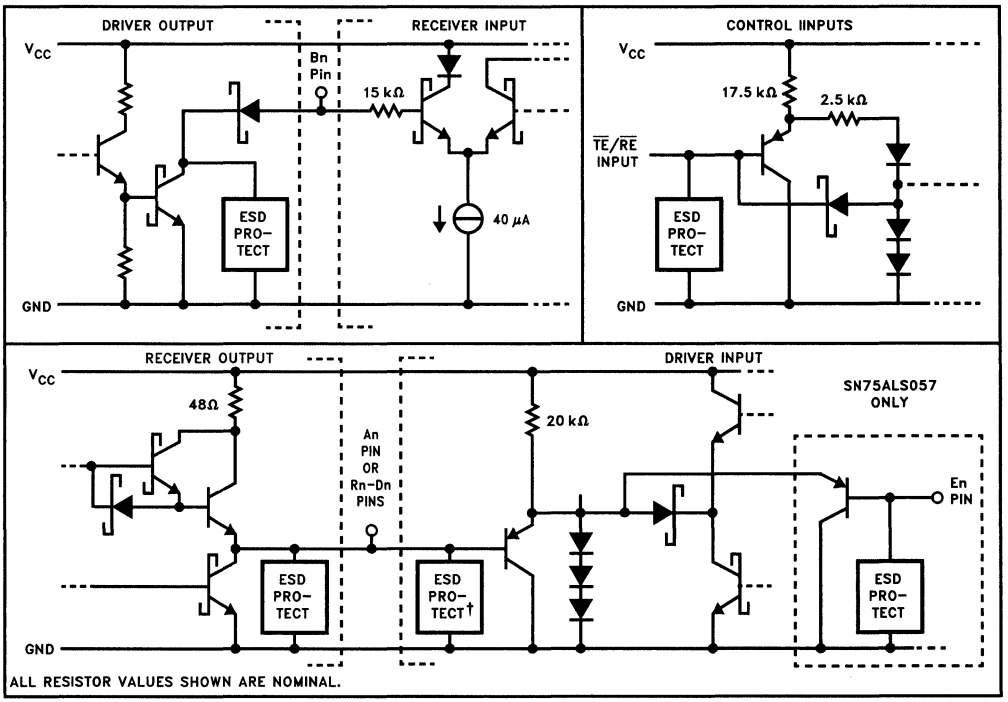
SN75ALS057
FUNCTION TABLE
TRANSMIT/RECEIVE

CONTROLS			CHANNELS	
$\overline{TE}$	$\overline{RE}$	En	D → B	B → R
L	L	L	D	R
L	L	H	T	R
L	H	L	D	D
L	H	H	T	D
H	L	X	D	R
H	H	X	D	D

H = high level, L = low level, R = receive, T = transmit, D = disable, X = irrelevant

Direction of data transmission is from An to Bn for the SN75ALS056 and from Dn to Bn for the SN75ALS057. Direction of data reception is from Bn to An for the SN75ALS056 and from Bn to Rn for the SN75ALS057. Data transfer is inverting in both directions.

schematics of inputs and outputs



† Additional ESD protection is on the SN75ALS057 only, which has separate receiver output and driver input pins.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 6 V
Control input voltage ..... 5.5 V
Driver input voltage ..... 5.5 V
Driver output voltage ..... 2.5 V
Receiver input voltage ..... 2.5 V
Receiver output voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm ($\frac{1}{16}$ inch) from case for 10 seconds ..... 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.5	V
V_{IH}	High-level driver and control input voltage	2			V
V_{IL}	Low-level driver and control input voltage			0.8	V
	Bus termination voltage	1.9		2.1	V
T_A	Operating free-air temperature	0		70	°C

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SN75ALS056 electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at An, T/$\overline{R}$, or $\overline{CS}$		I_I = −18 mA			−1.5	V
V_T	Receiver input threshold at Bn			1.426		1.674	mV
V_{OH}	High-level output voltage at An		Bn at 1.2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	An	Bn at 2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, I_{OL} = 16 mA			0.5	V
		Bn	An at 2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 2 V, V_L = 2 V, R_L = 18.5 Ω, See Figure 1	0.75		1.2	
I_{IH}	High-level input current	An, T/$\overline{R}$, or $\overline{CS}$	V_I = V_{CC}			40	μA
		Bn	V_I = 2 V, V_{CC} = 0 V or 5.25 V, An at 0.8 V, T/$\overline{R}$ at 0.8 V			100	
I_{IL}	Low-level input current at An, T/$\overline{R}$, or $\overline{CS}$		V_I = 0.4 V			−400	μA
I_{OS}	Short-circuit output current at An		An at 0 V, Bn at 1.2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V	−40		−120	mA
I_{CC}	Supply current					75	mA
$C_{o(B)}$	Driver output capacitance				4.5		pF

SN75ALS057 electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at Dn, En, $\overline{TE}$, or $\overline{RE}$		I_I = −18 mA			−1.5	V
V_T	Receiver input threshold at Bn			1426		1674	mV
V_{OH}	High-level output voltage at Rn		Bn at 1.2 V, $\overline{RE}$ at 0.8 V, I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	Rn	Bn at 2 V, $\overline{RE}$ at 0.8 V, I_{OL} = 16 mA			0.5	V
		Bn	Dn at 2 V, En at 2 V, $\overline{TE}$ at 0.8 V, V_L = 2 V, R_L = 18.5 Ω, See Figure 1	0.75		1.2	
I_{IH}	High-level input current	Dn, En, $\overline{TE}$, or $\overline{RE}$	V_I = V_{CC}			40	μA
		Bn	V_I = 2 V, V_{CC} = 0 V or 5.25 V, Dn at 0.8 V, En at 0.8 V, $\overline{TE}$ at 0.8 V			100	
I_{IL}	Low-level input current at Dn, En, $\overline{TE}$, or $\overline{RE}$		V_I = 0.4 V			−400	μA
I_{OS}	Short-circuit output current at Rn		Rn at 0, Bn at 1.2 V, $\overline{RE}$ at 0.8 V	−40		−120	mA
I_{CC}	Supply current					40	mA
$C_{o(B)}$	Driver output capacitance				4.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	An	Bn	$\overline{CL}$ at 0.8 V, V_L = 2 V,	T/$\overline{R}$ at 2 V, See Figure 2			19	ns
t_{PHL}	Propagation delay time, high-to-low-level output							18	
t_{PLH}	Propagation delay time low-to-high-level output	$\overline{CS}$	Bn	An and T/$\overline{R}$ at 2 V, See Figure 2	V_L = 2 V,			24	ns
t_{PHL}	Propagation delay time, high-to-low-level output							20	
t_{PLH}	Propagation delay time, low-to-high-level output	T/$\overline{R}$	Bn	$V_{I(An, Bn)}$ = 5 V, R_{L2} not connected, R_{L1} = 18 Ω,	$\overline{CS}$ at 0.8 V, C_L = 30 pF, See Figure 3			25	ns
t_{PHL}	Propagation delay time, high-to-low-level output							35	
t_{TLH}	Transition time, low-to-high-level output	An	Bn	$\overline{CS}$ at 0.8 V, V_L = 2 V,	T/$\overline{R}$ at 2 V, See Figure 2	1	3	11	ns
t_{THL}	Transition time, high-to-low-level output					1	3	6	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Bn	An	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, See Figure 4		18	ns
t_{PHL}	Propagation delay time, high-to-low-level output					18	
t_{PLZ}	Output disable time from low level	$\overline{CS}$	An	Bn at 2 V, T/$\overline{R}$ at 0.8 V, C_L = 5 pF, V_L = 5 V, R_{L1} = 390 Ω, R_{L2} not connected, See Figure 5		18	ns
t_{PZL}	Output enable time to low level	$\overline{CS}$	An	Bn at 2 V, T/$\overline{R}$ at 0.8 V, C_L = 30 pF, V_L = 5 V, R_{L1} = 390 Ω, R_{L2} = 1.6 kΩ, See Figure 5		15	ns
t_{PHZ}	Output disable time from high level	$\overline{CS}$	An	Bn at 0.8 V, T/$\overline{R}$ at 0.8 V, C_L = 5 pF, V_L = 0, R_{L1} = 390 Ω, R_{L2} not connected, See Figure 5		8	ns
t_{PZH}	Output enable time to high level	$\overline{CS}$	An	Bn at 0.8 V, T/$\overline{R}$ at 0.8 V, C_L = 30 pF, V_L = 0, R_{L1} not connected, R_{L2} = 1.6 kΩ, See Figure 5		17	ns
t_{PLZ}	Output disable time from low level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(An, Bn)}$ = 2 V, V_L = 5 V, R_{L1} = 390 Ω, R_{L2} not connected, C_L = 5 pF, See Figure 3		20	ns
t_{PZL}	Output enable time to low level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(An, Bn)}$ = 2 V, V_L = 5 V, R_{L1} = 390 Ω, R_{L2} = 1.6 kΩ, C_L = 30 pF, See Figure 3		40	ns
t_{PHZ}	Output disable time from high level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(An, Bn)}$ = 0, V_L = 0, R_{L1} = 390 Ω, R_{L2} not connected, C_L = 5 pF, See Figure 3		17	ns
t_{PZH}	Output enable time to high level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(An, Bn)}$ = 0, V_L = 0, R_{L1} not connected, R_{L2} = 1.6 kΩ, C_L = 30 pF, See Figure 3		15	ns
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	An or Rn	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, See Figure 6	3		ns

switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Dn or En	Bn	$\overline{TE}$ at 0.8 V, V_L = 2 V,	$\overline{RE}$ at 2 V, See Figure 2			19	ns
t_{PHL}	Propagation delay time, high-to-low-level output							18	
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{TE}$	Bn	Dn, En, $\overline{RE}$ at 2 V, R_{L1} = 18 Ω,	V_L = 2 V, See Figure 2			24	ns
t_{PHL}	Propagation delay time, high-to-low-level output							20	
t_{TLH}	Transition time, low-to-high-level output	Dn or En	Bn	$\overline{RE}$ at 2 V, $\overline{TE}$ at 0.8 V,	V_L = 2 V, See Figure 2		1 3	11	ns
t_{THL}	Transition time, high-to-low-level output						1 3	6	

receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Bn	Rn	$\overline{RE}$ at 0.9 V, $\overline{TE}$ at 2 V,	See Figure 4		18	ns
t_{PHL}	Propagation delay time, high-to-low-level output						18	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	Rn	Bn at 2 V, $\overline{TE}$ at 2 V, C_L = 5 pF, R_{L1} = 390 Ω, R_{L2} not connected,	V_L = 5 V, See Figure 5		18	ns
t_{PZL}	Output enable time to low level	$\overline{RE}$	Rn	Bn at 2 V, $\overline{TE}$ at 2 V, C_L = 30 pF, R_{L1} = 390 Ω, See Figure 5	V_L = 5 V, R_{L2} 1.6 kΩ,		15	ns
t_{PHZ}	Output disable time from high level	$\overline{RE}$	Rn	Bn at 0.8 V, $\overline{TE}$ at 2 V, C_L = 5 pF, R_{L1} = 390 Ω, R_{L2} not connected,	V_L = 0, See Figure 5		17	ns
t_{PZH}	Output enable time to high level	$\overline{RE}$	Rn	Bn at 0.8 V, $\overline{TE}$ at 2 V, C_L = 30 pF, R_{L1} not connected, R_{L2} = 1.6 kΩ,	V_L = 0, See Figure 5		17	ns
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	Cn	$\overline{TE}$ at 2.0 V, $\overline{RE}$ at 0.8 V, See Figure 6		3		ns

driver plus receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Dn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 0.8 V,	See Figure 7		40	ns
t_{PHL}	Propagation delay time, high-to-low-level output						40	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

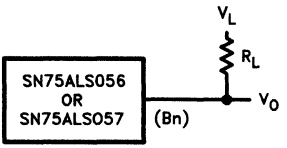
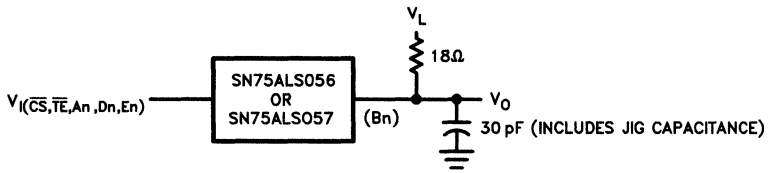
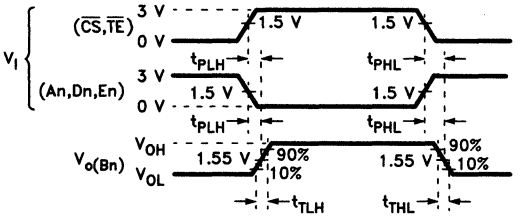


FIGURE 1. DRIVER LOW-LEVEL-OUTPUT-VOLTAGE TEST CIRCUIT



TEST CIRCUIT

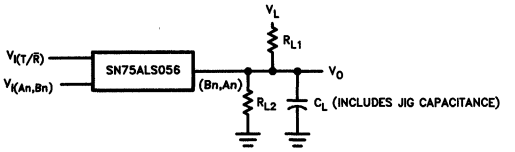


VOLTAGE WAVEFORMS

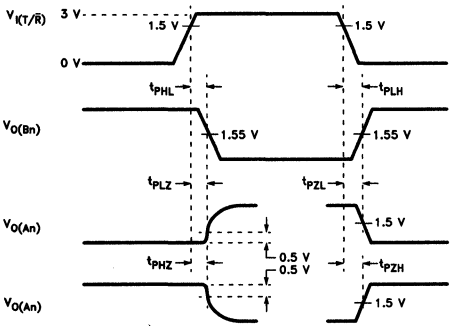
NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%.

FIGURE 2. DRIVER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



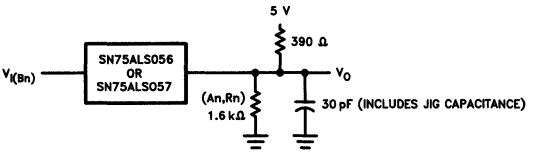
TEST CIRCUIT



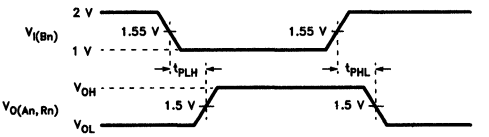
VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%.

FIGURE 3. PROPAGATION DELAY FROM T/$\overline{R}$ TO An OR Bn



TEST CIRCUIT

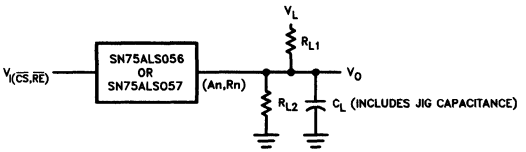


VOLTAGE WAVEFORMS

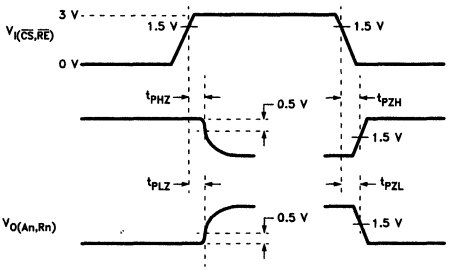
NOTE: $t_r = t_f \leq 10$ ns from 10% to 90%.

FIGURE 4. RECEIVER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



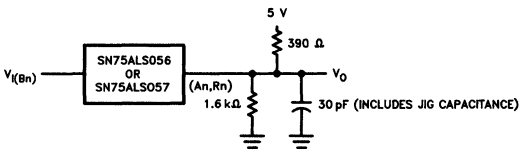
TEST CIRCUIT



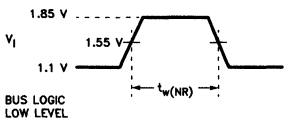
VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%.

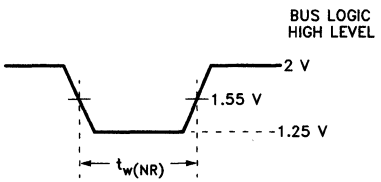
FIGURE 5. PROPAGATION DELAY FROM $\overline{CS}$ TO An OR $\overline{RE}$ TO Rn



TEST CIRCUIT



t_W is increased until the output voltage fall just reaches 2 V.



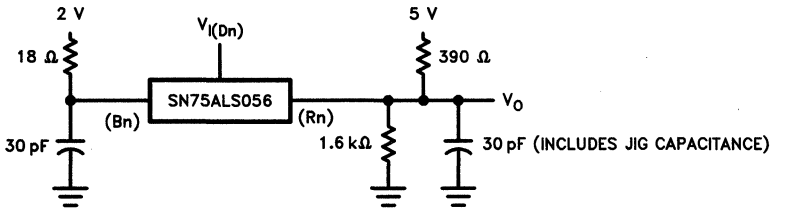
t_W is increased until the output voltage rise just reaches 0.8 V.

VOLTAGE WAVEFORMS

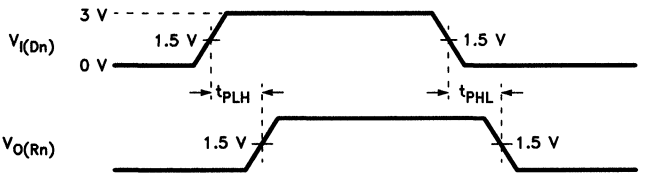
NOTE: $t_r = t_f \leq 2$ ns from 10% to 90%.

FIGURE 6. RECEIVER NOISE IMMUNITY

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



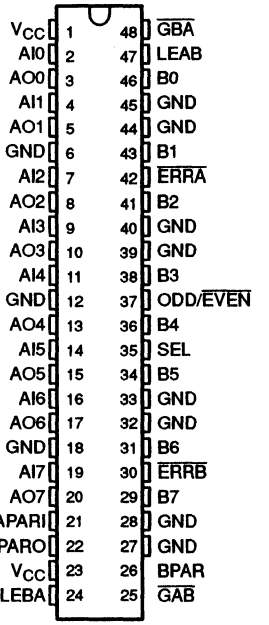
VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%.

FIGURE 7. DRIVER PLUS RECEIVER DELAY TIMES

- **Supports Draft Futurebus + Standard (IEEE P896.1, 90 July 16) and Pi-Bus Standard**
- **Packaged in Plastic Shrink Small-Outline 300-mil Packages (SSOP) and Very Small Outline Flatpack (VSOW)**
- **Open-Collector B Port Drives Load Impedances as Low as 10 Ω**
- **BTL Logic Level 1-V Bus Swing Reduces Power Consumption**
- **Latchable Transceiver With Output Sink of 24 mA at the A Bus and 100 mA at the B Bus**
- **Option to Generate and Check Parity or Feed-Through Data/Parity in Directions A-to-B or B-to-A**
- **Independent Latch Enables for A-to-B and B-to-A Directions**
- **ODD/$\overline{\text{EVEN}}$ Parity-Select Pin**
- **$\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ Output Pins for Parity Checking**
- **Ability to Simultaneously Generate and Check Parity**
- **ESD Protection Exceeds 2000 V Per MIL-STD 883C, Method 3015**

SN54BCT979 ... WD PACKAGE
SN74BCT979 ... DL PACKAGE
(TOP VIEW)



description

The 'BCT979 is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data bus in either direction. It has a specified current-sinking capability of 24 mA at the A-bus and 100 mA at the B-bus.

The 'BCT979 features independent latch enables (LEAB and LEBA) for the A-to-B direction and the B-to-A direction, a select pin for ODD/$\overline{\text{EVEN}}$ parity, and separate error signal output pins for checking parity.

When communication between buses occurs, parity is generated and passed on to either bus as APAR or BPAR. Error detection of the parity generated from AI0-AI7 and B0-B7 can be checked by $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$, provided that LEAB and LEBA are high and the mode select SEL is low. If SEL is high, the communication between buses is in a feed-through mode where parity is still generated and checked as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$.

PRODUCT PREVIEW

The 'BCT979 features open-collector driver outputs at the B port (B0-B7 and BPAR) with a series Schottky diode to reduce capacitive loading to the bus. If a 2-V pullup is used on the bus, the output signal swing is approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs are capable of driving an equivalent dc load of as low as 10 Ω.

The transceiver has a precision threshold set by an internal bandgap reference to give accurate input thresholds over V_{CC} and temperature variations.

This transceiver is compatible with Backplane Transceiver Logic (BTL) technology at significantly reduced power dissipation per channel.

The SN54BCT979 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT979 is characterized for operation from 0°C to 70°C.

PARITY FUNCTION TABLE (SEE NOTE 1)

INPUTS†			OUTPUTS	
ODD/$\overline{\text{EVEN}}$	Σ of inputs AO0-AO7 = H	APARI	BPAR‡	$\overline{\text{ERRA}}$
L	0, 2, 4, 6, 8	L	L	H
L	1, 3, 5, 7	L	H	L
L	0, 2, 4, 6, 8	H	L	L
L	1, 3, 5, 7	H	H	H
H	0, 2, 4, 6, 8	L	H	L
H	1, 3, 5, 7	L	L	H
H	0, 2, 4, 6, 8	H	H	H
H	1, 3, 5, 7	H	L	L

† If LEAB = H, current AI0-AI7 and APARI data is used. If LEAB = L, latched AI0-AI7 and APARI data is used.
‡ This is the value of BPAR if SEL = L. If SEL = H, BPAR = APARI.
NOTE 1: Parity functions for the A bus are shown. Parity functions for the B bus are similar, but use B0-B7 and BPAR as inputs and APARO and $\overline{\text{ERRB}}$ as outputs.

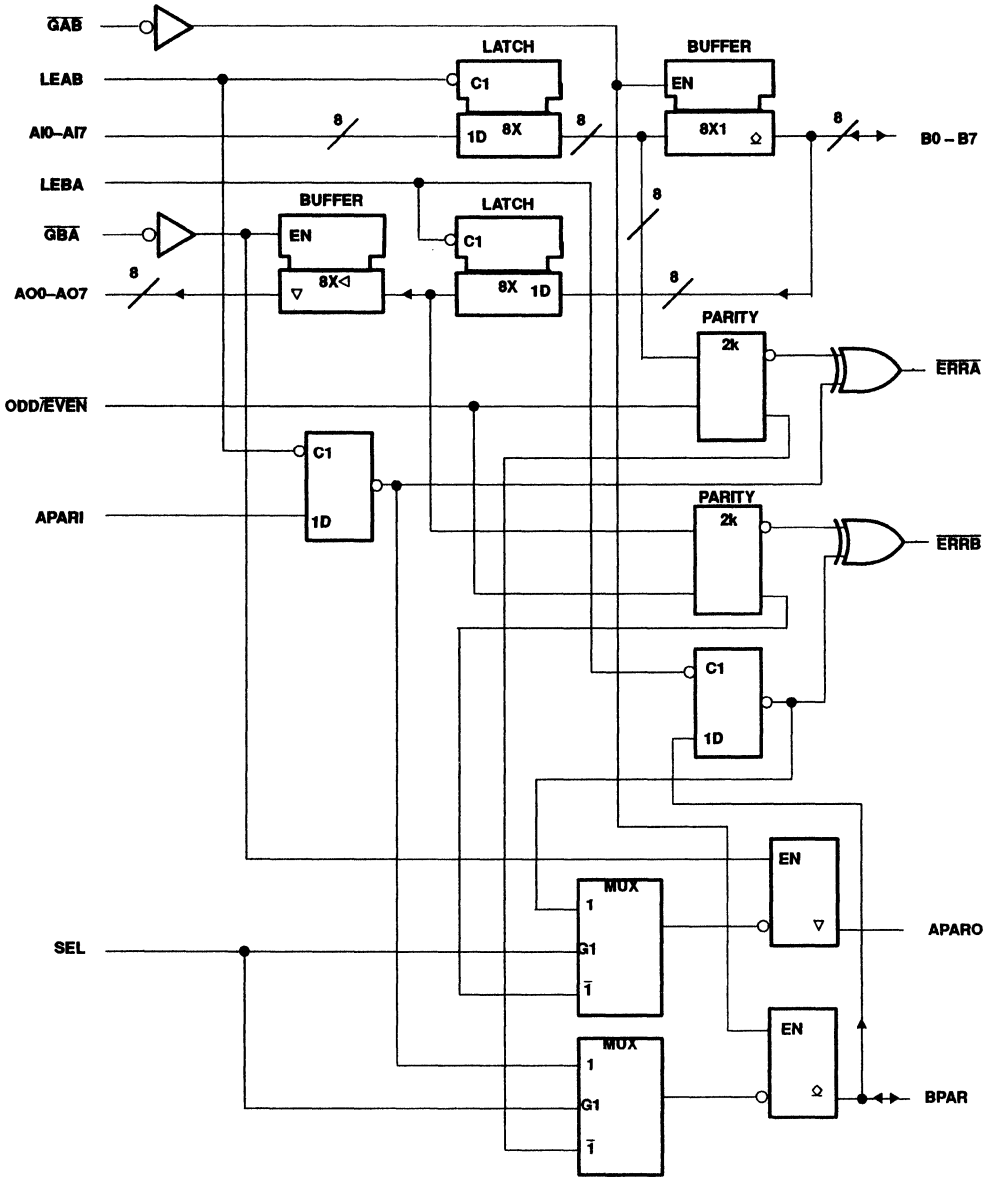
FUNCTION TABLE

CONTROL INPUTS					OPERATION§
$\overline{\text{GAB}}$	$\overline{\text{GBA}}$	SEL	LEAB	LEBA	
H	H	X	X	X	Isolation. AO0-AO7/APARO are in the high impedance state, and B0-B7/BPAR are high.
H	L	L	X	H	B to A mode parity is generated from B0-B7 data and output on APARO, and is checked against BPAR with the result output on $\overline{\text{ERRB}}$.
H	L	L	X	L	B to A mode parity is generated from latched B0-B7 data and output on APARO, and is checked against BPAR with the result output on $\overline{\text{ERRB}}$.
H	L	H	X	H	B to A mode BPAR is output on APARO. Parity is generated from B0-B7 data, checked against BPAR, and output on $\overline{\text{ERRB}}$.
H	L	H	X	L	B to A mode BPAR is output on APARO. Parity is generated from latched B0-B7 data, checked against BPARO, and output on $\overline{\text{ERRB}}$.
L	H	L	H	X	A to B mode parity is generated from AI0-AI7 data and output on BPAR, and is checked against APARI and output on $\overline{\text{ERRA}}$.
L	H	L	L	X	A to B mode parity is generated from latched AI0-AI7 data and output on BPAR, and is checked against APARI and output on $\overline{\text{ERRA}}$.
L	H	H	H	X	A to B mode APARI is output on BPAR. Parity is generated from AI0-AI7 data, checked against APARI, and output on $\overline{\text{ERRA}}$.
L	H	H	L	X	A to b mode APARI is output on BPAR. Parity is generated from latched AI0-AI7 data, checked against APARI, and output on $\overline{\text{ERRA}}$.
L	L	X	X	X	AO0-AO7/APARO and B0-B7/BPAR are active (high or low logic level).

§ Parity is generated from AI0-AI7 and from B0-B7 based on the level present at ODD/$\overline{\text{EVEN}}$. Parity is checked (AO0-AO7 against APARI and B0-B7 against BPAR) based on the level present at ODD/$\overline{\text{EVEN}}$. See parity function table.

PRODUCT PREVIEW

logic diagram (positive diagram)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V

Input voltage range: B0-B7, BPAR ..... −0.5 V to 5.5 V
Other Inputs ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 7 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Operating free-air temperature range: SN54BCT979 ..... −55°C to 125°C
SN74BCT979 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54BCT979			SN74BCT979			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	B0-B7, BPAR	1.6			1.6			V
		Other inputs	2			2			
V_{IL}	Low-level input voltage	B0-B7, BPAR			1.475			1.475	V
		Other inputs			0.8			0.8	
V_{OH}	High-level output voltage	B0-B7, BPAR			2			2	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	AO0-AO7, APARO, $\overline{ERRA}$, $\overline{ERRB}$			−3			−3	mA
I_{OL}	Low-level output current	AO0-AO7, APARO, $\overline{ERRA}$, $\overline{ERRB}$			24			24	mA
		B0-B7, BPAR			100			100	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54BCT979			SN74BCT979			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA			−1.2			−1.2	V
I_{OH}	B0-B7, BPAR	V_{CC} = 5.5 V, V_{OH} = 2 V			100			100	μA
V_{OH}	AO0-AO7, APARO, $\overline{ERRA}$, $\overline{ERRB}$	V_{CC} = 4.5 V, I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.5 V, I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
V_{OL}	AO0-AO7, APARO, $\overline{ERRA}$, $\overline{ERRB}$	V_{CC} = 4.5 V, I_{OL} = 20 mA		0.3	0.5				V
		V_{CC} = 4.5 V, I_{OL} = 24 mA					0.35	0.9	
	B0-B7, BPAR	V_{CC} = 4.5 V, I_{OL} = 80 mA	0.75		1.1	0.75		1.1	V
		V_{CC} = 4.5 V, I_{OL} = 100 mA			1.15			1.15	
I_I	LEAB, LEBA, $\overline{GAB}$, $\overline{GBA}$, SEL ODD/$\overline{EVEN}$, AI0-AI7, APARI	V_{CC} = 0, V_I = 7 V			100			100	μA
	B0-B7, BPAR	V_{CC} = 5.5 V, V_I = 5.5 V			1			1	mA
I_{IH}	LEAB, LEBA, $\overline{GAB}$, $\overline{GBA}$, SEL ODD/$\overline{EVEN}$, AI0-AI7, APARI	V_{CC} = 5.5 V, V_I = 2.7 V			20			20	μA
	B0-B7‡, BPAR	V_{CC} = 5.5 V, V_I = 2.1 V			100			100	μA
I_{IL}	LEAB, LEBA, $\overline{GAB}$, $\overline{GBA}$, SEL ODD/$\overline{EVEN}$, AI0-AI7, APARI	V_{CC} = 5.5 V, V_I = 0.5 V			−0.6			−0.6	μA
	B0-B7‡	V_{CC} = 5.5 V, V_I = 0.3 V			−100			−100	
I_{OZH}	AO0-AO7, APARO	V_{CC} = 5.5 V, V_O = 2.7 V			50			50	μA
I_{OZL}	AO0-AO7, APARO	V_{CC} = 5.5 V, V_O = 0.5 V			−50			−50	μA
I_{OS}§	AO0-AO7, APARO	V_{CC} = 5.5 V, V_O = 0	−60		−150	−60		−150	mA
I_{CC}	Outputs low	V_{CC} = 5.5 V, I_O = 0					69		mA
	Outputs high	V_{CC} = 5.5 V, I_O = 0					17		
	Outputs disabled	V_{CC} = 5.5 V, I_O = 0					21		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed 1 second.

timing requirements

			V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§				UNIT
			SN54BCT979		SN74BCT979		
			MIN	MAX	MIN	MAX	
t_{su}	Setup time	AI0-AI7, APARI before LEAB ↑	3		3		ns
		B0-B7, BPAR before LEBA ↑	5		5		
t_h	Hold time	AI0-AI7, APARI after LEAB ↑	1		1		ns
		B0-B7, BPAR after LEBA ↑	0		0		
t_w	Pulse duration	LEAB high	5		5		ns
		LEBA high	5		5		

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PRODUCT PREVIEW

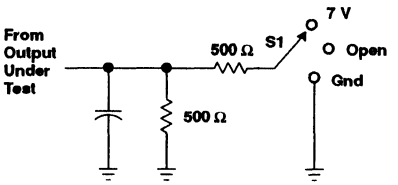
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'BCT979			SN54BCT979		SN74BCT979		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	AI	B		5.6						ns
t_{PHL}				5.8						
t_{PLH}	B	AO		5.6						ns
t_{PHL}				5.8						
t_{PLH}	APARI	BPAR		5.8						ns
t_{PHL}				6.1						
t_{PLH}	BPAR	APARO		5.8						ns
t_{PHL}				6.1						
t_{PLH}	AI, APARI	$\overline{ERRA}$		8.1						ns
t_{PHL}				8.1						
t_{PLH}	B, BPAR	$\overline{ERRB}$		8.1						ns
t_{PHL}				8.1						
t_{PLH}	ODD/$\overline{EVEN}$	$\overline{ERRA}$		10						ns
t_{PHL}				10.7						
t_{PLH}	ODD/$\overline{EVEN}$	$\overline{ERRB}$		10						ns
t_{PHL}				10.7						
t_{PLH}	ODD/$\overline{EVEN}$	APAR		10.2						ns
t_{PHL}				10.7						
t_{PLH}	ODD/$\overline{EVEN}$	BPAR		10.2						ns
t_{PHL}				10.7						
t_{PLH}	SEL	APARO, BPAR		6.3						ns
t_{PHL}				5.8						
t_{PLH}	LEAB	B, BPAR		6.6						ns
t_{PHL}				6.3						
t_{PLH}	LEBA	AO, APARO		6.6						ns
t_{PHL}				6.3						
t_{PLH}	LEAB	$\overline{ERRA}$		6.6						
t_{PHL}	LEAB	$\overline{ERRA}$		6.3						
t_{PLH}	LEBA	$\overline{ERRB}$		6.6						
t_{PHL}	LEBA	$\overline{ERRB}$		6.3						
t_{PZH}	$\overline{GBA}$	AO, APARO		7.2						ns
t_{PZL}				9.5						
t_{PZH}	$\overline{GAB}$	B, BPAR		7.2						ns
t_{PZL}				9.5						
t_{PHZ}	$\overline{GBA}$	AO, APARO		6.8						ns
t_{PLZ}				5.5						
t_{PHZ}	$\overline{GBA}$	AO, APARO		6.8						ns
t_{PLZ}				5.5						

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

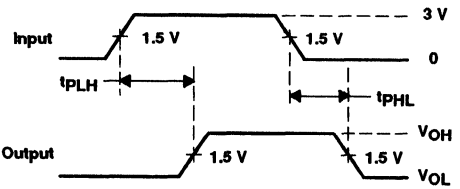
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

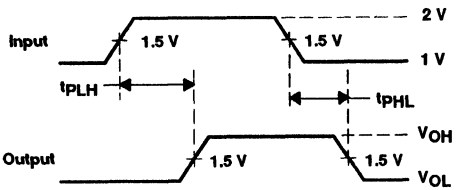


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

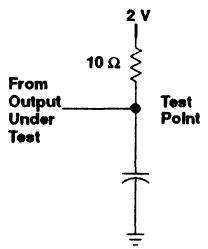
LOAD CIRCUIT FOR A OUTPUTS



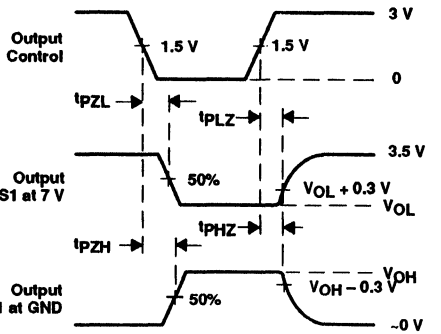
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



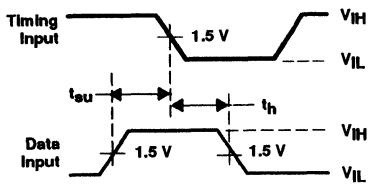
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A PORT)



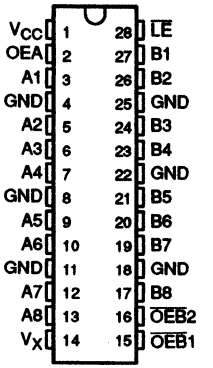
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

FIGURE 1. LOAD CIRCUITS AND VOLTAGE WAVEFORMS

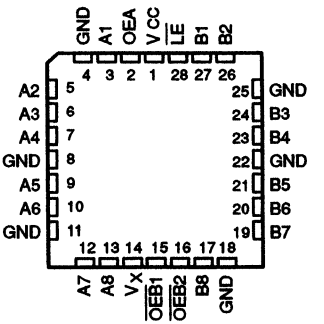
PRODUCT PREVIEW

- **Drives Heavily Loaded Backplanes With Equivalent Load Impedances Down to 10-Ω**
- **Compatible with Pi-Bus and IEEE 896 Futurebus Standards**
- **High-Drive (100 mA) Open-Collector Drivers on B Ports**
- **High-Speed Operation Enhances Performance of Backplane Buses and Facilitates Incident-Wave Switching**
- **Reduced Voltage Swing (1 V) Produces Less Noise and Reduces Power Comsumption**
- **High-Impedance State During Power-Up and Power-Down**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54F776 ... JT PACKAGE
SN74F776 ... DW OR NT PACKAGE
(TOP VIEW)



SN54F776 ... FK PACKAGE
(TOP VIEW)



description

The 'F776 is an octal bidirectional latched transceiver and is intended to provide the electrical interface to a high-performance wired-or bus. The B port inverting drivers are low-capacitance open-collector with controlled ramp and are designed to sink 100 mA from 2 V. The B port inverting receivers have a 100-mV threshold region and a 4-ns glitch filter.

The 'F776 B port interfaces to Backplane Transceiver Logic (BTL™). BTL features a reduced (1-V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading (<5 pF).

Incident-wave switching is used, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

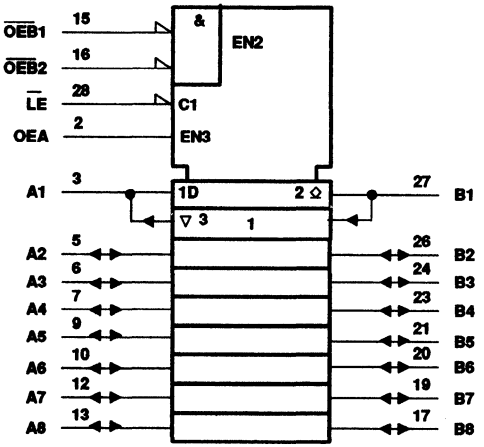
BTL offers low power consumption, EMI and crosstalk, low capacitive loading, superior noise margin, and low propagation delays. This results in a high bandwidth, reliable backplane. The 'F776 A port has TTL 3-state drivers and TTL receivers with a latch function. A separate high-level control voltage input (V_X) is provided to limit the A side output level to a given voltage level (such as 3.3 V). For 5 V systems, V_X is simply tied to V_{CC}.

The 'F776 has a designed feature to control the B output transitions during power sequencing. There are two possible sequences as follows:
1. When $\overline{LE}$ is low and $\overline{OEB}_n$ is low, the B outputs are disabled until the $\overline{LE}$ circuitry takes control. Then the B outputs follow the A inputs. This causes a maximum of one transition during power-up or power-down.
2. If $\overline{LE}$ is high or $\overline{OEB}_n$ is high, then the B outputs are disabled during power-up or power-down.

PRODUCT PREVIEW

BTL is a trademark of National Semiconductor Corporation.

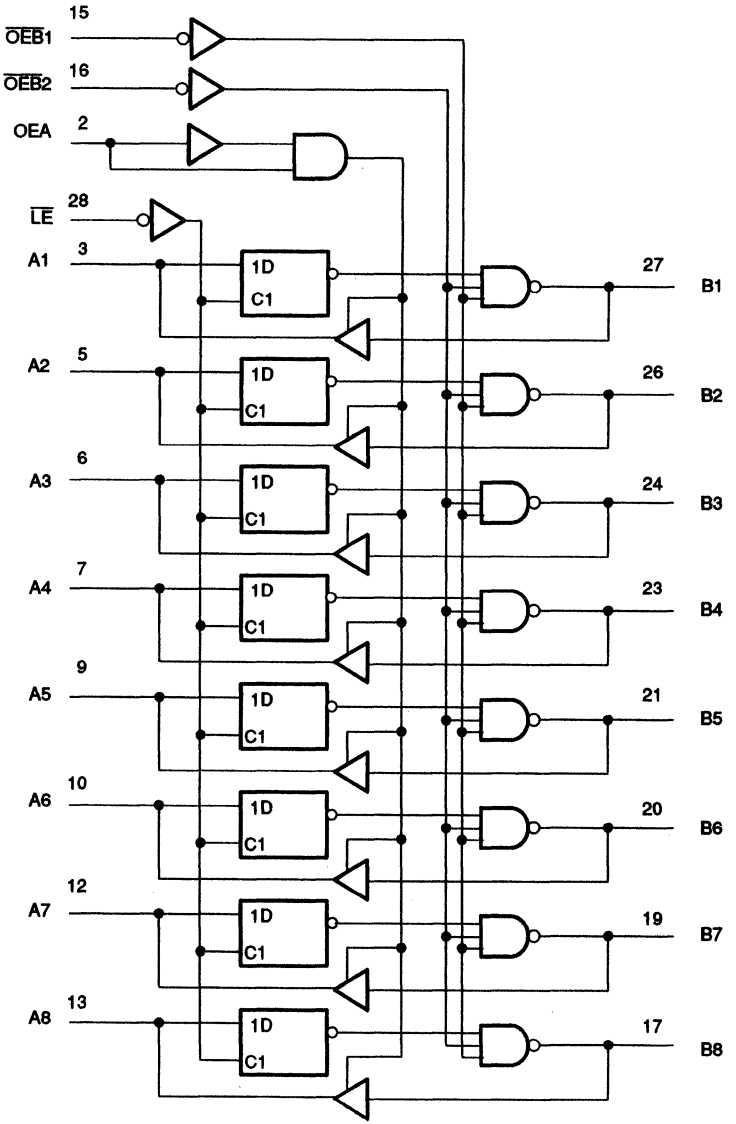
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

PRODUCT PREVIEW

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

PRODUCT PREVIEW

FUNCTION TABLE

INPUTS						LATCH	OUTPUTS		MODE
An	Bn†	$\overline{LE}$	OEA	$\overline{OEB1}$	$\overline{OEB2}$	STATE	An	Bn	
H	X	L	L	L	L	H	Z	H	A at high impedance, data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Q_0	Z	Q_0	A high impedance, latched data to B
—	—	L	H	L	L	‡	‡	‡	Feedback A to B and B to A
—	H	H	H	L	L	H§	H	Z§	Preconditioned latch enabling data transfer from B to A
—	L	H	H	L	L	H§	L	Z§	
—	—	H	H	L	L	Q_0	Q_0	Q_0	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A at high impedance
L	X	L	L	H	X	L	Z	Z	
X	X	H	L	H	X	Q_0	Z	Z	
H	X	L	L	X	H	H	Z	Z	
L	X	L	L	X	H	L	Z	Z	
X	X	H	L	X	H	Q_0	Z	Z	
—	H	L	H	H	X	H	H	Z	B at high impedance, data from B to A
—	L	L	H	H	X	L	L	Z	
—	H	H	H	H	X	Q_0	H	Z	
—	L	H	H	H	X	Q_0	L	Z	
—	H	L	H	X	H	H	H	Z	
—	L	L	H	X	H	L	L	Z	
—	H	H	H	X	H	Q_0	H	Z	
—	L	H	H	X	H	Q_0	L	Z	

H = High-voltage level, L = Low-voltage level, X = Don't care, — = Input not externally driven, Z = High-impedance (Off) state, Qn_0 = High or low voltage level one setup time prior to the low-to-high $\overline{LE}$ transition

† Precaution should be taken to ensure the B inputs do not float. If they are permitted to float, the B inputs will take on the low level.

‡ Condition will cause a feedback loop path; A to B and B to A.

§ The latch must be preconditioned high such that B inputs can assume a high or low level while $\overline{OEB1}$ and $\overline{OEB2}$ are low and $\overline{LE}$ is high.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range ..... −0.5 V to 7 V
Thresold control voltage, V_X ..... −0.5 V to 7 V
Input current ..... −40 mA to 5 mA
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54F776 (A1 thru A8) ..... 40 mA
SN54F776 (B1 thru B8) ..... 200 mA
SN74F776 (A1 thru A8) ..... 48 mA
SN74F776 (B1 thru B8) ..... 200 mA
Operating free-air temperature range: SN54F776 ..... −55°C to 125°C
SN74F776 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			SN54F776			SN74F776			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level output voltage	B1 thru B8	1.6			1.8			V
		All others	2			2			
V_{IL}	Low-level output voltage	B1 thru B8			1.45			1.45	V
		All others			0.8			0.8	
I_{IK}	Input clamp current	A1 thru A8			−40			−40	mA
		All others			−18			−18	
I_{OH}	High-level output current	A1 thru A8			−3			−3	mA
I_{OL}	Low-level output current	A1 thru A8			20			24	mA
		B1 thru B8			100			100	
T_A	Operating free-air temperature range		−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54F776			SN74F776			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	A1 thru A8	V_{CC} = 4.5 V, I_I = −18 mA			−0.5			−0.5	V
	B1 thru B8, Control inputs				−1.2			−1.2	
I_{OH}	B1 thru B8	V_{CC} = 5.5 V, V_{IL} = 1.45 V, V_{IH} 1.6 V, V_{OH} = 2.1 V			100			100	μA
V_{OH}	A1 thru A8	V_{CC} = 4.5 V, I_{OH} = −3 mA, V_X = V_{CC}	2.5	2.9		2.5			V
		V_{CC} = 4.5 V, I_{OH} = −0.4 mA, V_X = 3.13 V or 3.47 V	2.5			2.5			
V_{OL}	A1 thru A8	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_X = V_{CC}		0.3	0.5			0.5	V
	B1 thru B8	V_{CC} = 4.5 V, I_{OL} = 100 mA			1.5			1.5	
		V_{CC} = 4.5 V, I_{OL} = 4 mA	0.4			0.4			
I_{IH1}‡	Control inputs	V_{CC} = 5.5 V, V_I = 2.7 V			20			20	μA
	B1 thru B8	V_{CC} = 5.5 V, V_I = 2.1 V			100			100	
I_{IH2}‡	Control inputs	V_{CC} = 5.5 V, V_I = 7 V		1	100			100	μA
	A1 thru A8	V_{CC} = 5.5 V, V_I = 5.5 V		0.01	1			1	mA
	B1 thru B8			0.01	1				
I_{IL}	Control inputs	V_{CC} = 5.5 V, V_I = 0.5 V			−20			−20	μA
	B1 thru B8	V_{CC} = 5.5 V, V_I = 0.3 V			−100			−100	
I_{OZH}	A1 thru A8	V_{CC} = 5.5 V, V_O = 2.7 V			70			70	μA
I_{OZL}	A1 thru A8	V_{CC} = 5.5 V, V_O = 0.5 V			−70			−70	μA
I_{OS}§	A1 thru A8 only	V_{CC} = 5.5 V, B_n at 1.6 V, OEA, $\overline{OEB}$1, and $\overline{OEB}$2 at 2.7 V	−60	−75	−150	−60		−150	mA
I_X		V_{CC} = 5.5 V, V_X = V_{CC}, $\overline{LE}$, OEA, $\overline{OEB}$1, $\overline{OEB}$2 and A1 thru A8 at 2.7 V, B1 thru B8 at 2 V			±100			±100	μA
		V_{CC} = 5.5 V, V_X = 3.13 V or 3.47 V, $\overline{LE}$ and OEA at 2.7 V, $\overline{OEB}$1, $\overline{OEB}$2, A1 thru A8 and B1 thru B8 at 2 V			±10			±10	μA
I_{CCH}		V_{CC} = 5.5 V			100		70	100	mA
I_{CCL}		V_{CC} = 5.5 V			145		100	145	mA
I_{CCA}		V_{CC} = 5.5 V			100		80	100	m/

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should exceed one second.

timing requirements

		V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX¶				UNIT
		'F776		SN54F776		SN74F776		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Setup time, A to $\overline{LE}$	5		5		5		ns
t_h	Hold time, A to $\overline{LE}$	0		0		0		ns
t_w	Pulse duration, $\overline{LE}$ low	10		10		6		ns

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PRODUCT PREVIEW

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F776			SN54F776		SN74F776		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	5.5	7.5	12	4.5	13	2	8	ns
t_{PHL}			3.5	5.5	8	2.5	9	3	9	
t_{PLH}	B	A	5.5	7.5	12	4.5	13	5	12	ns
t_{PHL}			6	8.5	10.5	6	11.5	6	11	
t_{PLH}	$\overline{LE}$	B	3	5	8.5	2	11.5	2.5	10	ns
t_{PHL}			4	6	9	3	9.5	3	9.5	
t_{PLH}	$\overline{OEB}_n$	B	2	4.5	7.5	1.5	8.5	1.5	8.5	ns
t_{PHL}			4.5	7.5	10	3.5	10.5	3.5	10.5	
t_{PZH}	OEA	A	8	10.5	14.5	7	16.5	7.5	15.5	ns
t_{PZL}			8.5	12	14.5	8.5	18	8.5	17	
t_{PHZ}	OEA	A	2	4.5	7	2	7.5	2	7.5	ns
t_{PLZ}			2	4.5	7.5	2	8	2	8	
t_t‡	B ports 1.3 V to 1.7 V		0.5	2	4.5	0.5	4.5	0.5	4.5	ns
t_t‡	B ports 1.7 V to 1.3 V		0.5	2	4.5	0.5	4.5	0.5	4.5	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ Transition time is defined as the time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

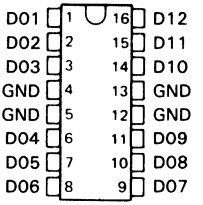
PRODUCT PREVIEW

5 Bus-Termination Array Products

D3228, JULY 1989 – REVISED MARCH 1990

- **Designed to Reduce Reflection Noise**
- **Repetitive Peak Forward Current . . . 200 mA**
- **12-Bit Array Structure Suited for Bus-Oriented Systems**
- **ESD Protection Exceeds 10 kV Per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)

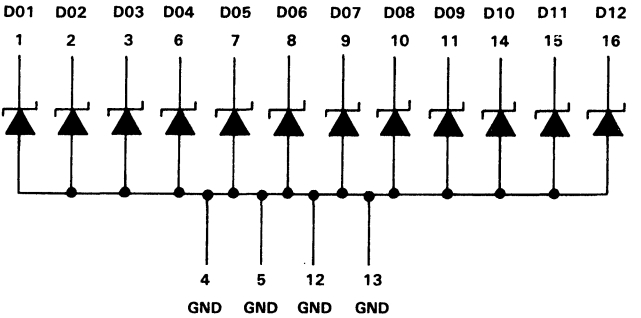


description

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 12-bit high-speed Schottky diode array suitable for a clamp to GND.

The SN74S1050 is characterized for operation from 0°C to 70°C.

schematic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, V_R . . . . . 7 V
Continuous forward current, I_F: any D terminal from GND . . . . . 50 mA
total through all GND terminals . . . . . 170 mA
Repetitive peak forward current,‡ I_{FRM}: any D terminal from GND . . . . . 200 mA
total through all GND terminals . . . . . 1 A
Continuous total power dissipation at (or below) 25°C free-air temperature . . . . . 625 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡These values apply for $t_w \leq 100\ \mu s$, duty cycle ≤ 20%.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
I_R	Static reverse current	V_R = 7 V				5	μA
V_F	Static forward voltage	I_F = 18 mA			0.75	0.95	V
		I_F = 50 mA			0.95	1.2	
V_{FM}	Peak forward voltage	I_F = 200 mA			1.45		V
C_T	Total capacitance	V_R = 0,	f = 1 MHz		5	10	pF
		V_R = 2 V,	f = 1 MHz		4	8	

NOTE 1: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
I_X	Internal crosstalk current	Total I_F = 1 A,	See Note 2		0.6	2	mA
		Total I_F = 198 mA,	See Note 2		0.02	0.2	

§All typical values are at T_A = 25°C.
NOTE 2: I_X is measured under the following conditions with one diode static and all others switching:
Switching diodes: t_w = 100 μs, duty cycle = 20%; static diode: V_R = 5 V.
The static diode's input current is the internal crosstalk current I_X.

switching characteristics at 25°C free-air temperature (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse recovery time	I_F = 10 mA, $I_{RM(REC)}$ = 10 mA, $i_{R(REC)}$ = 1 mA, R_L = 100 Ω		8	16	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.), or on the CLOCK lines of many clocked devices can result in improper operation of the device. The SN74S1050 and SN74S1052 diode termination arrays help suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to Ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients by the diode tracks the current-voltage characteristic curve for the diode. A typical current-voltage curve for the SN74S1050/S1052 is shown in Figure 1.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 2 was evaluated. The resulting waveforms with and without the diode are shown in Figure 3.

The maximum effectiveness of the diode in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

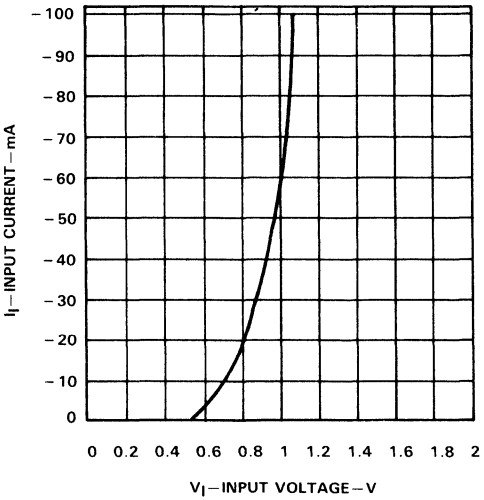


FIGURE 1. TYPICAL CURRENT-VOLTAGE CURVE

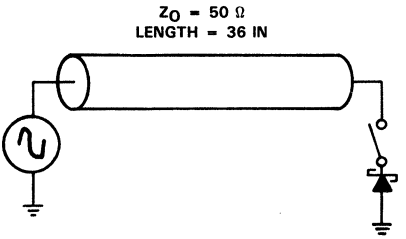
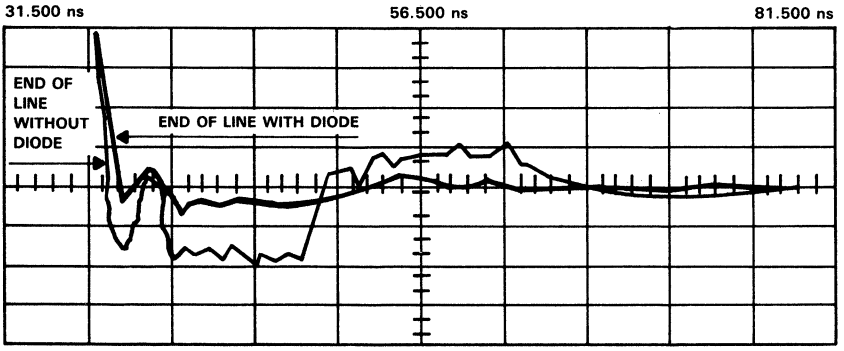


FIGURE 2. DIODE TEST SETUP



Y-COORDINATE = 1,800 VOLTS/DIV
TIMEBASE = 5.00 ns/VOLT
VMARKER 1 = −1.353 VOLTS
VMARKER 2 = −3.647 VOLTS

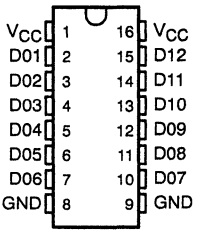
OFFSET = 0.000 VOLTS
DELAY = 56.500 ns
DELTA V = −2.293 VOLTS

FIGURE 3. SCOPE DISPLAY

D3423, SEPTEMBER 1990

- **Designed to Reduce Reflection Noise**
- **Repetitive Peak Forward Current . . . 200 mA**
- **12-Bit Array Structure Suited for Bus-Oriented Systems**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

SN74S1051 . . . D OR N PACKAGE
(TOP VIEW)

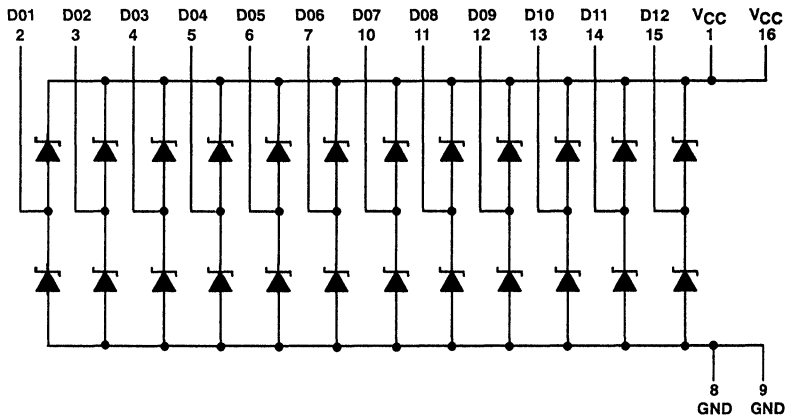


description

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 12-bit high-speed Schottky diode array suitable for clamping to V_{CC} and/or GND.

The 74S1051 is characterized for operation from 0°C to 70°C.

schematic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, V_R ..... 7 V
Continuous forward current, I_F: any D terminal from GND or to V_{CC} ..... 50 mA
total through all GND or V_{CC} terminals ..... 170 mA
Repetitive peak forward current‡, I_{FRM}: any D terminal from GND or to V_{CC} ..... 200 mA
total through all GND or V_{CC} terminals ..... 1 A
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 1) ..... 625 mW
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ These values apply for $t_w \leq 100\ \mu s$, duty cycle ≤ 20%.

NOTE 1: For operation above 25°C free-air temperature, derate linearly at the rate of 5 mW/°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
V_F	Static forward voltage	To V_{CC}	I_F = 18 mA		0.85	1.05	V
			I_F = 50 mA		1.05	1.3	
		From GND	I_F = 18 mA		0.75	0.95	V
			I_F = 50 mA		0.95	1.2	
V_{FM}	Peak forward voltage		I_F = 200 mA		1.45		V
I_R	Static reverse current	To V_{CC}	V_R = 7 V			5	μA
		From GND				5	
C_T	Total capacitance	V_R = 0,	f = 1 MHz		8	16	pF
		V_R = 2 V,	f = 1 MHz		4	8	

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open circuited during the measurement of these characteristics.

multiple-diode operation

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
I_X	Internal crosstalk current	Total I_F = 1 A,	See Note 3		0.8	2	mA
		Total I_F = 198 mA,	See Note 3		0.02	0.2	

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 3: I_X is measured under the following conditions with one diode static and all others switching: switching diodes: t_w = 100 μs, duty cycle = 0.2; static diode: V_R = 5 V. The static diode's input current is the internal crosstalk current I_X.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse recovery time	I_F = 10 mA, $I_{RM(REC)}$ = 10 mA, $i_{R(REC)}$ = 1 mA, R_L = 100 Ω		8	16	ns

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION INFORMATION

Large transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc), or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74S1051 and SN74S1053 diode termination arrays help suppress transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to Ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce transients, but they can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of transients is tracked by the current-voltage characteristic curve for that diode. Typical current-voltage curves for the SN74S1051 / S1053 are shown in Figures 1 and 2.

To illustrate how the diode arrays act to reduce transients at the end of a transmission line, the test setup in Figure 3 was evaluated. The resulting waveforms with and without the diode are shown in Figure 4.

The maximum effectiveness of the diode arrays in suppressing transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

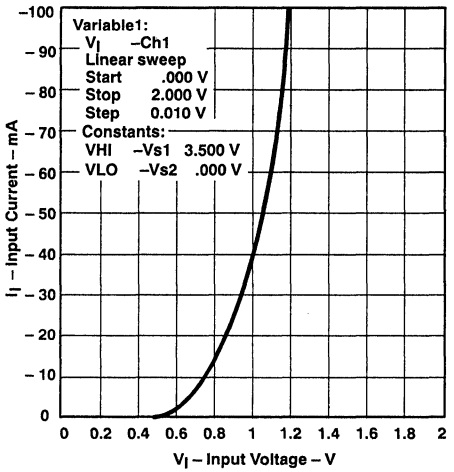


Figure 1. Typical Input Current vs Input Voltage (Lower Diode)

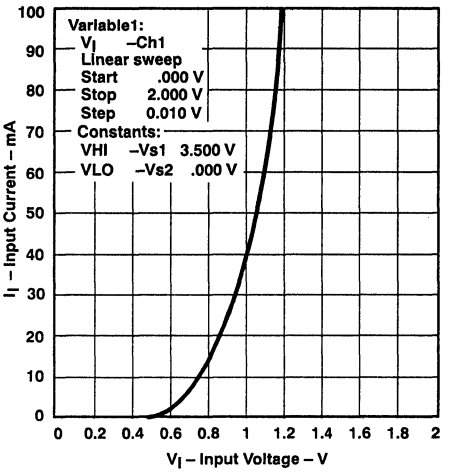


Figure 2. Typical Input Current vs Input Voltage (Upper Diode)

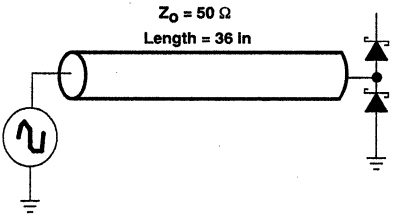


Figure 3. Diode Test Setup

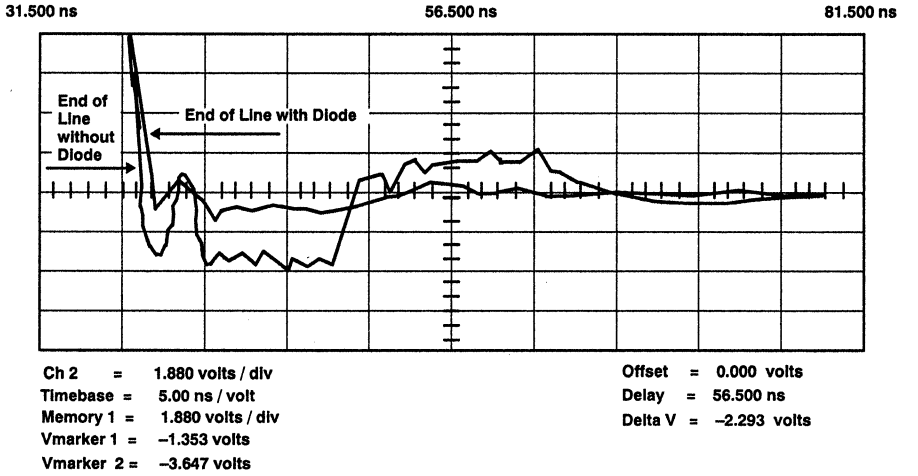


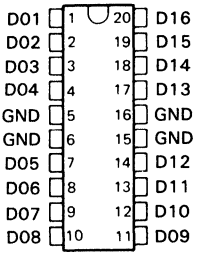
Figure 4. Scope Display

16-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

D3229, JULY 1989—REVISED MARCH 1990

- **Designed to Reduce Reflection Noise**
- **Repetitive Peak Forward Current . . . 200 mA**
- **16-Bit Array Structure Suited for Bus-Oriented Systems**
- **ESD Protection Exceeds 10 kV Per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)

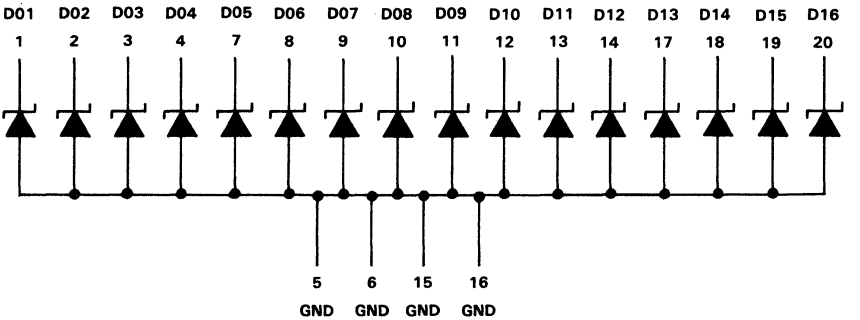


description

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 16-bit high-speed Schottky diode array suitable for a clamp to GND.

The SN74S1052 is characterized for operation from 0°C to 70°C.

schematic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, V_R . . . . . 7 V
Continuous forward current, I_F: any D terminal from GND . . . . . 50 mA
total through all GND terminals . . . . . 170 mA
Repetitive peak forward current,‡ I_{FRM}: any D terminal from GND . . . . . 200 mA
total through all GND terminals . . . . . 1 A
Continuous total power dissipation at (or below) 25°C free-air temperature . . . . . 735 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡These values apply for $t_w \leq 100\ \mu s$, duty cycle ≤ 20%.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
I_R	Static reverse current	V_R = 7 V				5	μA
V_F	Static forward voltage	I_F = 18 mA			0.75	0.95	V
		I_F = 50 mA			0.95	1.2	
V_{FM}	Peak forward voltage	I_F = 200 mA			1.45		V
C_T	Total capacitance	V_R = 0,	f = 1 MHz		5	10	pF
		V_R = 2 V,	f = 1 MHz		4	8	

NOTE 1: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
I_X	Internal crosstalk current	Total I_F = 1 A,	See Note 2		0.6	2	mA
		Total I_F = 270 mA,	See Note 2		0.02	0.2	

§All typical values are at T_A = 25°C.
NOTE 2: I_X is measured under the following conditions with one diode static and all others switching:
Switching diodes: t_w = 100 μs, duty cycle = 20%; static diode: V_R = 5 V.
The static diode's input current is the internal crosstalk current I_X.

switching characteristics at 25°C free-air temperature (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse recovery time	I_F = 10 mA, $I_{RM(REC)}$ = 10 mA, $I_{R(REC)}$ = 1 mA, R_L = 100 Ω		8	16	ns

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.), or on the CLOCK lines of many clocked devices can result in improper operation of the device. The SN74S1050 and SN74S1052 diode termination arrays help suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients by the diode tracks the current-voltage characteristic curve for the diode. A typical current-voltage curve for the SN74S1050/S1052 is shown in Figure 1.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 2 was evaluated. The resulting waveforms with and without the diode are shown in Figure 3.

The maximum effectiveness of the diode in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

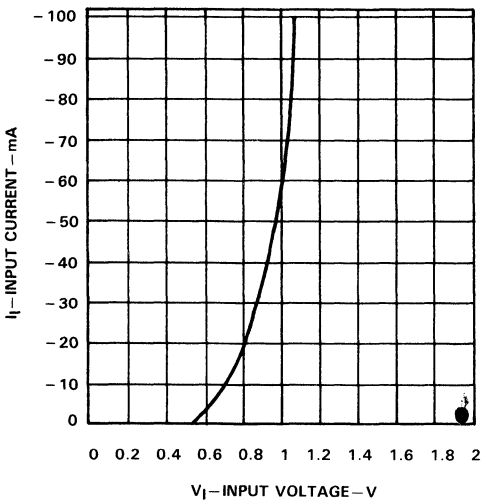


FIGURE 1. TYPICAL CURRENT-VOLTAGE CURVE

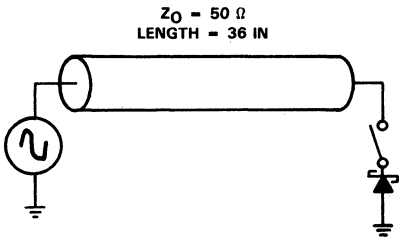
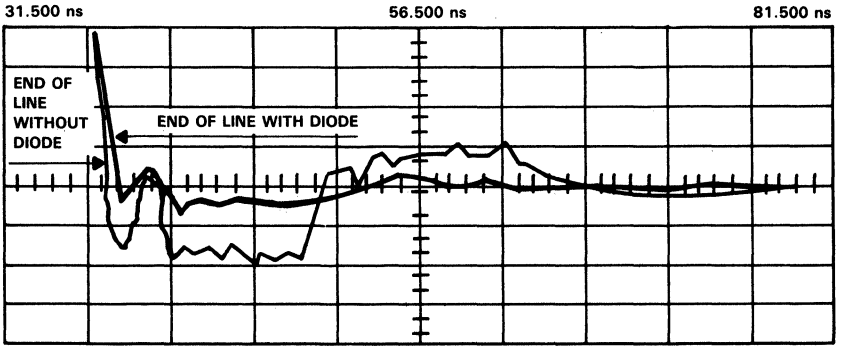


FIGURE 2. DIODE TEST SETUP



Y-COORDINATE = 1,800 VOLTS/DIV
TIMEBASE = 5.00 ns/VOLT
VMARKER 1 = −1.353 VOLTS
VMARKER 2 = −3.647 VOLTS

OFFSET = 0.000 VOLTS
DELAY = 56.500 ns
DELTA V = −2.293 VOLTS

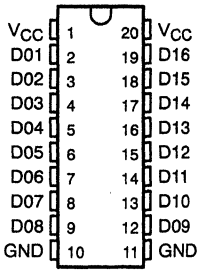
FIGURE 3. SCOPE DISPLAY

D3424, SEPTEMBER 1990

- **Designed to Reduce Reflection Noise**
- **Repetitive Peak Forward Current . . . 200 mA**
- **16-Bit Array Structure Suited for Bus-Oriented Systems**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE

(TOP VIEW)

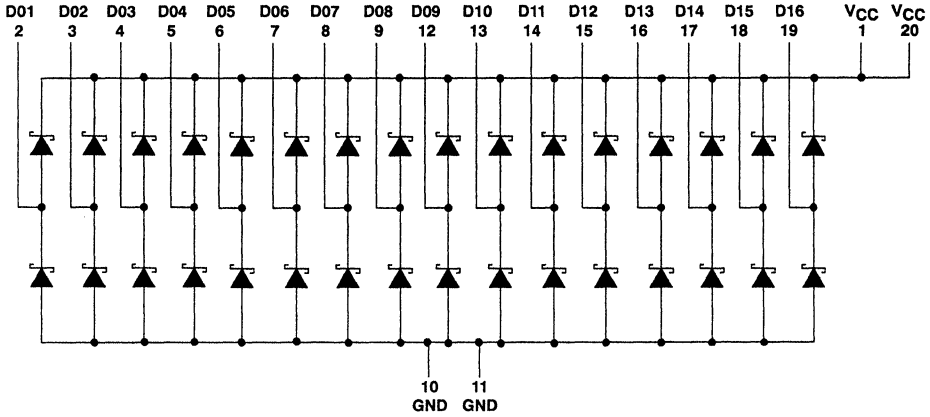


description

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 16-bit high-speed Schottky diode array suitable for clamping to V_{CC} and/or GND.

The 74S1053 is characterized for operation from 0°C to 70°C.

schematic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, V_R ..... 7 V
Continuous forward current, I_F: any D terminal from GND or to V_{CC} ..... 50 mA
total through all GND or V_{CC} terminals ..... 170 mA
Repetitive peak forward current‡, I_{FRM}: any D terminal from GND or to V_{CC} ..... 200 mA
total through all GND or V_{CC} terminals ..... 1 A
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 1) ..... 625 mW
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ These values apply for $t_w \leq 100\ \mu s$, duty cycle ≤ 20%.

NOTE 1: For operation above 25°C free-air temperature, derate linearly at the rate of 5 mW/°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
V_F	Static forward voltage	To V_{CC}	I_F = 18 mA		0.85	1.05	V
			I_F = 50 mA		1.05	1.3	
		From GND	I_F = 18 mA		0.75	0.95	V
			I_F = 50 mA		0.95	1.2	
V_{FM}	Peak forward voltage		I_F = 200 mA		1.45		V
I_R	Static reverse current	To V_{CC}	V_R = 7 V			5	μA
		From GND				5	
C_T	Total capacitance	V_R = 0,	f = 1 MHz		8	16	pF
		V_R = 2 V,	f = 1 MHz		4	8	

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open circuited during the measurement of these characteristics.

multiple-diode operation

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
I_X	Internal crosstalk current	Total I_F = 1 A,	See Note 3		0.8	2	mA
		Total I_F = 198 mA,	See Note 3		0.02	0.2	

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 3: I_X is measured under the following conditions with one diode static and all others switching: switching diodes: t_w = 100 μs, duty cycle = 0.2; static diode: V_R = 5 V. The static diode's input current is the internal crosstalk current I_X.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse recovery time	I_F = 10 mA, $I_{RM(REC)}$ = 10 mA, $i_{R(REC)}$ = 1 mA, R_L = 100 Ω		8	16	ns

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION INFORMATION

Large transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc), or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74S1051 and SN74S1053 diode termination arrays help suppress transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to Ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce transients, but they can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of transients is tracked by the current-voltage characteristic curve for that diode. Typical current-voltage curves for the SN74S1051 / S1053 are shown in Figures 1 and 2.

To illustrate how the diode arrays act to reduce transients at the end of a transmission line, the test setup in Figure 3 was evaluated. The resulting waveforms with and without the diode are shown in Figure 4.

The maximum effectiveness of the diode arrays in suppressing transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

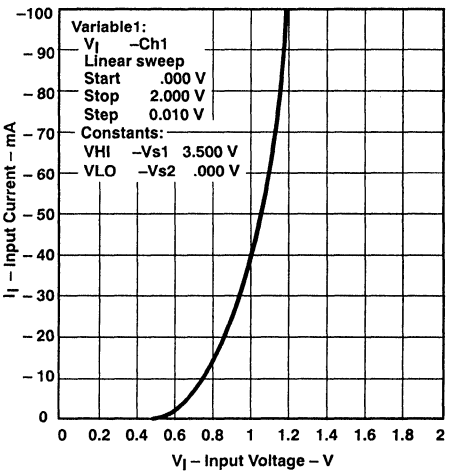


Figure 1. Typical Input Current vs Input Voltage (Lower Diode)

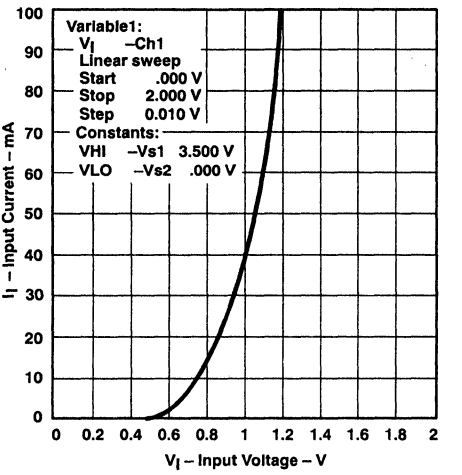


Figure 2. Typical Input Current vs Input Voltage (Upper Diode)

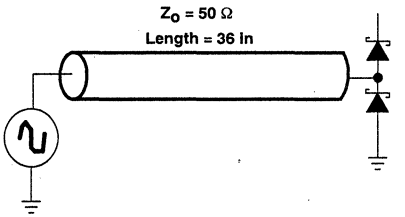


Figure 3. Diode Test Setup

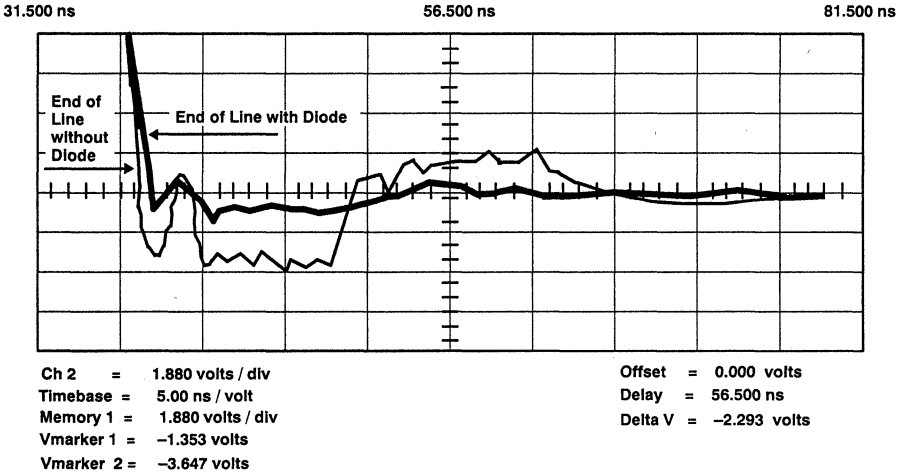


Figure 4. Scope Display

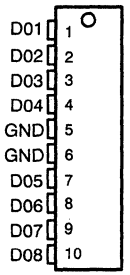
- **Designed to Reduce Reflection Noise**
- **Repetitive Peak Forward Current . . . 300 mA**
- **8-Bit Array Structure Suited for Bus-Oriented Systems**

description

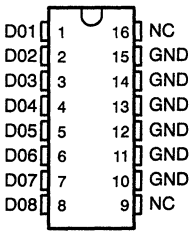
This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of an 8-bit high-speed Schottky diode array suitable for GND clamp.

The SN74S1056 is characterized for operation from 0°C to 70°C.

SC PACKAGE
(TOP VIEW)

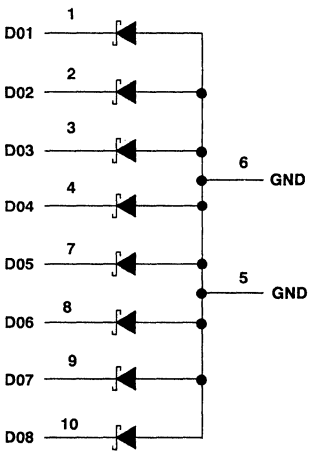


D PACKAGE
(TOP VIEW)

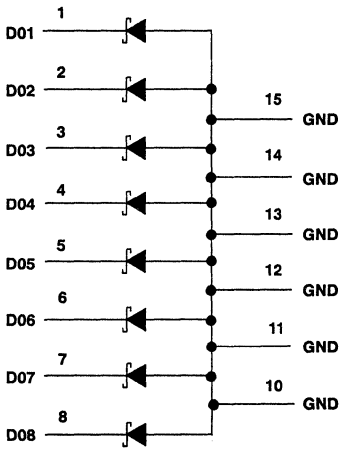


schematic diagrams

(SC PACKAGE)



(D PACKAGE)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady state reverse voltage, V_R ..... 7 V
Continuous forward current, I_F: any D terminal from GND ..... 50 mA
total through all GND terminals ..... 170 mA
Repetitive peak forward current, I_{FRM}‡: any D terminal from GND ..... 300 mA
total through all GND terminals ..... 1.2 A
Continuous total power dissipation at (or below) 25°C free-air temperature ..... 1000 mW
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ These values apply for $t_w \leq 100\ \mu s$, duty cycle ≤ 20%.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
I_R	Static reverse current	V_R = 7 V				10	μA
V_F	Static forward voltage	I_F = 18 mA			0.65	0.85	V
		I_F = 50 mA			0.8	1	
V_{FM}	Peak forward voltage	I_F = 300 mA			1.41		V
C_T	Total capacitance	V_I = 0 V,	f = 1 MHz		11	13	pF
		V_I = 2 V,	f = 1 MHz		8	11	

NOTE 1: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
I_X	Internal crosstalk current	Total GND current = 1.2 A,	See Note 2		0.6	2	mA
		Total GND current = 126 mA,	See Note 2		0.01	0.1	mA

§ All typical values are at T_A = 25°C.
NOTE 2: I_X is measured under the following conditions with one diode static, all others switching:
Switching diodes: t_w = 100 μs, duty cycle = 20%;
Static diode: V_R = 5 V
The static diode input current is the internal crosstalk current I_X.

switching characteristics, T_A = 25°C (see Note 3)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse recovery time	I_F = 10 mA, $I_{RM(REC)}$ = 10 mA, $I_{R(REC)}$ = 1 mA, R_L = 100 Ω		5	10	ns

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74S1056 diode termination array helps suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to Ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but they can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. A typical current-voltage for the SN74S1056 is shown in Figure 1.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 2(a) was evaluated. The resulting waveforms with and without the diode are shown in Figure 2(b).

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

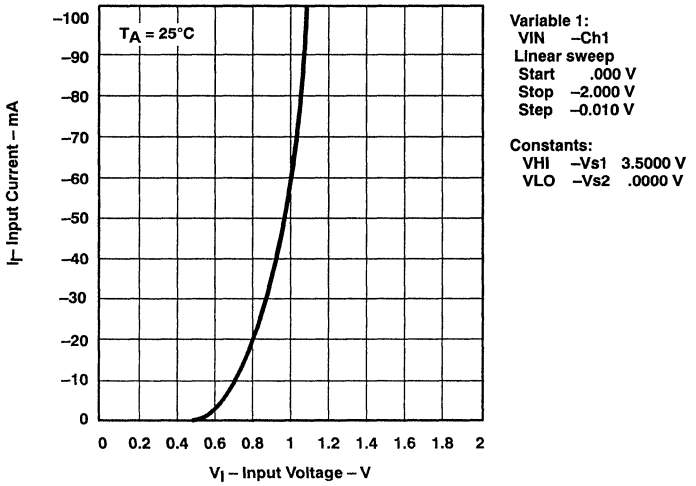
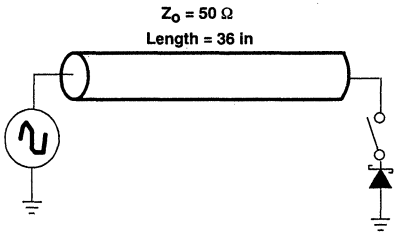
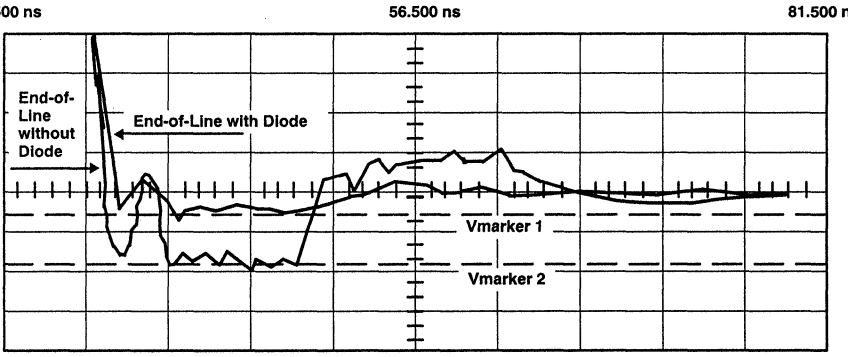


Figure 1. Typical Current-Voltage Curve



(a) DIODE TEST SETUP



Ch 2 = 1.880 volts / div
Timebase = 5.00 ns / volt
Memory 1 = 1.880 volts / div
Vmarker 1 = –1.353 volts
Vmarker 2 = –3.647 volts

Offset = 0.000 volts
Delay = 56.500 ns
Delta V = –2.293 volts

(b) SCOPE DISPLAY

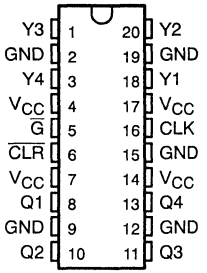
Figure 2. Diode Test Setup and Scope Display

6 Clock Driver Products

D3589, MAY 1990

- **Low Output Skew, Low Pulse Skew for Clock Distribution and Clock Generation Applications**
- **Four Outputs Toggle at the Clock Frequency, Four Outputs Switch at One-Half the Clock Frequency**
- **Advanced BiCMOS Design With TTL-Voltage-Compatible Inputs and Outputs**
- **f_{max} = 80 MHz**
- **High-Drive Outputs Eliminate the Need for External Buffering**
- **State-of-the-Art EPIC™-IIB BiCMOS Design Significantly Reduces Power Dissipation**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **Package Options Include Plastic "Small Outline" Packages and 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

The 'ABT337 contains four buffered outputs that switch at the clock frequency and four divide-by-two outputs that switch at one-half the clock frequency. When $\overline{G}$ is low and $\overline{CLR}$ is high, the Y outputs follow the CLK input and the Q outputs switch on the low-to-high transition of CLK.

This clock driver is specifically designed for applications requiring synchronized output signals at both the clock frequency and one-half the clock frequency. Taking $\overline{CLR}$ low asynchronously resets the Q outputs to a low level. High-drive outputs (± 48 mA) eliminate the need for external buffering of output signals.

The SN74ABT337 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{G}$	$\overline{CLR}$	CLK	Y1-Y4	Q1-Q4
H	X	X	Z	Z
L	L	L	L	L
L	L	H	H	L
L	H	L	L	Q_0
L	H	H	H	Q_0
L	H	↑	↑	toggle

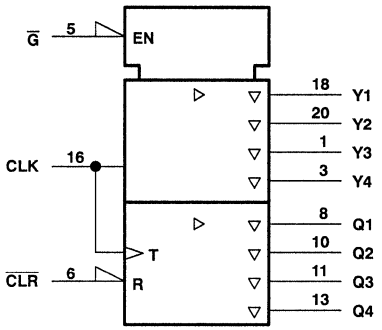
Q_0 = the level at the Q outputs after the most recent low-to-high transition of CLK.

PRODUCT PREVIEW

EPIC-IIB is a trademark of Texas Instruments Incorporated.

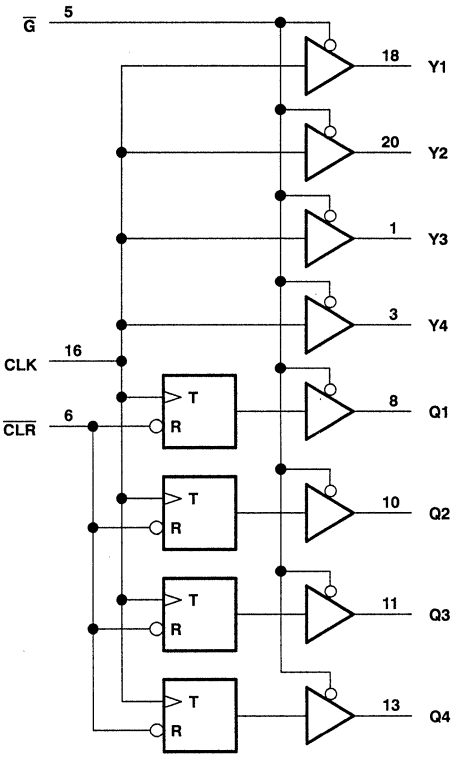
D3589, MAY 1990

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Input voltage range, V_I ..... – 0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state, V_O ..... – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... – 18 mA
Current into any output in the low state, I_O ..... 96 mA
Storage temperature range ..... – 65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		– 48	mA
I_{OL}	Low-level output current		48	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = – 18 mA				– 1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 48 mA		3.5			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.5	V
I_{OZ}	V_{CC} = 5.5 V						μA
I_I	V_{CC} = 5.5 V						μA
I_{CC}	V_{CC} = 5.5 V,	V_I = V_{CC} or GND,	I_O = 0	Outputs high			mA
				Outputs low			
				Outputs disabled			
C_i	V_I = V_{CC} or GND				5.5		pF
C_o	V_O = V_{CC} or GND						pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (see Note 1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	80	MHz
t_w	Pulse duration	$\overline{CLR}$ low			ns
		CLK high or low	4		
t_{su}	Setup time, $\overline{CLR}$ inactive before CLK↑				ns

switching characteristics over recommended operating free-air temperature range (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			80		MHz
t_{PLH}	CLK	Any Y or Q			ns
t_{PHL}					
t_{PHL}	$\overline{CLR}$	Any Q			ns
t_{PZH}	$\overline{G}$	Any Y or Q			ns
t_{PZL}					
t_{PHZ}	$\overline{G}$	Any Y or Q			ns
t_{PLZ}					
$t_{sk(o)}$	CLK	Any Y or Q			ns
$t_{sk(p)}$					

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

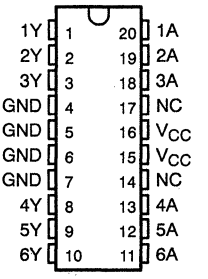
PRODUCT PREVIEW

D3427, OCTOBER 1989

- **Low-Skew Propagation Delay Specifications for Clock Driver Applications**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE

(TOP VIEW)



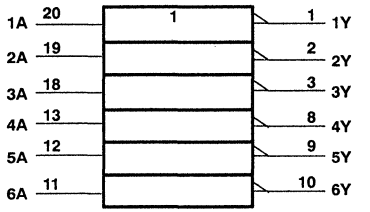
description

This device contains six independent inverters. They perform the Boolean function $Y = \overline{A}$.

The 74AC11204 is designed specifically for applications requiring low skew between switching outputs.

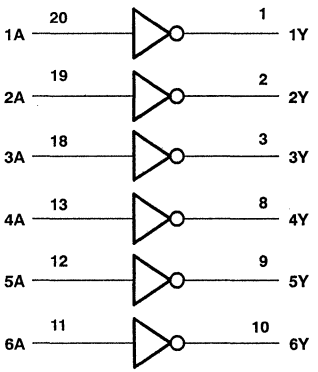
The 74AC11204 is characterized for operation from 25°C to 70°.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50mA
Continuous current through V_{CC} or GND pins ..... ±150mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	V_{CC} = 4.75 V	3.3			V
		V_{CC} = 5.25 V	3.7			
V_{IL}	Low-level input voltage	V_{CC} = 4.75 V			1.4	V
		V_{CC} = 5.25 V			1.6	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 4.75 V			−24	mA
		V_{CC} = 5.25 V			−24	
I_{OL}	Low-level output current	V_{CC} = 4.75 V			24	mA
		V_{CC} = 5.25 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		25		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA	4.75 V	4.65			4.65		V
		5.25 V	5.15			5.15		
	I_{OH} = – 24 mA	4.75 V	4.19			4.05		
		5.25 V	4.69			4.55		
	I_{OH} = – 75 mA†	5.25 V				3.6		
V_{OL}	I_{OL} = 50 μA	4.75 V			0.1		0.1	V
		5.25 V			0.1		0.1	
	I_{OL} = 24 mA	4.75 V			0.36		0.44	
		5.25 V			0.36		0.44	
	I_{OL} = 75 mA†	5.25 V					1.65	
I_I	$V_I = V_{CC}$ or GND	5.25 V			± 0.1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.25 V			4		40	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4				pF

† Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.

switching characteristics, T_A = 25°C to 70°C, V_{CC} = 5 V ± 0.25 V (see Notes 2 and 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	A	Y	3.7	5.7	ns
t_{PHL}			3.7	5.7	
$t_{sk(o)}$	A	Y		1	ns

NOTES: 2. All specifications are valid only for all outputs switching simultaneously and in phase.
3. Load circuit and voltage waveforms are shown in Section 1.

- **Low Skew Propagation Delay Specifications for Clock Driving Applications**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

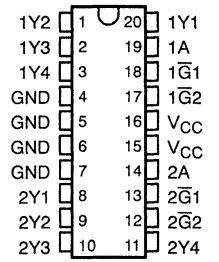
description

These devices contain dual-clock driver circuits that fan out one input signal to four outputs with minimum skew for clock distribution. They also offer two output-enable pins for each circuit that can force the outputs to be disabled to a high-impedance state or to a high- or low-logic level independent of the signal on the A input.

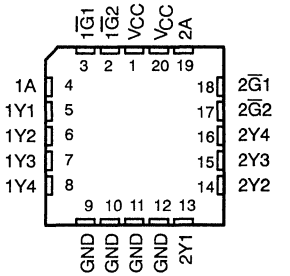
Skew parameters are specified for a reduced temperature and voltage range common to many applications.

The 54AC11208 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11208 is characterized for operation from – 40°C to 85°C.

54AC11208 . . . J PACKAGE
74AC11208 . . . DW OR N PACKAGE
(TOP VIEW)



54AC11208 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLES

OUTPUT CONTROL		DATA INPUT	OUTPUTS			
1G1	1G2	1A	1Y1	1Y2	1Y3	1Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

OUTPUT CONTROL		DATA INPUT	OUTPUTS			
2G1	2G2	2A	2Y1	2Y2	2Y3	2Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

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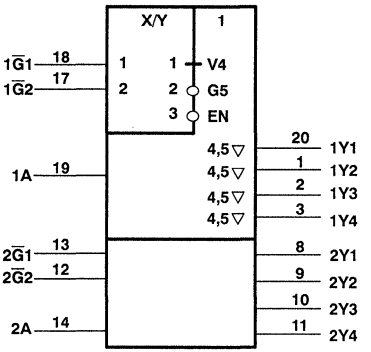
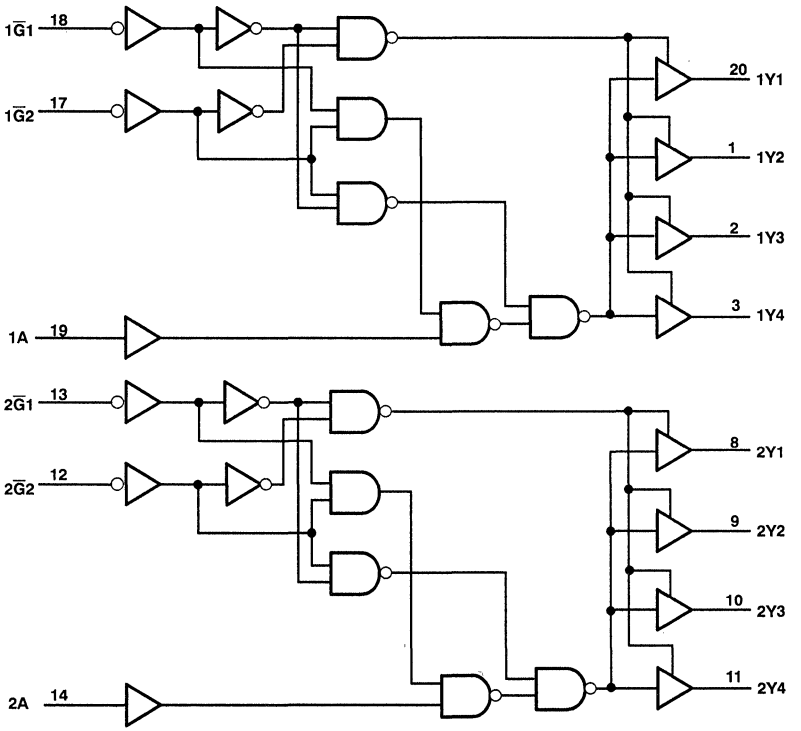
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND pins ..... ± 200 mA
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11208			74AC11208			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			– 4			– 4	mA
		V_{CC} = 4.5 V			– 24			– 24	
		V_{CC} = 5.5 V			– 24			– 24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		– 55		125	– 40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11208		74AC11208		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_I = V_{CC}$ or GND	5.5 V			± 0.5		± 10		± 5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4						pF
C_o	$V_I = V_{CC}$ or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11208		74AC11208		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	1A and 2A	Any Y	4.8	11.1	13.1	4.8	15.6	4.8	14.6	ns
t_{PHL}			5.1	12.2	14.3	5.1	16.7	5.1	15.6	
t_{PLH}	$1\overline{G}n$ and $2\overline{G}n$	Any Y	5.2	11.9	14.2	5.2	16.9	5.2	15.8	ns
t_{PHL}			7.8	13.3	15.7	7.8	18.4	7.8	17.4	
t_{PZH}	$1\overline{G}2$ or $2\overline{G}2$	Any Y	5.1	11.8	14.2	5.1	17.2	5.1	15.7	ns
t_{PZL}	$1\overline{G}1$ or $2\overline{G}1$		6.8	16.3	19.5	6.8	23.8	6.8	22.8	
t_{PHZ}	$1\overline{G}2$ or $2\overline{G}2$	Any Y	3.4	6.9	8.6	3.4	9.6	3.4	9.2	ns
t_{PLZ}	$1\overline{G}1$ or $2\overline{G}1$		4.1	7.5	9.4	4.1	10.5	4.1	10.2	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11208		74AC11208		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	1A and 2A	Any Y	4.2	5.5	9	4.2	10.5	4.2	9.9	ns
t_{PHL}			4.2	7	9.3	4.2	10.8	4.2	10.1	
t_{PLH}	$1\overline{G}n$ and $2\overline{G}n$	Any Y	4.6	7.3	9.6	4.6	11.5	4.6	10.7	ns
t_{PHL}			4.8	7.7	10.2	4.8	11.8	4.8	11	
t_{PZH}	$1\overline{G}2$ or $2\overline{G}2$	Any Y	4.3	7.2	9.4	4.3	11.3	4.3	10.4	ns
t_{PZL}	$1\overline{G}1$ or $2\overline{G}1$		5.3	9	12.2	5.3	14.3	5.3	13.5	
t_{PHZ}	$1\overline{G}2$ or $2\overline{G}2$	Any Y	3	5.4	7.5	3	8.5	3	8	ns
t_{PLZ}	$1\overline{G}1$ or $2\overline{G}1$		3.7	5.7	7.5	3.7	8.5	3.7	8.2	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics, V_{CC} = 5 V ± 0.25 V, T_A = 25°C to 70°C (see Notes 2 and 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	74ACT11208			UNIT
			MIN	TYP	MAX	
t_{PLH}	1A and 2A	Any Y	6		8.5	ns
t_{PHL}			6		8.5	
$t_{sk(o)}$	1A and 2A	Any Y			1	ns

NOTES: 2. Load circuit and voltage waveforms are shown in Section 1.
3. Specifications are valid for all outputs switching simultaneously and in-phase.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per bank	Outputs enabled	C_L = 50 pF, f = 1 MHz	95	pF
		Outputs disabled		10	

- **Inputs are TTL-Voltage Compatible**
- **Low-Skew Propagation Delay Specifications for Clock Driver Applications**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

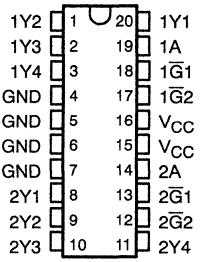
description

These devices contain dual-clock driver circuits that fan out one input signal to four outputs with minimum skew for clock distribution. They also offer two output-enable pins for each circuit that can force the outputs to be disabled to a high-impedance state or to a high- or low-logic level independent of the signal on the A input.

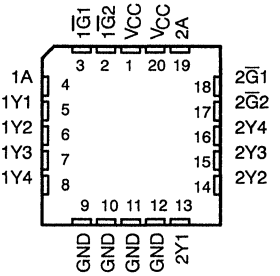
Skew parameters are specified for a reduced temperature and voltage range common to many applications.

The 54ACT11208 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11208 is characterized for operation from – 40°C to 85°C

54ACT11208 . . . J PACKAGE
74ACT11208 . . . DW OR N PACKAGE
(TOP VIEW)



54ACT11208 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLES

OUTPUT CONTROL		DATA INPUT	OUTPUTS			
$1\overline{G}1$	$1\overline{G}2$	1A	1Y1	1Y2	1Y3	1Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

OUTPUT CONTROL		DATA INPUT	OUTPUTS			
$2\overline{G}1$	$2\overline{G}2$	2A	2Y1	2Y2	2Y3	2Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

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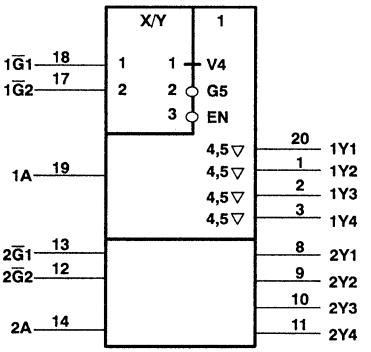
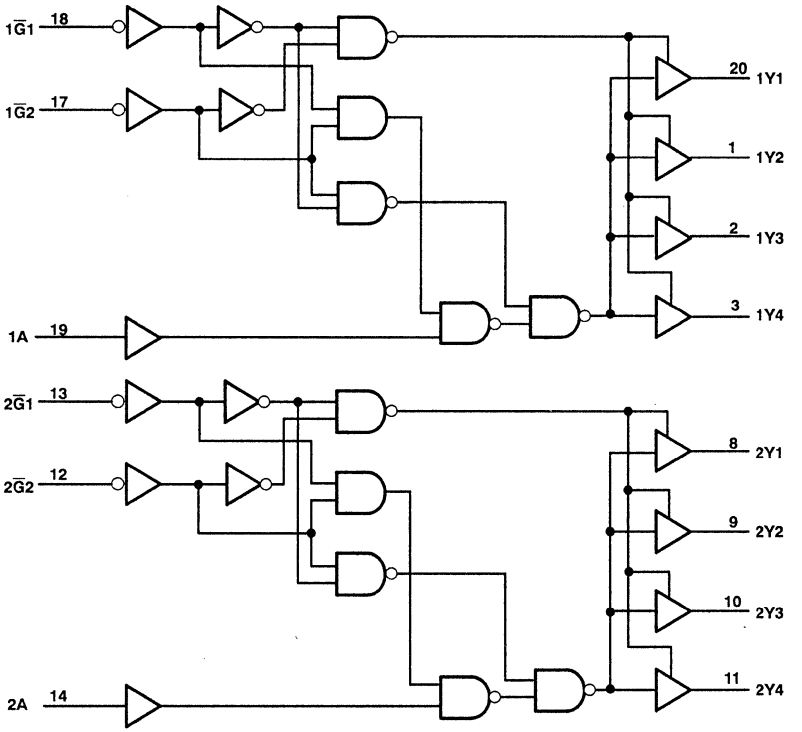
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50mA
Continuous current through V_{CC} or GND pins ..... ±200mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11208		74ACT11208		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11208		74ACT11208		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			± 0.5		± 10		± 5	μA
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11208		74ACT11208		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	1A and 2A	Any Y	5.3	8.5	10.9	5.3	12.6	5.3	11.7	ns
t_{PHL}			3.6	7.7	11	3.6	12.1	3.6	11.5	
t_{PLH}	1$\overline{G}$n and 2$\overline{G}$n	Any Y	4.7	8.5	11.7	4.7	13.7	4.7	12.8	ns
t_{PHL}			4.4	8.4	11.3	4.4	13.2	4.4	12.4	
t_{PZH}	1$\overline{G}$2 or 2$\overline{G}$2	Any Y	4.4	8.1	11.3	4.4	13.2	4.4	12.4	ns
t_{PZL}	1$\overline{G}$1 or 2$\overline{G}$1		5	9.6	13.3	5	16.1	5	14.9	
t_{PHZ}	1$\overline{G}$2 or 2$\overline{G}$2	Any Y	4.2	7.4	9.3	4.2	10.7	4.2	10.2	ns
t_{PLZ}	1$\overline{G}$1 or 2$\overline{G}$1		5.4	7.5	9.2	5.4	10.3	5.4	9.9	

switching characteristics, V_{CC} = 5 V ± 0.25 V, T_A = 25°C to 70°C (see Notes 2 and 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	74ACT11208			UNIT
			MIN	TYP	MAX	
t_{PLH}	1A and 2A	Any Y	7.6		10.2	ns
t_{PHL}	1A and 2A	Any Y	6.6		9.8	ns
$t_{sk(o)}$	1A and 2A	Any Y			1	ns

NOTES: 2. Load circuit and voltage waveforms are shown in Section 1.
3. Specifications are valid for all outputs switching simultaneously and in-phase.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per bank	Outputs enabled	C_L = 50 pF, f = 1 MHz	96	pF
		Outputs disabled		12	

D3590, JULY 1990

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

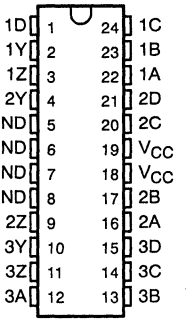
The 'AC11800 contains three independent 4-input AND/NAND gates. They perform the Boolean functions in positive logic $Y = ABCD$ and $Z = \overline{ABCD}$. These devices are designed to have low skew between outputs for clock driver applications.

The 54AC11800 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11800 is characterized for operation from – 40°C to 85°C.

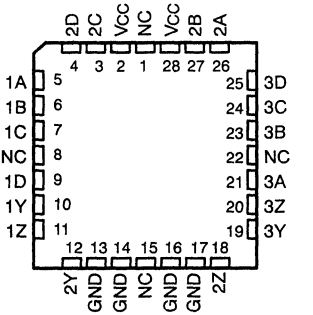
FUNCTION TABLE

INPUTS				OUTPUTS	
A	B	C	D	Y	Z
L	X	X	X	L	H
X	L	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
H	H	H	H	H	L

54AC11800 . . . JT PACKAGE
74AC11800 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11800 . . . FK PACKAGE
(TOP VIEW)



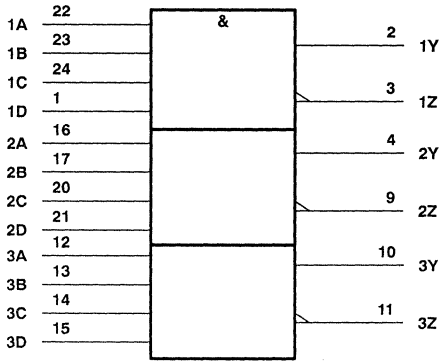
NC–No internal connection

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

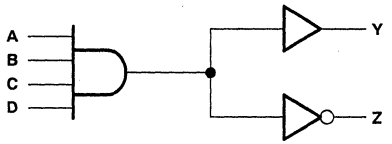
D3590, JULY 1990

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram, each section (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50mA
Continuous current through V_{CC} or GND pins ..... ± 150mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions

			54AC11800			74AC11800			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			– 4			– 4	mA
		V_{CC} = 4.5 V			– 24			– 24	
		V_{CC} = 5.5 V			– 24			– 24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		– 55		125	– 40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11800		74AC11800		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.4		2.28		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11800		74AC11800		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	5.6	9.4	1.5	11.3	1.5	10.6	ns
t_{PHL}			1.5	5.1	7.4	1.5	8.7	1.5	8.2	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11800		74AC11800		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	3.8	6.8	1.5	8	1.5	7.6	ns
t_{PHL}			1.5	3.8	6.2	1.5	7.3	1.5	6.8	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

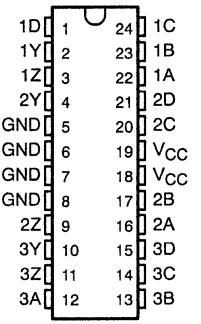
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF,	f = 1 MHz	27	pF

PRODUCT PREVIEW

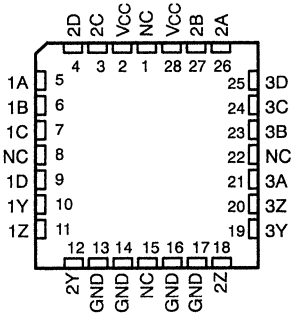
D3591, JULY 1990

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **500-mA Typical Latch-up Immunity at 125°C**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11800 . . . JT PACKAGE
74ACT11800 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11800 . . . FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

The 'ACT11800 contains three independent 4-input AND/NAND gates. They perform the Boolean functions in positive logic Y = ABCD and Z = $\overline{ABCD}$. These devices are designed to have low skew between outputs for clock driver applications.

The 54ACT11800 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11800 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

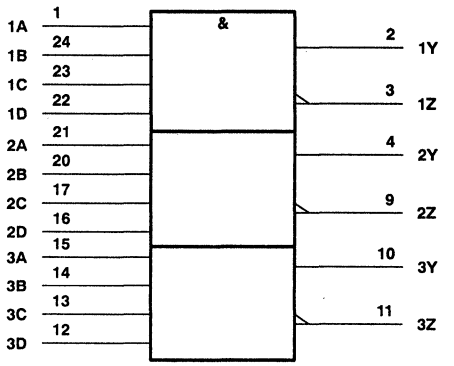
INPUTS				OUTPUTS	
A	B	C	D	Y	Z
L	X	X	X	L	H
X	L	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
H	H	H	H	H	L

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

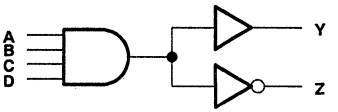
D3591, JULY 1990

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic) (one section)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50mA
Continuous current through V_{CC} or GND pins ..... ±150mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11800		74ACT11800		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2			2	V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

PRODUCT PREVIEW

D3591, JULY 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11800		74ACT111800		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 0.1		± 0.1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11800		74ACT11800		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y		3.8						ns
t_{PHL}				3.8						

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, TA = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF,	f = 1 MHz	27	pF

PRODUCT PREVIEW

D3593, JULY 1990

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

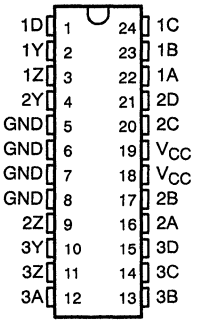
The 'AC11802 contains three independent 4-input AND/NAND gates. They perform the Boolean functions in positive logic $Y = A + B + C + D$ and $Z = \overline{A + B + C + D}$. These devices are designed to have low skew between outputs for clock driver applications.

The 54AC11802 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11802 is characterized for operation from – 40°C to 85°C.

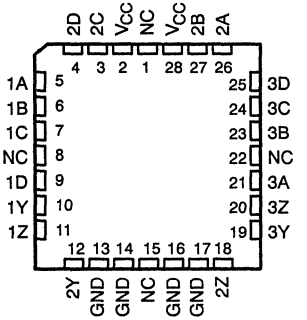
FUNCTION TABLE

INPUTS				OUTPUTS	
A	B	C	D	Y	Z
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	L	H

54AC11802 . . . JT PACKAGE
74AC11802 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11802 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

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TEXAS INSTRUMENTS
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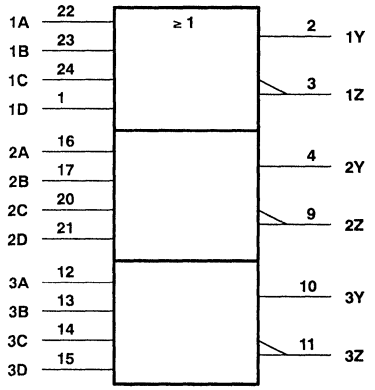
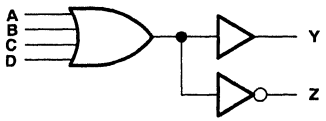
D3593, JULY 1990

logic symbol†



logic diagram (positive logic) (one section)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50mA
Continuous current through V_{CC} or GND pins ..... ± 150mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions

			SN54AC11802			SN74AC11802			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11802		74AC11802		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.28		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11802		74AC11802		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y		5.6						ns
t_{PHL}				5.1						

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11802		74AC11802		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y		3.8						ns
t_{PHL}				3.8						

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, TA = 25°C

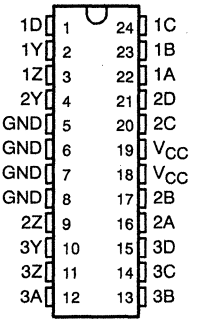
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	27	pF

PRODUCT PREVIEW

D3594, JULY 1990

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11802 . . . JT PACKAGE
74ACT11802 . . . DW OR NT PACKAGE
(TOP VIEW)

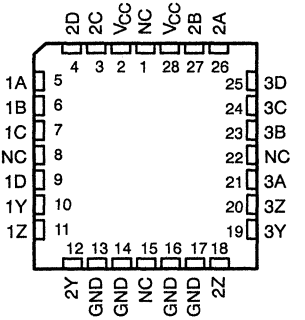


description

The 'ACT11802 contains three independent 4-input AND/NAND gates. They perform the Boolean functions in positive logic $Y = A + B + C + D$ and $Z = \overline{A + B + C + D}$. These devices are designed to have low skew between outputs for clock driver applications.

The 54ACT11802 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT11802 is characterized for operation from –40°C to 85°C.

54ACT11802 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
A	B	C	D	Y	Z
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	L	H

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

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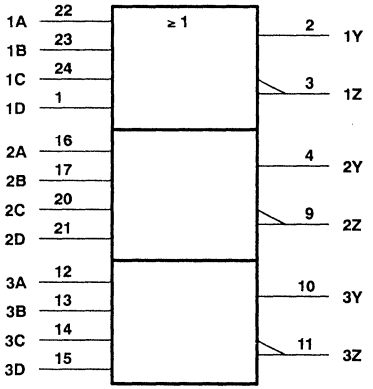
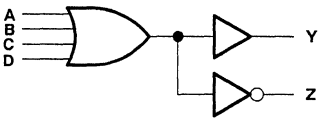
D3594, JULY 1990

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Pulbication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic) (one section)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ± 50 mA
Continuous current through V_{CC} or GND pins . . . . . ± 150 mA
Storage temperature range . . . . . – 65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11802		74ACT11802		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2			2	V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		– 24		– 24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
TA	Operating free-air temperature	– 55	125	– 40	85	°C

PRODUCT PREVIEW

D3594, JULY 1990

electrical characteristics over recomended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11802		74ACT11802		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA †	5.5 V				3.85				
	I_{OH} = – 75 mA †	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA †	5.5 V					1.65			
	IOL = 75 mA †	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 0.1		± 0.1	mA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	mA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF

† Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather that 0 V to V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11802		74AC11802		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y		3.8						ns
t_{PHL}				3.8						

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	27	pF

PRODUCT PREVIEW

TEXAS INSTRUMENTS
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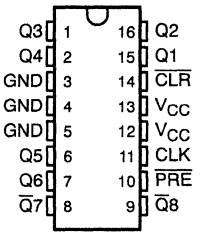
D3543, JULY 1990

- **Maximum Output Skew of 1 ns**
- **Maximum Pulse Skew of 1 ns**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN74AS303 . . . D† OR N PACKAGE
(TOP VIEW)



† Contact factory for information on availability of S.O. package.

description

The SN74AS303 contains eight flip-flops designed to have low skew between outputs. The eight outputs (six in-phase with CLK and two out-of-phase) toggle on successive CLK pulses. $\overline{PRE}$ and $\overline{CLR}$ inputs are provided to set the Q and $\overline{Q}$ outputs high or low independent of the CLK pin.

The 'AS303 has output and pulse skew parameters $t_{sk(o)}$ and $t_{sk(p)}$ to ensure performance as a clock driver when a divide-by-two function is required.

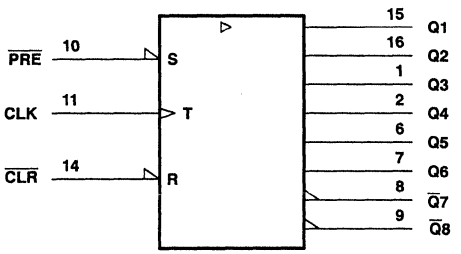
The SN74AS303 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{PRE}$	CLK	Q1–Q6	$\overline{Q}$7–$\overline{Q}$8
L	H	X	L	H
H	L	X	H	L
L	L	X	L‡	L‡
H	H	↑	$\overline{Q}_0$	Q_0
H	H	L	Q_0	$\overline{Q}_0$

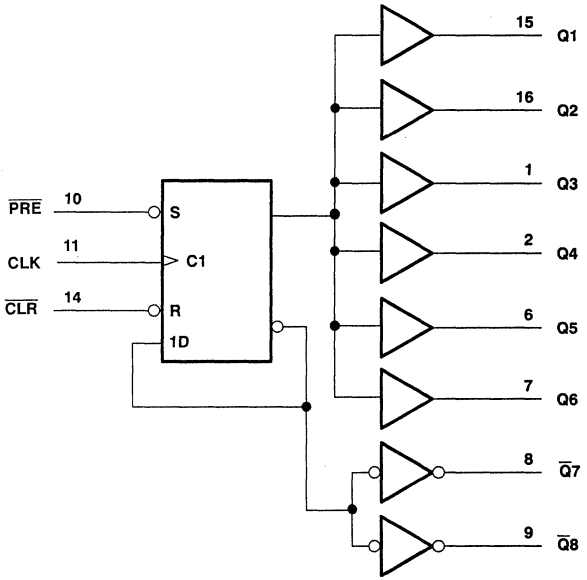
‡ This configuration will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 7 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			– 24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = – 18 mA			– 1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = – 2 mA	V_{CC}–2			V
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA	2	2.8		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			– 0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	– 50		– 150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		40	70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with CLK and $\overline{PRE}$ grounded, then with CLK and $\overline{CLR}$ grounded.

timing requirements (see Note 2)

PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	80	MHz
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	5		ns
		CLK high	4		
		CLK low	6		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ or $\overline{PRE}$ inactive	6		ns

switching characteristics over recommended operating free-air temperature range (see Note 2)

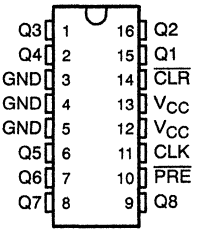
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
f_{max}§				80		MHz
t_{PLH}	CLK	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 50 pF	2	9	ns
t_{PHL}				2	9	ns
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 50 pF	3	12	ns
t_{PHL}				3	12	ns
$t_{sk(o)}$	CLK	Q	R_L = 500 Ω, C_L = 10 pF to 30 pF		1	ns
		$\overline{Q}$			1	
		Q, $\overline{Q}$			2	
$t_{sk(p)}$	CLK	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 10 pF to 30 pF		1	ns
t_r					4.5	ns
t_f					3.5	ns

§ f_{max} minimum values are at C_L = 0 to 30 pF.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

D3555, JULY 1990

- **Maximum Output Skew of 1 ns**
- **Maximum Pulse Skew of 1 ns**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include Plastic "Small Outline" Packages, and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

The SN74AS304 contains eight flip-flops designed to have low skew between outputs. The eight outputs (in-phase with CLK) toggle on successive CLK pulses. $\overline{PRE}$ and $\overline{CLR}$ pins are provided to set the Q outputs high or low independent of the CLK input.

The SN74AS304 has output and pulse skew parameters $t_{sk(o)}$ and $t_{sk(p)}$ to ensure performances as a clock driver when a divide-by-two function is required.

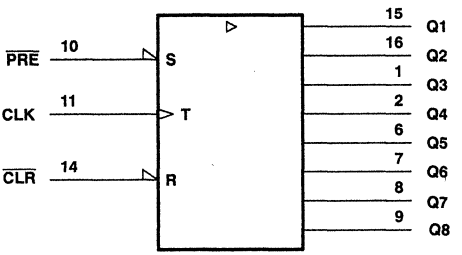
The SN74AS304 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{PRE}$	CLK	Q1–Q8
L	H	X	L
H	L	X	H
L	L	X	L†
H	H	↑	$\overline{Q}_0$
H	H	L	Q_0

† This configuration will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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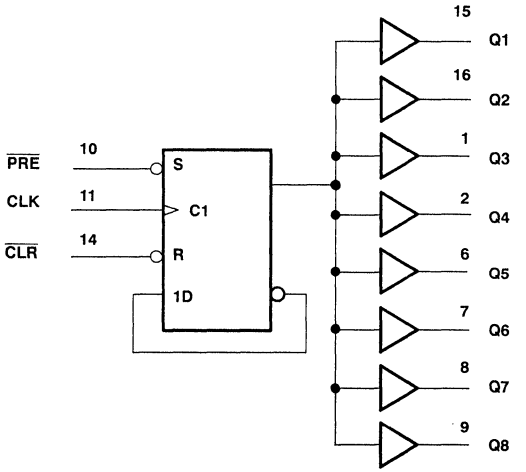
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 7 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			– 24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = – 18 mA			– 1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 2 mA	V_{CC}–2			V
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA	2	2.8		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			– 0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	– 50		– 150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		45	75	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with CLK and $\overline{PRE}$ grounded, then with CLK and $\overline{CLR}$ grounded.

timing requirements (see Note 2)

PARAMETER			MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency		0		80	MHz
t_w	Pulse duration	CLK high	4			ns
		CLK low	6			
		$\overline{CLR}$ or $\overline{PRE}$ low	5			
t_{su}	Setup time before CLK↑	$\overline{CLR}$ or $\overline{PRE}$ inactive	6			ns

switching characteristics over recommended operating free-air temperature range (see Note 2)

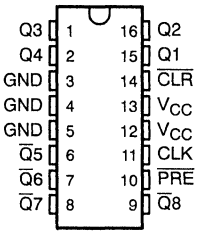
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}§				80			MHz
t_{PLH}	CLK	Q	R_L = 500 Ω, C_L = 50 pF	2	6	9	ns
t_{PHL}				2	6	9	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q	R_L = 500 Ω, C_L = 50 pF	3	7	12	ns
t_{PHL}				3	7	12	
$t_{sk(o)}$	CLK	Q	R_L = 500 Ω, C_L = 10 pF to 30 pF			1	ns
$t_{sk(p)}$	CLK	Q1, Q8	R_L = 500 Ω, C_L = 10 pF to 30 pF			1	ns
		Q2 to Q7				1.5	
t_r						4.5	ns
t_f						3.5	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ f_{max} minimum values are at C_L = 0 to 30 pF.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

D3596, JUNE 1990

- **Maximum Output Skew of 1 ns**
- **Maximum Pulse Skew of 1 ns**
- **Center Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

The SN74AS305 contains eight flip-flops designed to have low skew between outputs. The eight outputs (four in-phase with CLK and four out-of-phase) toggle on successive CLK pulses. $\overline{PRE}$ and $\overline{CLR}$ inputs are provided to set the Q and $\overline{Q}$ outputs high or low independent of the CLK pin.

The SN74AS305 has output and pulse skew parameters $t_{sk(o)}$ and $t_{sk(p)}$ to guarantee performances as a clock driver when a divide-by-two function is required.

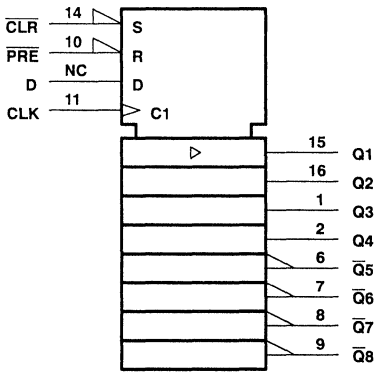
The SN74AS305 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{PRE}$	CLK	Q1-Q4	$\overline{Q5}$-$\overline{Q8}$
L	H	X	L	H
H	L	X	H	L
L	L	X	H†	H†
H	H	L	Q_0	$\overline{Q}_0$
H	H	↑	$\overline{Q}_0$	Q_0

† This configuration will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic symbol‡

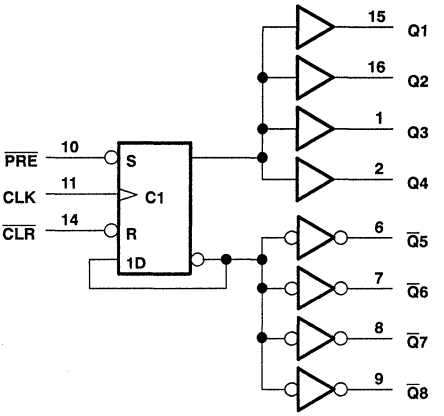


‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

D3596, JUNE 1990

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 7 V
Operating free-air temperature range: SN54AS305 ..... −55°C to 150°C
SN74AS305 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = – 18 mA			– 1.2	V
V_{OH}	V_{CC} = 4.5 V		V_{CC}– 2			V
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA	2	2.8		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7.0 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			– 0.5	mA
I_O	V_{CC} = 5.5 V,	V_I = 2.25 V	– 50		– 200	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		34	55	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: I_{CC} is measured with CLK and $\overline{PRE}$ grounded, then with CLK and $\overline{CLR}$ grounded.

timing requirements (see Note 2)

PARAMETER			MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency		0		100	MHz
t_w	Pulse duration	CLK high	4			ns
		CLK low	5			
		$\overline{CLR}$ or $\overline{PRE}$ low	5			
t_{su}	Setup time	$\overline{CLR}$ or $\overline{PRE}$ inactive	6			ns

switching characteristics over recommended operating free-air temperature range (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}‡				100			MHz
t_{PLH}	CLK	Q, $\overline{Q}$	R_L = 500 Ω,	2	6	8	ns
t_{PHL}			C_L = 50 pF,	2	6	8	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q, $\overline{Q}$	V_{CC} = 4.5 V to 5.5 V	3	7	10	ns
t_{PHL}				3	7	10	
$t_{sk(o)}$	CLK	Q, $\overline{Q}$	R_L = 500 Ω,			1	ns
$t_{sk(p)}$			C_L = 50 pF,			1	
t_r or t_f			V_{CC} = 4.75 V to 5.25 V			3	ns

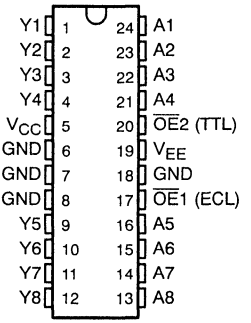
‡ f_{max} minimum values are at C_L = 0 to 30 pF.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

ECL/TTL Translator Products

- **10KH Compatible**
- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ECL and TTL Control Inputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



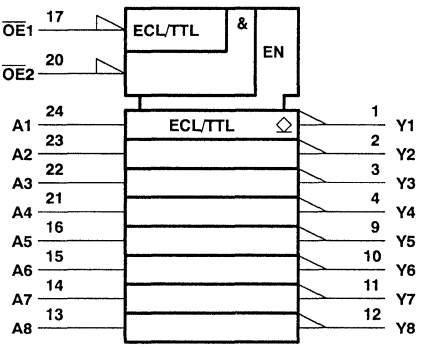
description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus oriented functions such as memory address drivers, clock drivers, and bus-oriented receivers and transmitters while eliminating the need for three-state overlap protection.

Two output enables, $\overline{OE}1$ and $\overline{OE}2$, are provided. These enable inputs are ANDed together with $\overline{OE}1$ being ECL-compatible and $\overline{OE}2$ being TTL-compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN10KHT5538 is characterized for operation from 0°C to 75°C.

logic symbol†

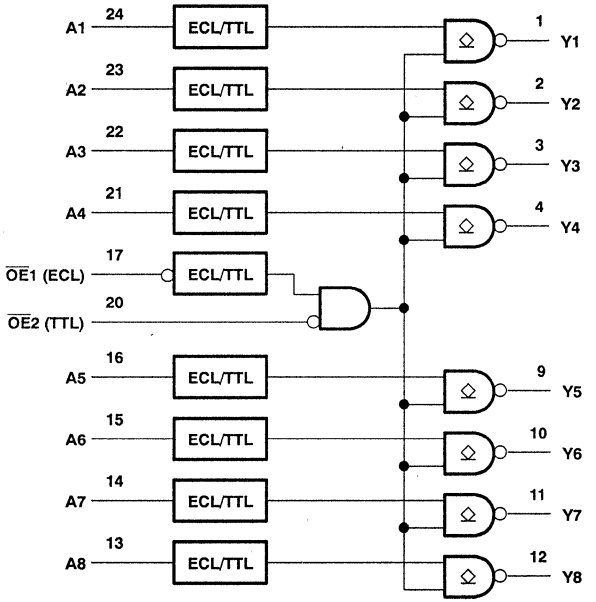


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

OUTPUT ENABLE		DATA INPUT	OUTPUT (TTL)
$\overline{OE}1$	$\overline{OE}2$	A	Y
H	X	X	H
X	H	X	H
L	L	L	H
L	L	H	L

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Supply voltage range, V_{EE} ..... – 8 V to 0 V
Input voltage range (TTL) (see Note 1) ..... – 1.2 V to 7 V
Input voltage range (ECL) ..... V_{EE} to 0 V
Input current range (TTL) ..... – 30 mA to 5 mA
Current into any output in the low state ..... 96 mA
Voltage applied to any output in the high state ..... – 0.5 V to V_{CC}
Operating temperature range ..... 0°C to 75°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage		4.5	5	5.5	V
V_{EE}	ECL supply voltage		−4.94	−5.2	−5.46	V
V_{IH}	TTL high-level input voltage		2			V
V_{IL}	TTL low-level input voltage				0.8	V
V_{IH}	ECL high-level input voltage (see Note 2)	0°C	−1170		−840	mV
		25°C	−1130		−810	mV
		75°C	−1070		−735	mV
V_{IL}	ECL low-level input voltage (see Note 2)	0°C	−1950		−1480	mV
		25°C	−1950		−1480	mV
		75°C	−1950		−1450	mV
V_{OH}	TTL high-level output voltage				5.5	V
I_{OL}	TTL low-level output current				48	mA
I_{IK}	TTL input clamp current				−18	mA
T_A	Operating free-air temperature		0		75	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{OE}2$ only	V_{CC} = 4.5 V,	V_{EE} = −4.94 V,	I_I = −18 mA				−1.2	V
I_I	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 7 V				0.1	mA
I_{IH}	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 2.7 V				20	μA
I_{IL}	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 0.5 V				−0.5	mA
I_{IH}	A inputs and $\overline{OE}1$	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −840 V	0°C			350	μA
		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −810 V	25°C			350	
		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −735 V	75°C			350	
I_{IL}	A inputs and $\overline{OE}1$	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −1950 V	0°C	0.5			μA
					25°C	0.5			
					75°C	0.5			
I_{OH}		V_{CC} = 4.5 V,	V_{EE} = −4.94 V,	V_{OH} = 5.5 V				250	μA
V_{OL}		V_{CC} = 4.5 V,	V_{EE} = −5.2 V ± 5%,	I_{OL} = 48 mA			0.38	0.55	V
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				66	95	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				79.5	114	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				−23	−33	mA
C_i		V_{CC} = 5.5 V,	V_{EE} = −5.2 V				5		pF
C_o		V_{CC} = 5.5 V,	V_{EE} = −5.2 V				5		pF

† All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.

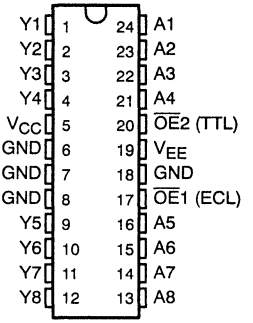
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
t_{PLH}	Any A	Y	6.4	9.1	11.7	ns
t_{PHL}			2.7	4.9	7.2	
t_{PLH}	$\overline{OE}1$ (ECL)	Y	7	10.1	13.3	ns
t_{PHL}			3.6	6.2	8.8	
t_{PLH}	$\overline{OE}2$ (TTL)	Y	6.5	9.1	11.6	ns
t_{PHL}			2.8	5.3	7.9	

† All typical values are at V_{CC} = 5 V, V_{EE} = – 5.2 V, T_A = 25°C.
NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

- 100K Compatible
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- ECL and TTL Control Inputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



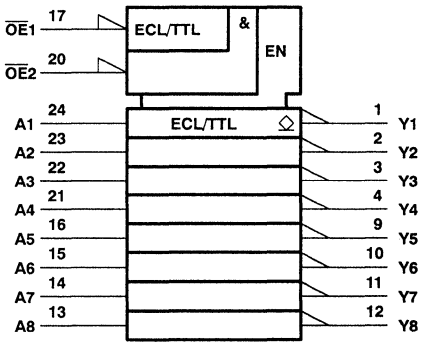
description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 100K signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus oriented functions such as memory address drivers, clock drivers, and bus-oriented receivers and transmitters while eliminating the need for three-state overlap protection.

Two output enables, $\overline{OE}1$ and $\overline{OE}2$, are provided. These enable inputs are ANDed together with $\overline{OE}1$ being ECL-compatible and $\overline{OE}2$ being TTL-compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN100KT5538 is characterized for operation from 0°C to 85°C.

logic symbol†

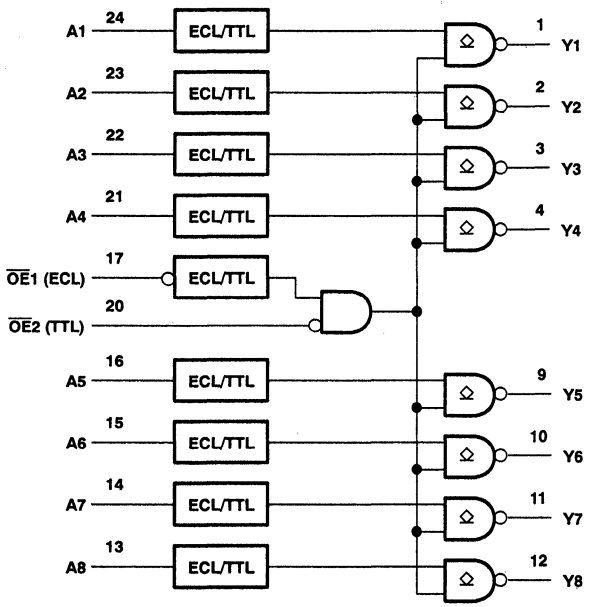


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

OUTPUT ENABLE		DATA INPUT	OUTPUT (TTL)
$\overline{OE}1$	$\overline{OE}2$	A	Y
H	X	X	H
X	H	X	H
L	L	L	H
L	L	H	L

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Supply voltage range, V_{EE} ..... −8 V to 0 V
Input voltage range (TTL) (see Note 1) ..... −1.2 V to 7 V
Input voltage range (ECL) ..... V_{EE} to 0 V
Input current range (TTL) ..... −30 mA to 5 mA
Current into any output in the low state ..... 96 mA
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Operating temperature range ..... 0°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage		4.5	5	5.5	V
V_{EE}	ECL supply voltage		−4.2	−4.5	−4.8	V
V_{IH}	High-level input voltage	TTL	2			V
		ECL (see Note 2)	−1150		−840	mV
V_{IL}	Low-level input voltage	TTL			0.8	V
		ECL (see Note 2)	−1810		−1490	mV
V_{OH}	TTL high-level output voltage				5.5	V
I_{OL}	TTL low-level output current				48	mA
I_{IK}	TTL input clamp current				−18	mA
T_A	Operating free-air temperature		0		85	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{OE}$2 only	V_{CC} = 4.5 V,	V_{EE} = −4.2 V,	I_I = −18 mA			−1.2	V
V_{OL}		V_{CC} = 4.5 V,	V_{EE} = −4.5 V ± 0.3 V,	I_{OL} = 48 mA		0.38	0.55	V
I_I	$\overline{OE}$2 only	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = 7 V			0.1	mA
I_{IH}	$\overline{OE}$2 only	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = 2.7 V			20	μA
	A inputs and $\overline{OE}$1	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = −840 mV			350	
I_{IL}	$\overline{OE}$2 only	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = 0.5 V			−0.5	mA
	A inputs and $\overline{OE}$1	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = −1810 mV	0.5			μA
I_{OH}		V_{CC} = 4.5 V,	V_{EE} = −4.2 V,	V_{OH} = 5.5 V			250	μA
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V			66	95	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V			79.5	114	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = −4.2 V			−23	−33	mA
C_i		V_{CC} = 5.5 V,	V_{EE} = −4.5 V			5		pF
C_o		V_{CC} = 5.5 V,	V_{EE} = −4.5 V			5		pF

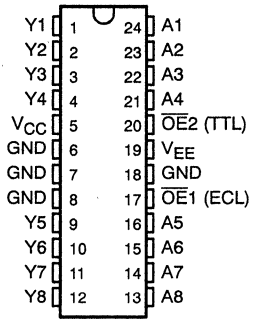
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
t_{PLH}	Any A	Y	6.4	9.1	11.7	ns
t_{PHL}			2.7	4.9	7.2	
t_{PLH}	$\overline{OE}$1 (ECL)	Y	7	10.1	13.3	ns
t_{PHL}			3.6	6.2	8.8	
t_{PLH}	$\overline{OE}$2 (TTL)	Y	6.5	9.1	11.6	ns
t_{PHL}			2.8	5.3	7.9	

† All typical values are at V_{CC} = 5 V, V_{EE} = −4.5 V, T_A = 25°C.
NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

- **10KH Compatible**
- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ECL and TTL Output-Enable Inputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters while eliminating the need for 3-state overlap protection.

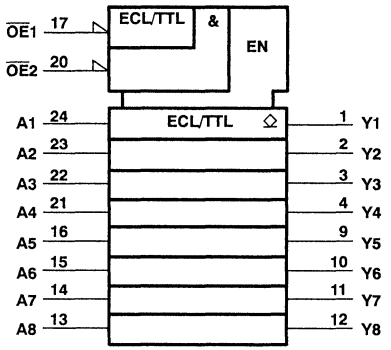
Two pins $\overline{OE}1$ and $\overline{OE}2$ are provided for output-enable control. These control inputs are ANDed together with $\overline{OE}1$ being ECL-compatible and $\overline{OE}2$ being TTL-compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN10KHT5539 is characterized for operation from 0°C to 75°C.

FUNCTION TABLE

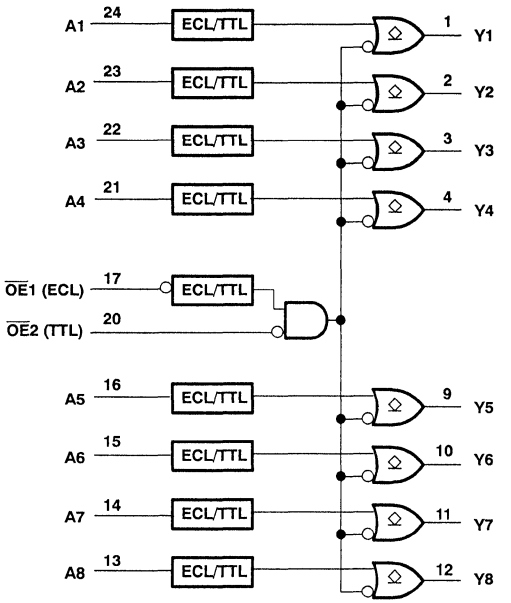
OUTPUT ENABLE		DATA INPUT	OUTPUT (TTL)
$\overline{OE}1$	$\overline{OE}2$	A	Y
X	H	X	H
H	X	X	H
L	L	L	L
L	L	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Supply voltage range, V_{EE} ..... – 8 V to 0 V
Input voltage range: TTL (see Note 1) ..... – 1.2 V to 7 V
ECL ..... V_{EE} to 0 V
Input current range, TTL ..... – 30 mA to 5 mA
Current into any output in the low state ..... 96 mA
Voltage applied to any output in the high state ..... – 0.5 V to V_{CC}
Operating free-air temperature range ..... 0°C to 75°C
Storage temperature range ..... – 65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage		4.5	5	5.5	V
V_{EE}	ECL supply voltage		−4.94	−5.2	−5.46	V
V_{IH}	TTL high-level input voltage		2			V
V_{IL}	TTL low-level input voltage				0.8	V
V_{IH}	ECL high-level input voltage†	T_A = 0°C	−1170		−840	mV
		T_A = 25°C	−1130		−810	
		T_A = 75°C	−1070		−735	
V_{IL}	ECL low-level input voltage†	T_A = 0°C	−1950		−1480	mV
		T_A = 25°C	−1950		−1480	
		T_A = 75°C	−1950		−1450	
V_{OH}	TTL high-level output voltage				5.5	V
I_{IK}	TTL input clamp current				−18	mA
I_{OL}	Low-level output current				48	mA
T_A	Operating free-air temperature range		0		75	°C

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{IK}	$\overline{OE}$2 only	V_{CC} = 4.5 V,	V_{EE} = −4.94 V,	I_I = −18 mA				−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{EE} = −4.94 V,	V_{OH} = 5.5 V				250	μA
V_{OL}		V_{CC} = 4.5 V,	V_{EE} = −5.2 V ± 5%,	I_{OL} = 48 mA			0.38	0.55	V
I_I	$\overline{OE}$2 only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 7 V				0.1	mA
I_{IH}	$\overline{OE}$2 only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 2.7 V				20	μA
I_{IL}	$\overline{OE}$2 only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 0.5 V				−0.5	mA
I_{IH}	A inputs and $\overline{OE}$1	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −840 mV	T_A = 0°C			350	μA
		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −810 mV	T_A = 25°C			350	
		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −735 mV	T_A = 75°C			350	
I_{IL}	A inputs and $\overline{OE}$1	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −1950 mV	T_A = 0°C	0.5			μA
					T_A = 25°C	0.5			
					T_A = 75°C	0.5			
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				63	91	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				79	114	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				−22	−32	mA
C_i		V_{CC} = 5 V,	V_{EE} = −5.2 V				6		pF
C_o		V_{CC} = 5 V,	V_{EE} = −5.2 V				5		pF

‡ All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.

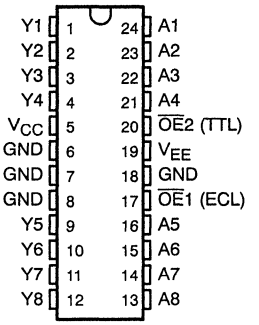
switching characteristics over recommended ranges of operating supply voltage and free-air temperature (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
t_{PLH}	Any A	Y	6.2	9.3	12.4	ns
t_{PHL}			2.6	4.9	7.3	
t_{PLH}	$\overline{OE}$1 (ECL)	Y	7.1	10.3	13.5	ns
t_{PHL}			3.2	5.8	8.4	
t_{PLH}	$\overline{OE}$2 (TTL)	Y	6.5	9.5	12.4	ns
t_{PHL}			2.7	5.3	8	

† All typical values are at V_{CC} = 5 V, V_{EE} = – 5.2 V, T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

- 100K Compatible
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- ECL and TTL Output-Enable Inputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 100K signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters while eliminating the need for three-state overlap protection.

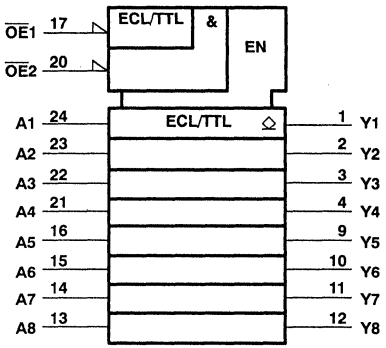
Two pins $\overline{OE}1$ and $\overline{OE}2$ are provided for output-enable control. These control inputs are ANDed together with $\overline{OE}1$ being ECL-compatible and $\overline{OE}2$ being TTL-compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN100KT5539 is characterized for operation from 0°C to 85°C.

FUNCTION TABLE

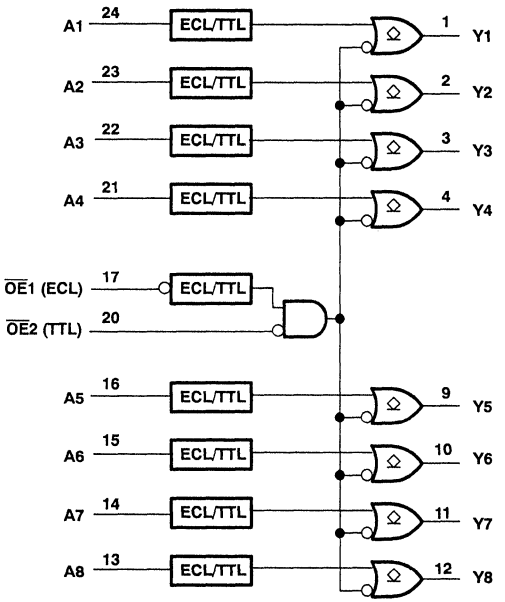
OUTPUT ENABLE		DATA INPUT	OUTPUT (TTL)
$\overline{OE}1$	$\overline{OE}2$	A	Y
H	X	X	H
X	H	X	H
L	L	L	L
L	L	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Supply voltage range, V_{EE} ..... −8 V to 0 V
Input voltage range: TTL (see Note 1) ..... −1.2 V to 7 V
ECL ..... V_{EE} to 0 V
Input current range: TTL ..... −30 mA to 5 mA
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state ..... 96 mA
Operating free-air temperature range ..... 0°C to 85°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage	4.5	5	5.5	V
V_{EE}	ECL supply voltage	−4.2	−4.5	−4.8	V
V_{IH}	TTL high-level input voltage	2			V
V_{IL}	TTL low-level input voltage			0.8	V
V_{IH}	ECL high-level input voltage†	−1150		−840	mV
V_{IL}	ECL low-level input voltage†	−1810		−1490	mV
V_{OH}	TTL high-level output voltage			5.5	V
I_{OL}	TTL low-level output current			48	mA
I_{IK}	TTL input clamp current			−18	mA
T_A	Operating free-air temperature range	0		85	°C

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}	$\overline{OE}2$ only	V_{CC} = 4.5 V,	V_{EE} = −4.2 V,	I_I = −18 mA			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{EE} = −4.2 V,	V_{OH} = 5.5 V			250	μA
V_{OL}		V_{CC} = 4.5 V,	V_{EE} = −4.5 V ± 0.3 V,	I_{OL} = 48 mA		0.38	0.55	V
I_I	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = 7 V			0.1	mA
I_{IH}	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = 2.7 V			20	μA
	A inputs and $\overline{OE}1$	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = −840 mV			350	μA
I_{IL}	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = 0.5 V			−0.5	mA
	A inputs and $\overline{OE}1$	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = −1810 mV	0.5			μA
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V			63	91	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V			79	114	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = −4.2 V			−22	−32	mA
C_i		V_{CC} = 5 V,	V_{EE} = −4.5 V			6		pF
C_o		V_{CC} = 5 V,	V_{EE} = −4.5 V			5		pF

‡ All typical values are at V_{CC} = 5 V, V_{EE} = −4.5 V, T_A = 25°C.

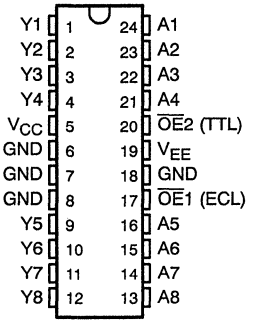
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
t_{PLH}	Any A	Y	6.2	9.3	12.4	ns
t_{PHL}			2.6	4.9	7.3	
t_{PLH}	$\overline{OE}1$ (ECL)	Y	7.1	10.3	13.5	ns
t_{PHL}			3.2	5.8	8.4	
t_{PLH}	$\overline{OE}2$ (TTL)	Y	6.5	9.5	12.4	ns
t_{PHL}			2.7	5.3	8	

† All typical values are at V_{CC} = 5 V, V_{EE} = – 4.5 V, T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

- **10KH Compatible**
- **ECL and TTL Control Inputs**
- **Inverting Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

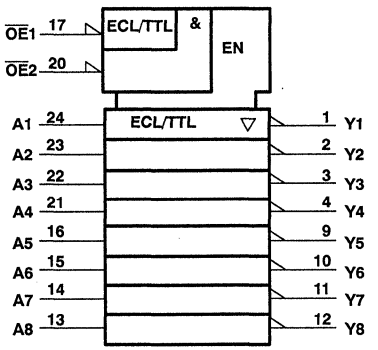
Two output-enable pins, $\overline{OE}1$ and $\overline{OE}2$, are provided. These control inputs are ANDed together with $\overline{OE}1$ being ECL compatible and $\overline{OE}2$ being TTL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN10KHT5540 is characterized for operation from 0°C to 75°C.

FUNCTION TABLE

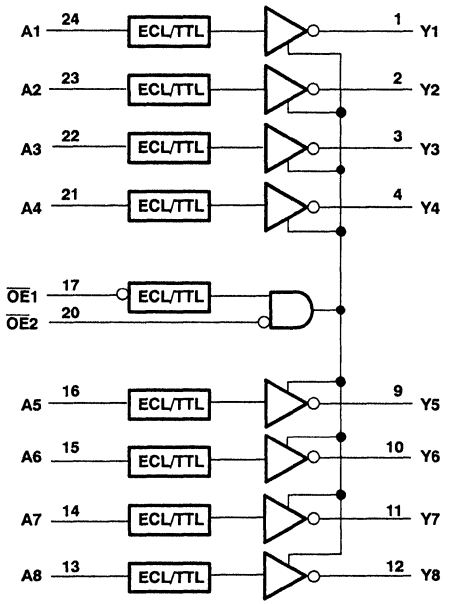
OUTPUT ENABLE		DATA INPUT	OUTPUT (TTL)
$\overline{OE}1$	$\overline{OE}2$	A	Y
X	H	X	Z
H	X	X	Z
L	L	L	H
L	L	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Supply voltage range, V_{EE} ..... – 8 V to 0 V
Input voltage range (TTL) (see Note 1) ..... – 1.2 V to 7 V
Input voltage range (ECL) ..... V_{EE} to 0 V
Voltage applied to any output in the disabled or power-off state ..... – 0.5 V to 5.5 V
Voltage applied to any output in the high state ..... – 0.5 V to V_{CC}
Input current range (TTL) ..... – 30 mA to 5 mA
Current into any output in the low state ..... 96 mA
Operating free-air temperature range ..... 0°C to 75°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage		4.5	5	5.5	V
V_{EE}	ECL supply voltage		– 4.94	– 5.2	– 5.46	V
V_{IH}	TTL high-level input voltage		2			V
V_{IL}	TTL low-level input voltage				0.8	V
V_{IH}‡	ECL high-level input voltage	T_A = 0°C	– 1170		– 840	mV
		T_A = 25°C	– 1130		– 810	
		T_A = 75°C	– 1070		– 735	
V_{IL}‡	ECL low-level input voltage	T_A = 0°C	– 1950		– 1480	mV
		T_A = 25°C	– 1950		– 1480	
		T_A = 75°C	– 1950		– 1450	
I_{IK}	TTL input clamp current				– 18	mA
I_{OH}	High-level output current				– 15	mA
I_{OL}	Low-level output current				48	mA
T_A	Operating free-air temperature		0		75	°C

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{OE}2$ only	V_{CC} = 4.5 V,	V_{EE} = −4.94 V,	I_I = −18 mA				−1.2	V
V_{OH}		V_{CC} = 4.5 V,	V_{EE} = −5.2 V ± 5%,	I_{OH} = −3 mA		2.4	3.3		V
		V_{CC} = 4.5 V,	V_{EE} = −5.2 V ± 5%,	I_{OH} = −15 mA		2	3.1		
V_{OL}		V_{CC} = 4.5 V,	V_{EE} = −5.2 V ± 5%,	I_{OL} = 48 mA			0.38	0.55	V
I_I	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 7 V				0.1	mA
I_{IH}	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 2.7 V				20	μA
I_{IL}	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 0.5 V				−0.5	mA
I_{IH}	Data inputs and $\overline{OE}1$	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −840 mV	T_A = 0°C			350	μA
		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −810 mV	T_A = 25°C			350	
		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −735 mV	T_A = 75°C			350	
I_{IL}	Data inputs and $\overline{OE}1$	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −1950 mV	T_A = 0°C	0.5			μA
					T_A = 25°C	0.5			
					T_A = 75°C	0.5			
I_{OZH}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_O = 2.7 V				50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_O = 0.5 V				−50	μA
I_{OS}‡		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_O = 0		−100		−225	mA
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				67	97	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				84	120	mA
I_{CCZ}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				81	116	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				−23	−33	mA
C_i		V_{CC} = 5 V,	V_{EE} = −5.2 V				5		pF
C_o		V_{CC} = 5 V,	V_{EE} = −5.2 V				7		pF

† All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.
‡ Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.

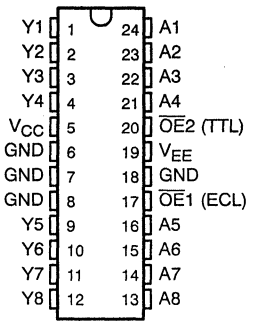
switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
t_{PLH}	A	Y	1.6	3.9	6.4	ns
t_{PHL}			1.6	4.2	6.4	
t_{PZH}	$\overline{OE}1$	Y	2.4	4.5	6.9	ns
t_{PZL}			3.5	5.9	8.7	
t_{PHZ}	$\overline{OE}1$	Y	2.8	5.2	8.1	ns
t_{PLZ}			2.2	4.6	8	
t_{PZH}	$\overline{OE}2$	Y	1.4	3.3	6.1	ns
t_{PZL}			2.5	4.7	7.9	
t_{PHZ}	$\overline{OE}2$	Y	1.6	4.1	6.5	ns
t_{PLZ}			0.7	3.3	6.4	

† All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

- **100K Compatible**
- **Inverting Outputs**
- **ECL and TTL Control Inputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 100K ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

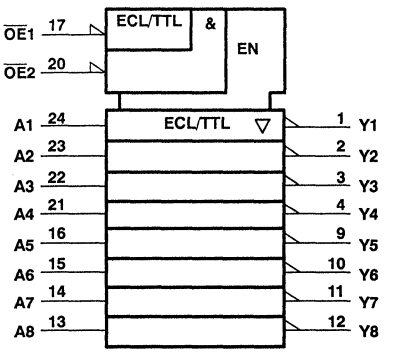
Two output-enable pins, $\overline{OE}1$ and $\overline{OE}2$, are provided. These control inputs are ANDed together with $\overline{OE}1$ being ECL compatible and $\overline{OE}2$ being TTL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN100KT5540 is characterized for operation from 0°C to 85°C.

FUNCTION TABLE

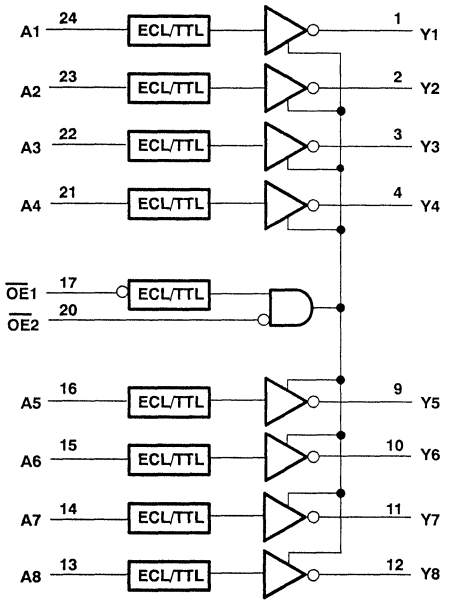
OUTPUT ENABLE		DATA INPUT	OUTPUT TTL
$\overline{OE}1$	$\overline{OE}2$	A	Y
X	H	X	Z
H	X	X	Z
L	L	L	H
L	L	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Supply voltage range, V_{EE} ..... – 8 V to 0 V
Input voltage range: TTL (see Note 1) ..... – 1.2 V to 7 V
ECL ..... V_{EE} to 0 V
Voltage applied to any output in the high state ..... – 0.5 V to V_{CC}
Voltage applied to any output in the disabled or power-off state ..... – 0.5 V to 5.5 V
Input current range (TTL) ..... – 30 mA to 5 mA
Current into any output in the low state ..... 96 mA
Operating free-air temperature range ..... 0°C to 85°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage	4.5	5	5.5	V
V_{EE}	ECL supply voltage	−4.2	−4.5	−4.8	V
V_{IH}	TTL high-level input voltage	2			V
V_{IL}	TTL low-level input voltage			0.8	V
V_{IH}	ECL high-level input voltage†	−1150		−840	mV
V_{IL}	ECL low-level input voltage†	−1810		−1490	mV
I_{IK}	TTL input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		85	°C

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}	$\overline{OE}2$ only	V_{CC} = 4.5 V,	V_{EE} = −4.2 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	V_{EE} = −4.5 V ± 0.3 V,	I_{OH} = −3 mA	2.4	3.3		V
		V_{CC} = 4.5 V,	V_{EE} = −4.5 V ± 0.3 V,	I_{OH} = −15 mA	2	3.1		
V_{OL}		V_{CC} = 4.5 V,	V_{EE} = −4.5 V ± 0.3 V,	I_{OL} = 48 mA		0.38	0.55	V
I_I	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = 7 V			0.1	mA
I_{IH}	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = 2.7 V			20	μA
I_{IL}	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = 0.5 V			−0.5	mA
I_{IH}	Data inputs and $\overline{OE}1$	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_{IH} = −840 mV			350	μA
I_{IL}	Data inputs and $\overline{OE}1$	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_{IL} = −1810 mV	0.50			μA
I_{OZH}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_O = 2.7 V			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_O = 0.5 V			−50	μA
I_{OS}§		V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_O = 0 V	−100		−225	mA
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V			67	97	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V			84	120	mA
I_{CCZ}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V			81	116	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V			−22	−33	mA
C_i		V_{CC} = 5 V,	V_{EE} = 4.5 V			5		pF
C_o		V_{CC} = 5 V,	V_{EE} = 4.5 V			7		pF

‡ All typical values are at V_{CC} = 5 V, V_{EE} = −4.5 V, T_A = 25°C.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

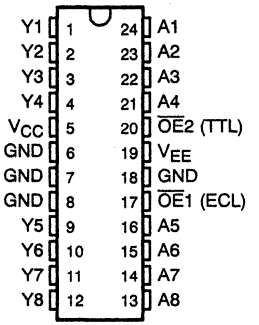
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
t_{PLH}	A	Y	1.6	3.9	6.4	ns
t_{PHL}			1.6	4.2	6.4	
t_{PZH}	$\overline{OE}1$	Y	2.4	4.5	6.9	ns
t_{PZL}			3.5	5.9	8.7	
t_{PHZ}	$\overline{OE}1$	Y	2.8	5.2	8.1	ns
t_{PLZ}			2.2	4.6	8	
t_{PZH}	$\overline{OE}2$	Y	1.4	3.3	6.1	ns
t_{PZL}			2.5	4.7	7.9	
t_{PHZ}	$\overline{OE}2$	Y	1.6	4.1	6.5	ns
t_{PLZ}			0.7	3.3	6.4	

† All typical values are at V_{CC} = 5 V, V_{EE} = −4.5 V, T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

- **10KH Compatible**
- **ECL and TTL Control Inputs**
- **Noninverting Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



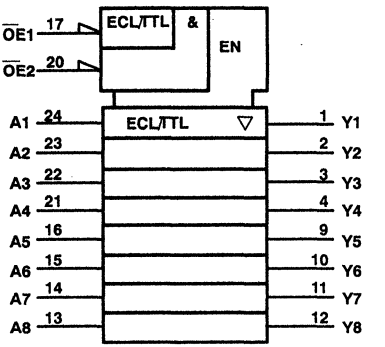
description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

Two output-enable pins, $\overline{OE}1$ and $\overline{OE}2$, are provided. These control inputs are ANDed together with $\overline{OE}1$ being ECL compatible and $\overline{OE}2$ being TTL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN10KHT5541 is characterized for operation from 0°C to 75°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

OUTPUT ENABLE		DATA INPUT	OUTPUT (TTL)
$\overline{OE}1$	$\overline{OE}2$	A	Y
X	H	X	Z
H	X	X	Z
L	L	L	L
L	L	H	H

TEXAS INSTRUMENTS
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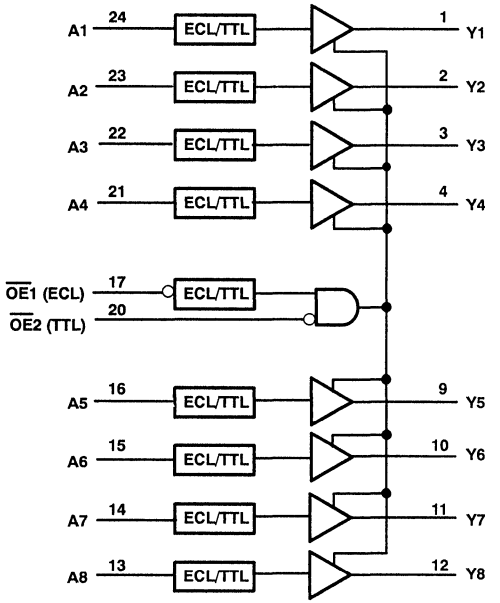
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... – 0.5 V to 7 V
Supply voltage, V_{EE} ..... – 8 V to 0 V
Input voltage (TTL) (see Note 1) ..... – 1.2 V to 7 V
Input voltage (ECL) ..... V_{EE} to 0 V
Voltage applied to any output in the disabled or power-off state ..... – 0.5 V to 5.5 V
Voltage applied to any output in the high state ..... – 0.5 V to V_{CC}
Input current (TTL) ..... – 30 mA to 5 mA
Current into any output in the low state ..... 96 mA
Operating free-air temperature range ..... 0°C to 75°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage		4.5	5	5.5	V
V_{EE}	ECL supply voltage		– 4.94	– 5.2	– 5.46	V
V_{IH}	TTL high-level input voltage		2			V
V_{IL}	TTL low-level input voltage				0.8	V
V_{IH}‡	ECL high-level input voltage	T_A = 0°C	– 1170		– 840	mV
		T_A = 25°C	– 1130		– 810	
		T_A = 75°C	– 1070		– 735	
V_{IL}‡	ECL low-level input voltage	T_A = 0°C	– 1950		– 1480	mV
		T_A = 25°C	– 1950		– 1480	
		T_A = 75°C	– 1950		– 1450	
I_{IK}	TTL input clamp current				– 18	mA
I_{OH}	High-level output current				– 15	mA
I_{OL}	Low-level output current				48	mA
T_A	Operating free-air temperature		0		75	°C

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{OE}2$ only	V_{CC} = 4.5 V,	V_{EE} = −4.94 V,	I_I = −18 mA				−1.2	V
I_I	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 7 V				0.1	mA
I_{IH}	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 2.7 V				20	μA
I_{IL}	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 0.5 V				−0.5	mA
I_{IH}	Data inputs and $\overline{OE}1$	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −840 mV	T_A = 0°C			350	μA
		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −810 mV	T_A = 25°C			350	
		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −735 mV	T_A = 75°C			350	
I_{IL}	Data inputs and $\overline{OE}1$	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −1950 mV	T_A = 0°C	0.5			μA
					T_A = 25°C	0.5			
					T_A = 75°C	0.5			
V_{OH}		V_{CC} = 4.5 V,	V_{EE} = −5.2 V ± 5%,	I_{OH} = −3 mA		2.4	3.3		V
		V_{CC} = 4.5 V,	V_{EE} = −5.2 V ± 5%,	I_{OH} = −15 mA		2	3.1		
V_{OL}		V_{CC} = 4.5 V,	V_{EE} = −5.2 V ± 5%,	I_{OL} = 48 mA			0.38	0.55	V
I_{OZH}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_O = 2.7 V				50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_O = 0.5 V				−50	μA
I_{OS}‡		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_O = 0		−100		−225	mA
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				64	97	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				80	120	mA
I_{CCZ}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				77	116	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				−22	−33	mA
C_i		V_{CC} = 5 V,	V_{EE} = −5.2 V				5		pF
C_o		V_{CC} = 5 V,	V_{EE} = −5.2 V				7		pF

† All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.
‡ Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.

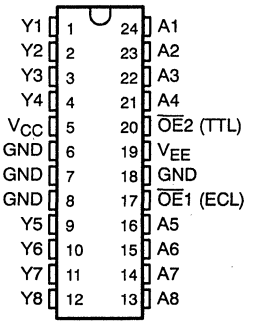
switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
t_{PLH}	A	Y	1.7	4	6.2	ns
t_{PHL}			1.6	4	6.2	
t_{PZH}	$\overline{OE}1$	Y	2.6	4.7	6.7	ns
t_{PZL}			3.2	5.9	8.5	
t_{PHZ}	$\overline{OE}1$	Y	2.9	5.4	7.8	ns
t_{PLZ}			1.9	4.9	7.8	
t_{PZH}	$\overline{OE}2$	Y	1.7	4	6.2	ns
t_{PZL}			2.5	5.1	7.7	
t_{PHZ}	$\overline{OE}2$	Y	2.1	4.3	6.4	ns
t_{PLZ}			1.1	3.7	6.3	

† All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

- **100K Compatible**
- **ECL and TTL Control Inputs**
- **Noninverting Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



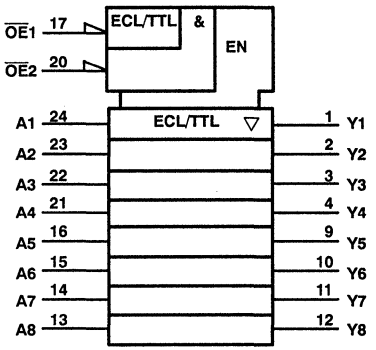
description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 100K ECL signal environment to a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

Two output-enable pins, $\overline{OE}1$ and $\overline{OE}2$ are provided. These control inputs are ANDed together with $\overline{OE}1$ being ECL compatible and $\overline{OE}2$ being TTL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN100KT5541 is characterized for operation from 0°C to 85°C.

logic symbol†

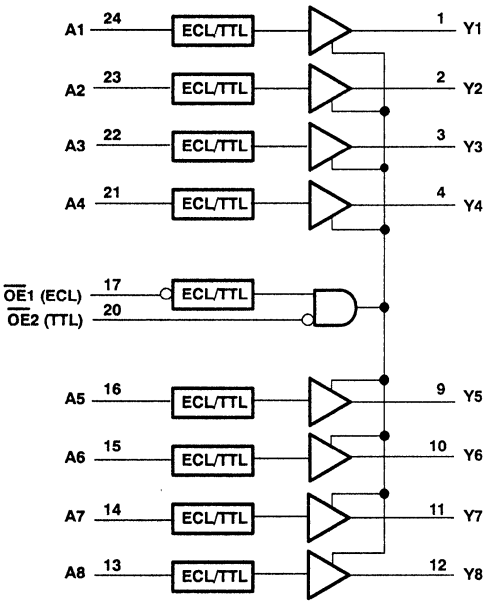


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

OUTPUT ENABLE		DATA INPUT	OUTPUT (TTL)
$\overline{OE}1$	$\overline{OE}2$	A	Y
X	H	X	Z
H	X	X	Z
L	L	L	L
L	L	H	H

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Supply voltage range, V_{EE} ..... – 8 V to 0 V
Input voltage range (TTL) (see Note 1) ..... – 1.2 V to 7 V
Input voltage range (ECL) ..... V_{EE} to 0 V
Voltage applied to any output in the high state ..... – 0.5 V to V_{CC}
Voltage applied to any output in the disabled or power-off state ..... – 0.5 V to 5.5 V
Input current range (TTL) ..... – 30 mA to 5 mA
Current into any output in the low state ..... 96 mA
Operating free-air temperature range ..... 0°C to 85°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage	4.5	5	5.5	V
V_{EE}	ECL supply voltage	– 4.2	– 4.5	– 4.8	V
V_{IH}	TTL high-level input voltage	2			V
V_{IL}	TTL low-level input voltage			0.8	V
V_{IH}	ECL high-level input voltage‡	– 1150		– 840	mV
V_{IL}	ECL low-level input voltage‡	– 1810		– 1490	mV
I_{IK}	TTL input clamp current			– 18	mA
I_{OH}	High-level output current			– 15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		85	°C

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{OE}2$ only	V_{CC} = 4.5 V,	V_{EE} = – 4.2 V,	I_I = – 18 mA			– 1.2	V
I_I	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_I = 7 V			0.1	mA
I_{IH}	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_I = 2.7 V			20	μA
I_{IL}	$\overline{OE}2$ only	V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_I = 0.5 V			– 0.5	mA
I_{IH}	Data inputs and $\overline{OE}1$	V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_{IH} = – 840 mV			350	μA
I_{IL}	Data inputs and $\overline{OE}1$	V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_{IL} = – 1810 mV	0.50			μA
V_{OH}		V_{CC} = 4.5 V,	V_{EE} = – 4.5 V ± 0.3 V,	I_{OH} = – 3 mA	2.4	3.3		V
		V_{CC} = 4.5 V,	V_{EE} = – 4.5 V ± 0.3 V,	I_{OH} = – 15 mA	2	3.1		
V_{OL}		V_{CC} = 4.5 V,	V_{EE} = – 4.5 V ± 0.3 V,	I_{OL} = 48 mA		0.38	0.55	V
I_{OZH}		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_O = 2.7 V			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_O = 0.5 V			– 50	μA
I_{OS}‡		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_O = 0 V	– 100		– 225	mA
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V			64	97	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V			80	120	mA
I_{CCZ}		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V			77	116	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V			– 22	– 33	mA
C_i		V_{CC} = 5 V,	V_{EE} = 4.5 V			5		pF
C_o		V_{CC} = 5 V,	V_{EE} = 4.5 V			7		pF

† All typical values are at V_{CC} = 5 V, V_{EE} = – 4.5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 2)

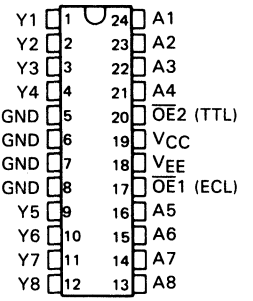
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
t_{PLH}	A	Y	1.7	4	6.2	ns
t_{PHL}			1.6	4	6.2	
t_{PZH}	$\overline{OE}1$	Y	2.6	4.7	6.7	ns
t_{PZL}			3.2	5.9	8.5	
t_{PHZ}	$\overline{OE}1$	Y	2.9	5.4	7.8	ns
t_{PLZ}			1.9	4.9	7.8	
t_{PZH}	$\overline{OE}2$	Y	1.7	4	6.2	ns
t_{PZL}			2.5	5.1	7.7	
t_{PHZ}	$\overline{OE}2$	Y	2.1	4.3	6.4	ns
t_{PLZ}			1.1	3.7	6.3	

† All typical values are at V_{CC} = 5 V, V_{EE} = – 4.5 V, T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

D3136, AUGUST 1988—REVISED DECEMBER 1988

- 10KH Compatible
- ECL and TTL Control Inputs
- P-N-P Inputs Reduce DC Loading
- Flow-Through Architectures Optimizes PCB Layout
- Center Pin V_{CC}, V_{EE} and GND Configurations Minimize High-Speed Switching Noise
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

These octal TTL-to-ECL translators are designed to provide efficient translation between a TTL signal environment and a 10KH ECL signal environment. The designer has a choice of inverting ('5542) or true ('5543) outputs. Two pins, $\overline{OE}1$ and $\overline{OE}2$, are provided for output enable control. These control inputs are negative ANDed together, with $\overline{OE}1$ being ECL compatible and $\overline{OE}2$ being TTL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment. The outputs, when disabled, go to a normal ECL logic low level.

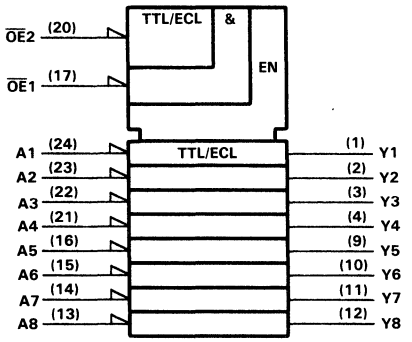
The SN10KHT5542 and SN10KHT5543 are characterized for operation from 0°C to 75°C.

FUNCTION TABLE

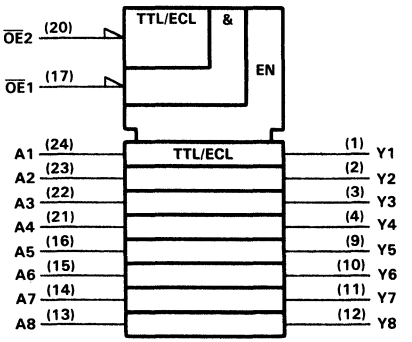
OUTPUT CONTROL		DATA INPUT	OUTPUT	
$\overline{OE}1$	$\overline{OE}2$	A	'5542	'5543
H	X	X	L	L
X	H	X	L	L
L	L	L	H	L
L	L	H	L	H

logic symbols†

SN10KHT5542



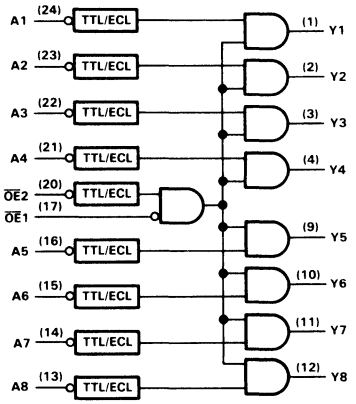
SN10KHT5543



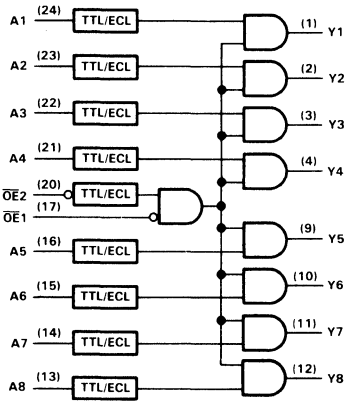
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

SN10KHT5542



SN10KHT5543



absolute maximum ratings over operating ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Supply voltage range, V_{EE} . . . . . −8 V to 0 V
Input voltage range (TTL) (See Note 1) . . . . . −1.2 V to 7 V
Input voltage range (ECL) . . . . . V_{EE} to 0 V
Input current range (TTL) . . . . . −30 mA to 5 mA
Operating ambient temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage		4.5	5.0	5.5	V
V_{EE}	ECL supply voltage		−4.94	−5.2	−5.46	V
V_{IH}	TTL high-level input voltage		2			V
V_{IH}	ECL high-level input voltage‡	0°C	−1170		−840	mV
		25°C	−1130		−810	
		75°C	−1070		−735	
V_{IL}	TTL low-level input voltage				0.8	V
V_{IL}	ECL low-level input voltage‡	0°C	−1950		−1480	mV
		25°C	−1950		−1480	
		75°C	−1950		−1450	
I_{IK}	TTL input clamp current				−18	mA
T_A	Operating ambient temperature (see Note 3)		0		75	°C

‡The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

NOTES: 2. If unused, $\overline{OE}1$ should be tied directly to −2 V.

3: Each 10KH series circuit has been designed to meet the dc specifications shown in the electrical characteristics table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board, and transverse air flow greater than 500 linear ft/min is maintained.

electrical characteristics over recommended operating ambient temperature range (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	A inputs and $\overline{OE}2$	V_{CC} = 4.5 V, V_{EE} = −4.94 V, I_I = −18 mA				−1.2	V
I_I	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = 7 V				0.1	mA
I_{IH}	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = 2.7 V				20	μA
	$\overline{OE}1$ only	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −840 mV	0°C			350	
		V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −810 mV	25°C			350	
		V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −735 mV	75°C			350	
I_{IL}	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = 0.5 V				−500	μA
	$\overline{OE}1$ only	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −1950 mV	0°C	0.5			
			25°C	0.5			
			75°C	0.5			
V_{OH}‡		V_{CC} = 4.5 V, V_{EE} = −5.2 V, ±5%, See Note 3	0°C	−1020		−840	mV
			25°C	−980		−810	
			75°C	−920		−735	
V_{OL}‡		V_{CC} = 4.5 V, V_{EE} = −5.2 V, ±5%, See Note 3	0°C	−1950		−1630	mV
			25°C	−1950		−1630	
			75°C	−1950		−1600	
I_{CCH}		V_{CC} = 5.5 V, V_{EE} = −5.46 V			15	22	mA
I_{CCL}		V_{CC} = 5.5 V, V_{EE} = −5.46 V			17	25	mA
I_{EE}		V_{CC} = 5.5 V, V_{EE} = −5.46 V			−78	−111	mA
C_i		V_{CC} = 5 V, V_{EE} = −5.2 V, f = 10 MHz			5		pF

switching characteristics over recommended ranges of operating ambient temperature and supply voltage (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	Any A	Y	0.1	1.7	3.7	ns
t_{PHL}			0.1	1.6	3.3	
t_{PLH}	$\overline{OE}1$ (ECL)	Y	0.8	2.8	5	ns
t_{PHL}			0.4	2.3	4.5	
t_{PLH}	$\overline{OE}2$ (TTL)	Y	0.8	3	5.3	ns
t_{PHL}			0.6	2.5	4.7	
t_r		Y		1.5		ns
t_f				1.5		

† All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

NOTES: 2. Each 10KH series circuit has been designed to meet the dc specifications shown in the electrical characteristics table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained.

3. Outputs are terminated through a 50-Ω resistor to −2 V.

4. Load circuit and switching waveforms are shown in Section 1.

electrical characteristics over recommended operating ambient temperature range (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	A inputs and $\overline{OE}2$	V_{CC} = 4.5 V, V_{EE} = −4.94 V, I_I = −18 mA				−1.2	V
I_I	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = 7 V				0.1	mA
I_{IH}	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = 2.7 V				20	μA
	$\overline{OE}1$ only	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −840 mV	0°C			350	
		V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −810 mV	25°C			350	
		V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −735 mV	75°C			350	
I_{IL}	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = 0.5 V				−500	μA
	$\overline{OE}1$ only	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −1950 mV	0°C	0.5			
			25°C	0.5			
			75°C	0.5			
V_{OH}‡		V_{CC} = 4.5 V, V_{EE} = −5.2 V, ±5%, See Note 3	0°C	−1020		−840	mV
			25°C	−980		−810	
			75°C	−920		−735	
V_{OL}‡		V_{CC} = 4.5 V, V_{EE} = −5.2 V, ±5%, See Note 3	0°C	−1950		−1630	mV
			25°C	−1950		−1630	
			75°C	−1950		−1600	
I_{CCH}		V_{CC} = 5.5 V, V_{EE} = −5.46 V			17	25	mA
I_{CCL}		V_{CC} = 5.5 V, V_{EE} = −5.46 V			15	22	mA
I_{EE}		V_{CC} = 5.5 V, V_{EE} = −5.46 V			−77	−111	mA
C_i		V_{CC} = 5 V, V_{EE} = −5.2 V, f = 10 MHz			5		pF

switching characteristics over recommended ranges of operating ambient temperature and supply voltage (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	Any A	Y	0.1	1.5	3	ns
t_{PHL}			0.1	1.5	3.3	
t_{PLH}	$\overline{OE}1$ (ECL)	Y	0.6	2.2	4.3	ns
t_{PHL}			0.5	2.4	4.3	
t_{PLH}	$\overline{OE}2$ (TTL)	Y	0.7	2.2	4.4	ns
t_{PHL}			0.5	2.6	4.7	
t_r		Y		1.5		ns
t_f				1.5		

† All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

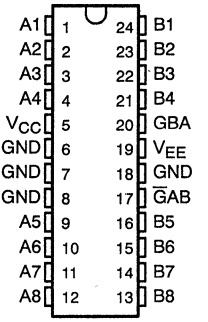
NOTES: 2. Each 10KH series circuit has been designed to meet the dc specifications shown in the electrical characteristics table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained.

3. Outputs are terminated through a 50-Ω resistor to −2 V.

4. Load circuit and voltage waveforms are shown in Section 1.

- **ECL and TTL Output-Enable Inputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN10KHT5562 and SN100KT5562 are noninverting TTL/ECL transceivers designed to translate signals between ECL and TTL environments. The A port (TTL port) is designed to source 15 mA and sink 48 mA. The B port (ECL port) is designed to drive a 50-Ω load terminated to –2 V.

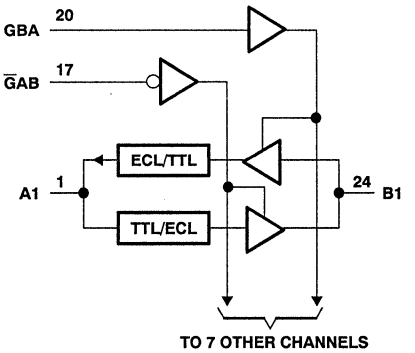
The A and B ports have complementary output-enable inputs, both of which are ECL-compatible. When the A-port output enable (GBA) is high, the device transmits data from the B bus to the A bus. When GBA is low, the A outputs are in the high-impedance state. When $\overline{G}$AB is low, the device transmits data from the A bus to the B bus; when $\overline{G}$AB is high, the B outputs are in the high-impedance state.

When GAB is low and $\overline{G}$BA is high, the device is in the isolation mode.

The SN10KHT5562 is compatible with 10KH ECL and is characterized for operation from 0°C to 75°C.

The SN100KT5562 is compatible with 100K ECL and is characterized for operation from 0°C to 85°C.

logic diagram (positive logic)



PRODUCT PREVIEW

- **ECL and TTL Output-Enable Inputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

description

The SN10KHT5563 and SN100KT5563 are inverting TTL/ECL transceivers designed to translate signals between ECL and TTL environments. The A port (TTL port) is designed to source 15 mA and sink 48 mA. The B port (ECL port) is designed to drive a 50-Ω load terminated to –2 V.

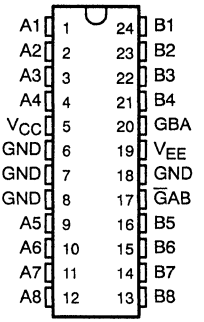
The A and B ports have complementary output-enable inputs, both of which are ECL-compatible. When the A-port output enable (GBA) is high, the device transmits data from the B bus to the A bus; when GBA is low, the A outputs are in the high-impedance state. When $\overline{G}$AB is low, the device transmits data from the A bus to the B bus; when $\overline{G}$AB is high, the B outputs are in the high-impedance state.

When GAB is low and $\overline{G}$BA is high, the device is in the isolation mode.

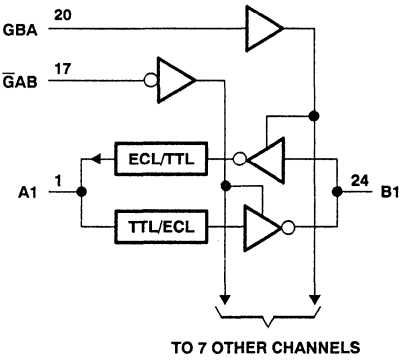
The SN10KHT5563 is compatible with 10KH ECL and is characterized for operation from 0°C to 75°C.

The SN100KT5563 is compatible with 100K ECL and is characterized for operation from 0°C to 85°C.

DW OR NT PACKAGE
(TOP VIEW)



logic diagram (positive logic)



PRODUCT PREVIEW

- **ECL and TTL Output-Enable Inputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

description

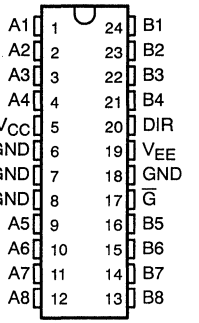
The SN10KHT5564 and SN100KT5564 are inverting TTL/ECL transceivers designed to translate signals between ECL and TTL environments. The A port (TTL port) is designed to source 15 mA and sink 48 mA. The B port (ECL port) is designed to drive a 50-Ω load terminated to –2 V.

When the output-enable input $\overline{G}$ is low, the device transmits data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control (DIR) input. When $\overline{G}$ is high, both buses are in the high-impedance state. Both $\overline{G}$ and DIR are ECL-compatible.

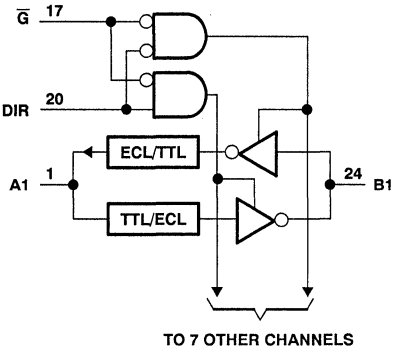
The SN10KHT5564 is compatible with 10KH ECL and is characterized for operation from 0°C to 75°C.

The SN100KT5564 is compatible with 100K ECL and is characterized for operation from 0°C to 85°C.

DW OR NT PACKAGE
(TOP VIEW)



logic diagram (positive logic)



PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **ECL and TTL Output-Enable Inputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

description

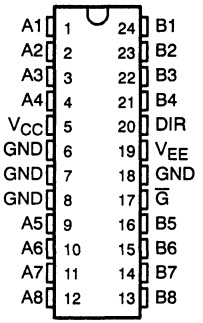
The SN10KHT5565 and SN100KT5565 are noninverting TTL/ECL transceivers designed to translate signals between ECL and TTL environments. The A port (TTL port) is designed to source 15 mA and sink 48 mA. The B port (ECL port) is designed to drive a 50-Ω load terminated to –2 V.

When the output-enable input $\overline{G}$ is low, the device transmits data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control (DIR) input. When $\overline{G}$ is high, both buses are in the high-impedance state. Both $\overline{G}$ and DIR are ECL-compatible.

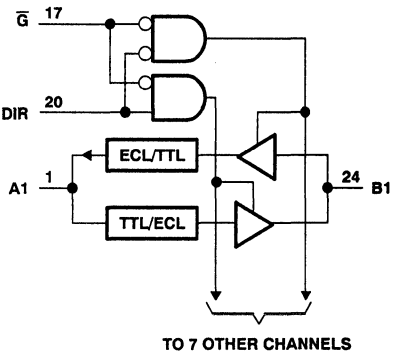
The SN10KHT5565 is compatible with 10KH ECL and is characterized for operation from 0°C to 75°C.

The SN100KT5565 is compatible with 100K ECL and is characterized for operation from 0°C to 85°C.

DW OR NT PACKAGE
(TOP VIEW)



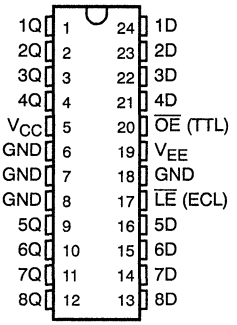
logic diagram (positive logic)



PRODUCT PREVIEW

- **10KH Compatible**
- **ECL and TTL Control Inputs**
- **Noninverting Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The eight latches of the SN10KHT5573 are transparent D-type latches. While latch enable ($\overline{LE}$) is low, the Q outputs follow the data (D) inputs. When $\overline{LE}$ is high, the Q outputs are latched at the levels that were set up at the D inputs.

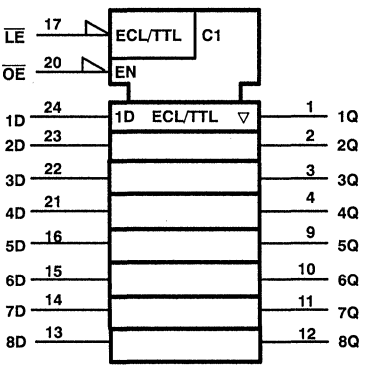
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive bus lines without need for interface or pullup components. Output-enable $\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN10KHT5573 is characterized for operation from 0° to 75°C.

FUNCTION TABLE

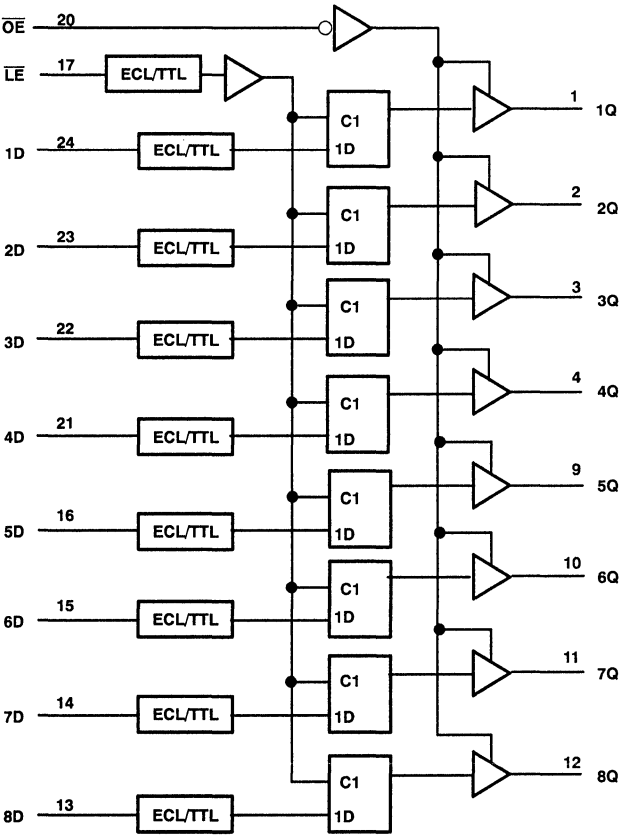
OUTPUT CONTROL		DATA INPUT	OUTPUT (TTL)
$\overline{OE}$	$\overline{LE}$	D	Q
L	L	L	L
L	L	H	H
L	H	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Supply voltage range, V_{EE} ..... – 8 V to 0 V
Input voltage range, TTL (see Note 1) ..... – 1.2 V to 7 V
Input voltage range, ECL ..... V_{EE} to 0 V
Input current range, TTL ..... – 30 mA to 5 mA
Current into any output in the low state ..... 96 mA
Voltage applied to any output in the disabled or power-off state ..... – 0.5 V to 5.5 V
Voltage applied to any output in the high state ..... – 0.5 V to V_{CC}
Operating free-air temperature range ..... 0°C to 75°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage		4.5	5	5.5	V
V_{EE}	ECL supply voltage		– 4.94	– 5.2	– 5.46	V
V_{IH}	TTL high-level input voltage		2			V
V_{IL}	TTL low-level input voltage				0.8	V
I_{IK}	TTL input clamp current				– 18	mA
V_{IH}	ECL high-level input voltage (see Note 2)	0°C	– 1170		– 840	mV
		25°C	– 1130		– 810	
		75°C	– 1070		– 735	
V_{IL}	ECL low-level input voltage (see Note 2)	0°C	– 1950		– 1480	mV
		25°C	– 1950		– 1480	
		75°C	– 1950		– 1450	
I_{OH}	High-level output current				– 15	mA
I_{OL}	Low-level output current				48	mA
T_A	Operating free-air temperature		0		75	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{OE}$ only	V_{CC} = 4.5 V,	V_{EE} = – 4.94 V,	I_I = – 18 mA				– 1.2	V
I_I	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_I = 7 V				0.1	mA
I_{IH}	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_I = 2.7 V				20	μA
I_{IL}	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_I = 0.5 V				– 0.5	mA
I_{IH}	Data inputs and $\overline{LE}$	V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_I = – 840 V	0°C			350	μA
		V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_I = – 810 V	25°C			350	
		V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_I = – 735 V	75°C			350	
I_{IL}	Data inputs and $\overline{LE}$	V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_I = – 1950 V	0°C	0.5			μA
					25°C	0.5			
					75°C	0.5			
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 3 mA,	V_{EE} = – 5.2 V ± 5%		2.4	3.3		V
		V_{CC} = 4.5 V,	I_{OH} = – 15 mA,	V_{EE} = – 5.2 V ± 5%		2	3.1		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA,	V_{EE} = – 5.2 V ± 5%			0.38	0.55	V
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V,	V_{EE} = – 5.46 V				50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.5 V,	V_{EE} = – 5.46 V				– 50	μA
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0 V,	V_{EE} = – 5.46 V		– 100		– 225	mA
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = – 5.46 V				62	89	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = – 5.46 V				78	111	mA
I_{CCZ}		V_{CC} = 5.5 V,	V_{EE} = – 5.46 V				75	108	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = – 5.46 V				– 34	– 48	mA
C_i		V_{CC} = 5 V,	V_{EE} = – 5.2 V				5		pF
C_o		V_{CC} = 5 V,	V_{EE} = – 5.2 V				7		pF

† All typical values are at V_{CC} = 5 V, V_{EE} = – 5.2 V, and T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements

		V_{CC} = 4.5 V to 5.5 V, V_{EE} = – 4.94 V to – 5.46 V, T_A = MIN to MAX§		UNIT
		MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ high	4		ns
t_{su}	Setup time, data before $\overline{LE}$↓	1		ns
t_h	Hold time, data after $\overline{LE}$↓	1		ns

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

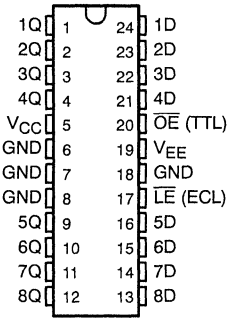
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX			UNIT
			MIN	TYP†	MAX	
t_{PLH}	D	Q	1.9	3.9	6.4	ns
t_{PHL}			2.3	4.2	6.8	
t_{PLH}	$\overline{LE}$	Q	2.2	4	6.7	ns
t_{PHL}			2.6	4.5	7.2	
t_{PZH}	$\overline{OE}$	Q	1.1	3.2	5.9	ns
t_{PZL}			2.3	4.6	7.8	
t_{PHZ}	$\overline{OE}$	Q	1.8	4	5.9	ns
t_{PLZ}			0.6	3.4	6.5	

† All typical values are at V_{CC} = 5 V, V_{EE} = – 5.2 V, and T_A = 25°C.
NOTE 3: Load circuit and voltage waveforms are shown in Section 1.7

- **100K Compatible**
- **ECL and TTL Control Inputs**
- **Noninverting Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 100K ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory address drivers, clock drivers, and bus oriented receivers and transmitters.

The eight latches of the SN100KT5573 are transparent D-type latches. While latch enable ($\overline{LE}$) is low, the Q outputs follow the data (D) inputs. When $\overline{LE}$ is high, the Q outputs are latched at the levels that were set up at the D inputs.

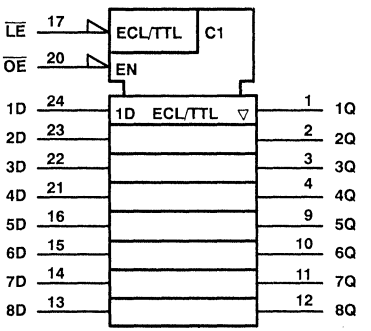
A buffered output-enable input ($\overline{OE}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. Output-enable $\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN100KT5573 is characterized for operation from 0° to 85° C.

FUNCTION TABLE

OUTPUT ENABLE		DATA INPUT	OUTPUT (TTL)
$\overline{OE}$	$\overline{LE}$	D	Q
L	L	L	L
L	L	H	H
L	H	X	Q_O
H	X	X	Z

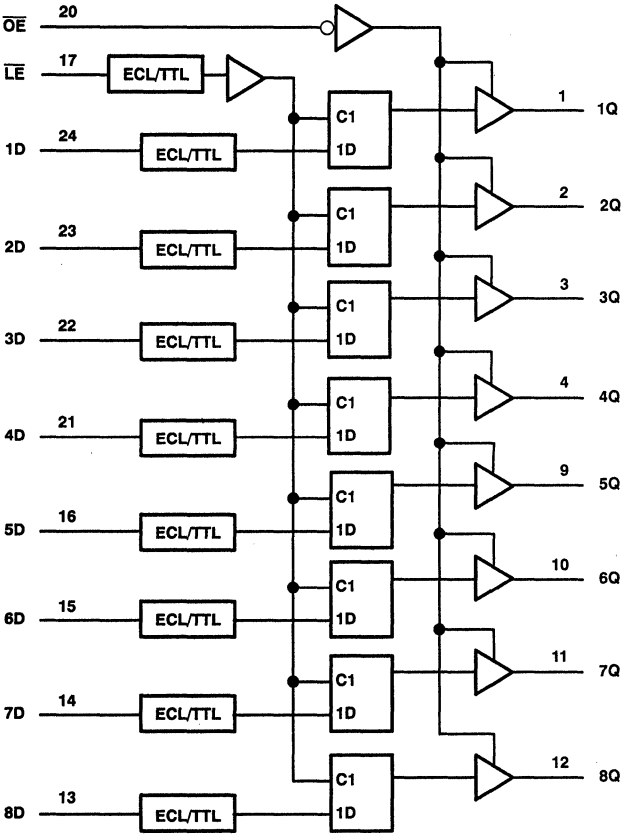
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Supply voltage range, V_{EE} ..... – 8 V to 0 V
Input voltage range, TTL (see Note 1) ..... – 1.2 V to 7 V
Input voltage range, ECL ..... V_{EE} to 0 V
Input current range, TTL ..... – 30 mA to 5 mA
Current into any output in the low state ..... 96 mA
Voltage applied to any output in the disabled or power-off state ..... – 0.5 V to 5.5 V
Voltage applied to any output in the high state ..... – 0.5 V to V_{CC}
Operating free-air temperature range ..... 0°C to 85°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage	4.5	5	5.5	V
V_{EE}	ECL supply voltage	−4.2	−4.5	−4.8	V
V_{IH}	TTL high-level input voltage	2			V
V_{IL}	TTL low-level input voltage			0.8	V
I_{IK}	TTL input clamp current			−18	mA
V_{IH}	ECL high-level input voltage†	−1150		−840	V
V_{IL}	ECL low-level input voltage†	−1810		−1490	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating temperature	0		85	°C

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}	$\overline{OE}$ only	V_{CC} = 4.5 V,	V_{EE} = −4.2 V,	I_I = −18 mA			−1.2	V
I_I	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = 7 V			0.1	mA
I_{IH}	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = 2.7 V			20	μA
I_{IL}	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = 0.5 V			−0.5	mA
I_{IH}	Data inputs and $\overline{LE}$	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_{IH} = −840 mV			350	μA
I_{IL}	Data inputs and $\overline{LE}$	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_{IL} = −1810 mV	0.50			μA
V_{OH}		V_{CC} = 4.5 V,	V_{EE} = −4.5 V ± 0.3 V,	I_{OH} = −3 mA	2.4	3.3		V
		V_{CC} = 4.5 V,	V_{EE} = −4.5 V ± 0.3 V,	I_{OH} = −15 mA	2	3.1		
V_{OL}		V_{CC} = 4.5 V,	V_{EE} = −4.5 V ± 0.3 V,	I_{OL} = 48 mA		0.38	0.55	V
I_{OZH}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_O = 2.7 V			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_O = 0.5 V			−50	μA
I_{OS}§		V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_O = 0 V	−100		−225	mA
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V			62	89	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V			77	111	mA
I_{CCZ}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V			75	108	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V			−34	−48	mA
C_i		V_{CC} = 5 V,	V_{EE} = −4.5 V			5		pF
C_o		V_{CC} = 5 V,	V_{EE} = −4.5 V			7		pF

‡ All typical values are at V_{CC} = 5 V, V_{EE} = −4.5 V, and T_A = 25°C.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

PRODUCT PREVIEW

timing requirements

		V_{CC} = 4.5 V to 5.5 V, V_{EE} = – 4.2 V to – 4.8 V, T_A = MIN to MAX†		UNIT
		MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ high	4		ns
t_{su}	Setup time, data before $\overline{LE}\downarrow$	1		ns
t_h	Hold time, data after $\overline{LE}\downarrow$	1		ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 2)

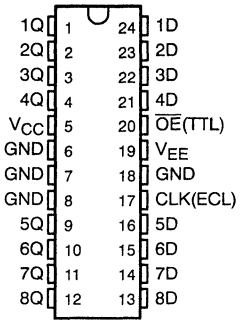
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX			UNIT
			MIN	TYP‡	MAX	
t_{PLH}	D	Q	1.9	3.9	6.4	ns
t_{PHL}			2.3	4.2	6.8	
t_{PLH}	$\overline{LE}$	Q	2.2	4	6.7	ns
t_{PHL}			2.6	4.5	7.2	
t_{PZH}	$\overline{OE}$	Q	1.1	3.2	5.9	ns
t_{PZL}			2.3	4.6	7.8	
t_{PHZ}	$\overline{OE}$	Q	1.8	4	5.9	ns
t_{PLZ}			0.6	3.4	6.5	

‡ All typical values are at V_{CC} = 5 V, V_{EE} = – 4.5 V, and T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

- **10KH Compatible**
- **ECL Clock and TTL Control Inputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The eight flip-flops of the SN10KHT5574 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels that were set up at the D inputs.

A buffered output-enable input ($\overline{OE}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

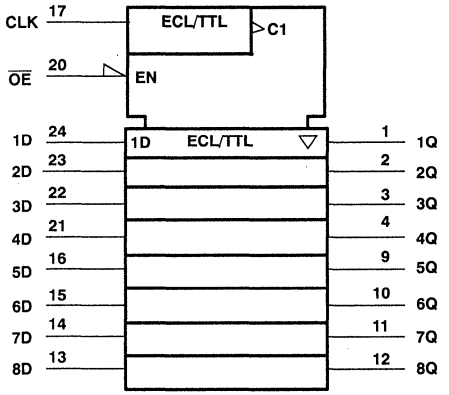
The output-enable input $\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN10KHT5574 is characterized for operation from 0°C to 75°C.

FUNCTION TABLE

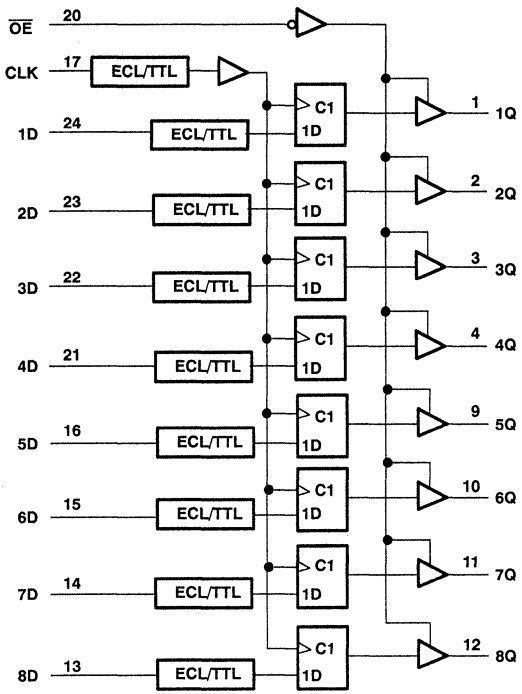
INPUTS			OUTPUT (TTL)
$\overline{OE}$	CLK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q_0
H	X	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Supply voltage range, V_{EE} ..... – 8 V to 0 V
Input voltage range: TTL (see Note 1) ..... – 1.2 V to 7 V
ECL ..... V_{EE} to 0 V
Voltage applied to any output in the disabled or power-off state ..... – 0.5 V to 5.5 V
Voltage applied to any output in the high state ..... – 0.5 V to V_{CC}
Input current range, (TTL) ..... – 30 mA to 5 mA
Current into any output in the low state ..... 96 mA
Operating free-air temperature range ..... 0°C to 75°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage		4.5	5	5.5	V
V_{EE}	ECL supply voltage		– 4.94	– 5.2	– 5.46	V
V_{IH}	TTL high-level input voltage		2			V
V_{IL}	TTL low-level input voltage				0.8	V
V_{IH}	ECL high-level input voltage‡	T_A = 0°C	– 1170		– 840	mV
		T_A = 25°C	– 1130		– 810	
		T_A = 75°C	– 1070		– 735	
V_{IL}	ECL low-level input voltage‡	T_A = 0°C	– 1950		– 1480	mV
		T_A = 25°C	– 1950		– 1480	
		T_A = 75°C	– 1950		– 1450	
I_{IK}	TTL input clamp current				– 18	mA
I_{OH}	High-level output current				– 15	mA
I_{OL}	Low-level output current				48	mA
T_A	Operating free-air temperature range		0		75	°C

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{OE}$ only	V_{CC} = 4.5 V,	V_{EE} = – 4.94 V,	I_I = – 18 mA				– 1.2	V
V_{OH}		V_{CC} = 4.5 V,	V_{EE} = – 5.2 V ±5%,	I_{OH} = – 3 mA		2.4	3.3		V
		V_{CC} = 4.5 V,	V_{EE} = – 5.2 V ±5%,	I_{OH} = – 15 mA		2	3.1		
V_{OL}		V_{CC} = 4.5 V,	V_{EE} = – 5.2 V ±5%,	I_{OL} = 48 mA			0.38	0.55	V
I_I	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_I = 7 V				0.1	mA
I_{IH}	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_I = 2.7 V				20	µA
I_{IL}	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_I = 0.5 V				– 0.5	mA
I_{IH}	Data inputs and CLK	V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_I = – 840 mV	T_A = 0°C			350	µA
		V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_I = – 810 mV	T_A = 25°C			350	
		V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_I = – 735 mV	T_A = 75°C			350	
I_{IL}	Data inputs and CLK	V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_I = – 1950 mV	T_A = 0°C	0.5			µA
					T_A = 25°C	0.5			
					T_A = 75°C	0.5			
I_{OZH}		V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_O = 2.7 V				50	µA
I_{OZL}		V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_O = 0.5 V				– 50	µA
I_{OS}‡		V_{CC} = 5.5 V,	V_{EE} = – 5.46 V,	V_O = 0 V		– 100		– 225	mA
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = – 5.46 V				66	95	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = – 5.46 V				76	110	mA
I_{CCZ}		V_{CC} = 5.5 V,	V_{EE} = – 5.46 V				74	106	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = – 5.46 V				– 43	– 61	mA
C_i		V_{CC} = 5.5 V,	V_{EE} = – 5.2 V,	f = 10 MHz			5		pF
C_o		V_{CC} = 5.5 V,	V_{EE} = – 5.2 V,	f = 10 MHz			7		pF

† All typical values are at V_{CC} = 5 V, V_{EE} = – 5.2 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements

			V_{CC} = 4.5 V to 5.5 V, V_{EE} = – 4.94 V to – 5.46 V, T_A = MIN to MAX§		UNIT
			MIN	MAX	
t_w	Pulse duration	CLK high	4		ns
		CLK low	4		
t_{su}	Setup time before CLK↑	Data high	1		ns
		Data low	1		
t_h	Hold time after CLK↑	Data high	1		ns
		Data low	1		

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

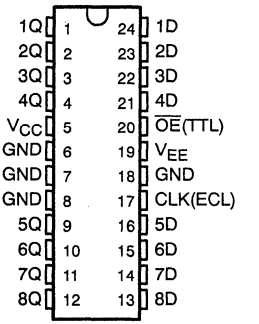
switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
f_{max}			200	300		MHz
t_{PLH}	CLK	Q	2.3	4.1	7	ns
t_{PHL}			2.9	4.6	7.4	
t_{PZH}	$\overline{OE}$	Q	1.9	3.6	6.3	ns
t_{PZL}			2.7	4.8	7.7	
t_{PHZ}	$\overline{OE}$	Q	2.1	3.9	6.1	ns
t_{PLZ}			0.5	3.4	6.3	

† All typical values are at V_{CC} = 5 V, V_{EE} = – 5.2 V, T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

- **100K Compatible**
- **ECL Clock and TTL Control Inputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 100K ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The eight flip-flops of the SN100KT5574 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels that were set up at the D inputs.

A buffered output-enable input ($\overline{OE}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

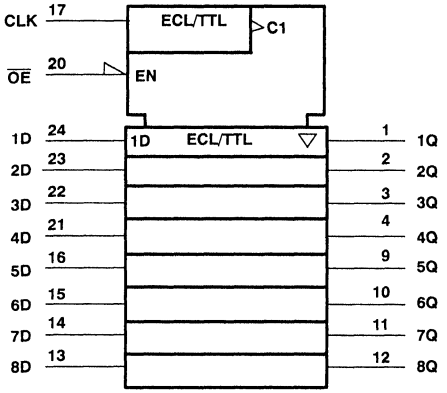
The output-enable input $\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN100KT5574 is characterized for operation from 0°C to 85°C.

FUNCTION TABLE

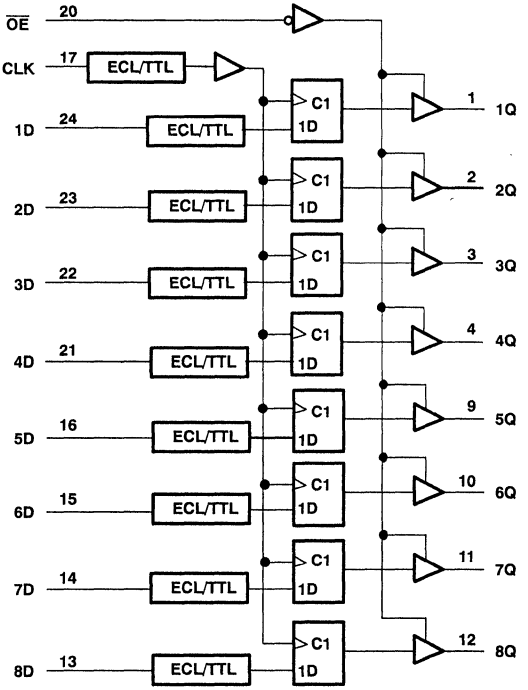
INPUTS			OUTPUT (TTL)
$\overline{OE}$	CLK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Supply voltage range, V_{EE} ..... – 8 V to 0 V
Input voltage range: TTL (see Note 1) ..... – 1.2 V to 7 V
ECL ..... V_{EE} to 0 V
Voltage applied to any output in the disabled or power-off state ..... – 0.5 V to 5.5 V
Voltage applied to any output in the high state ..... – 0.5 V to V_{CC}
Input current range, TTL ..... – 30 mA to 5 mA
Current into any output in the low state ..... 96 mA
Operating free-air temperature range ..... 0°C to 85°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage	4.5	5	5.5	V
V_{EE}	ECL supply voltage	– 4.2	– 4.5	– 4.8	V
V_{IH}	TTL high-level input voltage	2			V
V_{IL}	TTL low-level input voltage			0.8	V
I_{IK}	TTL input clamp current			– 18	mA
V_{IH}	ECL high-level input voltage‡	– 1150		– 840	mV
V_{IL}	ECL low-level input voltage‡	– 1810		– 1490	mV
I_{OH}	High-level output current			– 15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating temperature range	0		85	°C

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{OE}$ only	V_{CC} = 4.5 V,	V_{EE} = – 4.2 V,	I_I = – 18 mA			– 1.2	V
V_{OH}		V_{CC} = 4.5 V,	V_{EE} = – 4.5 V ± 0.3 V,	I_{OH} = – 3 mA	2.4	3.3		V
		V_{CC} = 4.5 V,	V_{EE} = – 4.5 V ± 0.3 V,	I_{OH} = – 15 mA	2	3.1		
V_{OL}		V_{CC} = 4.5 V,	V_{EE} = – 4.5 V ± 0.3 V,	I_{OL} = 48 mA		0.38	0.55	V
I_I	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_I = 7 V			0.1	mA
I_{IH}	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_I = 2.7 V			20	µA
I_{IL}	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_I = 0.5 V			– 0.5	mA
I_{IH}	Data inputs and CLK	V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_{IH} = – 840 mV			350	µA
I_{IL}	Data inputs and CLK	V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_{IL} = – 1810 mV	0.50			µA
I_{OZH}		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_O = 2.7 V			50	µA
I_{OZL}		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_O = 0.5 V			– 50	µA
I_{OS}‡		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_O = 0 V	– 100		– 225	mA
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V			66	95	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V			76	110	mA
I_{CCZ}		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V			74	106	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V			– 43	– 61	mA
C_i		V_{CC} = 5.5 V,	V_{EE} = – 4.5 V			5		pF
C_o		V_{CC} = 5.5 V,	V_{EE} = – 4.5 V			7		pF

† All typical values are at V_{CC} = 5 V, V_{EE} = – 4.5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements

			V_{CC} = 4.5 V to 5.5 V, V_{EE} = – 4.2 V to – 4.8 V, T_A = MIN to MAX§		UNIT
			MIN	MAX	
t_w	Pulse duration	CLK high	4		ns
		CLK low	4		
t_h	Hold time after CLK↑	Data high	1		ns
		Data low	1		
t_{su}	Setup time before CLK↑	Data high	1		ns
		Data low	1		

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

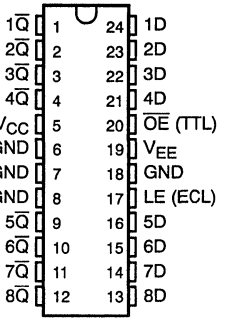
switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
f_{max}			200	300		MHz
t_{PLH}	CLK	Q	2.3	4.1	7	ns
t_{PHL}			2.9	4.6	7.4	
t_{PZH}	$\overline{OE}$	Q	1.9	3.6	6.3	ns
t_{PZL}			2.7	4.8	7.7	
t_{PHZ}	$\overline{OE}$	Q	2.1	3.9	6.1	ns
t_{PLZ}			0.5	3.4	6.3	

† All typical values are at V_{CC} = 5 V, V_{EE} = – 4.5 V, T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

- **ECL and TTL Control Inputs**
- **Inverting Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC}, V_{EE}, and GND Configuration Minimizes High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN10KHT5575 and SN100KT5575 are octal ECL-to-TTL inverting translators designed to provide efficient translation between 10KH or 100K ECL signal environments, respectively, and a TTL signal environment. These devices are designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory address drivers, clock drivers, receivers, and transmitters.

The eight latches of the '5575 are transparent D-type latches. When latch enable (LE) is high, the $\overline{Q}$ outputs follow the complements of the data (D) inputs. When LE is taken low, the $\overline{Q}$ outputs are latched at the inverse of the levels that were set up at the D inputs.

A buffered output-enable input ($\overline{OE}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive give the device the capability to drive bus lines without need for interface or pullup components. The $\overline{OE}$ input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

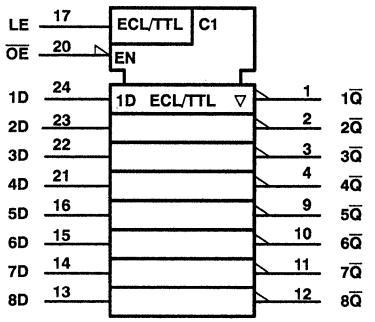
The SN10KHT5575 is compatible with 10KH ECL and is characterized for operation from 0°C to 75°C. The SN100KT5575 is compatible with 100K ECL and is characterized for operation from 0°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT (TTL)
$\overline{OE}$	LE	D	$\overline{Q}$
L	L	L	H
L	L	H	L
L	H	X	$\overline{Q}_0$
H	X	X	Z

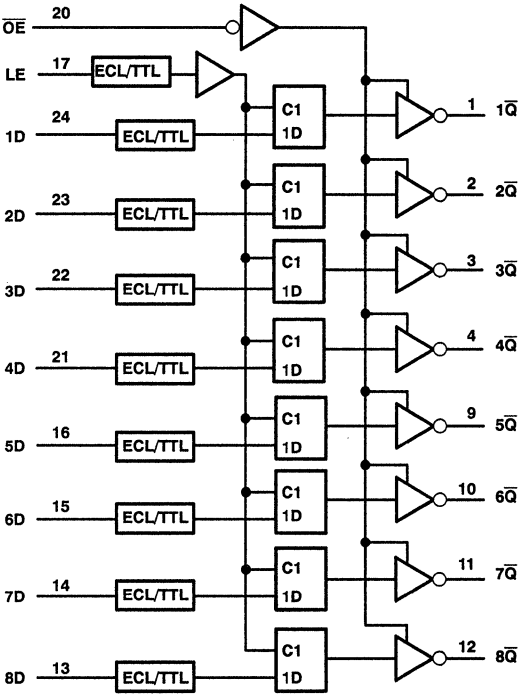
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

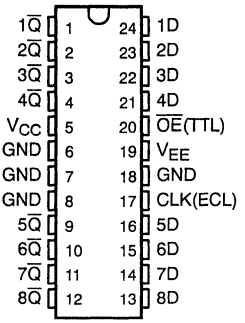
logic diagram (positive logic)



PRODUCT PREVIEW

- **ECL and TTL Control Inputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC}, V_{EE}, and GND Configuration Minimizes High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN10KHT5576 and SN100KT5576 are octal ECL-to-TTL inverting translators designed to provide efficient translation between an ECL signal environment and a TTL signal environment. These devices are designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory address drivers, clock drivers, receivers, and transmitters.

The eight flip-flops of the '5576 are edge-triggered D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs take on the complement of the logic levels that were set up at the D inputs. A buffered output-enable input ($\overline{OE}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive give the device the capability to drive bus lines without need for interface or pullup components. The $\overline{OE}$ input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

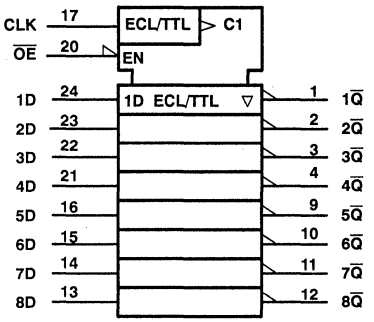
The SN10KHT5576 is compatible with 10KH ECL and is characterized for operation from 0°C to 75°C. The SN100KT5576 is compatible with 100K ECL and is characterized for operation from 0°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT (TTL)
$\overline{OE}$	CLK	D	$\overline{Q}$
L	↑	L	H
L	↑	H	L
L	L	X	$\overline{Q}_0$
H	X	X	Z

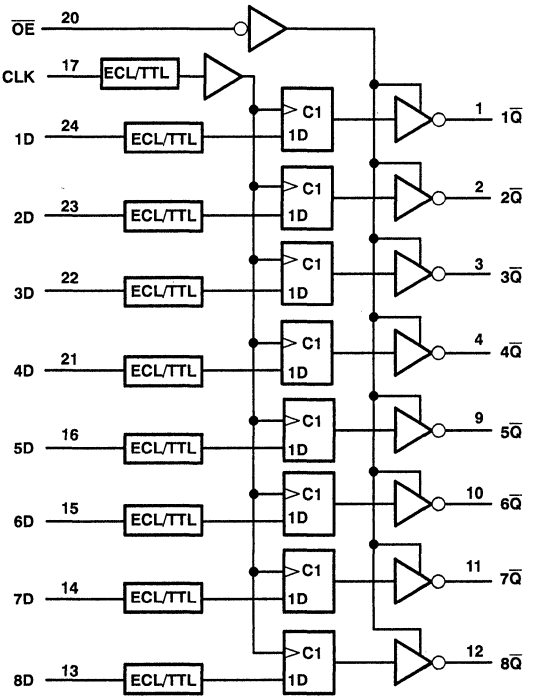
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

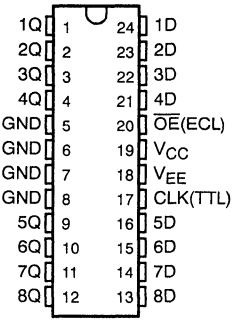
logic diagram (positive logic)



- **10KH Compatible**
- **TTL Clock and ECL Control Inputs**
- **Noninverting Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic DIPs**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**

DW OR NT PACKAGE

(TOP VIEW)



description

This octal TTL-to-ECL translator is designed to provide efficient translation between a TTL signal environment and a 10KH ECL signal environment. This device is designed specifically to improve the performance and density of TTL-to-ECL CPU/bus-oriented functions such as memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The eight flip-flops of the '5578 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels that were set up at the D inputs.

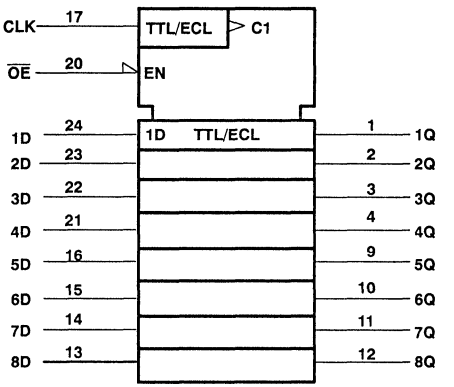
The output-control input $\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN10KHT5578 is characterized for operation from 0°C to 75°C.

FUNCTION TABLE

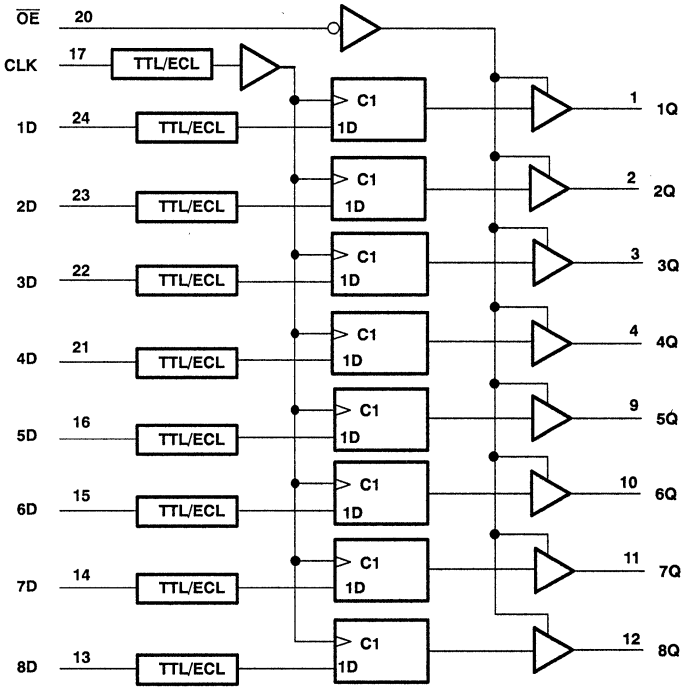
INPUTS			OUTPUT (ECL)
$\overline{OE}$	CLK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q_0
H	X	X	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Supply voltage range, V_{EE} ..... – 8 V to 0 V
Input voltage range (TTL) (see Note 1) ..... – 1.2 V to 7 V
Input voltage range (ECL) ..... V_{EE} to 0 V
Input current range (TTL) ..... – 30 mA to 5 mA
Current out of any output ..... 50 mA
Operating ambient temperature range ..... 0°C to 75°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage		4.5	5	5.5	V
V_{EE}	ECL supply voltage		−4.94	−5.2	−5.46	V
V_{IH}	TTL high-level input voltage		2			V
V_{IH}	ECL high-level input voltage†	0°C	−1170		−840	mV
		25°C	−1130		−810	mV
		75°C	−1070		−735	mV
V_{IL}	TTL low-level input voltage				0.8	V
V_{IL}	ECL low-level input voltage†	0°C	−1950		−1480	mV
		25°C	−1950		−1480	mV
		75°C	−1950		−1450	mV
I_{IK}	TTL input clamp current				−18	mA
T_A	Operating ambient temperature (see Note 2)		0		75	°C

electrical characteristics over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{IK}	D inputs and CLK	V_{CC} = 4.5 V,	V_{EE} = −4.94 V,	I_I = −18 mA				−1.2	V
I_I	D inputs and CLK	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 7 V				0.1	mA
I_{IH}	D inputs and CLK	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 2.7 V				20	μA
I_{IL}	D inputs and CLK	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 0.5 V				−0.5	mA
I_{IH}	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −840 V	0°C			350	μA
		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −810 V	25°C			350	
		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −735 V	75°C			350	
I_{IL}	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −1950 V	0°C	0.5			μA
					25°C	0.5			
					75°C	0.5			
V_{OH}†		V_{CC} = 4.5 V,	V_{EE} = −5.2 V ± 5%,	See Note 3	0°C	−1020		−840	mV
					25°C	−980		−810	
					75°C	−920		−735	
V_{OL}†		V_{CC} = 4.5 V,	V_{EE} = −5.2 V ± 5%,	See Note 3	0°C	−1950		−1630	mV
					25°C	−1950		−1630	
					75°C	−1950		−1600	
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				17.5	25	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				15	22	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				−104	−149	mA
C_i		V_{CC} = 5 V,	V_{EE} = −5.2 V,	f = 10 MHz			4		pF

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.
‡ All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.

NOTES: 2. Each 10KH series circuit has been designed to meet the dc specifications shown in the electrical characteristics table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board, and transverse air flow greater than 500 linear ft/min is maintained.
3. Outputs are terminated through a 50-Ω resistor to −2 V.

timing requirements

			V_{CC} = 4.5 V to 5.5 V, V_{EE} = −4.94 V to −5.46 V, T_A = MIN to MAX†		UNIT
			MIN	MAX	
f_{clock}	Clock frequency		0	180	MHz
t_w	Pulse duration, CLK	High	4		ns
		Low	4		
t_{su}	Setup time, data before CLK↑	High	1.5		ns
		Low	2.5		
t_h	Hold time, data after CLK↑	High	1		ns
		Low	1		

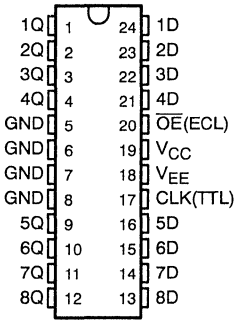
switching characteristics over recommended ranges of supply voltage and operating ambient temperature (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
f_{max}			180			MHz
t_{PLH}	CLK	Q	0.8	2.2	4	ns
t_{PHL}			0.8	2.1	3.8	
t_{PLH}	$\overline{OE}$	Q	0.5	1.4	3.2	ns
t_{PHL}			0.5	1.7	3.3	
t_r		Y		1.5		ns
t_f		Y		1.5		ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.
NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

- **100K Compatible**
- **TTL Clock and ECL Control Inputs**
- **Noninverting Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic DIPs**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**

DW OR NT PACKAGE
(TOP VIEW)



description

This octal TTL-to-ECL translator is designed to provide efficient translation between a TTL signal environment and a 100K ECL signal environment. This device is designed specifically to improve the performance and density of TTL-to-ECL CPU/bus-oriented functions such as memory-address drivers,clock drivers, and bus-oriented receivers and transmitters.

The eight flip-flops of the '5578 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels that were set up at the D inputs.

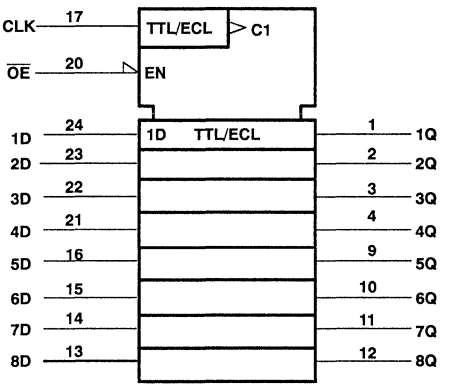
The output-control input $\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN100KT5578 is characterized for operation from 0°C to 85°C.

Function Table

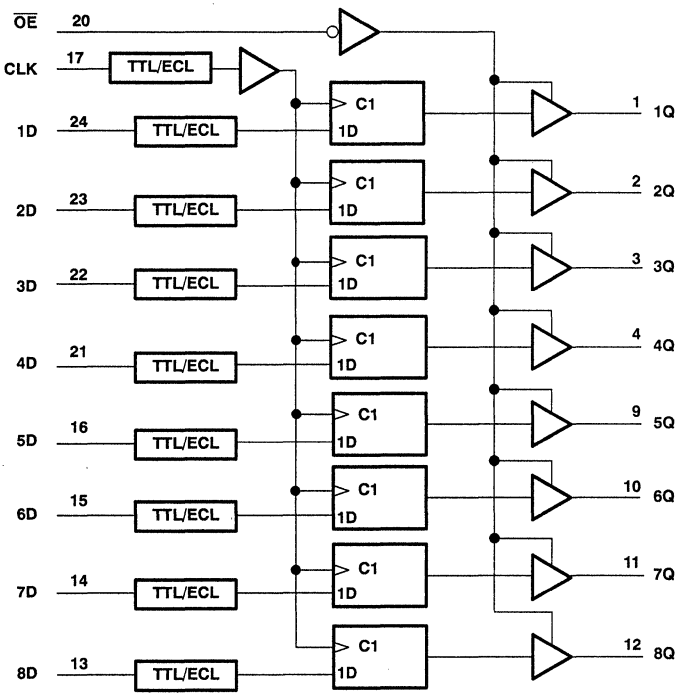
INPUTS			OUTPUT (ECL)
$\overline{OE}$	CLK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q_0
H	X	X	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Supply voltage range, V_{EE} . . . . . – 8 V to 0 V
Input voltage range (TTL) (see Note 1) . . . . . – 1.2 V to 7 V
Input voltage range (ECL) . . . . . V_{EE} to 0 V
Input current range (TTL) . . . . . – 30 mA to 5 mA
Current out of any output . . . . . 50 mA
Operating ambient temperature range . . . . . 0°C to 85°C
Storage temperature range . . . . . – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage	4.5	5	5.5	V
V_{EE}	ECL supply voltage	– 4.2	– 4.5	– 4.8	V
V_{IH}	TTL high-level input voltage	2			V
V_{IL}	TTL low-level input voltage			0.8	V
I_{IK}	TTL input clamp current			– 18	mA
V_{IH}	ECL high-level input voltage‡	– 1165		– 880	mV
V_{IL}	ECL low-level input voltage‡	– 1810		– 1475	mV
T_A	Operating ambient temperature (see Note 2)	0		85	°C

electrical characteristics over recommended operating ambient temperature range (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS			MIN	TYP§	MAX	UNIT
V_{IK}	D inputs and CLK	V_{CC} = 4.5 V,	V_{EE} = – 4.2 V,	I_I = – 18 mA			– 1.2	V
I_I	D inputs and CLK	V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_I = 7 V			0.1	mA
I_{IH}	D inputs and CLK	V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_I = 2.7 V			20	µA
I_{IL}	D inputs and CLK	V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_I = 0.5 V			– 0.5	mA
I_{IH}	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_{IH} = – 880 mV			350	µA
I_{IL}	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = – 4.8 V,	V_{IL} = – 1810 mV	0.50			µA
V_{OH}‡		V_{CC} = 4.5 V,	V_{EE} = – 4.5 V ± 0.3 V,	See Note 3	– 1020		– 880	mV
V_{OL}‡		V_{CC} = 4.5 V,	V_{EE} = – 4.5 V ± 0.3 V,	See Note 3	– 1810		– 1620	mV
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V			17	24	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V			14.5	21	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = – 4.8 V			– 104	– 149	mA
C_i		V_{CC} = 5 V,	V_{EE} = – 4.5 V,	f = 10 MHz		4		pF

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

§ All typical values are at V_{CC} = 5 V, V_{EE} = – 4.5 V, T_A = 25°C.

NOTES: 2. Each 100KT series circuit has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained.

3. Outputs are terminated through a 50-Ω resistor to – 2 V.

timing requirements

			V_{CC} = 4.5 V to 5.5 V, V_{EE} = – 4.2 V to – 4.8 V, T_A = MIN to MAX†		UNIT
			MIN	MAX	
f_{clock}	Clock frequency		0	180	MHz
t_w	Pulse duration, CLK	High	1.5		ns
		Low	2.5		
t_{su}	Setup time, data before CLK↑	High	4		ns
		Low	4		
t_h	Hold time, data after CLK↑	High	1		ns
		Low	1		

switching characteristics over recommended ranges of supply voltage and operating ambient temperature (see Note 4)

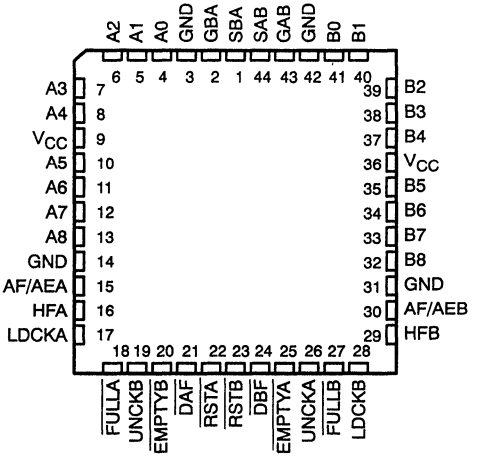
PARAMETER	FROM (IINPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
f_{max}			180			MHz
t_{PLH}	CLK	Q	0.8	2.3	4.1	ns
t_{PHL}			0.8	2.2	3.8	
t_{PLH}	$\overline{OE}$	Q	0.5	1.4	3	ns
t_{PHL}			0.5	1.7	3.4	
t_r		Y		1.5		ns
t_f		Y		1.5		ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, V_{EE} = – 4.5 V, T_A = 25°C.
NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

FIFO Products

- Independent Asynchronous Inputs and Outputs
- Low-Power Advanced CMOS Technology
- Bidirectional
- 1024 Words by 9 Bits Each
- Programmable Almost Full/Almost Empty Flag
- Empty, Full, and Half-Full Flags
- Access Times of 25 ns With a 50-pF Load
- Data Rates From 0 to 40 MHz
- Fall-Through Time . . . 22 ns Typ
- High Output Drive for Direct Bus Interface

FN PACKAGE
(TOP VIEW)



description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ACT2235 is arranged as two 1024- by 9-bit FIFOs for high speed and fast access times. It processes data at rates from 0 to 40 MHz with access times of 25 ns in a bit-parallel format.

The 'ACT2235 consists of bus transceiver circuits, two 1024 X 9 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. GAB and GBA enable inputs are provided to control the transceiver functions. The SAB and SBA control inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transistion between stored and real-time data. Eight fundamental bus-management functions can be performed as shown on the operating modes page.

PRODUCT PREVIEW

functional description

Bus Lines (A0-A8, B0-B8). Data inputs and outputs for 9-bit-wide data.

Resets ($\overline{RSTA}$, $\overline{RSTB}$). A reset is accomplished in each direction by taking reset inputs $\overline{RSTA}$ and $\overline{RSTB}$ low. This initializes the empty flags $\overline{EMPTYA}$ and $\overline{EMPTYB}$ and the half-full flags HFA and HFB low. The full flags $\overline{FULLA}$ and $\overline{FULLB}$ and the almost full/almost empty flags (AF/AEA) and (AF/AEB) are initialized high. Both FIFOs must be reset upon power up.

Load Clocks (LDCKA, LDCKB). Data on the A bus (A0-A8) is written into FIFO A on a low-to-high transition of load clock A (LDCKA). Data on the B bus (B0-B8) is written into FIFO B on a low-to-high transition of load clock B (LDCKB). When the FIFOs are full, load clock signals have no effect on the data residing in memory.

Unload Clocks (UNCKA, UNCKB). Data in FIFO A is read to the B bus (B0-B8) on a low-to-high transition of unload clock A (UNCKA). Data in FIFO B is read to the A bus (A0-A8) on a low-to-high transition of unload clock B (UNCKB). When the FIFOs are empty, unload clock signals have no effect on data residing in memory.

G Enables (GAB, GBA). The G enables (GAB and GBA) control the transceiver output functions. When GBA is low, the A bus (A0-A8) is in the high-impedance state. When GAB is low, the B bus (B0-B8) is in the high-impedance state.

S Control Inputs (SAB, SBA). The S control inputs (SAB and SBA) select whether real-time or stored data is transferred. A low level selects real-time data, and a high level selects stored data. Eight fundamental bus-management functions can be performed as shown in the operating modes page.

Define Flag Inputs ($\overline{DAF}$, $\overline{DBF}$). The high-to-low transition of define A flag ($\overline{DAF}$) stores the binary value on the A bus (A0-A8) as the almost empty/almost full offset value for FIFO A (X). The high-to-low transition of define B flag ($\overline{DBF}$) stores the binary value of the B bus (B0-B8) as the almost full/almost empty offset value for FIFO B (Y).

Empty Flags ($\overline{EMPTYA}$, $\overline{EMPTYB}$). The empty flags ($\overline{EMPTYA}$ and $\overline{EMPTYB}$) are low when their corresponding memories are empty and high when they are not empty.

Full Flags ($\overline{FULLA}$, $\overline{FULLB}$). The full flags $\overline{FULLA}$ and $\overline{FULLB}$ are low when their corresponding memories are full and high when they are not full.

Half-Full Flags (HFA, HFB). The half-full flags (HFA and HFB) are high when their corresponding memories contain 512 or more words and low when they contain 511 or less words.

Almost Full/Almost Empty flags (AF/AEA), (AF/AEB). The almost full/almost empty A flag (AF/AEA) is defined by the almost full/almost empty offset value for FIFO A (X). The AF/AEA flag is high when FIFO A contains X or less words or 1024 minus X words. The AF/AEA flag is low when FIFO A contains between X plus 1 or 1023 minus X words. The operation of the almost full/almost empty B flag (AF/AEB) is the same as AF/AEA for FIFO B.

Programming Procedure for AF/AEA

The almost full/almost empty flags (AF/AEA and AF/AEB) are programmed during each reset cycle. The almost full/almost empty offset value for FIFO A (X) and for FIFO B (Y) are either a user-defined value or the default values of X = 256 and Y = 256. Below are instructions to program AF/AEA using both methods. AF/AEB is programmed in the same manner for FIFO B.

User Defined X

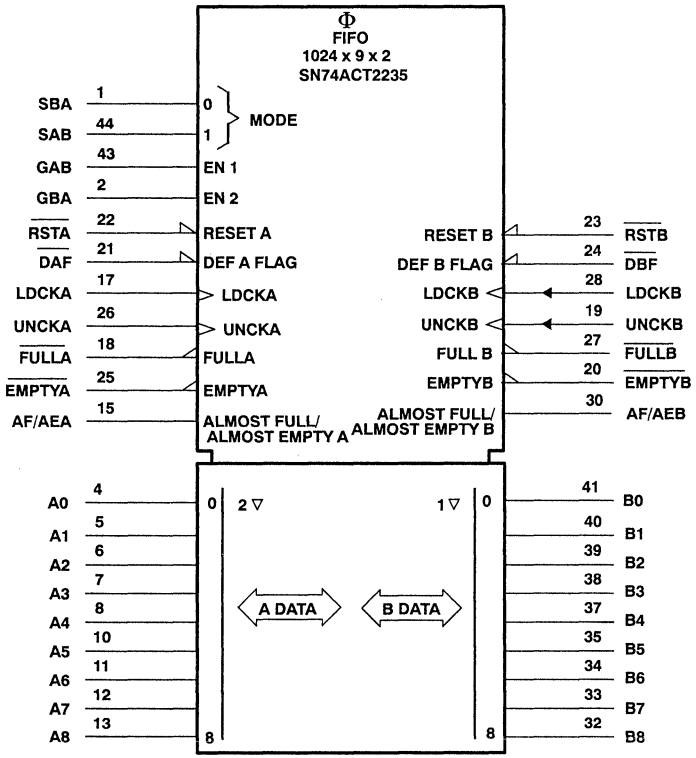
Step 1: Take $\overline{DAF}$ from high to low. This stores A0 thru A8 as X.
Step 2: If $\overline{RSTA}$ is not already low, take $\overline{RSTA}$ low.
Step 3: With $\overline{DAF}$ held low, take $\overline{RSTA}$ high. This defines the AF/AEA flag using X.
Step 4: To retain the current offset for the next reset, keep $\overline{DAF}$ low.

Default X

To redefine the AF/AE flag using the default value of X = 256, hold $\overline{DAF}$ high during the reset cycle.

PRODUCT PREVIEW

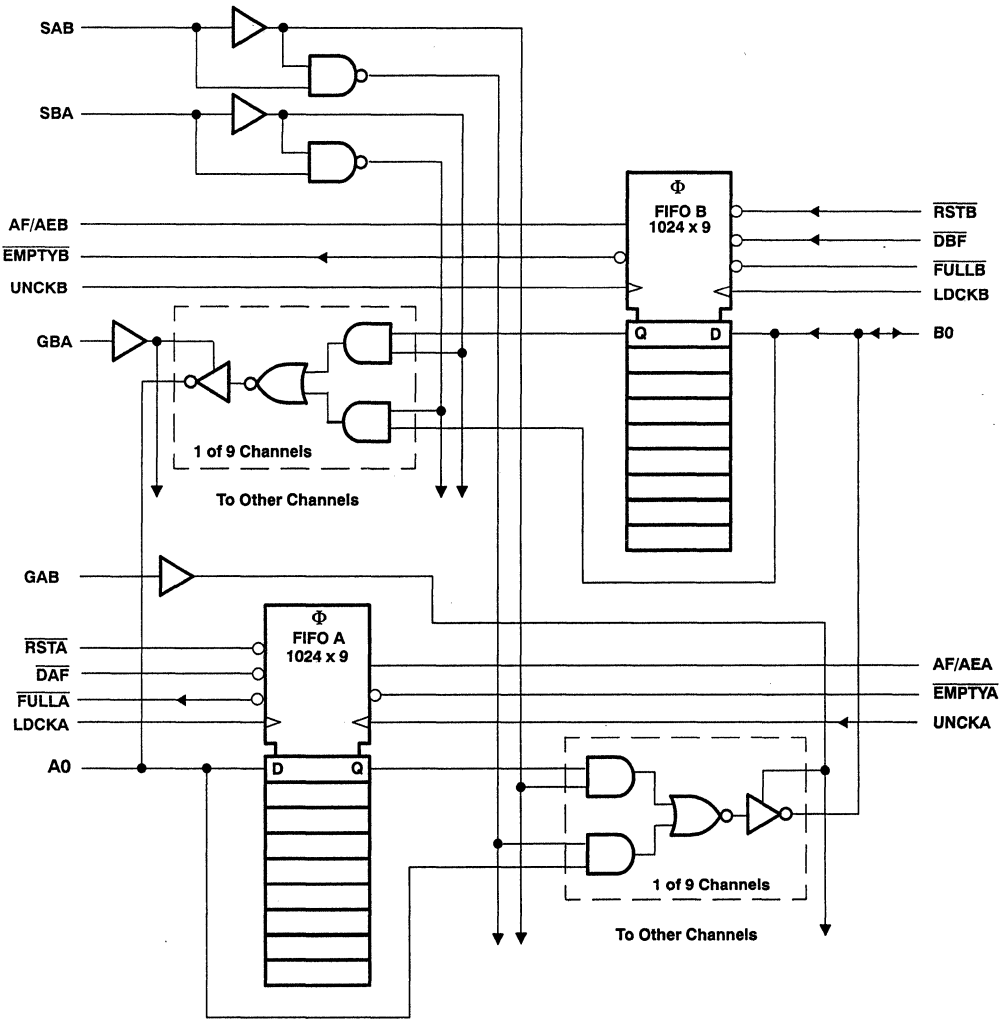
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

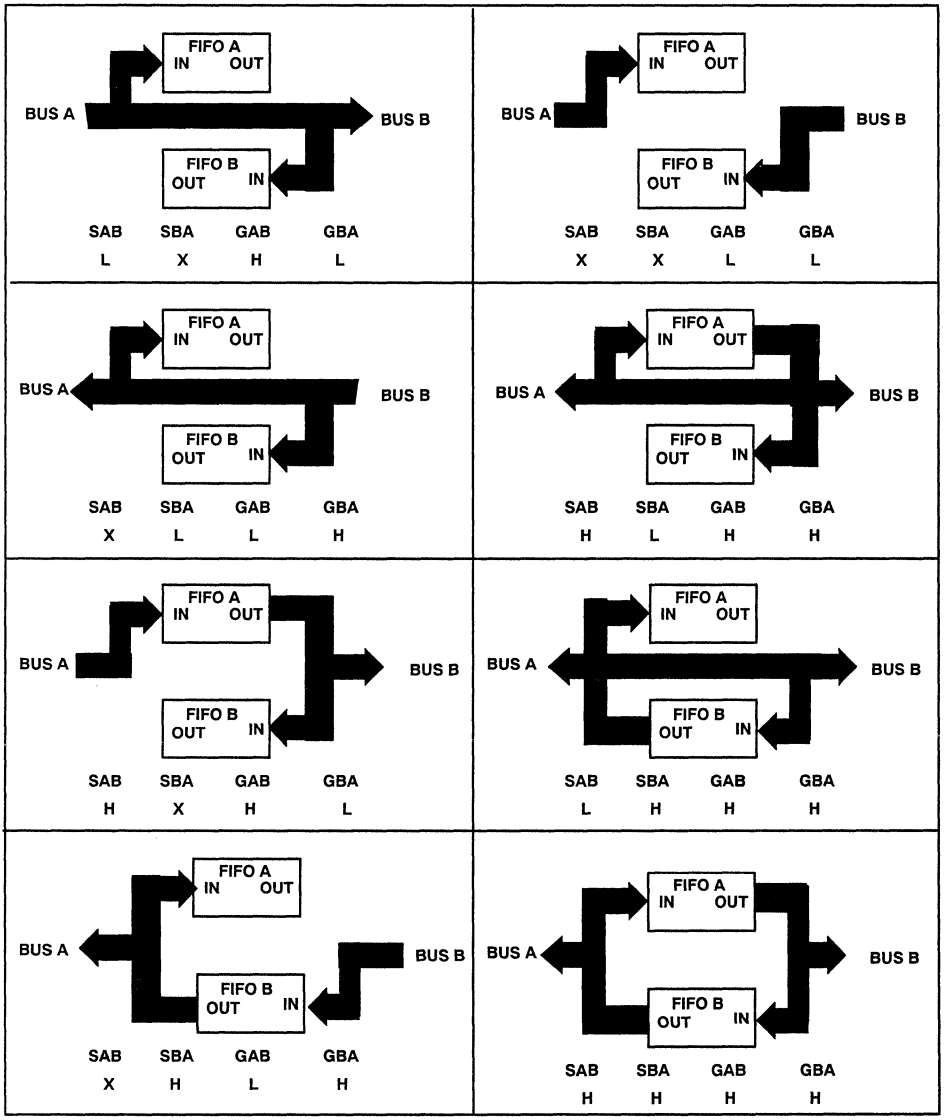
PRODUCT PREVIEW

logic diagram (positive logic)



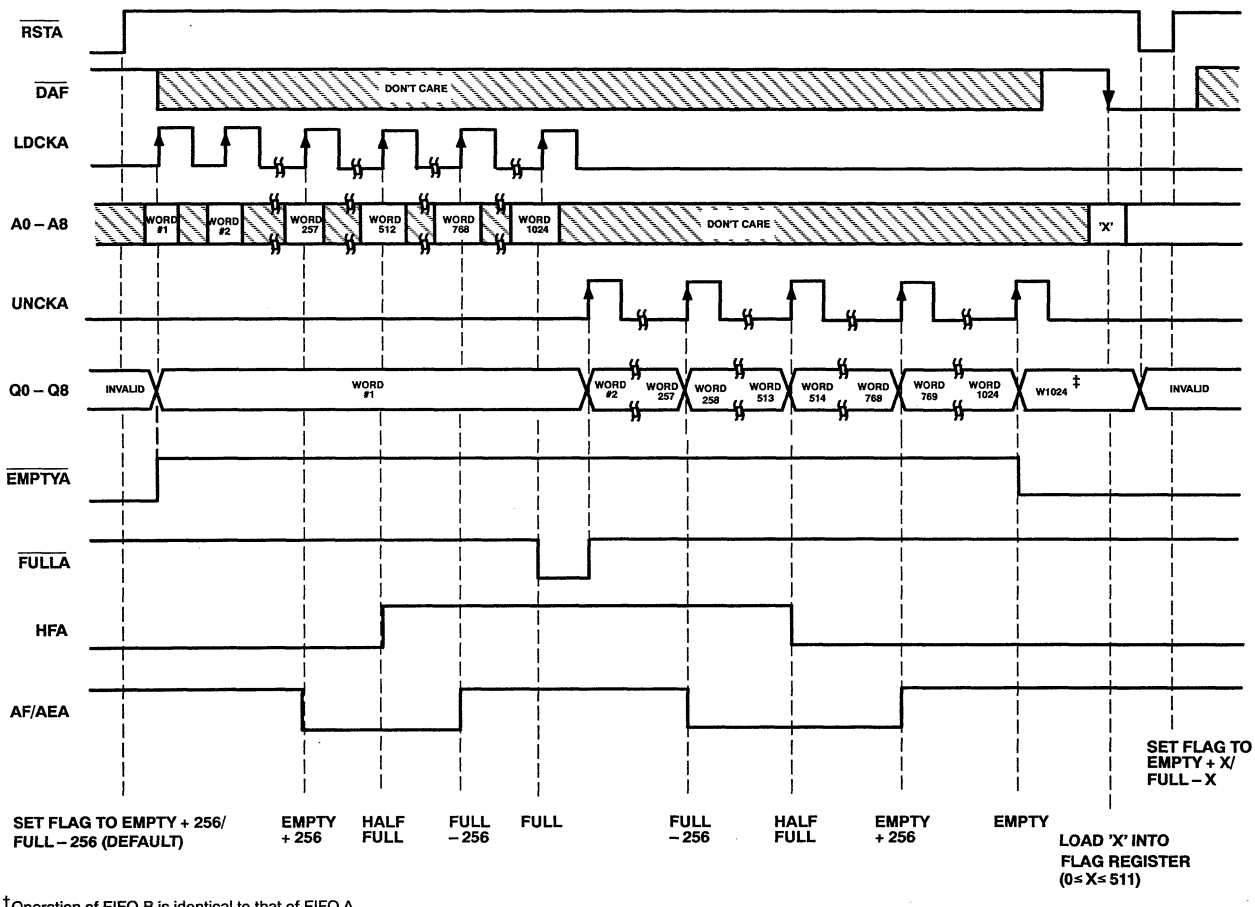
PRODUCT PREVIEW

operating modes



timing diagram

FIFO A TIMING DIAGRAM†



†Operation of FIFO B is identical to that of FIFO A

‡ Last valid data stays on outputs when FIFO goes empty due to a read.

TEXAS INSTRUMENTS
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SELECT MODE CONTROL TABLE

CONTROL		OPERATION	
SBA	SAB	A Bus	B Bus
L	L	Real Time B to A Bus	Real Time A to B Bus
H	L	FIFO B to A Bus	Real Time A to B Bus
L	H	Real Time B to A Bus	FIFO A to B Bus
H	H	FIFO B to A Bus	FIFO A to B Bus

OUTPUT ENABLE CONTROL TABLE

ENABLE		OPERATION	
GBA	GAB	A Bus	B Bus
H	H	A Bus Enabled	B Bus Enabled
H	L	A Bus Enabled	Isolation/Input to B Bus
L	H	Isolation/Input to A Bus	B Bus Enabled
L	L	Isolation/Input to A Bus	Isolation/Input to B Bus

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage: Control inputs ..... 7 V
I/O ports ..... 5.5 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	V
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
I_{OH}	High-level output current	A or B ports				−8	mA
		Status flags				−8	
I_{OL}	Low-level output current	A or B ports				16	mA
		Status flags				8	
f_{clock}	Clock frequency	LDCKA or LDCKB		0		40	MHz
		UNCKA or UNCKB		0		40	
t_w	Pulse duration	$\overline{RSTA}$ or $\overline{RSTB}$ low					ns
		LDCKA or LDCKB	high				
			low				
		UNCKA or UNCKB	high				
			low				
		$\overline{DAF}$ or $\overline{DBF}$ high					
t_{su}	Setup time	Data before LDCKA or LDCKB↑					ns
		Define AF/AE: D0-D8 before $\overline{DAF}$ or $\overline{DBF}$↓					
		Define AF/AE: $\overline{DAF}$ or $\overline{DBF}$↓ before $\overline{RSTA}$ or $\overline{RSTB}$↑					
		Define AF/AE (Default): $\overline{DAF}$ or $\overline{DBF}$ high before $\overline{RSTA}$ or $\overline{RSTB}$↑					
		$\overline{RSTA}$ or $\overline{RSTB}$ inactive (high) before LDCKA or LDCKB↑					
t_h	Hold time	Data after LDCKA or LDCKB↑					ns
		Define AF/AE: D0-D8 after $\overline{DAF}$ or $\overline{DBF}$↓					
		Define AF/AE: $\overline{DAF}$ or $\overline{DBF}$ low after $\overline{RSTA}$ or $\overline{RSTB}$↑					
		Define AF/AE (Default): $\overline{DAF}$ or $\overline{DBF}$ high after $\overline{RSTA}$ or $\overline{RSTB}$↑					
		$\overline{RSTA}$ or $\overline{RSTB}$ inactive (high) after LDCKA or LDCKB↑					
T_A	Operating free-air temperature			0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −8 mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} =16 mA			0.5	V
I_I	Input current	V_{CC} = 5.5 V,	V_I = V_{CC} or 0 V			±5	μA
I_{OZ}	High-impedance-state output current	V_{CC} = 5.5 V,	V_O = V_{CC} or 0 V			±5	μA
I_{CC1}‡	Supply current	f_{clock} = 25 MHz§			200	230	mA
I_{CC2}‡	Standby current	LDCKA or LDCKB = V_{IH},	V_I = V_{IH} or V_{IL}		20	25	mA
I_{CC3}‡	Power down current	V_I = V_{CC} − 0.2 V or 0 V				400	μA
C_i	Input capacitance	V_I = 0 V,	f = 1 MHz		4		pF
C_o	Output capacitance	V_O = 0 V,	f = 1 MHz		8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I_{CC} tested with outputs open.
§ For frequencies greater than 25 MHz, I_{CC} = 200 mA + (6 mA • [f − 25]).

PRODUCT PREVIEW

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†						UNIT
			ACT2235-XX			ACT2235-35		ACT2235-28.5	
			MIN	TYP‡	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK		40							MHZ
	UNCK		40							
t_{pd}	LDCKA↑, LDCKB↑	B, A		22						ns
t_{pd}	UNCKA↑, UNCKB↑	B, A		20						ns
t_{PLH}	LDCKA↑, LDCKB↑	$\overline{EMPTYA}$, $\overline{EMPTYB}$		12						ns
t_{PHL}	UNCKA↑, UNCKB↑	$\overline{EMPTYA}$, $\overline{EMPTYB}$		12						ns
t_{PHL}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	$\overline{EMPTYA}$, $\overline{EMPTYB}$		12						ns
t_{PHL}	LDCKA↑, LDCKB↑	$\overline{FULLA}$, $\overline{FULLB}$		12						ns
t_{PLH}	UNCKA↑, UNCKB↑	$\overline{FULLA}$, $\overline{FULLB}$		12						ns
t_{PLH}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	$\overline{FULLA}$, $\overline{FULLB}$		15						ns
t_{PLH}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	AF/AEA, AF/AEB								ns
t_{PLH}	LDCKA↑, LDCKB↑	HFA, HFB								ns
t_{PHL}	UNCKA↑, UNCKB↑	HFA, HFB								ns
t_{PHL}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	HFA, HFB								ns
t_{pd}	SAB, SBA§	B, A		11						ns
t_{pd}	A, B	B, A		8						ns
t_{pd}	LDCKA↑, LDCKB↑	AF/AEA, AF/AEB		6						ns
t_{pd}	UNCKA↑, UNCKB↑	AF/AEA, AF/AEB		5						ns
t_{en}	GBA, GAB	A, B		6						ns
t_{dis}	GBA, GAB	A, B		5						ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at 5 V, T_A = 25°C.
§ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

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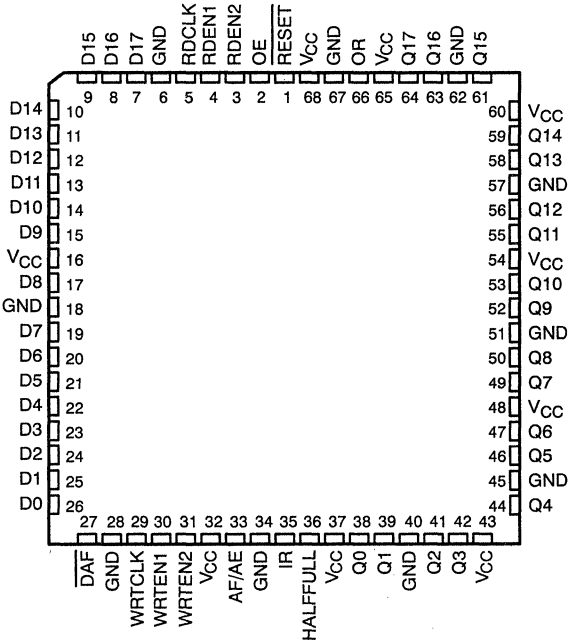
- Independent Asynchronous Inputs and Outputs
- 1024 Words by 18 Bits Each
- Read and Write Operations Can Be Synchronized to Independent System Clocks
- Programmable Almost Full/Almost Empty Flag
- Input Ready, Output Ready, and Half Full Flags
- Cascadable in Word Width and/or Word Depth
- Fast Access Times of 15 ns With a 50-pF Load
- High Output Drive for Direct Bus Interface
- 3-State Q Outputs

FN PACKAGE
(TOP VIEW)



description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7801 is a 1024 by 18-bit FIFO for high speed and fast access times. It processes data at rates up to 40 MHz and access times of 15 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word-width and word-depth.

The SN74ACT7801 has normal input bus to output bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent read and write (interrupts, requests) to their respective system clock.

inputs

Data In (D0-D17) – Data inputs for 18-bit wide data to be stored in the memory. Data lines D0-D8 also carry the Almost Full/Almost Empty Offset Value (X) on a high-to-low transition of Define Almost Full ($\overline{DAF}$).

Reset ($\overline{RESET}$) – A reset is accomplished by taking Reset ($\overline{RESET}$) low and generating a minimum of four Read Clock (RDCLK) and Write Clock (WRTCLK) cycles. This ensures that the internal read and write pointers are reset and that the Output Ready flag (OR), the Half Full flag (HF), and the Input Ready flag (IR) are low; the Almost Full/Almost Empty flag (AF/AE) is high. The FIFO must be reset upon power up. With the Define Almost Full ($\overline{DAF}$) at a low level, a low pulse on $\overline{RESET}$ defines the AF/AE status flag using the Almost Full/Almost Empty Offset Value (X), where X is the value previously stored. With $\overline{DAF}$ at a high level, a low level pulse on $\overline{RESET}$ defines the AF/AE flag using the default value of X = 256.

Write Enables (WRTEN1, WRTEN2) –The Write Enables (WRTEN1, WRTEN2) must be high before the rising edge of Write Clock (WRTCLK) for a word to be written into memory. The Write Enables do not affect the storage of the Almost Full/Almost Empty Offset Value (X).

Write Clock (WRTCLK) – Data is written into memory on a low-to-high transition of the Write Clock (WRTCLK) if the Input Ready status flag (IR) and the Write Enable control signals (WRTEN1, WRTEN2) are high. WRTCLK is a free running clock and functions as the synchronizing clock for all data transfers into the FIFO. The IR status flag is also driven synchronously with respect to the WRTCLK signal.

Read Enables (RDEN1, RDEN2) – Both Read Enables (RDEN1, RDEN2) must be high before the rising edge of Read Clock (RDCLK) to read a word out of memory. The Read Enables are not used to read the first word stored in memory.

Read Clock (RDCLK) – Data is read out of memory on a low-to-high transition at the Read Clock (RDCLK) input if the Output Ready status flag (OR), the Output Enable (OE), and the Read Enable control signals (RDEN1, RDEN2) are high. RDCLK is a free running clock and functions as the synchronizing clock for all data transfers out of the FIFO. The OR flag is also driven synchronously with respect to the RDCLK signal.

Define Almost Full ($\overline{DAF}$) – The high-to-low transition of the Define Almost Full ($\overline{DAF}$) input stores the binary value of Data Inputs D0-D8 as the Almost Full/Almost Empty Offset Value (X). With $\overline{DAF}$ held low, a low pulse on the Reset ($\overline{RESET}$) defines the Almost Full/Almost Empty flag (AF/AE) using X.

Output Enable (OE) – Data Out (Q0-Q17) and the Output Ready flag (OR) are at a high-impedance state when the Output Enable (OE) is low. OE must be high before the rising edge of Read Clock (RDCLK) to read a word from memory.

outputs

Data Out (Q0-Q17) – The first data word to be loaded into the FIFO is moved to the Data Out (Q0-Q17) register on the rising edge of the third Read Clock (RDCLK) pulse to occur after the first valid write. The Read Enable (RDEN1, RDEN2) inputs do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, and the Output Ready flag (OR) are high.

Input Ready Flag (IR) – The Input Ready Flag (IR) is high when the FIFO is not full and low when the device is full. During reset, the IR flag is set low on the rising edge of the second Write Clock (WRTCLK) pulse. The IR flag is set high on the rising edge of the second WRTCLK pulse after reset $\overline{RESET}$ goes high. After the FIFO is filled and IR is set low, IR is set high on the second WRTCLK pulse to occur after the first valid read.

Output Ready Flag (OR) – The Output Ready Flag (OR) is high when the FIFO is not empty and low when it is empty. During reset, the OR flag is set low on the rising edge of the third Read Clock (RDCLK) pulse. The OR flag is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.

Half Full Status Flag (HF) – The Half Full flag (HF) is high when the FIFO contains 513 or more words and is low when it contains 512 or less words.

Almost Full/Almost Empty Status Flag (AF/AE) – The Almost Full/Almost Empty flag (AF/AE) is defined by the Almost Full/Almost Empty Offset Value (X). The AF/AE flag is high when the FIFO contains X + 1 or less words, or 1025 minus X or more words. The AF/AE flag is low when the FIFO contains between X + 2 and 1024 minus X words.

Programming Procedure for AF/AE – The Almost Full/Almost Empty flag (AF/AE) is programmed during each reset cycle. The Almost Full/Almost Empty Offset Value (X) is either a user-defined value or the default value of X = 256. Below are instructions to program AF/AE using both methods.

User-Defined X

Step 1. Take $\overline{DAF}$ from high to low.

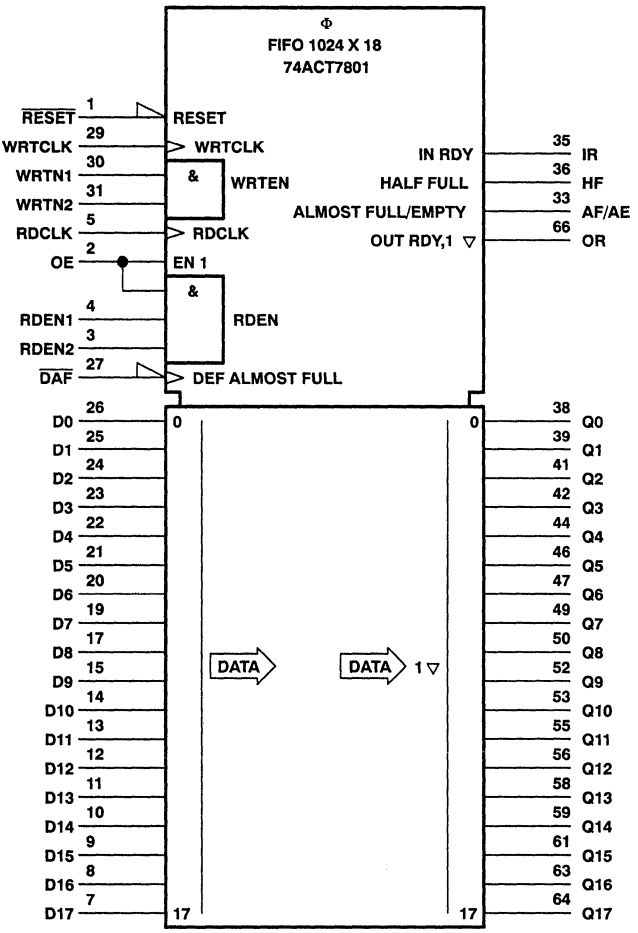
Step 2. If $\overline{RESET}$ is not already low, take $\overline{RESET}$ low.

Step 3. With $\overline{DAF}$ held low, take $\overline{RESET}$ high. This defines the AF/AE flag using X.

Step 4. To retain the current offset for the next reset, keep $\overline{DAF}$ low.

Default X – To redefine the AF/AE flag using the default value of X = 256, hold $\overline{DAF}$ high during the reset cycle.

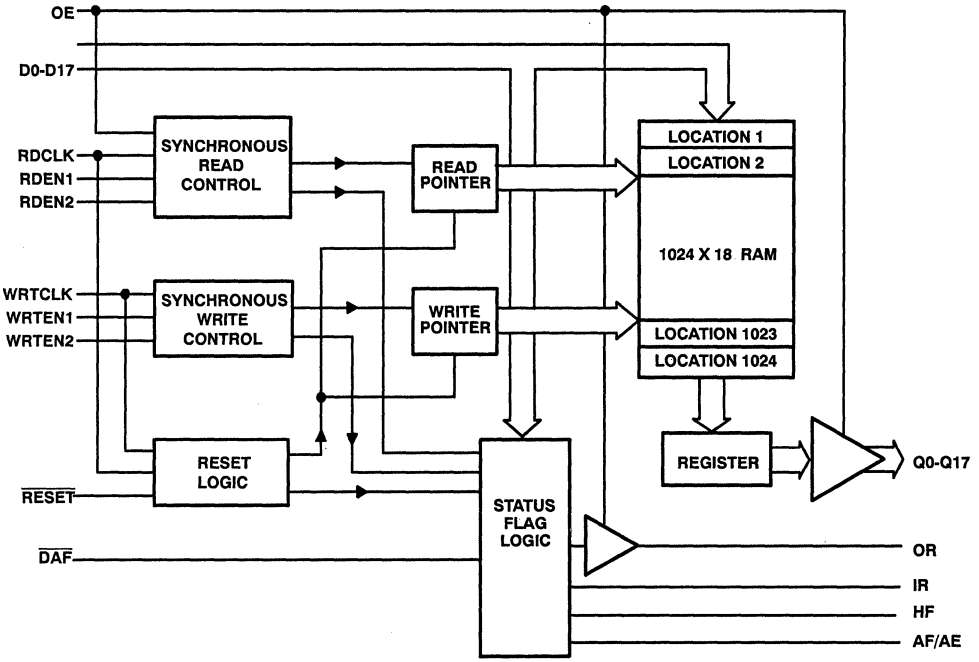
logic symbol†



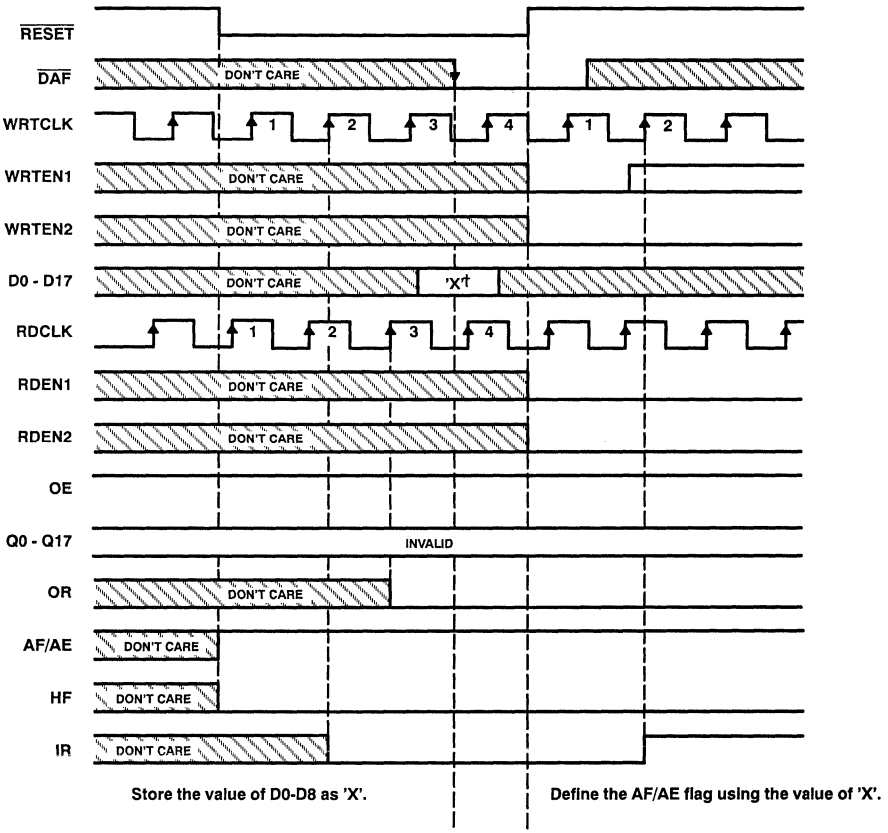
† This symbol is in accordance with ANSI/IEEE Std 91-1984.

D3489, APRIL 1990

functional block diagram



timing diagram



† 'X' is the binary value of D0 – D8 only

Figure 1. Reset Cycle: Define AF/AE Using the Value of 'X'

timing diagram

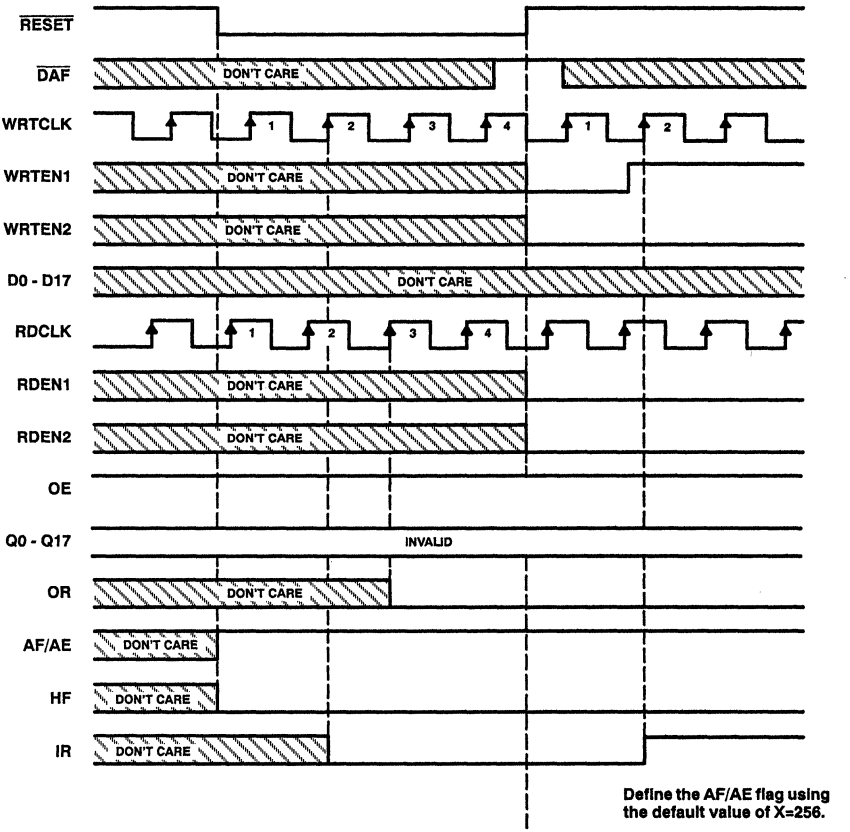


Figure 2. Reset Cycle: Define AF/AE Using the Default

timing diagram

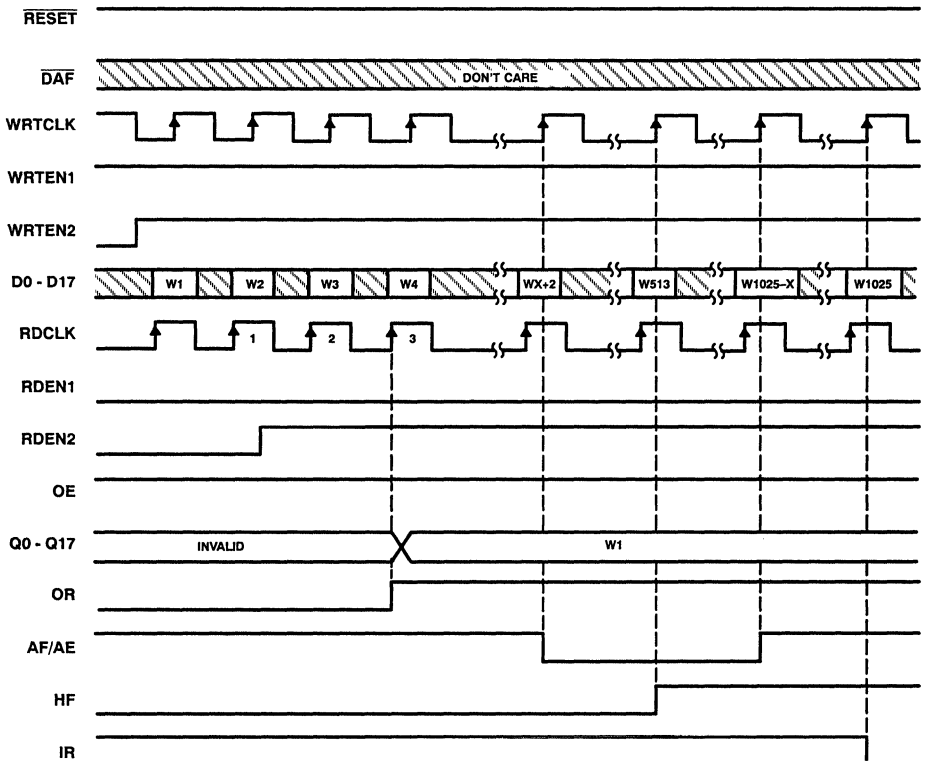


Figure 3. Write

timing diagram

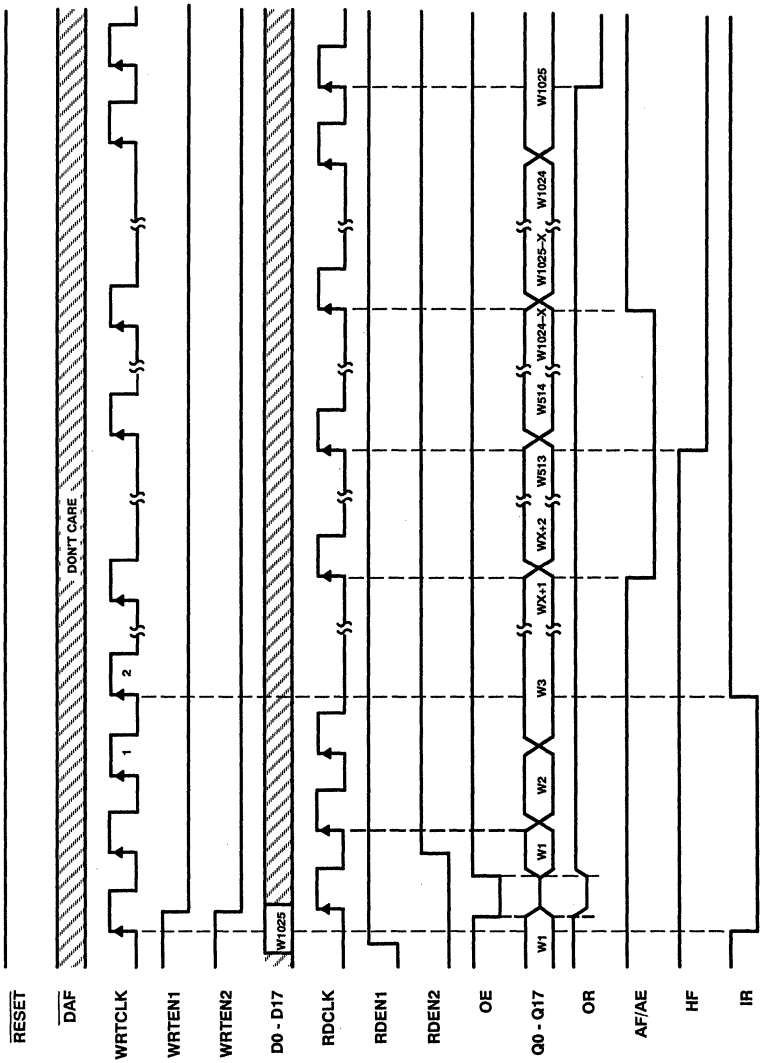


Figure 4. Read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Input voltage ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER			ACT7801-15		ACT7801-18		ACT7801-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8	V
I_{OH}	High-level output current			– 8		– 8		– 8	mA
I_{OL}	Low-level output current			16		16		16	mA
f_{clock}	Clock frequency		40		35		28.5		MHz
t_w	Pulse duration	Data in (D0-D17), high or low	10		12		14		ns
		WRTCLK high	7		8.5		10		
		WRTCLK low	15		15		15		
		RDCLK high	7		8.5		10		
		RDCLK low	15		15		15		
		$\overline{DAF}$ high	10		10		10		
		WRTEN1, WRTEN2 high or low	10		10		10		
		OE, RDEN1, RDEN2 high or low	10		10		10		
t_{su}	Setup time	Data in (D0-D17) before WRTCLK↑	5		5		5		ns
		WRTEN1, WRTEN2 before WRTCLK↑	5		5		5		
		OE, RDEN1, RDEN2 before RDCLK↑	5		5		5		
		RESET: $\overline{RESET}$ low before first WRTCLK and RDCLK↑	7		7		7		
		Define AF/AE: D0-D8 before $\overline{DAF}$↓	5		5		5		
		Define AF/AE: $\overline{DAF}$↓ before $\overline{RESET}$↑	7		7		7		
		Define AF/AE (default): $\overline{DAF}$ high before $\overline{RESET}$↑	5		5		5		
t_h	Hold time	Data in (D0-D17) after WRTCLK↑	1		1		1		ns
		WRTEN1, WRTEN2 after WRTCLK↑	1		1		1		
		OE, RDEN1, RDEN2 after RDCLK↑	1		1		1		
		RESET: $\overline{RESET}$ low after fourth WRTCLK and RDCLK↑	0		0		0		
		Define AF/AE: D0-D8 after $\overline{DAF}$↓	1		1		1		
		Define AF/AE: $\overline{DAF}$ low after $\overline{RESET}$↑	0		0		0		
		Define AF/AE (default): $\overline{DAF}$ high after $\overline{RESET}$↑	1		1		1		
T_A	Operating free-air temperature		0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = – 8 mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 16 mA			0.5	V
I_I	Input current	V_{CC} = 5.5 V,	V_I = V_{CC} or 0			± 5	μA
I_{OZ}	High-impedance-state output current	V_{CC} = 5.5 V,	V_O = V_{CC} or 0			± 5	μA
I_{CC1}‡	Supply current	f_{clock} = 25 MHz§			200	230	mA
I_{CC2}‡	Supply current, standby	WRTCLK = V_{IH},	V_I = V_{IH} or V_{IL}		20	25	mA
I_{CC3}‡	Supply current, power down	V_I = V_{CC} – 0.2 V or 0				400	μA
C_i		V_I = 0,	f = 1 MHz		4		pF
C_o		V_O = 0,	f = 1 MHz		8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I_{CC} tested with outputs open.
§ For frequencies greater than 25 MHz, I_{CC} = 200 mA + (6 mA • [f – 25 MHz]).

switching characteristics over recommended operating free-air temperature range (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 0°C to 70°C							UNIT
			ACT7801-15			ACT7801-18		ACT7801-20		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		40			35		28.5		MHz
t_{pd}	RDCLK↑	Any Q	5	12	15	5	18	5	20	ns
t_{pd}¶	RDCLK↑	Any Q		10.5						ns
t_{pd}	WRTCLK↑	IR	4		10	4	12	4	14	ns
t_{pd}	RDCLK↑	OR	4		10	4	12	4	14	ns
t_{pd}	WRTCLK↑	AF/AE	7		20	7	22	7	24	ns
t_{pd}	RDCLK↑	AF/AE	7		20	7	22	7	24	ns
t_{pd}	WRTCLK↑	HF	6		19	6	21	6	23	ns
t_{pd}	RDCLK↑	HF	6		19	6	21	6	23	ns
t_{PLH}	$\overline{RESET}$↓	AF/AE	4		19	4	21	4	23	ns
t_{PHL}	$\overline{RESET}$↓	HF	4		21	4	23	4	25	ns
t_{en}	OE	Any Q, OR	2		11	2	11	2	11	ns
t_{dis}	OE	Any Q, OR	2		14	2	14	2	14	ns

¶ This parameter is measured at 30 pF (see Figure 5).
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL CHARACTERISTICS

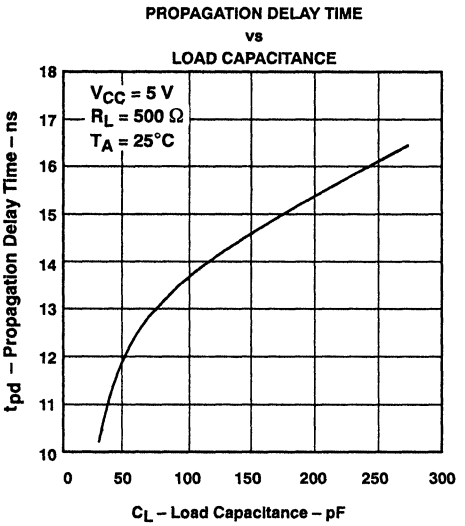


Figure 5

TYPICAL APPLICATION DATA

expanding the SN74ACT7801

The SN74ACT7801 is expandable in width and depth. Expanding in word depth offers special timing considerations:

1. After the first data word is loaded into the FIFO, the word is unloaded and the Output Ready flag (OR) goes high after N × 3 Read Clock (RDCLK) cycles, where N is the number of devices used in depth expansion.
2. After the FIFO is filled and the Input Ready flag (IR) goes low and the first word is unloaded, the IR flag is set high after N × 2 Write Clock cycles, where N is the number of devices used in depth expansion.

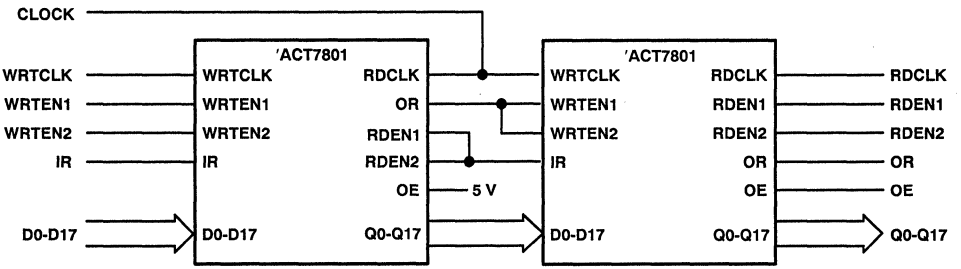


Figure 6. Word-Depth Expansion: 2048-Word by 18-Bit, N = 2

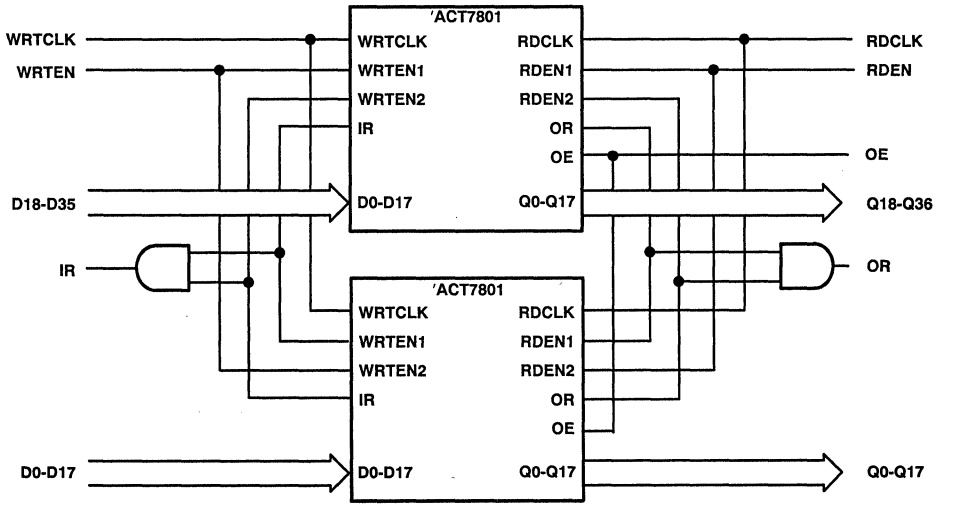
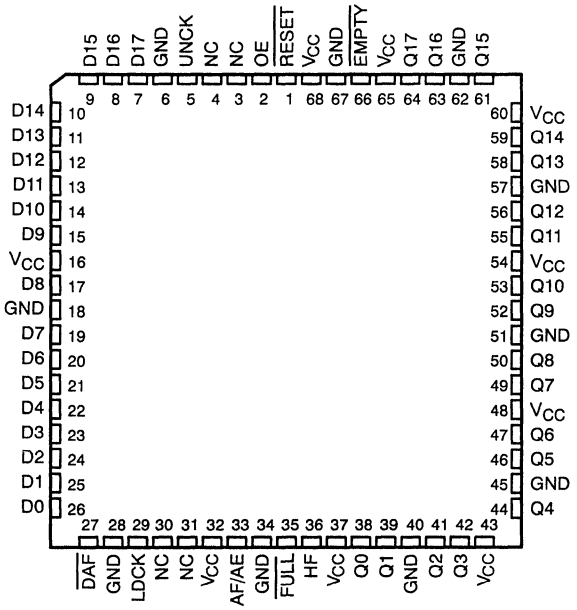


Figure 7. Word-Width Expansion: 1024-Word by 36-Bit

D3599, AUGUST 1990–REVISED OCTOBER 1990

- Independent Asynchronous Inputs and Outputs
- Low-Power Advanced CMOS Technology
- 1024 Words by 18 Bits Each
- Programmable Almost Full/Almost Empty Flag
- Empty, Full, and Half-Full Flags
- Fast Access Times of 25 ns With a 50-pF Load
- Fall-Through Time . . . 20 ns Typical
- Data Rates From 0 to 50 MHz
- High Output Drive for Direct Bus Interface
- 3-State Q Outputs

FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7802 is a 1024- by 18-bit FIFO for high-speed applications. It processes data in a bit-parallel format at rates up to 50 MHz and access times of 25 ns.

Data is written into the FIFO memory on a low-to-high transition on the Load Clock input (LDCK) and is read out on a low-to-high transition on the Unload Clock input (UNCK). The memory is full when the number of words clocked in exceeds by 1024 the number of words clocked out. When the memory is full, LDCK has no effect on the data in the memory; when the memory is empty, UNCK has no effect.

PRODUCT PREVIEW

The FIFO memory status is monitored by the Full ($\overline{FULL}$), Empty ($\overline{EMPTY}$), Half-Full (HF), and Almost Full/Almost Empty (AF/AE) flags. The $\overline{FULL}$ output is low when the memory is full; the $\overline{EMPTY}$ output is low when the memory is empty. The HF output is high when the memory contains 512 or more words and low when it contains less than 512 words. The level of the AF/AE flag is determined by both the number of words in the FIFO and a user-definable offset X. AF/AE is high when the FIFO is almost full or almost empty, i.e., when it contains X or less words or (1024-X) or more words. The Almost Full/Almost Empty offset value is either user-defined or the default value of 256; it is programmed during each reset cycle as follows:

- User-Defined X:
  - Take $\overline{DAF}$ low
  - Take $\overline{RESET}$ low
  - With $\overline{DAF}$ held low, take $\overline{RESET}$ high. This defines X as the value on D0-D8.
  - To retain the current offset, keep $\overline{DAF}$ low during the following reset cycle.
- Default X:
  - X defaults to 256 if $\overline{DAF}$ is held high during the reset cycle.

A low level on the Reset ($\overline{RESET}$) input resets the FIFO internal clock stack pointers and sets $\overline{FULL}$ high, AF/AE high, HF low, and $\overline{EMPTY}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up.

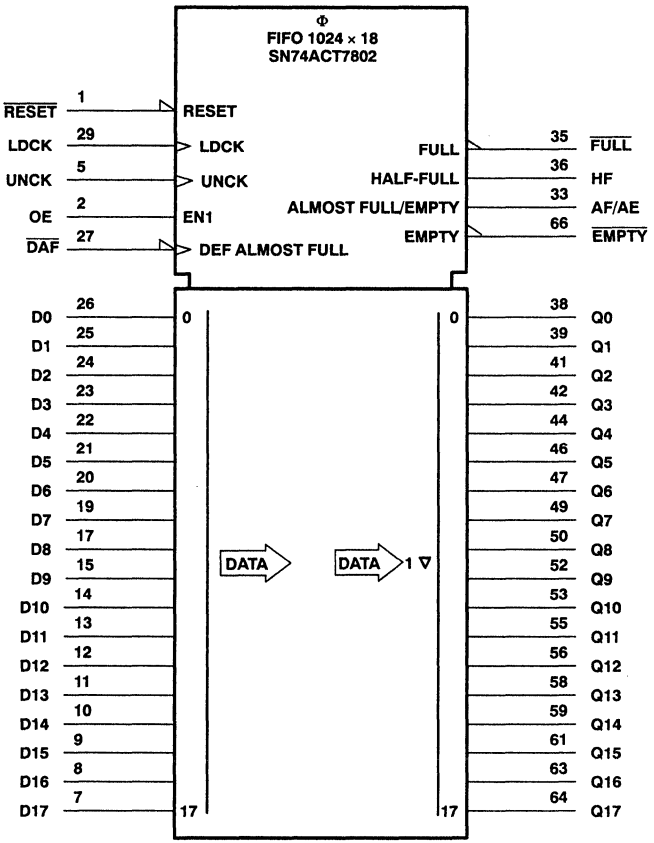
The Q outputs are noninverting and are in the high-impedance state when the Output Enable (OE) input is low.

When writing to the FIFO after a reset pulse or when the FIFO is empty, the first active transition on LDCK drives $\overline{EMPTY}$ high and causes the first word written to the FIFO to appear on the Q outputs. Therefore, an active transition on UNCK is not required to read the first word written to the FIFO. Each subsequent read from the FIFO requires an active transition on UNCK.

The 'ACT7802 can be cascaded in the word-width direction but not in the word-depth direction.

PRODUCT PREVIEW

logic symbol †

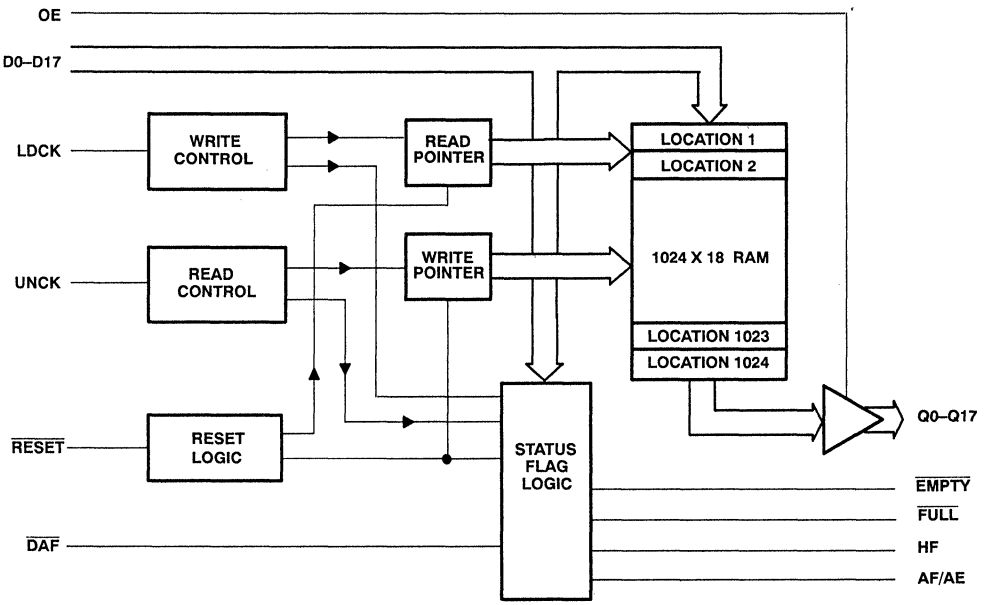


† This symbol is in accordance with ANSI/IEEE Std 91-1984.

PRODUCT PREVIEW

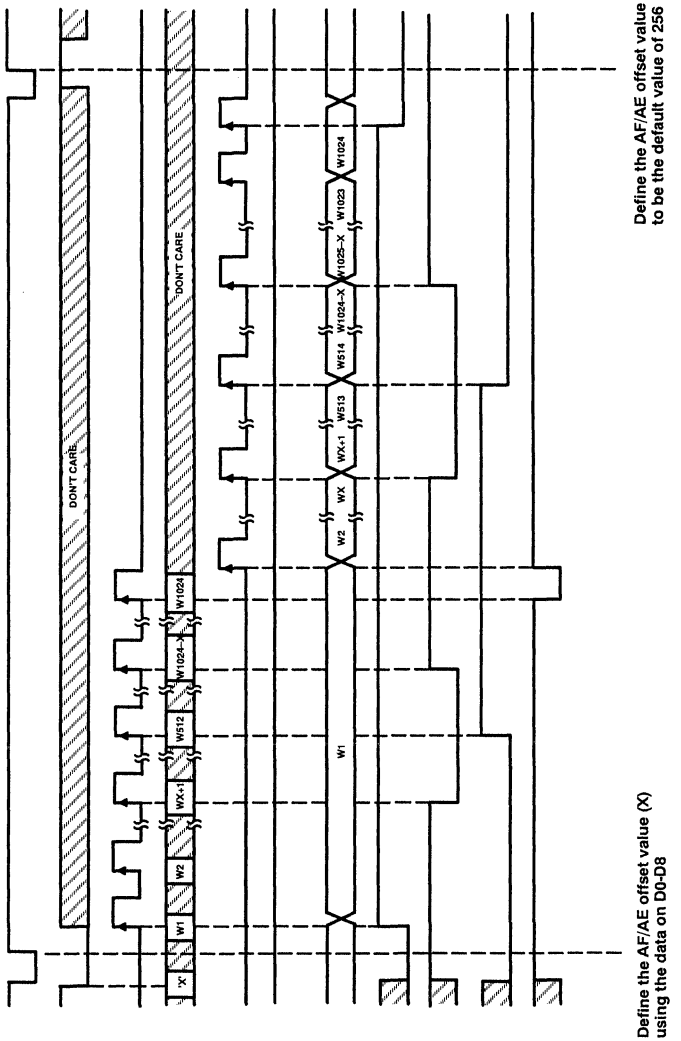
D3599, AUGUST 1990–REVISED OCTOBER 1990

functional block diagram



PRODUCT PREVIEW

timing diagram



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			ACT7802-XX		ACT7802-35		ACT7802-28.5		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		V
V_{IL}	Low-level input voltage			0.8					V
I_{OH}	High-level output current			−8		−8		−8	mA
I_{OL}	Low-level output current			16		16		16	mA
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	LDCK high							ns
		LDCK low							
		UNCK high							
		UNCK low							
		$\overline{DAF}$ high							
		$\overline{RESET}$ low							
t_{su}	Setup time	Data in (D0-D7) before LDCK↑							ns
		$\overline{RESET}$ inactive (high) before LDCK↑							
		LDCK (inactive) before $\overline{RESET}$↑							
		Define AF/AE: D0-D8 before $\overline{DAF}$↓							
		Define AF/AE: $\overline{DAF}$↓ before $\overline{RESET}$↑							
		Define AF/AE (default): $\overline{DAF}$ high before $\overline{RESET}$↑							
t_h	Hold time	Data in (D0-D7) after LDCK↑							ns
		$\overline{RESET}$ inactive (high) after LDCK↑							
		Define AF/AE: D0-D8 after $\overline{DAF}$↓							
		Define AF/AE: $\overline{DAF}$ low after $\overline{RESET}$↑							
		Define AF/AE (default): $\overline{DAF}$ high after $\overline{RESET}$↑							
T_A	Operating free-air temperature		0	70	0	70	0	70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = – 8 mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 16 mA			0.5	V
I_I	Input current	V_{CC} = 5.5 V,	V_I = V_{CC} or 0 V			± 5	μA
I_{OZ}	High-impedance-state output current	V_{CC} = 5.5 V,	V_O = V_{CC} or 0 V			± 5	μA
I_{CC1}‡	Supply current	f_{clock} = 30 MHz			200		mA
I_{CC2}‡	Supply current, standby	LDCK = V_{IH},	V_I = V_{IH} or V_{IL}		20		mA
I_{CC3}‡	Supply current, power down	V_I = V_{CC} – 0.2 V or 0			200		μA
C_i		V_I = 0 V,	f = 1 MHz				pF
C_o		V_O = 0 V,	f = 1 MHz				pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I_{CC} tested with outputs open.

TYPICAL APPLICATION DATA

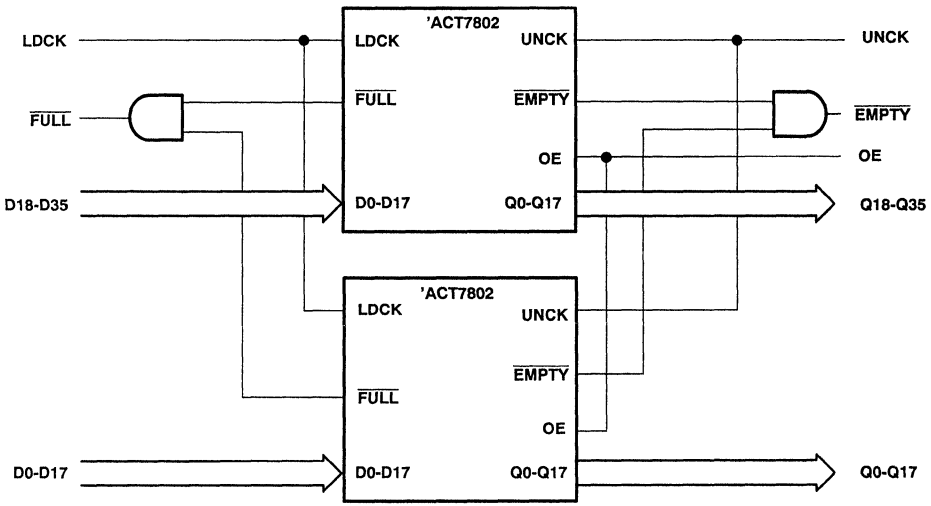


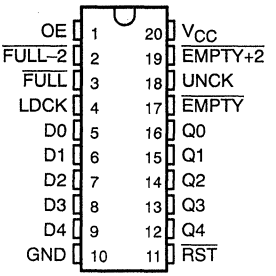
Figure 1. Word-Width Expansion: 1024-Word by 36-Bit

PRODUCT PREVIEW

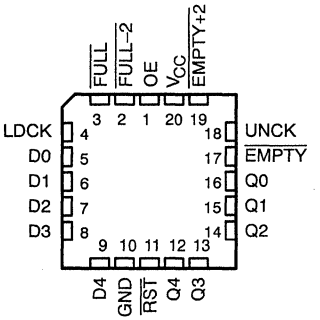
D3486, MARCH 1990

- **Independent Asynchronous Inputs and Outputs**
- **16 Words by 5 Bits**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 14 ns Typ**
- **3-State Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

This 80-bit memory uses Advanced Low-Power Schottky technology and features high speed and a fast fall-through time. It is organized as 16 words by 5 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

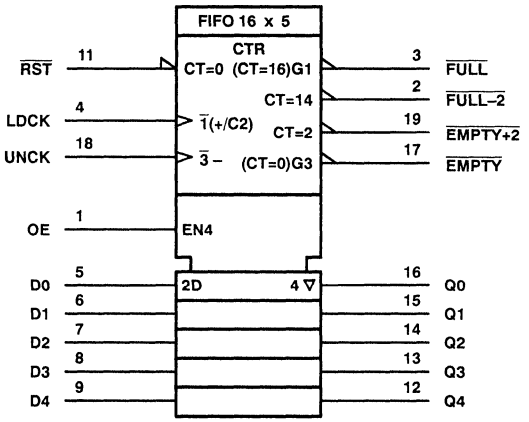
Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, $\overline{\text{FULL–2}}$, and $\overline{\text{FULL+2}}$ output flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when it is not full. The $\overline{\text{FULL–2}}$ output is low when the memory contains 14 data words. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The $\overline{\text{EMPTY+2}}$ output is low when two words remain in memory.

A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$, $\overline{\text{FULL–2}}$, and $\overline{\text{EMPTY+2}}$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK after either a $\overline{\text{RST}}$ pulse or from an empty condition causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

The SN74ALS229B is characterized for operation from 0°C to 70°C.

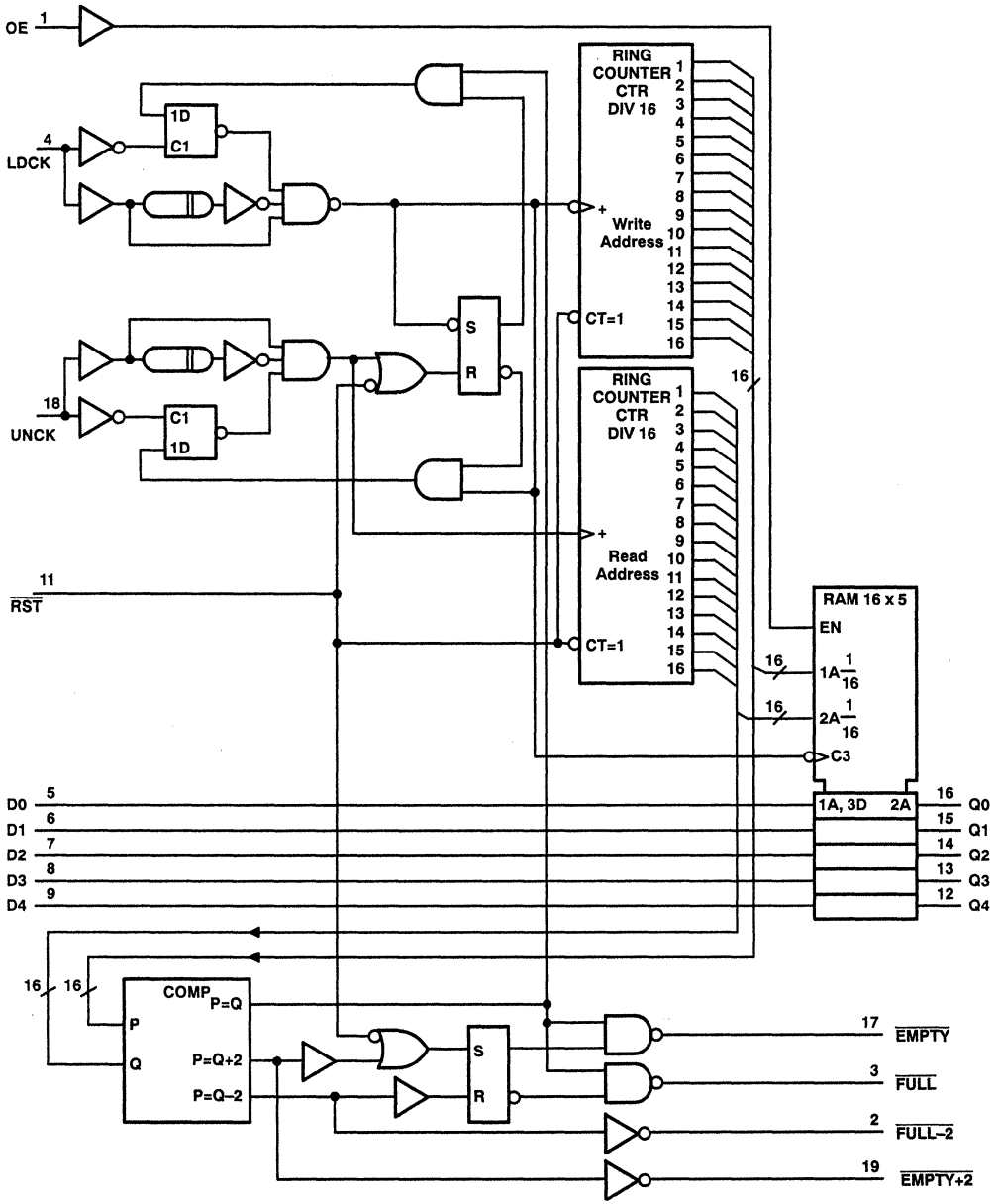
logic symbol†



† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

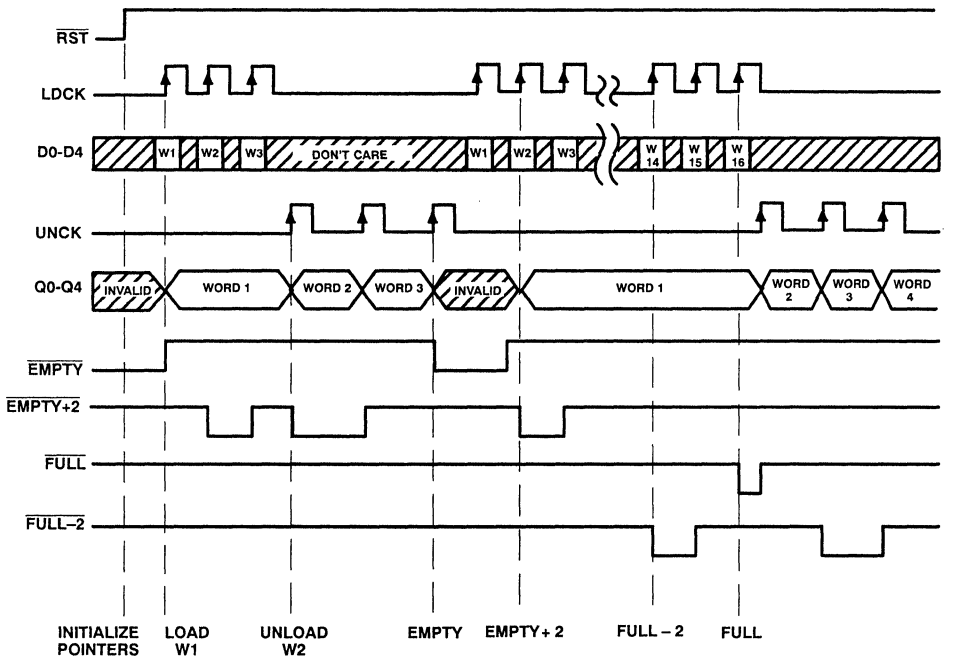
Pin numbers shown are for DW and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW and N packages.

timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltge		2			V
V_{IL}	Low-level input voltge				0.8	V
I_{OH}	High-level output curent	Q outputs			−1.6	mA
		Status flags			−0.4	
I_{OL}	Low-level output curent	Q outputs			24	mA
		Status flags			8	
f_{clock}	Clock frequency	LDCK	0		40	MHz
		UNCK	0		40	
t_w	Pulse duration	$\overline{RST}$ low	18			ns
		LDCK low	15			
		LDCK high	10			
		UNCK low	15			
		UNCK high	10			
t_{su}	Setup time	Data before LDCK↑	8			ns
		$\overline{RST}$ (inactive) before LDCK↑	5			
		LDCK (inactive) before $\overline{RST}$↑	5			
t_h	Hold time	Data after LDCK↑	5			ns
T_A	Operating free-air temperature		0		70	°C

NOTE 3: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse duration limits can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = −2.6 mA	2.4	3.2		V
	Status flags	V_{CC} = 4.5 V to 5.5 V,	I_{OL} = −0.4 mA	V_{CC}−2			
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	Status flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			85	140	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 2)

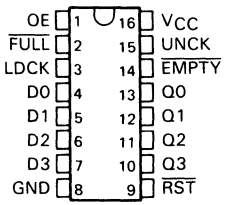
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	MAX	
	LDCK		40		
	UNCK		40		
t_{pd}	LDCK↑	Any Q	6	30	ns
t_{pd}	UNCK↑	Any Q	6	30	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$	5	25	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$	6	27	ns
t_{PHL}	$\overline{RST}$↓	$\overline{EMPTY}$	5	26	ns
t_{pd}	LDCK↑	$\overline{EMPTY+2}$	7	33	ns
t_{pd}	UNCK↑	$\overline{EMPTY+2}$	9	35	ns
t_{PLH}	$\overline{RST}$↓	$\overline{EMPTY+2}$	9	33	ns
t_{pd}	LDCK↑	$\overline{FULL-2}$	7	33	ns
t_{pd}	UNCK↑	$\overline{FULL-2}$	9	35	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL-2}$	9	33	ns
t_{PHL}	LDCK↑	$\overline{FULL}$	6	27	ns
t_{PLH}	UNCK↑	$\overline{FULL}$	5	25	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$	8	31	ns
t_{en}	OE↑	Q	2	15	ns
t_{dis}	OE↓	Q	1	15	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

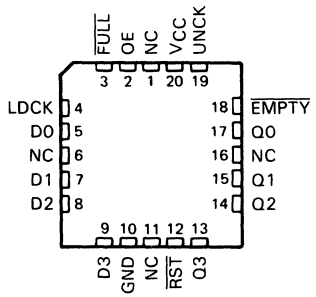
D3247, FEBRUARY 1989

- **Independent Asynchronous Inputs and Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs**
- **16 Words by 4 Bits**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 14 ns Typ**
- **3-State Outputs**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection.

description

This 64-bit memory uses Advanced Low-Power Schottky technology and features high speed and fast fall-through times. It is organized as 16 words by 4 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

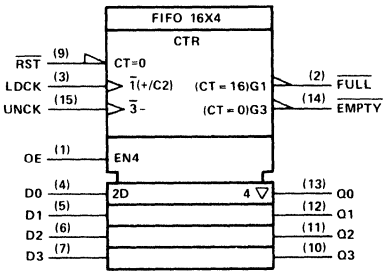
Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ output flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty.

A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK after either a $\overline{\text{RST}}$ pulse or from an empty condition causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect either the $\overline{\text{FULL}}$ or $\overline{\text{EMPTY}}$ output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

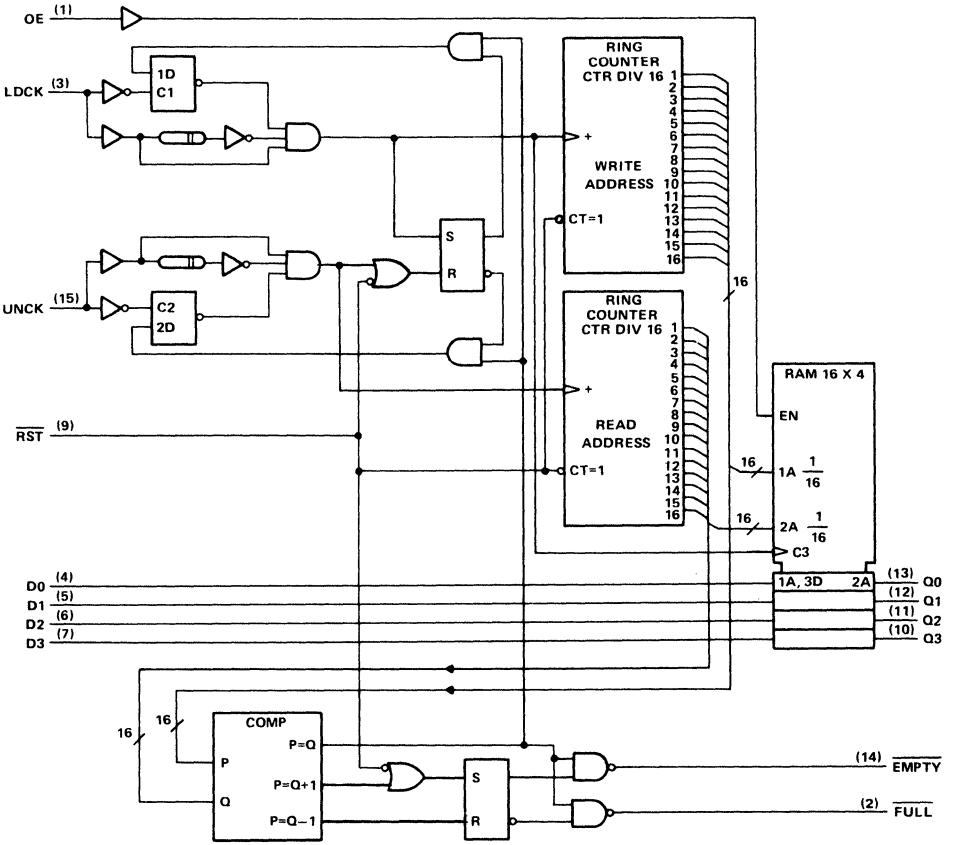
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic symbol†



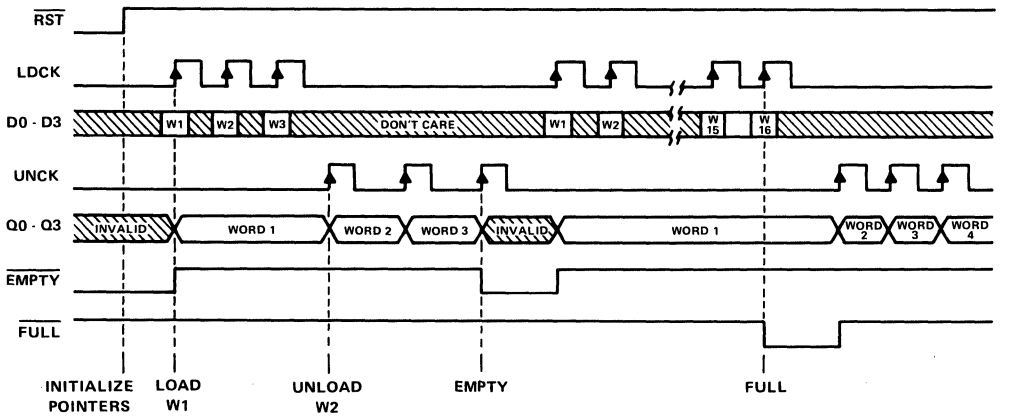
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

logic diagram (positive logic)



Pin numbers shown are for DW and N packages.

timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−2.6	mA
		$\overline{FULL}$, $\overline{EMPTY}$			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		$\overline{FULL}$, $\overline{EMPTY}$			8	
f_{clock}†	Clock frequency	LDCK	0		40	MHz
		UNCK	0		40	
t_w	Pulse duration	$\overline{RST}$ low	18			ns
		LDCK low	15			
		LDCK high	10			
		UNCK low	15			
		UNCK high	10			
t_{su}	Setup time	Data before LDCK↑	8			ns
		LDCK inactive before $\overline{RST}$↑	5			
t_h	Hold time	Data after LDCK↑	5			ns
		LDCK inactive after $\overline{RST}$↑	5			
T_A	Operating free-air temperature		0		70	°C

†The maximum possible clock frequency is 40 MHz. The maximum clock frequency when using a 50% duty cycle is 33.3 MHz.

NOTE 1: To ensure proper operation, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates limits for maximum V_{IL}, minimum V_{IH}, or minimum pulse duration can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	$\overline{FULL}$, EMPTY	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	$\overline{FULL}$, $\overline{EMPTY}$	V_{CC} = 4.5 V,	I_{OH} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			80	125	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 2)

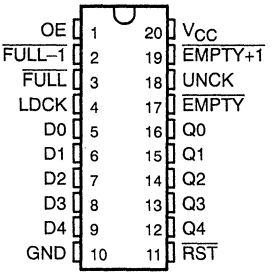
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}	LDCK			50		40		MHz
	UNCK			50		40		
t_{pd}	LDCK↑	Any Q		14	23	6	30	ns
t_{pd}	UNCK↑	Any Q		15	23	6	30	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$		13	20	5	25	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$		15	22	6	27	ns
t_{PHL}	$\overline{RST}$↓	$\overline{EMPTY}$		15	21	5	26	ns
t_{PHL}	LDCK↑	$\overline{FULL}$		15	22	6	27	ns
t_{PLH}	UNCK↑	$\overline{FULL}$		13	20	5	25	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$		16	23	7	28	ns
t_{en}	OE↑	Q		5	12	1	14	ns
t_{dis}	OE↓	Q		5	12	1	16	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

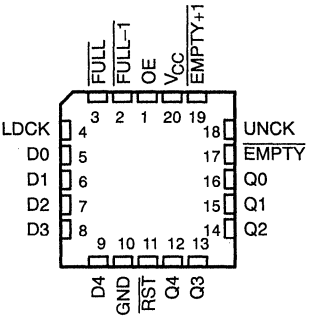
D3487, MARCH 1990

- **Independent Asynchronous Inputs and Outputs**
- **16 Words by 5 Bits**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 14 ns Typ**
- **3-State Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

This 80-bit memory uses Advanced Low-Power Schottky technology and features high speed and a fast fall-through time. It is organized as 16 words by 5 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect. When the memory is empty, UNCK signals have no effect.

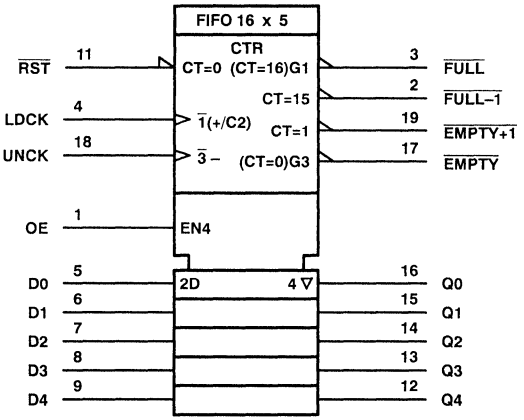
Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, $\overline{\text{FULL–1}}$, and $\overline{\text{FULL+1}}$ output flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when it is not full. The $\overline{\text{FULL–1}}$ output is low when the memory contains 15 data words. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The $\overline{\text{EMPTY+1}}$ output is low when two words remain in memory.

A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$, $\overline{\text{FULL–1}}$, and $\overline{\text{EMPTY+1}}$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a $\overline{\text{RST}}$ pulse or from an empty condition, causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

The SN74ALS233B is characterized for operation from 0°C to 70°C.

D3487, MARCH 1990

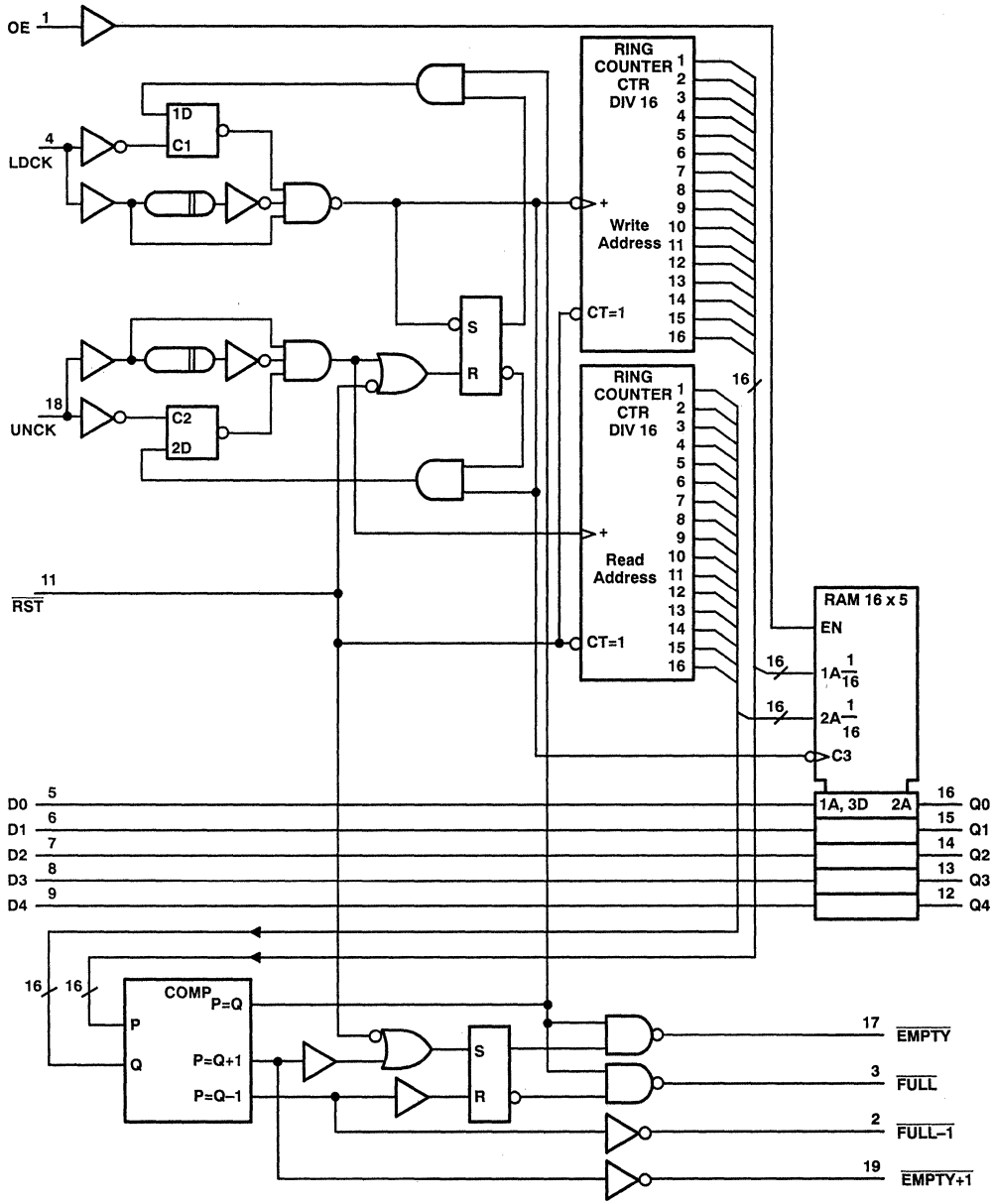
logic symbol†



† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

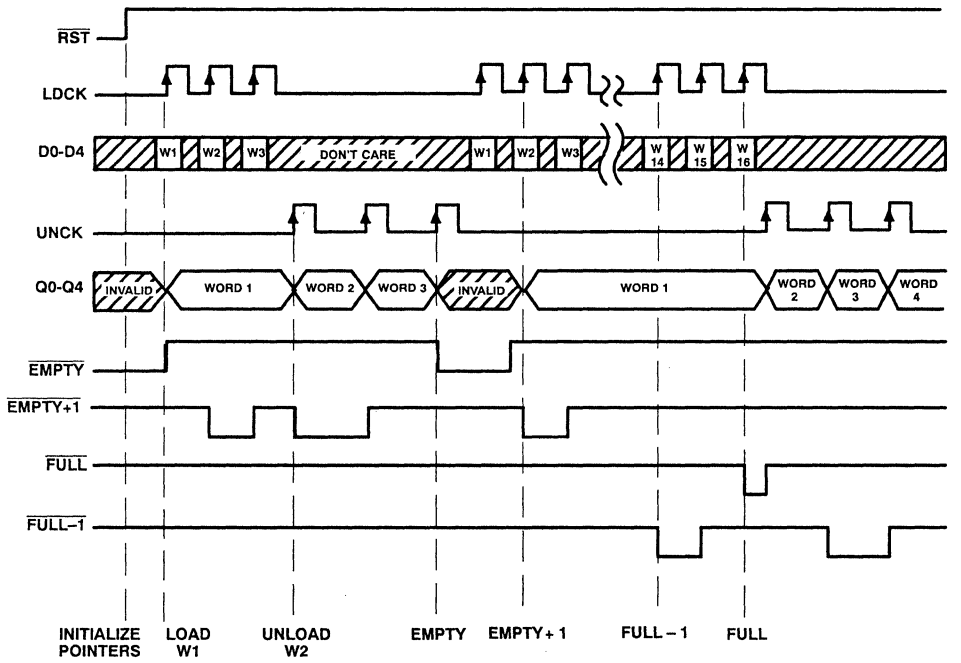
Pin numbers shown are for DW and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW and N packages.

timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−1.6	mA
		Status flags			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		Status flags			8	
fclock	Clock frequency	LDCK	0		40	MHz
		UNCK	0		40	
t_w	Pulse duration	$\overline{RST}$ low	18			ns
		LDCK low	15			
		LDCK high	10			
		UNCK low	15			
		UNCK high	10			
t_{su}	Setup time	Data before LDCK↑	8			ns
		$\overline{RST}$ (inactive) before LDCK↑	5			
		LDCK (inactive) before $\overline{RST}$↑	5			
t_h	Hold time	Data after LDCK↑	5			ns
T_A	Operating free-air temperature		0		70	°C

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse duration limits can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = −2.6 mA	2.4	3.2		V
	Status flags	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	$V_{CC}-2$			
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	Status flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			88	133	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 2)

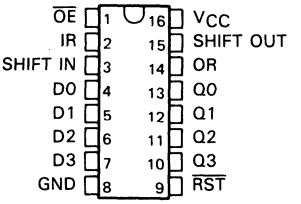
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	MAX	
	LDCK		40		
	UNCK		40		
t_{pd}	LDCK↑	Any Q	6	32	ns
t_{pd}	UNCK↑	Any Q	6	30	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$	5	25	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$	6	27	ns
t_{PHL}	$\overline{RST}$↓	$\overline{EMPTY}$	5	25	ns
t_{pd}	LDCK↑	$\overline{EMPTY+1}$	7	34	ns
t_{pd}	UNCK↑	$\overline{EMPTY+1}$	7	34	ns
t_{PLH}	$\overline{RST}$↓	$\overline{EMPTY+1}$	8	31	ns
t_{pd}	LDCK↑	$\overline{FULL-1}$	9	33	ns
t_{pd}	UNCK↑	$\overline{FULL-1}$	8	32	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL-1}$	11	32	ns
t_{PHL}	LDCK↑	$\overline{FULL}$	6	27	ns
t_{PLH}	UNCK↑	$\overline{FULL}$	5	25	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$	9	30	ns
t_{en}	OE↑	Q	2	15	ns
t_{dis}	OE↓	Q	1	15	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

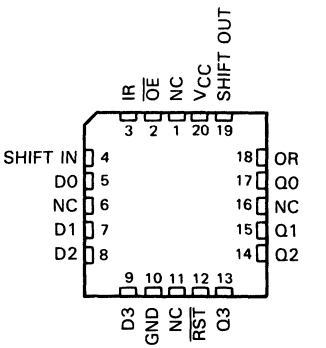
D2958, OCTOBER 1986—REVISED APRIL 1988

- **Asynchronous Operation**
- **Organized as 64 Words of 4 Bits**
- **Data Rates From 0 to 30 MHz**
- **3-State Outputs**
- **Similar to MMI67401B With Higher Speed and 3-State Outputs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS234 . . . J PACKAGE
SN74ALS234 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS234 . . . FK PACKAGE
SN74ALS234. . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN54ALS234 and SN74ALS234 are 256-bit memories utilizing Advanced Low-Power Schottky IMPACT™ Technology. They feature high speed with fast fall-through times and are organized as 64 words by 4 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ALS234 is designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the Shift In input. When Shift In goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional Shift In pulses have no effect. Data is shifted out of memory on the falling edge of the Shift Out input (see Figure 2). When the FIFO is empty, additional Shift Out pulses have no effect. The last data word remains at the outputs until a new word falls through or $\overline{RST}$ goes low.

Status of the 'ALS234 FIFO memory is monitored by the Output Ready (OR) and Input Ready (IR) flags. When the OR flag is high, valid data is available at the outputs. The OR flag is low when Shift Out is high and will stay low when the FIFO is empty. The IR status flag is high when the inputs are ready to receive more data. The IR flag is low when Shift In is high and stays low when the FIFO is full.

When the FIFO is empty, input data is shifted to the output automatically when Shift In goes low. If Shift Out is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

When the FIFO is full, data can be shifted in automatically by holding Shift In high and taking Shift Out low. A propagation delay after Shift Out goes low, IR will go high. If Shift In is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low when the FIFO is full and Shift In is high, only a high-level pulse is seen on the IR output (see Figure 4).

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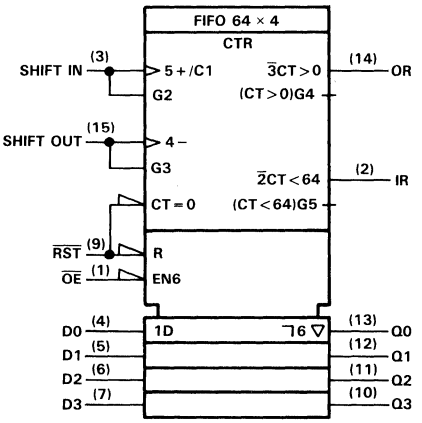
description (continued)

The FIFO must be reset after power up with a low-level pulse on the Master Reset input ($\overline{RST}$). This sets Input Ready (IR) high and Output Ready (OR) low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If Shift In is high when $\overline{RST}$ goes high, the input data is shifted in and IR goes low and remains low until Shift In goes low. If Shift In goes low before $\overline{RST}$ goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs and are at high impedance when Output Enable ($\overline{OE}$) is high. $\overline{OE}$ does not affect the IR and OR outputs.

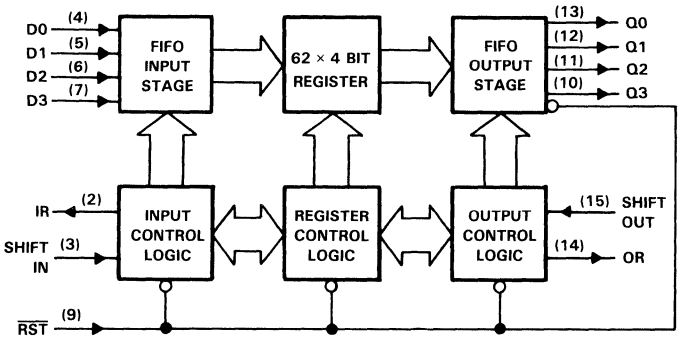
The SN54ALS234 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS234 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Pin numbers shown are for DW, J, and N packages.

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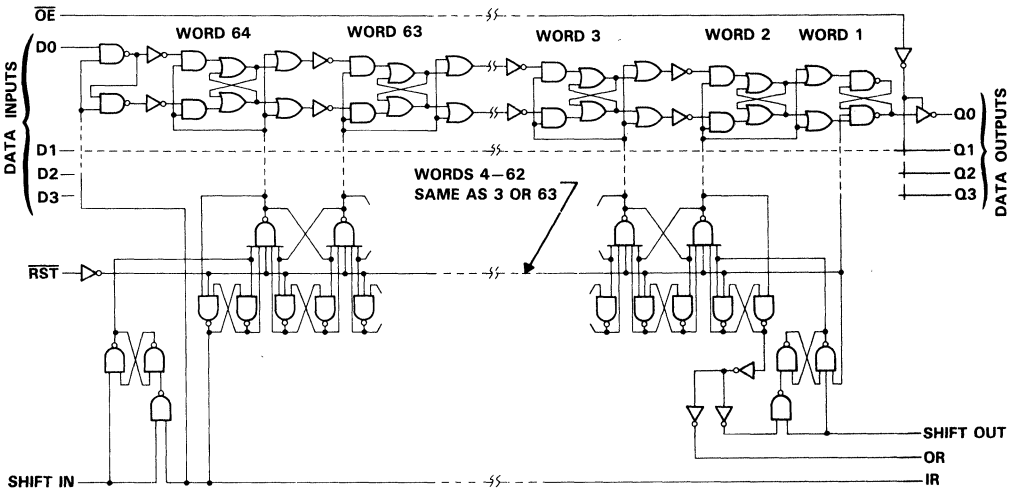
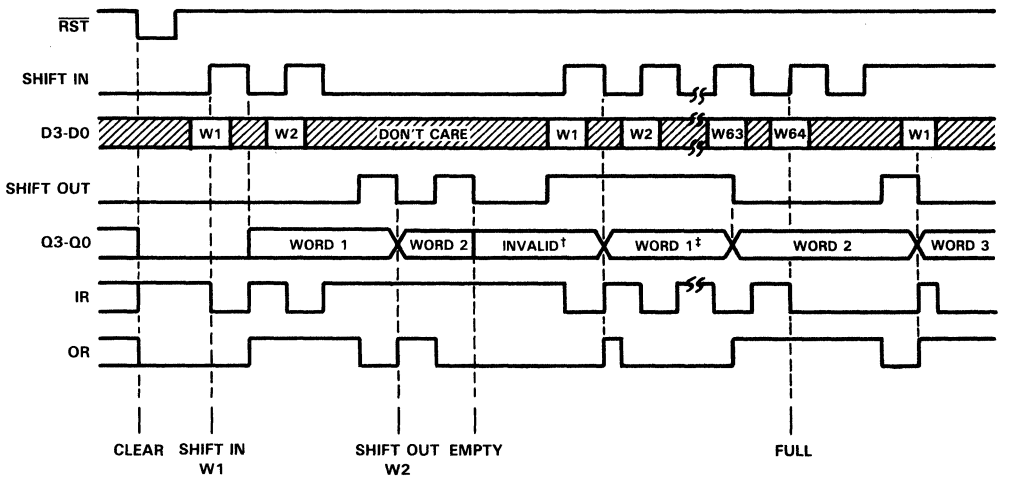
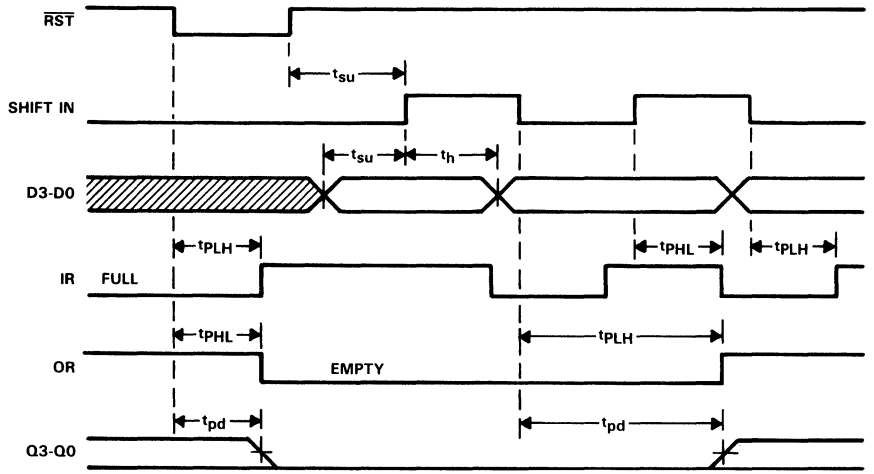
logic diagram (positive logic)



timing diagram

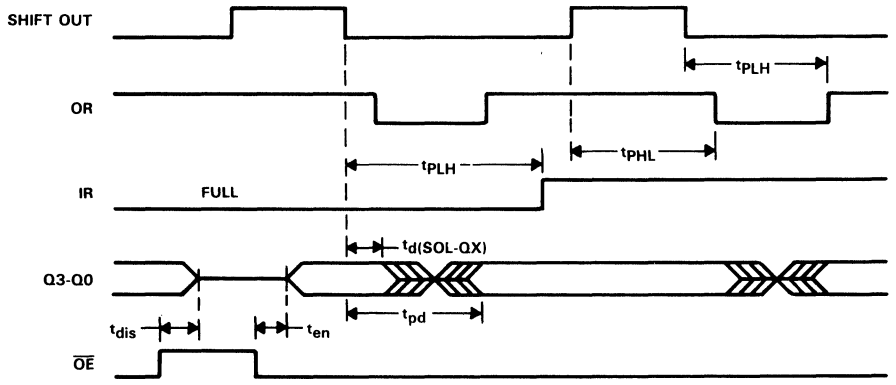


† The last data word shifted out of the FIFO remains at the output until a new word falls through or a $\overline{RST}$ pulse clears the FIFO.
‡ While the output data is considered valid only when the OR flag is high, the stored data remains at the output. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until Shift Out is taken low.



NOTE: SHIFT OUT is low

FIGURE 1. MASTER-RESET AND DATA-IN WAVEFORMS



NOTE: SHIFT IN is low

FIGURE 2. DATA-OUT WAVEFORMS

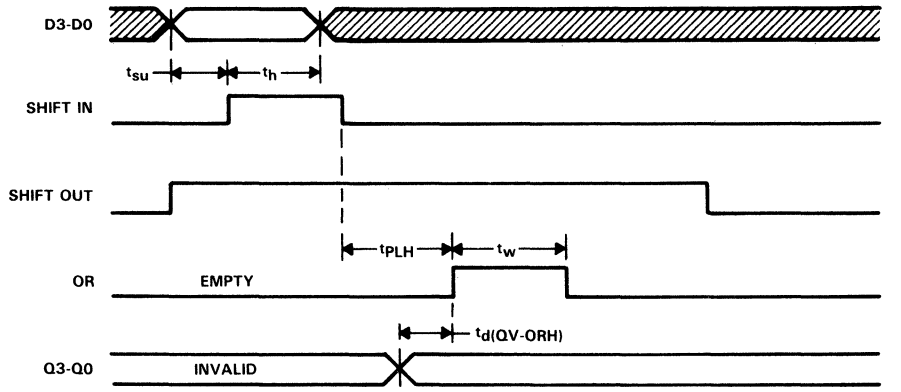


FIGURE 3. DATA FALL-THROUGH WAVEFORMS

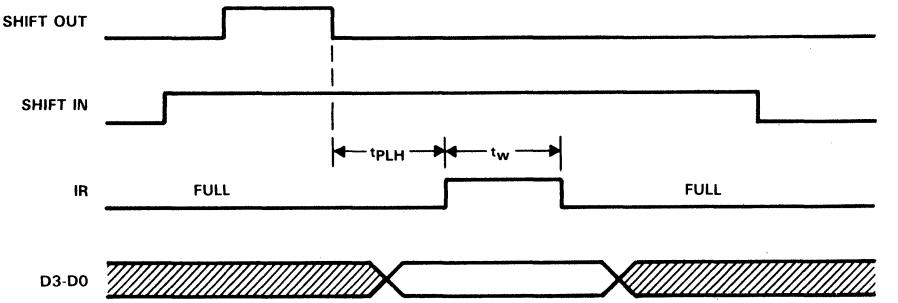


FIGURE 4. AUTOMATIC DATA-IN WAVEFORMS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS234 . . . . . −55°C to 125°C
SN74ALS234 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS234			SN74ALS234			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Q outputs			−1			−2.6	mA
		IR and OR			−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs			12			24	mA
		IR and OR			4			8	
f_{clock}	Clock frequency	SHIFT IN or SHIFT OUT	0		25	0		30	MHz
t_w	Pulse duration	SHIFT IN or SHIFT OUT high or low	17			15			ns
		$\overline{RST}$ low	20			15			
t_{su}	Setup time before SHIFT IN ↑	Data	0			0			ns
		$\overline{RST}$ high (inactive)	15			15			
t_h	Hold time, data after SHIFT IN ↑		19			17			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS234			SN74ALS234			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Q	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
	IR, OR	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		
V_{OL}	Q	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	IR, OR	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.4		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	I_{CCL}		100	155		100	145	mA
			I_{CCH}		97	152		97	142	
			I_{CCZ}		103	158		103	148	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS234			SN54ALS234		SN74ALS234		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	SHIFT IN			35		25		30		MHz
	SHIFT OUT			35		25		30		
t_w†	IR high			15		7		8		ns
t_w‡	OR high			19		7		8		ns
$t_{d(QV-ORH)}$	Q valid before OR ↑			6	9	−5	12	−5	12	ns
$t_{d(SOL-QX)}$	Q valid after SHIFT OUT ↓			13		4		4		ns
t_{pd}	SHIFT IN ↓	Q		600	800	350	1200	350	1000	ns
t_{PHL}	SHIFT IN ↑	IR		20	26	8	36	8	30	ns
t_{PLH}	SHIFT IN ↓	IR		16	21	6	28	6	25	ns
t_{PLH}§	SHIFT IN ↓	OR		600	800	350	1200	350	1000	ns
t_{pd}	SHIFT OUT ↓	Q		13	17	4	24	4	22	ns
t_{PHL}	SHIFT OUT ↑	OR		23	27	7	39	7	33	ns
t_{PLH}	SHIFT OUT ↓	OR		20	24	6	33	6	30	ns
t_{PLH}§	SHIFT OUT ↓	IR		600	800	350	1200	350	1000	ns
t_{PHL}	$\overline{RST}$ ↓	OR		22	26	10	40	10	34	ns
t_{PLH}	$\overline{RST}$ ↓	IR		17	21	6	31	6	27	ns
t_{PHL}	$\overline{RST}$ ↓	Q		14	17	5	21	5	19	ns
t_{dis}	$\overline{OE}$ ↑	Q		7	13	2	16	2	15	ns
t_{en}	$\overline{OE}$ ↓	Q		6	12	2	15	2	13	ns

† The IR output pulse occurs when the FIFO is full, Shift In is high, and Shift Out is pulsed (see Figure 4).
‡ The OR output pulse occurs when the FIFO is empty, Shift Out is high, and Shift In is pulsed (see Figure 3).
§ Data throughput or "fall through" times
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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TYPICAL APPLICATION INFORMATION

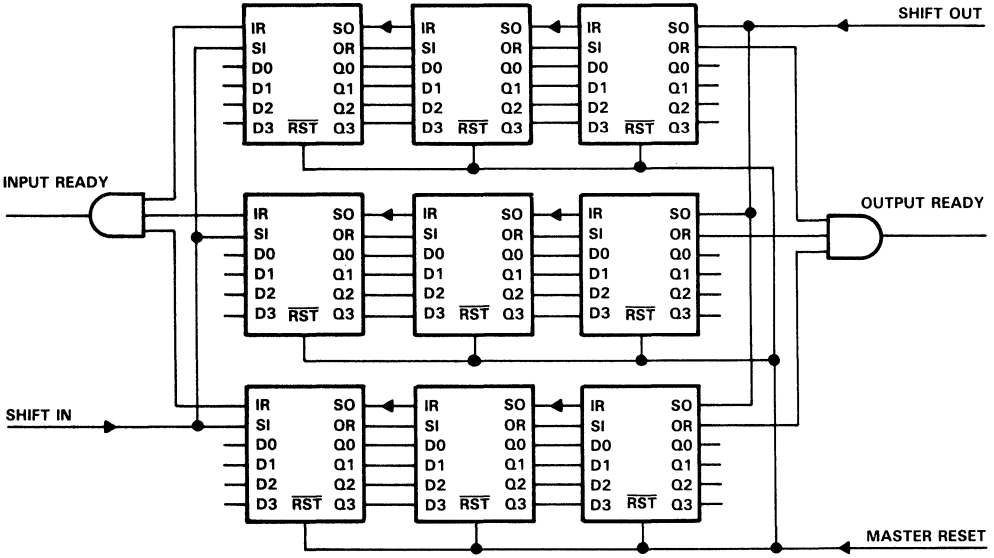

FIGURE 5. 192-WORD BY 12-BIT EXPANSION

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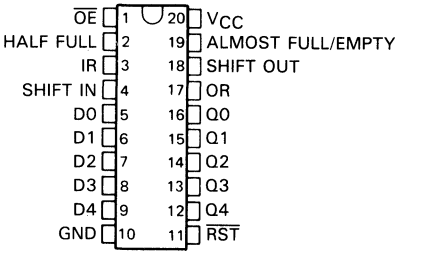
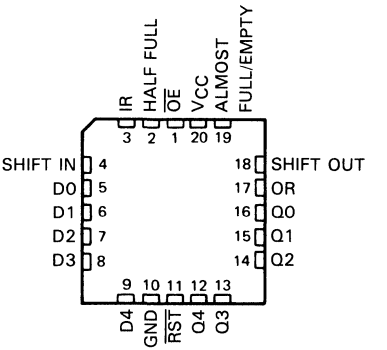
- **Asynchronous Operation**
- **Organized as 64 Words of 5 Bits**
- **Data Rates From 0 to 25 MHz**
- **3-State Outputs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS235 . . . J PACKAGE
SN74ALS235 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS235 . . . FK PACKAGE
SN74ALS235. . . FN PACKAGE
(TOP VIEW)



description

The SN54ALS235 and SN74ALS235 are 320-bit memories utilizing Advanced Low-Power Schottky IMPACT™ Technology. They feature high speed with fast fall-through times and are organized as 64 words by 5 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ALS235 is designed to process data at rates from 0 to 25 megahertz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the Shift In input. When Shift In goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional Shift In pulses have no effect. Data is shifted out of memory on the falling edge of the Shift Out input (see Figure 2). When the FIFO is emply, additional Shift Out pulses have no effect. The last data word remains at the outputs until a new word falls through or $\overline{RST}$ goes low.

Status of the 'ALS235 FIFO memory is monitored by the Output Ready (OR), Input Ready (IR), Almost Full/Empty, and Half Full flags. When the OR flag is high, valid data is available at the outputs. The OR flag is low when Shift Out is high and stays low when the FIFO is empty. The IR status flag is high when the inputs are ready to receive more data. The IR flag is low when Shift In is high and stays low when the FIFO is full. The Almost Full/Empty flag is high when the FIFO contains eight or less words (see Figure 5) or fifty-six or more words (see Figure 6). The Almost Full/Empty flag is low when the FIFO contains between nine and fifty-five words. The Half Full flag is high when the FIFO contains thirty-two or more words and is low when the FIFO contains thirty-one words or less (see Figure 7).

When the FIFO is empty, input data is shifted to the output automatically when Shift In goes low. If Shift Out is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

When the FIFO is full, data can be shifted in automatically by holding Shift In high and taking Shift Out low. One propagation delay after Shift Out goes low, IR will go high. If Shift In is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low, when the FIFO is full and Shift In is high, only a high-level pulse is seen on the IR output.

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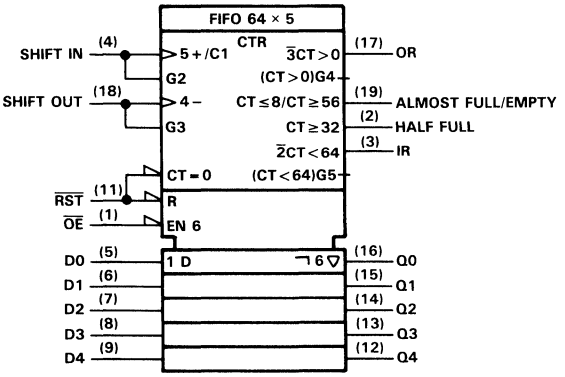
description (continued)

The FIFO must be reset after power up with a low-level pulse on the Master Reset input ($\overline{RST}$). This sets Input Ready (IR) high and Output Ready (OR) low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If Shift In is high when $\overline{RST}$ goes high, the input data is shifted in and IR goes low and remains low until Shift In goes low. If Shift In goes low before $\overline{RST}$ goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs and are at high impedance when Output Enable ($\overline{OE}$) is high. $\overline{OE}$ does not affect the status flag outputs (see Figure 2).

The SN54ALS235 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS235 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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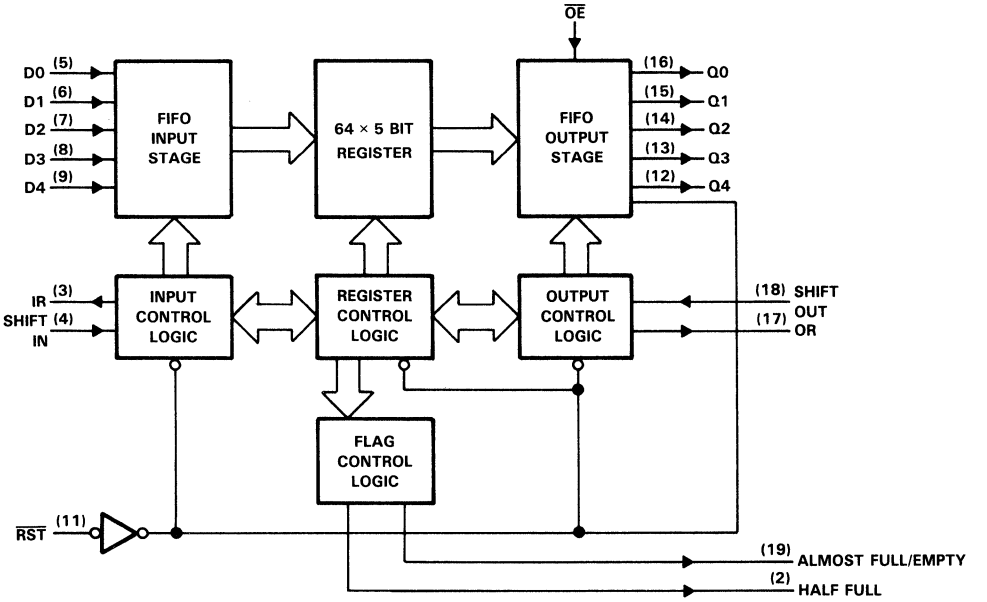
functional block diagram



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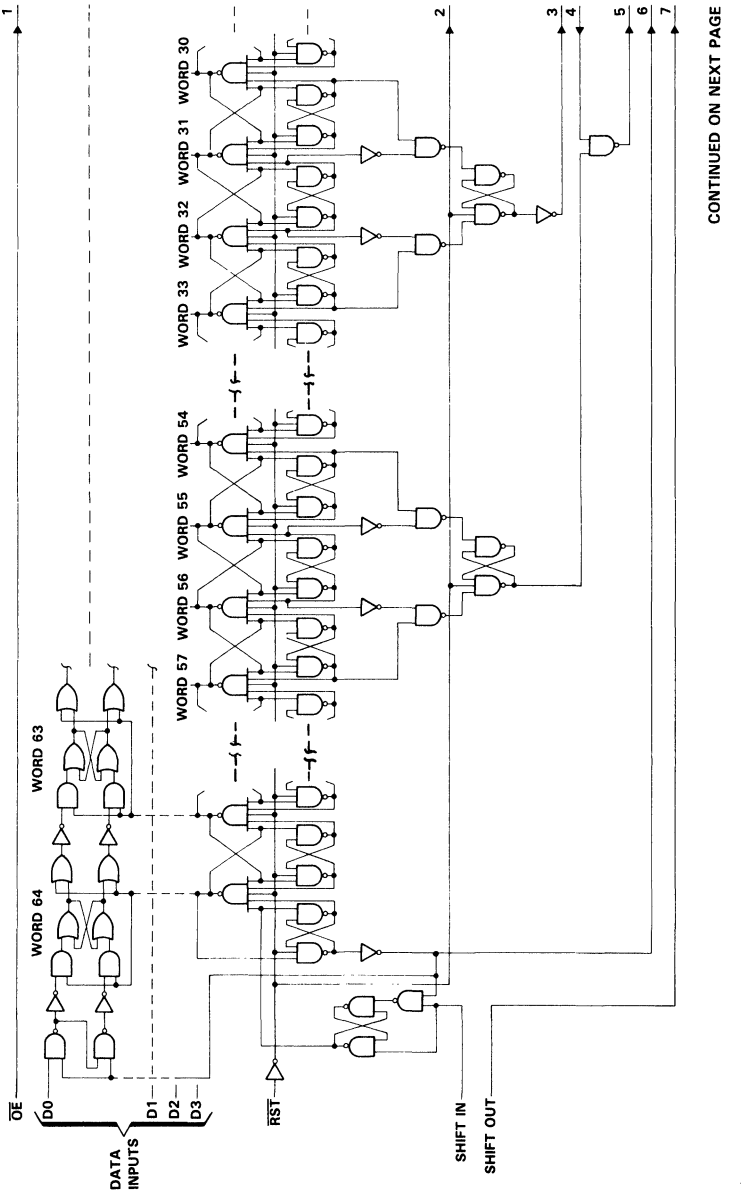
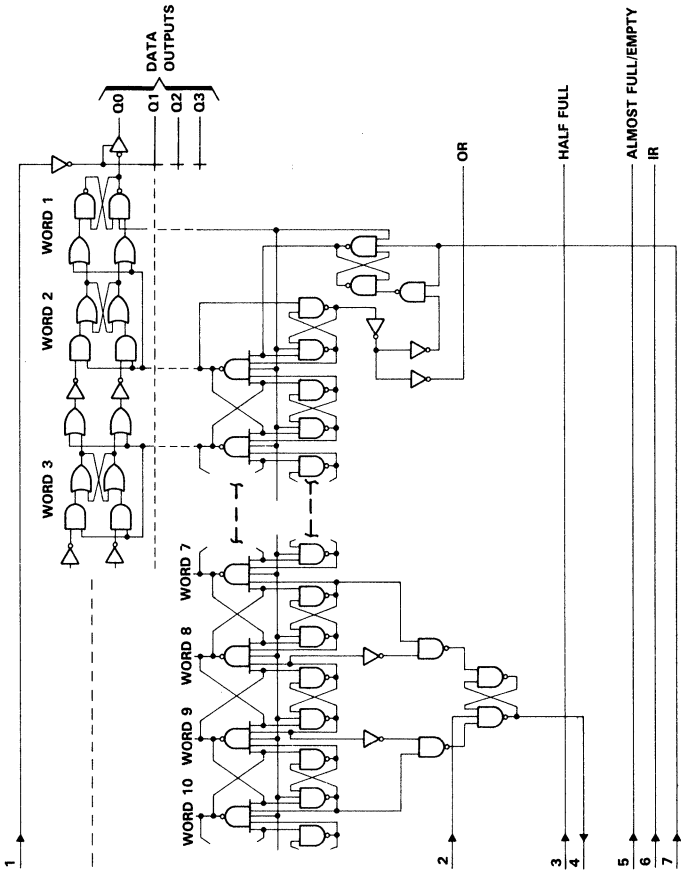
logic diagram (positive logic)

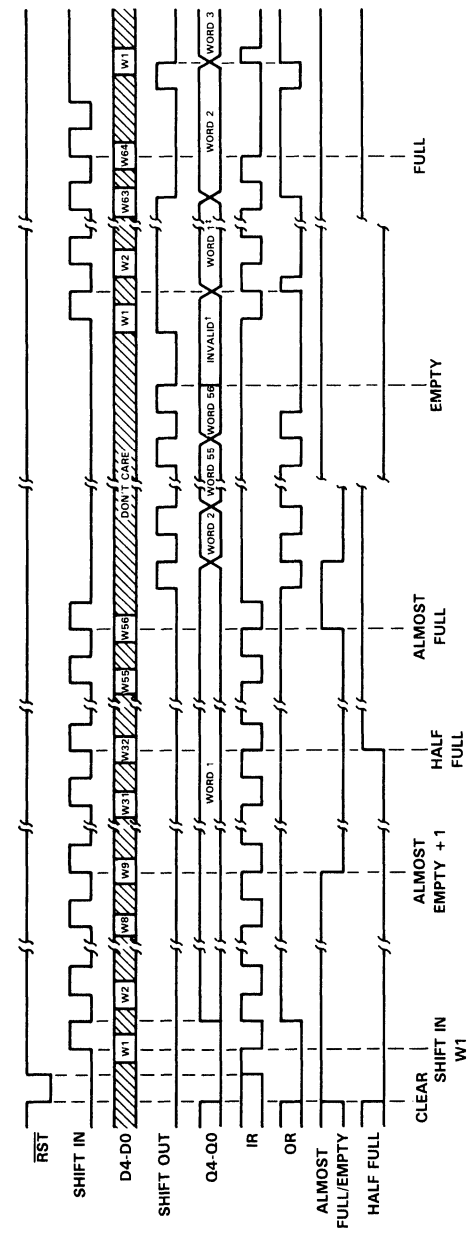


logic diagram (positive logic) (continued)

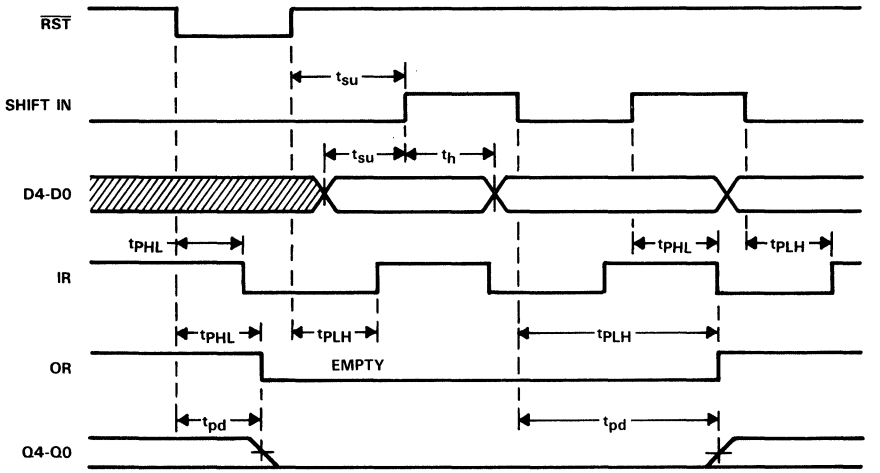


D2958, OCTOBER 1986

timing diagram

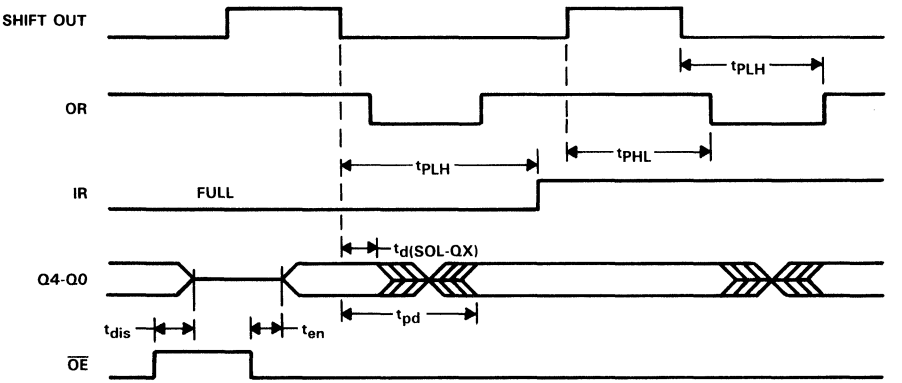


† The last data word shifted out of the FIFO remains at the output until a new word falls through or a $\overline{RST}$ pulse clears the FIFO.
‡ While the output data is considered valid only when the OR flag is high, the stored data remains at the output. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until Shift Out is taken low.



NOTE: SHIFT OUT is low

FIGURE 1. MASTER-RESET AND DATA-IN WAVEFORMS



NOTE: SHIFT IN is low

FIGURE 2. DATA-OUT WAVEFORMS

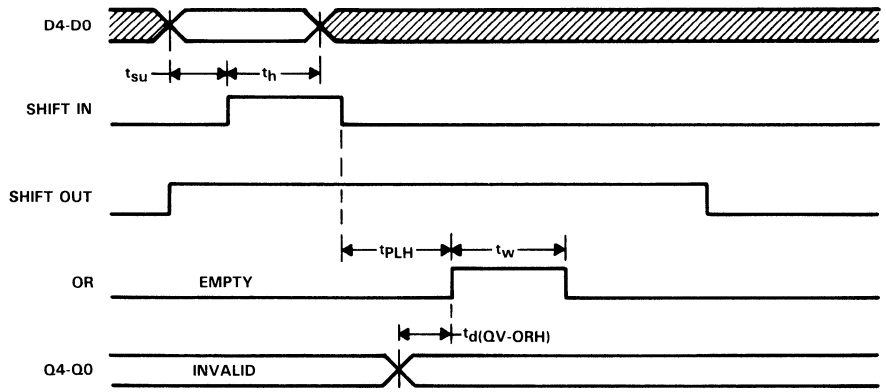


FIGURE 3. DATA FALL-THROUGH WAVEFORMS

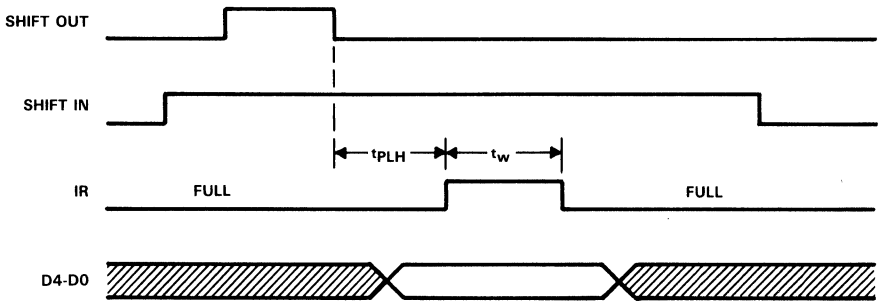


FIGURE 4. AUTOMATIC DATA-IN WAVEFORMS

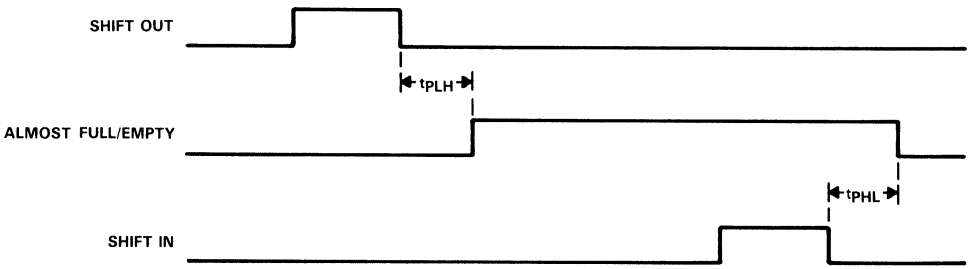


FIGURE 5. ALMOST-EMPTY WAVEFORMS

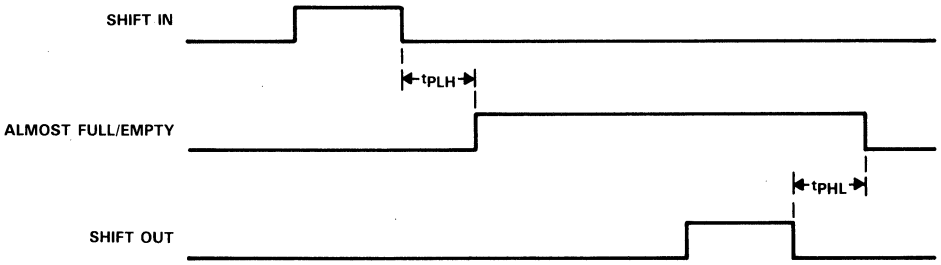


FIGURE 6. ALMOST-FULL WAVEFORMS

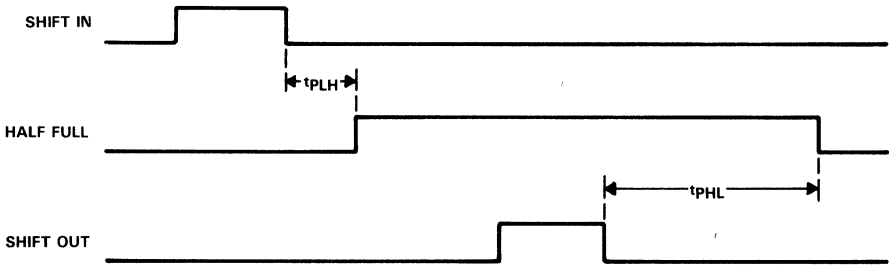


FIGURE 7. HALF-FULL WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS235 . . . . . −55°C to 125°C
SN74ALS235 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS235			SN74ALS235			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Q outputs			−1			−2.6	mA
		Flags			−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs			12			24	mA
		Flags			4			8	
f_{clock}	Clock frequency	SHIFT IN or SHIFT OUT	0		20	0		25	MHz
t_w	Pulse duration	SHIFT IN or SHIFT OUT high or low	17			15			ns
		$\overline{RST}$ low	20			15			
t_{su}	Setup time before SHIFT IN ↑	Data	0			0			ns
		$\overline{RST}$ high (inactive)	15			15			
t_h	Hold time, data after SHIFT IN ↑		19			17			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS235			SN74ALS235			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Q	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
	Flags	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		
V_{OL}	Q	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	Flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.4		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	I_{CCL}		112	175		112	165	mA
			I_{CCH}		105	170		105	160	
			I_{CCZ}		115	180		115	170	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS235			SN54ALS235		SN74ALS235		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	SHIFT IN			30		20		25		MHz
	SHIFT OUT			30		20		25		
t_w†	IR high			15		7		8		ns
t_w‡	OR high			19		7		8		ns
$t_{d(QV-ORH)}$	Q valid before OR ↑			6	9	−5	12	−5	12	ns
$t_{d(SOL-QX)}$	Q valid after SHIFT OUT ↓			13		4		4		ns
t_{pd}	SHIFT IN ↓	Q		600	800	350	1200	350	1000	ns
t_{PHL}	SHIFT IN ↑	IR		20	26	8	36	8	30	ns
t_{PLH}	SHIFT IN ↓	IR		16	21	6	28	6	25	ns
t_{PLH}§	SHIFT IN ↓	OR		600	800	350	1200	350	1000	ns
t_{PHL}	SHIFT IN ↓	ALMOST F/E		550	700	290	1050	290	880	ns
t_{PLH}	SHIFT IN ↓	ALMOST F/E		85	115	40	170	40	150	ns
t_{PLH}	SHIFT IN ↓	HALF FULL		340	410	180	590	180	510	ns
t_{pd}	SHIFT OUT ↓	Q		13	17	4	24	4	22	ns
t_{PHL}	SHIFT OUT ↑	OR		23	27	7	39	7	33	ns
t_{PLH}	SHIFT OUT ↓	OR		20	24	6	33	6	30	ns
t_{PLH}§	SHIFT OUT ↓	IR		600	800	350	1200	350	1000	ns
t_{PHL}	SHIFT OUT ↓	ALMOST F/E		550	700	290	1050	290	880	ns
t_{PLH}	SHIFT OUT ↓	ALMOST F/E		85	115	35	170	35	150	ns
t_{PHL}	SHIFT OUT ↓	HALF FULL		340	410	170	590	170	510	ns
t_{PHL}	$\overline{RST}$ ↓	OR		22	26	10	40	10	34	ns
t_{PLH}	$\overline{RST}$ ↑	IR		12	18	5	24	5	22	ns
t_{PHL}	$\overline{RST}$ ↓	IR		12	18	5	24	5	22	ns
t_{PHL}	$\overline{RST}$ ↓	Q		14	17	5	21	5	19	ns
t_{dis}	$\overline{OE}$ ↑	Q		7	13	2	16	2	15	ns
t_{en}	$\overline{OE}$ ↓	Q		6	12	2	15	2	13	ns

† The IR output pulse occurs when the FIFO is full, Shift In is high, and Shift Out is pulsed (see Figure 4).
‡ The OR output pulse occurs when the FIFO is empty, Shift Out is high, and Shift In is pulsed (see Figure 3).
§ Data throughput or "fall through" times
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2958, OCTOBER 1986

TYPICAL APPLICATION INFORMATION

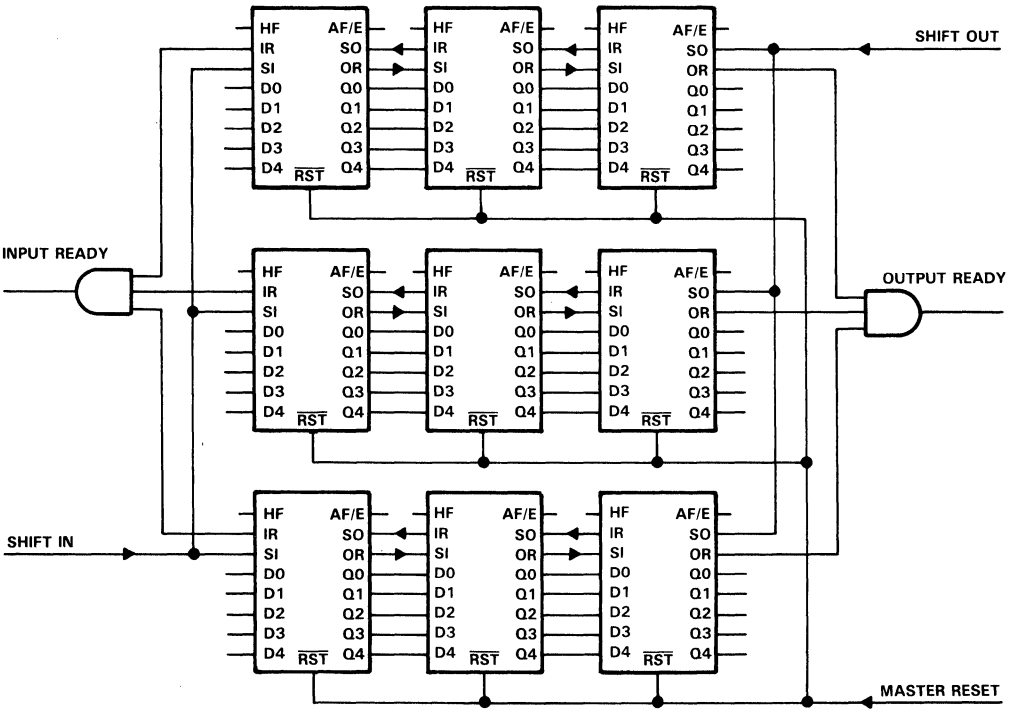
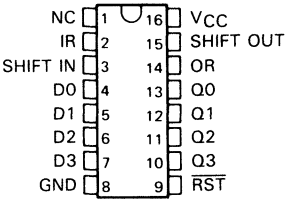


FIGURE 8. 192-WORD BY 15-BIT EXPANSION

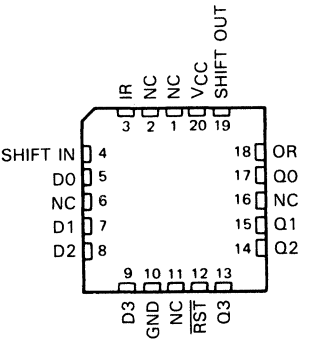
D2958, OCTOBER 1986—REVISED APRIL 1988

- **Asynchronous Operation**
- **Organized as 64 Words of 4 Bits**
- **Data Rates From 0 to 30 MHz**
- **Pin-Compatible With MMI67401B With Higher Speed**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS236 . . . J PACKAGE
SN74ALS236 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS236 . . . FK PACKAGE
SN74ALS236. . . FN PACKAGE
(TOP VIEW)



NC—No internal connection.

description

The SN54ALS236 and SN74ALS236 are 256-bit memories utilizing Advanced Low-Power Schottky IMPACT™ Technology. They feature high speed with fast fall-through times and are organized as 64 words by 4 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ALS236 is designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the Shift In input. When Shift In goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional Shift In pulses have no effect. Data is shifted out of memory on the falling edge of the Shift Out input (see Figure 2). When the FIFO is empty, additional Shift Out pulses have no effect. The last data word remains at the outputs until a new word falls through or $\overline{RST}$ goes low

Status of the 'ALS236 FIFO memory is monitored by the Output Ready (OR) and Input Ready (IR) flags. When the OR flag is high, valid data is available at the outputs. The OR flag is low when Shift Out is high and will stay low when the FIFO is empty. The IR status flag is high when the inputs are ready to receive more data. The IR flag is low when Shift In is high and stays low when the FIFO is full.

When the FIFO is empty, input data is shifted to the output automatically when Shift In goes low. If Shift Out is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

When the FIFO is full, data can be shifted in automatically by holding Shift In high and taking Shift Out low. A propagation delay after Shift Out goes low, IR will go high. If Shift In is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low when the FIFO is full and Shift In is high, only a high-level pulse is seen on the IR output (see Figure 4).

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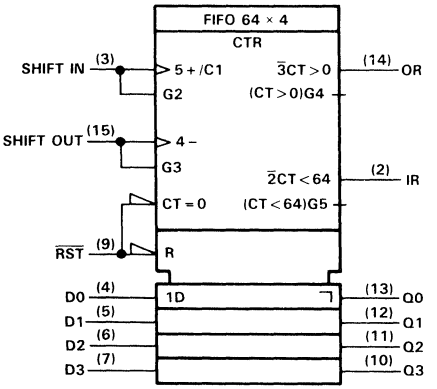
D2958, OCTOBER 1986—REVISED APRIL 1988

description (continued)

The FIFO must be reset after power up with a low-level pulse on the Master Reset input ($\overline{RST}$). This sets Input Ready (IR) high and Output Ready (OR) low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If Shift In is high when $\overline{RST}$ goes high, the input data is shifted in and IR goes low and remains low until Shift In goes low. If Shift In goes low before $\overline{RST}$ goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs.

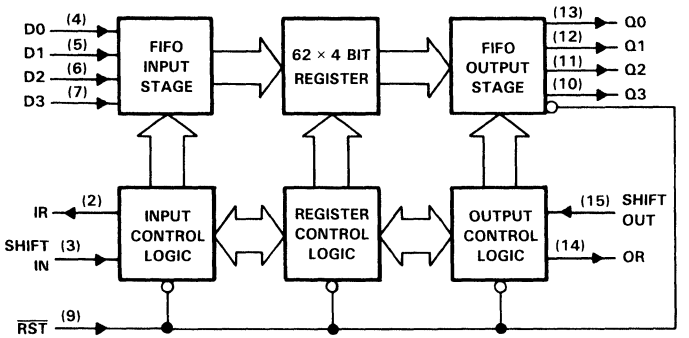
The SN54ALS236 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS236 is characterized for operation from 0°C to 70°C.

logic symbol†



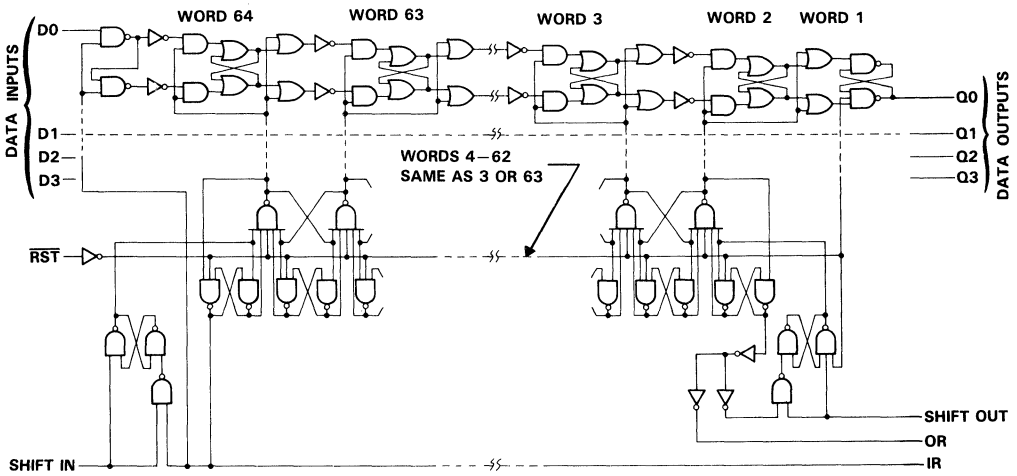
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram

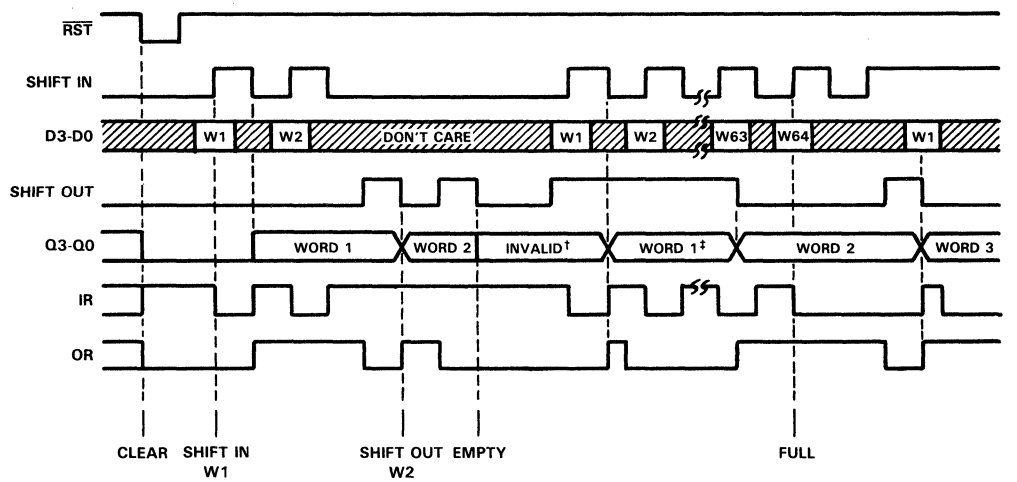


Pin numbers shown are for DW, J, and N packages.

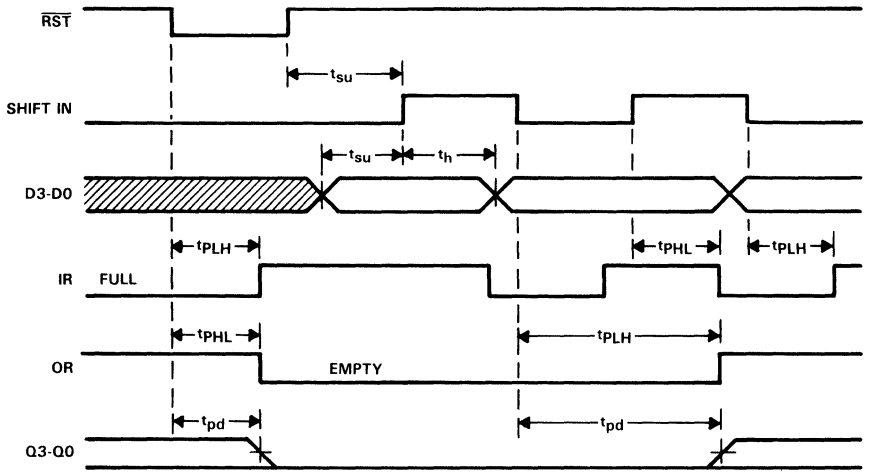
logic diagram (positive logic)



timing diagram

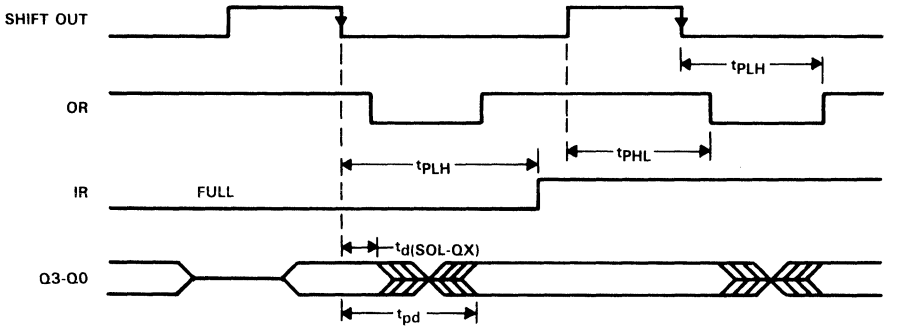


† The last data word shifted out of the FIFO remains at the output until a new word falls through or a $\overline{RST}$ pulse clears the FIFO.
‡ While the output data is considered valid only when the OR flag is high, the stored data remains at the output. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until SHIFT OUT is taken low.



NOTE: SHIFT OUT is low

FIGURE 1. MASTER-RESET AND DATA-IN WAVEFORMS



NOTE: SHIFT IN is low

FIGURE 2. DATA-OUT WAVEFORMS

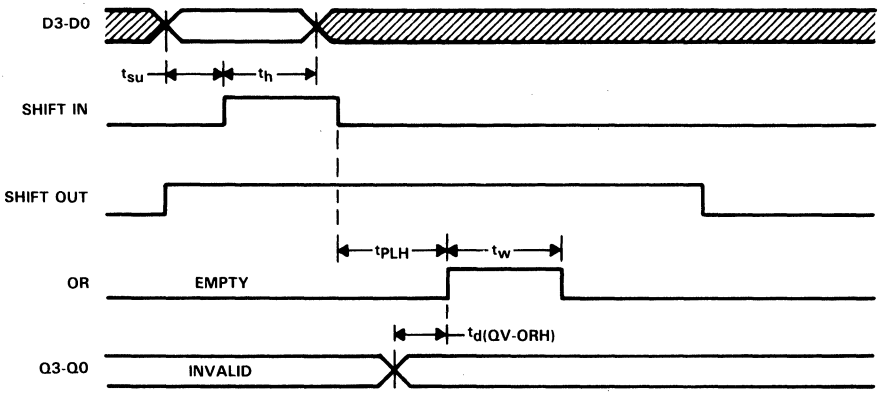


FIGURE 3. DATA FALL-THROUGH WAVEFORMS

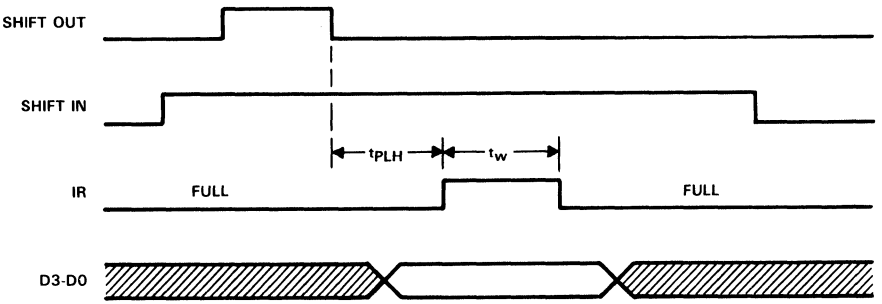


FIGURE 4. AUTOMATIC DATA-IN WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS236 . . . . . −55°C to 125°C
SN74ALS236 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS236			SN74ALS236			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Q outputs			−1			−2.6	mA
		IR and OR			−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs			12			24	mA
		IR and OR			4			8	
f_{clock}	Clock frequency	SHIFT IN or SHIFT OUT	0		25	0		30	MHz
t_w	Pulse duration	SHIFT IN or SHIFT OUT high or low	17			15			ns
		$\overline{RST}$ low	20			15			
t_{su}	Setup time before SHIFT IN ↑	Data	0			0			ns
		$\overline{RST}$ high (inactive)	15			15			
t_h	Hold time, data after SHIFT IN ↑		19			17			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS236			SN74ALS236			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Q	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
	IR, OR	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		
V_{OL}	Q	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	IR, OR	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.4		0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	I_{CCL}		100	155		100	145	mA
			I_{CCH}		97	152		97	142	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS236			SN54ALS236		SN74ALS236		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	SHIFT IN			35		25		30		MHz
	SHIFT OUT			35		25		30		
t_w†	IR high			15		7		8		ns
t_w‡	OR high			19		7		8		ns
$t_{d(QV-ORH)}$	Q valid before OR ↑			6	9	−5	12	−5	12	ns
$t_{d(SOL-QX)}$	Q valid after SHIFT OUT ↓			13		4		4		ns
t_{pd}	SHIFT IN ↓	Q		600	800	350	1200	350	1000	ns
t_{PHL}	SHIFT IN ↑	IR		20	26	8	36	8	30	ns
t_{PLH}	SHIFT IN ↓	IR		16	21	6	28	6	25	ns
t_{PLH}§	SHIFT IN ↓	OR		600	800	350	1200	350	1000	ns
t_{pd}	SHIFT OUT ↓	Q		13	17	4	24	4	22	ns
t_{PHL}	SHIFT OUT ↑	OR		23	27	7	39	7	33	ns
t_{PLH}	SHIFT OUT ↓	OR		20	24	6	33	6	30	ns
t_{PLH}§	SHIFT OUT ↓	IR		600	800	350	1200	350	1000	ns
t_{PHL}	$\overline{RST}$ ↓	OR		22	26	10	40	10	34	ns
t_{PLH}	$\overline{RST}$ ↓	IR		17	21	6	31	6	27	ns
t_{PHL}	$\overline{RST}$ ↓	Q		14	17	5	21	5	19	ns

† The IR output pulse occurs when the FIFO is full, Shift In is high, and Shift Out is pulsed (see Figure 4).
‡ The OR output pulse occurs when the FIFO is empty, Shift Out is high, and Shift In is pulsed (see Figure 3).
§ Data Throughput or "fall through" times
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION INFORMATION

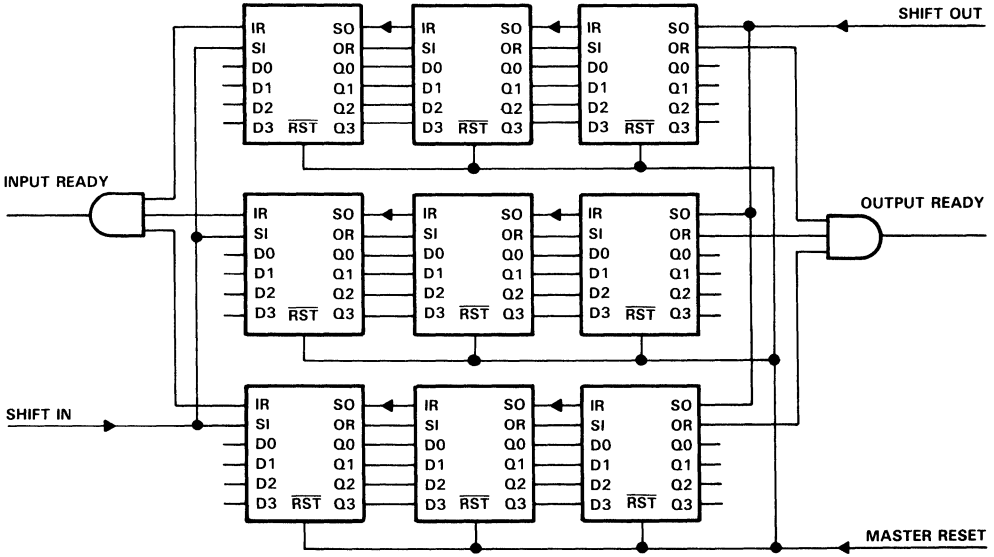
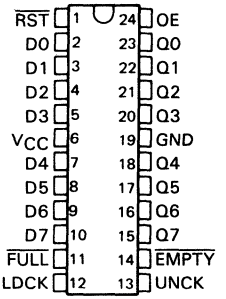


FIGURE 5. 192-WORD BY 12-BIT EXPANSION

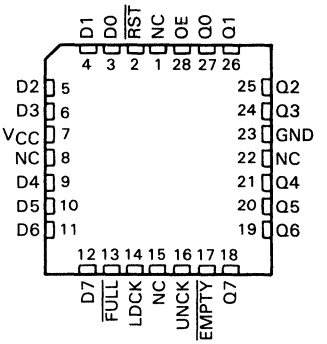
D3091, FEBRUARY 1988–REVISED MARCH 1990

- **Independent Asynchronous Inputs and Outputs**
- **64 Words by 8 Bits Each**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 20 ns Typ**
- **3-State Outputs**

NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

This 512-bit memory uses Advanced Low-Power Schottky IMPACT-X™ technology and features high speed and fast fall-through times. It is organized as 64 words by 8 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The function is used as a buffer to couple two buses operating at different clock rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition of the load clock input (LDCK) and is read out on a low-to-high transition of the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 64 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ output flags. The $\overline{\text{FULL}}$ output will be low when the memory is full, and high when the memory is not full. The $\overline{\text{EMPTY}}$ output will be low when the memory is empty, and high when it is not empty.

A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and $\overline{\text{FULL}}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a $\overline{\text{RST}}$ pulse or from an empty condition, causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. The first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at a high-impedance state when the output-enable input (OE) is low. The OE input does not effect either the $\overline{\text{FULL}}$ or $\overline{\text{EMPTY}}$ output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

The SN74ALS2232A is characterized for operation from 0°C to 70°C.

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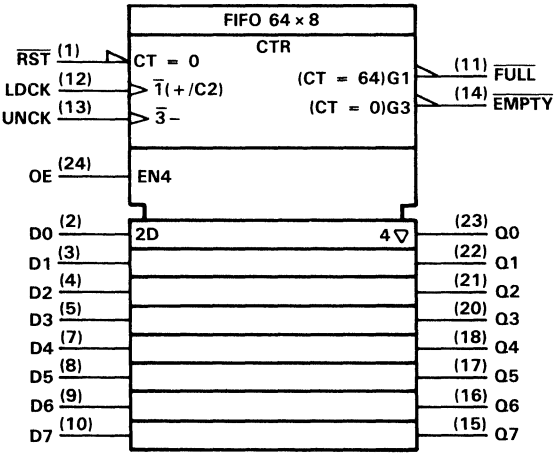
logic symbol†



†This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

Pin numbers shown are for the NT package.

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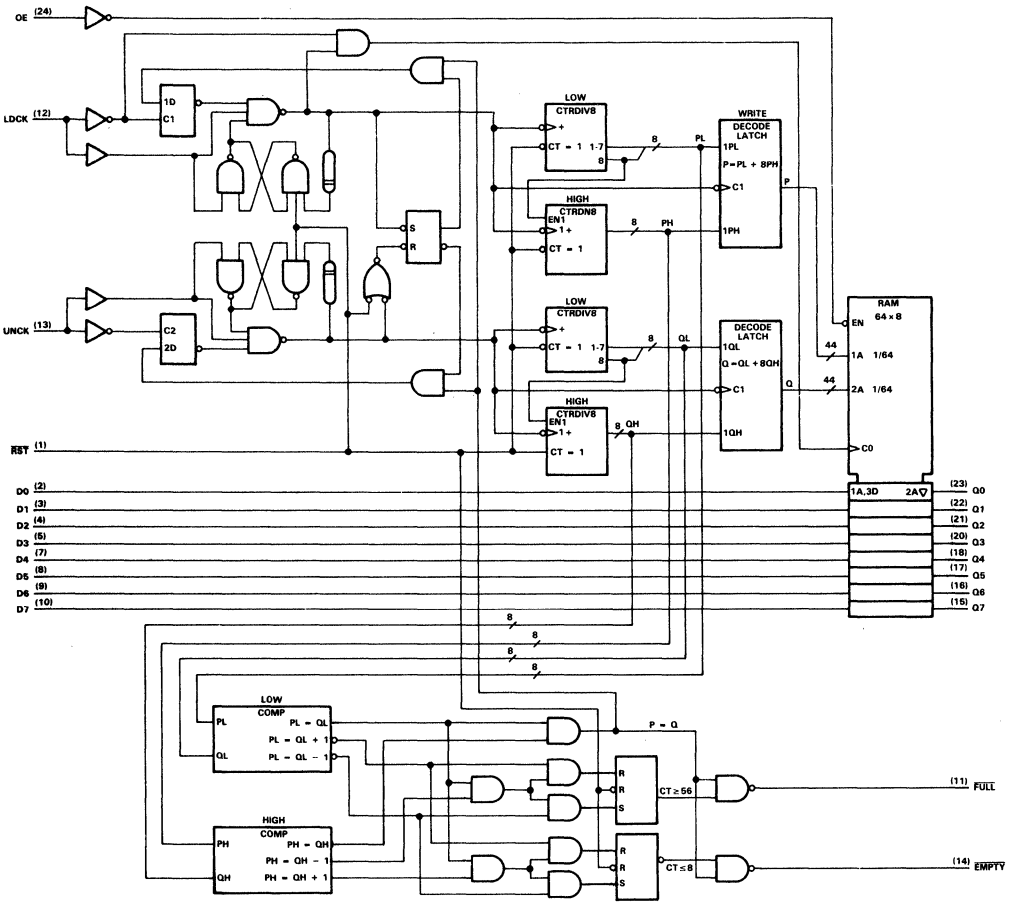
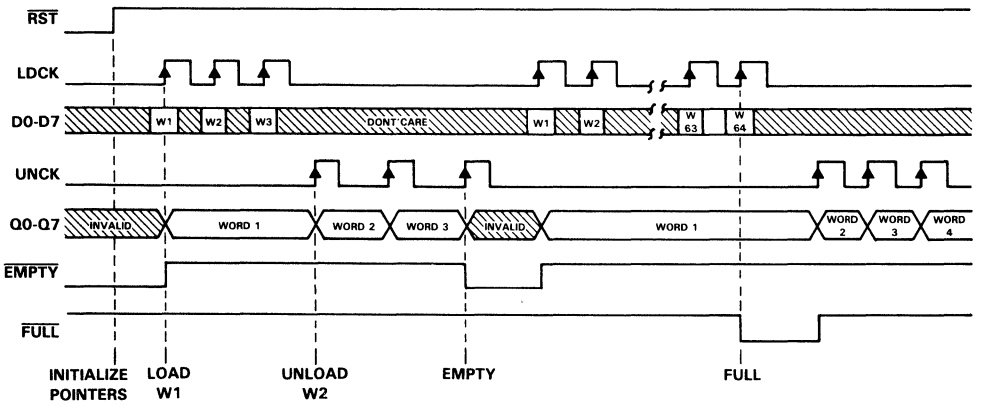
logic diagram (positive logic)



Pin numbers shown are for the NT package.

timing diagram



absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−2.6	mA
		$\overline{FULL}$, $\overline{EMPTY}$			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		$\overline{FULL}$, $\overline{EMPTY}$			8	
f_{clock}	Clock frequency	LDCK, UNCK	0		40	MHz
t_w	Pulse duration	$\overline{RST}$ low	25			ns
		LDCK low	13			
		LDCK high	12			
		UNCK low	13			
		UNCK high	12			
t_{su1}	Setup time, data before LDCK↑		5			ns
t_{su2}	Setup time, $\overline{RST}$ high (inactive) before LDCK↑		5			ns
t_h	Hold time, data after LDCK↑		5			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			1.2	V
V_{OH}	$\overline{FULL}$, $\overline{EMPTY}$	V_{CC} = MIN TO MAX,	I_{OH} = 0.4 mA	V_{CC}−2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
	$\overline{FULL}$, $\overline{EMPTY}$		I_{OL} = 4 mA		0.25	0.4	
			I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	CLKS	V_{CC} = 5.5 V,	V_{IN} = 0.4 V			−0.2	mA
	Others					−0.1	
I_O‡	Q outputs	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−130	mA
	$\overline{FULL}$, $\overline{EMPTY}$			−20		−112	
I_{CC}		V_{CC} = 5.5 V			175	270	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}	LDCK					40		MHz
	UNCK					40		
t_{pd}	LDCK↑	Any Q		18	26		30	ns
t_{pd}	UNCK↑	Any Q		18	24		27	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$		12	16		18	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$		12	17		20	ns
t_{PHL}	$\overline{RST}$↓	$\overline{EMPTY}$		12	17		20	ns
t_{PHL}	LDCK↑	$\overline{FULL}$		16	21		22	ns
t_{PLH}	UNCK↑	$\overline{FULL}$		10	15		18	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$		13	19		23	ns
t_{en}	OE↑	Q		11	15		17	ns
t_{dis}	OE↓	Q		11	17		19	ns

Note 1: Load circuit and voltage waveforms are shown in Section 1.

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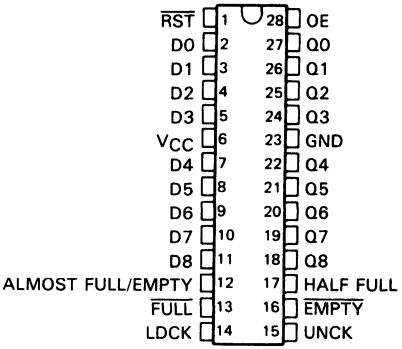
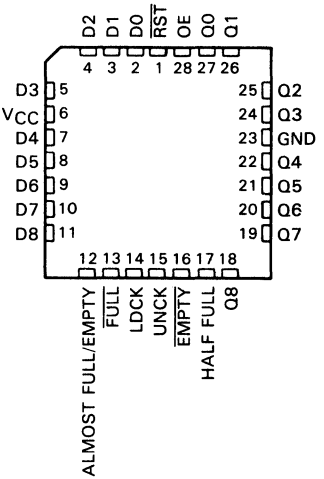
- **Independent Asynchronous Inputs and Outputs**
- **64 Words By 9 Bits**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 20 ns Typical**
- **3-State Outputs**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

This 576-bit memory uses Advanced Low-Power Schottky IMPACT—X™ technology and features high speed and fast fall-through times. It is organized as 64 words by 9 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The function is used as a buffer to couple two buses operating at different clock rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition of the load clock input (LDCK) and is read out on a low-to-high transition of the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 64 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, ALMOST FULL/EMPTY, and HALF FULL output flags. The $\overline{\text{FULL}}$ output will be low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output will be low when the memory is empty and high when it is not empty. The ALMOST FULL/EMPTY flag is high when the FIFO contains eight or less words or fifty-six or more words. The ALMOST FULL/EMPTY flag is low when the FIFO contains between nine and fifty-five words. The HALF FULL flag is high when the FIFO contains thirty-two or more words, and is low when the FIFO contains thirty-one words or less.

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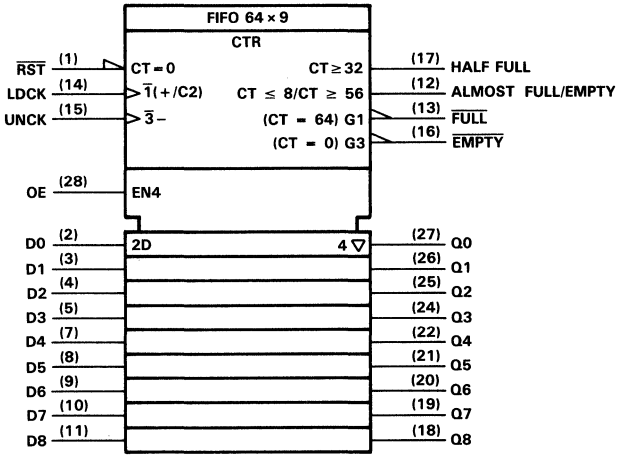
description (continued)

A low level on the reset input ($\overline{RST}$) resets the internal stack control pointers and also sets EMPTY low and $\overline{FULL}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a $\overline{RST}$ pulse or from an empty condition, causes $\overline{EMPTY}$ to go high and the data to appear on the Q outputs. The first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at a high-impedance state when the output-enable input (OE) is low. The OE input does not affect either the $\overline{FULL}$ or $\overline{EMPTY}$ output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

The SN74ALS2233A is characterized for operation from 0°C to 70°C.

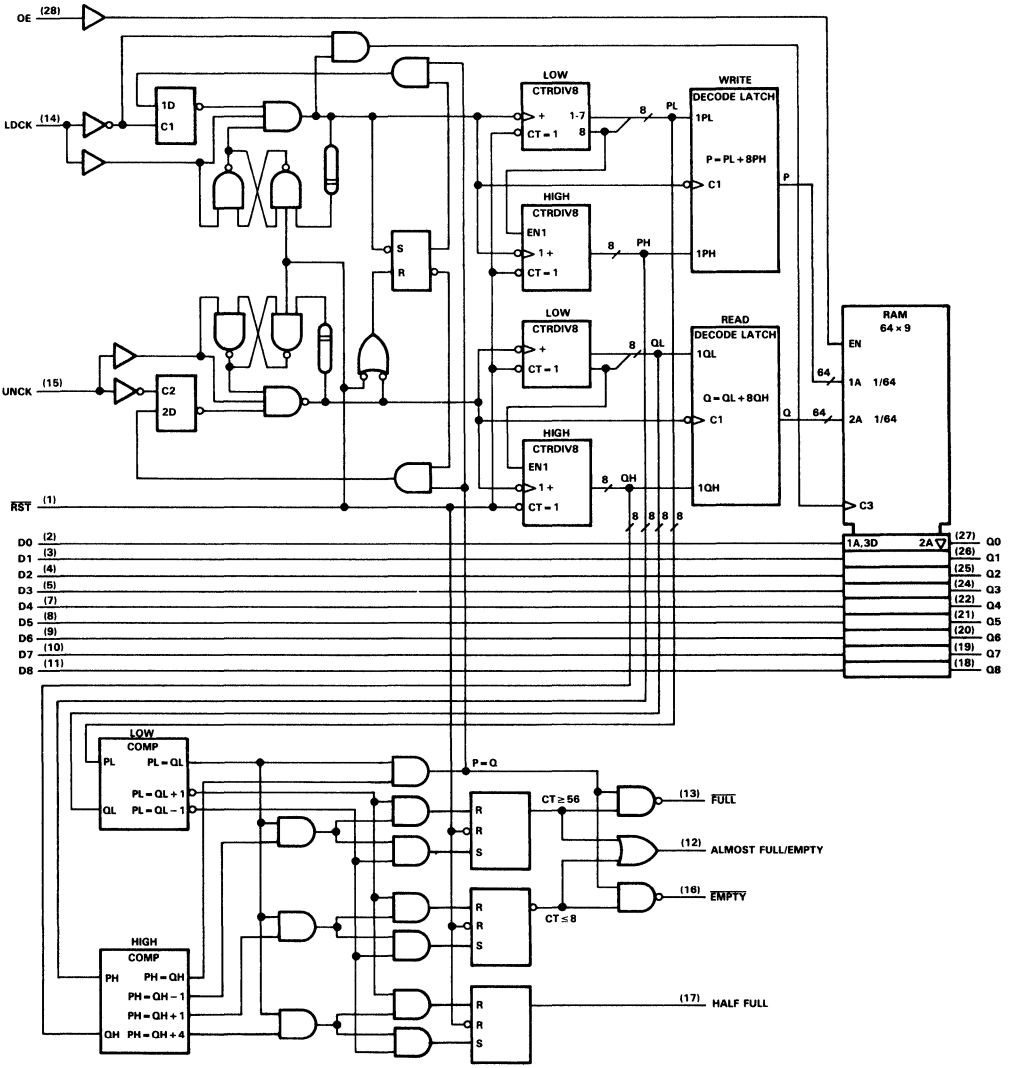
logic symbol†



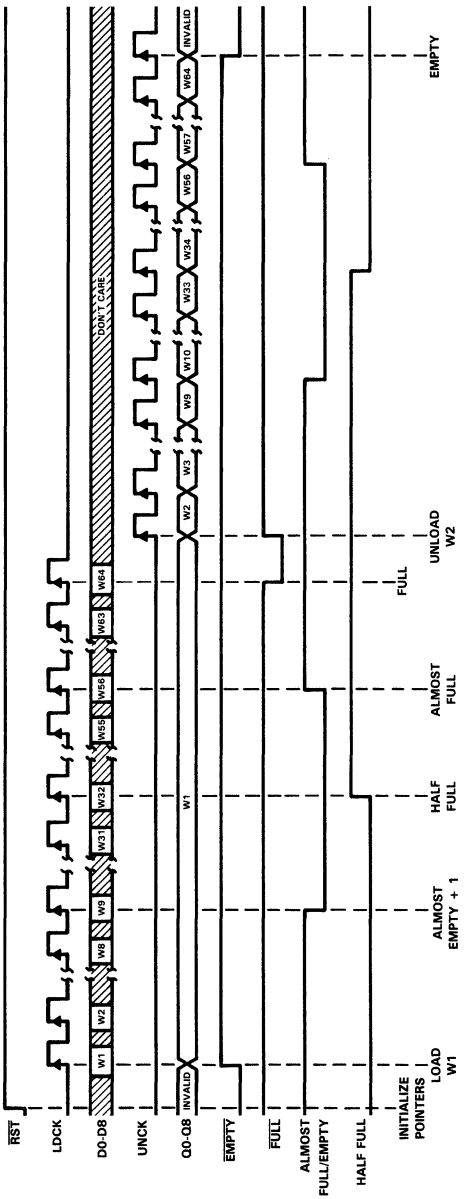
†This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

Pin numbers shown are for the N package.

logic diagram (positive logic)



timing diagram



absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−2.6	mA
		Flag outputs			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		Flag outputs			8	
f_{clock}	Clock frequency	LDCK, UNCK	0		40	MHz
t_w	Pusle duration	$\overline{RST}$ low	25			ns
		LDCK low	13			
		LDCK high	12			
		UNCK low	13			
		UNCK high	12			
t_{su1}	Setup time, data before LDCK↑		5			ns
t_{su2}	Setup time, $\overline{RST}$ high (inactive) before LDCK↑		5			ns
t_h	Hold time, data after LDCK↑		5			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDTIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			1.2	V
V_{OH}	Flag outputs	V_{CC} = MIN TO MAX,	I_{OH} = 0.4 mA	V_{CC}−2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	Q Outputs	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
	Flag outputs		I_{OL} = 4 mA		0.25	0.4	
			I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	CLKs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
	Others					−0.1	
I_O‡	Q outputs	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−130	mA
	Flag outputs			−20		−112	
I_{CC}		V_{CC} = 5.5 V			175	290	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}	LDCK					40		MHz
	UNCK					40		
t_{pd}	LDCK↑	Any Q		18	26		30	ns
t_{pd}	UNCK↑	Any Q		18	24		27	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$		12	16		18	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$		12	17		20	ns
t_{PHL}	RST↓	$\overline{EMPTY}$		12	17		20	ns
t_{PHL}	LDCK↑	$\overline{FULL}$		16	21		22	ns
t_{PLH}	UNCK↑	$\overline{FULL}$		10	15		18	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$		13	19		23	ns
t_{PLH}	LDCK↑	ALMOST		22	27		30	ns
t_{PHL}		FULL/EMPTY		19	25		28	
t_{PLH}	UNCK↑	ALMOST		22	27		30	ns
t_{PHL}		FULL/EMPTY		17	23		26	
t_{PLH}	$\overline{RST}$↓	ALMOST FULL/EMPTY		12	16		18	
t_{PLH}	LDCK↑	HALF FULL		22	27		30	ns
t_{PHL}	$\overline{RST}$↓	HALF FULL		28	32		35	ns
t_{PHL}	UNCK↑	HALF FULL		16	22		25	ns
t_{en}	OE↑	Q		11	15		17	ns
t_{dis}	OE↓	Q		11	17		19	ns

Note 1: Load circuits and voltage waveforms are shown in Section 1.

- **Independent Asychronous Inputs and Outputs**
- **Bidirectional**
- **32 Words by 9 Bits Each**
- **Programmable Depth**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 22 ns Typ**
- **3-State Outputs**

description

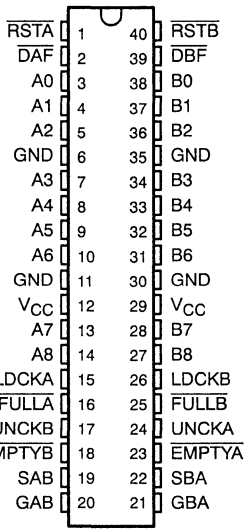
This 576-bit memory uses Advanced Low-Power Schottky IMPACT-X™ technology and features high speed and fast fall-through times. It consists of two FIFOs organized as 32 words by 9 bits each.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

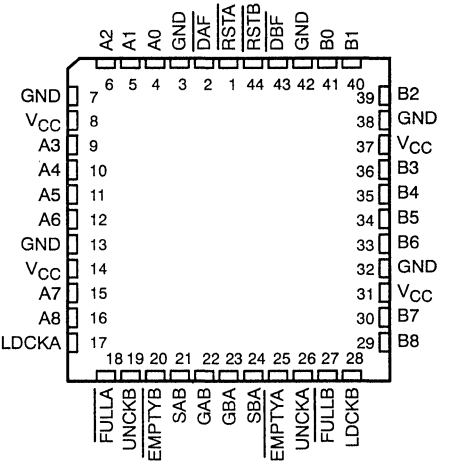
The 'ALS2238 consists of bus transceiver circuits, two 32 X 9 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enables GAB and GBA are provided to control the transceiver functions. The SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low level selects real-time data and a high selects stored data. Eight fundamental bus-management functions can be performed as shown on the operating modes page.

Data on the A or B data bus, or both, is written into the FIFOs on a low-to-high transition at the load clock input (LDCKA or LDCKB) and is read out on a low-to-high transition at the unload clock input (UNCKA or UNCKB). The memory is full when the number of words clocked in exceeds, by the defined depth, the number of words clocked out.

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



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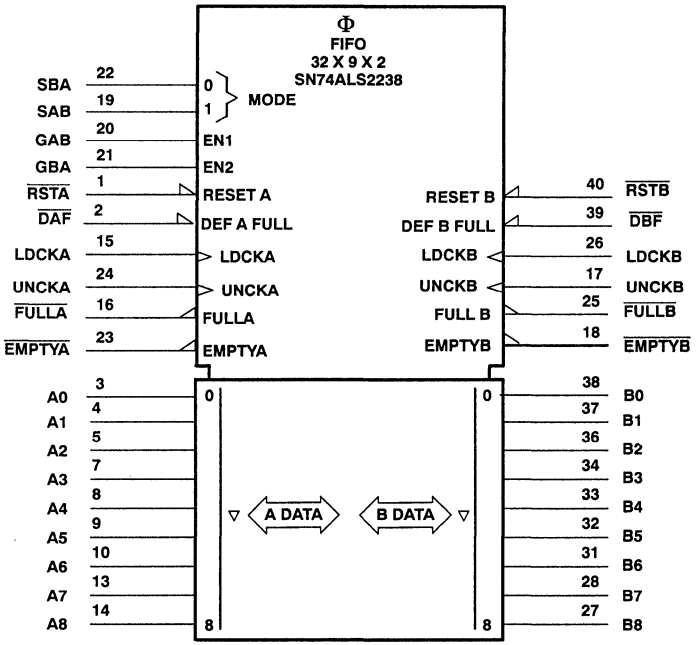
When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memories is monitored by the $\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$, $\overline{\text{EMPTYA}}$, and $\overline{\text{EMPTYB}}$ output flags. The $\overline{\text{FULLA}}$ and $\overline{\text{FULLB}}$ are definable full flags. A high-to-low transition on $\overline{\text{DAF}}$ stores the binary value of A0 through A4 into a register for use as the value of X. A high-to-low transition on $\overline{\text{DBF}}$ stores the binary value of B0 through B4 into a register for use as the value of Y. In this way, the depth of either FIFO can be defined to be one to thirty-two words deep. The value of X and Y must be defined after power-up or the stored value of X and Y will be ambiguous. The $\overline{\text{FULLA}}$ and $\overline{\text{FULLB}}$ outputs are low when their corresponding memories are full and high when the memories are not full.

The $\overline{\text{EMPTYA}}$ and $\overline{\text{EMPTYB}}$ outputs are low when their corresponding memories are empty and high when they are not empty. The status flag outputs are always active.

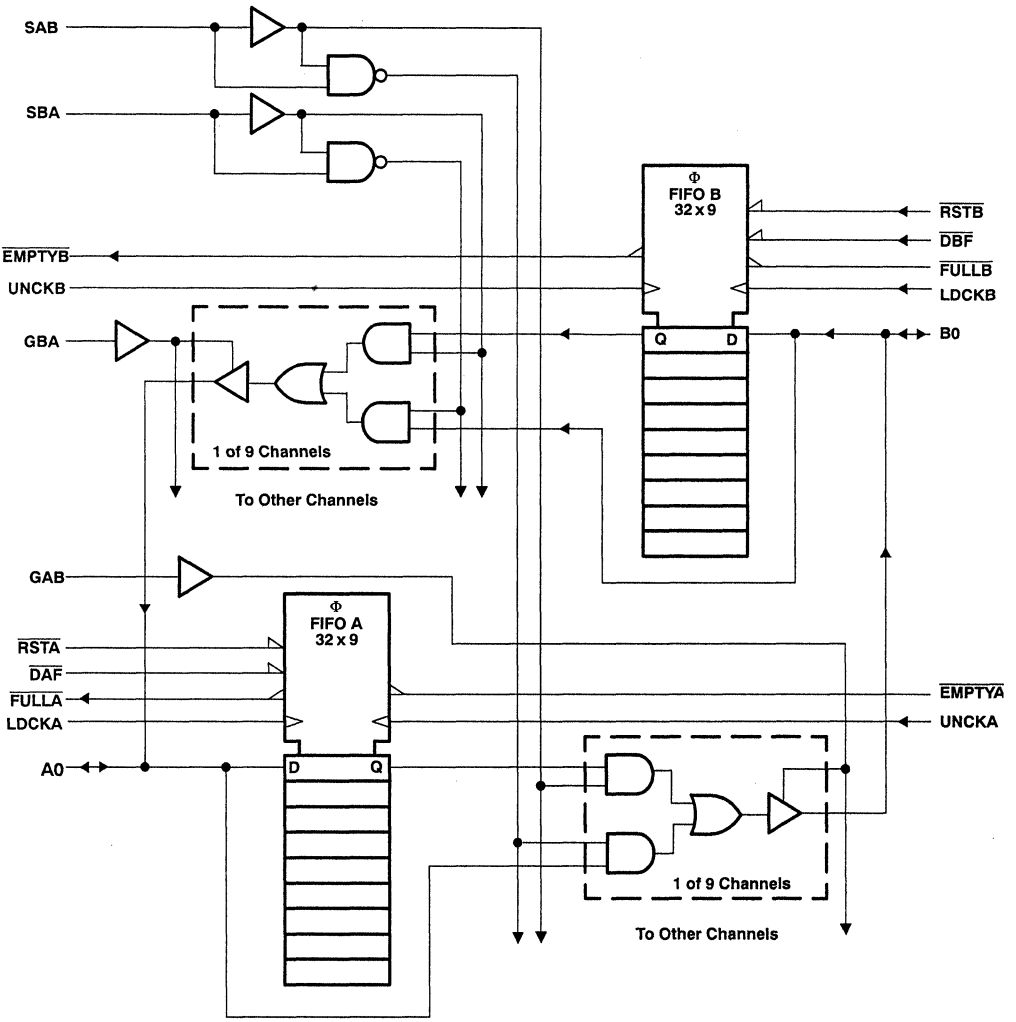
A low-level pulse on the $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ inputs resets the control pointers on FIFO A or FIFO B and also sets $\overline{\text{EMPTYA}}$ low and $\overline{\text{FULLA}}$ high or $\overline{\text{EMPTYB}}$ low and $\overline{\text{FULLB}}$ high. The outputs are not reset to any specific logic levels. With $\overline{\text{DAF}}$ at a low level, a low-level pulse on $\overline{\text{RSTA}}$ sets FIFO A to a depth of 32 minus X, where X is the value stored above. With $\overline{\text{DAF}}$ at a high level, a low level pulse on $\overline{\text{RSTA}}$ sets FIFO A to a depth of 32 words. The depth of FIFO B is set in a similar manner. The first low-to-high transition on LDCKA or LDCKB, either after a reset pulse or from an empty condition, will cause $\overline{\text{EMPTYA}}$ or $\overline{\text{EMPTYB}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

logic symbol†

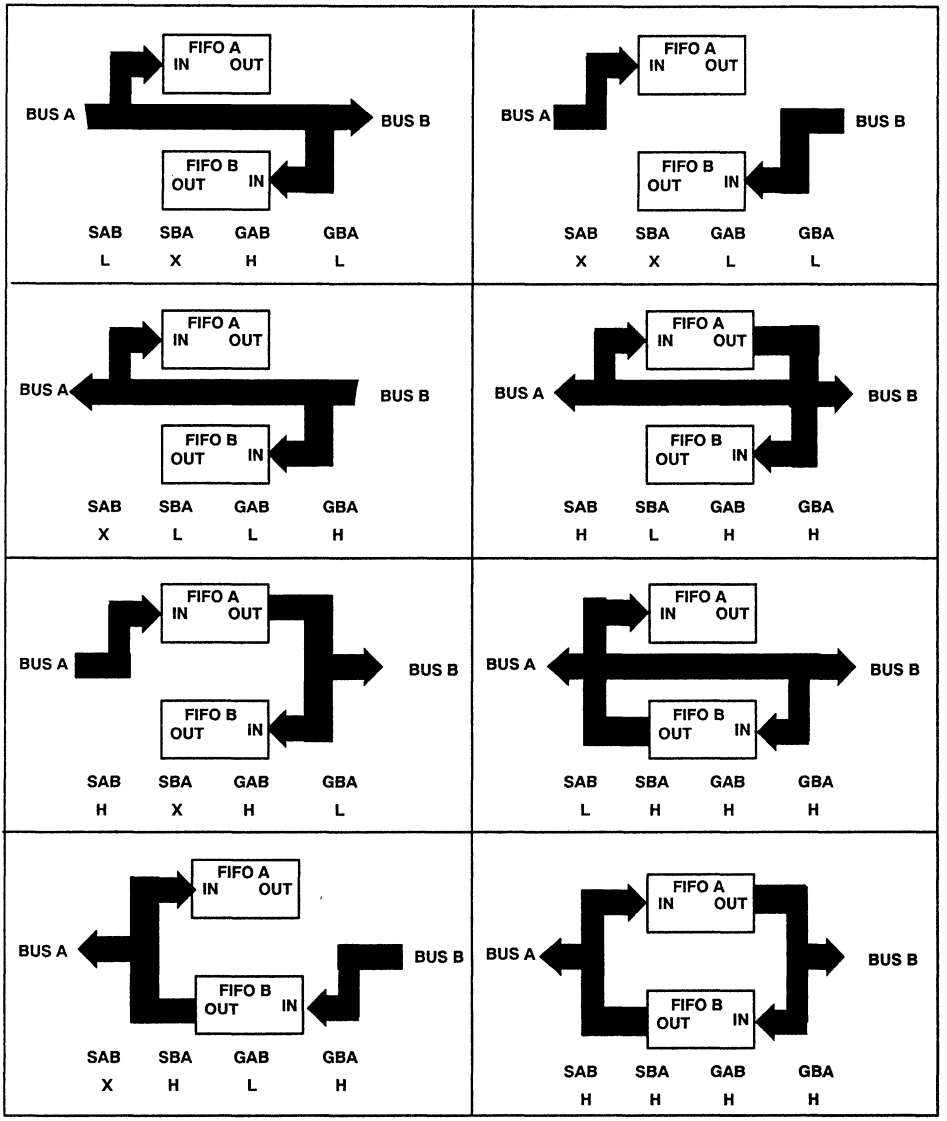


† This symbol is in accordance with ANSI/IEEE Std 91-1984.
Pin numbers shown are for the N package.

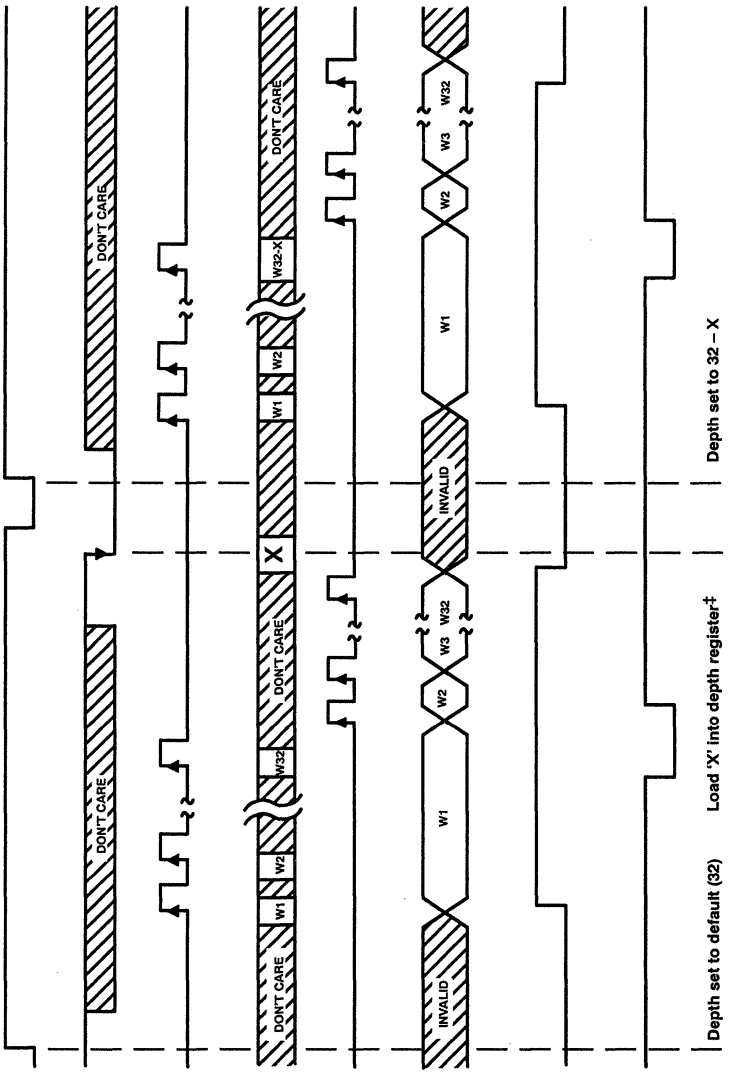
logic diagram (positive logic)



operating modes



timing diagram



† Operation of FIFO 'B' is the same as shown above.
‡ 'X' includes A0 through A4 only. A5 through A8 are ignored.

FUNCTION TABLES

SELECT MODE CONTROL TABLE

CONTROL		OPERATION	
SBA	SAB	A Bus	B Bus
L	L	Real Time B to A Bus	Real Time A to B Bus
H	L	FIFO B to A Bus	Real Time A to B Bus
L	H	Real Time B to A Bus	FIFO A to B Bus
H	H	FIFO B to A Bus	FIFO A to B Bus

OUTPUT ENABLE CONTROL TABLE

CONTROL		OPERATION	
GBA	GAB	A Bus	B Bus
H	H	A Bus Enabled	B Bus Enabled
H	L	A Bus Enabled	Isolation/Input to B Bus
L	H	Isolation/Input to A Bus	B Bus Enabled
L	L	Isolation/Input to A Bus	Isolation/Input to B Bus

programming procedure for depth of FIFO A†

PROGRAM:

Step 1. With $\overline{\text{RSTA}}$ at a high level, take $\overline{\text{DAF}}$ from a high level to a low level. The high-to-low transition on $\overline{\text{DAF}}$ stores the binary value of A0-A4 for use as the value of 'X' in defining the depth of FIFO A.

Step 2. With $\overline{\text{DAF}}$ held low, pulse the $\overline{\text{RSTA}}$ signal low. On the low-to-high transition of $\overline{\text{RSTA}}$, FIFO A is set to a depth of 32 minus 'X', where X is the value of A0-A4 stored above.

Step 3. To redefine the depth of FIFO A to 32 words, hold $\overline{\text{DAF}}$ at a high level and pulse the $\overline{\text{RSTA}}$ signal low.

† The programming procedures used to define the depth of FIFO B are the same as the procedure above.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage: Control inputs ..... 7 V
I/O ports ..... 5.5 V
Voltage applied to a diabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Maximum junction temperature ..... 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	A or B Ports			−15	mA
		Status flags			−0.4	
I_{OL}	Low-level output current	A or B Ports			24	mA
		Status flags			8	
f_{clock}	Clock frequency	LDCKA or LDCKB	0		40	MHz
		UNCKA or UNCKB	0		40	
t_w	Pulse duration	$\overline{RSTA}$ or $\overline{RSTB}$ low	17			ns
		LDCKA or LDCKB low	12.5			
		LDCKA or LDCKB high	10			
		UNCKA or UNCKB low	12.5			
		UNCKA or UNCKB high	10			
		$\overline{DAF}$ or $\overline{DBF}$ high	10			
t_{su}	Setup time	Data before LDCKA or LDCKB↑	7			ns
		Define Depth: D4-D0 before $\overline{DAF}$ or $\overline{DBF}$↓	6			
		Define Depth: $\overline{DAF}$ or $\overline{DBF}$↓ before $\overline{RSTA}$ or $\overline{RSTB}$↑	45			
		Define Depth (32): $\overline{DAF}$ or $\overline{DBF}$ high before $\overline{RSTA}$ or $\overline{RSTB}$↑	32			
		LDCKA or LDCKB (inactive) before $\overline{RSTA}$ or $\overline{RSTB}$↑	5			
t_h	Hold time	Data after LDCKA or LDCKB↑	3			ns
		Define Depth: D4-D0 after $\overline{DAF}$ or $\overline{DBF}$↓	4			
		Define Depth: $\overline{DAF}$ or $\overline{DBF}$ low after $\overline{RSTA}$ or $\overline{RSTB}$↑	0			
		Define Depth (32): $\overline{DAF}$ or $\overline{DBF}$ high after $\overline{RSTA}$ or $\overline{RSTB}$↑	0			
		LDCKA or LDCKB (inactive) after $\overline{RSTA}$ or $\overline{RSTB}$↑	5			
T_A	Operating free-air temperature		0		70	°C

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCKA or LDCKB and UNCKA or UNCKB clock inputs. Any excessive noise or glitching on the clock inputs (which violates the V_{IL}, V_{IH}, or minimum pulse duration limits) can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = – 18 mA			– 1.2	V
V_{OH}	Status flags	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = – 0.4 mA	V_{CC} – 2			V
	A or B ports	V_{CC} = 4.5 V,	I_{OH} = – 2 mA	V_{CC} – 2			
		V_{CC} = 4.5 V,	I_{OH} = – 3 mA	2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = – 15 mA	2			
V_{OL}	A or B ports	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	Status flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_I	$\overline{DAF}$, $\overline{DBF}$, $\overline{RSTA}$, $\overline{RSTB}$, GAB, GBA, SAB, SBA, LDCKA, LDCKB, UNCKA, UNCKB	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	A or B ports					0.2	
I_{IH}	$\overline{DAF}$, $\overline{DBF}$, $\overline{RSTA}$, $\overline{RSTB}$, GAB, GBA, SAB, SBA, LDCKA, LDCKB, UNCKA, UNCKB	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
	A or B ports‡					40	
I_{IL}	$\overline{DAF}$, $\overline{DBF}$, $\overline{RSTA}$, $\overline{RSTB}$, GAB, GBA, SAB, SBA, LCKA, LDCKB, UNCKA, UNCKB	V_{CC} = 5.5 V,	V_I = 0.4 V			– 0.2	mA
	A or B ports‡					– 0.4	
I_O§	A or B ports‡	V_{CC} = 5.5 V,	V_O = 2.25 V	– 20		– 130	mA
	Status flags			– 15		– 100	
I_{CC}		V_{CC} = 5.5 V			190	350	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the offstate output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output ccurrent, I_{OS}.

switching characteristics (see Note 2)

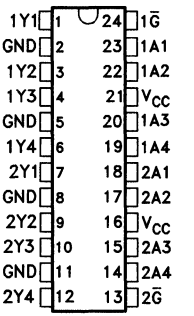
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX			UNIT
			MIN	TYP†	MAX	
f_{max}	LDCK		40			MHz
	UNCK		40			
t_{pd}	LDCKA↑, LDCKB↑	B/A	7	22	33	ns
t_{pd}	UNCKA↑, UNCKB↑	B/A	7	20	29	ns
t_{PLH}	LDCKA↑, LDCKB↑	$\overline{EMPTYA}$, $\overline{EMPTYB}$	5	12	22	ns
t_{PHL}	UNCKA↑, UNCKB↑	$\overline{EMPTYA}$, $\overline{EMPTYB}$	5	12	22	ns
t_{PHL}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	$\overline{EMPTYA}$, $\overline{EMPTYB}$	5	12	22	ns
t_{PHL}	LDCKA↑, LDCKB↑	$\overline{FULLA}$, $\overline{FULLB}$	5	12	22	ns
t_{PLH}	UNCKA↑, UNCKB↑	$\overline{FULLA}$, $\overline{FULLB}$	5	12	23	ns
t_{LH}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	$\overline{FULLA}$, $\overline{FULLB}$	6	15	28	ns
t_{pd}	SAB/SBA‡	B/A	2	11	18	ns
t_{pd}	A/B	B/A	2	8	15	ns
t_{en}	GBA/GAB	A/B	2	6	15	ns
t_{dis}	GBA/GAB	A/B	1	5	12	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **Package Options Include Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT25240 ... JT PACKAGE
SN74BCT25240 ... NT PACKAGE
(TOP VIEW)



description

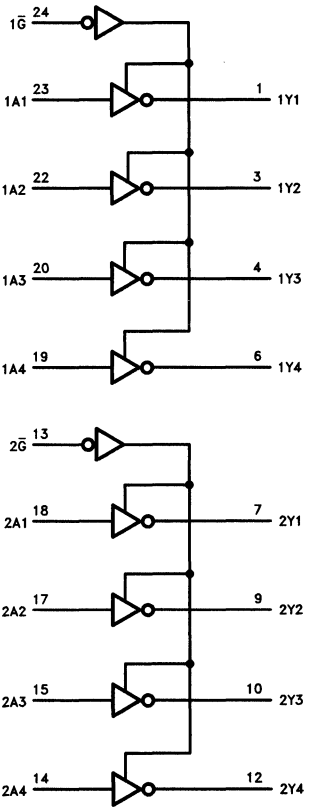
The 'BCT25240 is an octal inverting buffer/line driver. The outputs are designed to source up to 80 mA and to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω.

When the output-enable inputs $1\overline{G}$ and $2\overline{G}$ are low, the device transmits the inverted A-input data to the Y outputs. When $1\overline{G}$ and $2\overline{G}$ are high, the outputs are in the high-impedance state. Enable $1\overline{G}$ affects only the 1Y outputs; enable $2\overline{G}$ affects only the 2Y outputs.

The distributed V_{CC} and GND pins of the 'BCT25240 reduce switching noise for more reliable system operation.

The SN54BCT25240 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT25240 is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)

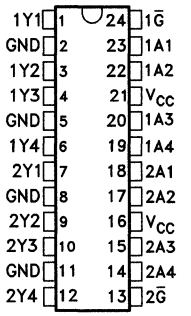


SN54BCT25244, SN74BCT25244 OCTAL 25-OHM LINE DRIVERS WITH 3-STATE OUTPUTS

TI0226—D3533, JUNE 1990

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **Package Options Include Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT25244 ... JT PACKAGE
SN74BCT25244 ... NT PACKAGE
(TOP VIEW)



description

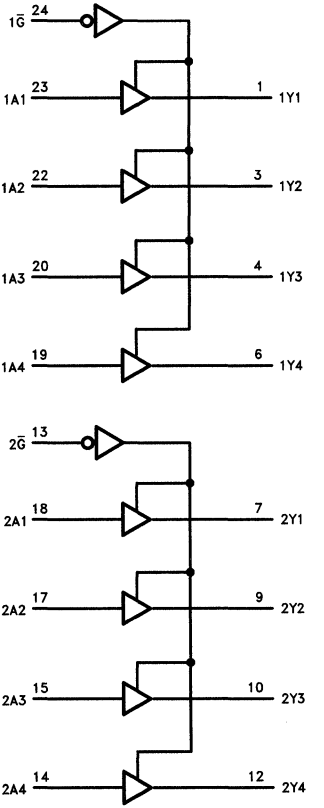
The 'BCT25244 is an octal noninverting buffer/line driver. The outputs are designed to source up to 80 mA and to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω.

When the output-enable inputs $1\overline{G}$ and $2\overline{G}$ are low, the device transmits data from the A inputs to the Y outputs. When $1\overline{G}$ and $2\overline{G}$ are high, the outputs are in the high-impedance state.

The distributed V_{CC} and GND pins of the 'BCT25244 reduce switching noise for more reliable system operation.

The SN54BCT25244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT25244 is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)

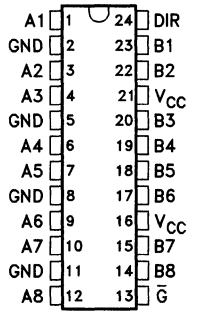


TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

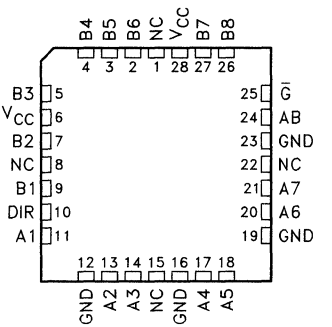
TI0220—D3514, MAY 1990

- **State-of-the-Art BICMOS Design Significantly Reduces I_{CCZ}**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 25 Ω or Greater**
- **Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs**
- **Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)**
- **ESD Protection Exceeds 2000 V per Mil-STD-883C, Method 3015**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT25245 ... JT PACKAGE
SN74BCT25245 ... DW or NT PACKAGE
(TOP VIEW)



SN54BCT25245 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These 25 Ω octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input $\overline{G}$ can be used to disable the device so that the buses are effectively isolated.

These transceivers are capable of sinking 188 mA of I_{OL} current (A port), which facilitates switching 25 Ω transmission lines on the incident wave. They are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers. The distributed V_{CC} and GND pins minimize the noise generated by the simultaneous switching of the outputs.

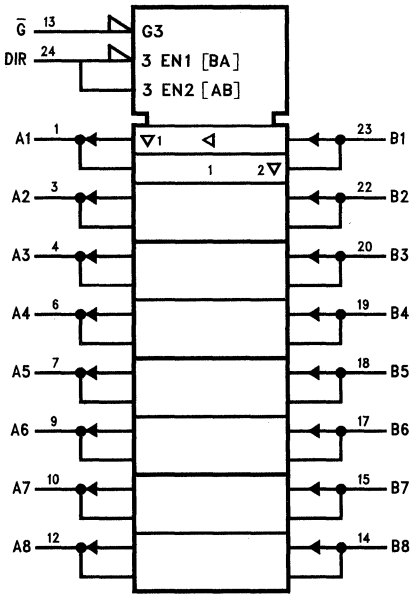
The SN54BCT25245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT25245 is characterized for operation from 0°C to 70°C.

D3514, MAY 1990—TI0220

FUNCTION TABLE

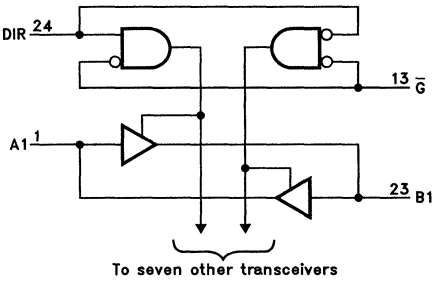
ENABLE INPUTS		OPERATION
$\overline{G}$	DIR	'BCT25245
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range (see Note 1): Control Inputs ..... −0.5 V to 7 V
I/O ports ..... −0.5 V to 5.5 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state (B port) ..... −0.5 V to V_{CC}
Input clamp current ..... −30 mA
Current into any output in the low state: SN54BCT25245 (A port) ..... 250 mA
(B port) ..... 40 mA
SN74BCT25245 (A port) ..... 376 mA
(B port) ..... 48 mA
Operating free-air temperature range: SN54BCT25245 ..... −55°C to 125°C
SN74BCT25245 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			'54BCT25245			'74BCT25245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A1-A8			−53			−80	mA
		B1-B8			−3			−3	
I_{OL}	Low-level output current	A1-A8			125			188	mA
		B1-B8			20			24	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'54BCT25245			'74BCT25245			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Any A	V_{CC} = 4.5 V, I_{OH} = −53 mA	2						V
		V_{CC} = 4.5 V, I_{OH} = −80 mA				2			
		V_{CC} = 4.75 V, I_{OH} = −3 mA				2.7			
	Any B	V_{CC} = 4.5 V, I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
V_{OL}	Any A	V_{CC} = 4.5 V, I_{OL} = 94 mA		0.38	0.55		0.42	0.55	V
		V_{CC} = 4.5 V, I_{OL} = 125 mA			0.8				
		V_{CC} = 4.5 V, I_{OL} = 188 mA						0.7	
	Any B	V_{CC} = 4.5 V, I_{OL} = 20 mA		0.3	0.5				
		V_{CC} = 4.5 V, I_{OL} = 24 mA					0.35	0.5	
I_I	A and B	V_{CC} = 5.5 V, V_I = 5.5 V			0.25			0.25	mA
	DIR and $\overline{G}$	V_{CC} = 5.5 V, V_I = 5.5 V			0.1			0.1	
I_{IH}‡	A and B	V_{CC} = 5.5 V, V_I = 2.7 V			70			70	μA
	DIR and $\overline{G}$	V_{CC} = 5.5 V, V_I = 2.7 V			20			20	
I_{IL}‡	A and B	V_{CC} = 5.5 V, V_I = 0.5 V			−0.6			−0.6	mA
	DIR and $\overline{G}$	V_{CC} = 5.5 V, V_I = 0.5 V			−0.6			−0.6	
I_{OS}§	B port only¶	V_{CC} = 5.5 V, V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	A to B	V_{CC} = 5.5 V		36	46		36	46	mA
	B to A			63	77		63	77	
I_{CCL}	A to B	V_{CC} = 5.5 V		48	60		48	60	mA
	B to A			95	115		95	115	
I_{CCZ}		V_{CC} = 5.5 V		12	16		12	16	mA
C_{in}	$\overline{G}$ and DIR	V_{CC} = 5.5 V, V_I = 2.5 V or 0.5 V		8			8		pF
C_{io}	A port	V_{CC} = 5.5 V, V_I = 2.5 V or 0.5 V		18			18		pF
	B port			8			8		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
¶ Testing for this parameter on the A port is not recommended.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT25245			'54BCT25245		'74BCT25245		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.2	3.3	5.1	1.2	5.8	1.2	5.7	ns
t_{PHL}			1.9	4.3	6.7	1.9	7.6	1.9	7.2	
t_{PLH}	B	A	1.2	3.3	4.8	1.2	5.7	1.2	5.5	ns
t_{PHL}			2.1	4	5.6	2.1	6.4	2.1	6.2	
t_{PZH}	$\overline{G}$	A	3.7	6.3	8.4	3.7	10.1	3.7	9.6	ns
t_{PZL}			4.5	7.4	9.2	4.5	11.1	4.5	10.3	
t_{PHZ}	$\overline{G}$	A	1.8	3.7	5.5	1.8	6.4	1.8	6.2	ns
t_{PLZ}			3.3	5.1	7.2	3.3	9.6	3.3	8.3	
t_{PZH}	$\overline{G}$	B	3.4	5.7	7.9	3.4	9.2	3.4	8.9	ns
t_{PZL}			4.3	6.6	8.7	4.3	10.1	4.3	9.7	
t_{PHZ}	$\overline{G}$	B	2.7	4.5	6.3	2.7	7.2	2.7	6.9	ns
t_{PLZ}			1.7	4.5	6.8	1.7	8.3	1.7	7.5	

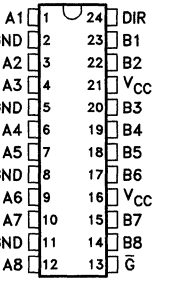
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54BCT25641, SN74BCT25641
25 Ω OCTAL BUS TRANSCEIVERS

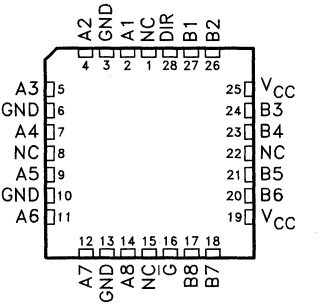
TI0283—D3601, JULY 1990

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater**
- **The A Port Features Open-Collector Outputs That Provide High I_{OL} to Allow for Heavy DC Loading on Open-Collector Outputs**
- **Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs**
- **Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)**
- **Local Bus-Latch Capability**
- **True Logic**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300 mil DIPs**

SN54BCT25641 ... JT PACKAGE
SN74BCT25641 ... DW OR NT PACKAGE
(TOP VIEW)



SN54BCT25641 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These noninverting 25-Ω octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input $\overline{G}$ can be used to disable the device so the buses are effectively isolated.

The A-port outputs of these transceivers are capable of sinking a large I_{OL}, which facilitates switching on the incident wave. They are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers. The distributed V_{CC} and GND pins minimize the noise generated by the simultaneous switching of the outputs.

The SN54BCT25641 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT25641 is characterized for operation from 0°C to 70°C.

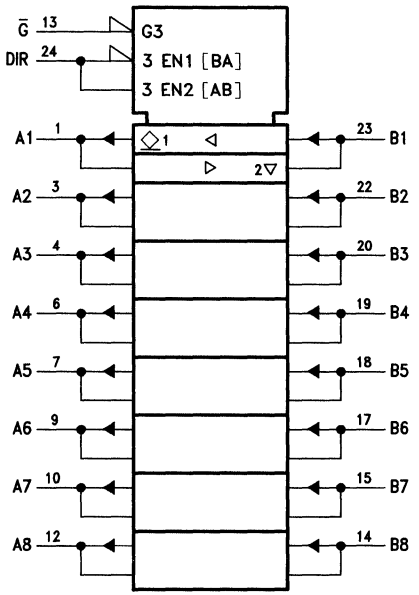
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TI0283—D3601, JULY 1990

FUNCTION TABLE

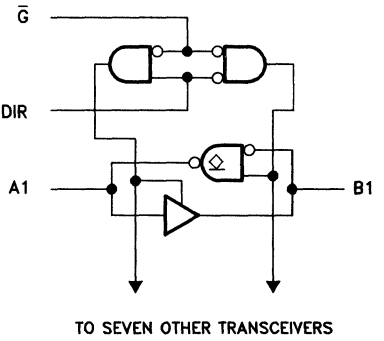
ENABLE INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B DATA TO A BUS
L	H	A DATA TO B BUS
H	X	ISOLATION

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91–1984 and IEC Publication 617–12.
Pin Numbers shown are for DW, JT, and NT packages.

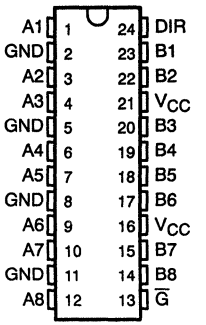
logic diagram (positive logic)



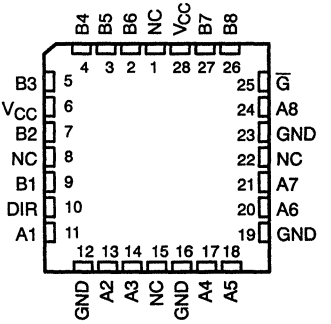
SCBS047—TI0221—D3395, DECEMBER 1989—REVISED JUNE 1990

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 25 Ω or Greater**
- **The A Port Features Open-Collector Outputs Which Provide 188 mA I_{OL} to Allow for Heavy DC Loading on Open-Collector Outputs**
- **Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs**
- **Eliminates Need for 3-State Overlap Protection on A Ports**
- **Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)**
- **ESD Protection Exceeds 2000 V per Mil-Standard-883C Method 3015**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT25642 ... JT PACKAGE
SN74BCT25642 ... DW OR NT PACKAGE
(TOP VIEW)



SN54BCT25642 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These 25 Ω octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input $\overline{G}$ can be used to disable the device so the buses are effectively isolated.

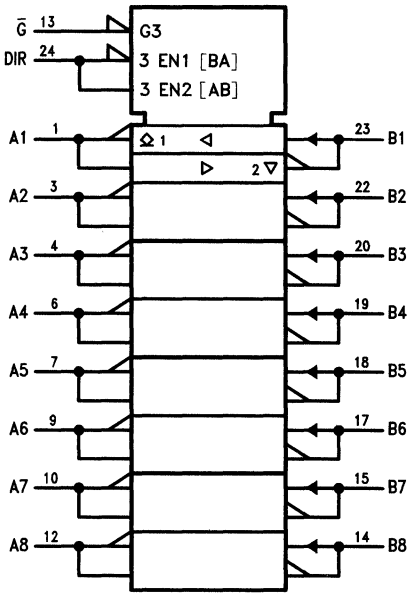
These transceivers are capable of sinking 188 mA of I_{OL} current (A port), which facilitates switching 25 Ω transmission lines on the incident wave. They are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers. The distributed V_{CC} and GND pins minimize the noise generated by the simultaneous switching of the outputs.

FUNCTION TABLE

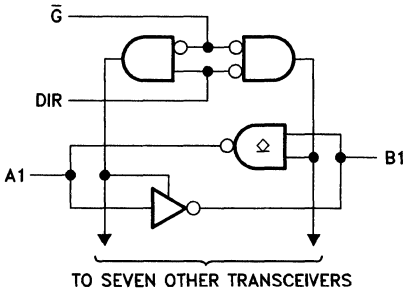
ENABLE INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	$\overline{B}$ Data to A Bus
L	H	$\overline{A}$ Data to B Bus
H	X	Isolation

The SN54BCT25642 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT25642 is characterized for operation from 0°C to 70°C.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range: Control Inputs (See Note 1)		−0.5 V to 7 V
I/O ports (See Note 1)		−0.5 V to 5.5 V
Voltage applied to any output in the disabled or power-off state		−0.5 V to 5.5 V
Voltage applied to any output in the high state		−0.5 V to V_{CC}
Input clamp current		−30 mA
Current into any output in the low state:	SN54BCT25642 (A ports)	250 mA
	(B ports)	40 mA
	SN74BCT25642 (A ports)	376 mA
	(B ports)	48 mA
Operating free-air temperature range:	SN54BCT25642	−55°C to 125°C
	SN74BCT25642	0°C to 70°C
Storage temperature range		−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			SN54BCT25642			SN74BCT25642			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage (A1–A8)				5.5			5.5	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current (B1–B8)				−3			−3	mA
I_{OL}	Low-level output current	A1–A8			125			188	mA
		B1–B8			20			24	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT25642			SN74BCT25642			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	Any B	V_{CC} = 4.75 V, I_{OH} = −3 mA				2.7			V
		V_{CC} = 4.5 V, I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
V_{OL}	Any A	V_{CC} = 4.5 V, I_{OL} = 94 mA		0.38	0.55		0.42	0.55	V
		V_{CC} = 4.5 V, I_{OL} = 125 mA			0.8				
		V_{CC} = 4.5 V, I_{OL} = 188 mA						0.7	
	Any B	V_{CC} = 4.5 V, I_{OL} = 20 mA		0.3	0.5				V
		V_{CC} = 4.5 V, I_{OL} = 24 mA					0.35	0.5	
I_{OH}	Any A	V_{CC} = 4.5 V, V_{OH} = 5.5 V			0.1			0.1	mA
I_I	A and B	V_{CC} = 5.5 V, V_I = 5.5 V			0.25			0.25	mA
	DIR and $\overline{G}$	V_{CC} = 5.5 V, V_I = 5.5 V			0.1			0.1	
I_{IH}‡	A and B	V_{CC} = 5.5 V, V_I = 2.7 V			70			70	μA
	DIR and $\overline{G}$	V_{CC} = 5.5 V, V_I = 2.7 V			20			20	
I_{IL}‡	A anb B	V_{CC} = 5.5 V, V_I = 0.5 V			−0.6			−0.6	mA
	DIR and $\overline{G}$	V_{CC} = 5.5 V, V_I = 0.5 V			−0.6			−0.6	
I_{OS}§	Any B	V_{CC} = 5.5 V, V_O = 0	−60		−150	−60		−150	mA
I_{CCL}	A to B	V_{CC} = 5.5 V		40	64		40	64	mA
I_{CCH}	A to B	V_{CC} = 5.5 V		25	40		25	40	mA
I_{CCZ}	A to B	V_{CC} = 5.5 V		7.6	13		7.6	13	mA
I_{CCL}	B to A	V_{CC} = 5.5 V		78	125		78	125	mA
I_{CCH}	B to A	V_{CC} = 5.5 V		34	55		34	55	mA
C_{io}	A Ports	V_{CC} = 5.5 V, V_I = 2.5 V or 0.5 V		15			15		pF
	B Ports			8			8		
C_i	Control inputs	V_{CC} = 5.5 V, V_I = 2.5 V or 0.5 V		8			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed 10 ms.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω‡, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω‡, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT25642			'54BCT25642		'74BCT25642		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	0.8	3.2	6	0.8	6.5	0.8	6.2	ns
t_{PHL}			0.5	2	3.9	0.5	4.1	0.5	4	
t_{PLH}	B	A	1.5	3.2	4.7	1.5	7.4	1.5	6.3	ns
t_{PHL}			1.7	4.5	4.8	1.7	6.7	1.7	5.9	
t_{PLH}	$\overline{G}$	A	2.8	5.5	10.4	2.8	12.9	2.8	11.6	ns
t_{PHL}			4.6	8.6	11.3	5.4	11.8	4.6	11.3	
t_{PZH}	$\overline{G}$	B	3.3	5.7	8.1	3.3	9.7	3.3	9.1	ns
t_{PZL}			3.8	6.6	8.8	3.8	10.2	3.8	9.8	
t_{PHZ}	$\overline{G}$	B	1.8	4.6	7	1.8	8	1.8	7.3	ns
t_{PLZ}			1.4	4.3	6.7	1.4	8.4	1.4	7.3	

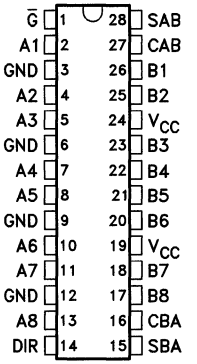
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ For port A, R1 = 100 Ω.

SN54BCT25646, SN74BCT25646
OCTAL 25-OHM REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0230—D3534, JUNE 1990

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **Package Options Include Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT25646 ... JT PACKAGE
SN74BCT25646 ... NT PACKAGE
(TOP VIEW)



description

The 'BCT25646 is an octal noninverting registered bus transceiver. The A-port outputs are designed to source up to 80 mA and to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω. The B-port outputs are designed to source 3 mA and to sink 24 mA.

When the output-enable input $\overline{G}$ is low, the device transmits data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control (DIR) input. The 'BCT25646 can transmit either real-time or previously stored data. In the A-to-B mode, a low-to-high transition on the clock input (CAB) stores the data present at the A bus. When the select input (SAB) is high, the data stored on the previous low-to-high transition of CAB appears on the B bus. When SAB is low, the current A-bus data appears on the B bus. Data flow from the B bus to the A bus uses the CBA and SBA inputs.

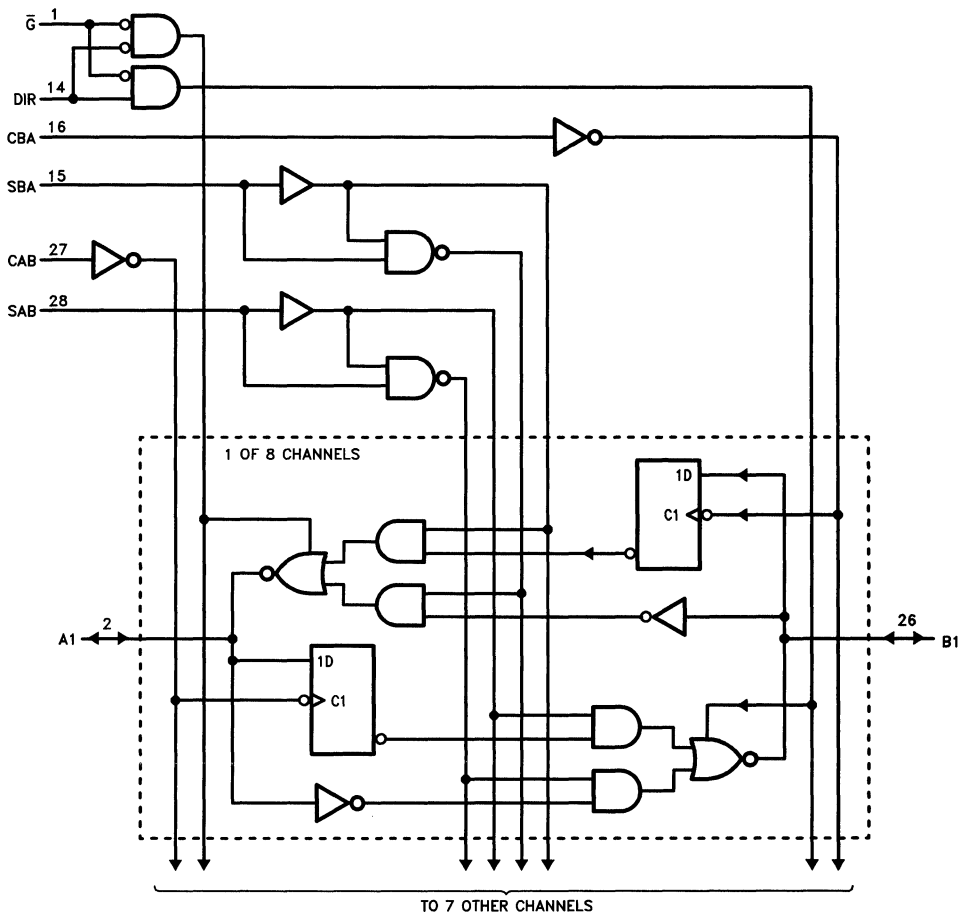
The distributed V_{CC} and GND pins of the 'BCT25646 reduce switching noise for more reliable system operation.

The SN54BCT25646 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT25646 is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PRODUCT PREVIEW

logic diagram (positive logic)

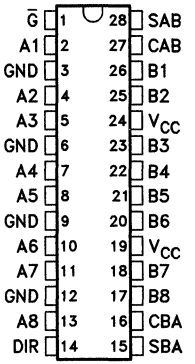


SN54BCT25648, SN74BCT25648
OCTAL 25-OHM REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0231—D3535, JUNE 1990

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **Package Options Include Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT25648 ... JT PACKAGE
SN74BCT25648 ... NT PACKAGE
(TOP VIEW)



description

The 'BCT25648 is an octal inverting registered bus transceiver. The A-port outputs are designed to source up to 80 mA and to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω. The B-port outputs are designed to source 3 mA and to sink 24 mA.

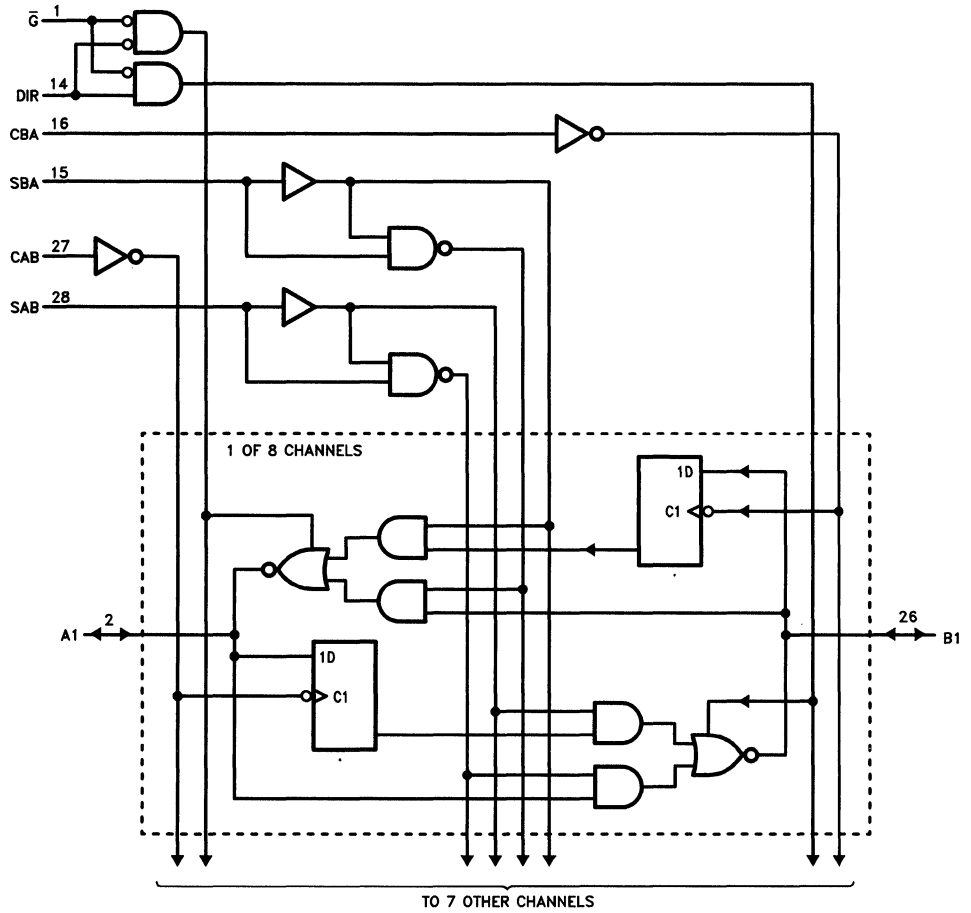
When the output-enable input $\overline{G}$ is low, the device transmits data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control (DIR) input. The 'BCT25648 can transmit either real-time or previously stored data. In the A-to-B mode, a low-to-high transition on the clock input (CAB) stores the data present at the A bus. When the select input (SAB) is high, the inverse of the data stored on the previous low-to-high transition of CAB appears on the B bus. When SAB is low, the inverse of the current A bus data appears on the B bus. Data flow from the B bus to the A bus uses the CBA and SBA inputs.

The distributed V_{CC} and GND pins of the 'BCT25648 reduce switching noise for more reliable system operation.

The SN54BCT25648 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT25648 is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic diagram (positive logic)

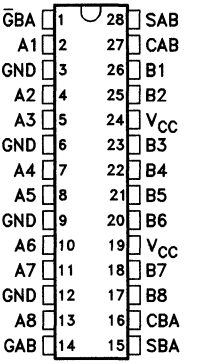


SN54BCT25651, SN74BCT25651
OCTAL 25-OHM REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0232—D3536, JUNE 1990

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **Package Options Include Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT25651 ... JT PACKAGE
SN74BCT25651 ... NT PACKAGE
(TOP VIEW)



description

The 'BCT25651 is an octal inverting registered bus transceiver. The A-port outputs are designed to source up to 80 mA and to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω. The B-port outputs are designed to source 3 mA and to sink 24 mA.

The A and B ports have separate output-enable inputs. When the A-to-B enable (GAB) is high, the B-bus outputs are active (high or low logic levels); when GAB is low, the B-bus outputs are in the high-impedance state. $\overline{G}$BA controls the A-bus outputs: when $\overline{G}$BA is low, the A-bus outputs are active (high or low logic levels); when $\overline{G}$BA is high, the A-bus outputs are in the high-impedance state.

The 'BCT25651 can transmit either real-time or previously stored data. In the A-to-B mode, a low-to-high transition on the clock input (CAB) stores the data present at the A bus. When the select input (SAB) is high, the inverse of the data stored on the previous low-to-high transition of CAB appears on the B bus. When SAB is low, the inverse of the current A-bus data appears on the B bus. Data flow from the B bus to the A bus uses the CBA and SBA inputs.

The distributed V_{CC} and GND pins of the 'BCT25651 reduce switching noise for more reliable system operation.

The SN54BCT25651 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT25651 is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
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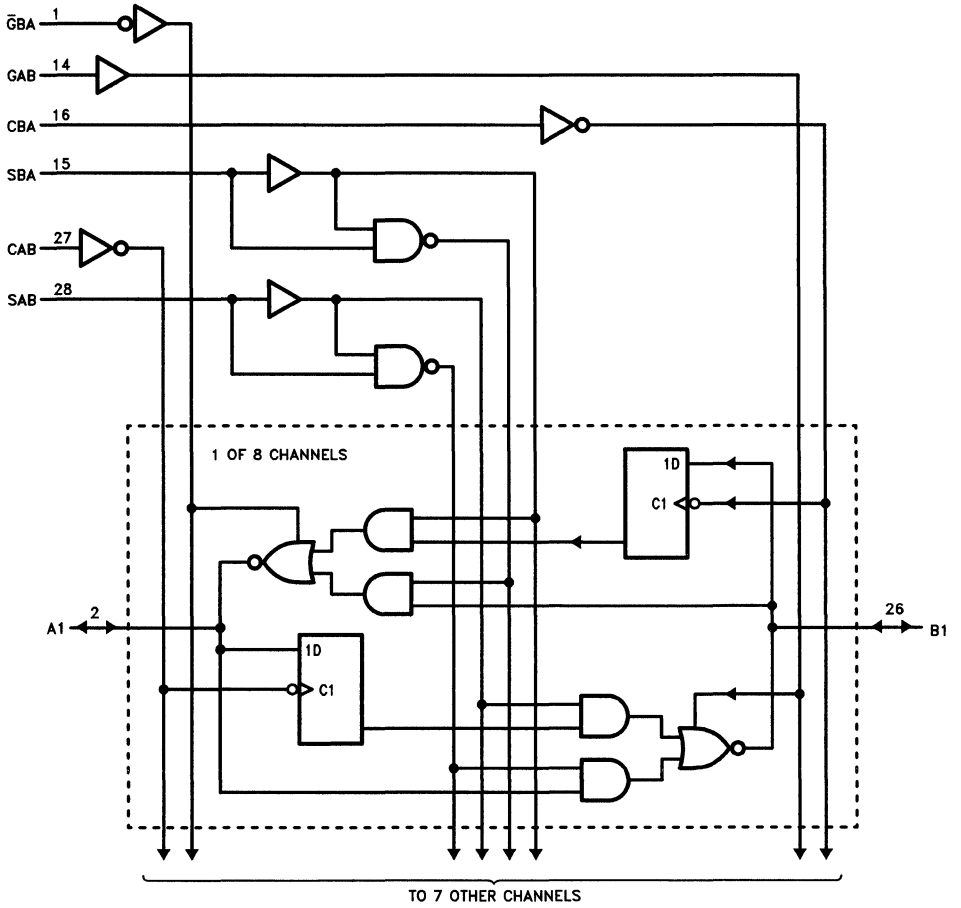
logic diagram (positive logic)

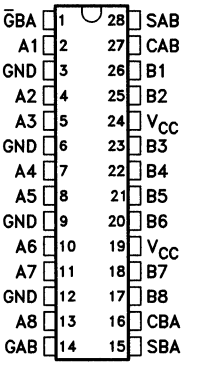


SN54BCT25652, SN74BCT25652
OCTAL 25-OHM REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0233—D3537, JUNE 1990

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **Package Options Include Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT25652 ... JT PACKAGE
SN74BCT25652 ... NT PACKAGE



description

The 'BCT25652 is an octal noninverting registered bus transceiver. The A-port outputs are designed to source up to 80 mA and to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω. The B-port outputs are designed to source 3 mA and to sink 24 mA.

The A and B ports have separate output-enable inputs. When the A-to-B enable (GAB) is high, the B-bus outputs are active (high or low logic levels); when GAB is low, the B-bus outputs are in the high-impedance state. $\overline{G}$BA controls the A-bus outputs: when $\overline{G}$BA is low, the A-bus outputs are active (high or low logic levels); when $\overline{G}$BA is high, the A-bus outputs are in the high-impedance state.

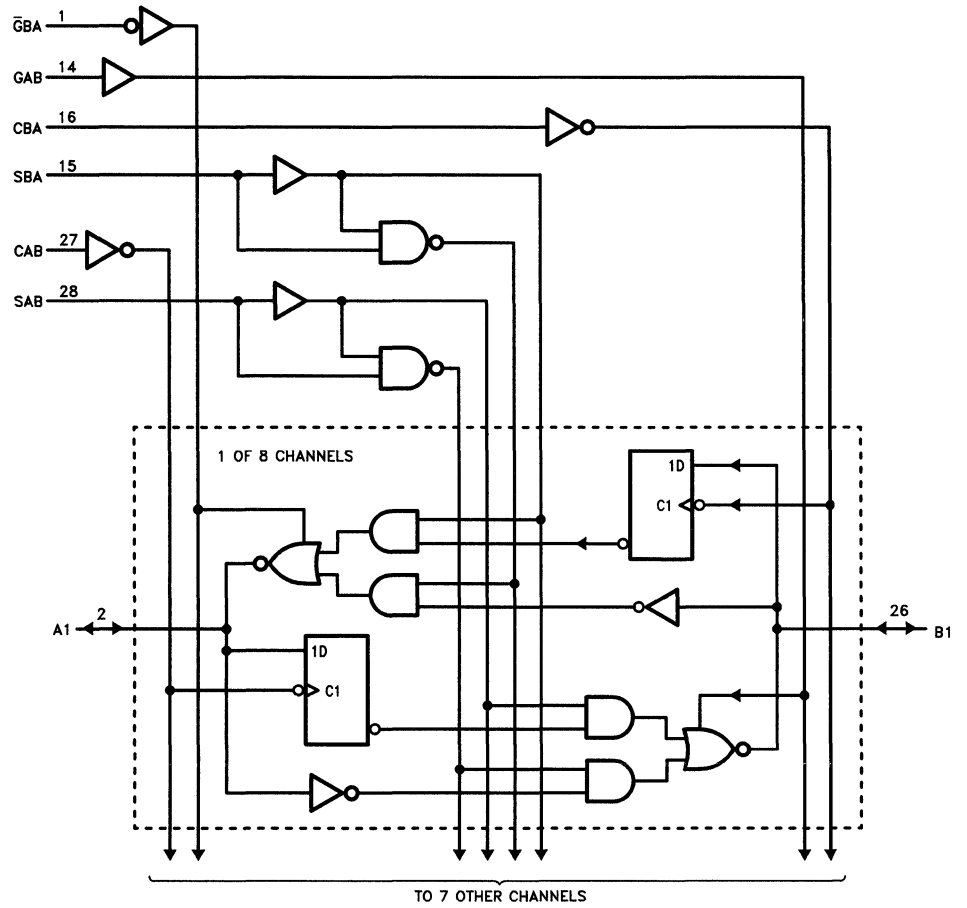
The 'BCT25652 can transmit either real-time or previously stored data. In the A-to-B mode, a low-to-high transition on the clock input (CAB) stores the data present at the A bus. When the select input (SAB) is high, the data stored on the previous low-to-high transition of CAB appears on the B bus. When SAB is low, the current A-bus data appears on the B bus. Data flow from the B bus to the A bus uses the CBA and SBA inputs.

The distributed V_{CC} and GND pins of the 'BCT25652 reduce switching noise for more reliable system operation.

The SN54BCT25652 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT25652 is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic diagram (positive logic)

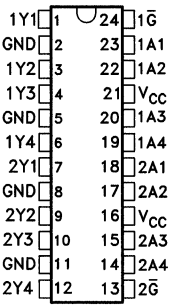


SN54BCT25756, SN74BCT25756
OCTAL 25-OHM LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

TI0242—D3562, JUNE 1990

- **Open-Collector Version of 'BCT25240**
- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater**
- **Data Flow-Through Pinout (All Inputs Are on Opposite Side from Outputs)**
- **Distributed V_{CC} and GND Pins Reduce Switching Noise for More Reliable System Operation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT25756 ... JT PACKAGE
SN74BCT25756 ... NT PACKAGE
(TOP VIEW)



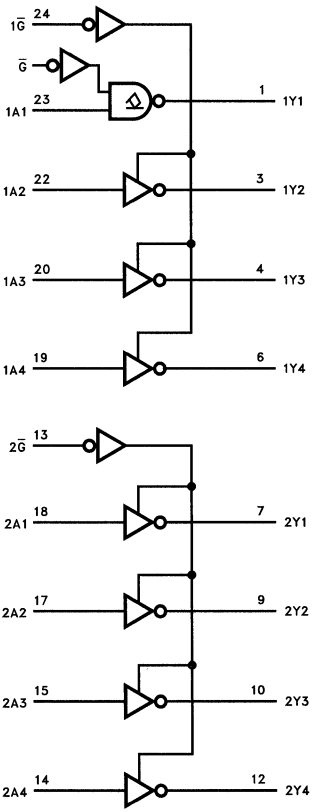
description

The 'BCT25756 is an open-collector version of the SN54BCT25240 and SN74BCT25240. Its outputs are designed to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω.

When the output-enable input $1\overline{G}$ (or $2\overline{G}$) is low, the device transmits the inverse of the appropriate A-input data to the corresponding Y outputs. Setting $1\overline{G}$ (or $2\overline{G}$) high turns the corresponding outputs off.

The SN54BCT25756 is characterized over the full military temperature range of −55°C to 125°C. The SN74BCT25756 is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)

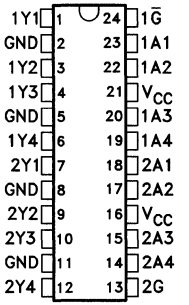


TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PRODUCT PREVIEW

- **25-Ω Open-Collector Version of 'BCT2241**
- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater**
- **Data Flow-Through Pinout (All Inputs Are on Opposite Side from Outputs)**
- **Distributed V_{CC} and GND Pins Reduce Switching Noise for More Reliable System Operation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT25757 ... JT PACKAGE
SN74BCT25757 ... NT PACKAGE
(TOP VIEW)



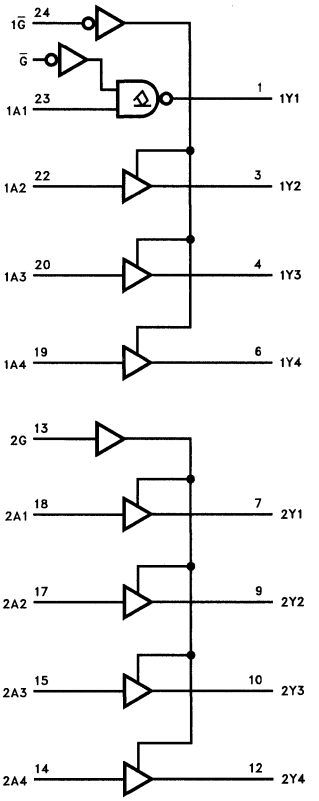
description

The 'BCT25757 is a 25-Ω open-collector version of the SN54BCT2241 and SN74BCT2241. Its outputs are designed to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω.

The 'BCT25757 has complementary output-enable inputs. When output-enable input $1\overline{G}$ is low, the device transmits the 1A-input data to the 1Y outputs; setting $1\overline{G}$ high turns the 1Y outputs off. Output enable 2G affects the 2Y outputs similarly, but is active-high.

The SN54BCT25757 is characterized over the full military temperature range of −55°C to 125°C. The SN74BCT25757 is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)

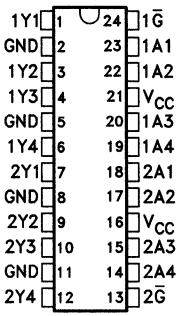


SN54BCT25760, SN74BCT25760
OCTAL 25-OHM LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

TI0241—D3564, JUNE 1990

- **Open-Collector Version of 'BCT25244**
- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater**
- **Data Flow-Through Pinout (All Inputs Are on Opposite Side from Outputs)**
- **Distributed V_{CC} and GND Pins Reduce Switching Noise for More Reliable System Operation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT25760 ... JT PACKAGE
SN74BCT25760 ... NT PACKAGE
(TOP VIEW)



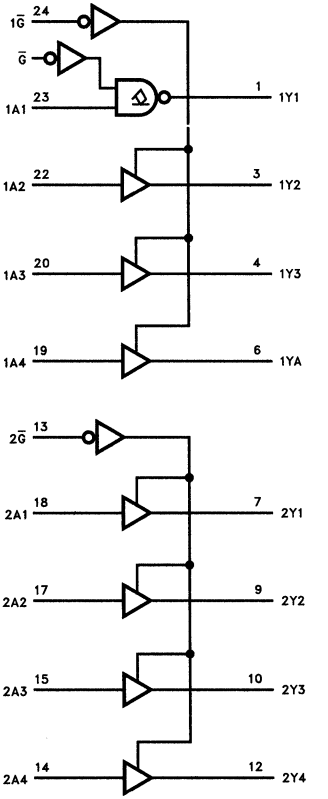
description

The 'BCT25760 is an open-collector version of the SN54BCT25244 and SN74BCT25244. Its outputs are designed to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω.

When the output-enable input $1\overline{G}$ (or $2\overline{G}$) is low, the device transmits the appropriate A-input data to the corresponding Y outputs. Setting $1\overline{G}$ (or $2\overline{G}$) high turns the corresponding outputs off.

The SN54BCT25760 is characterized over the full military temperature range of −55°C to 125°C. The SN74BCT25760 is characterized for operation from 0°C to 70°C.

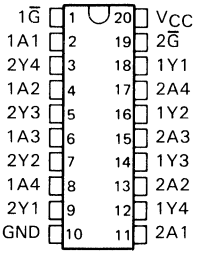
logic diagram (positive logic)



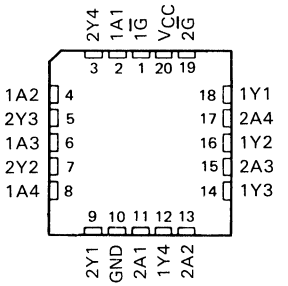
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **Buffers/Line Drivers for Driving MOS Devices**
- **I/O Ports Have 25-Ω Series Resistors, So No External Resistors Are Required**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS2240 . . . J PACKAGE
SN74ALS2240 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS2240 . . . FK PACKAGE
(TOP VIEW)

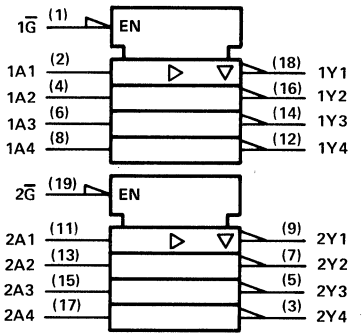


description

These octal buffers and line drivers are designed to drive the capacitive inputs of MOS devices and to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices feature high fan-out and improved fan-in.

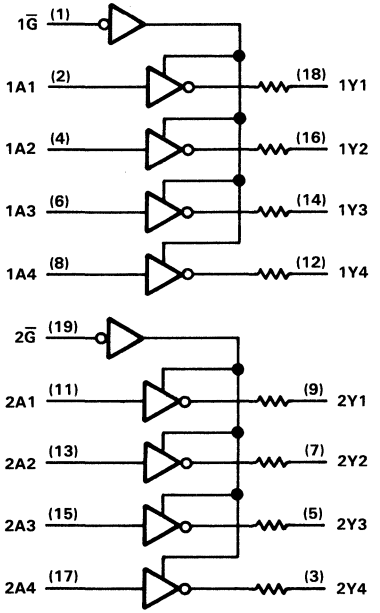
The SN54ALS2240 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS2240 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS2240 . . . . . −55°C to 125°C
SN74ALS2240 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS2240			SN74ALS2240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS2240			SN74ALS2240			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5		0.15	0.5	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8		0.35	0.8	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{OH}	V_{CC} = 4.5 V,	V_O = 2 V	−15			−15			mA
I_{OL}	V_{CC} = 4.5 V,	V_O = 2 V	15			15			mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		6	11		6	11	mA
		Outputs low		13	23		13	23	
		Outputs disabled		12	20		12	20	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS2240	SN54ALS2240		SN74ALS2240		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	6	2	14	2	10	ns
t_{PHL}			6	2	14	2	10	
t_{PZH}	$\overline{G}$	Y	10	5	20	5	17	ns
t_{PZL}			12	7	25	7	20	
t_{PHZ}	$\overline{G}$	Y	7	2	12	2	10	ns
t_{PLZ}			9	4	20	4	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

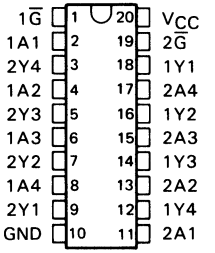
- **Buffers/Line Drivers for Driving MOS Devices**
- **P-N-P Inputs Reduce DC Loading**
- **Output Ports Have 25-Ω Series Resistors, So No External Resistors Are Required**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

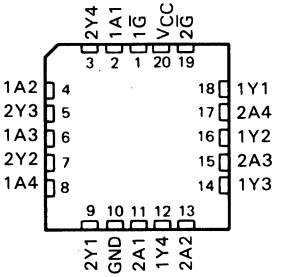
These octal buffers and line drivers are designed to drive the capacitive inputs of MOS devices and to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices feature high fan-out and improved fan-in.

The SN54ALS2244 is characaterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS2244 is characterized for operation from 0°C to 70°C.

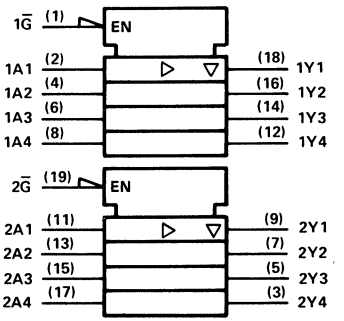
SN54ALS2244 . . . J PACKAGE
SN74ALS2244 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS2244 . . . FK PACKAGE
(TOP VIEW)

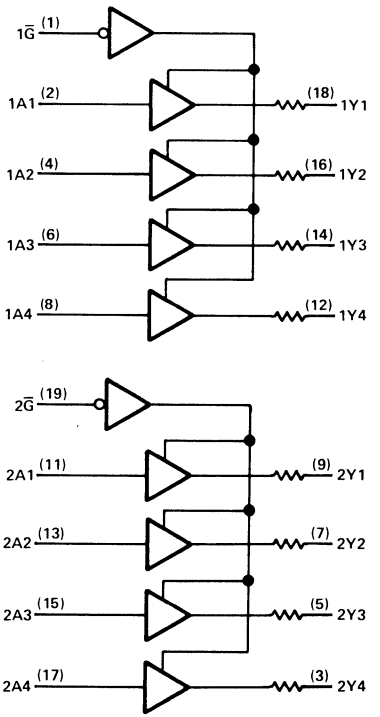


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to any output in the disabled or power-off state . . . . . 5.5 V
Operating free-air temperature ranges: SN54ALS2244 . . . . . −55°C to 125°C
SN74ALS2244 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS2244			SN74ALS2244			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS2244			SN74ALS2244			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 1 mA		0.15	0.5		0.15	0.5	V
		I_{OL} = 12 mA		0.45	0.8		0.45	0.8	
I_{OH}	V_{CC} = 4.5 V,	V_O = 2 V	−15			−15			mA
I_{OL}	V_{CC} = 4.5 V,	V_O = 2 V	15			15			mA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		11	17		11	17	mA
I_{CCL}				14	22		14	22	
I_{CCZ}				15	23		15	23	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}

switching characteristics (see Note 1)

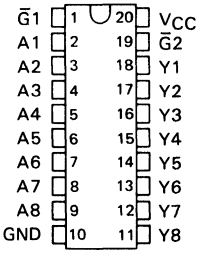
PARAMETER	FROM (INTPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS2244		SN74ALS2244		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	17	3	16	ns
t_{PHL}			3	19	3	17	
t_{PZH}	$\overline{G}$	Y	1	18	1	17	ns
t_{PZL}			1	15	1	14	
t_{PHZ}	$\overline{G}$	Y	1	9	1	9	ns
t_{PLZ}			1	9	1	9	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

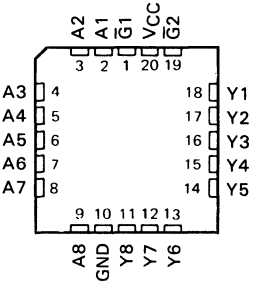
JUNE 1984—REVISED MAY 1986

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Outputs Have 25-Ω Series Resistor, So No External Resistors are Required**
- **Package Options Include Plastic "Small Outline" Packages, Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS2540, SN54ALS2541 . . . J PACKAGE
SN74ALS2540, SN74ALS2541 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS2540, SN54ALS2541 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed to drive capacitive input characteristics of MOS devices and have the performance of the popular SN54ALS240A/SN74ALS240A series. At the same time, they offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed-circuit-board layout.

The three-state control gate is a 2-input AND with active-low inputs such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

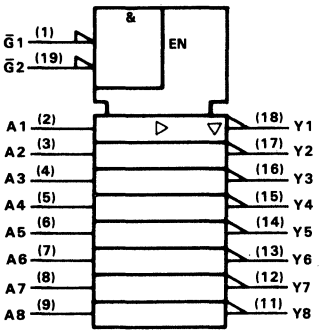
The 'ALS2540 offers inverting data and the 'ALS2541 offers true data at the outputs.

The SN54ALS' is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' is characterized for operation from 0°C to 70°C.

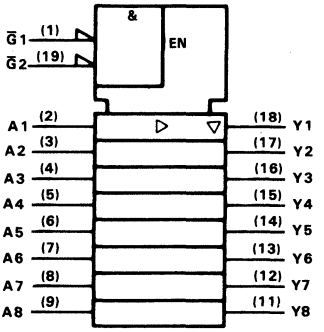
JUNE 1984—REVISED MAY 1986

logic symbols†

ALS2540



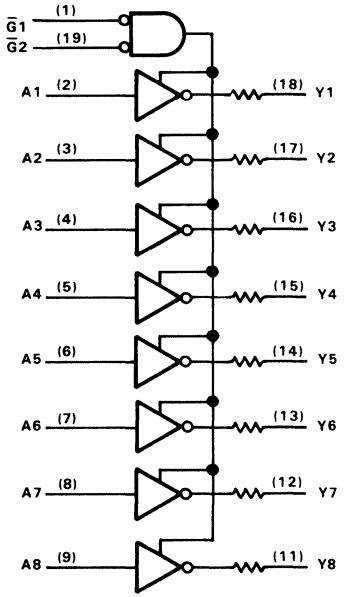
'ALS2541



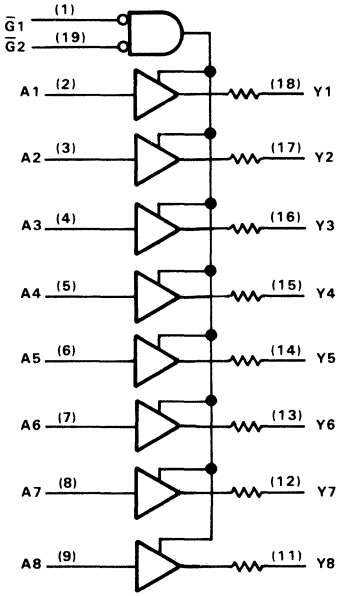
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'ALS2540



'ALS2541



All output resistors are 25 Ω.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS2540, SN54ALS2541 . . . . . −55°C to 125°C
SN74ALS2540, SN74ALS2541 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS2540 SN54ALS2541			SN74ALS2540 SN74ALS2541			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			12			12	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS2540 SN54ALS2541			SN74ALS2540 SN74ALS2541			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5		0.15	0.5	V
		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8		0.35	0.8	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_{OH}		V_{CC} = 4.5 V,	V_O = 2 V	−15			−15			mA
I_{OL}		V_{CC} = 4.5 V,	V_O = 2 V	30			30			mA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	'ALS2540	V_{CC} = 5.5 V	Outputs high		5	10		5	10	mA
			Outputs low		13	22		13	22	
			Outputs disabled		11	19		11	19	
	'ALS2541	V_{CC} = 5.5 V	Outputs high		6	14		6	14	mA
			Outputs low		15	25		15	25	
			Outputs disabled		13.5	22		13.5	22	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS2540 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS2540	SN54ALS2540		SN74ALS2540		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	7.5	2	14	2	12	ns
t_{PHL}			5.6	2	13	2	11	
t_{PZH}	$\overline{G}$	Y	9	5	18	5	15	ns
t_{PZL}			12.6	8	24	8	20	
t_{PHZ}	$\overline{G}$	Y	4	1	12	1	10	ns
t_{PLZ}			7	2	14	2	12	

'ALS2541 switching characteristics (see Note 1)

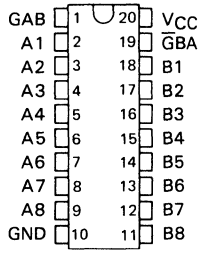
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS2541	SN54ALS2541		SN74ALS2541		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	8.7	2	17	2	15	ns
t_{PHL}			7	2	14	2	12	
t_{PZH}	$\overline{G}$	Y	9	5	18	5	15	ns
t_{PZL}			12.6	8	24	8	20	
t_{PHZ}	$\overline{G}$	Y	4	1	12	1	10	ns
t_{PLZ}			7	2	14	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

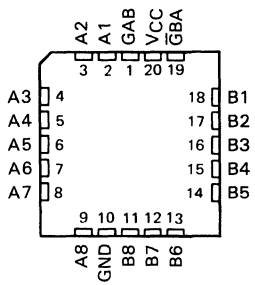
DECEMBER 1983—REVISED MAY 1986

- **Octal Bus Transceivers for Driving MOS Devices**
- **I/O Ports Have 25-Ω Series Resistors, So No External Resistors Are Required**
- **Local Bus-Latch Capability**
- **Choice of True or Inverting Logic**
- **Package Options Include Plastic "Small Outline" Packages, Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS' . . . J PACKAGE
SN74AS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54AS' . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'AS2620 or 'AS2623 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'AS2623 or complementary for the 'AS2620.

The SN54AS2620 and SN54AS2623 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74AS2620 and SN74AS2623 are characterized for operation from 0 °C to 70 °C.

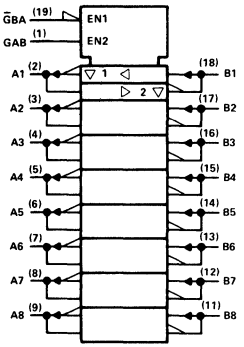
FUNCTION TABLE

ENABLE INPUTS		OPERATION	
$\overline{G}$BA	GAB	'AS2620	'AS2623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

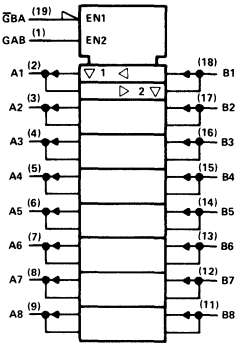
DECEMBER 1983—REVISED MAY 1986

logic symbols†

'AS2620



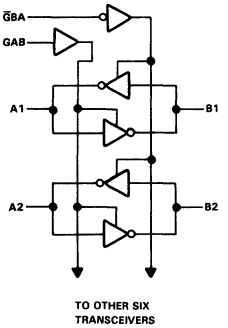
'AS2623



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'AS2620



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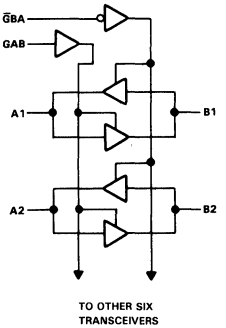


absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS2620, SN54AS2623 . . . . . −55 °C to 125 °C
SN74AS2620, SN74AS2623 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS2620 SN54AS2623			SN74AS2620 SN74AS2623			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS2620 SN54AS2623			SN74AS2620 SN74AS2623			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.4		0.15	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.7		0.35	0.7	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{OH}		V_{CC} = 4.5 V,	V_O = 2 V	−35			−35			mA
I_{OL}		V_{CC} = 4.5 V,	V_O = 2 V	35			35			mA
I_{CC}	'AS2620	V_{CC} = 5.5 V	Outputs high		62	100		62	100	mA
			Outputs low		74	121		74	121	
			Outputs disabled		48	77		48	77	
	'AS2623	V_{CC} = 5.5 V	Outputs high		57	93		57	93	
			Outputs low		116	189		116	189	
			Outputs disabled		72	116		72	116	

†All typical values are at V_{CC} = 5 V, T_A = 25 °C
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS2620 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS2620		SN74AS2620		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	9.5	1	8	ns
t_{PHL}			1	7.5	1	6.5	
t_{PLH}	B	A	1	9.5	1	8	ns
t_{PHL}			1	7.5	1	6.5	
t_{PZH}	$\overline{G}$BA	A	1	11	1	10	ns
t_{PZL}			1	12	1	11	
t_{PHZ}	$\overline{G}$BA	A	1	7.5	1	6	ns
t_{PLZ}			1	15	1	12	
t_{PZH}	GAB	B	1	9	1	8	ns
t_{PZL}			1	9	1	8	
t_{PHZ}	GAB	B	1	12	1	11	ns
t_{PLZ}			1	12	1	11	

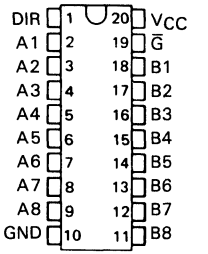
'AS2623 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS2623		SN74AS2623		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	9.5	1	8.5	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	B	A	1	10	1	9	ns
t_{PHL}			1	9	1	7.5	
t_{PZH}	$\overline{G}$BA	A	1	12.5	1	11	ns
t_{PZL}			1	12	1	11	
t_{PHZ}	$\overline{G}$BA	A	1	8.5	1	7.5	ns
t_{PLZ}			1	13	1	12	
t_{PZH}	GAB	B	1	13	1	12	ns
t_{PZL}			1	13.5	1	12	
t_{PHZ}	GAB	B	1	7.5	1	7	ns
t_{PLZ}			1	14.5	1	12.5	

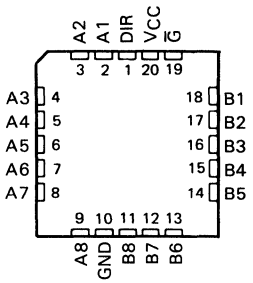
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Octal Bus Transceivers for Driving MOS Devices**
- **I/O Ports Have 25-Ω Series Resistors, So No External Resistors Are Required**
- **Choice of True or Inverting Logic**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS' . . . J PACKAGE
SN74AS' . . . DW or N PACKAGE
(TOP VIEW)



SN54AS' . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

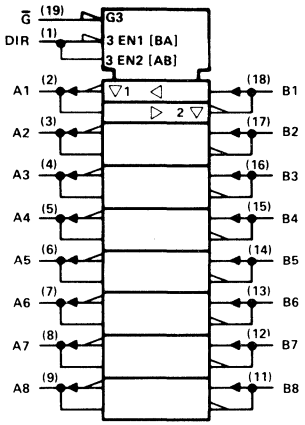
The SN54AS' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

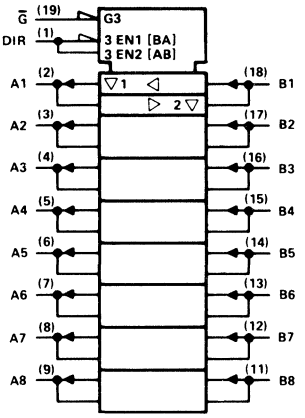
CONTROL INPUTS		OPERATION	
$\overline{G}$	DIR	'AS2640	'AS2645
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

logic symbols†

'AS2640



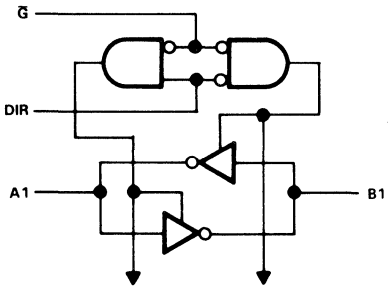
'AS2645



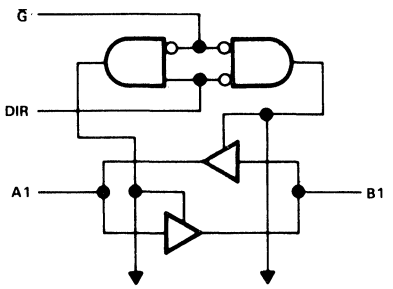
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagrams (positive logic)

'AS2640



'AS2645



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS2640, SN54AS2645 . . . . . −55°C to 125°C
SN74AS2640, SN74AS2645 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS2640 SN54AS2645			SN74AS2640 SN74AS2645			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-lvel input voltage			0.8			0.8	V
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS'			SN74AS'			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.4		0.15	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.7		0.35	0.7	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{OH}		V_{CC} = 4.5 V,	V_O = 2 V	−35			−35			mA
I_{OL}		V_{CC} = 4.5 V,	V_{OL} = 2 V	35			35			mA
I_{CC}	'AS2640	V_{CC} = 5.5 V	Outputs high		37	58		37	58	mA
			Outputs low		78	123		78	123	
			Outputs disabled		51	80		51	80	
	'AS2645		Outputs high		58	95		58	95	
			Outputs low		95	155		95	155	
			Outputs disabled		73	119		73	119	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parametes I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS2640 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS2640		SN74AS2640		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	9.5	1	7.5	ns
t_{PHL}			1	7	1	6.5	
t_{PZH}	$\overline{G}$	A or B	2	11	2	9	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	$\overline{G}$	A or B	1	8	1	7	ns
t_{PLZ}			2	15	2	13	

'AS2645 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS2645		SN74AS2645		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	12	1	10	ns
t_{PHL}			1	11	1	9.5	
t_{PZH}	$\overline{G}$	A or B	1	13	1	11.5	ns
t_{PZL}			1	13	1	10.5	
t_{PHZ}	$\overline{G}$	A or B	1	9	1	8	ns
t_{PLZ}			1	13	1	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

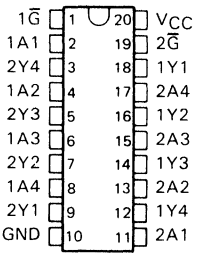
- **BiCMOS Design Substantially Reduces Standby Current**
- **Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

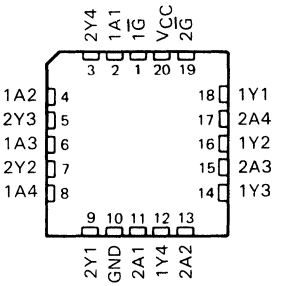
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT2241 and 'BCT2244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

The SN54BCT2240 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT2240 is characterized for operation from 0°C to 70°C.

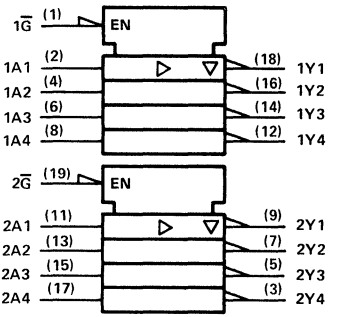
SN54BCT2240 . . . J PACKAGE
SN74BCT2240 . . . DW OR N PACKAGE
(TOP VIEW)



SN54BCT2240 . . . FK PACKAGE
(TOP VIEW)

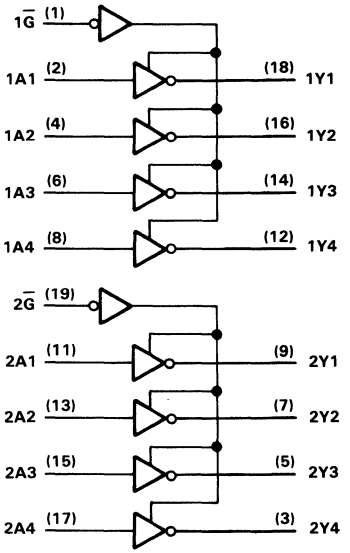


logic symbol†

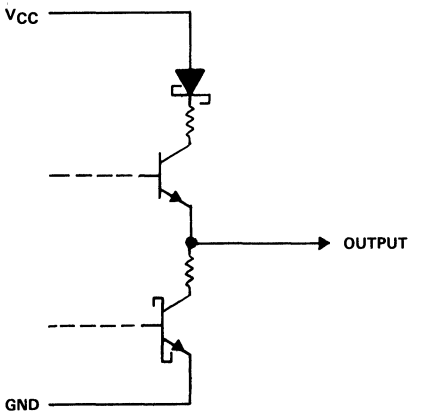


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of each output



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage (see Note 1) . . . . . −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Input clamp current . . . . . −30 mA
Current into any output in the low state . . . . . 24 mA
Operating free-air temperature range: SN54BCT2240 . . . . . −55°C to 125°C
SN74BCT2240 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT2240			SN74BCT2240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−12	mA
I_{OL}	Low-level output current			12			12	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT2240			SN74BCT2240			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_{OH} = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2		2	3.2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 1 mA		0.15	0.5		0.15	0.5	V
		I_{OL} = 12 mA		0.35	0.8		0.35	0.8	
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−1			−1	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		19	32		19	32	mA
I_{CCL}				46	76		46	76	
I_{CCZ}				6	8		6	8	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

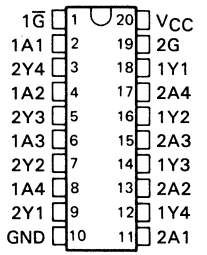
switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'BCT2240			SN54BCT2240		SN74BCT2240		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	0.5	3.4	4.8	0.5	6.3	0.5	5.7	ns
t_{PHL}			0.5	2.8	4	0.5	4.6	0.5	4.4	
t_{PZH}	$\overline{G}$	Y	2.6	6.2	8.2	2.6	10.1	2.6	9.3	ns
t_{PZL}			4.3	8.8	10.9	4.3	12.9	4.3	12.4	
t_{PHZ}	$\overline{G}$	Y	2	5.3	7.1	2	9.2	2	8.7	ns
t_{PLZ}			2.2	6.7	8.5	2.2	12.2	2.2	10.6	

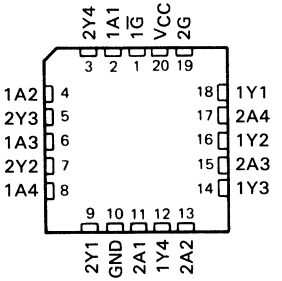
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

- **BiCMOS Design Substantially Reduces Standby Current**
- **Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54BCT2241 . . . J PACKAGE
SN74BCT2241 . . . DW OR N PACKAGE
(TOP VIEW)



SN54BCT2241 . . . FK PACKAGE
(TOP VIEW)

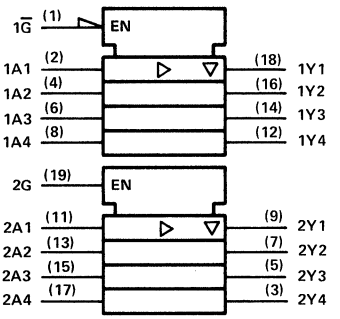


description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT2240 and 'BCT2244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

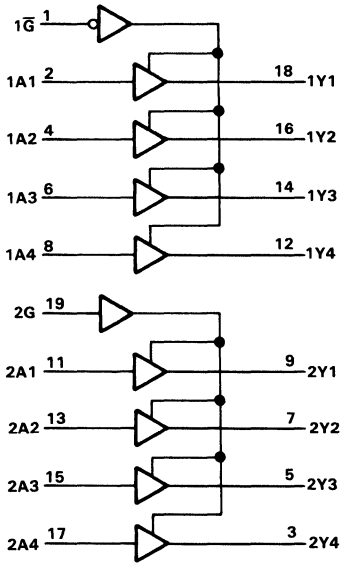
The SN54BCT2241 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT2241 is characterized for operation from 0°C to 70°C.

logic symbol†

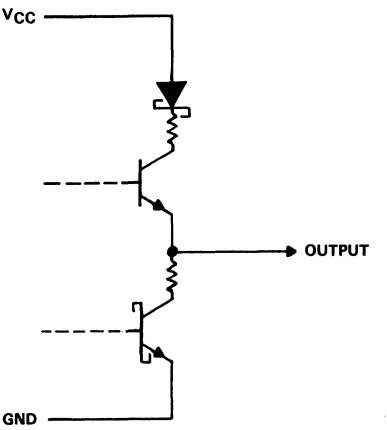


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of each output



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage (see Note 1) . . . . . −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Input clamp current . . . . . −30 mA
Current into any output in the low state . . . . . 24 mA
Operating free-air temperature range: SN54BCT2241 . . . . . −55°C to 125°C
SN74BCT2241 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT2241			SN74BCT2241			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−12	mA
I_{OL}	Low-level output current			12			12	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT2241			SN74BCT2241			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_{OH} = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2		2			
	V_{CC} = 4.75 V	I_{OH} = −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 1 mA		0.38	0.55		0.15	0.5	V
		I_{OL} = 12 mA					0.42	0.8	
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−1			−1	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		23	37		23	37	mA
I_{CCL}				48	76		48	76	
I_{CCZ}				6	9		6	9	
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		6			6		pF
C_o	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		11			11		pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX			UNIT
			'BCT2241			SN54BCT2241		SN74BCT2241	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.1	3	4.4	1.1	5.1	1.1	4.9	ns
t_{PHL}			2.9	4.9	6.6	2.9	7.2	2.9	6.9	
t_{PZH}	G or $\overline{G}$	Y	2.7	6	7.8	2.7	9.4	2.7	8.9	ns
t_{PZL}			4.1	7.7	9.4	4.1	10.9	4.1	10.3	
t_{PHZ}	G or $\overline{G}$	Y	2.5	5.2	7.2	2.5	9.7	2.5	8.7	ns
t_{PLZ}			3.2	7.1	9.5	3.2	12.9	3.2	11.3	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

- **BiCMOS Design Substantially Reduces Standby Current**
- **Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

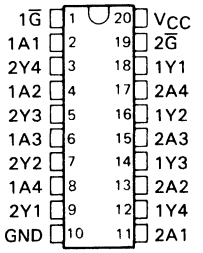
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT2240 and 'BCT2241, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low input control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

The SN54BCT2244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT2244 is characterized for operation from 0°C to 70°C.

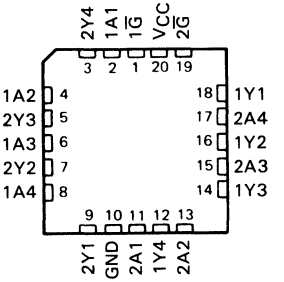
FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

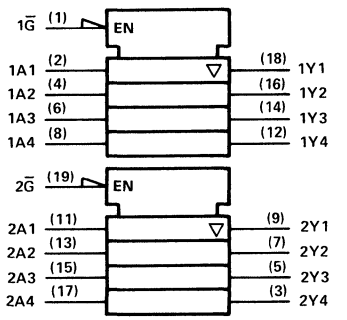
SN54BCT2244 . . . J PACKAGE
SN74BCT2244 . . . DW OR N PACKAGE
(TOP VIEW)



SN54BCT2244 . . . FK PACKAGE
(TOP VIEW)

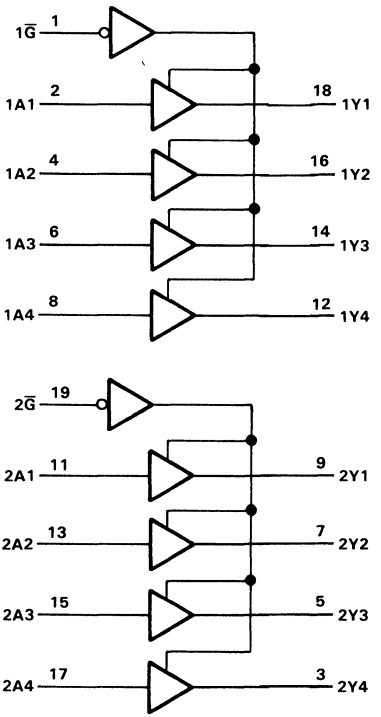


logic symbol†

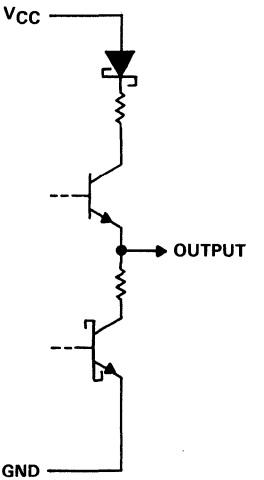


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of each output



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage (see Note 1)	−0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	−0.5 V to 5.5 V
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Input clamp current	−30 mA
Current into any output in the low state	24 mA
Operating free-air temperature range: SN54BCT2244	−55°C to 125°C
SN74BCT2244	0°C to 70°C
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT2244			SN74BCT2244			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−12	mA
I_{OL}	Low-level output current			12			12	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT2244			SN74BCT2244			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.4			2.4			V
		I_{OH} = −12 mA	2			2			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 1 mA		0.15	0.5		0.15	0.5	V
		I_{OL} = 12 mA		0.35	0.8		0.35	0.8	
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−1			−1	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		23	37		23	37	mA
I_{CCL}				53	77		53	77	
I_{CCZ}				6.5	10		6.5	10	
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		6			6		pF
C_o	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		11			11		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

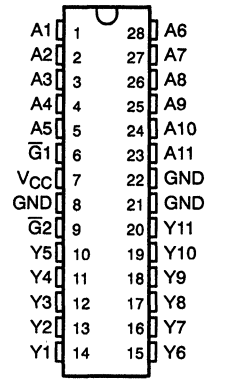
switching characteristics (see Note 2)

PARAMETER	FROM (INTPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX			UNIT
			'BCT2244			SN54BCT2244		SN74BCT2244	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	0.5	3	4.4	0.5	5.2	0.5	4.9	ns
t_{PHL}			1.6	4.6	6.3	1.6	7.1	1.6	6.7	
t_{PZH}	$\overline{G}$	Y	2.4	6.1	7.7	2.4	9.1	2.4	8.7	ns
t_{PZL}			3.9	7.6	9.4	3.9	10.8	3.9	10.4	
t_{PHZ}	$\overline{G}$	Y	1.7	5.2	6.9	1.7	8.1	1.7	7.8	ns
t_{PLZ}			2.8	6.5	8.3	2.8	10.9	2.8	9.8	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Package Options Include Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT2410 . . . JT PACKAGE
SN74BCT2410 . . . NT PACKAGE
(TOP VIEW)



description

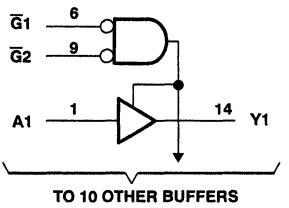
The 'BCT2410 is a noninverting 11-bit buffer/line driver specifically designed to drive MOS DRAMs of up to 4 megabits. It is also suitable for use with wide data paths or buses carrying parity. The outputs, which are designed to source 1 mA and sink 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The output-enable inputs $\overline{G}1$ and $\overline{G}2$ are routed internally to a two-input AND gate with active-low inputs. When both $\overline{G}1$ and $\overline{G}2$ are low, the Y outputs are active (high or low logic state). When either $\overline{G}1$ or $\overline{G}2$ is high, the Y outputs are in the high-impedance state.

The multiple ground pins of the 'BCT2410 reduce switching noise for more reliable system operation.

The SN54BCT2410 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74BCT2410 is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)

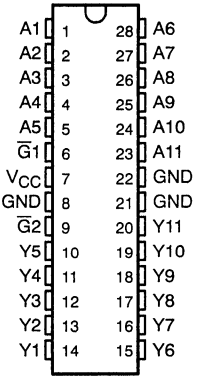


PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Package Options Include Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT2411 . . . JT PACKAGE
SN74BCT2411 . . . NT PACKAGE
(TOP VIEW)



description

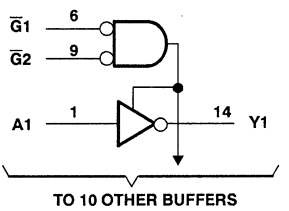
The 'BCT2411 is an inverting 11-bit buffer/line driver specifically designed to drive MOS DRAMs of up to 4 megabits. It is also suitable for use with wide data paths or buses carrying parity. The outputs, which are designed to source 1 mA and sink 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The output-enable inputs $\overline{G}1$ and $\overline{G}2$ are routed internally to a two-input AND gate with active-low inputs. When both $\overline{G}1$ and $\overline{G}2$ are low, the Y outputs are active (high or low logic state) and reflect the inverse of the data at the A inputs. When either $\overline{G}1$ or $\overline{G}2$ is high, the Y outputs are in the high-impedance state.

The multiple ground pins of the 'BCT2411 reduce switching noise for more reliable system operation.

The SN54BCT2411 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74BCT2411 is characterized for operation from 0°C to 70°C.

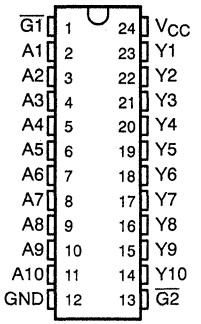
logic diagram (positive logic)



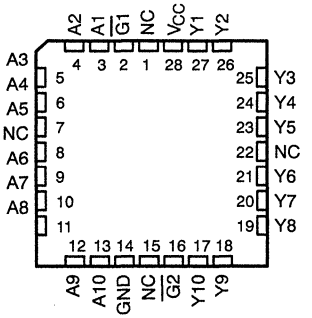
PRODUCT PREVIEW

- **BiCMOS Design Substantially Reduces I_{CCZ}**
- **Output Ports Have Equivalent 25-Ω Resistors, So No External Resistors Are Required**
- **Specifically Designed to Drive MOS DRAMs**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)**
- **Power-Up High-Impedance State**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT2827B . . . JT PACKAGE
SN74BCT2827B . . . DW OR NT PACKAGE
(TOP VIEW)



SN54BCT2827B . . . FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

These 10-bit buffers and bus drivers are specifically designed to drive the capacitive input characteristics of MOS DRAMs. They provide high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so if either $\overline{G1}$ or $\overline{G2}$ is high, all 10 outputs are in the high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down.

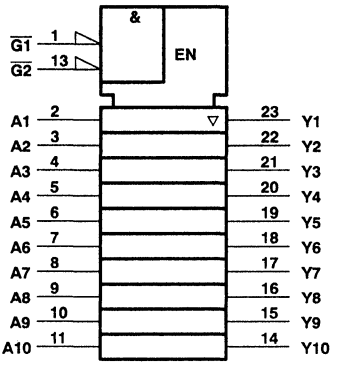
The SN54BCT2827B is characterized for operation over the full military temperature range of – 55°C to 125°C. The SN74BCT2827B is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{G1}$	$\overline{G2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

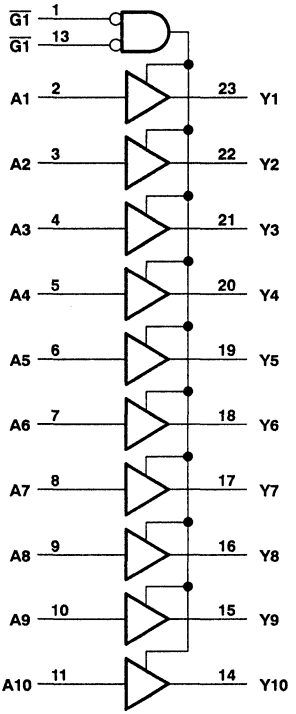
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic symbol†



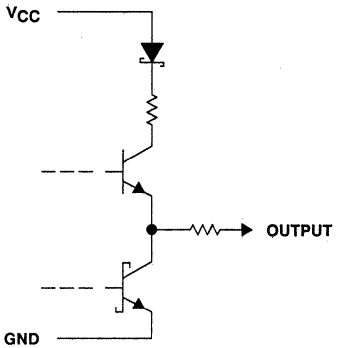
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

schematic of each output



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Input voltage range (see Note 1) ..... – 0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... – 0.5 V to 5.5 V
Voltage applied to any output in the high state ..... – 0.5 V to V_{CC}
Input clamp current ..... – 30 mA
Current into any output in the low state: SN54BCT2827B ..... 24 mA
SN74BCT2827B ..... 24 mA
Operating free-air temperature range: SN54BCT2827B ..... – 55°C to 125°C
SN74BCT2827B ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT2827B			SN74BCT2827B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			– 18			– 18	mA
I_{OH}	High-level output current			– 1			– 1	mA
I_{OL}	Low-level output current			12			12	mA
T_A	Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			SN54BCT2827B			SN74BCT2827B			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = – 18 mA			– 1.2			– 1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V	I_{OH} = – 1 mA	V_{CC}–2			V_{CC}–2			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 1 mA		0.15	0.5		0.15	0.5	V
		I_{OL} = 12 mA		0.35	0.8		0.35	0.8	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			– 20			– 20	µA
$I_{OL(sink)}$	V_{CC} = 4.5 V,	V_O = 2 V	50			50			mA
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			– 0.2			– 0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_I = 2.25 V	– 30		– 112	– 30		– 112	mA
I_{CCL}	V_{CC} = 5.5 V,	Outputs open		28	44		28	44	mA
I_{CCZ}	V_{CC} = 5.5 V,	Outputs open		3.8	6		3.8	6	mA
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		5			5		pF
C_o				8			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

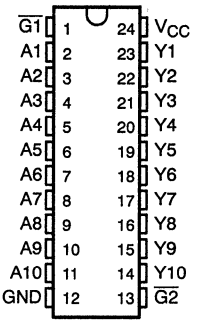
switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§			UNIT
			'BCT2827B			SN54BCT2827B		SN74BCT2827B	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	0.9	3.6	5.2	0.9	6.6	0.9	6	ns
t_{PHL}			2	5.1	7.2	2	8.2	2	7.8	
t_{PZH}	$\overline{G}$	Y	2.8	5.6	8	2.8	10.7	2.8	10.7	ns
t_{PZL}			5.6	8.9	11	5.6	13.7	5.6	12.9	
t_{PHZ}	$\overline{G}$	Y	3.2	6.7	9.3	3.2	11.8	3.2	10.9	ns
t_{PLZ}			2.7	5.3	7.1	2.7	9.5	2.7	8.3	

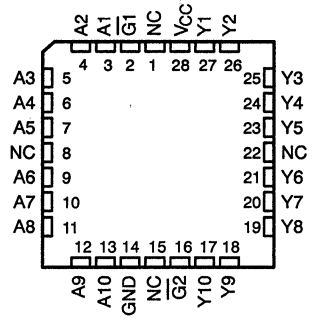
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating condtions.
NOTE 2: Load circuit and voltlage waveforms are shown in Section 1.

- **BiCMOS Design Substantially Reduces I_{CCZ}**
- **Output Ports Have Equivalent 25-Ω Resistors, So No External Resistors Are Required**
- **Specifically Designed to Drive MOS DRAMs**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Data Flow-Thru Pinout (All Inputs on Opposite Side From Outputs)**
- **Power-Up High-Impedance State**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT2828B . . . JT PACKAGE
SN74BCT2828B . . . DW OR NT PACKAGE
(TOP VIEW)



SN54BCT2828B . . . FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

These 10-bit buffers and bus drivers are specifically designed to drive the capacitive input characteristics of MOS DRAMs. They provide high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so if either $\overline{G1}$ or $\overline{G2}$ is high, all 10 outputs are in the high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down.

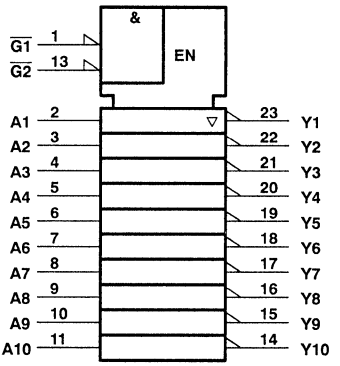
The SN54BCT2828B is characterized for operation over the full military temperature range of – 55°C to 125°C. The SN74BCT2828B is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{G1}$	$\overline{G2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

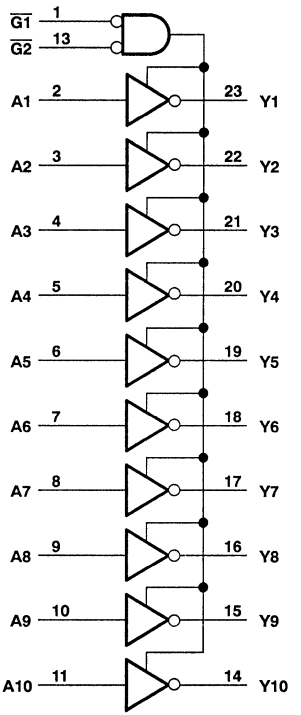
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

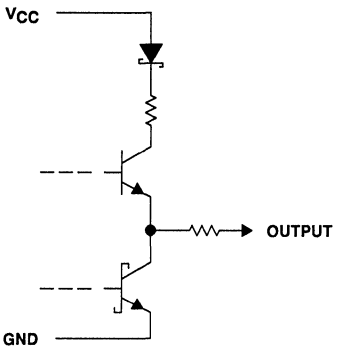
logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

PRODUCT PREVIEW

schematic of each output



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Input voltage range (see Note 1) ..... – 0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... – 0.5 V to 5.5 V
Voltage applied to any output in the high state ..... – 0.5 V to V_{CC}
Input clamp current ..... – 30 mA
Current into any output in the low state ..... 24 mA
Operating free-air temperature range: SN54BCT2828B ..... – 55°C to 125°C
SN74BCT2828B ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage ratings may be exceeded if the input clamp current ratings is observed.

recommended operating conditions

		SN54BCT2828B			SN74BCT2828B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			– 18			– 18	mA
I_{OH}	High-level output current			– 1			– 1	mA
I_{OL}	Low-level output current			12			12	mA
T_A	Operating free-air temperature	– 55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT2828B			SN74BCT2828B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = – 18 mA			– 1.2			– 1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V	I_{OH} = – 1 mA	V_{CC}–2			V_{CC}–2			V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 1 mA		0.15	0.5		0.15	0.5	V
		I_{OL} = 12 mA		0.35	0.8		0.35	0.8	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			– 20			– 20	µA
$I_{OL(sink)}$	V_{CC} = 4.5 V,	V_O = 2 V	50			50			mA
I_I	V_{CC} = 5.5 V,	V_O = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			– 0.2			– 0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_I = 2.25 V	– 30		– 112	– 30		– 112	mA
I_{CCL}	V_{CC} = 5.5 V,	Outputs open		28			28		mA
I_{CCZ}	V_{CC} = 5.5 V,	Outputs open		3.5			3.5		mA
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		5			5		pF
C_o				8			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

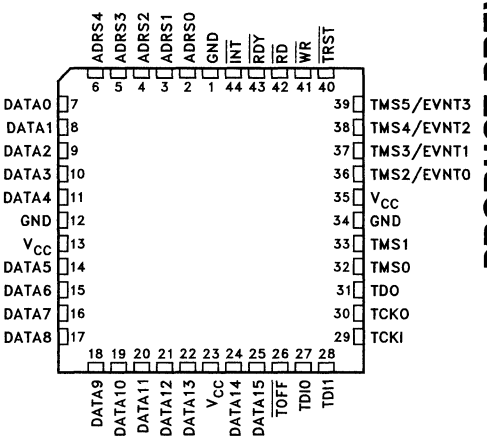
PRODUCT PREVIEW

TI0288—D3610, JULY 1990

PRODUCT PREVIEW

- **Members of the Texas Instruments SCOPE™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus**
- **Control Operation of up to Six Parallel Target Scan Paths**
- **Each Include Four Bidirectional Event Pins for Additional Test Capability**
- **Accommodate Delay to Target of up to 31 Clock Cycles**
- **30-MHz Operation**
- **Execute Instructions for up to 2^{32} Clock Cycles**
- **Scan Data up to 2^{32} Bits in Length**
- **Inputs are TTL-Voltage Compatible**
- **Compatible With TI's ASSET™ (Automated System Support for Emulation and Test)**
- **VLSI Devices, Each Containing Over 34,000 Transistors**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Packaged in 44-pin Plastic and Ceramic Leaded Chip Carriers**

SN54ACT8990 ... FJ PACKAGE
SN74ACT8990 ... FN PACKAGE
(TOP VIEW)



description

The 'ACT8990 is a member of Texas Instruments SCOPE™ testability IC family. This family of components facilitates testing of complex circuit board assemblies.

The 'ACT8990 test bus controller (TBC) is designed to control the operation of an IEEE Standard 1149.1 (JTAG) scan test path by taking input from a host and generating the proper signals to interface with the target device(s). The target(s) can be moved from any stable state to another stable state, loaded with instructions, and resulting test data scanned out to be read by the host. Four EVENT pins are provided to allow real-time interaction between the ACT8990 and its target(s). The EVENT pins can be configured to generate interrupt requests when some user-definable condition is present.

A 32-bit counter can be preset to allow a predetermined number of clock cycles or instruction executions to occur and can be programmed to set an interrupt flag when it reaches a count of zero.

Two 16-bit serial buffers (read and write) are implemented for the host interface.

The SN54ACT8990 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ACT8990 is characterized for operation from 0°C to 70°C.

SCOPE, ASSET, and EPIC are trademarks of Texas Instruments Incorporated.

description (continued)

The 'ACT8990 implements all the low-level functions, enabling the host to use higher-level abstraction such as:

- States of IEEE Standard 1149.1 for control.
- Variables indicating command finish, buffer full or empty for status.
- Strings and buffers for data.

The target interface may connect without external logic to:

- Six parallel chains of IEEE Standard 1149.1 targets, each with its own separate TMS signal. The parallel chains share one or two TDI signals, one TDO signal, and one $\overline{\text{TRST}}$ signal and TCK signal.
- Fanout devices that support many targets requiring two separate TMS signals for target selection and target control.
- Local targets (on-board the 'ACT8990) with one TDI input and remote targets with the other TDI input.

The target interface has four event detectors and two 16-bit event counters to support asynchronous functions. The 'ACT8990 can connect to the target via a retimed link with up to 31 bits of delay. This may be required when the clock rate is high and either the target is at a distance or the link involves fanout or buffer/driver devices. The 'ACT8990 operates with a clock period down to 33 ns (>30 MHz) over the commercial temperature range of 0° to 70°.

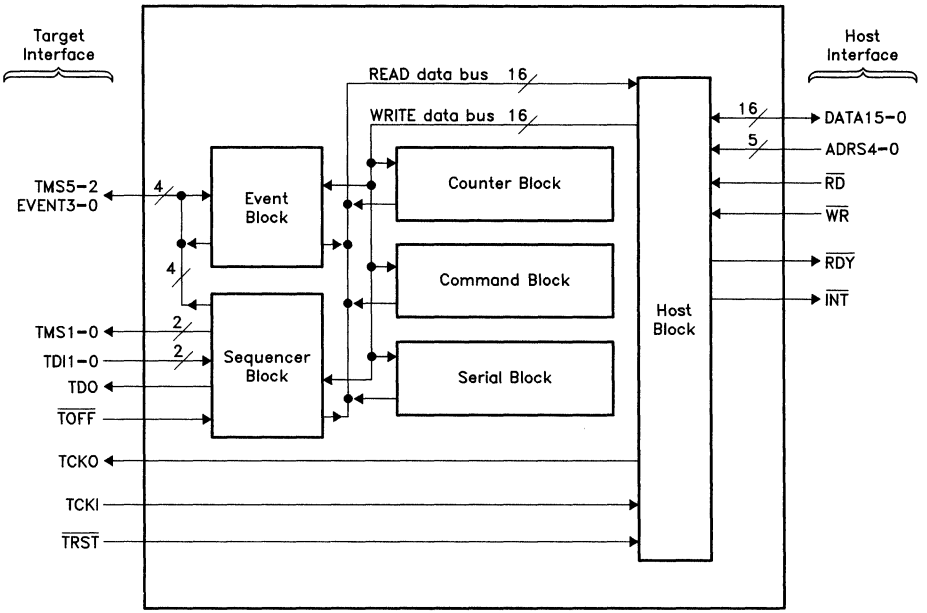
The host interface has a 16-bit data bus. The critical host interface timing is independent of the clock period.

The major functions of the 'ACT8990 are controlled by specific commands:

- The STATE command controls the target interface and target state diagrams. It can change the state to any stable state.
- The EXECUTE command causes the target to execute instructions that have been shifted into it. It uses the Run-Test/Idle state. It can execute instructions for a fixed time or until an event occurs.
- The SCAN command circulates data among targets and transfers data between the 'ACT8990 and targets. It uses the Shift-IR or Shift-DR states. It uses the read and write buffers, which can each hold two 16-bit data words.

TI0288—D3610, JULY 1990

functional block diagram



D3610, JULY 1990—TI0288

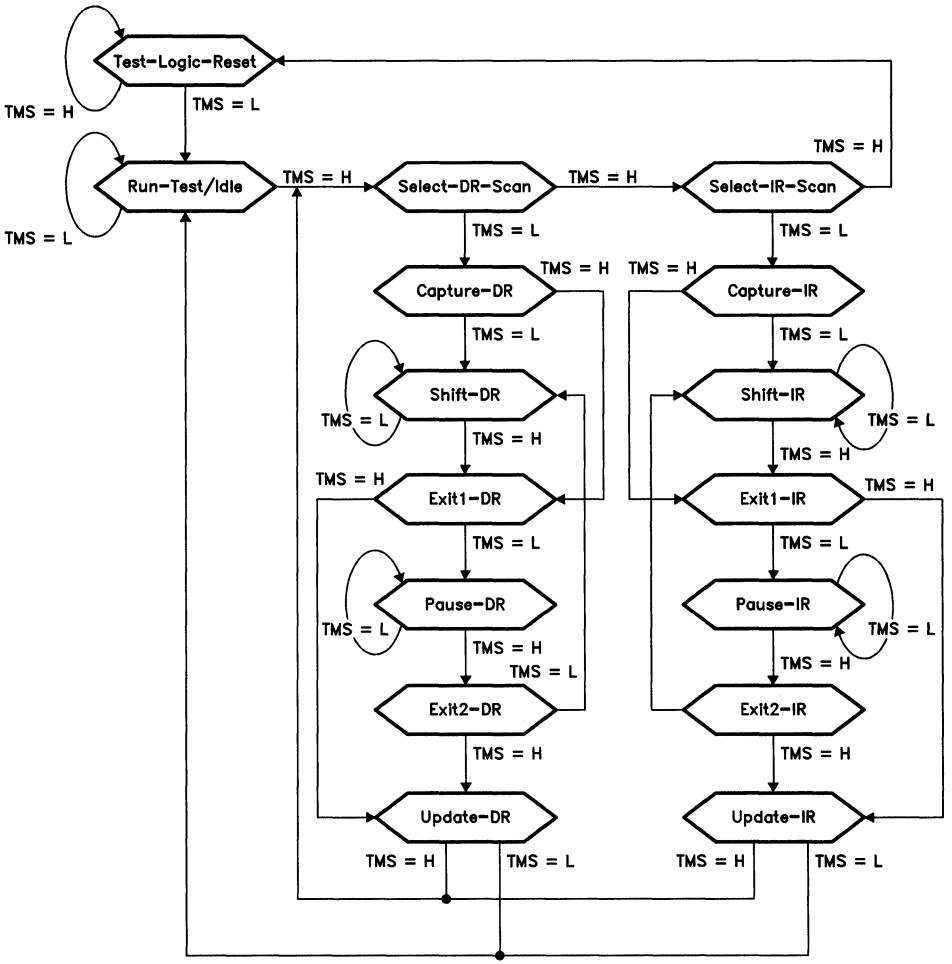


FIGURE 1. TAP STATE DIAGRAM

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state diagram description

The 'ACT8990 controls 1149.1 targets by generating and accepting TMS, TDO and TDI signals compatible with the IEEE Standard 1149.1 state diagram shown in Figure 1. There are six stable states (indicated by a looping arrow) and ten unstable states (indicated by two exiting arrows) in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to manipulate a data register and one to manipulate the instruction register. Only one register should be manipulated at a time.

Test-Logic-Reset
In this state, the test logic is inactive, and an internal reset signal is applied to all registers in the device. During device operation, the TAP returns to this state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup that forces it to a high level if left unconnected or if a board defect causes it to be open-circuited.

Run-Test/Idle
The TAP must pass through this state before executing any test operations. The TAP may retain this state indefinitely, and no registers are modified while in Run-Test/Idle.

Select-DR-Scan, Select-IR-Scan
No specific function is performed in these states, and the TAP exits either of them on the next TCK cycle.

Capture-DR
The selected data register is placed in the scan path (i.e., between TDI and TDO). Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK, causing the TAP state to change.

Shift-DR
In this state, data is serially shifted through the selected data register, from TDI to TDO, on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR).

On the falling edge of TCK in Shift-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO enables to the level present before it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO enables to a low level.

Exit1-DR, Exit2-DR
These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-DR to Exit1-DR.

Pause-DR
The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data.

Update-DR
If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated during this state only.

state diagram description (continued)

Capture-IR
The instruction register is preloaded with the IR status word and placed in the scan path.

Shift-IR
In this state, data is serially shifted through the instruction register, from TDI to TDO, on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). On the falling edge of TCK in Shift-IR, TDO goes from the high-impedance state to the active state.

Exit1-IR, Exit2-IR
These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-IR to Exit1-IR.

Pause-IR
The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR
The latches shadowing the instruction register are updated with the new instruction.

terminal descriptions

The signal pins on the 'ACT8990 (Terminal Function Table) are separated into two main categories: host interface and target interface.

host interface terminals

DATA15–0
These bidirectional pins form the 16-bit interface between the host and the controller. Information is written to and read from the registers via the DATA15–0 pins.

ADRS4–0
The address pins are used to select the register to be written to or read from.

$\overline{RD}$
$\overline{RD}$ is the strobe for reading data from a selected register. When low, $\overline{RD}$ acts as the output enable for the DATA15–0 bus.

$\overline{WR}$
$\overline{WR}$ is the strobe for writing data to a selected register.

$\overline{INT}$
This output has high-impedance capability and is used to output an interrupt signal to the host.

$\overline{RDY}$
$\overline{RDY}$ is asserted low during recovery time from a read or write operation or when certain accesses to the 'ACT8990 are not allowed.

$\overline{TRST}$
A software reset occurs when $\overline{TRST}$ is asserted low.

$\overline{TOFF}$
All I/O and output pins are in the high-impedance state when $\overline{TOFF}$ is low.

terminal descriptions (continued)

target interface terminals

TDI1–0
The test data in pins are the serial input pins for shifting test data from the target(s) into the 'ACT8990.

TDO
The test data out pin is the serial output from the 'ACT8990.

TMS1–0
The test mode selects are used to interface the TBC to target(s) and direct them through their states.

TCKI
Operation of the 'ACT8990 is synchronous to the TCKI input.

TCKO
Test clock out is the buffered TCKI signal and is distributed to the target(s).

EVNT3–0/TMS5–2
These pins are configurable to act as event pins or test-mode-select pins. As event pins, they can be set to output interrupt flags based on user-definable input conditions. As test-mode-select pins, they can control up to four additional scan paths.

TERMINAL FUNCTIONS

SIGNAL	GROUP	TYPE	DESCRIPTION
DATA15–0	Host Interface	I/O	Data Bus
ADRS4–0		Input	Address Bus
$\overline{RD}$		Input	Read Strobe
$\overline{WR}$		Input	Write Strobe
$\overline{RDY}$		Output	Ready
$\overline{INT}$		Output	Interrupt
TMS1–0	Target Interface	Output	Test Mode Select
EVNT3–0/TMS5–2		I/O	Event Pins/TMS
TDO		Output	Test Data Out
TCKO		Output	Test Clock Out
TCKI		Input	Test Clock In
TDI1–0		Input	Test Data In
$\overline{TOFF}$		Input	Test Off
$\overline{TRST}$		Input	Test Reset
V_{CC}	Power		5 V Power
GND			Ground

terms

JTAG
The Joint Test Action Group is the originator of IEEE Standard 1149.1.

SCOPE
System Controllability and Observability Partitioning Environment. This is the family name for Texas Instruments testability products.

host
The device directing the activity of the 'ACT8990 (processor-based system), typically a personal computer or other workstation.

terms (continued)

target
One or more devices controlled by the 'ACT8990 through its target interface. The target(s) must be IEEE Standard 1149.1-compatible.

fanout device
This is a device that allows the 'ACT8990 to control many parallel targets.

clock
The system test clock used by the controller and its target(s). The clock is input on TCKI and output on TCKO.

off and on
Output and bidirectional buffers are considered "off" when in a high-impedance state and "on" when in the active state and able to output a logic high or low level.

direct link
This is a connection between the 'ACT8990 and targets that involves delaying the target interface signals by less than one clock period. It can either be a "pin-to-pin" connection or a connection via "buffer/driver" devices.

retimed link
This is a connection between the 'ACT8990 and targets that involves delaying the target interface signals by one or more clock periods. It typically involves flip-flops distributed along a cable, within a fanout device, or on a board.

major command
Selected through the major command register, major commands instruct the controller to perform operations on the target(s) such as scan, state change, or the execution of an instruction. Major commands typically take many clock cycles to complete. There are three major commands: STATE, EXECUTE, and SCAN.

dead and alive
Major commands are dead, and the alive status bit (status1 register bit 15) is zero when the state machine implementing it is inactive. They are alive, and the alive status bit is one when the state machine is active.

awake and asleep
Alive major commands may be in one of two conditions. If awake, the awake status bit (status1 register bit 14) is one and the command actively performs its functions or ends. Otherwise, it is asleep, and the awake status bit is zero.

begin, suspend, resume, and end
Major commands begin when they become alive, suspend when they become asleep, resume when they become awake, and end when they go to the end state.

finish
Major commands finish when they become dead after reaching the end state and setting the finish flag.

minor command
Selected through the minor command register, minor commands instruct the controller to perform some functions within itself, such as SET, RESET, CLEAR or initiate a major command. Minor commands typically take few clock cycles to complete.

terms (continued)

null registers and null bits
These are registers and bits where no logic is implemented. Writes to them are ignored, and reads from them return zeroes.

sequence acceptor
The sequence acceptor accepts inputs from the TDI1–0 pins and link delay register and decodes them to determine which state is being returned from direct and retimed links.

link delay register
The link delay register uses the mode-source signal from the generator to produce a delayed-mode-source signal for the sequence acceptor. It models the delay in a direct or retimed link.

sequence generator
The sequence generator generates outputs on the TDO and TMS5–0 pins and to the link delay register to control the target state.

passing zero
A counter passes zero when it is operated at the all-zeroes value. Its value changes to all ones (if it decrements) or is updated (if it reloads). Other actions may also occur.

recirculate data
Data that was previously received from the target and is sent back by the shifter-FIFO.

overwrite data
Data sent to the target from the write buffer to replace data previously received from the target.

operation

clock
The timing of most of the 'ACT8990 functions is synchronous to the clock signal (TCKI). This signal is output on the test clock output (TCKO) to provide a signal that has undergone delays due to output buffers similar to those of the target interface outputs. TCKO may also be set to one, zero, or the high-impedance state by the clock format, clock data, and clock off bits in the control3 register.

reset
The two methods of initializing the 'ACT8990 are hardware reset and software reset. The reset timing is detailed in Figure 2.

Asserting the active-low $\overline{\text{TRST}}$ input causes a hardware reset that initializes the output and bidirectional pins:

- DATA15–0, $\overline{\text{INT}}$, $\overline{\text{RDY}}$, and TMS5–2/EVENT 3–0 take on the high-impedance state.
- TDO and TMS1–0 output the logic high level.
- TCKO outputs the clock.

The effects of $\overline{\text{TRST}}$ on DATA15–0, $\overline{\text{INT}}$, $\overline{\text{RDY}}$ and EVENT3–0 are immediate and asynchronous to the clock, while its effects on TMS1–0, TDO and TCKO are synchronous, occurring a few periods after $\overline{\text{TRST}}$ goes low. This means that during the initial power-on reset by $\overline{\text{TRST}}$, these four signals are undefined for a few clock periods but, during later assertions of $\overline{\text{TRST}}$, the changes on these pins are synchronous.

Taking $\overline{\text{TRST}}$ high causes hardware reset to end and software reset to begin. Note that if $\overline{\text{TOFF}}$ and $\overline{\text{TRST}}$ are both asserted, then all output and bidirectional pins are in the high-impedance state.

operation (continued)

A software reset occurs automatically after the hardware reset ends or when a RESET command is written to the minor command register. It initializes all internal logic as well as the output and bidirectional pins synchronously to the clock:

- The $\overline{INT}$ and $\overline{RDY}$ pins output the logic high level.
- The TMS5–2 and EVENT3–0 pins take on the high-impedance state.
- The TDO and TMS1–0 pins output the logic high level.
- The TCKO pin outputs the clock.
- The major commands become dead.
- The data buffers and shifter-FIFO are emptied.
- Counter1, counter20 and counter21 bits are all set to zero.
- The host interface register bits are all set to zero.

Hardware reset requires up to 5 clock periods after $\overline{TRST}$ is taken high. Software reset requires up to 8 clock periods after $\overline{TRST}$ is taken high or up to 8.5 clock periods after the rising edge of $\overline{WR}$.

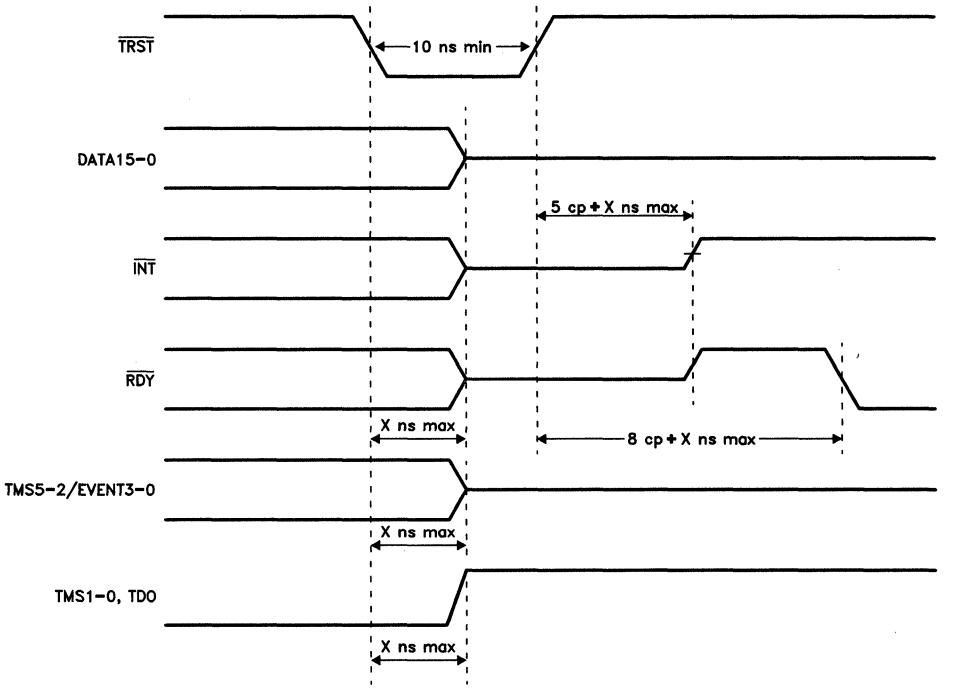

FIGURE 2. RESET TIMING DIAGRAM

architecture

The 'ACT8990 is constructed internally from six logic blocks, thirty-eight I/O buffers, and separate 16-bit read-data and write-data buses. This is summarized in the functional block diagram.

host interface

The host interface is constructed from the host block shown in Figure 3. The host block is the host-interface data-transfer and control logic. It also holds the hardware and software reset logic. Its four sections are:

- The data bus logic: transfers data between the data bus pins and the independent internal 16-bit read and write data buses.
- The address and access logic: operates during accesses by the host. It synchronizes the host signals to the clock, selects the registers to be accessed and controls the data bus logic and asserts $\overline{RDY}$ during the recovery time.
- The interrupt logic: asserts the $\overline{INT}$ pin based on the interrupt flag and enable signals.
- The reset logic: generates asynchronous and synchronous reset control signals in response to the assertion of the $\overline{TRST}$ pin or writing RESET commands.

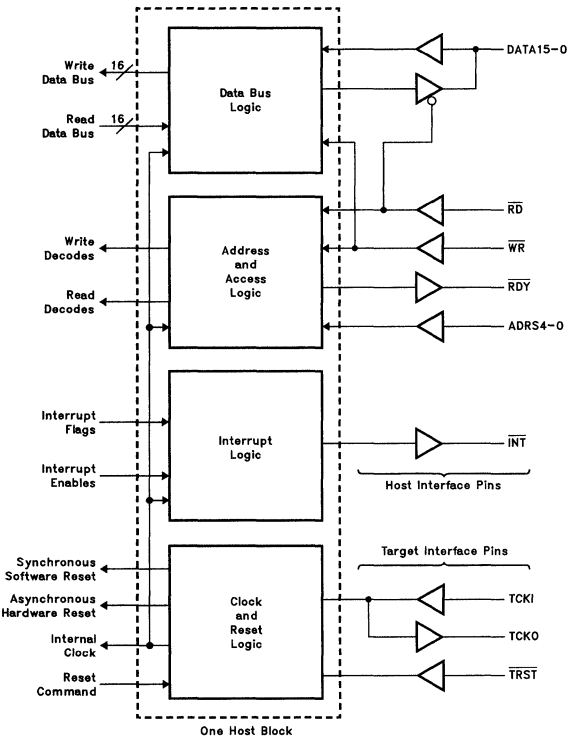

FIGURE 3. HOST INTERFACE

architecture (continued)

interrupts via the host interface

The 'ACT8990 asserts $\overline{INT}$ to make an interrupt request to the host when matching flag status bits and enable control bits are set. The flags are set by the 'ACT8990 when specific events occur. They are set or cleared by the host, either individually by SET or CLEAR commands or all at once by a RESET command. The enable bits are used by the host to select which flags may generate interrupt requests.

accesses via the host interface

The host asserts $\overline{WR}$ or $\overline{RD}$ to write or read registers via the host interface. The host interface logic is designed so that the assertion of $\overline{WR}$ and $\overline{RD}$ can be asynchronous to the clock. The write and read timing is detailed in Figures 4 and 5.

$\overline{WR}$ is the strobe for the DATA15–0 and ADRS4–0 pins, which are sampled on its rising edge. Their setup and hold times are relative to this edge. The sampled address and data are synchronous to the clock and used to load the selected register.

$\overline{RD}$ is the output enable for the DATA15–0 pins. The setup and hold times for $\overline{RD}$ and ADRS4–0 are relative to the time at which the host samples DATA15–0.

$\overline{RDY}$ is asserted during the recovery time following the rising edge of $\overline{RD}$ or $\overline{WR}$.

recovery time

The host must not access registers during the recovery time in which $\overline{RDY}$ is asserted. This occurs when internal control signals are generated that require several clock periods to become synchronous to the clock and complete their operations. The recovery time rules are:

- Writes are ignored while a write is completing and reads give invalid data while a write to the same address is completing. This requires up to 3.5 clock periods from the rising edge of $\overline{WR}$ to its next rising edge or to the falling edge of $\overline{RD}$.
- Reads from the status and capture registers give invalid data while a minor command is completing. This requires up to 4.5 clock periods from the rising edge of $\overline{WR}$ to the falling edge of $\overline{RD}$.
- Reads from the read buffer register give invalid data while a previous read is completing. This requires up to 4.5 clock periods from the rising edge of $\overline{RD}$ to its next falling edge.
- Writes are ignored and reads give invalid data during a software reset initiated by a RESET command. This requires up to 8.5 clock periods from the rising edge of $\overline{WR}$ to its next rising edge or to the falling edge of $\overline{RD}$.
- Writes are ignored and reads give invalid data during hardware and software resets initiated by asserting $\overline{TRST}$. This requires up to 6.5 clock periods from the rising edge of $\overline{TRST}$ to the rising edge of $\overline{WR}$ or the falling edge of $\overline{RD}$.

These rules may be met:

- Explicitly by the host software spacing accesses or polling $\overline{RDY}$.
- Implicitly by the host hardware using $\overline{RDY}$ to delay later accesses until the recovery time is ended.

$\overline{RDY}$ is asserted asynchronously when $\overline{TRST}$ is taken high or on the rising edge of $\overline{RD}$ or $\overline{WR}$, then later negated after a rising edge of the clock.

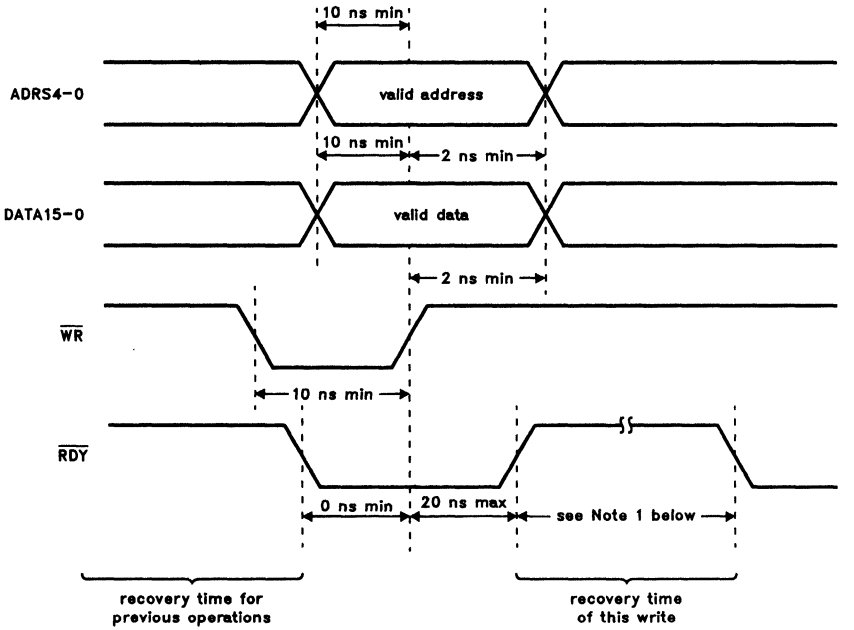

FIGURE 4. HOST WRITE TIMING DIAGRAM

NOTE 1:
Register recovery time is 3.5 cp + 30 ns max.
Minor command recovery time is 4.5 cp + 30 ns max.
Software reset recovery time is 8.5 cp + 30 ns max.

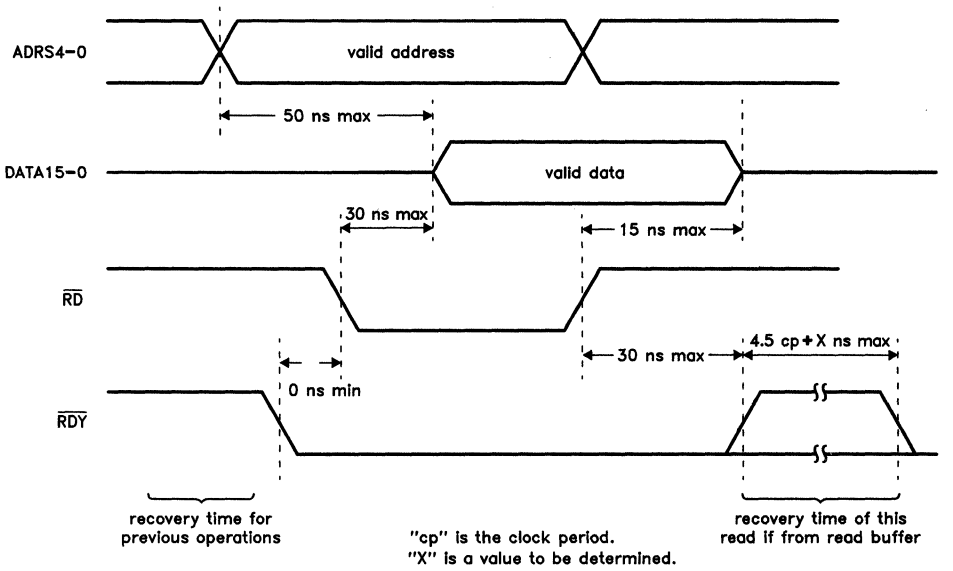

FIGURE 5. HOST READ TIMING DIAGRAM

register set

The 'ACT8990 has five address inputs (ADRS4–0) to select any one of the twenty-four 16-bit registers. When ADRS4–0 has values 00000-10111, the host is able to access a register via DATA15–0. When ADRS4–0 has values 11000-11111, then writes are ignored and all zeroes are read.

The 24 registers are listed in Table 3. For the convenience of the host, functions are partitioned as control and status, then arranged on byte boundaries to minimize the register space. Some register bits contain functions used only during manufacturing test.

The design of null registers and null bits is such that writing to them has no effect and reading from them obtains all zeroes.

control and status functions

The host configures the 'ACT8990 by writing to the control and update registers before, during, or after commands. These registers can be freely accessed by the host as their bits are not altered by the 'ACT8990.

The host examines the 'ACT8990 by reading the status and capture registers. Before reading them, the host must first write an OPERATE2 command to capture information in the status and capture registers. These register bits then indicate the 'ACT8990 state at the time of the command. The reason for this is that the reading of these registers is asynchronous to the changes in the 'ACT8990 internal flags and signals which occur every clock period. Thus the flags and signals cannot be read directly. The OPERATE2 command logic captures the values of the flags and signals in the clock period in which it executes.

register set (continued)

minor commands

Minor commands are begun by the host when it writes to the minor command register. They instruct the controller to perform some functions within itself. These commands require only a few clock periods and the $\overline{RDY}$ pin is asserted while they are alive. The minor commands are as follows:

- The CLEAR0/1 and SET0/1 commands modify selected interrupt flags.
- The OPERATE0/1 commands affect the operation of major commands.
- The OPERATE2 command operates functions related to the status registers and counters.
- The RESET command resets selected functions or the entire 'ACT8990.

major commands

Major commands are selected by the value in the major command register. They instruct the controller to perform operations on the target(s). They are begun by the host when an OPERATE0/1 command is written to the minor command register or, if the major command is the EXECUTE command, it may be begun by an event detection. The major commands may require many clock periods. They affect the awake and alive status bits (status1 register bits 14 and 15). When they finish, the finish flag (status0 register bit 15) is set and an interrupt may occur.

The STATE command controls the target state without performing any other explicit action. It can change the state from its current stable state to any stable state. It is used to implement:

- Exiting and entering the Test-Logic-Reset state.
- Additional state changes between other EXECUTE and SCAN commands.
- Context switches between parallel targets.
- Context switches between the data and control paths of a fanout expander.

The EXECUTE command makes the target execute instructions that have been shifted into it. It uses the Run-Test/Idle state. The instructions may be executed for up to 2^{32} clock periods. They can be executed for a fixed time or until an event occurs. Their execute times may also be benchmarked.

The SCAN command circulates data among targets and transfers data between the 'ACT8990 and targets. It uses the Shift-IR or Shift-DR states. The data may be up to 2^{32} bits long. During these operations, the read and write buffers can each hold up to two 16-bit words of data at a time.

counter1

This synchronous 32-bit counter is used to count the number of execute states sent by EXECUTE commands and data bits shifted by SCAN commands. It is configured by the bits in the control8 register and can be used independently of the commands.

The counter1 update registers and the capture registers load and store this counter. The host writes initial values to the update registers and reads current and final values from the capture registers. Reset fills counter1 and its update and capture registers with zeroes.

Counter1 can be loaded from the update register:

- By an OPERATE2 command, usually before EXECUTE and SCAN commands.
- When it passes zero, if the counter1 reload control bit is set.

Counter1 can be stored to the capture registers by an OPERATE2 command, usually during and after EXECUTE and SCAN commands.

register set (continued)

Counter1 is operated:

- By an OPERATE2 command.
- By a SCAN command sending scan states.
- As decided by the counter1 operate control bits:
  - Not at all.
  - When sending execute states during an EXECUTE command.
  - Throughout an EXECUTE command.
  - When a selected event detector detects an event on an EVENT pin directly or via counter20/21.
  - When a low level occurs on a selected EVENT pin.
  - When a high level occurs on a selected EVENT pin.

The effects of counter1 when passing zero are:

- SCAN commands are ended. The counter1 scan flag is sent and an interrupt may occur.
- EXECUTE commands are either not affected, suspended or ended as decided by the counter1 pause and end control bits. The counter1 execute flag is set and an interrupt may occur.
- If neither a SCAN nor EXECUTE command is alive, the counter1 execute flag is set and an interrupt may occur.

When an EXECUTE or SCAN command ends or aborts, the difference between the initial value written to the counter1 update registers and final value read from the capture registers is the number of execute states sent or data bits shifted. A later command may complete the actions of this command if the counter is not loaded again.

data buffers and shifter-FIFO

The target's data and instruction registers are operated on as a number of modules each containing a string of data. These strings are accessed with one or more SCAN commands that operate the data buffer and shifter-FIFO functions of the 'ACT8990. The data buffers and shifter-FIFO are configured by the values of the bits in the control4 register. These functions are shown in Figure 9.

On the host interface, these strings are handled as parallel data by the data buffers. On the target interface, the strings are handled as serial data by the shifter-FIFO. The data buffers and shifter-FIFO are loaded and stored by the transfer functions that are described in the next section.

The write buffer is accessed via the write buffer register. It is used by the SCAN commands to pass data to TDO. The read buffer is accessed via the read buffer register. It is used by the SCAN commands to store data from TDI via the shifter-FIFO. Reset empties the data buffers.

The data buffers can each hold up to two 16-bit words of data. Their status is indicated by the write empty inverted, read full, write OK inverted and read OK status bits. These data buffers and their status bits are operational at all times. Thus, the write buffer can be written to before a SCAN command begins and the read buffer can be read from after a SCAN command finishes.

When the write buffer1–0 control bits are 00, 01, or 10, the write buffer is unused. This reduces writes on the host interface as the send data is not taken from the buffer. Instead, send data is either all zeroes, all ones, or recirculate data (data received from the target by the shifter-FIFO). Options 00 and 01 provide an efficient way of sending the BYPASS and EXTEST instructions. Option 10 provides an efficient way of bypassing strings that are of no interest. In option 11, the write buffer holds data that the host writes.

On the target interface, the target data and instruction registers are in series with the shifter-FIFO. The shifter-FIFO is an extra module containing a null string. This module is positioned such that SCAN commands operate on it first before the target strings. An extra SCAN command may bypass this null string by recirculating it before other SCAN commands access all the strings. Reset fills the shifter-FIFO and its null string with ones. These features of the architecture are shown in Figure 6.

register set (continued)

The shifter-FIFO provides serial-to-parallel conversion and compensates for the delay that occurs to returned data when a retimed link connects the 'ACT8990 and targets. If allows SCAN commands to scan continuously without sleeping even though there is a delay between the sending of data bits on TDO and the return of matching data bits on TDI. The length of the shifter-FIFO sets the upper limit on the length of the retimed links for continuous scanning. The shifter-FIFO can be configured as 16 or 32 bits long by the serial length control bit.

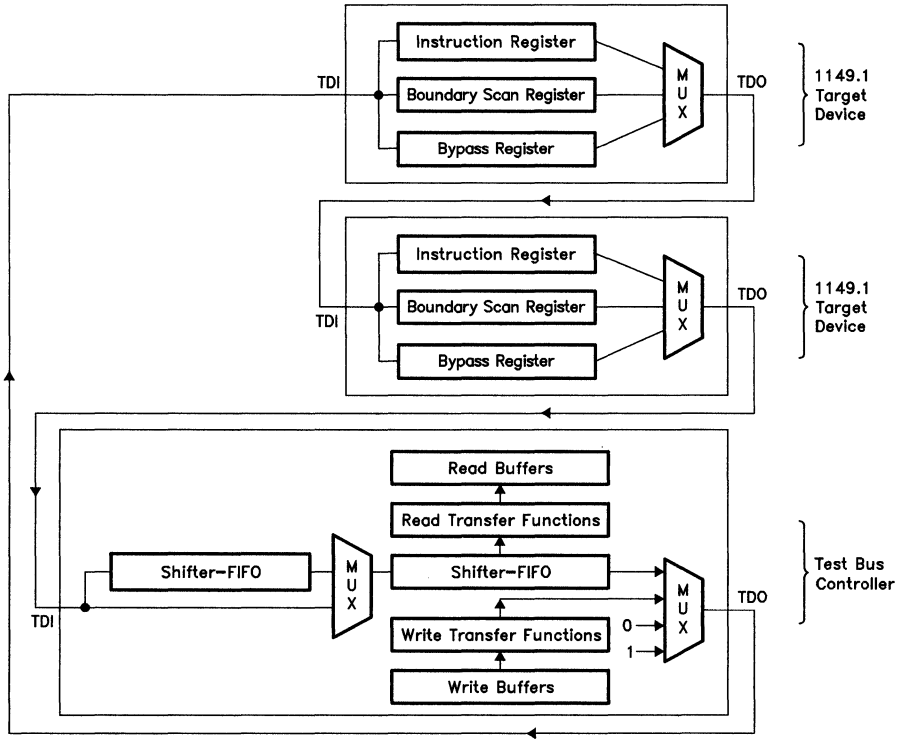

FIGURE 6. SCAN PATH OF THE TEST BUS CONTROLLER AND TARGET(S)

transfer functions

The strings of data in the shifter-FIFO, the target data and instruction registers may represent arithmetic quantities. In this case, the format of the strings may be interpreted as LSB first (least significant bit nearest TDO) or MSB first (most significant bit nearest TDO). These features of the architecture are shown in Figure 7.

The transfer functions convert data between the two serial formats used by the target data and instruction registers and the one parallel format used by the host. They are configured by the values of the bits in the control4 register. Physically, the transfer functions manipulate the bits in strings as they are passed from the serial-FIFO to the read buffer and from the write buffer to TDO. These functions are shown in Figures 6 and 9.

transfer functions (continued)

In the data buffers, bits 15 and 0 always represent the most and least significant bits in the word, respectively. The data buffers may hold whole words of 16 bits or partial words of less than 16 bits. When the read buffer holds a partial word, the upper bits that are not part of it are zero. When the write buffer holds a partial word, the upper bits that are not part of it are ignored.

The transfer format control bit (bit 11 of the control4 register) configures the transfer functions for operation with LSB-first or MSB-first strings:

- LSB-first format strings are passed between the host and target least significant word and bit first. Bit 0 of whole and partial words in the data buffers is sent and received first. The last word passed through the data buffers may be a partial word if the string is not a word multiple. In the target, the bit nearest TDO is considered the least-significant bit.
- MSB-first format strings are passed between the host and target most significant word and bit first. Bit 15 of whole words and a lower bit of partial words in the data buffers is sent and received first. The first word passed through the data buffers may be a partial word if the string is not a word multiple. In the target, the bit nearest TDO is considered the most-significant bit.

The value of the transfer format bit has no direct effect on data in the data buffers or shifter-FIFO. It only affects the formatting of data when it is loaded or stored. If different modules in the target contain data in different formats, they can be accessed by separate SCAN commands and the transfer format switched between commands.

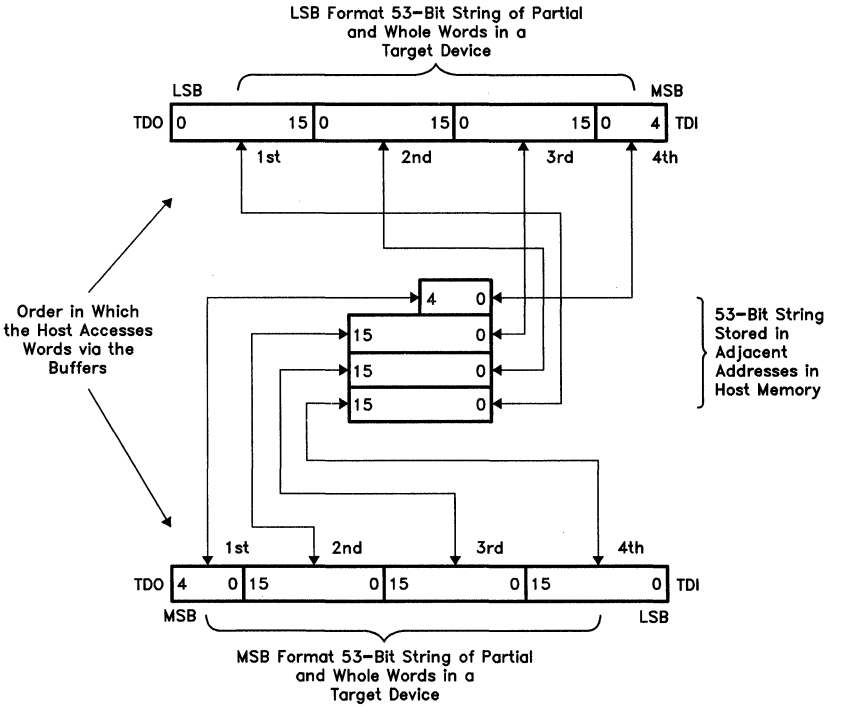

FIGURE 7. FORMAT OF STRINGS IN TARGET DEVICES AND THE HOST MEMORY

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target interface

The target interface is constructed from the sequencer block and the event block shown in Figures 8 through 10. They are detailed below:

The sequencer block is the target interface state machine. It is used by the major commands and has four sections:

- The requested state logic uses signals from the command blocks (command decode logic and major command state machines) to request that the sequence generator hold or change its state.
- The sequence generator is directed by the requested state logic to generate sequences on TMS5–0, output data on TDO, and generate the target interface state3–0 status bits on status2 register.
- The link delay logic generates a delayed-mode source for use by the sequence acceptor, from the mode source in the sequence generator, that matches the returned signals from the link delay logic.
- The sequence acceptor accepts data in source (DIS) and delayed mode source (DMS) signals and uses them to decide what state is being returned. It inputs data from the TDI1–0 input to the serial block (shifter-FIFO) (Figure 9). It indicates to the command block (Figure 10) (command state machines, counter control and status logic, and serial control and status logic) when temporary, scan, and execute states are being returned.

The event block (Figure 11) is used by the EXECUTE commands. It has three sections:

- The four event detectors are used for synchronization, masking, edge, and level detection logic for the EVENT pins and counter20/21. They output event detect flags for the command block (Figure 10) (command state machines and status logic).
- The event counter logic is the counter2 update registers (counter20 and counter21) and their control logic.
- The event input/output logic turns the output buffers on or off and outputs a value based on the countrol5 register event on and event data control bits. It inputs values to the status1 register event level status bits.

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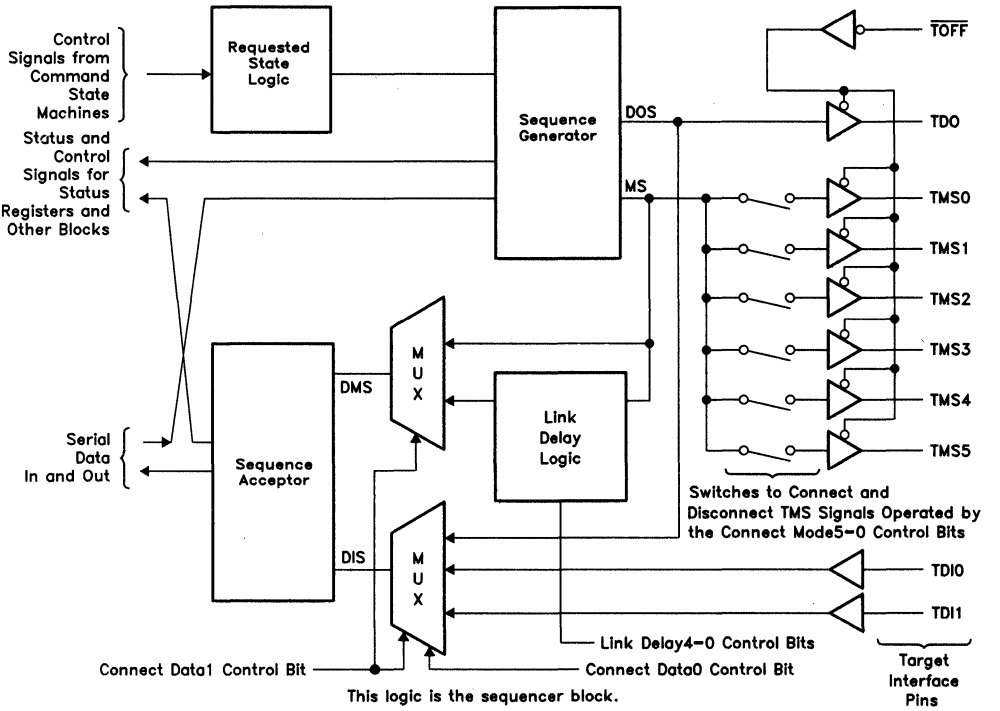

This logic is the sequencer block.

"MS" is the mode source signal.
"DMS" is the delayed-mode source signal.
"DOS" is the data-out source signal.
"DIS" is the data-in source signal.

FIGURE 8. SEQUENCE BLOCK

PRODUCT PREVIEW

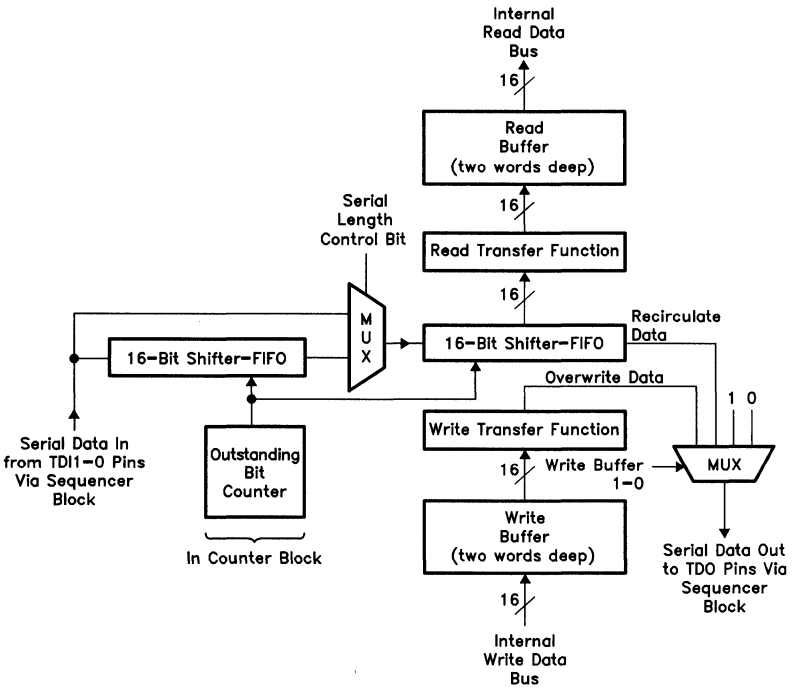

FIGURE 9. SERIAL BLOCK

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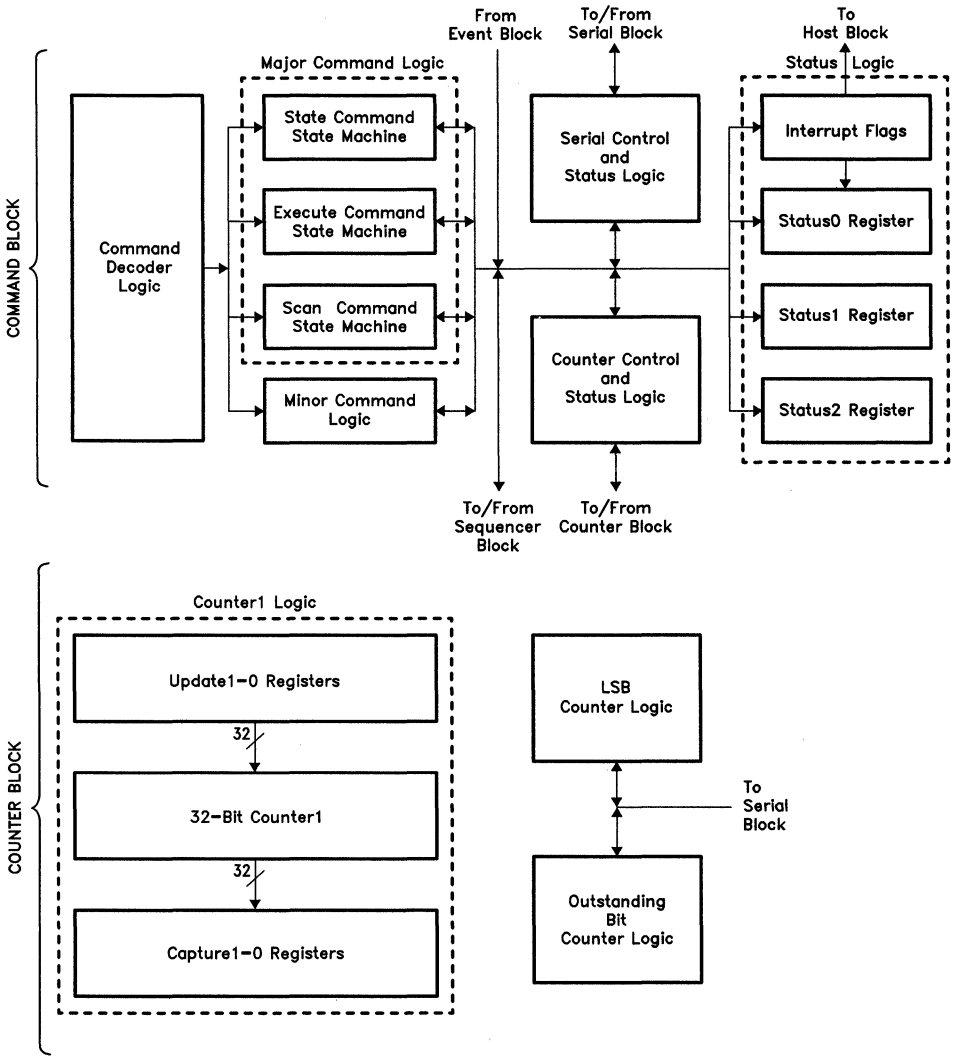

FIGURE 10. COMMAND AND COUNTER FUNCTIONS

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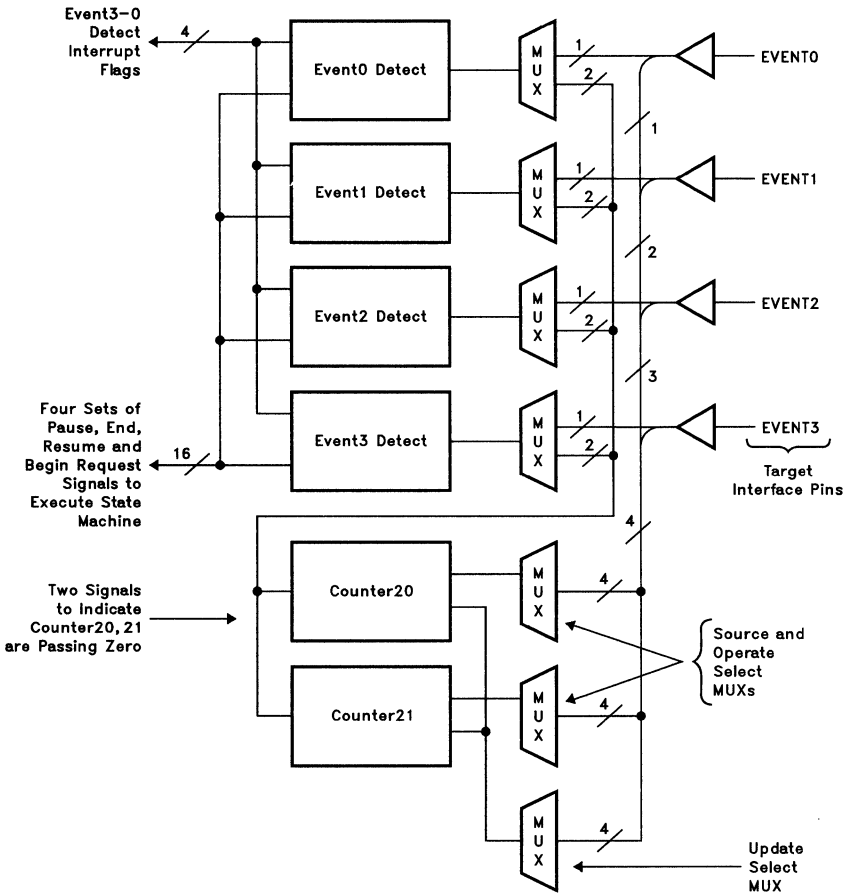


This logic is part of the event block.

FIGURE 11. EVENT DETECTORS AND COUNTERS

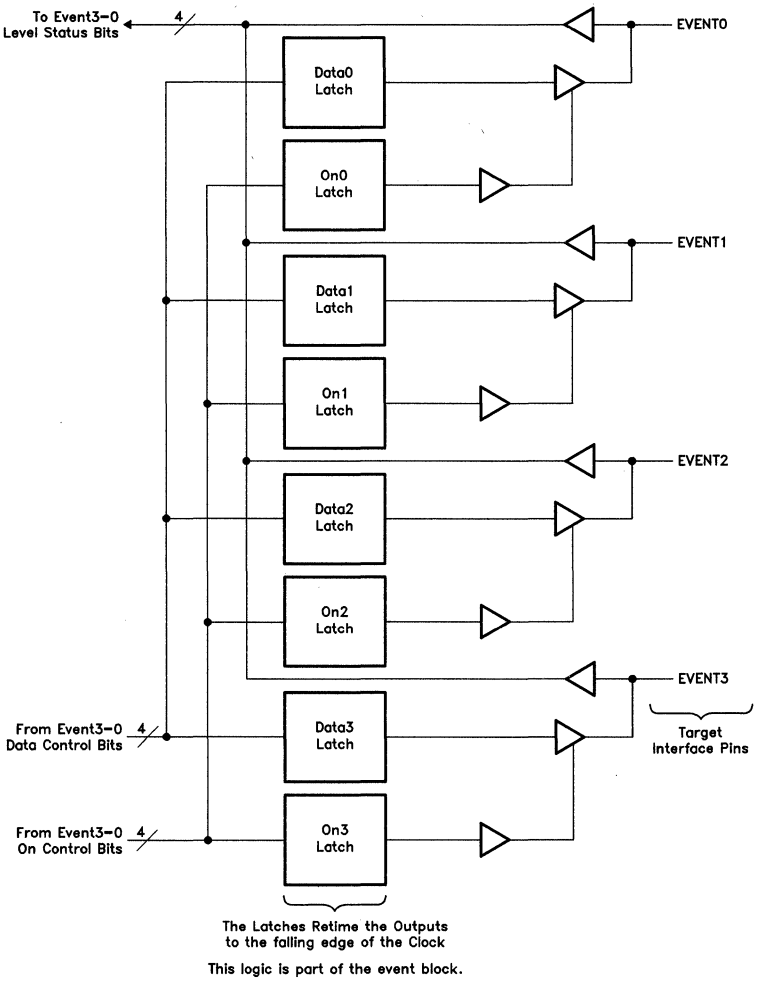


FIGURE 12. EVENT INPUT AND OUTPUT LOGIC

control functions

The control logic for the majority of the commands included in the 'ACT8990 is in the command and counter blocks (Figure 10). The command block has six sections:

- The command decode logic holds the major command opcodes while the commands are executed. It also selects which state machine to activate.
- The major command state machines are state machines for the STATE, EXECUTE and SCAN commands.

control functions (continued)

- The minor command logic generates control signals based on minor commands.
- The counter control and status logic outputs control signals and inputs status signals for the counter block.
- The serial control and status logic outputs control signals and inputs status signals for the serial block (Figure 9).
- The status logic consists of the interrupt flags and status2–0 registers.

The counter block is the counter used by the major commands. It has three sections:

- The counter1 logic consists of the counter1 update registers, counter1, and the capture registers. Signals from the command block (counter control and status logic) update and operate this counter during SCAN and EXECUTE commands.
- The LSB counter logic is two internal 4-bit counters that track the count of the least-significant bits of data sent and received during SCAN commands.
- The outstanding bit counter is an internal 6-bit counter that tracks the difference in the number of bits sent and returned during SCAN commands and temporary states sent and returned during STATE and EXECUTE commands.

data transfer functions

The data transfer logic for the SCAN command is in the serial block (see Figure 9). The serial block consists of the data buffers, shifter-FIFO, and transfer functions required by the SCAN commands. It has three sections:

- The data buffers are the read and write buffers that are each 16-bits wide and two levels deep. They are used to read recirculate data and write overwrite data during SCAN commands.
- The shifter-FIFO is a 16/32 bit shifter and 16/32-to-1 multiplexer that operates as a shifter-FIFO to send recirculate data.
- The transfer functions are a 16-to-1 multiplexer that provides the write transfer function and a partial barrel shifter and mask logic that provides the read transfer function.

target interface configuration

The reset value of the target interface is the same whether the device is in IEEE Standard 1149.1 mode or TI internal manufacturing test mode. After reset, the control registers configure the 'ACT8990 for immediate operation via the TMS1–0 pins. Changes to register values to alter the configuration should be made before major commands are executed. The register bits of concern are:

- If the machine format1–0 bits of the control3 register are 00, the target interface state machines are formatted for IEEE Standard 1149.1 operation. When 01, 10 or 11 they are configured for TI internal manufacturing test.
- If the out format1–0 bits of the control3 register are 00, the target interface pins are formatted for IEEE Standard 1149.1 operation. When 01, 10 or 11 they are configured for TI internal manufacturing test.
- If the mode format53, 42, 31 and 20 bits of the control3 register are 1, the matching TMS/EVENT pin outputs TMS signals. When 0, the pin inputs or outputs EVENT signals.

target interface internal signals

The 'ACT8990 has several important internal signals (Figure 8) that are related to those output and input on the target interface pins:

- The mode source is the test-mode-select signal that is generated internally and output on TMS5–0.
- The delayed mode source is the delayed test-mode-select signal that is generated and accepted internally.

data transfer functions (continued)

- The data out source is the test-data-out signal output on TDO or looped back to the data in source.
- The data in source is the signal selected as the test-data-in signal. It is the data out source of the sequence generator or the TDI1 or TDI0 pins.

target interface pins

The target interface timing is detailed in Figures 13 through 16. The target interface pins are as follows:

- The TCKI and TCKO pins input and output the test clock signal used by targets.
- The TDO pin is the test-data-out signal used to send data to targets.
- The TDI1–0 pins are test-data-in signals used to receive data from targets.
- The TMS5–0 pins are test-mode-select signals used to control the target test logic.
- The EVENT3–0 pins input and output extra signals.
- The $\overline{\text{TOFF}}$ pin is the test-off signal that, when low, turns the target interface output buffers off.
- The $\overline{\text{TRST}}$ pin is the test-reset signal that, when low, turns the host interface output buffers off and resets the 'ACT8990.

TMS/EVENT pins

The four TMS/EVENT pins are shared by the TMS5–2 outputs, the EVENT3–0 I/Os, and by counter20 and counter21. The mode format53, -42, -31, and -20 control bits (control3 register bits 3–0) configure these pins as TMS or EVENT signals.

When configured as TMS5–2 outputs, they can be turned off together by the mode off control bit (control3 register bit 6). They are used as TMS5–2 outputs controlled by the connect mode5–2 control bits (control2 register bits 5–2).

When configured as EVENT3–0 inputs and outputs, they can be turned off together by the event off control bit (control3 register bit 7). They are used as:

- General purpose I/O bits. Each input pin is readable from a status1 register bit. Each output buffer's data and the on/off condition is decided by the event data and the event on control bits in the control5 register. They can be used as inputs or push-pull, open-drain or open-source outputs.
- Event detectors. Each EVENT input has an event detector controlled by eight control6 or control7 register bits. They detect single synchronous or asynchronous events.
- Event counters. Counter20 and counter21 can be configured to count asynchronous edges on EVENT inputs. Passing zero may be detected by the event detectors.

target interface states

The target interface has a set of states indicated by sequences on the TMS5–0 outputs. The current state of the target interface can be read from the target interface state3–0 bits in the status2 register. These states and sequences allow the 'ACT8990 to control the target.

The target interface has two state groups:

- Temporary states are those states that the target remains in for one clock period only, then goes to one of two other states depending on the value of TMS.
- Stable states are those states that the target can remain in, or go to another state from, depending on the value of TMS.

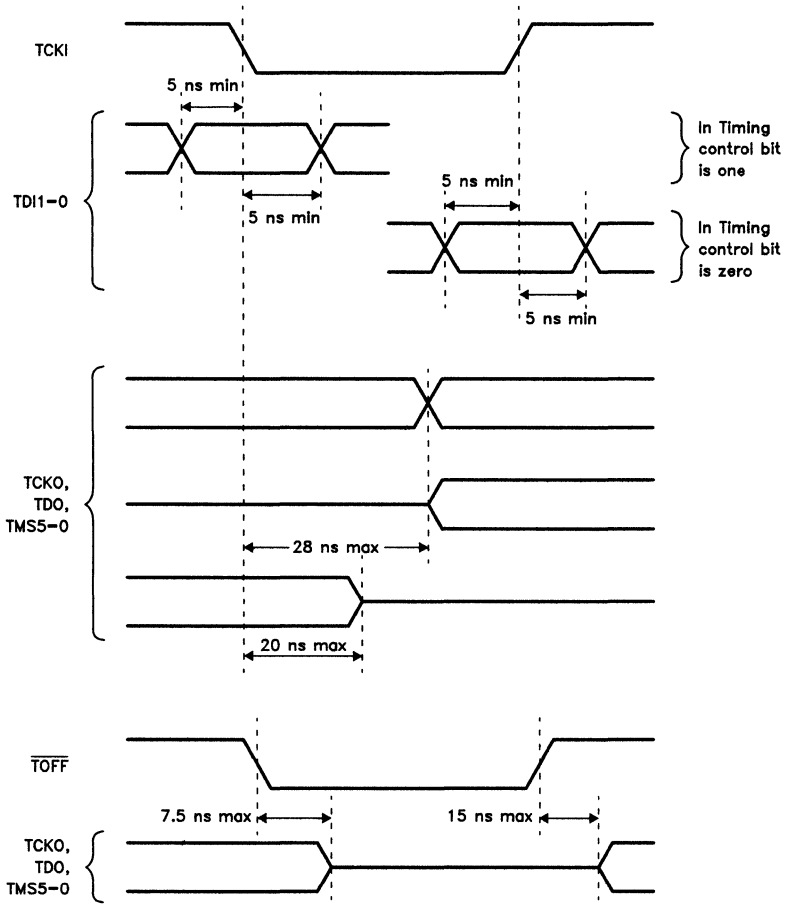


FIGURE 13. TIMING DIAGRAM

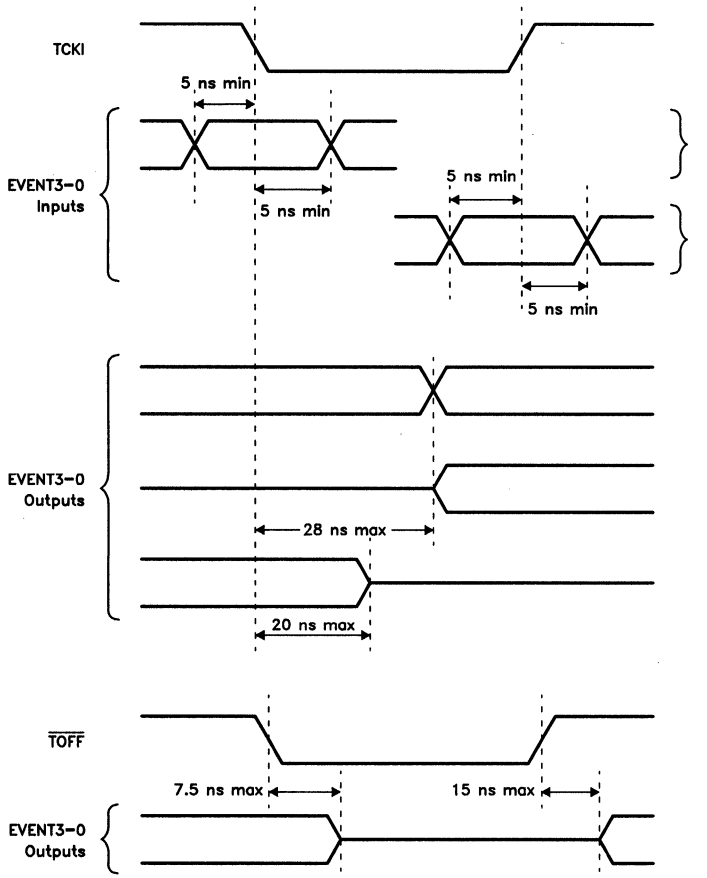


FIGURE 14. EVENT TIMING DIAGRAM

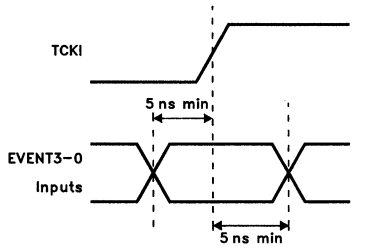


FIGURE 15. ASYNCHRONOUS EVENT TIMING DIAGRAM

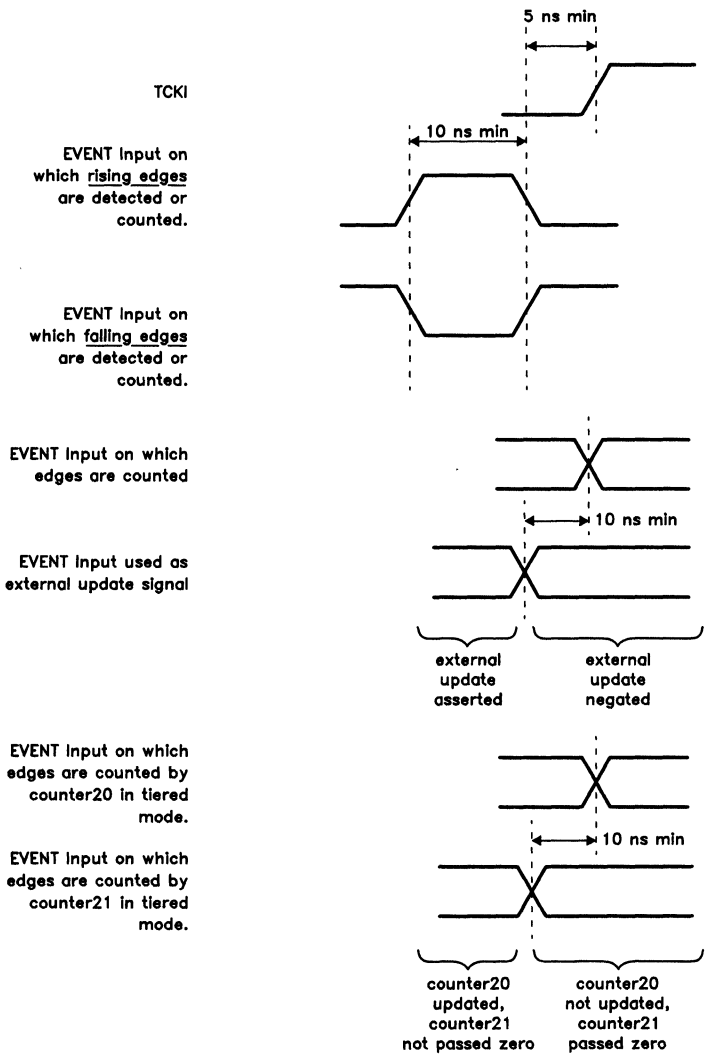


FIGURE 16. ASYNCHRONOUS EVENT EDGE TIMING DIAGRAM

event detection and counting

The detection of events occurring on the EVENT pins is either done by the event detectors alone or by counter20 and counter21 in combination with the event detectors.

event detectors

The four event detectors are shown in Figure 11. Each is controlled by eight bits in the control7 and control8 registers and has an event detect interrupt flag. Each has a matching EVENT pin on which it can detect the following:

- Synchronous events with a repetition rate less than once per 2 clock periods may be detected on the matching EVENT pin.
  - One followed by a zero (synchronous falling edge).
  - Zero followed by a one (synchronous rising edge).
  - Zero followed by a zero.
  - One followed by a one.
- Asynchronous events with a repetition rate less than once per 3 clock periods may be detected on the matching EVENT pin.
  - Falling edge.
  - Rising edge.
- Asynchronous events counted by counter20 and counter21. These counters are updated and operated in response to asynchronous levels and edges on any of the EVENT pins as configured by the control9 register. Many asynchronous events may be detected each clock period since counter updating and operation are not tied to the clock.
  - Counter20 passing zero.
  - Counter21 passing zero.

Event detection is always masked when the EVENT pin is in the output mode. It may also be selectively masked, as decided by the detect mask control bits, (control6 register bits 5 and 13) when scan, pause, and the associated temporary states (capture, exit1, and exit2) are returned.

When an event is detected, the following actions may occur:

- Interrupt requests may be issued to the host by setting an event detect flag.
- EXECUTE commands may be affected by setting the suspend, end, resume, or begin request status bits (status1 register bits 8–11).
- Counter1 may be operated.

event counters

Counter20 and counter21 are asynchronous 16-bit counters as shown in Figure 11. They are configured by bits in the control9 register. They are used to count asynchronous events on the EVENT pins. Counter20 or counter21 passing zero may be detected by an event detector that can request an EXECUTE command to suspend, end, resume, or begin. They can also be used independently of commands.

The counter2 update registers are used to load the counters with initial values. These counters have no capture registers, so their values cannot be read by the host. Reset causes counter20, counter21 and their update registers to be filled with zeroes.

Because these counters are asynchronous, changes in the values of the control9 register bits may create logical hazards that, in turn, cause spurious operation of the counters. This can be avoided by holding them in the update condition during configuration changes. The update inverted control bits are set to zero and the other bits are changed, then the update inverted bits are set to one.

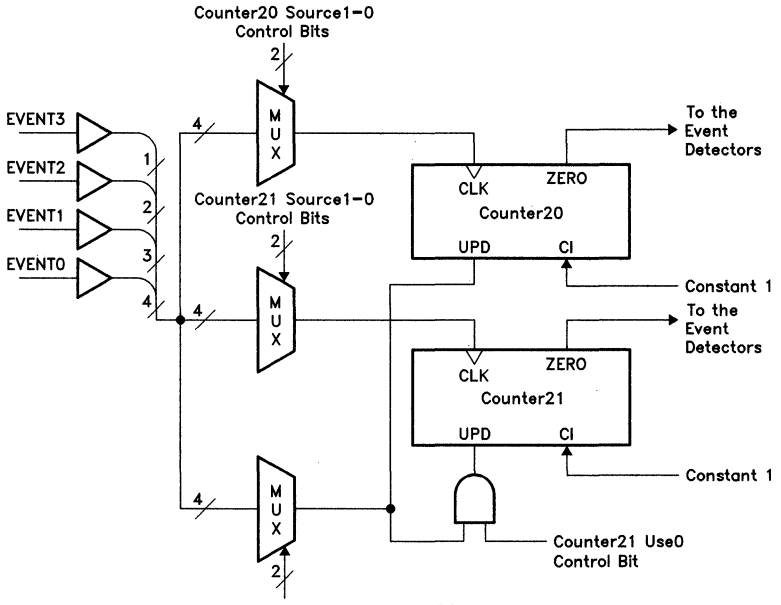
event detection and counting (continued)

The event counters are updated from the counter2 update registers as follows:

- Both counters are loaded by an OPERATE2 command before EXECUTE commands are begun.
- Either counter20 only, or both counter20 and counter21, are loaded by an external update. This is a selected level on an EVENT as configured by the external update enable, polarity and source1–0 control bits.
- When their individual update inverted control bits are zero.
- By the 'ACT8990 if their individual reload control bits are set when the counter passes zero.

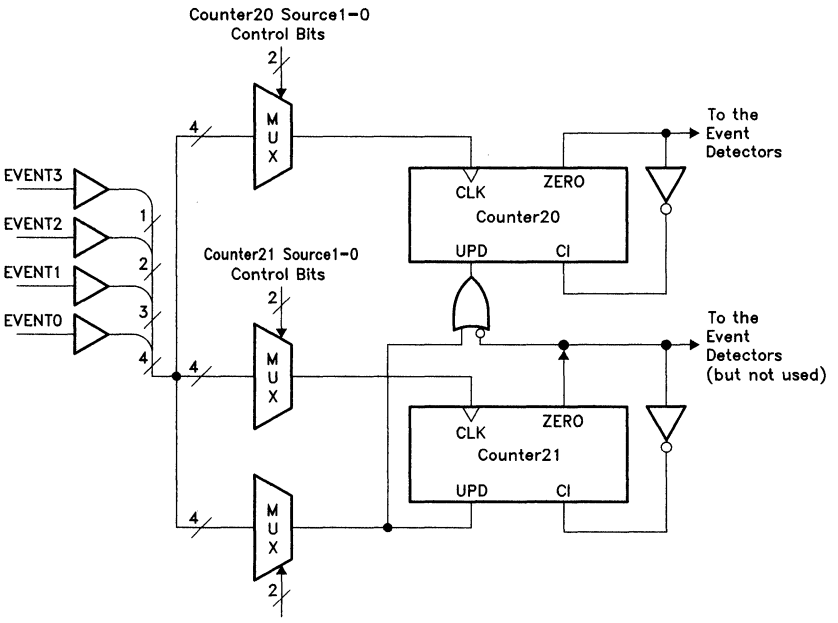
The event counters are incremented when a selected edge on an EVENT pin occurs, as configured by their individual reload, operate and source1–0 control bits. Also, they are used as separate or tiered 16-bit counters or concatenated as one 32-bit counter as selected by the counter2 use1–0 control bits (control9 register bits 10–9):

- Separate use means events are counted as decided by the control9 register and OPERATE2 command bits. They are independent 16-bit counters (see Figure 17).
- Tiered use is similar to separate use except that counter20 is held updated until the first time counter21 passes zero (see Figure 18).
- Concatenated use means events are counted as decided by the control9 register and OPERATE2 command bits only. They are a single 32-bit counter (see Figure 19).



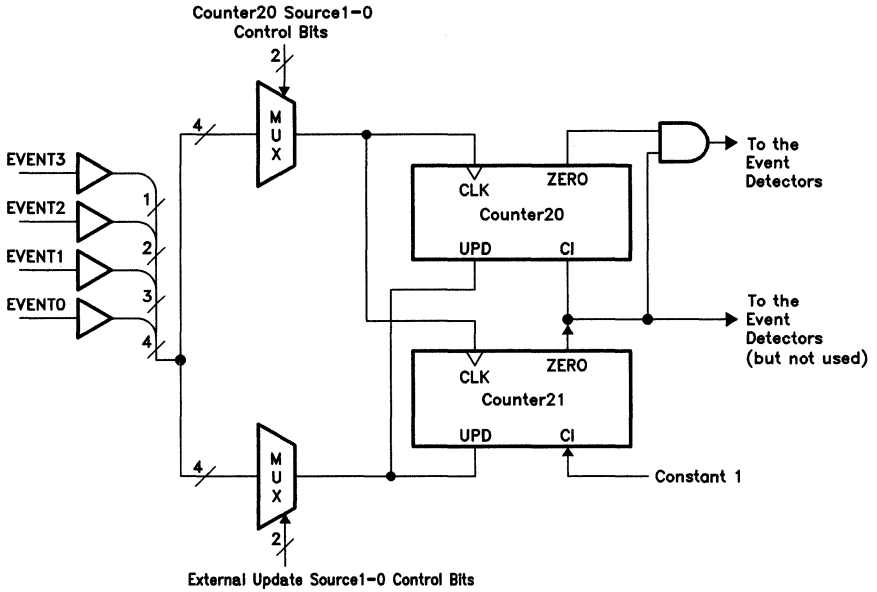
CLK is the counter clock input.
UPD is the counter asynchronous update input.
CI is the counter carry input.
ZERO is the counter passing-zero output.

FIGURE 17. SEPARATE USE OF COUNTER20 AND COUNTER21



CLK is the counter clock input
UPD is the counter asynchronous update input
CI is the counter carry input
ZERO is the counter passing-zero output

FIGURE 18. TIERED USE OF COUNTER20 AND COUNTER21



CLK is the counter clock input
UPD is the counter asynchronous update input
CI is the counter carry input
ZERO is the counter passing–zero output

FIGURE 19. CONCATENATED USE OF COUNTER20 AND COUNTER21

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register listing

ADRS4–0	REGISTER NAME	REGISTER USAGE	ACCESSIBILITY
00000	Control0	Interrupt enable control	Read-write
00001	Control1	Host and test control	Read-write
00010	Control2	Target interface control	Read-write
00011	Control3	Target interface control	Read-write
00100	Control4	Target interface control	Read-write
00101	Control5	Event output control	Read-write
00110	Control6	Event detector control	Read-write
00111	Control7	Event detector control	Read-write
01000	Control8	Counter1 control	Read-write
01001	Control9	Counter20/Counter21 control	Read-write
01010	Minor Command	Minor commands	Read-write
01011	Major Command	Major commands	Read-write
01100	Counter1 Update0	Counter1 update	Read-write
01101	Counter1 Update1	Counter1 update	Read-write
01110	Counter2 Update0	Counter20 update	Read-write
01111	Counter2 Update1	Counter21 update	Read-write
10000	Status0	Interrupt flag status	Read-only
10001	Status1	Status capture	Read-only
10010	Status2	Status capture	Read-only
10011	Status3	Null	Read-only
10100	Capture0	Counter1 capture	Read-only
10101	Capture1	Counter1 capture	Read-only
10110	Read Buffer	Read buffer	Read-only
10111	Write Buffer	Write buffer	Write-only

control0 register bits

BIT	DESCRIPTION
0	Event0 Detect Enable
1	Event1 Detect Enable
2	Event2 Detect Enable
3	Event3 Detect Enable
4	Counter1 Execute Enable
5	Counter1 Scan Enable
6	Null
7	Null
8	Suspend Enable
9	End Enable
10	Resume Enable
11	Begin Enable
12	Buffer Error Enable
13	Buffer Ready Enable
14	Abort Enable
15	Finish Enable

control0 register bit description

The control0 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control0 register address (from ADRS4–ADRS0) is 00000.

event0 detect enable
The status of this bit determines if an interrupt is asserted when the event0 detect flag is set.
0 No interrupt is asserted.
1 An interrupt is asserted.

event1 detect enable
The status of this bit determines if an interrupt is asserted when the event1 detect flag is set.
0 No interrupt is asserted.
1 An interrupt is asserted.

event2 detect enable
The status of this bit determines if an interrupt is asserted when the event2 detect flag is set.
0 No interrupt is asserted.
1 An interrupt is asserted.

event3 detect enable
The status of this bit determines if an interrupt is asserted when the event3 detect flag is set.
0 No interrupt is asserted.
1 An interrupt is asserted.

counter1 execute enable
The status of this bit determines if an interrupt is asserted when the counter1 execute flag is set.
0 No interrupt is asserted.
1 An interrupt is asserted.

counter1 scan enable
The status of this bit determines if an interrupt is asserted when the counter1 scan flag is set.
0 No interrupt is asserted.
1 An interrupt is asserted.

suspend enable
The status of this bit determines if an interrupt is asserted when the suspend flag is set.
0 No interrupt is asserted.
1 An interrupt is asserted.

end enable
The status of this bit determines if an interrupt is asserted when the end flag is set.
0 No interrupt is asserted.
1 An interrupt is asserted.

resume enable
The status of this bit determines if an interrupt is asserted when the resume flag is set.
0 No interrupt is asserted.
1 An interrupt is asserted.

control0 register bit description (continued)

begin enable
The status of this bit determines if an interrupt is asserted when the begin flag is set.
0 No interrupt is asserted.
1 An interrupt is asserted.

buffer error enable
The status of this bit determines if an interrupt is asserted when the buffer error flag is set.
0 No interrupt is asserted.
1 An interrupt is asserted.

buffer ready enable
The status of this bit determines if an interrupt is asserted when the buffer ready flag is set.
0 No interrupt is asserted.
1 An interrupt is asserted.

abort enable
The status of this bit determines if an interrupt is asserted when the abort flag is set.
0 No interrupt is asserted.
1 An interrupt is asserted.

finish enable
The status of this bit determines if an interrupt is asserted when the finish flag is set.
0 No interrupt is asserted.
1 An interrupt is asserted.

control1 register bits

BIT	DESCRIPTION
0	Observe Enable0
1	Observe Enable1
2	Capture Enable0
3	Capture Enable1
4	Unused
5	Unused
6	Unused
7	Unused
8	Serial Data Test
9	Link Delay Test
10	Serial Buffer Test
11	Counter Test
12	Flag Test
13	Unused
14	Unused
15	Unused

control1 register bit description

The control1 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control1 register address (from ADRS4–ADRS0) is 00001.

This register holds the control bits for the host interface and the manufacturing test functions. The bits in the upper byte must not be set when any major command is alive.

control1 register bit description (continued)

observe enable0
This bit enables the reading of the observe3–0 registers via the status3–0 register locations. The observe2–0 registers make key internal flip-flops observable for manufacturing test. The observe3 register makes the design revision number observable for manufacturing test and normal operation.
0 Normal operation.
1 Observe enabled.

observe enable1
This bit enables the reading of the observe5–4 registers via the capture1–0 register locations. These observe registers make the values of counter20 and counter21 observable for manufacturing test.
0 Normal operation.
1 Observe enabled.

capture enable0
This bit enables continuous capturing of the status3–0 registers for normal operation and manufacturing test.
0 Normal operation.
1 Capture enabled.

capture enable1
This bit enables continuous capturing of the capture1-0 registers for normal operation and manufacturing test.
0 Normal operation.
1 Capture enabled.

serial data test
This bit configures the shifter-FIFO, LSB counters, outstanding bit counter, and write and recirculate multiplexers for normal operation or manufacturing test.
0 Normal operation.
1 Enable manufacturing test.

link delay test
This bit configures the link delay register for normal operation or manufacturing test.
0 Normal operation.
1 Enable manufacturing test.

control1 register bit description (continued)

serial buffer test

This bit configures the write buffers, shifter-FIFO, read transfer functions, and read buffer for manufacturing test.

0 Normal operation.
1 Enable manufacturing test.

counter test

This bit configures counter1 and counter20/21 for manufacturing test.

0 Normal operation.
1 Enable manufacturing test.

flag test

This bit configures the interrupt- and the execute-command request flags for manufacturing test.

0 Normal operation.
1 Enable manufacturing test.

control2 register bits

BIT	DESCRIPTION
0	Connect Mode0
1	Connect Mode1
2	Connect Mode2
3	Connect Mode3
4	Connect Mode4
5	Connect Mode5
6	Null
7	Null
8	Null
9	Null
10	Null
11	Null
12	Null
13	Null
14	Null
15	Null

control2 register bit description

The control2 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control2 register address (from ADRS4–ADRS0) is 00010.

connect mode0
The status of this bit determines if TMS0 is connected to the mode source.
0 The mode source is disconnected from TMS0, whose value remains constant.
1 The mode source is connected to TMS0, whose value follows that of the mode source.

connect mode1
The status of this bit determines if TMS1 is connected to the mode source.
0 The mode source is disconnected from TMS1, whose value remains constant.
1 The mode source is connected to TMS1, whose value follows that of the mode source.

connect mode2
The status of this bit determines if TMS2 is connected to the mode source.
0 The mode source is disconnected from TMS2, whose value remains constant.
1 The mode source is connected to TMS2, whose value follows that of the mode source.

connect mode3
The status of this bit determines if TMS3 is connected to the mode source.
0 The mode source is disconnected from TMS3, whose value remains constant.
1 The mode source is connected to TMS3, whose value follows that of the mode source.

connect mode4
The status of this bit determines if TMS4 is connected to the mode source.
0 The mode source is disconnected from TMS4, whose value remains constant.
1 The mode source is connected to TMS4, whose value follows that of the mode source.

connect mode5
The status of this bit determines if TMS5 is connected to the mode source.
0 The mode source is disconnected from TMS5, whose value remains constant.
1 The mode source is connected to TMS5, whose value follows that of the mode source.

control3 register bits

BIT	DESCRIPTION
0	Mode Format20
1	Mode Format31
2	Mode Format42
3	Mode Format53
4	Clock Off
5	Data Off
6	Mode Off
7	Event Off
8	Out Format0
9	Out Format1
10	Machine Format0
11	Machine Format1
12	Clock Data
13	Clock Format
14	Null
15	Null

control3 register bit description

The control3 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control3 register address (from ADRS4–ADRS0) is 00011.

This register holds the format control bits that select the target interface output signals and turns their output buffers off and on. The clock off bit has precedence over the clock data and format bits. The TCKO pin control logic is designed so that changes in the values of the clock off, data, and format bits cause hazard-free changes in the configuration of the TCKO pin.

mode format20
This bit configures the TMS2/EVENT0 pin to be an EVENT input/output or a TMS output.
0 EVENT input/output.
1 TMS output.

mode format31
This bit configures the TMS3/EVENT1 pin to be an EVENT input/output or a TMS output.
0 EVENT input/output.
1 TMS output.

mode format42
This bit configures the TMS4/EVENT2 pin to be an EVENT input/output or a TMS output.
0 EVENT input/output.
1 TMS output.

mode format53
This bit configures the TMS5/EVENT3 pin to be an EVENT input/output or a TMS output.
0 EVENT input/output.
1 TMS output.

The changes in the state of the output pins caused by the clock, data mode, and event off bits are clean; spurious signal values do not occur.

clock off
This bit turns the TCKO output on or off.
0 On.
1 Off.

control3 register bit description (continued)

data off
This bit turns the TDO output on or off.
0 On.
1 Off.

mode off
This bit turns all pins operating as TMS outputs on or off.
0 On.
1 Off.

event off
This bit turns all pins operating as EVENT outputs on or off.
0 On.
1 Off.

out format1–0
These bits decide the format of several target interface outputs. The effect on the TMS1-0 pins is:
00 They output the TMS signal for IEEE Standard 1149.1 operation.
01 They output other signals for TI internal manufacturing test mode.
10 They output other signals for TI internal manufacturing test mode.
11 They output other signals for TI internal manufacturing test mode.

The effect on the TDO pin is:
00 It outputs data in the Shift-DR and Shift-IR states, and outputs the logic high level in other states for IEEE Standard 1149.1 operation.
01 It outputs data in the Shift-DR and Shift-IR states, and outputs the logic high level in other states for TI internal manufacturing test mode.
10 It outputs data in the Shift-DR and Shift-IR states, and outputs the logic high level in other states for TI internal manufacturing test mode.
11 It outputs data in the Shift-DR and Shift-IR states, and outputs the logic high level in other states for TI internal manufacturing test mode.

machine format1–0
These bits decide the format of the sequencer block state machines.
00 The sequencer block state machines state diagram is that of IEEE Standard 1149.1.
01 The sequencer block state machines state diagram is that required by TI internal manufacturing test mode.
10 The sequencer block state machines state diagram is that required by TI internal manufacturing test mode.
11 The sequencer block state machines state diagram is that required by TI internal manufacturing test mode.

clock data
This bit selects the output level on the TCKO pin when the clock format bit is one.
0 A constant zero is output.
1 A constant one is output.

clock format
This bit configures the TCKO pin to output either the clock or a logic level determined by the clock data bit.
0 The clock is output.
1 A level is output.

control4 register bits

BIT	DESCRIPTION
0	Link Delay0
1	Link Delay1
2	Link Delay2
3	Link Delay3
4	Link Delay4
5	Serial Length
6	Connect Data0
7	Connect Data1
8	Write Buffer0
9	Write Buffer1
10	Read Buffer
11	Transfer Format
12	In Timing0
13	In Timing1
14	Null
15	Null

control4 register bit description

The control4 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control4 register address (from ADRS4–ADRS0) is 00100.

link delay 4–0

These bits decide the length of the link delay register. The mode source is passed through the link delay register to generate a delayed-mode source which allows the 'ACT8990 internal functions to decode the TDI and EVENT signals. The length of the link delay register is set by the host to match the length of the direct or retimed link. If the link is direct, then these 5 bits are set to all zeroes. If the link is retimed, then these bits are set to a binary value equal to the number of clock cycles by which the mode source is to be delayed.

serial length

This bit configures the shifter-FIFO length as 16 or 32 bits.

0 16 bits.
1 32 bits.

connect data1–0

These bits select the data-in source to be used as either the data-out source for loopback operation or one of the TDI1-0 inputs.

00–01 The data-out source is used as the data-in source and the TDI1–0 inputs are ignored. The connect mode bits are ignored and the TMS outputs are disconnected from the mode source and hold their prior values. The link delay bits are ignored and the link delay register is bypassed, so a zero link delay is used.
10 The TDI0 input is the data-in source; the TDI1 input is ignored.
11 The TDI1 input is the data-in source; the TDI0 input is ignored.

write buffer1–0

This bit selects the write buffer option. Options 00 and 01 provide an efficient way of sending the BYPASS and EXTEST instructions. Option 10 provides an efficient way of bypassing strings that are of no interest. In option 11 the write buffer is used.

control4 register bit description (continued)

00 Send zeroes.
01 Send ones.
10 Send recirculate data from the shifter-FIFO.
11 Send overwrite data from the write buffer.

read buffer

This bit selects the read buffer option. In option 1, the read buffer is used.

0 Ignore receive data.
1 Read receive data into the read buffer.

transfer format

This bit selects the data format used by the transfer functions.

0 LSB-first format.
1 MSB-first format.

in timing0

This bit configures the TDI1–0 inputs to be sampled on the falling or rising edge of TCKI. Together with the use of TCKI or TCKO as the clock for the target devices, this simplifies the connections of the 'ACT8990 to targets operating at high clock rates.

0 Rising edge.
1 Falling edge.

in timing1

This bit configures the EVENT3–0 inputs to be sampled on the falling or rising edge of TCKI. Together with the use of TCKI or TCKO as the clock for the target devices, this simplifies the connections of the 'ACT8990 to targets operating at high clock rates.

0 Rising edge.
1 Falling edge.

control5 register bits

BIT	DESCRIPTION
0	Event0 Data
1	Event1 Data
2	Event2 Data
3	Event3 Data
4	Null
5	Null
6	Null
7	Null
8	Event0 On
9	Event1 On
10	Event2 On
11	Event3 On
12	Null
13	Null
14	Null
15	Null

control5 register bit description

The control5 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control5 register address (from ADRS4–ADRS0) is 00101.

control5 register bit description (continued)

This register holds the control bits for the four EVENT pin output buffers.

event0 data
This bit determines the EVENT0 value when the output buffer is on.
0 Zero.
1 One.

event1 data
This bit determines the EVENT1 value when the output buffer is on.
0 Zero.
1 One.

event2 data
This bit determines the EVENT2 value when the output buffer is on.
0 Zero.
1 One.

event3 data
This bit determines the EVENT3 value when the output buffer is on.
0 Zero.
1 One.

event0 on
This bit determines whether the EVENT0 output buffer is off or on.
0 Off.
1 On.

event1 on
This bit determines whether the EVENT1 output buffer is off or on.
0 Off.
1 On.

event2 on
This bit determines whether the EVENT2 output buffer is off or on.
0 Off.
1 On.

event3 on
This bit determines whether the EVENT3 output buffer is off or on.
0 Off.
1 On.

control6 register bits

BIT	DESCRIPTION
0	Detect0 Suspend
1	Detect0 End
2	Detect0 Resume
3	Detect0 Begin
4	Detect0 Sync
5	Detect0 Mask
6	Detect0 Select0
7	Detect0 Select1
8	Detect1 Suspend
9	Detect1 End
10	Detect1 Resume
11	Detect1 Begin
12	Detect1 Sync
13	Detect1 Mask
14	Detect1 Select0
15	Detect1 Select1

control6 register bit description

The control6 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control6 register address (from ADRS4–ADRS0) is 00110.

No more than one bit in each group of suspend, end, resume, and begin bits should be set at any time. Such a configuration has no application, as it causes several conflicting request flags to be set when an event is detected.

detect0 suspend
This bit determines whether event detection sets the suspend request flag and so may cause EXECUTE commands to suspend.
0 No.
1 Yes.

detect0 end
This bit determines whether event detection sets the end request flag and so may cause EXECUTE commands to end.
0 No.
1 Yes.

detect0 resume
This bit determines whether event detection sets the resume request flag and so may cause EXECUTE commands to resume.
0 No.
1 Yes.

detect0 begin
This bit determines whether event detection sets the begin request flag and so may cause EXECUTE commands to begin.
0 No.
1 Yes.

detect0 sync
This bit selects asynchronous or synchronous event detection.
0 Asynchronous.
1 Synchronous.

control6 register bit description (continued)

detect0 mask
This bit determines whether event detection is masked when scan, pause, and the associated temporary states Capture-DR, Exit1-DR, Exit2-DR, Capture-IR, Exit1-IR and Exit2-IR are returned.
0 Not masked.
1 Masked.

detect0 select1–0
These bits select the event to be detected.

If the detect0 sync bit is zero:
00 A falling edge on EVENT0.
01 A rising edge on EVENT0.
10 Counter20 passing zero.
11 Counter21 passing zero.

If the detect0 sync bit is one:
00 A one, then zero on EVENT0.
01 A zero, then one on EVENT0.
10 A zero, then zero on EVENT0.
11 A one, then one on EVENT0.

detect1 suspend
This bit determines whether event detection sets the suspend request flag and so may cause EXECUTE commands to suspend.
0 No.
1 Yes.

detect1 end
This bit determines whether event detection sets the end request flag and so may cause EXECUTE commands to end.
0 No.
1 Yes.

detect1 resume
This bit determines whether event detection sets the resume request flag and so may cause EXECUTE commands to resume.
0 No.
1 Yes.

detect1 begin
This bit determines whether event detection sets the begin request flag and so may cause EXECUTE commands to begin.
0 No.
1 Yes.

detect1 sync
This bit selects asynchronous or synchronous event detection.
0 Asynchronous.
1 Synchronous.

detect1 mask
This bit determines whether event detection is masked when scan, pause, and the associated temporary states Capture-DR, Exit1-DR, Exit2-DR, Capture-IR, Exit1-IR and Exit2-IR are returned.
0 Not masked.
1 Masked.

control6 register bit description (continued)

detect1 select1–0
These bits select the event to be detected.

If the detect1 sync bit is zero:
00 A falling edge on EVENT1.
01 A rising edge on EVENT1.
10 Counter20 passing zero.
11 Counter21 passing zero.

If the detect1 sync bit is one:
00 A one, then zero on EVENT1.
01 A zero, then one on EVENT1.
10 A zero, then zero on EVENT1.
11 A one, then one on EVENT1.

control7 register bits

BIT	DESCRIPTION
0	Detect2 Suspend
1	Detect2 End
2	Detect2 Resume
3	Detect2 Begin
4	Detect2 Sync
5	Detect2 Mask
6	Detect2 Select0
7	Detect2 Select1
8	Detect3 Suspend
9	Detect3 End
10	Detect3 Resume
11	Detect3 Begin
12	Detect3 Sync
13	Detect3 Mask
14	Detect3 Select0
15	Detect3 Select1

control7 register bit description

The control7 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control7 register address (from ADRS4–ADRS0) is 00111.

No more than one bit in each group of suspend, end, resume, and begin bits should be set at any time. Such a configuration has no application, as it causes several conflicting request flags to be set when an event is detected.

detect2 suspend
This bit determines whether event detection sets the suspend request flag and so may cause EXECUTE commands to suspend.
0 No.
1 Yes.

detect2 end
This bit determines whether event detection sets the end request flag and so may cause EXECUTE commands to end.
0 No.
1 Yes.

control7 register bit description (continued)

detect2 resume
This bit determines whether event detection sets the resume request flag and so may cause EXECUTE commands to resume.
0 No.
1 Yes.

detect2 begin
This bit determines whether event detection sets the begin request flag and so may cause EXECUTE commands to begin.
0 No.
1 Yes.

detect2 sync
This bit selects asynchronous or synchronous event detection.
0 Asynchronous.
1 Synchronous.

detect2 mask
This bit determines whether event detection is masked when scan, pause, and the associated temporary states Capture-DR, Exit1-DR, Exit2-DR, Capture-IR, Exit1-IR and Exit2-IR are returned.
0 Not masked.
1 Masked.

detect2 select1–0
These bits select the event to be detected.

If the detect2 sync bit is zero:
00 A falling edge on EVENT2.
01 A rising edge on EVENT2.
10 Counter20 passing zero
11 Counter21 passing zero.

If the detect2 sync bit is one:
00 A one, then zero on EVENT2.
01 A zero, then one on EVENT2.
10 A zero, then zero on EVENT2.
11 A one, then one on EVENT2.

detect3 suspend
This bit determines whether event detection sets the suspend request flag and so may cause EXECUTE commands to suspend.
0 No.
1 Yes.

detect3 end
This bit determines whether event detection sets the end request flag and so may cause EXECUTE commands to end.
0 No.
1 Yes.

detect3 resume
This bit determines whether event detection sets the resume request flag and so may cause EXECUTE commands to resume.
0 No.
1 Yes.

control7 register bit description (continued)

detect3 begin
This bit determines whether event detection sets the begin request flag and so may cause EXECUTE commands to begin.
0 No.
1 Yes.

detect3 sync
This bit selects asynchronous or synchronous event detection.
0 Asynchronous.
1 Synchronous.

detect3 mask
This bit determines whether event detection is masked when scan, pause, and the associated temporary states Capture-DR, Exit1-DR, Exit2-DR, Capture-IR, Exit1-IR and Exit2-IR are returned.
0 Not masked.
1 Masked.

detect3 select1–0
These bits select the event to be detected.

If the detect3 sync bit is zero:
00 A falling edge on EVENT3.
01 A rising edge on EVENT3.
10 Counter20 passing zero
11 Counter21 passing zero.

If the detect3 sync bit is one:
00 A one, then zero on EVENT3.
01 A zero, then one on EVENT3.
10 A zero, then zero on EVENT3.
11 A one, then one on EVENT3.

control8 register bits

BIT	DESCRIPTION
0	Counter1 Suspend
1	Counter1 End
2	Counter1 Reload
3	Counter1 Operate0
4	Counter1 Operate1
5	Counter1 Operate2
6	Counter1 Source0
7	Counter1 Source1
8	Unused
9	Unused
10	Unused
11	Unused
12	Unused
13	Unused
14	Unused
15	Unused

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control8 register bit description

The control8 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control8 register address (from ADRS4–ADRS0) is 01000.

counter1 suspend
This bit determines whether the counter passing zero sets the suspend request flag and so may cause EXECUTE commands to suspend.

0 No.
1 Yes.

counter1 end
This bit determines whether the counter passing zero sets the end request flag and so may cause EXECUTE commands to end.

0 No.
1 Yes.

counter1 reload
This bit determines whether the counter is loaded from its update register or decremented to all ones when it passes zero.

0 It is decremented to the value of all ones.
1 It is loaded from its update register.

counter1 operate2–0
These bits determine when the counter is operated. If based on an event detector or EVENT pin, the counter1 source1–0 bits select the particular pin.

000 It is not operated at any time.
001 It is not operated at any time.
010 Whenever EXECUTE commands send execute states.
011 Whenever EXECUTE commands are alive.
100 By an event detector.
101 By an event detector.
110 By a logic low level on an EVENT pin.
111 By a logic high level on an EVENT pin.

counter1 source1–0
These bits determine which EVENT pin level or event detection operates the counter when selected by counter1 operate2–0.

00 EVENT0 or event detector0.
01 EVENT1 or event detector1.
10 EVENT2 or event detector2.
11 EVENT3 or event detector3.

control9 register bits

BIT	DESCRIPTION
0	External Update Polarity
1	External Update Source0
2	External Update Source1
3	Counter20 Update Inverted
4	Counter20 Reload
5	Counter20 Operate
6	Counter20 Source0
7	Counter20 Source1
8	External Update Enable
9	Counter2 Use0
10	Counter2 Use1
11	Counter21 Update Inverted
12	Counter21 Reload
13	Counter21 Operate
14	Counter21 Source0
15	Counter21 Source1

control9 register bit description

The control9 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control9 register address (from ADRS4–ADRS0) is 01001.

external update polarity
This bit determines whether logic low or high level on an EVENT pin causes the external updating.
0 Logic low.
1 Logic high.

external update source1–0
These bits determine which EVENT pin externally updates the counter.
00 EVENT0 is used.
01 EVENT1 is used.
10 EVENT2 is used.
11 EVENT3 is used.

counter20 update inverted
This bit determines whether the counter is updated from its update register.
0 It is updated.
1 It is not updated.

counter20 reload
This bit determines whether the counter is loaded from its update register or decremented to all ones when it passes zero.
0 It is decremented to the value of all ones.
1 It is loaded from its update register.

counter20 operate
This bit determines when the counter is operated by an EVENT pin as selected by counter20 source1–0.
0 It is operated by falling edges.
1 It is operated by rising edges.

control9 register bit description (continued)

counter20 source1–0
These bits determine which EVENT pin operates the counter.
00 EVENT0 is used.
01 EVENT1 is used.
10 EVENT2 is used.
11 EVENT3 is used.

external update enable
This bit determines whether the counters may be externally updated from their update registers asynchronously by an EVENT pin.
0 They may not be updated asynchronously.
1 They may be updated asynchronously.

counter2 use1–0
These bits determine whether counter20 and counter21 are used as separate or tiered 16-bit counters or concatenated as one 32-bit counter.
00 or 01 Separate counters.
10 Tiered counters.
11 Concatenated counters.

These bits also decide if counter20 only or both counter20 and counter21 may be updated asynchronously by a signal on an event pin.
00 Only counter20 may be externally updated.
01, 10, or
11 Both counter20 and counter21 may be externally updated.

counter21 update inverted
This bit determines whether the counter is updated from its update register.
0 It is updated.
1 It is not updated.

counter21 reload
This bit determines whether the counter is loaded from its update register or decremented to all ones when it passes zero.
0 It is decremented to the value of all ones.
1 It is loaded from its update register.

counter21 operate
This bit determines when the counter is operated by an EVENT pin as selected by counter21 source1–0.
0 It is operated by falling edges.
1 It is operated by rising edges.

counter21 source1–0
These bits determine which EVENT pin operates the counter.
00 EVENT0 is used.
01 EVENT1 is used.
10 EVENT2 is used.
11 EVENT3 is used.

minor command register bits

BIT	DESCRIPTION
0	Minor Opcode0
1	Minor Opcode1
2	Minor Opcode2
3	Minor Opcode3
4	Minor Opcode4
5	Minor Opcode5
6	Minor Opcode6
7	Minor Opcode7
8	Null
9	Null
10	Null
11	Null
12	Minor Opcode12
13	Minor Opcode13
14	Minor Opcode14
15	Minor Opcode15

minor command register bit description

The minor command register is set by the host to select a particular minor command to be executed and to direct its operations while it is alive. The bits are not altered by the device. The minor command register address (from ADRS4–ADRS0) is 01010.

The act of writing to the minor command register causes the selected minor command to begin.

The minor commands require only a few clock periods to complete their operations, during which the $\overline{\text{RDY}}$ pin is asserted. They do not affect the awake and alive status bits during their operations. They do not affect the finish interrupt flag when they finish.

Note that the operate0/1 minor commands are used to begin the major command selected by the value of the major command register.

minor opcode7–0
The minor opcode7–0 bits specify options for the command.

minor opcode15–12
The minor opcode15–12 bits select the minor command:

0000 Select a CLEAR0 command.
0001 Select a CLEAR1 command.
0010 Select a SET0 command.
0011 Select a SET1 command.
0100 Select an OPERATE0 command.
0101 Select an OPERATE1 command.
0110 Select an OPERATE2 command.
0111 Select a RESET command.
1XXX No effect.

minor command register bit description (continued)

CLEAR0

This command is used to selectively clear the interrupt flags in the lower byte (bits 7–0) of the status0 register.

The CLEAR0 command is selected by minor opcode15–12 bits = 0000.

The minor opcode7–0 bits specify options for the command. If a bit is zero, then the specified option is not selected.

7	Unused.
6	Unused.
5	Clear the interrupt flag in bit 5.
4	Clear the interrupt flag in bit 4.
3	Clear the interrupt flag in bit 3.
2	Clear the interrupt flag in bit 2.
1	Clear the interrupt flag in bit 1.
0	Clear the interrupt flag in bit 0.

CLEAR1

This command is used to selectively clear the interrupt flags in the upper byte (bits 15–8) of the status0 register.

The CLEAR1 command is selected by minor opcode15–12 bits = 0001.

The minor opcode7–0 bits specify options for the command. If a bit is zero, then the specified option is not selected.

7	Clear the interrupt flag in bit 15.
6	Clear the interrupt flag in bit 14.
5	Clear the interrupt flag in bit 13.
4	Clear the interrupt flag in bit 12.
3	Clear the interrupt flag in bit 11.
2	Clear the interrupt flag in bit 10.
1	Clear the interrupt flag in bit 9.
0	Clear the interrupt flag in bit 8.

SET0

This command is used to selectively set the interrupt flags in the lower byte (bits 7–0) of the status0 register.

The SET0 command is selected by minor opcode15–12 bits = 0010.

The minor opcode7–0 bits specify options for the command. If a bit is zero, then the specified option is not selected.

7	Unused.
6	Unused.
5	Set the interrupt flag in bit 5.
4	Set the interrupt flag in bit 4.
3	Set the interrupt flag in bit 3.
2	Set the interrupt flag in bit 2.
1	Set the interrupt flag in bit 1.
0	Set the interrupt flag in bit 0.

minor command register bit description (continued)

SET1

This command is used to selectively set the interrupt flags in the upper byte (bits 15–8) of the status0 register.

The SET1 command is selected by minor opcode15–12 bits = 0011.

The minor opcode7–0 bits specify options for the command. If a bit is zero, then the specified option is not selected.

7	Set the interrupt flag in bit 15.
6	Set the interrupt flag in bit 14.
5	Set the interrupt flag in bit 13.
4	Set the interrupt flag in bit 12.
3	Set the interrupt flag in bit 11.
2	Set the interrupt flag in bit 10.
1	Set the interrupt flag in bit 9.
0	Set the interrupt flag in bit 8.

OPERATE0

This command is used to:

- Begin STATE, SCAN, or EXECUTE commands.
- Abort SCAN or EXECUTE commands.
- Enable EXECUTE commands to begin (usually from an EVENT pin).

This command is also used to selectively clear the request flags (observable in the status1 register) used by EXECUTE commands. The similar OPERATE1 command is used to selectively set them. These flags affect the EXECUTE command in the following ways:

- Request it to begin or end.
- Request an awake command to resume.
- Request an asleep command to resume.

When the command acknowledges the request, the request flag is cleared and a matching acknowledge-interrupt flag is set. The affected command will alter the awake and alive status bits and set the appropriate finish, abort, suspend, end, resume, or begin interrupt flag when it responds.

The OPERATE0 command is selected by minor opcode15–12 bits = 0100.

The minor opcode7–0 bits specify options for the command. If a bit is zero, then the specified option is not selected.

7	Begin a STATE, SCAN or EXECUTE command.
6	Abort a SCAN or EXECUTE command.
5	Enable an EXECUTE command to begin.
4	Unused.
3	Clear the EXECUTE command begin-request flag.
2	Clear the EXECUTE command resume-request flag.
1	Clear the EXECUTE command end-request flag.
0	Clear the EXECUTE command suspend-request flag.

OPERATE1

This command is used to:

- Begin STATE, SCAN, or EXECUTE commands.
- Abort SCAN or EXECUTE commands.
- Enable EXECUTE commands to begin (usually from an EVENT pin).

minor command register bit description (continued)

This command is also used to selectively set the request flags (observable in the status1 register) used by EXECUTE commands. The similar OPERATE0 command is used to selectively clear them. These flags affect the EXECUTE command in the following ways:

- Request it to begin or end.
- Request an awake command to suspend.
- Request an asleep command to resume.

When the command acknowledges the request, the request flag is cleared and a matching acknowledge-interrupt flag is set. The affected command will alter the awake and alive status bits and set the appropriate finish, abort, suspend, end, resume, or begin interrupt flag when it responds.

The OPERATE1 command is selected by minor opcode15–12 bits = 0101.

The minor opcode7–0 bits specify options for the command. If a bit is zero, then the specified option is not selected.

7	Begin a STATE, SCAN or EXECUTE command.
6	Abort a SCAN or EXECUTE command.
5	Enable an EXECUTE command to begin.
4	Unused.
3	Set the EXECUTE command begin-request flag.
2	Set the EXECUTE command resume-request flag.
1	Set the EXECUTE command end-request flag.
0	Set the EXECUTE command suspend-request flag.

OPERATE2

The OPERATE2 command is used to operate various functions.

The OPERATE2 command is selected by minor opcode15–12 bits = 0110.

The minor opcode7–0 bits specify options for the command. If a bit is zero, then the specified option is not selected.

7	Unused.
6	Capture status2, status1 and status0.
5	Update counter21.
4	Update counter20.
3	Unused.
2	Capture counter1.
1	Operate counter1.
0	Update counter1.

RESET

This command is used to software-reset either selected functions or the entire 'ACT8990.

The RESET command is selected by minor opcode15–12 bits = 0111.

minor command register bit description (continued)

The minor opcode7–0 bits specify options for the command. If a bit is zero, then the specified option is not selected.

7	Unused.
6	Unused.
5	Unused.
4	Unused.
3	Reset the request flag.
2	Reset the data buffers.
1	Reset the interrupt flags.
0	Software reset the entire 'ACT8990.

major command register bits

BIT	DESCRIPTION
0	Major Opcode0
1	Major Opcode1
2	Major Opcode2
3	Major Opcode3
4	Major Opcode4
5	Major Opcode5
6	Major Opcode6
7	Major Opcode7
8	Major Opcode8
9	Null
10	Null
11	Null
12	Major Opcode12
13	Major Opcode13
14	Major Opcode14
15	Major Opcode15

major command register bit description

The major command register is set by the host to select a particular major command to be executed and to direct its operations while it is alive. The bits are not altered by the device. The major command register address (from ADRS4–ADRS0) is 01011.

The act of writing an OPERATE0/1 minor command with bit 7 set, causes the selected major command to begin.

The major commands may require many clock periods to complete their operations, during which the awake and alive status bits are affected. When they finish, the finish interrupt flag is set. The major commands do not assert the $\overline{\text{RDY}}$ pin.

Note that the major command register should not be written to while a major command is alive.

major opcode8–0
The major opcode8–0 bits specify options for the command.

major command register bit description (continued)

major opcode15–12

The major opcode15–12 bits select the major command:

0000	No effect.
0001	Select a STATE command to change the target-interface state.
0010	Select an EXECUTE command to cause the IEEE Standard 1149.1 target to execute an instruction.
0011	Select a SCAN command to scan data and instructions between the IEEE Standard 1149.1 target and the 'ACT8990.
01XX	No effect.
1XXX	No effect.

Major commands cause the 'ACT8990 to interface with its IEEE Standard 1149.1 target(s). There are three major commands: STATE, EXECUTE, and SCAN.

STATE

The STATE command is used to change the state of the target interface and target(s) from their current state to the state selected by the major opcode2–0 bits.

During the STATE command no action other than the state change occurs:

- The event detectors and counters are ignored.
- Counter1 is ignored and not operated, even if the Run-Test/Idle state is entered.
- The data buffers are ignored and not loaded from or stored to, even if the Shift-DR or Shift-IR states are entered.
- The shifter-FIFO is ignored and not operated, even if the Shift-DR or Shift-IR states are entered.

The command (see Figure 20) has two operating states that can be used together with the major opcode2–0 bits by the Sequencer block to select which IEEE Standard 1149.1 state the target interface and target(s) should be held in or moved to. The states are:

- Dead: the command is either finished or not yet begun.
- End: the Sequencer block is moving the target interface to the state selected by the major opcode2–0 bits.

If the current state and selected state are different, the state change (see Figure 1) uses the following rules:

- If the current state is Test-Logic-Reset, then the change occurs first through the stable Run-Test/Idle state, then via temporary states only.
- If the current state is not Test-Logic-Reset, then the change occurs via temporary states only.

If the current state and selected state are the same, the state change (see Figure 1) uses the following rules:

- If major opcode2 is 0 (the state is Test-Logic-Reset or Run-Test/Idle), then no change occurs.
- If major opcode2 is 1 (the state is Shift-DR, Shift-IR, Pause-DR or Pause-IR), then the change occurs via temporary states only through the matching update and capture states, returning to the same state.

The STATE command can be begun only by OPERATE0/1 minor commands. Note that the EXECUTE command can be configured to behave like the STATE command by going directly to its end state after it begins, the difference being that the EXECUTE command can be begun by a signal on an EVENT pin via the event detectors and counters.

major command register bit description (continued)

The STATE command is selected by major opcode15–12 bits = 0001. The major opcode11-4 bits are ignored.

The major opcode2–0 bits select the end state (the state of the target after the command ends).

000 Test-Logic-Reset.
001 Test-Logic-Reset.
010 Run-Test/Idle.
011 Run-Test/Idle.
100 Shift-DR.
101 Shift-IR.
110 Pause-DR.
111 Pause-IR.

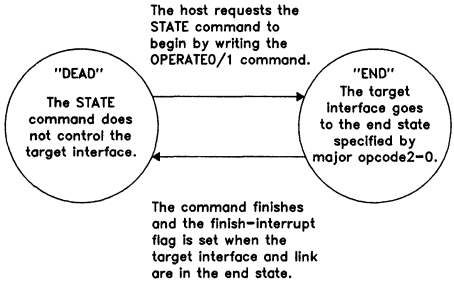


FIGURE 20. STATE DIAGRAM OF THE STATE COMMAND

major command register bit description (continued)

EXECUTE

The EXECUTE command is used to make the target(s) execute instructions (in the Run-Test/Idle state) that have been shifted into their instruction register(s).

The command (see Figure 21) has four operating states (dead, execute, sleep and end) that are used together with the major opcode bits by the sequencer block to select which IEEE Standard 1149.1 state the target interface and target(s) should be held in or moved to.

The combination of the command operating states and changes between these states caused by minor commands, counter1, the event detectors, and counters allow the target(s) instructions to begin, suspend, resume and end under host software or the 'ACT8990 hardware control.

When the 'ACT8990 is configured for IEEE Standard 1149.1 target(s) (by setting the machine format1–0 and output format1–0 control bits to zero), the command operating states are:

- Dead: the command is either finished or not yet begun.
- Execute: the target interface is in (or moving to) the Run-Test/Idle state in which IEEE Standard 1149.1 target(s) execute their instruction(s).
- Sleep: the target interface is in (or moving to) the Pause-DR or Pause-IR states (as selected by the major opcode3 bit) in which IEEE Standard 1149.1 target(s) may not execute their instruction(s).
- End: the command is about to finish and the sequencer block is moving the target interface to a state selected by the major opcode2–0 bits.

The command state may be changed by:

- Host software: the OPERATE0/1 minor commands may set and clear flags to request the command to begin, suspend, resume or end.
- Host software: the OPERATE0/1 minor commands may request the command to abort.
- The EXECUTE command itself: its major opcode4 bit may be set to automatically suspend itself every time it enters the execute state.
- The event detectors and counters: they may set flags to request the command to begin, suspend, resume or end.
- Counter1: it may set flags to request the command to suspend or end.

The command is suspended by an EVENT pin via an event detector, by an OPERATE0/1 command, or by counter1 passing zero. The executing command goes to the sleep state selected by the major opcode3 bit in which it does not operate counter1.

major command register bit description (continued)

The command is ended by an EVENT pin via an event detector, by an OPERATE0/1 command, or by counter1 passing zero. The executing or sleeping command goes to the end state selected by the major opcode2–0 bits and finishes. End requests have priority over suspend or resume requests.

The command is resumed by an EVENT pin via an event detector or by an OPERATE0/1 command. The sleeping command goes to the execute state selected by the major opcode3 bit in which it may operate counter1.

The command is begun by an EVENT pin via an event detector or by an OPERATE0/1 command. The dead command goes to the end, sleep or execute state selected by the major opcode7–6 bits. Attempts to set the begin-request flag are ignored until they are enabled by OPERATE0/1 commands.

The command is aborted by an OPERATE0/1 command. The executing or sleeping command goes to the sleep state selected by the major opcode3 bit and finishes. Abort requests have priority over suspend or resume requests.

The alive status bit is asserted when the command begins and negated when it finishes. The awake status bit is one (the command is awake) when the target interface is moving to or already in the execute or end states. The awake status bit is zero (the command is asleep) when the target interface is moving to or already in the sleep state.

This command allows only one contiguous block of execute states to be outstanding in the retimed link. If the command is asleep and a resume request occurs, the device will not respond until the link is empty of execute states. If the command is asleep or executing and an end or abort request occurs, the device responds immediately.

The command finishes when the link is empty of execute and temporary states and holds only the end or sleep state. It then sets the finish flag (and possibly the abort flag).

The EXECUTE command is selected by major opcode15–12 bits = 0010.

The major opcode11–9 bits are ignored.

The major opcode8 bit selects suspend and resume options.

0 The command clears only the respective suspend or resume requests when it suspends or resumes.

1 The command clears both suspend and resume requests when it either suspends or resumes.

The major opcode7–6 bits select the begin options.

00 or 01 The command goes directly to the end state when it begins. It is similar to a STATE command but may be begun by EVENT pins.

10 The command goes directly to the sleep state when it begins.

11 The command goes directly to the execute state when it begins.

The major opcode5–4 bits select suspend, end, and abort options.

00 The command pauses or ends when counter1 passes zero.

01 The command pauses or ends when counter1 passes zero.

10 The command does not use counter1 and ends after a single execute state is sent.

11 The command does not use counter1 and aborts after a single execute state is sent.

The major opcode3 bit selects the execute and sleep states for IEEE Standard 1149.1 operation if machine format1–0 bits are 00. If machine format1–0 bits are 01, 10, or 11, then other states are selected for TI internal manufacturing test mode.

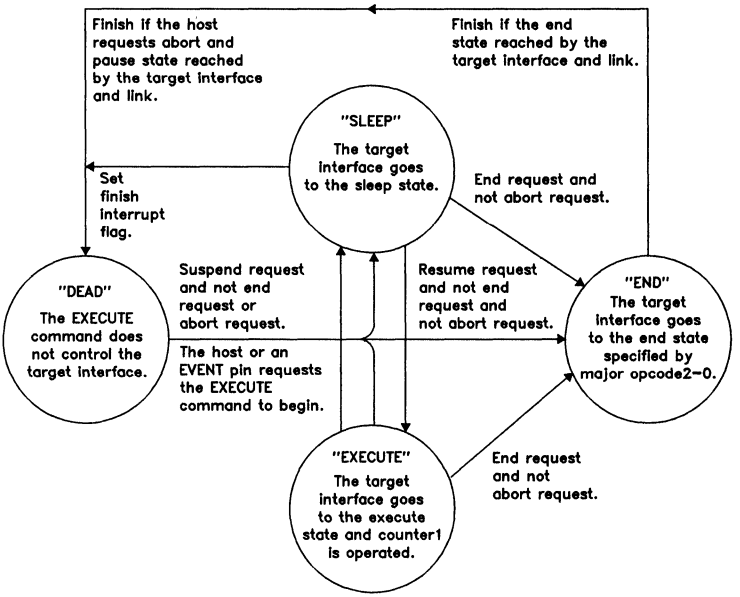
0 Use Run-Test/Idle and Pause-DR states.

1 Use Run-Test/Idle and Pause-IR states.

major command register bit description (continued)

The major opcode2–0 bits selects the end state.

000	Test-Logic-Reset.
001	Test-Logic-Reset.
010	Run-Test/Idle.
011	Run-Test/Idle.
100	Shift-DR.
101	Shift-IR.
110	Pause-DR.
111	Pause-IR.



NOTES: 1. The begin, end, suspend, and resume requests are caused by either the host writing OPERATE0/1 commands, by the detection and counting of events on event pins, or by counter1 passing zero.

2. Counter1 passing zero can cause pause or end requests.

3. When the command begins, the target interface goes to the execute, pause, or end states as selected by major opcode5–4.

FIGURE 21. STATE DIAGRAM OF THE EXECUTE COMMAND

major command register bit description (continued)

SCAN

The SCAN command is used to scan instructions and data (in the Shift-IR or Shift-DR states) between the 'ACT8990 parallel write and read buffers and the target(s) serial instruction or data registers.

The command (see Figure 22) has four operating states (dead, scan, sleep and end) that are used together with the major opcode bits by the sequencer block to select which IEEE Standard 1149.1 state the target interface and target(s) should be held in or moved to.

The combination of the command operating states and changes between these states allow the command to perform all low-level scan functions. The host functions are limited to the following: 1) before the command begins, selecting the number of bits to be scanned by loading the value into counter1 and 2) during the command, capturing the write and read buffer status in status2 register and appropriately loading data to the write buffer or storing data from the read buffer.

When the 'ACT8990 is configured for IEEE Standard 1149.1 target(s) (by setting the machine format1–0 and output format1–0 control bits to zero), the SCAN command operating states are:

- Dead: the command is either finished or not yet begun.
- Scan: the target interface is in (or moving to) the Shift-DR or Shift-IR state (as selected by the major opcode3 bit) in which the 'ACT8990 will scan data between itself and the target(s).
- Sleep: the target interface is in (or moving to) the Pause-DR or Pause-IR state (as selected by the major opcode3 bit) in which the 'ACT8990 will not scan data between itself and the target(s).
- End: the command is about to finish and the sequencer block is moving the target interface to a state selected by the major opcode2–0 bits.

The command state may be changed by:

- Host software: the OPERATE0/1 minor commands may request the command to abort.
- The Write Buffer: the command suspends and resumes the scanning of data (by entering its sleep and scan states) depending on the availability of data in the write buffer.
- The Read Buffer: the command suspends the resumes the scanning of data (by entering its sleep and scan states) depending on the availability of space in the read buffer.
- Counter1: the command ends (by entering its end state) when counter1 passes zero and the correct number of bits have been scanned.

major command register bit description (continued)

The target registers are treated as a number of modules each containing a string of data. Each string is accessed with one or more SCAN commands. The string length is defined as one plus the value of the counter1 register, giving a range of one to 2^{32} bits per SCAN command. The command ends when counter1 passes zero, decrements to all ones, and all data bits are sent. The command then goes to the end state and finishes.

The SCAN command may be aborted by an OPERATE0/1 command. It responds in either the scan or the sleep states when on a word boundary by going to the sleep state and finishing.

The alive status bit is asserted when the command begins and negated when it finishes. The awake status bit is one (the command is awake) when the target interface is moving to or already in the scan or end states. The awake status bit is zero (the command is asleep) when the target interface is moving to or already in the sleep state.

The SCAN command does not allow the number of outstanding data bits to exceed the shifter-FIFO length as selected by the serial length control bit.

The command finishes when the link is empty of scan and temporary states and holds only the stable end or sleep state. It then sets the finish flag (and possibly the abort flag).

The SCAN command is selected by major opcode15–12 bits = 0011.

The major opcode11–6 bits are ignored.

The major opcode5–4 bits select the suspend, end, and abort options.

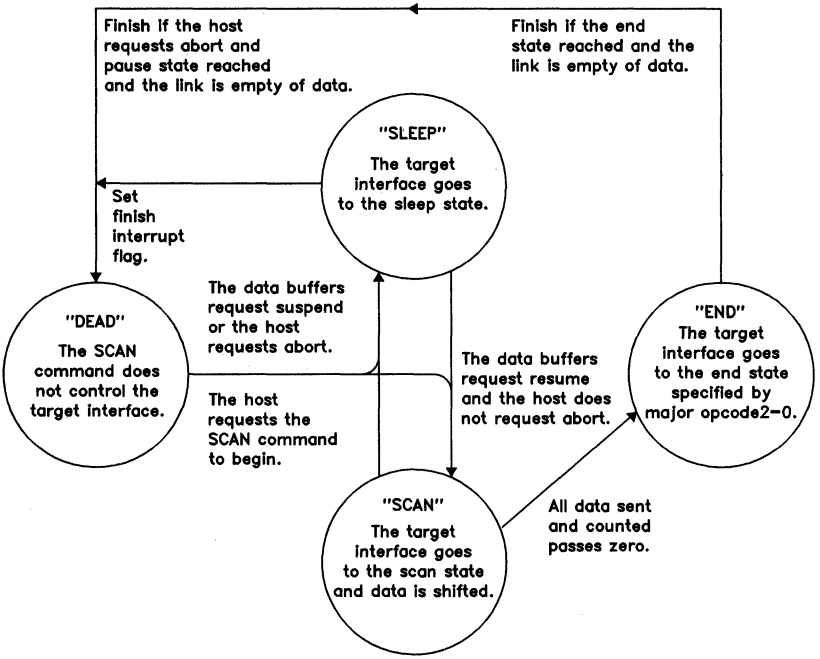
00	The command ends when counter1 passes zero.
01	The command ends when counter1 passes zero and suspends after all bits are sent.
10	The command does not use counter1 and ends after a single bit is sent.
11	The command does not use counter1 and aborts after a single bit is sent.

The major opcode3 bit selects the scan and sleep states.

0	Use Shift-DR and Pause-DR states.
1	Use Shift-IR and Pause-IR states.

The major opcode2–0 bits select the end state.

000	Test-Logic-Reset.
001	Test-Logic-Reset.
010	Run-Test/Idle.
011	Run-Test/Idle.
100	Shift-DR.
101	Shift-IR.
110	Pause-DR.
111	Pause-IR.



NOTES: 1. The data buffers request suspend if read is full and write is empty.
2. The data buffers request resume if read is not full and write is not empty.
3. The command is begun and aborted by the host writing OPERATE0/1 commands.

FIGURE 22. STATE DIAGRAM OF THE SCAN COMMAND

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counter1 update0, counter1 update1 register bits

BIT	DESCRIPTION	
	COUNTER1 UPDATE0	COUNTER1 UPDATE1
0	Counter1 Update0	Counter1 Update16
1	Counter1 Update1	Counter1 Update17
2	Counter1 Update2	Counter1 Update18
3	Counter1 Update3	Counter1 Update19
4	Counter1 Update4	Counter1 Update20
5	Counter1 Update5	Counter1 Update21
6	Counter1 Update6	Counter1 Update22
7	Counter1 Update7	Counter1 Update23
8	Counter1 Update8	Counter1 Update24
9	Counter1 Update9	Counter1 Update25
10	Counter1 Update10	Counter1 Update26
11	Counter1 Update11	Counter1 Update27
12	Counter1 Update12	Counter1 Update28
13	Counter1 Update13	Counter1 Update29
14	Counter1 Update14	Counter1 Update30
15	Counter1 Update15	Counter1 Update31

counter1 update1–0 registers bit description

The counter1 update1–0 registers are set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The counter1 update0 register address (from ADRS4–ADRS0) is 01100. The counter1 update1 register address (from ADRS4–ADRS0) is 01101.

Counter1 update registers load the 32-bit counter used in major commands. Registers 0 and 1 are the least and most significant words. Bits 0 and 15 are the least and most significant bits of each register. Reset causes the counter1 update register bits to be reset to all zeroes. Counter1 is usually loaded before major commands begin. It is also reloaded from these registers when it passes zero during EXECUTE commands if the counter control bits are appropriately set.

These registers are loaded to the counter by the OPERATE2 command.

counter2 update0, counter2 update1 register bits

BIT	DESCRIPTION	
	COUNTER2 UPDATE0	COUNTER2 UPDATE1
0	Counter2 Update0	Counter2 Update16
1	Counter2 Update1	Counter2 Update17
2	Counter2 Update2	Counter2 Update18
3	Counter2 Update3	Counter2 Update19
4	Counter2 Update4	Counter2 Update20
5	Counter2 Update5	Counter2 Update21
6	Counter2 Update6	Counter2 Update22
7	Counter2 Update7	Counter2 Update23
8	Counter2 Update8	Counter2 Update24
9	Counter2 Update9	Counter2 Update25
10	Counter2 Update10	Counter2 Update26
11	Counter2 Update11	Counter2 Update27
12	Counter2 Update12	Counter2 Update28
13	Counter2 Update13	Counter2 Update29
14	Counter2 Update14	Counter2 Update30
15	Counter2 Update15	Counter2 Update31

counter2 update1–0 registers bit description

The counter2 update1–0 registers are set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The counter2 update0 register address (from ADRS4–ADRS0) is 01110. The counter2 update1 register address (from ADRS4–ADRS0) is 01111.

Counter2 update registers load counter20 and counter21. When concatenated, registers 0 and 1 are the least and most significant words. Bits 0 and 15 are the least and most significant bits of each register. Reset causes the counter2 update register bits to be reset to all zeroes. Counter20/21 are usually loaded before major commands begin. They are also reloaded from these registers when they pass zero or as decided by an EVENT pin (external update) if the counter control bits are appropriately set.

These registers are loaded to the counter by the OPERATE2 command and when the counter20 and counter21 update inverted control bits are zero.

status0 register bits

BIT	DESCRIPTION
0	Event0 Detect
1	Event1 Detect
2	Event2 Detect
3	Event3 Detect
4	Counter1 Execute
5	Counter1 Scan
6	Null
7	Null
8	Suspend Acknowledge
9	End Acknowledge
10	Resume Acknowledge
11	Begin Acknowledge
12	Buffer Error
13	Buffer Ready
14	Abort
15	Finish

status0 register bit description

The host may only read the status0 register. It is used to examine the 'ACT8990 during and after commands. The bits are altered by the device when an OPERATE2 command occurs. The status0 register address (ADRS4–ADRS0) is 10000.

This register holds the interrupt flag bits that indicate a specific status condition that has occurred in the device. If the matching interrupt-enable bit in the control0 register is set, then the $\overline{INT}$ pin will be asserted. The interrupt flags are selectively cleared and set by the CLEAR0/1 and SET0/1 commands.

These bits are loaded from the interrupt flags by an OPERATE2 command.

event0 detect
This flag indicates if an event has been detected by event detector0.
0 No.
1 Yes.

event1 detect
This flag indicates if an event has been detected by event detector1.
0 No.
1 Yes.

event2 detect
This flag indicates if an event has been detected by event detector2.
0 No.
1 Yes.

event3 detect
This flag indicates if an event has been detected by event detector3.
0 No.
1 Yes.

status0 register bit description (continued)

counter1 execute
This flag indicates if counter1 has passed zero, as configured by the control8 register, usually for an EXECUTE command.
0 No.
1 Yes.

counter1 scan
This flag indicates if counter1 has passed zero during a SCAN command.
0 No.
1 Yes.

suspend acknowledge
This flag indicates if an EXECUTE command has responded to a suspend request.
0 No.
1 Yes.

end acknowledge
This flag indicates if an EXECUTE command has responded to an end request.
0 No.
1 Yes.

resume acknowledge
This flag indicates if an EXECUTE command has responded to a resume request.
0 No.
1 Yes.

begin acknowledge
This flag indicates if an EXECUTE command has responded to a begin request.
0 No.
1 Yes.

buffer error
This bit indicates if a buffer error has occurred (i.e., an over-write or under-read to the write and read buffers).
0 No.
1 Yes.

buffer ready
This bit indicates if the data buffers are ready for reading. This occurs when:
- Only the write buffer is used and becomes empty.
- Only the read buffer is used and becomes full.
- Both are used, where the write buffer becomes empty and the read buffer becomes full.

0 No.
1 Yes.

abort
This flag indicates if a major command has aborted.
0 No.
1 Yes.

finish
This flag indicates if a major command has finished.
0 No.
1 Yes.

status1 register bits

BIT	DESCRIPTION
0	Event0 Level
1	Event1 Level
2	Event2 Level
3	Event3 Level
4	Null
5	Null
6	Null
7	Null
8	Suspend Request
9	End Request
10	Resume Request
11	Begin Request
12	Null
13	Null
14	Awake
15	Alive

status1 register bit description

The host may only read the status1 register. It is used to examine the 'ACT8990 during and after commands. The bits are altered by the device when an OPERATE2 command occurs. The status1 register address (ADRS4–ADRS0) is 10001.

These bits are loaded from the internal status signals by an OPERATE2 command.

event0 level
This flag indicates the level of this pin.
0 Low.
1 High.

event1 level
This flag indicates the level of this pin.
0 Low.
1 High.

event2 level
This flag indicates the level of this pin.
0 Low.
1 High.

event3 level
This flag indicates the level of this pin.
0 Low.
1 High.

status1 register bit description (continued)

suspend request
This flag indicates if an EXECUTE command has been requested to suspend.
0 No.
1 Yes.

end request
This flag indicates if an EXECUTE command has been requested to end.
0 No.
1 Yes.

resume request
This flag indicates if an EXECUTE command has been requested to resume.
0 No.
1 Yes.

begin request
This flag indicates if an EXECUTE command has been requested to begin.
0 No.
1 Yes.

awake
This status bit indicates the state of major commands.
0 A major command is alive and asleep, or none are alive.
1 A major command is alive and awake, or ending.

The target-interface send functions are moving towards or already in the execute or scan state when awake during EXECUTE or SCAN commands. The target-interface send functions are moving towards or already in the end state selected by major opcode2–0 when ending during STATE, EXECUTE or SCAN commands.

alive
This status bit indicates the state of major commands.
0 No command is alive.
1 A major command is alive.

status2 register bits

BIT	DESCRIPTION
0	Target Interface State0
1	Target Interface State1
2	Target Interface State2
3	Target Interface State3
4	Null
5	Null
6	Null
7	Null
8	Write OK Inverted
9	Write Empty Inverted
10	Null
11	Null
12	Read OK
13	Read Full
14	Null
15	Null

status2 register bit description

The host may only read the status2 register. It is used to examine the 'ACT8990 during and after commands. The bits are altered by the device when an OPERATE2 command occurs. The status2 register address (ADRS4–ADRS0) is 10010.

These bits are loaded from the internal status signals by an OPERATE2 command.

target interface state2–0
These bits indicate which stable state the target interface is sending.

000 Test-Logic-Reset.
001 Test-Logic-Reset.
010 Run-Test/Idle.
011 Run-Test/Idle.
100 Shift-DR.
101 Shift-IR.
110 Pause-DR.
111 Pause-IR.

target interface state3
This bits indicates if the target interface is sending a stable state or a temporary state.

0 The target is in the stable state indicated by bits 2–0.
1 The target interface is in a temporary state and bits 2–0 are all zeroes.

write OK inverted
This bit indicates the status of the write buffer at all times. It is active if at least one word of the buffer is empty.

0 At least one word of the serial write buffer is empty.
1 The serial write buffer is full.

status2 register bit description (continued)

write empty inverted

This bits indicates the status of the write buffer at all times. If the buffer is empty, two words may be written into it.

0 The serial write buffer is empty.
1 The serial write buffer is not empty.

read OK

This bit indicates the status of the read buffer at all times. When active, at least one word is full and may be read.

0 The serial read buffer is empty.
1 At least one word of the serial read buffer is full.

read full

The status of this bit indicates the condition of the serial read buffer at all times.

0 At least one word of the serial read buffer is empty.
1 Both words of the serial read buffer are full.

status3 register bits

BIT	DESCRIPTION
0	Null
1	Null
2	Null
3	Null
4	Null
5	Null
6	Null
7	Null
8	Null
9	Null
10	Null
11	Null
12	Null
13	Null
14	Null
15	Null

status3 register bit description

The status3 register address (ADRS4–ADRS0) is 10011.

All bits in this register are null; writes have no effect and reads obtain zeroes.

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capture0, capture1 register bits

BIT	DESCRIPTION	
	CAPTURE0	CAPTURE1
0	Capture0	Capture16
1	Capture1	Capture17
2	Capture2	Capture18
3	Capture3	Capture19
4	Capture4	Capture20
5	Capture5	Capture21
6	Capture6	Capture22
7	Capture7	Capture23
8	Capture8	Capture24
9	Capture9	Capture25
10	Capture10	Capture26
11	Capture11	Capture27
12	Capture12	Capture28
13	Capture13	Capture29
14	Capture14	Capture30
15	Capture15	Capture31

capture1–0 registers bit description

The host may only read the capture1–0 registers. They are used to examine the 'ACT8990 during and after commands. The bits are altered by the device when an OPERATE2 command occurs. The capture0 register address (ADRS4–ADRS0) is 10100. The capture1 register address (ADRS4–ADRS0) is 10101.

These registers hold the value of counter1. They are loaded from counter1 by an OPERATE2 command or when the capture enable1 bit is set.

capture15–0
The capture0 register stores the current value of the counter1 least significant word. Bits 0 and 15 are the least and most significant bits, respectively. Reset causes this register to reset to all zeroes.

capture31–16
The capture1 register stores the current value of the counter1 most significant word. Bits 16 and 31 are the least and most significant bits, respectively. Reset causes this register to be reset to all zeroes.

read buffer register bits

BIT	DESCRIPTION
0	Read Buffer0
1	Read Buffer1
2	Read Buffer2
3	Read Buffer3
4	Read Buffer4
5	Read Buffer5
6	Read Buffer6
7	Read Buffer7
8	Read Buffer8
9	Read Buffer9
10	Read Buffer10
11	Read Buffer11
12	Read Buffer12
13	Read Buffer13
14	Read Buffer14
15	Read Buffer15

read buffer register bit description

The host may only read this register. It is used to access the read buffer used by the SCAN commands. The read buffer register address (ADRS4–ADRS0) is 10110.

read buffer15–0
These bits are the most significant word of the two words that make up the read buffer.

write buffer register bits

BIT	DESCRIPTION
0	Write Buffer0
1	Write Buffer1
2	Write Buffer2
3	Write Buffer3
4	Write Buffer4
5	Write Buffer5
6	Write Buffer6
7	Write Buffer7
8	Write Buffer8
9	Write Buffer9
10	Write Buffer10
11	Write Buffer11
12	Write Buffer12
13	Write Buffer13
14	Write Buffer14
15	Write Buffer15

write buffer register bit description

The host may only write to this register. It is used to access the write buffer used by the SCAN commands. The write buffer register address (ADRS4–ADRS0) is 10111.

write buffer15–0
These bits are the most significant word of the two words that make up the write buffer.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_I < 0 or V_I > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pin ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		SN54ACT8990			SN74ACT8990			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−8			−8	mA
I_{OL}	Low-level output current			8			8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		V_{CC}	TEST CONDITIONS	T_A = 25°C			SN54ACT8990		SN74ACT8990		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		4.5 V	I_{OH} = −20 μA	4.4			4.4		4.4		V
			I_{OH} = −8 mA	3.7			3.7		3.7		
		5.5 V	I_{OH} = −20 μA	5.4			5.4		5.4		
V_{OL}		4.5 V to 5.5 V	I_{OL} = 20 μA			0.1		0.1		0.1	V
			I_{OL} = 8 mA			0.5		0.5		0.5	
I_I	ADRS, $\overline{RD}$, $\overline{WR}$, TCKI	5.5 V	V_I = V_{CC} or GND			±1		±1		±1	μA
	All others	5.5 V	V_I = V_{CC}			±1		±1		±1	μA
			V_I = GND		−70						
I_{OZ}	TDO, TMS, $\overline{INT}$, $\overline{RDY}$	5.5 V	V_O = V_{CC} or GND			±10		±10		±10	μA
	All others†	5.5 V	V_O = V_{CC}			±10		±10		±10	μA
			V_O = GND		−70						
I_{CC}		5.5 V	V_I = V_{CC} or GND, I_O = 0					450		450	μA

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

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timing requirements over recommended operating free-air temperature range (see Note 2)

			SN54ACT8990		SN74ACT8990		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency						MHz
t_w	Pulse duration	TCKI high or low					ns
		$\overline{TRST}$ low					
		$\overline{WR}$ low					
		EVENT3–0 high or low					
t_{su}	Setup time	TDI1–0 before TCKI ↑					ns
		EVENT3–0 before TCKI ↑					
		ADRS4–0 and DATA15–0 before $\overline{WR}$ ↑					
t_h	Hold time	TDI1–0 after TCKI ↑					ns
		EVENT3–0 after TCKI ↑					
		ADRS4–0 and DATA15–0 after $\overline{WR}$ ↑					
t_r	Recovery time	$\overline{TRST}$ high to $\overline{RDY}$ low					ns
		$\overline{WR}$ ↑ to $\overline{RDY}$ low					
		$\overline{RD}$ ↑ to $\overline{RDY}$ low					

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT8990		SN74ACT8990		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	TCKI						MHz
t_{PLZ}	$\overline{TRST}$ ↓	$\overline{RDY}$, $\overline{INT}$, DATA15–0					ns
t_{PHZ}							
t_{PZL}	$\overline{TRST}$ ↓	$\overline{RDY}$, $\overline{INT}$, DATA15–0					ns
t_{PZH}							
t_{PLZ}	$\overline{TRST}$ ↓	TMS/EVENT					ns
t_{PHZ}							
t_{PZL}	$\overline{TRST}$ ↓	TMS/EVENT					ns
t_{PZH}							
t_{PLZ}	$\overline{RD}$ ↑	DATA15–0					ns
t_{PHZ}							
t_{PZL}	$\overline{RD}$ ↑	DATA15–0					ns
t_{PZH}							
t_{PLZ}	$\overline{TCKI}$ ↓	TCKO, TMS5–0, TDO					ns
t_{PHZ}							
t_{PZL}	$\overline{TCKI}$ ↓	TCKO, TMS5–0, TDO					ns
t_{PZH}							
t_{PLZ}	$\overline{TOFF}$ ↓	TCKO, TMS5–0, TDO					ns
t_{PHZ}							
t_{PZL}	$\overline{TOFF}$ ↓	TCKO, TMS5–0, TDO					ns
t_{PZH}							
t_{PLZ}	$\overline{TCKI}$ ↓	EVENT3–0					ns
t_{PHZ}							
t_{PZL}	$\overline{TCKI}$ ↓	EVENT3–0					ns
t_{PZH}							
t_{PLZ}	$\overline{TOFF}$ ↓	EVENT3–0					ns
t_{PHZ}							
t_{PZL}	$\overline{TOFF}$ ↓	EVENT3–0					ns
t_{PZH}							

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (continued)

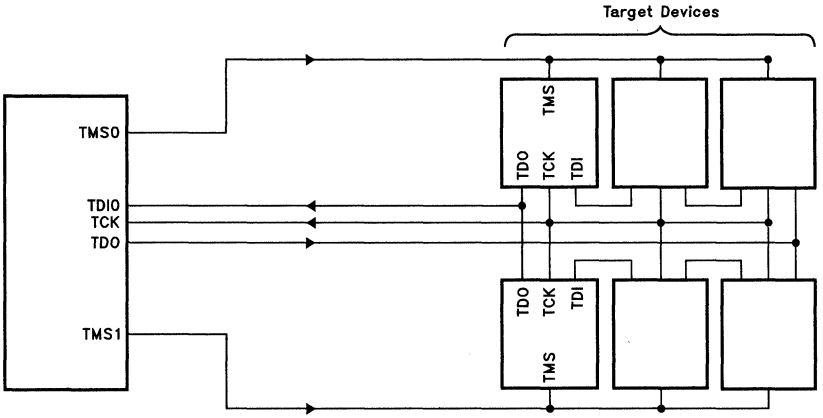
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT8990		SN74ACT8990		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	$\overline{TRST}$ ↑	$\overline{INT}$, $\overline{RDY}$					ns
t_{PHL}							
t_{PLH}	$\overline{TRST}$ ↓	TDO, TMS1–0					ns
t_{PLH}	ADRS4–0	DATA15–0					ns
t_{PHL}							
t_{PLH}	$\overline{WR}$ ↑	$\overline{RDY}$					ns
t_{PHL}							
t_{PLH}	$\overline{RD}$ ↓	DATA15–0					ns
t_{PHL}							
t_{PLH}	$\overline{RD}$ ↑	$\overline{RDY}$					ns
t_{PHL}	$\overline{RDY}$ ↓	$\overline{RD}$					ns
t_{PLH}	TCKI	$\overline{INT}$					ns
t_{PHL}							
t_{PLH}	TCKI ↓	TCKO, TMS5–0, TDO					ns
t_{PHL}							
t_{PLH}	$\overline{TOFF}$ ↑	TCKO, TMS5–0, TDO					ns
t_{PHL}							
t_{PLH}	TCKI ↓	EVENT3–0					ns
t_{PHL}							
t_{PLH}	$\overline{TOFF}$ ↑	EVENT3–0					ns
t_{PHL}							

APPLICATION INFORMATION

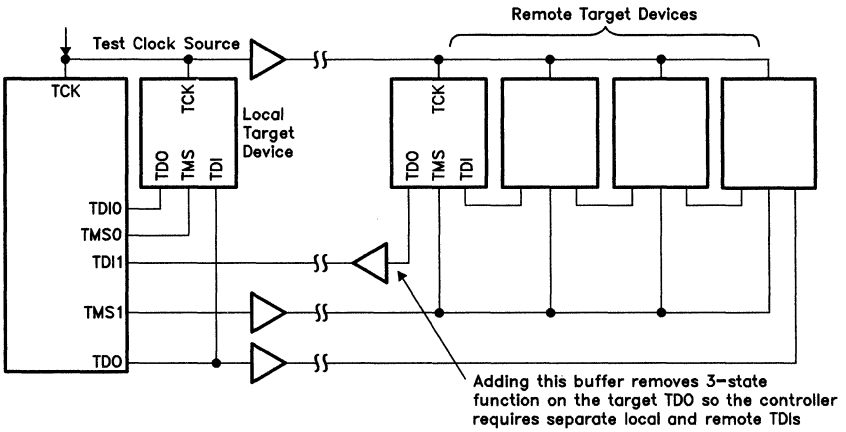
direct links

A direct link is a connection between the 'ACT8990 and targets that does not delay the target interface signals more than one clock period. Typically, it is pin to pin or uses TTL buffer devices. This method is used when the output buffer delay plus external buffer and cable delays meet the required setup timing values.

A direct link to a target is shown in Figure 23. The 'ACT8990 TDI, TDO, and TMS pins are connected to the TDO, TDI, and TMS pins of the target. The test clock is input and output on the TCKI and TCKO pins.



Two Parallel Chains of Targets with Separate TMS Inputs



Local and Remote Targets with Separate TMS Inputs and TDO Outputs

FIGURE 23. DIRECT LINKS TO TARGETS

APPLICATION INFORMATION (continued)

retimed links

A retimed link is an arrangement of one or more flip-flops in the connection between the 'ACT8990 and the target. Retimed links buffer and retime the target interface signals to meet the proper setup and hold time requirements between the 'ACT8990 and its targets. This may be required when the clock rate is high and either the target is at a distance or the connection involves fanout or TTL buffer devices. The length of the link is the total number of flip-flops in the outgoing and return paths. The 'ACT8990 supports retimed links up to 31 bits long.

A retimed link to a target is shown in Figure 24. The TDI, TDO, and TMS pins of the 'ACT8990 are connected to the target TDO, TDI, and TMS pins. The test clock is input and output on the TCKI and TCKO pins. The presence of the flip-flops delays the signals at the TDI1–0 and EVENT3–0 pins relative to the target interface state at the TMS5–0 and TDO outputs. To provide the major commands, data buffers and shifter-FIFO with the delayed mode source signal required to operate with retimed links, the mode source is passed through a link delay register whose length, set by the link delay4–0 control bits, matches the link itself. This is shown in Figure 8.

The STATE command finishes only when the requested state and equal numbers of temporary states have been sent and returned so that the whole link is in one stable state.

The EXECUTE command allows only one contiguous block of execute states to be outstanding in the retimed link. It decodes the mode source and the delayed mode source to identify execute states as they are sent and returned. This ensures that the end of a prior block of states being returned has been reached before the next block of states is sent. This command finishes only when the requested end state and equal numbers of temporary states have been sent and returned so that the whole link is in one stable state.

The SCAN command does not allow the number of outstanding data bits (the difference between the number of bits sent on TDO and the number of bits received on TDI) to exceed the shifter-FIFO length selected by the serial length control bit (control4 register bit 5). The number of outstanding data bits is counted by decoding the mode source and the delayed mode source to identify scan states as they are sent and returned. The SCAN command is used to control the operation of the shifter-FIFO. The scan command finishes only when the requested end state has been sent and returned so that the whole retimed link is in one stable state.

For retimed links shorter than the selected shifter-FIFO length, the 'ACT8990 scans data continuously without suspending the SCAN command. This is because it sends data bits from the shifter-FIFO until matching data bits are returned from the target. The 'ACT8990 compensates for the delay of data within the link without a reduction in the data transfer rate.

For retimed links longer that the selected shifter-FIFO length, the 'ACT8990 scans data in bursts and periodically suspends the SCAN command. This is because all of the data bits from the shifter-FIFO are sent before matching data bits are returned from the target. The 'ACT8990 compensates for the delay of data within the link, but at a reduced data transfer rate. The host sees this as a slowing in the filling and emptying of the data buffer as the suspend and resume commands are handled with the 'ACT8990.

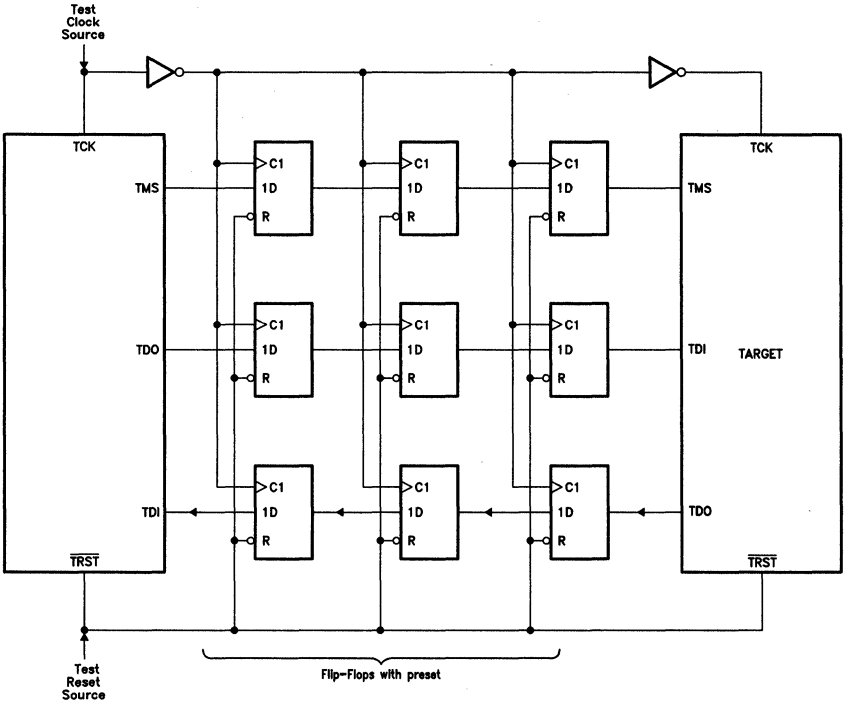


FIGURE 24. RETIMED LINK TO TARGET

APPLICATION INFORMATION (continued)

target switching

When the 'ACT8990 is linked to several parallel targets, its architecture allows the host to operate on them individually or in groups. A target may be operated on individually by setting the corresponding connect mode control bit to one while holding the other targets in some selected stable state with their connect mode control bits set to zero. Targets may be operated on as a group when the connect mode control bits for all targets in the group are set to one and all other connect mode control bits are set to zero.

Target switching is the method provided to suspend operations on one target and resume operations on any other target. To support target switching, the host must maintain records of the stable state, the link delay value, and the shifter string value for the targets that it is not currently operating on.

When the host decides to suspend operations on target A, it allows any major command that is alive to finish (end state). The connect data1 control bit is set to zero to disconnect all TMS pins and enter the loopback mode. The data in the shifter-FIFO from target A is stored and replaced with the data from target B by a short SCAN command whose end state matches that of target B. The link delay4–0 control bits and connect mode5-0 bits are set to match the link to target B. The connect data1 control bit is set to one to connect all TMS pins and target B may be operated on.

SN54ACT8994, SN74ACT8994
DIGITAL BUS MONITORS

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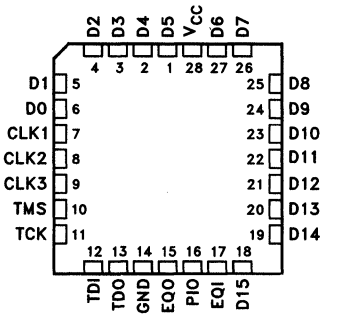
- **Members of the Texas Instruments SCOPE™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus**
- **Operation is Synchronous to the JTAG Test Clock (Offline Mode) or System Clock(s) (Online Mode)**
- **Each Contain a 1024-Word by 16-Bit Random-Access Memory (RAM) to Store the States of a Digital Bus**
- **Direct Memory Access (DMA) Speeds Memory and Register File Read/Write Operations**
- **Perform Parallel Signature Analysis (PSA) of Inputs with User-Definable Tap Bits**
- **Inputs Are Maskable During PSA Operations**
- **Cascaded PSA Mode Allows Compression of Data Paths > 16 Bits in Width**
- **Compatible with TI's ASSET™ (Automated Support System for Emulation and Test) Software**
- **Each Contain TI's Event Qualification Module for Real-Time System Test**
- **Eight Protocols for On-line Signal Monitoring and Test Operations**
- **Inputs are TTL-Voltage Compatible**
- **Power-Down Mode When RAM is Idling Reduces Power Dissipation**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic and Ceramic Chip Carriers**

SN54ACT8994 ... FK PACKAGE
SN74ACT8994 ... FN PACKAGE
(TOP VIEW)



description

The 'ACT8994 digital bus monitor (DBM) is designed to monitor and/or store the value of a digital bus up to sixteen bits in width. It resides in parallel with the bus being monitored.

Data clocked into the device can be stored in a scannable random-access memory (RAM). Up to 1024 words of sixteen bits can be stored. A parallel signature analysis (PSA) can also be performed on the data or on the contents of the memory. This allows the designer to check the signature after a predetermined number of clock cycles and examine up to 1024 prior patterns if an error is detected.

The 'ACT8994 can be operated in an on-line or off-line mode. In the on-line mode, the device operates synchronously to one or more of the external clock (CLK1–CLK3) inputs and/or the JTAG test clock (TCK) generated by the programmable clock interface (PCI) circuit, which allows real-time system tests to be performed by using the system clock(s) to control operation of the device.

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description (continued)

In the off-line mode, the device operates synchronously to TCK according to IEEE Standard 1149.1. The test access port (TAP) monitors TCK and the level of the test mode select (TMS) input to issue control signals and direct the device through its states (see Figure 1).

In the on-line mode, the event qualification module (EQM) allows data sample, storage, and/or PSA operations to be performed according to one of eight protocols. Register files in the EQM store compare patterns that allow the user to define specific values of the 16-bit bus for which the test operations are to be performed. Additional register files are provided for data mask patterns that cause the device to ignore data appearing on any combination of the data (D) inputs. Event-qualification-in (EQI) and event-qualification-out (EQO) pins allow global event qualification test schemes to be developed. Eight event-qualification protocols include various start/stop, start/pause/resume, and do-while algorithms.

The 1024-word by 16-bit RAM can be serially written to or read from one address at a time or via direct memory access (DMA) instructions provided to speed transfer of large amounts of data to and from the RAM. DMA is also implemented for accessing the register files in the EQM. IEEE Standard 1149.1-compatible read and write instructions are included.

There are two methods for initiating 'ACT8994 DMA operations. The first method monitors the serial data stream on the test data in (TDI) input and starts DMA when an expected 8-bit pattern is recognized. The second method initiates DMA when the TAP enters the Shift-DR TAP state from Pause-DR.

Many of the functional characteristics of the 'ACT8994 are user-definable, greatly increasing the flexibility and versatility of the device. Any combination of data bits can be masked from PSA and/or storage operations, and the user defines the tap bits for parallel signature generation. Many of the internal error and status signals can be output via EQO to monitor real-time test operations.

The RAM can be powered down when it is not being accessed, greatly decreasing total power dissipation.

The polynomial input/output (PIO) is a bidirectional pin used when cascading more than one DBM in a PSA operation. PIO is used as a feedback TAP for the PSA algorithm.

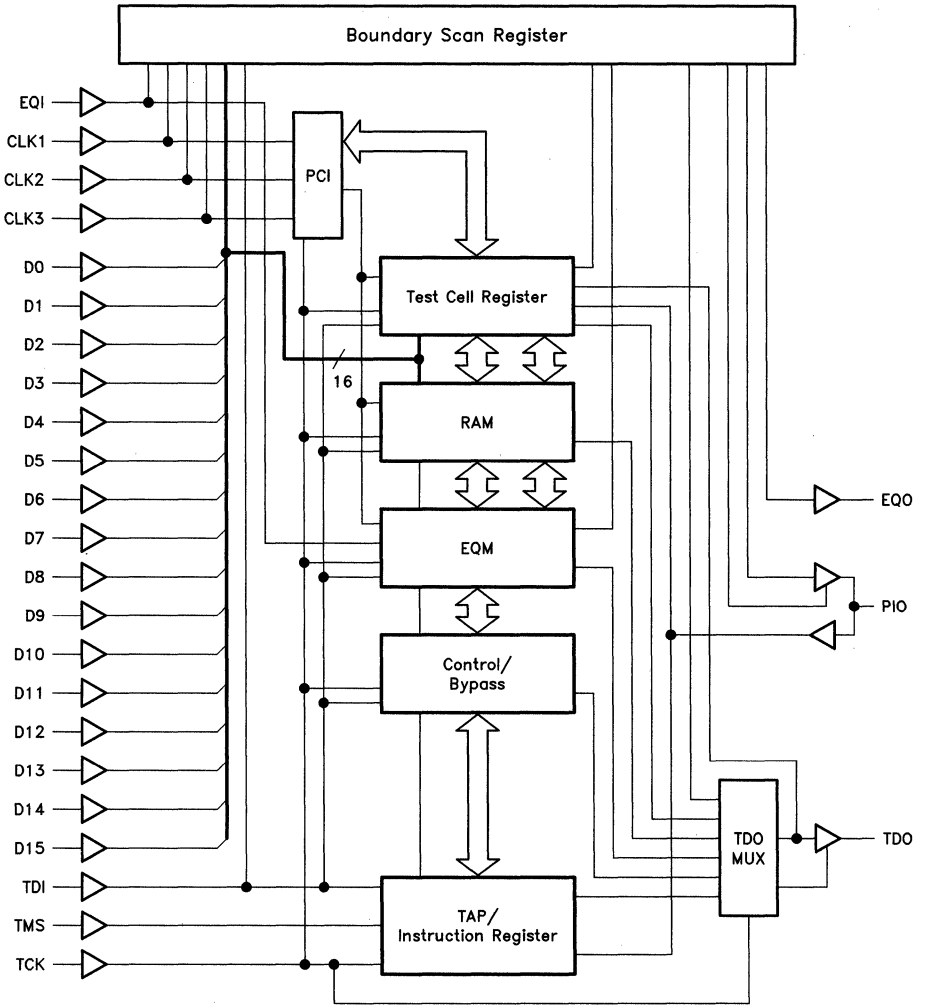
The device contains nine serial shift registers. For all registers, the most significant bit (MSB) is defined to be the bit nearest TDI. The least significant bit (LSB) is defined to be the bit nearest test data out (TDO).

The SN54ACT8994 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ACT8994 is characterized for operation from 0°C to 70°C.

D3604, JULY 1990—TI0285

PRODUCT PREVIEW

functional block diagram



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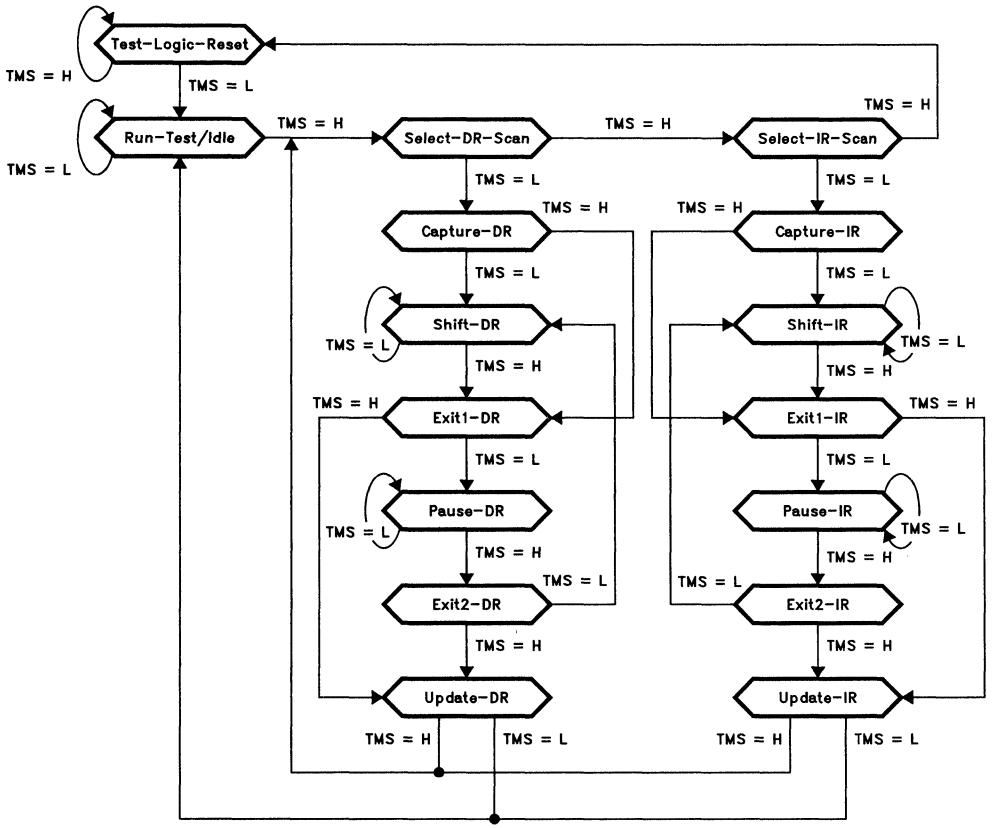

FIGURE 1. TAP STATE DIAGRAM

signal descriptions

TDI—Test Data In
One of the four pins required by IEEE Standard 1149.1. TDI is the serial input for shifting data through the instruction register or one of the data registers. An internal pullup forces TDI high if left floating or if a board continuity failure leaves the pin open.

TDO—Test Data Out
One of the four pins required by IEEE Standard 1149.1. TDO is the serial output for shifting data through the instruction register or data registers.

TCK—Test Clock
One of the four pins required by IEEE Standard 1149.1. Operation of the 'ACT8994 in the off-line mode is synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.

TMS—Test Mode Select
One of the four pins required by IEEE Standard 1149.1. The level of TMS at the rising edge of TCK directs the 'ACT8994 through its states (see Figure 1). An internal pullup forces TMS high if left floating or if a board continuity failure leaves the pin open.

D15–D0—Data Inputs
This sixteen-bit bus inputs data to be compressed and/or stored. Each bit can be individually masked so that it is not comprehended during test operations.

CLK1/CLK2/CLK3—Clock 1–Clock 3
In the on-line mode, operation of the 'ACT8994 is synchronous to one or a combination of these clocks and/or TCK. The programmable clock interface (PCI) circuit monitors the clock inputs and issues the on-line clock to the device.

PIO—Polynomial Input/Output
This I/O pin is used when cascading more than one DBM to provide signature analysis on more than sixteen bits. Its configuration as an input or output depends on the significance (most, middle, or least) of the DBM in the scan path.

EQI—Event Qualification In
This pin accepts data from the outside world when the 'ACT8994 operates in the on-line mode. This allows test operations to be performed when a user-defined condition exists. Eight protocols for on-line test operations are implemented in the 'ACT8994.

EQO—Event Qualification Out
This pin outputs signals when certain conditions have been observed. It can be configured to output sixteen different error and status signals during on-line monitoring. When more than one DBM is in use, the EQO outputs are typically wire-ANDed or wire-ORed together to implement global qualification schemes.

state diagram description

The TAP proceeds through the states in Figure 1 according to IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram, one to manipulate a data register and one to manipulate the instruction register. No more than one register should be manipulated at a time.

The function performed in any state occurs on the rising edge of TCK after the state is entered, and the function is also performed on the rising edge of TCK on the cycle in which the TAP state changes. For example, the first shift operation in Shift-DR occurs on the first rising edge of TCK after the TAP has entered Shift-DR from either Capture-DR or Exit2-DR and the last shift occurs on the rising edge of TCK in which the TAP state changes from Shift-DR to Exit1-DR.

Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.

Test-Logic-Reset
In this state, the test logic is inactive and an internal reset signal is applied to all registers in the device. During device operation, the TAP returns to this state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup that forces it to a high level if left unconnected or if a board defect causes it to be open-circuited. The device powers up in the Test-Logic-Reset state.

Passing through the Test-Logic-Reset state is equivalent to a power-down/power-up operation. All registers are set to their reset values during Test-Logic-Reset.

Run-Test/Idle
The TAP must pass through this state before executing any test operations. Storage and PSA operations in the off-line mode are executed in Run-Test/Idle.

Select-DR-Scan, Select-IR-Scan
No specific function is performed in these states, and the TAP exits either of them on the next TCK cycle. These states are provided to steer the TAP to the data and instruction register shift states.

Capture-DR
The selected data register is placed in the scan path (i.e., between TDI and TDO). Depending on the current instruction, data may or may not be loaded or captured by the selected register on the rising edge of TCK in Capture-DR.

Shift-DR
In this state, data is serially shifted through the selected data register, from TDI to TDO, on each TCK cycle. The first shift does not occur until the first TCK rising edge after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR).

On the falling edge of TCK as the TAP enters Shift-DR from Capture-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO enables to the level dictated by the LSB of the selected data register. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO enables to a low level as the bypass register, which preloads with a logic 0, is selected after a reset.

If the TAP enters Shift-DR from Exit2-DR, TDO enables to the value present before it was last disabled.

state diagram description (continued)

During DMA operations, data is transferred to or from the RAM or register files while the TAP is in the Shift-DR state. During a DMA write operation, data is serially input via TDI but is not shifted out via TDO. When a DMA write operation is active, the value of TDO is unknown.

During a DMA read operation, data is serially output via TDO and TDI is ignored.

Exit1-DR, Exit2-DR
These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-DR to Exit1-DR.

When the TAP state changes from Shift-DR to Exit1-DR, the last shift occurs on the TCK cycle in which the state changes.

Pause-DR
The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data. The device can also be configured to begin DMA read or write operations on either the RAM or the EQM register files if the TAP enters Pause-DR and then returns to Shift-DR via Exit2-DR.

Update-DR
If the current instruction calls for the shadow latches in the selected data register to be updated with current data, the latches are updated during this, and only this, state.

Capture-IR
The instruction register is preloaded with the IR status word (see **instruction register description**) and placed in the scan path.

Shift-IR
In this state, data is serially shifted through the instruction register, from TDI to TDO, on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). On the falling edge of TCK in Shift-IR, TDO goes from the high-impedance state to the active state. If the TAP enters Shift-IR from Capture-IR, TDO enables to a high level. If the TAP enters Shift-IR from Exit2-IR, TDO enables to the value present before it was last disabled.

Exit1-IR, Exit2-IR
These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-IR to Exit1-IR.

When the TAP state changes from Shift-IR to Exit1-IR, the last shift occurs on the TCK cycle in which the state changes.

Pause-IR
The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data. EQO can be configured to output an error signal during Pause-IR if an invalid instruction has been loaded.

state diagram description (continued)

Update-IR

In this state, the latches shadowing the instruction register are updated with the new instruction. If an invalid instruction is present in the IR and the TAP enters this state, the BYPASS instruction is executed. If the TAP does not pass through Test-Logic-Reset before the next Capture-IR TAP state, Bit 7 of the IR preloads with a logic 0 during Capture-IR.

TABLE 1. REGISTER SUMMARY

REGISTER NAME	SYMBOL	LENGTH (BITS)	FUNCTION/CONTENTS
Instruction	IR	8	Issue command and control information to the device
Test Cell	TCR	16	PSA operations, compare functions on D inputs
Control	CTLR	45	Configuration and enable control, data mask and PSA tap bits
RAM	RAMR	26/16†	Address and read/write data for 1024 x 16 RAM
Event Qualification 1	EQR1	32	Control signals, EQM test instruction, 16-bit loop counter
Event Qualification 2	EQR2	56/48†	Address and data for event count, expected data, and compare mask data
Boundary Scan	BSR	24	Capture and force test data at I/O periphery
Header	HR	8	DMA triggering/compare pattern
Bypass	BR	1	Removes the 'ACT8994 from the scan path

† The length of this register depends on the current instruction. See **instruction register opcode descriptions** for details.

'ACT8994 registers

The device contains nine serial shift registers that contain the configuration data needed to run various test operations. Included in the registers are one eight-bit instruction register and eight data registers of varying lengths. Any register can be accessed via the TAP to load new data and/or examine existing data. Table 1 summarizes the registers, and Figure 2 shows how the data registers are connected. The select signals for MUX1 in the diagram are determined by the current instruction. The select signal for MUX2 is issued by the TAP. Unless one of the four DMA instructions is active, one of the registers between TDI and TDO is always selected for shift operations.

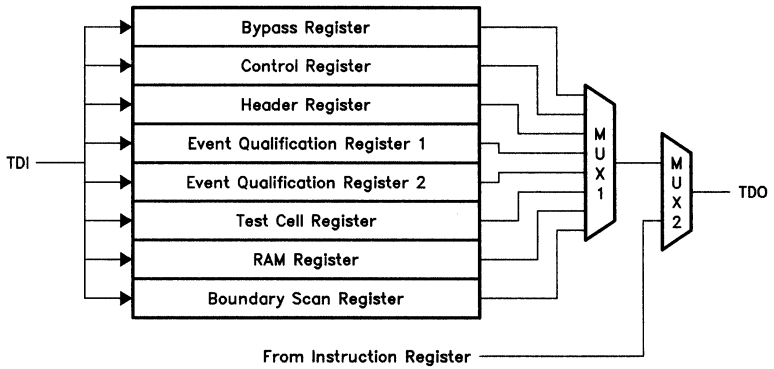

FIGURE 2. DATA REGISTER DIAGRAM

instruction register description

The eight-bit instruction register (IR) contains the current instruction to the device. All operations of the device are dependent on the current instruction, which is decoded and latched to provide the proper control and enable signals for the test operation to be performed. The instructions supported in the 'ACT8994, a description of the test, and the selected data register (i.e., the data register placed between TDI and TDO for any subsequent shift operations) are shown in Table 2.

The reset value of the IR is 81h. (In this datasheet, the values of registers are often given in hexadecimal format, indicated by the 'h' following the value.) During Capture-IR, the instruction register preloads with the IR status word (see Table 3), which contains two status bits, $\overline{\text{IRERR}}$ and OVF.

All valid instructions exhibit even parity. If the IR value does not exhibit even parity and the TAP enters the pause-IR state, the error signal $\overline{\text{IRERR}}$ (a logic 0) is generated and is output via EQO if the appropriate bits in the control register are set. If an invalid instruction is updated, $\overline{\text{IRERR}}$ stays active and is loaded into bit 7 of the IR during the next Capture-IR TAP state (unless the TAP passes through Test-Logic-Reset in the interim). When an invalid instruction is loaded (i.e., when the TAP enters Update-IR while an invalid instruction is in the IR), the BYPASS instruction is executed.

The overflow (OVF) status signal is generated if the RAM address counter is incremented past its maximum value of 3FFh during a DMA or storage operation. OVF is active-high and is written to bit 6 of the IR during Capture-IR. A bit in the control register can be set to prohibit the address counter from overflowing, but OVF is still asserted if the test attempts to do so.

Figure 3 shows the instruction register bits and order of scan.

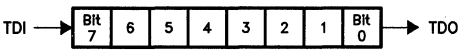

FIGURE 3. INSTRUCTION REGISTER BITS AND ORDER OF SCAN

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TABLE 2. INSTRUCTION REGISTER OPCODES

BINARY OPCODE	HEX VALUE	INSTRUCTION	SELECTED DATA REGISTER
00000000	00h	EXTEST	Boundary Scan
10000001	81h	BYPASS	Bypass
10000010	82h	SAMPLE/PRELOAD	Boundary Scan
00000011	03h	BYPASS	Bypass
10001000	88h	RUNN	Bypass
00001001	09h	RUNT	Bypass
10001110	8Eh	SCANCN	Control
00010001	11h	SCANEQN	Event Qualification 1
01100000	60h	READFILE	Event Qualification 2
11100001	E1h	WRITEFILE	Event Qualification 2
11100010	E2h	READRAM	RAM
01100011	63h	WRITERAM	RAM
11100100	E4h	DMARIN	RAM†
01100101	65h	DMAROUT	RAM†
01100110	66h	DMAFIN	Event Qualification 2†
11100111	E7h	DMAFOUT	Event Qualification 2†
11101000	E8h	SCANTCR	Test Cell
01101001	69h	READTCR	Test Cell
01101010	6Ah	INITRAM	Bypass
11101011	EBh	TOGRAM	Bypass
01101100	6Ch	PSARAM	Bypass
11101101	EDh	SCANHDR	Header
All other		BYPASS	Bypass

† DMA instructions are executed while in the Shift-DR TAP state and the normal TDI–TDO data flow is inhibited. The indicated data register is selected only if the TAP leaves and re-enters Shift-DR without loading a new instruction. If this happens, the DMA operation is aborted.

TABLE 3. INSTRUCTION REGISTER STATUS WORD

IR BIT	VALUE‡
7	$\overline{\text{IRERR}}$
6	OVF
5	0
4	0
3	0
2	0
1	0
0	1

‡ This value is loaded in the instruction register during the Capture-IR TAP state. The reset value of $\overline{\text{IRERR}}$ = 1. The reset value of OVF = 0.

register scan timing

Figure 4 shows a timing diagram that illustrates an instruction register scan and a data register scan (in this case, the bypass register) with the TAP beginning in the Test-Logic-Reset state. All register scans, with the exception of the DMA instructions, are executed in the same fashion. Note that the value of TDI is a "don't care" until the first TCK rising edge after the TAP enters Shift-IR or Shift-DR (because the first shift does not occur until then) and that the last shift occurs on the TCK cycle in which the TAP state changes from Shift-IR to Exit1-IR or from Shift-DR to Exit1-DR. Also note that TDO is active only when the TAP state is Shift-IR or Shift-DR.

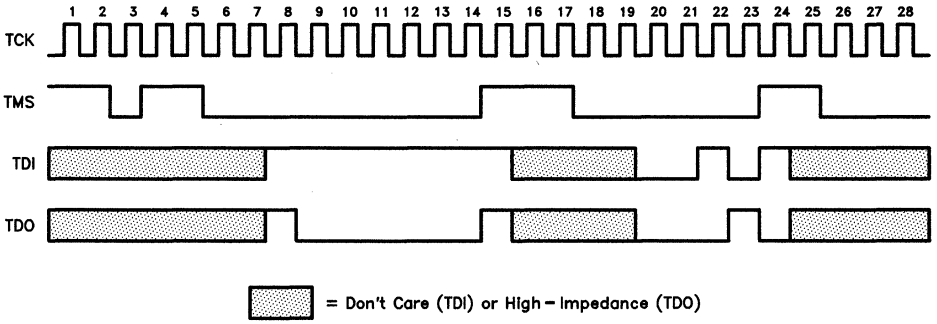

FIGURE 4. REGISTER SCAN TIMING

Other concepts are illustrated in the figure. As a BYPASS instruction (FFh) is shifted into the IR, the reset IR status word (81h) is shifted out via TDO. After the IR is updated with BYPASS (cycle 16), the TAP moves through Select-DR-Scan and Capture-DR to Shift-DR and data is shifted through the bypass register. Since the bypass register is one bit wide (see **bypass register description**), the data is delayed by one bit from TDI to TDO. Another important note is that the last bit shifted into the bypass register (a logic 1 during TCK cycle 24) is not shifted out to the next device in the scan path.

For both the instruction register scan and data register scan, TDO becomes active on the falling edge of TCK as the TAP enters the appropriate shift state. During the instruction register scan, TDO enables to a high level because the LSB of the instruction register always preloads with a logic 1. During the bypass register scan, TDO enables to a low level because the bypass register always preloads with a logic 0.

instruction register opcode descriptions

The basic functions of each instruction are described herein. Example executions for several instructions follow **data register descriptions**.

EXTEST
The boundary scan register is selected in the scan path. Data appearing at the input pins is captured and data previously loaded into the output boundary scan cells is applied from the outputs.

BYPASS
The bypass register is selected in the scan path. All other registers retain their states.

SAMPLE/PRELOAD
Data appearing at the I/O pins is captured on the rising edge of TCK in Capture-DR. The boundary scan register is selected in the scan path.

RUNN
The test operation specified by OP3–OP0 (bits 44–41 in the control register) is performed in the on-line test mode as controlled by the EQM. While RUNN is executing, operation of the device, except for the TAP, is synchronous to the on-line clock generated by the PCI circuit.

Test operations running under RUNN become active at the falling edge of TCK in Update-IR and remain active until they either terminate normally according to the selected protocol (i.e., the protocol reaches END OF TEST) or a new instruction is loaded and updated. This allows RUNN to operate in the background mode. If an instruction register scan occurs while RUNN is active and the new instruction loaded and updated is also RUNN, no disruption in the on-line test will occur (cascaded PSA operations are affected, however. See **cascaded PSA operations**).

RUNT
The test operation specified by OP3–OP0 (bits 44–41 in the control register) is performed in the off-line test mode and is synchronous to TCK. Test operations running under RUNT are active only while the TAP is in the Run-Test/Idle state. The test begins on the first rising edge of TCK after entering Run-Test/Idle and terminates at either the end of the protocol or on the TCK cycle in which the TAP state changes to Select-DR-Scan.

SCANCN
The control register is placed in the scan path. During Capture-DR, the current value of the register is preloaded. All other registers retain their states.

SCANEQN
The event qualification register 1 is placed in the scan path. During Capture-DR, the current value of the register is preloaded. All other registers retain their states.

READFILE
The event qualification register 2 is configured as a 56-bit register and placed in the scan path. During the Capture-DR TAP state, the EQM register file data at the address appearing in bits 39 through 36 is loaded into bits 55 through 40 and the register file data at the address appearing in bits 3 through 0 is loaded into bits 35 through 20 (expected data) and 19 through 4 (compare mask data). During the Update-DR TAP state, the register file addresses for the next Capture-DR/Shift-DR operation are latched. The address and data are offset by one cycle, meaning that the data referenced by a particular address is loaded into the register during the next Capture-DR state.

instruction register opcode descriptions (continued)

WRITEFILE
The event qualification register 2 is configured as a 56-bit register and placed in the scan path. During the Update-DR TAP state, the data in bits 55 through 40 is loaded into the EQM register file at the address appearing in bits 39 through 36 and the data appearing in bits 35 through 20 (expected data) and 19 through 4 (compare mask data) is loaded into the register file at the address appearing in bits 3 through 0.

READRAM
The RAM register is configured as a 26-bit register and placed in the scan path. During the Capture-DR TAP state, the RAM data at the address appearing in bits 9 through 0 is loaded into bits 25 through 10. During the Update-DR TAP state, the RAM address for the next Capture-DR/Shift-DR operation is latched. The address and data are offset by one cycle, meaning that the data referenced by a particular address is loaded into the RAM during the next Capture-DR state.

WRITERAM
The RAM register is configured as a 26-bit register and placed in the scan path. During the Update-DR TAP state, the data in bits 25 through 10 is loaded into the RAM at the address appearing in bits 9 through 0.

DMAFIN
During this DMA instruction, data is loaded via TDI into the register files adjacent to the event qualification register 2 for storing the event count, expected data, and compare data values. While DMAFIN is executing, the output from TDO is meaningless. DMAFIN executes while the TAP is in the Shift-DR state. If the TAP leaves and returns to Shift-DR while DMAFIN is the current instruction, the event qualification register 2 is selected in the scan path and the register file write is aborted. During DMAFIN, the event qualification register 2 is configured as a 48-bit register (the eight address bits are disregarded).

DMAFOUT
The register files of event qualification register 2 are read using this DMA instruction. Data is output via TDO and the data at TDI is ignored. DMAFOUT executes in the Shift-DR state. If the TAP leaves and returns to Shift-DR while DMAFOUT is the current instruction, the event qualification register 2 is selected in the scan path and the register file read is aborted. During DMAFOUT, the event qualification register 2 is configured as a 48-bit register (the eight address bits are disregarded).

DMARIN
During this DMA instruction, data is loaded via TDI into the RAM. While DMARIN is executing, the output from TDO is meaningless. DMARIN executes while the TAP is in the Shift-DR state. If the TAP leaves and returns to Shift-DR while DMARIN is the current instruction, the RAM register is selected in the scan path and the RAM write is aborted.

During DMARIN, the RAM register is configured as a 16-bit register (the ten address bits are disregarded).

DMAROUT
The RAM is read using this DMA instruction. Data is output via TDO and the data at TDI is ignored. DMAROUT executes in the Shift-DR state. If the TAP leaves and returns to Shift-DR while DMAROUT is the current instruction, the RAM register is selected in the scan path and the RAM read is aborted. During DMAROUT, the RAM register is configured as a 16-bit register (the ten address bits are disregarded).

SCANTCR
The test cell register is placed in the scan path. During Capture-DR, the data appearing at the D inputs is preloaded. All other registers retain their last states.

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instruction register opcode descriptions (continued)

READTCR
The test cell register is placed in the scan path. During Capture-DR, the current value of the register is preloaded. All other registers retain their last states. This instruction is primarily useful for reading the results of a PSA operation.

INITRAM
The RAM register is configured as a 26-bit register and selected in the scan path. The value present in RAMR bits 25 through 10 is loaded into the RAM at consecutive addresses beginning with the address contained in RAMR bits 9 through 0. This instruction executes while the TAP is in the Run-Test/Idle state. On each TCK cycle, the RAM address is incremented and the data is loaded into the appropriate RAM location. The first pattern is written into the RAM on the first rising TCK edge after entering Run-Test/Idle, and the last pattern is written on the rising edge of TCK as the TAP state changes from Run-Test/Idle to Select-DR-Scan. The same pattern is written each time.

TOGRAM
The RAM register is selected in the scan path. This instruction is similar to INITRAM, the only difference being that the data to be loaded into the RAM (RAMR bit 25 through 10) is toggled on each TCK cycle. The first pattern written is the true data (the value loaded into the register during Shift-DR). This instruction is useful when a checkerboard pattern or alternating ones and zeroes are to be loaded into the RAM, usually for testing purposes.

PSARAM
The contents of the RAM are loaded into the test cell register on each TCK cycle while the TAP is in Run-Test/Idle. A PSA operation is performed on each pattern, and the resulting signature can be read using READTCR. This instruction is useful for performing a self-test on the RAM. By loading a known pattern or set of patterns using INITRAM or TOGRAM and following with PSARAM, the generated signature can be compared against a known value to verify the RAM functionality.

SCANHDR
The header register is selected in the scan path. All other registers retain their states.

data register descriptions

The following sections contain descriptions of the various data registers in the 'ACT8994. The length of the register, order of scan, and function of the bits are explained. The use of many of the signals described will become apparent later in the datasheet.

control register description

The 45-bit control register (CTLR) issues configuration, control, and enable signals to the device. Table 4 lists the signals of the CTLR. The function of each signal is explained below.

Bits 44–41 OP3–OP0

These four bits control the test operation to be performed during RUNN and RUNT (see Table 15 and **RUNN, RUNT opcode descriptions**). The primary function of the 'ACT8994 is to execute various test operations according to OP3–OP0.

Bit 40 SELDP

During RUNN, either current or registered data may be input into the TCR and/or RAM. Current data is the data present at the D inputs at the rising edge of the clock issued by the PCI. Registered data is the data present at the prior rising edge of the clock. Using registered data allows the device to capture the pattern that preceded the expected data pattern.

If SELDP = 0, use current data as input.
If SELDP = 1, use registered data as input.

Bit 39 HALTM

The RAM can be configured to allow address rollovers (i.e., increment address from 3FFh to 000h) or to halt RAM writes after an address of 3FFh. When rollovers are not allowed, no additional writes to memory are performed after writing to address 3FFh and the address counter stops at 0000h. The overflow status bit, OVF (see **instruction register description**) is set independently of HALTM if an INITRAM, TOGRAM, or DMARIN instruction attempts to continue RAM writes after writing to address 3FFh.

If HALTM = 0, allow address counter to roll over after reaching 3FFh.
If HALTM = 1, do not allow additional RAM writes after reaching 3FFh.

Bit 38 PARENA

The parity error signal generated when an instruction is loaded ($\overline{\text{IRERR}}$) can be output via EQO during the Pause-IR TAP state. PARENA enables and disables this function.

If PARENA = 0, disable parity error output from EQO.
If PARENA = 1, enable parity error output from EQO.

The polarity of the error signal (active-high or active-low) is determined by EQR1 bit 23.

Bit 37 CMPSEL

During RUNN, either current or registered data may input to the EQM to be compared against expected data during EQM-controlled test operations. Along with SELDP (CTLR bit 40), CMPSEL determines the alignment of data during on-line test operations. See **alignment of compare and data signals under RUNN** for illustrations of the use of current and registered data.

If CMPSEL = 0, use current data as compare input.
If CMPSEL = 1, use registered data as compare input.

control register description (continued)

Bit 36 POLSEL

The polarity of the clock generated by the programmable clock interface (PCI) circuit is controlled by POLSEL. (Bits 35–32 determine the logic equation of the clock).

If POLSEL = 0, use true (noninverted) clock from PCI.
If POLSEL = 1, use inverted clock from PCI.

Bits 35-32 SELD-SELA

The PCI generates the internal clock signal for the on-line EQM protocols according to these four bits. See Table 14 and **PCI description** for details.

Bits 31–16 PTAP15–PTAP00

The algorithm used to generate parallel signatures is partially configured using these bits. One of the inputs to the exclusive-OR gates used during PSA is a feedback bit from the LSB of a shift register. The PTAP bits determine which stages of the shift register use the feedback bit as an input.

If PTAPxx = 0, exclude the feedback bit from shift register stage xx.
If PTAPxx = 1, include the feedback bit from shift register stage xx.

See **parallel signature analysis operations** for details of the PTAP bits and their use.

Bits 15–0 DATMSK15–DATMSK00

Any combination of data inputs can be masked during parallel signature analysis operations in the TCR. The inputs are masked using the appropriate DATMSKxx signal. When an input is masked, it is ignored and has no effect on the generated signature.

If DATMSKxx = 0, include Dxx in PSA operation.
If DATMSKxx = 1, mask (exclude) Dxx from PSA operation.

During Capture-DR, the control register preloads with its current value. The reset value of the CTLR is 0000 0000 0000h. The register bits and order of scan are illustrated in Figure 5.

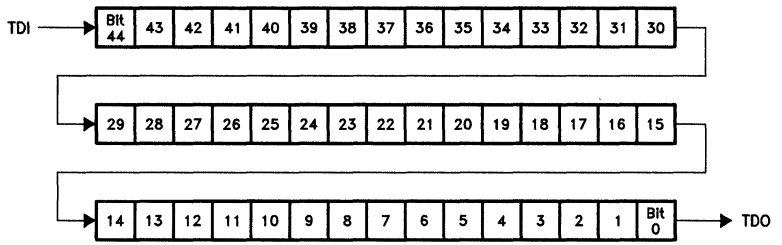

FIGURE 5. CONTROL REGISTER BITS AND ORDER OF SCAN

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TABLE 4. CONTROL REGISTER BITS

BIT NUMBER	SIGNAL	DESCRIPTION
44	OP3	RUNN, RUNT Opcode Bit 3
43	OP2	RUNN, RUNT Opcode Bit 2
42	OP1	RUNN, RUNT Opcode Bit 1
41	OP0	RUNN, RUNT Opcode Bit 0
40	SELDP	Current/Registered Data Select for TCR/RAM Input
39	HALTM	RAM Address Overflow Enable
38	PARENA	Instruction Register Parity Enable
37	CMPSEL	Current/Registered Data Select for EQM Compare
36	POLSEL	PCI Clock Polarity Select
35	SELD	PCI Clock Select D
34	SELC	PCI Clock Select C
33	SELB	PCI Clock Select B
32	SELA	PCI Clock Select A
31	PTAP15	PSA Tap for input D15
30	PTAP14	PSA Tap for input D14
29	PTAP13	PSA Tap for input D13
28	PTAP12	PSA Tap for input D12
27	PTAP11	PSA Tap for input D11
26	PTAP10	PSA Tap for input D10
25	PTAP9	PSA Tap for input D9
24	PTAP8	PSA Tap for input D8
23	PTAP7	PSA Tap for input D7
22	PTAP6	PSA Tap for input D6
21	PTAP5	PSA Tap for input D5
20	PTAP4	PSA Tap for input D4
19	PTAP3	PSA Tap for input D3
18	PTAP2	PSA Tap for input D2
17	PTAP1	PSA Tap for input D1
16	PTAP0	PSA Tap for input D0
15	DATMSK15	Data mask for PSA on input D15
14	DATMSK14	Data mask for PSA on input D14
13	DATMSK13	Data mask for PSA on input D13
12	DATMSK12	Data mask for PSA on input D12
11	DATMSK11	Data mask for PSA on input D11
10	DATMSK10	Data mask for PSA on input D10
9	DATMSK9	Data mask for PSA on input D9
8	DATMSK8	Data mask for PSA on input D8
7	DATMSK7	Data mask for PSA on input D7
6	DATMSK6	Data mask for PSA on input D6
5	DATMSK5	Data mask for PSA on input D5
4	DATMSK4	Data mask for PSA on input D4
3	DATMSK3	Data mask for PSA on input D3
2	DATMSK2	Data mask for PSA on input D2
1	DATMSK1	Data mask for PSA on input D1
0	DATMSK0	Data mask for PSA on input D0

event qualification register 1 description

The event qualification register 1 (EQR1) is a 32-bit register that contains select and enable signals for event-qualified testing. It also contains the 16-bit loop counter, which controls the number of times an EQM protocol is executed. Table 5 lists the EQR1 signals.

Bits 31–29 CMD2–CMD0
These three bits determine the event qualification protocol to be executed as shown in Table 17. See **event qualification protocols.**

Bit 28 SYNEOT
The EOT (end-of-test) signal is active while an event protocol is in the EOT state. It can be cleared synchronously (when a new protocol begins executing) or asynchronously (when the internal RUN signal becomes inactive), depending on the value of SYNEOT.

If SYNEOT = 0, clear EOT asynchronously.
If SYNEOT = 1, clear EOT synchronously.

Bit 27 RACDIS
The RAM address is cleared (set to 000h) at the beginning of an event protocol. RACDIS can be configured to disable this feature.

If RACDIS = 0, the RAM address clear is enabled.
If RACIDS = 1, the RAM address clear is disabled.

Bits 26–23 EQOSELD–EQOSELA
Several status signals and the instruction register parity error signal can be output via EQO during event-qualified testing. The EQO output signal is selected with these four bits according to Table 18.

Bits 22–20 EQISELC–EQISELA
The EQI (event) input to the EQM can be configured to input one of seven different signals during event-qualified testing. This signal is used as the event that triggers certain operations according to the protocol being executed. The input is configured according to these three bits as shown in Table 16.

Bit 19 LCNTDIS
The event loop counter keeps track of the number of times an event protocol has been executed and sets $\overline{\text{LCMIN}}$ low when the value of the counter decrements to one. The loop counter can be disabled with LCNTDIS. If LCNTDIS is set high, the protocol continues execution until a new instruction is loaded in the IR.

If LCNTDIS = 0, the event loop counter is enabled and decrements according to the protocol being executed.
If LCNTDIS = 1, the event loop counter is disabled and does not decrement. Under this condition, $\overline{\text{LCMIN}}$ never becomes active unless the loop counter was originally loaded with the value 0001h.

Bit 18 ECNTDIS
The event counter can be disabled using ECNTDIS in the same way as the loop counter can be disabled using LCNTDIS. When ECNTDIS is set high, the test specified during on-line testing is never executed because all protocols are triggered to begin an operation when the event counter has decremented to one. This feature is useful if EQO is being used to output an internal status signal related to the state of the bus being monitored.

If ECNTDIS = 0, the event counter is enabled and decrements each time an event is observed.
If ECNTDIS = 1, the event counter is disabled and $\overline{\text{ECMIN}}$ never beomes active.

event qualification register 1 description (continued)

Bit 17 POPDIS

During protocol execution, new expected and compare data is often loaded after a protocol has completed a DO TEST loop. The loading of new data can be disabled with POPDIS. If the same expected and compare data are to be used throughout the protocol, setting POPDIS high reduces the amount of data that must be loaded in the EQM register files prior to test execution.

If POPDIS = 0, new data is loaded prior to each event protocol execution.
If POPDIS = 1, the current expected and compare data is used for each event protocol execution.

Bit 16 ENACMP

One of the signals that can be output via EQO is the compare term (CTERM), an asynchronous signal that is active (a logic 1) when the data appearing at the D inputs matches the expected value in the register file. This signal can be output as soon as a match is found (first matching pattern after RUNN has been updated in the IR) or when the event protocol starts execution (internal signal RUN goes active).

If ENACMP = 0, EQO becomes active after protocol execution begins.
If ENACMP = 1, EQO becomes active as soon as a match is found.

Bits 15–0 LCNT15–LCNT00

These bits contain the number of times the event protocol is to be executed. While an event protocol is active, these bits are configured as a counter and decrement prior to each execution. When the value of LCNT15–LCNT00 is 0001h, the status signal $\overline{\text{LCMIN}}$ becomes active (goes to a logic 0).

During Capture-DR, the EQR1 preloads with its current value. The reset value of the EQR1 is 0000 0000h. The register bits and order of scan are illustrated in Figure 6.

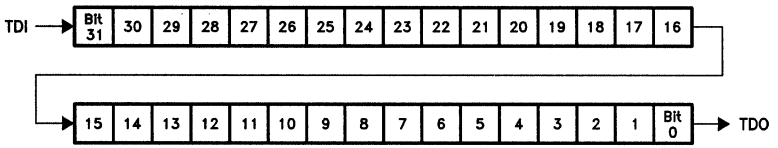

FIGURE 6. EVENT QUALIFICATION REGISTER 1 BITS AND ORDER OF SCAN

TABLE 5. EVENT QUALIFICATION REGISTER 1 BITS

BIT NUMBER	SIGNAL	DESCRIPTION
31	CMD2	EQM Protocol Select 2
30	CMD1	EQM Protocol Select 1
29	CMD0	EQM Protocol Select 0
28	SYNEOT	Synchronous/Asynchronous End Of Test Flag
27	RACDIS	RAM Address Clear Strobe Disable
26	EQOSELD	EQO Select D
25	EQOSELC	EQO Select C
24	EQOSELB	EQO Select B
23	EQOSELA	EQO Select A
22	EQISELC	EQI Select C
21	EQISELB	EQI Select B
20	EQISELA	EQI Select A
19	LCNTDIS	Loop Count Disable
18	ECNTDIS	Event Count Disable
17	POPDIS	Expected and Compare Data Pop Disable
16	ENACMP	Compare Term Enable
15	LCNT15	Loop Count 15
14	LCNT14	Loop Count 14
13	LCNT13	Loop Count 13
12	LCNT12	Loop Count 12
11	LCNT11	Loop Count 11
10	LCNT10	Loop Count 10
9	LCNT09	Loop Count 09
8	LCNT08	Loop Count 08
7	LCNT07	Loop Count 07
6	LCNT06	Loop Count 06
5	LCNT05	Loop Count 05
4	LCNT04	Loop Count 04
3	LCNT03	Loop Count 03
2	LCNT02	Loop Count 02
1	LCNT01	Loop Count 01
0	LCNT00	Loop Count 00

event qualification register 2 description

The event qualification register 2 (EQR2) is used to load the event counter and expected and mask data for event-qualified operations. Depending on the current instruction, it is either 48 or 56 bits in length and can be thought of as three 16-bit segments that hold data to be loaded into or out of register files and two four-bit segments that hold the register file address. One four-bit address segment serves the event counter and the other serves both the expected and mask data register files.

During execution of the IEEE Standard 1149.1-compatible instructions READFILE and WRITEFILE, the register is 56 bits long. During the Capture-DR and Update-DR TAP states, the data appearing in the register's 16-bit segments is loaded into or out of the address specified by one of the register's two four-bit segments.

During execution of the DMA instructions DAMFIN and DMAFOUT, the register is 48 bits long, containing only the three 16-bit data segments. Loading and unloading of the register files occurs in the Shift-DR TAP state as a continuous data stream is shifted in through TDI or out through TDO. On each 48th TCK, the data in the register is loaded into or out of the register file and the register file address is incremented for the next read or write.

Bits 55–40 EVCNT15–EVCNT00
These bits hold the data to be parallel-loaded into or out of the event counter register file.

Bits 39–36 EVADR3–EVADR0
These bits contain the address of the event counter register file.

Bits 35–20 EXPDATA15–EXPDATA00
These bits hold the data to be parallel-loaded into or out of the expected data register file.

Bits 19–4 MSKDAT15–MSKDAT00
These bits hold the data to be parallel-loaded into or out of the compare mask data register file.

Bits 3–0 ECADR3–ECADR0
These bits contain the address of the expected data and compare mask data register files. The same address is used for these registers for any of the four instructions that access the EQR2.

The three register files associated with the EQR2 are each 16 bits wide and 16 words deep. The register signals are shown in Table 6 and the register bits and order of scan are shown in Figure 7. Note that in two places (between bits 40 and 39 are between bits 4 and 3) the order of scan breaks in two. This illustrates the dependence of the register length on the instruction used to access it. The reset value of the EQR2 is 00 0000 0000 000h.

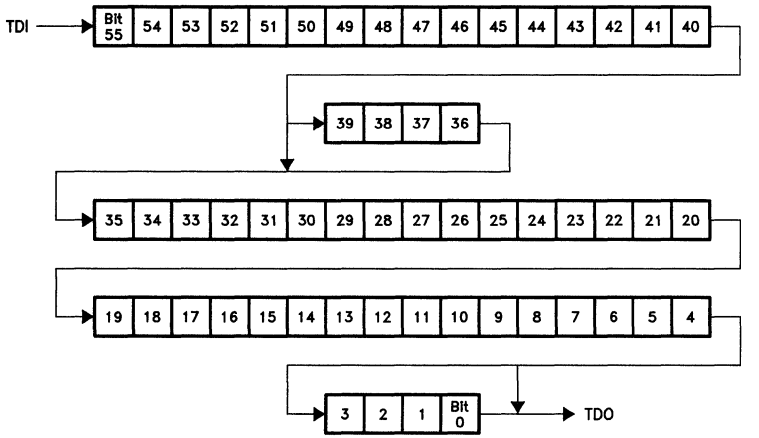

FIGURE 7. EVENT QUALIFICATION REGISTER 2 BITS AND ORDER OF SCAN

TABLE 6. EVENT QUALIFICATION REGISTER 2 BITS

BIT NUMBER	SIGNAL	DESCRIPTION
55	EVCNT15	Event Counter Data 15
54	EVCNT14	Event Counter Data 14
53	EVCNT13	Event Counter Data 13
52	EVCNT12	Event Counter Data 12
51	EVCNT11	Event Counter Data 11
50	EVCNT10	Event Counter Data 10
49	EVCNT09	Event Counter Data 09
48	EVCNT08	Event Counter Data 08
47	EVCNT07	Event Counter Data 07
46	EVCNT06	Event Counter Data 06
45	EVCNT05	Event Counter Data 05
44	EVCNT04	Event Counter Data 04
43	EVCNT03	Event Counter Data 03
42	EVCNT02	Event Counter Data 02
41	EVCNT01	Event Counter Data 01
40	EVCNT00	Event Counter Data 00
39	EVADR3	Event Counter Address 3
38	EVADR2	Event Counter Address 2
37	EVADR1	Event Counter Address 1
36	EVADR0	Event Counter Address 0
35	EXPDAT15	Expected Data 15
34	EXPDAT14	Expected Data 14
33	EXPDAT13	Expected Data 13
32	EXPDAT12	Expected Data 12
31	EXPDAT11	Expected Data 11
30	EXPDAT10	Expected Data 10
29	EXPDAT09	Expected Data 09
28	EXPDAT08	Expected Data 08
27	EXPDAT07	Expected Data 07
26	EXPDAT06	Expected Data 06
25	EXPDAT05	Expected Data 05
24	EXPDAT04	Expected Data 04
23	EXPDAT03	Expected Data 03
22	EXPDAT02	Expected Data 02
21	EXPDAT01	Expected Data 01
20	EXPDAT00	Expected Data 00

TABLE 6. EVENT QUALIFICATION REGISTER 2 BITS (continued)

BIT NUMBER	SIGNAL	DESCRIPTION
19	MSKDAT15	Mask Data 15
18	MSKDAT14	Mask Data 14
17	MSKDAT13	Mask Data 13
16	MSKDAT12	Mask Data 12
15	MSKDAT11	Mask Data 11
14	MSKDAT10	Mask Data 10
13	MSKDAT09	Mask Data 09
12	MSKDAT08	Mask Data 08
11	MSKDAT07	Mask Data 07
10	MSKDAT06	Mask Data 06
9	MSKDAT05	Mask Data 05
8	MSKDAT04	Mask Data 04
7	MSKDAT03	Mask Data 03
6	MSKDAT02	Mask Data 02
5	MSKDAT01	Mask Data 01
4	MSKDAT00	Mask Data 00
3	EMADR3	Expected and Mask Address 3
2	EMADR2	Expected and Mask Address 2
1	EMADR1	Expected and Mask Address 1
0	EMADR0	Expected and Mask Address 0

header register description

The header register (HR) is an eight-bit register used to initiate DMA write operations on the RAM and on the EQM register files. When a DMA write instruction (DMAFIN or DMARIN) is active, the DMA controller compares data being shifted from TDI to TDO against the current value of the HR. If the value of the HR is anything other than 00h, the DMA operation begins on the first TCK cycle after the DMA controller finds a match between the data flow and the HR.

When the value of the HR is 00h, DMA write operations are not initiated by the TDI–TDO data flow but when the TAP state changes from Shift-DR to Pause-DR and back to Shift-DR.

The reset value of the HR is 00h. Figure 8 shows the register bits and order of scan.

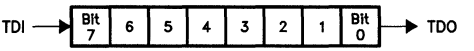

FIGURE 8. HEADER REGISTER BITS AND ORDER OF SCAN

RAM register description

The RAM register (RAMR) is used to load the address and data for RAM read and write operations. Depending on the current instruction, it is either 26 or 16 bits in length and can be thought of as one 16-bit segment that holds data to be loaded into or out of the RAM and one ten-bit segment that holds the RAM address.

During execution of the IEEE Standard 1149.1-compatible instructions READRAM and WRITERAM, the register is 26 bits long. During the Capture-DR and Update-DR TAP states, the data appearing in the register's 16-bit segment is loaded into or read from the RAM at the address specified by the register's ten-bit address segment.

During execution of the DMA instructions DAMRIN and DMAROUT, the register is 16 bits long, containing only the 16-bit data segment. Loading and unloading of the RAM occurs in the Shift-DR TAP state as a continuous data stream is shifted in through TDI or out through TDO. On each 16th TCK, the data in the register is loaded into or out of the RAM and the RAM address is incremented for the next read or write.

Bits 25–10 RAMDAT15–RAMDAT00
These bits hold the data to be parallel-loaded into or out of the addressed RAM location.

Bits 9–0 RAMADR9–RAMADR0
These bits contain the RAM address for read and write operations.

The RAM is 16 bits wide and 1024 words deep. The signals of the register are shown in Table 7 and the register bits and order of scan are shown in Figure 9. Just as with the EQR2, the break in data flow between bits 10 and 9 indicates the dependence of the register length on the current instruction.

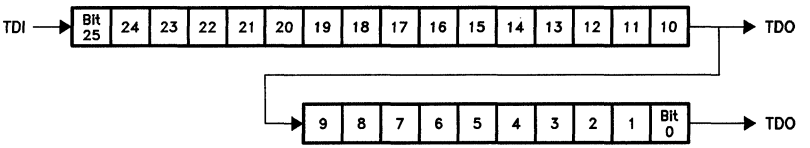

FIGURE 9. RAM REGISTER BITS AND ORDER OF SCAN

TABLE 7. RAM REGISTER BITS

BIT NUMBER	SIGNAL	DESCRIPTION
25	RAMDAT15	RAM Data 15
24	RAMDAT14	RAM Data 14
23	RAMDAT13	RAM Data 13
22	RAMDAT12	RAM Data 12
21	RAMDAT11	RAM Data 11
20	RAMDAT10	RAM Data 10
19	RAMDAT09	RAM Data 09
18	RAMDAT08	RAM Data 08
17	RAMDAT07	RAM Data 07
16	RAMDAT06	RAM Data 06
15	RAMDAT05	RAM Data 05
14	RAMDAT04	RAM Data 04
13	RAMDAT03	RAM Data 03
12	RAMDAT02	RAM Data 02
11	RAMDAT01	RAM Data 01
10	RAMDAT00	RAM Data 00
9	RAMADR9	RAM Address 9
8	RAMADR8	RAM Address 8
7	RAMADR7	RAM Address 7
6	RAMADR6	RAM Address 6
5	RAMADR5	RAM Address 5
4	RAMADR4	RAM Address 4
3	RAMADR3	RAM Address 3
2	RAMADR2	RAM Address 2
1	RAMADR1	RAM Address 1
0	RAMADR0	RAM Address 0

test cell register description

The test cell register (TCR) is a 16-bit register. It performs parallel signature analysis operations on the data inputs or the contents of the RAM and stores the resulting signature to be scanned out and compared against an expected value. The TCR can be accessed by two instructions, SCANTCR and READTCR.

The TCR also contains the results of the SAMPLE/PRELOAD instruction, in which the current value of the D15–D0 data bus is captured.

The reset value of the TCR is 0000h.

The register bits and order of scan are shown in Figure 10.

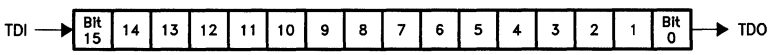

FIGURE 10. TEST CELL REGISTER BITS AND ORDER OF SCAN

boundary scan register description

The boundary scan register (BSR) is a 24-bit register that includes a boundary scan cell for all the non-JTAG I/O pins of the device and one internal directional signal for PIO. The BSR is used to capture the data appearing at the device periphery and to apply data from device outputs.

The reset value of the BSR depends on the current data at the I/O boundary.

Table 8 lists the signals of the BSR. The register bits and order of scan are shown in Figure 11.

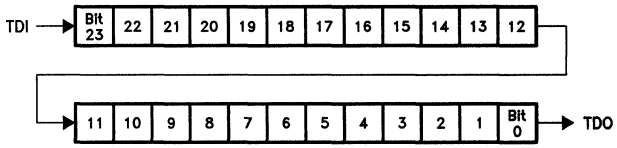

FIGURE 11. BOUNDARY SCAN REGISTER BITS AND ORDER OF SCAN

TABLE 8. BOUNDARY SCAN REGISTER CONFIGURATION

BIT NUMBER	SIGNAL	DESCRIPTION
23	D15	Data Input 15
22	D14	Data Input 14
21	D13	Data Input 13
20	D12	Data Input 12
19	D11	Data Input 11
18	D10	Data Input 10
17	D9	Data Input 9
16	D8	Data Input 8
15	D7	Data Input 7
14	D6	Data Input 6
13	D5	Data Input 5
12	D4	Data Input 4
11	D3	Data Input 3
10	D2	Data Input 2
9	D1	Data Input 1
8	D0	Data Input 0
7	CLK3	Clock 3
6	CLK2	Clock 2
5	CLK1	Clock 1
4	PIO_IN	PIO Input Signal
3	PIO_OUT	PIO Output Signal
2	ENPIO	PIO Direction Control
1	EQI	Event Qualification Input
0	EQO	Event Qualification Output

bypass register description

The bypass register (BR) is a one-bit register required by IEEE Standard 1149.1. It is included to provide an abbreviated scan path through the 'ACT8994 when the current test operations do not require it to load or read one of the other registers.

The bypass register is the selected data register at power-up. The BR is also selected if an invalid instruction is loaded in the IR.

The BR preloads with 0h during the Capture-DR TAP state. The register bit is illustrated in Figure 12.

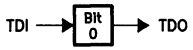

FIGURE 12. BYPASS REGISTER BIT AND ORDER OF SCAN

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instruction execution examples

The following section illustrates the execution of several instructions as well as the resulting data. For these examples, assume that the relevant instruction has been loaded and updated in the IR prior to the data that is shown in the example.

The WRITERAM instruction is illustrated by the data in Table 9. In the table, the term "scan sequence" means the data register Capture/Shift/Exit/Update sequence is used for scanning a data register and updating the contents. During each scan sequence, the data in bits 25 through 10 is loaded into the RAM at the address appearing in bits 9 through 0. Note that during scan sequence 4, RAM address 000h is written to a second time, erasing the data written during sequence 1.

The WRITEFILE instruction executes similarly to WRITERAM, with the event qualification register 2 being used to access the register files in the EQM.

TABLE 9. WRITERAM EXECUTION

SCAN SEQUENCE	RAM REGISTER CONTENTS		RAM CONTENTS†	
	BITS 25 → 10	BITS 9 → 0	ADDRESS	DATA
1	0101 0101 0101 0101	00 0000 0000	00 0000 0000	0101 0101 0101 0101
2	1010 1010 1010 1010	00 0000 0001	00 0000 0001	1010 1010 1010 1010
3	1111 0000 1111 0000	00 0000 0010	00 0000 0010	1111 0000 1111 0000
4	0000 1111 0000 1111	00 0000 0000	00 0000 0000	0000 1111 0000 1111
5	1111 0000 0000 1111	00 0000 0011	00 0000 0011	1111 0000 0000 1111

† The RAM contents are updated on the falling edge of TCK in Update-DR.

Table 10 illustrates the offset between data and address used by the READRAM instruction. In this example, READRAM is used to read the contents of the RAM, which is assumed to be the data written using the WRITERAM instruction in the prior example.

Since the data read during the Capture-DR TAP state is taken from the current address (bits 9 through 0), scan sequence 1 is used to load the first address to be read and the remainder of the register is a "don't care". During scan cycle 2, two things happen. First, during Capture-DR, the data in RAM address 000h is preloaded into bits 25 through 10 of the register. Second, the next address to be read is scanned into the register during Shift-DR. The value scanned into bits 25 through 10 during Shift-DR is irrelevant since these bits will be overwritten with data from the RAM during the Capture-DR TAP state of scan sequence 3.

READFILE executes similarly to READRAM, with the event qualification register 2 accessing the EQM's register files.

TABLE 10. READRAM EXECUTION

SCAN SEQUENCE	RAM REGISTER CONTENTS†	
	BITS 25 → 10	BITS 9 → 0
1	xxxx xxxx xxxx xxxx	00 0000 0000
2	0000 1111 0000 1111	00 0000 0001
3	1010 1010 1010 1010	00 0000 0010
4	1111 0000 1111 0000	00 0000 0011
5	1111 0000 0000 1111	xx xxxx xxxx

† The data in bits 25 through 10 is the value of the RAM as captured in the register. The data in bits 9 through 0 is the next address to be read as scanned in via TDI.
x = don't care.

The READRAM, WRITERAM, READFILE, and WRITEFILE instructions are useful when a small amount of data is to be written to or read from the RAM or EQM register files and are provided for strict adherence to IEEE Standard 1149.1. However, DMA instructions are often more efficient when large amounts of data are to be transferred. DMAFIN, the DMA instruction to load the register files, is illustrated in Table 11. For this example, the user wishes to load the register files with all ones and then return to the Run-Test/Idle state. The table shows the procedure required to do this using DMAFIN. Recall that there are two methods to initiate DMA operations, one using the header register and one using the Pause-DR TAP state. This example initiates DMA using the Pause-DR method, which means that the value of the HR must be 00h (see **header register description**). Assume that at TCK cycle 0 the TAP is moving from Update-IR to Run-Test/Idle after having loaded and updated 66h (DMAFIN) in the IR.

TABLE 11. DMAFIN EXECUTION

TCK CYCLE	TMS‡	TDI‡	COMMENT
0	L	X	Update-IR → Run-Test/Idle
1	H	X	Run-Test/Idle → Select-DR-Scan
2	L	X	Select-DR-Scan → Capture-DR
3	L	X	Capture-DR → Shift-DR
4	H	X	Shift-DR → Exit1-DR
5	L	X	Exit1-DR → Pause-DR, start DMA during next Shift-DR
6	H	X	Pause-DR → Exit2-DR
7	L	X	Exit2-DR → Shift-DR
8–774	L	H	Load register files using Shift-DR state, loop for 767 TCK cycles
775	H	H	Shift-DR → Exit1-DR, perform last shift
776	H	X	Exit1-DR → Update-DR
777	L	X	Update-DR → Run-Test/Idle

‡ Value must be present at the rising edge of TCK.

The DMA instruction for loading the RAM, DMARIN, executes similarly to that in Table 12. In this example, the other method of initiating DMA, comparing the TDI–TDO data flow against the contents of the header register, is illustrated. Prior to executing DMARIN, the user has executed SCANHDR and loaded the HR with F9h, which is used as the trigger pattern for the DMA RAM write.

TABLE 12. DMARIN EXECUTION

TCK CYCLE	TMS†	TDI†	COMMENT
0	L	X	Update-IR → Run-Test/Idle
1	H	X	Run-Test/Idle → Select-DR-Scan
2	L	X	Select-DR-Scan → Capture-DR
3	L	X	Capture-DR → Shift-DR
4	L	H	Shift-DR, begin looking for header pattern (F9h)
5	L	H	
6	L	H	
7	L	L	
8	L	L	
9	L	H	
10	L	H	
11	L	H	
12	L	H	
13	L	H	Prior eight bits now match the value of the HR, begin DMA next cycle
14–1036	L	L	Load RAM using Shift-DR state, loop for 1023 TCK cycles
1037	H	L	Shift-DR → Exit1-DR, perform last shift
1038	H	X	Exit1-DR → Update-DR
1039	L	X	Update-DR → Run-Test/Idle

†Value must be present at the rising edge of TCK.

The fastest way (fewest clock cycles required) to load the RAM is to use INITRAM or TOGRAM. These instructions are applicable when the same data pattern is to be loaded in each RAM location or when the data in each location is to be the inverse of the data in an adjacent location. To begin the procedure, the user should load the IR with WRITERAM and scan the RAMR with the data to be written and the starting address. After this is complete, scan the IR with INITRAM or TOGRAM and loop in the Run-Test/Idle state as shown in Table 13 for 1023 TCK cycles (if the entire RAM is to be loaded). The final RAM location is written to as the TAP state changes from Run-Test/Idle to Select-DR-Scan.

Assume that the RAMR has been loaded with the value 3AAA800h. Bits 9 through 0 (the ten address bits) are 000h, and bits 25 through 10 (the sixteen data bits) are AAAAh. If INITRAM is executed according to the table, each RAM location will contain the value AAAAh. If TOGRAM is executed instead of INITRAM, the RAM will contain alternating patterns of AAAAh and 5555h, beginning with AAAAh in location 000h and ending with 5555h in location 3FFh.

TABLE 13. INITRAM, TOGRAM EXECUTION

TCK CYCLE	TMS‡	COMMENT
0	L	Update-IR → Run-Test/Idle
1–1023	L	Loop in Run-Test/Idle, load RAM
1024	H	Run-Test/Idle → Select-DR-Scan, start next operation

‡ Value must be present at the rising edge of TCK.

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PCI description

The programmable clock interface (PCI) circuit generates the on-line clock used for test operations run under the RUNN instruction. By driving the CLK1, CLK2, and/or CLK3 inputs with system clock, status, interrupt, ready, or any of a number of other signals, the user can synchronize on-line test operations to different system conditions. The device issues its on-line clock according to one of several logic equations (see Table 14). The PCI increases the flexibility of the device by allowing on-line test operations to be triggered by multiple real-time system signals.

TABLE 14. PCI LOGIC EQUATIONS

POLSEL (CTLR BIT 36)	SELD (CTLR BIT 35)	SELC (CTLR BIT 34)	SELB (CTLR BIT 33)	SELA (CTLR BIT 32)	RUNN ON-LINE CLOCK (OCLK)
0	0	0	0	0	TCK†
0	0	0	0	1	CLK1†
0	0	0	1	0	CLK2†
0	0	0	1	1	CLK3†
0	0	1	0	0	$\overline{CLK1}\bullet\overline{CLK2}$
0	0	1	0	1	$CLK1\bullet\overline{CLK2}$
0	0	1	1	0	$\overline{CLK1}\bullet CLK2$
0	0	1	1	1	$CLK1\bullet CLK2$
0	1	0	0	0	$\overline{CLK1}\bullet\overline{CLK2}\bullet\overline{CLK3}$
0	1	0	0	1	$CLK1\bullet\overline{CLK2}\bullet\overline{CLK3}$
0	1	0	1	0	$\overline{CLK1}\bullet CLK2\bullet\overline{CLK3}$
0	1	0	1	1	$CLK1\bullet CLK2\bullet\overline{CLK3}$
0	1	1	0	0	$\overline{CLK1}\bullet\overline{CLK2}\bullet CLK3$
0	1	1	0	1	$CLK1\bullet\overline{CLK2}\bullet CLK3$
0	1	1	1	0	$\overline{CLK1}\bullet CLK2\bullet CLK3$
0	1	1	1	1	$CLK1\bullet CLK2\bullet CLK3$
1	0	0	0	0	$\overline{TCK}$
1	0	0	0	1	$\overline{CLK1}$
1	0	0	1	0	$\overline{CLK2}$
1	0	0	1	1	$\overline{CLK3}$
1	0	1	0	0	$CLK1 + CLK2$
1	0	1	0	1	$\overline{CLK1} + CLK2$
1	0	1	1	0	$CLK1 + \overline{CLK2}$
1	0	1	1	1	$\overline{CLK1} + \overline{CLK2}$
1	1	0	0	0	$CLK1 + CLK2 + CLK3$
1	1	0	0	1	$\overline{CLK1} + CLK2 + CLK3$
1	1	0	1	0	$CLK1 + \overline{CLK2} + CLK3$
1	1	0	1	1	$\overline{CLK1} + \overline{CLK2} + CLK3$
1	1	1	0	0	$CLK1 + CLK2 + \overline{CLK3}$
1	1	1	0	1	$\overline{CLK1} + CLK2 + \overline{CLK3}$
1	1	1	1	0	$CLK1 + \overline{CLK2} + \overline{CLK3}$
1	1	1	1	1	$\overline{CLK1} + \overline{CLK2} + \overline{CLK3}$

† Available for both RUNN and RUNT.

TABLE 15. RUNN, RUNT OPCODES

OP3 (CTLR BIT 44)	OP2 (CTLR BIT 43)	OP1 (CTLR BIT 42)	OP0 (CTLR BIT 41)	OPCODE/FUNCTION
0	0	0	0	Sample
0	0	0	1	Sample
0	0	1	0	Sample
0	0	1	1	Sample
0	1	0	0	PSA, no cascade
0	1	0	1	PSA, MSD cascade
0	1	1	0	PSA, MID cascade
0	1	1	1	PSA, LSD cascade
1	0	0	0	Trace
1	0	0	1	Trace
1	0	1	0	Trace
1	0	1	1	Trace
1	1	0	0	Trace and PSA, no cascade
1	1	0	1	Trace and PSA, MSD cascade
1	1	1	0	Trace and PSA, MID cascade
1	1	1	1	Trace and PSA, LSD cascade

RUNN, RUNT opcode description

The primary functions of the 'ACT8994 are those opcodes run under the RUNN and RUNT instructions. The test operation performed is determined by OP3–OP0 (CTLR bits 44 through 41) as shown in Table 15. During the event protocols (see **event protocol description**), the opcodes below are executed in the DO TEST state:

SAMPLE
The data at the D inputs is captured in the TCR, taking a snapshot of the current data.

PSA
A parallel signature analysis is performed on the data appearing at the D inputs. The TCR is configured as a linear-feedback shift register (LFSR) according to the conditions previously loaded in PTAP15–PTAP00. See **parallel signature analysis operations** for details of PSA tests.

Four opcodes initiate the PSA operation, and there are four different options for cascading more than one DBM (see **cascaded PSA operations**):

No cascade: The PIO pin is placed in the high-impedance state, and the device's TDI and TDO pins perform their normal function.

MSD cascade: The device is configured as the most significant device in a multiple-DBM PSA chain. The TDI input is ignored and the LFSR data is shifted out via TDO to a middle significant DBM. PIO is configured as an input.

MID cascade: The device is configured as a middle significant device (neither most nor least significant) in a multiple-DBM PSA chain. TDI accepts serial LFSR input, and the LFSR data is shifted out via TDO. PIO is configured as an input.

LSD cascade: The device is configured as the least significant device in a multiple-DBM PSA chain. TDI is the serial input in the LFSR chain, and TDO is placed in the high-impedance state. PIO is configured as an output.

RUNN, RUNT opcode description (continued)

TRACE

The data appearing at the D inputs is stored in the RAM. The RAM address is cleared to 000h prior to execution (unless RACDIS = 1) and is incremented after each write cycle. The device can be configured to allow write cycles to continue after the maximum address is reached (thus overwriting data) or to discontinue write cycles after RAM address 03FFh has been written to.

TRACE/PSA

The TRACE and PSA operations are executed simultaneously. The same PSA cascading options available under PSA are available under TRACE/PSA.

event qualification module description

The EQM controls test operations in the on-line mode. It contains an event controller to issue enable and control signals, a programmable clock interface circuit to issue the on-line clock, and register files to store the loop counter, event counter, expected (compare) data, and mask data.

When RUNN is the current instruction, on-line test operations are active according to one of eight protocols. The protocols are state machines synchronous to the on-line clock (in the descriptions and diagrams of EQM operations and protocols, the on-line clock is referred to as OCLK). There are eight protocols that may be executed, all of which use three status signals to determine the next state. Those signals are EVENT, $\overline{\text{ECMIN}}$, and $\overline{\text{LCMIN}}$.

EVENT is an active-high signal and indicates that a protocol is to be triggered. Table 16 lists the signals that may be chosen to assert EVENT.

EVENT = 1 if the selected condition(s) exists.
EVENT = 0 otherwise.

$\overline{\text{ECMIN}}$, the event counter minimum indicator, is an active-low signal and becomes active (goes low) when the event counter (EQR2 bits 55 through 40) has decremented to one, indicating that the event has occurred the specified number of times. Note that the event counter does not necessarily decrement on each match found. There must be one non-event between events for the EQM to recognize the events as separate and decrement the event counter (this is illustrated in Figure 13). In the example of the figure, the event counter is set to 2h and the expected data pattern (EQR2 bits 15 through 0) is 0001h.

$\overline{\text{ECMIN}}$ = 0 if the event counter = 1.
$\overline{\text{ECMIN}}$ = 1 otherwise.

$\overline{\text{LCMIN}}$, the loop counter minimum indicator, is an active-low signal and becomes active (goes low) when the loop counter (EQR1 bits 15 through 0) has decremented to one, indicating that the event protocol has executed the specified number of times.

$\overline{\text{LCMIN}}$ = 0 if the loop counter = 1.
$\overline{\text{LCMIN}}$ = 1 otherwise.

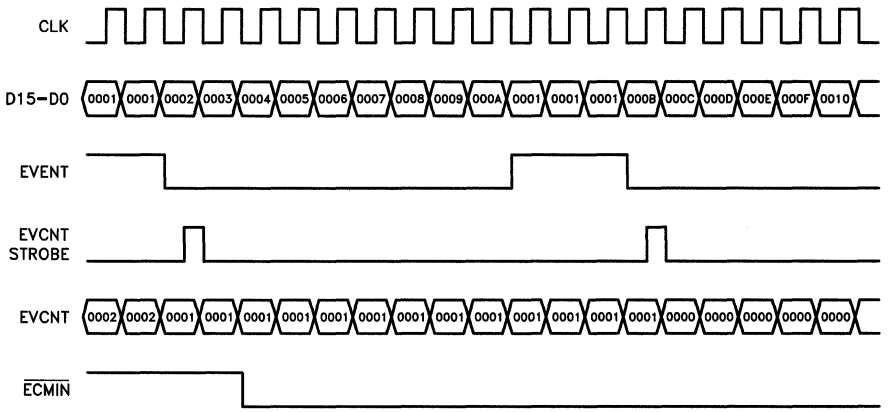

FIGURE 13. EVENT COUNTER

TABLE 16. EVENT SELECT

EQISELC (EQR1 BIT 22)	EQISELB (EQR1 BIT 21)	EQISELA (EQR1 BIT 20)	EVENT†
0	0	0	CTERM
0	0	1	DCTERM
0	1	0	EQI
0	1	1	$\overline{\text{EQI}}$
1	0	0	DEQI
1	0	1	$\overline{\text{DEQI}}$
1	1	0	L
1	1	1	L

† EVENT is the active-high signal used for triggering EQM protocols.

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EVENT signal descriptions

CTERM
This asynchronous signal becomes active when the EQM compare cells detect a match between the D input data and the expected data from the EQM register files. CTERM is enabled by ENACMP in the EQR1 to become active either on the first match after the RUNN instruction is executed or on the first match after an event protocol has started.

DCTERM
DCTERM is a synchronized version of CTERM. DCTERM becomes active on the first rising edge of OCLK after CTERM becomes valid.

EQI
EQI is the level present at the EQI input pin.

$\overline{\text{EQI}}$
$\overline{\text{EQI}}$ is the inverse of the level present at the EQI input pin.

DEQI
The synchronized version of EQI is DEQI, which becomes valid on the rising edge of OCLK.

$\overline{\text{DEQI}}$
$\overline{\text{DEQI}}$ is the inverse of DEQI.

event qualification protocols

The on-line test operations implemented using the RUNN instruction are executed according to one of eight protocols. CMD2–CMD0 are decoded as shown in Table 17 to select the protocol.

TABLE 17. EQM PROTOCOL DECODE

CMD2 (EQR1 BIT 32)	CMD1 (EQR1 BIT 31)	CMD0 (EQR1 BIT 30)	SELECTED EQM PROTOCOL
0	0	0	Protocol 1
0	0	1	Protocol 2
0	1	0	Protocol 3
0	1	1	Protocol 4
1	0	0	Protocol 5
1	0	1	Protocol 6
1	1	0	Protocol 7
1	1	1	Protocol 8

The state machines for the eight on-line protocols are shown in Figures 14 through 21. Decisions are made by the protocol state machine based on the values of the internal signals EVENT, $\overline{\text{ECMIN}}$, and $\overline{\text{LCMIN}}$ as shown in the figures. The term DO TEST in the figures refers to the RUNN opcode selected by OP3–OP0. Although any of the opcodes may be executed with any of the protocols, certain tests are more compatible with some protocols than with others.

The EQM operates synchronously to the on-line clock, OCLK, which is issued by the PCI as described earlier (see **PCI description**).

The EQM register files hold the expected and compare mask data used for triggering test operations as well as the event and loop counters. The addresses of the register files and the RAM are reset to all zeroes prior to the execution of any protocol.

There are two counters associated with the protocols. Each counter performs one of two functions during the protocol execution. The event counter keeps track of the number of times EVENT (which is based on some signal(s) as selected by the current protocol) becomes active, and decrements accordingly, or it delays the start of test execution for a certain number of OCLK cycles. The loop counter keeps track of the number of times the protocol has been executed or specifies the number of clocks for which a test is to be executed. The protocol terminates when the loop counter has decremented.

Protocols can be initiated by the signal present on EQI. This is useful when a test operation is to be triggered by a signal from the outside world. The signal input to EQI is configurable as shown previously in Table 16 to provide additional flexibility.

In Figures 14 through 21, four signals are indicated in the state diagrams, and they represent actions that occur at certain points in the execution of the protocols. The four signals are:

DEC: decrement the event counter.

DLC: decrement the loop counter.

LEV: load the event counter with a new value from the register file.

LND: load new expected and compare mask data from the register file.

As new data is loaded into either the event counter or expected and compare mask data, the register file address increments automatically. Data is not erased as it is loaded, and the 16-word deep register files can be re-used (i.e., increment from file address Fh to 0h and beyond) in the same test operation.

event qualification protocols (continued)

In the protocols and descriptions, the term "event" refers to the signal, as determined according to Table 16, selected to activate the state diagram signal EVENT.

In the protocol descriptions that follow, LCNT and ECNT represent the values of the loop counter and event counter, respectively.

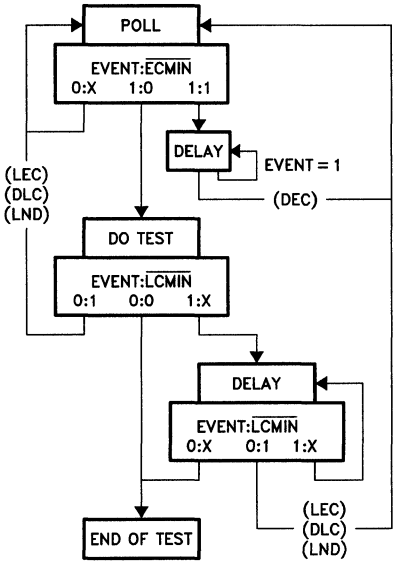


FIGURE 14. EQM PROTOCOL 1

Protocol 1 (see Figure 14) executes a test after an event has been observed a specified number of times and repeats the test for the number of times specified by the loop counter. The test executes once (after the event counter has decremented) for each loop count. Protocol 1 can be summarized as:

```
For LCNT times do
  Begin
    After ECNT events, DO TEST
  End
END OF TEST
```

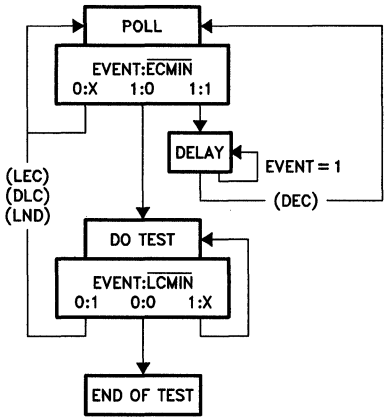


FIGURE 15. EQM PROTOCOL 2

Protocol 2 (see Figure 15) is similar to protocol 1, the difference being that the specified test executes while the event is valid, rather than only once after the event is observed. This protocol provides a do-while test and is useful when EQI is used to trigger EVENT. The protocol can be summarized as:

```
For LCNT times do
  Begin
    After ECNT events, DO TEST while EVENT = 1
  End
END OF TEST
```

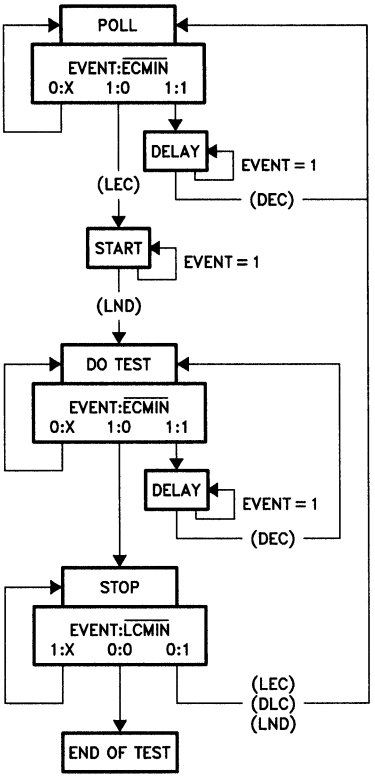


FIGURE 16. EQM PROTOCOL 3

Protocol 3 (see Figure 16) recognizes separate start and stop events. The test begins execution after a certain event occurs and stops after another (possibly different) event occurs. If the start and stop events are patterns (i.e., one of the compare terms is used as the event trigger), they are contained in consecutive register file locations. Protocol 3 can be summarized as:

```
For LCNT times do
  Begin
    After ECNT events, start DO TEST
    After ECNT events, stop DO TEST
  End
END OF TEST
```

Note that, although ECNT appears twice in the protocol summary, the user can specify different values for the start and stop events, as the event counter is reloaded after the test begins.

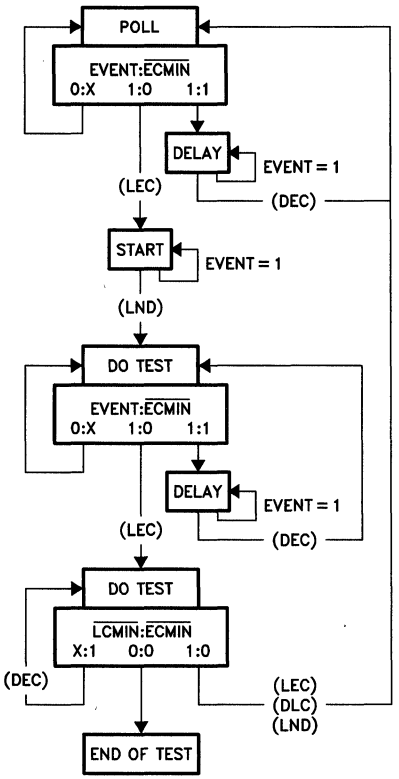


FIGURE 17. EQM PROTOCOL 4

Protocol 4 (see Figure 17) is similar to Protocol 3, the difference being that after the stop event has occurred, the test continues for some number of OCLKs. Protocol 4 can be summarized as:

For LCNT times do
  Begin
    After ECNT events, start DO TEST
    After ECNT events, stop DO TEST after ECNT OCLKs
  End
END OF TEST

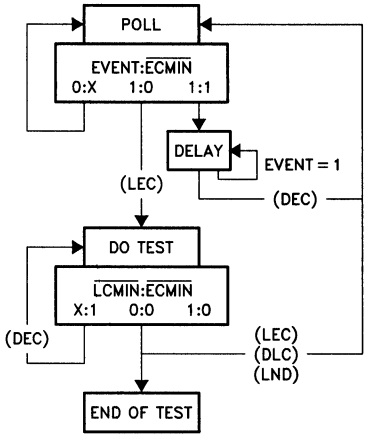


FIGURE 18. EQM PROTOCOL 5

Protocol 5 (see Figure 18) specifies that the test be executed for some number of OCLKs after an event has occurred and can be summarized as:

For LCNT times do
  Begin
    After ECNT events, DO TEST for ECNT OCLKs
  End
END OF TEST

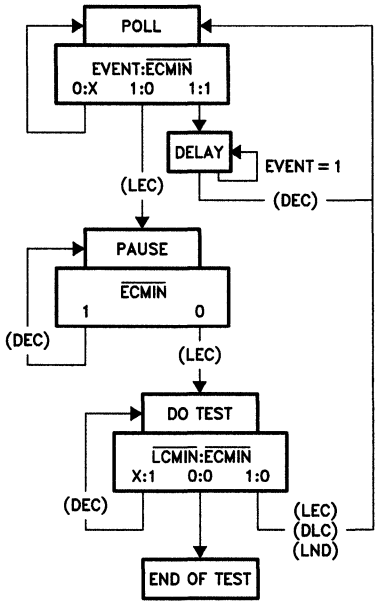


FIGURE 19. EQM PROTOCOL 6

Protocol 6 (see Figure 19) includes a pause for ECNT OCLKs after the triggering event has been observed.

```
For LCNT times do
  Begin
    After ECNT events, pause for ECNT OCLKs
    DO TEST for ECNT OCLKs
  End
END OF TEST
```

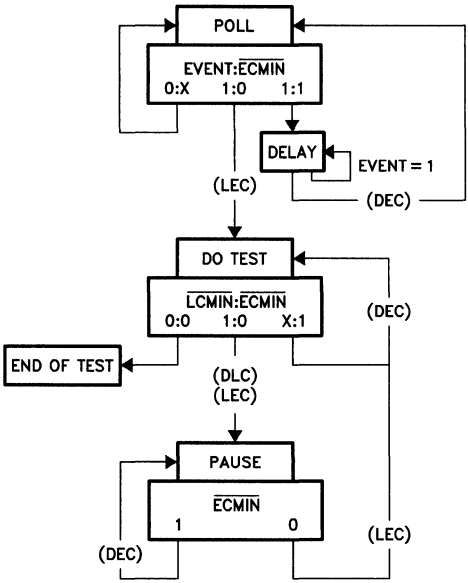


FIGURE 20. EQM PROTOCOL 7

During protocol 7 (see Figure 20), a test is executed after an event occurs without an intermediate pause; following that, the pause/test algorithm is implemented. The protocol summary is:

After ECNT events, DO TEST for ECNT OCLKs For (LCNT − 1) times do
  Begin
    Pause for ECNT OCLKs
    DO TEST for ECNT OCLKs
  End
END OF TEST

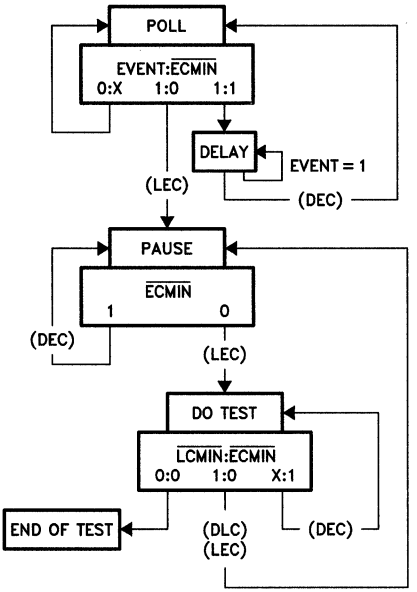


FIGURE 21. EQM PROTOCOL 8

Protocol 8 (see Figure 21) starts a pause/test algorithm after a number of events are observed and can be summarized as:

After ECNT events, For LCNT times do
  Begin
    Pause for ECNT OCLKs
    DO TEST for ECNT OCLKs
  End
END OF TEST

EQO output during RUNN

Any of several internal status signals can be selected to be output via EQO during online testing as shown in Table 18.

TABLE 18. EQO SELECT†

EQOSELD (EQR1 BIT 26)	EQOSELC (EQR1 BIT 25)	EQOSELB (EQR1 BIT 24)	EQOSELA (EQR1 BIT 23)	EQO OUTPUT SIGNAL
0	0	0	0	H
0	0	0	1	L
0	0	1	0	EOT
0	0	1	1	$\overline{\text{EOT}}$
0	1	0	0	RUN
0	1	0	1	$\overline{\text{RUN}}$
0	1	1	0	TGATE
0	1	1	1	$\overline{\text{TGATE}}$
1	0	0	0	CTERM
1	0	0	1	$\overline{\text{CTERM}}$
1	0	1	0	DCTERM
0	0	1	1	$\overline{\text{DCTERM}}$
1	1	0	0	H
1	1	0	1	L
1	1	1	0	H
1	1	1	1	L

† This table is valid unless PARENA = 1 (CTLR Bit 38) and the TAP is in the Pause-DR state. See **control register bit description** for details.

CTERM

This asynchronous signal becomes active when the EQM compare cells detect a match between the D input data and the expected data from the EQM register files. CTERM is enabled by ENACMP in the EQR1 to become active either on the first match after the RUNN instruction is executed or on the first match after an event protocol has started. $\overline{\text{CTERM}}$ is the inverse of CTERM. This is the same signal discussed earlier as one of the signals that may be selected to assert EVENT.

DCTERM

DCTERM is a synchronized version of CTERM. DCTERM becomes active on the first rising edge of OCLK after CTERM becomes valid. $\overline{\text{DCTERM}}$ is the inverse of DCTERM. This is the same signal discussed earlier as one of the signals that may be selected to assert EVENT.

RUN

The RUN status signal indicates that an event protocol is active, but not necessarily that a test operation is being performed (i.e., the protocol state machine may or may not be in DO TEST). RUN becomes active as soon as an event protocol begins execution and goes inactive after the protocol has terminated. $\overline{\text{RUN}}$ is the inverse of RUN.

TGATE

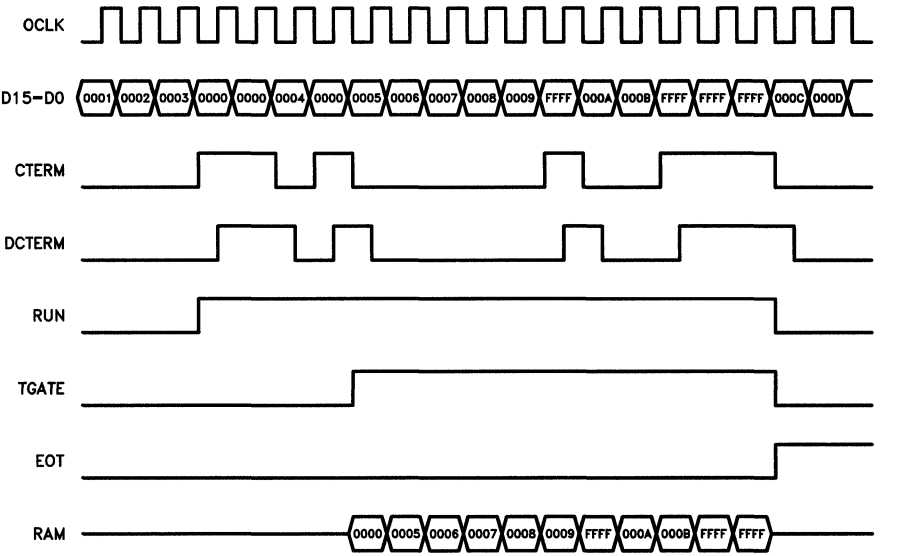
TGATE is active (high) when a test operation under an event qualification protocol is executing (i.e., the protocol state machine is in DO TEST). $\overline{\text{TGATE}}$ is the inverse of TGATE.

EQO output during RUNN (continued)

EOT

The EOT signal goes high when an event protocol enters the end-of-test state, meaning that the event protocol has terminated. $\overline{EOT}$ is the inverse of EOT.

Figure 22 illustrates the relationship of the internal status signals to the test operation.



SELDP = 0
CMPSEL = 0
START EXPDATA = 0000h, EVCNT = 2
STOP EXPDATA = FFFFh, EVCNT = 2
RUNN OPCODE = 1000 = TRACE
EQM Protocol = 3

FIGURE 22. EQM STATUS SIGNALS

operation under RUNT

Under RUNT, which is active only in the Run-Test/Idle state, the current data at the D inputs (i.e., the value of D15–D0 at the rising edge of the selected clock) is input into the TCR and/or RAM. Figure 23 shows the timing for a TRACE operation under RUNT, and the contents of the RAM after several write cycles have occurred. The first pattern stored is the one present at the first rising edge of the clock after entering Run-Test/Idle, and the last pattern stored is the one present at the rising edge of the clock as the TAP state changes from Run-Test/Idle to Select-DR-Scan.

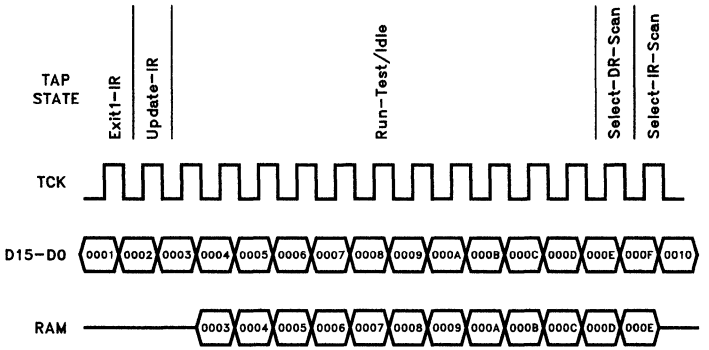


FIGURE 23. RUNT TIMING DIAGRAM

alignment of compare and data signals under RUNN

Under RUNN, several options are available for the compare function and storage of data as controlled by SELDP and CMPSEL (CTLR bits 40 and 37, respectively). The data input in both the RAM (and/or TCR) and the EQM compare circuitry can be delayed one clock cycle to implement the desired test methodology. The four options are illustrated in Figures 24 through 27, which illustrate the alignment of compare and data signals for a portion of a TRACE operation under RUNN. In the figures, the compare pattern to start the operation is 0003h and the compare pattern to stop the operation is 000Fh. The data alignment is the same for any test that runs under RUNN.

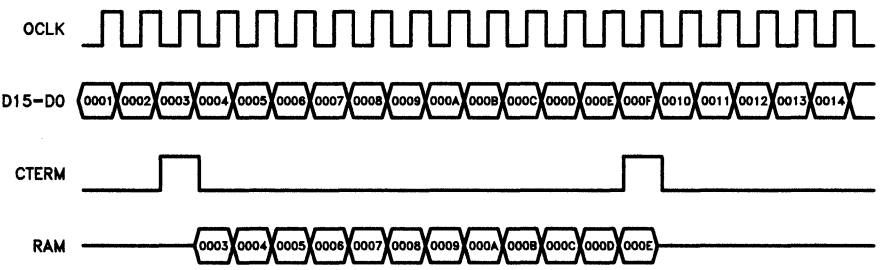


FIGURE 24. RUNN TIMING DIAGRAM: SELDP = 0, CMPSEL = 0

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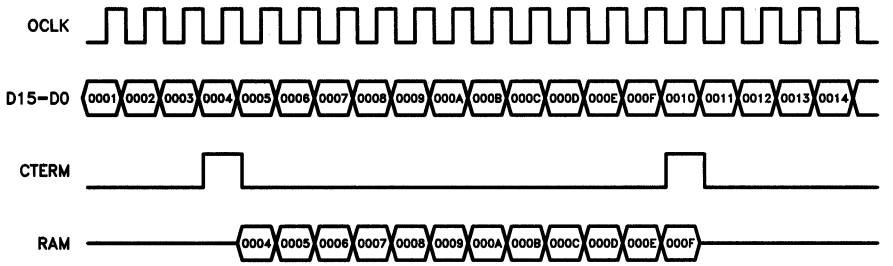

FIGURE 25. RUNN TIMING DIAGRAM: SELDP = 0, CMPSEL = 1

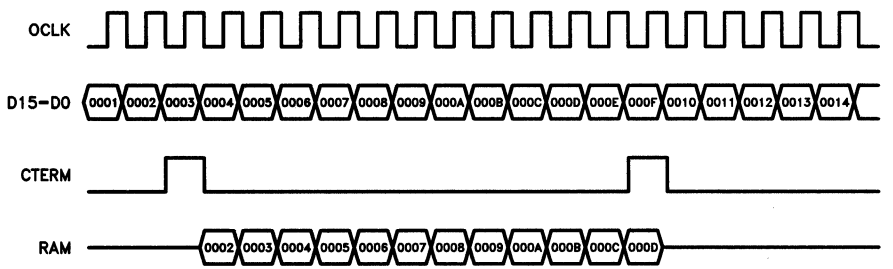

FIGURE 26. RUNN TIMING DIAGRAM: SELDP = 1, CMPSEL = 0

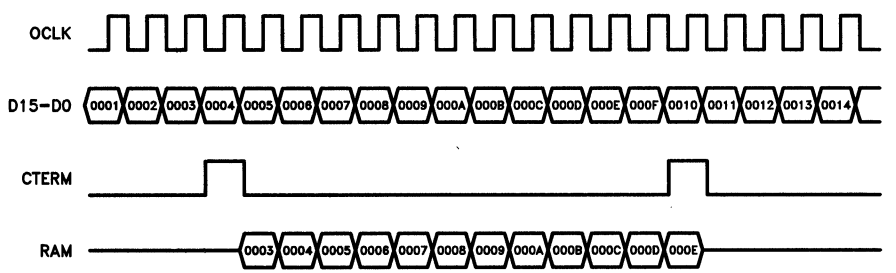

FIGURE 27. RUNN TIMING DIAGRAM: SELDP = 1, CMPSEL = 1

parallel signature analysis operations

The TCR can be configured by OP3–OP0 to perform PSA operations on the D inputs. Additionally, multiple DBMs can be cascaded to perform PSA on more than 16 bits with the PIO pin configured for feedback.

PSA operations use an LFSR technique to perform exclusive-OR functions on pairs of data and use the result as the input to an adjacent D-type flip-flop. Parallel signature analysis can be performed under RUNN and RUNT and as a self-test operation on the RAM.

The flexibility of the device in performing PSA operations is greatly enhanced by the DATMSK bits and PTAP bits of the control register. The user can configure the device such that any combination of the D inputs can be ignored during PSA and select the feedback (FBAK) bit from the operation as an input to one of the exclusive-OR gates in each shift register stage.

The basic configuration for parallel signature analysis is shown in Figure 28. On each clock cycle the results of exclusive-OR functions are shifted to another cell as one of the inputs for the next exclusive-OR. A unique signature is developed and can be scanned out for comparison against an expected or known value.

The output of the shift register stages is determined by the various input signals as shown in Table 19.

PSA operations do not affect storage in the RAM when a simultaneous PSA/TRACE operation is being performed.

TABLE 19. PSA TRUTH TABLE

INPUTS					OUTPUT
PTAPnn	FBAK	DATMSKnn	Dn	Q_{n-1}†	Q_n†
0	X	0	0	0	0
0	X	0	0	1	1
0	X	0	1	0	1
0	X	0	1	1	0
0	X	1	X	0	0
0	X	1	X	1	1
1	0	0	0	0	0
1	0	0	0	1	1
1	1	0	1	0	1
1	1	0	0	1	0
1	1	1	X	0	0
1	1	1	X	1	1
1	1	0	0	0	1
1	1	0	0	1	1
1	1	0	1	0	0
1	1	0	1	1	1
1	1	1	X	0	1
1	1	1	X	1	0

† Q_n = the value of register n after the rising edge of CLK. Q_{n-1} = the value of register (n−1) prior to the rising edge of CLK. See Figure 28.

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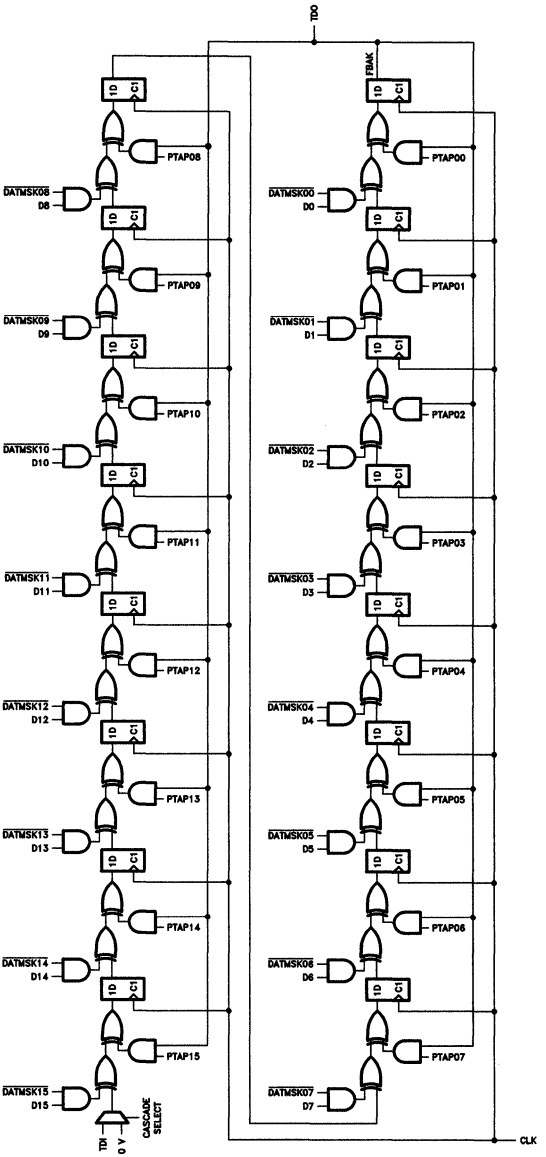

FIGURE 28. PSA CIRCUIT

cascaded PSA operations

More than one 'ACT8994 can be cascaded to perform PSA operations on buses wider than 16 bits. The RUNN and RUNT opcodes include options for configuring the device for stand-alone signatures or as the most significant device (MSD), mid significant device (MID), or least significant device (LSD) in a cascaded configuration.

Figure 29 shows a configuration in which three devices are cascaded. When the PSA opcode includes configuration as an MSD or MID, the PSA circuit is configured such that PIO is an input and replaces, in the circuit of Figure 28, the Q output of register 0 (Q_0) as the FBAK bit. Q_0 is routed through TDO to drive the TDI input of the next device in the chain. A device configured as a MSD ignores its TDI input.

When the PSA opcode configures a device as the LSD, Q_0 is used to drive PIO, now enabled and used as an output, which is tied to the PIO inputs of the MSD and MID(s). The TDO pin of an LSD is in the high-impedance state.

During a cascaded PSA operation, the TDI and TDO pins of the device are used in the shifting of data. Although an instruction register scan can occur while RUNN is active, and updating the IR with another RUNN instruction will not affect device operations, the scanning of data through the IR will contaminate the signature being generated. When a cascaded PSA operation is active, it is recommended that the device go to the Run-Test/Idle state for the duration of the test.

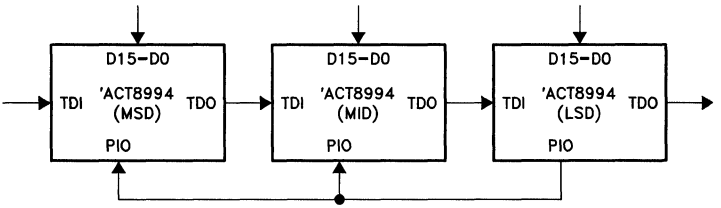

FIGURE 29. CASCADED PSA CONFIGURATION

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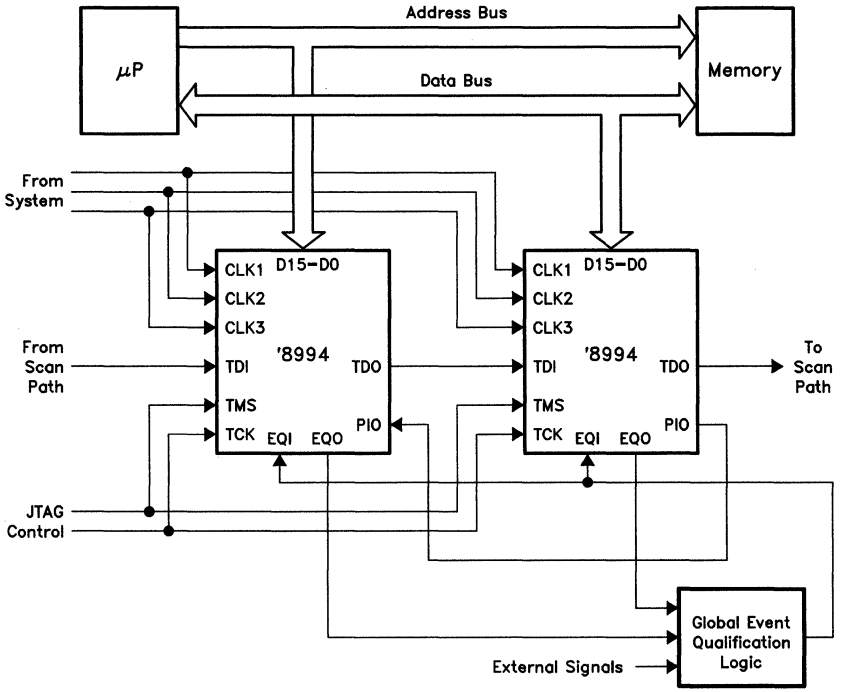

FIGURE 30. TYPICAL DBM APPLICATION

Figure 30 shows a typical application of the 'ACT8994. In the figure, two DBMs reside in parallel with a microprocessor and memory. The CLK inputs, used for on-line operations under RUNN, are driven by system signals (interrupt, clock, enable, control, etc.). The DBMs are configured for cascaded PSA operations by connecting their PIO pins.

Global event qualification schemes are implemented by combining, in the global event qualification logic block, the EQO outputs of the DBMs with some external qualifiers chosen by the user.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_I < 0 or V_I > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			'54ACT8994		'74ACT8994		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	EQO		−3.4		−4	mA
		PIO		−12		−16	
		TDO		−20		−24	
I_{OL}	Low-level output current	EQO		3.4		4	mA
		PIO		12		16	
		TDO		20		24	
T_A	Operating free-air temperature		−55	125	0	70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'54ACT8994		'74ACT8994		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	EQO	V_{CC} = 4.5 V, I_{OH} = −3.4 mA	3.7				V
		V_{CC} = 4.5 V, I_{OH} = −4 mA			3.7		
	PIO	V_{CC} = 4.5 V, I_{OH} = −12 mA	3.7				
		V_{CC} = 4.5 V, I_{OH} = −16 mA			3.7		
	TDO	V_{CC} = 4.5 V, I_{OH} = −20 mA	3.7				
		V_{CC} = 4.5 V, I_{OH} = −24 mA			3.7		
V_{OL}	EQO	V_{CC} = 4.5 V, I_{OL} = 3.4 mA		0.5			V
		V_{CC} = 4.5 V, I_{OL} = 4 mA				0.5	
	PIO	V_{CC} = 4.5 V, I_{OL} = 12 mA		0.5			
		V_{CC} = 4.5 V, I_{OL} = 16 mA				0.5	
	TDO	V_{CC} = 4.5 V, I_{OL} = 20 mA		0.5			
		V_{CC} = 4.5 V, I_{OL} = 24 mA				0.5	
I_{OZ}†	PIO, TDO	V_{CC} = 5.5 V, V_O = V_{CC} or GND		±10		±5	μA
I_I		V_{CC} = 5.5 V, V_I = V_{CC} or GND		±1		±1	μA
I_{CCQ} (RAM disabled)		V_{CC} = 5.5 V, V_I = V_{CC} or GND, I_O = 0		200		200	μA
I_{CC} (RAM enabled)		V_{CC} = 5.5 V, V_I = V_{CC} or GND, I_O = 0		175		175	mA

† For I/O pins, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range

			'54ACT8994		'74ACT8994		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}		TCK	0	35	0	35	MHz
		Any CLK	0	35	0	35	
t_w	Pulse duration	TCK high or low	10		10		ns
		Any CLK high or low	10		10		
t_{su}	Setup time	TMS before TCK ↑	10		10		ns
		Any D before TCK ↑	10		10		
		Any D before any CLK	10		10		
		TDI before TCK ↑	10		10		
		PIO before TCK ↑	10		10		
		PIO before any CLK	10		10		
		EQI before any CLK	10		10		
t_h	Hold time	TMS after TCK ↑	5		5		ns
		Any D after TCK ↑	5		5		
		Any D after any CLK	5		5		
		TDI after TCK ↑	5		5		
		PIO after TCK ↑	5		5		
		PIO after any CLK	5		5		
		EQI after any CLK	5		5		
t_d	Delay time	Power-up to TCK ↑	100		100		ns

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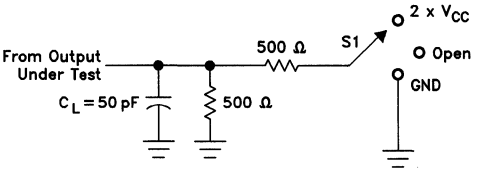
switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'54ACT8994		'74ACT8994		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	TCK		35		35		MHz
	Any CLK		35		35		
t_{PLH}	Any D	EQO					ns
t_{PHL}							
t_{PLH}	TCK ↓	TDO					ns
t_{PHL}							
t_{PLH}	TCK ↓	PIO					ns
t_{PHL}							
t_{PLH}	TCK ↓	EQO					ns
t_{PHL}							
t_{PLH}	EQI	EQO					ns
t_{PHL}							
t_{PLH}	Any CLK	TDO					ns
t_{PHL}							
t_{PLH}	Any CLK	PIO					ns
t_{PHL}							
t_{PLH}	Any CLK	EQO					ns
t_{PHL}							
t_{PZH}	TCK ↓	TDO					ns
t_{PZL}							
t_{PHZ}	TCK ↓	TDO					ns
t_{PLZ}							
t_{PZH}	TCK ↓	PIO					ns
t_{PZL}							
t_{PHZ}	TCK ↓	PIO					ns
t_{PLZ}							

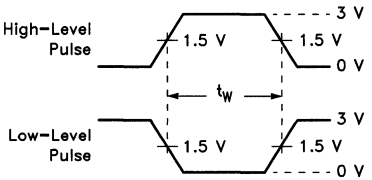
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

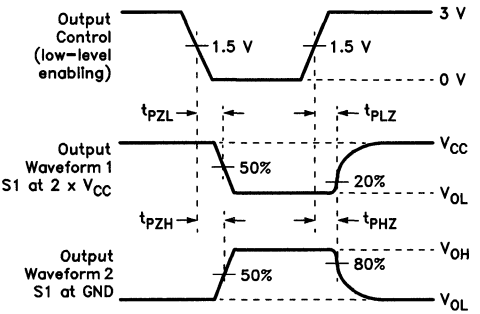


LOAD CIRCUIT FOR OUTPUTS

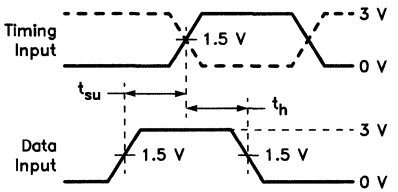
TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND



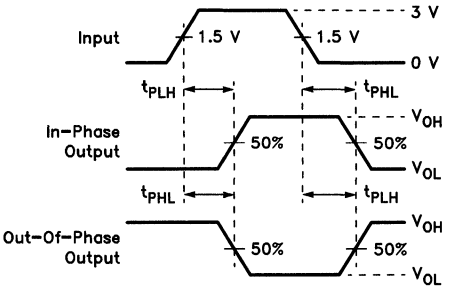
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

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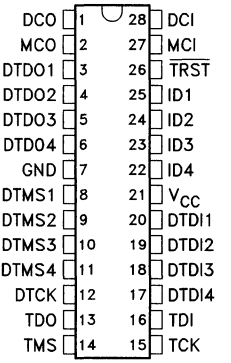
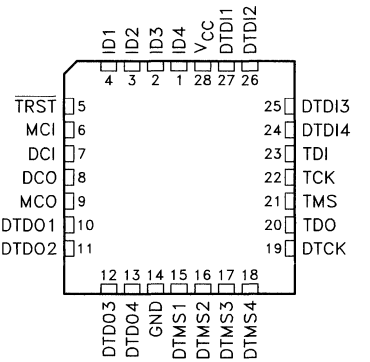
PRODUCT PREVIEW

- **Members of the Texas Instruments SCOPE™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus**
- **Select Up to Four Secondary Scan Paths to Be Included in a Primary Scan Path**
- **Allow Partitioning of System Scan Paths**
- **Six Data Registers: Control, Select, Counter, Boundary Scan, ID Bus, Bypass**
- **Include Eight-Bit Programmable Binary Counter to Count or Initiate Interrupt Signals**
- **Include Four-Bit Identification Bus for Scan Path Communication**
- **Inputs are TTL Compatible**
- **Compatible with TI's ASSET™ (Automated Support System for Emulation and Test) Software**
- **Can be Cascaded Horizontally or Vertically**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54ACT8997 . . . JT PACKAGE
SN74ACT8997 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ACT8997 . . . FK PACKAGE
(TOP VIEW)



description

The 'ACT8997 is a member of Texas Instruments SCOPE™ testability IC family. This family of components facilitates testing of complex circuit board assemblies.

The 'ACT8997 enhances the scan capability of TI's SCOPE™ family by allowing augmentation of a system's primary scan path with secondary scan paths (SSPs), which can be individually selected by the 'ACT8997 to be included in the primary scan path. The device also provides buffering of test signals to reduce the need for external logic.

By loading the proper values into the instruction register and data registers, the user can select up to four SSPs to be included in a primary scan path. Any combination of the SSPs can be selected at a time. By selecting the bypass register, all secondary scan paths can be removed from a primary scan path.

Any of the device's six data registers, or the instruction register, may be placed in the device's scan path (i.e., placed between TDI (test data in) and TDO (test data out) for subsequent shift and scan operations).

All operations of the device except counting are synchronous to the test clock pin, TCK. The eight-bit programmable up/down counter can be used to count transitions on the DCI (device condition input) pin and output interrupt signals via the DCO (device condition output) pin. The device can be configured to count on either the rising or falling edge of DCI.

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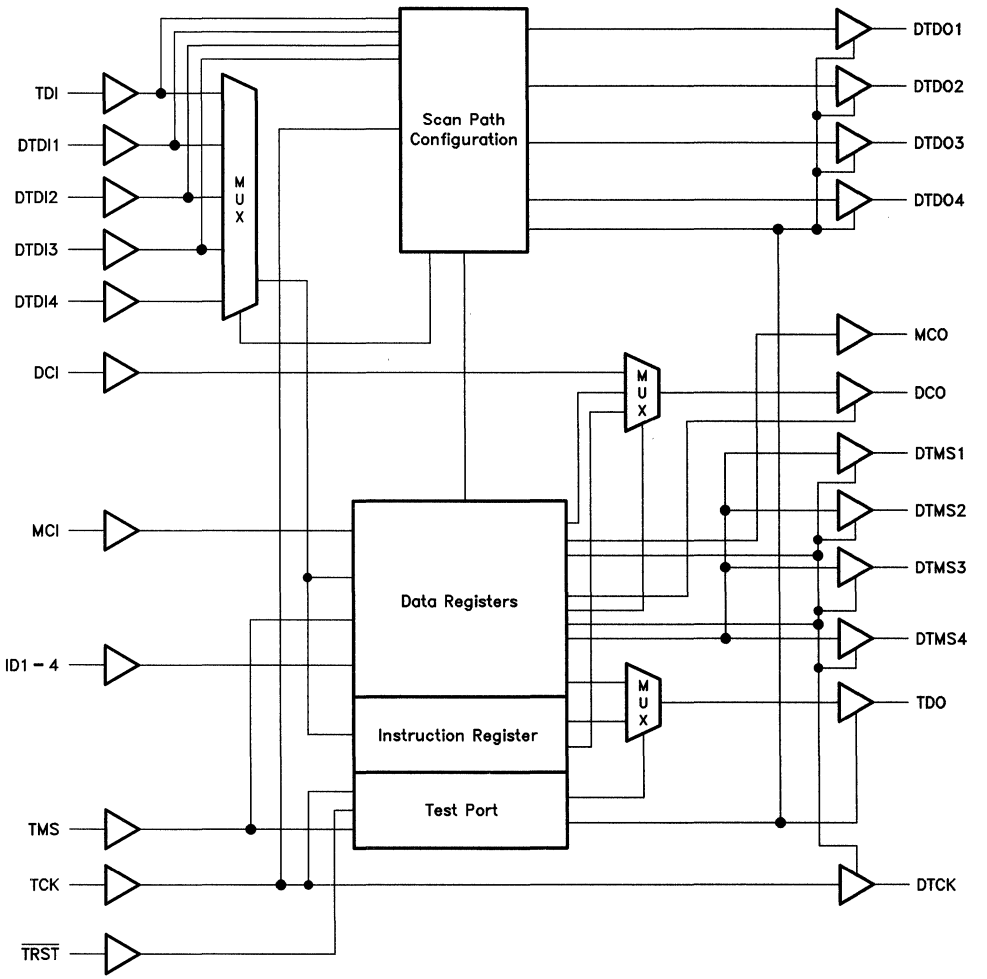
PRODUCT PREVIEW

description (continued)

The test access port (TAP) is a finite-state machine compatible with IEEE Standard 1149.1.

The SN54ACT8997 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ACT8997 is characterized for operation from 0°C to 70°C.

functional block diagram



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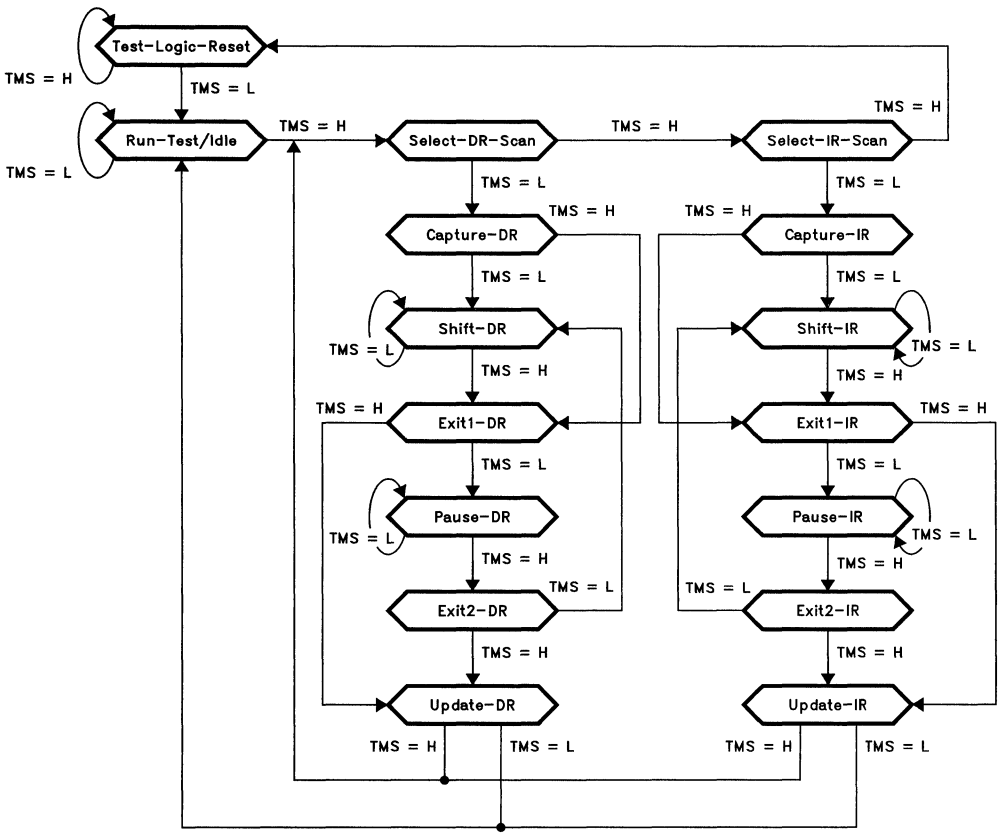

FIGURE 1. TAP STATE DIAGRAM

state diagram description

The TAP proceeds through the states in Figure 1 according to IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state which does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to manipulate a data register and one to manipulate the instruction register. No more than one register can be manipulated at a time.

Test-Logic-Reset
In this state, the test logic is inactive and an internal reset signal is applied to all registers in the device. During device operation, the TAP returns to this state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup that forces it to a high level if left unconnected or if a board defect causes it to be open-circuited. The device powers up in the Test-Logic-Reset state.

Run-Test/Idle
The TAP must pass through this state before executing any test operations. The TAP may retain this state indefinitely, and no registers are modified while in Run-Test/Idle.

Select-DR-Scan, Select-IR-Scan
No specific function is performed in these states; and the TAP exits either of them on the next TCK cycle.

Capture-DR
The selected data register is placed in the scan path (i.e., between TDI and TDO). Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK causing the TAP state to change.

Shift-DR
In this state, data is serially shifted through the selected data register, from TDI to TDO, on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). On the falling edge of TCK in Shift-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the level present before it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the logic low level.

Exit1-DR, Exit2-DR
These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-DR to Exit1-DR.

Pause-DR
The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data.

Update-DR
If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated only during this state.

Capture-IR
The instruction register is preloaded with the IR status word (see Table 4) and placed in the scan path.

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state diagram description (continued)

Shift-IR

In this state, data is serially shifted through the instruction register, from TDI to TDO, on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). On the falling edge of TCK in Shift-IR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the level present before it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the high level.

Exit1-IR, Exit2-IR

These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-IR to Exit1-IR.

Pause-IR

The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR

In this state, the latches shadowing the instruction register are updated with the new instruction.

signal descriptions

TDI—Test Data In

One of the four pins required by IEEE Standard 1149.1. TDI is the serial input for shifting information into the instruction register or data registers. TDI is typically driven by the TDO pin of the primary bus controller. An internal pullup forces TDI to a high level if left unconnected.

TDO—Test Data Out

One of the four pins required by IEEE Standard 1149.1. TDO is the serial output for shifting information out of the instruction register or data registers. TDO is typically connected to the TDI pin of the next testable device in the primary scan path.

TCK—Test Clock

One of the four pins required by IEEE Standard 1149.1. All operations of the 'ACT8997, except for the count function, are synchronous to TCK. Data on the device inputs is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.

TMS—Test Mode Select

One of the four pins required by IEEE Standard 1149.1. The level of TMS at the rising edge of TCK directs the 'ACT8997 through its states. An internal pullup forces TMS to a high level if left unconnected.

$\overline{\text{TRST}}$—Test Reset

This active-low pin implements the optional reset function of IEEE Standard 1149.1. When asserted, $\overline{\text{TRST}}$ causes the 'ACT8997 to go to the Test-Logic-Reset state and configure the instruction register and data registers to their power-up values. An internal pullup forces $\overline{\text{TRST}}$ to a high level if left unconnected.

signal descriptions (continued)

DTMS1–DTMS4—Device Test Mode Select 1–4
Any combination of these four pins can be selected to follow the TMS pin to direct the secondary scan path(s) through the states in Figure 1. The unselected DTMS pins can be independently set to a high or low level. The TMS circuit monitors input from the control register to determine the configuration of the DTMS pins.

MCI—Master Condition Input
This pin receives interrupt and protocol signals from a PBC. The level on MCI is buffered and output on MCO.

MCO—Master Condition Output
This pin transmits interrupt and protocol signals to the secondary scan path(s).

DCI—Device Condition Input
This pin receives interrupt and protocol signals from the secondary scan path(s). When the counter register is instructed to count up or down, the DCI pin is configured as the counter clock.

DCO—Device Condition Output
DCO is configured by the control register to output protocol and interrupt signals, and may be configured by the control register to output an error signal if the instruction register is loaded with an invalid value. DCO is further configured by the control register as:
1) Active-high or active-low (reset condition = active-low).
2) Open-drain or three-state (reset condition = open-drain).

DTDI1–DTDI4—Device Test Data In 1–4
These pins receive the serial test data outputs of the selected secondary scan path(s).

DTDO1–DTDO4—Device Test Data Out 1–4
These pins output serial test data to the TDI input(s) of the secondary scan path(s).

DTCK—Device Test Clock
This pin outputs the buffered test clock TCK to the secondary scan path(s).

ID1–ID4—Identification 1–4
This four-bit data bus can be hardwired to provide indentification of the subsystem under test. The value present on the bus can be scanned out through the boundary scan or ID bus registers.

functional block description

The 'ACT8997 is intended to link secondary scan paths for inclusion in a primary scan path. Any combination of the four secondary scan paths can be linked, or the device can be bypassed entirely.

The least significant bit (LSB) of any value scanned into any register of the device is the first bit shifted in (nearest to TDO). The most significant bit (MSB) is the last bit shifted in (nearest to TDI).

The 'ACT8997 is divided into functional blocks as detailed below.

test port
The test port decodes the signals on TCK, TMS, and $\overline{\text{TRST}}$ to control the operation of the circuit. The test port includes a TAP that issues the proper control instructions to the data registers according to the IEEE Standard 1149.1 protocol. The TAP state diagram is shown in Figure 1.

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functional block description (continued)

instruction register

The instruction register (IR) is an eight-bit wide serial shift register that issues commands to the device. Data is input to the instruction register via TDI (or one of the DTDI pins) and shifted out via TDO. All device operations are initiated by loading the proper instruction or set of instructions into the IR.

data registers

Six parallel data registers are included in the 'ACT8997: bypass, control, counter, boundary scan, ID bus, and select. The ID bus register is a part of the boundary scan register. Each data register is serially loaded via TDI or DTDI and outputs data via TDO.

scan path configuration circuit

This circuit decodes bits in the select and control registers to determine which, if any, of the secondary scan paths are to be included in the primary scan path.

TABLE 1. REGISTER SUMMARY

REGISTER NAME	LENGTH (BITS)	FUNCTION
Instruction	8	Issue command information to the device.
Control	10	Configuration and enable control.
Counter	8	Count events on DCI, output interrupts via DCO.
Select	8	Select one or more secondary scan paths.
Boundary Scan	10	Capture and force test data at device periphery.
ID Bus	4	Provide identification code.
Bypass	1	Remove the 'ACT8997 from the scan path.

instruction register description

The instruction register (IR) is an eight-bit serial register that outputs control signals to the device. Table 2 lists the instructions implemented in the 'ACT8997, and the data register selected by each instruction. The MSB of the IR is an even-parity bit. If the value scanned into the IR during Shift-IR does not contain even parity, an error signal, $\overline{\text{IRERR}}$, is generated internally as shown in Table 3. The 'ACT8997 can be configured to output $\overline{\text{IRERR}}$ via DCO if the TAP enters the Pause-IR state.

During the Capture-IR state, the IR status word is loaded. The IR status word contains information about the most recently loaded values of the instruction and select registers and the logic level present at the DCI input. The IR status word is encoded as shown in Table 4.

Figure 2 illustrates the order of scan for the instruction register.

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instruction register description (continued)

TABLE 2. INSTRUCTION REGISTER OPCODES

BINARY CODE BIT 7 → BIT 0 MSB → LSB	HEX VALUE	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER
00000000	00	EXTEST	Boundary Scan	Boundary Scan
10000001	81	BYPASS†	Bypass Scan	Bypass
10000010	82	SAMPLE/PRELOAD	Sample Boundary	Boundary Scan
00000011	03	INTEST	Boundary Scan	Boundary Scan
10000100	84	BYPASS†	Bypass Scan	Bypass
00000101	05	BYPASS†	Bypass Scan	Bypass
00000110	06	BYPASS†	Bypass Scan	Bypass
10000111	87	BYPASS†	Bypass Scan	Bypass
10001000	88	COUNT	Count	Counter
10001001	09	COUNT	Count	Counter
00001010	0A	BYPASS†	Bypass Scan	Bypass
10001011	8B	BYPASS†	Bypass Scan	Bypass
00001100	0C	BYPASS†	Bypass Scan	Bypass
10001101	8D	BYPASS	Bypass Scan	Bypass
10001110	8E	SCANCN	Control Register Scan	Control
00001111	0F	SCANCT	Control Register Scan	Control
11111010	FA	SCANCNT	Counter Scan	Counter
01111011	7B	READCNT	Counter Read	Counter
11111100	FC	SCANIDB	ID Bus Register Scan	ID Bus
01111101	7D	READIDB	ID Bus Register Read	ID Bus
01111110	7E	SCANSEL	Select Register Scan	Select
ALL OTHER		BYPASS	Bypass Scan	Bypass

† A SCOPE opcode exists but is not supported by the 'ACT8997.

instruction register description (continued)

TABLE 3. $\overline{\text{IRERR}}$ FUNCTION TABLE

NUMBER OF INSTRUCTION REGISTER BITS = 1	$\overline{\text{IRERR}}$
0, 2, 4, 6, 8	1
1, 3, 5, 7	0

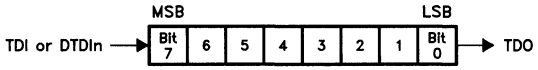

FIGURE 2. INSTRUCTION REGISTER BITS AND ORDER OF SCAN

TABLE 4. INSTRUCTION REGISTER STATUS WORD

IR BIT	VALUE†
7	$\overline{\text{IRERR}}$ (see Table 3)
6	0
5	0
4	0
3	Level present at DCI input (1 = H, 0 = L)
2	0
1	0
0	1

† This value is loaded in the instruction register during the Capture-IR TAP state.

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instruction register opcode descriptions

The operation of the 'ACT8997 is dependent on the instruction loaded into the instruction register. Each instruction selects one of the data registers to be placed between TDI or DTDI and TDO during the Shift-DR TAP state.

All the required instructions of IEEE Standard 1149.1 are implemented in the 'ACT8997.

boundary scan
This instruction implements the required EXTEST and INTEST operations of IEEE Standard 1149.1. The boundary scan register (which includes the ID bus register) is placed in the scan path. Data appearing at input pins included in the boundary scan register is captured. Data previously loaded into the output pins included in the boundary scan register is forced through the outputs.

bypass scan
This instruction implements the required BYPASS operation of IEEE Standard 1149.1. The bypass register is placed in the scan path and preloads with a logic 0 during Capture-DR.

sample boundary
This instruction implements the required SAMPLE/PRELOAD operation of IEEE Standard 1149.1. The boundary scan register is placed in the scan path, and data appearing at the inputs and outputs included in the boundary scan register is sampled on the rising edge of TCK in Capture-DR.

count
The counter register begins counting on each DCI transition. The count begins from the value present in the register before the count instruction was loaded. The counter can be programmed to count up or down on either the low-to-high or high-to-low transition of DCI. Counting occurs only while in the Run-Test/Idle TAP state.

counter register read
The counter register is placed in the scan path. During Capture-DR, the prior preloaded value of the counter is loaded into the counter register. At Update-DR, a new preload value is loaded.

counter register scan
The counter register is placed in the scan path. During Capture-DR, the current value of the counter is loaded in the counter register. At Update-DR, a new preload value is loaded.

control register scan
The control register is placed in the scan path for a subsequent shift operation.

ID bus register scan
The ID bus register (a subset of the boundary scan register) is placed in the scan path for a subsequent shift operation. The data appearing on the ID bus is loaded into the ID bus register on the rising edge of TCK in Capture-DR.

ID bus register read
The ID bus register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

select register scan
The select register is placed in the scan path for a subsequent shift operation.

control register description

The control register (CTLR) is a ten-bit serial register that controls the enable and select functions of the 'ACT8997. A reset operation forces all bits to a logic low level. The contents of the control register are latched and decoded during the Update-DR TAP state. The specific function of each bit is listed in Table 5.

The enable and select functions of the control register bits are mapped as follows:

Bit 9—$\overline{\text{Up}}$/Down
This bit sets the count mode of the counter register (reset condition = count up).

Bit 8—Latch on Zero
The counter register can be configured to stop counting when its value is 00000000 and ignore subsequent transitions on the counter clock, DCI. The latch-on-zero option is valid only in the count-down mode (reset condition = do not latch on zero). The value of this bit has no effect on the operation of the counter if CTLR bit 10 = 0.

Bit 7—DCO Polarity Select
DCO can be configured as an active-low or active-high output (reset condition = active-low). When active-low, DCO does not invert the signal selected to drive it. When active-high, DCO inverts the selected signal.

Bit 6/Bit 5—DCO Source Select 1/DCO Source Select 0
DCO can be used to output the $\overline{\text{IRERR}}$ signal generated by the 'ACT8997 (see Table 3). Bits 6 and 5 can be set to output $\overline{\text{IRERR}}$ via DCO on the falling edge of TCK in the Pause-IR state. DCO can also be configured to become active when the value of the counter is 00000000, to follow DCI, or be set to a static high or low level (reset condition = static high level).

Bit 4—Parity Mask
The signal $\overline{\text{IRERR}}$ can be masked from appearing on DCO even if bits 6 and 5 are set such that it is output in the Pause-IR state (reset condition = do not mask $\overline{\text{IRERR}}$).

Bit 3—DCO Drive Select
DCO can be configured as either an open-drain or 3-state output (reset condition = open-drain). The open-drain configuration allows multiple DCO outputs to be used in a wired-OR or wired-AND application. The three-state configuration allows the DCO output to be connected to a bus.

Bit 2—DCO Enable
When configured as a 3-state output, DCO can be placed in the high-impedance state (reset condition = disabled). If configured as an open-drain output and disabled, DCO outputs a high level.

Bit 1—DCI Polarity Select
The level at the DCI input can be inverted before being applied to the internal logic of the device (reset condition = do not invert DCI).

Bit 0—Device Test Pins Output Enable
DTCK, DTDO, and the DTMS1–4 pins can be placed in the high-impedance state (disabled) with this bit (reset condition = enabled).

Several control register bits affect the functionality of the DCO output. The DCO function table is given in Table 6.

Figure 3 illustrates the order of scan for the control register.

TABLE 5. CONTROL REGISTER BIT MAPPING

BIT	VALUE	FUNCTION
9	0	Configure counter to count up
	1	Configure counter to count down
8	0	Do not stop counting when the count reaches 00000000
	1	Stop counting when the count reaches 00000000
7	0	Configure DCO as an active-low output
	1	Configure DCO as an active-high output
6, 5	00	DCO = H or L (depends on CTLR Bit 7)
	01	DCO = $\overline{\text{IRERR}}$
	10	DCO = $\overline{\text{CE}}$, an internal logic 0 generated when the count is 00000000
	11	DCO = DCI
4	0	Do not mask $\overline{\text{IRERR}}$ from DCO
	1	Mask $\overline{\text{IRERR}}$ from DCO
3	0	Configure DCO as an open-drain output
	1	Configure DCO as a 3-state output
2	0	Disable DCO
	1	Enable DCO
1	0	DCI = DCI
	1	DCI = $\overline{\text{DCI}}$ (invert the DCI signal before applying it to the internal logic)
0	0	Enable DTCK, DTDO1–4, and DTMS1–4
	1	Disable DTCK, DTDO1–4, and DTMS1–4

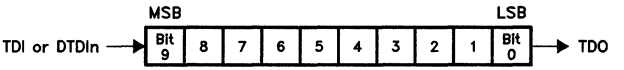

FIGURE 3. CONTROL REGISTER BITS AND ORDER OF SCAN

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TABLE 6. DCO FUNCTION TABLE

DCI	INTERNAL SIGNALS†		CONTROL REGISTER BITS‡							DCO
	$\overline{IRERR}$	$\overline{CE}$	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	
X	X	X	X	X	X	X	0	0	X	H
X	X	X	X	X	X	X	1	0	X	Z
X	X	X	0	0	0	X	X	1	X	H
X	X	X	1	0	0	X	X	1	X	L
X	X	X	0	0	1	1	X	1	X	H
X	X	X	1	0	1	1	X	1	X	L
X	0	X	0	0	1	0	X	1	X	L in Pause-IR§, H otherwise
X	1	X	0	0	1	0	X	1	X	H
X	0	X	1	0	1	0	X	1	X	H in Pause-IR§, L otherwise
X	1	X	1	0	1	0	X	1	X	L
X	X	0	0	1	0	X	X	1	X	L
X	X	0	1	1	0	X	X	1	X	H
X	X	1	0	1	0	X	X	1	X	H
X	X	1	1	1	0	X	X	1	X	L
L	X	X	0	1	1	X	X	1	0	L
L	X	X	0	1	1	X	X	1	1	H
L	X	X	1	1	1	X	X	1	0	H
L	X	X	1	1	1	X	X	1	1	L
H	X	X	0	1	1	X	X	1	0	H
H	X	X	0	1	1	X	X	1	1	L
H	X	X	1	1	1	X	X	1	0	L
H	X	X	X	1	1	1	X	X	1	H

† These signals are generated as described elsewhere in this datasheet.

‡ The control register must contain these values after the TAP has passed through its most recent Update-DR state.

§ DCO becomes active on the falling edge of TCK as the TAP enters the Pause-IR state and becomes inactive on the falling edge of TCK as the TAP enters Exit2-IR.

select register description

The select register (SR) is an eight-bit serial register that determines which, if any, of the seconday scan paths will be included in the primary scan path. A reset operation forces all bits to a logic 0.

The register is divided into four two-bit sections, each of which controls one SSP. Figure 4 shows the mapping of the bits to the SSPs and the order of scan. For each SSP, the higher-order bit is the MSB and the lower-order bit is the LSB (e.g., bit 3 is the MSB of SSP2 and bit 2 is the LSB of SSP2).

Although any combination of SSPs can be selected, the order of scan for each combination is fixed (see data flow description for details).

The SR bit decoding is shown in Table 7.

TABLE 7. SELECT REGISTER BIT DECODING

MSB	LSB	DTMSn SOURCE	DTDOn STATUS
0	0	H	Z
0	1	L	Z
1	X	TMS	Active†

† The DTDO1–4 outputs are active only in the Shift-IR and Shift-DR TAP states.

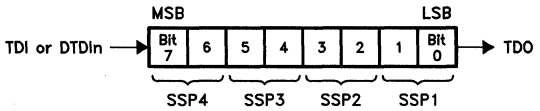

FIGURE 4. SELECT REGISTER BITS AND ORDER OF SCAN

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boundary scan register/ID bus register description

The boundary scan register (BSR) is a ten-bit serial register that can be used to capture data appearing at selected device inputs, force data through device outputs, and apply data to the device's internal logic. The BSR is made up of boundary scan cells (BSCs). Table 8 lists the device signal for each of the ten BSCs that comprise the BSR.

The four BSCs connected to the ID1–4 pins form a subset of the BSR called the ID bus register (IDBR). The IDBR can be scanned without accessing the remaining BSCs of the BSR.

Figure 5 illustrates the order of scan for the boundary scan register and ID bus register.

TABLE 8. BOUNDARY SCAN REGISTER BIT MAPPING

BIT	PIN NAME	SIGNAL DESCRIPTION
9	MCI	Master Condition In
8	MCO	Master Condition Out
7	DCI	Device Condition In
6	$\overline{\text{DCOTS}}$†	Enable control for DCO in 3-state configuration (active-low)
5	$\overline{\text{DCOOD}}$†	Enable control for DCO in open-drain configuration (active-low)
4	DCO	Device Condition Out
3	ID4	Identification Bus Bit 4
2	ID3	Identification Bus Bit 3
1	ID2	Identification Bus Bit 2
0	ID1	Identification Bus Bit 1

† This internal signal cannot be observed from the I/O pins of the device.

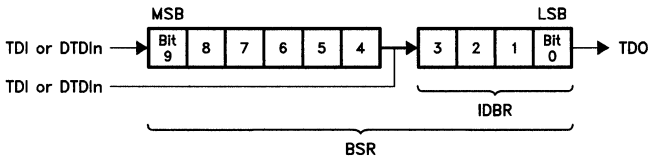

FIGURE 5. BOUNDARY SCAN REGISTER BITS AND ORDER OF SCAN

bypass register description

The bypass register (BR) is a one-bit serial register. The function of the BR is to provide a means of effectively removing the 'ACT8997 from the primary scan path when neither it nor any of the secondary scan paths are needed for the current test operation. At power up, the BR is placed in the scan path. During Capture-DR, the BR is preloaded with a logic low level.

Figure 6 shows the order of the scan for the bypass register.

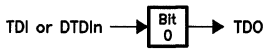

FIGURE 6. BYPASS REGISTER BITS AND ORDER OF SCAN

counter register description

The counter register (CNTR) is an eight-bit serial register that performs a binary count if configured to do so by the control register; it uses the DCI pin as its clock. The counter can be preloaded with an initial value before counting begins, and the current value of the counter can be scanned out. Many of the features of the CNTR are configured by a bit in the control register, including:

1) Count direction up or down (control register bit 9).
2) Stop counting when the value of the register is 00000000 (control register bit 8).
3) DCI transition on which the counter counts (control register bit 1).

An internal signal, $\overline{CE}$, is generated as a logic low level when the value of the CNTR is 00000000. For any other value of the CNTR, $\overline{CE}$ is high.

The counter register can be used to count events occurring on the secondary scan path(s) and can output interrupt signals via DCO when the count has reached zero.

Figure 7 shows the order of scan for the counter register.

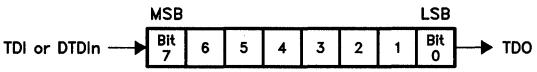

FIGURE 7. COUNTER REGISTER BITS AND ORDER OF SCAN

data flow description

The direction of serial data flow in the 'ACT8997 is dependent on the current instruction and value of the select register. Figure 8 shows the data flow when one or more SSPs have been selected. When more than one SSP has been selected, the order of scan is determined by which SSPs have been selected, as shown in Table 9. Note that the 'ACT8997 adds one bit of delay from TDI or DTDI to DTDO.

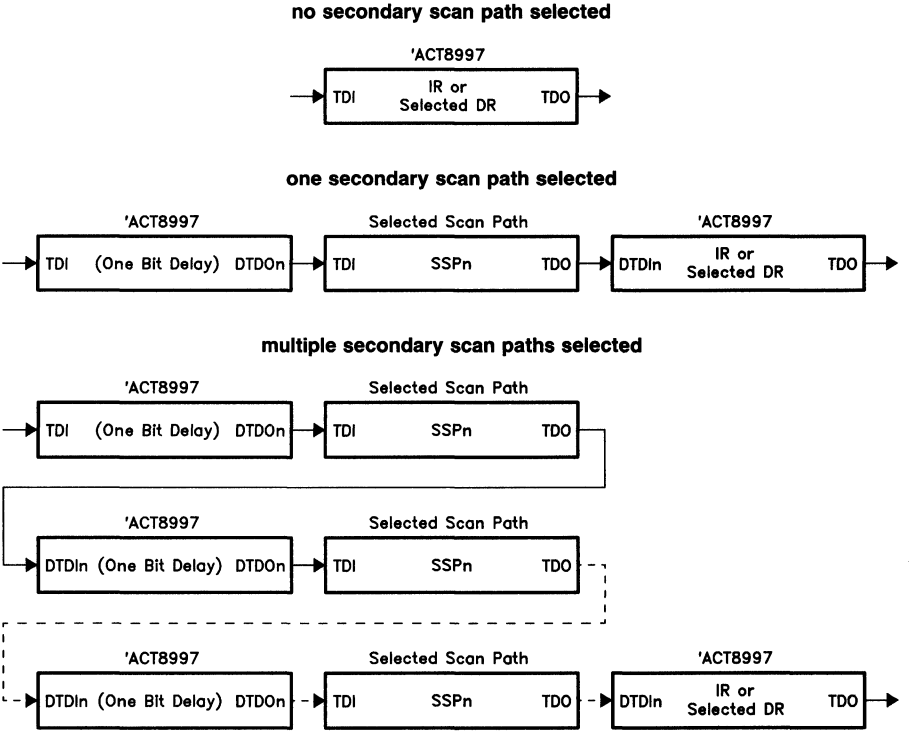

FIGURE 8. DATA FLOW IN THE 'ACT8997

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TABLE 9. SCAN PATH CONFIGURATIONS

SR BIT				SSPn CONFIGURATION				SCAN PATH CONFIGURATION†‡
7	5	3	1	SSP4	SSP3	SSP2	SSP1	
0	0	0	0	Inactive	Inactive	Inactive	Inactive	TDI–SPL–TDO
0	0	0	1	Inactive	Inactive	Inactive	Active	TDI–(1)–SSP1–SPL–TDO
0	0	1	0	Inactive	Inactive	Active	Inactive	TDI–(1)–SSP2–SPL–TDO
0	0	1	1	Inactive	Inactive	Active	Active	TDI–(1)–SSP1–(1)–SSP2–SPL–TDO
0	1	0	0	Inactive	Active	Inactive	Inactive	TDI–(1)–SSP3–SPL–TDO
0	1	0	1	Inactive	Active	Inactive	Active	TDI–(1)–SSP1–(1)–SSP3–SPL–TDO
0	1	1	0	Inactive	Active	Active	Inactive	TDI–(1)–SSP2–(1)–SSP3–SPL–TDO
0	1	1	1	Inactive	Active	Active	Active	TDI–(1)–SSP1–(1)–SSP2–(1)–SSP3–SPL–TDO
1	0	0	0	Active	Inactive	Inactive	Inactive	TDI–(1)–SSP4–SPL–TDO
1	0	0	1	Active	Inactive	Inactive	Active	TDI–(1)–SSP1–(1)–SSP4–SPL–TDO
1	0	1	0	Active	Inactive	Active	Inactive	TDI–(1)–SSP1–(1)–SSP2–(1)–SSP4–SPL–TDO
1	0	1	1	Active	Inactive	Active	Active	TDI–(1)–SSP2–(1)–SSP4–SPL–TDO
1	1	0	0	Active	Active	Inactive	Inactive	TDI–(1)–SSP3–(1)–SSP4–SPL–TDO
1	1	0	1	Active	Active	Inactive	Active	TDI–(1)–SSP1–(1)–SSP3–(1)–SSP4–SPL–TDO
1	1	1	0	Active	Active	Active	Inactive	TDI–(1)–SSP2–(1)–SSP3–(1)–SSP4–SPL–TDO
1	1	1	1	Active	Active	Active	Active	TDI–(1)–SSP1–(1)–SSP2–(1)–SSP3–(1)–SSP4–SPL–TDO

† The scan path configuration is the order of scan, beginning with the TDI pin of the 'ACT8997 and ending with the TDO pin of the 'ACT8997.
‡ A '(1)' indicates one bit of delay through the 'ACT8997.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_I < 0 or V_I > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pin ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			'54ACT8997		'74ACT8997		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	TDO, DTDO1–4, MCO		−8.5		−10	mA
		DTMS1–4, DCO, DTCK		−13.6		−16	
I_{OL}	Low-level output current	TDO, DTDO1–4, MCO		8.5		10	mA
		DCO		13.6		16	
		DTMS1–4		20.4		24	
		DTCK		40.8		48	
T_A	Operating free-air temperature		−55	125	0	70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	PIN(S)	TEST CONDITIONS	V_{CC}	'54ACT8997		'74ACT8997		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	TDO, DTDO1–4, MCO	I_{OH} = −8.5 mA	4.5 V	3.7				V
		I_{OH} = −10 mA	4.5 V			3.7		
	DTMS1–4, DCO, DTCK	I_{OH} = −13.6 mA	4.5 V	3.7				V
		I_{OH} = −16 mA	4.5 V			3.7		
V_{OL}	TDO, DTDO1–4, MCO	I_{OL} = 8.5 mA	4.5 V		0.5			V
		I_{OL} = 10 mA	4.5 V				0.5	
	DCO	I_{OL} = 13.6 mA	4.5 V		0.5			V
		I_{OL} = 16 mA	4.5 V				0.5	
	DTMS1–4	I_{OL} = 20.4 mA	4.5 V		0.5			V
		I_{OL} = 24 mA	4.5 V				0.5	
	$\overline{DTCK}$	I_{OL} = 40.8 mA	4.5 V		0.5			V
		I_{OL} = 48 mA	4.5 V				0.5	
I_{OZ}†	DTDO1–4, DTMS1–4, DCO, DTCK	V_O = V_{CC} or GND	5.5 V		±10		±5	μA
I_I	MCI, DCI, TCK, ID1–4	V_I = V_{CC} or GND	5.5 V		±1		±1	μA
	TDI, DTDI1–4, TMS, $\overline{TRST}$	V_I = V_{CC} or GND	5.5 V	−0.1	−20	−0.1	−20	
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V		100		100	μA
ΔI_{CC}‡		One input at V_{IH} or V_{IL}, Other inputs at V_{CC} or GND	5.5 V		2		0.5	mA

† For I/O pins, the parameter I_{OZ} includes the input leakage current.
‡ This is the increase in supply current for each input being driven at TTL levels rather than V_{CC} or GND.

timing requirements over recommended ranges of operating free-air temperature and supply voltage

			'54ACT8997		'74ACT8997		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK					MHz
		DCI (Count mode)					
t_w	Pulse duration	TCK high or low					ns
		DCI high or low (Count mode)					
t_{su}	Setup time	TMS before TCK ↑					ns
		TDI before TCK ↑					
		Any DTDI before TCK ↑					
		MCI before TCK ↑					
		DCI before TCK ↑					
		Any ID before TCK ↑					
t_h	Hold time	TMS after TCK ↑					ns
		TDI after TCK ↑					
		Any DTDI after TCK ↑					
		MCI after TCK ↑					
		DCI after TCK ↑					
		Any ID after TCK ↑					
t_d	Delay time	Power up to TCK ↑					ns

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switching characteristics over recommended ranges of operating free-air temperature and supply voltage

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'54ACT8997		'74ACT8997		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	TCK			20		20	MHz
	DCI (Count mode)			20		20	
t_{PLH}	TCK ↓	TDO					ns
t_{PHL}							
t_{PLH}	TCK ↓	An DTMS					ns
t_{PHL}							
t_{PLH}	TCK ↓	Any DTDO					ns
t_{PHL}							
t_{PLH}	TCK ↓	DCO (open-drain)					ns
		DCO (three-state)					
t_{PHL}	TCK ↓	DCO (open-drain)					ns
		DCO (three-state)					
t_{PLH}	TMS	Any DTMS					ns
t_{PHL}							
t_{PLH}	MCI	MCO					ns
t_{PHL}							
t_{PLH}	DCI	DCO (open-drain)					ns
		DCO (three-state)					
t_{PHL}	DCI	DCO (open-drain)					ns
		DCO (three-state)					
t_{PLH}	TCK	DTCK					ns
t_{PHL}							

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switching characteristics over recommended ranges of operating free-air temperature and supply voltage (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'54ACT8997		'74ACT8997		UNIT
			MIN	MAX	MIN	MAX	
t_{PHZ}	TCK ↓	DTCK					ns
t_{PLZ}							
t_{PHZ}	TCK ↓	TDO					ns
t_{PLZ}							
t_{PHZ}	TCK ↓	Any DTDO					ns
t_{PLZ}							
t_{PHZ}	TCK ↓	DCO					ns
t_{PLZ}							
t_{PHZ}	TCK ↓	Any DTMS					ns
t_{PLZ}							
t_{PZH}	TCK ↓	DTCK					ns
t_{PZL}							
t_{PZH}	TCK ↓	TDO					ns
t_{PZL}							
t_{PZH}	TCK ↓	Any DTDO					ns
t_{PZL}							
t_{PZH}	TCK ↓	DCO					ns
t_{PZL}							
t_{PZH}	TCK ↓	Any DTMS					ns
t_{PZL}							

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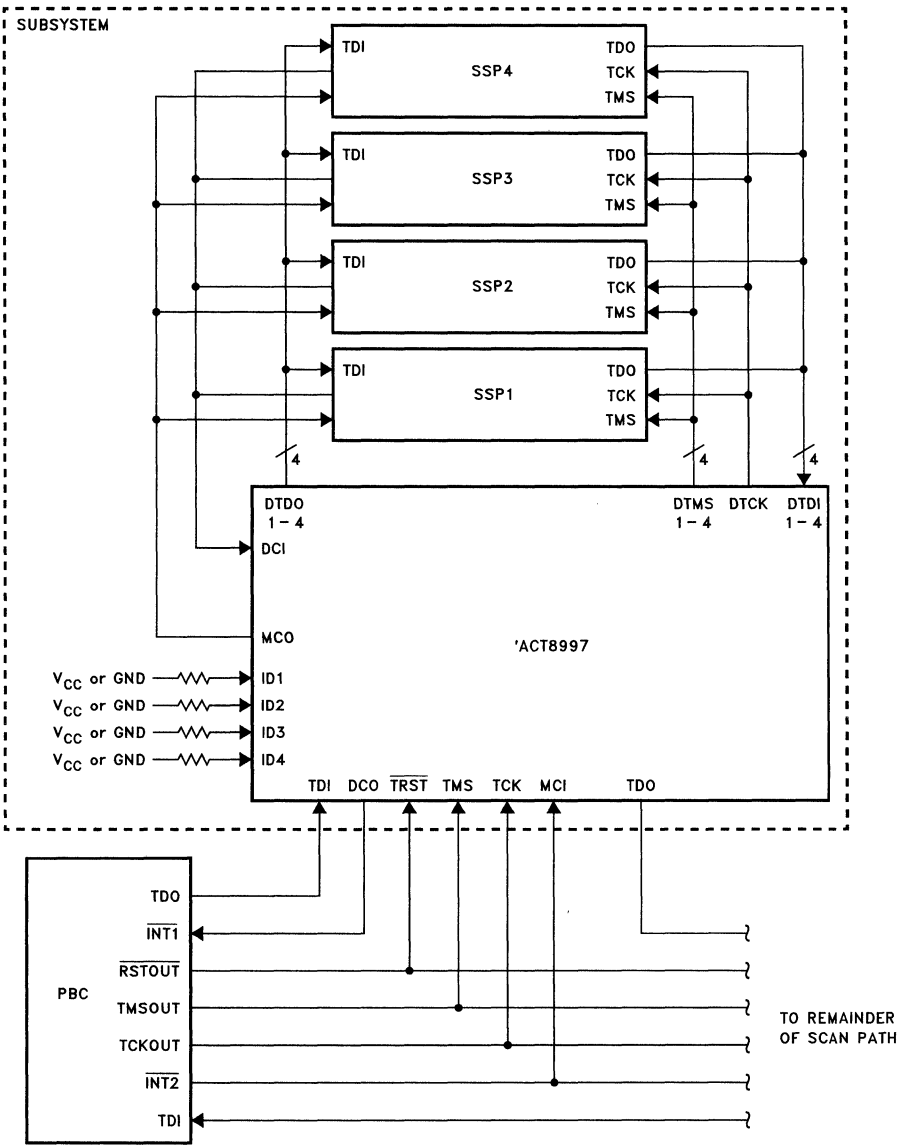
PRODUCT PREVIEW

APPLICATION INFORMATION

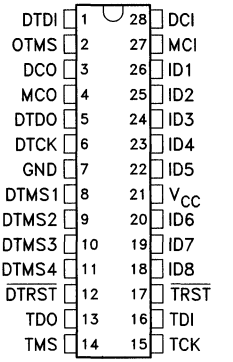


SN54ACT8999, SN74ACT8999
SCAN PATH SELECTORS WITH 8-BIT BIDIRECTIONAL DATA BUSES

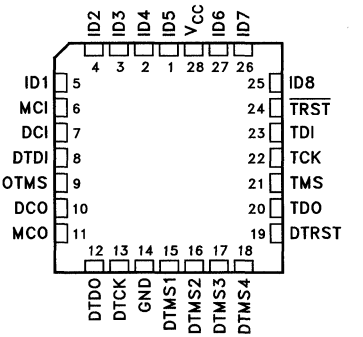
TI0287—D3598, JUNE 1990

- **Members of the Texas Instruments SCOPE™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus**
- **Select One of Four Secondary Scan Paths to Be Included in a Primary Scan Path**
- **Allow Partitioning of System Scan Paths**
- **Provide Communication between Primary and Remote Test Bus Controllers**
- **Six Data Registers: Control, Select, Counter, Boundary Scan, ID Bus, Bypass**
- **Include Eight-Bit Programmable Binary Counter to Count or Initiate Interrupt Signals**
- **Include Eight-Bit Identification Bus for Local or Global Bus Communication**
- **Inputs are TTL Compatible**
- **Compatible with TI's ASSET™ (Automated Support System for Emulation and Test) Software**
- **Can be Cascaded Horizontally or Vertically**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54ACT8999 ... JT PACKAGE
SN74ACT8999 ... DW OR NT PACKAGE
(TOP VIEW)



SN54ACT8999 ... FK PACKAGE
(TOP VIEW)



description

The 'ACT8999 is a member of Texas Instruments SCOPE™ testability IC family. This family of components facilitates testing of complex circuit board assemblies.

The 'ACT8999 enhances the scan capability of TI's SCOPE™ family by allowing augmentation of a system's primary scan path with secondary scan paths (SSPs). The SSPs can be individually selected by the 'ACT8999 for inclusion in the primary scan path. The device also provides buffering of test signals to reduce the need for external logic.

By loading the proper values into the instruction register and data registers, the user can select one of four secondary scan paths. This has the effect of shortening the scan path to allow maximum test throughput when an individual subsystem (board or box) is to be tested. By selecting the bypass register, all secondary scan paths can be removed from a primary scan path.

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description (continued)

Any of the device's six data registers, or the instruction register, may be placed in the device's scan path (i.e., placed between TDI (test data in) and TDO (test data out) for subsequent shift and scan operations).

All operations of the device except counting are synchronous to TCK (test clock). The eight-bit programmable up/down counter can be used to count transitions on the DCI (device condition input) pin and output interrupt signals via the DCO (device condition output) pin. The device can be configured to count on either the rising or falling edge of DCI.

If a system's test architecture contains more than one test bus controller, the eight-bit bidirectional bus can be used to interface a higher-level primary bus controller (PBC) with one or more lower-level remote bus controllers (RBCs). A protocol allows the PBC to pass control of the 'ACT8999 to an RBC, freeing the PBC for other tasks. The eight-bit bus can also be hardwired to provide one of 256 codes for subsystem identification.

The test access port (TAP) is a finite-state machine compatible with the IEEE Standard 1149.1.

The SN54ACT8999 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ACT8999 is characterized for operation from 0°C to 70°C.

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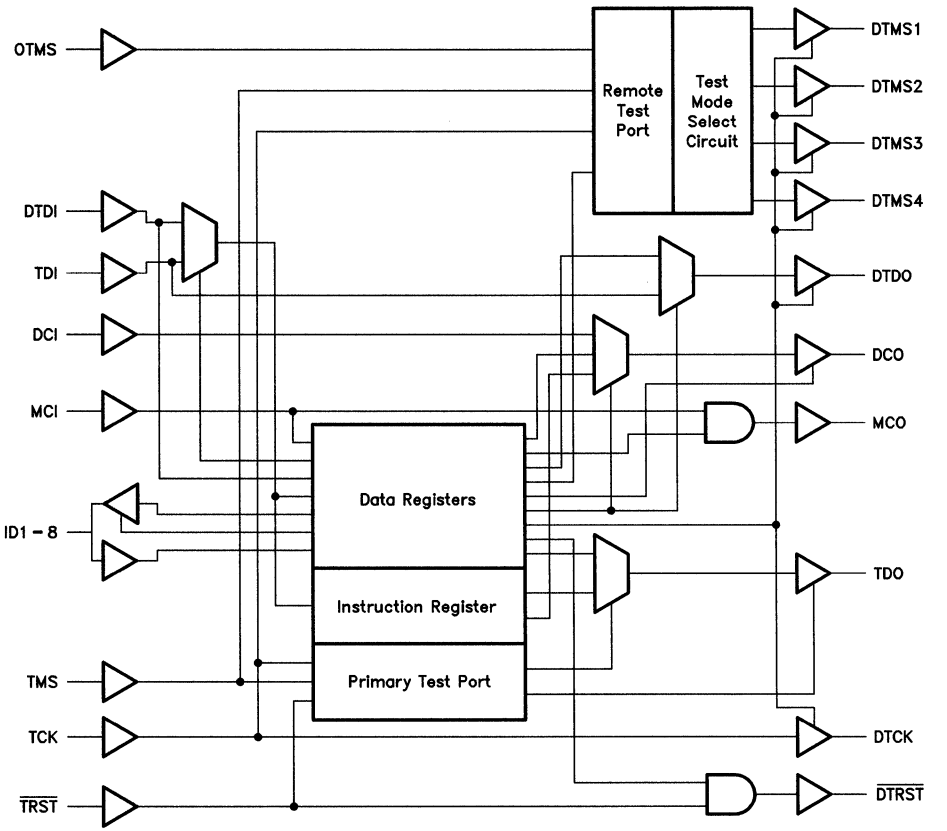
PRODUCT PREVIEW

functional block diagram



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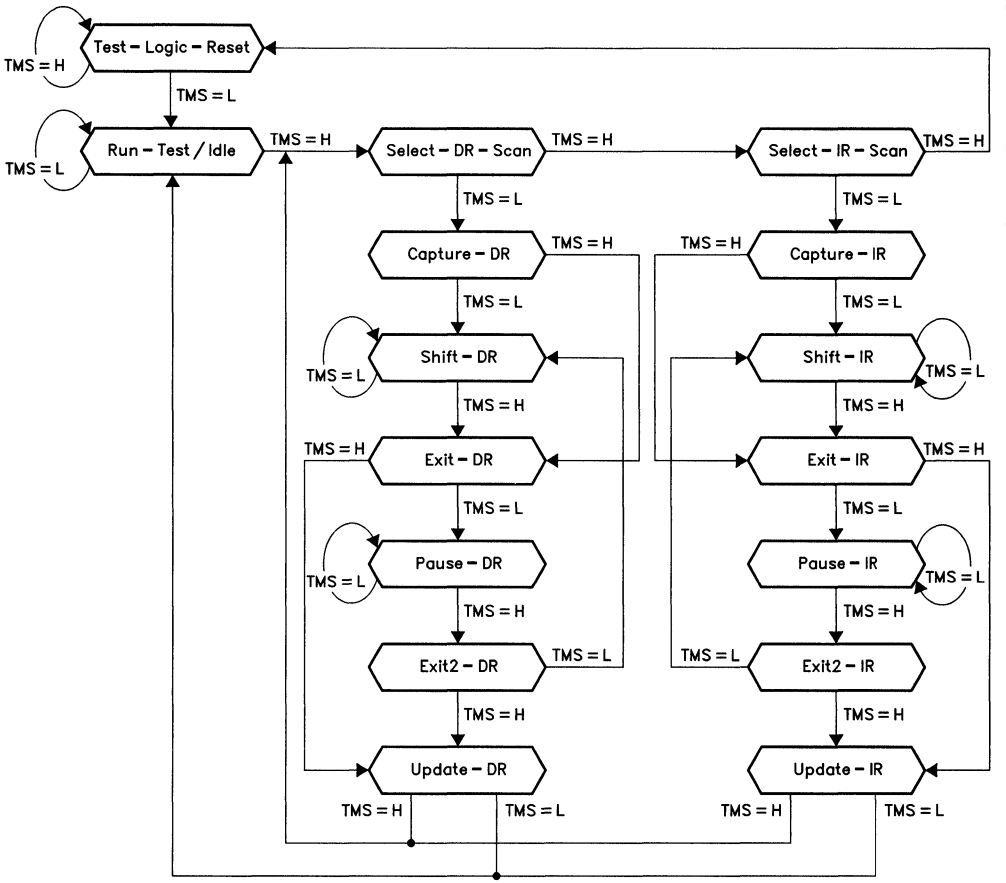

FIGURE 1. TAP STATE DIAGRAM

state diagram description

The TAP proceeds through the states in Figure 1 according to IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to manipulate a data register and one to manipulate the instruction register. No more than one register can be manipulated at a time.

Test-Logic-Reset
The device powers up in the Test-Logic-Reset state. In this state, the test logic is inactive and an internal reset signal is applied to all registers in the device. Also, during device operation, the TAP returns to this state in no more than five TCK cycles if TMS (test mode select) is high. The TMS pin has an internal pullup that forces it to a high level if left unconnected or if a board defect causes it to be open-circuited.

Run-Test/Idle
The TAP must pass through this state before executing any test operations. The TAP may retain this state indefinitely, and no registers are modified while in Run-Test/Idle.

Select-DR-Scan, Select-IR-Scan
No specific function is performed in these states; the TAP exits either of them on the next TCK cycle.

Capture-DR
The selected data register is placed in the scan path (i.e., between TDI and TDO). Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK causing the TAP state to change.

Shift-DR
In this state, data is serially shifted through the selected data register, from TDI to TDO, on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). On the falling edge of TCK, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the level present before it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the low level.

Exit1-DR, Exit2-DR
These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-DR to Exit1-DR.

Pause-DR
The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data.

Update-DR
If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated only during this state.

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state diagram description (continued)

Capture-IR
The instruction register is preloaded with the IR status word (see Table 4) and placed in the scan path.

Shift-IR
In this state, data is serially shifted through the instruction register, from TDI to TDO, on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). On the falling edge of TCK in Shift-IR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the high level.

Exit1-IR, Exit2-IR
These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-IR to Exit1-IR.

Pause-IR
The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR
In this state, the latches shadowing the instruction register are updated with the new instruction.

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signal descriptions

TDI—Test Data In
One of the four pins required by IEEE Standard 1149.1, TDI is the serial input for shifting information into the instruction register or data registers. TDI is typically driven by the TDO pin of the primary bus controller. An internal pullup resistor forces TDI to a high level if left unconnected.

TDO—Test Data Out
One of the four pins required by IEEE Standard 1149.1, TDO is the serial output for shifting information from the instruction register or data registers. TDO is typically connected to the TDI pin of the next testable device in the primary scan path.

TCK—Test Clock
One of the four pins required by IEEE Standard 1149.1. Operation of the 'ACT8999, except for the count function, is synchronous to TCK. Data appearing at the device inputs is captured on the rising edge of TCK; outputs change on the falling edge of TCK.

TMS—Test Mode Select
One of the four pins required by IEEE Standard 1149.1. The level of TMS at the rising edge of TCK directs the 'ACT8999 through its state machine. An internal pullup resistor forces TMS to a high level if left unconnected.

$\overline{\text{TRST}}$—Test Reset
This active-low pin implements the optional reset function of IEEE Standard 1149.1. When asserted, $\overline{\text{TRST}}$ causes the 'ACT8999 to enter the Test-Logic-Reset state and to configure the instruction register and data registers to their power-up values. $\overline{\text{TRST}}$ is also output, without inversion, via $\overline{\text{DTRST}}$ (device test reset). An internal pullup forces $\overline{\text{TRST}}$ to a high level if left unconnected.

OTMS—Optional Test Mode Select
This pin can be used instead of TMS to control (with TCK) the select register. This is useful when a remote bus controller is available to control the secondary scan path(s). An internal pullup resistor forces OTMS to a high level if left unconnected.

DTMS1–DTMS4—Device Test Mode Select 1–4
Either none or one of these four output pins can be selected to follow the TMS pin or OTMS pin to include a secondary scan path in the primary scan path. The unselected DTMS pins can be independently set to a static high or low level. The TMS circuit monitors input from the control register to determine the configuration of the DTMS pins.

MCI—Master Condition Input
This pin receives interrupt and protocol signals from a PBC.

MCO—Master Condition Output
This pin transmits interrupt and protocol signals to an RBC and/or the secondary scan path(s). It also outputs an active-low error signal during the Pause-DR TAP state if an RBC loads an invalid value in the select register.

DCI—Device Condition Input
This pin receives interrupt and protocol signals from an RBC and/or the secondary scan path(s). When the counter register is instructed to count up or down, the DCI pin is configured as the counter clock.

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signal descriptions (continued)

DCO—Device Condition Output
DCO is configured by the control register to output protocol and interrupt signals to a PBC. It can also be configured by the control register to output an error signal if the instruction register or select register are loaded with invalid values. DCO is further configured by the control register as:
1) Active-high or active-low (reset condition = active-low).
2) Open-drain or three-state (reset condition = open-drain).

DTDI—Device Test Data In
This pin receives the serial test data output of the selected secondary scan path.

DTDO—Device Test Data Out
This pin outputs serial test data to the TDI input(s) of the secondary scan paths.

DTCK—Device Test Clock
This pin outputs the buffered test clock TCK to the secondary scan path(s).

$\overline{\text{DTRST}}$—Device Test Reset
This active-low output transmits a reset signal to the secondary scan path(s). $\overline{\text{DTRST}}$ can be asserted by a bit in the control register or by setting $\overline{\text{TRST}}$ low.

ID1–ID8—Identification 1–8
This eight-bit data bus can be used to communicate with an RBC and pass data and control instructions. By wiring pullup and pulldown resistors to these pins, one of 255 unique identification codes can be assigned to the device, allowing a test controller to verify or determine the identity of the subsystem under test.

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functional block description

The 'ACT8999 implements two separate functions in one package. The primary function of the device is to include a selected secondary scan path in the system's primary scan path to enable a PBC to perform controlling and observing test functions on the selected path. This is accomplished by driving the TMS pin(s) of a secondary scan path with one of the DTMS pins of the device. This approach allows a system to have built-in testability at all levels without requiring that the primary system scan path always include all subsystem scan paths. As a result, test throughput is improved and the amount of test data that must be interpreted is reduced. The device includes error detection circuitry that prevents the user from inadvertently activating more than one secondary scan path at a time.

Another function of the device is provided by the 8-bit identification bus. This bus can be hard-wired with pullup and pulldown resistors to supply an identification code to the test controller(s) to verify that test operations are being performed on the proper portion of the system. The bus can also transfer data and instructions to another device, such as a local or remote bus controller, and pass control of the scan path select function to that device. This frees the primary controller to activate another secondary scan path elsewhere in the system or perform higher-level test control functions. When the RBC is ready to return control of the device, interrupt signals alert the primary controller.

The least significant bit (LSB) of any value to be scanned into any register of the device is defined to be the first bit shifted in (nearest to TDO). The most significant bit (MSB) is defined to be the last bit shifted in (nearest to TDI).

The 'ACT8999 is divided into functional blocks as detailed below.

test ports

The test ports decode the signals on TCK, TMS, OTMS, and $\overline{\text{TRST}}$ to control the operation of the circuit. The test ports include a TAP that issues the proper control instructions to the data registers according to the IEEE Standard 1149.1 protocol. The TAP state diagram is shown in Figure 1.

Two test ports are included on the 'ACT8999, allowing different test controllers to command different sections of the device.

TMS circuit

The TMS circuit decodes bits in the select and control registers to determine which one, if any, of the DTMS pins (which provide mode select signals to the secondary scan path(s)) will follow the TMS pin or OTMS pin. The unselected DTMS pins are set by the circuit to a static high or low level.

instruction register

The instruction register (IR) is an eight-bit-wide serial shift register that issues commands to the device. Data is input into the instruction register via TDI or DTDI and shifted out via TDO. All device operations are initiated by loading the proper instruction or set of instructions into the IR.

data registers

Six parallel data registers are included in the 'ACT8999: bypass, control, counter, boundary scan, ID bus, and select. The ID bus register is a part of the boundary scan register. Each data register is serially loaded via TDI or DTDI and outputs data via TDO.

Table 1 summarizes the registers in the 'ACT8999.

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TABLE 1. REGISTER SUMMARY

REGISTER NAME	LENGTH (BITS)	FUNCTION
Instruction	8	Issue command information to the device
Remote Instruction	8	Issue command information to the select register
Control	13	Configuration and enable control
Counter	8	Count events on DCI, output interrupts via DCO
Select	8	Select one of four DTMS pins to follow TMS or OTMS
Boundary Scan	15	Capture and force test data at device periphery
ID Bus	8	Pass test commands and data between a PBC and RBC(s)
Bypass	1	Remove the 'ACT8999 from the scan path

instruction register description

The instruction register is an eight-bit serial shift register that outputs commands to the device. Table 2 lists the instructions implemented in the 'ACT8999 and the data register selected by each instruction.

The most significant bit of the IR is an even-parity bit. If the value scanned into the IR during Shift-IR does not contain even parity, an error signal, $\overline{\text{IRERR}}$, is generated internally as shown in Table 3. The 'ACT8999 can be configured to output $\overline{\text{IRERR}}$ via DCO if the TAP enters the Pause-IR state.

The IR status word is loaded during the Capture-IR state. The IR status word contains information about the most recently loaded values of the instruction and select registers and the logic level present at the DCI input. The IR status word is encoded as shown in Table 4.

Figure 2 illustrates the order of scan for the instruction register.

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TABLE 2. INSTRUCTION REGISTER OPCODES

BINARY CODE BIT 7 → BIT 0 MSB → LSB	HEX VALUE	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER
00000000	00	EXTEST	Boundary Scan	Boundary Scan
10000001	81	BYPASS†	Bypass Scan	Bypass
10000010	82	SAMPLE/PRELOAD	Sample Boundary	Boundary Scan
00000011	03	INTEST	Boundary Scan	Boundary Scan
10000100	84	BYPASS†	Bypass Scan	Bypass
00000101	05	BYPASS†	Bypass Scan	Bypass
00000110	06	BYPASS†	Bypass Scan	Bypass
10000111	87	BYPASS†	Bypass Scan	Bypass
10001000	88	COUNT	Count	Counter
00001001	09	COUNT	Count	Counter
00001010	0A	BYPASS†	Bypass Scan	Bypass
10001011	8B	BYPASS†	Bypass Scan	Bypass
00001100	0C	BYPASS†	Bypass Scan	Bypass
10001101	8D	BYPASS	Bypass Scan	Bypass
10001110	8E	SCANCN	Control Register Scan	Control
00001111	0F	SCANCT	Control Register Scan	Control
11111010	FA	SCANCNT	Counter Scan	Counter
01111011	7B	READCNT	Counter Read	Counter
11111100	FC	SCANIDB	ID Bus Register Scan	ID Bus
01111101	7D	READIDB	ID Bus Register Read	ID Bus
01111110	7E	SCANSEL	Select Register Scan	Select
ALL OTHER		BYPASS	Bypass Scan	Bypass

† A SCOPE™ opcode exists but is not supported by the 'ACT8999.

TABLE 3. $\overline{\text{IRERR}}$ FUNCTION TABLE

NUMBER OF INSTRUCTION REGISTER BITS = 1	$\overline{\text{IRERR}}$
0, 2, 4, 6, 8	1
1, 3, 5, 7	0

TABLE 4. INSTRUCTION REGISTER STATUS WORD

IR BIT	VALUE‡
7	$\overline{\text{IRERR}}$ (see Table 3)
6	0
5	0
4	0
3	Level present at DCI input (1 = H, 0 = L)
2	$\overline{\text{SRERR}}$ (see Table 8)
1	0
0	1

‡ This value is loaded in the instruction register during the Capture-IR TAP state.

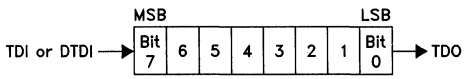

FIGURE 2. INSTRUCTION REGISTER BITS AND ORDER OF SCAN

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instruction register opcode descriptions

The operation of the 'ACT8999 is dependent on the instruction loaded into the instruction register. Each instruction selects one of the data registers to be placed between TDI or DTDI and TDO during the shift-DR TAP state.

All the required instructions of IEEE Standard 1149.1 are implemented in the 'ACT8999.

boundary scan
This instruction implements the required EXTEST and INTEST operations of IEEE Standard 1149.1. The boundary scan register (which includes the ID bus register) is placed in the scan path. Data on input pins included in the boundary scan register is captured; data previously loaded into the output pins included in the boundary scan register is forced through the outputs.

bypass scan
This instruction implements the required BYPASS operation of IEEE Standard 1149.1. The bypass register is placed in the scan path and preloads with a logic 0 during Capture-DR.

sample boundary
This instruction implements the required SAMPLE/PRELOAD operation of IEEE Standard 1149.1. The boundary scan register is placed in the scan path and data appearing at the inputs and outputs included in the boundary scan register is sampled on the rising edge of TCK in Capture-DR.

count
The counter register begins counting on each DCI transition. The count begins at the value in the register before the count instruction was loaded. The counter can be programmed to count up or down on either the low-to-high or high-to-low transition of DCI. Counting occurs only while the device is in the Run-Test/Idle TAP state.

counter register read
The counter register is placed in the scan path. During Capture-DR, the prior preloaded value of the counter is loaded into the counter register. At Update-DR, a new preload value is loaded.

counter register scan
The counter register is placed in the scan path. During Capture-DR, the current value of the counter is loaded in the counter register. At Update-DR, a new preload value is loaded.

control register scan
The control register is placed in the scan path for a subsequent shift operation.

ID bus register scan
The ID bus register (part of the boundary scan register) is placed in the scan path for a subsequent shift operation. The data on the ID bus is loaded into the ID bus register on the rising edge of TCK in Capture-DR.

ID bus register read
The ID bus register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

select register scan
The select register is placed in the scan path for a subsequent shift operation

control register description

The control register (CTLR) is a 13-bit serial register that controls the enable and select functions of the 'ACT8999. A reset operation forces all bits to a logic 0. The contents of the control register are latched and decoded during the Update-DR TAP state. The specific function of each bit is listed in Table 5.

The enable and select functions of the control register bits are mapped as follows:

Bit 12—$\overline{\text{Up}}$/Down
This bit sets the count mode of the counter register (reset condition = count up).

Bit 11—Latch on Zero
The counter register can be configured to stop counting when its value is 00000000 and ignore subsequent transitions on the counter clock, DCI. The latch-on-zero option is valid only in the count-down mode (reset condition = do not latch on zero). The value of this bit has no effect on the operation of the counter if CTLR bit 12 = 0.

Bit 10—DCO Polarity Select
DCO can be configured as an active-low or active-high output (reset condition = active-low). When active-low, DCO does not invert the signal selected to drive it; when active-high, DCO inverts the selected signal.

Bit 9/Bit 8—DCO Source Select 1/DCO Source Select 0
DCO can be used to output two error signals generated by the 'ACT8999: $\overline{\text{IRERR}}$ (see Table 3) and $\overline{\text{SRERR}}$ (see Table 8). Bits 9 and 8 can be set to output $\overline{\text{IRERR}}$ via DCO on the falling edge of TCK in the Pause-IR state and $\overline{\text{SRERR}}$ via DCO on the falling edge of TCK in the Pause-DR state. DCO can also be configured to become active when the value of the counter is 00000000, to follow DCI, or be set to a static high or low level (reset condition = static high level).

Bit 7—Parity Mask
The internal error signals can be masked from appearing on DCO even if bits 9 and 8 are set such that $\overline{\text{IRERR}}$ and $\overline{\text{SRERR}}$ will be output in the Pause-IR and Pause-DR states (reset condition = do not mask $\overline{\text{IRERR}}$ or $\overline{\text{SRERR}}$).

Bit 6—DCO Drive Select
DCO can be configured as either an open-drain or 3-state output (reset condition = open-drain). The open-drain configuration allows multiple DCO outputs to be used in a wired-OR or wired-AND application. The three-state configuration allows the DCO output to be connected to a bus.

Bit 5—DCO Enable
When configured as a 3-state output, DCO can be placed in the high-impedance state (reset condition = disabled). If configured as an open-drain output and disabled, DCO outputs a high level.

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control register description (continued)

Bit 4—DCI Polarity Select
The level at the DCI input can be inverted before being applied to the internal logic of the device (reset condition = do not invert DCI).

Bit 3—Device Test Pins Output Enable
DTCK, DTDO, and the DTMS1–4 pin can be placed in the high-impedance state (disabled) with this bit (reset condition = enabled).

Bit 2—ID Bus Enable
The ID bus (ID1–8) is a bidirectional bus. The output buffers are enabled and disabled with this bit (reset condition = output buffers disabled).

Bit 1—Remote Bus Controller Enable
An RBC can issue protocol and data instructions to the select register if the 'ACT8999 is configured to allow it (reset condition = RBC disabled). When an RBC is enabled, the TAP in the select register operates according to the OTMS signal.

Bit 0—Device Test Reset
$\overline{\text{DTRST}}$ can be configured to output a reset signal independently of the level on $\overline{\text{TRST}}$ (reset condition = no reset signal issued).

Several control register bits affect the functionality of the DCO output. The DCO function table is given in Table 6.

Figure 3 illustrates the order of scan for the control registers.

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TABLE 5. CONTROL REGISTER BIT MAPPING

BIT	VALUE	FUNCTION
12	0	Configure counter to count up.
	1	Configure counter to count down.
11	0	Do not stop counting when the count reaches 00000000.
	1	Stop counting when the count reaches 00000000.
10	0	Configure DCO as an active-low output.
	1	Configure DCO as an active-high output.
9, 8	00	DCO = H or L (depends on CTLR Bit 10).
	01	DCO = ($\overline{\text{IRERR}}$ • $\overline{\text{SRERR}}$).
	10	DCO = $\overline{\text{CE}}$, an internal logic 0 generated when the count is 00000000.
	11	DCO = DCI.
7	0	Do not mask $\overline{\text{IRERR}}$ and $\overline{\text{SRERR}}$ from DCO.
	1	Mask $\overline{\text{IRERR}}$ and $\overline{\text{SRERR}}$ from DCO.
6	0	Configure DCO as an open-drain output.
	1	Configure DCO as a 3-state output.
5	0	Disable DCO.
	1	Enable DCO.
4	0	DCI = DCI.
	1	DCI = $\overline{\text{DCI}}$ (invert the DCI signal before applying it to the internal logic).
3	0	Enable DTCK, DTDO, and DTMS1–4.
	1	Disable DTCK, DTDO, and DTMS1–4.
2	0	Disable ID1–8.
	1	Enable ID1–8.
1	0	Disable RBC.
	1	Enable RBC.
0	0	$\overline{\text{DTRST}}$ = $\overline{\text{TRST}}$.
	1	$\overline{\text{DTRST}}$ = L.

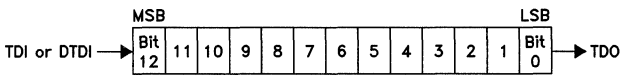

FIGURE 3. CONTROL REGISTER BITS AND ORDER OF SCAN

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TABLE 6. DCO FUNCTION TABLE

DCI	INTERNAL SIGNALS†			CONTROL REGISTER BITS‡							DCO
	$\overline{IRERR}$	$\overline{SRERR}$	$\overline{CE}$	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	
X	X	X	X	X	X	X	X	0	0	X	H
X	X	X	X	X	X	X	X	1	0	X	Z
X	X	X	X	0	0	0	X	X	1	X	H
X	X	X	X	1	0	0	X	X	1	X	L
X	X	X	X	0	0	1	1	X	1	X	H
X	X	X	X	1	0	1	1	X	1	X	L
X	0	X	X	0	0	1	0	X	1	X	L in Pause-IR§, H otherwise
X	X	0	X	0	0	1	0	X	1	X	L in Pause-DR§, H otherwise
X	1	1	X	0	0	1	0	X	1	X	H
X	0	X	X	1	0	1	0	X	1	X	H in Pause-IR§, L otherwise
X	X	0	X	1	0	1	0	X	1	X	H in Pause-DR§, L otherwise
X	1	1	X	1	0	1	0	X	1	X	L
X	X	X	0	0	1	0	X	X	1	X	L
X	X	X	0	1	1	0	X	X	1	X	H
X	X	X	1	0	1	0	X	X	1	X	H
X	X	X	1	1	1	0	X	X	1	X	L
L	X	X	X	0	1	1	X	X	1	0	L
L	X	X	X	0	1	1	X	X	1	1	H
L	X	X	X	1	1	1	X	X	1	0	H
L	X	X	X	1	1	1	X	X	1	1	L
H	X	X	X	0	1	1	X	X	1	0	H
H	X	X	X	0	1	1	X	X	1	1	L
H	X	X	X	1	1	1	X	X	1	0	L
H	X	X	X	1	1	1	X	X	1	1	H

† These signals are generated as described elsewhere in this datasheet.

‡ The control register must contain these values after the TAP has passed through its most recent Update-DR state.

§ DCO is active on the falling edge of TCK as the TAP enters the appropriate pause state (Pause-IR or Pause-DR) and is inactive on the falling edge of TCK as the TAP enters the appropriate exit2 state (Exit2-IR or Exit2-DR).

select register description

The select register (SR) is an eight-bit serial register that determines which one, if any, of the DTMS lines follows the TMS or OTMS input. A reset operation forces all bits to a logic 0. The register is divided into four two-bit sections, each of which controls one DTMS output. Figure 4 shows the mapping of the bits to the DTMS outputs and the order of scan. For each DTMS pin, the higher order bit is the MSB and the lower order bit is the LSB (e.g., bit 3 is the MSB of DTMS2 and bit 2 is the LSB of DTMS2).

Only one of the four DTMS outputs can be selected to drive a secondary scan path with TMS or OTMS. If the select register is loaded with an invalid value, an error signal, $\overline{\text{SRERR}}$, is generated internally as shown in Table 8. If the TAP enters the Pause-DR state, $\overline{\text{SRERR}}$ may be output via DCO (see Table 8). If the TAP enters the Update-DR state while an invalid value is in the SR, all four DTMS outputs are set to a high level. The SR bit decoding is shown in Table 7.

The SR can also be accessed from an RBC. A test port in the register contains a TAP that can be enabled by the control register to monitor the values of TCK and OTMS to perform scan operations on the SR.

TABLE 7. SELECT REGISTER BIT DECODING

MSB	LSB	DTMSn SOURCE
0	0	High
0	1	Low
1	0	OTMS
1	1	TMS

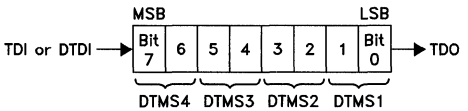

FIGURE 4. SELECT REGISTER BITS AND ORDER OF SCAN

TABLE 8. $\overline{\text{SRERR}}$ FUNCTION TABLE

SELECT REGISTER BITS								$\overline{\text{SRERR}}$
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
0	X	0	X	0	X	0	X	1
1	X	0	X	0	X	0	X	1
0	X	1	X	0	X	0	X	1
0	X	0	X	1	X	0	X	1
0	X	0	X	0	X	1	X	1
1	X	1	X	X	X	X	X	0
1	X	X	X	1	X	X	X	0
1	X	X	X	X	X	1	X	0
X	X	1	X	1	X	X	X	0
X	X	1	X	X	X	1	X	0
X	X	X	X	1	X	1	X	0

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boundary scan register/ID bus register description

The boundary scan register (BSR) is a 15-bit serial register that can be used to capture data appearing at selected device inputs, force data through device outputs, and apply data to the device's internal logic. The BSR is made up of boundary scan cells (BSCs). Table 9 lists the device signal for each of the fifteen BSCs that comprise the BSR.

The eight BSCs connected to the ID1–8 pins form a subset of the BSR called the ID bus register (IDBR). The IDBR can be scanned without accessing the remaining BSCs of the BSR.

The IDBR is used when the ID bus is enabled to allow communication between a PBC and one or more RBCs.

Figure 5 illustrates the order of scan for the boundary scan register and ID bus register.

TABLE 9. BOUNDARY SCAN REGISTER BIT MAPPING

BIT	PIN NAME	SIGNAL DESCRIPTION
14	MCI	Master Condition In
13	MCO	Master Condition Out
12	DCI	Device Condition In
11	$\overline{\text{DCOTS}}$†	Enable control for DCO in 3-state configuration (active-low)
10	$\overline{\text{DCOOD}}$†	Enable control for DCO in open-drain configuration (active-low)
9	DCO	Device Condition Out
8	$\overline{\text{IDBOE}}$†	Enable control for ID bus (active-low)
7	ID8	Identification Bus Bit 8
6	ID7	Identification Bus Bit 7
5	ID6	Identification Bus Bit 6
4	ID5	Identification Bus Bit 5
3	ID4	Identification Bus Bit 4
2	ID3	Identification Bus Bit 3
1	ID2	Identification Bus Bit 2
0	ID1	Identification Bus Bit 1

† This internal signal cannot be observed from the I/O pins of the device.

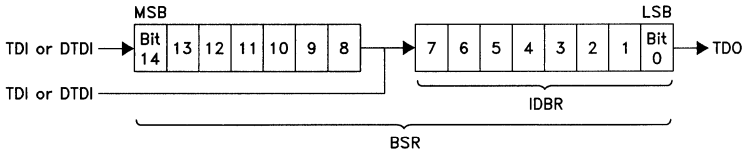

FIGURE 5. BOUNDARY SCAN REGISTER BITS AND ORDER OF SCAN

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bypass register description

The bypass register (BR) is a one-bit serial register. The function of the BR is to provide a means of effectively removing the 'ACT8999 from the primary scan path when it is not needed for the current test operation or other function of the PBC. At power-up, the BR is placed in the scan path.

Figure 6 shows the order of the scan for the bypass register.

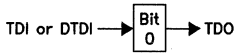

FIGURE 6. BYPASS REGISTER BITS AND ORDER OF SCAN

counter register description

The counter register (CNTR) is an eight-bit serial register that performs a binary count if configured to do so by the control register; it uses the DCI pin as its clock. The counter can be preloaded with an initial value before counting begins, and the current value of the counter can be scanned out. Many of the features of the CNTR are configured by a bit in the control register, including:

1) Count direction (up or down).
2) Stop counting when the value of the register is 00000000.
3) DCI transition on which the counter counts (low-to-high or high-to-low).

An internal signal, $\overline{CE}$, is generated as a logic 0 when the value of the CNTR is 00000000. For any other value of the CNTR, $\overline{CE} = 1$.

The counter register can be used to count events occurring on the secondary scan path(s) and can output interrupt signals via DCO when the count has reached zero.

Figure 7 shows the order of scan for the counter register.

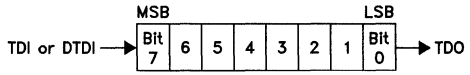

FIGURE 7. COUNTER REGISTER BITS AND ORDER OF SCAN

enabling a remote bus controller

Bit 1 in the control register allows a remote bus controller to control parts of the 'ACT8999. When an RBC is enabled, the remote test port (RTP) in the select register is activated. The remote test port operates according to the same state diagram as the primary test port but only has access to the select register. Operation of the RTP is synchronous to TCK. OTMS is the RTP's mode select pin.

The RTP contains an eight-bit instruction register. Data is shifted in via DTDI and shifted out via DTDO. As shown in Table 10, only one instruction selects something other than the bypass register to be included in the scan path. When SCANSEL is executed, the select register is placed between DTDI and DTDO. The function of the select register, and the decoding of the select register bits by the TMS circuit, is identical regardless of which test port accesses the register.

An internal error signal, $\overline{\text{RSRERR}}$, is generated if an RBC loads an invalid value in the select register, and the MCO output goes low if the $\overline{\text{RSRERR}}$ is active and the remote TAP enters the Pause-DR state. The function table for $\overline{\text{RSRERR}}$ is shown in Table 11.

The RTP does not have access to the control register, so it cannot disable itself. The PBC must reset bit 1 in the control register to return control of the select register to the primary test port.

TABLE 10. REMOTE TEST PORT INSTRUCTION REGISTER OPCODES

BINARY CODE BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER
01111110	SCANSEL	Select Register Scan	Select
ALL OTHER	BYPASS	Bypass Scan	Bypass

TABLE 11. $\overline{\text{RSRERR}}$ FUNCTION TABLE

SELECT REGISTER BITS								$\overline{\text{RSRERR}}$	MCO†
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		
0	X	0	X	0	X	0	X	1	MCI
1	X	0	X	0	X	0	X	1	MCI
0	X	1	X	0	X	0	X	1	MCI
0	X	0	X	1	X	0	X	1	MCI
0	X	0	X	0	X	1	X	1	MCI
1	X	1	X	X	X	X	X	0	L
1	X	X	X	1	X	X	X	0	L
1	X	X	X	X	X	1	X	0	L
X	X	1	X	1	X	X	X	0	L
X	X	1	X	X	X	1	X	0	L
X	X	X	X	1	X	1	X	0	L

† This table is valid only when the remote TAP is in the Pause-DR state. Under any other condition, MCO = MCI.

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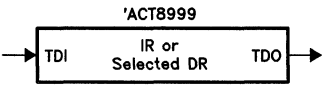
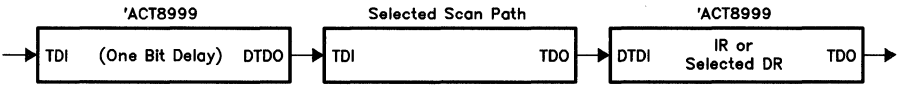
data flow description

The direction of serial data flow in the 'ACT8999 is dependent on the current instruction. Figure 8 shows the data flow for the different operating modes of the device. Note that when a secondary scan path is selected, the 'ACT8999 adds one bit of delay from TDI to DTDO.

RBC disabled, no secondary scan path selected



RBC disabled, secondary scan path selected



RBC enabled

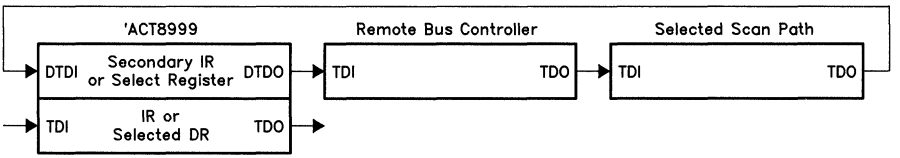


FIGURE 8. DATA FLOW IN THE 'ACT8999

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bus communication protocol

The eight-bit identification bus (ID1–8) allows data transfer between a PBC and an RBC. Control register bit 2 configures the 'ACT8999 to transmit or receive command and test data via the ID bus register. The DCI, DCO, MCI, and MCO pins are used to signal the PBC and RBC(s) that a data transfer is required. The 'ACT8999 can accommodate either local or global handshake protocol depending on the number of DCO inputs that the PBC can accommodate.

Figure 9 shows a protocol for local communication between the PBC and an RBC. In this mode, communication is initiated by the PBC by driving the MCI input of the 'ACT8999 to a low level. MCI is buffered and output on MCO, which notifies the RBC that control of a scan path is to be relinquished. Prior to activating the MCI signal, the PBC scans the value 00000000 into the IDBR and enables the output buffers of ID1–8. When the RBC recognizes that MCO has gone low, it samples the ID bus and looks for the 00000000 value to verify that the PBC is going to issue further commands. Upon verifying the value on the ID bus, the RBC drives DCI low, which is buffered and output via DCO. (In this example, DCI is configured as noninverting and DCO is configured as active-low.) When the PBC sees that DCO is active, it takes MCI high, forcing MCO high. When the PBC sees that MCO is high, it takes DCO high (inactive), completing one handshake cycle.

A similar operation can ensue when the RBC initiates communication with the PBC as shown in Figure 9. Commands and test data can be exchanged between two bus controllers via the ID bus.

Figure 10 shows one way of using the ID bus to interface a PBC to multiple RBCs. The timing is similar to the local communication example in Figure 9 except that the PBC waits for all RBCs to acknowledge transmissions before switching MCI.

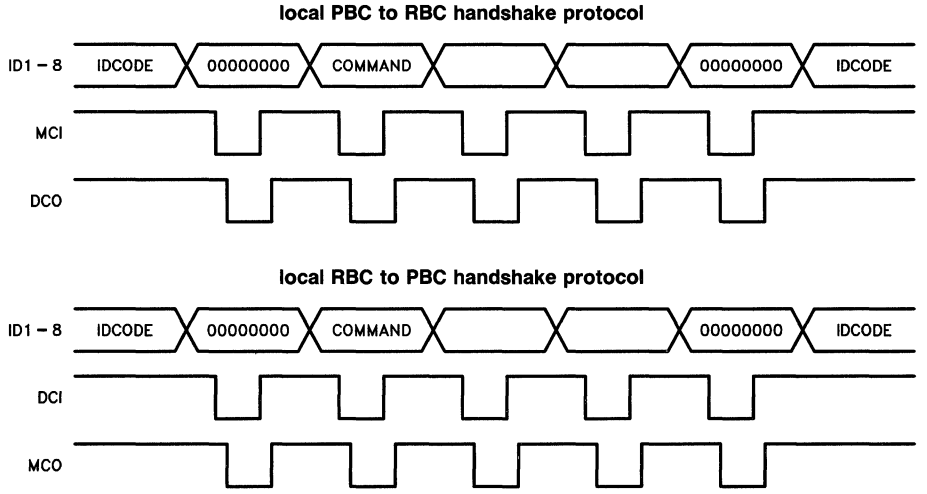

FIGURE 9. LOCAL BUS COMMUNICATION PROTOCOL

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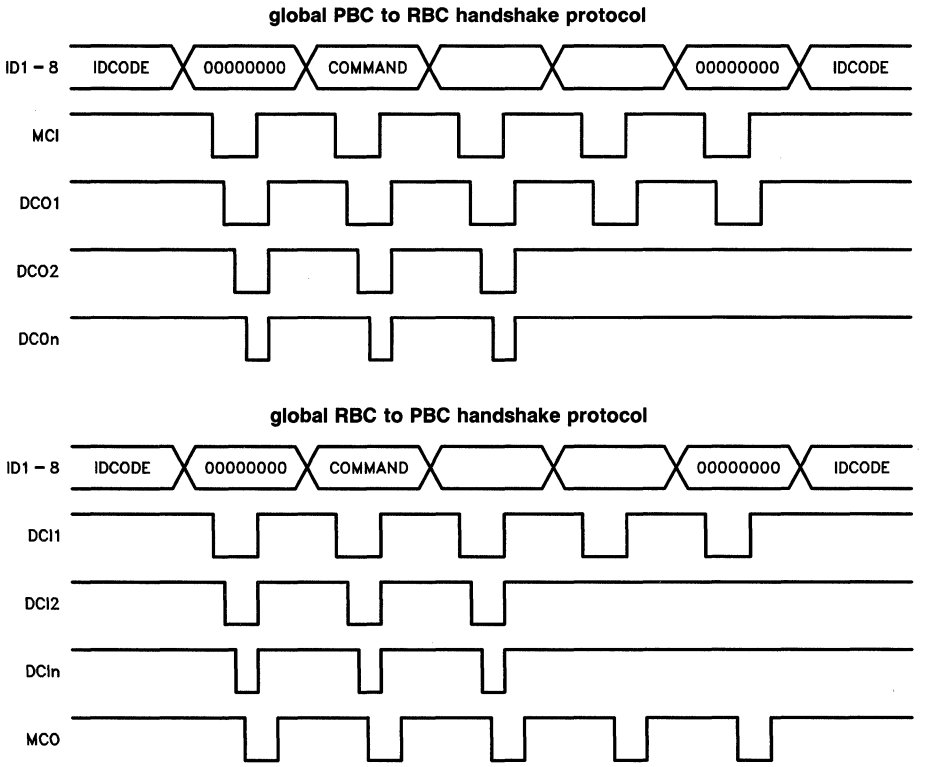

FIGURE 10. GLOBAL BUS COMMUNICATION PROTOCOL

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_I < 0 or V_I > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pin ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			'54ACT8999		'74ACT8999		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		
V_{IL}	Low-level input voltage			0.8		0.8	
V_{OH}	High-level output voltage	DCO		5.5		5.5	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	
I_{OH}	High-level output current	ID1–8		−1.6		−2	mA
		TDO, DTDO, MCO		−8.5		−10	
		DTMS1–4, DCO, $\overline{\text{DTRST}}$, DTCK		−13.6		−16	
I_{OL}	Low-level output current	ID1–8		1.6		2	
		TDO, DTDO, MCO		8.5		10	
		DTMS1–4, DCO		13.6		16	
		$\overline{\text{DTRST}}$		20.4		24	
		DTCK		40.8		48	
T_A	Operating free-air temperature		−55	125	0	70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	'54ACT8999		'74ACT8999		UNIT
				MIN	MAX	MIN	MAX	
I_{OH}	DCO (open-drain)	V_O = 5.5 V	5.5 V		20		10	μA
V_{OH}	ID1–8	I_{OH} = −1.6 mA	4.5 V	3.7				V
		I_{OH} = −2 mA	4.5 V			3.7		
	TDO, DTDO, MCO	I_{OH} = −8.5 mA	4.5 V	3.7				
		I_{OH} = −10 mA	4.5 V			3.7		
	DTMS1–4, DCO (3-state), $\overline{DTRST}$, DTCK	I_{OH} = −13.6 mA	4.5 V	3.7				
		I_{OH} = −16 mA	4.5 V			3.7		
V_{OL}	ID1–8	I_{OL} = 1.6 mA	4.5 V		0.5			V
		I_{OL} = 2 mA	4.5 V				0.5	
	TDO, DTDO, MCO	I_{OL} = 8.5 mA	4.5 V		0.5			
		I_{OL} = 10 mA	4.5 V				0.5	
	DTMS1–4, DCO	I_{OL} = 13.6 mA	4.5 V		0.5			
		I_{OL} = 16 mA	4.5 V				0.5	
	$\overline{DTRST}$	I_{OL} = 20.4 mA	4.5 V		0.5			
		I_{OL} = 24 mA	4.5 V				0.5	
	DTCK	I_{OL} = 40.8 mA	4.5 V		0.5			
		I_{OL} = 48 mA	4.5 V				0.5	
I_{OZ}†	ID1–8, DTDO, DTMS1–4, DTCK	V_O = V_{CC} or GND	5.5 V		±10		±5	μA
	DCO	V_O = V_{CC} or GND	5.5 V		±20		±10	
I_I	MCI, DCI, TCK	V_I = V_{CC} or GND	5.5 V		±1		±1	μA
	TDI, DTDI, TMS, OTMS, $\overline{TRST}$	V_I = V_{CC} or GND	5.5 V	−0.1	−20	−0.1	−20	
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V		100		100	μA
ΔI_{CC}‡		One input at V_{IH} or V_{IL}, Other inputs at V_{CC} or GND	5.5 V		2		0.5	mA

† For I/O pins, the parameter I_{OZ} includes the input leakage current.
‡ This is the increase in supply current for each input being driven at TTL levels rather than V_{CC} or GND.

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timing requirements over recommended ranges of operating free-air temperature and supply voltage

			'54ACT8999		'74ACT8999		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}		TCK	0	20	0	20	MHz
		DCI (Count mode)	0	20	0	20	
t_w	Pulse duration	TCK high or low					ns
		DCI high or low (Count mode)					
t_{su}	Setup time	TMS before TCK ↑					ns
		OTMS before TCK ↑					
		TDI before TCK ↑					
		DTDI before TCK ↑					
		MCI before TCK ↑					
		DCI before TCK ↑					
		Any ID before TCK ↑					
t_h	Hold time	TMS after TCK ↑					ns
		OTMS after TCK ↑					
		TDI after TCK ↑					
		DTDI after TCK ↑					
		MCI after TCK ↑					
		DCI after TCK ↑					
		Any ID after TCK ↑					
t_d	Delay time	Power up to TCK ↑					ns

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switching characteristics over recommended ranges of operating free-air temperature and supply voltage

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'54ACT8999 MIN	'54ACT8999 MAX	'74ACT8999 MIN	'74ACT8999 MAX	UNIT
f_{max}	TCK		20		20		MHz
	DCI (Count mode)		20		20		
t_{PLH}	TCK ↓	TDO					ns
t_{PHL}							
t_{PLH}	TCK ↓	$\overline{DTRST}$					ns
t_{PHL}							
t_{PLH}	TCK ↓	Any DTMS					ns
t_{PHL}							
t_{PLH}	TCK ↓	DTDO					ns
t_{PHL}							
t_{PLH}	TCK ↓	Any ID					ns
t_{PHL}							
t_{PLH}	TLK ↓	MCO					ns
t_{PHL}							
t_{PLH}	TCK ↓	DCO (open-drain)					ns
		DCO (three-state)					
t_{PHL}	TCK ↓	DCO (open-drain)					ns
		DCO (three-state)					
t_{PLH}	TMS	Any DTMS					ns
t_{PHL}							
t_{PLH}	OTMS	Any DTMS					ns
t_{PHL}							
t_{PLH}	MCI	MCO					ns
t_{PHL}							
t_{PLH}	DCI	DCO (open-drain)					ns
		DCO (three-state)					
t_{PHL}	DCI	DCO (open-drain)					ns
		DCO (three-state)					
t_{PLH}	$\overline{TRST}$	$\overline{DTRST}$					ns
t_{PHL}							
t_{PLH}	TCK	DTCK					ns
t_{PHL}							

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switching characteristics over recommended ranges of operating free-air temperature and supply voltage (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'54ACT8999		'74ACT8999		UNIT
			MIN	MAX	MIN	MAX	
t_{PHZ}	TCK ↓	DTCK					ns
t_{PLZ}							
t_{PHZ}	TCK ↓	TDO					ns
t_{PLZ}							
t_{PHZ}	TCK ↓	DTDO					ns
t_{PLZ}							
t_{PHZ}	TCK ↓	DCO					ns
t_{PLZ}							
t_{PHZ}	TCK ↓	Any DTMS					ns
t_{PLZ}							
t_{PHZ}	TCK ↓	Any ID					ns
t_{PLZ}							
t_{PZH}	TCK ↓	DTCK					ns
t_{PZL}							
t_{PZH}	TCK ↓	TDO					ns
t_{PZL}							
t_{PZH}	TCK ↓	DTDO					ns
t_{PZL}							
t_{PZH}	TCK ↓	DCO					ns
t_{PZL}							
t_{PZH}	TCK ↓	Any DTMS					ns
t_{PZL}							
t_{PZH}	TCK ↓	Any ID					ns
t_{PZL}							

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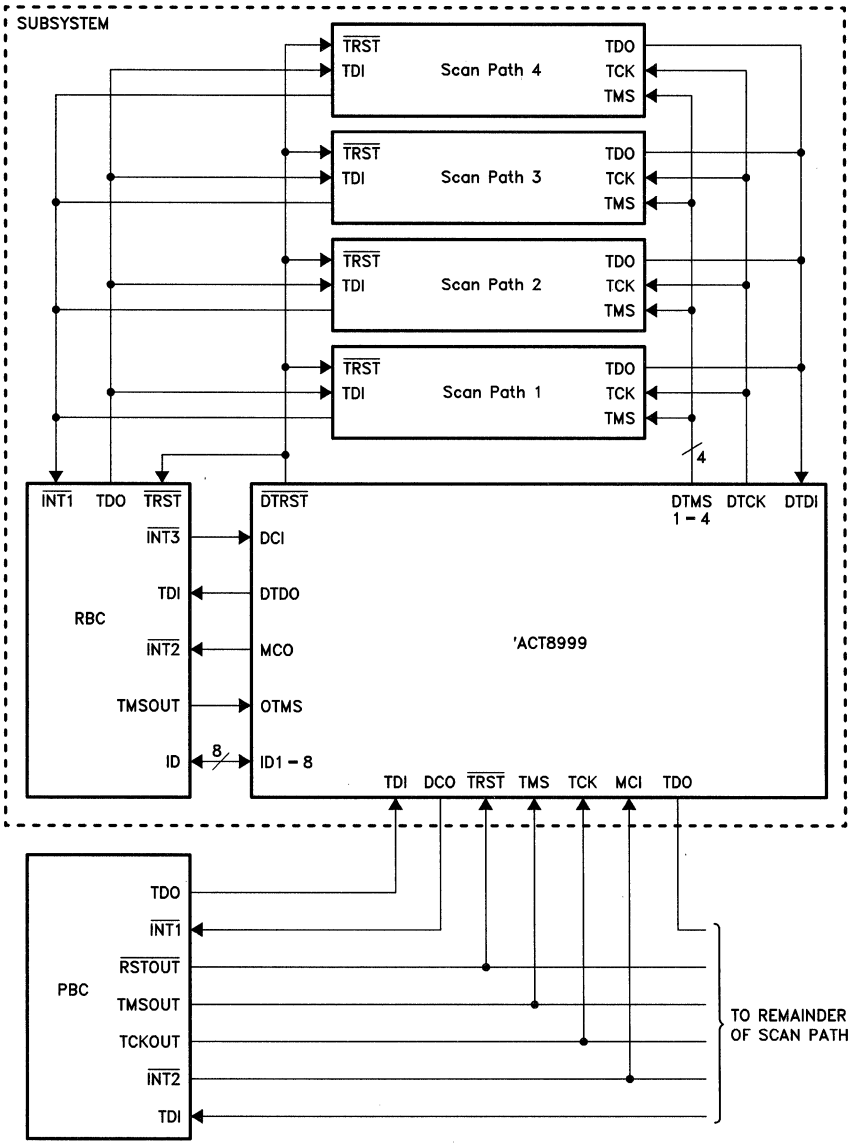
APPLICATION INFORMATION



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SCBS042—TI0037—D3413, FEBRUARY 1990

- **Members of Texas Instruments SCOPE™ Family of Testability Products**
- **Octal Test Integrated Circuits**
- **Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus**
- **Functionally Equivalent to SN54/74F244 and SN54/74BCT244 in the Normal Function Mode**
- **Test Operation Synchronous to Test Access Port (TAP)**
- **Implement Optional "Test Reset" Signal on TAP by Recognizing a Double-High (10 V) on TMS Pin**
- **SCOPE™ Instruction Set**
  - **Conform to the IEEE 1149.1 Boundary Scan**
  - **Provide Data Compression of Inputs**
  - **Provide Pseudo-Random Pattern Generation from Outputs**
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  - **Output to High-Impedance-State Mode**
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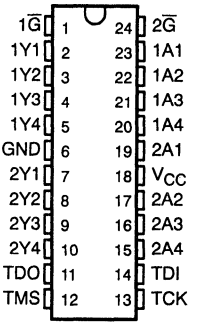
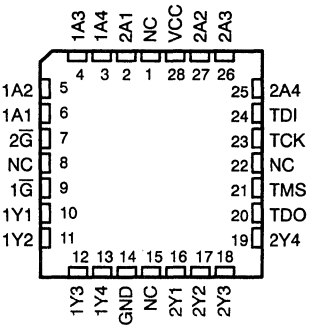
SN54BCT8244 ... JT PACKAGE
SN74BCT8244 ... DW OR NT PACKAGE
(TOP VIEW)



SN54BCT8244 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN54BCT8244 and SN74BCT8244 are members of Texas Instruments SCOPE™ testability IC family. This family of components blends test circuitry with standard logic functions to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the SN54/74F244 and SN54/74BCT244 octal buffers. In the test mode, the test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal buffers.

In the test mode, the normal operation of the SCOPE™ octal buffer is inhibited and the test circuitry is enabled to observe and control the device's I/O boundary. When enabled, the test circuitry can perform boundary scan test operations as described in the IEEE Standard 1149.1 specification. Four dedicated test pins are used to control the operation of the test circuitry: TDI (test data in), TDO (test data out), TMS (test mode select), and TCK (test clock). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

SCOPE is a trademark of Texas Instruments Incorporated.

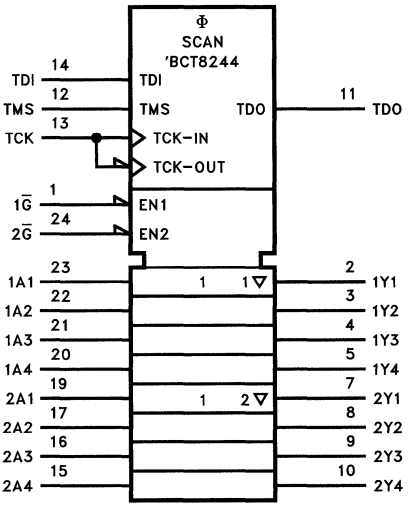
description (continued)

The SN54BCT8244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT8244 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(NORMAL MODE)

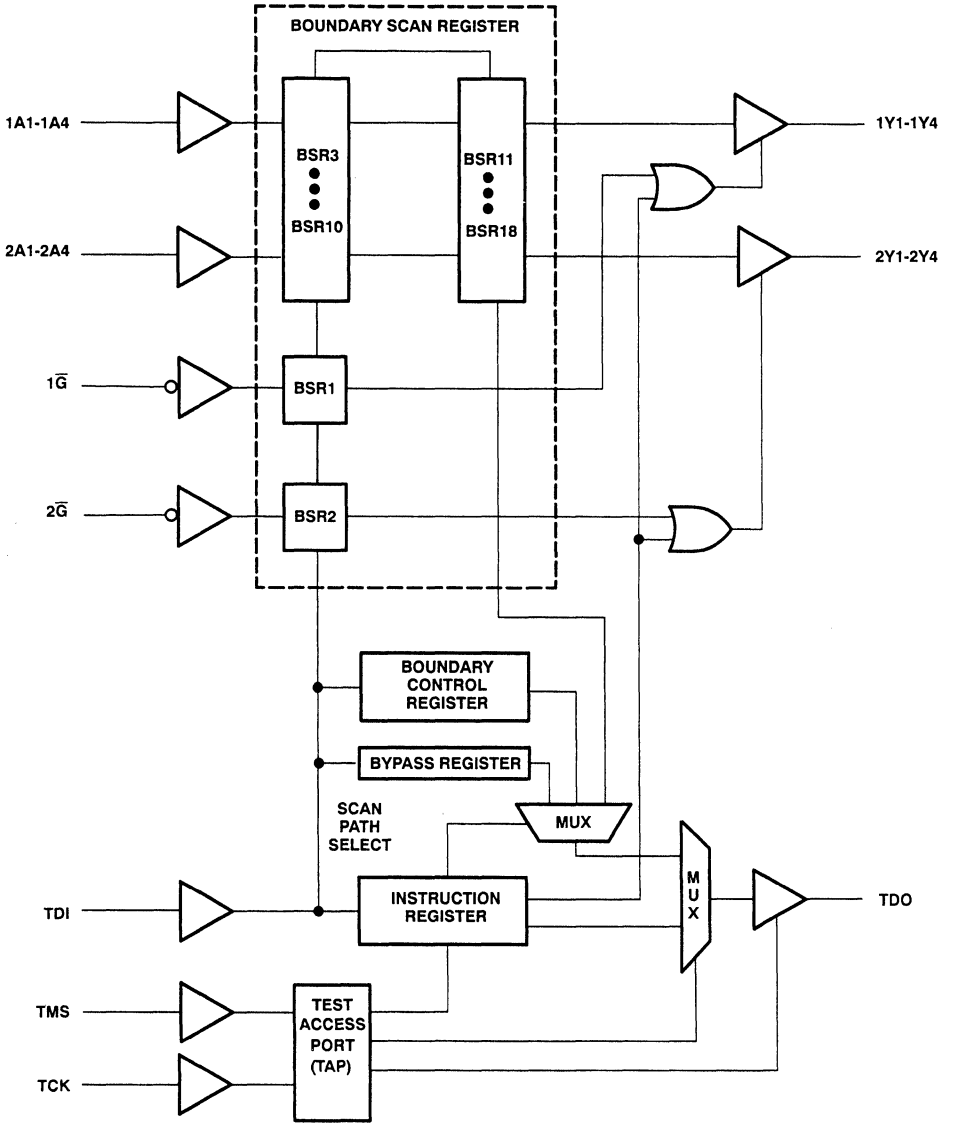
OUTPUT ENABLE $\overline{G}$	DATA INPUT A	OUTPUT Y
H	X	Z
L	L	L
L	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

functional block diagram



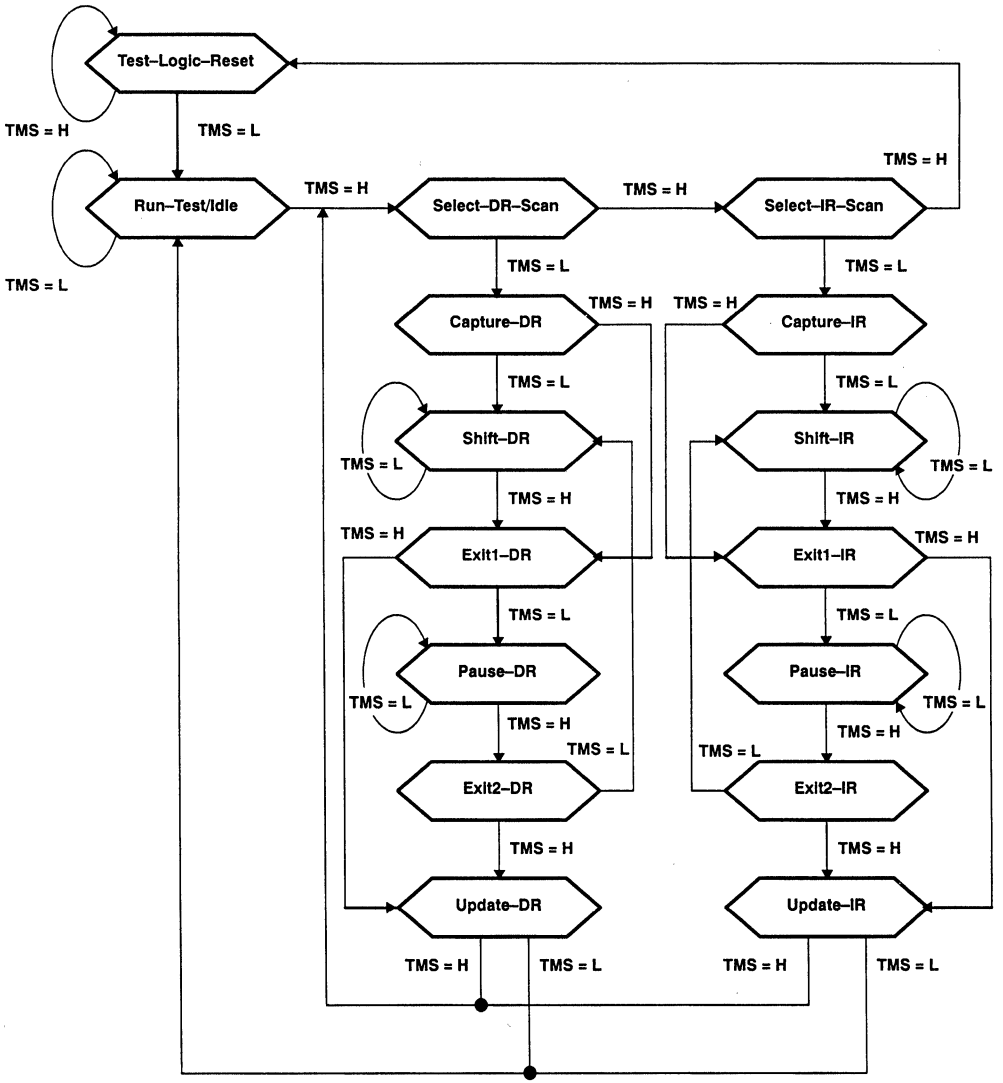


FIGURE 1. TAP STATE DIAGRAM

state diagram description

The TAP proceeds through the states of Figure 1 according to the IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow in Figure 1) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram, one to manipulate a data register and one to manipulate the instruction register. It is necessary to finish manipulating one register before accessing another.

Test-Logic-Reset
In this state, the test logic is not active and the device operates in its normal function mode. The state diagram is constructed such that the TAP will return to this state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup resistor that will force it high if left unconnected, or if a board defect causes it to be open-circuited. The device powers up in the Test-Logic-Reset state.

Run-Test/Idle
The TAP must pass through this state before executing any test operations. The test operations controlled by the boundary control register (see Table 2) are performed while in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan
No specific function is performed in these states, and the TAP will exit either of them on the next TCK cycle.

Capture-DR
The selected data register is placed in the scan path. Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK causing the TAP state to change. On the falling edge of TCK in Capture-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to a low level.

Shift-DR
While in this state, data is serially shifted through the selected data register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR).

Exit1-DR, Exit2-DR
These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-DR to Exit1-DR.

Pause-DR
The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data.

Update-DR
If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated during this, and only this, state. TDO goes to the high-impedance state on the falling edge of TCK in Update-DR.

state diagram description (continued)

Capture-IR
The instruction register is preloaded with a 10000001 pattern and placed in the scan path. On the falling edge of TCK in Capture-IR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to a logic 0.

Shift-IR
While in this state, data is serially shifted through the instruction register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR).

Exit1-IR, Exit2-IR
These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

Pause-IR
The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR
The latches shadowing the instruction register are updated with the new instruction. TDO goes to the high-impedance state on the falling edge of TCK in Update-IR.

instruction register description

Serial test information is conveyed by means of a 4-wire test bus. Commands, data, and control signals are all passed along the 4-wire bus. The function of the TAP is to extract the state control information and synchronous control signals for the bus and generate the appropriate on-chip control signals for the test structures in the device. The TAP monitors two signals from the bus, TCK and TMS. Figure 1 shows the TAP state diagram. The functional block diagram illustrates the IEEE Standard 1149.1 4-wire test bus and boundary scan architecture, and the relationship between the TAP, the test bus, and the boundary scan test elements.

Data is captured on the rising edge of TCK and outputs change after the falling edge of TCK.

As shown in the functional block diagram, the 'BCT8244 contains an eight-bit instruction register and three data registers: the 18-bit boundary scan register, the two-bit boundary control register, and the one-bit bypass register. Any register can be thought of as a serial shift register with a shadow latch on each bit. Latches may be loaded during the Update-DR and Update-IR TAP states.

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the test operation to be performed, the state of the functional inputs and outputs (whether or not the device will perform its normal function during the test operation), which of the three data registers is to be selected for inclusion in the scan path during the next data register scan operation, and from where to preload the data register during the Capture-DR state. Table 1 lists the instructions supported by the 'BCT8244. Any SCOPE™ instructions not supported default to BYPASS.

The IR is loaded during the Capture-IR state with the value 10000001. As an instruction is shfited in, this value will be shifted out via TDO and can be inspected as verification that the IR is in the scan path.

The instruction register order of scan is shown in Figure 2.

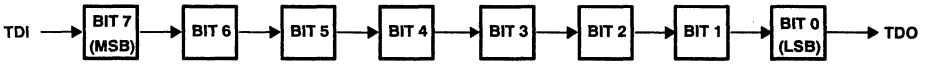


FIGURE 2. INSTRUCTION REGISTER ORDER OF SCAN

data register descriptions

boundary scan register

The boundary scan register (BSR) contains 18 bits, one for each functional input and output on the device. The BSR is used to store test data that is to be applied internally and/or externally to the device and to capture and store data that is applied to the functional inputs and outputs of the device. The origination of the value loaded in the BSR during the Capture-DR state is determined by the current instruction.

The boundary scan register order of scan is shown in Figure 3.

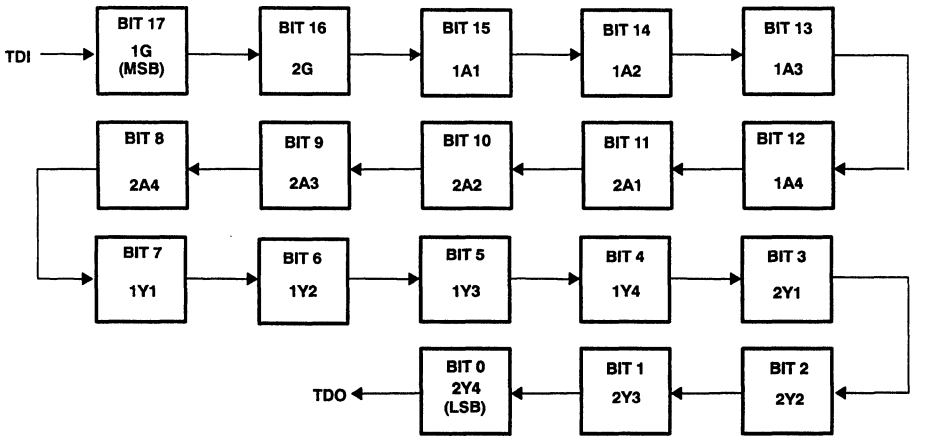


FIGURE 3. BOUNDARY SCAN REGISTER ORDER OF SCAN

boundary control register

The boundary control register (BCR) contains two bits and is used to inplement additional test operations not included in the SCOPE™ instruction set, including pseudo-random pattern generation (PRPG) and parallel signature analysis (PSA) operations. The BCR retains its current value during the Capture-DR state. The BCR resets to the PSA operation.

The boundary control register order of scan is shown in Figure 4.

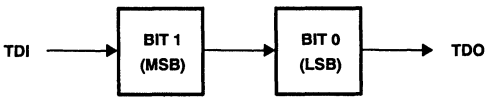


FIGURE 4. BOUNDARY CONTROL REGISTER ORDER OF SCAN

data register descriptions (continued)

bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation. The bypass register is loaded with a low level during the Capture-DR state.

The bypass register order of scan is shown in Figure 5.

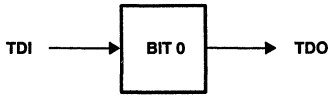


FIGURE 5. BYPASS REGISTER ORDER OF SCAN

Table 1. Instruction Register Opcodes

BINARY CODE†‡ BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
X0000000	EXTEST	Boundary Scan	Boundary Scan	Test
X0000001	BYPASS§	Bypass Scan	Bypass	Normal
X0000010	SAMPLE/PRELOAD	Sample Boundary	Boundary Scan	Normal
X0000011	INTEST	Boundary Scan	Boundary Scan	Test
X0000100	BYPASS§	Bypass Scan	Bypass	Normal
X0000101	BYPASS§	Bypass Scan	Bypass	Normal
X0000110	TRIBYP	Control Boundary to High-Impedance	Bypass	Modified Test
X0000111	SETBYP	Control Boundary to 1/0	Bypass	Test
X0001000	BYPASS§	Bypass Scan	Bypass	Normal
X0001001	RUNT	Boundary Run Test	Bypass	Test
X0001010	READBN	Boundary Read	Boundary Scan	Normal
X0001011	READBT	Boundary Read	Boundary Scan	Test
X0001100	CELLTST	Boundary Self-test	Boundary Scan	Normal
X0001101	TOPHIP	Boundary Toggle Outputs	Bypass	Test
X0001110	SCANCN	Boundary Control Register Scan	Boundary Control	Normal
X0001111	SCANCT	Boundary Control Register Scan	Boundary Control	Test
ALL OTHER	BYPASS	Bypass Scan	Bypass	Normal

† The SCOPE™ instruction set specifies even parity in the eight-bit instruction. This feature is not implemented in the 'BCT8244.
‡ X = Don't care.
§ This symbol (§) indicates that a SCOPE™ opcode exists but is not supported in the 'BCT8244.

instruction register opcode descriptions

The 'BCT8244 runs test instructions based on the value scanned into the instruction register. The test functions are defined as follows:

boundary scan
This instruction simultaneously executes the IEEE Standard 1149.1 EXTEST and INTEST instructions. The boundary scan register is selected in the scan path. Data appearing at the device inputs and outputs is captured. Data previously loaded into the boundary scan register is applied to the device inputs and through the device outputs.

bypass scan
Conforms to the IEEE Standard 1149.1 BYPASS instruction. The one-bit bypass register is selected in the scan path. A logic 0 is loaded in the bypass register. The device operates in the normal mode.

sample boundary
Conforms to the IEEE Standard 1149.1 SAMPLE/PRELOAD instruction. Data appearing at the device inputs and outputs is sampled without affecting normal device operation. The boundary scan register is selected in the scan path.

control boundary to high-impedance
The device outputs are placed in the high-impedance state. the bypass register is selected in the scan path. Device inputs remain operational and the internal logic function will be performed.

control boundary to 1/0
The data in the boundary scan register is applied to the functional inputs and through the device outputs. The bypass register is selected in the scan path.

boundary run test
A test operation is run as decoded by the boundary control register. The desired test must be preloaded in the boundary control register and the TAP placed in the Run-Test/Idle state. The four test operations decoded by the boundary control register are:

- parallel signature analysis (PSA)
  Data appearing on the functional data inputs is compressed into sixteen bits. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figure 6 shows the algorithm through which the signature is generated.
- pseudo-random pattern generation (PRPG)
  A pseudo-random pattern is generated at the functional outputs. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figure 7 shows the algorithm through which the patterns are generated. Note that a seed value of all zeroes will not produce additional patterns.
- simultaneous PSA and PRPG
  Both PSA and PRPG operations are performed as shown in Figure 8.
- sample inputs/toggle outputs
  Data appearing at the functional inputs is sampled on each TCK rising edge and the functional outputs are toggled on each TCK falling edge.

instruction register opcode descriptions (continued)

boundary read
The boundary scan register is selected in the scan path. No load operation is performed prior to shifting. This instruction is useful for inspecting data after a PSA operation.

boundary control register scan
The two-bit boundary control register is placed in the scan path. This register must be loaded prior to executing a boundary run test operation.

boundary self-test
The boundary scan register is selected in the scan path. This operation tests the logic in the boundary scan cells by loading the inverse of the current value of the cells. By loading a known value in the boundary scan register, executing CELLTST, and inspecting the resulting data through a scan operation, the integrity of the boundary scan register can be verified.

boundary toggle outputs
Functional outputs are toggled on each TCK falling edge. Data appearing on the device's functional inputs is not captured.

tap bits for PSA and PRPG

The BCR opcodes are as shown in Table 2. The use of these tap bits and the algorithms used for 8- and 16-bit PSA and PRPG operations are shown in Figures 6 through 8. The two enable inputs, $1\overline{G}$ and $2\overline{G}$, are ignored during these operations.

Table 2. Boundary Control Register Opcodes

BINARY CODE BIT 1 → BIT 0 MSB → LSB	DESCRIPTION
00	Sample inputs/toggle outputs
01	PRPG/16-bit mode
10	PSA/16-bit mode
11	Simultaneous PRPG and PSA/8-bit mode

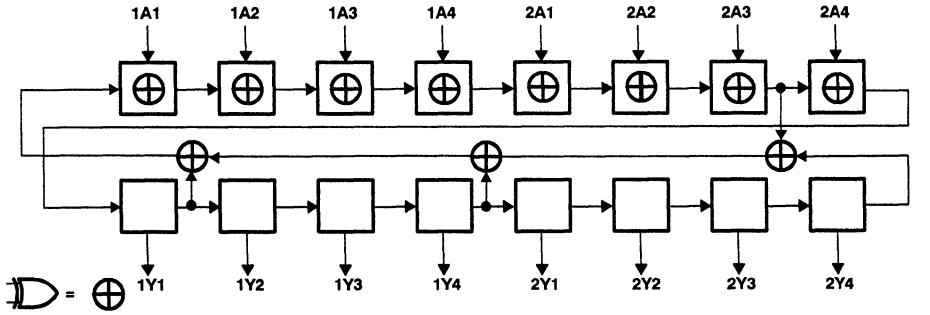


FIGURE 6. 16-BITS PSA CONFIGURATION

A PSA operation on the eight data inputs proceeds as the eight data outputs are held static.

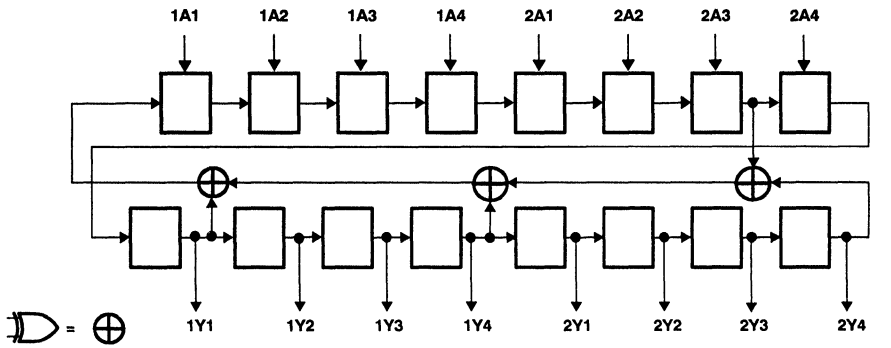


FIGURE 7. 16-BIT PRPG CONFIGURATION

A PRPG operation from the eight data outputs proceeds while the eight data inputs are ignored.

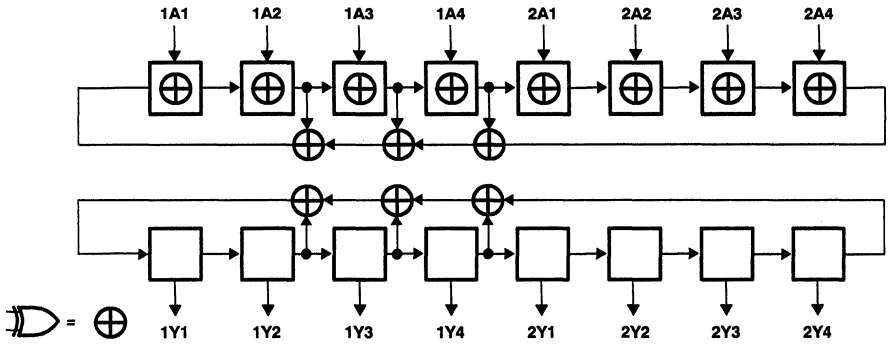


FIGURE 8. 8-BIT PSA AND PRPG CONFIGURATION

Simultaneously, an eight-bit PSA operation proceeds on the eight data inputs, while an 8-bit PRPG operation proceeds from the eight data outputs.

timing description

All test operations of the 'BCT8244 are synchronous to TCK. Data on the TDI, TMS, and functional inputs is captured on the rising edge of TCK. Data appears on the TDO and functional output pins after the falling edge of TCK.

The 'BCT8244 is advanced through its state diagram (see Figure 1) by changing the value of TMS and applying a clock pulse to TCK. A simple timing example is shown in Figure 9. In this example, the device begins in the Test-Logic-Reset state and is loaded with an instruction to select the bypass register in the scan path. The binary logic value 101 is shifted through the bypass register from TDI to TDO and the device is returned to the Test-Logic-Reset state. Table 3 explains the function of the test circuitry during each TCK cycle.

Table 3. Explanation of Timing Example

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION/COMMENT
1	Test-Logic-Reset	Recycle on reset state.
2	Run-Test/Idle	Begin advancing towards desired state.
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	IR loads with 10000001; TDO becomes active after falling edge of TCK.
6	Shift-IR	Ready to shift in instruction; TDI must be active before next clock.
7–13	Shift-IR	A BYPASS instruction (11111111) is serially loaded into the IR.
14	Exit1-IR	Note that TMS goes high prior to TCK #14. The last bit of the instruction is shifted in as the TAP advances from Shift-IR to Exit1-IR.
15	Update-IR	The IR is updated with the new instruction. TDO goes inactive (high-impedance) on the falling edge of TCK #15.
16	Select-DR-Scan	
17	Capture-DR	The bypass register loads with a logic 0; TDO becomes active.
18	Shift-DR	The bypass register is now in the scan path. Data will shift from TDI to TDO.
19–20	Shift-DR	The binary value '101' is shifted from TDI to TDO through the bypass register. Note that the last value shifted in (a logic 1) remains in the bypass register and is not shifted to the next test element.
21	Exit1-DR	
22	Update-DR	
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed.

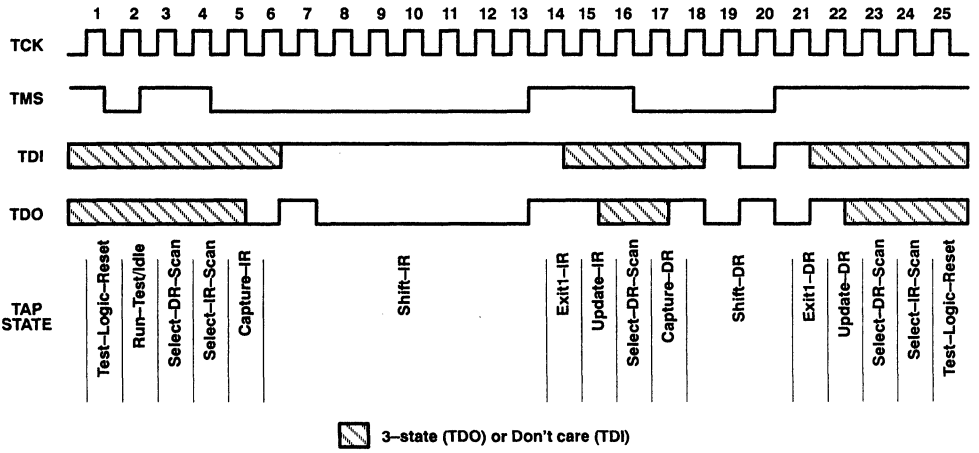


FIGURE 9. TIMING EXAMPLE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range (except TMS) ..... −0.5 V to 7 V
Input voltage range (TMS) ..... −0.5 V to 12 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54BCT8244 (TDO) ..... 40 mA
SN54BCT8244 (Any Y) ..... 96 mA
SN74BCT8244 (TDO) ..... 48 mA
SN74BCT8244 (Any Y) ..... 128 mA
Operating free-air temperature range: SN54BCT8244 ..... −55°C to 125°C
SN74BCT8244 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54BCT8244			SN74BCT8244			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IHH}	Double high-level input voltage	TMS	10		12	10		12	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	TDO			−3			−3	mA
		Any Y			−12			−15	
I_{OL}	Low-level output current	TDO			20			24	mA
		Any Y			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT8244			SN74BCT8244			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	Any Y	V_{CC} = 4.75 V	I_{OH} = −3 mA	2.7	3.4		2.7	3.4		V
		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
			I_{OH} = −12 mA	2	3.2					
	TDO		I_{OH} = −15 mA				2	3.1		
			I_{OH} = −1 mA	2.5	3.4		2.5	3.4		
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
V_{OL}	Any Y	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
			I_{OL} = 64 mA					0.42	0.55	
	TDO		I_{OL} = 20 mA		0.3	0.5				
			I_{OL} = 24 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V, V_I = 5.5 V				0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V, V_I = 2.7 V		−1		−100	−1		−100	µA
I_{IHH}	TMS	V_{CC} = 5.5 V, V_I = 10 V				1			1	mA
I_{IL}		V_{CC} = 5.5 V, V_I = 0.5 V				−200			−200	µA
I_{OZH}	Any Y	V_{CC} = 5.5 V, V_O = 2.7 V				50			50	µA
	TDO	V_{CC} = 5.5 V, V_O = 2.7 V		−1		−100	−1		−100	
I_{OZL}	Any Y	V_{CC} = 5.5 V, V_O = 0.5 V				−50			−50	µA
	TDO	V_{CC} = 5.5 V, V_O = 0.5 V				−200			−200	
I_{OS}‡		V_{CC} = 5.5 V, V_O = 0		−100		−225	−100		−225	mA
I_{CC}		V_{CC} = 5.5 V, Outputs open	Outputs high		3.5	7.5		3.5	7.5	mA
			Outputs low		31	52		31	52	
			Outputs disabled		1.5	3.5		1.5	3.5	
C_i		V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			10			10		pF
C_o		V_{CC} = 5 V, V_O = 2.5 V or 0.5 V			18			18		pF

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§				UNIT
			'BCT8244		'54BCT8244		'74BCT8244		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	20	0	20	0	20	MHz
t_w	Pulse duration	TCK high or low	25		25		25		ns
		TMS reset high	50		50		50		
t_{su}	Setup time	TMS before TCK ↑	15		15		15		ns
		TDI before TCK ↑	6		6		6		
		Any A before TCK ↑	6		6		6		
		Any $\overline{G}$ before TCK ↑	6		6		6		
t_h	Hold time	TMS after TCK ↑	0		0		0		ns
		TDI after TCK ↑	4.5		4.5		4.5		
		Any A after TCK ↑	4.5		4.5		4.5		
		Any $\overline{G}$ after TCK ↑	4.5		4.5		4.5		
t_d	Delay time, power-up to TCK ↑		100		100		100		ns

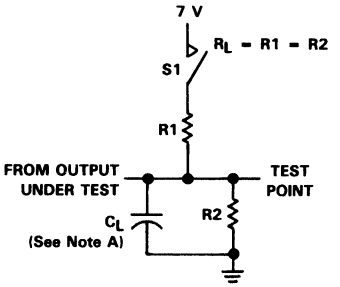
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT8244			'54BCT8244		'74BCT8244		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		20			20		20		MHz
t_{PLH}	Any A	Y	1.6	5.6	7.6	1.6	10.3	1.6	8.8	ns
t_{PHL}			1.7	6	8.2	1.7	10.7	1.7	9.6	
t_{PLH}	TCK ↓	Y	6.5	13.4	17	6.5	25.2	6.5	21.4	ns
t_{PHL}			5.7	13	16.3	5.7	23.7	5.7	20.5	
t_{PLH}	TCK ↓	TDO	3	11.1	14.3	3	21	3	17.9	ns
t_{PHL}			3	10.8	13.9	3	19.8	3	17.2	
t_{PLH}	TCK ↑	Y	7.5	17.3	22	7.5	33.3	7.5	27.5	ns
t_{PHL}			7.5	18.1	22.8	7.5	34.2	7.5	28.3	
t_{PZH}	Any $\overline{G}$	Y	2.3	6.6	8.7	2.3	11.6	2.3	10.4	ns
t_{PZL}			2.6	7.9	10	2.6	13.2	2.6	12	
t_{PZH}	TCK ↓	Y	7.2	13.8	17.5	7.2	25.7	7.2	22.3	ns
t_{PZL}			7.3	15.1	18.9	7.3	27.3	7.3	23.8	
t_{PZH}	TCK ↓	TDO	3.4	7.8	10.1	3.4	13.9	3.4	12.3	ns
t_{PZL}			4.4	9.4	11.8	4.4	15.3	4.4	14	
t_{PHZ}	Any $\overline{G}$	Y	1.7	6.2	8.2	1.7	10.7	1.7	9.9	ns
t_{PLZ}			1	6	8.1	1	11	1	9.6	
t_{PHZ}	TCK ↓	Y	4	11.5	14.8	4	21.9	4	19	ns
t_{PLZ}			5.2	12.1	15.5	5.2	23.4	5.2	19.9	
t_{PHZ}	TCK ↓	TDO	4	8.6	11	4	15.3	4	14	ns
t_{PLZ}			3.9	8	10.5	3.9	14.7	3.9	12.9	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

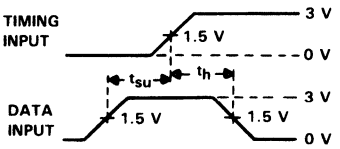
PARAMETER MEASUREMENT INFORMATION



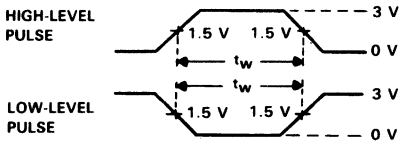
LOAD CIRCUIT

SWITCH POSITION TABLE

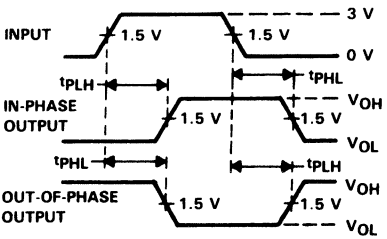
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



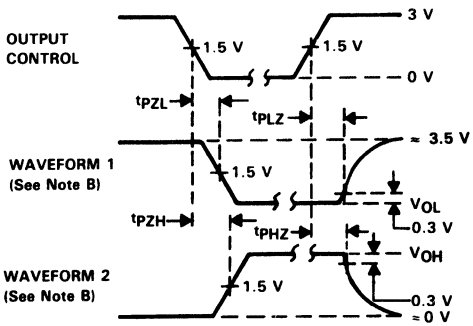
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

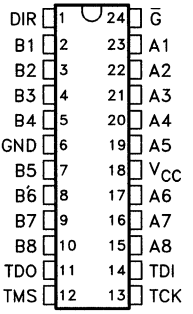
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns. Pulse polarity can be either a high-to-low-to-high or low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 10. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

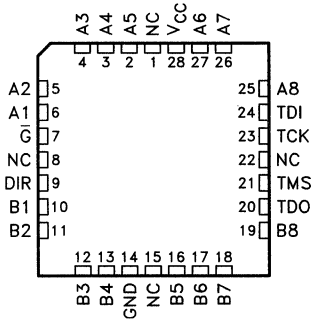
TI0038—D3514, MAY 1990

- **Members of Texas Instruments SCOPE™ Family of Testability Products**
- **Octal Test Integrated Circuits**
- **Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus Protocol**
- **Functionally Equivalent to SN54/74F245 and SN54/74BCT245 in the Normal Function Mode**
- **Test Operation Synchronous to Test Access Port (TAP)**
- **Implement Optional "Test Reset" Signal on TAP by Recognizing a Double-High (10 V) on TMS Pin**
- **SCOPE™ Instruction Set**
  - **Conform to the IEEE 1149.1 Boundary Scan**
  - **Provide Data Compression of Inputs**
  - **Provide Pseudo-Random Pattern Generation from Outputs**
  - **Sample Input/Toggle Output Mode**
  - **Output to High-Impedance-State Mode**
- **Fabricated Using TI's State-of-the-Art BiCMOS Technology**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT8245 ... JT PACKAGE
SN74BCT8245 ... DW OR NT PACKAGE
(TOP VIEW)



SN54BCT8245 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN54BCT8245 and SN74BCT8245 are members of Texas Instruments SCOPE™ testability IC family. This family of components blends test circuitry with standard logic functions to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the SN54/74F245 and SN54/74BCT245 octal bus transceivers. In the test mode, the test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal bus transceivers.

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description (continued)

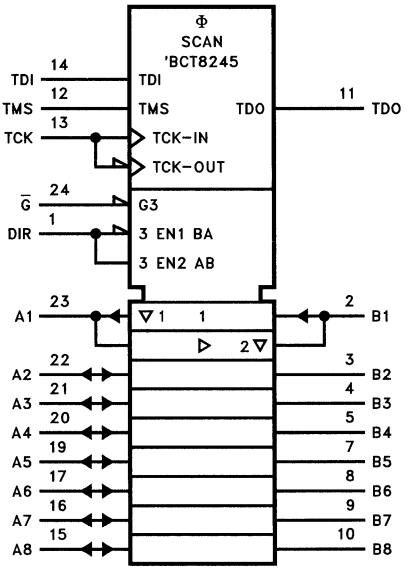
In the test mode, the normal operation of the SCOPE™ octal bus transceiver is inhibited and the test circuitry is enabled to observe and control the device's I/O boundary. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in the IEEE Standard 1149.1 specification. Four dedicated test pins are used to control the operation of the test circuitry: TDI (test data in), TDO (test data out), TMS (test mode select), and TCK (test clock). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54BCT8245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT8245 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(Normal Mode)

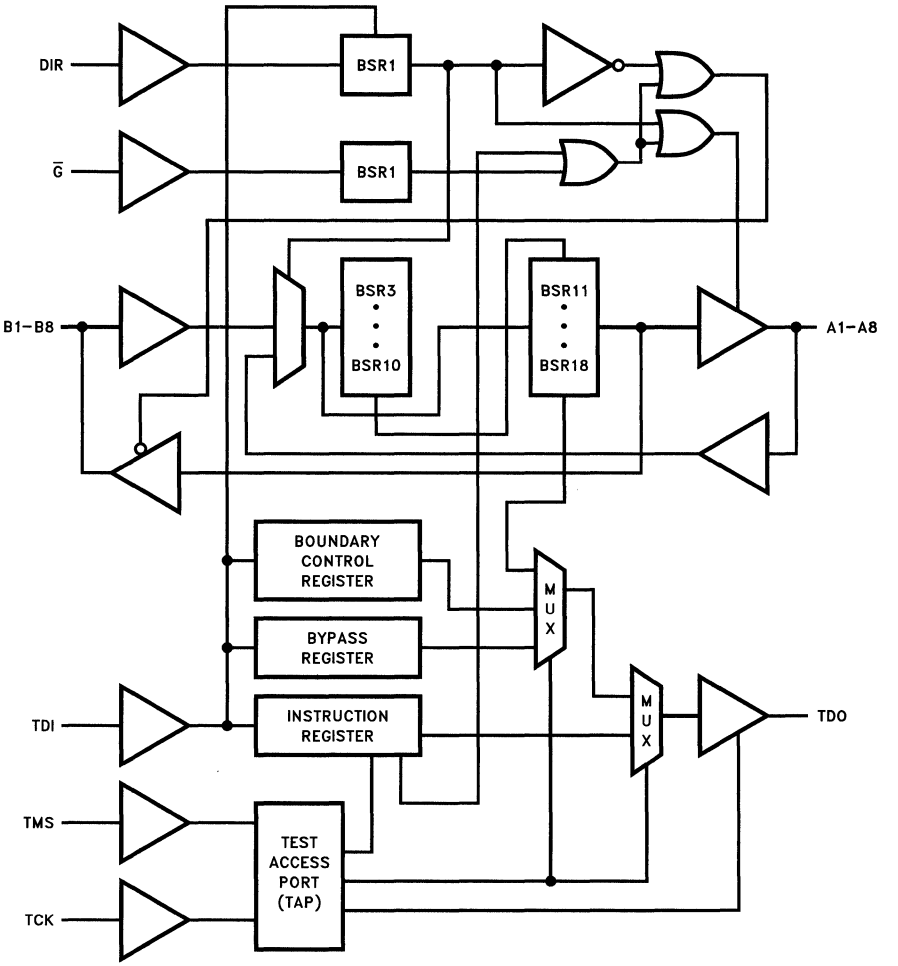
ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

functional block diagram



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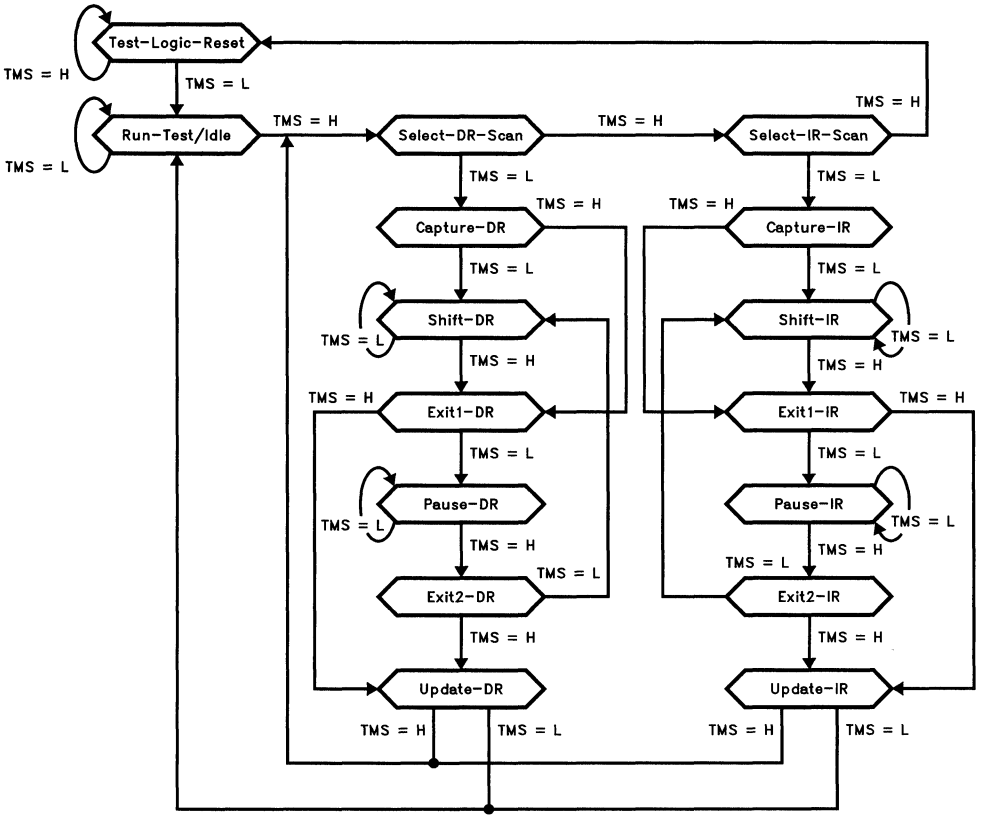


FIGURE 1. TAP STATE DIAGRAM

state diagram description

The TAP proceeds through the states shown in Figure 1 according to the IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow in Figure 1) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram, one to manipulate a data register and one to manipulate the instruction register. It is necessary to finish manipulating one register before accessing another.

Test-Logic-Reset
In this state, the test logic is not active and the device operates in its normal function mode. The state diagram is constructed such that the TAP will return to this state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup resistor that will force it high if left unconnected, or if a board defect causes it to be open-circuited. The device powers up in the Test-Logic-Reset state.

Run-Test/Idle
The TAP must pass through this state before executing any test operations. The test operations controlled by the boundary control register (see Table 2) are performed while in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan
No specific function is performed in these states, and the TAP will exit either of them on the next TCK cycle.

Capture-DR
The selected data register is placed in the scan path. Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK causing the TAP state to change. On the falling edge of TCK in Capture-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to a low level.

Shift-DR
While in this state, data is serially shifted through the selected data register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR).

Exit1-DR, Exit2-DR
These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-DR to Exit1-DR.

Pause-DR
The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data.

Update-DR
If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated during this, and only this, state. TDO goes to the high-impedance state on the falling edge of TCK in Update-DR.

state diagram description (continued)

Capture-IR
The instruction register is preloaded with a 10000001 pattern and placed in the scan path. On the falling edge of TCK in Capture-IR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to a low level.

Shift-IR
While in this state, data is serially shifted through the instruction register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR).

Exit1-IR, Exit2-IR
These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-IR to Exit1-IR.

Pause-IR
The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR
The latches shadowing the instruction register are updated with the new instruction. TDO goes to the high-impedance state on the falling edge of TCK in Update-IR.

instruction register description

Serial test information is conveyed by means of a 4-wire test bus. Commands, data, and control signals are all passed along the 4-wire bus. The function of the TAP is to extract the state control information and synchronous control signals for the bus and generate the appropriate on-chip control signals for the test structures in the device. The TAP monitors two signals from the bus, TCK and TMS. Figure 1 shows the TAP state diagram. The functional block diagram illustrates the IEEE Standard 1149.1 4-wire test bus and boundary scan architecture, and the relationship between the TAP, the test bus, and the boundary scan test elements.

Data is captured on the rising edge of TCK and outputs change after the falling edge of TCK.

As shown in the functional block diagram, the 'BCT8245 contains an eight-bit instruction register and three data registers: the 18-bit boundary scan register, the two-bit boundary control register, and the one-bit bypass register. Any register can be thought of as a serial shift register with a shadow latch on each bit. Latches may be loaded during the Update-DR and Update-IR TAP states.

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the test operation to be performed, the state of the functional inputs and outputs (whether or not the device will perform its normal function during the test operation), which of the three data registers is to be selected for inclusion in the scan path during the next data register scan operation, and the source of the data preloaded in the data register during the Capture-DR state. Table 1 lists the instructions supported by the 'BCT8245. Any SCOPE™ instructioins not supported default to BYPASS.

The IR is loaded during the Capture-IR state with the value 10000001. As an instruction is shifted in, this value will be shifted out via TDO and can be inspected as verification that the IR is in the scan path.

The instruction register order of scan is shown in Figure 2.

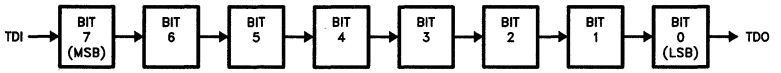


FIGURE 2. INSTRUCTION REGISTER ORDER OF SCAN

data register descriptions

boundary scan register

The boundary scan register (BSR) contains 18 bits, one for each functional input and output on the device. The BSR is used to store test data that is to be applied internally and/or externally to the device and to capture and store data that is applied to the functional inputs and outputs of the device. The origination of the value loaded in the BSR during the Capture-DR state is determined by the current instruction.

The boundary scan register order of scan is shown in Figures 3 and 4. Note that the order of scan depends on the level of the DIR signal, which determines the direction of data flow (A to B or B to A).

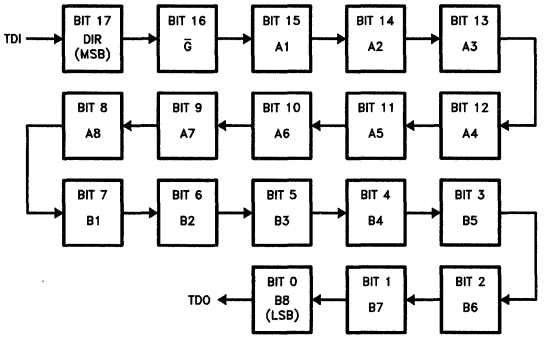


FIGURE 3. BOUNDARY SCAN REGISTER ORDER OF SCAN (A TO B MODE)

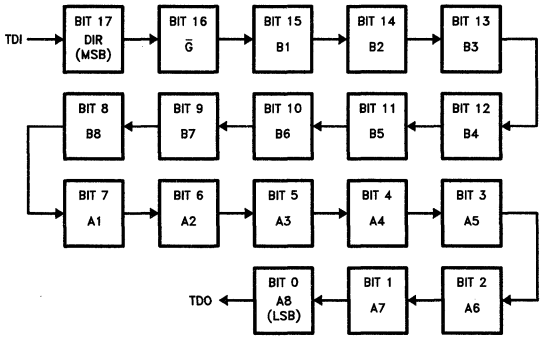


FIGURE 4. BOUNDARY SCAN REGISTER ORDER OF SCAN (B TO A MODE)

data register descriptions (continued)

boundary control register

The boundary control register (BCR) contains two bits and is used to inplement additional test operations not included in the SCOPE™ instruction set, including pseudo-random pattern generation (PRPG) and parallel signature analysis (PSA) operations. The BCR retains its current value during the Capture-DR state. The BCR resets to the PSA operation.

The boundary control register order of scan is shown in Figure 5.

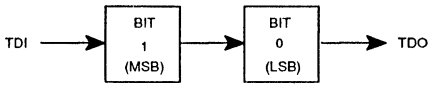


FIGURE 5. BOUNDARY CONTROL REGISTER ORDER OF SCAN

bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation. The bypass register is loaded with a logic 0 during the Capture-DR state.

The bypass register order of scan is shown in Figure 6.

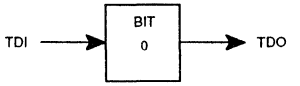


FIGURE 6. BYPASS REGISTER ORDER OF SCAN

TABLE 1. INSTRUCTION REGISTER OPCODES

BINARY CODE†‡ BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE§	DESCRIPTION	SELECTED DATA REGISTER	MODE
X0000000	EXTEST	Boundary Scan	Boundary Scan	Test
X0000001	BYPASS*	Bypass Scan	Bypass	Normal
X0000010	SAMPLE/PRELOAD	Sample Boundary	Boundary Scan	Normal
X0000011	INTEST	Boundary Scan	Boundary Scan	Test
X0000100	BYPASS*	Bypass Scan	Bypass	Normal
X0000101	BYPASS*	Bypass Scan	Bypass	Normal
X0000110	TRIBYP	Control Boundary to High-Impedance	Bypass	Modified Test
X0000111	SETBYP	Control Boundary to 1/0	Bypass	Test
X0001000	BYPASS*	Bypass Scan	Bypass	Normal
X0001001	RUNT	Boundary Run Test	Bypass	Test
X0001010	READBN	Boundary Read	Boundary Scan	Normal
X0001011	READBT	Boundary Read	Boundary Scan	Test
X0001100	CELLTST	Boundary Self-test	Boundary Scan	Normal
X0001101	TOPHIP	Boundary Toggle Outputs	Bypass	Test
X0001110	SCANCN	Boundary Control Register Scan	Boundary Control	Normal
X0001111	SCANCT	Boundary Control Register Scan	Boundary Control	Test
ALL OTHER	BYPASS	Bypass Scan	Bypass	Normal

† The SCOPE™ instruction set specifies even parity in the eight-bit instruction. This feature is not implemented in the 'BCT8245.
‡ X = Don't care.
§ A SCOPE™ opcode exists but is not supported in the 'BCT8245.

instruction register opcode descriptions

The 'BCT8245 runs test instructions based on the value scanned into the instruction register. The test functions are defined as follows:

boundary scan
This instruction simultaneously executes the IEEE Standard 1149.1 EXTEST and INTEST instructions. The boundary scan register is selected in the scan path. Data appearing at the device inputs and outputs is captured. Data previously loaded into the boundary scan register is applied to the device inputs and through the device outputs.

bypass scan
Conforms to the IEEE Standard 1149.1 BYPASS instruction. The one-bit bypass register is selected in the scan path. A logic 0 is loaded in the bypass register. The device operates in the normal mode.

sample boundary
Conforms to the IEEE Standard 1149.1 SAMPLE/PRELOAD instruction. Data appearing at the device inputs and outputs is sampled without affecting normal device operation. The boundary scan register is selected in the scan path.

control boundary to high-impedance
The device outputs are placed in the high-impedance state. The bypass register is selected in the scan path. Device inputs remain operational and the internal logic function will be performed.

control boundary to 1/0
The data in the boundary scan register is applied to the functional inputs and through the device outputs. The bypass register is selected in the scan path.

instruction register opcode descriptions (continued)

boundary run test
A test operation is run as decoded by the boundary control register. The desired test must be preloaded in the boundary control register and the TAP placed in the Run-Test/Idle state. The four test operations decoded by the boundary control register are:

— parallel signature analysis (PSA)
Data appearing on the functional data inputs is compressed into sixteen bits. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figures 7 and 8 show the algorithm through which the signature is generated.

— pseudo-random pattern generation (PRPG)
A pseudo-random pattern is generated at the functional outputs. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figures 9 and 10 show the algorithm through which the patterns are generated. Note that a seed value of all zeroes will not produce additional patterns.

— simultaneous PSA and PRPG
Both PSA and PRPG operations are performed as shown in Figures 11 and 12.

— sample inputs/toggle outputs
Data appearing at the functional inputs is sampled on each TCK rising edge and the functional outputs are toggled on each TCK falling edge.

boundary read
The boundary scan register is selected in the scan path. No load operation is performed prior to shifting. This instruction is useful for inspecting data after a PSA operation.

boundary control register scan
The two-bit boundary control register is placed in the scan path. This register must be loaded prior to executing a boundary run test operation.

boundary self-test
The boundary scan register is selected in the scan path. This operation tests the logic in the boundary scan cells by loading the inverse of the current value of the cells. By loading a known value in the boundary scan register, executing CELLTST, and inspecting the resulting data through a scan operation, the integrity of the boundary scan register can be verified.

boundary toggle outputs
Functional outputs are toggled on each TCK falling edge. Data appearing on the device's functional inputs is not captured.

tap bits for PSA and PRPG

The BCR opcodes are shown in Table 2. The use of these tap bits and the algorithms used for 8- and 16-bit PSA and PRPG operations are shown in Figures 7 through 12. The enable input $\overline{G}$ is ignored during PSA and PRPG operations, and DIR is not used except to determine the direction of data flow.

TABLE 2. BOUNDARY CONTROL REGISTER OPCODES

BINARY CODE BIT 1 → BIT 0 MSB → LSB	DESCRIPTION
00	Sample inputs/toggle outputs
01	PRPG/16-bit mode
10	PSA/16-bit mode
11	Simultaneous PRPG and PSA/8-bit mode

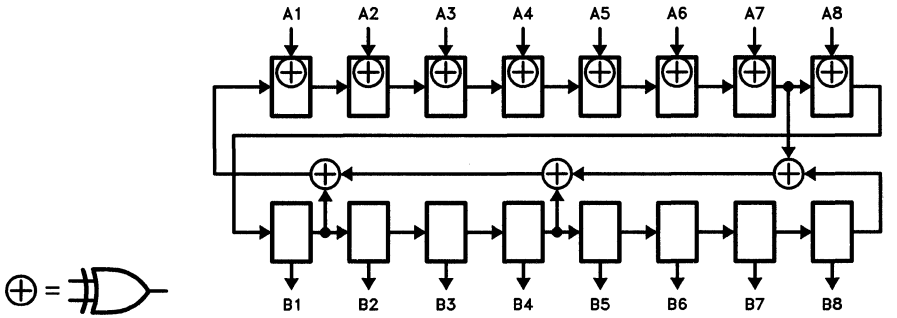


FIGURE 7. 16-BIT PSA CONFIGURATION (A TO B MODE)

A PSA operation on the 8 data inputs proceeds as the 8 data outputs are held static.

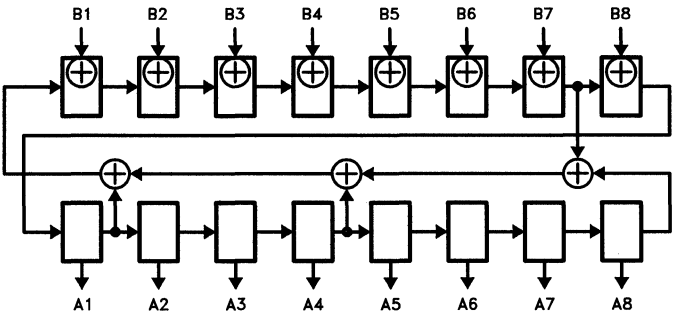


FIGURE 8. 16-BIT PSA CONFIGURATION (B TO A MODE)

A PSA operation on the 8 data inputs proceeds as the 8 data outputs are held static.

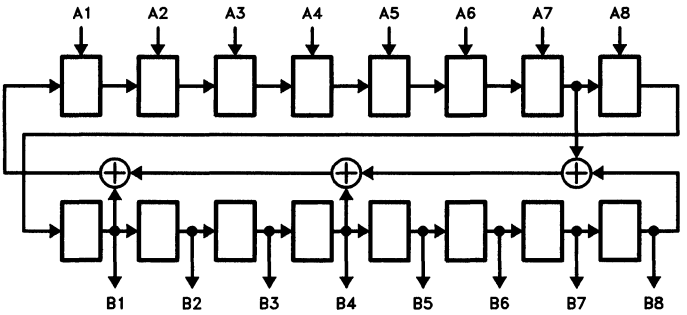


FIGURE 9. 16-BIT PRPG CONFIGURATION (A TO B MODE)

A PRPG operation from the 8 data outputs proceeds while the inputs are ignored.

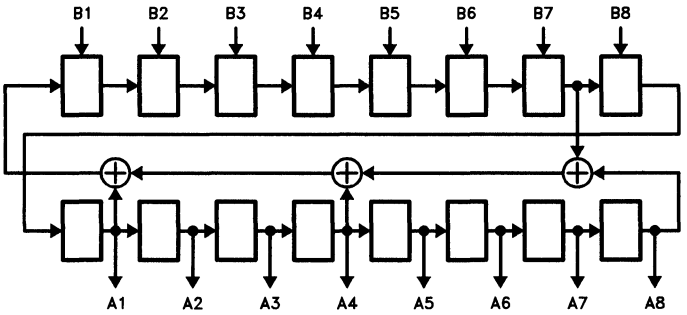


FIGURE 10. 16-BIT PRPG CONFIGURATION (B TO A MODE)

A PRPG operation from the 8 data outputs proceeds while the inputs are ignored.

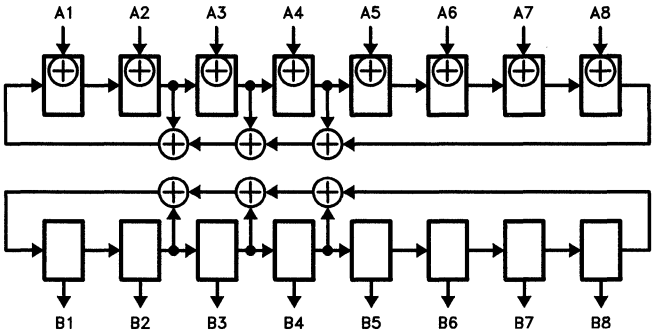


FIGURE 11. 8-BIT PSA AND PRPG CONFIGURATION (A TO B MODE)

Simultaneously, an 8-bit PSA operation proceeds on the 8 data inputs, while an 8-bit PRPG operation proceeds from the 8 data outputs.

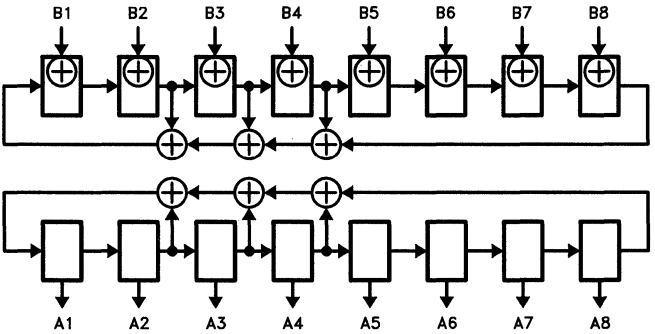


FIGURE 12. 8-BIT PSA AND PRPG CONFIGURATION (B TO A MODE)

Simultaneously, an 8-bit PSA operation proceeds on the 8 data inputs, while an 8-bit PRPG operation proceeds from the 8 data outputs.

timing description

All test operations of the 'BCT8245 are synchronous to TCK. Data on the TDI, TMS, and functional inputs is captured on the rising edge of TCK. Data appears on the TDO and functional output pins on the falling edge of TCK.

The 'BCT8245 is advanced through its state diagram (see Figure 1) by changing the value of TMS and applying a clock pulse to TCK. A simple timing example is shown in Figure 13. In this example, the device begins in the Test-Logic-Reset state and is loaded with an instruction to select the bypass register in the scan path. The binary logic value 101 is shifted through the bypass register from TDI to TDO, and the device is returned to the Test-Logic-Reset state. Table 3 explains the function of the test circuitry during each TCK cycle.

TABLE 3. EXPLANATION OF TIMING EXAMPLE

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION/COMMENT
1	Test-Logic-Reset	Recycle on reset state
2	Run-Test/Idle	Begin advancing towards desired state
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	IR loads with 10000001; TDO becomes active after falling edge of TCK.
6	Shift-IR	Ready to shift in instruction; TDI must be active before next clock.
7–13	Shift-IR	A BYPASS instruction (11111111) is serially loaded into the IR.
14	Exit1-IR	Note that TMS goes high prior to TCK #14. The last bit of the instruction is shifted in as the TAP advances from Shift-IR to Exit1-IR.
15	Update-IR	The IR is updated with the new instruction. TDO goes inactive (high-impedance) on the falling edge of TCK #15.
16	Select-DR-Scan	
17	Capture-DR	The bypass register loads with a logic 0; TDO becomes active.
18	Shift-DR	The bypass register is now in the scan path. Data will shift from TDI to TDO.
19–20	Shift-DR	The binary value '101' is shifted from TDI to TDO through the bypass register. Note that the last value shifted in (a logic 1) remains in the bypass register and is not shifted to the next test element.
21	Exit1-DR	
22	Update-DR	
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed

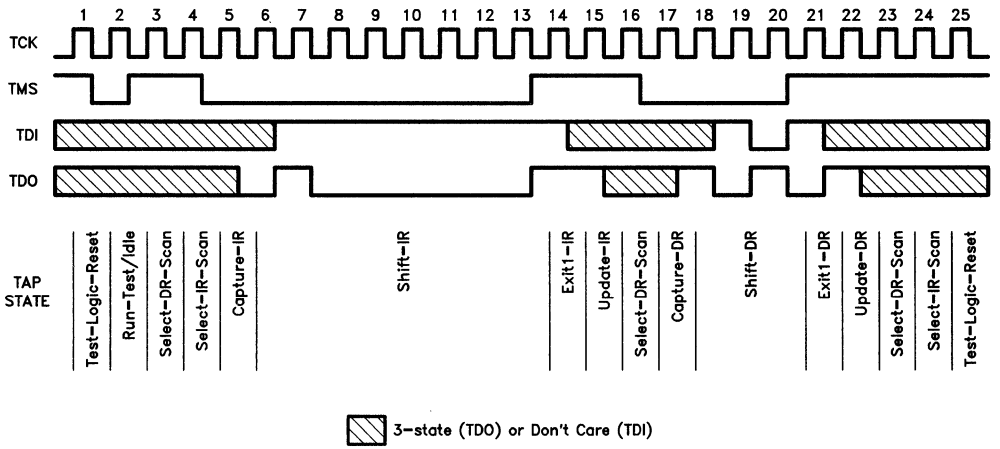


FIGURE 13. TIMING EXAMPLE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, (I/O ports) ..... −0.5 V to 5.5 V
Input voltage range (excluding I/O ports) ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54BCT8245 (Any A, TDO) ..... 40 mA
SN54BCT8245 (Any B) ..... 96 mA
SN74BCT8245 (Any A, TDO) ..... 48 mA
SN74BCT8245 (Any B) ..... 128 mA
Operating free-air temperature range: SN54BCT8245 ..... −55°C to 125°C
SN74BCT8245 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54BCT8245			SN74BCT8245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IHH}	Double high-level input voltage	TMS	10		12	10		12	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	Any A, TDO			−3			−3	mA
		Any B			−12			−15	
I_{OL}	Low-level output current	Any A, TDO			20			24	mA
		Any B			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT8245			SN74BCT8245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	Any A, TDO	V_{CC} = 4.75 V	I_{OH} = −1 mA	2.7	3.4		2.7	3.4		V
		V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	Any B	V_{CC} = 4.75 V	I_{OH} = −3 mA	2.7	3.4		2.7	3.4		
		V_{CC} = 4.75 V	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
V_{OL}	Any A, TDO	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
	Any B	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I	Except A or B	V_{CC} = 5.5 V, V_I = 5.5 V				0.1			0.1	mA
	Any A or B	V_{CC} = 5.5 V, V_I = 5.5 V				0.25			0.25	
I_{IH}‡		V_{CC} = 5.5 V, V_I = 2.7 V		−1	−35	−100	−1	−35	−100	μA
I_{IHH}	TMS	V_{CC} = 5.5 V, V_I = 10 V				1			1	mA
I_{IL}‡		V_{CC} = 5.5 V, V_I = 0.5 V			−70	−200		−70	−200	μA
I_{OZH}	TDO	V_{CC} = 5.5 V, V_O = 2.7 V		−1	−35	−100	−1	−35	−100	μA
I_{OZL}	TDO	V_{CC} = 5.5 V, V_O = 0.5 V			−70	−200		−70	−200	μA
I_{OS}§		V_{CC} = 5.5 V, V_O = 0		−100		−225	−100		−225	mA
I_{CC}*		V_{CC} = 5.5 V, Outputs Open	Outputs high		3.6	7.5		3.6	7.5	mA
			Outputs low		35	52		35	52	
			Outputs disabled		1.5	3.5		1.5	3.5	
C_i		V_{CC} = 5.5 V, V_I = 0.5 V			8			8		pF
C_{io}		V_{CC} = 5.5 V, V_O = 0.5 V			14			14		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
* I_{CCH} and I_{CCL} are measured in the A to B mode.

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'BCT8245		'54BCT8245		'74BCT8245		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	20	0	20	0	20	MHz
t_w	Pulse duration	TCK high or low	25		25		25		ns
		TMS reset high	50		50		50		
t_{su}	Setup time	TMS before TCK ↑	12		12		12		ns
		TDI before TCK ↑	6		6		6		
		Any A or B before TCK ↑	6		6		6		
		DIR or $\overline{G}$ before TCK ↑	6		6		6		
t_h	Hold time	TMS after TCK ↑	0		0		0		ns
		TDI after TCK ↑	4.5		4.5		4.5		
		Any A or B after TCK ↑	4.5		4.5		4.5		
		DIR or $\overline{G}$ after TCK ↑	4.5		4.5		4.5		
t_d	Delay time	Power-up to TCK ↑	100		100		100		ns

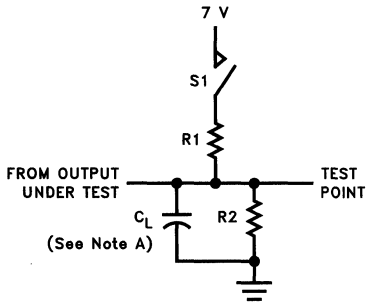
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 14)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT8245			'54BCT8245		'74BCT8245		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		20			20		20		MHz
t_{PLH}	A or B	B or A	1.6	5.5	7.6	1.6	9.6	1.6	8.7	ns
t_{PHL}	A or B	B or A	1.7	5.7	8	1.7	9.9	1.7	9.4	ns
t_{PLH}	TCK ↓	A or B	3.9	10.9	15.7	3.9	21.5	3.9	19.8	ns
t_{PHL}	TCK ↓	A or B	3.9	10.8	15.3	3.9	21.5	3.9	19.5	ns
t_{PLH}	TCK ↓	TDO	3.2	8.5	12.3	3.2	16.8	3.2	15.4	ns
t_{PHL}	TCK ↓	TDO	3.2	8.3	12	3.2	16.2	3.2	15	ns
t_{PLH}	TCK ↑	A or B	6.2	13.9	21	6.2	29	6.2	25	ns
t_{PHL}	TCK ↑	A or B	6.6	15	22	6.6	29	6.6	26	ns
t_{PZH}	$\overline{G}$	A or B	2.3	6.3	8.7	2.3	11.1	2.3	10.6	ns
t_{PZH}	TCK ↓	A or B	4.7	11.7	16.7	4.7	23.1	4.7	21.1	ns
t_{PZH}	TCK ↓	TDO	2.4	6.2	9	2.4	11.3	2.4	10.8	ns
t_{PZL}	$\overline{G}$	A or B	2.6	8.2	11.7	2.6	14.3	2.6	13.8	ns
t_{PZL}	TCK ↓	A or B	5.5	13.6	19.7	5.5	26.8	5.5	24.8	ns
t_{PZL}	TCK ↓	TDO	3.2	7.6	10.6	3.2	13.2	3.2	12.6	ns
t_{PHZ}	$\overline{G}$	A or B	1.7	6	8.4	1.7	10.2	1.7	9.6	ns
t_{PHZ}	TCK ↓	A or B	3.4	9.1	13.2	3.4	18.7	3.4	17.3	ns
t_{PHZ}	TCK ↓	TDO	2.6	7.1	10.2	2.6	13	2.6	12.8	ns
t_{PLZ}	$\overline{G}$	A or B	1.5	5.6	8	1.5	10.5	1.5	9.7	ns
t_{PLZ}	TCK ↓	A or B	3.6	10	14.6	3.6	19.5	3.6	17.8	ns
t_{PLZ}	TCK ↓	TDO	2.2	5.9	8.7	2.2	12.7	2.2	11.6	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

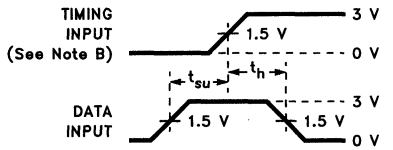
PARAMETER MEASUREMENT INFORMATION



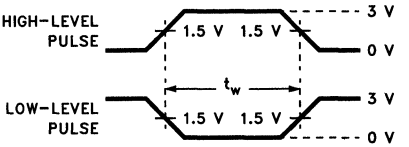
LOAD CIRCUIT

SWITCH POSITION TABLE

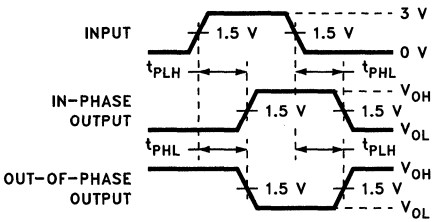
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



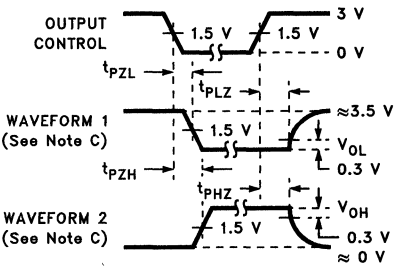
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

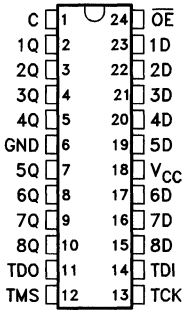
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 14. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

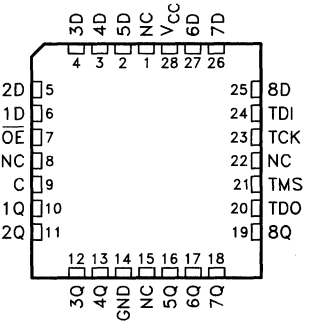
TI0222—D8373 JUNE 1990

- **Members of Texas Instruments SCOPE™ Family of Testability Products**
- **Octal Test Integrated Circuits**
- **Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus**
- **Functionally Equivalent to SN54/74F373 and SN54/74BCT373 in the Normal Function Mode**
- **Test Operation Synchronous to Test Access Port (TAP)**
- **Implement Optional "Test Reset" Signal on TAP by Recognizing a Double-High on TMS Pin**
- **SCOPE™ Instruction Set**
  - **Conform to the IEEE 1149.1 Boundary Scan**
  - **Provide Data Compression of Inputs**
  - **Provide Pseudo-Random Pattern Generation From Outputs**
  - **Sample Input/Toggle Output Mode**
  - **Output to High-Impedance State Mode**
- **Fabricated Using TI's State-of-the-Art BiCMOS Technology**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT8373 ... JT PACKAGE
SN74BCT8373 ... DW OR NT PACKAGE
(TOP VIEW)



SN54BCT8373 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN54BCT8373 and SN74BCT8373 are members of Texas Instruments SCOPE™ testability IC family. This family of components blends test circuitry with standard logic functions to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode these devices are functionally equivalent to the SN54/74F373 and SN54/74BCT373 octal D-type latches. In the test mode, the test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self-test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ octal latches.

SCOPE is a trademark of Texas Instruments Incorporated.

description (continued)

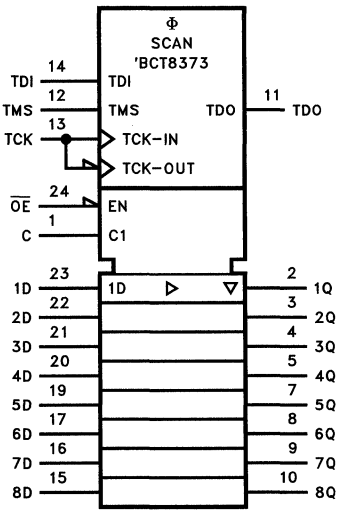
In the test mode the normal operation of the SCOPE™ octal latch is inhibited and the test circuitry is enabled to observe and control the device's I/O boundary. When enabled, the test circuitry can perform boundary scan test operations as described in the IEEE Standard 1149.1 specification. Four dedicated test pins are used to control the operation of the test circuitry: TDI (test data in), TDO (test data out), TMS (test mode select), and TCK (test clock). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54BCT8373 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT8373 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH LATCH)

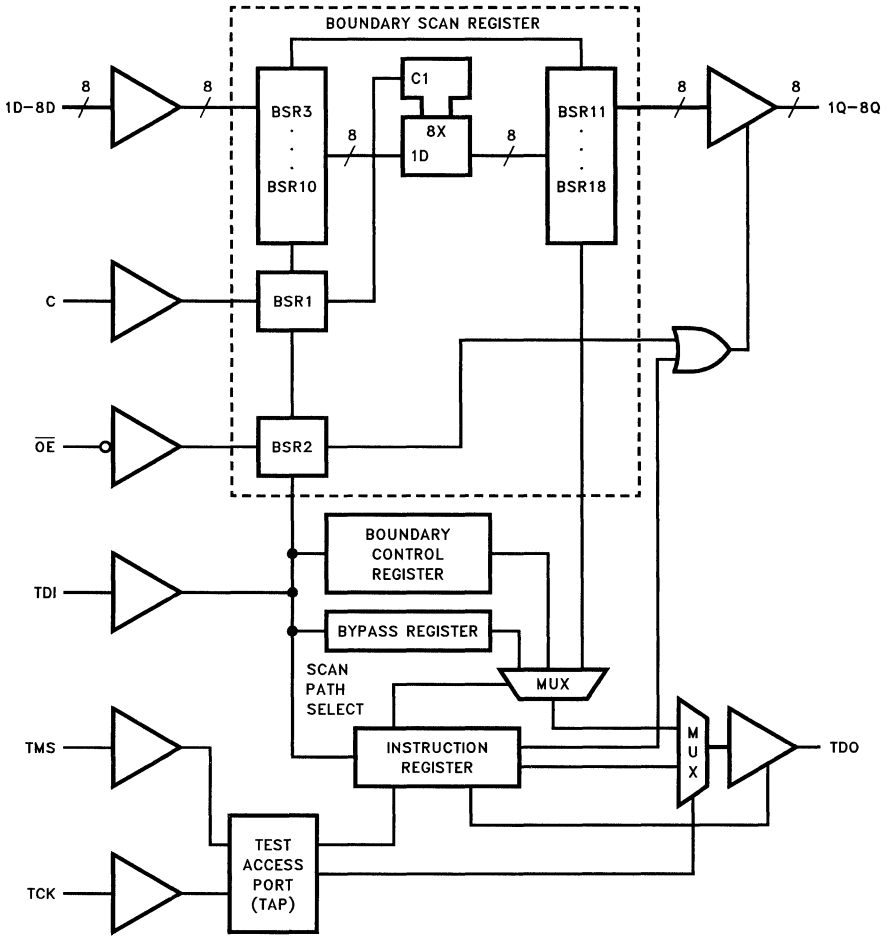
INPUTS			OUTPUT
$\overline{OE}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

functional block diagram



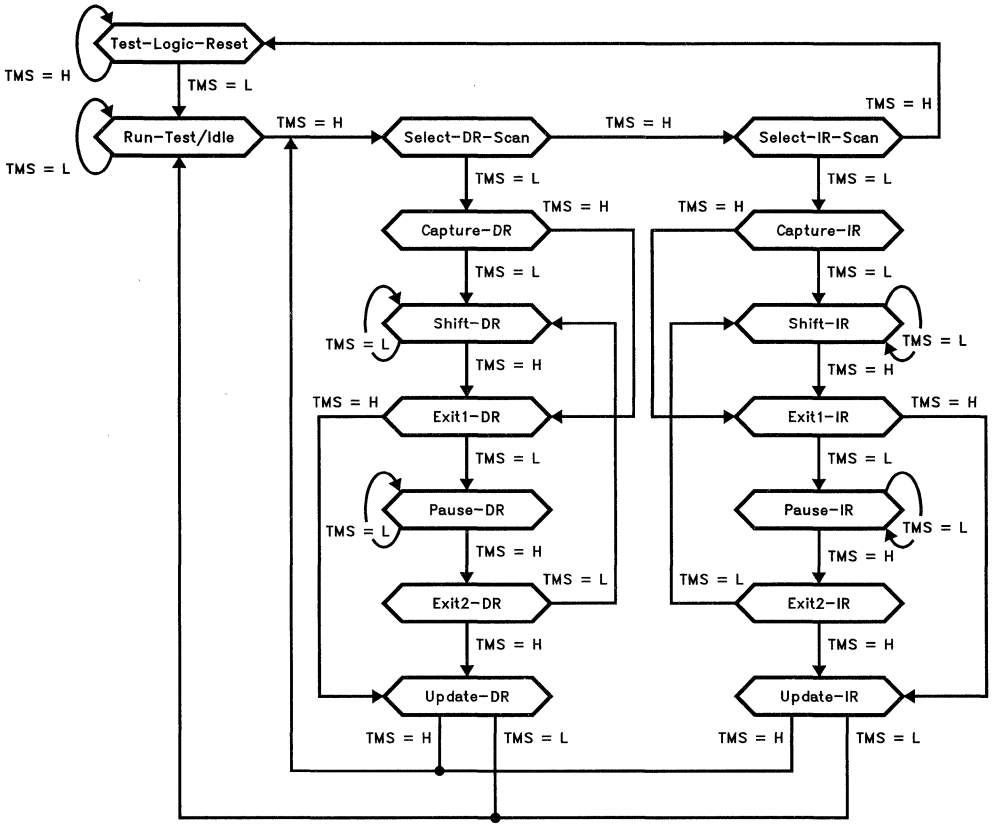


FIGURE 1. TAP STATE DIAGRAM

state diagram description

The TAP proceeds through the states shown in Figure 1 according to the IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow in Figure 1) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram, one to manipulate a data register and one to manipulate the instruction register. It is necessary to finish manipulating one register before accessing another.

Test-Logic-Reset
In this state, the test logic is not active and the device operates in its normal function mode. The state diagram is constructed such that the TAP will return to this state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup resistor that will force it high if left unconnected, or if a board defect causes it to be open-circuited. The device powers up in the Test-Logic-Reset state.

Run-Test/Idle
The TAP must pass through this state before executing any test operations. The test operations controlled by the boundary control register (see Table 2) are performed while in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan
No specific function is performed in these states, and the TAP will exit either of them on the next TCK cycle.

Capture-DR
The selected data register is placed in the scan path. Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK causing the TAP state to change. On the falling edge of TCK in Capture-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to a low level.

Shift-DR
While in this state, data is serially shifted through the selected data register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR).

Exit1-DR, Exit2-DR
These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-DR to Exit1-DR.

Pause-DR
The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data.

Update-DR
If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated during this, and only this, state. TDO goes to the high-impedance state on the falling edge of TCK in Update-DR.

state diagram description (continued)

Capture-IR
The instruction register is preloaded with a 10000001 pattern and placed in the scan path. On the falling edge of TCK in Capture-IR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to a low level.

Shift-IR
While in this state, data is serially shifted through the instruction register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR).

Exit1-IR, Exit2-IR
These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-IR to Exit1-IR.

Pause-IR
The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR
The latches shadowing the instruction register are updated with the new instruction. TDO goes to the high-impedance state on the falling edge of TCK in Update-IR.

instruction register description

Serial test information is conveyed by means of a 4-wire test bus. Commands, data, and control signals are all passed along the 4-wire bus. The function of the TAP is to extract the state control information and synchronous control signals for the bus and generate the appropriate on-chip control signals for the test structures in the device. The TAP monitors two signals from the bus, TCK and TMS. Figure 1 shows the TAP state diagram. The functional block diagram illustrates the IEEE Standard 1149.1 4-wire test bus and boundary scan architecture, and the relationship between the TAP, the test bus, and the boundary scan test elements.

Data is captured on the rising edge of TCK, and outputs change after the falling edge of TCK.

As shown in the functional block diagram, the 'BCT8373 contains an eight-bit instruction register and three data registers: the 18-bit boundary scan register, the two-bit boundary control register, and the one-bit bypass register. Any register can be thought of as a serial shift register with a shadow latch on each bit. Latches may be loaded during the Update-DR and Update-IR TAP states.

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the test operation to be performed, the state of the functional inputs and outputs (whether or not the device will perform its normal function during the test operation), which of the three data registers is to be selected for inclusion in the scan path during the next data register scan operation, and the source of the data preloaded in the data register during the Capture-DR state. Table 1 lists the instructions supported by the 'BCT8373. Any SCOPE™ instructions not supported default to BYPASS.

The IR is loaded during the Capture-IR state with the value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path.

The instruction register order of scan is shown in Figure 2.

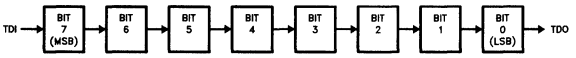


FIGURE 2. INSTRUCTION REGISTER ORDER OF SCAN

data register descriptions

boundary scan register

The boundary scan register (BSR) contains 18 bits, one for each functional input and output on the device. The BSR is used to store test data that is to be applied internally and/or externally to the device, and to capture and store data that is applied to the functional inputs and outputs of the device. The origination of the value loaded in the BSR during the Capture-DR state is determined by the current instruction.

The boundary scan register order of scan is shown in Figure 3.

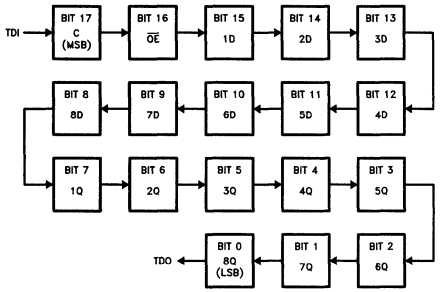


FIGURE 3. BOUNDARY SCAN REGISTER ORDER OF SCAN

boundary control register

The boundary control register (BCR) contains two bits and is used to implement additional test operations not included in the SCOPE™ instruction set, including pseudo-random pattern generation (PRPG) and parallel signature analysis (PSA) operations. The BCR retains its current value during the Capture-DR state. The BCR resets to the PSA operation.

The boundary control register order of scan is shown in Figure 4.

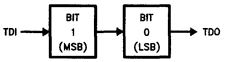


FIGURE 4. BOUNDARY CONTROL REGISTER ORDER OF SCAN

bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation. The bypass register is loaded with a logic 0 during the Capture-DR state.

The bypass register order of scan is shown in Figure 5.

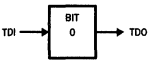


FIGURE 5. BYPASS REGISTER ORDER OF SCAN

TABLE 1. INSTRUCTION REGISTER OPCODES

BINARY CODE†‡ BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
X0000000	EXTEST	Boundary Scan	Boundary Scan	Test
X0000001	BYPASS§	Bypass Scan	Bypass	Normal
X0000010	SAMPLE	Sample Boundary	Boundary Scan	Normal
X0000011	INTEST	Boundary Scan	Boundary Scan	Test
X0000100	BYPASS§	Bypass Scan	Bypass	Normal
X0000101	BYPASS§	Bypass Scan	Bypass	Normal
X0000110	TRIBYP	Control Boundary to High-Impedance	Bypass	Modified Test
X0000111	SETBYP	Control Boundary to 1/0	Bypass	Test
X0001000	BYPASS§	Bypass Scan	Bypass	Normal
X0001001	RUNT	Boundary Run Test	Bypass	Test
X0001010	READBN	Boundary Read	Boundary Scan	Normal
X0001011	READBT	Boundary Read	Boundary Scan	Test
X0001100	CELLTST	Boundary Self-test	Boundary Scan	Normal
X0001101	TOPHIP	Boundary Toggle Outputs	Bypass	Test
X0001110	SCANCN	Boundary Control Register Scan	Boundary Control	Normal
X0001111	SCANCT	Boundary Control Register Scan	Boundary Control	Test
ALL OTHER	BYPASS	Bypass Scan	Bypass	Normal

† The SCOPE instruction set specifies even parity in the eight-bit instruction. This feature is not implemented in the 'BCT8373.
‡ X = Don't care.
§ A SCOPE opcode exists but is not supported in the 'BCT8373.

instruction register opcode descriptions

The 'BCT8373 runs test instructions based on the value scanned into the instruction register. The test functions are defined as follows:

boundary scan
This instruction simultaneously executes the IEEE Standard 1149.1 EXTEST and INTEST instructions. The boundary scan register is selected in the scan path. Data appearing at the device inputs and outputs is captured. Data previously loaded into the boundary scan register is applied to the device inputs and through the device outputs.

bypass scan
Conforms to the IEEE Standard 1149.1 BYPASS instruction. The one-bit bypass register is selected in the scan path. A logic 0 is loaded in the bypass register. The device operates in the normal mode.

sample boundary
Conforms to the IEEE Standard 1149.1 SAMPLE instruction. Data appearing at the device inputs and outputs is sampled without affecting normal device operation. The boundary scan register is selected in the scan path.

control boundary to high-impedance
The device outputs are placed in the high-impedance state. The bypass register is selected in the scan path. Device inputs remain operational, and the internal logic function will be performed.

control boundary to 1/0
The data in the boundary scan register is applied to the functional inputs and through the device outputs. The bypass register is selected in the scan path.

instruction register opcode descriptions (continued)

boundary run test
A test operation is run as decoded by the boundary control register. The desired test must be preloaded in the boundary control register, and the TAP placed in the Run-Test/Idle state. The four test operations decoded by the boundary control register are:

- parallel signature analysis (PSA)
  Data appearing on the functional data inputs is compressed into sixteen bits. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figure 6 shows the algorithm through which the signature is generated.
- pseudo-random pattern generation (PRPG)
  A pseudo-random pattern is generated at the functional outputs. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figure 7 shows the algorithm through which the patterns are generated. Note that a seed value of all zeroes will not produce additional patterns.
- simultaneous PSA and PRPG
  Both PSA and PRPG operations are performed as shown in Figure 8.
- sample inputs/toggle outputs
  Data appearing at the functional inputs is sampled on each TCK rising edge, and the functional outputs are toggled on each TCK falling edge.

boundary read
The boundary scan register is selected in the scan path. No load operation is performed prior to shifting. This instruction is useful for inspecting data after a PSA operation.

boundary control register scan
The two-bit boundary control register is placed in the scan path. This register must be loaded prior to executing a boundary run test operation.

boundary self-test
The boundary scan register is selected in the scan path. This operation tests the logic in the boundary scan cells by loading the inverse of the current value of the cells. By loading a known value in the boundary scan register, executing CELLTST, and inspecting the resulting data through a scan operation, the integrity of the boundary scan register can be verified.

boundary toggle outputs
Functional outputs are toggled on each TCK falling edge. Data appearing on the device's functional inputs is not captured.

tap bits for PSA and PRPG

The BCR opcodes are shown in Table 2. The use of these TAP bits and the algorithms used for 8- and 16-bit PSA and PRPG operations are shown in Figures 6 through 8. The two control inputs, C and $\overline{OE}$, are ignored during these operations.

TABLE 2. BOUNDARY CONTROL REGISTER OPCODES

BINARY CODE BIT 1 → BIT 0 MSB → LSB	DESCRIPTION
00	Sample inputs/toggle outputs
01	PRPG/16-bit mode
10	PSA/16-bit mode
11	Simultaneous PRPG and PSA/8-bit mode

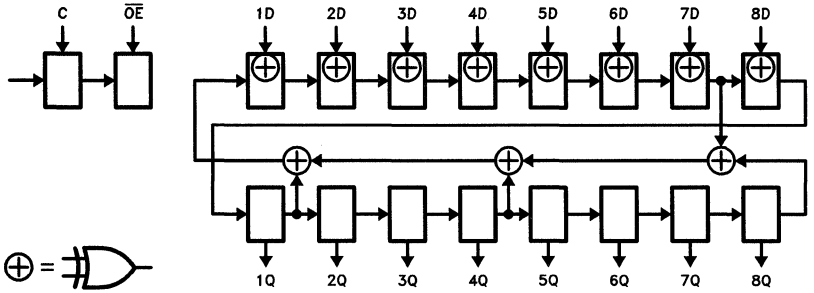


FIGURE 6. 16-BIT PSA CONFIGURATION

A PSA operation on the 8 data inputs proceeds as the 8 data outputs are held static.

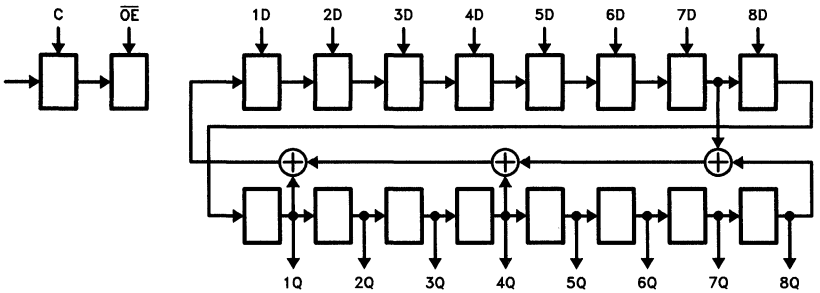


FIGURE 7. 16-BIT PRPG CONFIGURATION

A PRPG operation from the eight data outputs proceeds while the inputs are ignored.

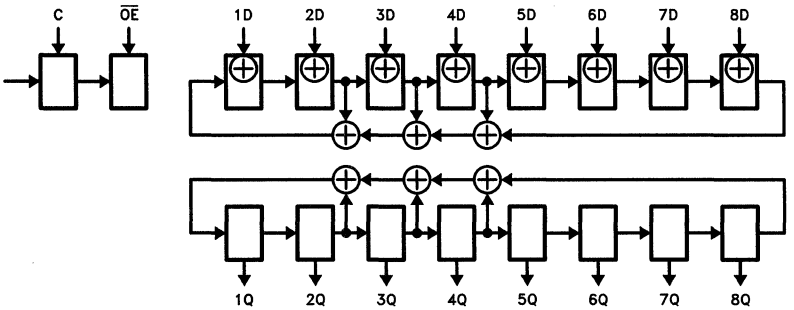


FIGURE 8. 8-BIT PSA AND PRPG CONFIGURATION

Simultaneously, an 8-bit PSA operation proceeds on the 8 data inputs, while an 8-bit PRPG operation proceeds from the 8 data outputs.

timing description

All test operations of the 'BCT8373 are synchronous to TCK. Data on the TDI, TMS, and functional inputs is captured on the rising edge of TCK. Data appears on the TDO and functional output pins on the falling edge of TCK.

The 'BCT8373 is advanced through its state diagram (see Figure 1) by changing the value of TMS and applying a clock pulse to TCK. A simple timing example is shown in Figure 9. In this example, the device begins in the Test-Logic-Reset state and is loaded with an instruction to select the bypass register in the scan path. The binary logic value 101 is shifted through the bypass register from TDI to TDO, and the device is returned to the Test-Logic-Reset state. Table 3 explains the function of the test circuitry during each TCK cycle.

TABLE 3. EXPLANATION OF TIMING EXAMPLE

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION/COMMENT
1	Test-Logic-Reset	Recycle on reset state.
2	Run-Test/Idle	Begin advancing towards desired state.
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	IR loads with 10000001; TDO becomes active after falling edge of TCK.
6	Shift-IR	Ready to shift in instruction; TDI must be active before next clock.
7–13	Shift-IR	A BYPASS instruction (11111111) is serially loaded into the IR.
14	Exit1-IR	Note that TMS goes high prior to TCK #14. The last bit of the instruction is shifted in as the TAP advances from Shift-IR to Exit1-IR.
15	Update-IR	The IR is updated with the new instruction. TDO goes inactive (high-impedance) on the falling edge of TCK #15.
16	Select-DR-Scan	
17	Capture-DR	The bypass register loads with a logic 0; TDO becomes active.
18	Shift-DR	The bypass register is now in the scan path. Data will shift from TDI to TDO.
19–20	Shift-DR	The binary value '101' is shifted from TDI to TDO through the bypass register. Note that the last value shifted in (a logic 1) remains in the bypass register and is not shifted to the next test element.
21	Exit1-DR	
22	Update-DR	
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed.

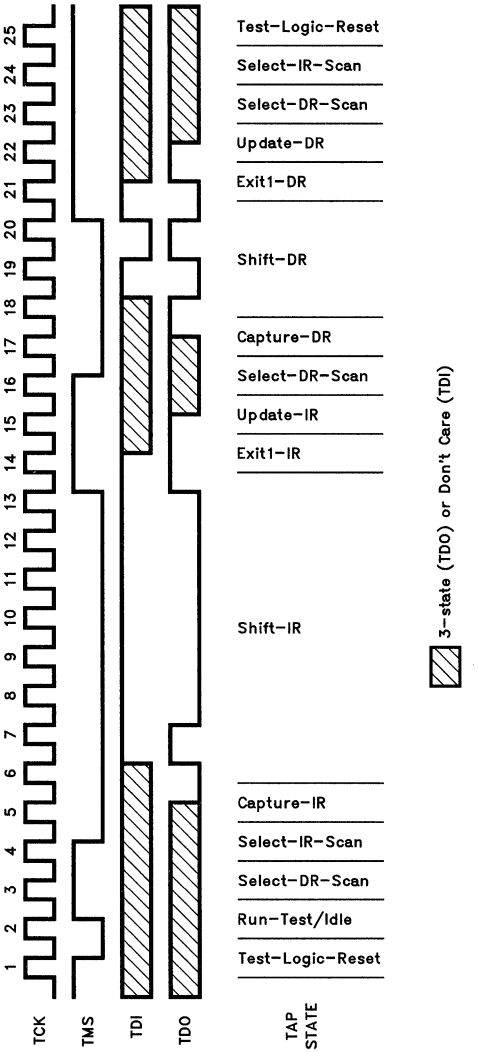


FIGURE 9. TIMING EXAMPLE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except TMS) ..... −0.5 V to 7 V
Input voltage range, V_I (TMS) ..... −0.5 V to 12 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54BCT8373 (TDO) ..... 40 mA
SN54BCT8373 (Any Q) ..... 96 mA
SN74BCT8373 (TDO) ..... 48 mA
SN74BCT8373 (Any Q) ..... 128 mA
Operating free-air temperature range: SN54BCT8373 ..... −55°C to 125°C
SN74BCT8373 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54BCT8373			SN74BCT8373			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IHH}	Double high-level input voltage	TMS	10	8.6	12	10	8.6	12	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	TDO			−3			−3	mA
		Any Q			−12			−15	
I_{OL}	Low-level output current	TDO			20			24	mA
		Any Y			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT8373			SN74BCT8373			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	Any Q	V_{CC} = 4.75 V	I_{OH} = −3 mA	2.7	3.4		2.7	3.4		V
		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
	TDO		I_{OH} = −1 mA	2.5	3.4		2.5	3.4		
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
V_{OL}	Any Q	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
			I_{OL} = 64 mA					0.42	0.55	
	TDO		I_{OL} = 20 mA		0.3	0.5				
			I_{OL} = 24 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V, V_I = 5.5 V				0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V, V_I = 2.7 V		−1	−35	−100	−1	−35	−100	µA
I_{IHH}	TMS	V_{CC} = 5.5 V, V_I = 10 V			0.3	1		0.3	1	mA
I_{IL}		V_{CC} = 5.5 V, V_I = 0.5 V			−70	−200		−70	−200	µA
I_{OZH}	Any Q	V_{CC} = 5.5 V, V_O = 2.7 V				50			50	µA
	TDO	V_{CC} = 5.5 V, V_O = 2.7 V		−1	−35	−100	−1	−35	−100	
I_{OZL}	Any Q	V_{CC} = 5.5 V, V_O = 0.5 V				−50			−50	µA
	TDO	V_{CC} = 5.5 V, V_O = 0.5 V			−70	−200		−70	−200	
I_{OS}‡		V_{CC} = 5.5 V, V_O = 0		−100		−225	−100		−225	mA
I_{CC}		V_{CC} = 5.5 V, Outputs open	Outputs high		3.5	7		3.5	7	mA
			Outputs low		35	52		35	52	
			Outputs disabled		1.5	3.5		1.5	3.5	
C_i		V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			10			10		pF
C_i	$\overline{OE}$	V_{CC} = 5 V, V_I = 0.5 V			8			8		pF
C_o		V_{CC} = 5 V, V_O = 2.5 V or 0.5 V			14			14		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

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timing requirements

			V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'BCT8373			'54BCT8373		'74BCT8373		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0		20	0	20	0	20	MHz
t_w	Pulse duration	TCK high or low	25			25		25		ns
		TMS reset high	50			50		50		
t_{su}	Setup time	TMS before TCK ↑	15			15		15		ns
		TDI before TCK ↑	6			6		6		
		Any D before TCK ↑	6			6		6		
		$\overline{OE}$ before TCK ↑	6			6		6		
t_h	Hold time	TMS after TCK ↑	0			0		0		ns
		TDI after TCK ↑	4.5			4.5		4.5		
		Any D after TCK ↑	4.5			4.5		4.5		
		$\overline{OE}$ after TCK ↑	4.5			4.5		4.5		
t_{pu}		Wait time, power up to TCK ↑	100			100		100		ns

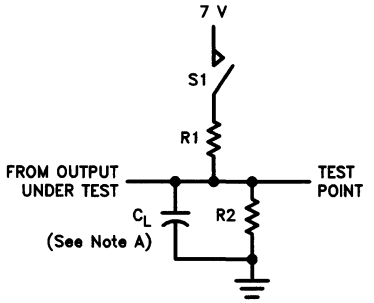
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT8373			'54BCT8373		'74BCT8373		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		20			20		20		MHz
t_{PLH}	D	Any Q	2	5.6	9	2	11.5	2	10	ns
t_{PHL}			2	5.5	9	2	10.6	2	10	
t_{PLH}	C	Q	3	6.7	10.5	3	12.9	3	11.4	ns
t_{PHL}			3	6.7	10.5	3	12.8	3	11.6	
t_{PLH}	TCK ↓	Any Q	3.9	10.9	15.7	3.9	21.5	3.9	19.8	ns
t_{PHL}			3.9	10.8	15.3	3.9	21.5	3.9	19.5	
t_{PLH}	TCK ↓	TDO	3.2	8.5	12.3	3.2	16.8	3.2	15.4	ns
t_{PHL}			3.2	8.3	12	3.2	16.2	3.2	15	
t_{PLH}	TCK ↑	Any Q	6.2	13.7	21	6.2	29	6.6	25	ns
t_{PHL}			6.6	15	22	6.6	29.6	6.6	26	
t_{PZH}	$\overline{OE}$	Any Q	2.4	5.6	9	2.4	11.1	2.4	10.6	ns
t_{PZL}			3	6.8	10.9	3	12.9	3	12	
t_{PHZ}	$\overline{OE}$	Any Q	2.5	5.7	9.5	2.5	10.9	2.5	10	ns
t_{PLZ}			2.4	5.5	9	2.4	10.5	2.4	9.6	
t_{PZH}	TCK ↓	Any Q	4.7	11.7	16.7	4.7	23.1	4.7	21.1	ns
t_{PZL}			5.5	13.6	19.7	5.5	24.4	5.5	22.9	
t_{PHZ}	TCK ↓	Any Q	3.4	9	13.2	3.4	18.7	3.4	17.3	ns
t_{PLZ}			3.6	10	14.6	3.6	19.5	3.6	17.8	
t_{PZH}	TCK ↑	Any Q	6.9	15.5	21.7	6.9	30	6.9	27	ns
t_{PZL}			7.8	17.6	24.9	7.8	32	7.8	29	
t_{PHZ}	TCK ↑	Any Q	5	12.7	18.3	5	25.5	5	22.8	ns
t_{PLZ}			4.6	12.2	17.5	4.6	24.7	4.6	22	
t_{PZH}	TCK ↓	TDO	2.4	6.2	9	2.4	11.3	2.4	10.8	ns
t_{PZL}			3.2	7.6	10.6	3.2	13.2	3.2	12.6	
t_{PHZ}	TCK ↓	TDO	2.6	7.1	10.2	2.6	13	2.6	12.8	ns
t_{PLZ}			2.2	5.9	8.7	2.2	12.7	2.2	11.6	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

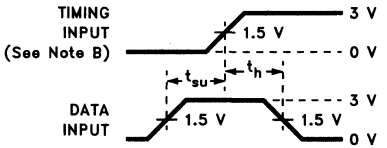
PARAMETER MEASUREMENT INFORMATION



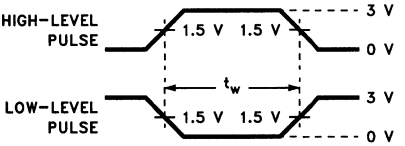
LOAD CIRCUIT

SWITCH POSITION TABLE

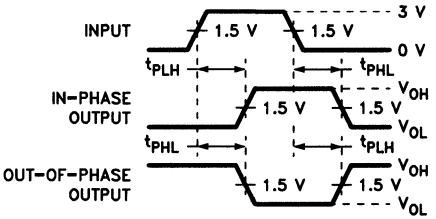
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



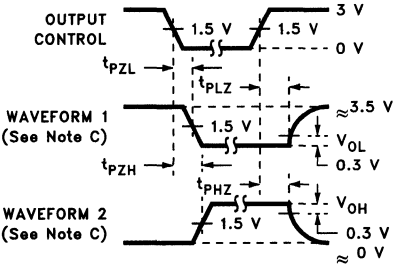
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

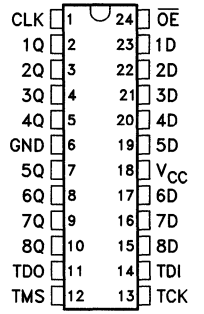
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 10. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

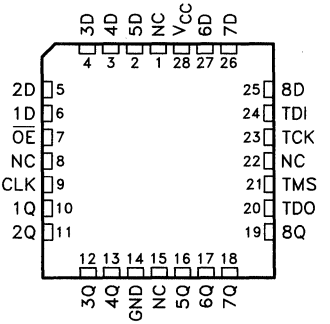
TI0223—D3641, JUNE 1990

- **Members of Texas Instruments SCOPE™ Family of Testability Products**
- **Octal Test Integrated Circuits**
- **Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus**
- **Functionally Equivalent to SN54/74F374 and SN54/74BCT374 in the Normal Function Mode**
- **Test Operation Synchronous to Test Access Port (TAP)**
- **Implement Optional "Test Reset" Signal on TAP by Recognizing a Double-High on TMS Pin**
- **SCOPE™ Instruction Set**
  - **Conform to the IEEE 1149.1 Boundary Scan**
  - **Provide Data Compression of Inputs**
  - **Provide Pseudo-Random Pattern Generation From Outputs**
  - **Sample Input/Toggle Output Mode**
  - **Output to High-Impedance State Mode**
- **Fabricated Using TI State-of-the-Art BiCMOS Technology**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT8374 ... JT PACKAGE
SN74BCT8374 ... DW OR NT PACKAGE
(TOP VIEW)



SN54BCT8374 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN54BCT8374 and SN74BCT8374 are members of Texas Instruments SCOPE™ testability IC family. This family of components blends test circuitry with standard logic functions to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode these devices are functionally equivalent to the SN54/74F374 and SN54/74BCT374 octal D-type flip-flops. In the test mode, the test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ octal flip-flops.

In the test mode the normal operation of the SCOPE™ octal flip-flop is inhibited and the test circuitry is enabled to observe and control the device's I/O boundary. When enabled, the test circuitry can perform boundary scan test operations as described in the IEEE Standard 1149.1 specification. Four dedicated test pins are used to control the operation of the test circuitry: TDI (test data in), TDO (test data out), TMS

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description (continued)

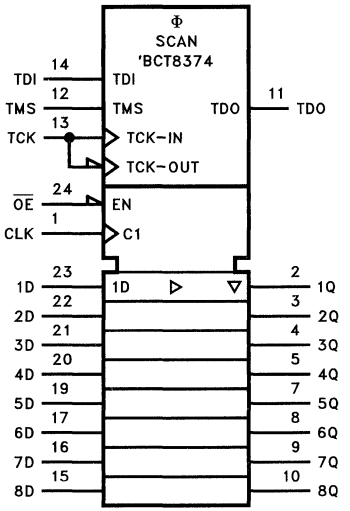
(test mode select), and TCK (test clock). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54BCT8374 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT8374 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(Normal Mode) (Each Flip-Flop)

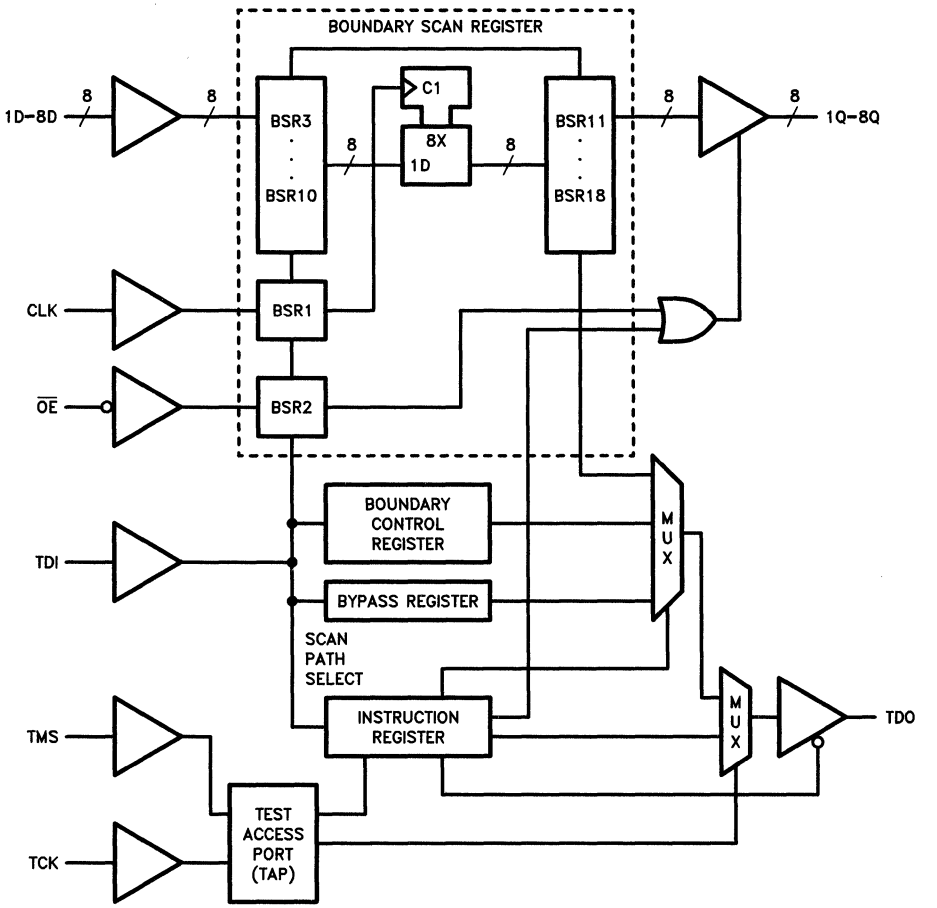
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

functional block diagram



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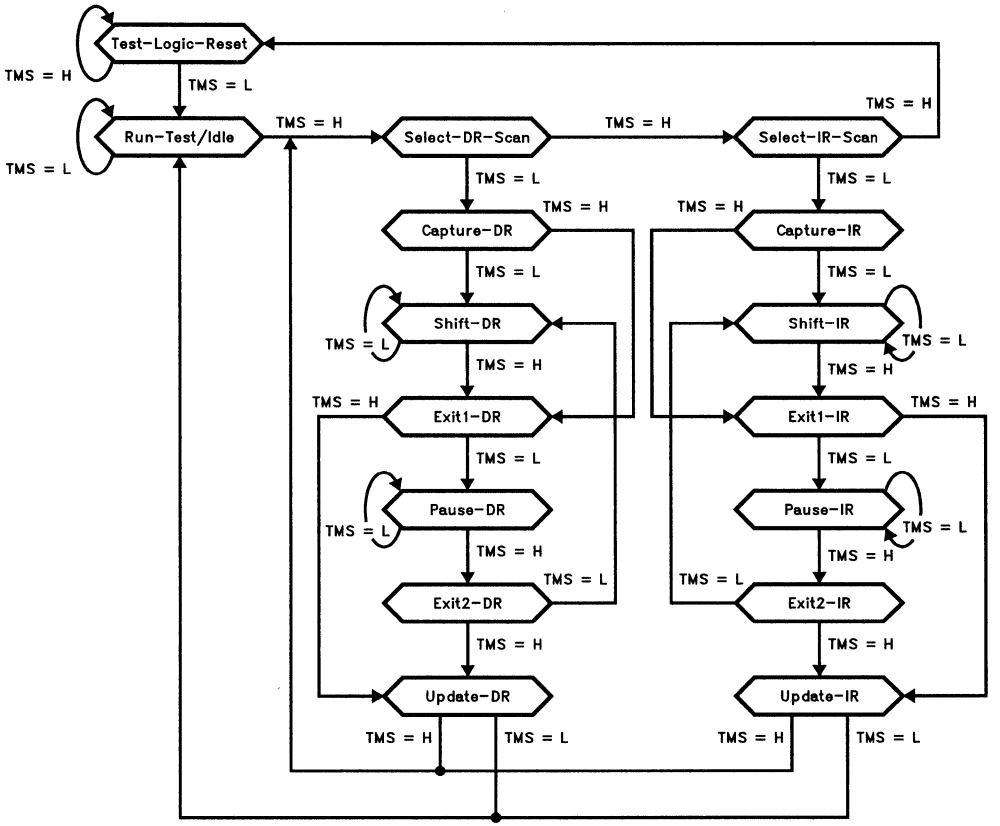

FIGURE 1. TAP STATE DIAGRAM

state diagram description

The TAP proceeds through the states shown in Figure 1 according to the IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow in Figure 1) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram, one to manipulate a data register and one to manipulate the instruction register. It is necessary to finish manipulating one register before accessing another.

state diagram description (continued)

Test-Logic-Reset
In this state, the test logic is not active and the device operates in its normal function mode. The state diagram is constructed such that the TAP will return to this state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup resistor that will force it high if left unconnected, or if a board defect causes it to be open-circuited. The device powers up in the Test-Logic-Reset state.

Run-Test/Idle
The TAP must pass through this state before executing any test operations. The test operations controlled by the boundary control register (see Table 2) are performed while in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan
No specific function is performed in these states, and the TAP will exit either of them on the next TCK cycle.

Capture-DR
The selected data register is placed in the scan path. Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK causing the TAP state to change. On the falling edge of TCK in Capture-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to a low level.

Shift-DR
While in this state, data is serially shifted through the selected data register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR).

Exit1-DR, Exit2-DR
These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-DR to Exit1-DR.

Pause-DR
The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data.

Update-DR
If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated during this, and only this, state. TDO goes to the high-impedance state on the falling edge of TCK in Update-DR.

Capture-IR
The instruction register is preloaded with a 10000001 pattern and placed in the scan path. On the falling edge of TCK in Capture-IR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to a low level.

Shift-IR
While in this state, data is serially shifted through the instruction register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR).

state diagram description (continued)

Exit1-IR, Exit2-IR
These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-IR to Exit1-IR.

Pause-IR
The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR
The latches shadowing the instruction register are updated with the new instruction. TDO goes to the high-impedance state on the falling edge of TCK in Update-IR.

instruction register description

Serial test information is conveyed by means of a 4-wire test bus. Commands, data, and control signals are all passed along the 4-wire bus. The function of the TAP is to extract the state control information and synchronous control signals for the bus and generate the appropriate on-chip control signals for the test structures in the device. The TAP monitors two signals from the bus, TCK and TMS. Figure 1 shows the TAP state diagram. The functional block diagram illustrates the IEEE Standard 1149.1 4-wire test bus and boundary scan architecture, and the relationship between the TAP, the test bus, and the boundary scan test elements.

Data is captured on the rising edge of TCK. Outputs change after the falling edge of TCK.

As shown in the functional block diagram, the 'BCT8374 contains an eight-bit instruction register and three data registers: the 18-bit boundary scan register, the two-bit boundary control register, and the one-bit bypass register. Any register can be thought of as a serial shift register with a shadow latch on each bit. Latches may be loaded during the Update-DR and Update-IR TAP states.

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the test operation to be performed, the state of the functional inputs and outputs (whether or not the device will perform its normal function during the test operation), which of the three data registers is to be selected for inclusion in the scan path during the next data register scan operation, and the source of the data preloaded in the data register during the Capture-DR state. Table 1 lists the instructions supported by the 'BCT8374. Any SCOPE™ instructions not supported default to BYPASS.

The IR is loaded during the Capture-IR state with the value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path.

The instruction register order of scan is shown in Figure 2.

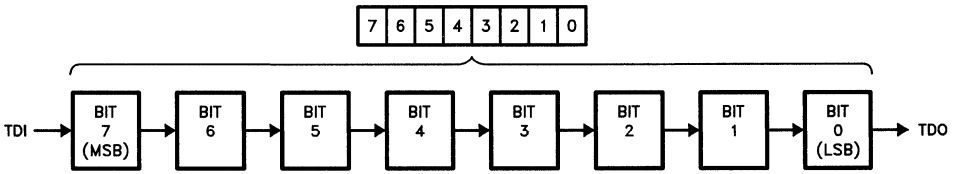

FIGURE 2. INSTRUCTION REGISTER ORDER OF SCAN

data register descriptions

boundary scan register

The boundary scan register (BSR) contains 18 bits, one for each functional input and output on the device. The BSR is used to store test data that is to be applied internally and/or externally to the device, and to capture and store data that is applied to the functional inputs and outputs of the device. The origination of the value loaded in the BSR during the Capture-DR state is determined by the current instruction.

The boundary scan register order of scan is shown in Figure 3.

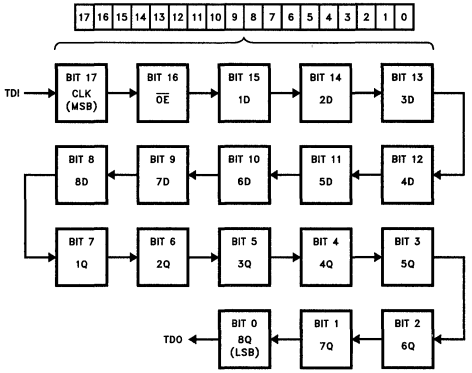

FIGURE 3. BOUNDARY SCAN REGISTER ORDER OF SCAN

boundary control register

The boundary control register (BCR) contains two bits and is used to implement additional test operations not included in the SCOPE™ instruction set, including pseudo-random pattern generation (PRPG) and parallel signature analysis (PSA) operations. The BCR retains its current value during the Capture-DR state. The BCR resets to the PSA operation.

The boundary control register order of scan is shown in Figure 4.

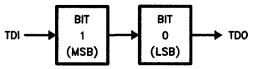

FIGURE 4. BOUNDARY CONTROL REGISTER ORDER OF SCAN

bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation. The bypass register is loaded with a logic 0 during the Capture-DR state.

The bypass register order of scan is shown in Figure 5.

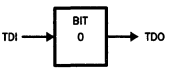

FIGURE 5. BYPASS REGISTER ORDER OF SCAN

TABLE 1. INSTRUCTION REGISTER OPCODES

BINARY CODE†‡ BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
X0000000	EXTEST	Boundary Scan	Boundary Scan	Test
X0000001	BYPASS§	Bypass Scan	Bypass	Normal
X0000010	SAMPLE	Sample Boundary	Boundary Scan	Normal
X0000011	INTEST	Boundary Scan	Boundary Scan	Test
X0000100	BYPASS§	Bypass Scan	Bypass	Normal
X0000101	BYPASS§	Bypass Scan	Bypass	Normal
X0000110	TRIBYP	Control Boundary to High-Impedance	Bypass	Modified Test
X0000111	SETBYP	Control Boundary to 1/0	Bypass	Test
X0001000	BYPASS§	Bypass Scan	Bypass	Normal
X0001001	RUNT	Boundary Run Test	Bypass	Test
X0001010	READBN	Boundary Read	Boundary Scan	Normal
X0001011	READBT	Boundary Read	Boundary Scan	Test
X0001100	CELLTST	Boundary Self-test	Boundary Scan	Normal
X0001101	TOPHIP	Boundary Toggle Outputs	Bypass	Test
X0001110	SCANCN	Boundary Control Register Scan	Boundary Control	Normal
X0001111	SCANCT	Boundary Control Register Scan	Boundary Control	Test
ALL OTHER	BYPASS	Bypass Scan	Bypass	Normal

† The SCOPE instruction set specifies even parity in the eight-bit instruction. This feature is not implemented in the 'BCT8374.
‡ X = Don't care.
§ A SCOPE opcode exists but is not supported in the 'BCT8374.

instruction register opcode descriptions

The 'BCT8374 runs test instructions based on the value scanned into the instruction register. The test functions are defined as follows:

boundary scan
This instruction simultaneously executes the IEEE Standard 1149.1 EXTEST and INTEST instructions. The boundary scan register is selected in the scan path. Data appearing at the device inputs and outputs is captured. Data previously loaded into the boundary scan register is applied to the device inputs and through the device outputs.

bypass scan
Conforms to the IEEE Standard 1149.1 BYPASS instruction. The one-bit bypass register is selected in the scan path. A logic 0 is loaded in the bypass register. The device operates in the normal mode.

sample boundary
Conforms to the IEEE Standard 1149.1 SAMPLE instruction. Data appearing at the device inputs and outputs is sampled without affecting normal device operation. The boundary scan register is selected in the scan path.

control boundary to high-impedance
The device outputs are placed in the high-impedance state. The bypass register is selected in the scan path. Device inputs remain operational, and the internal logic function will be performed.

control boundary to 1/0
The data in the boundary scan register is applied to the functional inputs and through the device outputs. The bypass register is selected in the scan path.

instruction register opcode descriptions (continued)

boundary run test
A test operation is run as decoded by the boundary control register. The desired test must be preloaded in the boundary control register, and the TAP placed in the Run-Test/Idle state. The four test operations decoded by the boundary control register are:

- parallel signature analysis (PSA)
  Data appearing on the functional data inputs is compressed into sixteen bits. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figure 6 shows the algorithm through which the signature is generated.
- pseudo-random pattern generation (PRPG)
  A pseudo-random pattern is generated at the functional outputs. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figure 7 shows the algorithm through which the patterns are generated. Note that a seed value of all zeroes will not produce additional patterns.
- simultaneous PSA and PRPG
  Both PSA and PRPG operations are performed as shown in Figure 8.
- sample inputs/toggle outputs
  Data appearing at the functional inputs is sampled on each TCK rising edge, and the functional outputs are toggled on each TCK falling edge.

boundary read
The boundary scan register is selected in the scan path. No load operation is performed prior to shifting. This instruction is useful for inspecting data after a PSA operation.

boundary control register scan
The two-bit boundary control register is placed in the scan path. This register must be loaded prior to executing a boundary run test operation.

boundary self-test
The boundary scan register is selected in the scan path. This operation tests the logic in the boundary scan cells by loading the inverse of the current value of the cells. By loading a known value in the boundary scan register, executing CELLTST, and inspecting the resulting data through a scan operation, the integrity of the boundary scan register can be verified.

boundary toggle outputs
Functional outputs are toggled on each TCK falling edge. Data appearing on the device's functional inputs is not captured.

tap bits for PSA and PRPG

The BCR opcodes are shown in Table 2. The use of these tap bits and the algorithms used for 8- and 16-bit PSA and PRPG operations are shown in Figures 6 through 8. The two control inputs, CLK and $\overline{OE}$, are ignored during these operations.

TABLE 2. BOUNDARY CONTROL REGISTER OPCODES

BINARY CODE BIT 1 → BIT 0 MSB → LSB	DESCRIPTION
00	Sample inputs/toggle outputs
01	PRPG/16-bit mode
10	PSA/16-bit mode
11	Simultaneous PRPG and PSA/8-bit mode

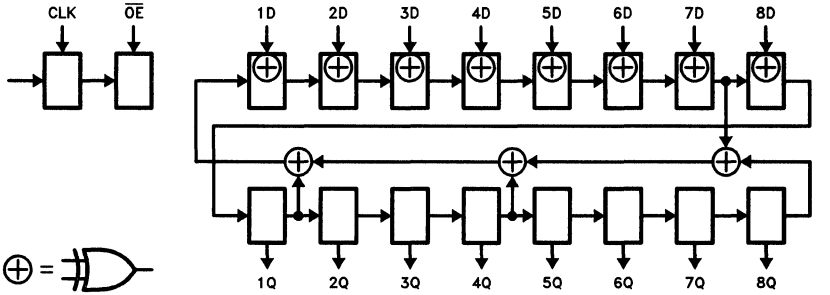

FIGURE 6. 16-BIT PSA CONFIGURATION

A PSA operation on the 8 data inputs proceeds as the 8 data outputs are held static.

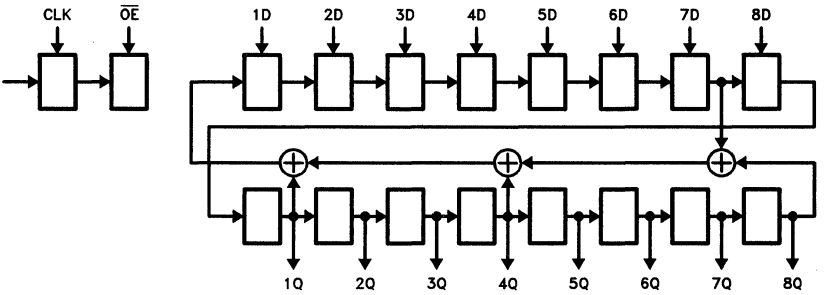

FIGURE 7. 16-BIT PRPG CONFIGURATION

A PRPG operation from the 8 data outputs proceeds while the inputs are ignored.

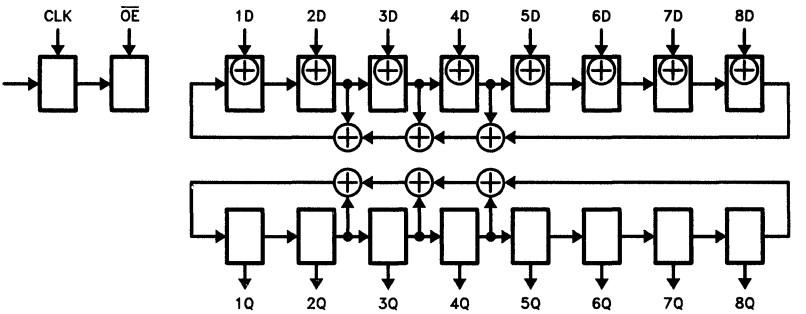

FIGURE 8. 8-BIT PSA AND PRPG CONFIGURATION

Simultaneously, an 8-bit PSA operation proceeds on the 8 data inputs, while an 8-bit PRPG operation proceeds from the 8 data outputs.

timing description

All test operations of the 'BCT8374 are synchronous to TCK. Data on the TDI, TMS, and functional inputs is captured on the rising edge of TCK. Data appears on the TDO and functional output pins on the falling edge of TCK.

The 'BCT8374 is advanced through its state diagram (see Figure 1) by changing the value of TMS and applying a clock pulse to TCK. A simple timing example is shown in Figure 9. In this example, the device begins in the Test-Logic-Reset state and is loaded with an instruction to select the bypass register in the scan path. The binary logic value 101 is shifted through the bypass register from TDI to TDO, and the device is returned to the Test-Logic-Reset state. Table 3 explains the function of the test circuitry during each TCK cycle.

TABLE 3. EXPLANATION OF TIMING EXAMPLE

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION/COMMENT
1	Test-Logic-Reset	Recycle on reset state.
2	Run-Test/Idle	Begin advancing towards desired state.
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	IR loads with 10000001; TDO becomes active after falling edge of TCK.
6	Shift-IR	Ready to shift in instruction; TDI must be active before next clock.
7–13	Shift-IR	A BYPASS instruction (11111111) is serially loaded into the IR.
14	Exit1-IR	Note that TMS goes high prior to TCK #14. The last bit of the instruction is shifted in as the TAP advances from Shift-IR to Exit1-IR.
15	Update-IR	The IR is updated with the new instruction. TDO goes inactive (high-impedance) on the falling edge of TCK #15.
16	Select-DR-Scan	
17	Capture-DR	The bypass register loads with a logic 0; TDO becomes active.
18	Shift-DR	The bypass register is now in the scan path. Data will shift from TDI to TDO.
19–20	Shift-DR	The binary value '101' is shifted from TDI to TDO through the bypass register. Note that the last value shifted in (a logic 1) remains in the bypass register and is not shifted to the next test element.
21	Exit1-DR	
22	Update-DR	
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed.

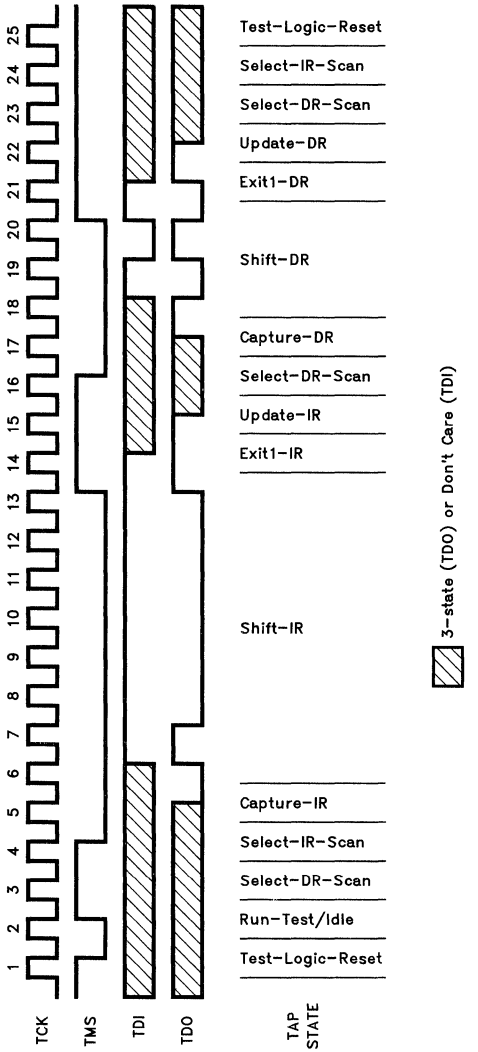

FIGURE 9. TIMING EXAMPLE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54BCT8374 (TDO) ..... 40 mA
SN54BCT8374 (Any Q) ..... 96 mA
SN74BCT8374 (TDO) ..... 48 mA
SN74BCT8374 (Any Q) ..... 128 mA
Operating free-air temperature range: SN54BCT8374 ..... −55°C to 125°C
SN74BCT8374 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54BCT8374			SN74BCT8374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IHH}	Double high-level input voltage	TMS	10		12	10		12	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	TDO			−3			−3	mA
		Any Q			−12			−15	
I_{OL}	Low-level output current	TDO			20			24	mA
		Any Y			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

TI0223—D3641, JUNE 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54BCT8374			SN74BCT8374			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA					−1.2			−1.2	V
V_{OH}	Any Q	V_{CC} = 4.75 V		I_{OH} = −3 mA	2.7	3.4		2.7	3.4		V
		V_{CC} = 4.5 V		I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
				I_{OH} = −12 mA	2	3.2					
				I_{OH} = −15 mA				2	3.1		
	TDO	V_{CC} = 4.5 V		I_{OH} = −1 mA	2.5	3.4		2.5	3.4		
				I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
V_{OL}	Any Q	V_{CC} = 4.5 V		I_{OL} = 48 mA		0.38	0.55				V
				I_{OL} = 64 mA					0.42	0.55	
	TDO	V_{CC} = 4.5 V		I_{OL} = 20 mA		0.3	0.5				
				I_{OL} = 24 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V, V_I = 5.5 V					0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V, V_I = 2.7 V			−1		−100	−1		−100	μA
I_{IHH}	TMS	V_{CC} = 5.5 V, V_I = 10 V					1			1	mA
I_{IL}		V_{CC} = 5.5 V, V_I = 0.5 V					−200			−200	μA
I_{OZH}	Any Q	V_{CC} = 5.5 V, V_O = 2.7 V					50			50	μA
	TDO	V_{CC} = 5.5 V, V_O = 2.7 V			−1		−100	−1		−100	
I_{OZL}	Any Q	V_{CC} = 5.5 V, V_O = 0.5 V					−50			−50	μA
	TDO	V_{CC} = 5.5 V, V_O = 0.5 V					−200			−200	
I_{OS}‡		V_{CC} = 5.5 V, V_O = 0			−100		−225	−100		−225	mA
I_{CC}		V_{CC} = 5.5 V,	Outputs open	Outputs high		3.5	7		3.5	7	mA
				Outputs low		35	52		35	52	
				Outputs disabled		1.5	3		1.5	3	
C_i		V_{CC} = 5 V, V_I = 2.5 V or 0.5 V				10			10		pF
C_o		V_{CC} = 5 V, V_O = 2.5 V or 0.5 V				14			14		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

timing requirements

			V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'BCT8374			'54BCT8374		'74BCT8374		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0		20	0	20	0	20	MHz
		CLK	0		70	0	70	0	70	
t_w	Pulse duration	TCK high or low	25			25		25		ns
		CLK high or low	5			5		5		
		TMS reset high	50			50		50		
t_{su}	Setup time	Data before CLK ↑	3			3		3		ns
		TMS before TCK ↑	12			12		12		
		TDI before TCK ↑	6			6		6		
		Any D before TCK ↑	6			6		6		
		$\overline{OE}$ before TCK ↑	6			6		6		
t_h	Hold time	Data after CLK ↓	2			2		2		ns
		TMS after TCK ↑	0			0		0		
		TDI after TCK ↑	4.5			4.5		4.5		
		Any D after TCK ↑	4.5			4.5		4.5		
		$\overline{OE}$ after TCK ↑	4.5			4.5		4.5		
t_{pu}		Wait time, power up to TCK ↑	100			100		100		ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

TEXAS INSTRUMENTS
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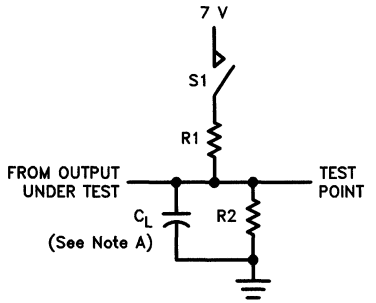
switching characteristics (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT8374			'54BCT8374		'74BCT8374		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		20			20		20		MHz
t_{PLH}	CLK	Any Q	3	7.1	10	3	12.5	3	11.5	ns
t_{PHL}			3	7.4	10.5	3	12.5	3	12	
t_{PLH}	TCK↓	Any Q	3.9	10.9	15.7	3.9	21.5	3.9	19.8	ns
t_{PHL}			3.9	10.8	15.3	3.9	21.5	3.9	19.5	
t_{PLH}	TCK↓	TDO	3.2	8.5	12.3	3.2	16.8	3.2	15.4	ns
t_{PHL}			3.2	8.3	12	3.2	16.3	3.2	15	
t_{PLH}	TCK↑	Any Q	6.2	13.9	21	6.2	29	6.2	25	ns
t_{PHL}			6.6	15	22	6.6	29.6	6.6	26	
t_{PZH}	$\overline{OE}$	Any Q	2.4	6.5	9	2.4	11	2.4	10.6	ns
t_{PZL}			3	7.8	10.9	3	12.9	3	12	
t_{PHZ}	$\overline{OE}$	Any Q	2.5	7.1	9.5	2.5	10.9	2.5	10	ns
t_{PLZ}			2.4	6.4	9	2.4	10.5	2.4	9.5	
t_{PZH}	TCK↓	Q	4.7	11.7	16.7	4.7	23.1	4.7	21.1	ns
t_{PZL}			5.5	13.6	19.7	5.5	24.4	5.5	22.9	
t_{PHZ}	TCK↓	Any Q	3.4	9	13.2	3.4	18.7	3.4	17.3	ns
t_{PLZ}			3.6	10	14.6	3.6	19.5	3.6	17.8	
t_{PZH}	TCK↓	TDO	2.4	6.2	9	2.4	11.3	2.4	10.8	ns
t_{PZL}			3.2	7.6	10.6	3.2	13.2	3.2	12.6	
t_{PHZ}	TCK↓	TDO	2.6	7.1	10.2	2.6	13	2.6	12.8	ns
t_{PLZ}			2.2	5.9	8.7	2.2	12.7	2.2	11.6	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

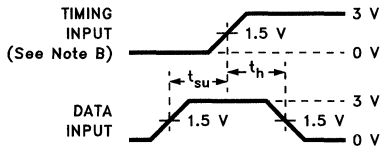
PARAMETER MEASUREMENT INFORMATION



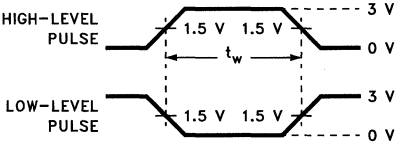
LOAD CIRCUIT

SWITCH POSITION TABLE

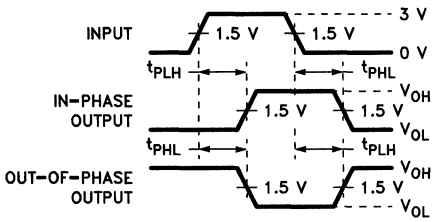
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



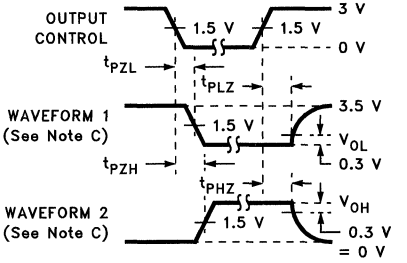
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

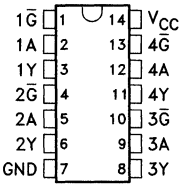
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 10. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TI0280—D3595, JULY 1990

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **High-Impedance State During Power-Up and Power-Down**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic DIPs**

D or N PACKAGE
(TOP VIEW)

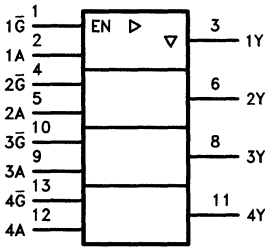


description

These bus buffers feature independent line drivers with three-state outputs. Each output is disabled when the associated $\overline{G}$ is high.

The SN64BCT125 is characterized for operation from −40°C to 85°C and 0°C to 70°C.

logic symbol†



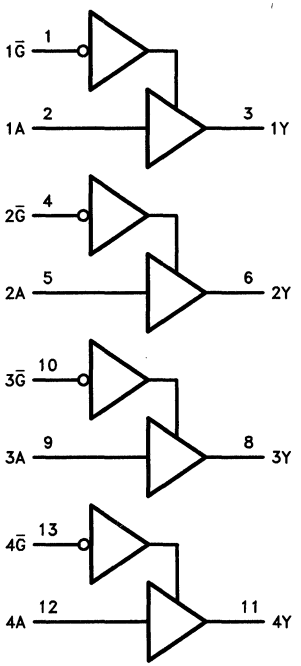
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	H
L	L	L
H	X	Z

H = high level,
L = low level,
X = irrelevant

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	−0.5 V to 5.5 V
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Current into any output in the low state	128 mA
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		V
		I_{OH} = −15 mA	2	3.1		
V_{OL}	V_{CC} = 4.5V	I_{OH} = 64 mA		0.42	0.55	V
I_{OZH}	V_{CC} = 0 V to 5.5 V, V_O = 2.7 V				50	mA
I_{OZL}	V_{CC} = 0 V to 5.5 V, V_O = 0.5 V				−50	μA
I_{OZ}	$\overline{G}$ at 0.8 V, V_O = 2.7 V or 0.5 V	V_{CC} = 0 to 1.3 V (power up)			±50	μA
		V_{CC} = 1.3 V to 0 (power down)			±50	
I_I	V_{CC} = 0, V_I = 7 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				25	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V				−20	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−100		−225	mA
I_{CCL}	V_{CC} = 5.5 V			46	49	mA
I_{CCH}	V_{CC} = 5.5 V			19	31	mA
I_{CCZ}	V_{CC} = 5.5 V			6	12	mA
C_i	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			4		pF
C_o	V_{CC} = 5 V, V_O = 2.5 V or 0.5 V			9		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

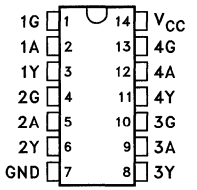
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω				UNIT
			T_A = 25°C			T_A = −40°C to 85°C		T_A = 0°C to 70°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.6	3.5	5.2	1.6	6	1.6	5.7	ns
t_{PHL}			2.7	5	6.9	2.7	8	2.7	7.7	
t_{PZH}	$\overline{G}$	Y	3.4	6.7	9	3.4	11.1	3.4	10.3	ns
t_{PZL}			5	8.2	10.4	5	12.8	5	11.7	
t_{PHZ}	$\overline{G}$	Y	3	5.8	7.4	3	9.4	3	8.9	ns
t_{PLZ}			2.8	5.5	7.3	2.8	9.9	2.8	8.6	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **High-Impedance State During Power-Up and Power-Down**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic DIPs**

D or N PACKAGE
(TOP VIEW)

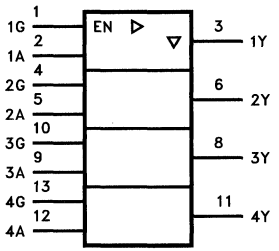


description

These bus buffers feature independent line drivers with three-state outputs. Each output is disabled when the associated G is high.

The SN64BCT126 is characterized for operation from −40°C to 85°C and 0°C to 70°C.

logic symbol†



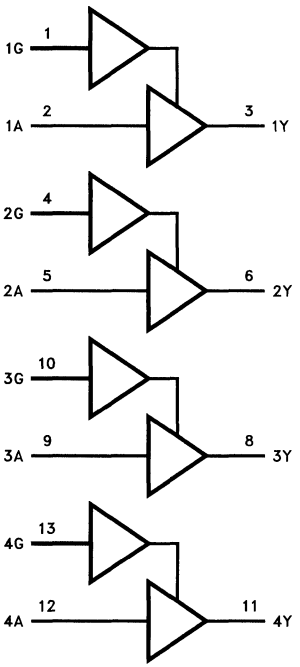
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS		OUTPUT
G	A	Y
H	H	H
H	L	L
L	X	Z

H = high level,
L = low level,
X = irrelevant

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	−0.5 V to 5.5 V
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Current into any output in the low state	128 mA
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		V
		I_{OH} = −15 mA	2	3.1		
V_{OL}	V_{CC} = 4.5V	I_{OH} = 64 mA		0.42	0.55	V
I_{OZH}	V_{CC} = 0 V to 5.5 V, V_O = 2.7 V				50	mA
I_{OZL}	V_{CC} = 0 V to 5.5 V, V_O = 0.5 V				−50	μA
I_{OZ}	$\overline{G}$ at 0.8 V,	V_{CC} = 0 to 1.3 V (power up)			±50	μA
	V_O = 2.7 V or 0.5 V	V_{CC} = 1.3 V to 0 (power down)			±50	
I_I	V_{CC} = 0, V_I = 7 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				25	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V				−20	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−100		−225	mA
I_{CCL}	V_{CC} = 5.5 V			35	51	mA
I_{CCH}	V_{CC} = 5.5 V			21	33	mA
I_{CCZ}	V_{CC} = 5.5 V			5	8	mA
C_i	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			4		pF
C_o	V_{CC} = 5 V, V_O = 2.5 V or 0.5 V			9		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

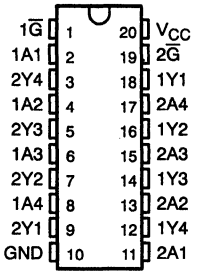
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω				UNIT
			T_A = 25°C			T_A = −40°C to 85°C		T_A = 0°C to 70°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	3.6	4.9	1.5	5.6	1.5	5.4	ns
t_{PHL}			2.7	5.3	6.9	2.7	7.7	2.7	7.4	
t_{PZH}	$\overline{G}$	Y	2.6	4.8	6.4	2.6	7.2	2.6	10.7	ns
t_{PZL}			3.7	6.4	8.3	3.7	10.5	3.7	10	
t_{PHZ}	$\overline{G}$	Y	3.2	6.6	8.2	3.2	9.6	3.2	9.1	ns
t_{PLZ}			3.4	6.5	8	3.4	12.3	3.4	10.7	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

- **State-of-the-Art BiCMOS Design Substantially Reduces Standby Current**
- **High-Impedance State During Power Up and Power Down**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include "Small Outline" Packages, and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

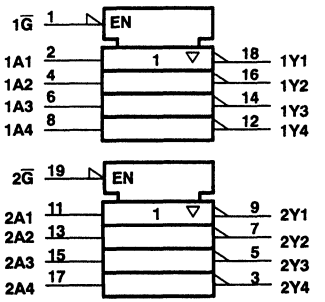
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT241 and 'BCT244, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

The SN64BCT240 is characterized for operation from −40°C to 85°C and 0°C to 70°C.

FUNCTION TABLE
(each buffer)

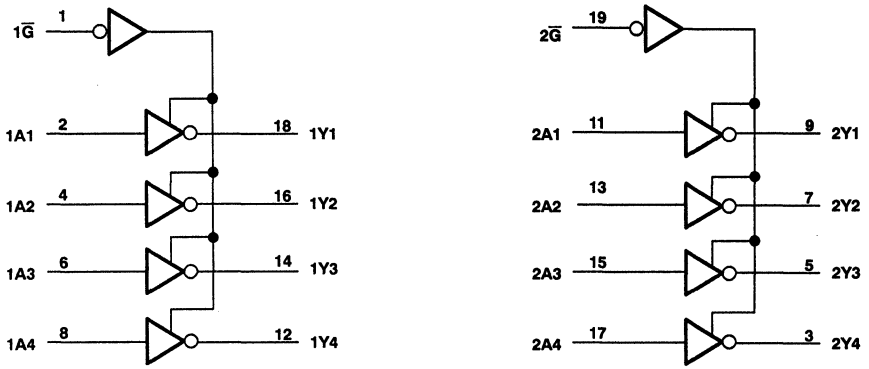
INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range (see Note 1) ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state ..... 128 mA
Operating free-air temperature range ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V		I_{OH} = −3 mA	2.4	3.3		V
			I_{OH} = −15 mA	2	3.1		
	V_{CC} = 4.75 V		I_{OH} = −3 mA	2.7			
V_{OL}	V_{CC} = 4.5 V		I_{OH} = 64 mA		0.42	0.55	V
I_{OZH}	V_{CC} = 0 V to 5.5 V,	V_O = 2.7 V				50	μA
I_{OZL}	V_{CC} = 0 V to 5.5 V,	V_O = 0.5 V				−50	μA
I_{OZ}	$\overline{G}$ at 0.8 V,	V_O = 2.7 V or 0.5 V	V_{CC} = 0V to 2.3 V (power up)			±50	μA
			V_{CC} = 1.8 V to 0 V (power down)			±50	μA
I_I	V_{CC} = 0 V to 5.5 V,	V_I = 5.5 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V				−1	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0V		−100		−225	μA
I_{CCL}	V_{CC} = 5.5 V				19	31	mA
I_{CCH}	V_{CC} = 5.5 V				46	71	mA
I_{CCZ}	V_{CC} = 5.5 V				6	9	mA
C_i	V_{CC} = 5.5 V,	V_I = 2.5 V or 0.5 V			6		pF
C_o	V_{CC} = 5.5 V,	V_O = 2.5 V or 0.5 V			11		pF

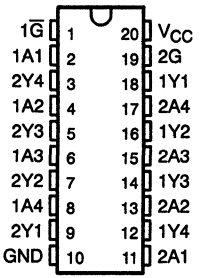
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω		V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω				UNIT
			T_A = 25°C		T_A = −40°C to 85°C		T_A = 0°C to 70°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	0.5	4.8	0.5	6.4	0.5	5.6	ns
t_{PHL}			0.4	3.5	0.4	4.5	0.4	4	
t_{PZH}	$\overline{G}$	Y	1	7.9	1	9.2	1	8.8	ns
t_{PZL}			1	9.4	1	10.8	1	10.5	
t_{PHZ}	$\overline{G}$	Y	1	6.8	1	8.5	1	8.1	ns
t_{PLZ}			1	8.1	1	10.6	1	9.5	

- **State-of-the-Art BiCMOS Design Substantially Reduces Standby Current**
- **High-Impedance State During Power Up and Power Down**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT240 and 'BCT244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output-enable) inputs, and complementary G and $\overline{G}$ inputs.

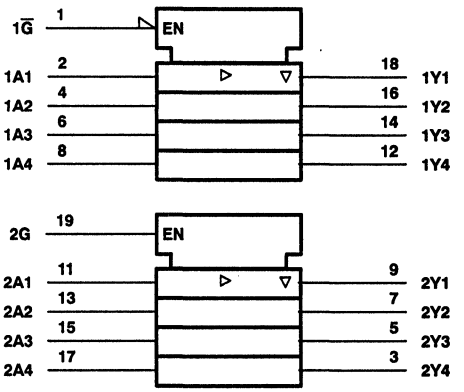
The SN64BCT241 is characterized for operation from −40°C to 85°C and 0°C to 70°C.

FUNCTION TABLES

INPUTS		OUTPUT
1$\overline{G}$	1A	1Y
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT
2G	2A	2Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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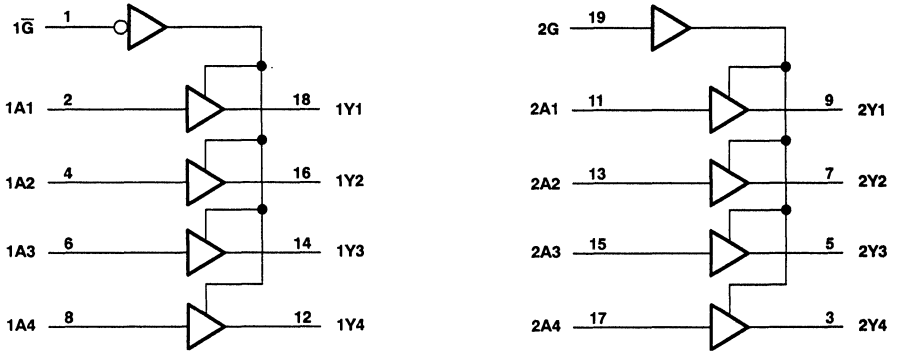
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state ..... 128 mA
Operating free-air temperature range ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}		V_{CC} = 4.5 V		I_{OH} = −3 mA	2.4	3.3		V
				I_{OH} = −15 mA	2	3.1		
		V_{CC} = 4.75 V		I_{OH} = −3 mA	2.7			
V_{OL}		V_{CC} = 4.5 V		I_{OH} = 64 mA		0.42	0.55	V
I_{OZH}		V_{CC} = 0 V to 5.5 V,	V_O = 2.7 V				50	mA
I_{OZL}		V_{CC} = 0 V to 5.5 V,	V_O = 0.5 V				−50	μA
I_{OZ}		$\overline{G}$ at 0.8 V,	V_O = 2.7 V or 0.5 V	V_{CC} = 0 V to 2.3 V (power up)			±50	μA
				V_{CC} = 1.8 V to 0 V (power down)			±50	
I_I		V_{CC} = 0 V to 5.5 V,	V_I = 5.5 V				0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V				20	μA
I_{IL}	G or $\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.5 V				−1	mA
	Any A						−1.6	mA
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0		−100		−225	mA
I_{CCL}		V_{CC} = 5.5 V				23	43	mA
I_{CCH}		V_{CC} = 5.5 V				53	85	mA
I_{CCZ}		V_{CC} = 5.5 V				4	10	mA
C_i		V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V			6		pF
C_o		V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V			11		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

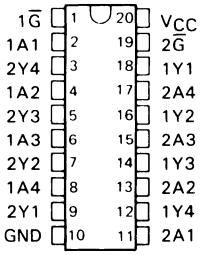
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF R1 = 500 Ω, R2 = 500 Ω, T_A = MIN TO MAX†				UNIT
			'BCT241		T_A = −40°C to 85°C		T_A = 0°C to 70°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	0.5	4.5	0.5	5.2	0.5	4.9	ns
t_{PHL}			1	5.4	1	6.3	1	5.9	
t_{PZH}	$\overline{G}$ or G	Y	1	7.8	1	9.1	1	8.7	ns
t_{PZL}			1	8.6	1	10	1	9.4	
t_{PHZ}	$\overline{G}$ or G	Y	1	6.8	1	8.4	1	8.1	ns
t_{PLZ}			1	8.1	1	11	1	9.9	

SCBS027—TI0208—D3249, FEBRUARY 1989—REVISED AUGUST 1989

- **3-State True Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Impedance State During Power Up and Power Down**
- **P-N-P Inputs Reduce DC Loading**
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT240 and 'BCT241, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

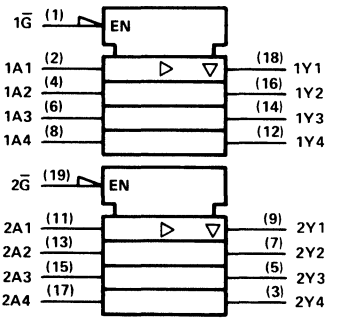
The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

The SN64BCT244 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

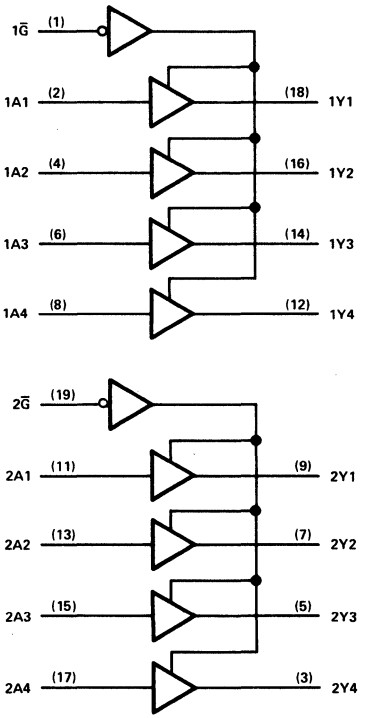
OUTPUT CONTROL	DATA INPUT	OUTPUT
$1\overline{G}$, $2\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage	−0.5 V to 7 V
Voltage applied to any output in the disbled or power-off state	−0.5 V to 5.5 V
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Current into any output in the low state	128 mA
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		V
		I_{OH} = −15 mA	2	3.1		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 64 mA		0.42	0.55	V
I_I	V_{CC} = 5.5 V, V_I = 5.5 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V				−1	mA
I_{OZH}	V_{CC} = 0 V to 5.5 V, V_O = 2.7 V				50	μA
I_{OZL}	V_{CC} = 0 V to 5.5 V, V_O = 0.5 V				−50	μA
I_{OZ}	$\overline{G}$ at 0.8 V, V_O = 2.7 V or 0.5 V	V_{CC} = 0 V to 2.3 V (power up)			±50	μA
		V_{CC} = 1.8 V to 0 V (power down)			±50	
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−100		−225	mA
I_{CCH}	V_{CC} = 5.5 V	Outputs high		23	40	mA
I_{CCL}		Outputs low		53	80	mA
I_{CCS}		Outputs disabled		4	10	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

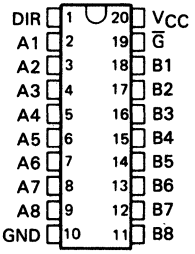
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN TO MAX§		UNIT
			'BCT244			SN64BCT244		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	1.2	2.5	4.4	0.9	5.3	ns
t_{PHL}			1.7	3.2	5	1.4	6	
t_{PZH}	$\overline{G}$	Y	2	5.7	7.8	2	9	ns
t_{PZL}			2	5.9	8.1	2	9.4	
t_{PHZ}	$\overline{G}$	Y	2	5.4	6.7	2	8	ns
t_{PLZ}			2	6.1	7.6	2	9.8	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

- **BiCMOS Design Substantially Reduces Standby Current**
- **3-State True Outputs Drive Bus Lines Directly**
- **High-Impedance State During Power Up and Power Down**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous communication between data buses. Implementing the control function minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can disable the device so that the buses are effectively isolated.

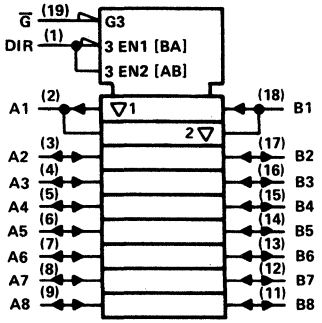
The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

The SN64BCT245 is characterized for operation from −40°C to 85°C and 0°C to 70°C.

FUNCTION TABLE

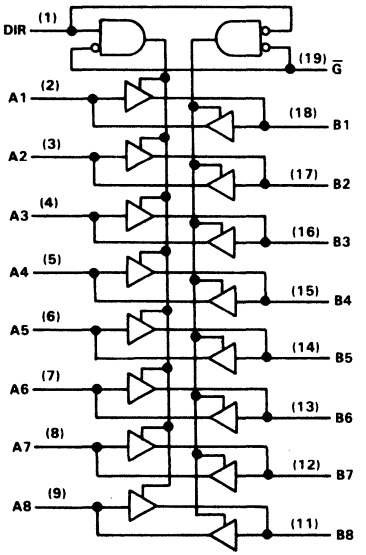
ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range (see Note 1) ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state ..... 128 mA
Operating free-air temperature range: ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	A1–A8			−3	mA
		B1–B8			−15	mA
I_{OL}	Low-level output current	A1–A8			24	mA
		B1–B8			64	mA
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,		I_{IK} = −18 mA			−1.2	V
V_{OH}	Any A	V_{CC} = 4.5 V		I_{OH} = −1 mA	2.5	3.4		V
	Any B			I_{OH} = −3 mA	2.4	3.3		
				I_{OH} = −15 mA	2	3.1		
V_{OL}	Any A	V_{CC} = 4.5 V		I_{OL} = 24 mA		0.35	0.5	V
	Any B			I_{OL} = 64 mA		0.42	0.55	
I_{OZ}	Power up	$\overline{G}$ at 0.8 V,	V_{CC} = 0 to 2.3 V	V_O = 2.7 V			70	μA
				V_O = 0.5 V			−0.65	mA
	Power down	$\overline{G}$ at 0.8 V,	V_{CC} = 2 V to 0	V_O = 2.7 V			70	μA
				V_O = 0.5 V			−0.65	mA
I_I‡	A and B	V_{CC} = 0 V to 5.5 V,		V_I = 5.5 V			1	mA
	DIR and $\overline{G}$	V_{CC} = 0 V to 5.5 V,		V_I = 5.5 V			0.1	
I_{IH}‡	A and B	V_{CC} = 5.5 V,		V_I = 2.7 V			70	μA
	DIR and $\overline{G}$						20	
I_{IL}	A and B	V_{CC} = 5.5 V,		V_I = 0.5 V			−0.65	mA
	DIR and $\overline{G}$						−1.2	
I_{OS}§	Any A	V_{CC} = 5.5 V,		V_O = 0	−60		−150	mA
	Any B				−100		−225	
I_{CCH}		V_{CC} = 5.5 V,		See Note 2		36	57	mA
I_{CCL}		V_{CC} = 5.5 V,		See Note 2		57	90	
I_{CCZ}		V_{CC} = 5.5 V				10	15	
C_{in}	$\overline{G}$ and DIR	V_{CC} = 5 V,		V_I = 2.5 V or 0.5 V		7		pF
C_{IO}	A to B					9		
C_{IO}	B to A					12		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: I_{CCH} and I_{CCL} are measured in the A to B mode.

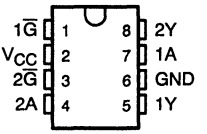
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω,				UNIT
					T_A = 40°C to 85°C		T_A = 0°C to 70°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	6	1	7.2	1	7	ns
t_{PHL}			1.5	6.6	1.5	7.6	1.5	7	
t_{PZH}	$\overline{G}$	A or B	1.5	9.4	1.5	11.2	1.5	10.9	ns
t_{PZL}			1.5	10.2	1.5	11.8	1.5	11.6	
t_{PHZ}	$\overline{G}$	A or B	1.5	8.3	1.5	9.7	1.5	9.3	ns
t_{PLZ}			1.5	7.8	1.5	9.6	1.5	9.1	

SCBS048—TI0210—D3488, MARCH 1990

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Impedance State During Power Up and Power Down**
- **P-N-P Inputs Reduce DC Loading**
- **State-of-the-Art BiCMOS Design Substantially Reduces Standby Current**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015**
- **Package Options Include "Small Outline" Packages, and Standard Plastic DIPs**

D OR P PACKAGE
(TOP VIEW)



description

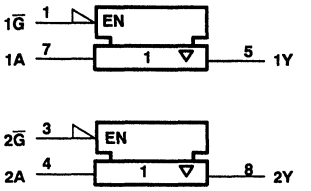
These dual buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN64BCT306 is characterized for operation from −40°C to 85°C and 0°C to 70°C.

FUNCTION TABLE

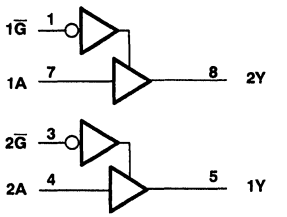
OUTPUT ENABLE $\overline{G}$	DATA INPUT A	OUTPUT Y
H	X	Z
L	L	L
L	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state ..... 128 mA
Operating free-air temperature range ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA					−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA		2.4	3.3		V
		I_{OH} = −15 mA		2	3.1		
V_{OL}	V_{CC} = 4.5 V	I_{OH} = 64 mA			0.42	0.55	V
I_{OZH}	V_{CC} = 0 V to 5.5 V, V_O = 2.7 V					50	mA
I_{OZL}	V_{CC} = 0 V to 5.5 V, V_O = 0.5 V					−50	μA
I_{OZ}	$\overline{G}$ at 0.8 V, V_O = 2.7 V or 0.5 V	V_{CC} = 0 V to 2.3 V (power up)				±50	μA
		V_{CC} = 1.8 V to 0 V (power down)				±50	μA
I_I	V_{CC} = 0 V to 5.5 V, V_I = 5.5 V					0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V					20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V					−1	mA
I_{OS}§	V_{CC} = 5.5 V, V_O = 0 V			−100		−225	mA
I_{CCL}	V_{CC} = 5.5 V				53	80	mA
I_{CCH}	V_{CC} = 5.5 V				23	40	mA
I_{CCZ}	V_{CC} = 5.5 V				4	10	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

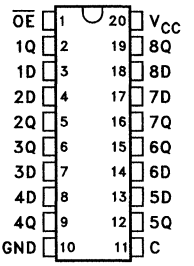
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω		V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω				UNIT
			T_A = 25°C		T_A = −40°C to 85°C		T_A = 0°C to 70°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.2	4.4	0.9	5.3	0.7	5	ns
t_{PHL}			1.7	5	1.4	6	1.4	5.5	
t_{PZH}	$\overline{G}$	Y	2	7.8	2	9	2	8.7	ns
t_{PZL}			2	8.1	2	9.4	2	8.9	
t_{PHZ}	$\overline{G}$	Y	2	6.7	2	8	2	7.7	ns
t_{PLZ}			2	7.6	2	9.8	2	8.9	

TI0290—D3251, JUNE 1990

PRODUCT PREVIEW

- **8-Latches in a Single Package**
- **Full Parallel Access for Loading**
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CC}**
- **3-State True Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Impedance State During Power Up and Power Down**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

These octal latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

The eight latches of the 'BCT373 are transparent D-type latches. While the enable (C) is high, the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface components.

The output enable ($\overline{OE}$) does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

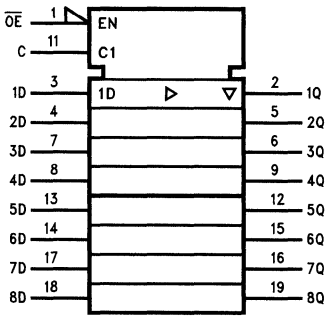
The outputs are in a high-impedance state during power up and power down when the supply voltage is less than approximately 3 V.

The SN64BCT373 is characterized for operation from −40°C to 85°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

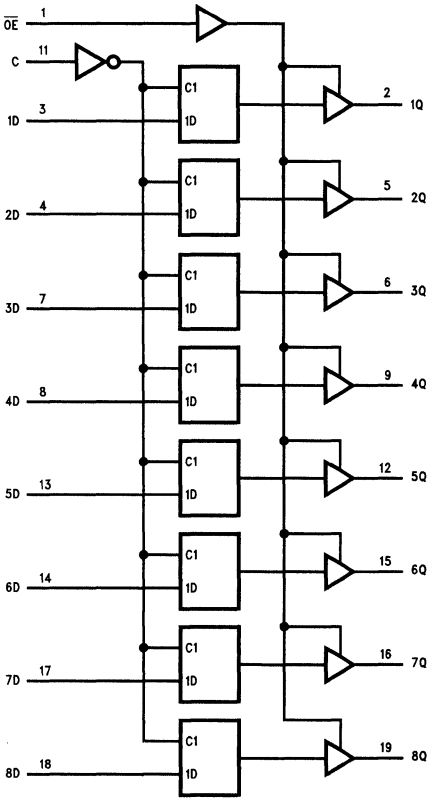
TI0290—D3251, JUNE 1990

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, (see Note 1)	−0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	−0.5 V to 7 V
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Input clamp current	−30 mA
Current into any output in the low state	128 mA
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V		I_{OH} = −3 mA	2.4	3.3		V
			I_{OH} = −15 mA	2	3.1		
V_{OL}	V_{CC} = 4.5 V		I_{OL} = 64 mA		0.42	0.55	V
V_{OZH}	V_{CC} = 0 to 5.5 V,	V_O = 2.7 V				50	μA
V_{OZL}	V_{CC} = 0 to 5.5 V,	V_O = 0.5 V				−50	μA
I_{OZ}	$\overline{OE}$ at 0.8 V,	V_{CC} = 0 to 2.35 V (power up)				±50	μA
	V_O = 2.7 V or 0.5 V	V_{CC} = 2 V to 0 (power down)				±50	
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V				0.4	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V				−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0		−100		−225	mA
I_{CCL}	V_{CC} = 5.5 V				37	60	mA
I_{CCH}	V_{CC} = 5.5 V				2	5	mA
I_{CCZ}	V_{CC} = 5.5 V				5	8	mA
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V			6		pF
C_o	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V			11		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

timing requirements

		V_{CC} = 5 V, T_A = 25°C	V = 4.5 V to 5.5 V				UNIT
		'BCT373	T_A = −40°C to 85°C		T_A = 0°C to 70°C		
		MIN MAX	MIN	MAX	MIN	MAX	
t_{su}	Setup time, data before enable C ↓	2	2		2		ns
t_h	Hold time, data after enable C ↓	5.5	5.5		5.5		ns
t_w	Pulse duration, enable C high	7.5	7.5		7.5		ns

switching characteristics (see Figure 1)

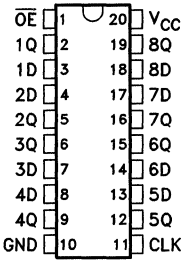
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω				UNIT
			'BCT373			T_A = −40°C to 85°C		T_A = 0°C to 70°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Any Q	2	5.9	7.7	1.5	10.1	2	9.3	ns
t_{PHL}			2	6.7	8.5	1	10.3	1.5	9.5	
t_{PLH}	C	Any Q	2	6.2	8.2	2	10.1	2	9.3	ns
t_{PHL}			2	5.9	7.8	2	9.2	2	8.8	
t_{PZH}	$\overline{OE}$	Any Q	1	7.8	9.6	1	12.3	1	11.8	ns
t_{PZL}			1	8.2	10.2	1	12.5	1	12	
t_{PHZ}	$\overline{OE}$	Any Q	1	4.9	6.6	1	7.4	1	7	ns
t_{PLZ}			1	5	6.7	1	8.1	1	7.4	

SN64BCT374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

TI0256—JUNE 1990

- **8 D-Type Flip-Flops in a Single Package**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CC}**
- **3-State True Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Impedance State During Power Up and Power Down**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C Method 3015**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
L	H	X	Q_0
L	↓	X	X_0
H	X	X	Z

description

These octal flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'BCT374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels that were set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive bus lines without need for interface or pull up components.

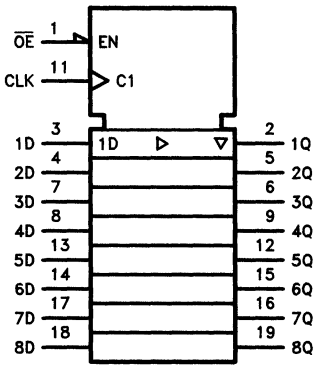
The output-enable ($\overline{OE}$) does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs are in a high-impedance state during power up and power down when the supply voltage is less than approximately 3 V.

The SN64BCT374 is characterized for operation from −40°C to 85°C and 0°C to 70°C.

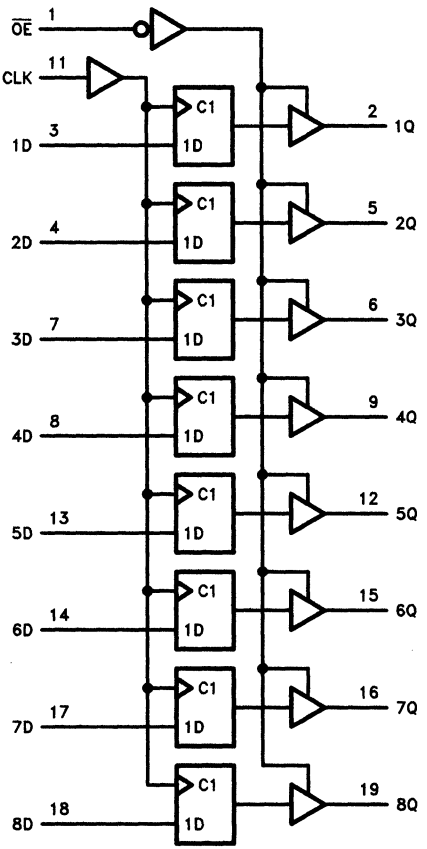
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage (see Note 1)	−0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	−0.5 V to 5.5 V
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Input clamp current	−30 mA
Current into any output in the low state	128 mA
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input-clamp-current rating is observed.

PRODUCT PREVIEW

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		V
		I_{OH} = −15 mA	2	3.1		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 64 mA		0.42	0.55	V
I_{OZH}	V_{CC} = 0 V to 5.5 V, V_O = 2.7 V				50	μA
I_{OZL}	V_{CC} = 0 V to 5.5 V, V_O = 0.5 V				−50	μA
I_{OZ}	$\overline{OE}$ at 0.8 V,	V_{CC} = 0 V to 2.35 V (power up)			±50	μA
	V_O = 2.7 V or 0.5 V	V_{CC} = 2 V to 0 V (power down)			±50	
I_I	V_{CC} = 5.5 V, V_I = 5.5 V				0.4	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V				−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0 V		−100		−225	mA
I_{CCL}	V_{CC} = 5.5 V			37	60	mA
I_{CCH}	V_{CC} = 5.5 V			2	5	mA
I_{CCZ}	V_{CC} = 5.5 V			5	8	mA
C_i	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			6		pF
C_o	V_{CC} = 5 V, V_O = 2.5 V or 0.5 V			10		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

timing requirements

		V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V				UNIT
		'BCT374		T_A = −40°C to 85°C		T_A = 0°C to 70°C		
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		70		70		70	MHz
t_{su}	Setup time, Data before CLK↑	6.5		6.5		6.5		ns
t_h	Hold time, Data before CLK↑	0		0		0		ns
t_w	Pulse duration, CLK high	7		8		7		ns

switching characteristics (see Figure 1)

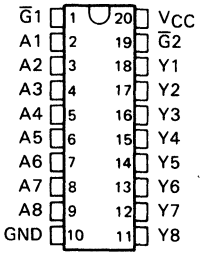
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω				UNIT
			'BCT374			T_A = −40°C to 85°C		T_A = 0°C to 70°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			70			70		70		MHz
t_{PLH}	CLK	Q	2	7.2	9.1	2	11.6	2	10.6	ns
t_{PHL}			2	7.1	8.8	2	10.6	2	10	
t_{PZH}	$\overline{OE}$	Q	1	8.3	10.1	1	12.7	1	12.3	ns
t_{PZL}			1	8.6	10.6	1	13	1	12.7	
t_{PHZ}	$\overline{OE}$	Q	1	4.7	6.3	1	7.1	1	6.8	ns
t_{PLZ}			1	4.8	6.3	1	7.5	1	6.8	

SCBS031—TI0211—D3254, FEBRUARY 1989

PRODUCT PREVIEW

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State True Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Impedance State During Power Up and Power Down**
- **P-N-P Inputs Reduce DC Loading**
- **Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed to have the performance of the popular SN64BCT240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed-circuit-board layout.

The three-state control gate is a 2-input AND gate with active-low inputs so that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

The outputs are in the high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

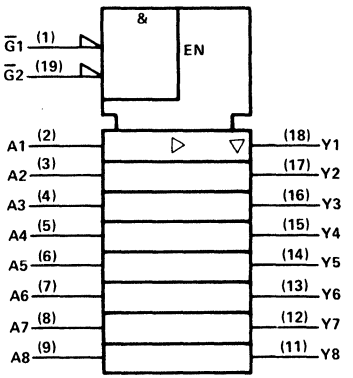
The SN64BCT541 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Z = High Impedance

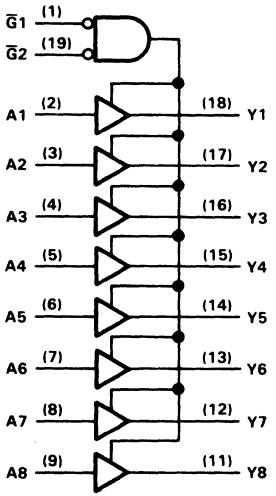
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state ..... 128 mA
Operating free-air temperature range ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA					−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA		2.4	3.3		V
		I_{OH} = −15 mA		2	3.1		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 64 mA			0.42	0.55	V
I_{OZH}	V_{CC} = 0 V to 5.5 V, V_O = 2.7 V					50	μA
I_{OZL}	V_{CC} = 0 V to 5.5 V, V_O = 0.5 V					−50	μA
I_{OZ}	$\overline{G}$ at 0.8 V,	V_{CC} = 0 V to 2.35 V (power up)				±50	μA
	V_O = 2.7 V or 0.5 V	V_{CC} = 2 V to 0 (power down)				±50	
I_I	V_{CC} = 5.5 V, V_I = 7 V					0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V					20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V					−0.6	mA
I_{OS}§	V_{CC} = 5.5 V, V_O = 0			−100		−225	mA
I_{CCL}	V_{CC} = 5.5 V				47	72	mA
I_{CCH}	V_{CC} = 5.5 V				27	40	mA
I_{CCZ}	V_{CC} = 5.5 V				5	7	mA
C_i	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V				5		pF
C_o	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V				10		

switching characteristics

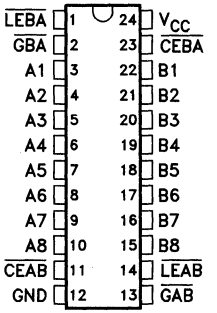
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	2.1	3.7	5.3	1.7	6.3	ns
t_{PHL}			3.7	5.5	7.5	3.2	8.7	
t_{PZH}	$\overline{G}$	Y	5.3	7.2	9.3	4.4	11	ns
t_{PZL}			6	8	10.4	5.4	12.4	
t_{PHZ}	$\overline{G}$	Y	3.5	5.6	7.6	3	9.1	ns
t_{PLZ}			3.4	5.2	7.2	3	9.4	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25° C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

PRODUCT PREVIEW

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **Package Options Include "Small-Outline" Packages and Standard 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN64BCT543 is a noninverting octal bus transceiver. It contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ and $\overline{LEBA}$) and output-enable ($\overline{GAB}$ and $\overline{GBA}$) inputs permit independent control for either direction of data flow.

When the A-to-B chip enable ($\overline{CEAB}$) is high, the latches are in storage mode and the B outputs are in the high-impedance state. When $\overline{CEAB}$ is low, latch characteristics and B-output functionality are controlled by $\overline{LEAB}$ and $\overline{GAB}$ as follows:

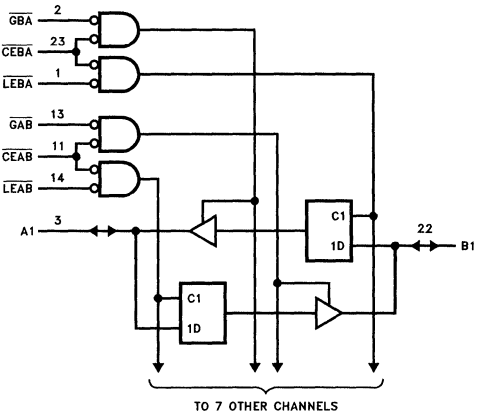
- when $\overline{LEAB}$ is low, the latches are transparent; taking $\overline{LEAB}$ high stores the data present at the A inputs.
- when $\overline{GAB}$ is low, the B outputs are active (high or low logic level) and reflect the data present in the A-to-B latches; when $\overline{GAB}$ is high, the B outputs are in the high-impedance state.

B-to-A data flow is controlled via the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$ inputs in a manner analogous to that described above for A-to-B data flow.

The SN64BCT543 featues power-up three-state circuitry for hot-card insertion applications.

The SN64BCT543 is characterized for operation from 0°C to 70°C and from −40°C to 125°C.

logic diagram (positive logic)

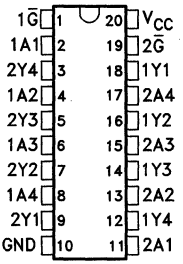


SN64BCT2240
OCTAL BUFFER/MOS DRIVERS WITH 3-STATE OUTPUTS

TI0225—D3527, JUNE 1990

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **Package Options Include "Small-Outline" Packages and Standard 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

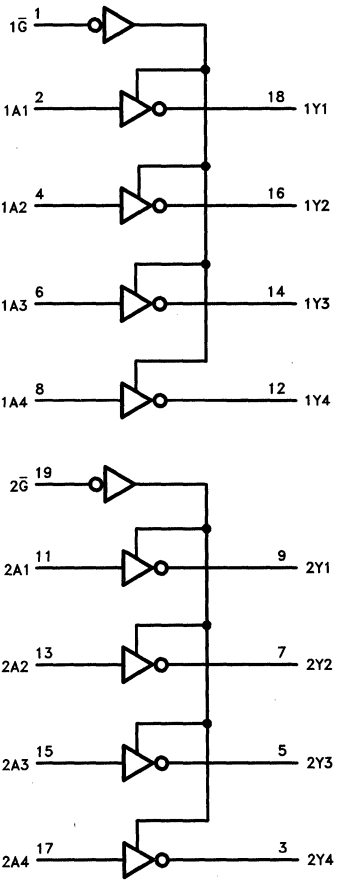
The SN64BCT2240 is an inverting octal buffer/MOS driver specifically designed to drive MOS DRAMs. The outputs, which are designed to source or sink up to 12 mA, include 33-Ω series resistors to reduce overshoot and undershoot.

When the output-enable inputs $1\overline{G}$ and $2\overline{G}$ are low, the Y outputs reflect the inverse of the data present at the A inputs. When $1\overline{G}$ and $2\overline{G}$ are high, the outputs are in the high-impedance state. Enable $1\overline{G}$ affects only the 1Y outputs; enable $2\overline{G}$ affects only the 2Y outputs.

The SN64BCT2240 features power-up three-state circuitry for hot-card insertion applications.

The SN64BCT2240 is characterized for operation from 0°C to 70°C and from −40°C to 125°C.

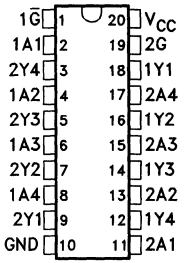
logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **Package Options Include "Small-Outline" Packages and Standard 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

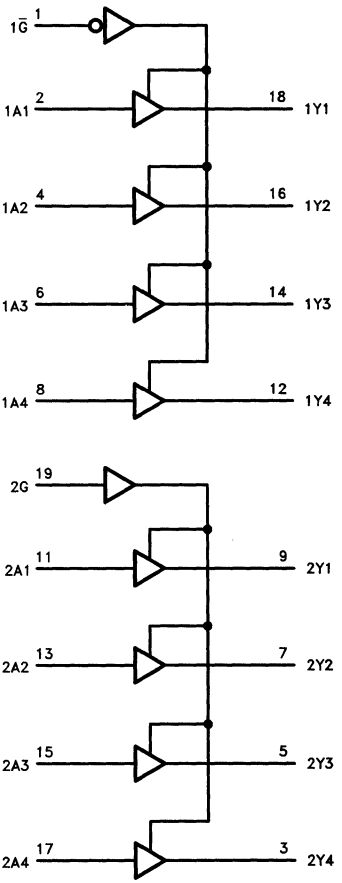
The SN64BCT2241 is a noninverting octal buffer/MOS driver specifically designed to drive MOS DRAMs. The outputs, which are designed to source or sink up to 12 mA, include 33-Ω series resistors to reduce overshoot and undershoot.

The SN64BCT2241 features complementary output-enable inputs $1\overline{G}$ and 2G. The 1Y outputs are active (high or low logic level) when active-low enable $1\overline{G}$ is low; when $1\overline{G}$ is high, the 1Y outputs are in the high-impedance state. The 2Y outputs are active when 2G is high and in the high-impedance state when 2G is low.

The SN64BCT2241 features power-up three-state circuitry for hot-card insertion applications.

The SN64BCT2241 is characterized for operation from 0°C to 70°C and from −40°C to 125°C.

logic diagram (positive logic)



PRODUCT PREVIEW

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **Package Options Include "Small-Outline" Packages and Standard 300-mil DIPs**

description

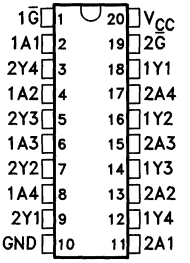
The SN64BCT2244 is a noninverting octal buffer/MOS driver specifically designed to drive MOS DRAMs. The outputs, which are designed to source or sink up to 12 mA, include 33-Ω series resistors to reduce overshoot and undershoot.

When the output-enable inputs $1\overline{G}$ and $2\overline{G}$ are low, the Y outputs reflect the data present at the A inputs. When $1\overline{G}$ and $2\overline{G}$ are high, the outputs are in the high-impedance state. Enable $1\overline{G}$ affects only the 1Y outputs; enable $2\overline{G}$ affects only the 2Y outputs.

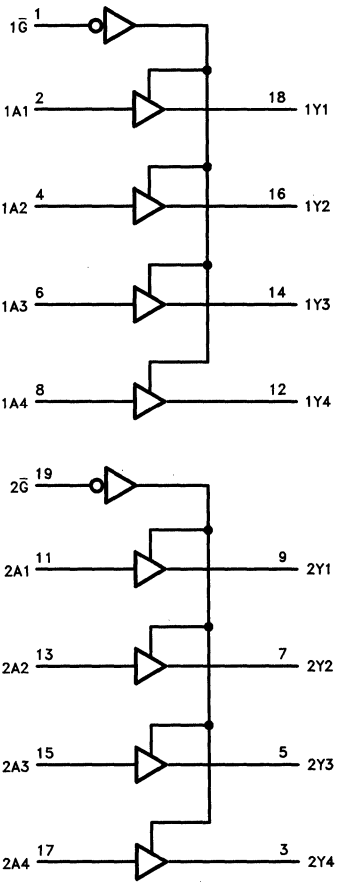
The SN64BCT2244 features power-up three-state circuitry for hot-card insertion applications.

The SN64BCT2244 is characterized for operation from 0°C to 70°C and from −40°C to 125°C.

DW OR N PACKAGE
(TOP VIEW)



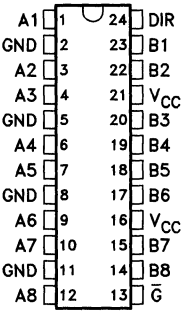
logic diagram (positive logic)



TI0278—D3587, JUNE 1990

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 25-Ω or Greater**
- **Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs**
- **Data Flow-Through Pinout (All inputs on Opposite Side From Outputs)**
- **High-Impedance State During Power Up and Power Down**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic "Small Outline" Packages, and Standard Plastic 300-mil DIPs**

DW or NT PACKAGE
(TOP VIEW)



description

These 25-Ω octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input $\overline{G}$ can be used to disable the device so the buses are effectively isolated.

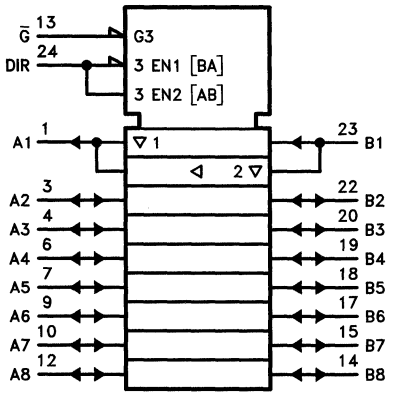
These transceivers are capable of sinking 188 mA of I_{OL} current through the A port, which facilitates switching 25-Ω transmission lines on the incident wave. They are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers. The distributed V_{CC} and GND pins minimize the noise generated by the simultaneous switching of the outputs.

The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V. The SN64BCT25245 is characterized for operation from −40°C to 85°C and 0°C to 70°C.

FUNCTION TABLE, EACH SECTION

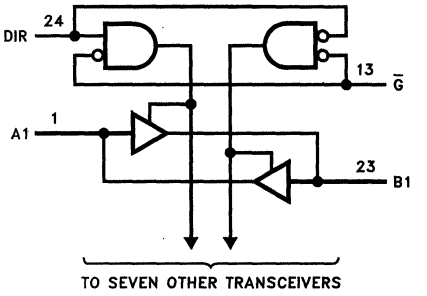
ENABLE INPUTS		OPERATION
$\overline{G}$	DIR	'64BCT25245
L	L	B Data To A Bus
L	H	A Data To B Bus
H	X	Bus Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage: Control Inputs (see Note 1)	−0.5 V to 7 V
I/O ports (see Note 1)	−0.5 V to 5.5 V
Voltage applied to any output in the disabled or power-off state	−0.5 V to 7 V
Voltage applied to any output in the high state (B Port)	−0.5 V to V_{CC}
Input clamp current	−30 mA
Current into any output in the low state: A Port	376 mA
B Port	48 mA
Operating free-air temperature range:	−55°C to 125°C
	−40°C to 85°C
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

TI0278—D3587, JUNE 1990

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	A1-A8			−80	mA
		B1-B8			−3	mA
I_{OL}	Low-level output current	A1-A8			188	mA
		B1-B8			24	mA
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2	V
V_{OH}	Any A	V_{CC} = 4.75 V, I_{OH} = −3 mA		2.7			V
		V_{CC} = 4.5 V, I_{OH} = −80 mA		2			
	Any B	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.4	3.3		
V_{OL}	Any A	V_{CC} = 4.5 V, I_{OL} = 94 mA			0.42	0.55	V
		V_{CC} = 4.5 V, I_{OL} = 188 mA				0.7	
	Any B	V_{CC} = 4.5 V, I_{OL} = 24 mA			0.35	0.5	
I_{OZ}	Power Up	$\overline{G}$ at 0.8 V, V_{CC} = 0 to 2.3 V	V_O = 2.7 V			70	µA
			V_O = 0.5 V			−0.6	mA
	Power Down	$\overline{G}$ at 0.8 V, V_{CC} = 0 to 2 V	V_O = 2.7 V			70	µA
			V_O = 0.5 V			−0.6	mA
I_I	A and B	V_{CC} = 0 to 5.5 V, V_I = 5.5 V				0.25	mA
	DIR and $\overline{G}$	V_{CC} = 0 to 5.5 V, V_I = 5.5 V				0.1	
I_{IH}‡	A and B	V_{CC} = 5.5 V, V_I = 2.7 V				70	µA
	DIR and $\overline{G}$	V_{CC} = 5.5 V, V_I = 2.7 V				20	
I_{IL}‡	A and B	V_{CC} = 5.5 V, V_I = 0.5 V				−0.6	mA
	DIR and $\overline{G}$	V_{CC} = 5.5 V, V_I = 0.5 V				−0.6	
I_{OS}§	B port only¶	V_{CC} = 5.5 V, V_O = 0 V				−150	mA
I_{CCL}	A to B	V_{CC} = 5.5 V			48	60	mA
I_{CCH}					36	46	
I_{CCL}	B to A	V_{CC} = 5.5 V			95	115	mA
I_{CCH}					63	77	mA
I_{CCZ}		V_{CC} = 5.5 V			12	16	mA
C_{in}	$\overline{G}$ and DIR	V_{CC} = 5.5 V, V_I = 2.5 V or 0.5 V			8		pF
C_{io}	A port	V_{CC} = 5.5 V, V_I = 2.5 V or 0.5 V			18		pF
C_{io}	B port				8		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed 10 ms.
¶ Testing for this parameter on the A port is not recommended.

switching characteristics (see Note 2), (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω,				UNIT
			'64BCT25245			T_A = −40°C to 85°C		T_A = 0°C to 70°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.2	3.3	5.1	1.2	5.7	1.2	5.7	ns
t_{PHL}			1.9	4.3	6.7	1.9	7.3	1.9	7.2	
t_{PLH}	B	A	1.2	3.3	4.8	1.2	5.5	1.2	5.5	ns
t_{PHL}			2.1	4	5.6	2.1	6.3	2.1	6.2	
t_{PZH}	$\overline{G}$	A	3.7	6.3	8.4	3.7	9.7	3.7	9.6	ns
t_{PZL}			4.5	7.4	9.2	4.5	10.6	4.5	10.3	
t_{PHZ}	$\overline{G}$	A	1.8	3.7	5.5	1.8	6.2	1.8	6.2	ns
t_{PLZ}			3.3	5.1	7.2	3.3	8.8	3.3	8.3	
t_{PZH}	$\overline{G}$	B	3.4	5.7	7.9	3.4	8.9	3.4	8.9	ns
t_{PZL}			4.3	6.6	8.7	4.3	9.9	4.3	9.7	
t_{PHZ}	$\overline{G}$	B	2.7	4.5	6.3	2.7	6.9	2.7	6.9	ns
t_{PLZ}			1.7	4.5	6.8	1.7	7.7	1.7	7.5	

NOTE 2: For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

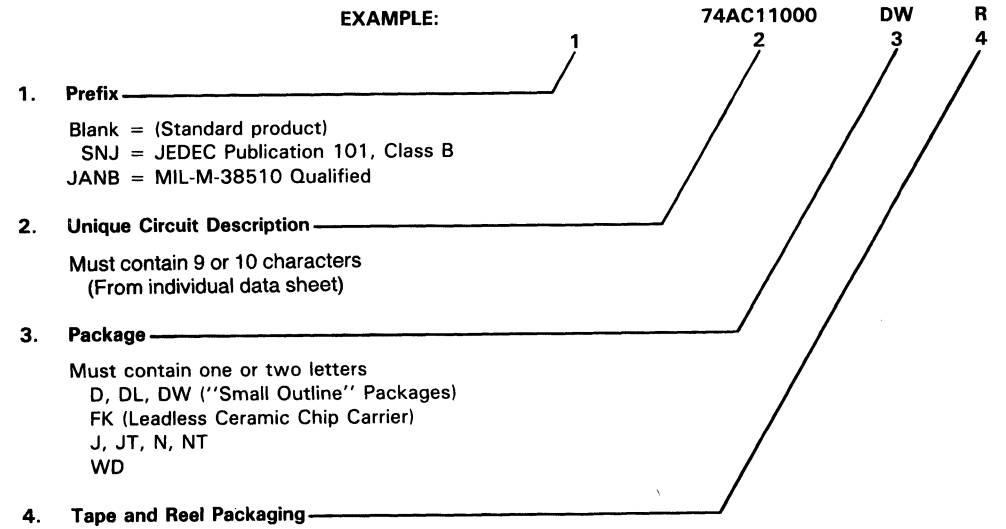
PACKAGE DIAGRAM OUTLINE INDEX

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.



1. **Prefix**

   Blank = (Standard product)
   SNJ = JEDEC Publication 101, Class B
   JANB = MIL-M-38510 Qualified

2. **Unique Circuit Description**

   Must contain 9 or 10 characters
   (From individual data sheet)

3. **Package**

   Must contain one or two letters
   D, DL, DW ("Small Outline" Packages)
   FK (Leadless Ceramic Chip Carrier)
   J, JT, N, NT
   WD

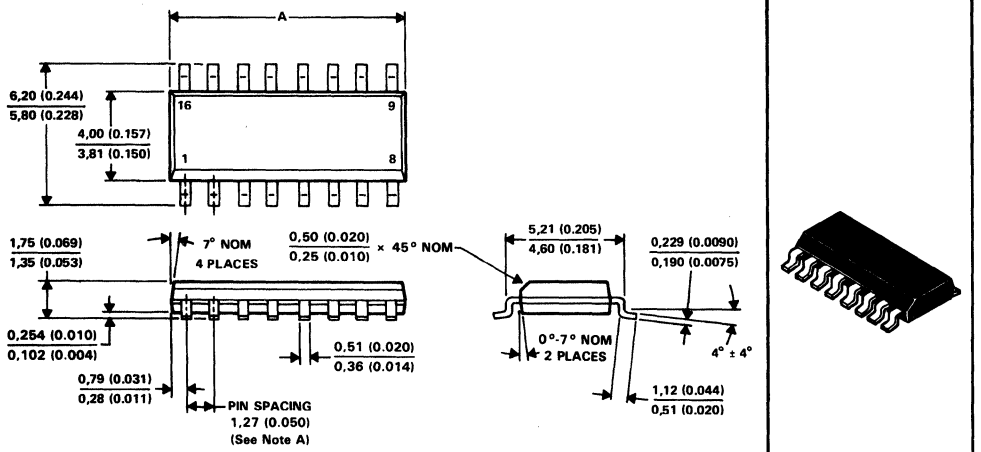
4. **Tape and Reel Packaging**

   Must be designated by the letter R and valid for surface mount packages only.
   All orders for tape and reel must be for whole reels.

D008, D014 and D016 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008, D014, and D016
(16-pin package used for illustration)



DIM \ PINS	8	14	16
A MIN	4,80 (0.189)	8,55 (0.337)	9,80 (0.386)
A MAX	5,00 (0.197)	8,74 (0.344)	10,00 (0.394)

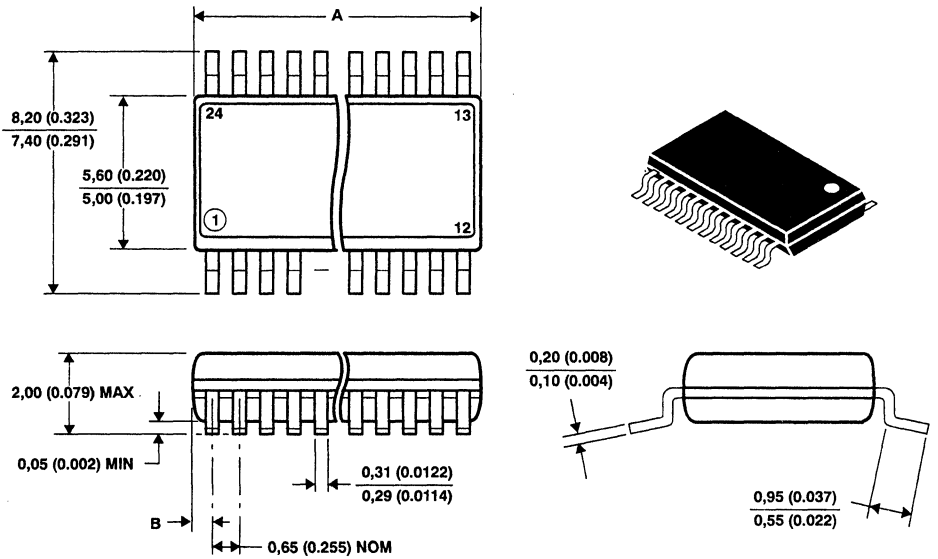
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,125 (0.005) radius of true position at maximum material dimension.
B. Lead tips to be planar within ±0,051 (0.002).
C. Body dimensions do not include mold flash or protrusion.
D. Mold protrusion shall not exceed 0,15 (0.006).
E. Interlead flash shall be controlled by TI Statistical Process Control (Additional information is available through TI field offices).

DB020 and DB024 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DB020 and DB024
(24-pin package used for illustration)



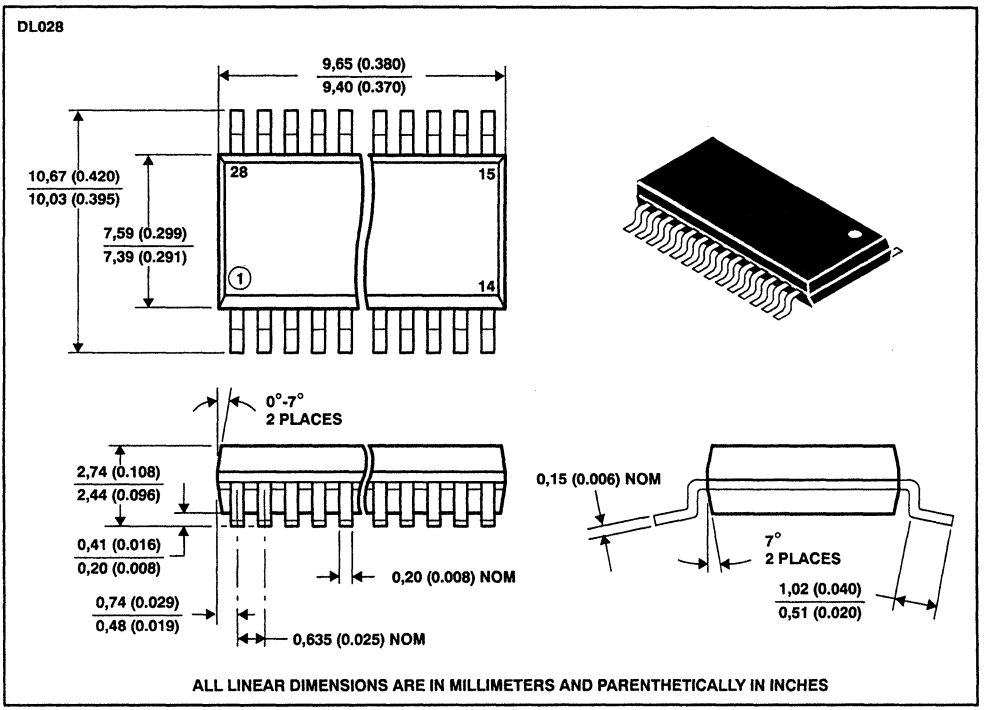
DIM \ PINS	20	24
A MIN	6,90 (0.272)	7,90 (0.311)
A MAX	7,50 (0.295)	8,50 (0.335)
B MAX	0,83 (0.033)	0,68 (0.027)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold protrusion does not exceed 0,15 (0.006).
C. Interlead flash is controlled by TI statistical process control (additional information available through TI field office).
D. Lead tips are planar within ±0,05 (0.002).

DL028 plastic "small outline" package

This "small outline" package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

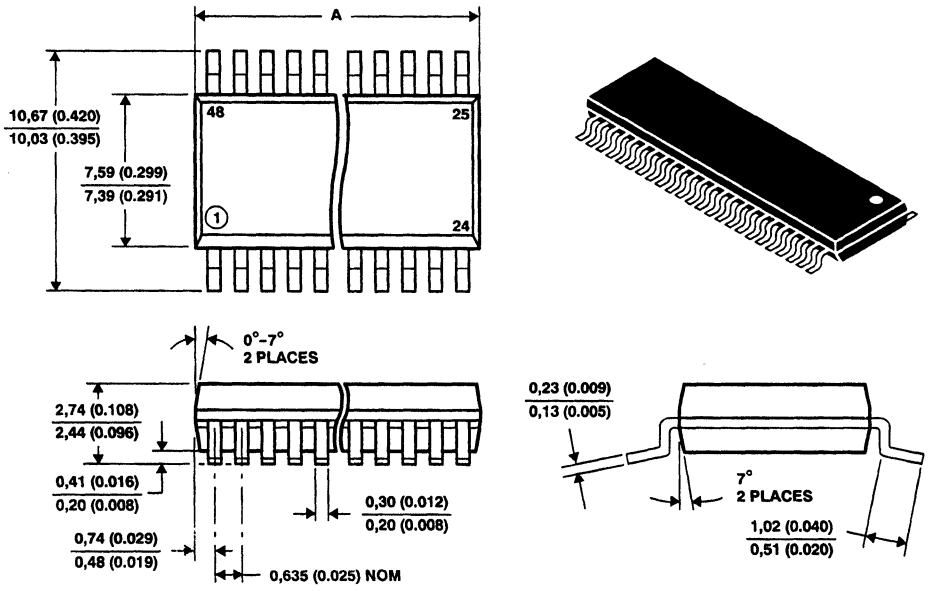


NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold protrusion does not exceed 0,15 (0.006).
C. Interlead flash is controlled by TI statistical process control (additional information available through TI field office).
D. Lead tips are planar within ±0,05 (0.002).

DL048 and DL056 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DL048 and DL056
(48-pin package used for illustration)



DIM \ PINS	48	56
A MIN	15,75 (0.620)	18,29 (0.720)
A MAX	16,00 (0.630)	18,54 (0.730)

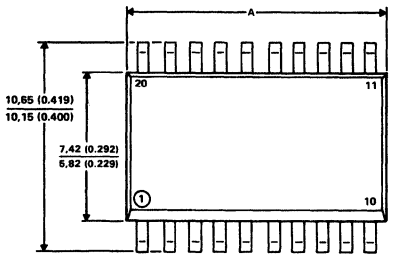
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

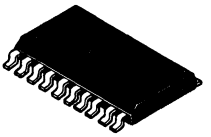
NOTES: A. Body dimensions do not include mold flash or protrusion.
B. End protrusion shall not exceed 0,15 (0.006).
C. Interlead flash shall be controlled by TI Statistical Process Control (Additional information is available through TI field offices).
D. Lead tips to be planar within ±0,05 (0.002).

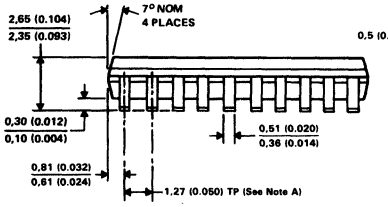
DW020, DW024, and DW028 plastic "small outline" packages

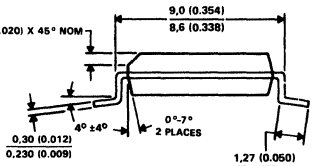
Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW020
DW024
DW028
(20-pin package used for illustration)









PINS / DIM	16	20	244	28
A MIN	10,16 (0.400)	12,70 (0.500)	15,24 (0.600)	17,78 (0.700)
A MAX	10,41 (0.410)	12,95 (0.510)	15,49 (0.610)	18,03 (0.710)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

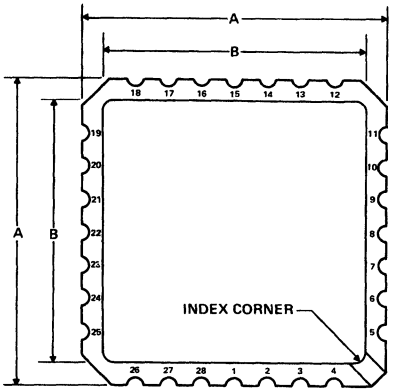
NOTES: A. Leads are within 0,125 (0.005) radius of true position at maximum material dimension.
B. Lead tips to be planar within ±0,051 (0.002).
C. Body dimensions do not include mold flash or protrusion.
D. Mold protrusion shall not exceed 0,15 (0.006).
E. Interlead flash shall be controlled by TI Statistical Process Control (Additional information is available through TI field offices).

FK020 and FK028 ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

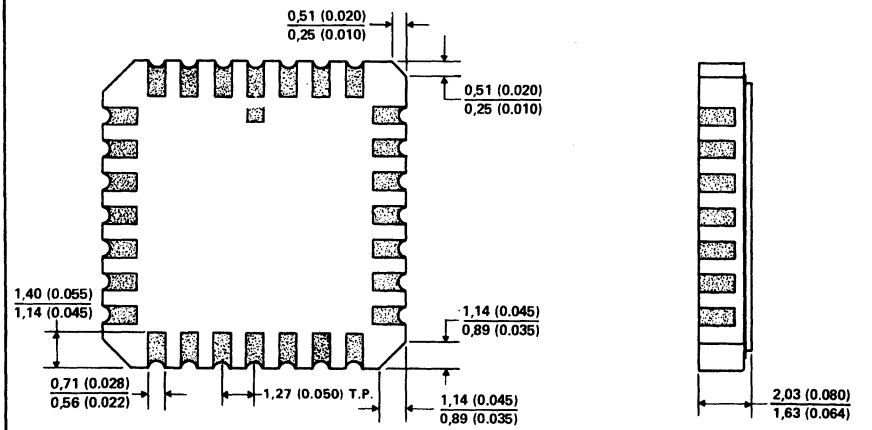
FK020 and FK028
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)

*All dimensions and notes for the specified JEDEC outline apply.

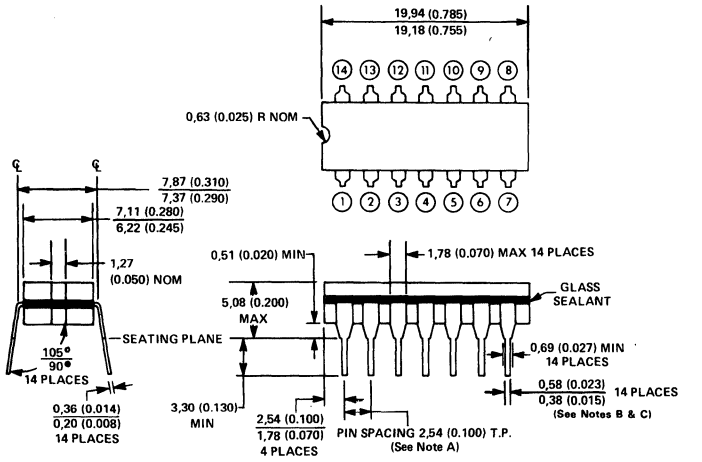


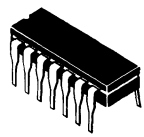
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

J014 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

J014





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

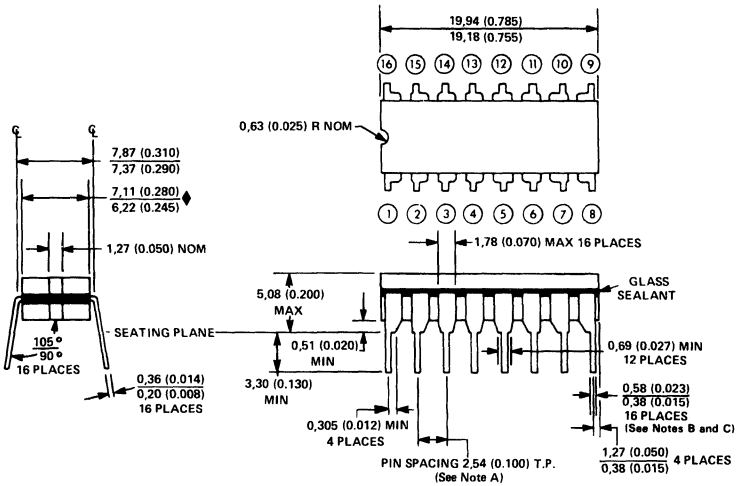
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

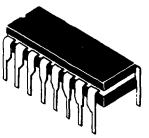
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J016 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

J016





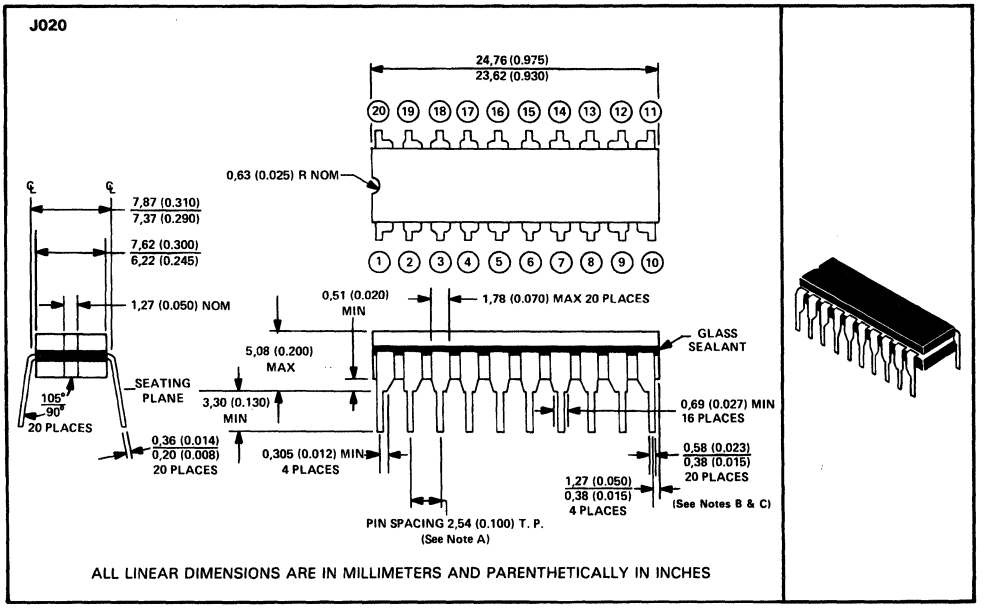
♦ For memories of 64 bits and up, a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, and complex HCMOS parts, this maximum is 7,62 (0.300). All other dimensions apply without modification.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J020 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

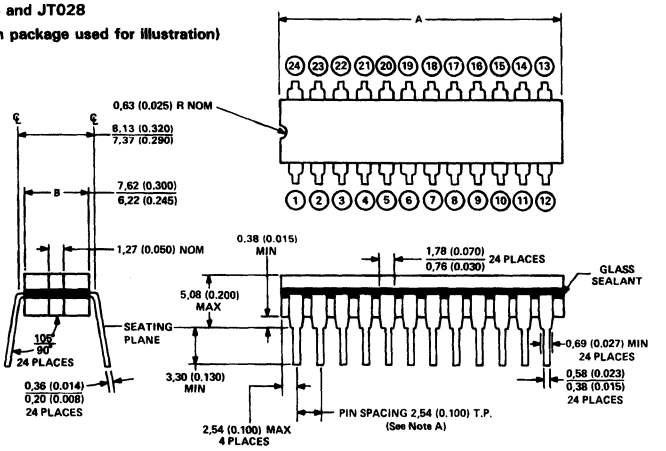


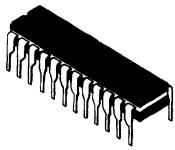
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

JT024 and JT028 ceramic dual-in-line packages

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the pins are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") pins require no additional cleaning or processing when used in soldered assembly.

JT024 and JT028
(24-pin package used for illustration)





DIM \ PINS	24	28
A MIN	31,50 (1.240)	36,58 (1.440)
A MAX	32,51 (1.280)	37,08 (1.480)
B MIN	6,22 (0.245)	7,24 (0.285)
B MAX	7,62 (0.300)	7,39 (0.291)

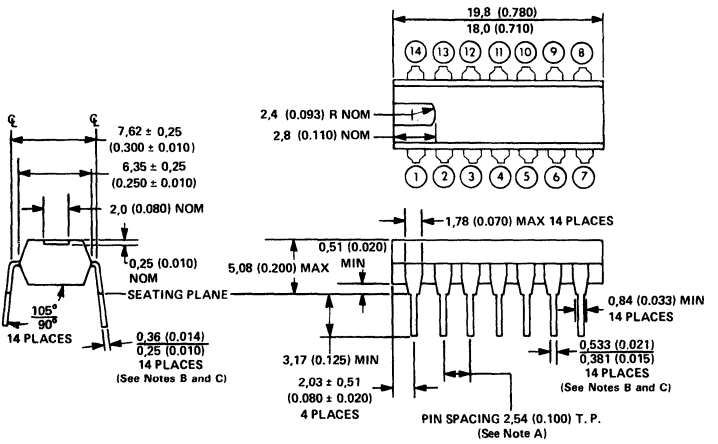
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

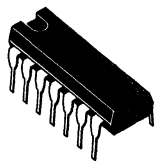
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

N014 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N014





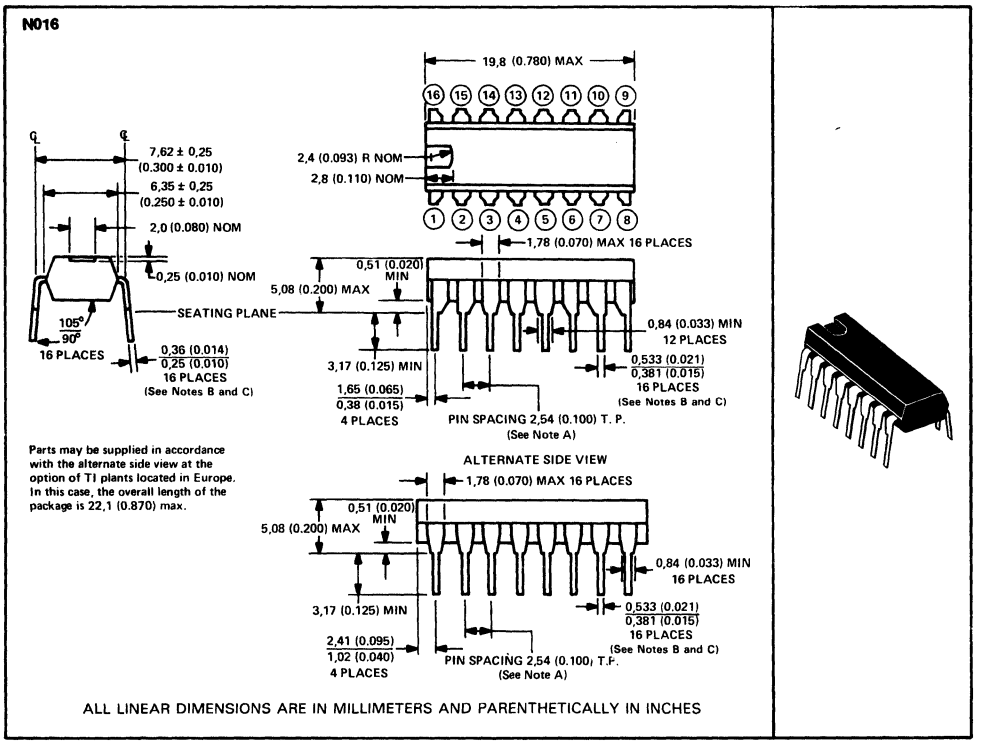
Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N016 plastic dual-in-line package

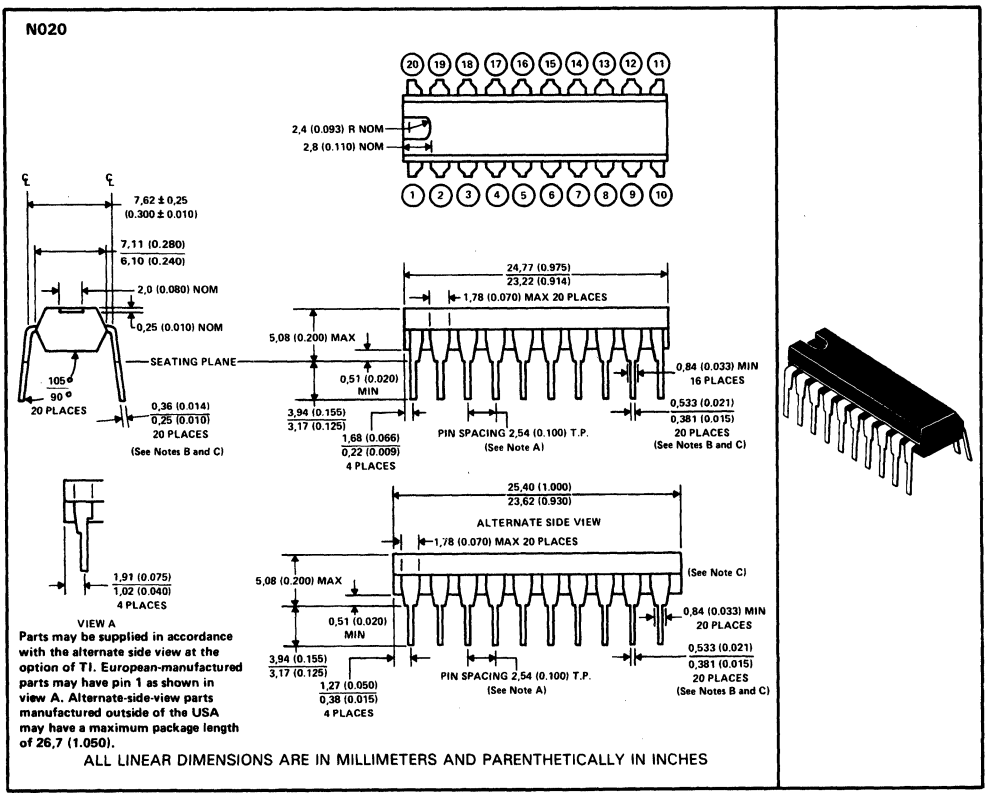
This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N020 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



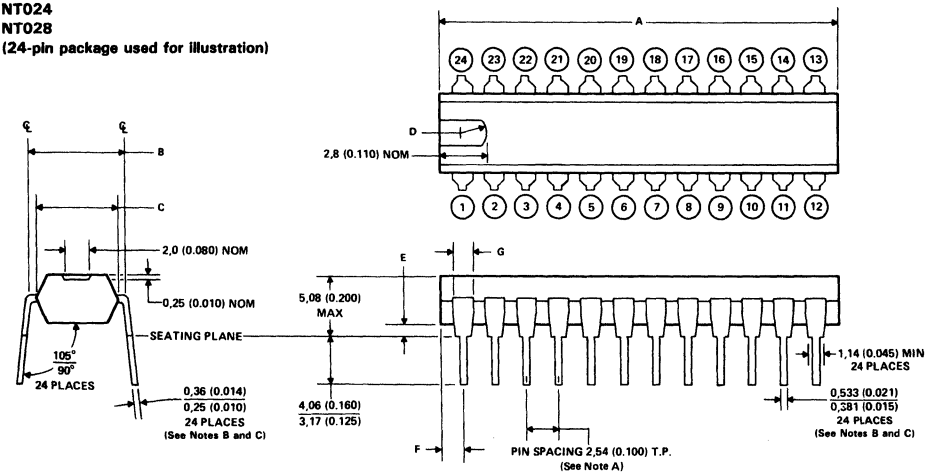
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NT024 and NT028 plastic dual-in-line packages

Each of these packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin and 28-pin packages, the letter N is used by itself since the 24-pin and 28-pin packages may be available in more than one row-spacing. For the 24-pin and 28-pin packages, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

NT024
NT028
(24-pin package used for illustration)



DIM / DESIGNATION	A MIN	A MAX	B	C MAX	D R NOM	E MIN	F MIN	F MAX	G MIN	G MAX
NT024	28,6 (1.125)	31,8 (1.250)	7,62 ± 0,25 (0.300 ± 0.010)	7,1 (0.280)	2,4 (0.093)	0.38 (0.015)	0,71 (0.028)	2,16 (0.085)	1,14 (0.045)	1,78 (0.070)
NT028	34,0 (1.338)	37,1 (1.462)	7,88 ± 0,25 (0.310 ± 0.010)	7,1 (0.280)	1,02 (0.040)	0,51 (0.020)	0,51 (0.020)	2,03 (0.080)	1,02 (0.040)	1,78 (0.070)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

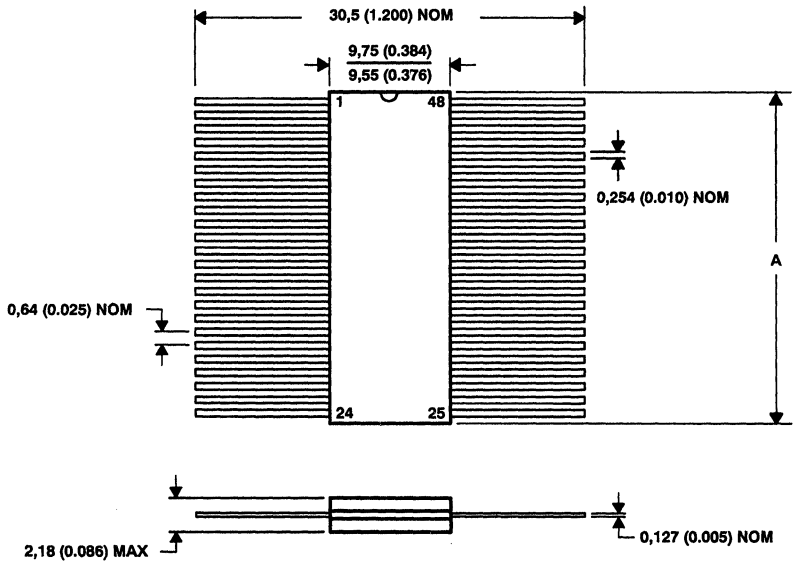
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

WD048 and WD056 ceramic flat packages†

These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

† These packages are under development.

WD048 and WD056
(48-pin package used for illustration)



DIM \ PINS	48	56
A MIN	15,60 (0.614)	18,11 (0.713)
A MAX	15,90 (0.626)	18,47 (0.727)

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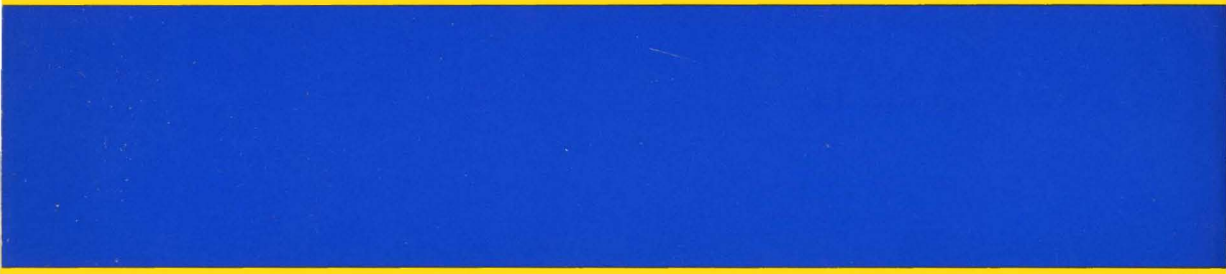

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