TEXAS INSTRUMENTS

MOS Memory

Commercial and Military Specifications

Data Book

1991

MOS Memory Data Book

Commercial and Military Specifications

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INTRODUCTION

The 1991 MOS Memory Data Book from Texas Instruments includes complete detailed specifications on the expanding MOS Memory product line including Dynamic Random-Access Memories (DRAMs), Single-In-Line Package DRAM Memory Modules (SIPs), Erasable Programmable Read-Only Memories (EPROMs), One-Time Programmable Read-Only Memories (OTP PROMs), Electrically Erasable Programmable Read-Only Memories (Flash EEPROMs), and Application Specific Memories (ASMs). Also included are military specifications for DRAMs, EPROMs, and ASMs, as well as specifications for the Datapath VLSI Memory Management products.

The data book is divided into 14 chapters. Below you will find a brief description of each chapter.

Chapter 1. General Information – Includes an alphanumeric index for quickly finding device numbers, a part number guide with ordering information, and an IC Line-up chart for a quick overview.

Chapter 2. Selection Guide – An easy-to-use reference guide that includes specific device information. Page numbers are also shown for easy access to the detailed specifications.

Chapter 3. Alternate Source Directory – Lists alternate vendor part numbering examples in addition to alternate sources for TI devices (based on published data).

Chapter 4. Glossary/Timing Conventions/Data Sheet Structure – Defines terms and standards used throughout the data book.

Chapters 5 - 10. Product specifications for over 100 devices can be found in these sections.

Chapter 11. Logic Symbols – Includes an explanation and examples of the IEEE standard.

Chapter 12. Quality and Reliability – Details selected processes and the philosophies of Texas Instruments that are used to ensure high quality standards.

Chapter 13. Electrostatic Discharge Guidelines – Because all MOS Memory devices are ESD-sensitive, handling guidelines are included.

Chapter 14. Mechanical Data – Detailed package drawings and specifications are shown in this section.

Additional and/or updated information on these products is available from:

Texas Instruments
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1-800-232-3200

For ordering information or further assistance please contact your nearest Texas Instruments Sales Office or Distributor as listed in the back of this book.

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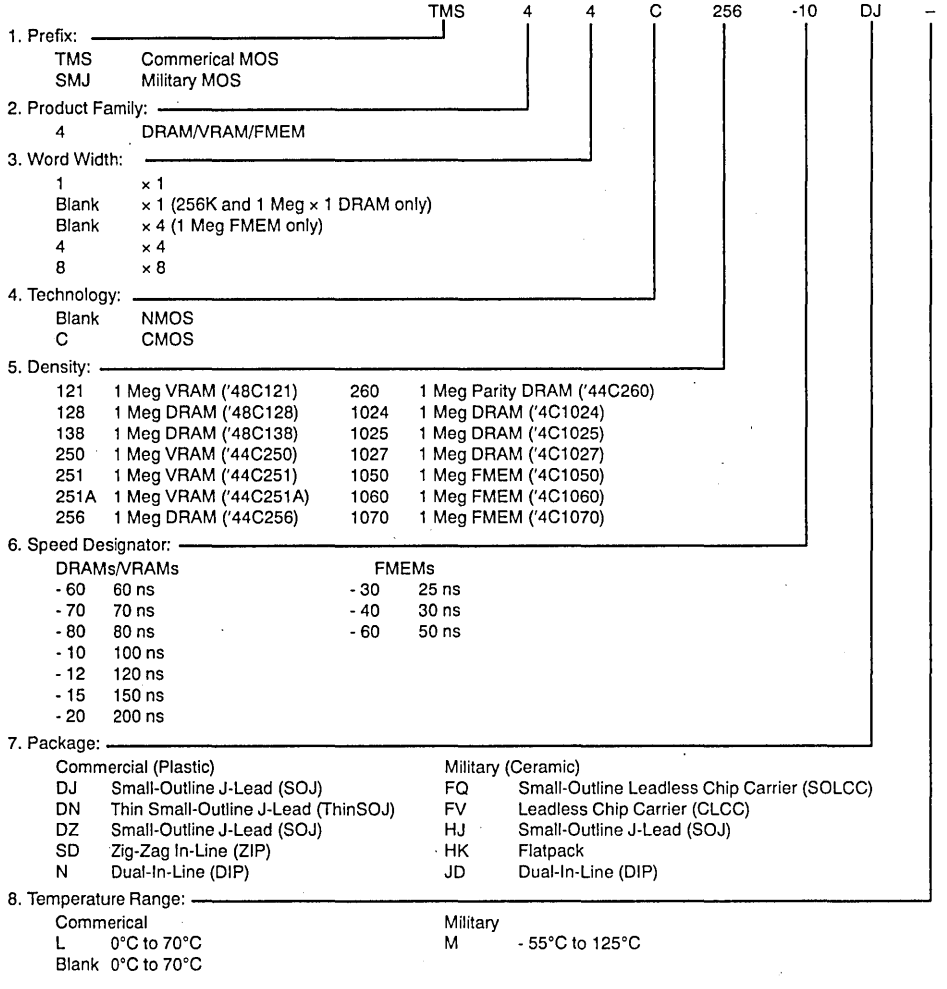
CHAPTER 7. EPROM/OTP PROM/FLASH EEPROM

Alphanumeric Index

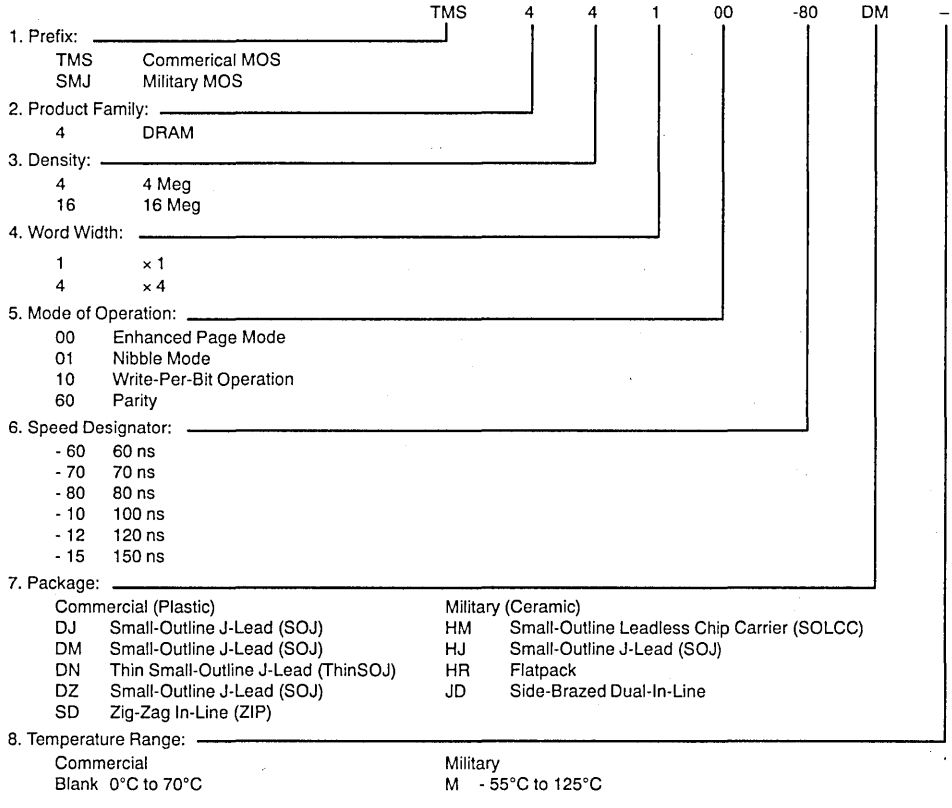
DRAM/VRAM/FMEM Ordering Information

Factory orders for 1 Meg DRAMs, VRAMs, and FMEMs described in this book should include an eight-part type number as explained in the following example:



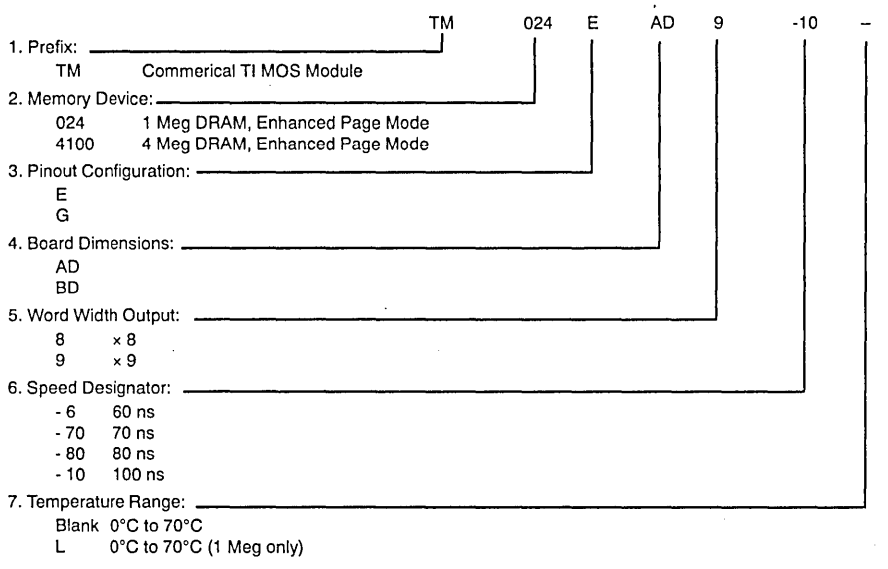
DRAM Ordering Information

Factory orders for the 4 Meg and 16 Meg DRAMs described in this book should include an eight-part type number as explained in the following example:



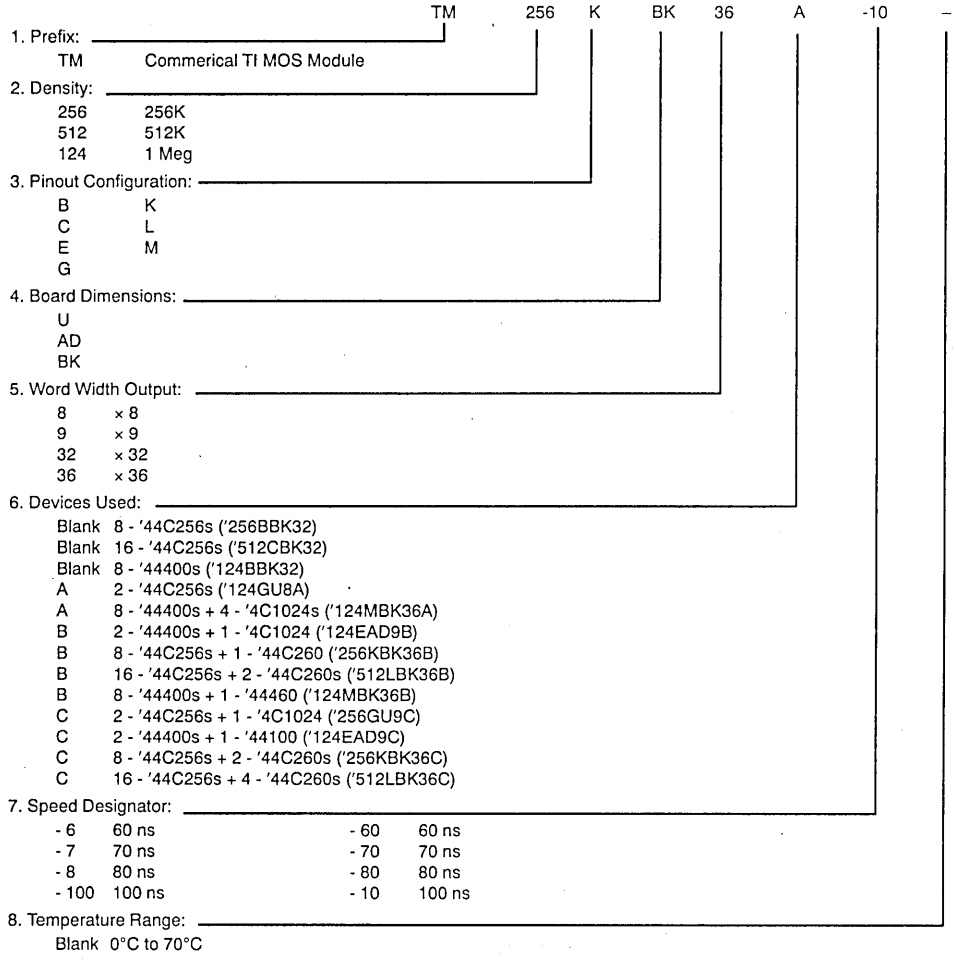
Standard DRAM Module Ordering Information

Factory orders for the standard DRAM Modules described in this book should include a seven-part type number as explained in the following example:



Differentiated DRAM Module Ordering Information

Factory orders for the mixed DRAM Modules described in this book should include an eight-part type number as explained in the following example:



EPROM/OTP PROM/Flash EEPROM Ordering Information

Factory orders for EPROMs, OTPs, and Flash EEPROMs described in this book should include a nine-part type number as explained in the following example:

TMS 27 P C 512 –10 FM L 4

1. Prefix:
   - TMS — Commerical MOS
   - SMJ — Military MOS
2. Product Family:
   - 27 — EPROM/OTP
   - 29 — Flash EEPROM
   - 87 — Latched EPROM
3. Erasability:
   - P — Non-erasable
   - Blank — Erasable
4. Technology:
   - C — CMOS
   - F — CMOS Flash EEPROM
5. Density:

816	16K	512	512K
128	128K	010A	1 Meg
256	256K	210A	1 Meg
257	256K	020	2 Meg
258	256K	040	4 Meg
259	256K	240	4 Meg
510	512K		

6. Speed Designator:

80 ns	- 8, - 80	170 ns	- 1, - 17, - 170
100 ns	- 10, - 100	200 ns	- 2, - 20, - 200
120 ns	- 12, - 120	250 ns	Blank, - 20, - 200
150 ns	- 1, - 15, - 150	300 ns	- 30, - 300

7. Package:

OTPs (Plastic)		EPROMs (Ceramic)		Flash EEPROMs	
N	Dual-In-Line (DIP)	J	Dual-In-Line (DIP)	J	Ceramic Dual-In-Line (DIP)
FM	Chip Carrier			N	Plastic Dual-In-Line (DIP)
				FM	Plastic Chip Carrier

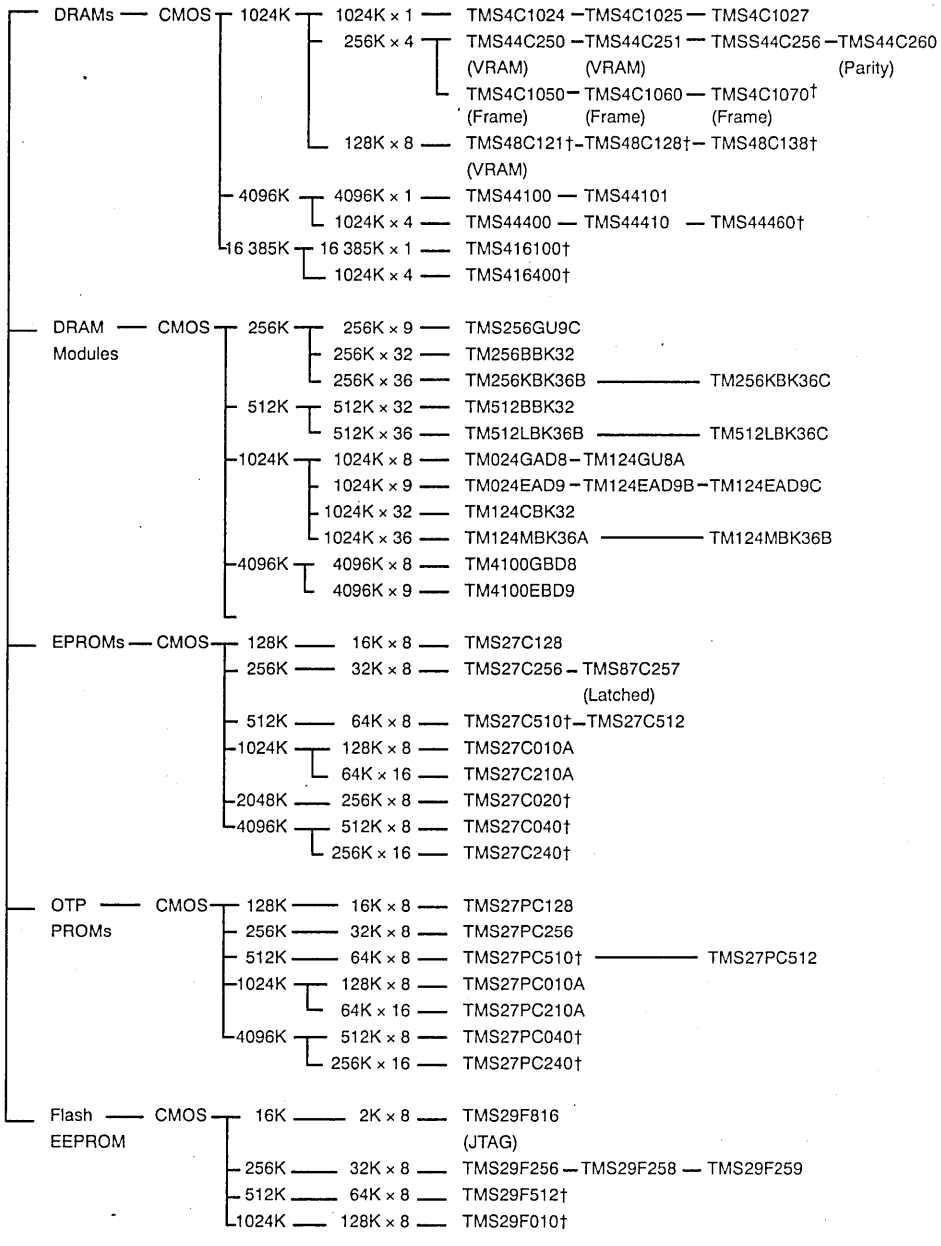
8. Temperature Range:

Commerical		Military	
L	0°C to 70°C	M	- 55°C to 125°C
E	- 40°C to 85°C		
Q	- 40°C to 125°C		

9. 168 Hour Burn-in Option:

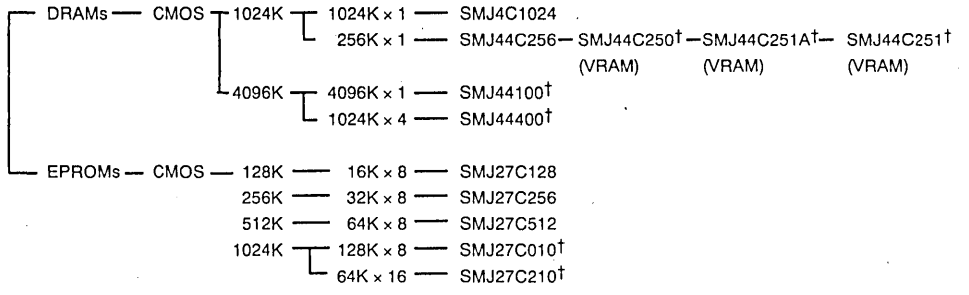
Commerical		Military	
4	168 Hour Burn-in	Blank	5004 Processing
Blank	No Burn-in		

MOS Memory IC Line-up



† Product under development by TI

MOS Memory Military IC Line-up



† Product under development by TI

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DRAM

Density	Organization (Words × Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby (mW)				
1024K	1024K × 1	TMS4C1024-60‡ TMS4C1024-70‡ TMS4C1024-80 TMS4C1024-10 TMS4C1024-12	60 70 80 100 120	5 ± 10%	253 440 413 358 303	11	18, 20/26, 20/26, 20	N, DJ DN, SD	CMOS Enhanced Page Mode	5-23
		SMJ4C1024-10 SMJ4C1024-12 SMJ4C1024-15	100 120 150	5 ± 10%	385 330 303	17	20/26, 20, 20	HJ, FQ, HK	Military CMOS Enhanced Page Mode	9-23
		TMS4C1025-80 TMS4C1025-10 TMS4C1025-12	80 100 120	5 ± 10%	413 358 303	11	18, 20/26, 20/26, 20	N, DJ DN, SD	CMOS Nibble Mode	5-23
		TMS4C1027-80 TMS4C1027-10 TMS4C1027-12	80 100 120	5 ± 10%	413 358 303	11	18, 20/26, 20/26, 20	N, DJ DN, SD	CMOS Static Mode	5-23
	256K × 4	TMS44C256-60‡ TMS44C256-70‡ TMS44C256-80 TMS44C256-10 TMS44C256-12	60 70 80 100 120	5 ± 10%	523 440 413 358 303	11	20, 20/26, 20/26, 20	N, DJ DN, SD	CMOS Enhanced Page Mode	5-1
		SMJ44C256-10 SMJ44C256-12 SMJ44C256-15	100 120 150	5 ± 10%	385 330 303	17	20, 20/26, 20	JD, HJ, FQ	Military CMOS Enhanced Page Mode	9-3
	128K × 8	TMS48C128-70 TMS48C128-80 TMS48C128-10	70 80 100	5 ± 10%	468 440 385	11	24/26	DJ	CMOS Enhanced Page Mode	5-63
		TMS48C138-70 TMS48C138-80 TMS48C138-10	70 80 100	5 ± 10%	468 440 385	11	24/26	DJ	CMOS Enhanced Page Mode Write-per- Bit Opera- tion	5-63
4096K	4096K × 1	TMS44100-60 TMS44100-70 TMS44100-80 TMS44100-10	60 70 80 100	5 ± 10%	550 495 440 385	11	20/26, 20/26, 20	DJ, DM, SD	CMOS Enhanced Page Mode	5-87
		SMJ44100-80§ SMJ44100-10§ SMJ44100-12§	80 100 120	5 ± 10%	468 440 385	22	18, 20, 20, 20	JD, HM HJ, HR	Military CMOS Enhanced Page Mode	9-41
		TMS44101-60 TMS44101-70 TMS44101-80 TMS44101-10	60 70 80 100	5 ± 10%	523 468 413 358	11	20/26, 20/26, 20	DJ, DM, SD	CMOS Nibble Mode	5-107

† N Plaastic Dual In-Line Package (DIP)
DJ Plastic Small-Outline J-Lead (SOJ)
DN Plastic Thin Small-Outline J-Lead (ThinSoJ)
DM Plastic Small-Outline J-Lead (SOJ)
FQ Ceramic Small-Outline Leadless Chip Carrier (Military) (SOLCC)
HJ Ceramic Small-Outline Leadless J-Lead (Military) (SOLCC)
HK Flatpack (Military)
HM Plastic Small-Outline Leadless Chip Carrier (Military) (SOLCC)
HR Flatpack (Military)
JD Ceramic Side-Brazed Dual In-Line Package (Military) (DIP)
SD Plastic Zig-Zag In-Line Package (ZIP)

‡ Available only in DJ package

§ Advance Information for product under development by TI

DRAM (Concluded)

Density	Organization (Words × Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby (mW)				
4096K (cont'd)	1024K × 4	TMS44400-60 TMS44400-70 TMS44400-80 TMS44400-10	60 70 80 100	5 ± 10%	550 495 440 385	11	20/26, 20/26, 20	DJ, DM, SD	CMOS Enhanced Page Mode	5-125
		SMJ44400-80‡ SMJ44400-10‡ SMJ44400-12‡	80 100 120	5 ± 10%	468 440 358	22	20, 20, 20, 20	JD, HM HJ, HR	Military CMOS Enhanced Page Mode	9-61
		TMS44410-60 TMS44410-70 TMS44410-80 TMS44410-10	60 70 80 100	5 ± 10%	523 468 413 358	11	20/26, 20/26, 20	DJ, DM, SD	CMOS Enhanced Page Mode Write-per-Bit Operation	5-145
16 385K	16 385K × 1	TMS416100-60‡ TMS416100-70‡ TMS416100-80‡ TMS416100-10‡	60 70 80 100	5 ± 10%	495 440 385 330	11	24/28	DZ	CMOS Enhanced Page Mode	5-165
	4096K × 4	TMS416400-60‡ TMS416400-70‡ TMS416400-80‡ TMS416400-10‡	60 70 80 100	5 ± 10%	495 440 385 330	11	24/28	DZ	CMOS Enhanced Page Mode	5-187

† DJ Plastic Small-Outline J-Lead (SOJ)
DM Plastic Small-Outline J-Lead (SOJ)
DZ Plastic Small-Outline J-Lead (SOJ)
HJ Ceramic Small-Outline Leadless J-Lead (Military) (SOLCC)
HM Plastic Small-Outline Leadless Chip Carrier (Military) (SOLCC)
HR Flatpack (Military)
JD Ceramic Side-Brazed Dual In-Line Package (Military) (DIP)
SD Plastic Zig-Zag In-Line Package (ZIP)

‡ Advance Information for product under development by TI

DRAM Module

Density	Organization (Words × Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package	Page
					Active (mW)	Standby (mW)			
2304K	256K × 9	TM256GU9C-6	60	5 ± 5%	1496	31	30	Single-Sided, Socketable	6-1
		TM256GU9C-70	70	5 ± 10%	1320	33			
		TM256GU9C-80	80	5 ± 10%	1238	33			
		TM256GU9C-10	100	5 ± 10%	1073	33			
8192K	1024K × 8	TM024GAD8-6	60	5 ± 5%	3990	84	30	Single-Sided, Socketable	6-7
		TM024GAD8-70	70	5 ± 10%	3520	88			
		TM024GAD8-80	80	5 ± 10%	3300	88			
		TM024GAD8-10	100	5 ± 10%	2860	88			
		TM124GU8A-6	60	5 ± 5%	998	21	30	Single-Sided, Socketable	6-13
		TM124GU8A-70	70	5 ± 10%	935	22			
		TM124GU8A-80	80	5 ± 10%	825	22			
		TM124GU8A-10	100	5 ± 10%	715	22			
	256K × 32	TM256BBK32-6	60	5 ± 5%	3990	84	72	Single-Sided, Socketable	6-21
		TM256BBK32-70	70	5 ± 10%	3520	88			
		TM256BBK32-80	80	5 ± 10%	3300	88			
		TM256BBK32-10	100	5 ± 10%	2860	88			
9216K	1024K × 9	TM024EAD9-6	60	5 ± 5%	4489	95	30	Single-Sided, Socketable	6-31
		TM024EAD9-70	70	5 ± 10%	3960	99			
		TM024EAD9-80	80	5 ± 10%	3713	99			
		TM024EAD9-10	100	5 ± 10%	3218	99			
		TM124EAD9B-6	60	5 ± 5%	1496	32	30	Single-Sided, Socketable	6-37
		TM124EAD9B-70	70	5 ± 10%	1403	33			
		TM124EAD9B-80	80	5 ± 10%	1238	33			
		TM124EAD9B-10	100	5 ± 10%	1073	33			
		TM124EAD9C-6	60	5 ± 5%	1496	32	30	Single-Sided, Socketable	6-37
		TM124EAD9C-70	70	5 ± 10%	1403	33			
		TM124EAD9C-80	80	5 ± 10%	1238	33			
		TM124EAD9C-10	100	5 ± 10%	1073	33			
	256K × 36	TM256KBK36B-6	60	5 ± 5%	4489	95	72	Single-Sided, Socketable	6-45
		TM256KBK36B-70	70	5 ± 10%	3960	99			
		TM256KBK36B-80	80	5 ± 10%	3713	99			
		TM256KBK36B-10	100	5 ± 10%	3218	99			
		TM256KBK36C-6	60	5 ± 5%	4988	105	72	Single-Sided, Socketable	6-55
		TM256KBK36C-70	70	5 ± 10%	4400	110			
		TM256KBK36C-80	80	5 ± 10%	4125	110			
		TM256KBK36C-10	100	5 ± 10%	3575	110			
16 384K	512K × 32	TM512CBK32-6	60	5 ± 5%	4074	168	72	Double-Sided, Socketable	6-21
		TM512CBK32-70	70	5 ± 10%	3608	176			
		TM512CBK32-80	80	5 ± 10%	3388	176			
		TM512CBK32-10	100	5 ± 10%	2948	176			
18 432K	512K × 36	TM512LBK36B-6	60	5 ± 5%	4583	189	72	Double-Sided, Socketable	6-45
		TM512LBK36B-70	70	5 ± 10%	4059	198			
		TM512LBK36B-80	80	5 ± 10%	3812	198			
		TM512LBK36B-10	100	5 ± 10%	3317	198			
		TM512LBK36C-6	60	5 ± 5%	5093	210	72	Double-Sided, Socketable	6-55
		TM512LBK36C-70	70	5 ± 10%	4510	220			
		TM512LBK36C-80	80	5 ± 10%	4235	220			
		TM512LBK36C-10	100	5 ± 10%	3685	220			

DRAM Module (Concluded)

Density	Organization (Words × Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package	Page
					Active (mW)	Standby (mW)			
32 768K	4096K × 8	TM4100GBD8-6	60	5 ± 5%	3990	84	30	Single-Sided, Socketable	6-65
		TM4100GBD8-70	70	5 ± 10%	3740	88			
		TM4100GBD8-80	80	5 ± 10%	3300	88			
		TM4100GBD8-10	100	5 ± 10%	2860	88			
	1024K × 32	TM124BBK32-6	60	5 ± 5%	3990	84	72	Single-Sided, Socketable	6-73
		TM124BBK32-70	70	5 ± 10%	3740	88			
		TM124BBK32-80	80	5 ± 10%	3300	88			
		TM124BBK32-10	100	5 ± 10%	2860	88			
36 864K	4096K × 9	TM4100EBD9-6	60	5 ± 5%	4489	95	30	Single-Sided, Socketable	6-81
		TM4100EBD9-70	70	5 ± 10%	4208	99			
		TM4100EBD9-80	80	5 ± 10%	3713	99			
		TM4100EBD9-10	100	5 ± 10%	3218	99			
	1024K × 36	TM124MBK36A-6†	60	5 ± 5%	5985	126	72	Double-Sided, Socketable	6-89
		TM124MBK36A-7†	70	5 ± 5%	5250	126			
		TM124MBK36A-8†	80	5 ± 5%	4725	126			
		TM124MBK36B-6†	60	5 ± 5%	4489	95	72	Single-Sided, Socketable	6-97
		TM124MBK36B-7†	70	5 ± 5%	4016	95			
		TM124MBK36B-8†	80	5 ± 5%	3544	95			

† Advance Information for product under development by TI

EPROM/Flash EEPROM

Density	Organization (Words × Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby CMOS (mW)				
128K	16K × 8	TMS27C128-100	100	5 ± 5%	158	1.4	28	J	CMOS	7-1
		TMS27C128-120	120	5 ± 5%	158					
		TMS27C128-12	120	5 ± 10%	165					
		TMS27C12-1	150	5 ± 5%	158					
		TMS27C128-15	150	5 ± 10%	165					
		TMS27C128-2	200	5 ± 5%	158					
		TMS27C128-20	200	5 ± 10%	165					
		TMS27C128	250	5 ± 5%	158					
		TMS27C128-25	250	5 ± 10%	165					
		SMJ27C128-12	120	5 ± 10%	220	1.7	28	J	Military CMOS	9-81
		SMJ27C128-15	150							
		SMJ27C128-17	170							
		SMJ27C128-20	200							
		SMJ27C128-25	250							
		SMJ27C128-30	300							
256K	32K × 8	TMS27C256-120	120	5 ± 5%	158	1.4	28	J	CMOS	7-15
		TMS27C256-12	120	5 ± 10%	165					
		TMS27C256-150	150	5 ± 5%	158					
		TMS27C256-15	150	5 ± 10%	165					
		TMS27C256-1	170	5 ± 5%	158					
		TMS27C256-17	170	5 ± 10%	165					
		TMS27C256-2	200	5 ± 5%	158					
		TMS27C256-20	200	5 ± 10%	165					
		TMS27C256	250	5 ± 5%	158					
		TMS27C256-25	250	5 ± 10%	165					
		SMJ27C256-15	150	5 ± 10%	220	1.7	28	J	Military CMOS	9-91
		SMJ27C256-17	170							
		SMJ27C256-20	200							
		SMJ27C256-25	250							
		SMJ27C256-30	300							
		TMS29F256-170	170	5 ± 5%	83	17	28, 28, 32	J, N, FM	CMOS 5-V Flash EEPROM; EPROM Pinout	7-27
		TMS29F256-200	200	5 ± 5%						
		TMS29F256-20	200	5 ± 10%						
		TMS29F256-250	250	5 ± 5%						
		TMS29F256-25	250	5 ± 10%						
		TMS29F256-300	300	5 ± 5%						
		TMS29F256-30	300	5 ± 10%						
		TMS29F258-170	170	5 ± 5%	83	17	28, 28, 32	J, N, FM	CMOS 5-V Flash EEPROM; EEPROM Pinout	7-27
		TMS29F258-200	200	5 ± 5%						
		TMS29F258-20	200	5 ± 10%						
		TMS29F258-250	250	5 ± 5%						
		TMS29F258-25	250	5 ± 10%						
		TMS29F258-300	300	5 ± 5%						
		TMS29F258-30	300	5 ± 10%						
		TMS29F259-170	170	5 ± 5%	83	17	28, 28, 32	J, N, FM	CMOS 5-V Flash EEPROM; 12-V Flash Memory Pinout	7-27
		TMS29F259-200	200	5 ± 5%						
		TMS29F259-20	200	5 ± 10%						
		TMS29F259-250	250	5 ± 5%						
		TMS29F259-25	250	5 ± 10%						
		TMS29F259-300	300	5 ± 5%						
		TMS29F259-30	300	5 ± 10%						

† J Ceramic Dual In-Line Package (DIP)
N Plastic Dual In-Line Package (DIP)
FM Plastic Chip Carrier

EPROM/Flash EEPROM

Density	Organization (Words × Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby CMOS (mW)				
256K (cont'd)	32K × 8 (cont'd)	TMS87C257-150 TMS87C257-1 TMS87C257-2 TMS87C257	150 170 200 250	5 ± 5%	158	1.4	28	J	CMOS Latched EPROM	7-47
512K	64K × 8	TMS27C510-120‡ TMS27C510-12‡ TMS27C510-150‡ TMS27C510-15‡ TMS27C510-170‡ TMS27C510-17‡ TMS27C510-200‡ TMS27C510-20‡ TMS27C510-250‡ TMS27C510-25‡	120 120 150 150 170 170 200 200 250 250	5 ± 5% 5 ± 10% 5 ± 5% 5 ± 10% 5 ± 5% 5 ± 10% 5 ± 5% 5 ± 10% 5 ± 5% 5 ± 10%	158 165 158 165 158 165 158 165 158 165	1.4	32	J	CMOS; 1 Meg EPROM Compatible Pinout	7-57
		TMS27C512-100 TMS27C512-10 TMS27C512-120 TMS27C512-12 TMS27C510-150 TMS27C512-15 TMS27C512-2 TMS27C512-20 TMS27C512 TMS27C512-25	100 100 120 120 150 150 200 200 250 250	5 ± 5% 5 ± 10% 5 ± 5% 5 ± 10% 5 ± 5% 5 ± 10% 5 ± 5% 5 ± 10% 5 ± 5% 5 ± 10%	158 165 158 165 158 165 158 165 158 165	1.4	28	J	CMOS	7-69
		SMJ27C512-20 SMJ27C512-25 SMJ27C512-30	200 250 300	5 ± 10%	263	1.8	28	J	Military CMOS	9-101
		TMS29F512-100‡ TMS29F512-120‡ TMS29F512-12‡ TMS29F512-150‡ TMS29F512-15‡ TMS29F512-200‡ TMS29F512-20‡	100 120 120 150 150 200 200	5 ± 5% 5 ± 5% 5 ± 10% 5 ± 5% 5 ± 10% 5 ± 5% 5 ± 10%	79 79 83 79 83 79 83	5.5	32, 32, 32	J, N, FM	CMOS 5-V Flash EEPROM	7-81
1024K	128K × 8	TMS27C010A-100 TMS27C010A-120 TMS27C010A-12 TMS27C010A-150 TMS27C010A-15 TMS27C010A-200 TMS27C010A-20	100 120 120 150 150 200 200	5 ± 5% 5 ± 5% 5 ± 10% 5 ± 5% 5 ± 10% 5 ± 5% 5 ± 10%	158 158 165 158 165 158 165	0.55	32	J	CMOS	7-85
		SMJ27C010-17 SMJ27C010-20 SMJ27C010-25	170 200 250	5 ± 10%	220	1.5	32	J	Military CMOS	9-113
		TMS29F010-100‡ TMS29F010-120‡ TMS29F010-12‡ TMS29F010-150‡ TMS29F010-15‡ TMS29F010-200‡ TMS29F010-20‡	100 120 120 150 150 200 200	5 ± 5% 5 ± 5% 5 ± 10% 5 ± 5% 5 ± 10% 5 ± 5% 5 ± 10%	79 79 83 79 83 79 83	5.5	32, 32, 32	J, N, FM	CMOS 5-V Flash EEPROM	7-95

† J Ceramic Dual In-Line Package (DIP)
N Plastic Dual In-Line Package (DIP)
FM Plastic Leaded Chip Carrier
‡ Advance Information for product under development by TI

EPROM/Flash EEPROM (Concluded)

Density	Organization (Words × Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby CMOS (mW)				
1024K (cont'd)	64K × 16	TMS27C210A-120‡	120	5 ± 5%	158	0.55	40	J	CMOS	7-119
		TMS27C210A-12‡	120	5 ± 10%	165					
		TMS27C210A-150‡	150	5 ± 5%	158					
		TMS27C210A-15‡	150	5 ± 10%	165					
		TMS27C210A-200‡	200	5 ± 5%	158					
		TMS27C210A-20‡	200	5 ± 10%	165					
		TMS27C210A-250‡	250	5 ± 5%	158					
		TMS27C210A-25‡	250	5 ± 10%	165					
		SMJ27C210A-17	170	5 ± 10%	220	1.5	32	J	Military CMOS	9-115
		SMJ27C210A-20	200							
		SMJ27C210A-25	250							
2048K	256K × 8	TMS27C020-100‡	100	5 ± 5%	158	0.55	32	J	CMOS	7-129
		TMS27C020-120‡	120	5 ± 5%	158					
		TMS27C020-12‡	120	5 ± 10%	165					
		TMS27C020-150‡	150	5 ± 5%	158					
		TMS27C020-15‡	150	5 ± 10%	165					
		TMS27C020-200‡	200	5 ± 5%	158					
		TMS27C020-20‡	200	5 ± 10%	165					
		TMS27C020-250‡	250	5 ± 5%	158					
		TMS27C020-25‡	250	5 ± 10%	165					
4096K	512K × 8	TMS27C040-8‡	80	5 ± 5%	263	0.55	32	J	CMOS	7-139
		TMS27C040-80‡	80	5 ± 10%	275					
		TMS27C040-100‡	100	5 ± 5%	263					
		TMS27C040-10‡	100	5 ± 10%	275					
		TMS27C040-120‡	120	5 ± 5%	263					
		TMS27C040-12‡	120	5 ± 10%	275					
		TMS27C040-150‡	150	5 ± 5%	263					
		TMS27C040-15‡	150	5 ± 10%	275					
	256K × 16	TMS27C240-8‡	80	5 ± 5%	263	0.55	40	J	CMOS	7-149
		TMS27C240-80‡	80	5 ± 10%	275					
		TMS27C240-100‡	100	5 ± 5%	263					
		TMS27C240-10‡	100	5 ± 10%	275					
		TMS27C240-120‡	120	5 ± 5%	263					
		TMS27C240-12‡	120	5 ± 10%	275					
		TMS27C240-150‡	150	5 ± 5%	263					
		TMS27C240-15‡	150	5 ± 10%	275					

† J Ceramic Dual In-Line Package (DIP)

‡ Advance Information for product under development by TI

One-Time Programmable (OTP) PROM

Density	Organization (Words × Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby CMOS (mW)				
128K	16K × 8	TMS27PC128-1	150	5 ± 5%	158	1.4	28, 32	N, FM	CMOS	7-1
		TMS27PC128-15	150	5 ± 10%	165					
		TMS27PC128-2	200	5 ± 5%	158					
		TMS27PC128-20	200	5 ± 10%	165					
		TMS27PC128	250	5 ± 5%	158					
		TMS27PC128-25	250	5 ± 10%	165					
256K	32K × 8	TMS27PC256-150	150	5 ± 5%	158	1.4	28, 32	N, FM	CMOS	7-15
		TMS27PC256-15	150	5 ± 10%	165					
		TMS27PC256-1	170	5 ± 5%	158					
		TMS27PC256-17	170	5 ± 10%	165					
		TMS27PC256-2	200	5 ± 5%	158					
		TMS27PC256-20	200	5 ± 10%	165					
		TMS27PC256	250	5 ± 5%	158					
		TMS27PC256-25	250	5 ± 10%	165					
512K	64K × 8	TMS27PC510-120‡	120	5 ± 5%	158	1.4	32, 32	N, FM	CMOS 1 Meg OTP Compatible Pinout	7-57
		TMS27PC510-150‡	150	5 ± 5%	158					
		TMS27PC510-15‡	150	5 ± 10%	165					
		TMS27PC510-170‡	170	5 ± 5%	158					
		TMS27PC510-17‡	170	5 ± 10%	165					
		TMS27PC510-200‡	200	5 ± 5%	158					
		TMS27PC510-20‡	200	5 ± 10%	165					
		TMS27PC510-250‡	250	5 ± 5%	158					
		TMS27PC510-25‡	250	5 ± 10%	165					
		TMS27PC512-100	100	5 ± 5%	158	1.4	28, 32	N, FM	CMOS	7-69
		TMS27PC512-10	100	5 ± 10%	165					
		TMS27PC512-120	120	5 ± 5%	158					
		TMS27PC512-12	120	5 ± 10%	165					
		TMS27PC512-150	150	5 ± 5%	158					
		TMS27PC512-15	150	5 ± 10%	165					
		TMS27PC512-2	200	5 ± 5%	158					
		TMS27PC512-20	200	5 ± 10%	165					
		TMS27PC512	250	5 ± 5%	158					
		TMS27PC512-25	250	5 ± 10%	165					
1024K	128K × 8	TMS27PC010A-100	100	5 ± 5%	158	0.55	32	FM	CMOS	7-85
		TMS27PC010A-120	120	5 ± 5%	158					
		TMS27PC010A-12	120	5 ± 10%	165					
		TMS27PC010A-150	150	5 ± 5%	158					
		TMS27PC010A-15	150	5 ± 10%	165					
		TMS27PC010A-200	200	5 ± 5%	158					
		TMS27PC010A-20	200	5 ± 10%	165					
1024K (cont'd)	64K × 16	TMS27PC210A-120‡	120	5 ± 5%	158	0.55	44	FN	CMOS	7-119
		TMS27PC210A-12‡	120	5 ± 10%	165					
		TMS27PC210A-150‡	150	5 ± 5%	158					
		TMS27PC210A-15‡	150	5 ± 10%	165					
		TMS27PC210A-200‡	200	5 ± 5%	158					
		TMS27PC210A-20‡	200	5 ± 10%	165					
		TMS27PC210A-250‡	250	5 ± 5%	158					
		TMS27PC210A-25‡	250	5 ± 10%	165					

† N Plastic Dual In-Line Package (DIP)
FM Plastic Leaded Chip Carrier
FN Plastic Leaded Chip Carrier

‡ Advance Information for product under development by TI

One-Time Programmable (OTP) PROM (Concluded)

Density	Organization (Words × Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby CMOS (mW)				
4096K	512K × 8	TMS27PC040-8‡	80	5 ± 5%	263	0.55	32	FM	CMOS	7-139
		TMS27PC040-80‡	80	5 ± 10%	275					
		TMS27PC040-100‡	100	5 ± 5%	263					
		TMS27PC040-10‡	100	5 ± 10%	275					
		TMS27PC040-120‡	120	5 ± 5%	263					
		TMS27PC040-12‡	120	5 ± 10%	275					
		TMS27PC040-150‡	150	5 ± 5%	263					
		TMS27PC040-15‡	150	5 ± 10%	275					
	256K × 16	TMS27PC240-8‡	80	5 ± 5%	263	0.55	44	FN	CMOS	7-149
		TMS27PC240-80‡	80	5 ± 10%	275					
		TMS27PC240-100‡	100	5 ± 5%	263					
		TMS27PC240-10‡	100	5 ± 10%	275					
		TMS27PC240-120‡	120	5 ± 5%	263					
		TMS27PC240-12‡	120	5 ± 10%	275					
		TMS27PC240-150‡	150	5 ± 5%	263					
		TMS27PC240-15‡	150	5 ± 10%	275					

† FM Plastic Leaded Chip Carrier
FN Plastic Leaded Chip Carrier
‡ Advance Information for product under development by TI

Application Specific Memories (ASM)

Density	Organization (Words × Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby (mW)				
16K	2K × 8	TMS29F816‡	TBD	5 ± 10%	TBD	TBD	18	FM	SCOPE Diary Storage Device	8-1
1024K	256K × 4	TMS44C250-1 TMS44C250-10 TMS44C250-12	100 100 120	5 ± 5% 5 ± 10% 5 ± 10%	578 605 523	184 193 193	28, 28	DZ, SD	CMOS Multiport Video RAM	8-3
		SMJ44C250-10‡ SMJ44C250-1‡ SMJ44C250-12‡ SMJ44C250-2‡	100 100 120 120	5 ± 10% 5 ± 5% 5 ± 10% 5 ± 5%	635 635 550 550	90 90 83 83	28, 28	HJ, JD	Military CMOS Multiport Video RAM	9-117
		TMS44C251-1 TMS44C251-10 TMS44C251-12	100 100 120	5 ± 5% 5 ± 10% 5 ± 10%	578 605 523	184 193 193	28, 28	DZ, SD	CMOS Multiport Video RAM	8-31
		SMJ44C251-10‡ SMJ44C251-1‡ SMJ44C251-12‡ SMJ44C251-2‡	100 100 120 120	5 ± 10% 5 ± 5% 5 ± 10% 5 ± 5%	TBD	TBD	28, 28	HJ, JD	Military CMOS Multiport Video RAM	9-147
		SMJ44C251A-10‡ SMJ44C251A-1‡ SMJ44C251A-12‡ SMJ44C251A-2‡	100 100 120 120	5 ± 10% 5 ± 5% 5 ± 10% 5 ± 5%	635 635 550 550	90 90 83 83	28, 28	HJ, JD	Military CMOS Multiport Video RAM	9-149
		TMS44C260-60 TMS44C260-70 TMS44C260-80 TMS44C260-10	60 70 80 100	5 ± 10%	523 440 413 358	11	24/26	DJ	CMOS Parity and Enhanced Page Mode	8-73
		TMS4C1050-30 TMS4C1050-40 TMS4C1050-60	25 30 50	5 ± 10%	275 248 193	55	16, 20/26, 20	N, DJ, SD	CMOS Field Memory	8-125
		TMS4C1060-30 TMS4C1060-40 TMS4C1060-60	25 30 50	5 ± 10%	275 248 193	55	16, 20/26, 20	N, DJ, SD	CMOS Field Memory	8-125
		TMS4C1070-30‡ TMS4C1070-40‡ TMS4C1070-60‡	25 30 50	5 ± 10%	275 248 193	55	18, 20/26, 20	N, DJ, SD	CMOS Field Memory	8-141
	128K × 8	TMS48C121-80‡ TMS48C121-10‡ TMS48C121-12‡	80 100 120	5 ± 10%	660 523 468	193 193 165	40	DZ	CMOS Mulitport Video RAM	8-91
4096K	1024K × 4	TMS44460-60‡ TMS44460-70‡ TMS44460-80‡ TMS44460-10‡	60 70 80 100	5 ± 10%	523 468 413 358	11	24/26	DJ	CMOS Parity and Enhanced Page Mode	8-155

† N Plastic Dual In-Line (DIP)
DJ Plastic Small-Outline J-Lead (SOJ)
DZ Plastic Small-Outline J-Lead (SOJ)
FM Plastic Leaded Chip Carrier
HJ Ceramic Small-Outline J-Lead (Military) (SOJ)
JD Ceramic Side-Brazed Dual In-Line Package (Military) (DIP)
SD Plastic Zig-Zag In-Line Package (ZIP)

‡ Advance Information for product under development by TI

DRAM

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
256K × 4 Enhanced Page Mode	TI		TMS44C256
		AT&T	M441024
		Fujitsu	MB81C4256
		Hitachi	HM514256/8
		Hyundai	HY51C4256
		Micron	MT4C4256/MT4C4258
		Mitsubishi	M5M44C256
		Motorola	MCM514256A
		NEC	μPD424256
		NMB	AAA1M104
		OKI	MSM414256/MSM514256
		Panasonic	MN41C4256
		Samsung	KM44C256
		Sharp	LH64256/270
		Siemens	HYB514256
		Toshiba	TC514256
256K × 4 Military Enhanced Page Mode	TI		SMJ44C256
		Micron	MT4C4256
1 Meg × 1 Enhanced Page Mode	TI		TMS4C1024
		Fujitsu	MB81C1000
		Goldstar	GM71C1000
		Hitachi	HM511000
		Hyundai	HY51C1000
		Micron	MT4C1024/5/6
		Mitsubishi	M5M4C1000
		Mosaic	MDM11000
		NEC	μPD421000
		OKI	MSM41000
		Panasonic	MN41C1000
		Toshiba	TC511000
		Vitelic	V56C100
1 Meg × 1 Military Enhanced Page Mode	TI		SMJ4C1024
		Micron	MT4C1024

DRAM (Continued)

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
1 Meg x 1 Nibble Mode	TI		TMS4C1025
		Dense-Pac	DPD1MM1K
		Hitachi	HM511001
		Hyundai	HY51C1001
		Micron	MT4C1025
		Mitsubishi	M5M4C1001
		Motorola	MCM511001
		NEC	μDP421001
		NMB	AAA1M200
		OKI	MSM41001
		Samsung	KM41C1001
		Toshiba	TC511001
1 Meg x 1 Static Column Decode Mode	TI		TMS4C1027
		Fujitsu	MB81C1002
		Hitachi	HM511002
		Micron	MT4C1026
		Mitsubishi	M5M4C1002
		Motorola	MCM511002
		NEC	μPD421002
		NMB	AAA1M100
		OKI	MSM41002
		Samsung	KM41C1002
		Siemens	HYB511002
		Toshiba	TC511002
1 Meg x 4 Enhanced Page Mode	TI		TMS44400
	TI		TMS44410 (write-per-bit)
		Fujitsu	MB814400
		Hitachi	HM514400
		Micron	MT4C4001/003
		Mitsubishi	M5M44400
		Mosaic	MDM41000
		Motorola	MCMS14400
		NEC	μPD424400
		NMB	AAA4M104
		OKI	MSM514400
		Panasonic	MN41C41000
		Samsung	KM44C1000
		Siemens	HYB514400
		Toshiba	TC514400

† Product under development by TI

DRAM (Concluded)

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
1 Meg × 4 Military Enhanced Page Mode	TI	 Micron	SMJ44400† MT4001
4 Meg × 1 Enhanced Page Mode	TI	 Dense-Pac Fujitsu Hitachi Micron Mitsuibishi Mosaic Motorola NEC NMB OKI Panasonic Samsung Siemens Toshiba	TMS44100 DPD4MM1K MB814100 HM514100 MT4C1004/5/6 M5M44100 MDM14000 MCM514100 mPD424100 AAA4M100 MSM514100 MN41C4000 KM41C4000/44C1000 HYB514100 TC514100
4 Meg × 1 Military Enhanced Page Mode	TI	 Micron	SMJ44100† MT4C1004
4 Meg × 1 Nibble Mode	TI	 Mitsubishi NEC OKI	TMS44101 M5M44101 μPD424101 MSM5144101
4 Meg × 4 Enhanced Page Mode	TI	 Hitachi	TMS416400† HM511640
16 Meg × 1 Enhanced Page Mode	TI	 Hitachi	TMS416100† HM511610

† Product under development by TI

DRAM Modules

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
256K x 9	TI		TM256GU9
		Fujitsu	MB85240
		Hitachi	HB561003/HB561409
		Micron	MT9259/MT8C9259
		OKI	MSC2304YS9
1 Meg x 8	TI		TM024GAD8
		Dense-Pac	DPD1MX8
		Fujitsu	MB85230/MB855231
		Fujitsu	MB85250
		Hitachi	HB56A181/HB56C18
		Micron	MT8C8024/25/26
		Mitsubishi	MH1M08A
		Motorola	MCM81000
		NEC	MC-421000A8
		OKI	MSC2313A
		Samsung	KMM581000
		Toshiba	THM81000
1 Meg x 8	TI		TM124GU8A
		Dense-Pac	DPD1MX8
		Fujitsu	MB85230/MB855231
		Fujitsu	MB85250
		Hitachi	HB56A181/HB56C18
		Micron	MT8C8024/25/26
		Mitsubishi	MH1M08A
		Motorola	MCM81000
		NEC	MC-421000A8
		OKI	MSC2313A
		Samsung	KMM581000
		Toshiba	THM81000
1 Meg x 9	TI		TM024EAD9
		Dense-Pac	DPD1MX9
		Fujitsu	MB85235/MB85237
		Fujitsu	MB85265
		Hitachi	HB56A19/HB56C19
		Micron	MT8C9024/25/26
		Mitsubishi	MH1M09A
		Motorola	MCM9L1000
		Samsung	KMM591000
		Siemens	HYM910005
		Toshiba	THM91000

DRAM Modules (Continued)

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
1 Meg × 9	TI		TM124EAD9B
		Dense-Pac	DPD1MX8
		Fujitsu	MB85230/MB855231
		Fujitsu	MB85250
		Hitachi	HB56A181/HB56C18
		Micron	MT8C8024/25/26
		Mitsubishi	MH1M08A
		Motorola	MCM81000
		NEC	MC-421000A9
		OKI	MSC2312
		Samsung	KMM581000
		Toshiba	THM81000
1 Meg × 9	TI		TM124EAD9C
		Dense-Pac	DPD1MX9
		Fujitsu	MB85235/MB85237
		Fujitsu	MB85265
		Hitachi	HB56A19/HB56C19
		Micron	MT8C9024/25/26
		Mitsubishi	MH1M09A
		Motorola	MCM9L1000
		NEC	MC-421000A9
		OKI	MSC2312
		Samsung	KMM591000
		Siemens	HYM910005
		Toshiba	THM91000
4 Meg × 8	TI		TM4100GBD8
		Dense-Pac	DPD4MX8
		Hitachi	HB56A48A
4 Meg × 9	TI		TM4100EBD9
		Dense-Pac	DPD4MX9
		Hitachi	HB56A49A
		NEC	MC-424100A9
		OKI	MSC2340
		Siemens	HYM940005
256K × 36	TI		TM256KBK36B
	TI		TM256KBK36C
		Hitachi	HB56D25636
		Micron	MT8C36256
		NEC	MC-424256A36
		OKI	MSC2320A
		Samsung	KMM36256
		Toshiba	THM3625600A
		Vitelic	VM55C104K36

DRAM Modules (Concluded)

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
512K × 36	TI		TM512LBK36B
	TI		TM512LBK36C
		Hitachi	HB56D51236
		Micron	MT8C36512
		NEC	MC-424512A36
		OKI	MSC2321A
		Samsung	KMM36512
		Toshiba	THM365120AS
		Vitelic	VM55C1042K36
1 Meg × 36	TI		TM124MBK36A
	TI		TM124MBK36B
		Hitachi	HB56D136B
		NEC	MC-421000A36

EPROMs/OTPs/Flash EEPROMs

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
16K × 8	TI		TMS27C128
CMOS	TI		TMS27PC128
		AMD	AM27C128
		Atmel	AT27C128
		Cypress	CY7C251
		Fujitsu	MBM27C128/MBM27128
		GI	27C128
		Intel	27C128
		Hitachi	HN27128A/HN4827128G
		Microchip	27HC256
		Mitsubishi	M5L27128/M5M27C128
		National	NMC27CP128
		NEC	mPD27128
		OKI	MSM27128/MSM27C128
		S-MOS	SPM27129C
		SEEQ	27128
		Sharp	LH57126/7/8
		Toshiba	TMM27128
		VLSI	VT27C128
		VTI	VT27C128
		Waferscale	WS57C128F/WS57C251
16K × 8	TI		SMJ27C128
Military		AMD	AM27128
CMOS		Intel	MD27128A
		Microchip	27C128
		SEEQ	27128

EPROMs/OTPs/Flash EEPROMs (Continued)

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
32K × 8	TI		TMS27C256
CMOS	TI		TMS27PC256
		AMD	Am27C256/Am27256
		Atmel	AT27C256/AT27256
		Catalyst	CAT27HC256
		Cypress	CY7C271/4/7/9
		Fujitsu	MBM27C256/MBM27256
		Hitachi	HN27C256/HN27256
		GI	27C256/27256
		Intel	27256/27C256
		Microchip	27C256
		Mitsubishi	M5M27C256/M5L27256
		Motorola	MCM67256/9
		National	NMC27C256
		NEC	mPD27256
		OKI	MSM27C256/MSM27256
		Panatech	RD27C256
		S-MOS	SPM27C256
		SEEQ	27C256
		SGS	M27256A
		Sharp	LH57254/5/6
		Signetics	27C256
		Thomson	TS27C256
		Toshiba	TMM27256/TC57256/54256
		Waferscale	WS57C256F
32K × 8	TI		SMJ27C256
Military		AMD	Am27256
CMOS		Atmel	AT27C256
		Intel	MD27256/27C256
		Microchip	27C256
		SEEQ	DM27256/27C256
		Signetics	27C256
32K × 8	TI		TMS29F256 (5-V EEPROM)
Flash EEPROM	TI		TMS29F258 (5-V EEPROM)
	TI		TMS29F259 (5-V EEPROM)
		AMD	Am28F256
		Intel	28F256 (12-V EPROM)

EPROMs/OTPs/Flash EEPROMs (Continued)

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
64K × 8	TI		TMS27C512
CMOS	TI		TMS27PC512
	TI		TMS27C510†
	TI		TMS27PC510†
		AMD	Am27512/Am27C512
		Atmel	AT27C512
		Catalyst	CAT27512
		Cypress	CY7C285/6/7/9
		Fujitsu	MBM27C512
		GI	27C512
		Hitachi	HN27512
		Intel	27C512
		Mitsubishi	M5L27512
		National	NMC27C512
		NEC	mPD27C512
		OKI	MSM27512
		Panatech	TMS27C512
		Toshiba	TMM27512/TC57512/54512
64K × 8	TI		SMJ27C512
Military		AMD	Am27512
CMOS		Atmel	AT27C512
		Intel	MD27512
		Microchip	27C512
64K × 8	TI		TMS29F512†
Flash EEPROM		AMD	Am28F512
		Intel	28F512 (12-V EPROM)
		National	NMC48F512
64K × 16	TI		TMS27C210A
CMOS	TI		TMS27PC210A
		AMD	Am27C1024
		Atmel	AT27C1024
		Catalyst	CAT27C210
		Fujitsu	MBM27C1024
		Hitachi	HN27C1024
		Intel	27C210
		Microchip	27HC1616
		National	NMC27C1024
		NEC	mPD27C1000
		OKI	MSM271024/MSM27C1024
		SGS	M27C1024
		Toshiba	TC571024
		Waferscale	WS27C210

† Product under development by TI

EPROMs/OTPs/Flash EEPROMs (Concluded)

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
64K × 16 Military CMOS	TI	 Atmel	SMJ27C210 AT27C1024
128K × 8 CMOS	TI TI	 AMD Atmel Catalyst Dense-Pac Fujitsu Hitachi Intel Mosaic Mitsubishi NEC National OKI SGS Sharp Toshiba Waferscale	TMS27C010A TMS27PC010A Am27C010 AT27C010 CAT27010 DPV27C101 MBM27C1000/1 HN27C101/301 27C010 MLM8128 M5M27C100/1/2 μPD27C1000 NMC27C010/020 MCM271000 M27C1011 LH571000/0001 TC571000/TC54100 WS27C010
128K × 8 Military CMOS	TI	 AMD Atmel	SMJ27C010 Am27C010 AT27C010
128K × 8 CMOS Flash EEPROM	TI	 AMD Catalyst Hitachi Intel SEEQ Signetics	TMS29F010† Am28F010 CAT28F010 HN29C101 28F010 (12-V EPROM) 28C010 48F010
256K × 8 CMOS	TI	 AMD Intel Mitsubishi National	TMS27C020† Am27C020/2048 27C020 M5M27C201/2 NMC27020
512K × 8 CMOS	TI TI	 AMD Intel Mitsubishi National Toshiba	TMS27C040† TMS27PC040† Am27C040 27C040 M5M27C402 NMC27040 TC57400
256K × 16 CMOS	TI TI	 AMD Hitachi	TMS27C240† TMS27PC240† Am27C04096 HN27C4096

† Product under development by TI

Application Specific Memories

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
256K x 4	TI		TMS44C250
Video RAM	TI		TMS44C251
		Fujitsu	MB81C4251/MB81C4253
		Hitachi	HM534251/2/3
		NEC	μPD42274
		Micron	MT42C4256
		Mitsubishi	M5M442256
		OKI	MSM514251/MSM514252
		Samsung	KM42C4256
		Toshiba	TC524256/TC524257
256K x 4	TI		SMJ44C250†
Military	TI		SMJ44C251†
Video RAM	TI		SMJ44C251A†
		Micron	MT42C4256 883C
256K x 4	TI		TMS44C260
Parity		Micron	MT4C1664
128K x 8	TI		TMS48C121†
Video RAM		Hitachi	HM538121/2/3
		Micron	MT42C8128
		Mitsubishi	N5N482128
		NEC	μPD424400
		Toshiba	TC528126A

† Product under development by TI

GENERAL CONCEPTS AND TYPES OF MEMORIES

Address – Any given memory location in which data can be stored or from which it can be retrieved.

Automatic Chip-Select/Power Down – see Chip Enable Input.

Bit – Contraction of Binary digIT; i.e., a 1 or a 0. In electrical terms, the value of a bit may be represented by the presence or absence of charge, voltage, or current.

Byte – A word of 8 bits (see Word).

C of C – Certification of Conformance.

CDIP – Ceramic Dual In-Line Package.

CERPAC – CERamic flat PACk (hermetic).

CMOS – A complementary MOS technology that uses transisitors with electron (N-channel) and hole (P-channel) conduction.

Chip Enable Input – A control input to an integrated circuit that, when active, permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and, when inactive, causes the integrated circuit to be in a reduced-power standby mode.

Chip Select Input – Chip select inputs are gating inputs that control the input to and output from the memory. They may be of two kinds:

1. Synchronous – Clocked/latched with the memory clock. Affects the inputs and outputs for the duration of that memory cycle.
2. Asynchronous – Has direct asynchronous control of inputs and outputs. In the read mode, an asynchronous chip select functions like an output enable.

Column Address Strobe ($\overline{\text{CAS}}$) – A clock used in dynamic RAMs to control the input of column addresses. It can be active high (CAS) or active low ($\overline{\text{CAS}}$).

CPAK – Ceramic flatPAcK.

CSOJ – Ceramic Small-Outline J-lead integrated circuit package.

CZIP – Ceramic Zig-zag In-line Package.

Data – Any information stored or retrieved from a memory device.

Die – Unpackaged semiconductor.

DIP – Dual In-line Package.

DESC – Defense Electronics Supply Center.

Dynamic (Read/Write) Memory (DRAM) – A read/write memory in which the cells require the repetitive application of control signals in order to retain the stored data.

NOTES:

1. The words "read/write" may be omitted from the term when no misunderstanding will result.
2. Such repetitive application of the control signals is normally called a refresh operation.
3. A dynamic memory may use static addressing or sensing circuits.
4. This definition applies whether the control signals are generated inside or outside the integrated circuit.

Electrically Erasable Programmable Read-Only Memory (EEPROM) – A nonvolatile memory that can be field-programmed like an OTP PROM or EPROM but that can be electrically erased by a combination of electrical signals at its inputs.

EPIC – Enhanced Performance Implanted CMOS.

Erasable and Programmable Read-Only Memory (EPROM) – A field-programmable read-only memory that can have the data content of each memory cell altered more than once.

Erase – Typically associated with EPROMs and EEPROMs. The procedure whereby programmed data is removed and the device returns to its unprogrammed state.

ESD – Electrostatic Discharge.

Field Memory (FMEM) – A serial-access memory that performs high-speed, asynchronous read/write operations. (Used mainly for fields of digital TV/VTR that require higher speed operation, lower power consumption, and larger capacity.)

Fit – Originally stood for Failures-In-Time. Currently means a failure rate of one failure in one billion hours.

FRAM – First-in first-out pseudo-static RAM or Field RAM.

Field-Programmable Read-Only Memory – See One-Time Programmable Read-Only Memory.

Fixed Memory – A common term for ROMs, EPROMs, EEPROMs, etc., containing data that is not normally changed. A more precise term for EPROMs and EEPROMs is nonvolatile since their data may be easily changed.

Fully Static RAM – In a fully static RAM, the periphery as well as the memory array is fully static. The periphery is thus always active and ready to respond to input changes without the need of clocks. There is no precharge required for static periphery.

GENERIC DATA – Group A, B, C, & D Quality Conformance Data.

JAN – Joint Army Navy. Specifically, a JM38510 qualified device.

JANB – Class B screened JAN device.

JANS – Class S screened JAN device.

JEDEC – Joint Electronic Device Engineering Council.

JTAG – Joint Testability Action Group.

K – When used in the context of specifying a given number of bits of information, $1K = 2^{10} = 1024$ bits. Thus, $64K = 64 \times 1024 = 65\,536$ bits.

Large-Scale Integration (LSI) – The description of any IC technology that enables condensing more than 100 gates onto a single chip.

LDCC – Ceramic Leaded Chip Carrier.

LCCC – Leadless Ceramic Chip Carrier.

Mask-Programmed Read-Only Memory – A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask, the data content thereafter being unalterable.

Memory – A medium capable of storing information that can be retrieved.

Memory Card – A pocket-size memory storage system.

Memory Cell – The smallest subdivision of a memory into which a unit of data has been or can be entered in which it is or can be stored, and from which it can be retrieved.

Metal-Oxide Semiconductor (MOS) – The technology involving photolithographic layering of metal and oxide to produce a semiconductor device.

MIL-M-38510 – A military controlling specification pertaining mainly to JAN qualified devices (microcircuits).

MIL-STD-883 – A military controlling specification containing detailed descriptions of the screening processes pertaining to Class B and Class S devices (microcircuits).

NMOS – A type of MOS technology in which the basic conduction mechanism is governed by electrons. (Short for N-channel MOS.)

Nonvolatile Memory – A memory in which the data content is maintained whether the power supply is connected or not.

OTP – One-Time Programmable.

One-Time Programmable (OTP) Read-Only Memory – A read-only memory that, after being manufactured, can have the data content of each memory cell altered once. Also referred to as OTP.

Output Enable – A control input that, when true, permits data to appear at the memory output, and when false, causes the output to assume a high-impedance state. (See also chip select.)

PDIP – Plastic Dual-In-line Package.

PLCC – Plastic Leaded Chip Carrier.

PMOS – A type of MOS technology in which the basic conduction mechanism is governed by holes. (Short for P-channel MOS.)

Parallel Access – A feature of a memory by which all the bits of a byte or word are entered simultaneously at several inputs or retrieved simultaneously from several outputs.

Power Down – A mode of a memory during which the device is operating in a low-power or standby mode. Normally read or write operations of the memory are not possible under this condition.

Program – Typically associated with EPROM and OTP memories, the procedure whereby logical 0s (or 1s) are stored into various desired locations in a previously erased device.

Program Enable – An input signal that, when true, puts a programmable memory device into the program mode.

Programmable Read-Only Memory (PROM) – See One-Time Programmable (OTP) Read-Only Memory.

Printed Wiring Board (PWB) – A substrate of epoxy glass, clad material, or other material upon which a pattern of conductive traces is formed to interconnect the components that will be mounted upon it.

Read – A memory operation whereby data is output from a desired address location.

Read-Only Memory (ROM) – A memory in which the contents are not intended to be altered during normal operation. NOTE: Unless otherwise qualified, the term "read-only memory" implies that the contents are determined by its structure and are unalterable.

Read/Write Memory – A memory in which each cell may be selected by applying appropriate electrical input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electrical input signals.

Row Address Strobe ($\overline{\text{RAS}}$) – A clock used in dynamic RAMs to control the input of the row addresses. It can be active high (RAS) or active low ($\overline{\text{RAS}}$).

SCD – Source Control Drawings.

Scaled-MOS (SMOS) – MOS technology under which the device is scaled down in size in three dimensions and in operating voltages allowing improved performance.

Semi-Static (Quasi-Static, Pseudo-Static) RAM – In a semi-static RAM, the periphery is clock-activated (i.e., dynamic). Thus the periphery is inactive until clocked, and only one memory cycle is permitted per clock. The peripheral circuitry must be allowed to reset after each active memory cycle for a minimum precharge time. No refresh is required.

Serial Access – A feature of a memory by which all the bits are entered sequentially at a single input or retrieved sequentially from a single output.

SIP – Single In-line Package.

Small Outline Integrated Circuit (SOIC) – A package in which an integrated circuit chip can be mounted to form a surface-mounted component. It is made of a plastic material that can withstand high temperatures and has leads formed in a gull-wing shape along its two longer sides for connection to a PWB footprint.

SMD – Standard Military Drawing.

SOLCC – Small Outline Leadless ceramic Chip Carrier.

SOJ – Small Outline J-lead package.

Static RAM (SRAM) – A read/write random-access device within which information is stored as latched voltage levels. The memory cell is a static latch that retains data as long as power is applied to the memory array. No refresh is required. The type of periphery circuitry sub-categorizes static RAMs.

ThinSOJ – Thin Small-Outline J-lead package.

ThinSOP – Thin Small-Outline package.

Very-Large-Scale Integration (VLSI) – The description of an IC technology that is much more complex than large-scale integration (LSI) and involves a much higher equivalent gate count. At this time an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.

Video RAM (VRAM) – A dual-port dynamic random-access memory with a on-chip serial data register.

Volatile Memory – A memory in which the data content is lost when the power supply is disconnected.

Word – A series of one or more bits that occupy a given address location and then can be stored and retrieved in parallel.

Write – A memory operation whereby data is written into a desired address location.

Write Enable – A control signal that when true causes the memory to assume the write mode, and when false causes it to assume the read mode.

ZIP – Zig-zag In-line Package.

OPERATING CONDITIONS AND CHARACTERISTICS (INCLUDING LETTER SYMBOLS)

Capacitance

The inherent capacitance on every pin, which can vary with various inputs and outputs.

Example symbology:

C_i	Input capacitance
C_o	Output capacitance
$C_{i(D)}$	Input capacitance, data input

Current

High-level input current, I_{IH}

The current into an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}

The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input current, I_{IL}

The current into an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}

The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state (high-impedance state) output current (of a three-state output,) I_{OZ}

The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}

The current into* an output when the output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{BB}, I_{CC}, I_{DD}, I_{PP}

The current into, respectively, the V_{BB}, V_{CC}, V_{DD}, V_{PP} supply terminals.

*Current out of a terminal is given as a negative value.

Operating Free-Air Temperature

The temperature (T_A) range over which the device will operate and meet the specified electrical characteristics.

Voltage

High-level input voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic elment within specification limits is guaranteed.

Low-level output voltage, V_{OL}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

Supply voltages, V_{BB}, V_{CC}, V_{DD}, V_{PP}

The voltages supplied to the corresponding voltage pins that are required for the device to function. From one to four of these supplies may be necessary, along with ground V_{SS}.

Time Intervals

New or revised data sheets in this book use letter symbols in accordance with standards recently adopted by JEDEC, the IEEE, and the IEC. Two basic forms are used. The first form is usually used in this book when intervals can easily be classified as access, cycle, disable, enable, hold, refresh, setup, transistion, or valid times and for pulse durations. The second form can be used generally but in this book primarily for time intervals not easily classifiable. The second (unclassified) form will be described first. Since some manufacturers use this form for all time intervals, symbols in the un-classified form are given with the examples for most of the classified time intervals.

Unclassified time intervals

Generalized letter symbols can be used to identify almost any time interval without classifying it using traditional or contrived definitions. Symbols for unclassified time intervals identify two signal events listed in from-to sequence using the format:

$t_{AB\text{-}CD}$

Subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval. Every effort is made to keep the A and C subscript length down to one letter, if possible (e.g., R for $\overline{RAS}$ and C for $\overline{CAS}$).

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high

L = low or transition to low

V = a valid steady-state level

X = unknown, changing, or "don't care" level

Z = high-impedance (off) state

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur.

For examples of symbols of this type, see TMS44C256 (e.g., t_{RLCL}).

Classified time intervals (general comments, specific times follow)

Because of the information contained in the definitions, frequently the identification of one or both of the two signal events that begin and end the intervals can be significantly shortened compared to the unclassified forms. For example, it is not necessary to indicate in the symbol that an access time ends with valid data at the output. However, if both signals are named (e.g., in a hold time), the from-to sequence is maintained.

Access time

The time interval between the application of a specific input pulse and the availability of valid signals at an output.

Example symbology:

Classifed	Unclassified	Description
$t_{a(A)}$	t_{AVQV}	Access time from address
$t_{a(S)}$, $t_{a(CS)}$	t_{SLQV}	Access time from chip select (low)

Cycle time

The time interval between the start and end of a cycle.

NOTE: The cycle time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval that must be allowed for the digital circuit to perform a specified function (e.g., read, write, etc.) correctly.

Example symbology:

Classifed	Unclassified	Description
$t_{c(R)}$, $t_{c(rd)}$	$t_{AVAV(R)}$	Read cycle time
$t_{c(W)}$	$t_{AVAV(W)}$	Write cycle time

NOTE: R is usually used as the abbreviation for "read"; however, in the case of dynamic memories, "rd" is used to permit R to stand for $\overline{RAS}$.

Disable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Example symbology:

Classifed	Unclassified	Description
$t_{dis(S)}$	t_{SHQZ}	Output disable time after chip select (high)
$t_{dis(W)}$	t_{WLQZ}	Output disable time after write enable (low)

These symbols supersede the older forms t_{PVZ} or t_{PXZ}.

Enable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: For memories these intervals are often classified as access times.

Example symbology:

Classifed	Unclassified	Description
$t_{en(SL)}$	t_{SLQV}	Output enable time after chip select low

These symbols supersede the older from t_{PZV}.

Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classifed	Unclassified	Description
$t_{h(D)}$	t_{WHDX}	Data hold time (after write high)
$t_{h(RHrd)}$	t_{RHWH}	Read (write enable high) hold time after $\overline{RAS}$ high
$t_{h(CHrd)}$	t_{CHWH}	Read (write enable high) hold time after $\overline{CAS}$ high
$t_{h(CLCA)}$	$t_{CL\text{-}CAX}$	Column address hold time after $\overline{CAS}$ low
$t_{h(RLCA)}$	$t_{RL\text{-}CAX}$	Column address hold time after $\overline{RAS}$ low
$t_{h(RA)}$	$t_{RL\text{-}RAX}$	Row address hold time (after $\overline{RAS}$ low)

These last three symbols supersede the older forms:

NEW FORM	OLD FORM
$t_{h(CLCA)}$	$t_{h(AC)}$
$t_{h(RLCA)}$	$t_{h(ARL)}$
$t_{h(RA)}$	$t_{h(AR)}$

NOTE: The from-to sequence in the order of subscripts in the unclassified form is maintained in the classified form. In the case of hold times, this causes the order to seem reversed from what would be suggested by the terms.

Pulse duration (width)

The time interval between the specified reference points on the leading and trailing edges of the pulse waveform.

Example symbology:

Classifed	Unclassified	Description
$t_{w(W)}$	t_{WLWH}	Write pulse duration
$t_{w(RL)}$	t_{RLRH}	Pulse duration, $\overline{RAS}$ low

Refresh time interval

The time interval between the beginnings of successive signals that are intended to restore the level in a dynamic memory cell to its original level.

NOTE: The refresh time interval is the actual time interval between two refresh operations and is determined by the system in which the digital circuit operates. A maximum value is specified that is the longest interval for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classifed	Unclassified	Description
t_{rf}		Refresh time interval

Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classifed	Unclassified	Description
$t_{su(D)}$	t_{DVWH}	Data setup time (before write high)
$t_{su(CA)}$	t_{CAV-CL}	Column address setup time (before $\overline{CAS}$ low)
$t_{su(RA)}$	t_{RAV-RL}	Row address setup time (before $\overline{RAS}$ low)

Transition times (also called rise and fall times)

The time interval between two reference points (10% and 90% unless otherwise specified) on the same waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

Example symbology:

Classifed	Unclassified	Description
t_t		Transition time (general)
$t_{t(CH)}$	t_{CHCH}	Low-to-high transition time of $\overline{CAS}$
$t_{r(C)}$	t_{CHCH}	$\overline{CAS}$ rise time
$t_{f(C)}$	t_{CLCL}	$\overline{CAS}$ fall time

Valid time

(a) General

The time interval during which a signal is (or should be) valid.

(b) Output data-valid time

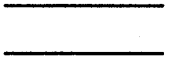
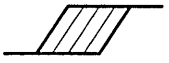
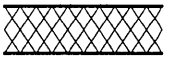
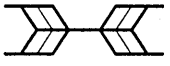
The time interval in which output data continues to be valid following a change of input conditions that could cause the output data to change at the end of the interval.

Example symbology:

Classified	Unclassified	Description
$t_{v(A)}$	t_{AXQX}	Output data valid time after change of address

This supersedes the older form t_{PVX}.

TIMING DIAGRAMS CONVENTIONS

Timing Diagram Symbol	Meaning: Input Forcing Functions	Meaning: Output Response Functions
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated intervals
	Low-to-high changes permitted	Will be changing from low to high sometime during designated intervals
	Don't care	State unknown or changing
	(Does not apply)	Centerline represents high-impedance (off) state.

BASIC DATA SHEET STRUCTURE

The front page of the data sheet begins with a list of key features such as organization, interface, compatibility, operation (static or dynamic), access and cycle times, technology (N- or P-channel, silicon or metal oxide gate), and power. In addition, the top view of the device is shown with the pinout provided. Next a general description of the device, system interface considerations, and elaboration on other device characteristics are presented. The next section is an explanation of the device's operation which includes the function of each pin (i.e., the relationship between each input (output) and a given type of memory). The functions basically involve starting, achieving, and ending a given type of memory cycle (e.g., programming or erasing EPROMs, or reading a memory location).

Augmenting the descriptive text there appears a logic symbol prepared in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12 and explained in Section 11 of this book. Following the symbol is usually a functional block diagram, a flowchart of the basic internal structure of the device showing the signal paths for data, addresses, and control signals, as well as the internal architecture. Usually the next few pages contain the absolute maximum ratings (e.g., voltage supplies, input voltage, and temperature) applicable over the operating free-air temperature range. If the device is used outside of these values, it may be permanently destroyed or at least it would not function as intended. Next, typically, are the recommended operating conditions, (e.g., supply voltages, input voltages, and operating temperature). The memory device is guaranteed to work reliably and to meet all data sheet parameters when operated in accord with the recommended operating conditions and within the specified timing. If the device is operated outside of these limits (minimum/maximum), it is no longer guaranteed to meet the data sheet parameters. Operation beyond the absolute maximum ratings can result in catastrophic failures.

The next section provides a table of electrical characteristics over full ranges of recommended operating conditions (e.g., input and output currents, output voltages, etc.). These are presented as minimum, typical, and maximum values. Typical values are representative of operation at an ambient temperature of $T_A = 25°$ C with all power supply voltages at nominal value. Next, input and output capacitances are presented. Each pin has a capacitance (whether an input, an output, or control pin). Minimum capacitances are not given, as the typical and maximum values are the most crucial.

The next few tables involve the device timing characteristics. The parameters are presented as minimum, typical (or nominal), and maximum. The timing requirements over recommended ranges of supply voltage and operating free-air temperature indicate the device control requirements such as hold times, setup times, and transition times. These values are referenced to the relative positioning of signals on the timing diagrams, which follow. The switching characteristics over recommended supply voltage range are device performance characteristics inherent to device operation once the inputs are applied. These parameters are guaranteed for the test conditions given. The interrelationship of the timing requirements to the switching characteristics is illustrated in timing diagrams for each type of memory cycle (e.g., read, write, program.)

At the end of a data sheet additional applications information may be provided such as how to use the device, graphs of electrical characteristics, or other data on electrical characteristics.

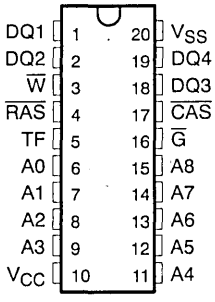
This data sheet is applicable to all TMS44C256s symbolized with Revision "D" and subsequent revisions as described on page 5-21.

- **262 144 × 4 Organization**
- **Single 5-V Supply (10% Tolerance)**
- **Performance Ranges:**

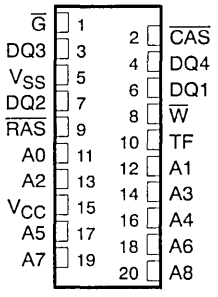
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS44C256-60	60 ns	15 ns	30 ns	110 ns
TMS44C256-70	70 ns	18 ns	35 ns	130 ns
TMS44C256-80	80 ns	20 ns	40 ns	150 ns
TMS44C256-10	100 ns	25 ns	45 ns	180 ns
TMS44C256-12	120 ns	30 ns	55 ns	220 ns

- **Enhanced Page Mode Operation with $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 512-Cycle Refresh in 8 ms (Max)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs and Clocks Are TTL Compatible**
- **High-Reliability Plastic 20-Pin 300-Mil-Wide DIP, 20/26 J-Lead Surface Mount (SOJ) ('44C256-60 and '44C256-70 Available in SOJ Only), 20/26 J-Lead Thin Surface Mount (ThinSOJ), or 20-Pin Zig-Zag In-Line (ZIP) Packages**
- **Operation of TI's Megabit CMOS DRAMs Can Be Controlled by TI's SN74ALS6301 and SN74ALS6302 Dynamic RAM Controllers**
- **Operating Free-Air Temperature . . . 0°C to 70°C**

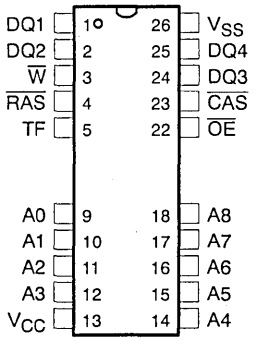
N Package
(Top View)



SD Package
(Top View)



DJ and DN Packages†
(Top View)



†The packages shown here are for pinout reference only. The DJ package is actually 75% of the length of the N package.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Data-Output Enable
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS44C256 series are high-speed, 1 048 576-bit dynamic random access memories, organized as 262 144 words of four bits each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at low cost.

EPIC is a trademark of Texas Instruments Incorporated

description (continued)

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, 100 ns, and 120 ns. Maximum power dissipation is as low as 305 mW operating and 11 mW standby on 120 ns devices.

The EPIC technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{CC} peaks are 140 mA typical, and a – 1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 54/74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS44C256 is offered in a 20-pin dual-in-line (N suffix) package, a 20-pin zig-zag in-line (SD suffix) package, a 20/26 J-lead plastic surface mount SOJ (DJ suffix), and a 20/26 J-lead thin plastic surface mount SOJ (DN suffix). The TMS44C256-60 and TMS44C256-70 are available in the 20/26 J-lead plastic surface mount SOJ (DJ suffix) only. These packages are guaranteed for operation from 0°C to 70°C.

operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS44C256 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as "enhanced page mode." Valid column address may be presented immediately after $t_{h(RA)}$ (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting a write operation with $\overline{G}$ grounded.

data in (DQ1-DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{G}$ must be high to bring the output buffers to high-impedance prior to impressing data on the I/O lines.

data out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{G}$ are brought low. In a read cycle the output becomes valid after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying $t_{d(GHD)}$.

output enable ($\overline{G}$)

$\overline{G}$ controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every eight milliseconds to retain data. This can be achieved by strobing each of the 512 rows (A0-A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter $t_{d(CLRL)R}$] and holding it low after $\overline{RAS}$ falls [see parameter $t_{d(RLCH)R}$]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

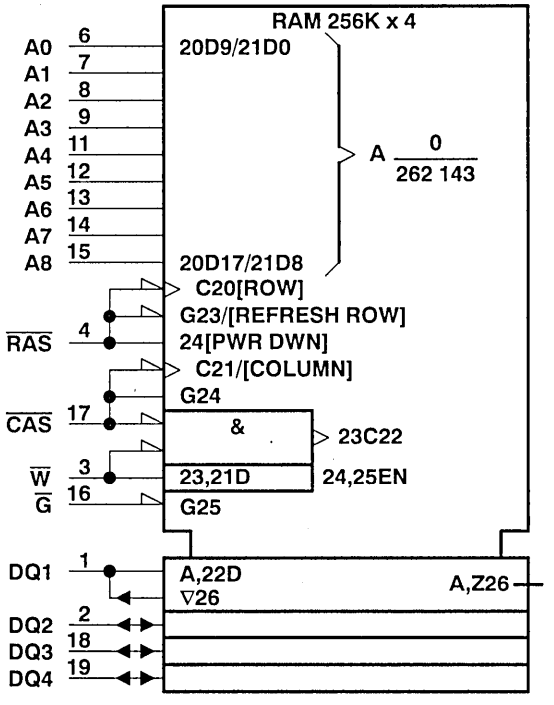
power-up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after power-up to the full V_{CC} level.

test function pin

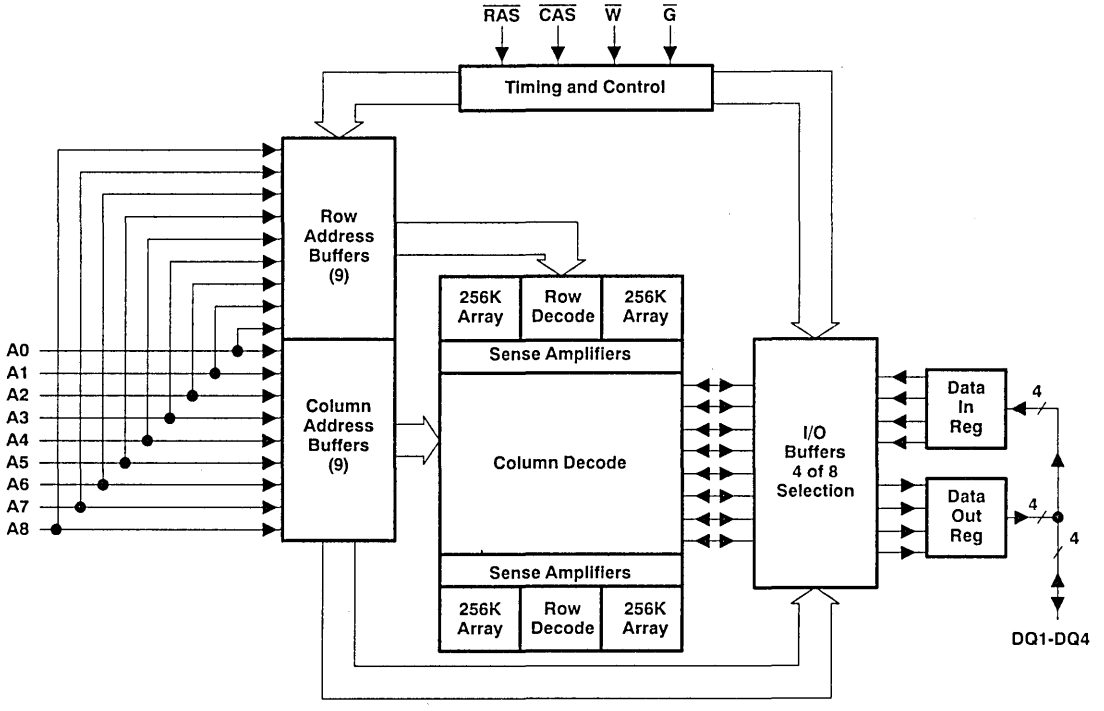
During normal device operation the TF pin must either be disconnected or biased at a voltage less than or equal to V_{CC}.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS44C256-60		TMS44C256-70		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 5.8 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10	µA
I_{CC1}	Read/write cycle current	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V		95		80	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		2		2	mA
I_{CC3}	Average refresh circuit ($\overline{RAS}$-only, or CBR)	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low, after $\overline{CAS}$ low (CBR)		90		80	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60	mA

PARAMETER		TEST CONDITIONS	TMS44C256-80		TMS44C256-10		TMS44C256-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 5.8 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read/write cycle current	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V		75		65		55	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		2		2		2	mA
I_{CC3}	Average refresh circuit ($\overline{RAS}$-only, or CBR)	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low, after $\overline{CAS}$ low (CBR)		70		60		50	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		45		35	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			5	pF
$C_{i(W)}$	Input capacitance, write-enable input			5	pF
$C_{i(G)}$	Input capacitance, output-enable input			5	pF
C_O	Output capacitance			7	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER		ALT. SYMBOL	TMS44C256-60		TMS44C256-70		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}		15		18	ns
$t_{a(CA)}$	Access time from column-address	t_{CAA}		30		35	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low	t_{RAC}		60		70	ns
$t_{a(G)}$	Access time from $\overline{G}$ low	t_{GAC}		15		18	ns
$t_{a(CP)}$	Access time from column precharge	t_{CAP}		35		40	ns
$t_{d(CLZ)}$	$\overline{CAS}$ low to output in low Z	t_{CLZ}	0		0		ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)	t_{OFF}	0	15	0	18	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high (see Note 4)	t_{GOFF}	0	15	0	18	ns

PARAMETER		ALT. SYMBOL	TMS44C256-80		TMS44C256-10		TMS44C256-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}		20		25		30	ns
$t_{a(CA)}$	Access time from column-address	t_{CAA}		40		45		55	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low	t_{RAC}		80		100		120	ns
$t_{a(G)}$	Access time from $\overline{G}$ low	t_{GAC}		20		25		30	ns
$t_{a(CP)}$	Access time from column precharge	t_{CAP}		40		50		60	ns
$t_{d(CLZ)}$	$\overline{CAS}$ low to output in low Z	t_{CLZ}	0		0		0		ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)	t_{OFF}	0	20	0	25	0	30	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high (see Note 4)	t_{GOFF}	0	20	0	25	0	30	ns

NOTE 4: $t_{dis(CH)}$ and $t_{dis(G)}$ are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

PARAMETER		ALT. SYMBOL	TMS44C256-60		TMS44C256-70		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	110		130		ns
$t_{c(W)}$	Write cycle time	t_{WC}	110		130		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	155		181		ns
$t_{c(P)}$	Page-mode read or write cycle time (see Note 7)	t_{PC}	40		45		ns
$t_{c(PM)}$	Page-mode read-modify-write cycle time	t_{PCM}	85		96		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	15	10 000	18	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	40		50		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	60	10 000	70	10 000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RASP}	60	100 000	70	100 000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		15		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ low (see Note 10)	t_{DS}	0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	15		18		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	15		18		ns
$t_{h(CA)}$	Column-address hold time after $\overline{RAS}$ low	t_{CAH}	10		15		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	10		10		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	50		55		ns

Continued next page.

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. To guarantee $t_{c(P)}$ min, $t_{su(CA)}$ should be greater than or equal to $t_{w(CH)}$.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. (Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$]).
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. (Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$]).
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

PARAMETER		ALT. SYMBOL	TMS44C256-80		TMS44C256-10		TMS44C256-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	150		180		220		ns
$t_{c(W)}$	Write cycle time	t_{WC}	150		180		220		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	205		245		295		ns
$t_{c(P)}$	Page-mode read or write cycle time (see Note 7)	t_{PC}	50		55		65		ns
$t_{c(PM)}$	Page-mode read-modify-write cycle time	t_{PCM}	100		120		135		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		15		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	20	10 000	25	10 000	30	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	60		70		90		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	80	10 000	100	10 000	120	10 000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RASP}	80	100 000	100	100 000	120	100 000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		15		20		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ low (see Note 10)	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	20		25		30		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	20		25		30		ns
$t_{h(CA)}$	Column-address hold time after $\overline{RAS}$ low	t_{CAH}	15		20		20		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	12		15		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	60		70		80		ns

Continued next page.

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. To guarantee $t_{c(P)}$ min, $t_{su(CA)}$ should be greater than or equal to $t_{w(CH)}$.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. (Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$]).
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. (Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$]).
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

PARAMETER		ALT. SYMBOL	TMS44C256-60		TMS44C256-70		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(D)}$	Data hold time after $\overline{CAS}$ low (see Note 10)	t_{DH}	10		15		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	50		55		ns
$t_{h(WLGL)}$	$\overline{G}$ hold time after $\overline{W}$ low	t_{GH}	15		18		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 13)	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 13)	t_{RRH}	0		0		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	15		15		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 12)	t_{WCR}	50		55		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	60		70		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	15		18		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 14)	t_{CWD}	40		46		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)	t_{RCD}	20	45	20	52	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address (see Note 15)	t_{RAD}	15	30	15	35	ns
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	30		35		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	30		35		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)	t_{RWD}	85		98		ns
$t_{d(CAWL)}$	Delay time, column-address to $\overline{W}$ low (see Note 14)	t_{AWD}	55		63		ns
$t_{d(GHD)}$	Delay time, $\overline{G}$ high before data at DQ	t_{GDD}	15		18		ns
$t_{d(GLRH)}$	Delay time, $\overline{G}$ low to $\overline{RAS}$ high	t_{GSR}	10		10		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	15		15		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8	ms
t_t	Transition time	t_T	3	50	3	50	ns

Continued next page.

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
14. Read-modify-write operation only.
15. Maximum value specified only to guarantee access time.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

PARAMETER		ALT. SYMBOL	TMS44C256-80		TMS44C256-10		TMS44C256-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(D)}$	Data hold time after $\overline{CAS}$ low (see Note 10)	t_{DH}	15		20		25		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	60		70		85		ns
$t_{h(WLGL)}$	$\overline{G}$ hold time after $\overline{W}$ low	t_{GH}	20		25		30		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 13)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 13)	t_{RRH}	0		0		0		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	15		20		25		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 12)	t_{WCR}	60		70		85		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	80		100		120		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	20		25		30		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 14)	t_{CWD}	50		60		70		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)	t_{RCD}	22	60	25	75	25	90	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address (see Note 15)	t_{RAD}	17	40	20	55	20	65	ns
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	40		45		55		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	40		45		55		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)	t_{RWD}	110		135		160		ns
$t_{d(CAWL)}$	Delay time, column-address to $\overline{W}$ low (see Note 14)	t_{AWD}	70		80		95		ns
$t_{d(GHD)}$	Delay time, $\overline{G}$ high before data at DQ	t_{GDD}	20		25		30		ns
$t_{d(GLRH)}$	Delay time, $\overline{G}$ low to $\overline{RAS}$ high	t_{GSR}	10		10		10		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	20		25		25		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		10		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
14. Read-modify-write operation only.
15. Maximum value specified only to guarantee access time.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

PARAMETER MEASUREMENT INFORMATION

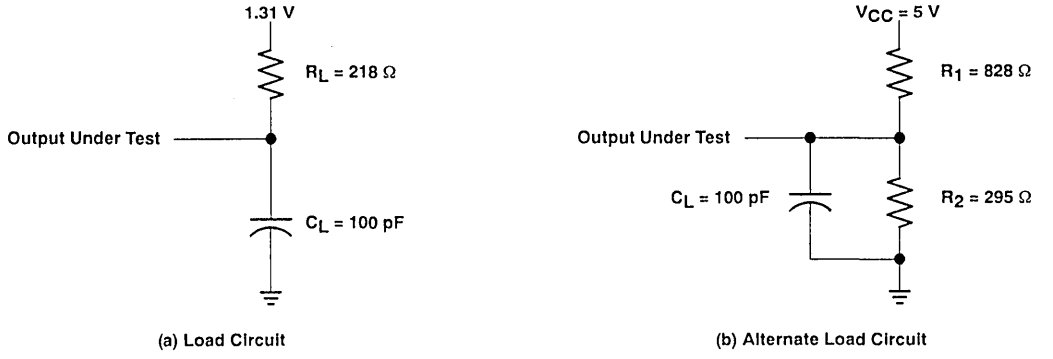
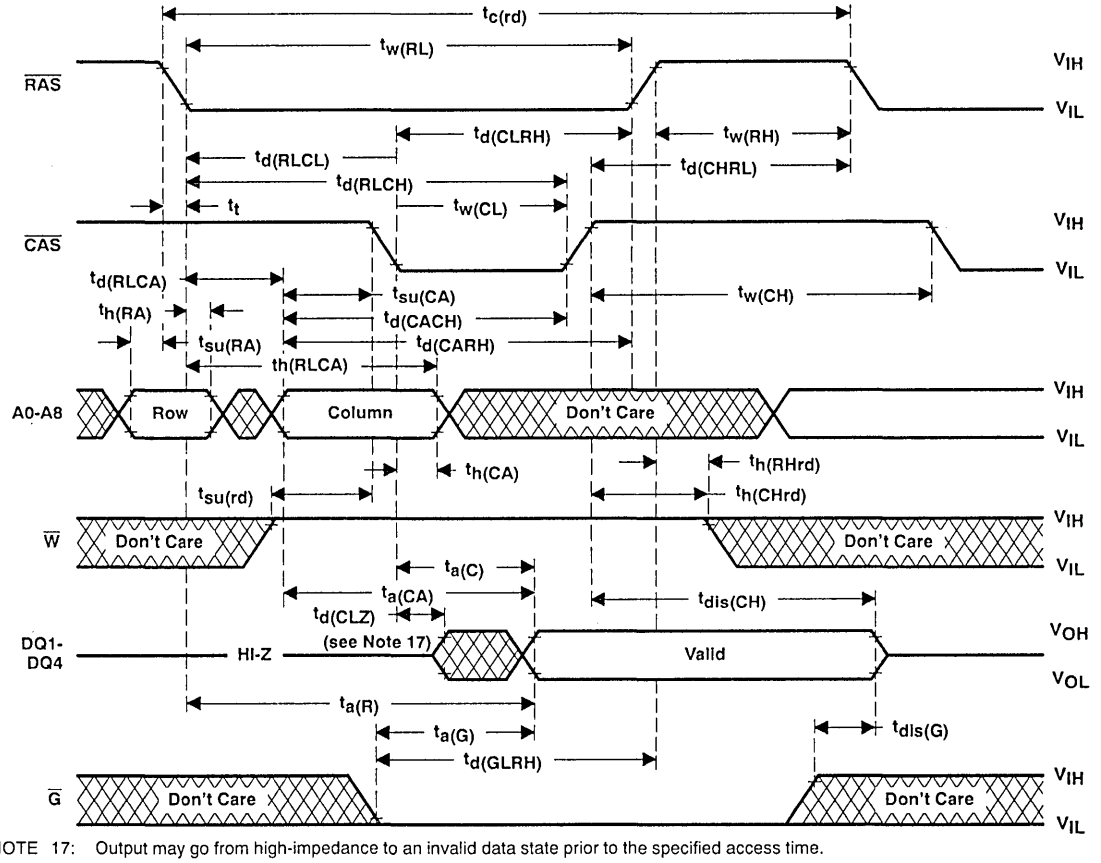


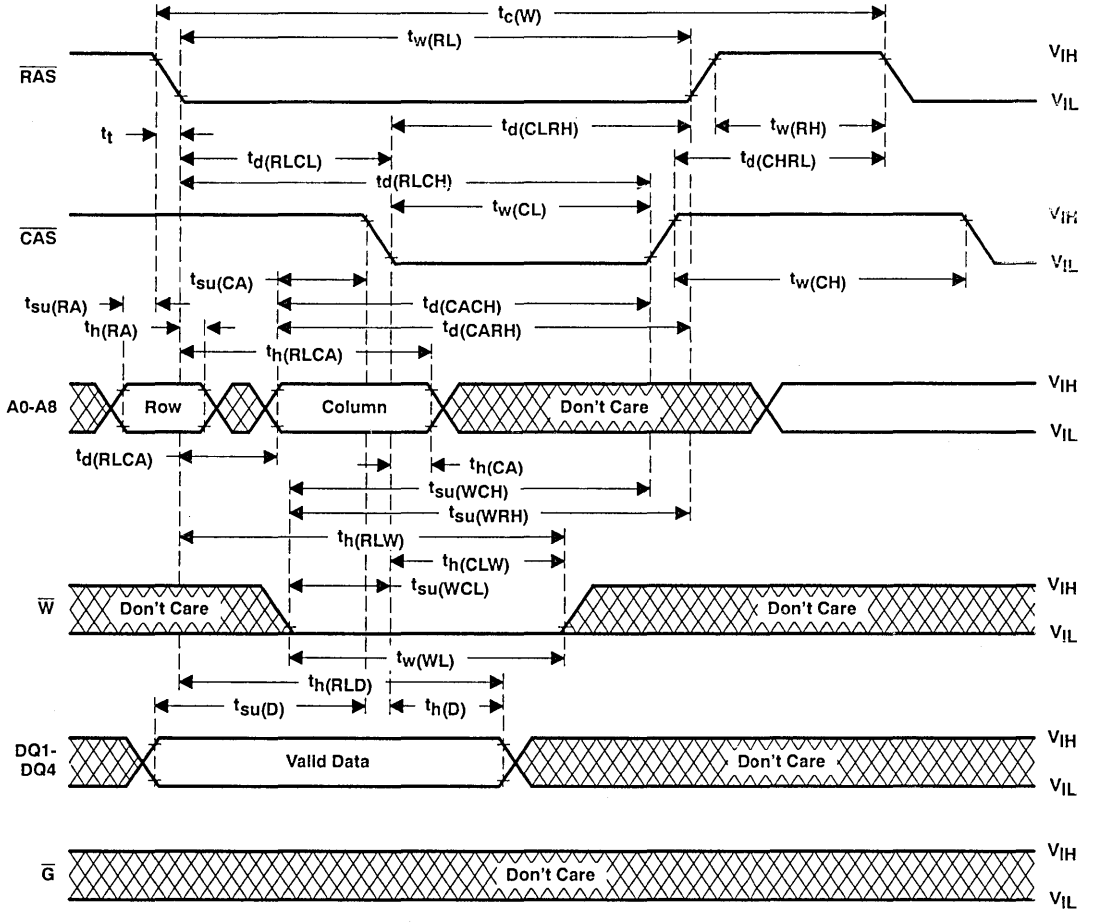
Figure 1. Load Circuits for Timing Parameters

read cycle timing

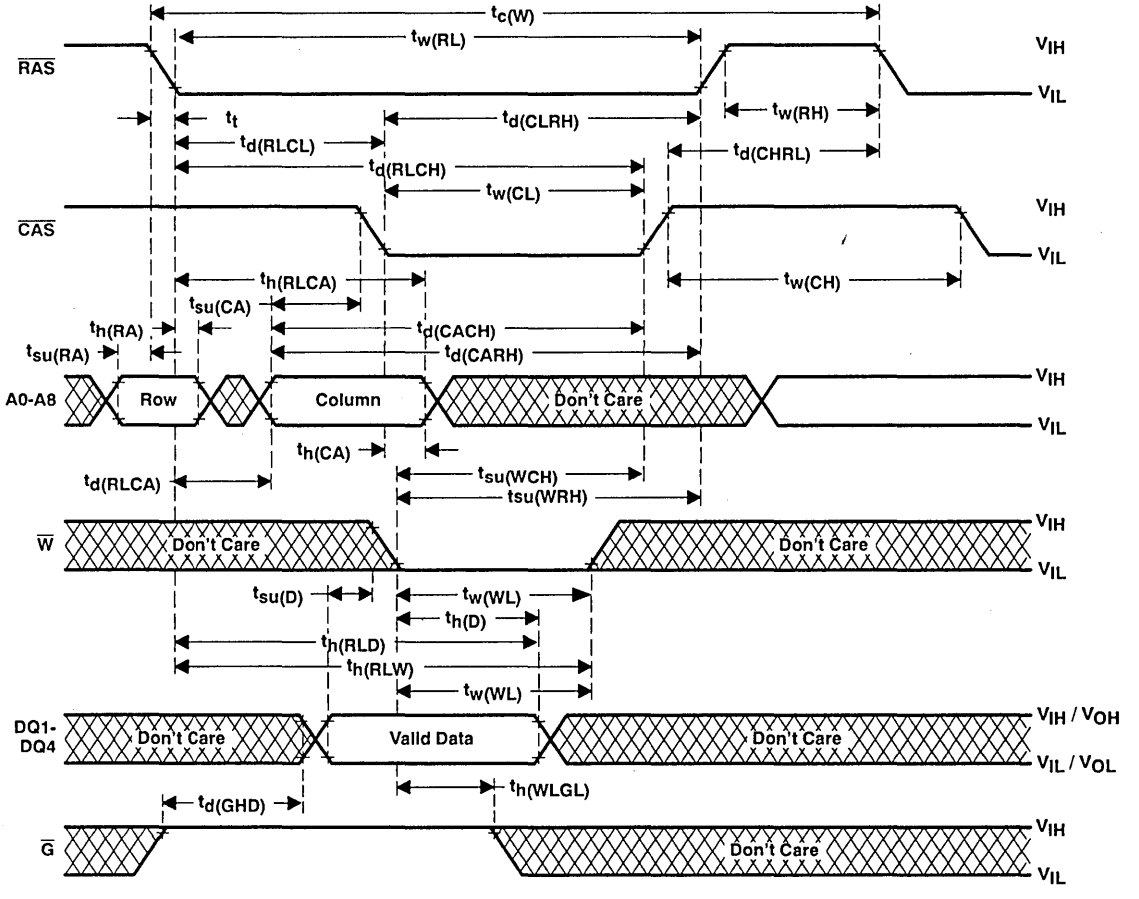


NOTE 17: Output may go from high-impedance to an invalid data state prior to the specified access time.

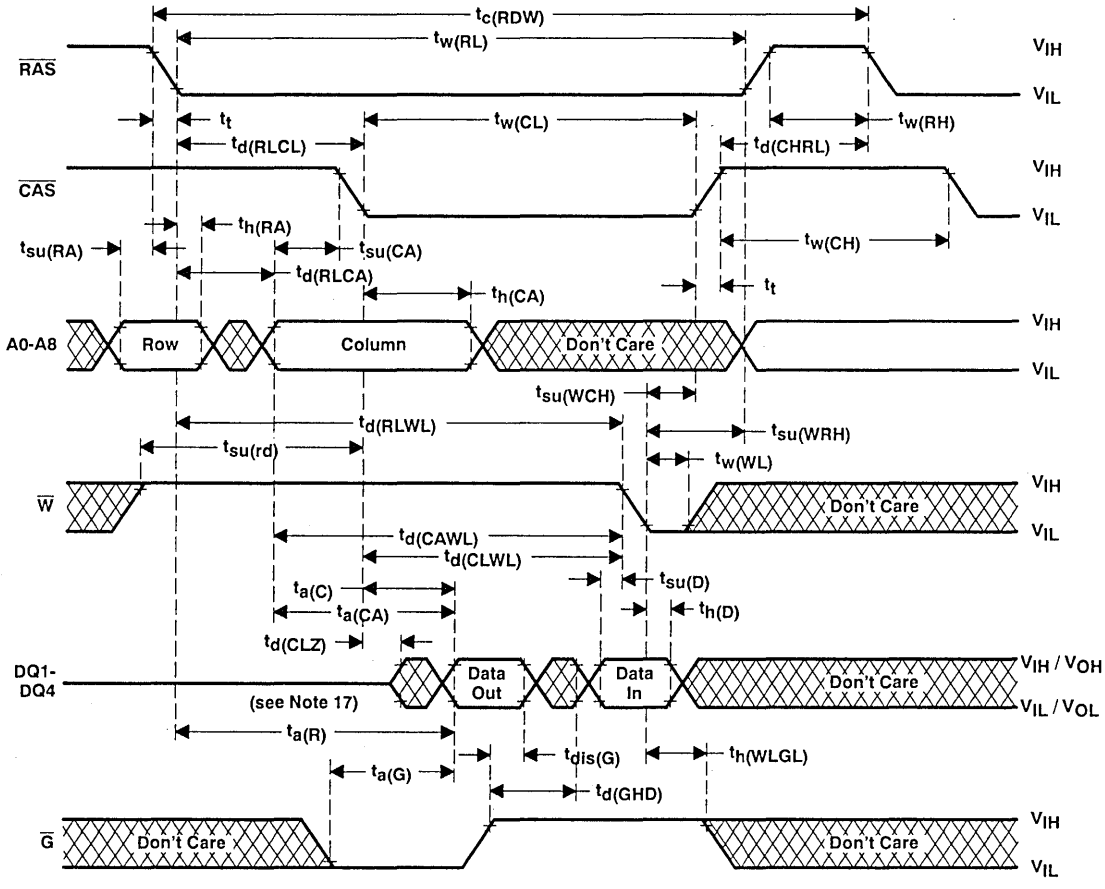
early write cycle timing



late write cycle timing

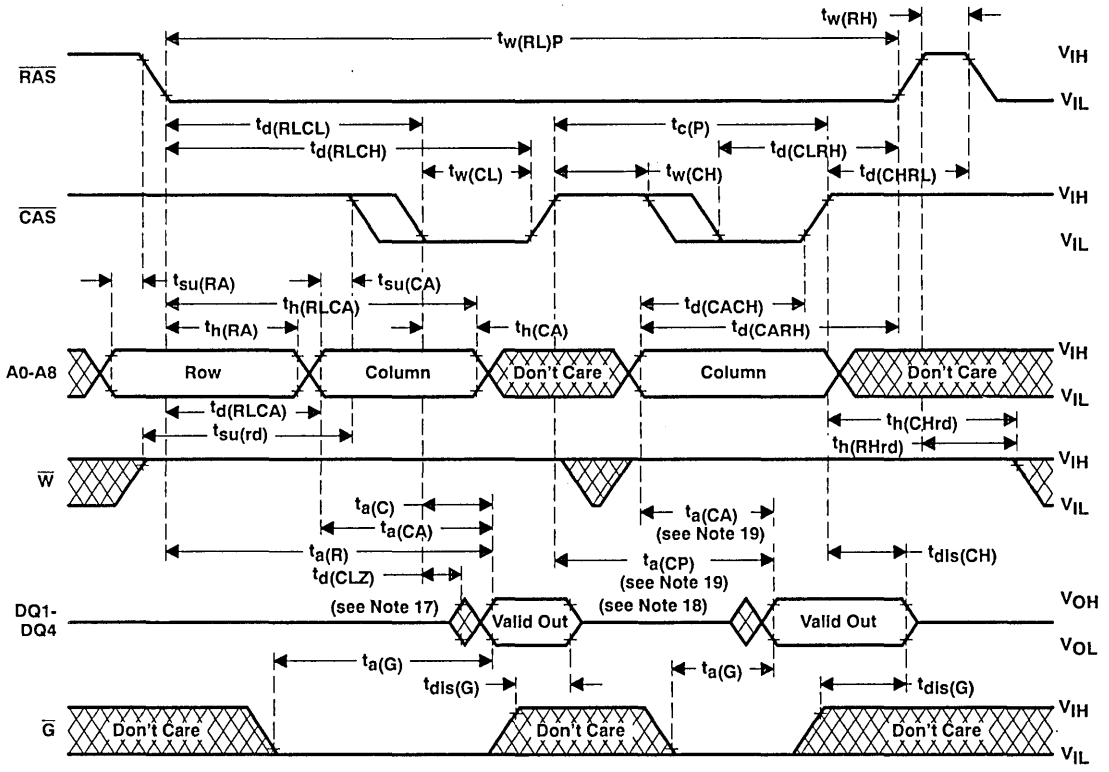


read-write/read-modify-write cycle timing



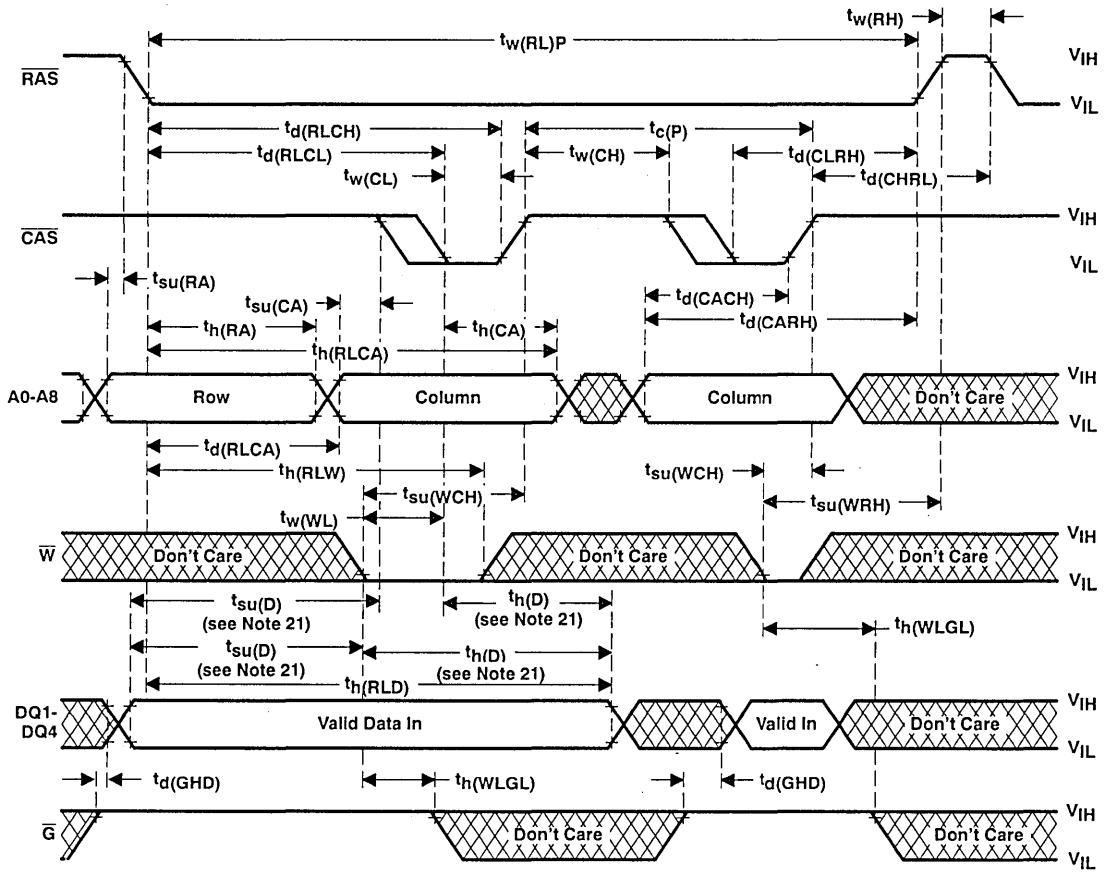
NOTE 17: Output may go from high-impedance to an invalid data state prior to the specified access time.

enhanced page-mode read cycle timing



NOTES: 17. Output may go from high-impedance to an invalid data state prior to the specified access time.
18. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
19. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

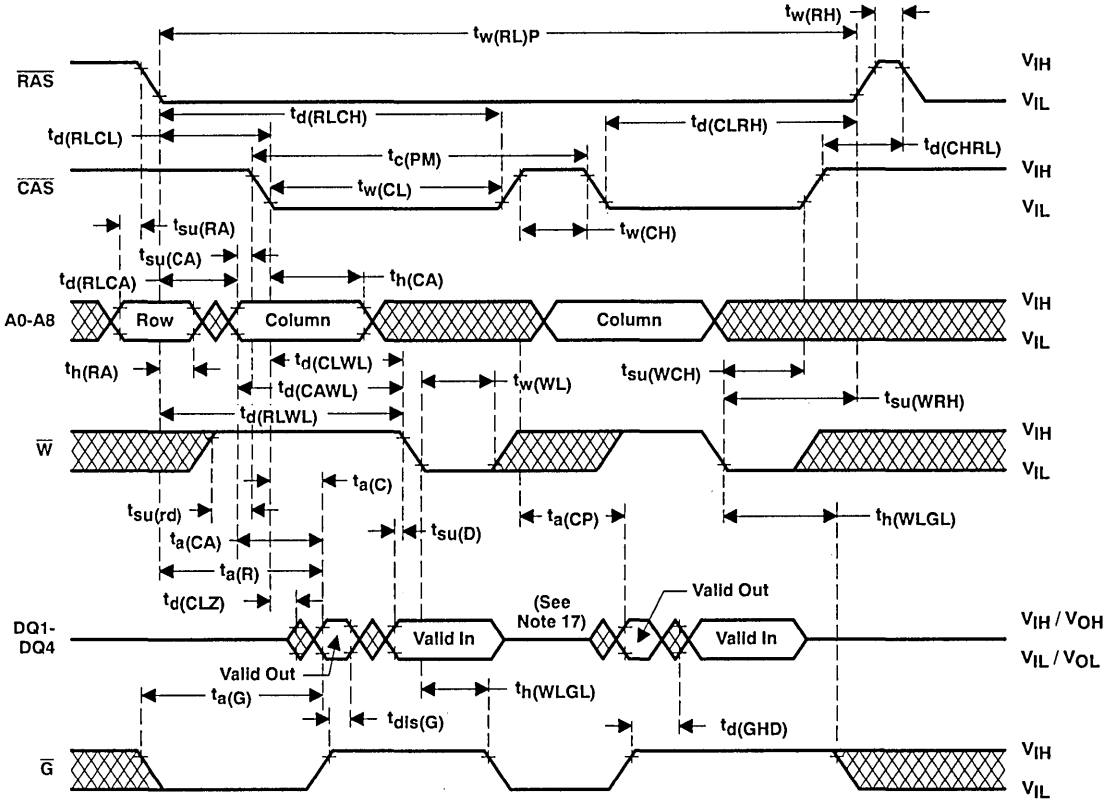
enhanced page-mode write cycle timing



NOTES: 20. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

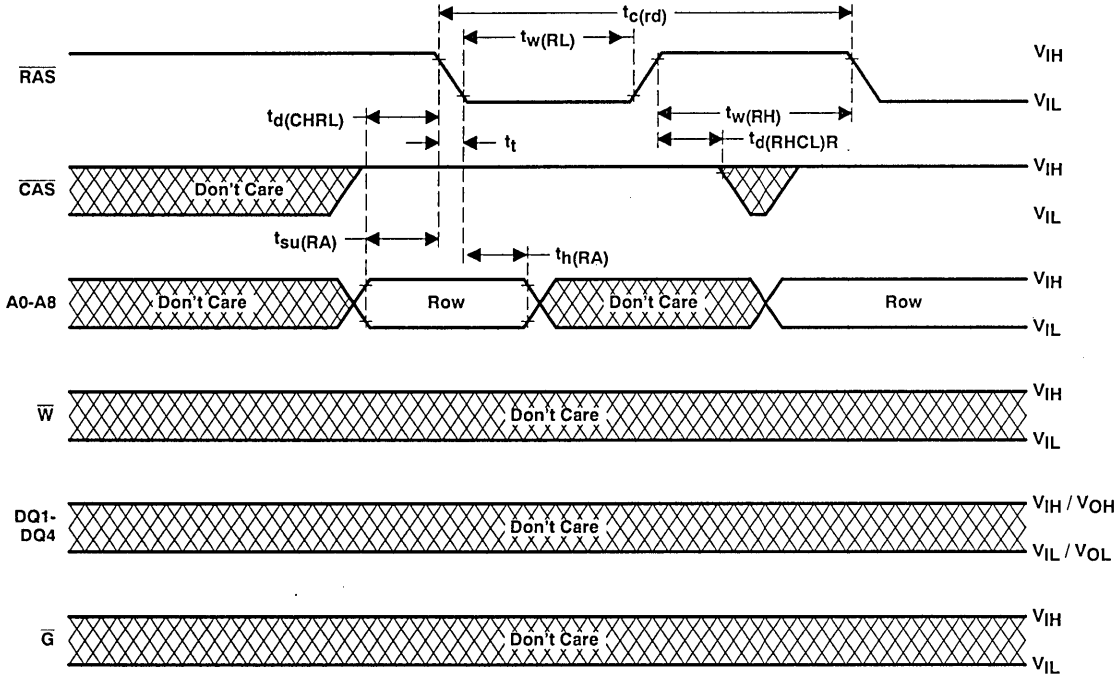
21. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

enhanced page-mode read-modify-write cycle timing

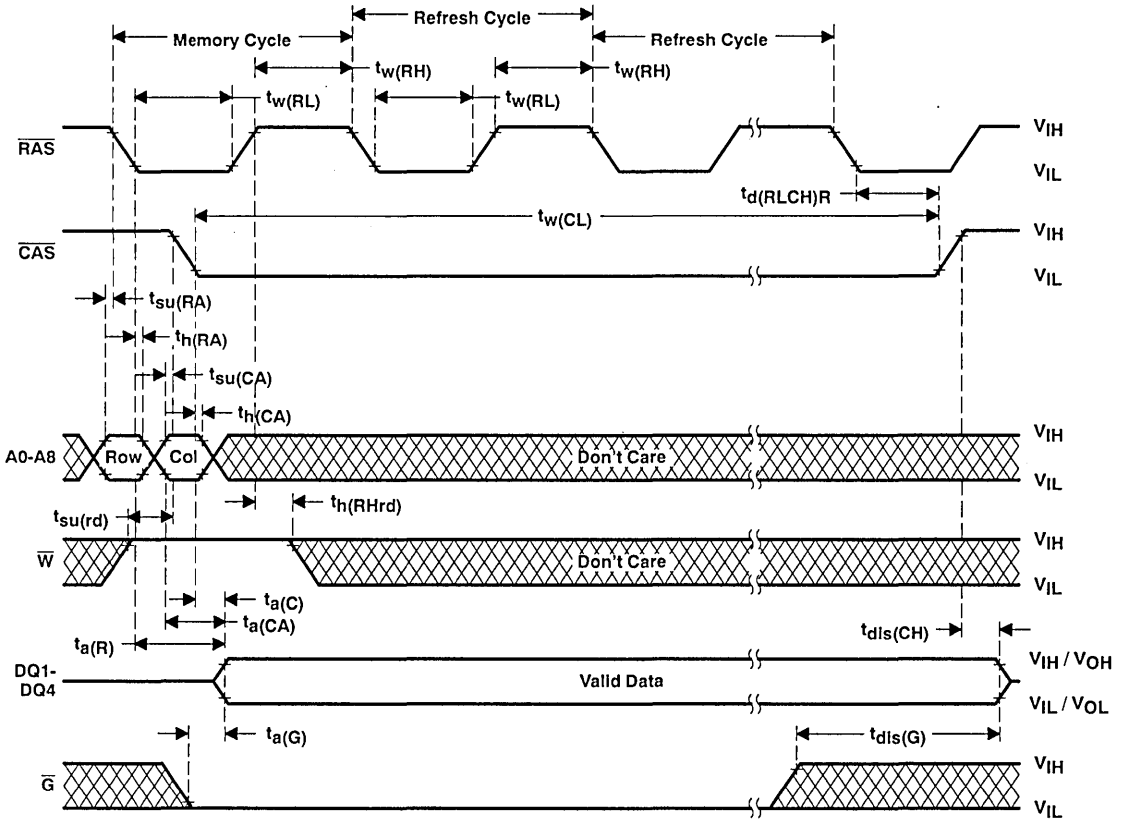


NOTES: 17. Output may go from high-impedance to an invalid data state prior to the specified access time.
22. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

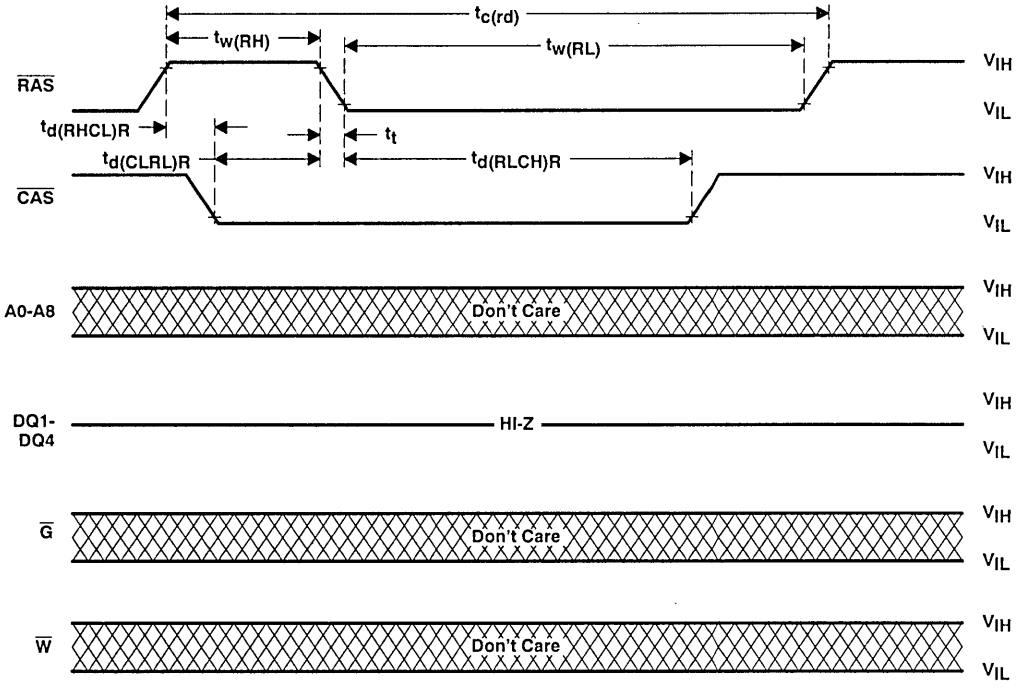
$\overline{\text{RAS}}$-only refresh timing



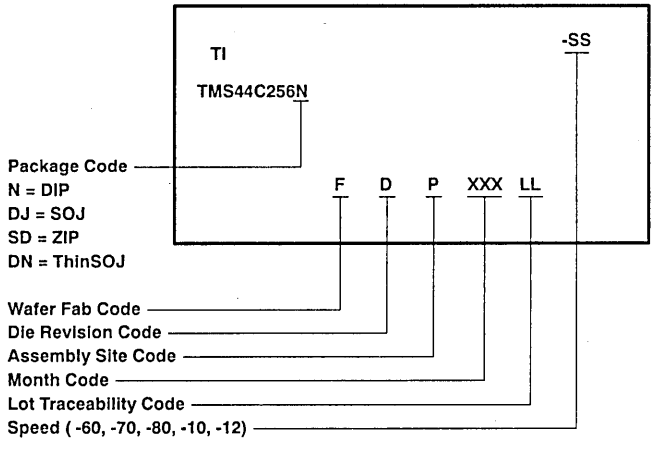
hidden refresh cycle (enhanced page mode)



automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



device symbolization



SMGS024F — MAY 1986 — REVISED NOVEMBER 1990

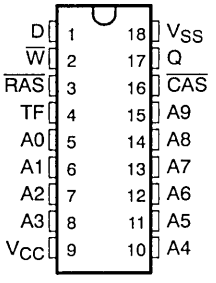
This Data Sheet Is Applicable to All TMS4C1024/5/7s Symbolized with Revision "D" and Subsequent Revisions as Described on Page 5-62.

- **1 048 576 × 1 Organization**
- **Single 5-V Supply (10% Tolerance)**
- **Performance Ranges:**

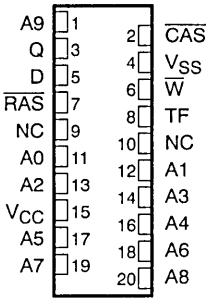
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS4C1024-60	60 ns	15 ns	30 ns	110 ns
TMS4C1024-70	70 ns	18 ns	35 ns	130 ns
TMS4C102_-80	80 ns	20 ns	40 ns	150 ns
TMS4C102_-10	100 ns	25 ns	45 ns	180 ns
TMS4C102_-12	120 ns	30 ns	55 ns	220 ns

- **TMS4C1024 – Enhanced Page Mode Operation for Faster Memory Access**
  - **Higher Data Bandwidth than Conventional Page-Mode Parts**
  - **Random Single-Bit Access Within a Row With a Column Address**
- **TMS4C1025 – 4-Bit Nibble Mode Operation**
  - **Four Sequential Single-Bit Access Within a Row By Toggling $\overline{CAS}$**
- **TMS4C1027– Static Column Decode Mode Operation**
  - **Random Single-Bit Access Within a Row With Only a Column Address Change**
- **One of TI's CMOS Megabit DRAM Family, Including TMS44C256 – 256K × 4 Enhanced Page Mode**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 512-Cycle Refresh in 8 ms (Max)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks Are TTL Compatible**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**
- **High-Reliability Plastic 18-Pin 300-Mil-Wide DIP, 20/26 J-Lead Surface Mount (SOJ), 20/26 Thin J-Lead Surface Mount (ThinSOJ) or 20-Pin Zig-Zag In-line (ZIP) Packages**

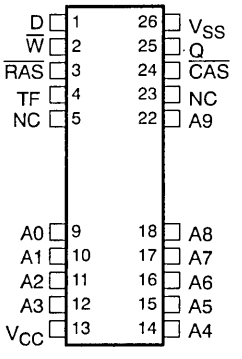
N Package
(Top View)



SD Package
(Top View)



DJ and DN Packages†
(Top View)



†The packages shown here are for pinout reference only. The DJ package is actually 75% of the length of the N package.

PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

- **Operations of TI's Megabit CMOS DRAMs Can Be Controlled by TI's SN74ALS6301 and SN74ALS6302 Dynamic RAM Controllers**

EPIC is a trademark of Texas Instruments Incorporated.

description

The TMS4C1024, TMS4C1025, and TMS4C1027 are high-speed, 1 048 576-bit dynamic random access memories, organized as 1 048 576 words of one bit each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, 100 ns, and 120 ns. Maximum power dissipation is as low as 305 mW operating and 11 mW standby on 120 ns devices.

The EPIC technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{CC} peaks are 140 mA typical, and a – 1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4C102_ are offered in an 18-pin plastic dual-in-line (N suffix) package, a 20/26 J-lead plastic surface mount SOJ (DJ suffix) package, a 20/26 J-lead thin plastic surface mount SOJ (DN suffix), and a 20-pin zig-zag in-line (SD suffix) package. The TMS4C1024-60 and TMS4C1024-70 are available in the 20/26 J-lead plastic surface mount SOJ (DJ suffix) only. These packages are characterized for operation from 0°C to 70°C.

operation

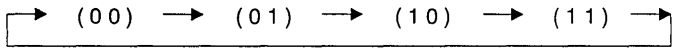
enhanced page mode (TMS4C1024)

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS4C1024 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as "enhanced page mode". Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

nibble mode (TMS4C1025)

Nibble-mode operation allows high-speed read, write, or read-write-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The next sequential bits can be read or written by cycling $\overline{CAS}$ while $\overline{RAS}$ remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Row A9 and column A9 provide the two binary bits for initial selection, with row A9 being the least-significant address and column A9 being the most significant. Thereafter, the falling edge of $\overline{CAS}$ will access the next bit of the circular 4-bit nibble in the following sequence.



Data written in a sequence of more than 4 consecutive cycles shall be capable of being read back without exiting from the nibble mode. In a sequence of consecutive nibble-mode cycles the control of the high-impedance state for the data out (Q) pin is determined by each individual cycle. This facilitates fully mixed nibble-mode cycles (e.g., read/write/read-modify-write/read etc.).

static column decode mode (TMS4C1027)

The static column decode mode of operation allows high-speed read, write, or read-modify-write by reducing the number of required signal setup, hold, and transition timings. This is achieved by first addressing the row and column in the normal manner, but after the first access, maintaining $\overline{CAS}$ low. Subsequently changing the column address produces valid data at $t_{a(CA)}$. The first bit is accessed in the normal manner with read coming out at $t_{a(R)}$ time. Similarly, write or read-modify-write cycle times can be achieved with appropriate toggling of $\overline{W}$. The addresses are latched during the write operation, and remain latched unitl $\overline{CAS}$ or $\overline{W}$ no longer remains low.

address (A0 through A9) (TMS4C1024, TMS4C1025)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits onto the column-address buffer.

address (A0 through A9) (TMS4C1027)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Ten row-address bits are set up on pins A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9. Row addresses must be stable on or before the falling edges of $\overline{RAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. In a write cycle, the later of $\overline{CAS}$ or $\overline{W}$ latches the column address bits.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every eight milliseconds to retain data. This can be achieved by strobing each of the 512 rows (A0-A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter $t_{d(CLRL)R}$] and holding it low after $\overline{RAS}$ falls [see parameter $t_{d(RLCH)R}$]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh cycles.

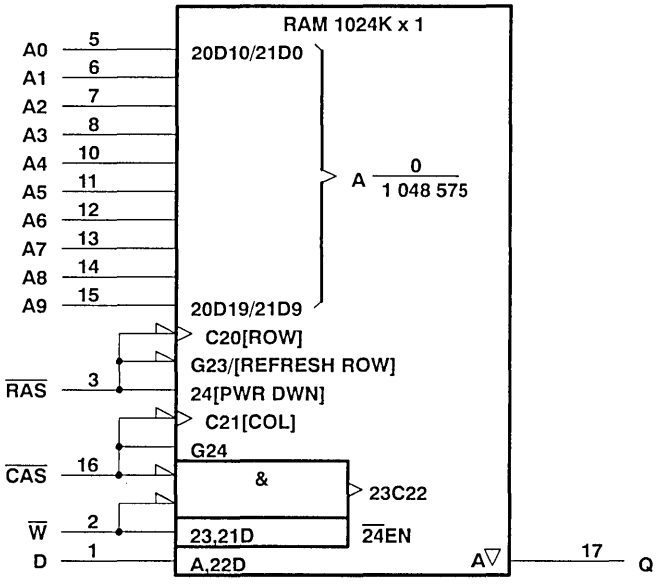
power-up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved.

test function pin

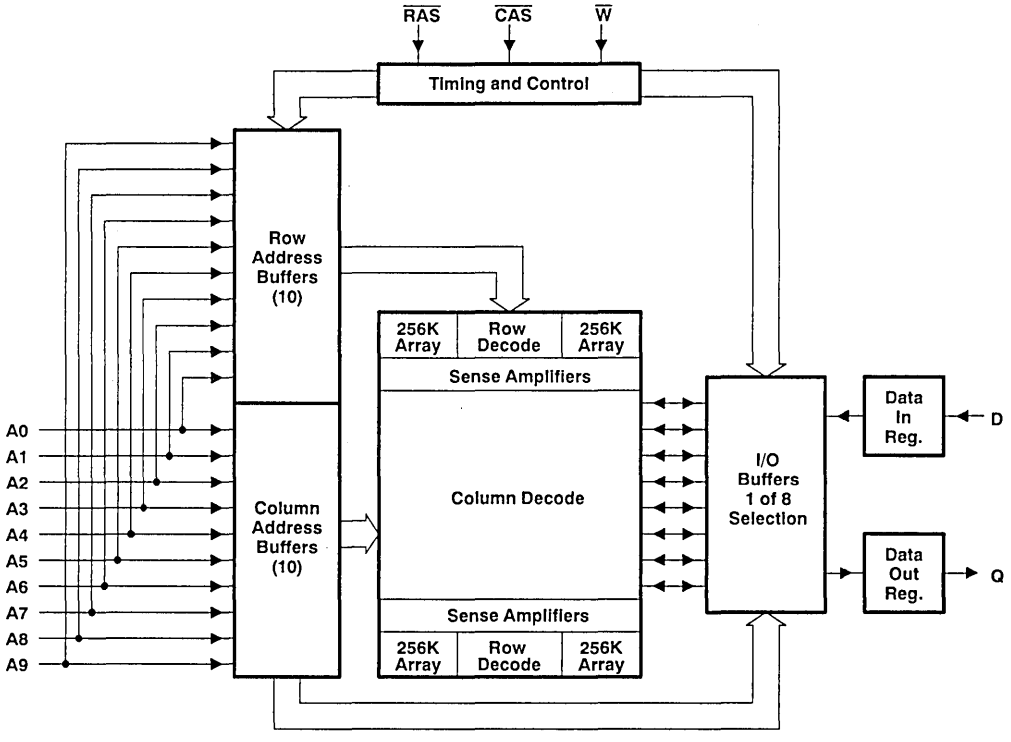
During normal device operation the TF pin must either be disconnected or biased at a voltage less than or equal to V_{CC}.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers are for the 18-pin dual-in-line N package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4C1024-60		TMS4C1024-70		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 to V_{CC}		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10	µA
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.5 V		95		80	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		2		2	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only, or CBR)	Minimum cycle, V_{CC} = 5.5 V $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low, after $\overline{CAS}$ low (CBR)		90		80	mA
I_{CC4}	Average page current (TMS4C1024)	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60	mA

PARAMETER		TEST CONDITIONS	TMS4C1024-80 TMS4C1025-80 TMS4C1027-80		TMS4C1024-10 TMS4C1025-10 TMS4C1027-10		TMS4C1024-12 TMS4C1025-12 TMS4C1027-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.5 V		75		65		55	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		2		2		2	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only, or $\overline{CBR}$)	Minimum cycle, V_{CC} = 5.5 V $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low, after $\overline{CAS}$ low (CBR)		70		60		50	mA
I_{CC4}	Average page current (TMS4C1024)	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		45		35	mA
I_{CC5}	Average nibble current (TMS4C1025)	$t_{c(N)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling for 4 cycles		50		45		40	mA
I_{CC6}	Average static column decode current (TMS4C1027)	$t_{c(rdW)SC}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		45		35	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(D)}$	Input capacitance, data input			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			5	pF
$C_{i(W)}$	Input capacitance, write-enable input			5	pF
C_O	Output capacitance			7	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER		ALT. SYMBOL	TMS4C1024-60		TMS4C1024-70		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low†	t_{CAC}		15		18	ns
$t_{a(CA)}$	Access time from column-address†	t_{CAA}		30		35	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low†	t_{RAC}		60		70	ns
$t_{a(CP)}$	Access time from column precharge (TMS4C1024 only)	t_{CAP}		35		40	ns
$t_{d(CLZ)}$	$\overline{CAS}$ low to output in low Z	t_{CLZ}	0		0		ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)†	t_{OFF}	0	15	0	18	ns

PARAMETER		ALT. SYMBOL	TMS4C102_-80		TMS4C102_-10		TMS4C102_-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low†	t_{CAC}		20		25		30	ns
$t_{a(CA)}$	Access time from column-address†	t_{CAA}		40		45		55	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low†	t_{RAC}		80		100		120	ns
$t_{a(CP)}$	Access time from column precharge (TMS4C1024 only)	t_{CAP}		40		50		60	ns
$t_{d(CLZ)}$	$\overline{CAS}$ low to output in low Z	t_{CLZ}	0		0		0		ns
$t_{a(C)N}$	Access time $\overline{CAS}$ low (TMS4C1025 only)	t_{NCAC}		20		25		25	ns
$t_{a(WHQ)}$	Access time from $\overline{W}$ high (TMS4C1027 only)	t_{WRA}		20		30		35	ns
$t_{a(WLQ)}$	Access time from $\overline{W}$ low (TMS4C1027 only)	t_{ALW}		75		95		115	ns
$t_{h(CAQ)}$	Static column decode mode output hold time after address change (TMS4C1027 only)	t_{AOH}	5		5		5		ns
$t_{h(WQ)}$	Static column decode mode output hold time after $\overline{W}$ low (TMS4C1027 only)	t_{WOH}	0		0		0		ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)†	t_{OFF}	0	20	0	25	0	30	ns

†Parameters apply uniformly to TMS4C1024, TMS4C1025, TMS4C1027.

NOTE 4: $t_{dis(CH)}$ is specified when the output is no longer driven.

PARAMETER MEASUREMENT INFORMATION

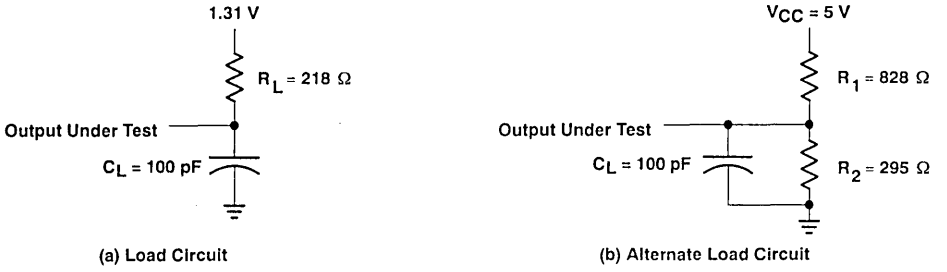


Figure 1. Load Circuits For Timing Parameters

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		ALT.	TMS4C1024-60		TMS4C1024-70		UNIT
		SYMBOL	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	110		130		ns
$t_{c(W)}$	Write cycle time	t_{WC}	110		130		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	130		153		ns
$t_{c(P)}$	Page-mode read or write cycle time (see Note 7)	t_{PC}	40		45		ns
$t_{c(PM)}$	Page-mode read-modify-write cycle time	t_{PCM}	60		68		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	15	10 000	18	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	40		50		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	60	10 000	70	10 000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RASP}	60	100 000	70	100 000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		15		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time (see Note 10)	t_{DS}	0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	15		18		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	15		18		ns
$t_{h(CA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	10		15		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	10		10		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	50		55		ns
$t_{h(D)}$	Data hold time (see Note 10)	t_{DH}	10		15		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	50		55		ns

Continued next page.

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. To guarantee $t_{c(P)}$ min, $t_{su(CA)}$ should be greater than or equal to $t_{w(CH)}$.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed.
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		ALT. SYMBOL	TMS4C1024-80		TMS4C1024-10		TMS4C1024-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	150		180		220		ns
$t_{c(W)}$	Write cycle time	t_{WC}	150		180		220		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	175		210		255		ns
$t_{c(P)}$	Page-mode read or write cycle time (see Note 7)	t_{PC}	50		55		65		ns
$t_{c(PM)}$	Page-mode read-modify-write cycle time	t_{PCM}	75		85		100		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		15		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	20	10 000	25	10 000	30	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	60		70		90		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	80	10 000	100	10 000	120	10 000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RASP}	80	100 000	100	100 000	120	100 000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		15		20		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time (see Note 10)	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	20		25		30		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	20		25		30		ns
$t_{h(CA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	15		20		20		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	12		15		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	60		70		80		ns
$t_{h(D)}$	Data hold time (see Note 10)	t_{DH}	15		20		25		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	60		70		85		ns

Continued next page.

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. To guarantee $t_{c(P)}$ min, $t_{su(CA)}$ should be greater than or equal to $t_{w(CH)}$.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed.
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		ALT.	TMS4C1024-60		TMS4C1024-70		UNIT
		SYMBOL	MIN	MAX	MIN	MAX	
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 15)	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 15)	t_{RRH}	0		0		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	15		15		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 12)	t_{WCR}	50		55		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	60		70		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	15		18		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 13)	t_{CWD}	15		18		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	20	45	20	52	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address (see Note 14)	t_{RAD}	15	30	15	35	ns
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	30		35		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	30		35		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)	t_{RWD}	60		70		ns
$t_{d(CAWL)}$	Delay time, column-address to $\overline{W}$ low (see Note 13)	t_{AWD}	30		35		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	15		15		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8	ms
t_t	Transition time	t_T	3	50	3	50	ns

Continued next page.

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Read-modify-write operation only.
14. Maximum value specified only to guarantee access time.
15. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		ALT. SYMBOL	TMS4C1024-80		TMS4C1024-10		TMS4C1024-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 15)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 15)	t_{RRH}	0		0		0		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	15		20		25		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 12)	t_{WCR}	60		70		85		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	80		100		120		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	20		25		30		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 13)	t_{CWD}	20		25		30		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	22	60	25	75	25	90	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address (see Note 14)	t_{RAD}	17	40	20	55	20	65	ns
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	40		45		55		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	40		45		55		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)	t_{RWD}	80		100		120		ns
$t_{d(CAWL)}$	Delay time, column-address to $\overline{W}$ low (see Note 13)	t_{AWD}	40		45		55		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	20		25		25		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		10		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Read-modify-write operation only.
14. Maximum value specified only to guarantee access time.
15. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		ALT. SYMBOL	TMS4C1025-80		TMS4C1025-10		TMS4C1025-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	150		180		220		ns
$t_{c(W)}$	Write cycle time	t_{WC}	150		180		220		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	175		210		255		ns
$t_{c(N)}$	Nibble-mode read or write cycle time	t_{NC}	40		45		50		ns
$t_{c(rdW)N}$	Nibble-mode read-modify-write cycle time	t_{NRMW}	65		75		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		15		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	20	10 000	25	10 000	25	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	60		70		90		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	80	10 000	100	10 000	120	10 000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		15		20		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time (see Note 10)	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	20		25		25		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	20		25		25		ns
$t_{h(CA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	15		20		20		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	12		15		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	60		70		80		ns
$t_{h(D)}$	Data hold time (see Note 10)	t_{DH}	15		20		25		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	60		70		85		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high	t_{RRH}	0		0		10		ns

Continued next page.

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed.
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		ALT. SYMBOL	TMS4C1025-80		TMS4C1025-10		TMS4C1025-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	15		20		25		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Notes 11 and 12)	t_{WCR}	60		70		85		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	80		100		120		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	20		25		25		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 13)	t_{CWD}	20		25		25		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	22	60	25	75	25	90	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	t_{RAD}	17	40	20	55	20	65	ns
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	40		45		55		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	40		45		55		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)	t_{RWD}	80		100		120		ns
$t_{d(CAWL)}$	Delay time, column-address to $\overline{W}$ low (see Note 13)	t_{AWD}	40		45		55		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	20		25		25		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		10		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. read-modify-write operation only.
14. Maximum value specified only to guarantee access time.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		ALT. SYMBOL	TMS4C1027-80		TMS4C1027-10		TMS4C1027-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	150		180		220		ns
$t_{c(W)}$	Write cycle time	t_{WC}	150		180		220		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	175		210		255		ns
$t_{c(rd)SC}$	Static column decode mode read cycle time	t_{SCR}	45		50		60		ns
$t_{c(W)SC}$	Static column decode mode write cycle time	t_{SCW}	45		50		60		ns
$t_{c(rdW)SC}$	Static column decode mode read-modify-write cycle time	t_{SCRMW}	80		100		120		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		15		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	20	10 000	25	10 000	30	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	60		70		90		ns
$t_{w(RL)}$	Non-static column decode mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	80	10 000	100	10 000	120	10 000	ns
$t_{w(RL)P}$	Static column decode mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RASP}	80	100 000	100	100 000	120	100 000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		15		20		ns
$t_{w(CA)}$	Static column decode mode column-address pulse duration	t_{ADP}	40		45		55		ns
$t_{w(WH)}$	Static column decode mode $\overline{W}$ high pulse duration, inactive	t_{WI}	10		10		15		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$, $\overline{W}$ low (see Note 10)	t_{ASC}	0		0		0		ns
$t_{su(CAR)}$	Row-address setup time before $\overline{RAS}$	t_{CAR}	45		50		60		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	20		25		30		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	20		25		30		ns

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NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed.
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		ALT. SYMBOL	TMS4C1027-80		TMS4C1027-10		TMS4C1027-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(WHCH)}$	Setup time, $\overline{W}$ high to $\overline{CAS}$ high for early write, high impedance	t_{WH}	0		0		0		ns
$t_{h(CA)}$	Column-address hold time after $\overline{CAS}$ or $\overline{W}$ low (see Note 10)	t_{CAH}	15		20		20		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	12		15		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 18)	t_{AR}	80		100		120		ns
$t_{h(D)}$	Data hold time (see Note 10)	t_{DH}	15		20		25		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 17)	t_{DHR}	60		70		85		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 18)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 18)	t_{RRH}	0		0		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	15		20		25		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 17)	t_{WCR}	60		70		85		ns
$t_{h(RHCA)}$	Column-address hold time after $\overline{RAS}$ high	t_{AH}	10		10		15		ns
$t_{h(WLCA2)}$	Static column decode mode second column-address hold time after $\overline{W}$ low (see Note 13)	t_{AHLW}	75		95		115		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	80		100		120		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	20		25		30		ns

Continued next page.

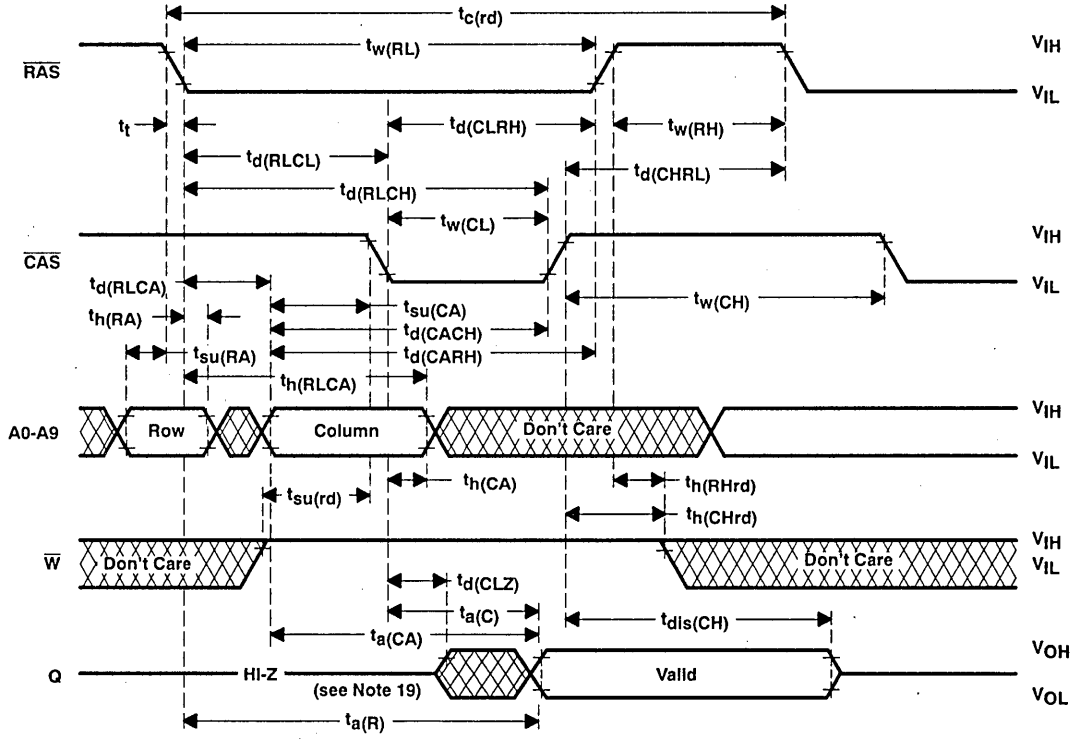
NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
13. Read-modify-write operation only.
17. The minimum value is measured when $t_{d(RLCA)}$ is set to $t_{d(RLCA)}$ min as a reference.
18. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		ALT. SYMBOL	TMS4C1027-80		TMS4C1027-10		TMS4C1027-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 13)	t_{CWD}	20		25		30		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	22	60	25	75	25	90	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	t_{RAD}	17	40	20	55	20	65	ns
$t_{d(WLCA)}$	Delay time, $\overline{W}$ low to column address (see Note 14)	t_{LWAD}	20	35	25	50	30	60	ns
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	40		45		55		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	40		45		55		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)	t_{RWD}	80		100		120		ns
$t_{d(RLWL2)}$	Static column decode mode delay time, $\overline{RAS}$ low to second $\overline{W}$ low	t_{RSW}	80		100		120		ns
$t_{d(CAWL)}$	Delay time, column-address to $\overline{W}$ low (see Note 13)	t_{AWD}	40		45		55		ns
$t_{d(WQ)}$	Delay time, $\overline{W}$ high to output transition from high impedance to active	t_{OW}	0		0		0		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	20		25		25		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		10		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

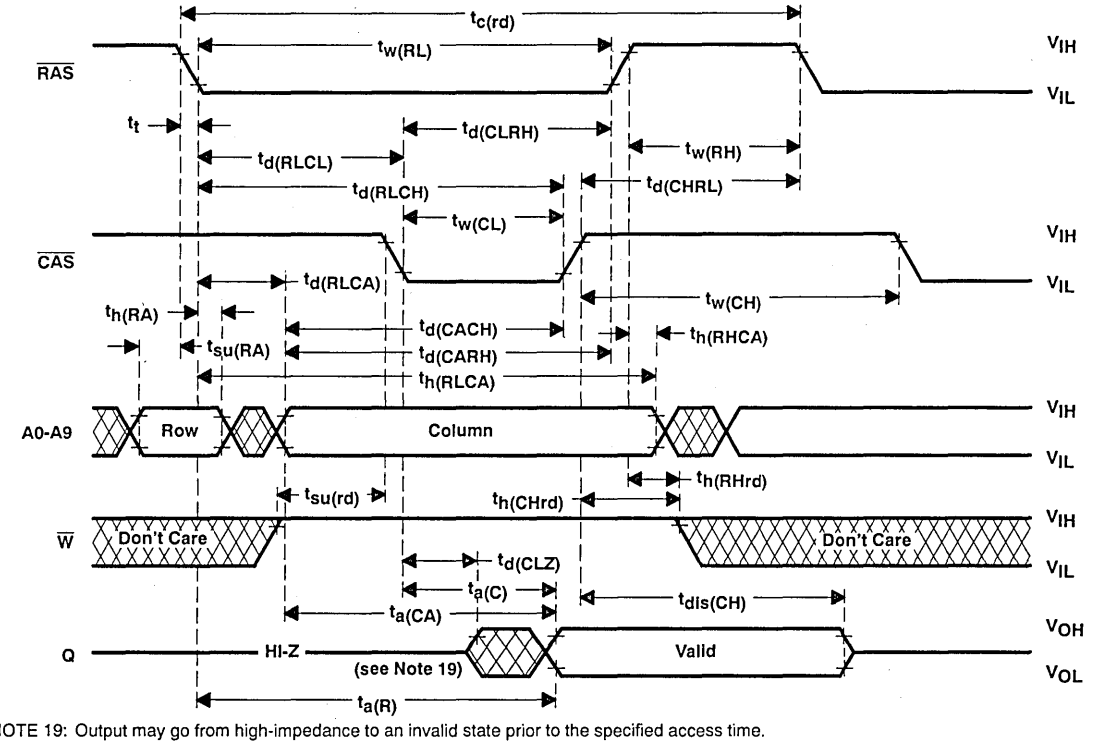
NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
13. Read-modify-write operation only.
14. Maximum value specified only to guarantee access time.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

read cycle timing



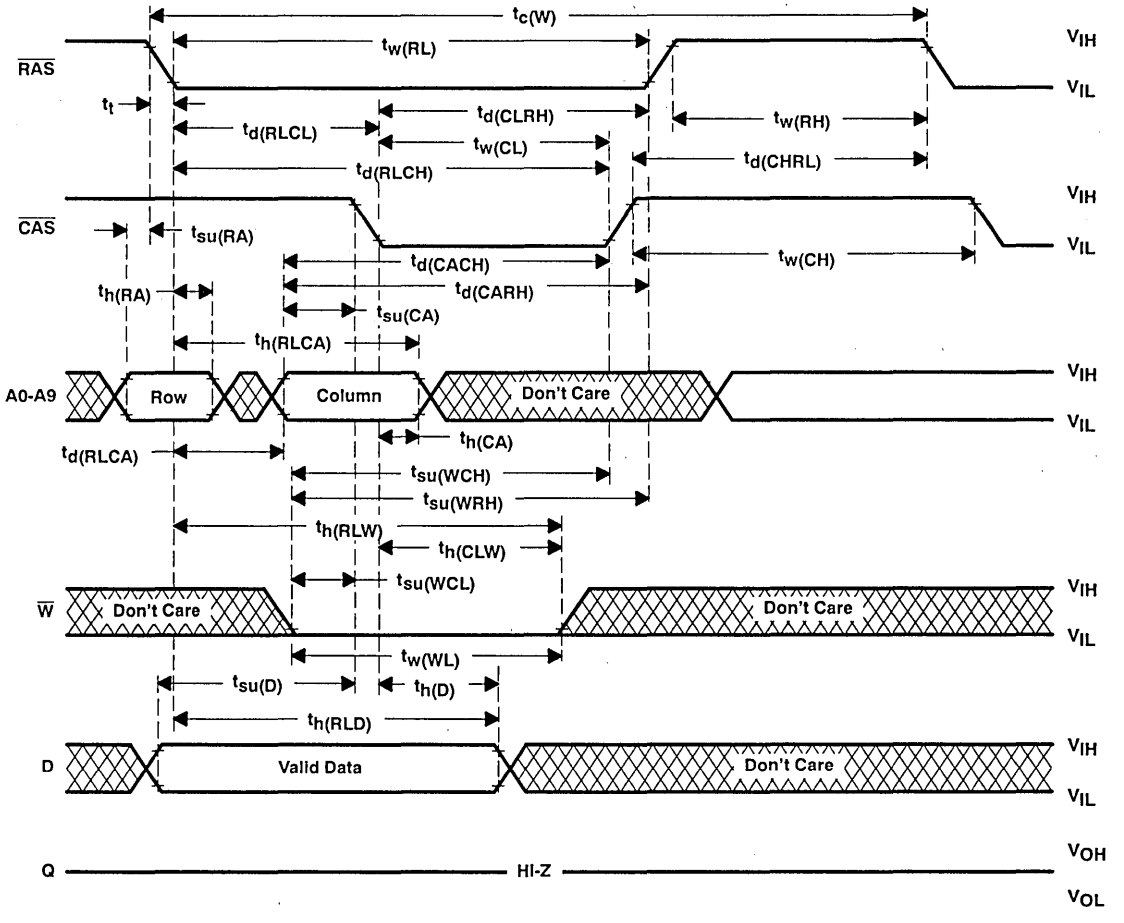
NOTE 19: Output may go from high-impedance to an invalid state prior to the specified access time.

read cycle timing

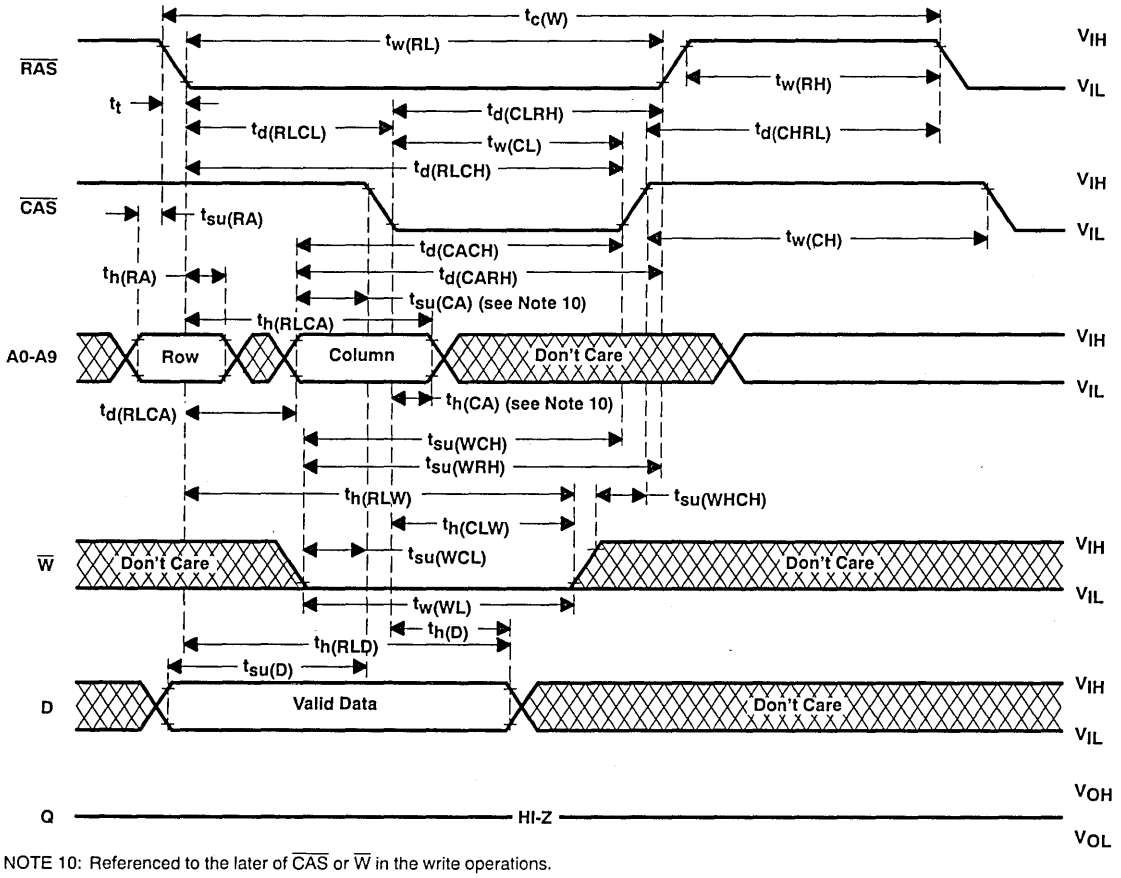


NOTE 19: Output may go from high-impedance to an invalid state prior to the specified access time.

early write cycle timing

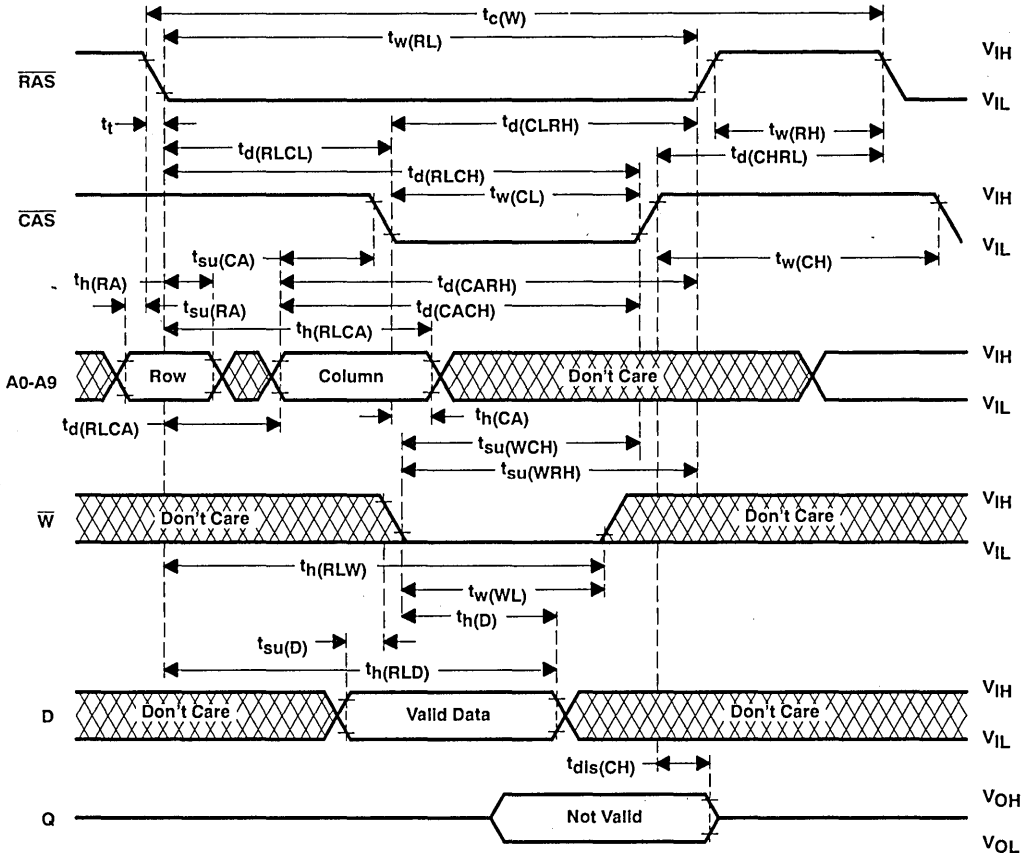


early write cycle timing

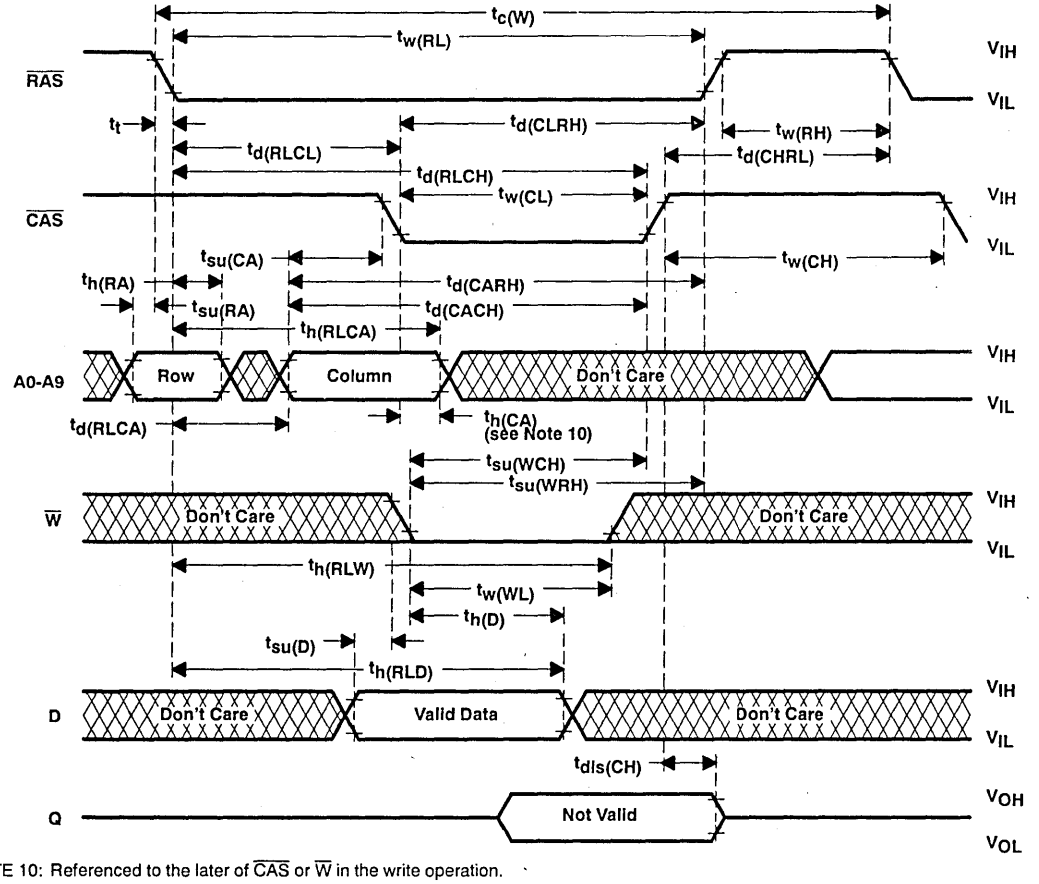


NOTE 10: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in the write operations.

write cycle timing

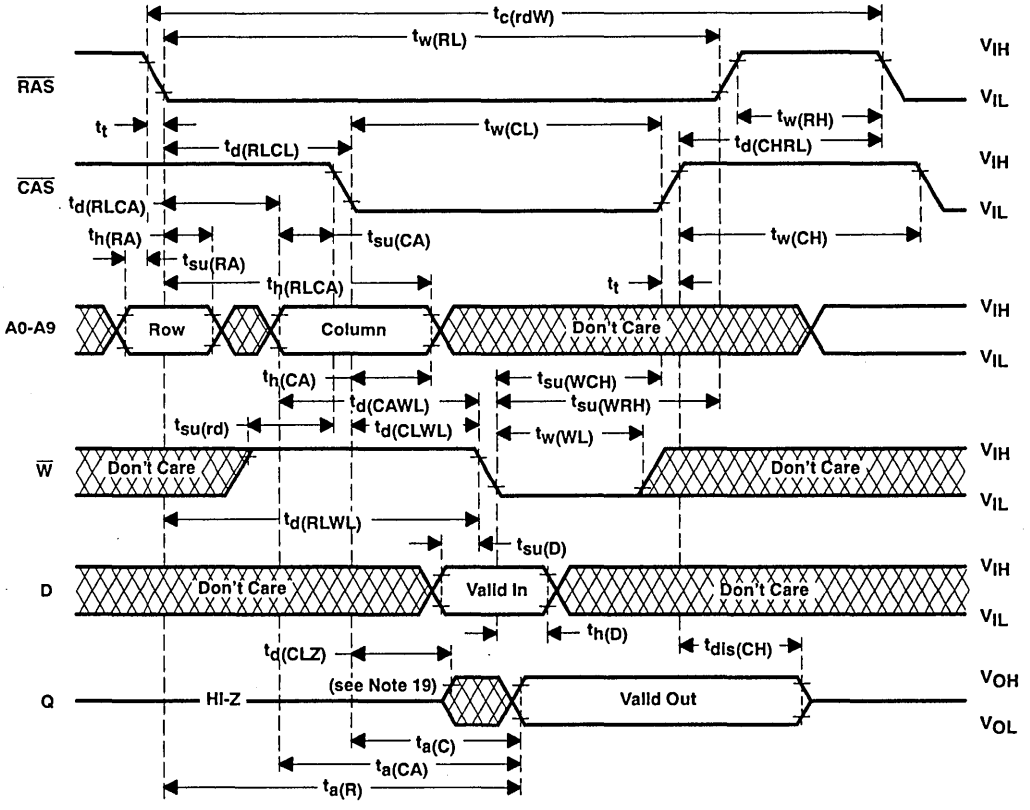


write cycle timing



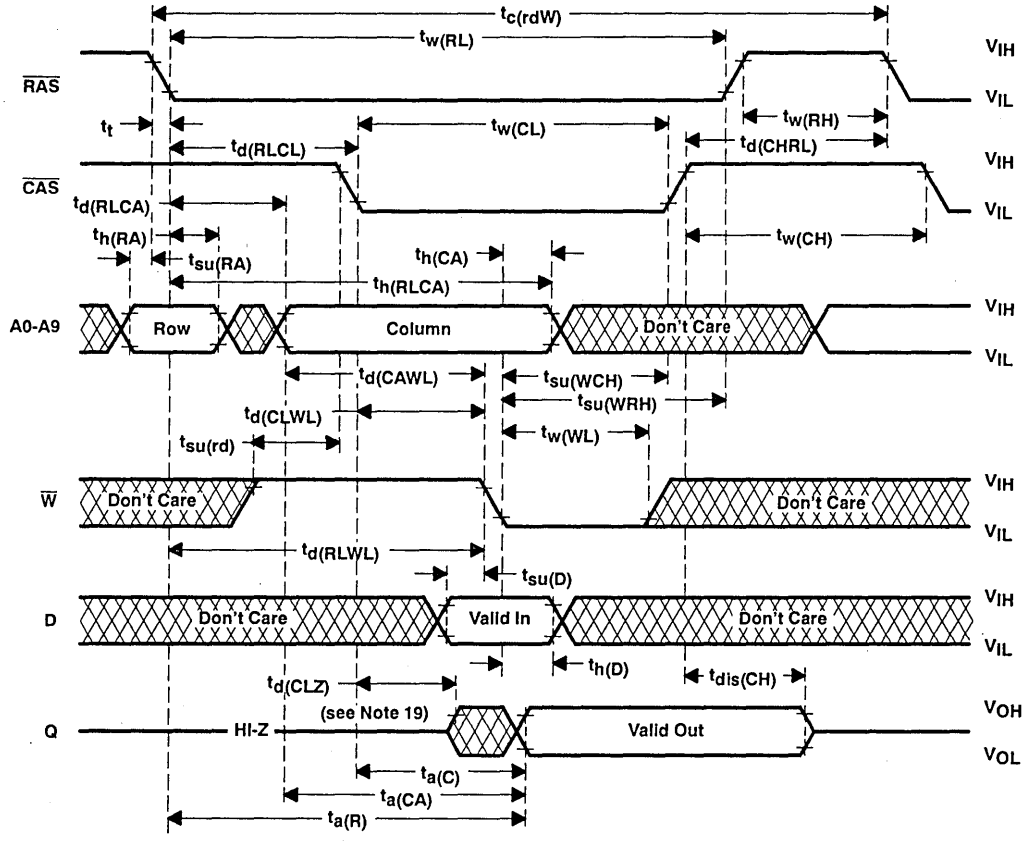
NOTE 10: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in the write operation.

read-write/read-modify-write cycle timing



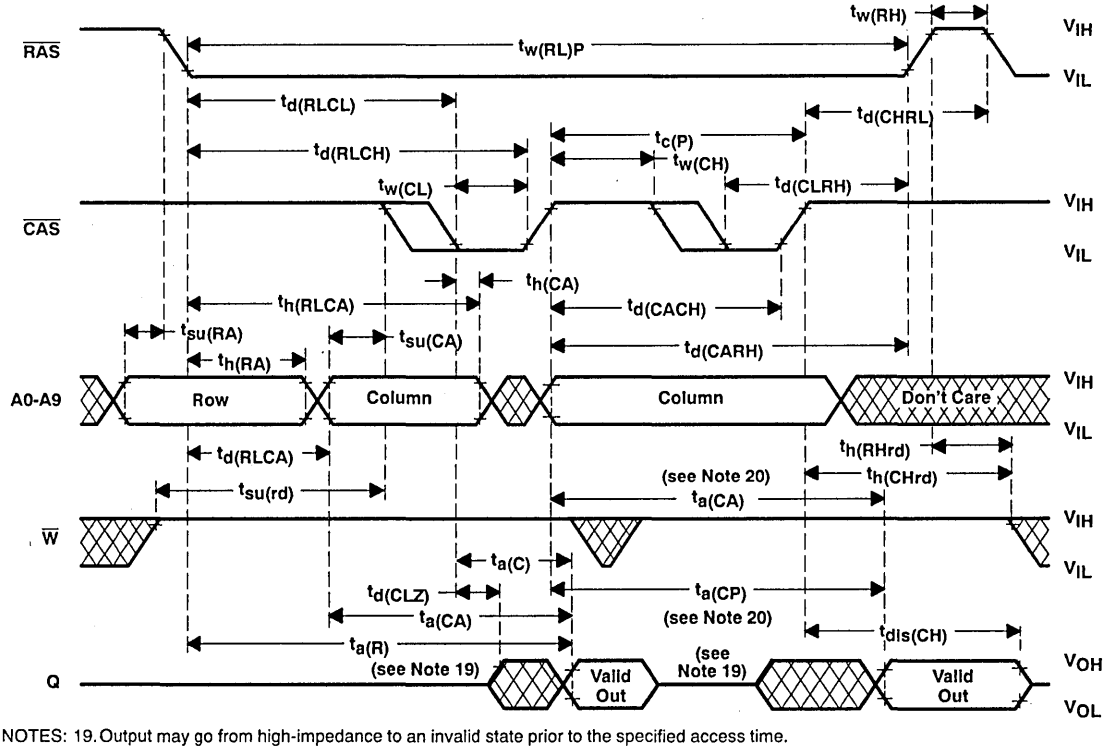
NOTE 19: Output may go from high-impedance to an invalid state prior to the specified access time.

read-write/read-modify-write cycle timing



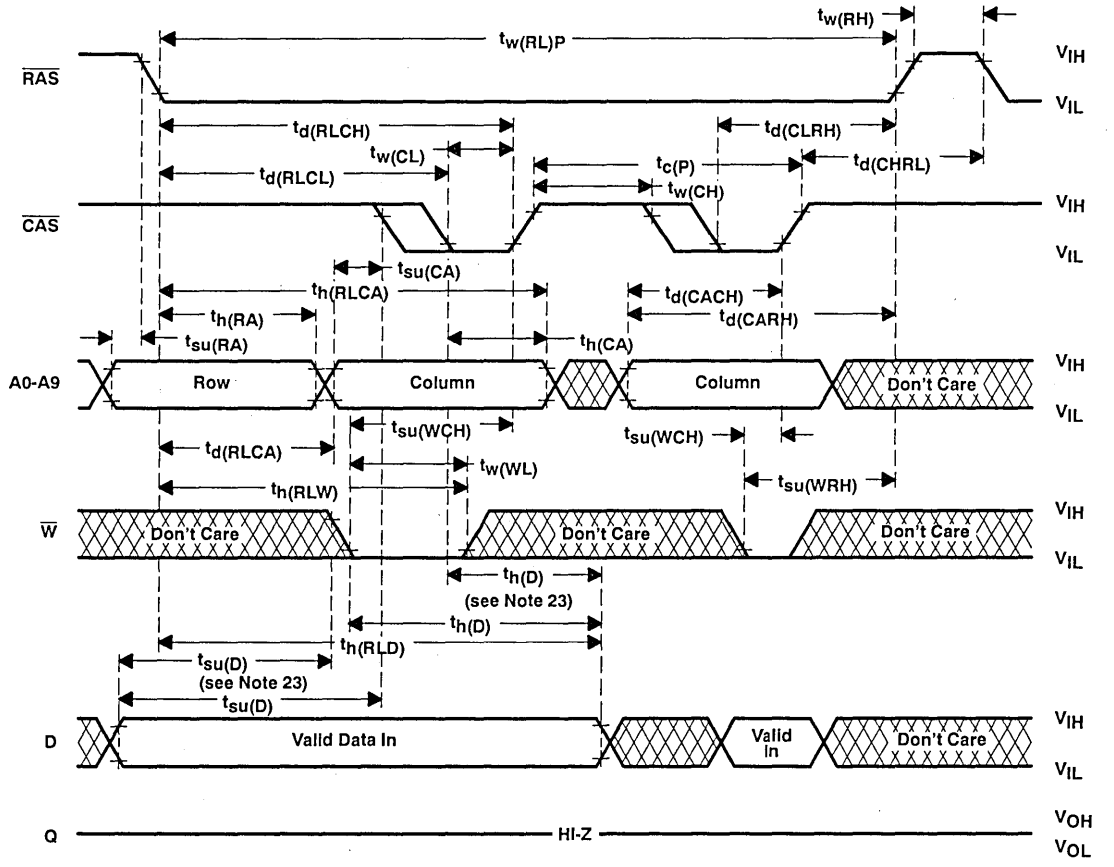
NOTE 19: Output may go from high-impedance to an invalid state prior to the specified access time.

enhanced page-mode read cycle timing



NOTES: 19. Output may go from high-impedance to an invalid state prior to the specified access time.
20. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
21. A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.

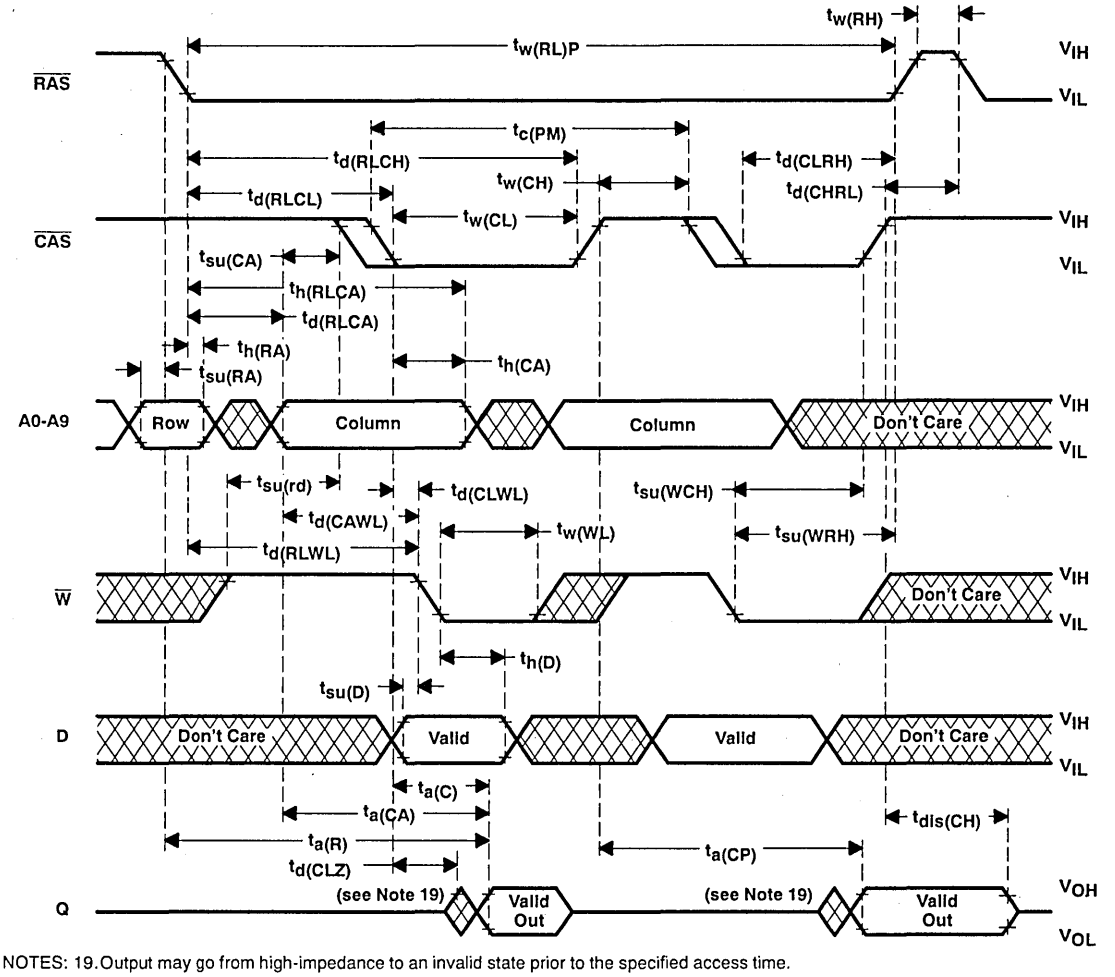
enhanced page-mode write cycle timing



NOTES: 22. A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

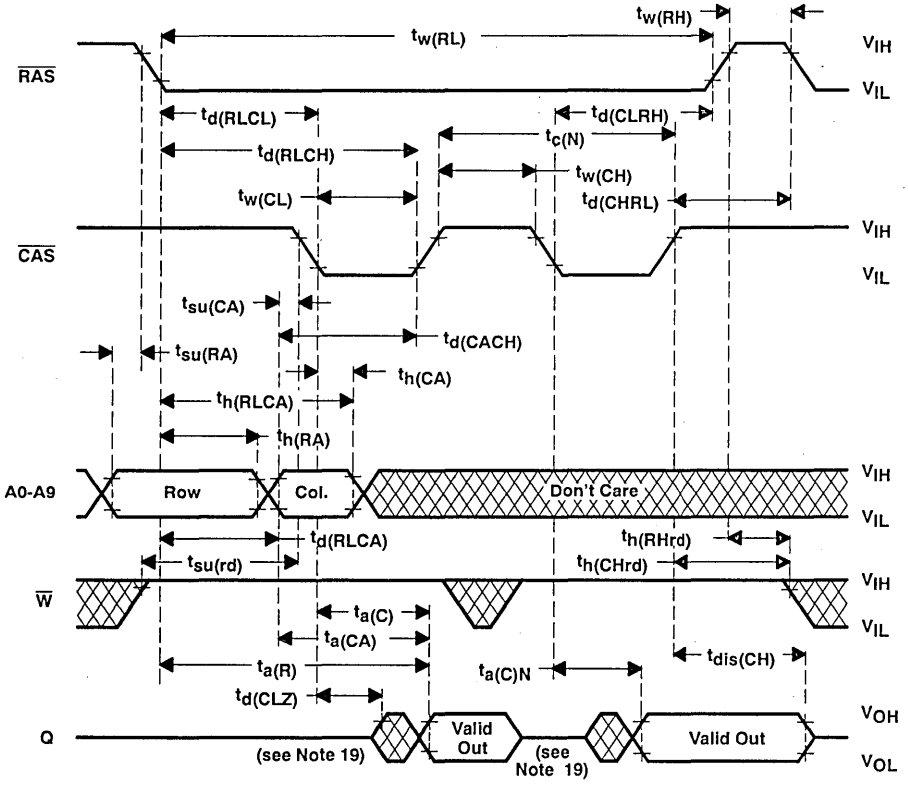
23. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

enhanced page-mode read-modify-write cycle timing



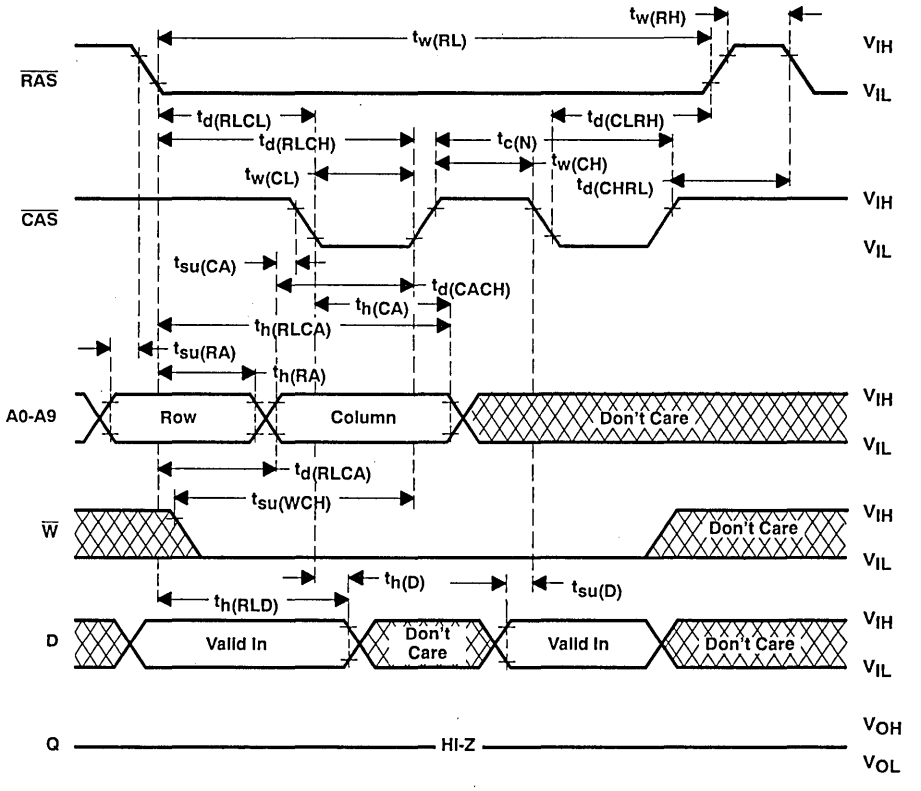
NOTES: 19. Output may go from high-impedance to an invalid state prior to the specified access time.
24. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

nibble-mode read cycle timing

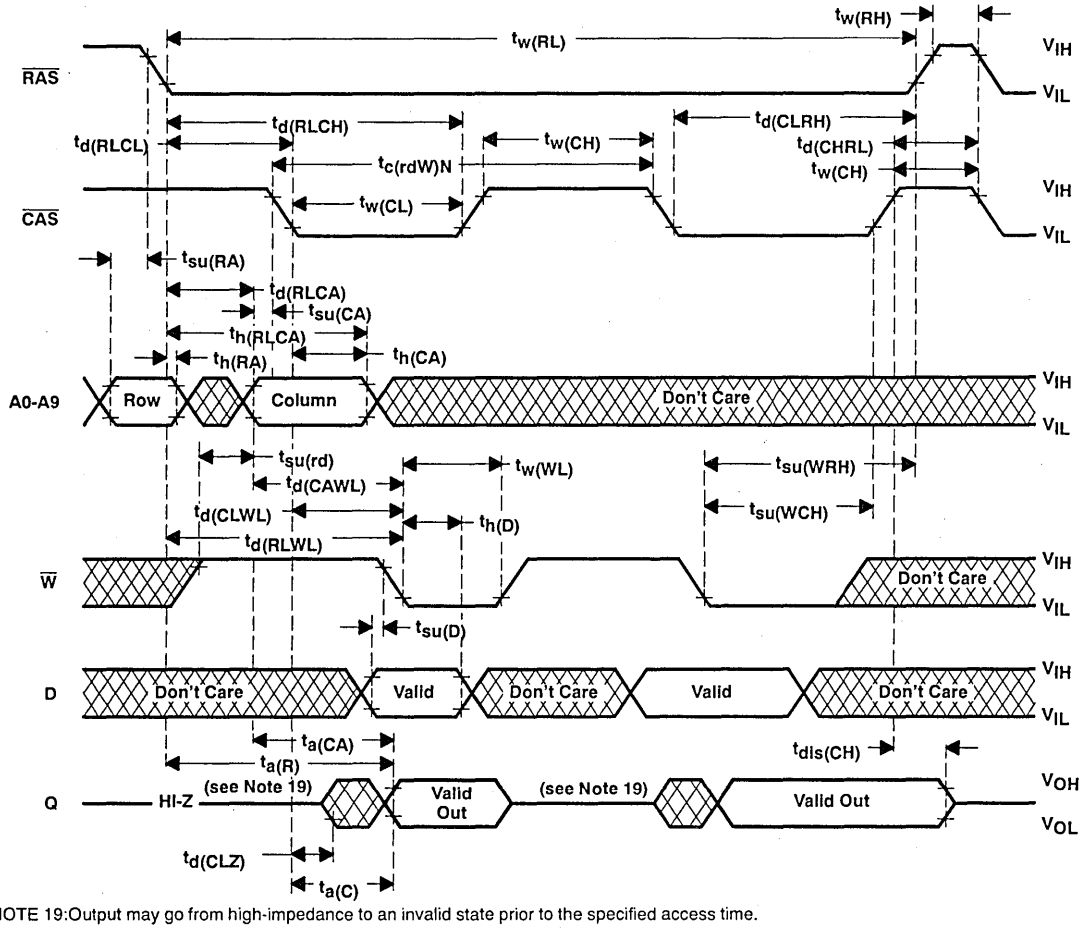


NOTE 19: Output may go from high-impedance to an invalid state prior to the specified access time.

nibble-mode write cycle timing

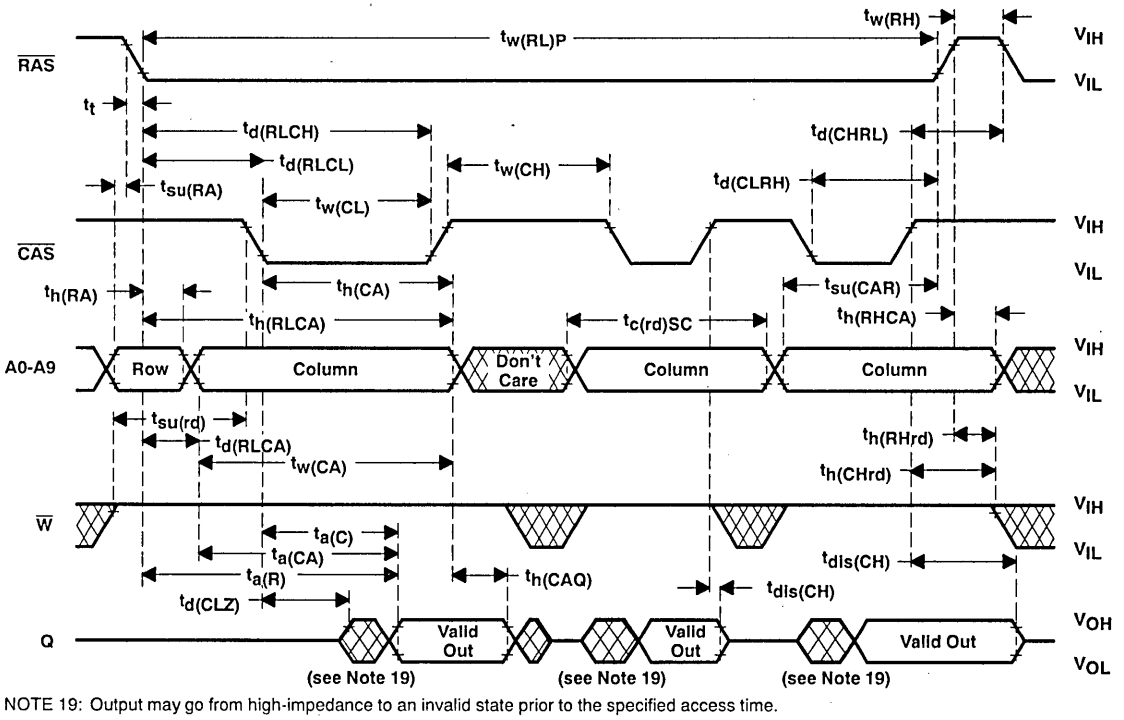


nibble-mode read-modify-write cycle timing



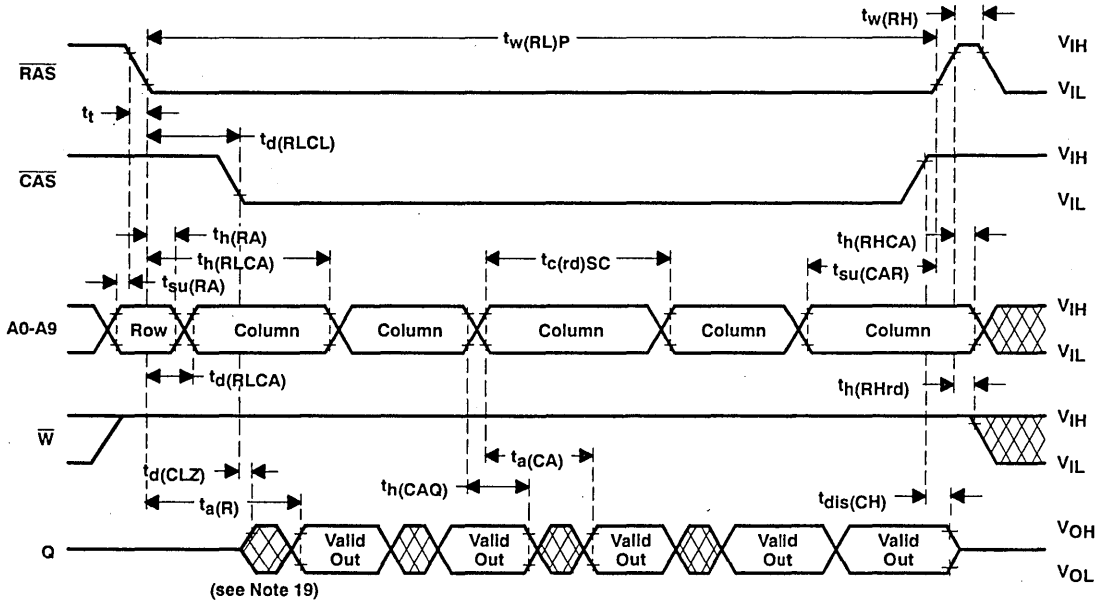
NOTE 19:Output may go from high-impedance to an invalid state prior to the specified access time.

static column decode mode read timing with $\overline{CAS}$ cycling



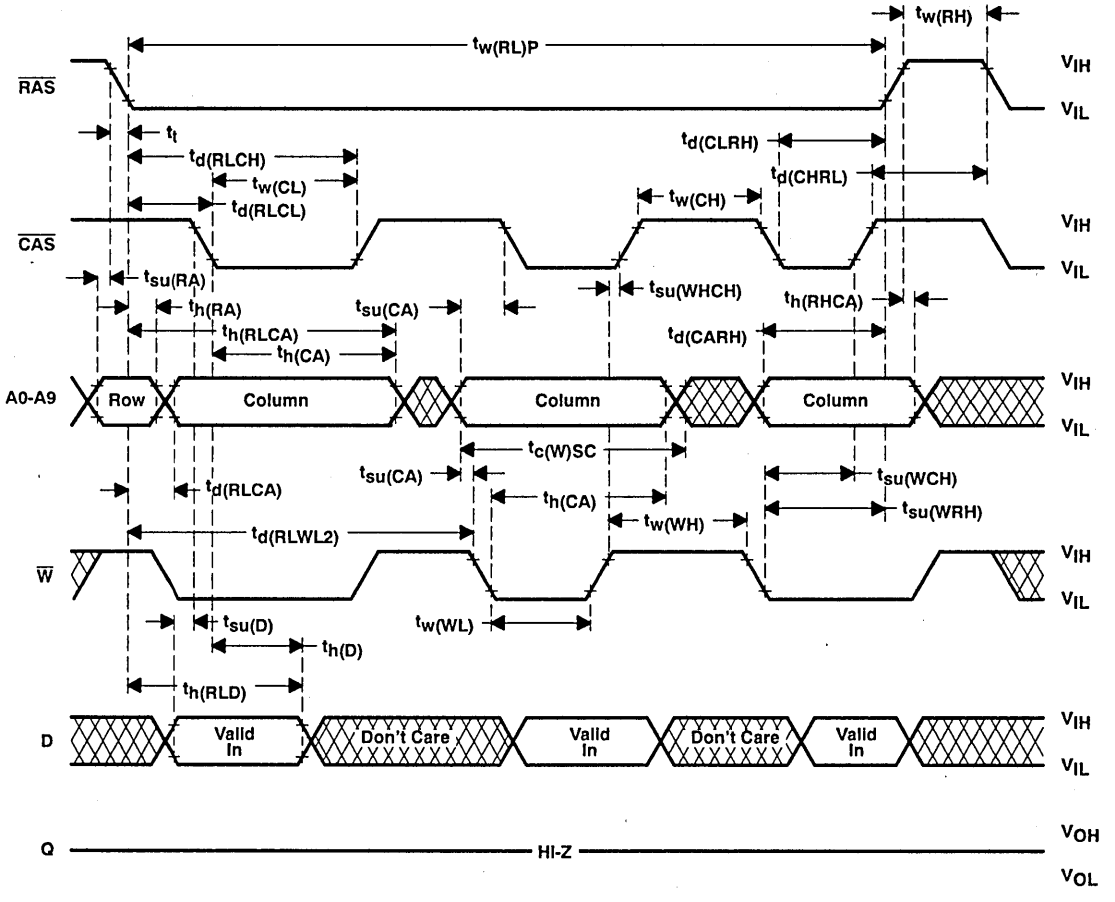
NOTE 19: Output may go from high-impedance to an invalid state prior to the specified access time.

static column decode mode read cycle timing

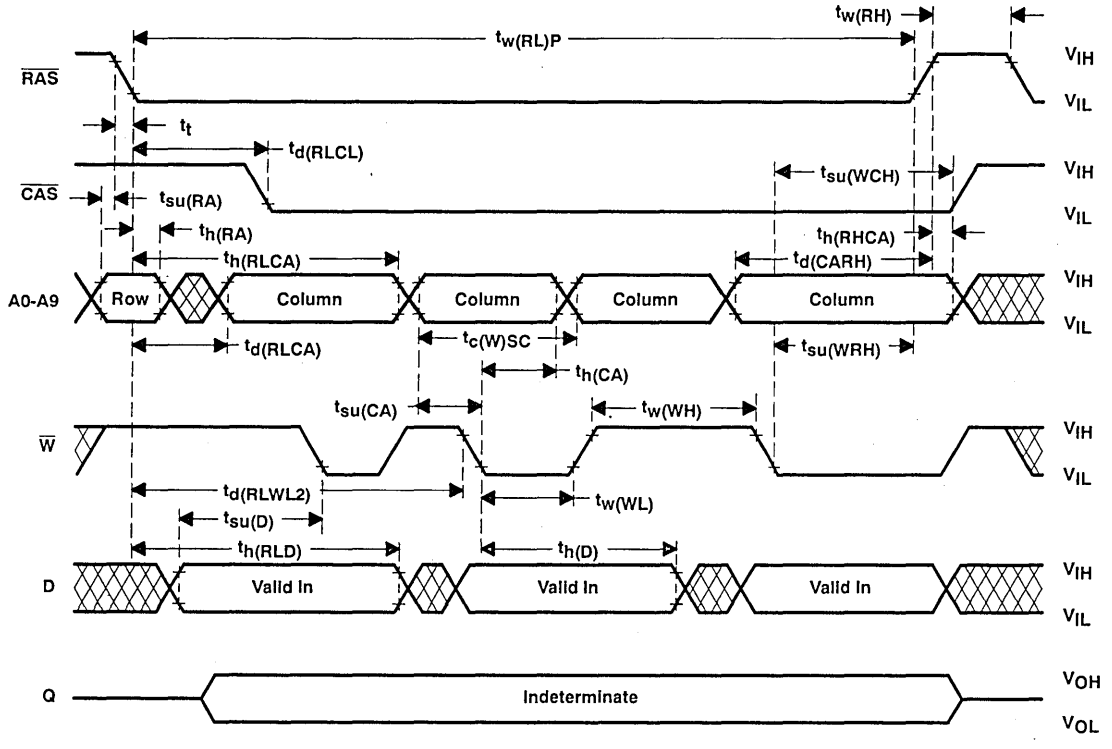


NOTE 19: Output may go from high-impedance to an invalid state prior to the specified access time.

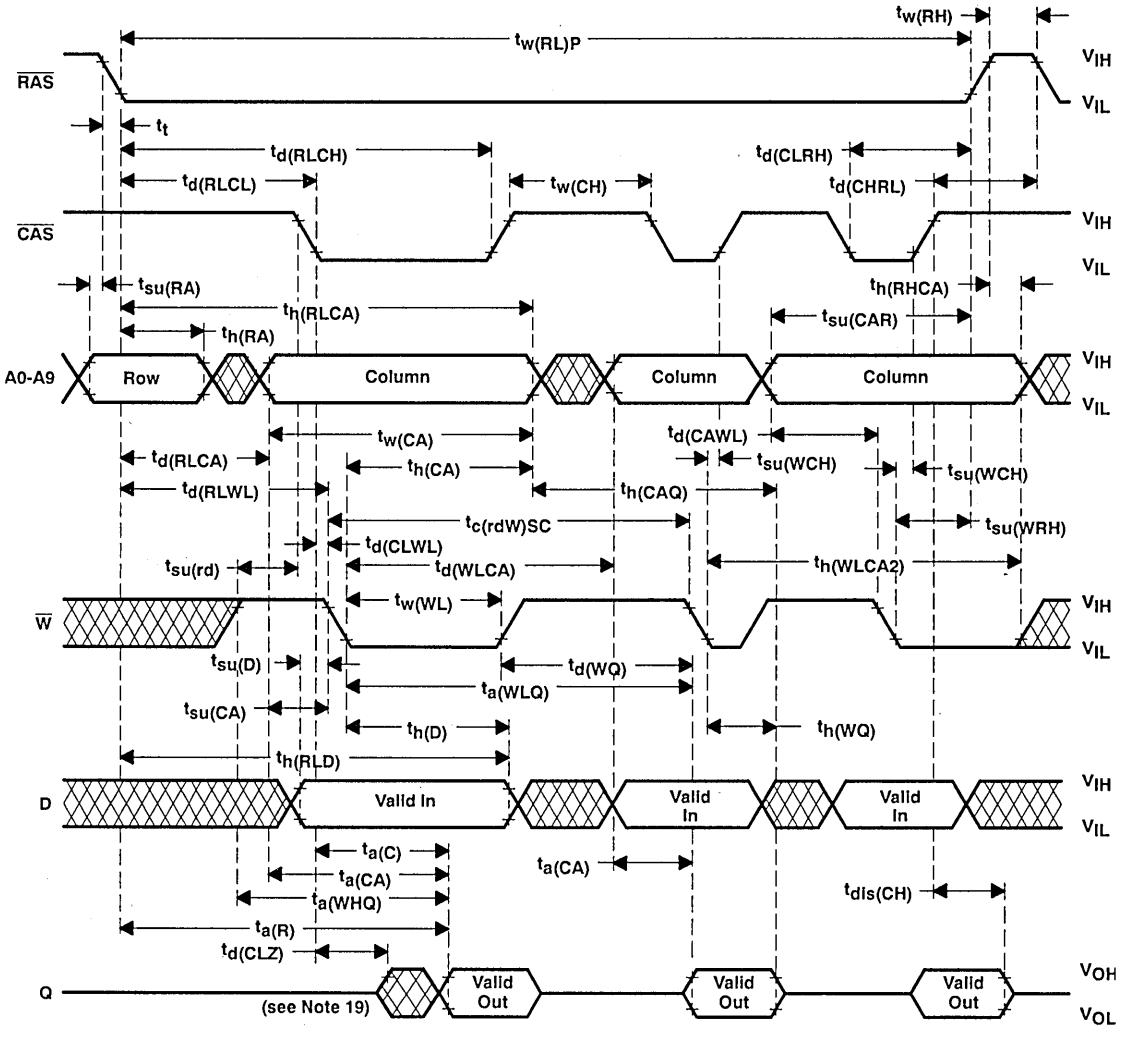
static column decode mode early write cycle timing



static column decode mode late write cycle timing

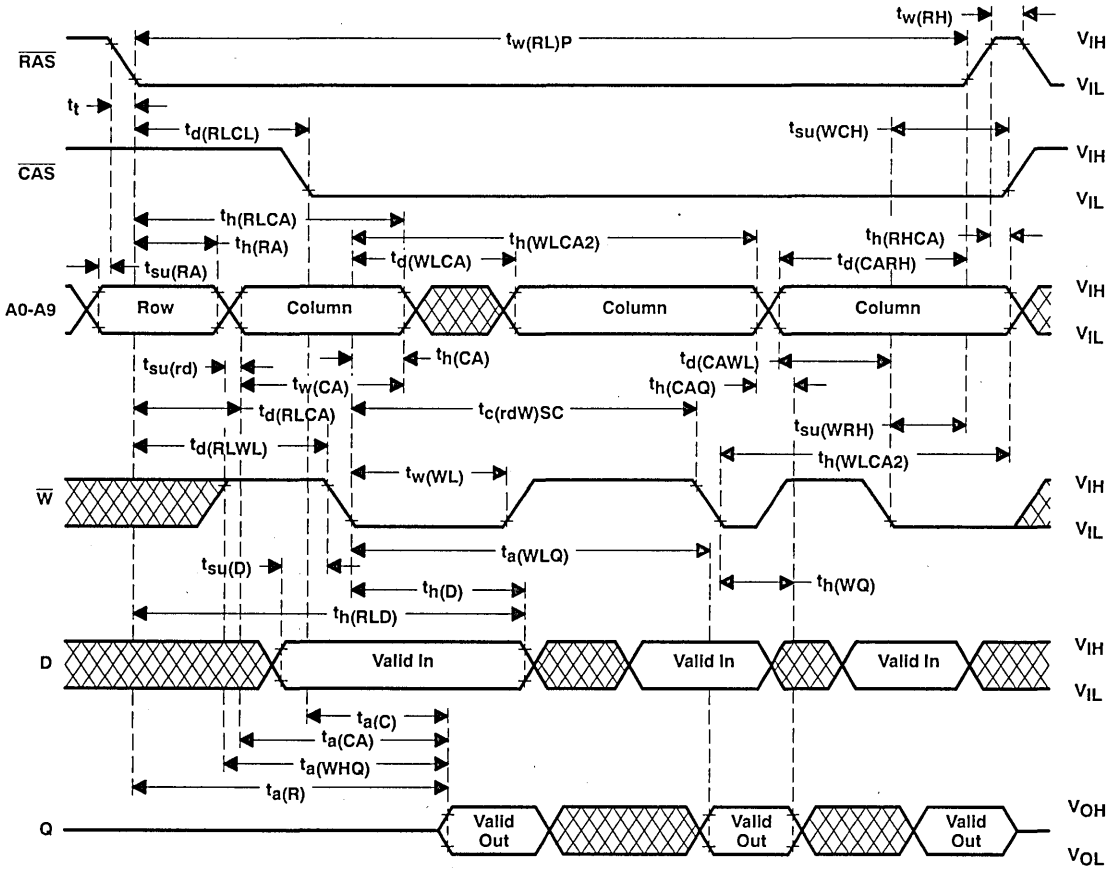


static column decode mode read-modify-write cycle timing with $\overline{CAS}$ cycling

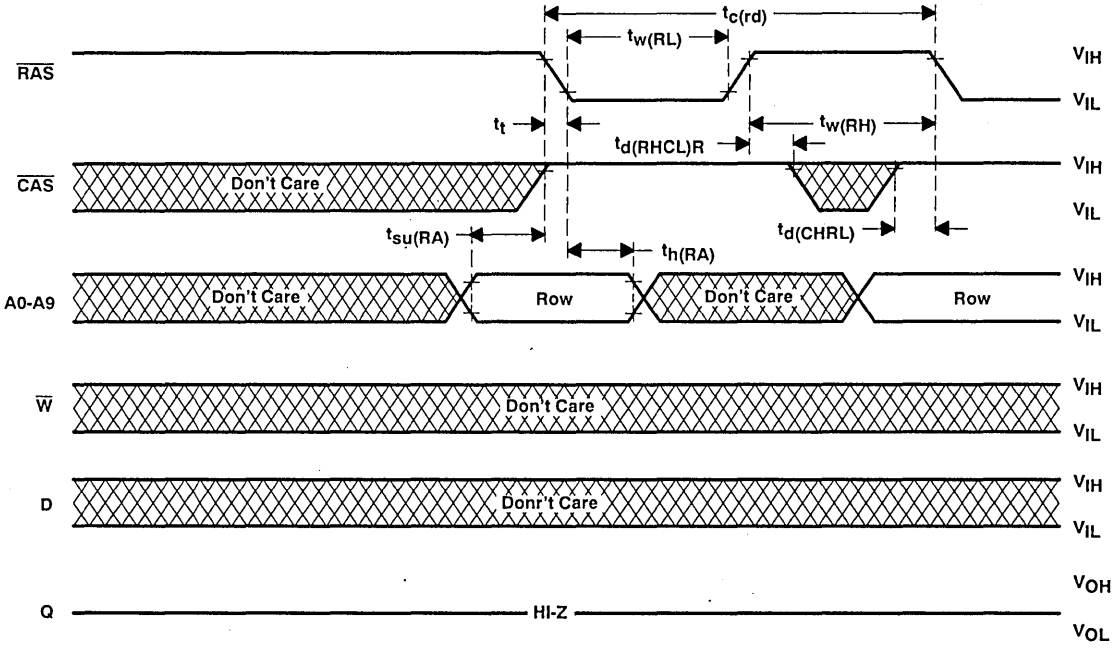


NOTE 19: Output may go from high-impedance to an invalid data state prior to the specified access time.

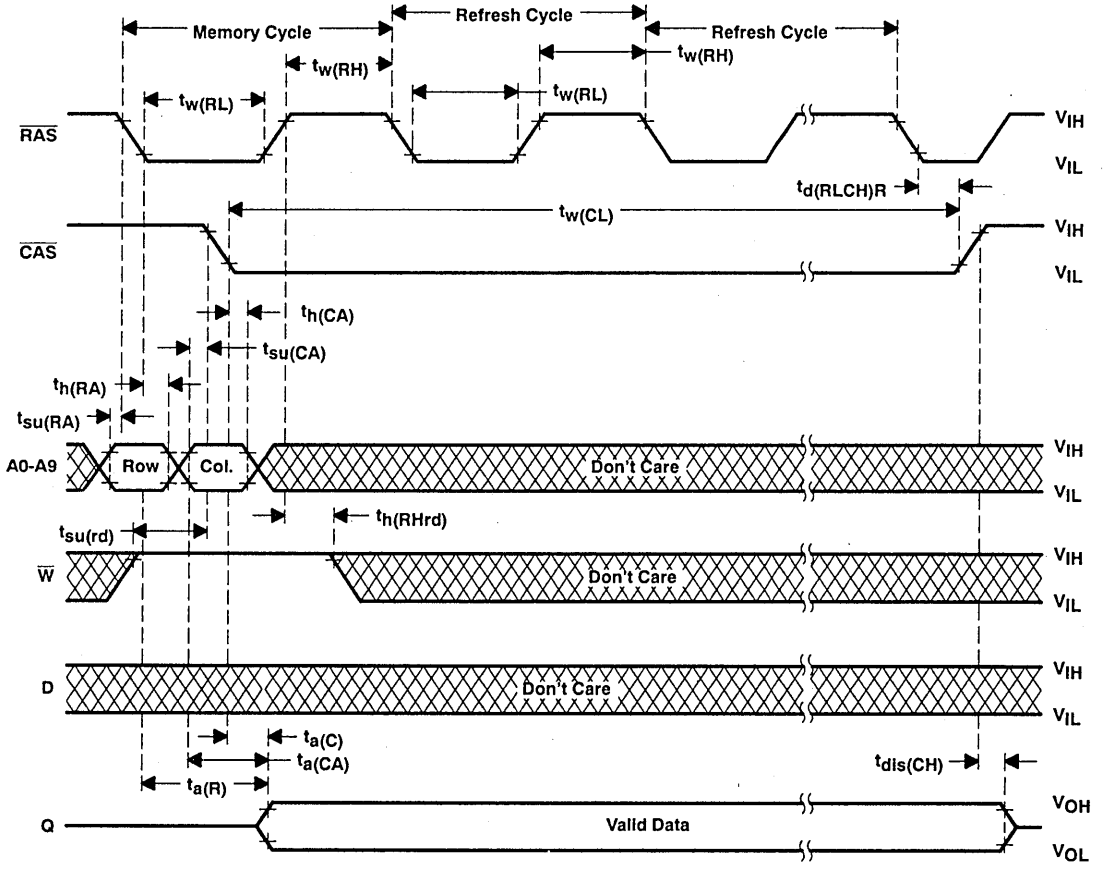
static column decode mode with read-modify-write cycle timing



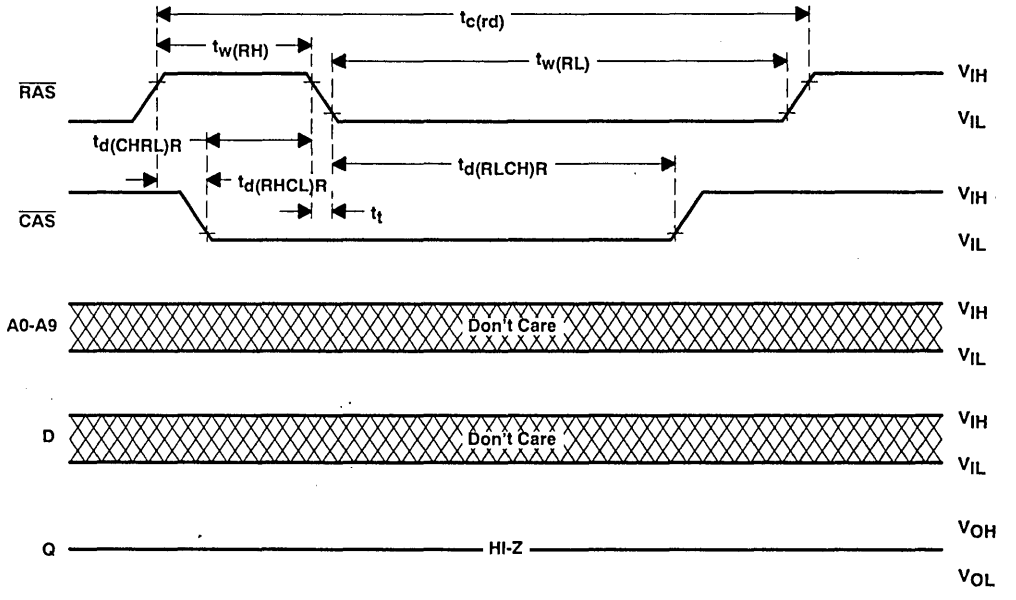
$\overline{RAS}$ only refresh timing



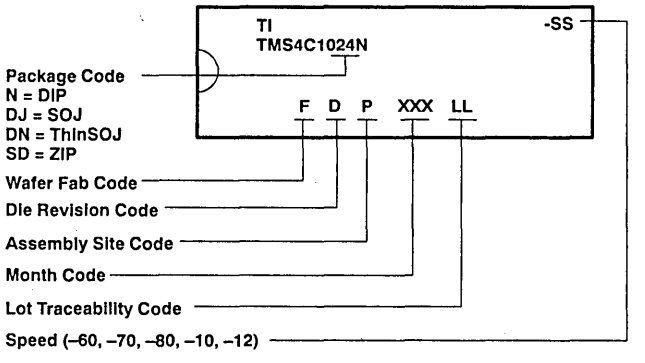
hidden refresh cycle



automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh timing



device symbolization

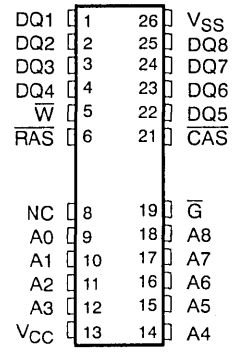


- 131 072 × 8 Organization
- Single 5-V Supply (10% Tolerance)
- Performance Ranges:

	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MAX)
'48C128/C138-70	70 ns	25 ns	40 ns	130 ns
'48C128/C138-80	80 ns	25 ns	40 ns	150 ns
'48C128/C138-10	100 ns	30 ns	45 ns	180 ns

- TMS48C128 — Enhanced Page Mode Operation with $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
- TMS48C138 — Write-Per-Bit Operation
- Long Refresh Period . . . 512-Cycle Refresh in 8 ms (Max)
- 3-State Unlatched Output
- Lower Power Dissipation
- Texas Instruments EPIC™ CMOS Process
- All Inputs and Clocks Are TTL Compatible
- High-Reliability Plastic 24/26-lead 300-Mil-Wide Surface Mount (SOJ) Package
- Operating Free-Air Temperature Range . . . 0°C to 70°C

DJ Package† (Top View)



†The package is shown for pinout reference only.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
$\overline{G}$	Data-Output Enable
NC	No Connect
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS48C128 and the TMS48C138 series are high-speed, 1 048 576-bit dynamic random-access memories organized as 131 072 words of eight bits each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 413 mW operating and 11 mW standby on 80 ns devices.

The EPIC™ technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{CC} peaks are 140 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS48C128 and TMS48C138 are offered in a 300-mil 24/26-lead plastic surface mount SOJ (DJ suffix) package. This package is characterized for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 256 columns specified by column addresses A0 through A7 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS48C128 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as "enhanced page mode." Valid column address may be presented immediately after t_{RAH} (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low) if t_{CAA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CAP} (access time from rising edge of $\overline{CAS}$).

write-per-bit operation (TMS48C138)

The $\overline{W}$ pin selects the write-per-bit option. The TMS48C138 is equipped with two modes of write operations. If $\overline{W}$ is held low on the falling edge of $\overline{RAS}$ (during a random access operation), the write-per-bit mode is enabled. When $\overline{RAS}$ has latched the write-per-bit mask on-chip, input data is driven onto the DQ pins and is latched on the falling edge of the latter of $\overline{CAS}$ or $\overline{W}$ (for early write operation, $\overline{W}$ can remain low for the entire $\overline{RAS}$ low period). If a 0 is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, then the write circuits for that particular I/O will be inhibited and data will not be written from that I/O. If a 1 is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, then the write circuits for that particular I/O will not be inhibited and data will be written from that I/O.

Important: The write-per-bit operation is selected only if $\overline{W}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{W}$ is held high on the falling edge of $\overline{RAS}$, the write-per-bit function is not enabled and the write operation is identical to a standard ×4 or ×8 DRAM, with all I/Os being written by the data appearing on the DQ pins when the latter of $\overline{W}$ or $\overline{CAS}$ is brought low.

Table 1. State When $\overline{RAS}$ Falls

$\overline{W}$	DQ1-DQ8	MODE
1	X	Write enable at DQ1-DQ8
0	1	Write to DQ enabled
0	0	Write to DQ disabled

address (A0 through A8)

Seventeen address bits are required to decode 131 072 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched on to the chip by the row-address strobe ($\overline{RAS}$). Then eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the first column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting a write operation with $\overline{G}$ grounded.

data in (DQ1-DQ8)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1-DQ8)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{G}$ are brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{CAA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state.

output enable ($\overline{G}$)

$\overline{G}$ controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every eight milliseconds to retain data. This can be achieved by strobing each of the 512 rows (A0-A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

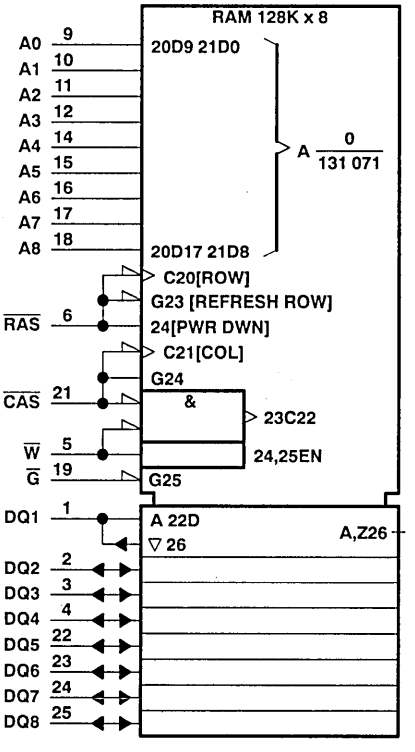
$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

power-up

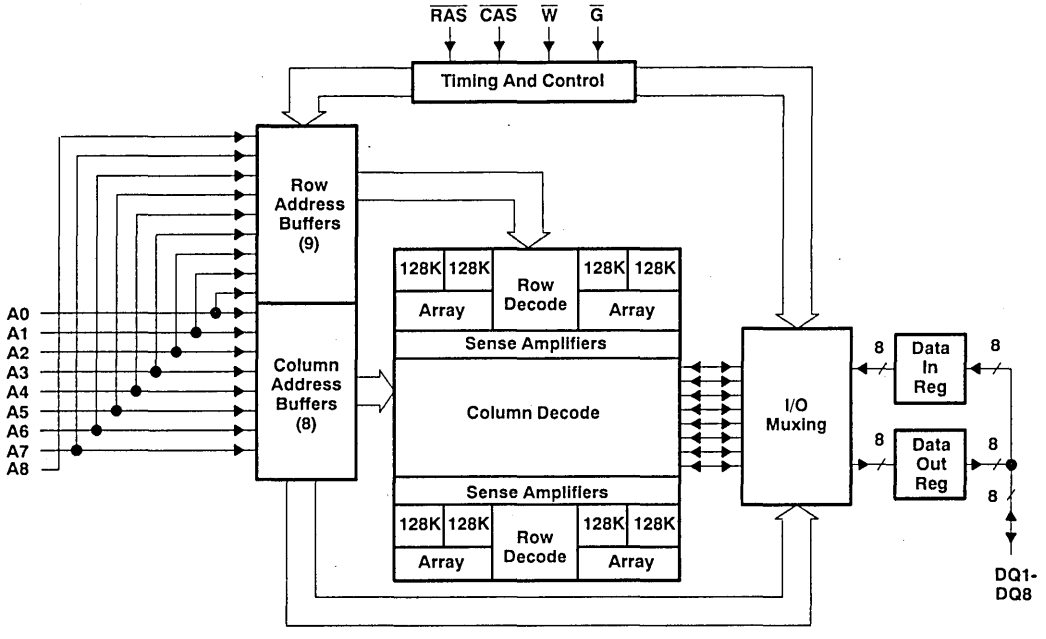
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after power-up to the full V_{CC} level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1†		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

† Characterized at 5.5 V V_{CC}.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'48C128-70 '48C138-70		'48C128-80 '48C138-80		'48C128-10 '48C138-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 5.8 V, V_{CC} = 5 V, All other pins = 0 to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read/write cycle current	t_{RWC} = minimum, V_{CC} = 5.5 V		85		80		70	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		2		2		2	mA
I_{CC3}	Average refresh circuit ($\overline{RAS}$-only or CBR)	t_{RWC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		80		75		65	mA
I_{CC4}	Average page current	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		60		50		45	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
$C_{i(G)}$	Input capacitance, output-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER		'48C128-70 '48C138-70		'48C128-80 '48C138-80		'48C128-10 '48C138-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		25		25		30	ns
t_{CAA}	Access time from column address		40		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80		100	ns
t_{GAC}	Access time from $\overline{G}$ low		25		25		30	ns
t_{CAP}	Access time from column precharge		45		45		50	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 4)	0	20	0	20	0	25	ns
t_{GOFF}	Output disable time after $\overline{G}$ high (see Note 4)	0	20	0	20	0	25	ns

NOTE 4: t_{OFF} and t_{GOFF} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

		'48C128-70 '48C138-70		'48C128-80 '48C138-80		'48C128-10 '48C138-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time (see Note 6)	130		150		180		ns
t_{WC}	Write cycle time	130		150		180		ns
t_{RWC}	Read-write/read-modify-write cycle time	185		205		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 7)	50		50		55		ns
t_{PCM}	Page-mode read-modify-write cycle time	105		105		120		ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 8)	25	10 000	25	10 000	30	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	50		60		70		ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	70	10 000	80	10 000	100	10 000	ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	70	100 000	80	100 000	100	100 000	ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time before $\overline{W}$ low (see Note 10)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	20		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	20		20		25		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low (see Note 10)	15		15		20		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		12		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 12)	55		60		70		ns
t_{DH}	Data hold time after $\overline{CAS}$ low (see Note 10)	15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 12)	55		60		70		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	0		0		10		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (see Note 11)	15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 12)	55		60		70		ns

Continued next page.

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_T = 5 ns.
7. To guarantee $t_{c(P)}$ min, $t_{su(CA)}$ should be greater than or equal to $t_{w(CH)}$.
8. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time (t_{CAS}).
9. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
13. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5) (concluded)

		'48C128-70 '48C138-70		'48C128-80 '48C138-80		'48C128-10 '48C138-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{GH}	$\overline{G}$ command hold time	20		20		25		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	70		80		100		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	25		25		30		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 14)	55		55		65		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)	20	45	22	55	25	70	ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 15)	15	30	17	40	20	55	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	40		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	40		40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)	100		110		135		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (see Note 14)	70		70		80		ns
t_{CLZ}	Delay time, $\overline{CAS}$ low to DQ in low-Z	0		0		0		ns
t_{GDD}	Delay time, $\overline{G}$ high before data at DQ	20		20		25		ns
t_{GSR}	Delay time, $\overline{G}$ low to $\overline{RAS}$ high	25		25		30		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	15		20		25		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	0		0		0		ns
t_{WBS}	Write-per-bit setup time	0		0		0		ns
t_{WBH}	Write-per-bit hold time	10		10		10		ns
t_{WDS}	Write-per-bit selection setup time	0		0		0		ns
t_{WDH}	Write-per-bit selection hold time	10		10		10		ns
t_{REF}	Refresh time interval		8		8		8	ms
t_T	Transition time	3	50	3	50	3	50	ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
14. Read-modify-write operation only.
15. Maximum value specified only to guarantee access time.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

PARAMETER MEASUREMENT INFORMATION

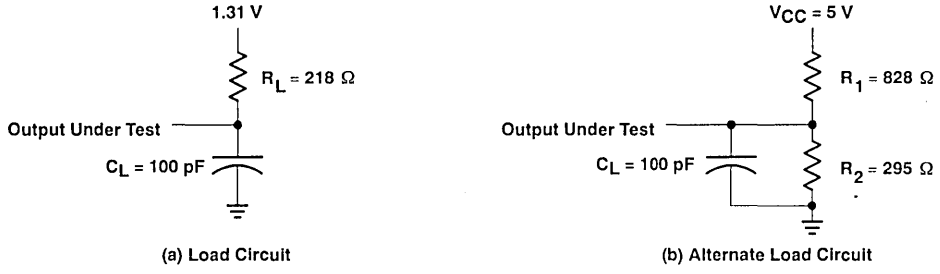
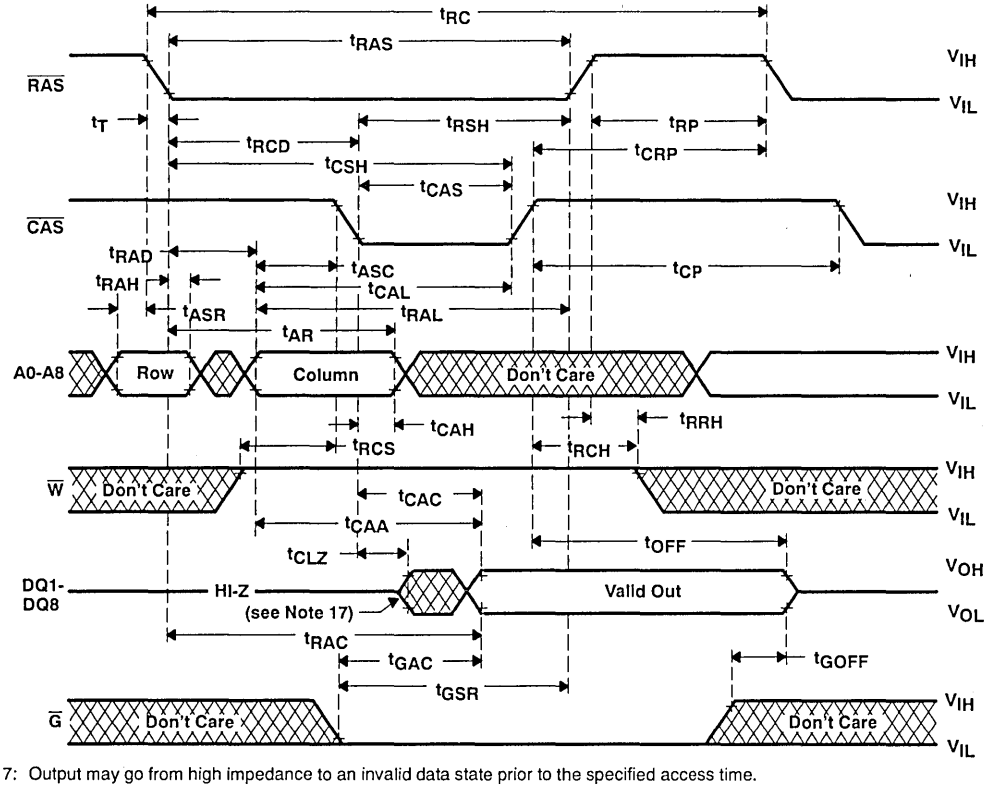


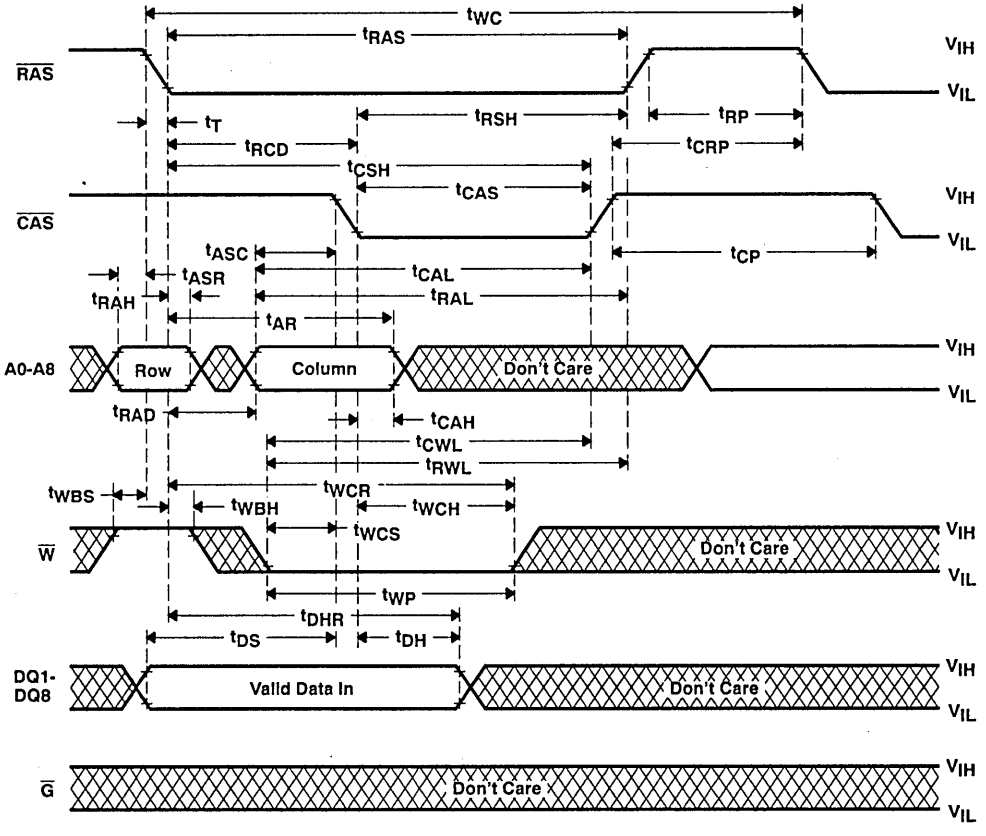
Figure 1. Load Circuits For Timing Parameters

read cycle timing

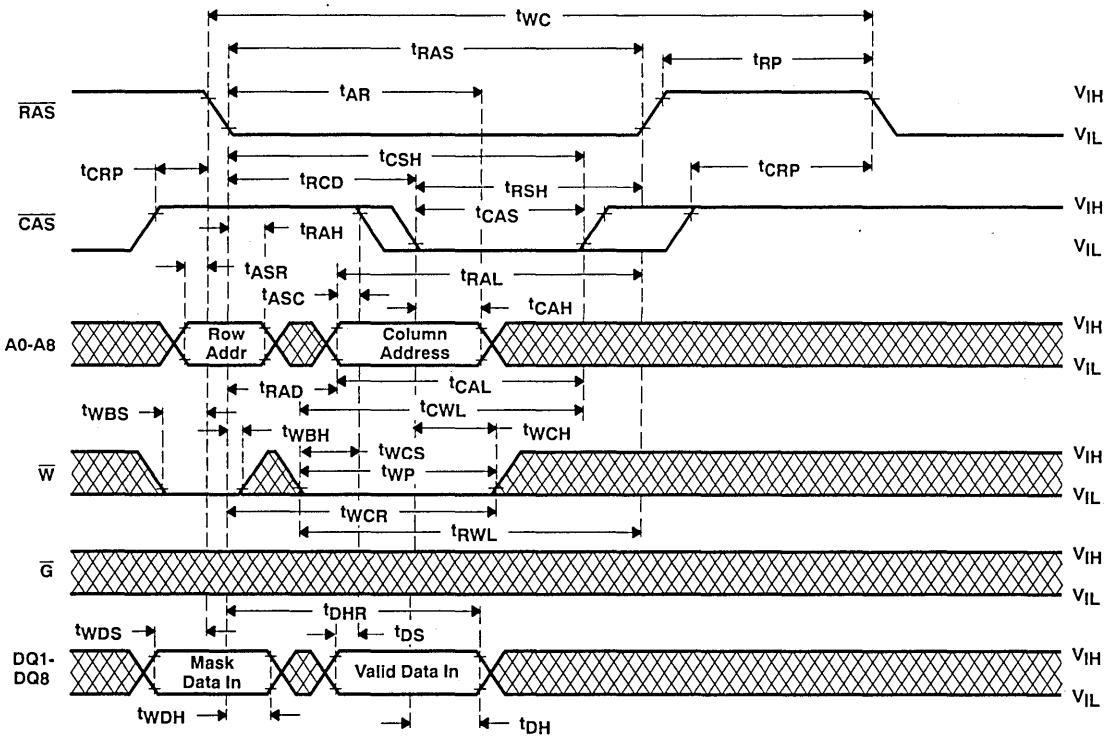


NOTE 17: Output may go from high impedance to an invalid data state prior to the specified access time.

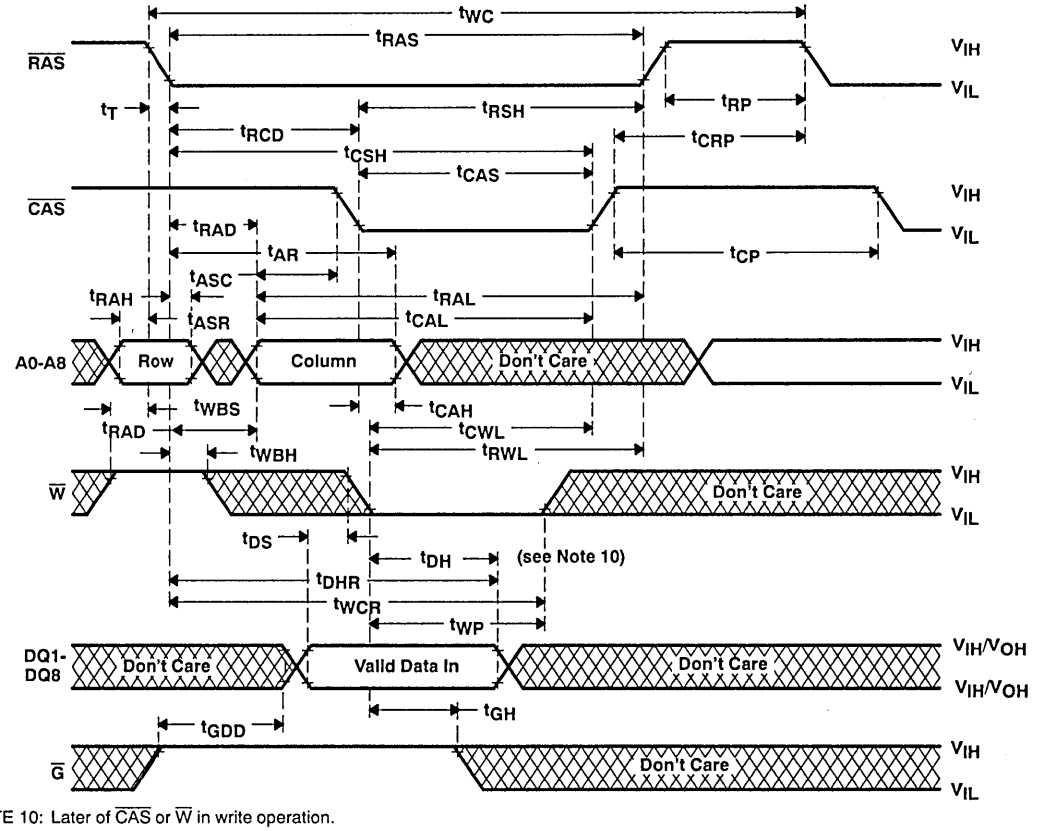
early write cycle timing



early write cycle (write-per-bit selected)

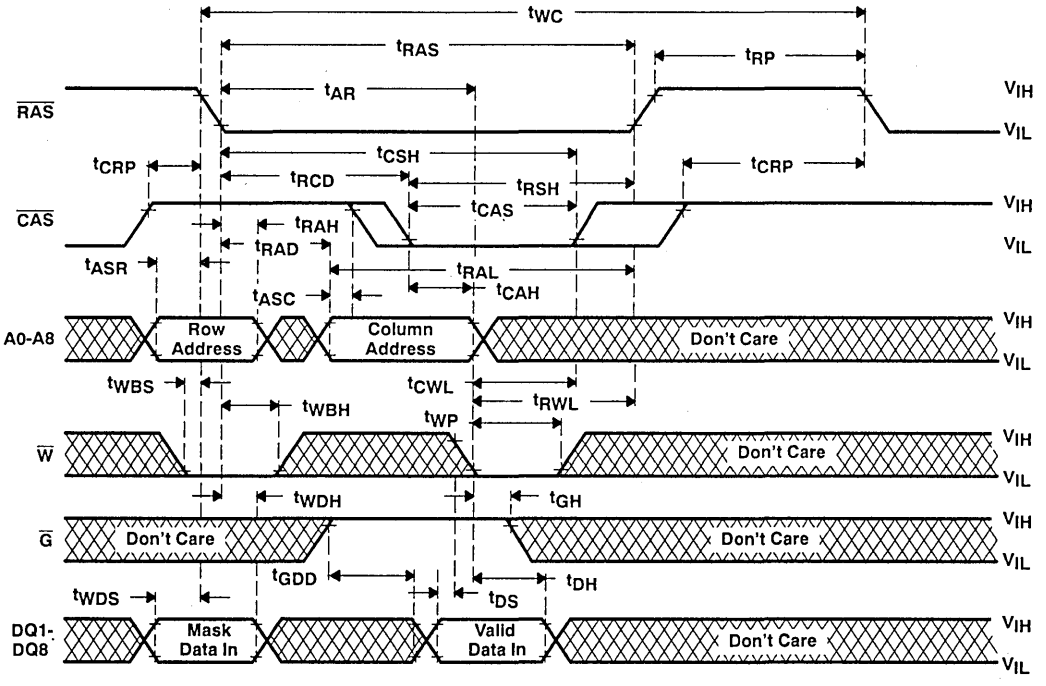


write cycle timing

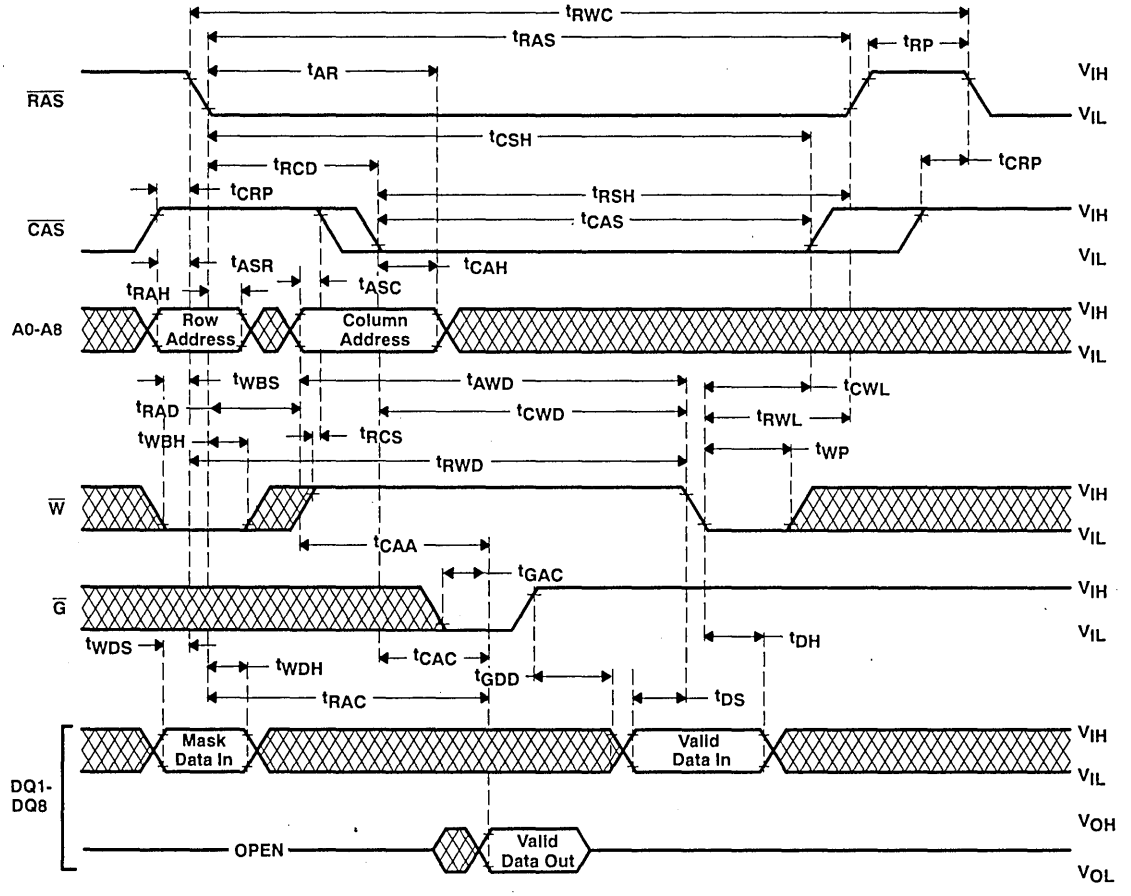


NOTE 10: Later of $\overline{CAS}$ or $\overline{W}$ in write operation.

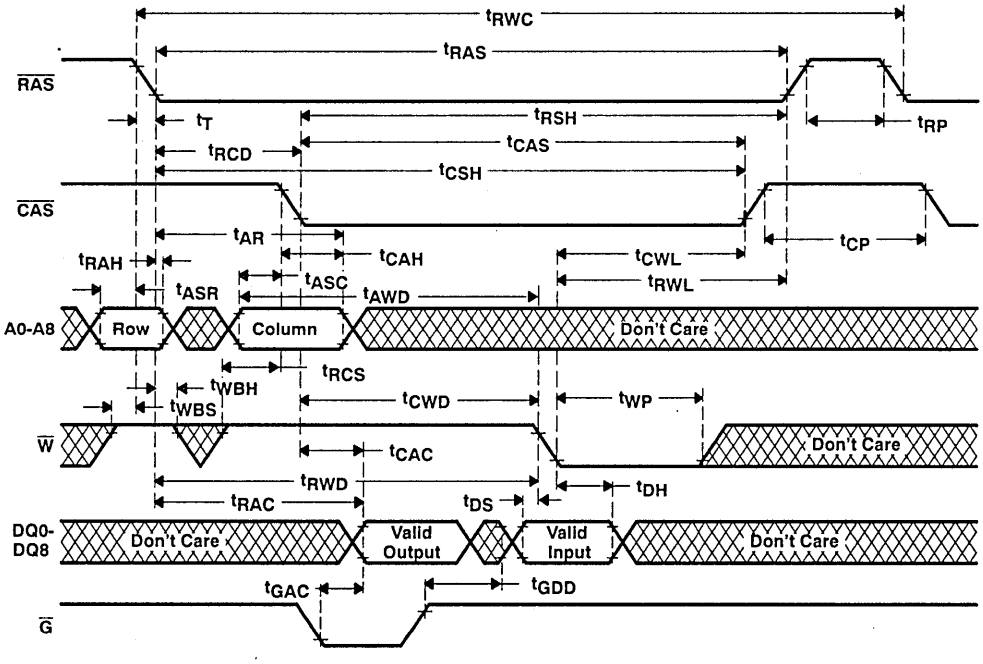
write cycle (write-per-bit selected)



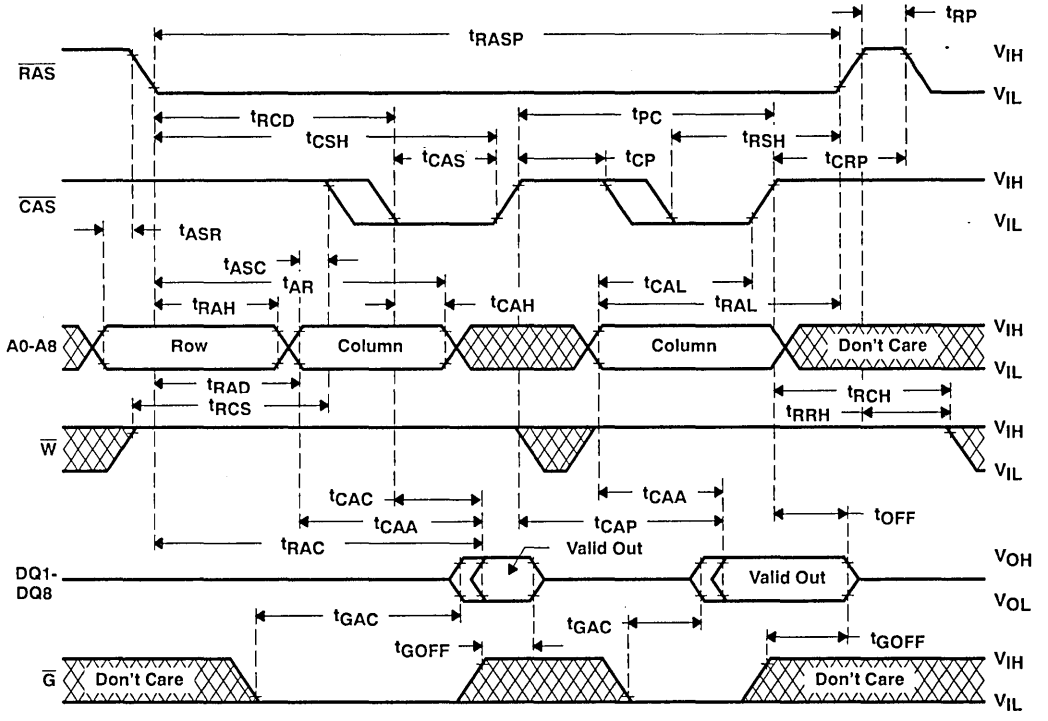
read-modify-write cycle (write-per-bit selected)



read-modify-write cycle timing

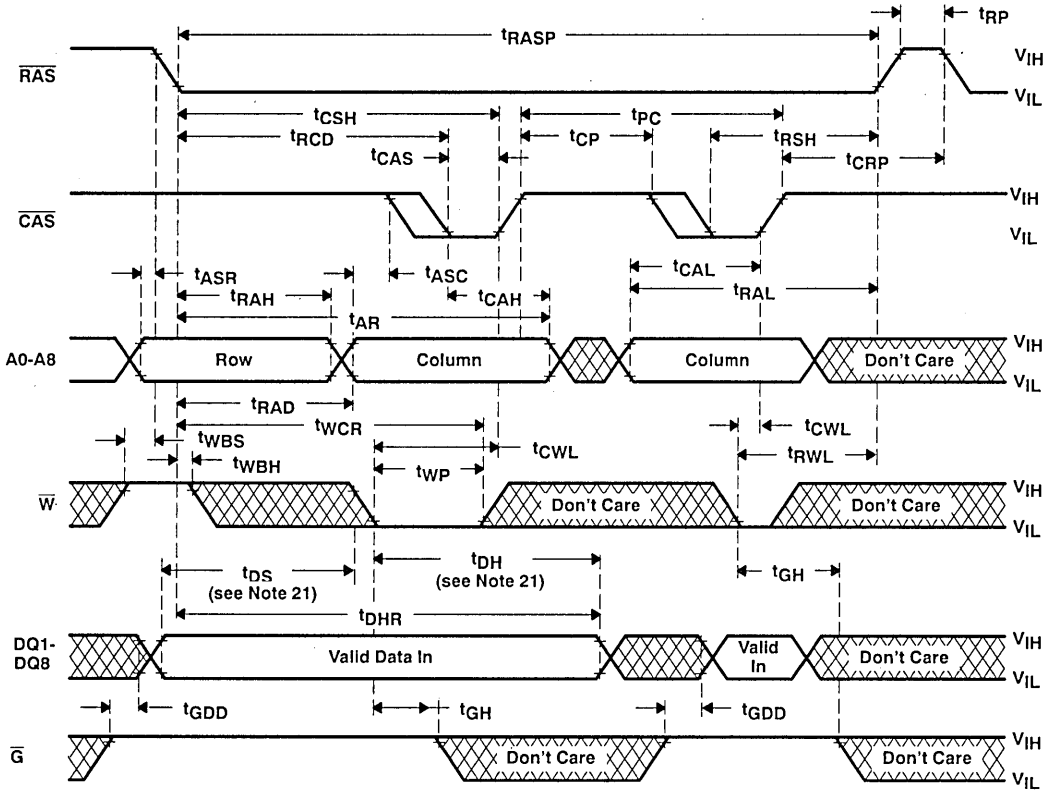


enhanced page-mode read cycle timing



NOTES:17. Output may go from high impedance to an invalid data state prior to the specified access time.
18. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
19. Access time is t_{CAP} or t_{CAA} dependent.

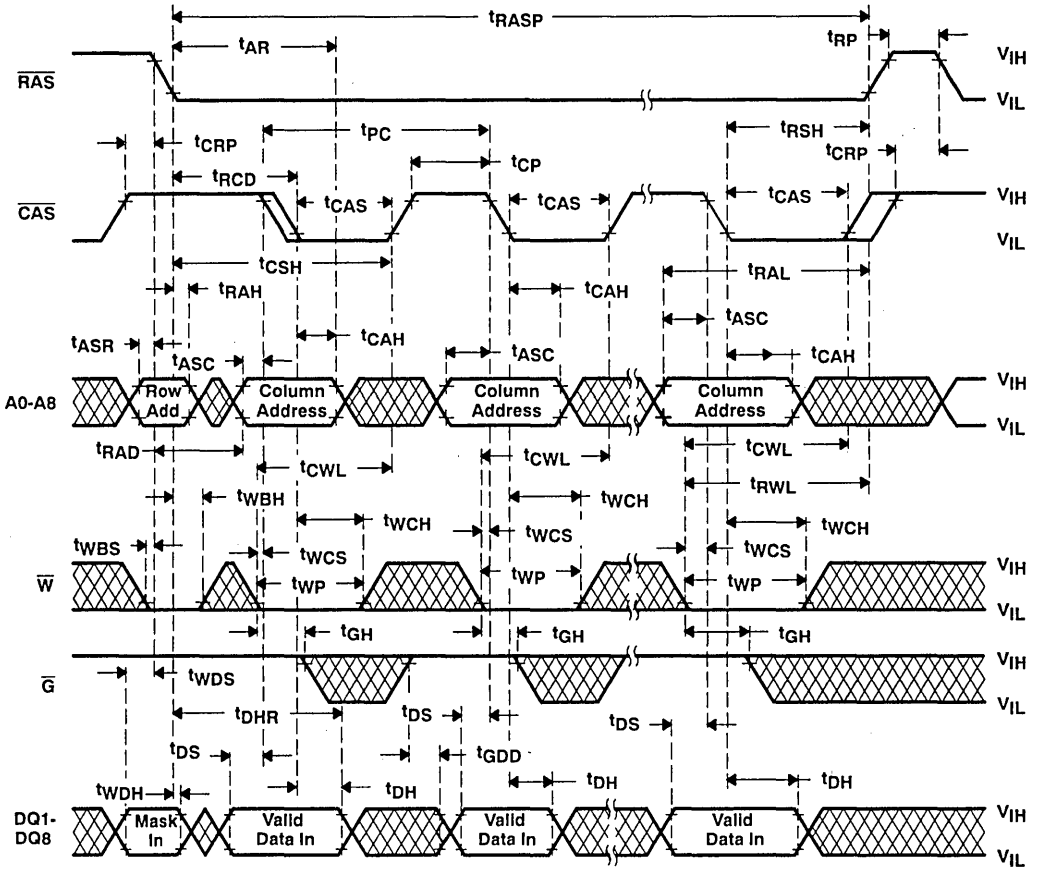
enhanced page-mode write cycle timing



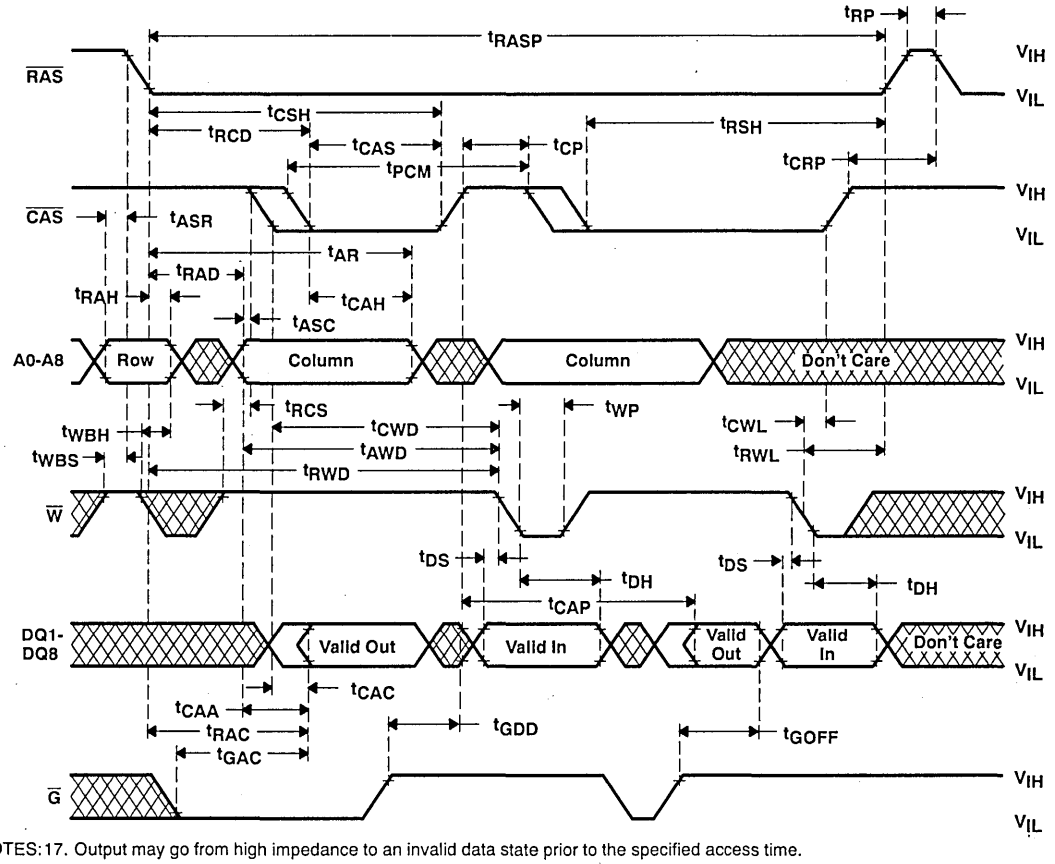
NOTES: 20. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

21. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

enhanced page-mode write cycle (write-per-bit selected)

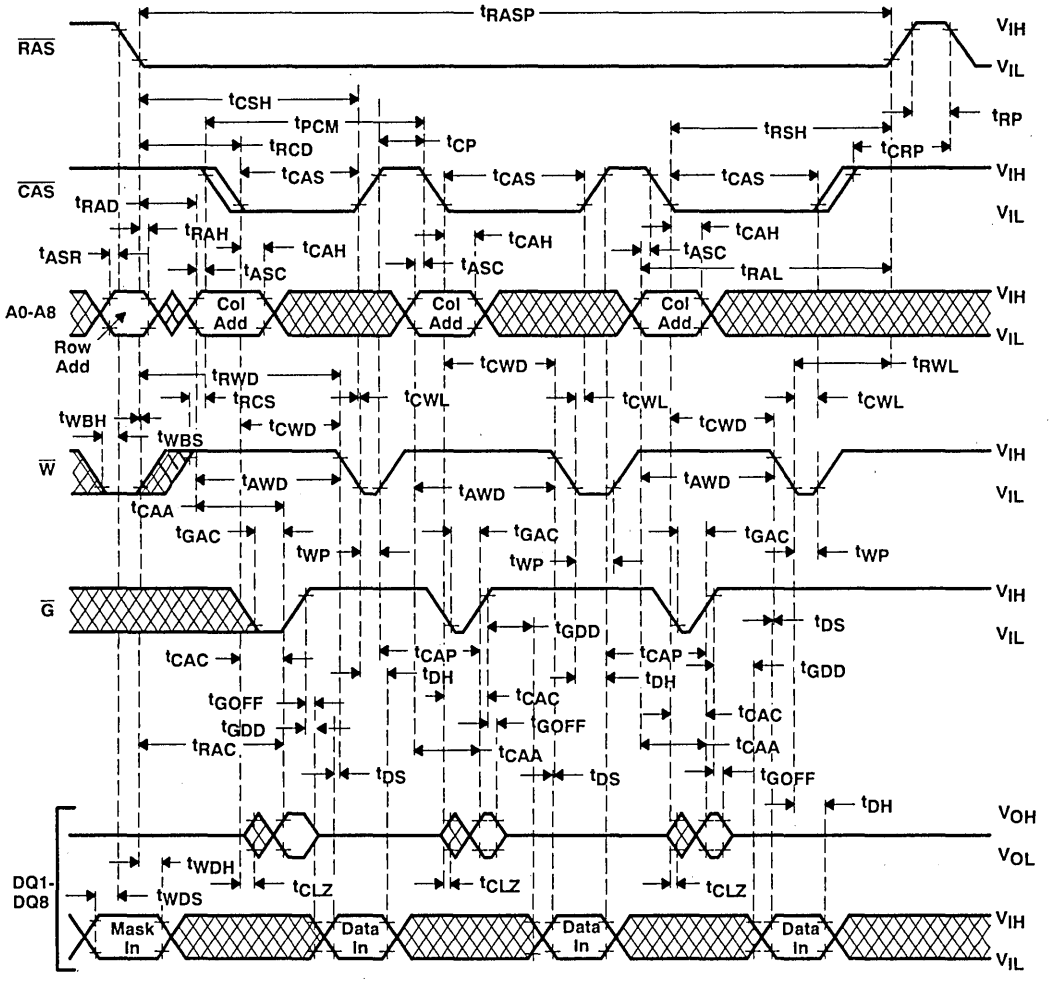


enhanced page-mode read-modify-write cycle timing

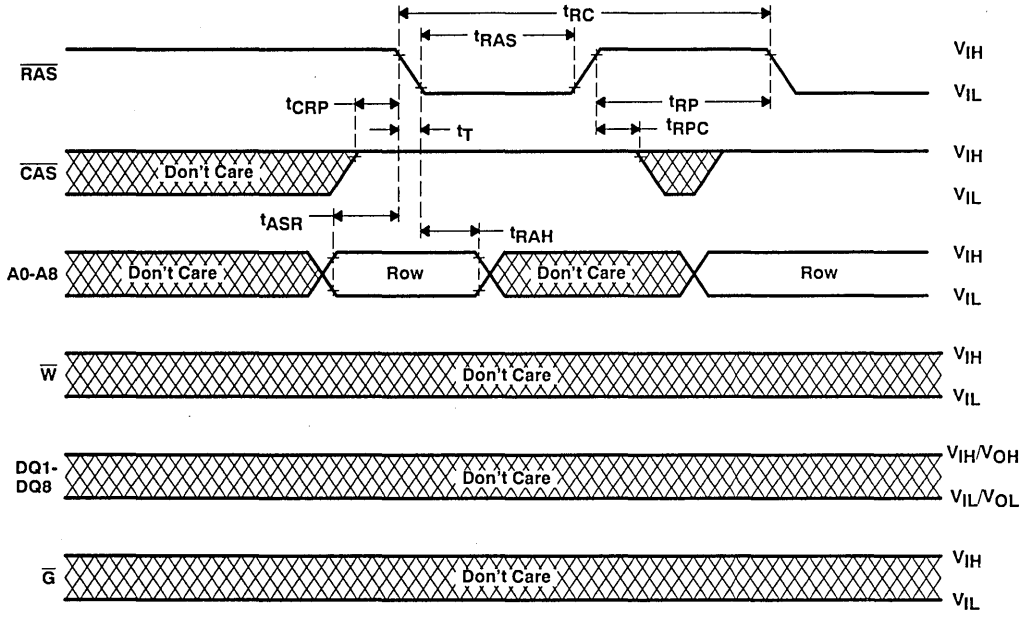


NOTES: 17. Output may go from high impedance to an invalid data state prior to the specified access time.
22. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.

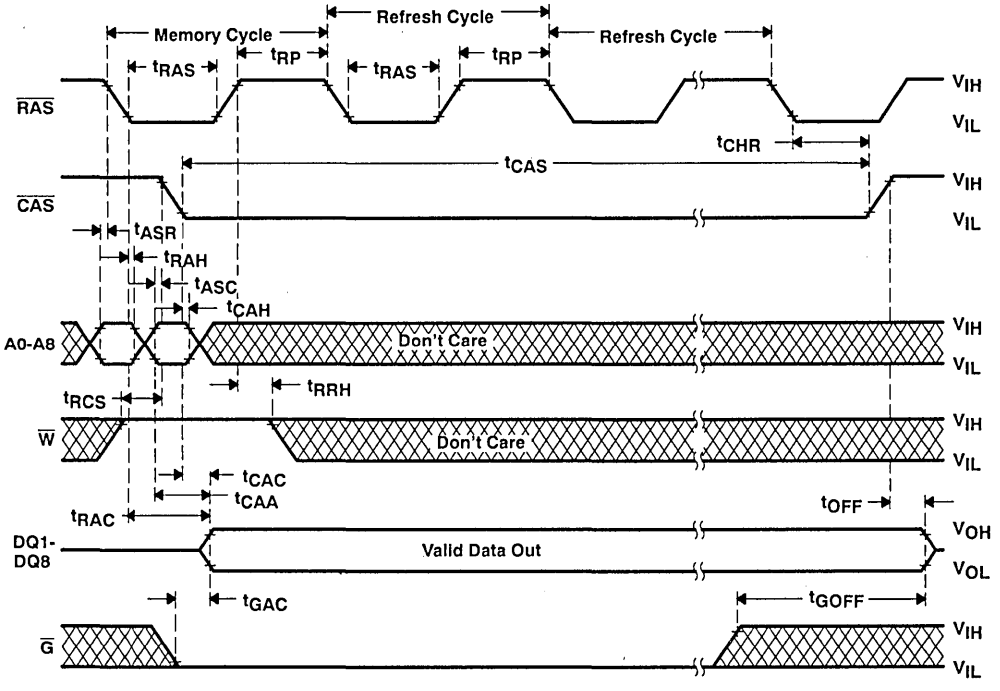
enhanced page-mode read-modify-write cycle (write-per-bit selected)



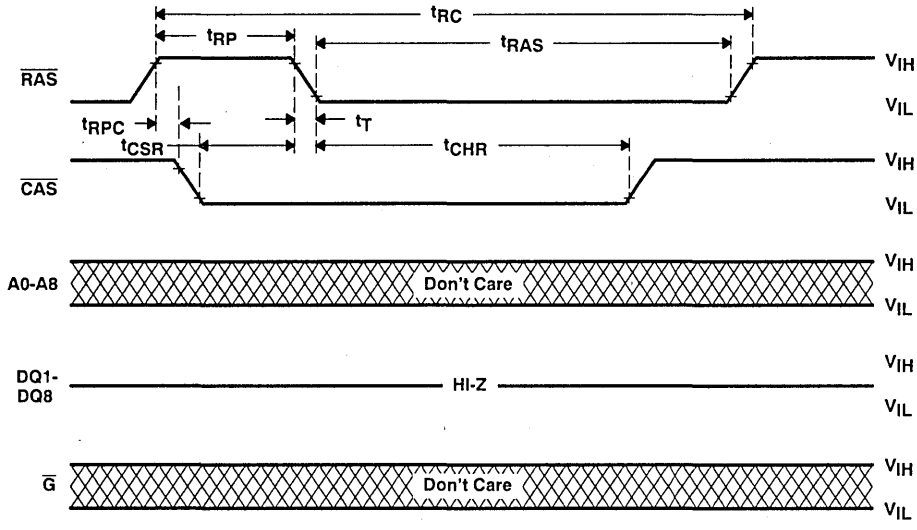
$\overline{\text{RAS}}$-only refresh timing



hidden refresh cycle



automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



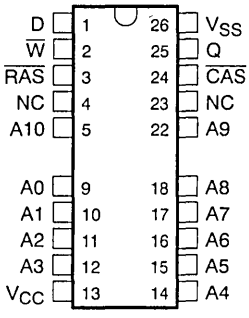
This Data Sheet is Applicable to All TMS44100s Symbolized With Revision "B" and Subsequent Revisions as Described on Page 5-106.

- **Organization . . . 4 194 304 × 1**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

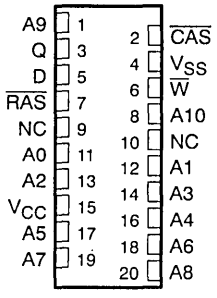
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS44100-60	60 ns	15 ns	30 ns	110 ns
TMS44100-70	70 ns	18 ns	35 ns	130 ns
TMS44100-80	80 ns	20 ns	40 ns	150 ns
TMS44100-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page-Mode Operation for Faster Memory Access**
  - **— Higher Data Bandwidth than Conventional Page-Mode Parts**
  - **— Random Single-Bit Access Within a Row With a Column Address**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 1024-Cycle Refresh in 16 ms (Max)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks are TTL Compatible**

DM and DJ Packages† (Top View)



SD Package† (Top View)



†The packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0-A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

- **High-Reliability Plastic 300-mil and 350-mil 20/26-Lead Surface Mount (SOJ) Packages and a 20-Pin Zig-Zag In-line Package**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**

description

The TMS44100 series are high-speed 4 194 304-bit dynamic random-access memories, organized as 4 194 304 words of one bit each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 360 mW operating and 6 mW standby.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS44100 is offered in a 300-mil 20/26-lead plastic surface mount SOJ package (DJ suffix), a 350-mil 20/26-lead plastic surface mount SOJ package (DM suffix), and a 20-pin plastic ZIP package (SD suffix). All packages are characterized for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS44100 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0 through A10)

Twenty address bits are required to decode 1 of 4 194 304 storage cell locations. Eleven row-address bits are set up on inputs A0 through A10 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The eleven column-address bits are set up on pins A0 through A10 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{AA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every sixteen milliseconds to retain data. This can be achieved by strobing each of the1024 rows (A0-A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used

for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter t_{CSR}] and holding it low after $\overline{RAS}$ falls [see parameter t_{CHR}]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

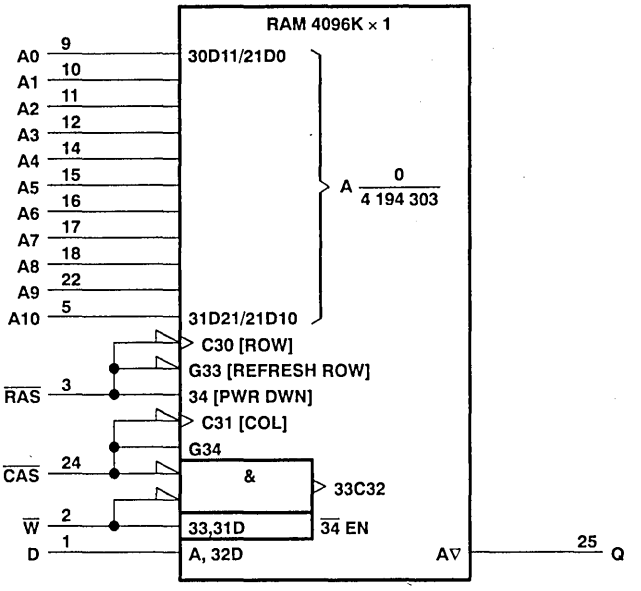
power-up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

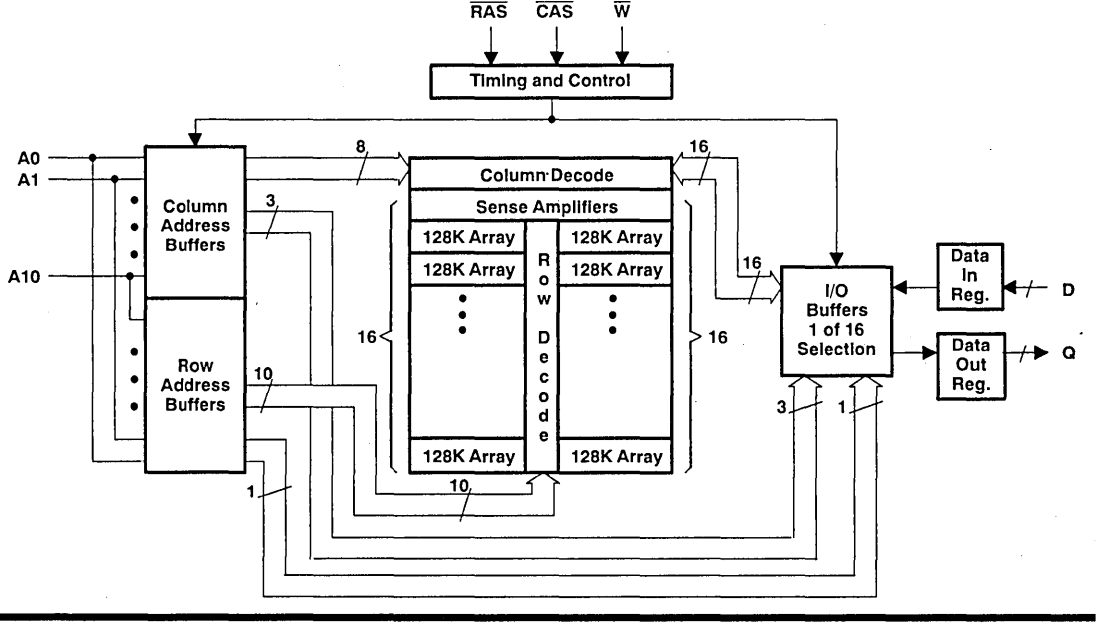
An industry standard Design For Test (DFT) mode is incorporated in the TMS44100. A $\overline{CAS}$-before-$\overline{RAS}$ cycle with $\overline{W}$ low (WCBR) cycle is used to enter test mode. In the test mode, data is written into and read from eight sections of the array in parallel. Data is compared upon reading and if all bits are equal, the data out pin will go high. If any one bit is different, the data out pin will go low. Any combination of read, write, read-write, or page-mode can be used in the test mode. The test mode function reduces test times by enabling the 4 meg DRAM to be tested as if it were a 512K DRAM, where row address 10, column address 10, and also column address 0 are not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 20/26 pin SOJ package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS44100-60		TMS44100-70		TMS44100-80		TMS44100-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	μA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	μA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		95		85		75		65	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		1		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		95		85		75		65	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60		50		40	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(D)}$	Input capacitance, data input			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS44100-60		TMS44100-70		TMS44100-80		TMS44100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	0	25	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS44100-60		TMS44100-70		TMS44100-80		TMS44100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		180		ns
t_{RWC}	Read-write cycle time	130		153		175		210		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		55		ns
t_{PRWC}	Page-mode read-write cycle time	60		68		75		85		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTS}	$\overline{W}$-low setup time (test mode only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 13)	50		55		60		75		ns
t_{DH}	Data hold time (see Note 10)	10		15		15		20		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 13)	50		55		60		75		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 12)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 12)	0		0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		75		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	30		35		40		45		ns

Continued next page.

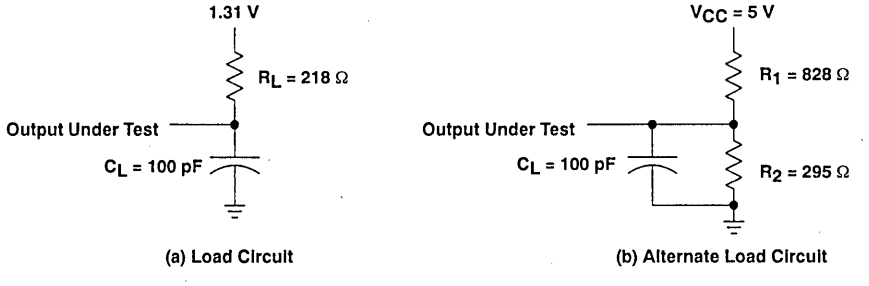
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		TMS44100-60		TMS44100-70		TMS44100-80		TMS44100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	15		18		20		25		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	30	15	35	15	40	20	50	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	52	20	60	25	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	60		70		80		100		ns
t_{TAA}	Access time from address (test mode)	35		40		45		50		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		55		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		105		ns
t_{REF}	Refresh time interval		16		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	2	50	ns

NOTE 14: The maximum value is specified only to assure access time.

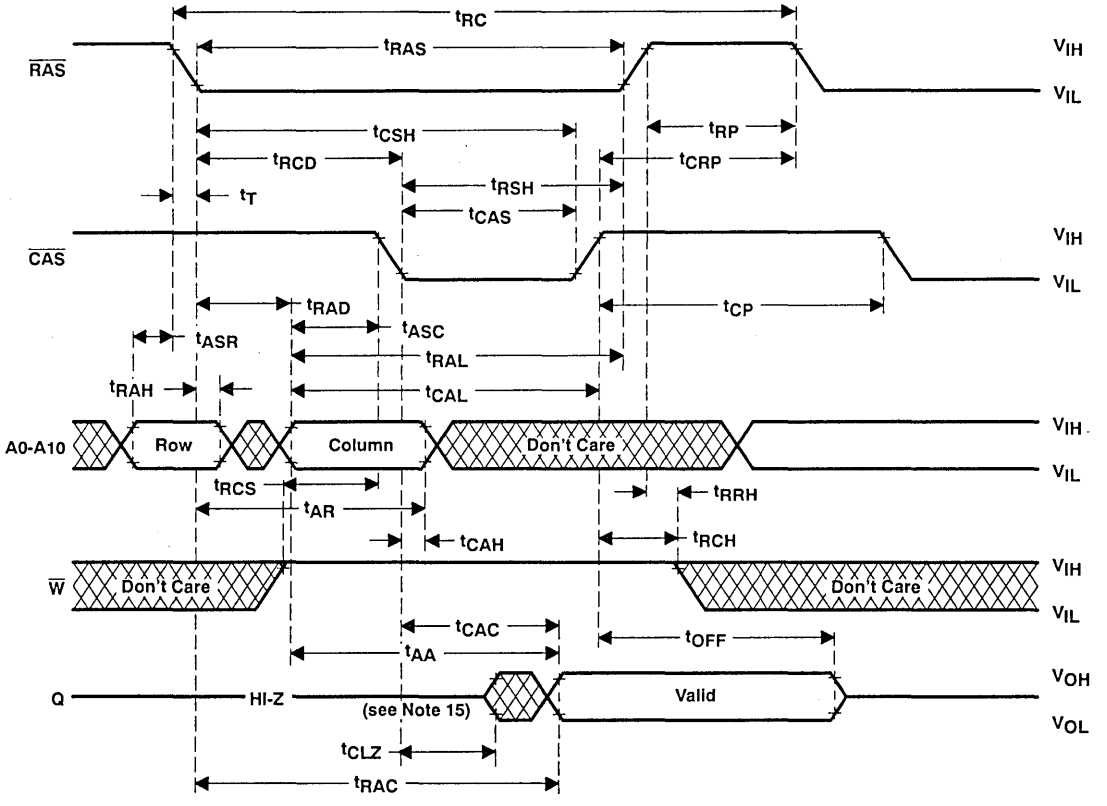
PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

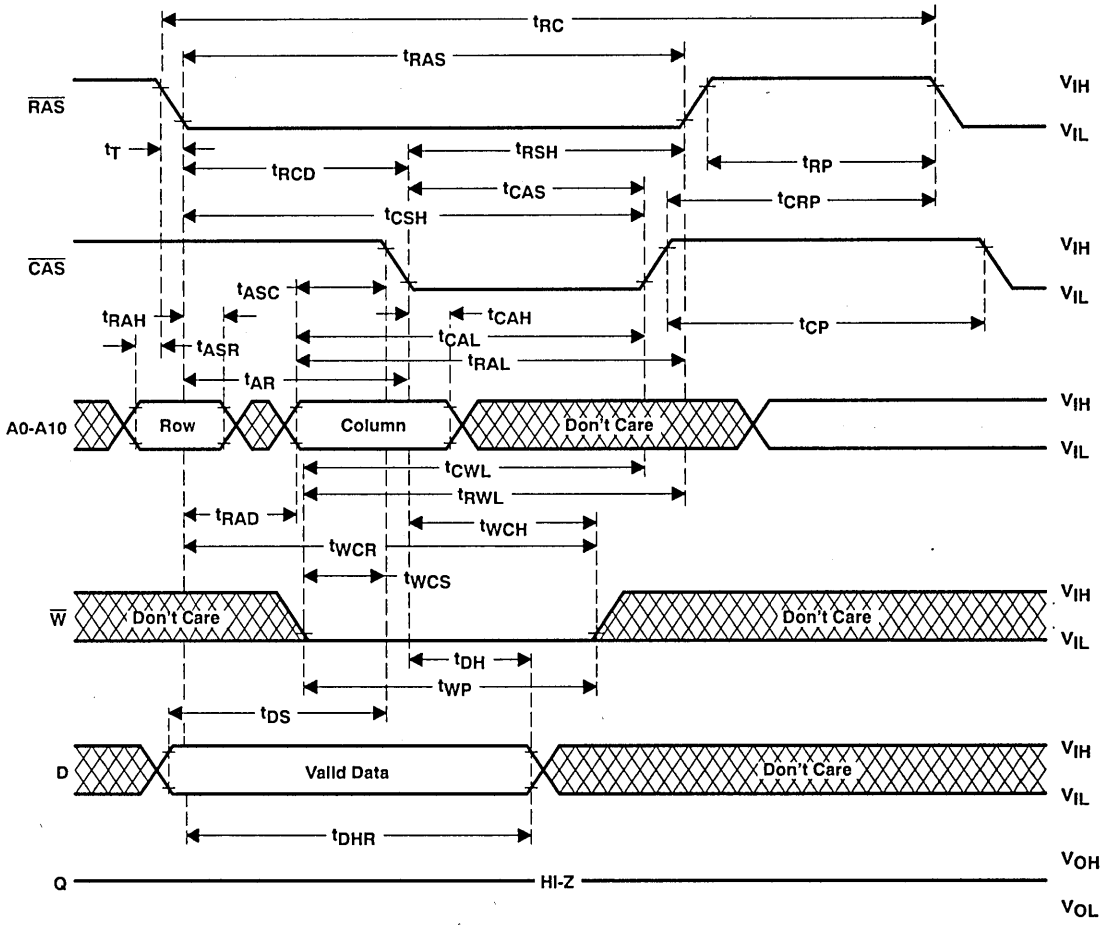
Figure 1. Load Circuits for Timing Parameters

read cycle timing

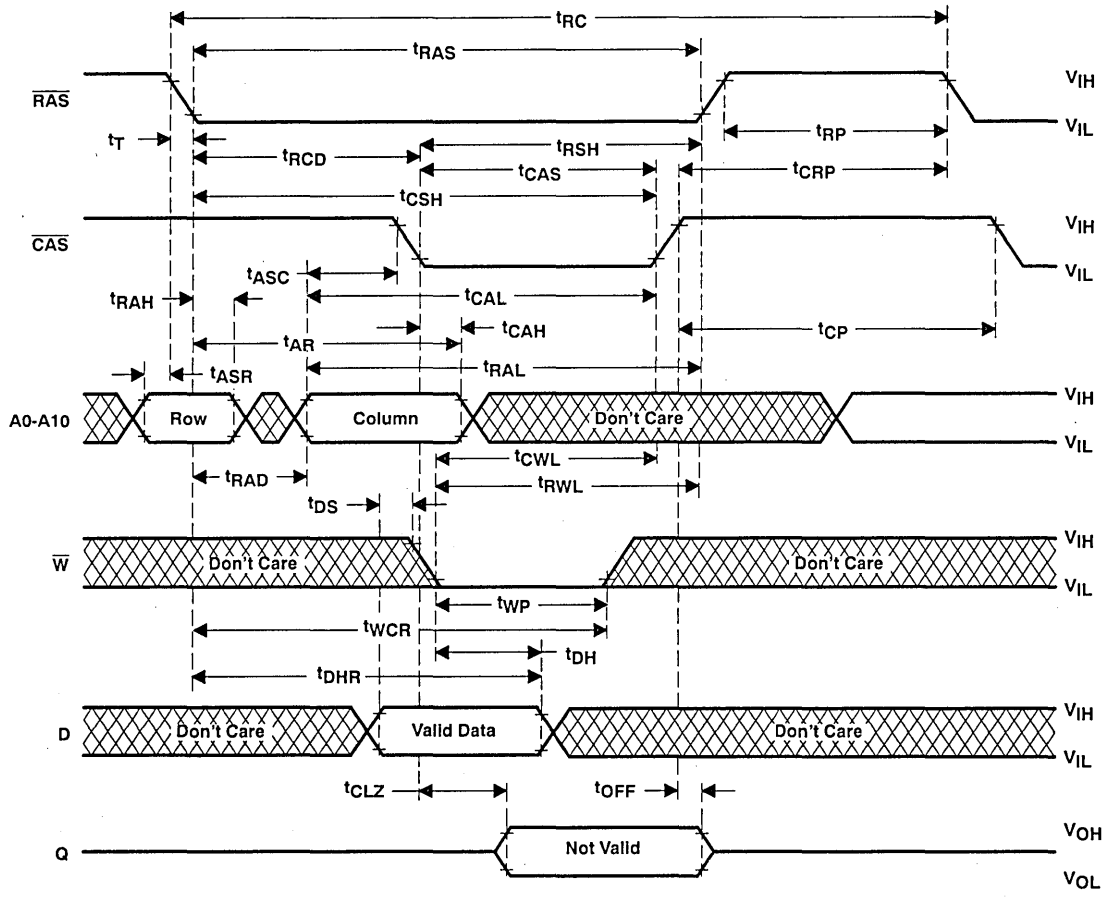


NOTE 15: Output may go from three-state to an invalid data state prior to the specified access time.

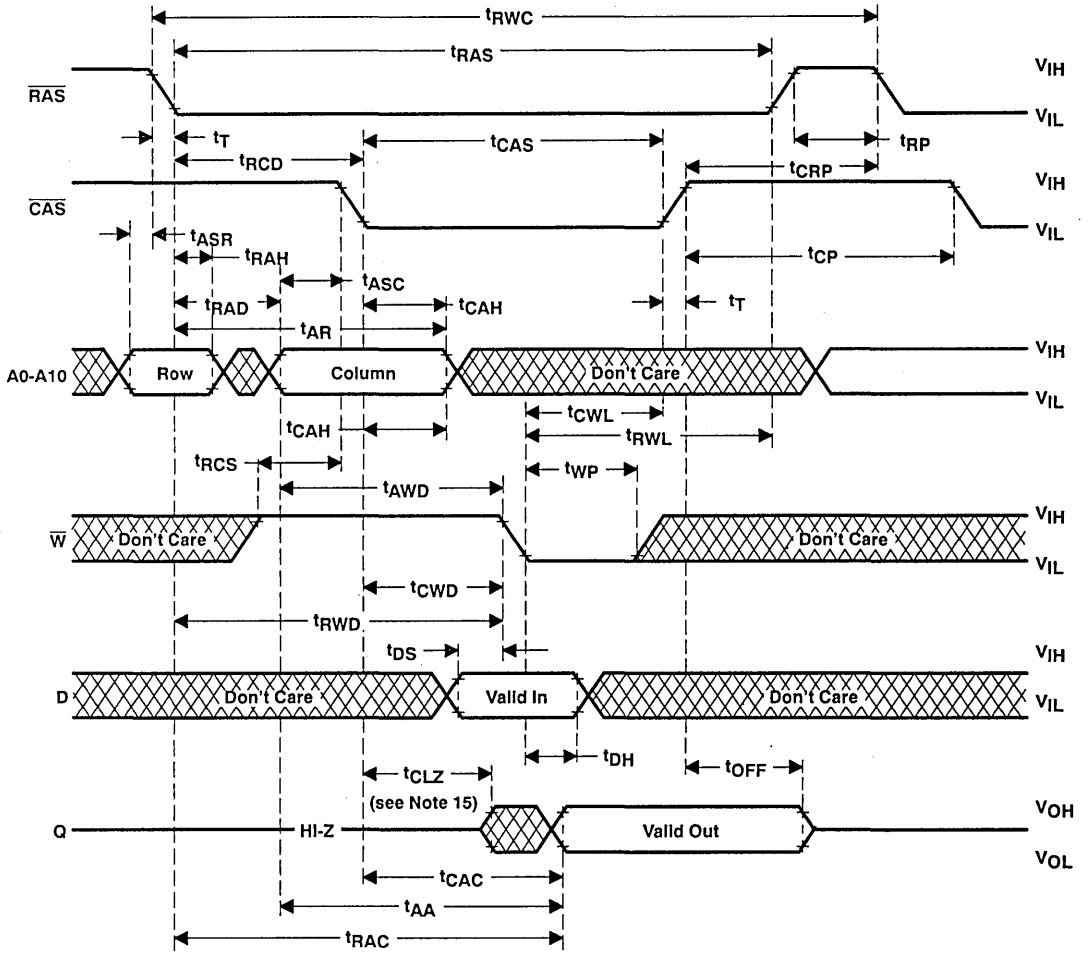
early write cycle timing



write cycle timing

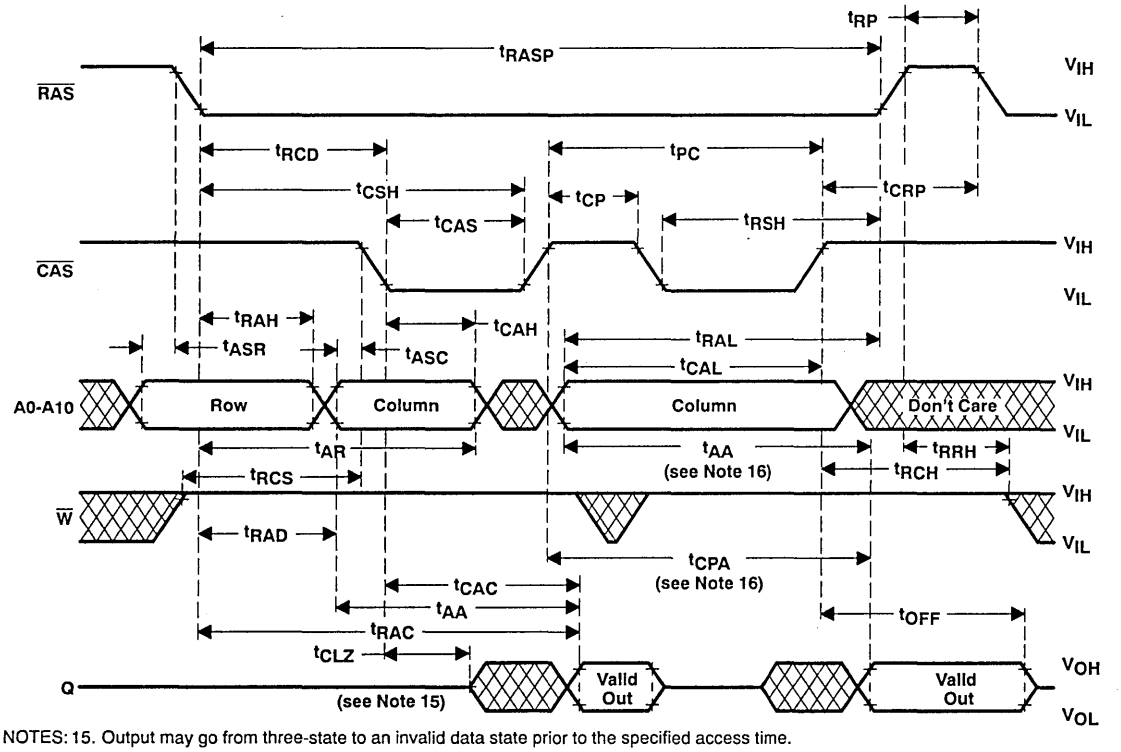


read-write cycle timing



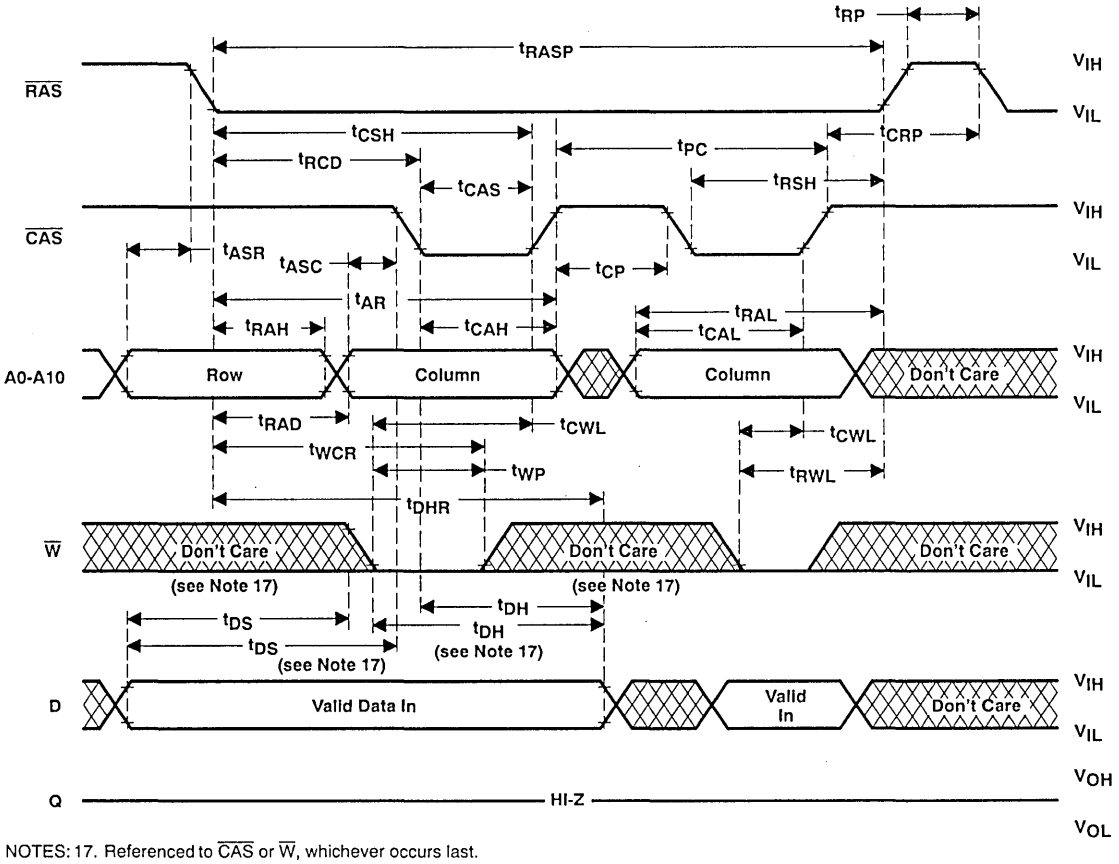
NOTE 15: Output may go from three-state to an invalid data state prior to the specified access time.

enhanced page-mode read cycle timing



NOTES: 15. Output may go from three-state to an invalid data state prior to the specified access time.
16. Access time is t_{CPA} or t_{AA} dependent.

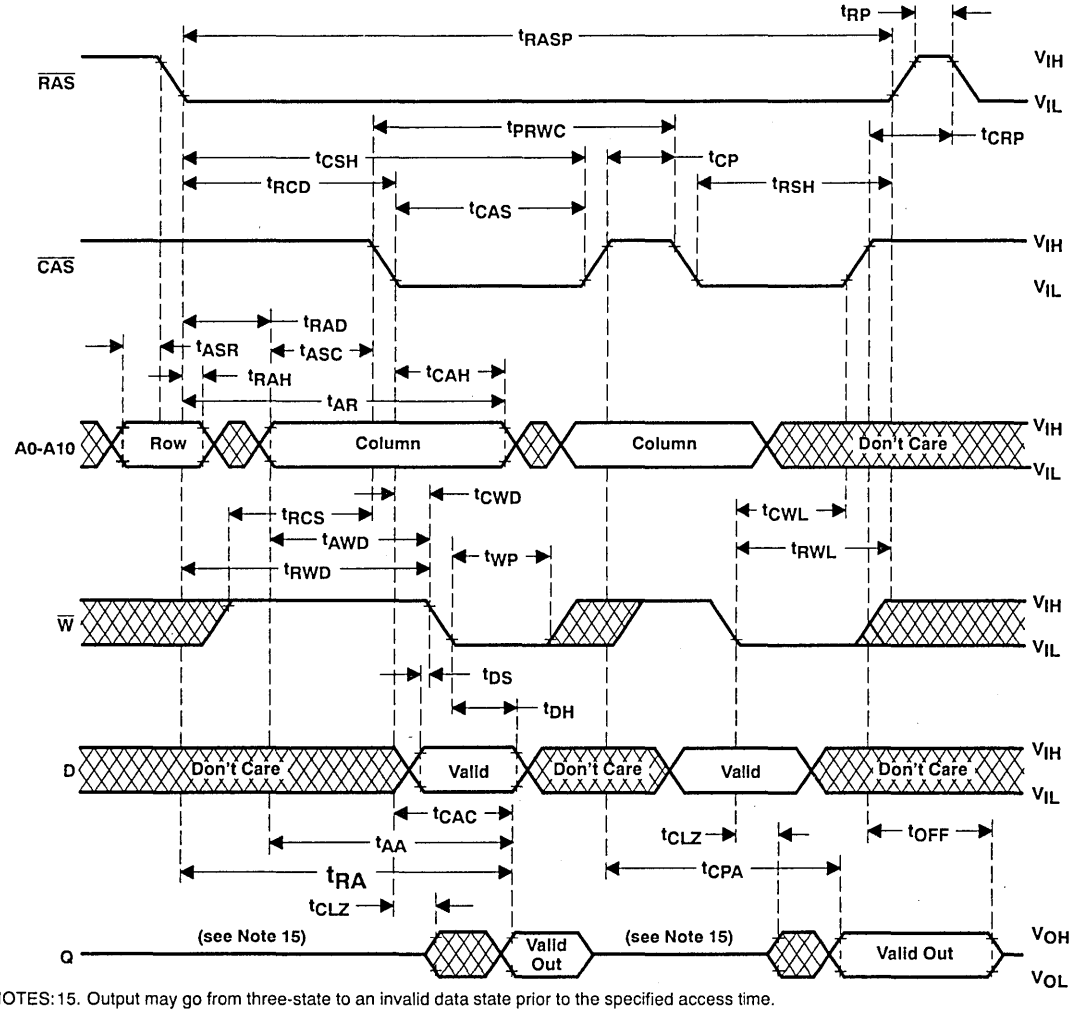
enhanced page-mode write cycle timing



NOTES: 17. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

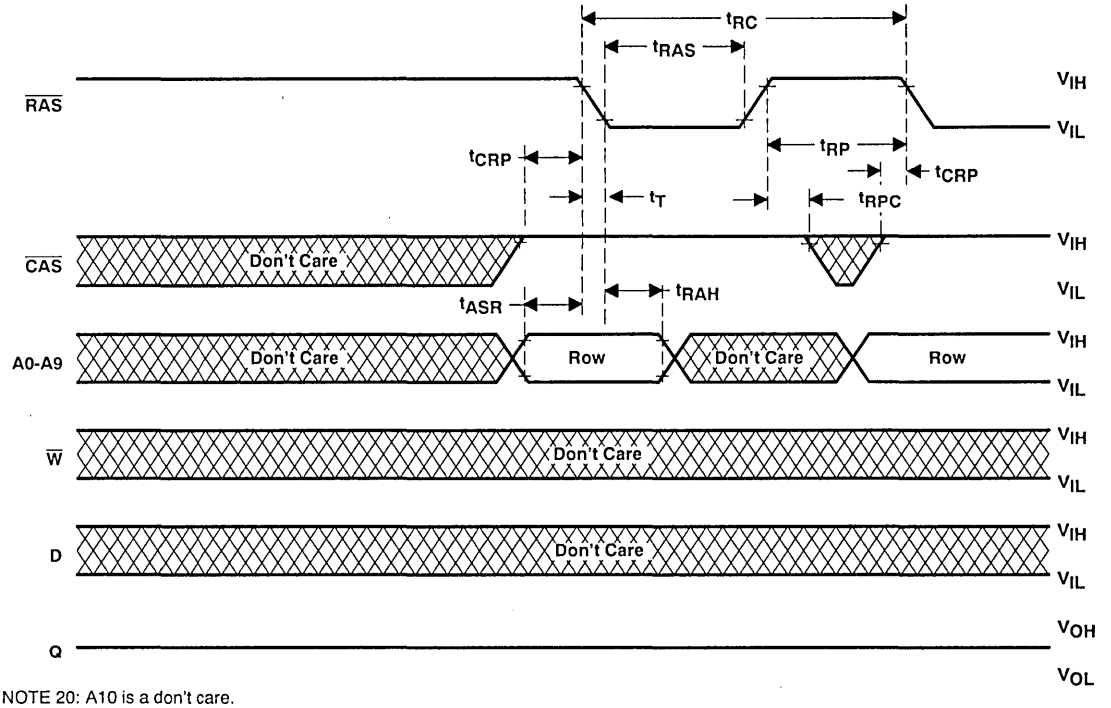
18. A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

enhanced page-mode read-write cycle timing



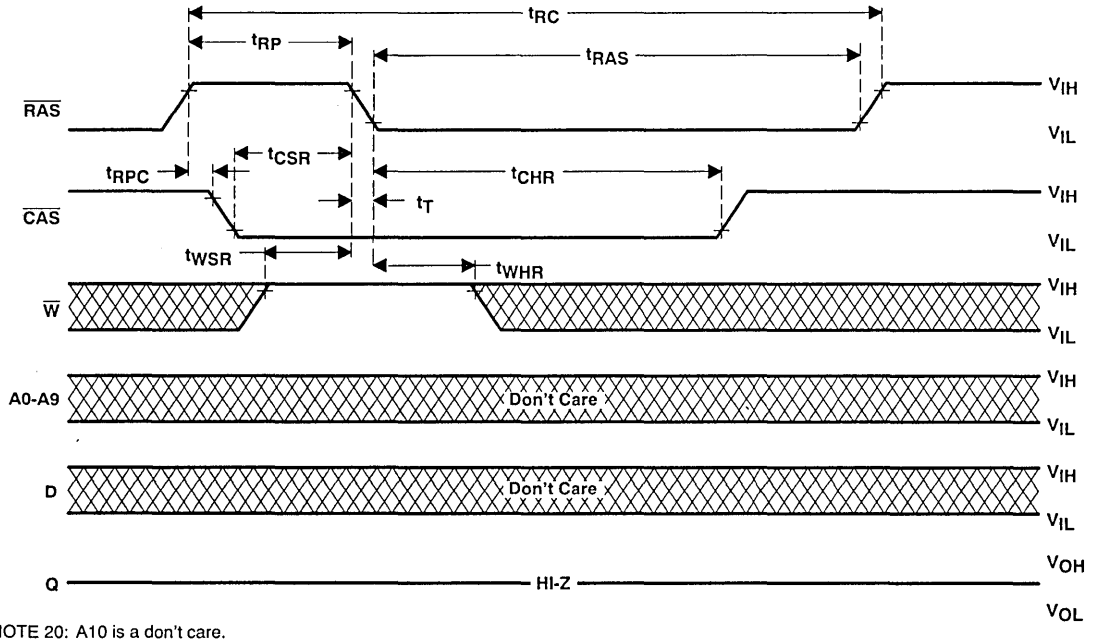
NOTES: 15. Output may go from three-state to an invalid data state prior to the specified access time.
19. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing



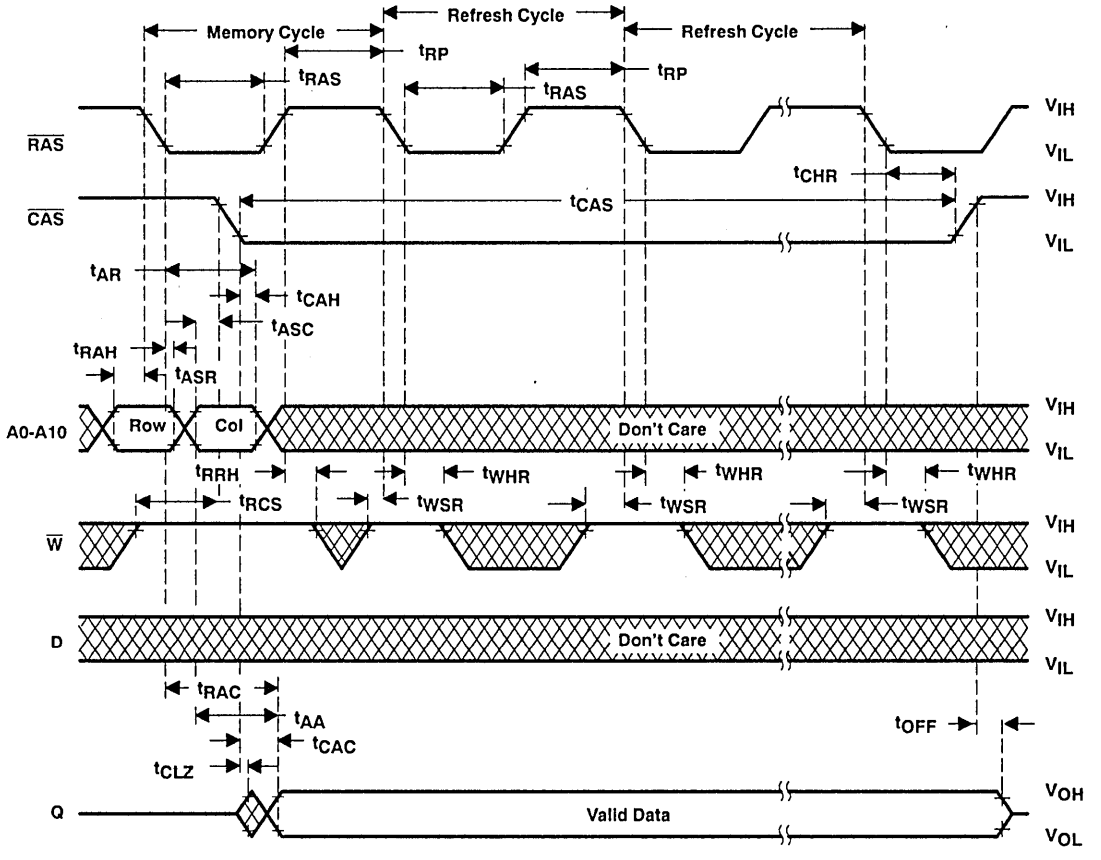
NOTE 20: A10 is a don't care.

automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



NOTE 20: A10 is a don't care.

hidden refresh cycle (read)



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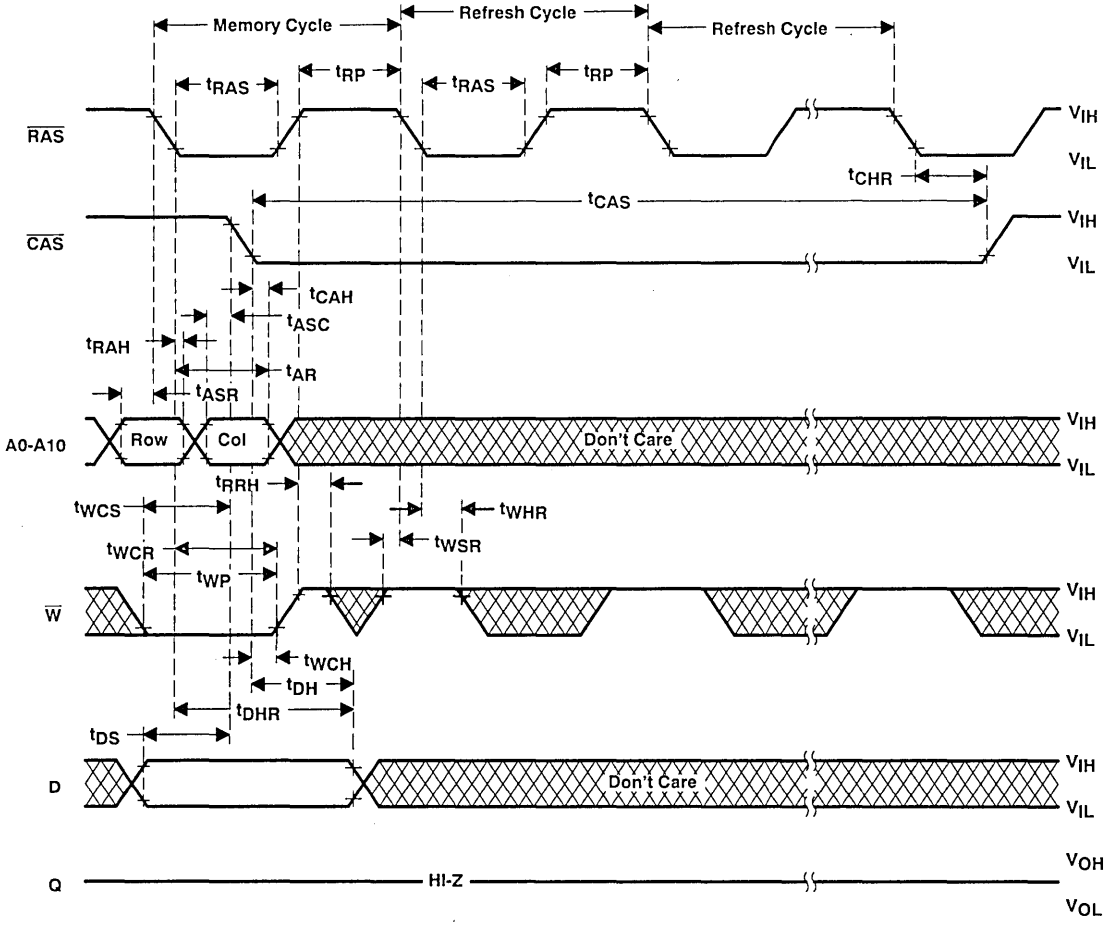
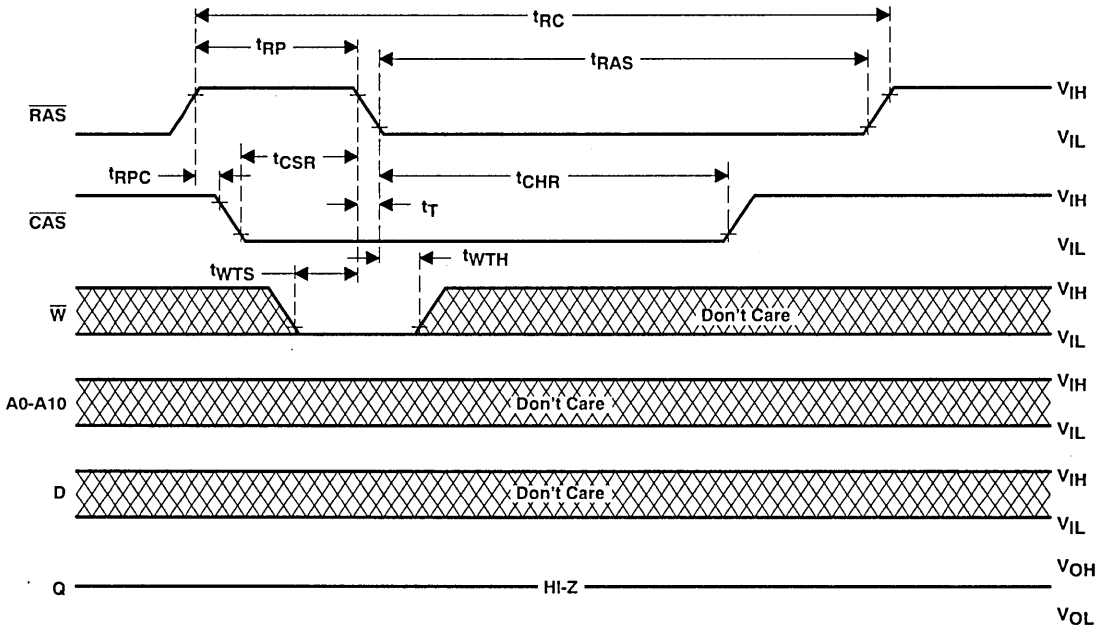
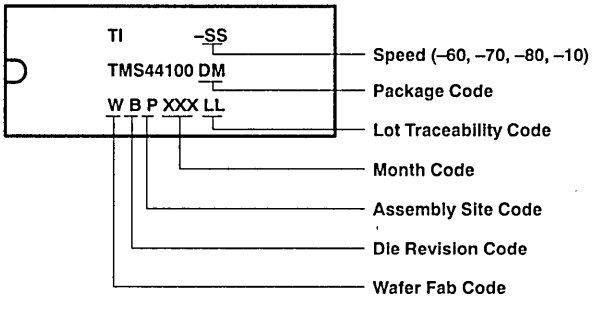
hidden refresh cycle (write)



test mode entry cycle



device symbolization



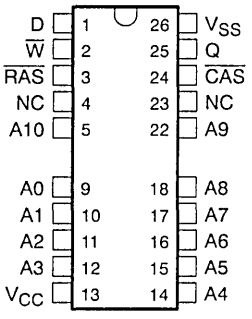
This Data Sheet is Applicable to All TMS44101s Symbolized with Revision "B" and Subsequent Revisions as Described on Page 5-124.

- **Organization . . . 4 194 304 × 1**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

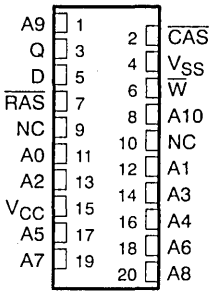
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS44101-60	60 ns	15 ns	30 ns	110 ns
TMS44101-70	70 ns	18 ns	35 ns	130 ns
TMS44101-80	80 ns	20 ns	40 ns	150 ns
TMS44101-10	100 ns	25 ns	45 ns	180 ns

- **4-Bit Nibble Mode Operation**
  - **— Four Sequential Single-Bit Access Within a Row by Toggling $\overline{CAS}$**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 1024-Cycle Refresh in 16 ms (Max)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks are TTL Compatible**

DM and DJ Packages† (Top View)



SD Package† (Top View)



†The packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0-A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

- **High-Reliability Plastic 300-mil and 350-mil 20/26-Lead Surface Mount (SOJ) Packages and a 20-Pin Zig-Zag In-line Package**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**

description

The TMS44101 series are high-speed 4 194 304-bit dynamic random-access memories, organized as 4 194 304 words of one bit each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 360 mW operating and 6 mW standby.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

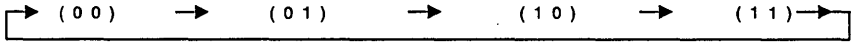
The TMS44101 is offered in a 350-mil 20/26-lead plastic surface mount SOJ package (DM suffix), a 300-mil 20/26-lead plastic surface mount SOJ package (DJ suffix), and a 20-pin plastic ZIP package (SD suffix). All packages are guaranteed for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

operation

nibble mode

Nibble-mode operation allows high-speed read, write, or read-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at t_{CAC} as long as t_{RAC} and t_{AA} are satisfied. The next sequential bits can be read or written by cycling $\overline{CAS}$ while $\overline{RAS}$ remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Row A10 and column A10 provide the two binary bits for initial selection, with row A10 being the least-significant address and column A10 being the most significant. Therefore, the falling edge of $\overline{CAS}$ will access the next bit of the circular 4-bit nibble in the following sequence



Data written in a sequence of more than 4 consecutive cycles shall be capable of being read back without exiting from the nibble mode. In a sequence of consecutive nibble-mode cycles the control of the high-impedance state for the data out (Q) pin is determined by each individual cycle. This facilitates fully mixed nibble-mode cycles (e.g., read/write/read-write, etc.)

address (A0 through A10)

Twenty address bits are required to decode 1 of 4 194 304 storage cell locations. Eleven row-address bits are set up on inputs A0 through A10 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The eleven column-address bits are set up on pins A0 through A10 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{AA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every sixteen milliseconds to retain data. This can be achieved by strobing each of the1024 rows (A0-A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter t_{CSR}] and holding it low after $\overline{RAS}$ falls [see parameter t_{CHR}]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

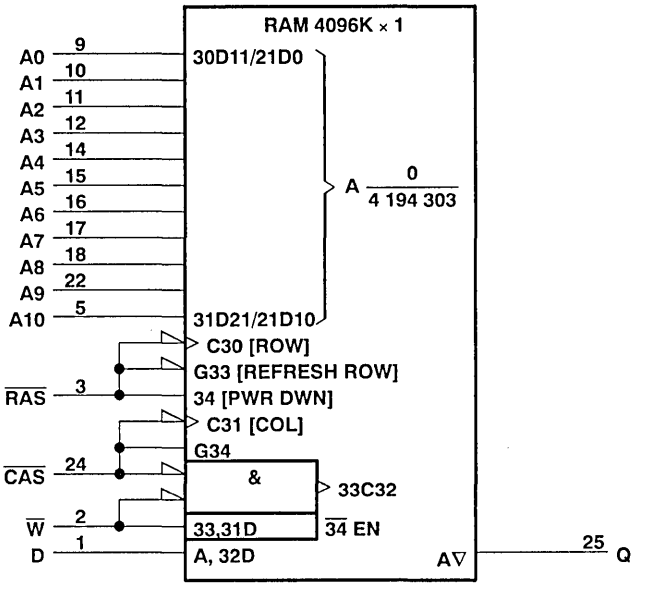
power-up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

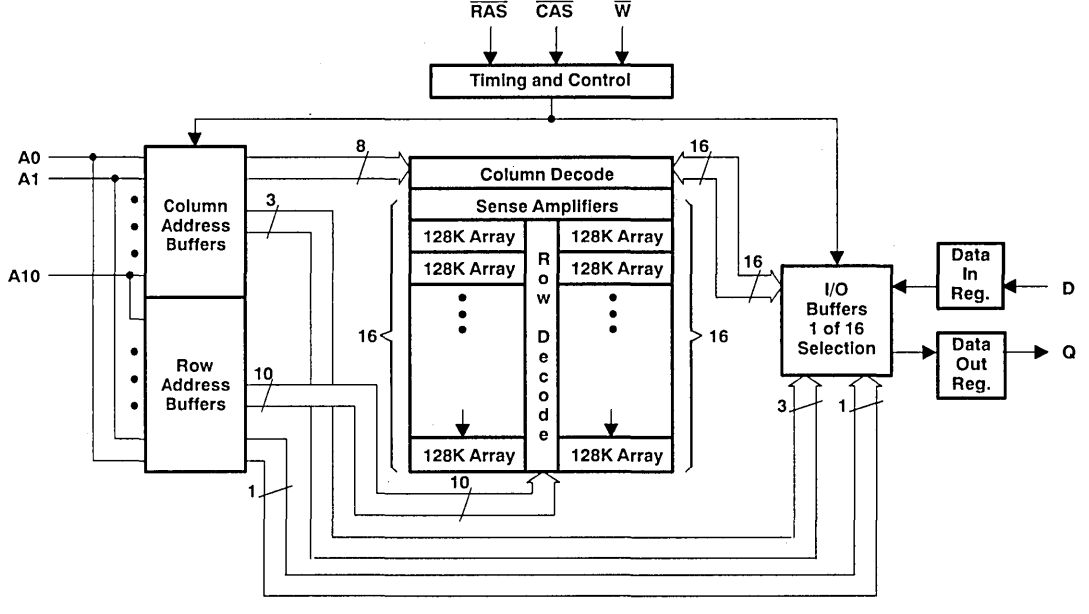
An industry standard Design For Test (DFT) mode is incorporated in the TMS44101. A $\overline{CAS}$-before-$\overline{RAS}$ cycle with $\overline{W}$ low (WCBR) cycle is used to enter the test mode. In the test mode, data is written into and read from eight sections of the array in parallel. Data is compared upon reading and if all bits are equal, the data out pin will go high. If any one bit is different, the data out pin will go low. Any combination read, write, read-write, or page-mode can be used in the test mode. The test mode function reduces test times by enabling the 4 meg DRAM to be tested as if it were a 512K DRAM, where row address 10, column address 10, and also column address 0 are not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 20/26 pin SOJ package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS44101-60		TMS44101-70		TMS44101-80		TMS44101-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)‡	V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)‡	V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		95		85		75		65	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V		1		1		1		1	
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)‡	$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		95		85		75		65	mA
I_{CC5}	Average nibble mode current‡	$\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60		50		40	mA

‡ Minimum cycle, V_{CC} = 5.5 V.

NOTE 3: Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 4)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(D)}$	Input capacitance, data input			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 4: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS44101-60		TMS44101-70		TMS44101-80		TMS44101-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{NCAC}	Access time from $\overline{CAS}$ low (nibble operation)		15		18		20		25	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 5)	0	15	0	18	0	20	0	25	ns

NOTE 5: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS44101-60		TMS44101-70		TMS44101-80		TMS44101-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 6)	110		130		150		180		ns
t_{RWC}	Read-write cycle time	130		153		175		210		ns
t_{NC}	Nibble-mode read or write cycle time	35		38		40		45		ns
t_{NRWC}	Nibble-mode read-write cycle time	55		61		65		75		ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low (see Note 7)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 8)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 9)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTS}	$\overline{W}$-low setup time (test mode only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		20		ns

Continued next page.

NOTES: 6. All cycle times assume t_T = 5 ns.
7. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
8. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
9. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		TMS44101-60		TMS44101-70		TMS44101-80		TMS44101-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{DHR}	Data hold time after $\overline{RAS}$ low	50		55		60		75		ns
t_{DH}	Data hold time (see Note 9)	10		15		15		20		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low	50		55		60		75		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 10)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 10)	0		0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low	50		55		60		75		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$-low (Read-write operation only)	30		35		40		45		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$-low (Read-write operation only)	15		18		20		25		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 11)	15	30	15	35	15	40	20	50	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 11)	20	45	20	52	20	60	25	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$-low (Read-write operation only)	60		70		80		100		ns
t_{TAA}	Access time from address (test mode)	35		40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		105		ns
t_{REF}	Refresh time interval		16		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	2	50	ns

NOTES: 9. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. The maximum value is specified only to guarantee access time.

PARAMETER MEASUREMENT INFORMATION

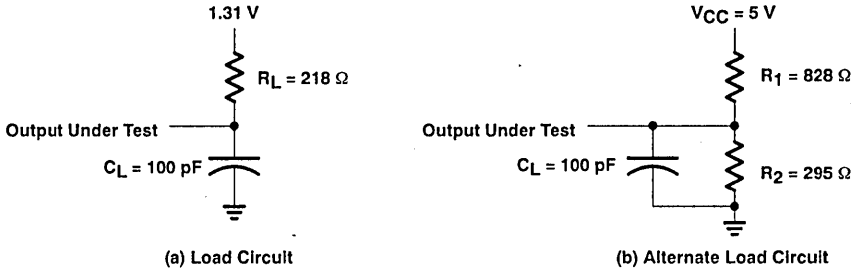
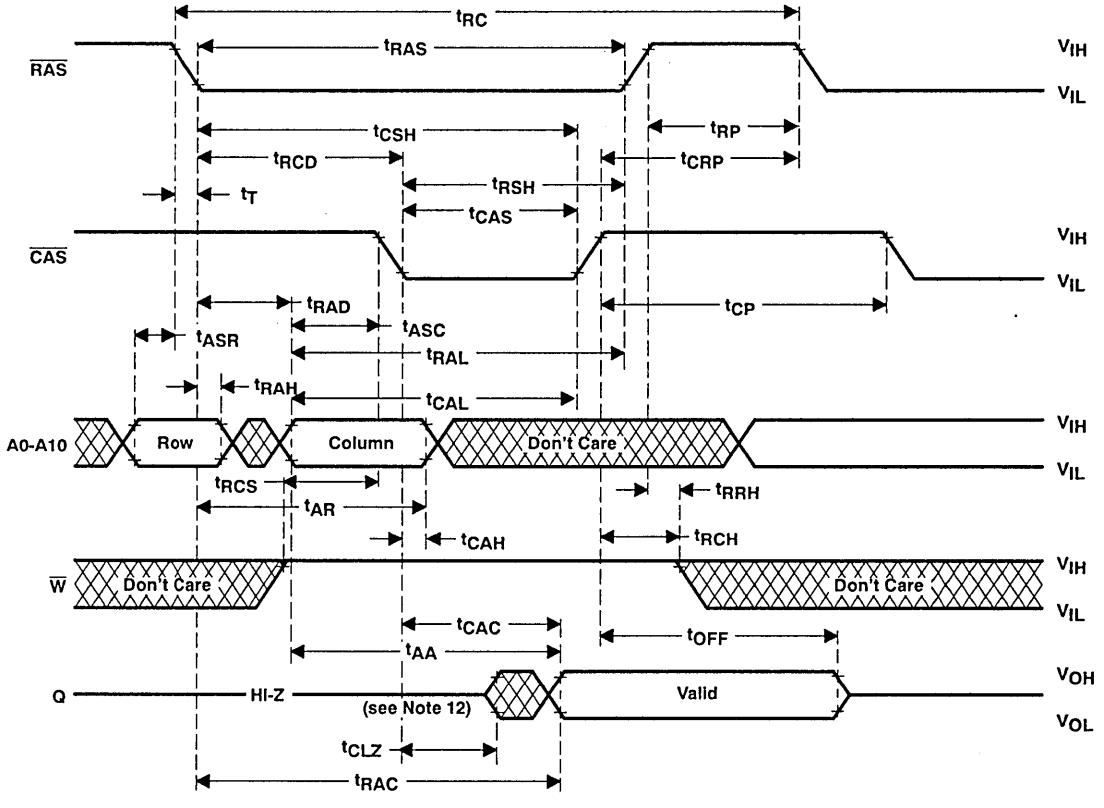


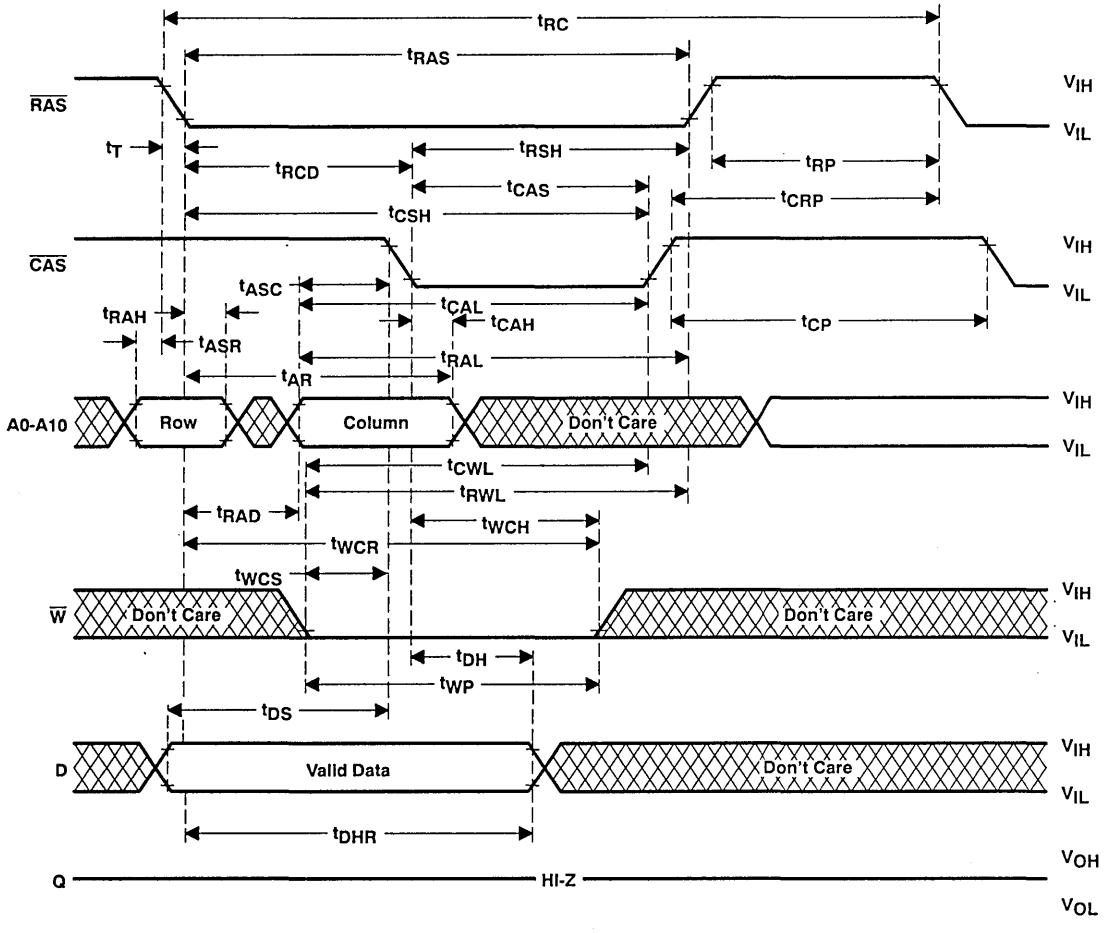
Figure 1. Load Circuits for Timing Parameters

read cycle timing

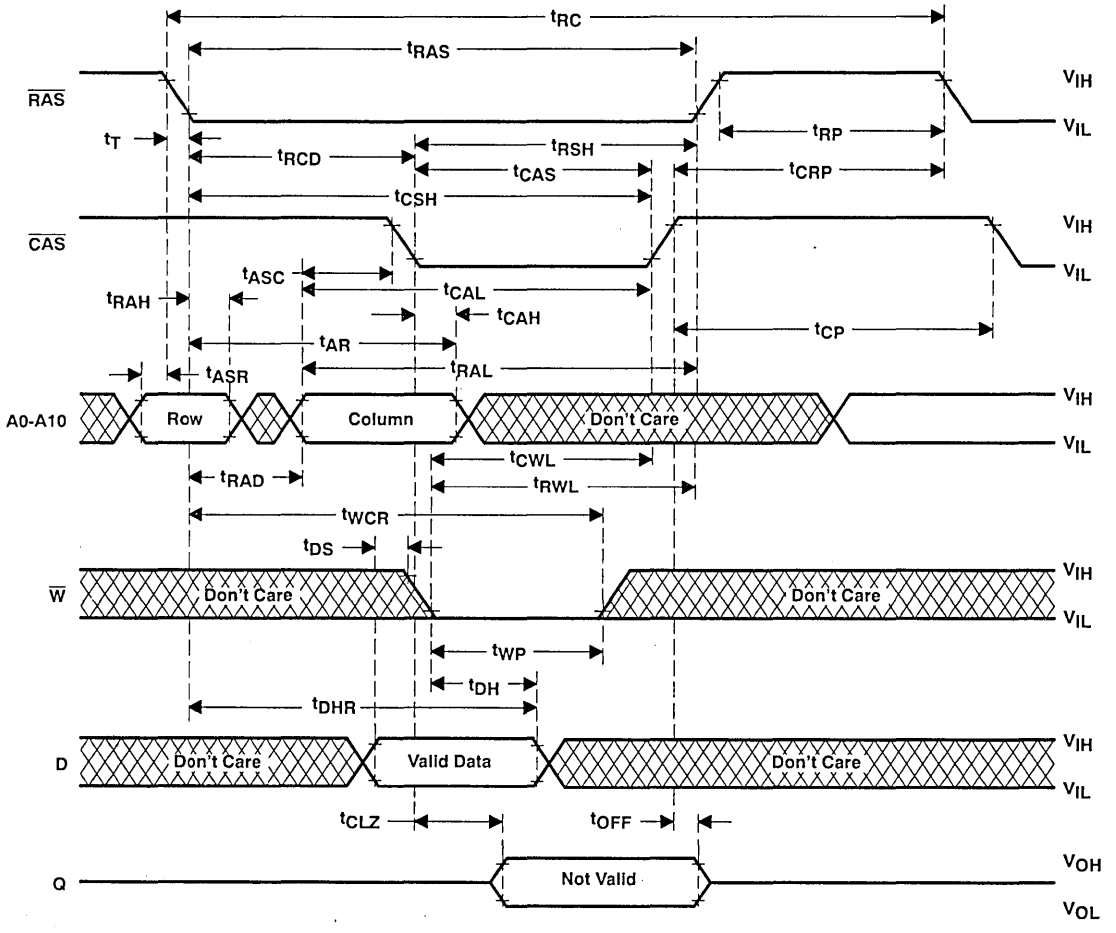


NOTE 12: Output may go from three-state to an invalid data state prior to the specified access time.

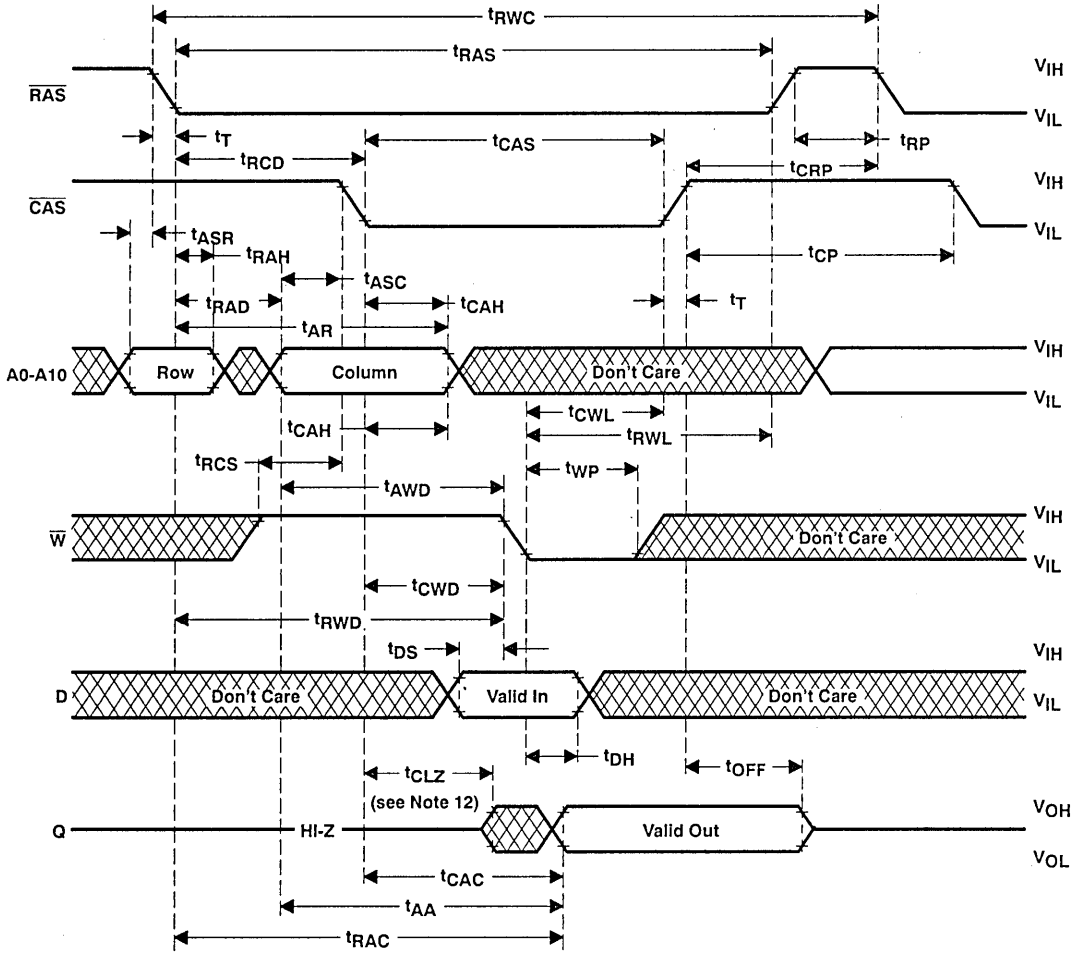
early write cycle timing



write cycle timing

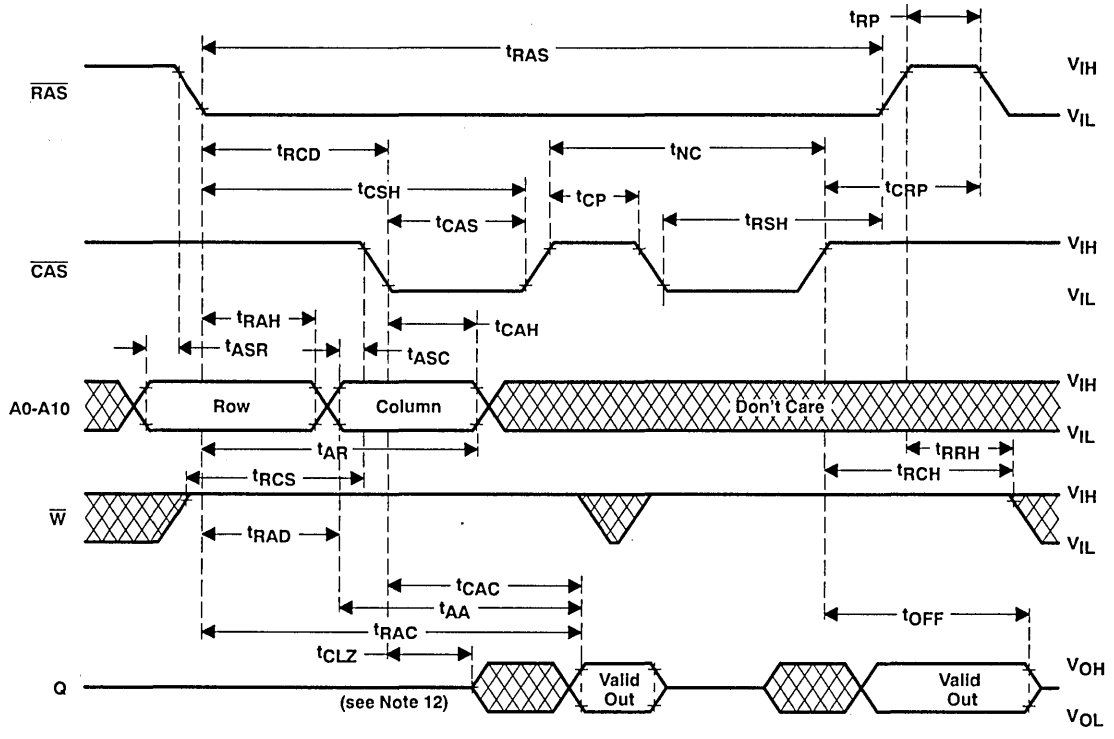


read-write cycle timing



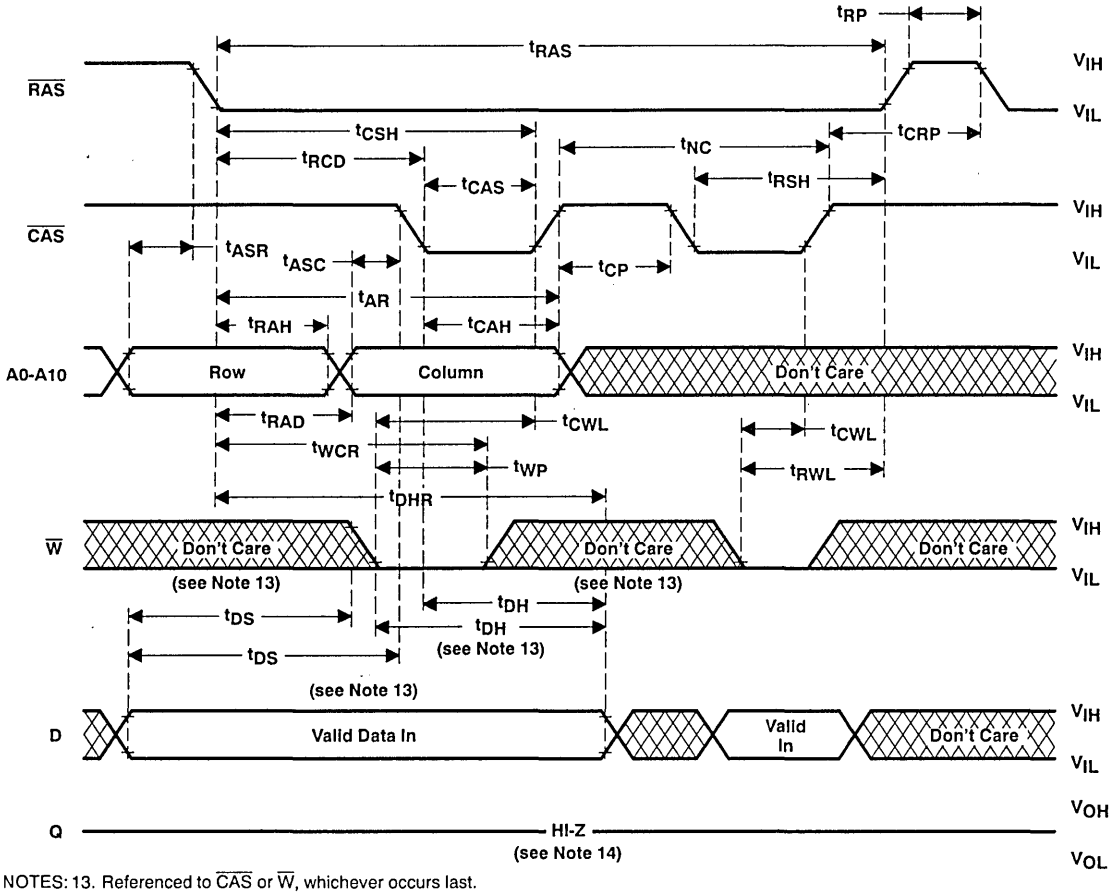
NOTE 12: Output may go from three-state to an invalid data state prior to the specified access time.

nibble-mode read cycle timing



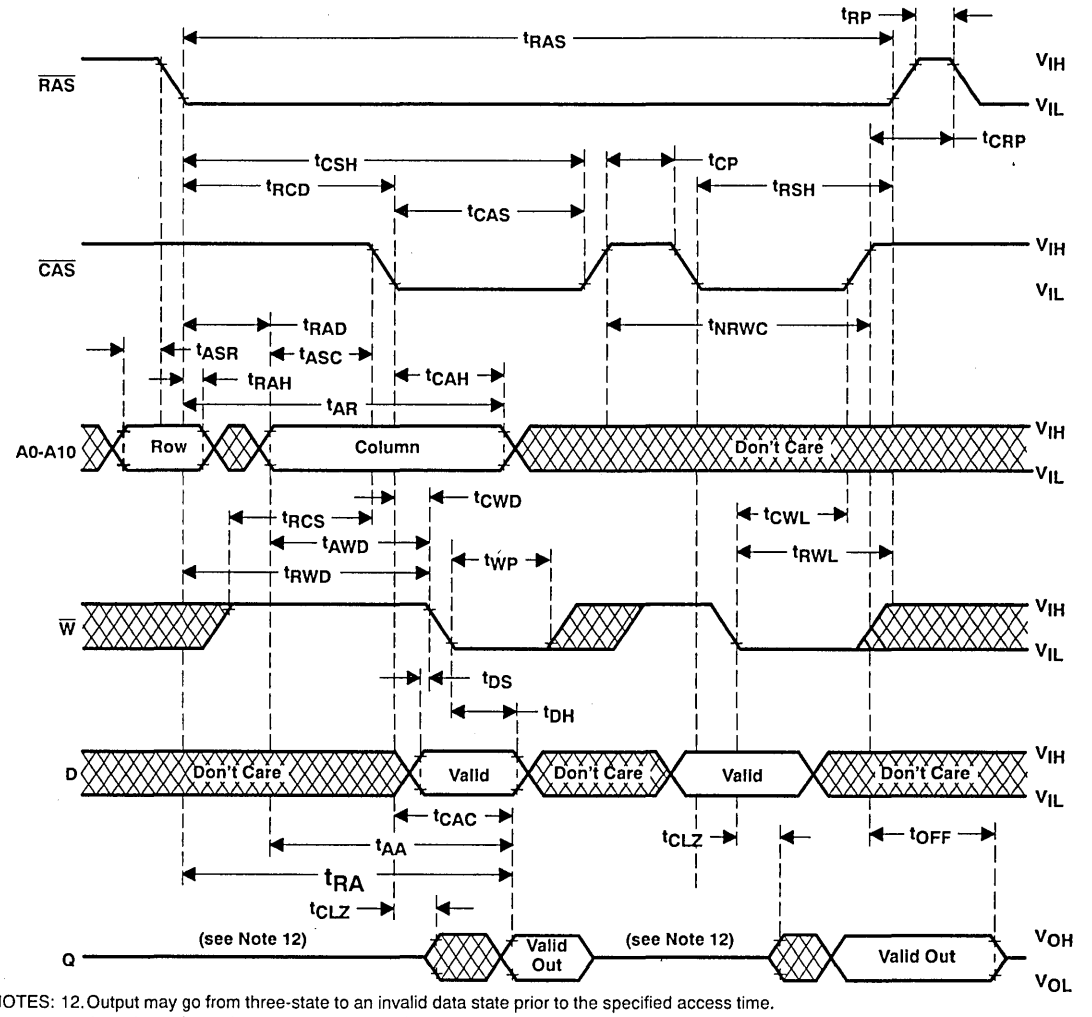
NOTE 12: Output may go from three-state to an invalid data state prior to the specified access time.

nibble-mode write cycle timing



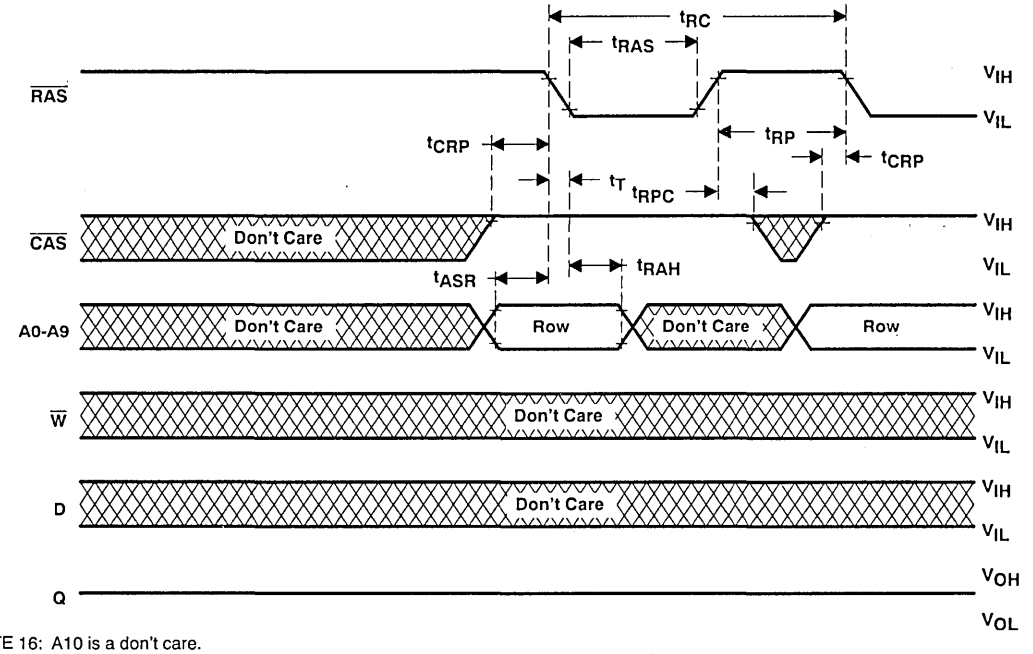
NOTES: 13. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
14. The output may go to an invalid state if a late write is completed.

nibble-mode read-write cycle timing



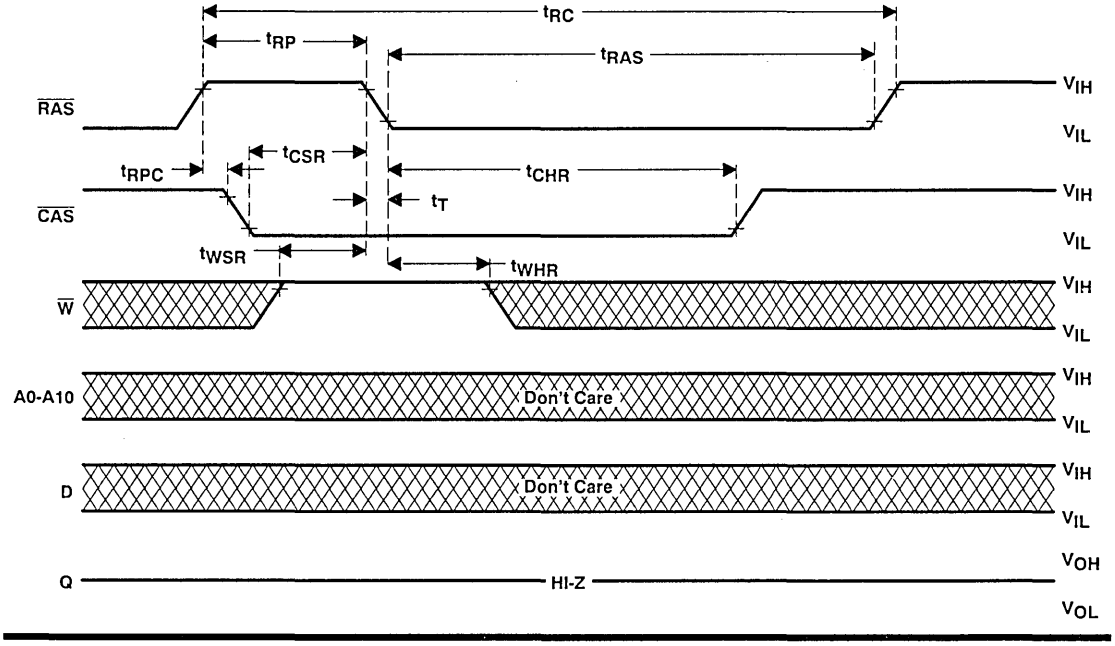
NOTES: 12. Output may go from three-state to an invalid data state prior to the specified access time.
15. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

RAS-only refresh timing

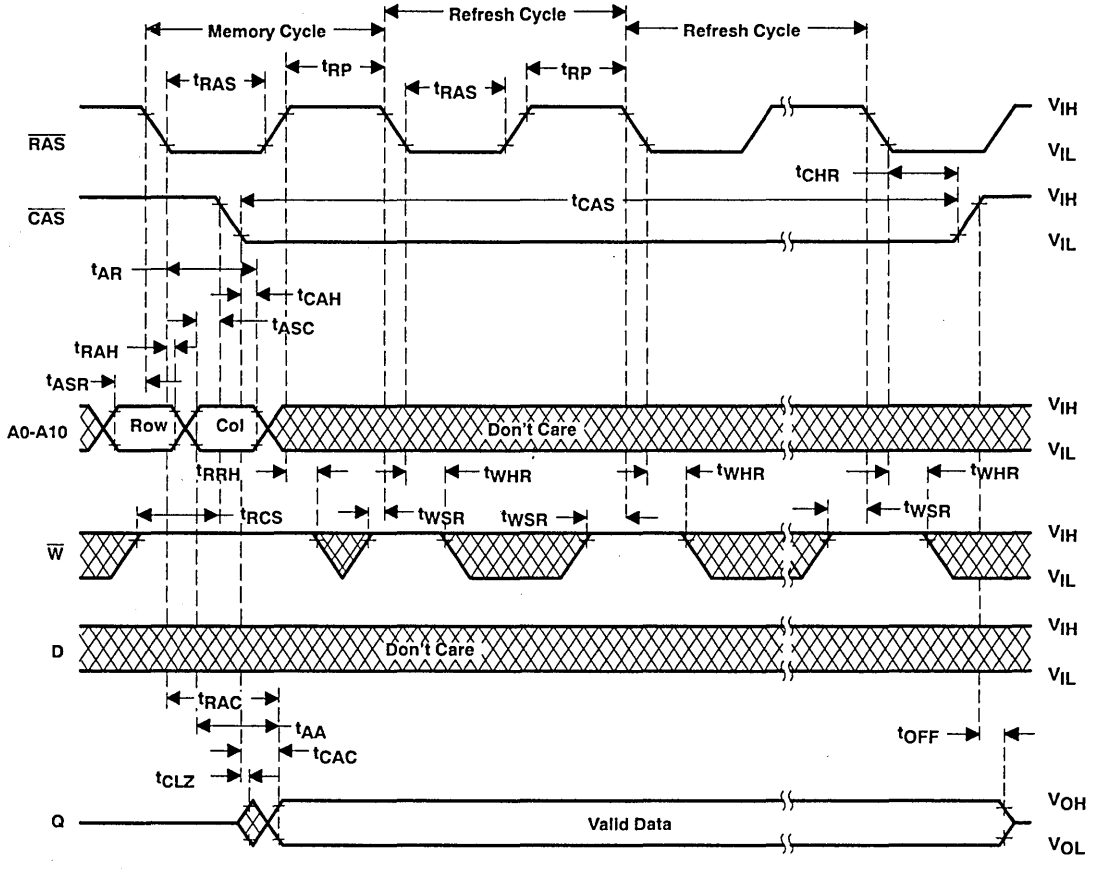


NOTE 16: A10 is a don't care.

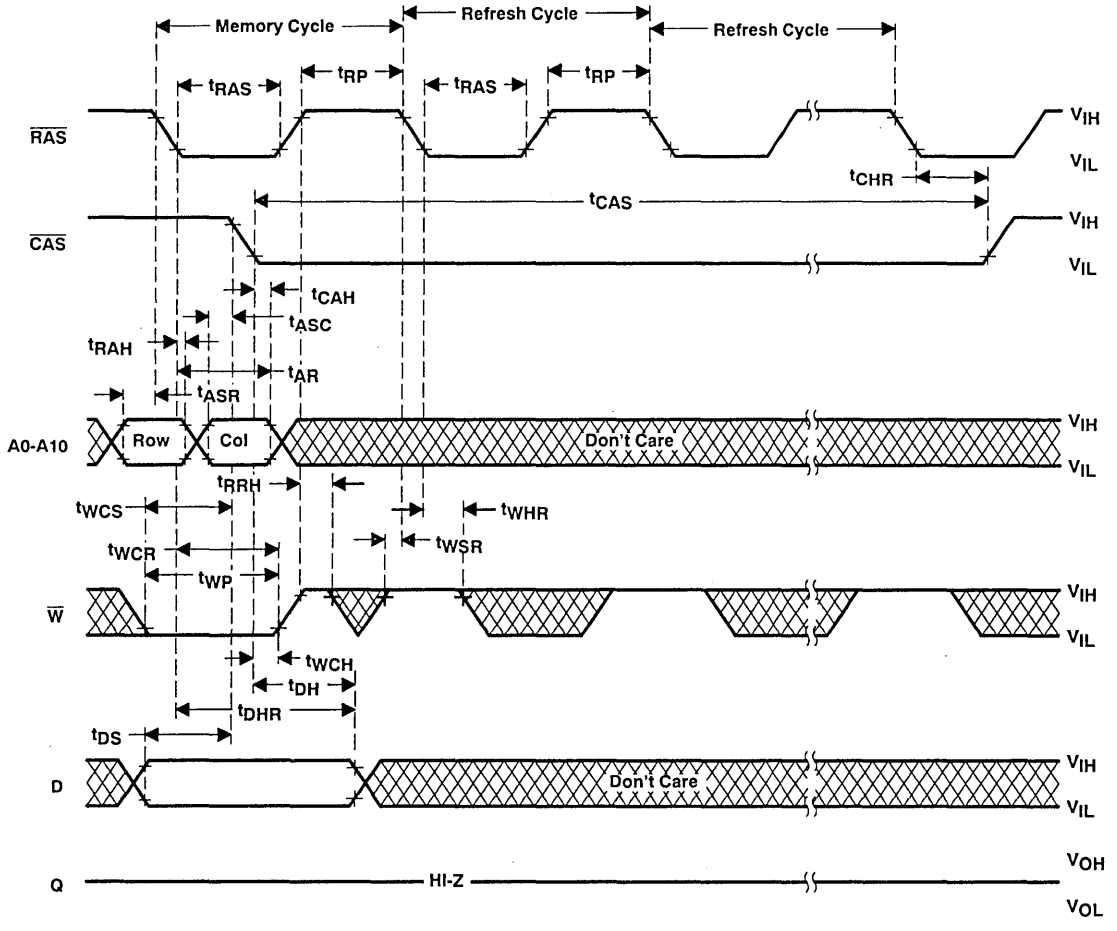
automatic (CAS-before-RAS) refresh cycle timing



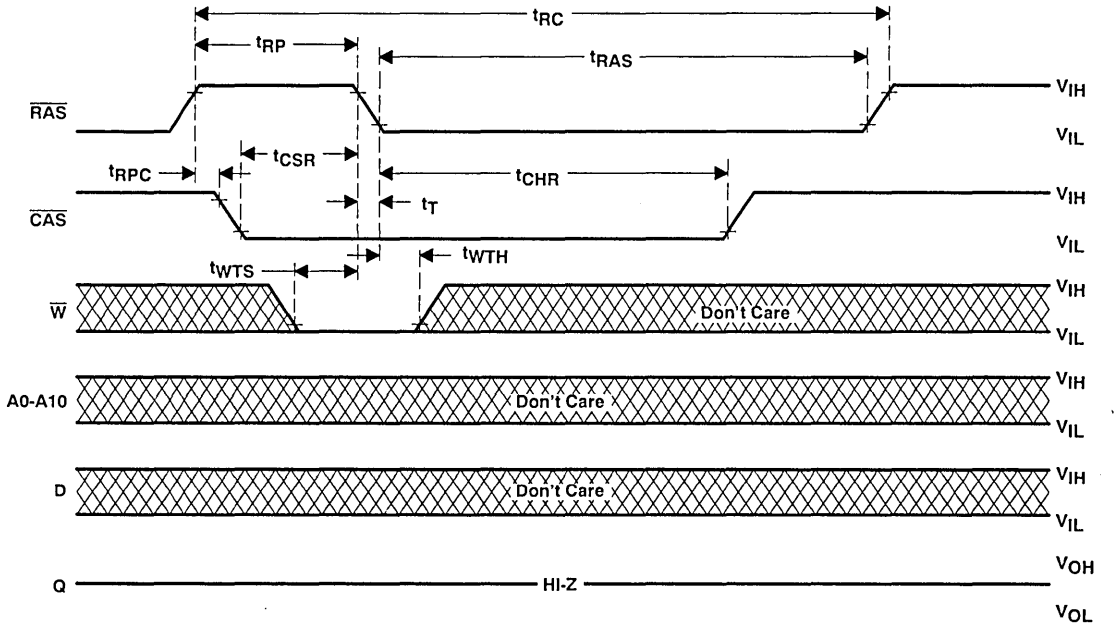
hidden refresh cycle (read)



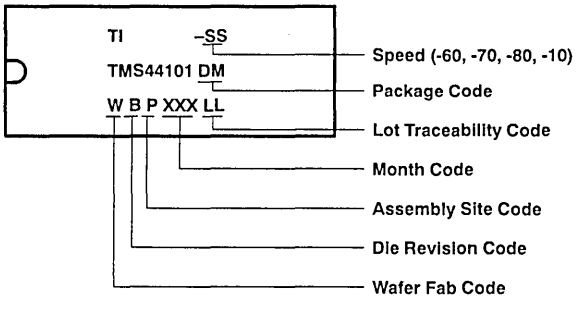
hidden refresh cycle (write)



test mode entry cycle



device symbolization



REV A — SMHS440B — OCTOBER 1989 — REVISED JANUARY 1991

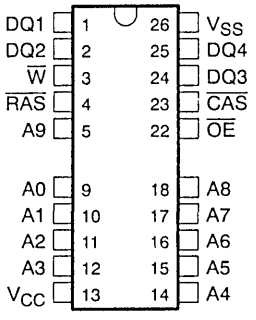
This Data Sheet Is Applicable to All TMS44400s Symbolized With Revision "B" and Subsequent Revisions as Described on Page 5-144.

- **Organization . . . 1 048 576 × 4**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

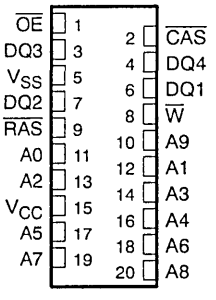
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS44400-60	60 ns	15 ns	30 ns	155 ns
TMS44400-70	70 ns	18 ns	35 ns	181 ns
TMS44400-80	80 ns	20 ns	40 ns	205 ns
TMS44400-10	100 ns	25 ns	50 ns	245 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
  - **— Higher Data Bandwidth than Conventional Page-Mode Parts**
  - **— Random Single-Bit Access Within a Row With a Column Address**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 1024-Cycle Refresh in 16 ms (Max)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **High-Reliability Plastic 300-Mil and 350-Mil 20/26-Lead Surface Mount (SOJ) Packages and 20-Pin Zig-Zag In line (ZIP) Package**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**

DM AND DJ Packages†
(Top View)



SD Package†
(Top View)



†The packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS44400 series are high-speed 4 194 304-bit dynamic random-access memories, organized as 1 048 576 words of four bits each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 360 mW operating and 6 mW standby.

EPIC is a trademark of Texas Instruments Incorporated.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS44400 is offered in a 300-mil 20/26-lead plastic surface mount SOJ package (DJ), a 350-mil 20/26-lead plastic surface mount SOJ package (DM) and a 20-pin zig-zag in-line package (SD suffix). All packages are characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS44400 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0 through A9)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data in/out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OED}.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every sixteen milliseconds to retain data. This can be achieved by strobing each of the1024 rows (A0-A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter t_{CSR}] and holding it low after $\overline{RAS}$ falls [see parameter t_{CHR}]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

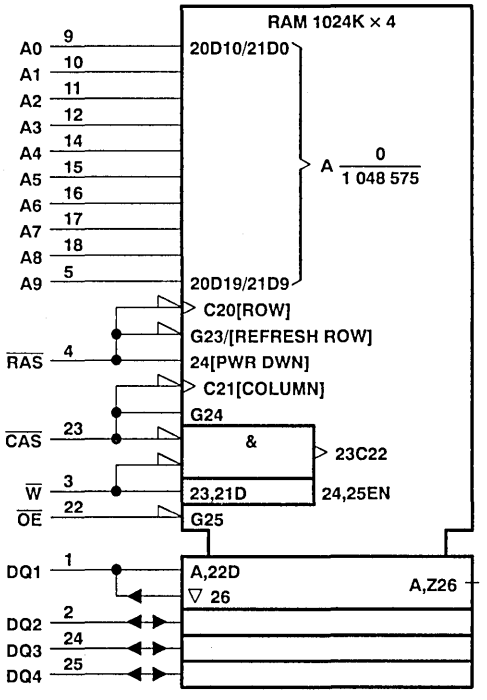
power-up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

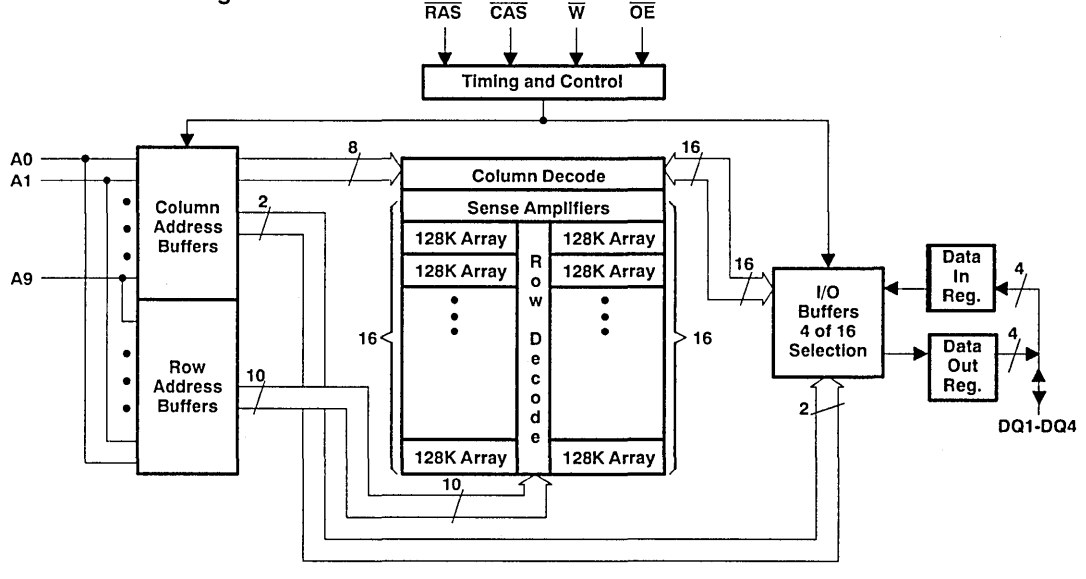
A Design For Test (DFT) mode is incorporated in the TMS44400. A $\overline{CAS}$-before-$\overline{RAS}$ with $\overline{W}$ low (WCBR) cycle is used to enter test mode. In the test mode, data is written into and read from eight sections of the array in parallel. All data is written into the array through DQ1. Data is compared upon reading and if all bits are equal, all DQ pins will go high. If any one bit is different, a DQ pin will go low. Any combination of read, write, read-write, or page-mode can be used in the test mode. The test mode function reduces test times by enabling the 1 meg × 4 DRAM to be tested as if it were a 512K DRAM where column address 0 is not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 20/26 pin SOJ packages.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS44400-60		TMS44400-70		TMS44400-80		TMS44400-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 to V_{CC}		± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		95		85		75		65	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		1		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		95		85		75		65	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60		50		40	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS44400-60		TMS44400-70		TMS44400-80		TMS44400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20		25	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)	0	15	0	18	0	20	0	25	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS44400-60		TMS44400-70		TMS44400-80		TMS44400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		180		ns
t_{RWC}	Read-write cycle time	155		181		205		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		55		ns
t_{PRWC}	Page-mode read-write cycle time	85		96		105		120		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTS}	$\overline{W}$-low setup time (test mode only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		75		ns
t_{DH}	Data hold time (see Note 11)	10		15		15		20		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		75		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	0		0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		75		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	55		63		70		80		ns

Continued next page.

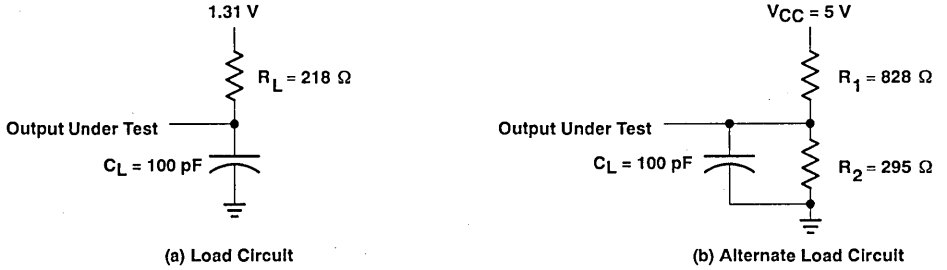
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		TMS44400-60		TMS44400-70		TMS44400-80		TMS44400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	40		46		50		60		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		25		ns
t_{OED}	$\overline{OE}$ to data delay	15		18		20		25		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	30	15	35	15	40	20	50	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	52	20	60	25	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	85		98		110		135		ns
t_{TAA}	Access time from address (test mode)	35		40		45		50		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		55		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		105		ns
t_{REF}	Refresh time interval		16		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	2	50	ns

NOTE 14: The maximum value is specified only to guarantee access time.

PARAMETER MEASUREMENT INFORMATION

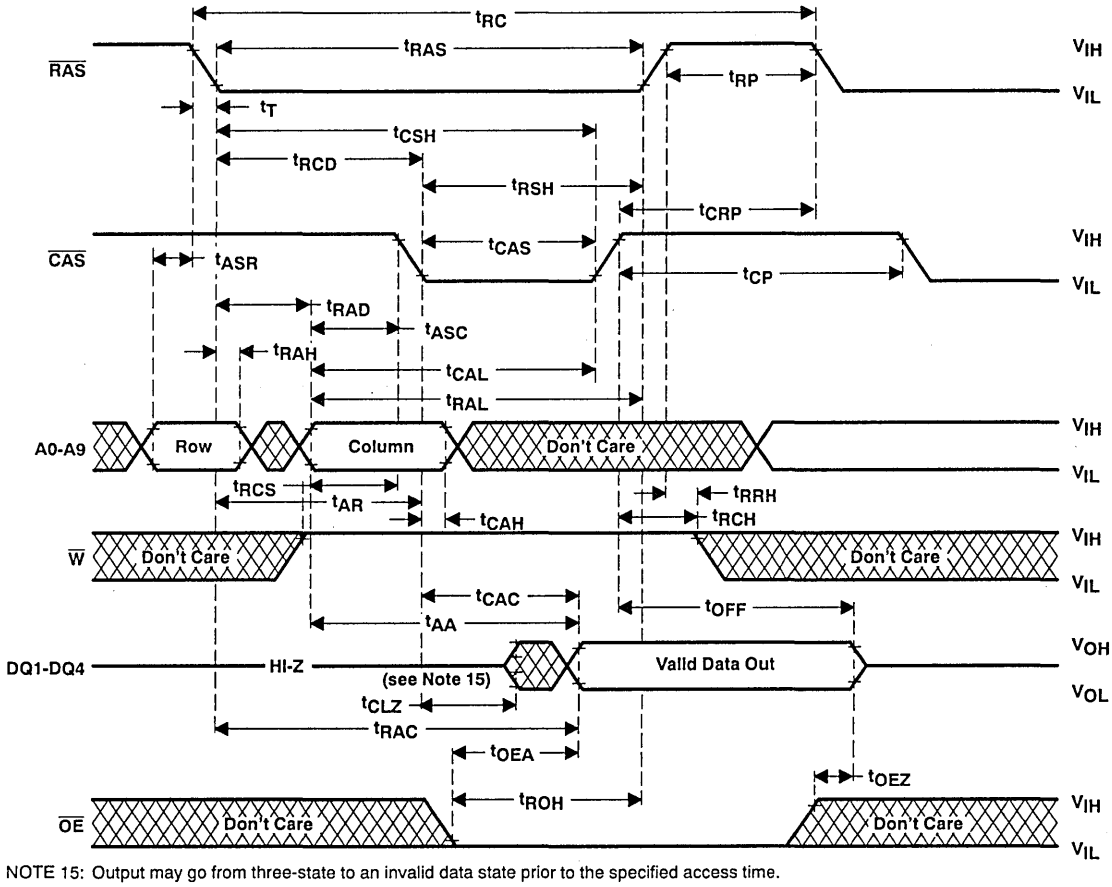


(a) Load Circuit

(b) Alternate Load Circuit

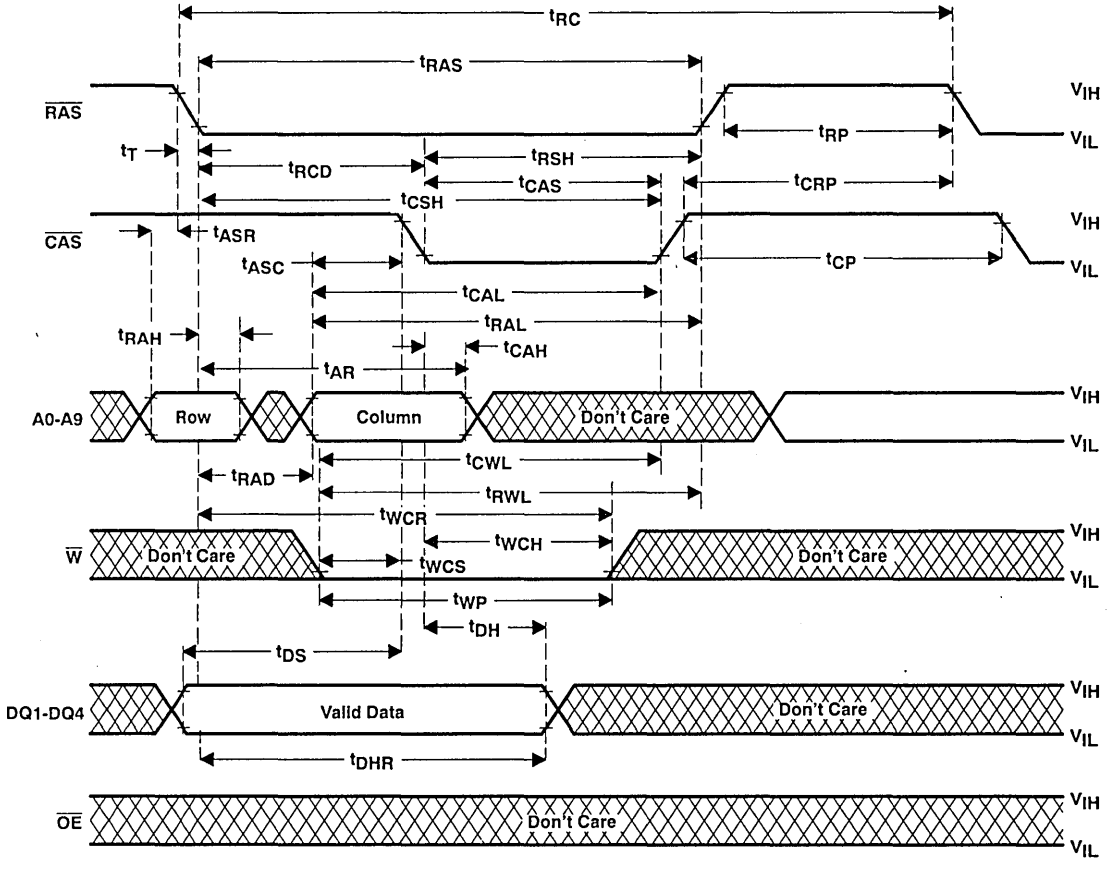
Figure 1. Load Circuits for Timing Parameters

read cycle timing

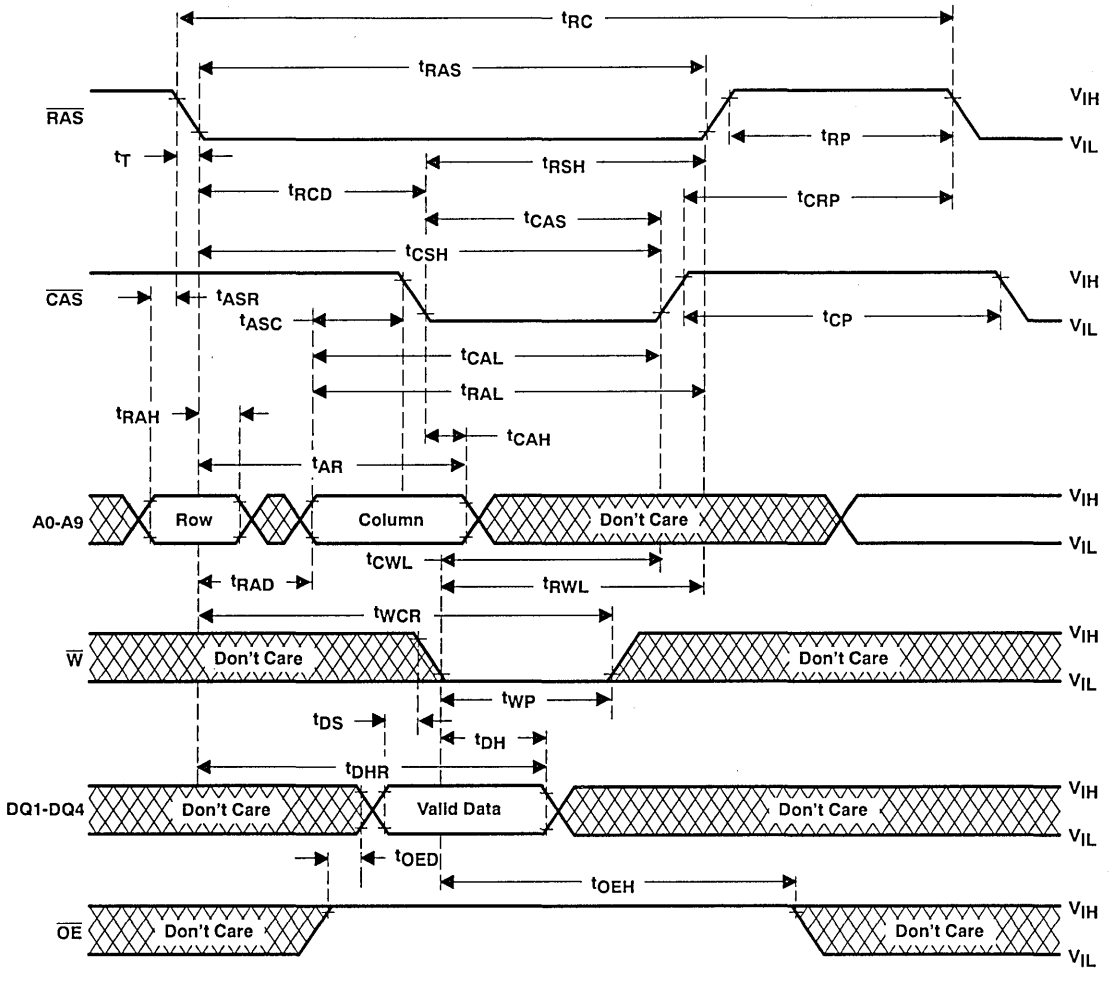


NOTE 15: Output may go from three-state to an invalid data state prior to the specified access time.

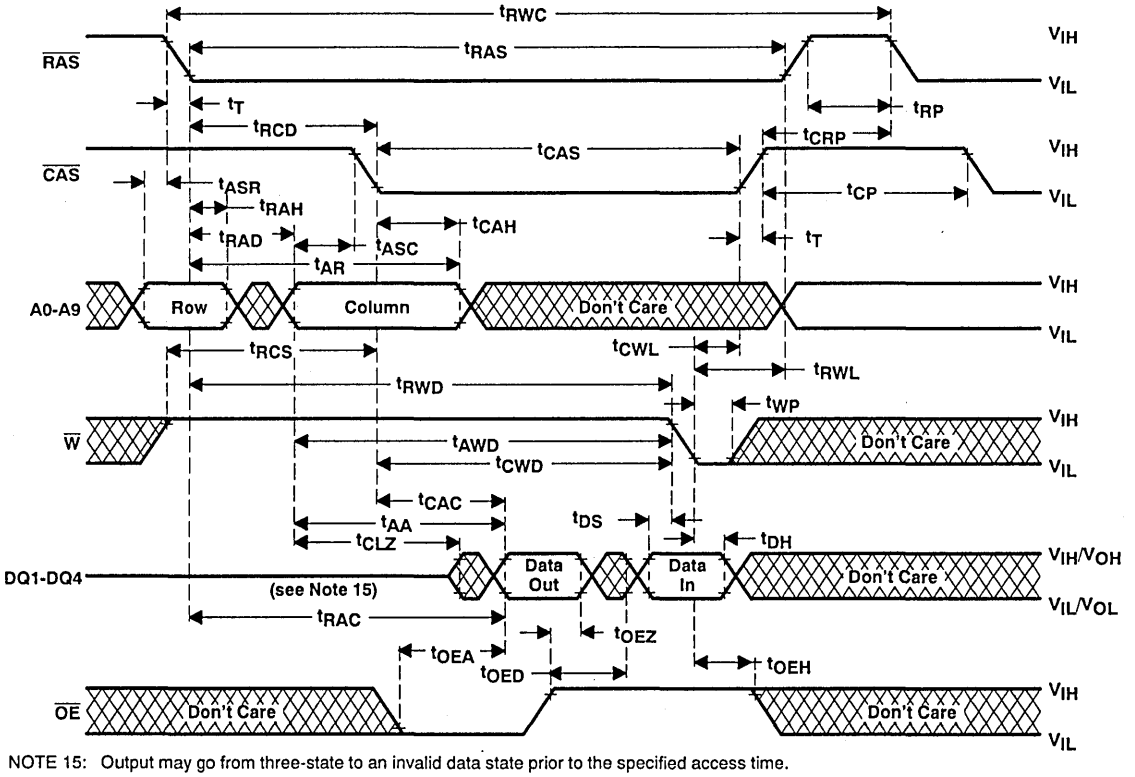
early write cycle timing



write cycle timing

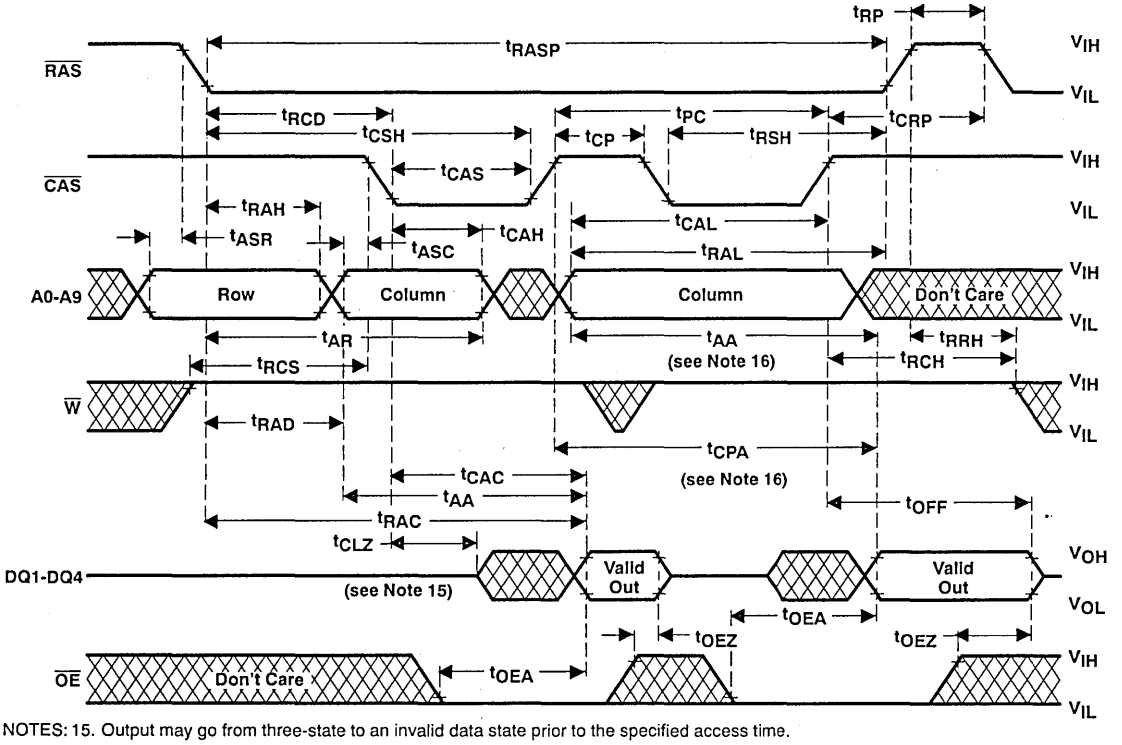


read-write cycle timing



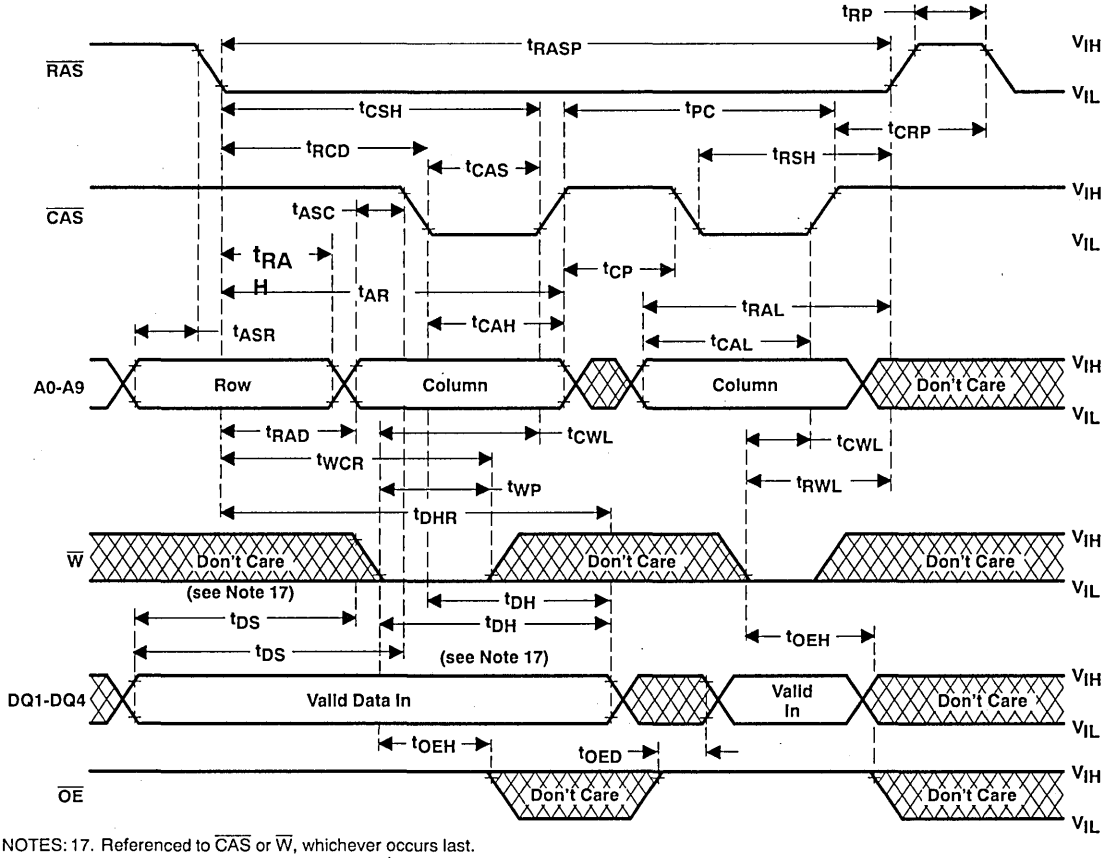
NOTE 15: Output may go from three-state to an invalid data state prior to the specified access time.

enhanced page-mode read cycle timing



NOTES: 15. Output may go from three-state to an invalid data state prior to the specified access time.
16. Access time is t_{CPA} or t_{AA} dependent.

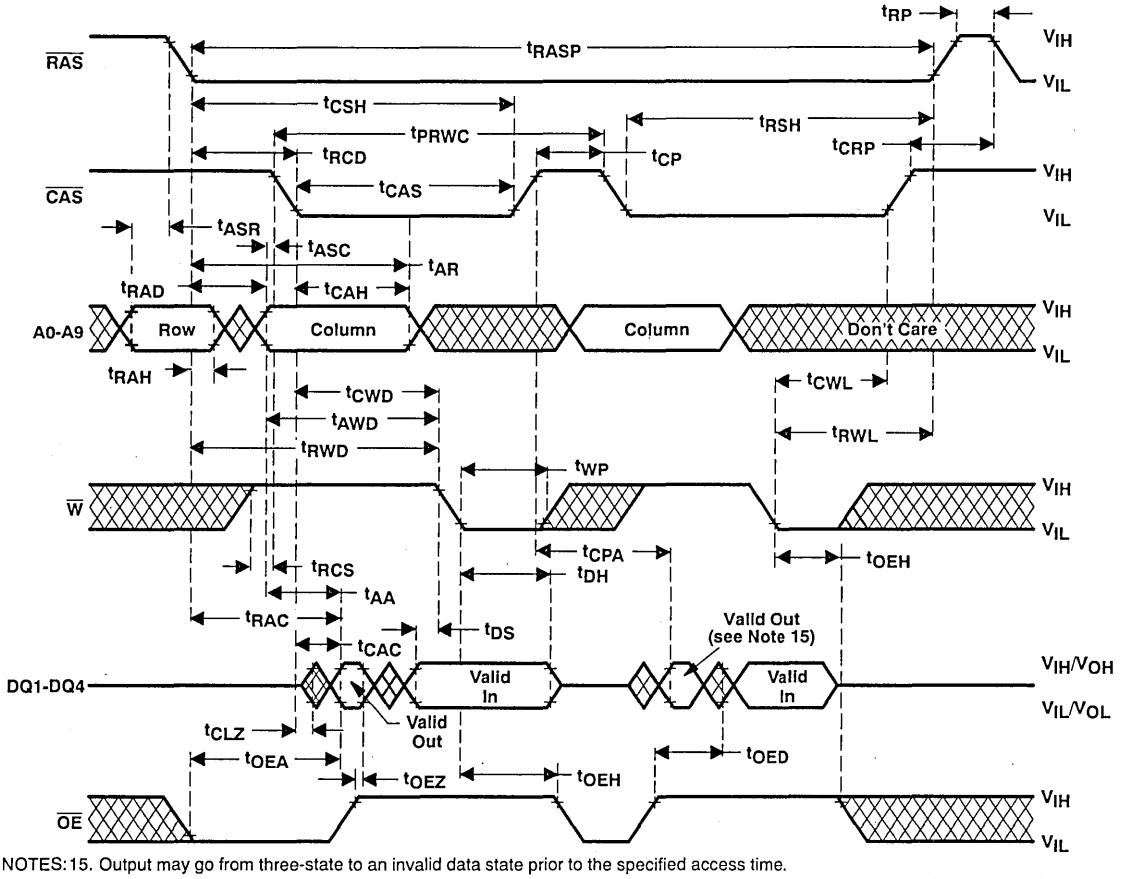
enhanced page-mode write cycle timing



NOTES: 17. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

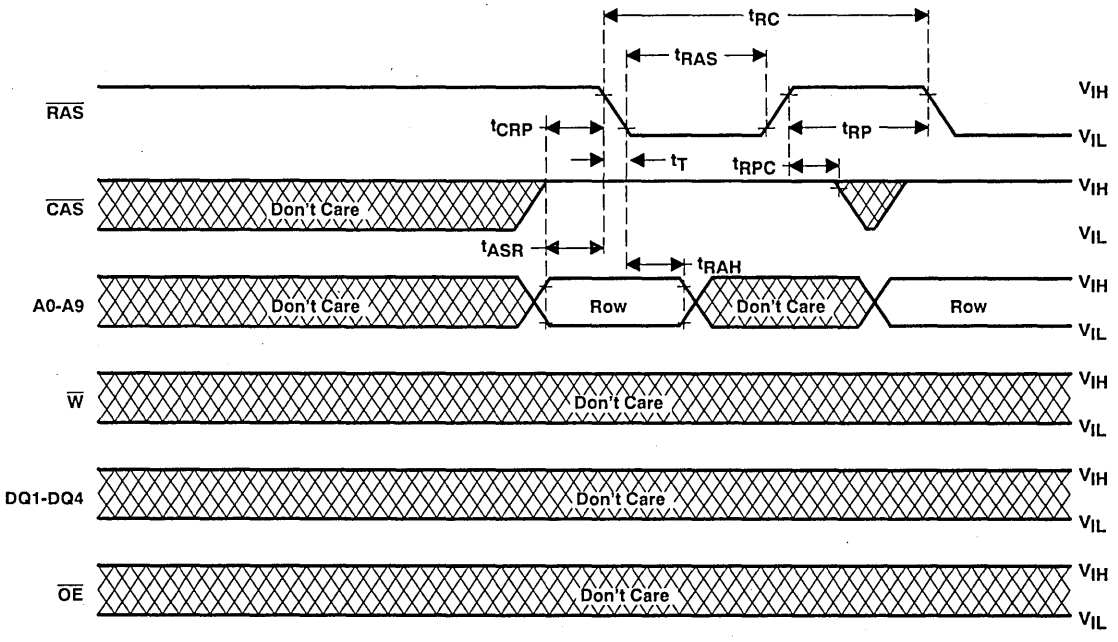
18. A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

enhanced page-mode read-write cycle timing

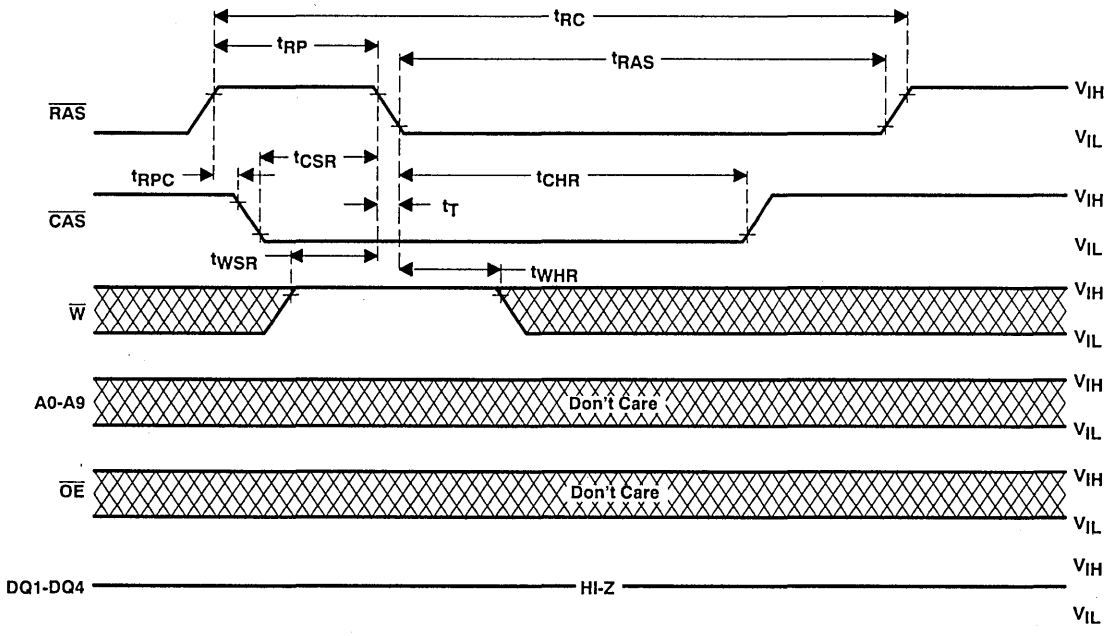


NOTES: 15. Output may go from three-state to an invalid data state prior to the specified access time.
19. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

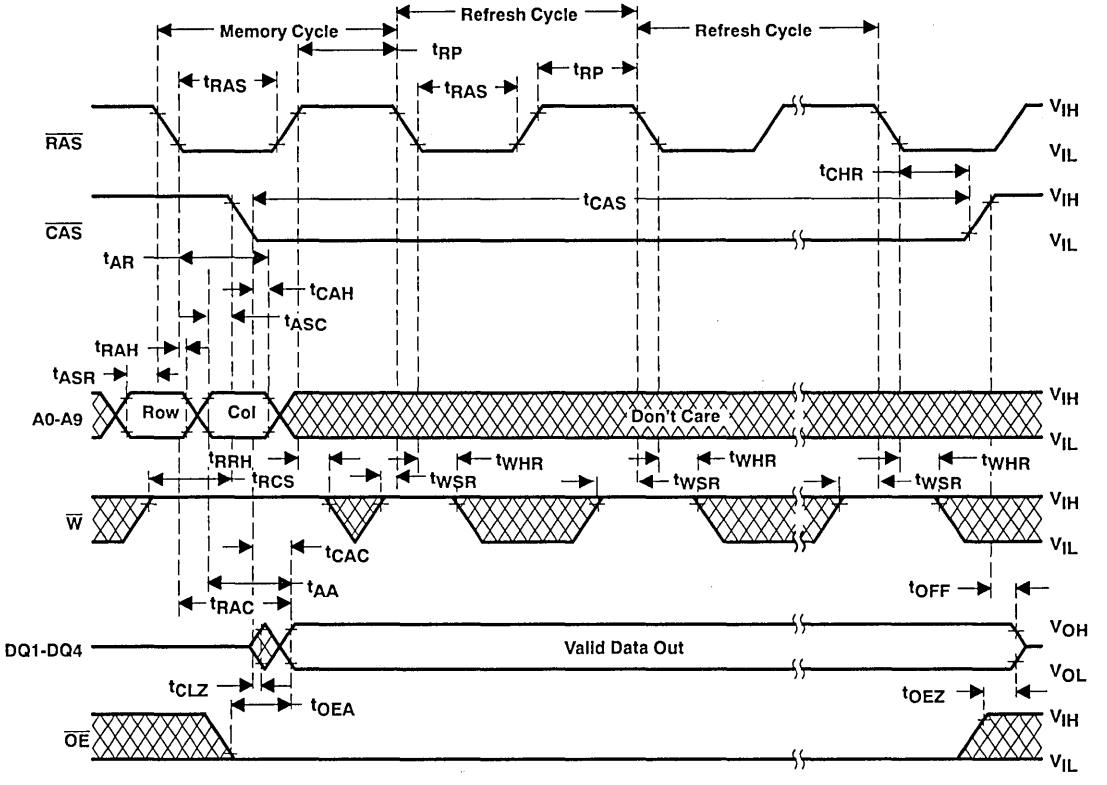
$\overline{\text{RAS}}$-only refresh timing



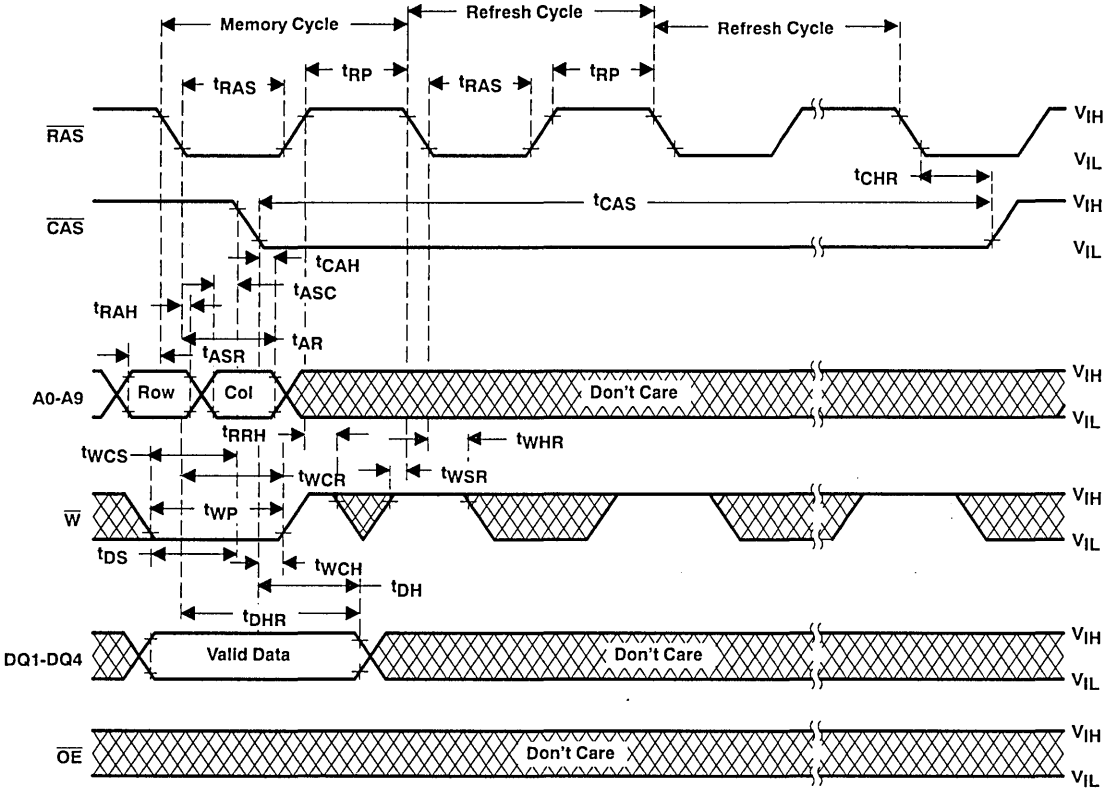
automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



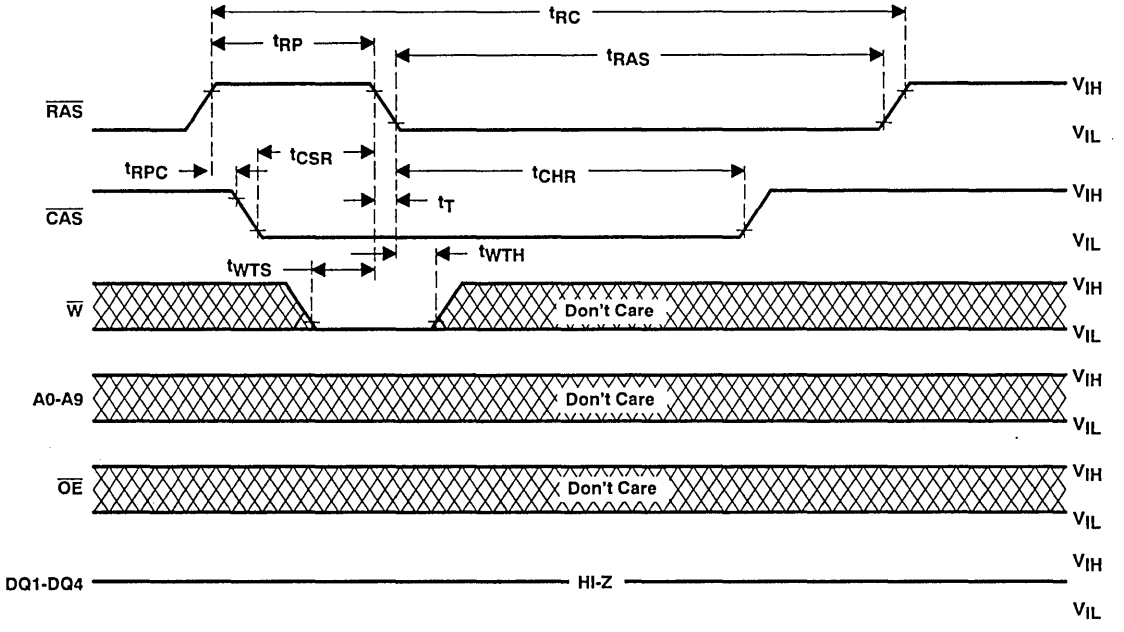
hidden refresh cycle (read)



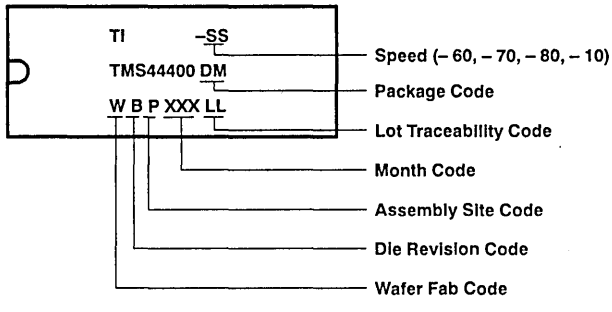
hidden refresh cycle (write)



test mode entry cycle



device symbolization

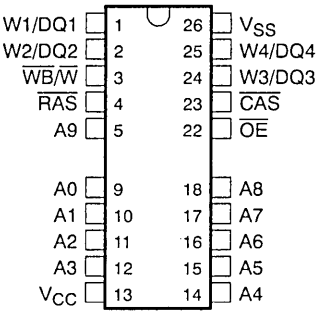


- **Organization . . . 1 048 576 × 4**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

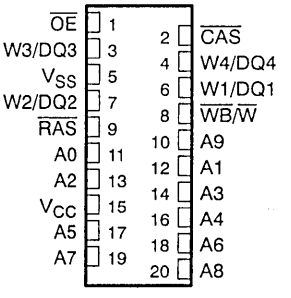
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS44410-60	60 ns	15 ns	30 ns	155 ns
TMS44410-70	70 ns	18 ns	35 ns	181 ns
TMS44410-80	80 ns	20 ns	40 ns	205 ns
TMS44410-10	100 ns	25 ns	45 ns	245 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
  - **—Higher Data Bandwidth than Conventional Page-Mode Parts**
  - **—Random Single-Bit Access Within a Row With a Column Address**
  - **—Write-Per-Bit Functionality**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 1024-Cycle Refresh in 16 ms (Max)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **High-Reliability Plastic 300-mil and 350-mil 20/26-Lead Surface Mount (SOJ) Packages and 20-Pin Zig-Zag In line (ZIP) Package**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**

DM and DJ Package†
(Top View)



SD Package†
(Top View)



† The packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
W1/DQ1-W4/DQ4	Write-Per-Bit Data Mask/Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{WB/W}$	Write-Per-Bit Enable/Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS44410 series are high-speed 4 194 304-bit dynamic random-access memories, organized as 1 048 576 words of four bits each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 360 mW operating and 6 mW standby.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

EPIC is a trademark of Texas Instruments Incorporated.

The TMS44410 is offered in a 350-mil 20/26-lead plastic surface mount SOJ package (DM), a 300-mil 20/26-lead plastic surface mount SOJ package (DJ), and a 20-pin zig-zag in-line package (SD suffix). These packages are guaranteed for operation from 0°C to 70°C.

operation

enhanced page-mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS44410 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

write-per-bit operation

The TMS44410 allows for writing only to selected quadrants using write-per-bit operations. This is accomplished by having $\overline{WB}/\overline{W}$ low when $\overline{RAS}$ drops, which latches in the write mask from the Wn/DQn pins. For each quadrant which the Wn/DQn pin is held low when $\overline{RAS}$ drops, the write operations will be inhibited and will remain inhibited until $\overline{RAS}$ is taken high. The setup and hold times for both $\overline{WB}/\overline{W}$ and Wn/DQn pins are referenced to the falling edge of $\overline{RAS}$. Write-per-bit functionality can be used on all write, read-write, page-mode, and hidden refresh write cycles.

By keeping $\overline{WB}/\overline{W}$ high when $\overline{RAS}$ drops, the TMS44410 will complete a standard, nonwrite-per-bit, write operation (see t_{WBH}).

address (A0 through A9)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write-per-bit enable/write enable ($\overline{WB}/\overline{W}$)

The read or write mode is selected through the write-per-bit enable/write-enable ($\overline{WB}/\overline{W}$) input. A logic high on the $\overline{WB}/\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{WB}/\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

write-per-bit data mask/data in/out (W1/DQ1-W4DQ4)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OED}.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every sixteen milliseconds to retain data. This can be achieved by strobing each of the1024 rows (A0-A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter t_{CSR}] and holding it low after $\overline{RAS}$ falls [see parameter t_{CHR}]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

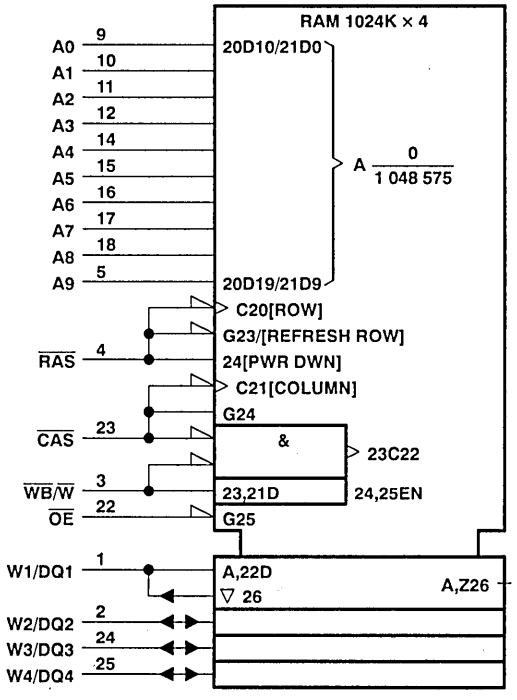
power-up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

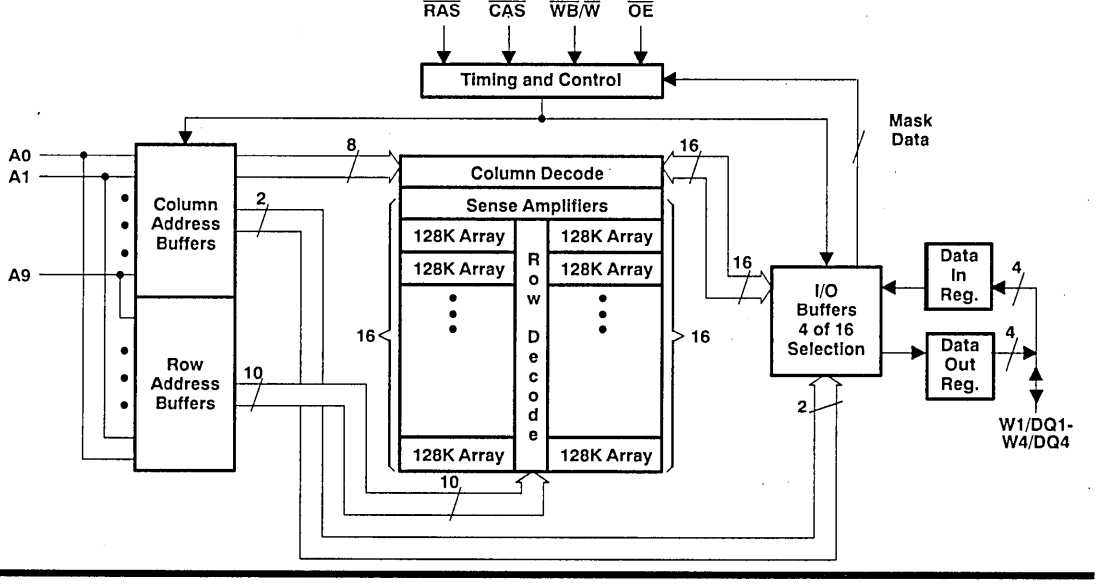
A Design For Test (DFT) mode is incorporated in the TMS44410. A $\overline{CAS}$-before-$\overline{RAS}$ with $\overline{WB}/\overline{W}$ low (WCBR) cycle is used to enter test mode. In the test mode, data is written into and read from eight sections of the array in parallel. All data is written into the array through DQ1. Data is compared upon reading and if all bits are equal, all DQ pins will go high. If any one bit is different; all the DQ pins will go low. Any combination read, write, read-write, or page-mode can be used in the test mode. The test mode function reduces test times by enabling the 1 meg × 4 DRAM to be tested as if it were a 512K DRAM where column address 0 is not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12, for the SOJ packages.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 20: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTES: 21. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS44410-60		TMS44410-70		TMS44410-80		TMS44410-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I=0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		95		85		75		65	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		1		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ high (CBR)		95		85		75		65	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60		50		40	mA

NOTES: 22. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
23. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(D)}$	Input capacitance, data inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 24: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS44410-60		TMS44410-70		TMS44410-80		TMS44410-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20		25	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)	0	15	0	18	0	20	0	25	ns

NOTE 25: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS44410-60		TMS44410-70		TMS44410-80		TMS44410-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		180		ns
t_{RWC}	Read-write cycle time	155		181		205		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		55		ns
t_{PRWC}	Page-mode read-write cycle time	85		96		105		120		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{WB}/\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{WB}/\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{WB}/\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{WB}/\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTS}	$\overline{WB}/\overline{W}$-low setup time (test mode only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		75		ns
t_{DH}	Data hold time (see Note 11)	10		15		15		20		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		75		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	0		0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		75		ns
t_{WHR}	$\overline{WB}/\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTH}	$\overline{WB}/\overline{W}$-low hold time (test mode only)	10		10		10		10		ns
t_{WBS}	Write setup before $\overline{RAS}$ low (WPB)	0		0		0		0		ns
t_{WDS}	Data setup before $\overline{RAS}$ low (WPB)	0		0		0		0		ns
t_{WBH}	Write hold after $\overline{RAS}$ low (WPB)	10		10		10		10		ns

Continued next page.

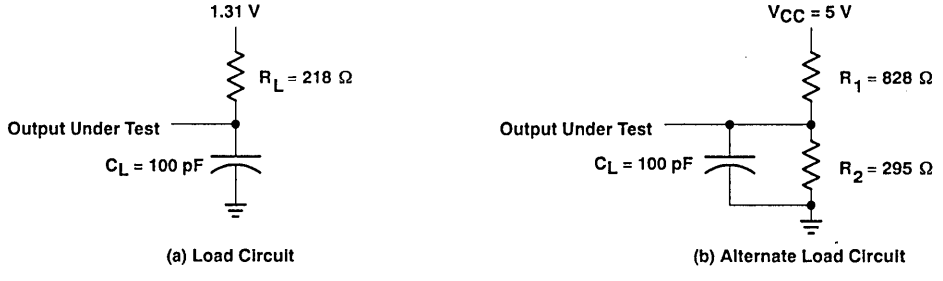
NOTES: 26. All cycle times assume t_T = 5 ns.
27. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
28. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
29. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
30. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
31. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
32. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		TMS44410-60		TMS44410-70		TMS44410-80		TMS44410-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{WDH}	Data hold after $\overline{RAS}$ low (WPB)	10		10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{WB/W}$ low (Read-write operation only)	55		63		70		80		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{WB/W}$ low (Read-write operation only)	40		46		50		60		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		25		ns
t_{OED}	$\overline{OE}$ to data delay	15		18		20		25		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	30	15	35	15	40	20	50	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	25	52	20	60	25	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{WB/W}$ low (Read-write operation only)	85		98		110		135		ns
t_{TAA}	Access time from address (test mode)	35		40		45		50		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		55		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		105		ns
t_{REF}	Refresh time interval		16		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	2	50	ns

NOTE 33: The maximum value is specified only to guarantee access time.

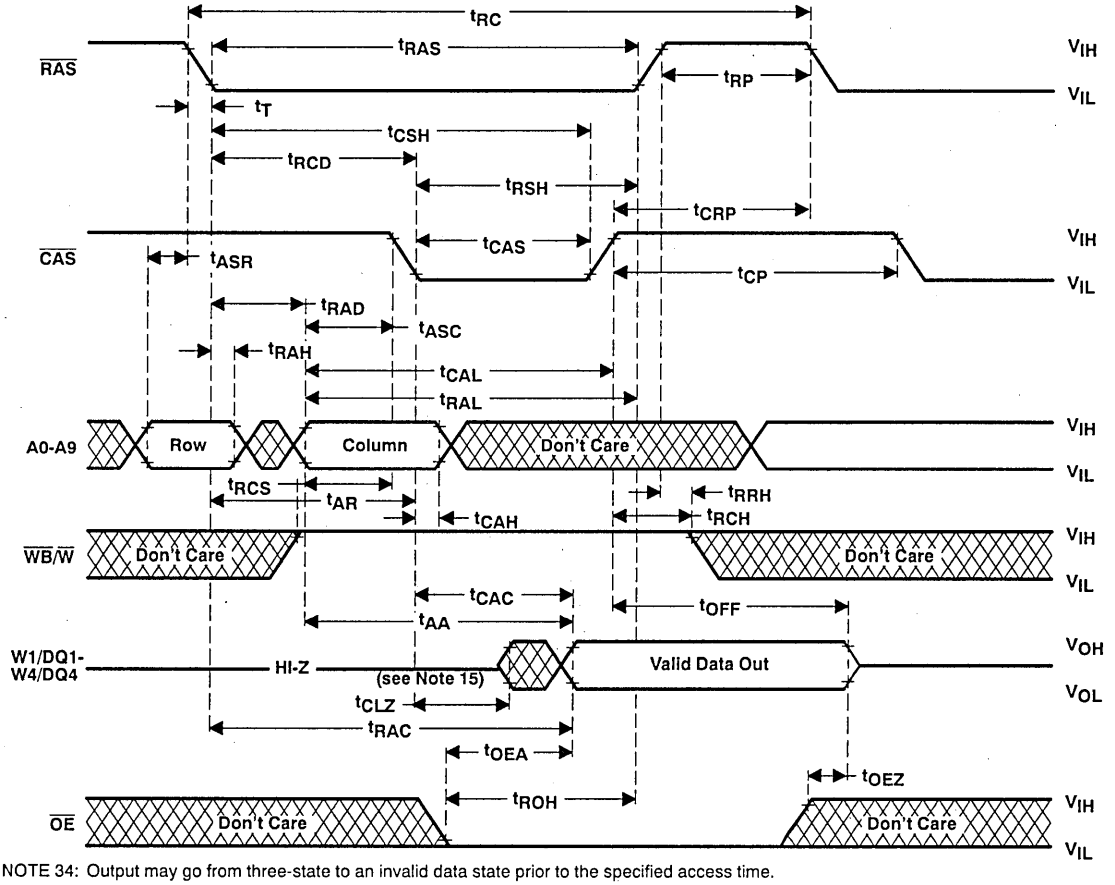
PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

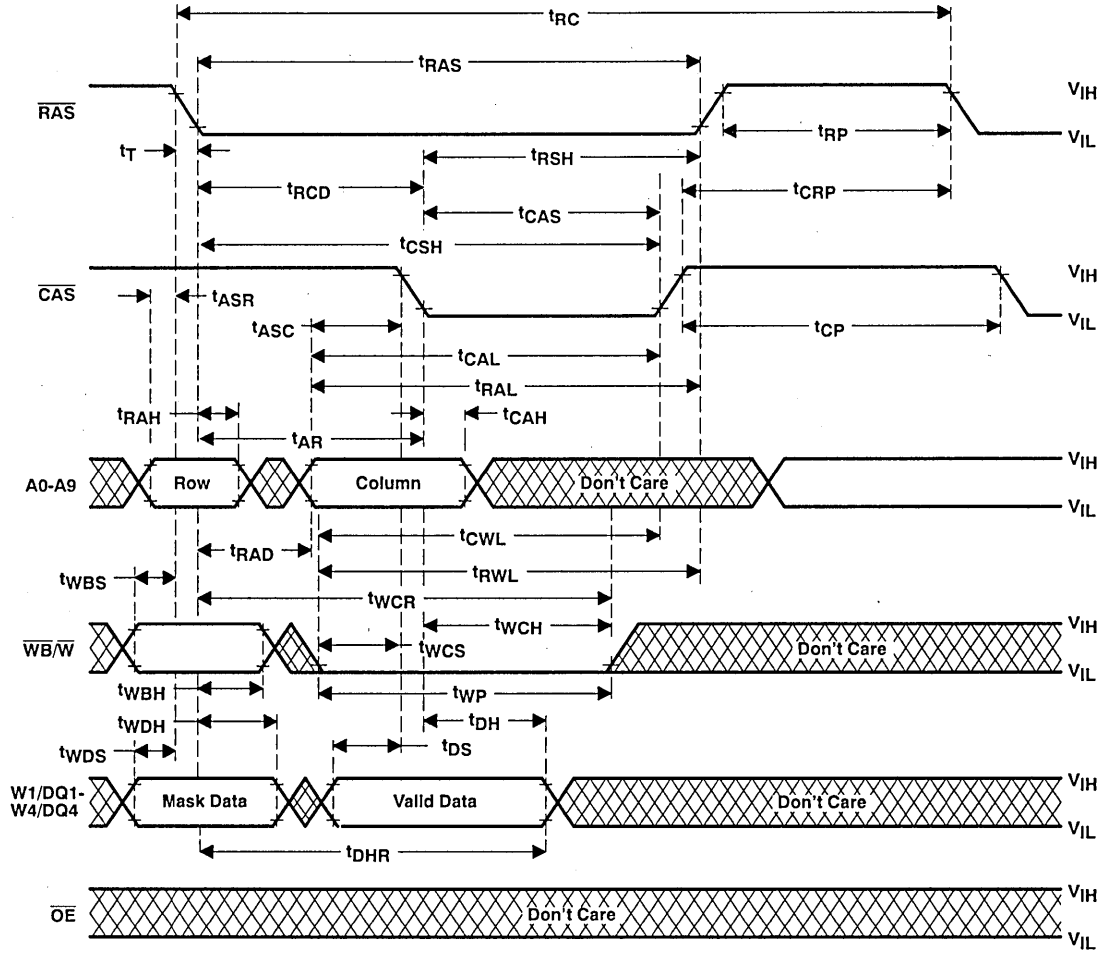
Figure 2. Load Circuits for Timing Parameters

read cycle timing

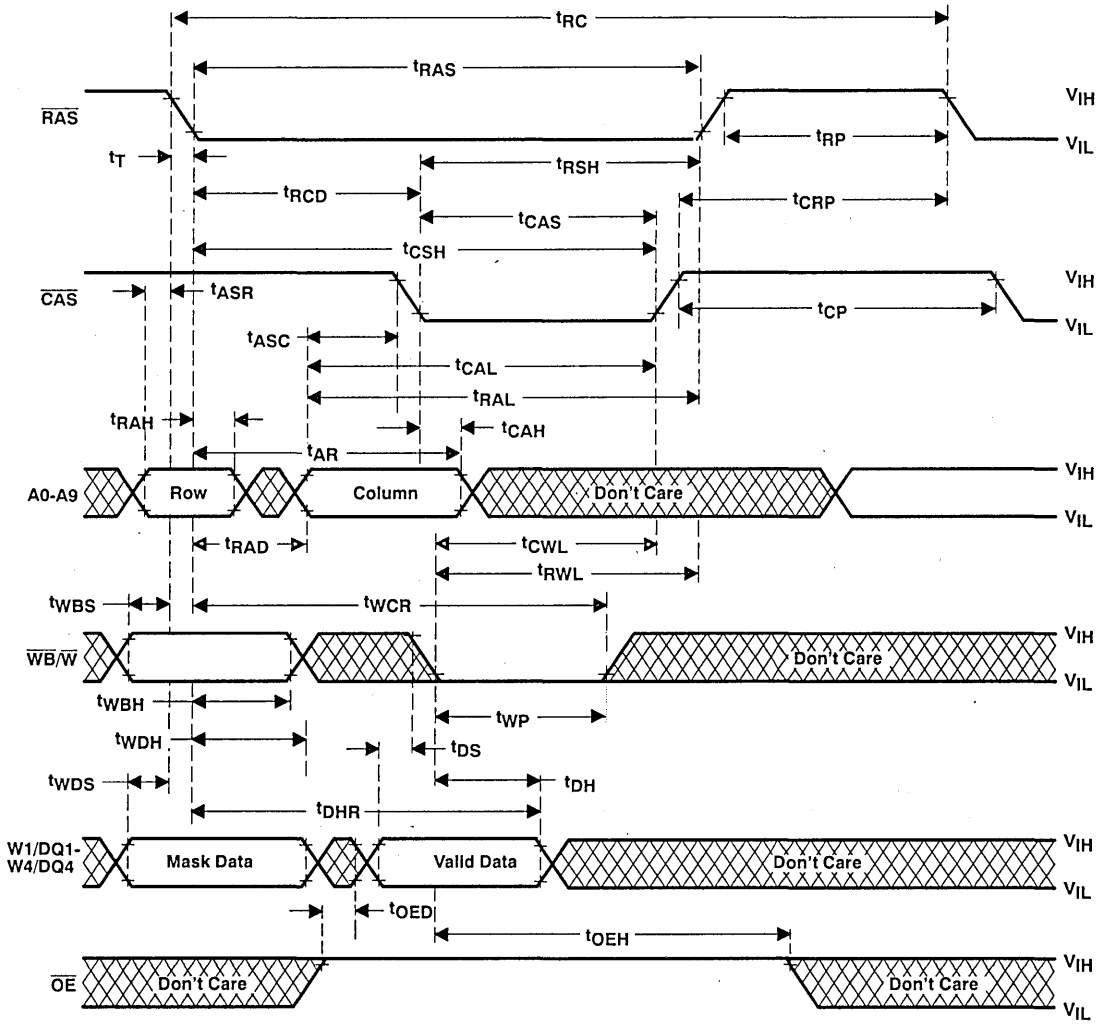


NOTE 34: Output may go from three-state to an invalid data state prior to the specified access time.

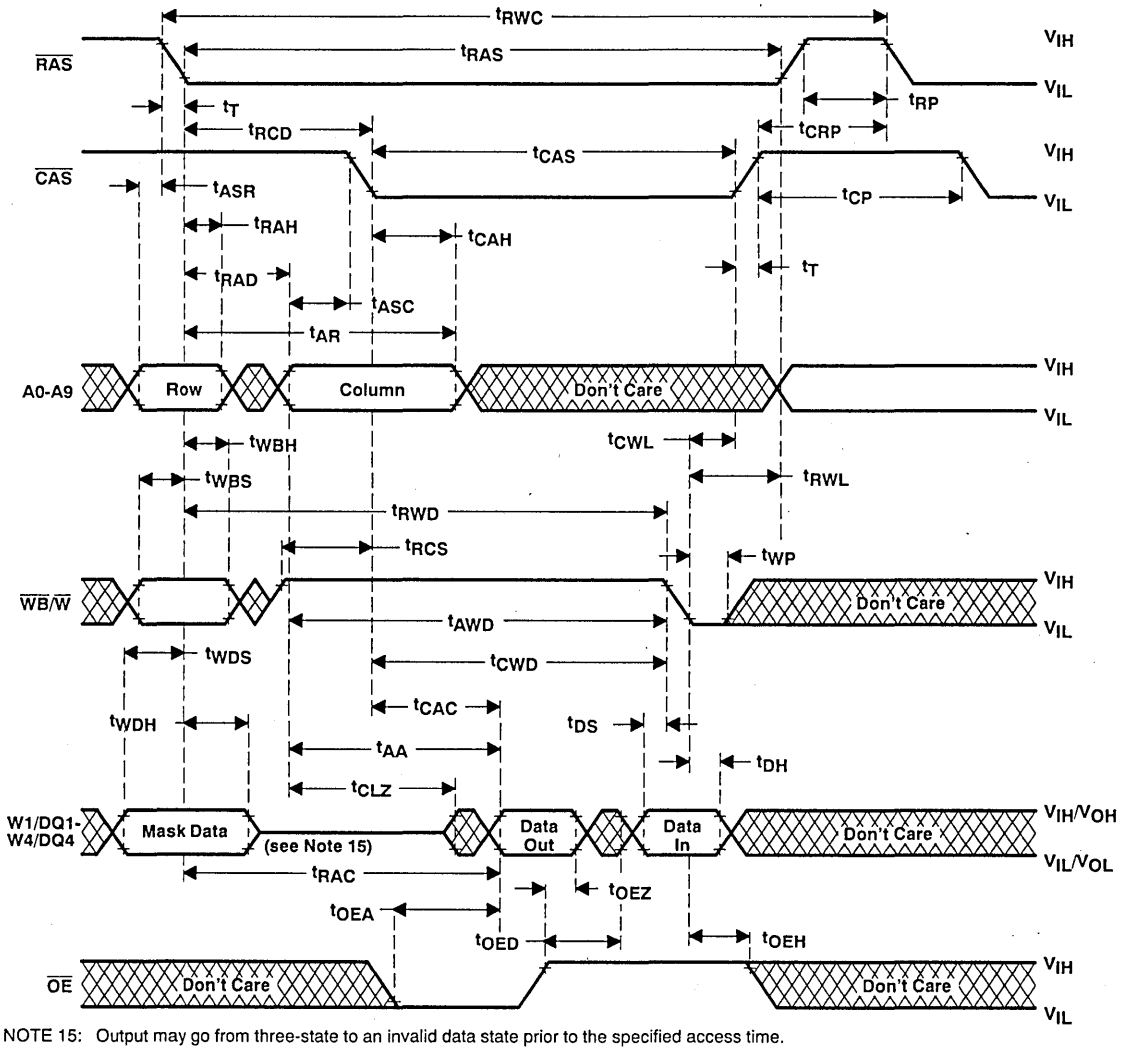
early write cycle timing



write cycle timing

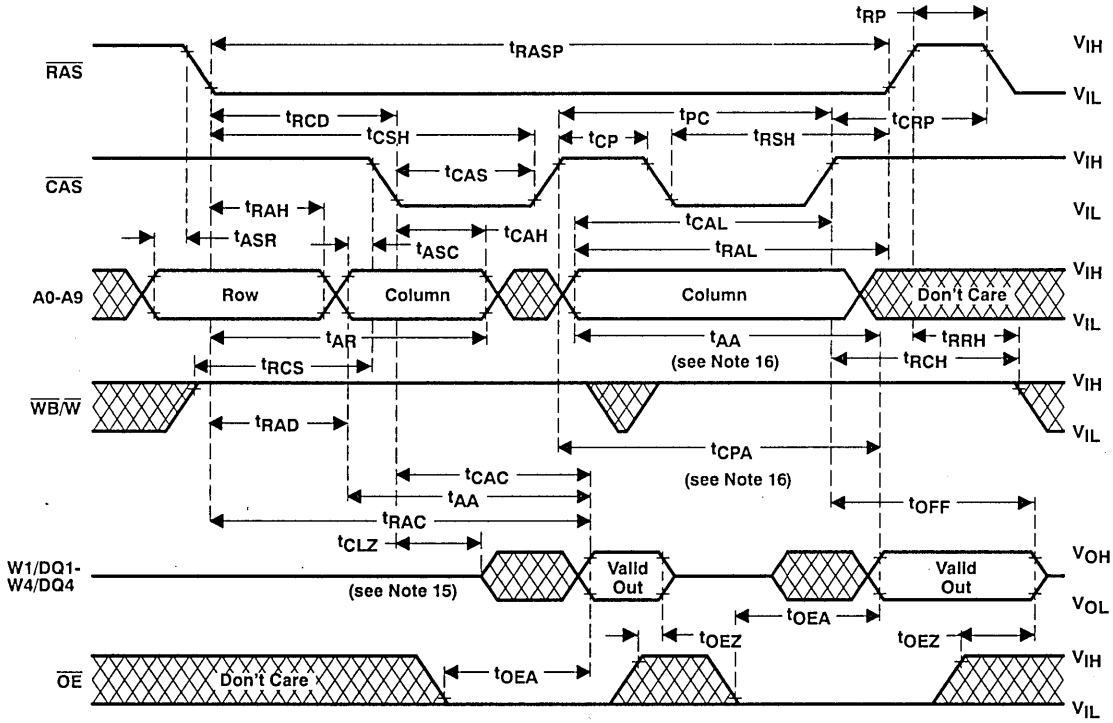


read-write cycle timing



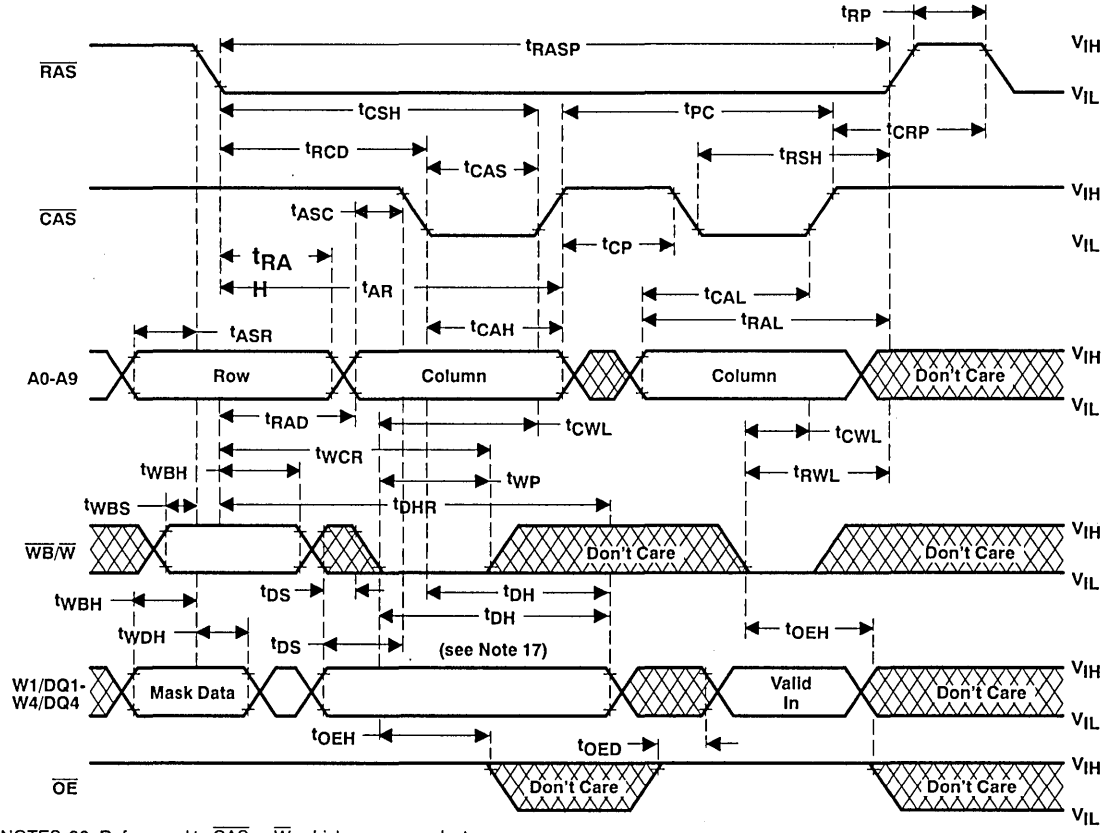
NOTE 15: Output may go from three-state to an invalid data state prior to the specified access time.

enhanced page-mode read cycle timing



NOTES: 15. Output may go from three-state to an invalid data state prior to the specified access time.
35. Access time is t_{CPA} or t_{AA} dependent.

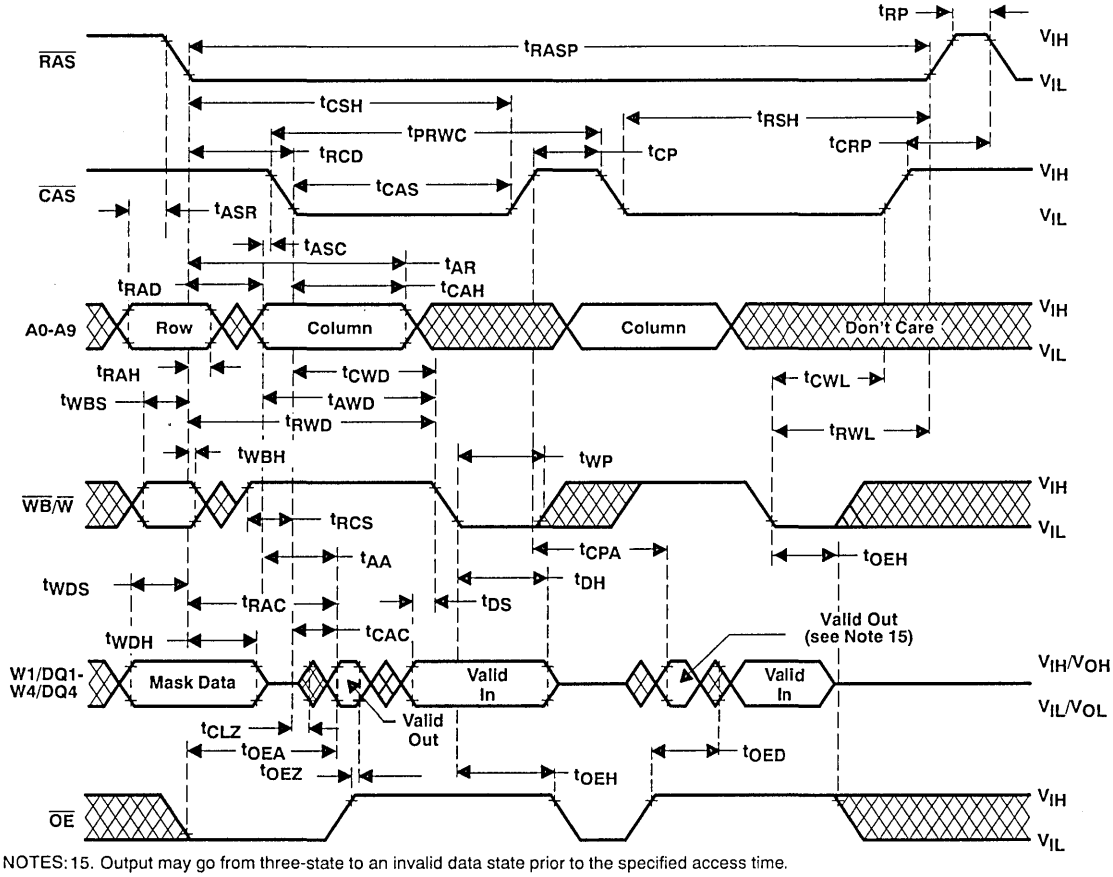
enhanced page-mode write cycle timing



NOTES: 36. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

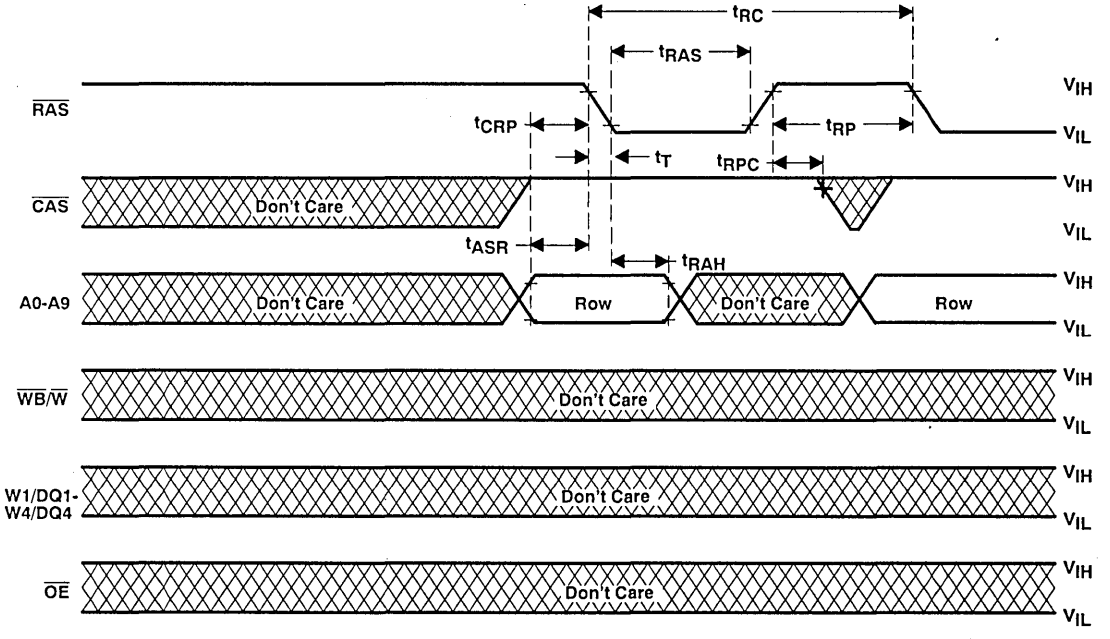
37. A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

enhanced page-mode read-write cycle timing

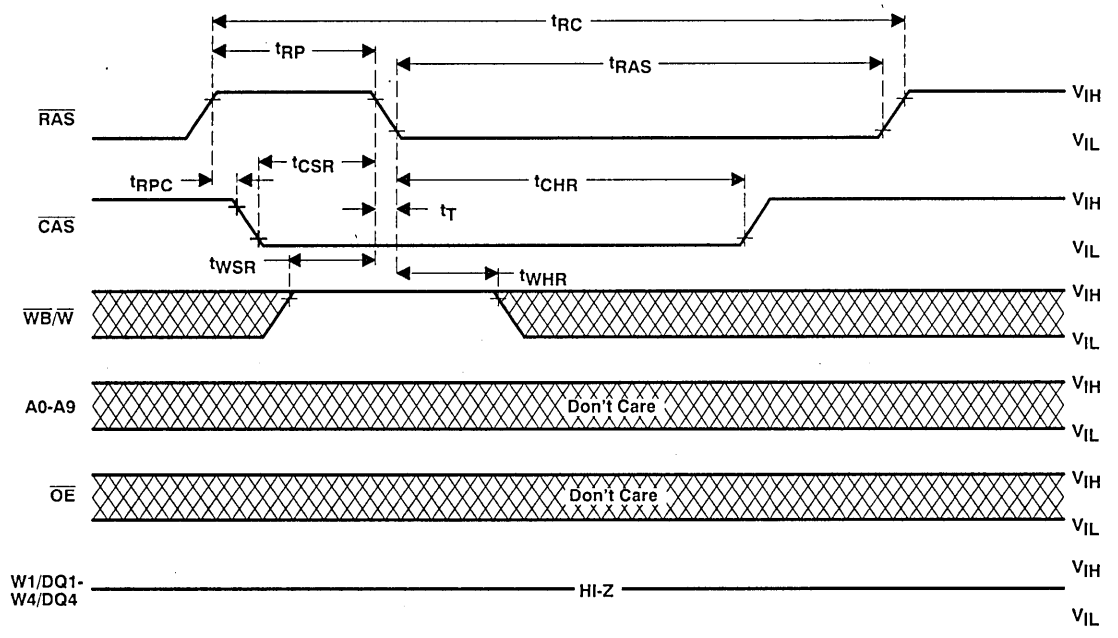


NOTES: 15. Output may go from three-state to an invalid data state prior to the specified access time.
38. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

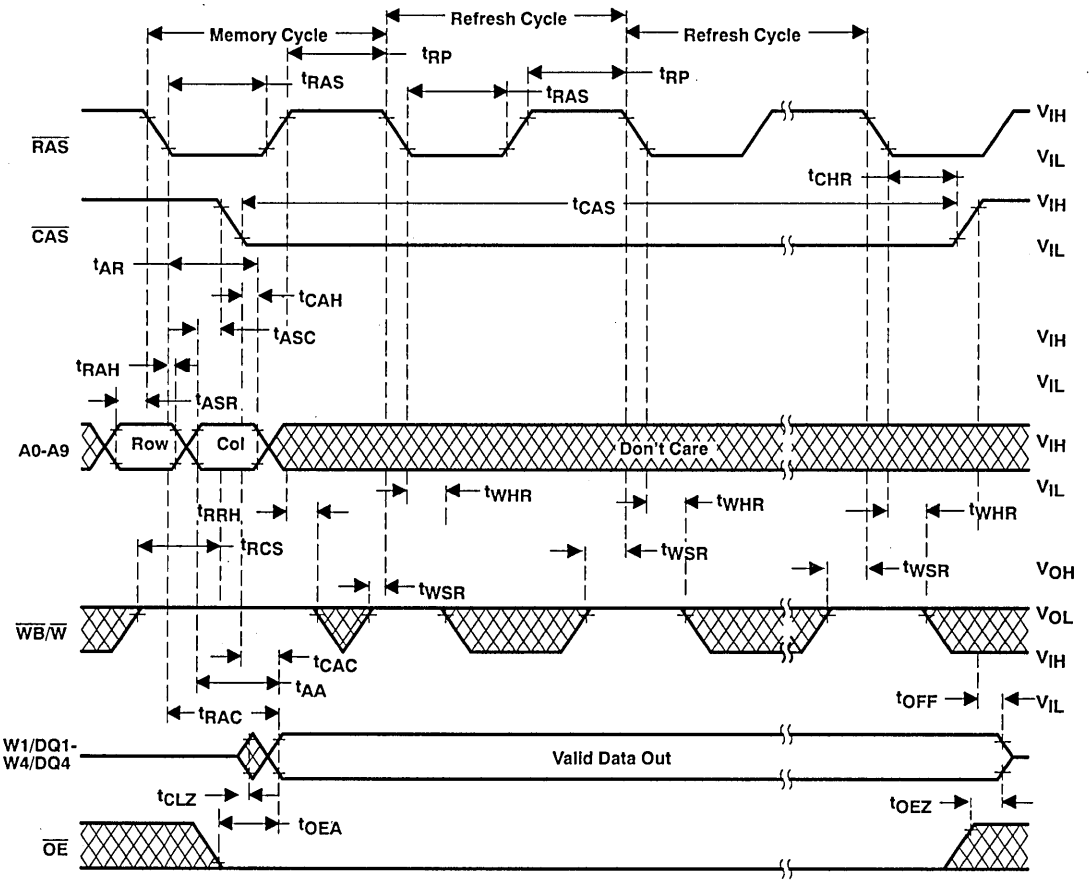
$\overline{\text{RAS}}$-only refresh timing



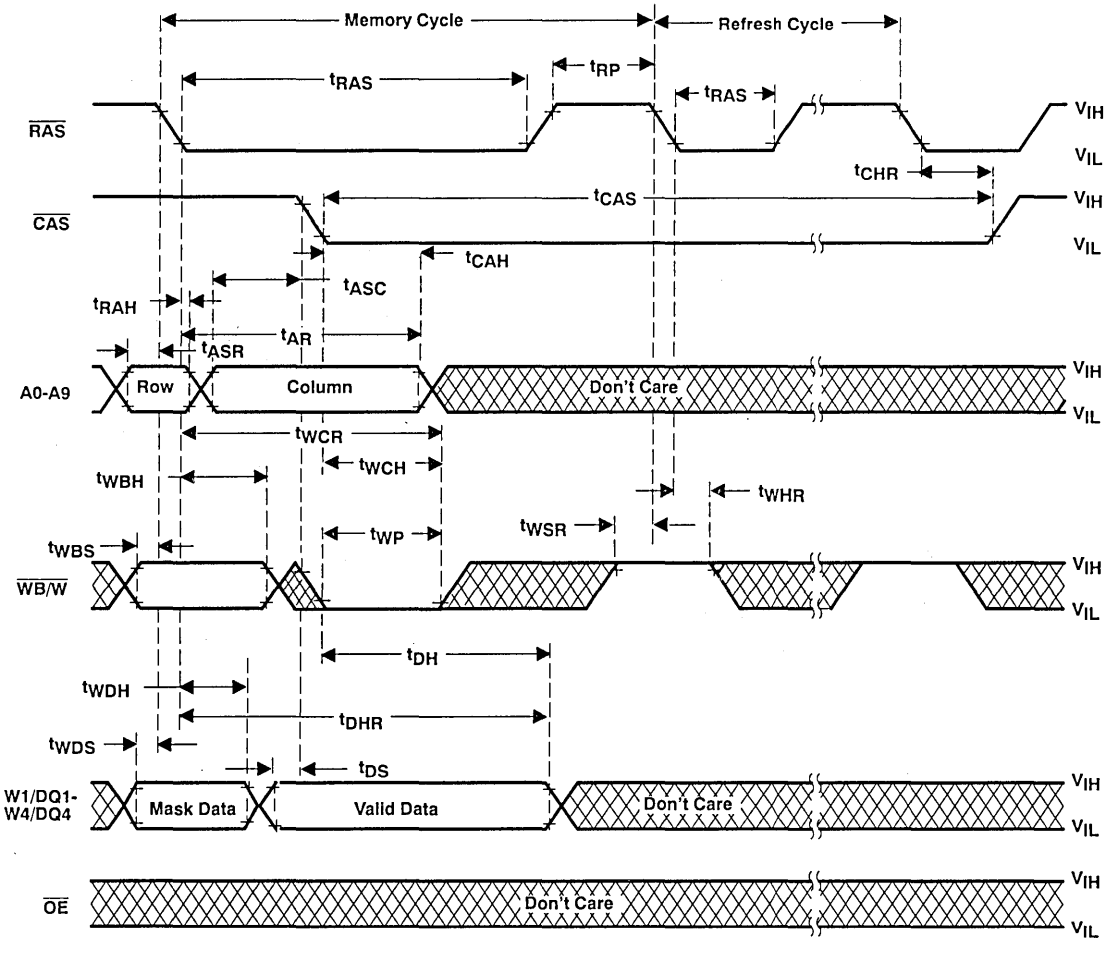
automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



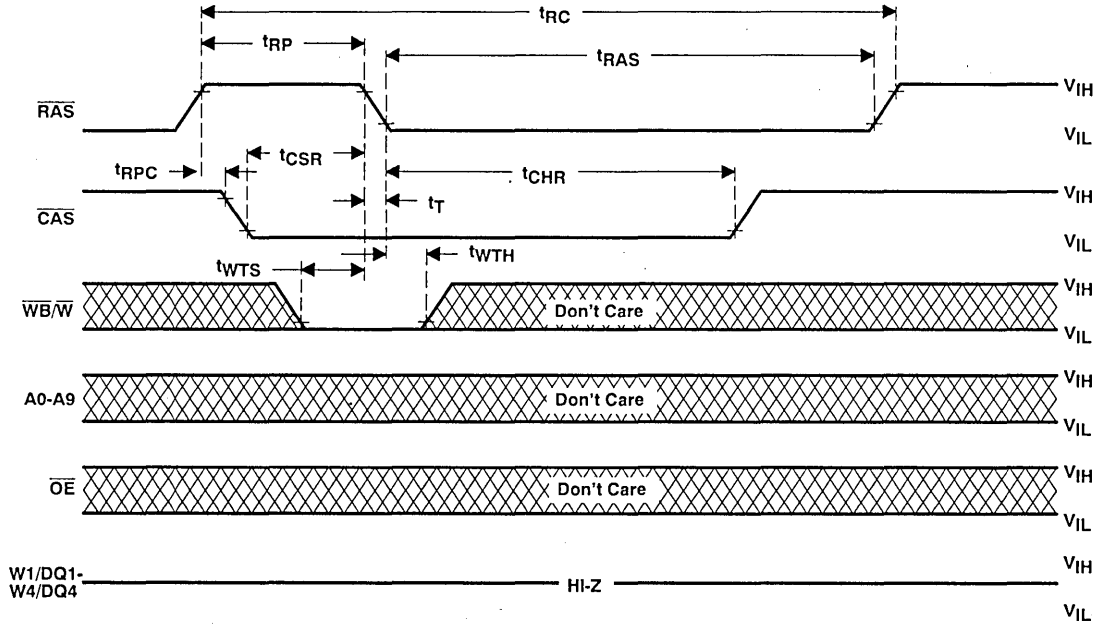
hidden refresh cycle (read)



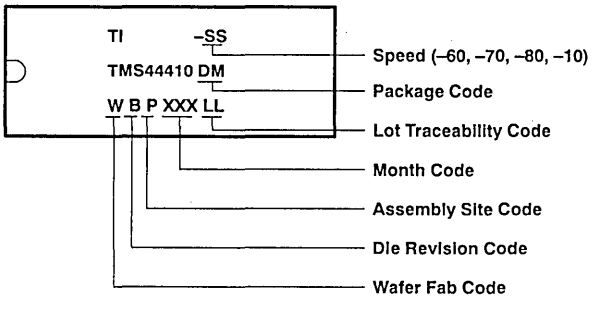
hidden refresh cycle (write)



test mode entry cycle



device symbolization

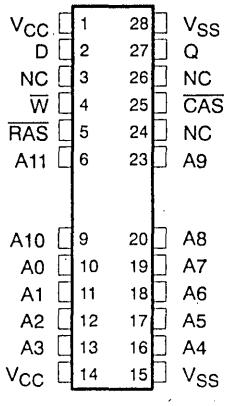


- **Organization . . . 16 777 216 × 1**
- **Single 5-V Power Supply (10% Tolerance)**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
TMS416100-60	60 ns	15 ns	30 ns	110 ns
TMS416100-70	70 ns	18 ns	35 ns	130 ns
TMS416100-80	80 ns	20 ns	40 ns	150 ns
TMS416100-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 4096 Cycles Refresh in 64 ms**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs, Outputs and Clocks are TTL Compatible**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**
- **This Specification Is Fully Compatible with the Preliminary 16 Megabit DRAM Specification From Hitachi.**

DZ Package
(Top View)



PIN NOMENCLATURE	
A0-A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connect
Q	Data Out
$\overline{RAS}$	Row-Address strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

ADVANCE INFORMATION

description

The TMS416100 series are high-speed 16 777 216-bit dynamic random-access memories, organized as 16 777 216-bit words by one bit each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns.

All inputs, outputs, and clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS416100 is offered in a 400-mil 24/28-pin surface mount SOJ package (DZ suffix). The package is characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$-low width.

EPIC is a trademark of Texas Instruments, Incorporated

The Column Address Buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch, while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output enable.

This feature allows the TMS416100 to operate at a higher data bandwidth than conventional page-mode parts, since retrieval begins as soon as the column address is valid, rather than when $\overline{CAS}$ transitions low. The performance improvement is referred to as "enhanced page mode". Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) and t_{RAC} have been satisfied. In the event that the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0-A11)

Twenty-four address bits are required to decode 1 of 16 777 216 storage cell locations. Twelve row-address bits are set on inputs A0 through A11 and latched during a normal access and during $\overline{RAS}$-only refresh as the device requires 4096 refresh cycles. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable $\overline{W}$ input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data-in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out (Q)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fan-out of two Series 74 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change, but retains the state just read.

refresh

A refresh operation must be performed at least once every sixty-four milliseconds to retain data. This can be achieved by strobing each of the 4096 rows (A0-A11). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at a high (inactive) level, thus conserving power since the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after the specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden refresh cycle. An internal refresh address provides the refresh address during hidden refresh.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

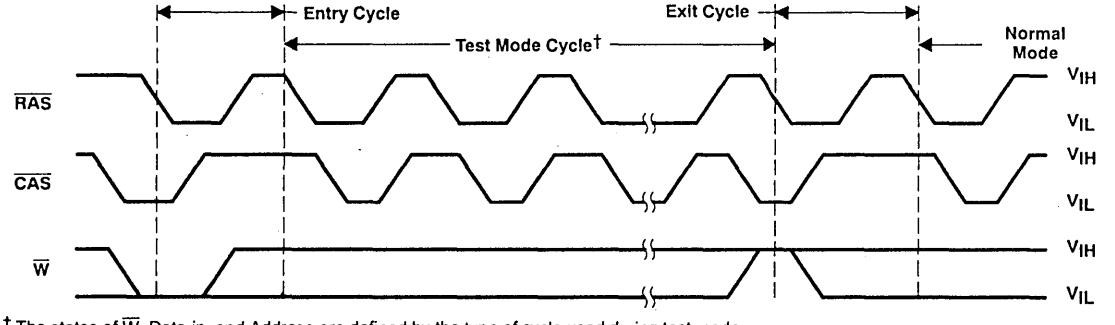
power-up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

The test mode is initiated with a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle while simultaneously holding the $\overline{W}$ input low (WCBR). The initiate cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in test mode, any desired data sequence can be performed on the device. The device exits the test mode if a $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, with $\overline{W}$ input held high,or a $\overline{RAS}$-only refresh (ROR) cycle is performed.

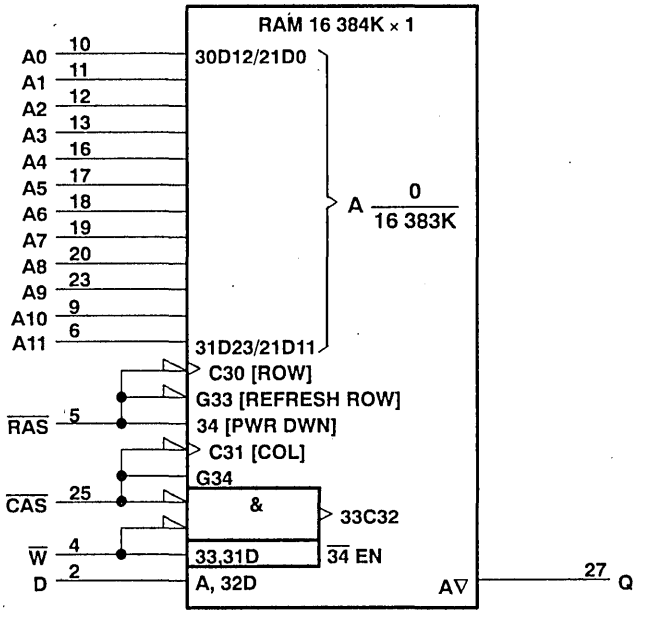
Test mode causes the part to be internally reconfigured into a 1024K × 16 bit device, with 16-bit parallel read and write data path. Column addresses CA0, CA1, CA10, and CA11 are not used. During a read cycle all 16 bits of the internal data bus are compared. If all bits are the same data state, the output pin will go high. If one or more bits disagree, the output pin will go low. Test time in test mode can thus be reduced by a factor of 16, compared to normal memory mode.



† The states of $\overline{W}$, Data-in, and Address are defined by the type of cycle used during test mode.

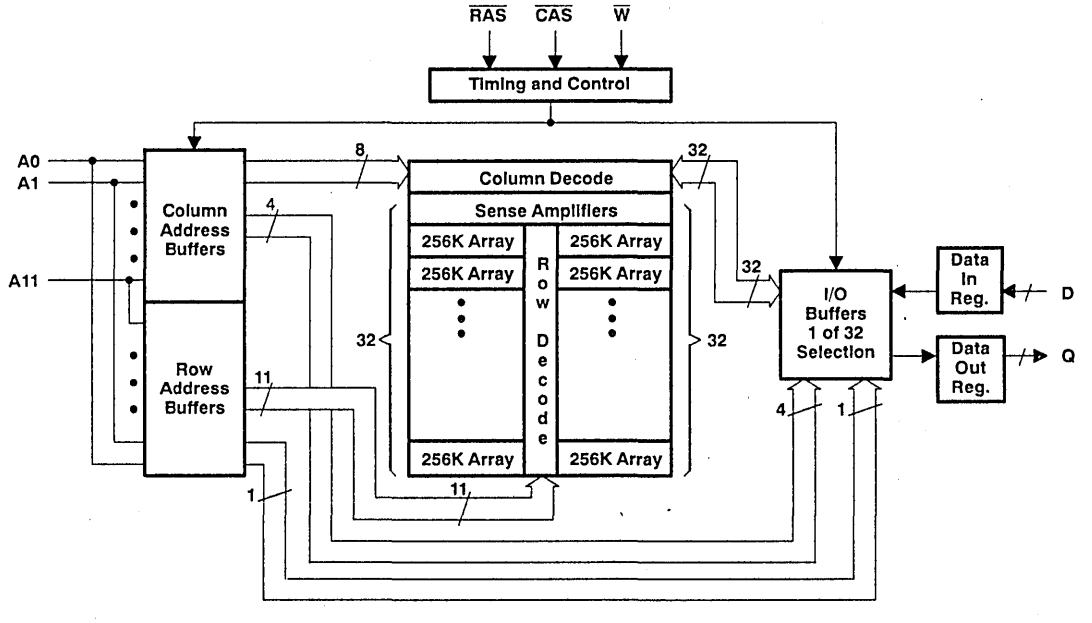
Figure 1. Test Mode Cycle

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin (see Note 1) ..... – 1 V to 7 V
Voltage on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS416100-60		TMS416100-70		TMS416100-80		TMS416100-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)‡	V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)‡	V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		90		80		70		60	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		1		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR)‡	$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		90		80		70		60	mA
I_{CC4}	Average page current (see Note 4)‡	$\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60		50		45	mA
I_{CC7}	Standby current output enable‡	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled		5		5		5		5	mA

‡ Minimum cycle, V_{CC} = 5.5 V.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(D)}$	Input capacitance, data input			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 5: V_{CC} equal to 5.0 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS416100-60		TMS416100-70		TMS416100-80		TMS416100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OH}	Output disable start of $\overline{CAS}$ high	3		3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	0	25	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS416100-60		TMS416100-70		TMS416100-80		TMS416100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		180		ns
t_{RWC}	Read-write cycle time	130		153		175		210		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		55		ns
t_{PRWC}	Page-mode read-write cycle time	60		68		75		85		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTS}	$\overline{W}$-low setup time (test mode only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	15		15		15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		75		ns
t_{DH}	Data hold time (see Note 10)	15		15		15		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		75		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	5		5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		75		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		10		ns

Continued next page.

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

ADVANCE INFORMATION

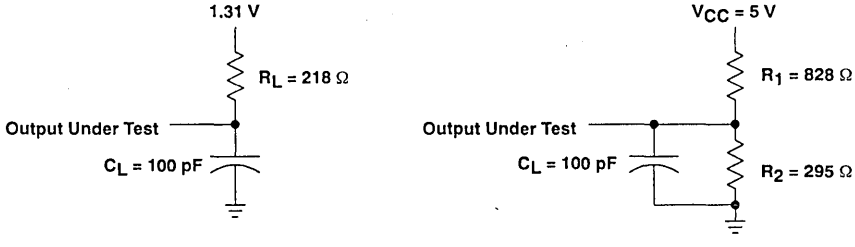
timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		TMS416100-60		TMS416100-70		TMS416100-80		TMS416100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	30		35		40		45		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	15		18		20		25		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	30	15	35	15	40	15	55	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	60		70		80		100		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{TAA}	Access time from address (test mode)	35		40		45		50		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		55		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		105		ns
t_{REF}	Refresh time interval		64		64		64		64	ms
t_T	Transition time	3	30	3	30	3	30	3	30	ns

NOTE 14: The maximum value is specified only to guarantee access time.

ADVANCE INFORMATION

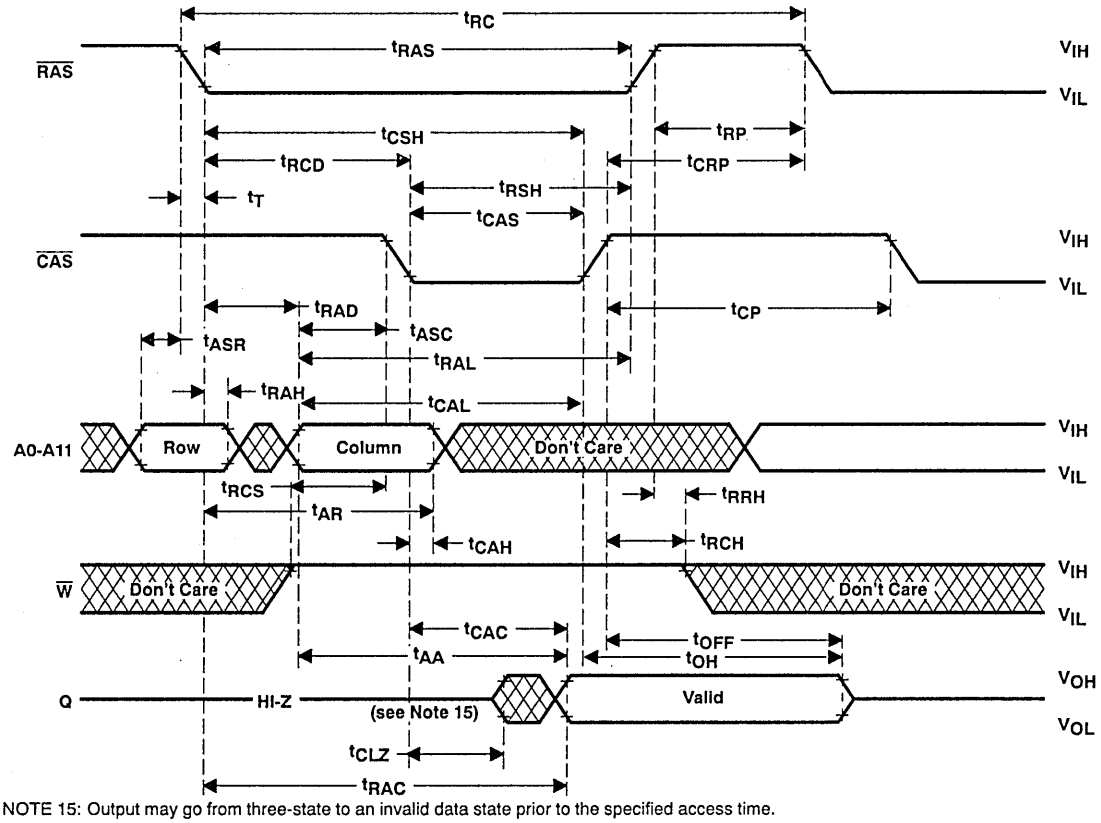
PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

Figure 2. Load Circuits for Timing Parameters

read cycle timing

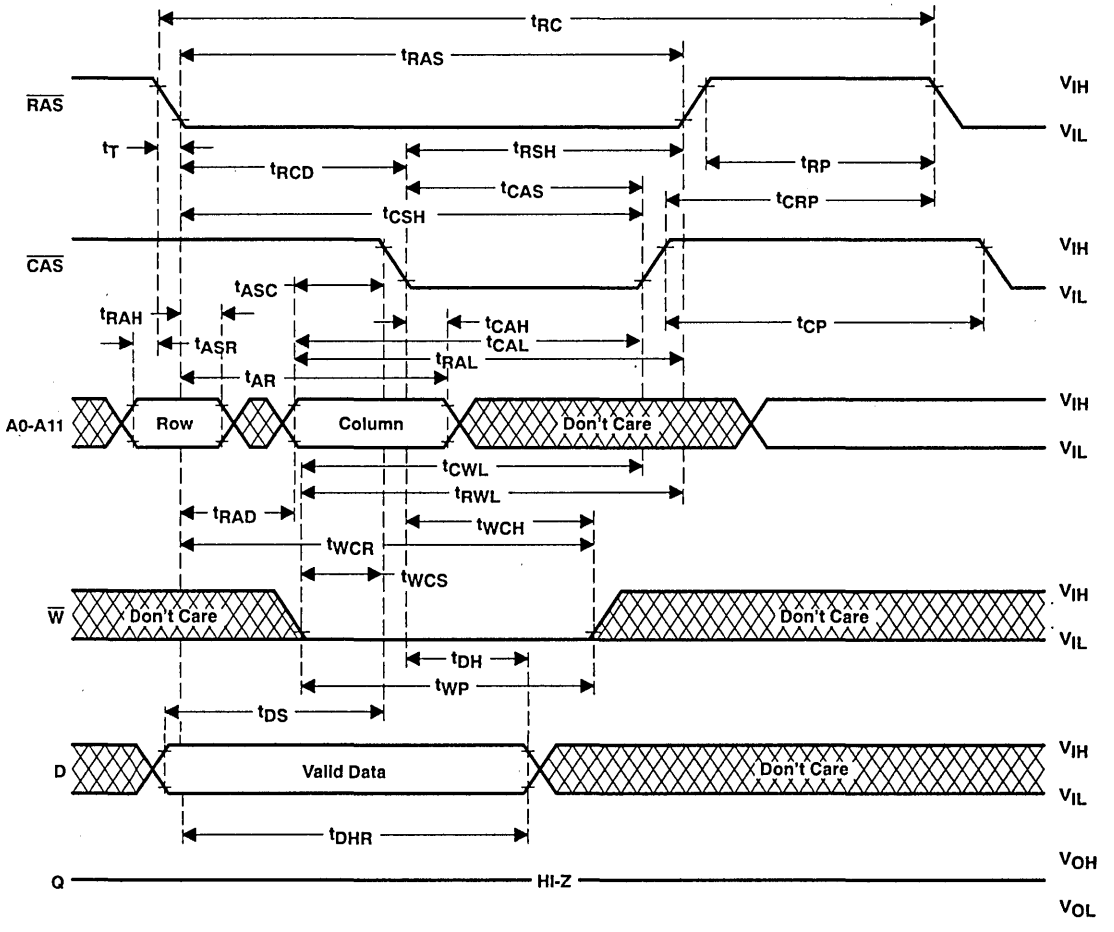


NOTE 15: Output may go from three-state to an invalid data state prior to the specified access time.

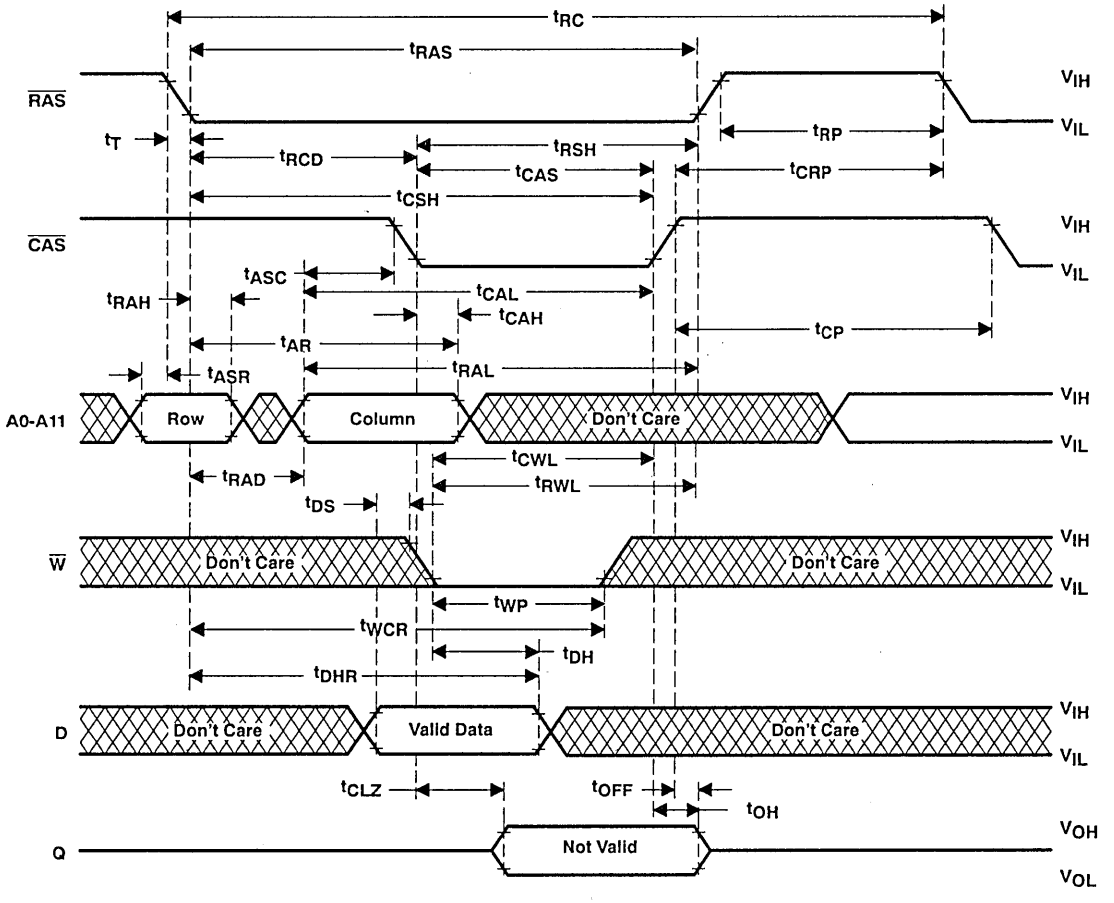
ADVANCE INFORMATION

ADVANCE INFORMATION

early write cycle timing

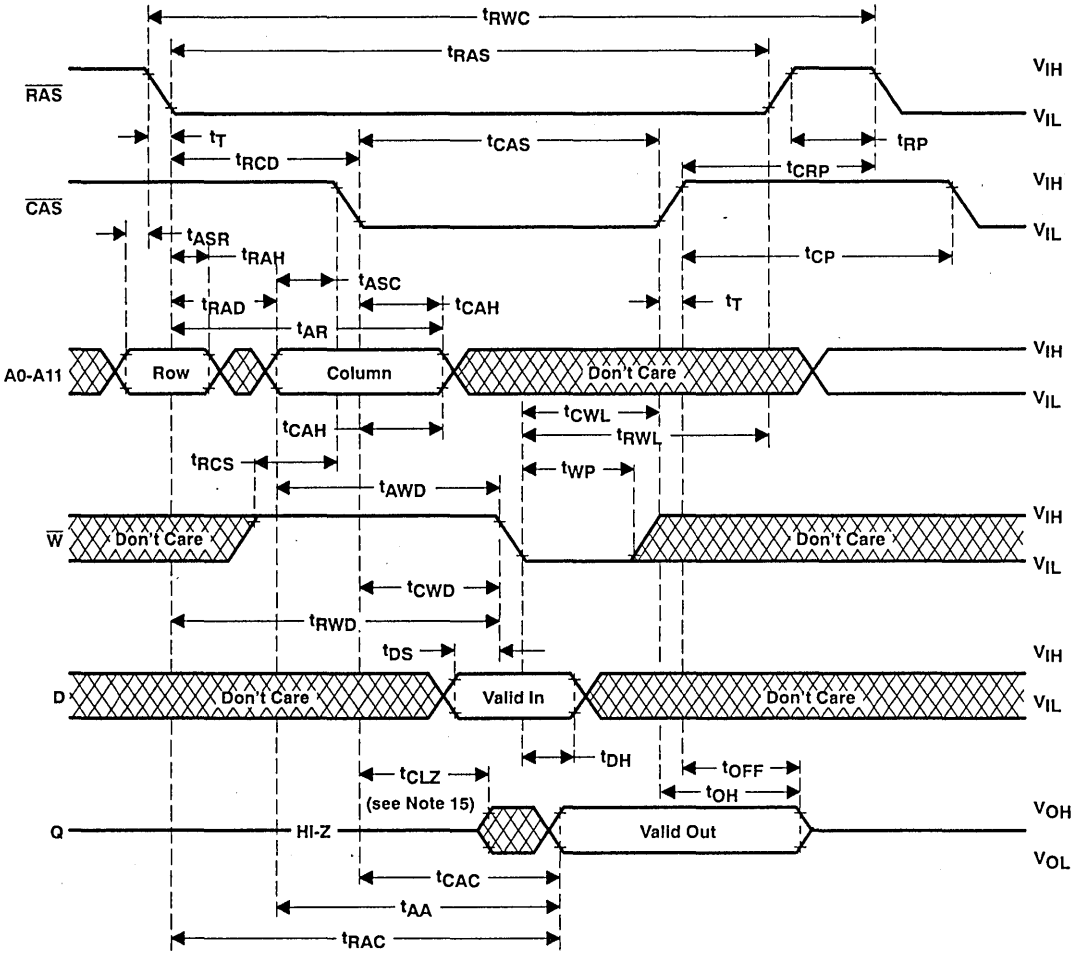


write cycle timing



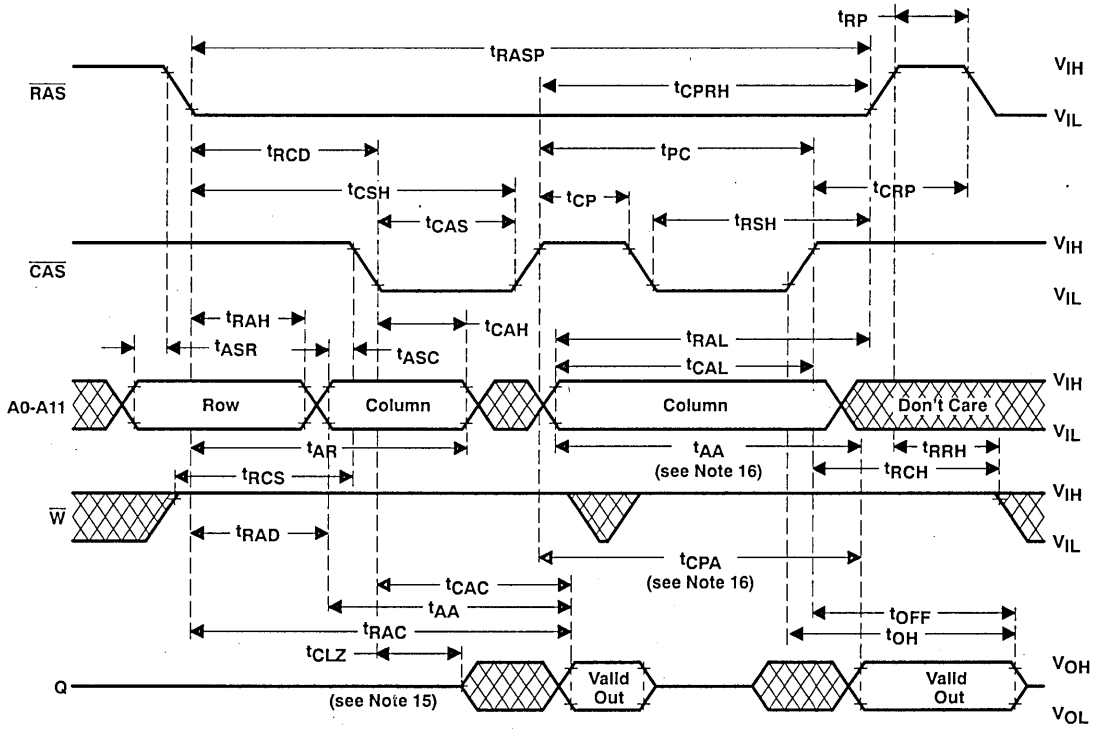
ADVANCE INFORMATION

read-write cycle timing



NOTE 15: Output may go from three-state to an invalid data state prior to the specified access time.

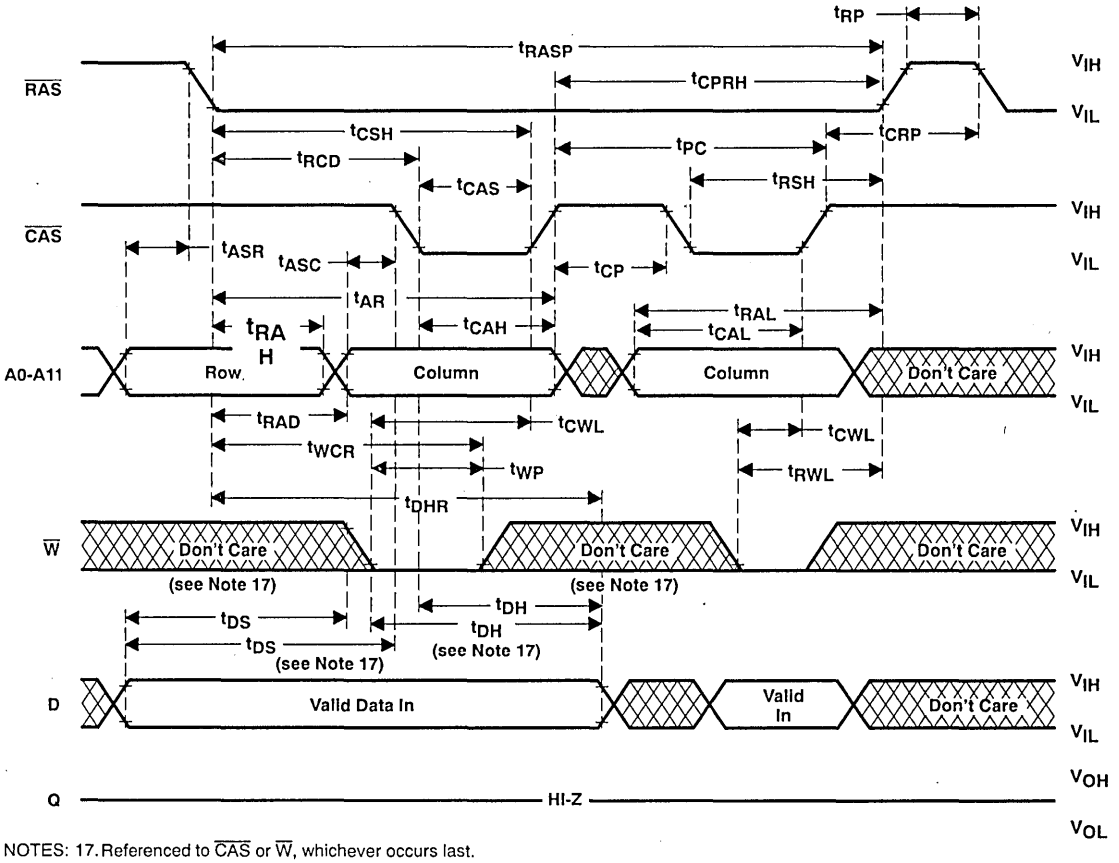
enhanced page-mode read cycle timing



NOTES: 15. Output may go from three-state to an invalid data state prior to the specified access time.
16. Access time is t_{CPA} or t_{AA} dependent.

ADVANCE INFORMATION

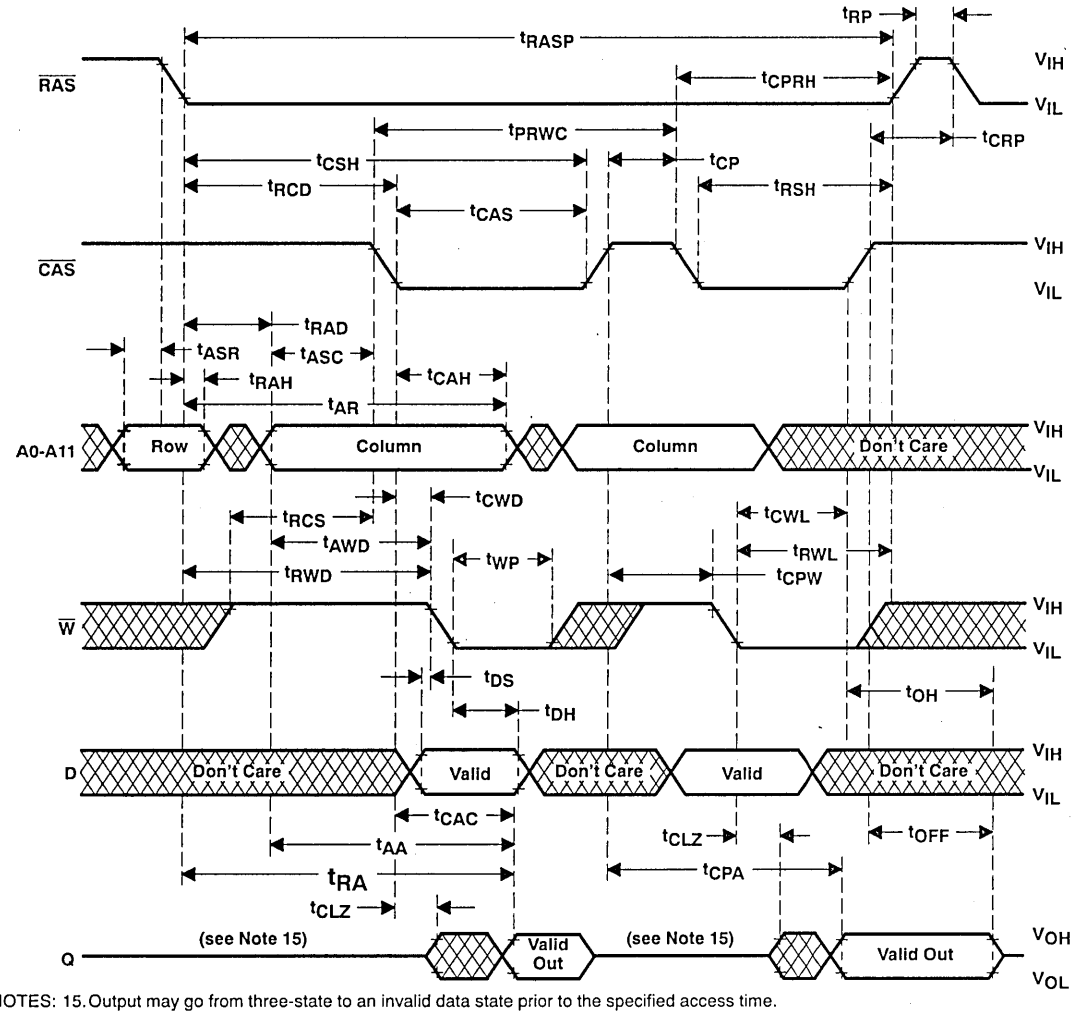
enhanced page-mode write cycle timing



NOTES: 17. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
18. A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

ADVANCE INFORMATION

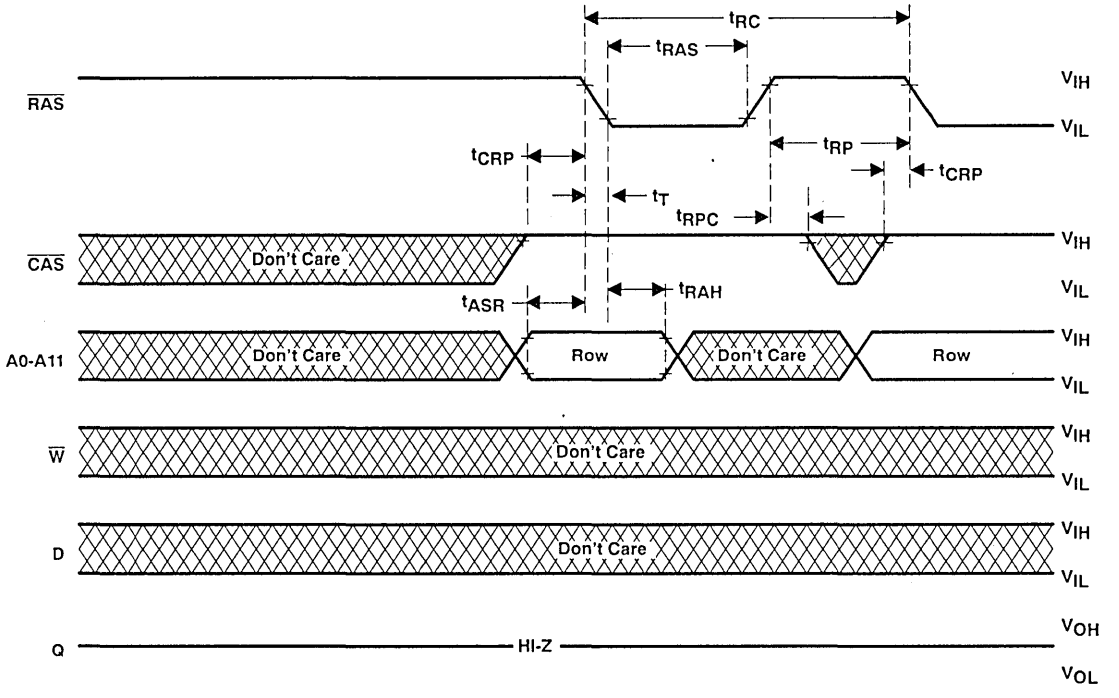
enhanced page-mode read-write cycle timing



NOTES: 15. Output may go from three-state to an invalid data state prior to the specified access time.
19. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

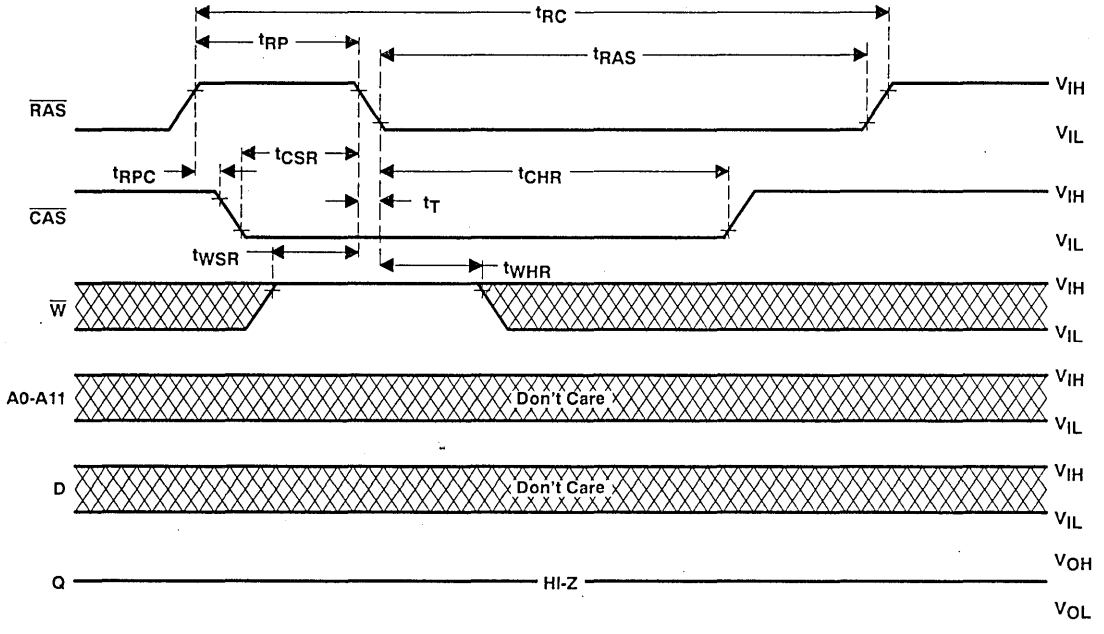
ADVANCE INFORMATION

$\overline{\text{RAS}}$-only refresh timing



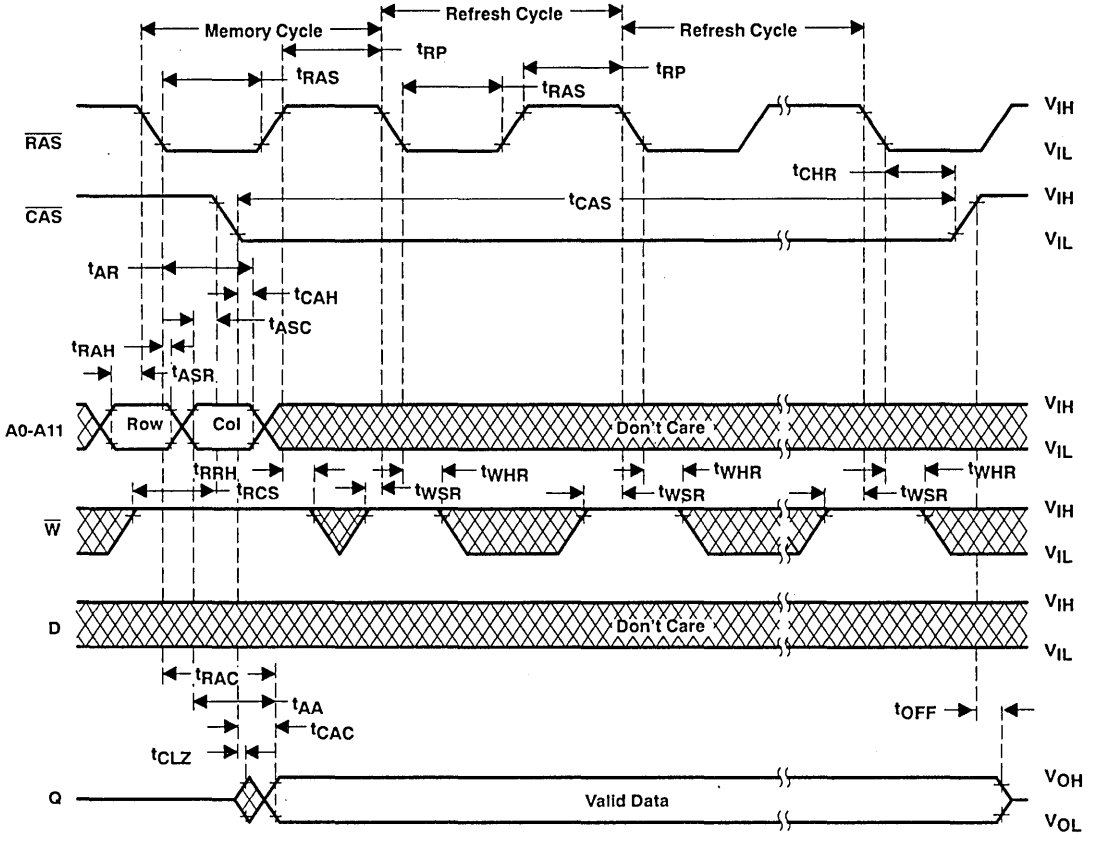
ADVANCE INFORMATION

automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing

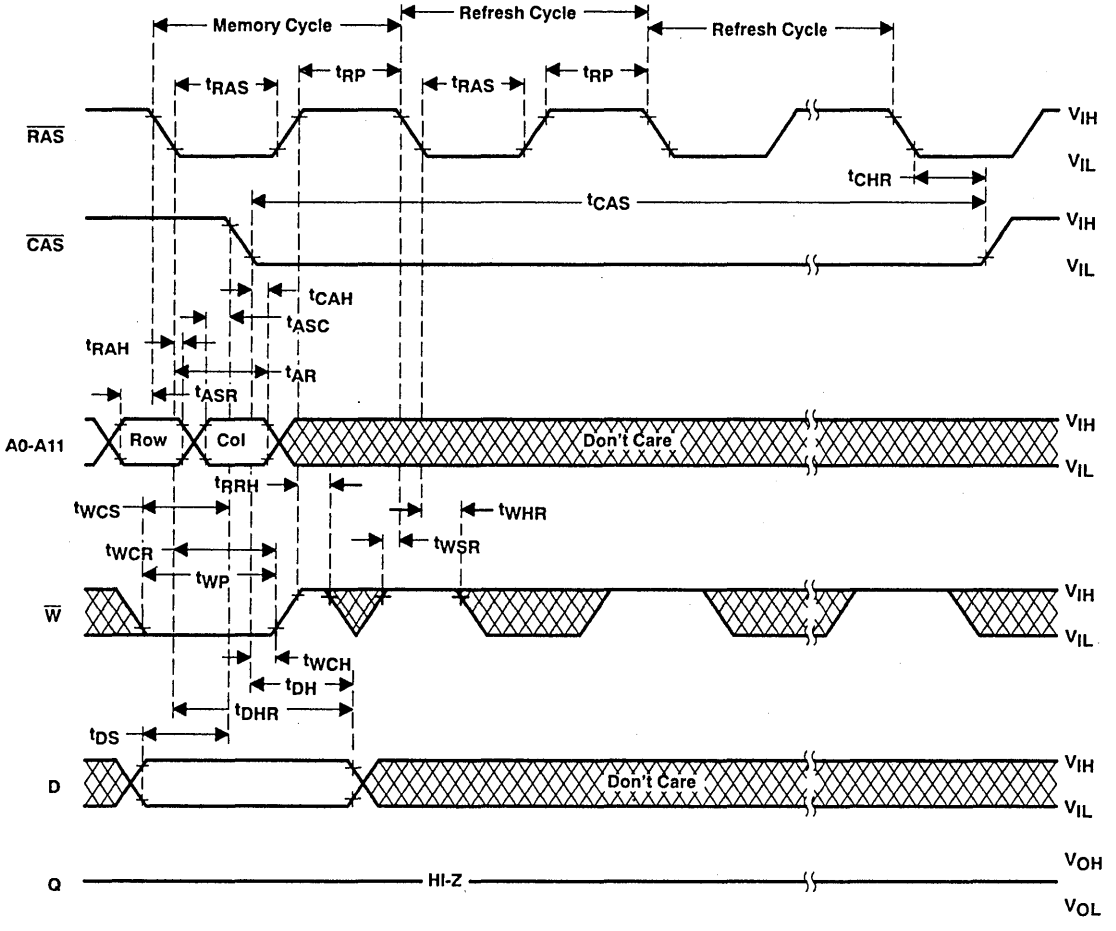


ADVANCE INFORMATION

hidden refresh cycle (read)

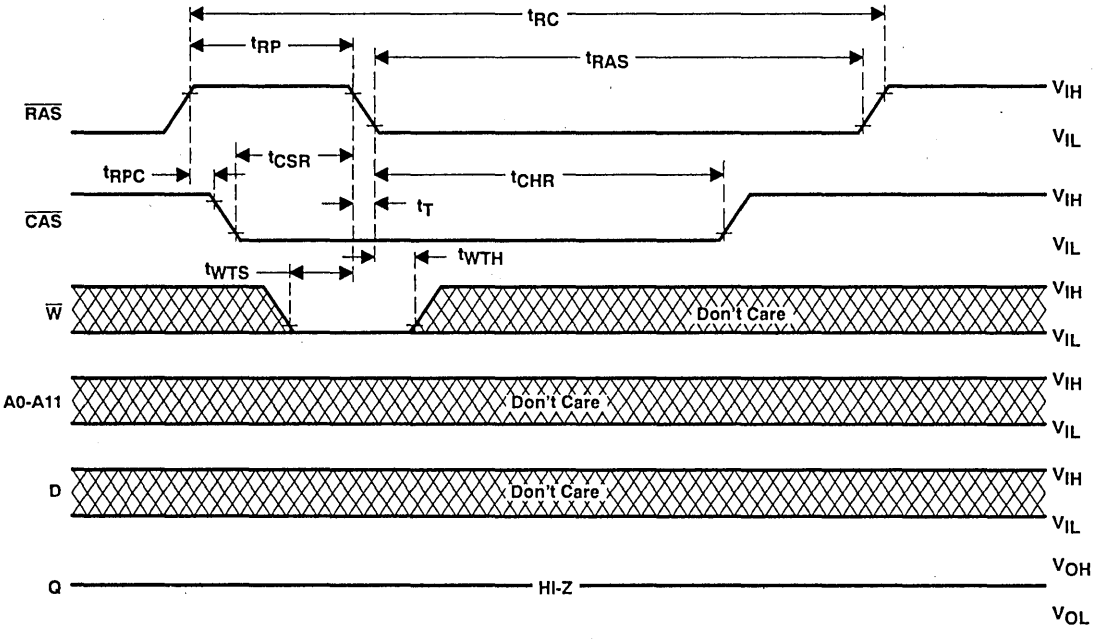


hidden refresh cycle (write)

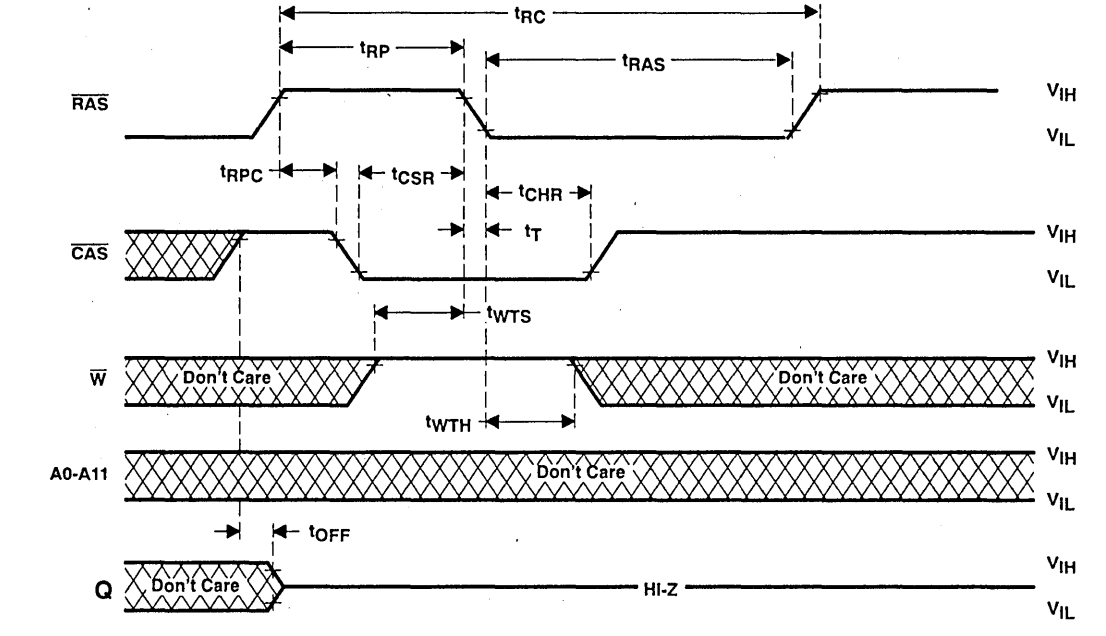


ADVANCE INFORMATION

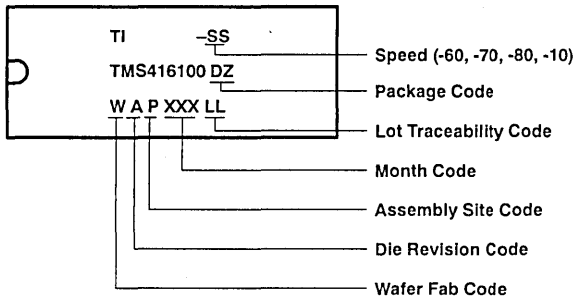
test mode entry cycle



test mode exit cycle ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)



device symbolization

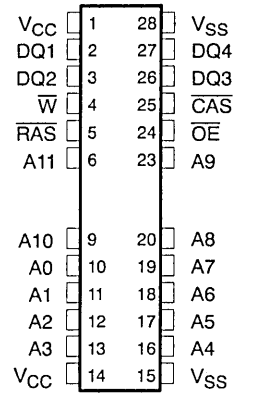


- **Organization . . . 4 194 304 × 4**
- **Single 5-V Power Supply (10% Tolerance)**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
TMS416400-60	60 ns	15 ns	30 ns	110 ns
TMS416400-70	70 ns	18 ns	35 ns	130 ns
TMS416400-80	80 ns	20 ns	40 ns	150 ns
TMS416400-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 4096 Cycles Refresh in 64 ms**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs, Outputs, and Clocks are TTL Compatible**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**
- **This specification is Fully Compatible with the Preliminary 16 Megabit DRAM Specification From Hitachi**

DZ Package
(Top View)



PIN NOMENCLATURE	
A0-A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

ADVANCE INFORMATION

description

The TMS416400 series are high-speed 16 777 216-bit dynamic random-access memories, organized as 4 194 304-bit words by four bits each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns.

All inputs, outputs, and clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS416400 is offered in a 400-mil 28/24-pin surface mount SOJ package (DZ suffix). The package is characterized for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments, Incorporated

operation

enhanced page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$ low width.

The Column Address Buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch, while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output enable.

This feature allows the TMS416400 to operate at a higher data bandwidth than conventional page-mode parts, since retrieval begins as soon as the column address is valid, rather than when $\overline{CAS}$ transitions low. The performance improvement is referred to as "enhanced page mode". Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) and t_{RAS} have been satisfied. In the event that the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0-A11)

Twenty-two address bits are required to decode 1 of 4 194 304 storage cell locations. Twelve row-address bits are set on inputs A0 through A11 and latched onto the chip by the Row Address Strobe $\overline{RAS}$. Ten column-address bits are set on A0 through A9. CA10 and CA11 are not used. Row address A11 is required during a normal access and during $\overline{RAS}$ only refresh as the device requires 4096 refresh cycles. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable $\overline{W}$ input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data-in/data-out (DQ1-DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In the early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fan-out of two Series 74 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change, but retains the state just read.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain for the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every sixty-four milliseconds to retain data. This can be achieved by strobing each of the 4096 rows (A0-A11). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at a high (inactive) level, thus conserving power since the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after the specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden refresh cycle. An internal refresh address provides the refresh address during hidden refresh.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

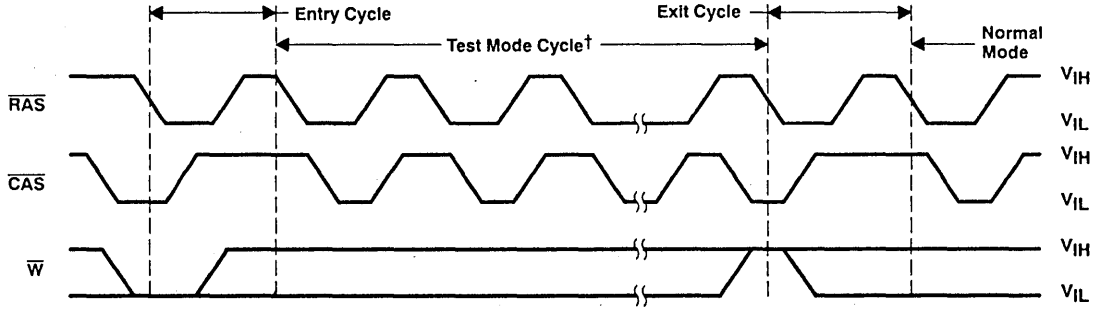
power-up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full VCC level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

The test mode is initiated with a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle while simultaneously holding the $\overline{W}$ input low (WCBR). The initiate cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in test mode, any desired data sequence can be performed on the device. The device exits test mode if a $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, with $\overline{W}$ input held high, or a $\overline{RAS}$-only refresh (ROR) cycle is performed.

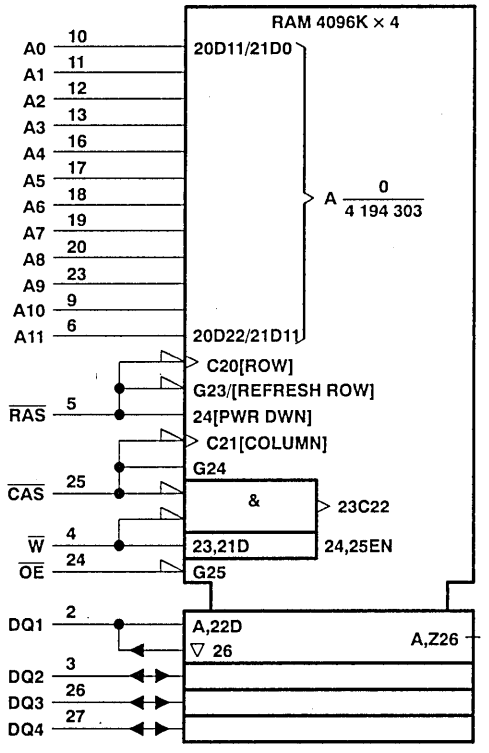
The part is configured as 1024K × 4 × 4 bit device in test mode, where each DQ pin has a separate 4-bit parallel read and write data bus where CA0 and CA1 are ignored. During a read cycle, the 4 internal bits are compared for each DQ pin separately. If the 4 bits agree, the DQ pin will go high, if not, the DQ pin will go low. All 4 bits are written to the state of their respective DQ pin during a parallel write. Thus, each DQ pin is independent of the other and any data pattern desired may be written on each DQ pin. Test time is thus reduced by a factor of 4 for this series.



† The states of $\overline{W}$, Data-in, and Address are defined by the type of cycle used during test mode.

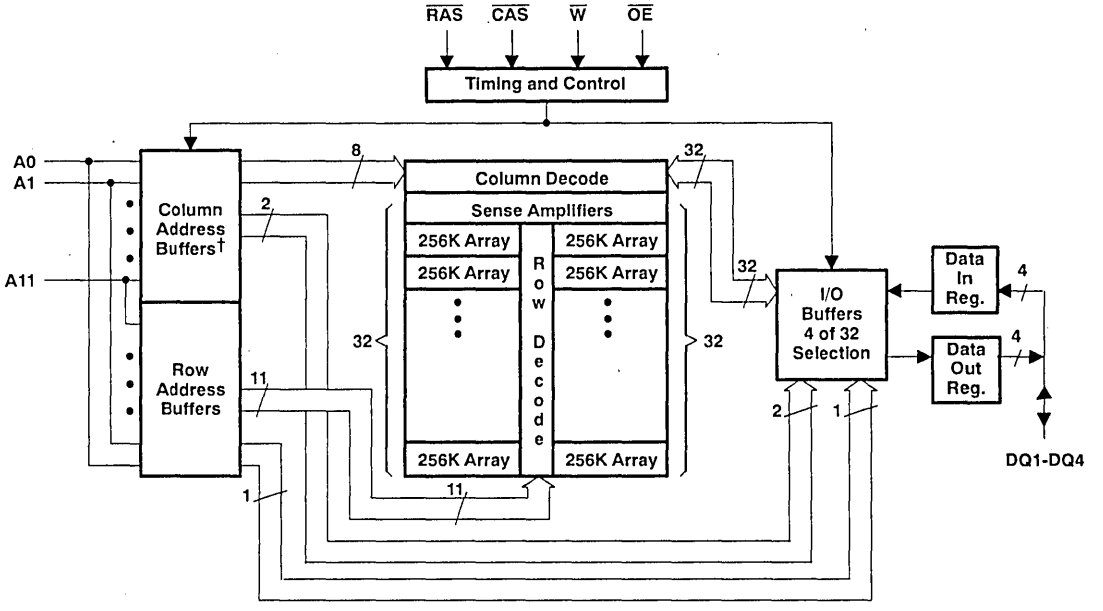
Figure 1. Test Mode Cycle

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



† Column Address 10 and Column Address 11 are not used.

absolute maximum ratings over operating free-air temperature†

Voltage on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: Then algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS416400-60		TMS416400-70		TMS416400-80		TMS416400-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)‡	V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)‡	V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		90		80		70		60	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		1		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR)‡	$\overline{RAS}$ cycling $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		90		80		70		60	mA
I_{CC4}	Average page current (see Note 4)‡	$\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60		50		45	mA
I_{CC7}	Standby current output enable‡	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled		5		5		5		5	mA

‡ Minimum cycle, V_{CC} = 5.5 V.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one adddress change while $\overline{CAS}$ = V_{IH}.

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			10	pF

NOTE 5: V_{CC} equal to 5.0 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS416400-60		TMS416400-70		TMS416400-80		TMS416400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20		25	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OH}	Output disable start of $\overline{CAS}$ high	3		3		3		3		ns
t_{OHO}	Output disable time start of $\overline{OE}$ high	3		3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)	0	15	0	18	0	20	0	25	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS416400-60		TMS416400-70		TMS416400-80		TMS416400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		180		ns
t_{RWC}	Read-write cycle time	155		181		205		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		55		ns
t_{PRWC}	Page-mode read-write cycle time	85		96		105		120		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		0		ns
t_{RCS}	Read setup before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTS}	$\overline{W}$-low setup time (test-mode only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	15		15		15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		75		ns
t_{DH}	Data hold time (see Note 11)	15		15		15		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		75		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	5		5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		75		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		10		ns

Continued next page.

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		TMS416400-60		TMS416400-70		TMS416400-80		TMS416400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	55		63		70		80		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	40		46		50		60		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		25		ns
t_{OED}	$\overline{OE}$ to data delay	15		18		20		25		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	30	15	35	15	40	15	55	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	85		98		110		135		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	55		63		70		80		ns
t_{TAA}	Access time from address (test mode)	35		40		45		50		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		55		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		105		ns
t_{REF}	Refresh time interval		64		64		64		64	ms
t_T	Transition time	3	30	3	30	3	30	3	30	ns

NOTE 14: The maximum value is specified only to guarantee access time.

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

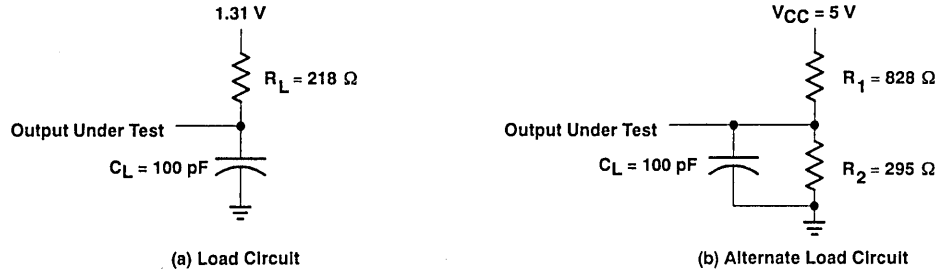
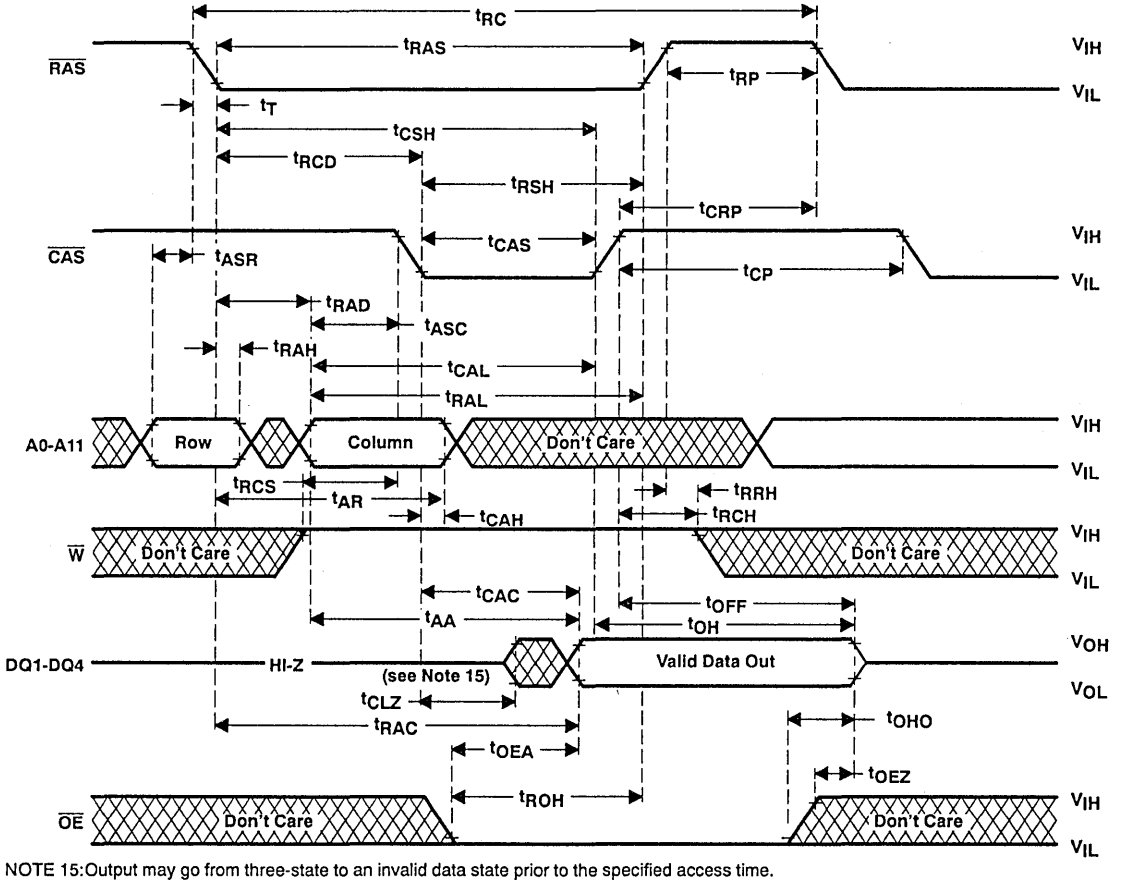


Figure 2. Load Circuits for Timing Parameters

read cycle timing

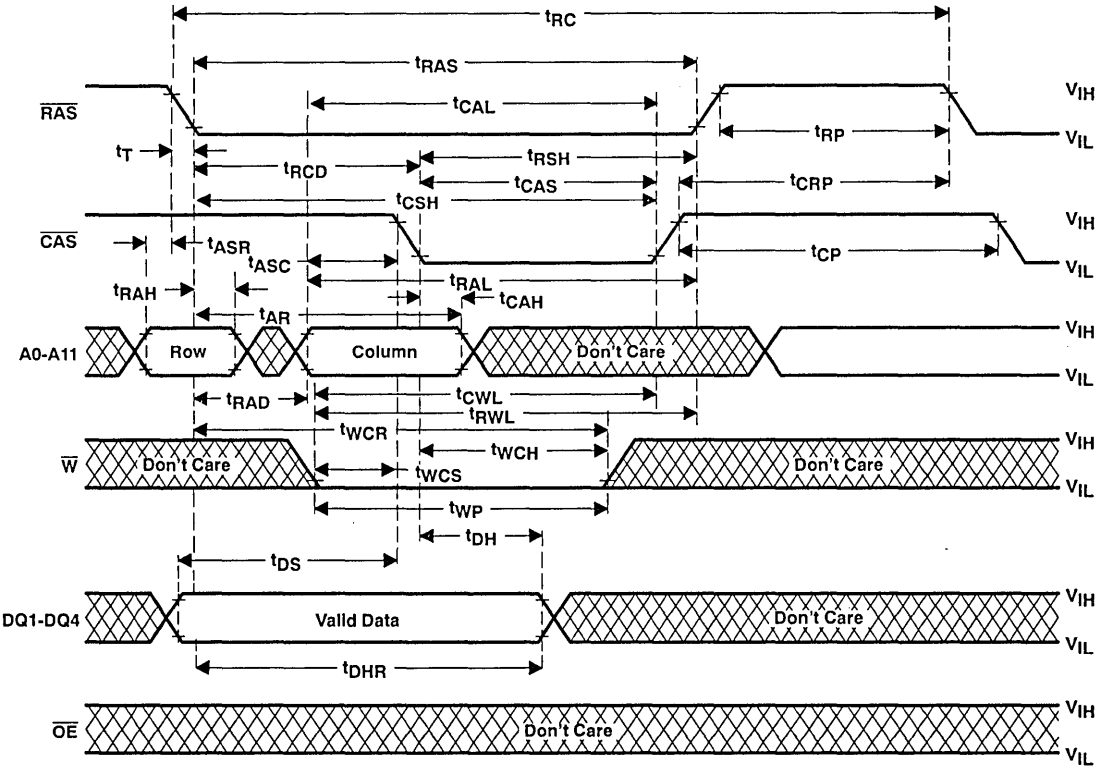


NOTE 15: Output may go from three-state to an invalid data state prior to the specified access time.

ADVANCE INFORMATION

ADVANCE INFORMATION

early write cycle timing



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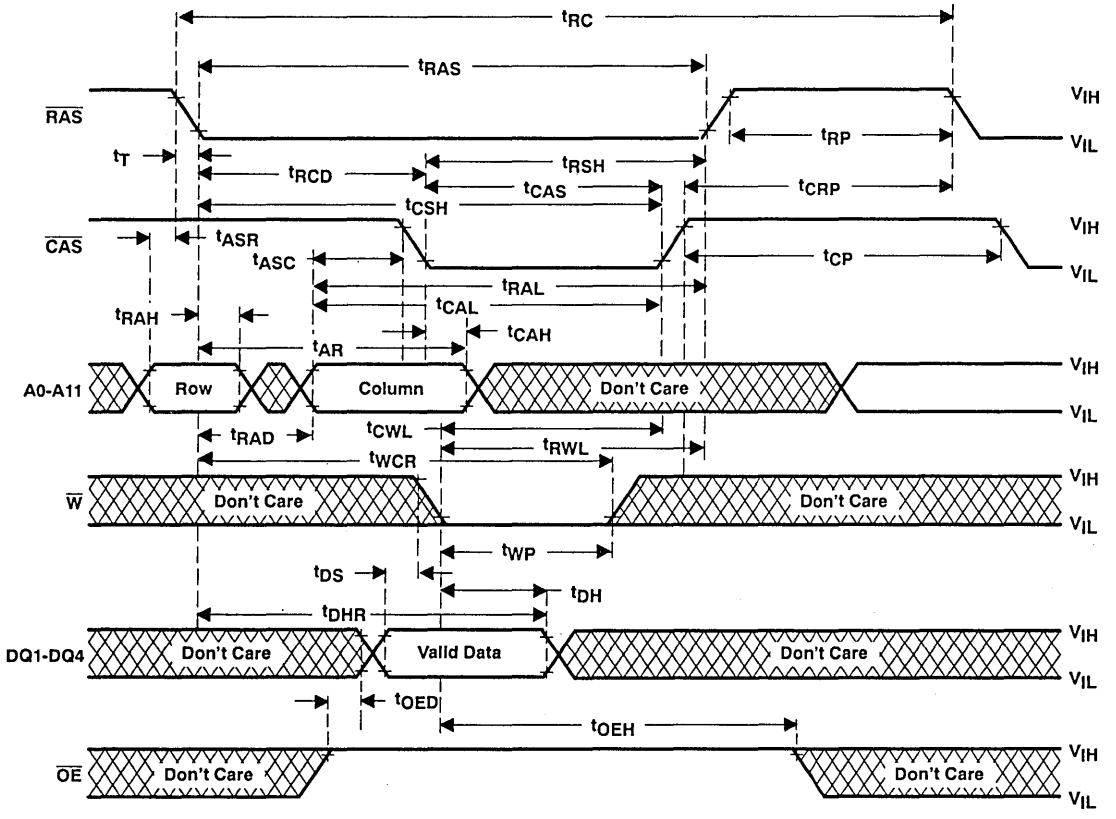
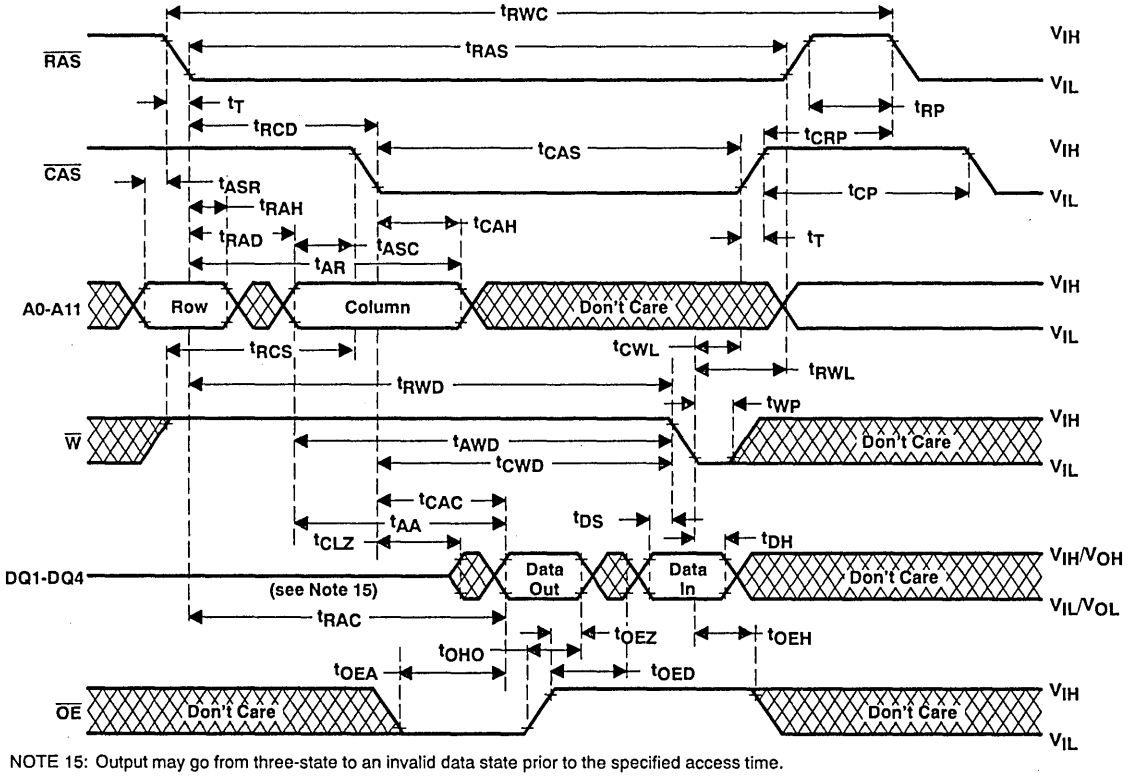
write cycle timing



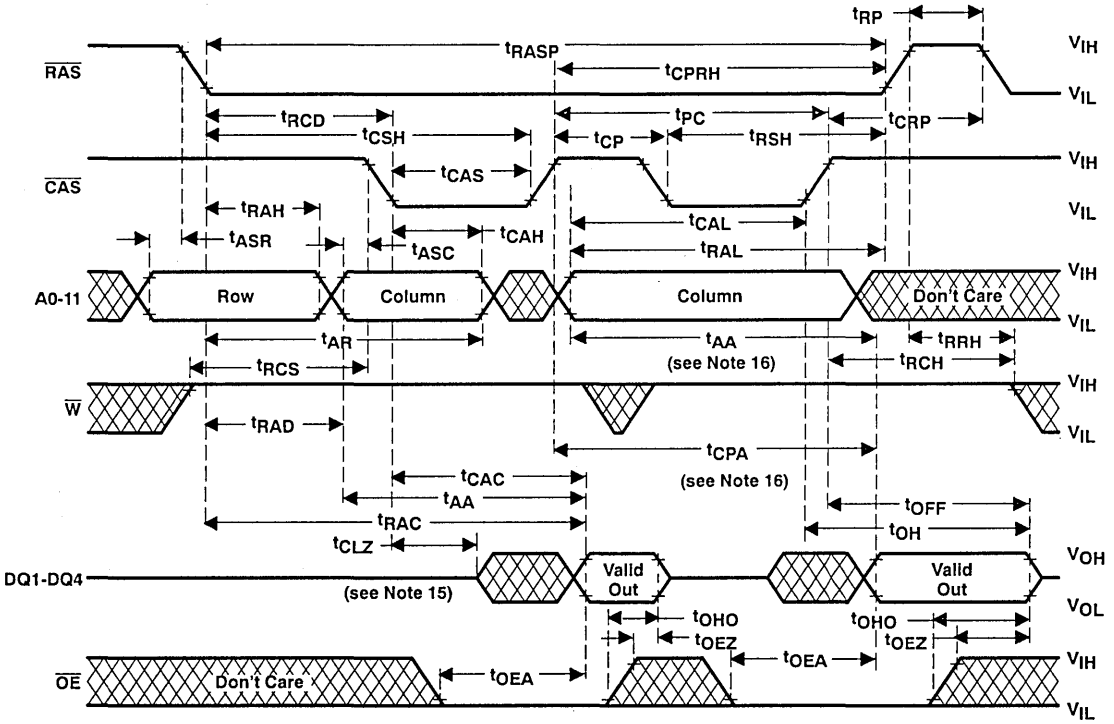
ADVANCE INFORMATION

read-write cycle timing



NOTE 15: Output may go from three-state to an invalid data state prior to the specified access time.

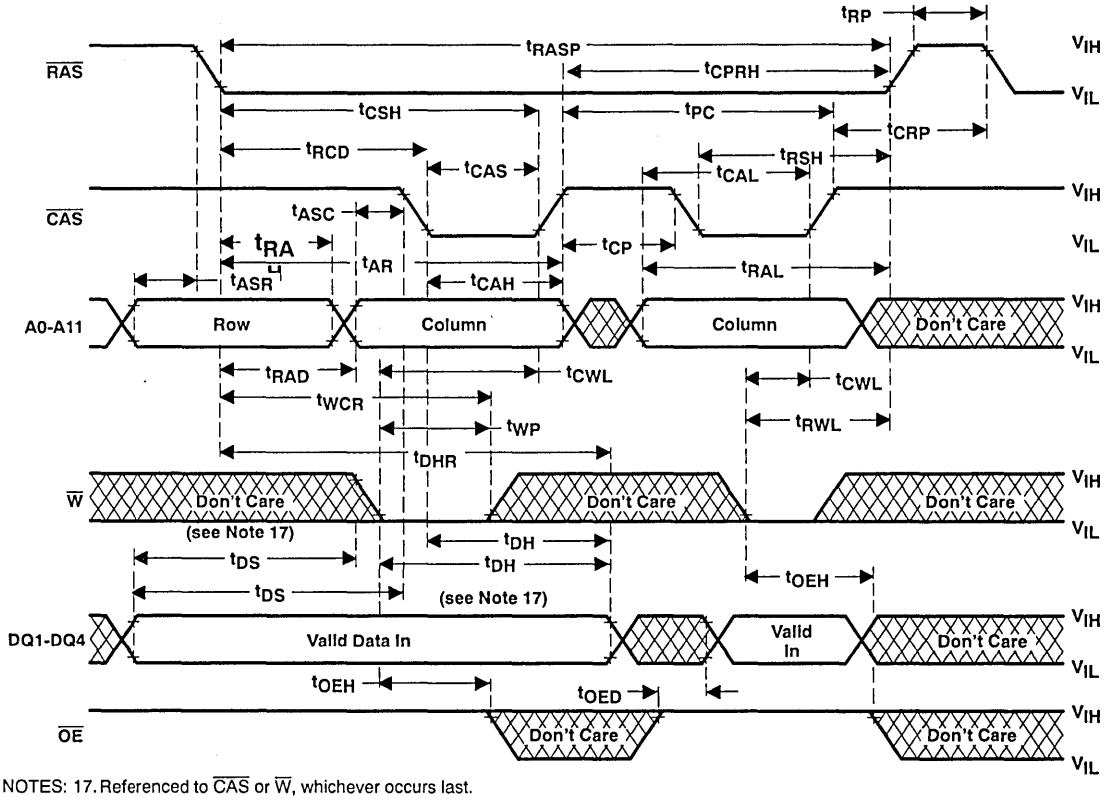
enhanced page-mode read cycle timing



NOTES: 15. Output may go from three-state to an invalid data state prior to the specified access time.
16. Access time is t_{CPA} or t_{AA} dependent.

ADVANCE INFORMATION

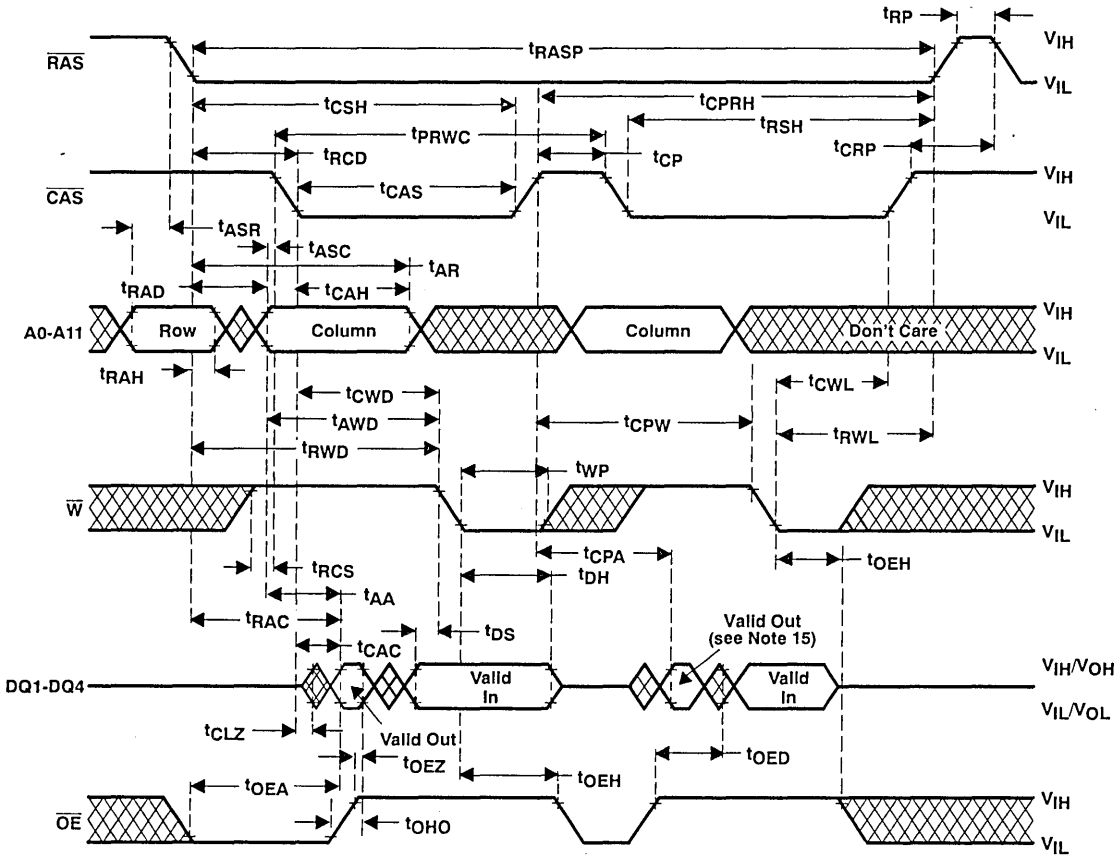
enhanced page-mode write cycle timing



NOTES: 17. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
18. A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

ADVANCE INFORMATION

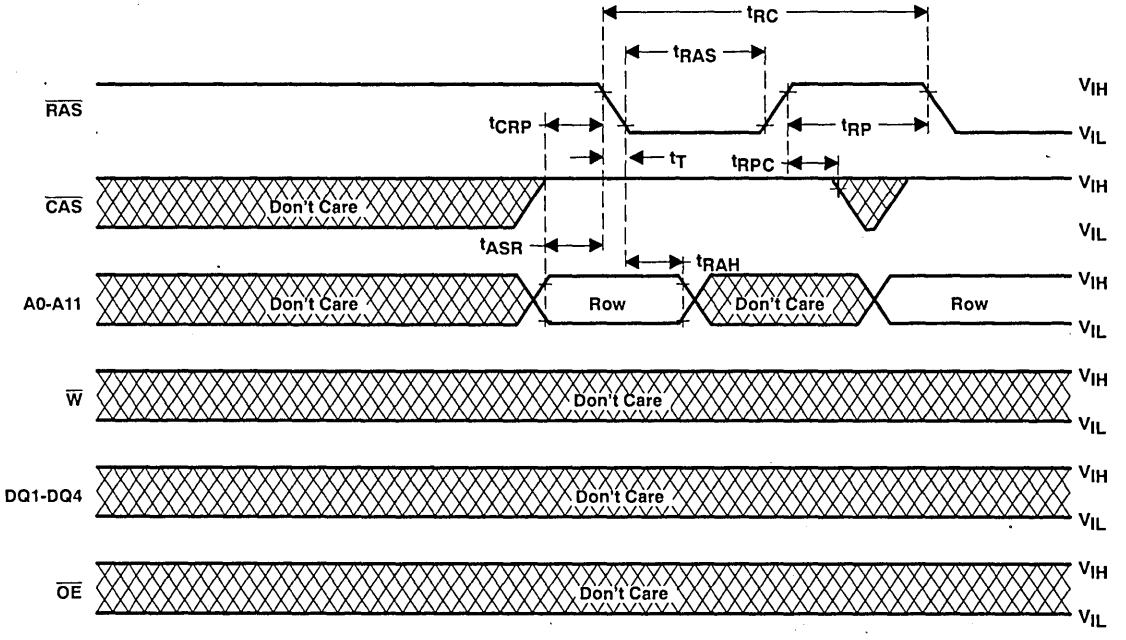
enhanced page-mode read-write cycle timing



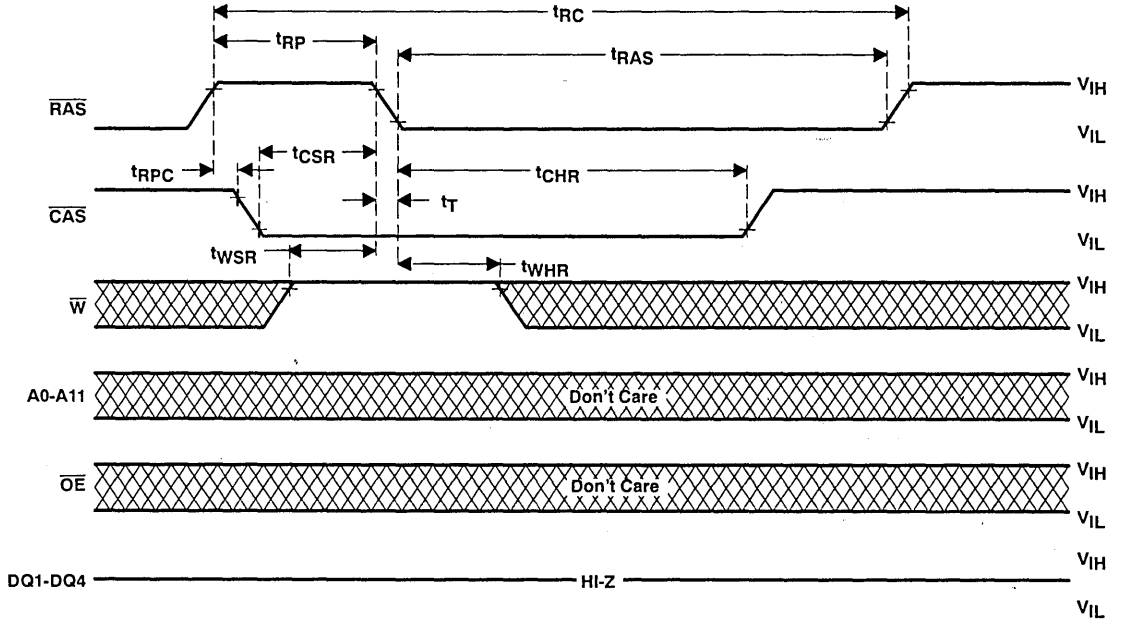
NOTES: 15. Output may go from three-state to an invalid data state prior to the specified access time.
19. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

ADVANCE INFORMATION

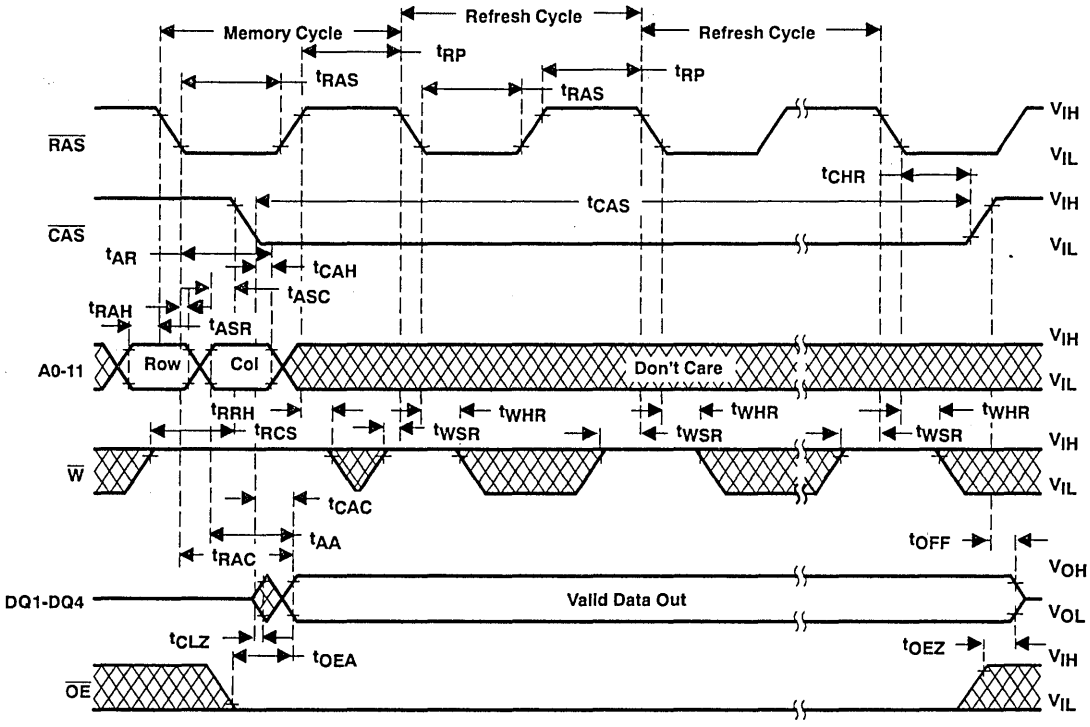
RAS-only refresh timing



automatic (CAS-before-RAS) refresh cycle timing

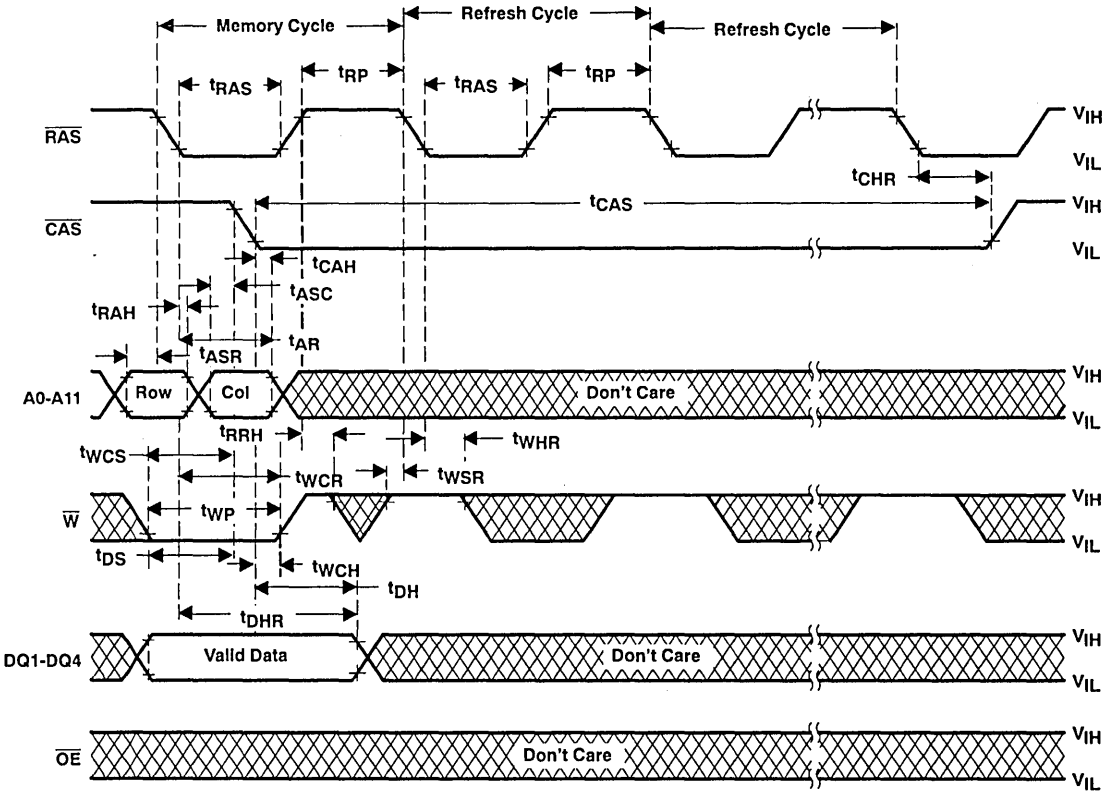


hidden refresh cycle (read)



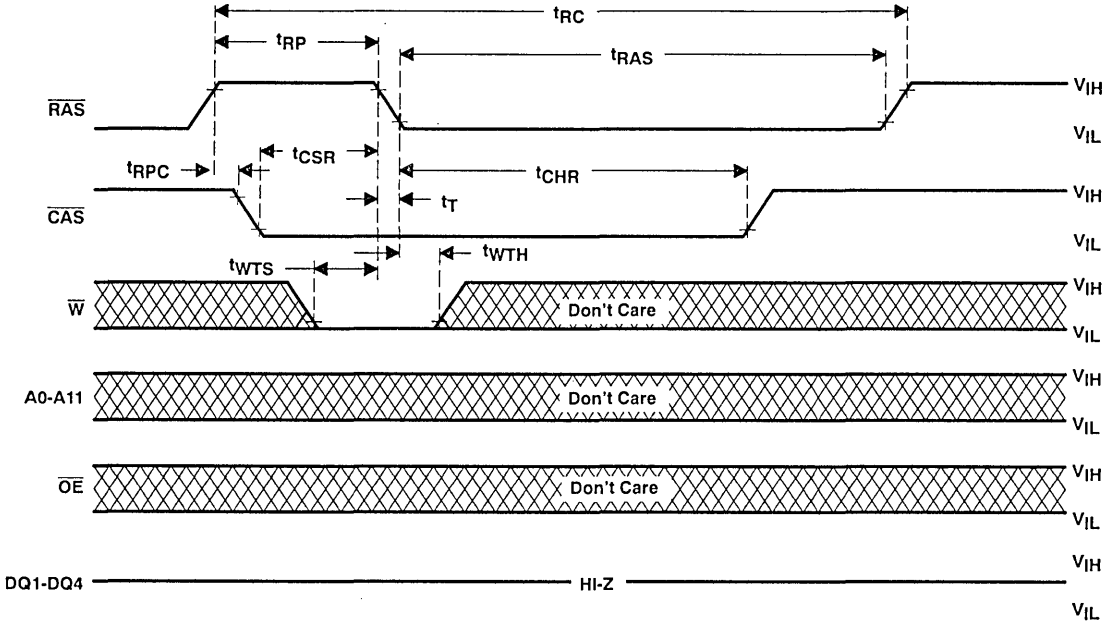
ADVANCE INFORMATION

hidden refresh cycle (write)

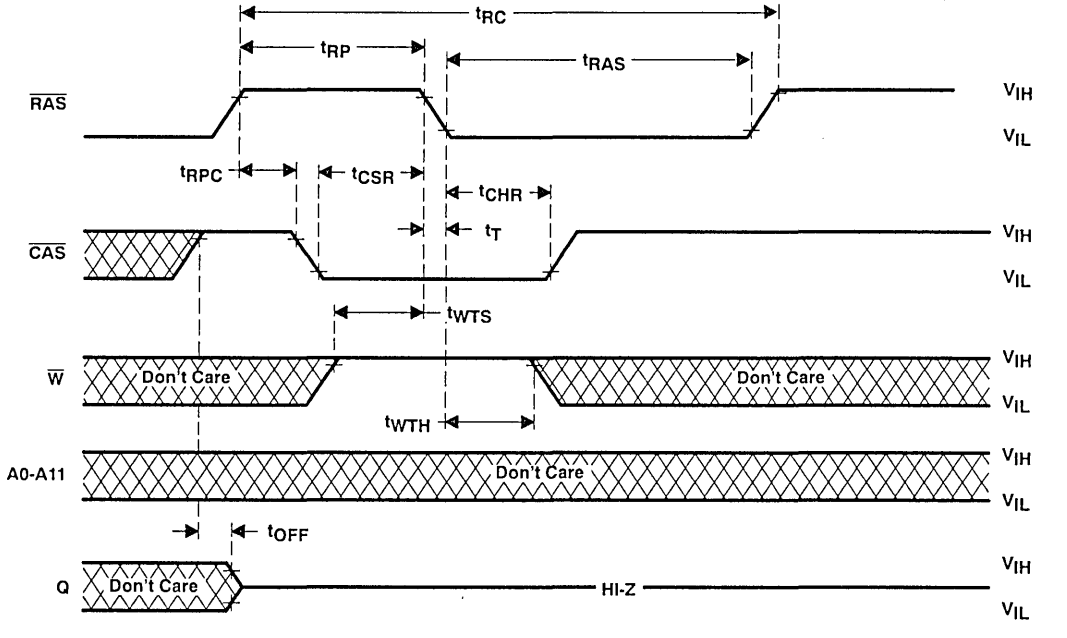


ADVANCE INFORMATION

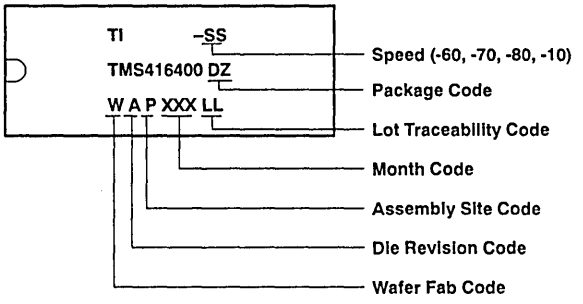
test mode entry cycle



test mode exit cycle (CAS-before-RAS refresh cycle)



device symbolization



REV A — SMMS292B — AUGUST 1989 — REVISED JANUARY 1991

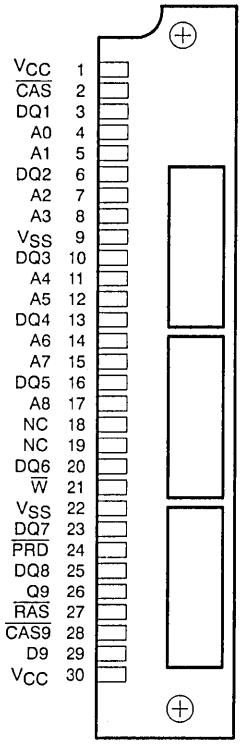
This Data Sheet is Applicable to All TM256GU9Cs Symbolized with Code "D" as Described on Page 6-6.

- **262 144 × 9 Organization**
- **Single 5-V Power Supply**
- **30-Pin Single-In-Line Package (SIP)**
- **Utilizes Three 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJs) Packages**
- **Long Refresh Period . . . 8 ms (512 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Outputs**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)	V_{CC} TOLERANCE
'256GU9C-6	60 ns	15 ns	110 ns	5%
'256GU9C-70	70 ns	18 ns	130 ns	10%
'256GU9C-80	80 ns	20 ns	150 ns	10%
'256GU9C-10	100 ns	25 ns	180 ns	10%

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**

U Single-In-line Package (Top View)



description

The TM256GU9C is a 2304K, dynamic random-access memory module organized as 262 144 × 9 [bit nine is generally used for parity] in a 30-pin single-in-line package.

The TM256GU9C is composed of two TMS44C256, 262 144 × 4-bit dynamic RAMs in 20/26-lead plastic small-outline J-lead (SOJs) packages, and one TMS4C1024, 1 048 576 × 1 bit dynamic RAM in a 20/26-lead plastic small-outline J-lead (SOJ) package .

PIN NOMENCLATURE	
A0-A8	Address Inputs
CAS, CAS9	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
D9	Data In
NC	No Connect
PRD	Presence Detect (V_{SS})
Q9	Data Out
RAS	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground

The TM256GU9C is mounted on a substrate together with three 0.2-μF decoupling capacitors. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. With the elimination of bypass capacitors on the motherboard, reduced P.C. board size, and fewer plated through-holes, a cost savings can be realized.

The TM256GU9C features $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns maximum. All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM256GU9C is characterized for operation from 0°C to 70°C.

operation

The TM256GU9C operates as two TMS44C256s and one TMS4C1024 connected as shown in the functional block diagram. The common I/O features of the TM256GU9C dictates the use of early write cycles to prevent contention on the DQ lines.

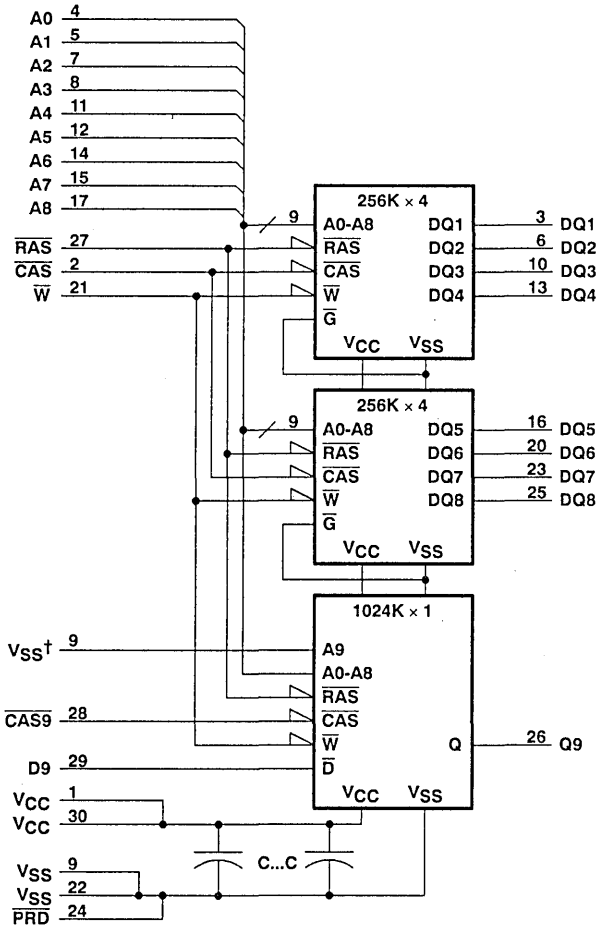
specifications

Refresh period is extended to 8 milliseconds and, during this period, each of the 512 rows must be strobed with $\overline{RAS}$ in order to retain data.

single-in-line package and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness on contact area
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

functional block diagram



† Address pin A9 is connected to V_{SS}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range on any pin (see Note 1)	−1 V to 7 V
Voltage range on V_{CC}	−1 V to 7 V
Short circuit output current	50 mA
Power dissipation	3 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (TM256GU9C-6)	4.75	5	5.25	V
V_{CC}	Supply voltage (TM256GU9C-70/-80/-10)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negataive (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM256GU9C-6		TM256GU9C-70		TM256GU9C-80		TM256GU9C-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10		±10	μA
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.5 V		285		240		225		195	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		6		6		6		6	mA
I_{CC3}	Average refresh current	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high		270		240		210		180	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		210		180		150		135	mA

NOTE 3: V_{CC} equal 5 V ± 0.5 V and the bias on pins under test is 0 V.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		15	pF
$C_{i(DQ)}$	Output capacitance, data inputs/outputs		7	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ input		15	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		15	pF
$C_{i(CAS9)}$	Input capacitance, $\overline{CAS9}$ input		5	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ input		10	pF
$C_{i(D9)}$	Input capactiance, D9 input		5	pF
$C_{o(Q9)}$	Output capacitance, Q9 input		7	pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	TM256GU9C-6		TM256GU9C-70		TM256GU9C-80		TM256GU9C-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}		15		18		20		25	ns
$t_{a(CA)}$	Access time from column-address	t_{CAA}		30		35		40		45	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low	t_{RAC}		60		70		80		100	ns
$t_{a(CP)}$	Access time from column precharge	t_{CAP}		35		40		40		50	ns
$t_{d(CLZ)}$	$\overline{CAS}$ low to output in low Z	t_{CLZ}	0		0		0		0		ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)	t_{OFF}	0	15	0	18	0	20	0	25	ns

NOTE 4: $t_{dis(CH)}$ is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		ALT. SYMBOL	TM256GU9C-6		TM256GU9C-70		TM256GU9C-80		TM256GU9C-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 5)	t_{RC}	110		130		150		180		ns
$t_{c(W)}$	Write cycle time	t_{WC}	110		130		150		180		ns
$t_{c(P)}$	Page-mode read or write cycle time (see Note 6)	t_{PC}	40		45		50		55		ns
$t_{w(CH)}$	Pulse duration $\overline{CAS}$ high	t_{CP}	10		10		10		10		ns
$t_{w(CL)}$	Pulse duration $\overline{CAS}$ low	t_{CAS}	15	10 000	18	10 000	20	10 000	25	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	40		50		60		70		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low	t_{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low	t_{RASP}	60	100 000	70	100 000	80	100 000	100	100 000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		15		15		15		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		0		ns
$t_{su(D)}$	Data setup time before $\overline{CAS}$ low	t_{DS}	0		0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low	t_{WCS}	0		0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	15		18		20		25		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	15		18		20		25		ns
$t_{h(CA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	10		15		15		20		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	10		10		12		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 7)	t_{AR}	50		55		60		70		ns
$t_{h(D)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	10		15		15		20		ns

NOTES: 5. All cycle times assume t_t = 5 ns.
6. To guarantee $t_{c(P)}$ min, $t_{su(CA)}$ should be greater than or equal to $t_{w(CH)}$.
7. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		ALT. SYMBOL	TM256GU9C-6		TM256GU9C-70		TM256GU9C-80		TM256GU9C-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 7)	t_{DHR}	50		55		60		70		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 8)	t_{RCH}	0		0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 8)	t_{RRH}	0		0		0		0		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	15		15		15		20		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 7)	t_{WCR}	50		55		60		70		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	60		70		80		100		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	15		18		20		25		ns
$t_{d(RLCL)}$	Delay time $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	t_{RCD}	20	45	20	52	22	60	25	75	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address (see Note 9)	t_{RAD}	15	30	15	35	17	40	20	55	ns
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	30		35		40		45		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	30		35		40		45		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 10)	t_{CHR}	15		15		20		25		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 10)	t_{CSR}	10		10		10		10		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 10)	t_{RPC}	0		0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	3	50	ns

NOTES: 7. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
8. Either $t_{h(CHrd)}$ or $t_{h(RHrd)}$ must be satisfied for the read cycle.
9. Maximum value specified only to guarantee access time.
10. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

device symbolization

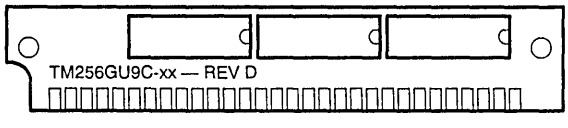


Figure 1. Device Symbolization

This Data Sheet is Applicable to All TM024GAD8s Manufactured With TMS4C1024s Symbolized With Revision "D" and Subsequent Revisions.

- **TM024GAD8 . . . 1 048 576 × 8 Organization**
- **Single 5-V Supply (10% Tolerance)**
- **30-Pin Single-In-Line Package (SIP) — Leadless Module for Use With Sockets**
- **Utilizes Eight 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period . . . 8 ms (512 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Performance of Unmounted RAMs:**

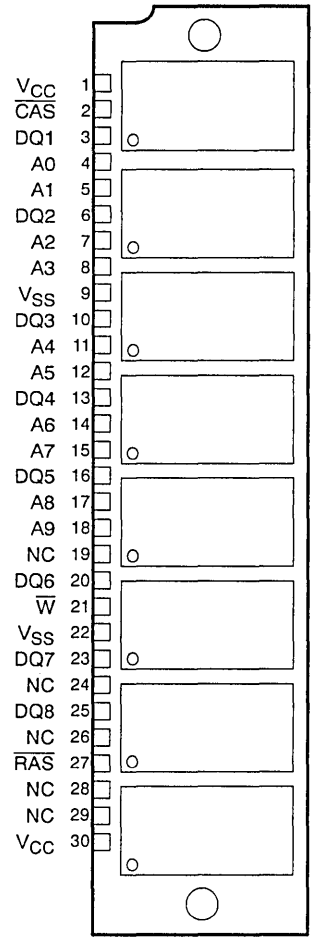
	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)	V_{CC} TOLERANCE
TMS4C1024-6	60 ns	15 ns	110 ns	5%
TMS4C1024-70	70 ns	18 ns	130 ns	10%
TMS4C1024-80	80 ns	20 ns	150 ns	10%
TMS4C1024-10	100 ns	25 ns	180 ns	10%

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free Air Temperature . . . 0°C to 70°C**

description

The TM024GAD8 is a 8192K (dynamic) random-access memory module organized as 1 048 576 × 8 in a 30-pin single-in-line (SIP) module. The TM024GAD8 is composed of eight TMS4C1024DJ, 1 048 576 × 1-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJ), mounted on a substrate together with decoupling capacitors.

AD Single-In-Line Package (Top View)



PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

The TMS4C1024DJ is described in its data sheet and is fully electrically tested and processed according to TI MIL-STD-883B flows (as amended for commercial applications) prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed.

The TM024GAD8 SIP is available in the AD single-sided, leadless module for use with sockets.

The TM024GAD8 SIP is rated for operation from 0°C to 70°C.

operation

The TM024GAD8 operates as eight TMS4C1024DJs connected as shown in the functional block diagram. Refer to the TMS4C1024 data sheet for details of its operation. The common I/O feature of the TM024GAD8 dictates the use of early write cycles to prevent contention on D and Q.

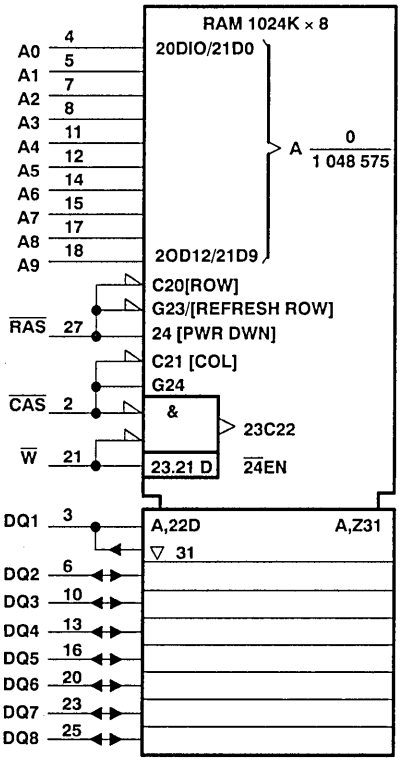
specifications

For TMS4C1024DJ electrical specifications, refer to the TMS4C1024 data sheet.

single-in-line package and components

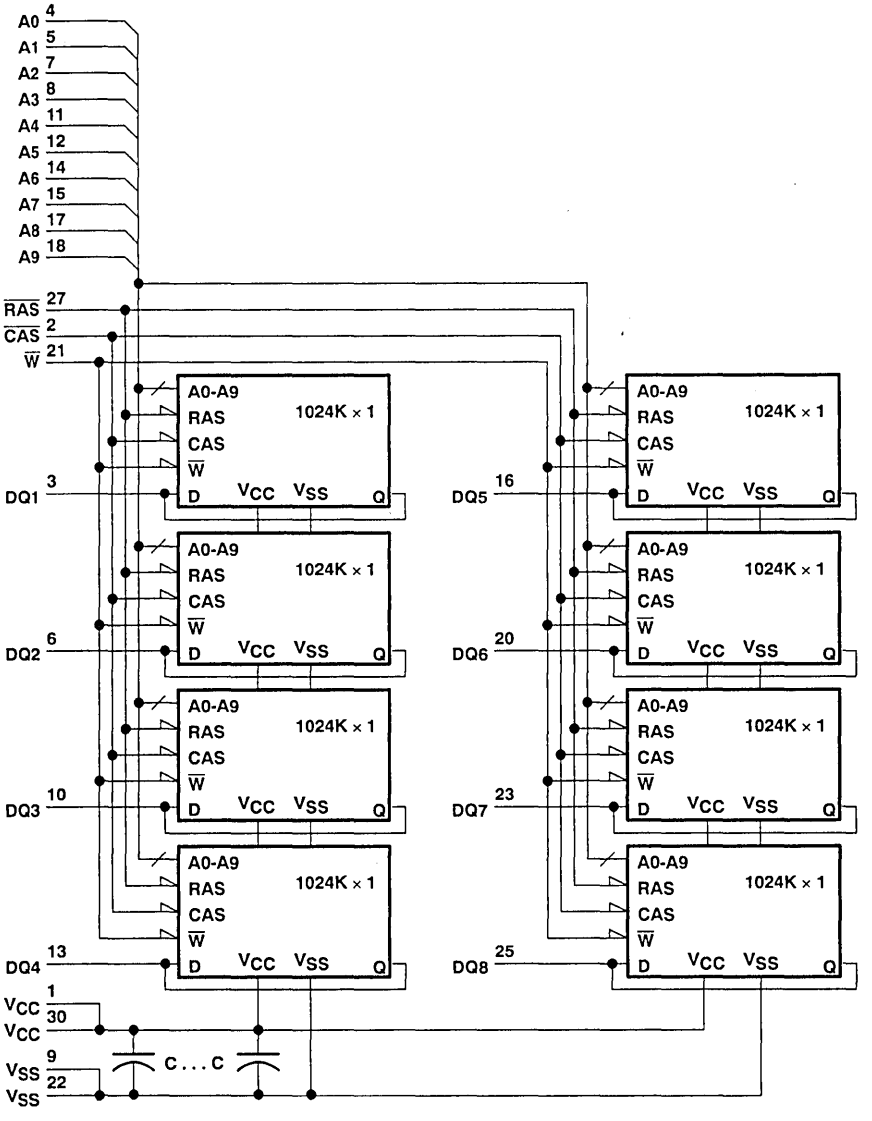
PC substrate: 1,27 (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate (or coat) on top of copper

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 9-1084 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 8 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (TM024GAD8-6)	4.75	5	5.25	V
V_{CC}	Supply voltage (TM024GAD8-70/-80/-10)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

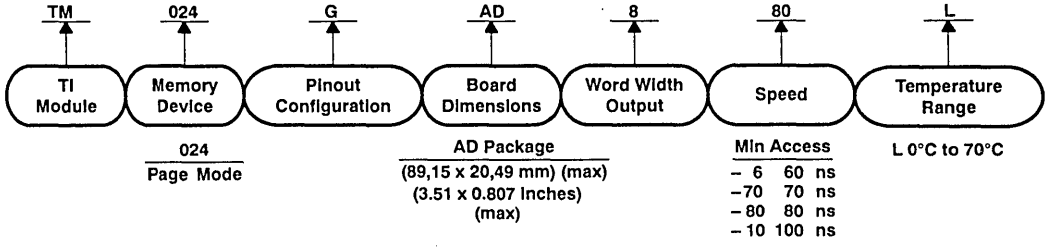
PARAMETER		TEST CONDITIONS	TM024GAD8-6		TM024GAD8-70		TM024GAD8-80		TM024GAD8-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.5 V		760		640		600		520	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		16		16		16		16	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		720		640		560		480	mA
I_{CC4}	Average page current	$t_{c(P)}$=minimum, V_{CC}=5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		560		480		400		360	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		40	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		40	pF
$C_{i(W)}$	Input capacitance, write-enable input		40	pF
C_o	Output capacitance (DQ1-DQ8)		10	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

TI single-in-line package nomenclature



SMMS181 — JANUARY 1991

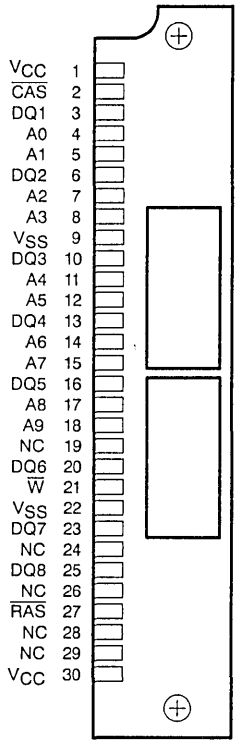
This Data Sheet is Applicable to All TM124GU8As Symbolized with Revision "B" and Subsequent Revisions as Described on Page 6-19.

- **1 048 576 × 8 Organization**
- **Single 5-V Power Supply**
- **30-Pin Single-In-Line Package (SIP)**
- **TM124GU8A Utilizes Two 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **Long Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Outputs**
- **Performance Ranges:**

	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)	V_{CC} TOLERANCE
'124GU8A-6	60 ns	30 ns	110 ns	±5%
'124GU8A-70	70 ns	35 ns	130 ns	±10%
'124GU8A-80	80 ns	40 ns	150 ns	±10%
'124GU8A-10	100 ns	45 ns	180 ns	±10%

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**

U Single-In-Line Package (Top View)



PIN NOMENCLATURE	
A0-A9	Address Inputs
CAS	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Internal Connect
RAS	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TM124GU8A is a dynamic random-access memory module organized as 1 048 576 × 8 in a 30-pin single-in-line package.

The TM124GU8A is composed of two TMS44400, 1 048 576 × 4 bit dynamic RAMs in 20/26-lead plastic small-outline J-lead packages (SOJs).

The TM124GU8A is mounted on a substrate with decoupling capacitors. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated through-holes, a cost savings can be realized.

The TM124GU8A features $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns. All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM124GU8A is characterized for operation from 0°C to 70°C.

operation

The TM124GU8A operates as two TMS44400s connected as shown in the functional block diagram. The common I/O features of the TM124GU8A dictates the use of early write cycles to prevent contention on the DQ lines.

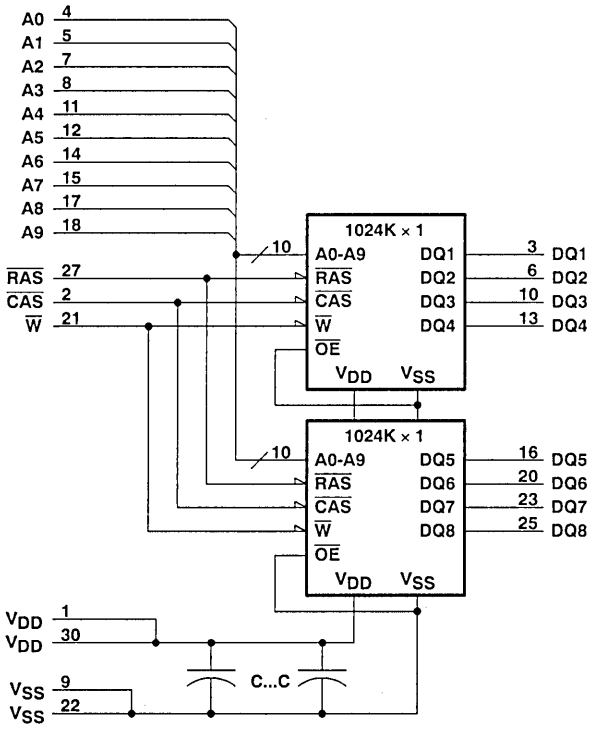
specifications

Refresh period is extended to 16 milliseconds and, during this period, each of the 1024 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

single-in-line package and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness on contact area
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1)	– 1 V to 7 V
Voltage range on V_{CC}	– 1 V to 7 V
Short circuit output current	50 mA
Power dissipation	2 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	– 55°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (TM124GU8A-6)	4.75	5	5.25	V
V_{CC}	Supply voltage (TM124GU8A-70/-80/-10)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM124GU8A-6		TM124GU8A-70		TM124GU8A-80		TM124GU8A-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10		±10	μA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		190		170		150		130	mA
I_{CC2}	Standby Current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		4		4		4		4	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} − 0.2 V (CMOS)		2		2		2		2	mA
I_{CC3}	Average refresh current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high		190		170		150		130	mA
I_{CC4}	Average page current (see Note 4)	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		140		120		100		80	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measrued with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		10	pF
$C_{i(DQ)}$	Input capacitance, data inputs/outputs		7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		14	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		14	pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124GU8A-6		'124GU8A-70		'124GU8A-80		'124GU8A-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 5)	0	15	0	18	0	20	0	25	ns

NOTE 5: t_{OFF} is specified when the otuput is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124GU8A-6		'124GU8A-70		'124GU8A-80		'124GU8A-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note6)	110		130		150		180		ns
t_{PC}	Page-mode read or write cycle time (see Note 7)	40		45		50		55		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTS}	$\overline{W}$-low setup time (test mode only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 8)	50		55		60		75		ns
t_{DH}	Data hold time	10		15		15		20		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 8)	50		55		60		75		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 9)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 9)	0		0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		75		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		10		ns

Continued next page.

NOTES: 6. All cycle times assume t_T = 5 ns.
7. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
8. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'124GU8A-6		'124GU8A-70		'124GU8A-80		'124GU8A-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 10)	15	30	15	35	15	40	20	50	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	25	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{TAA}	Access time from address (test mode)	35		40		45		50		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		55		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		105		ns
t_{REF}	Refresh time interval		16		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	2	50	ns

NOTE 10: The maximum value is specified only to guarantee access time.

device symbolization

The specifications contained in this data sheet are applicable to all TM124GU8As symbolized as shown in Figure 1. Please note that the location of the part number may vary.

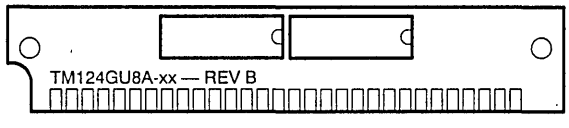


Figure 1. Device Symbolization

SMMS232 — JANUARY 1991

This Data Sheet is Applicable to All TM256BBK32s and TM512CBK32s Symbolized with Revision "B" and Subsequent Revisions as Described on Page 6-30.

- **TM256BBK32 . . . 262 144 × 32 Organization**
- **TM512CBK32 . . . 524 288 × 32 Organization**
- **Single 5-V Power Supply**
- **72-pin Single-In-Line Package (SIP) – Leadless Module for Use with Sockets**
- **TM256BBK32 . . . Utilizes Eight 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **TM512CBK32 . . . Utilizes Sixteen 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **Distributed Refresh Period . . . 8 ms (512 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines, in Four Blocks**
- **Performance Ranges:**

	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	READ OR WRITE CYCLE (MIN)	V_{CC} TOLERANCE
'256BBK32-6	60 ns	15 ns	110 ns	5%
'256BBK32-70	70 ns	18 ns	130 ns	10%
'256BBK32-80	80 ns	20 ns	150 ns	10%
'256BBK32-10	100 ns	25 ns	180 ns	10%
'512CBK32-6	60 ns	15 ns	110 ns	5%
'512CBK32-70	70 ns	18 ns	130 ns	10%
'512CBK32-80	80 ns	20 ns	150 ns	10%
'512CBK32-10	100 ns	25 ns	180 ns	10%

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**

description

TM256BBK32

The TM256BBK32 is a 8388K dynamic random-access memory module organized as four times 262 144 × 8 in a 72-pin single-in-line package (SIP).

The SIP is composed of eight TMS44C256DJ, 262 144 × 4-bit dynamic RAMs, each in a 20/26-lead plastic small-outline J-lead package (SOJs), mounted on a substrate together with decoupling capacitors. Each TMS44C256DJ is described in the TMS44C256 data sheet.

The TM256BBK32 SIP is available in the single-sided BK leadless module for use with sockets.

The TM256BBK32 SIP features $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns. This device is characterized for operation from 0°C to 70°C.

TM512CBK32

The TM512CBK32 is a 16 777K dynamic random-access memory module organized as four times 524 288 × 8 in a 72-pin single-in-line package (SIP).

The SIP is composed of sixteen TMS44C256DJ, 262 144 × 4-bit dynamic RAMs, each in a 20/26-lead plastic small-outline J-lead package (SOJs), mounted on a substrate with decoupling capacitors. Each TMS44C256DJ is described in the TMS44C256 data sheet.

The TM512CBK32 SIP is available in a double-sided BK leadless module for use with sockets.

The TM512CBK32 SIP features $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns. This device is rated for operation from 0°C to 70°C.

operation

TM256BBK32

The TM256BBK32 operates as eight TMS44C256DJs connected as shown in the functional block diagram. Refer to the TMS44C256 data sheet for details of operation.

The common I/O feature of the TM256BBK32 dictates the use of early write cycles to prevent contention on D and Q.

TM512CBK32

The TM512CBK32 operates as sixteen TMS44C256DJs connected as shown in the functional block diagram. Refer to the TMS44C256 data sheets for details of operation.

The common I/O feature of the TM512CBK32 dictates the use of early write cycles to prevent contention on D and Q.

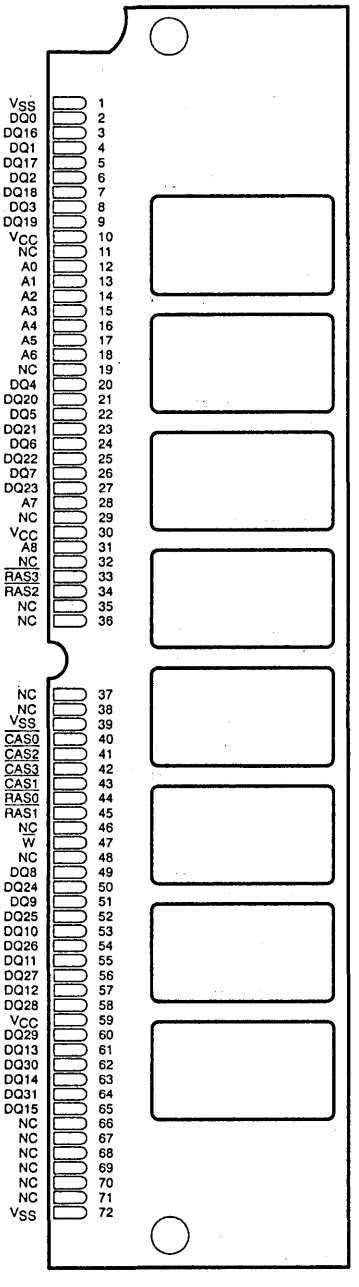
specifications

Refresh period is extended to 8 milliseconds and, during this period, each of the 512 rows must be strobed with $\overline{RAS}$ in order to retain data. Address line A8 must be used as most significant refresh address line (lowest frequency) to assure correct refresh for the TMS44C256. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

single-in-line package and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness on contact area
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and gold plate on top of copper

BK Single-In-line Package† (Top View)



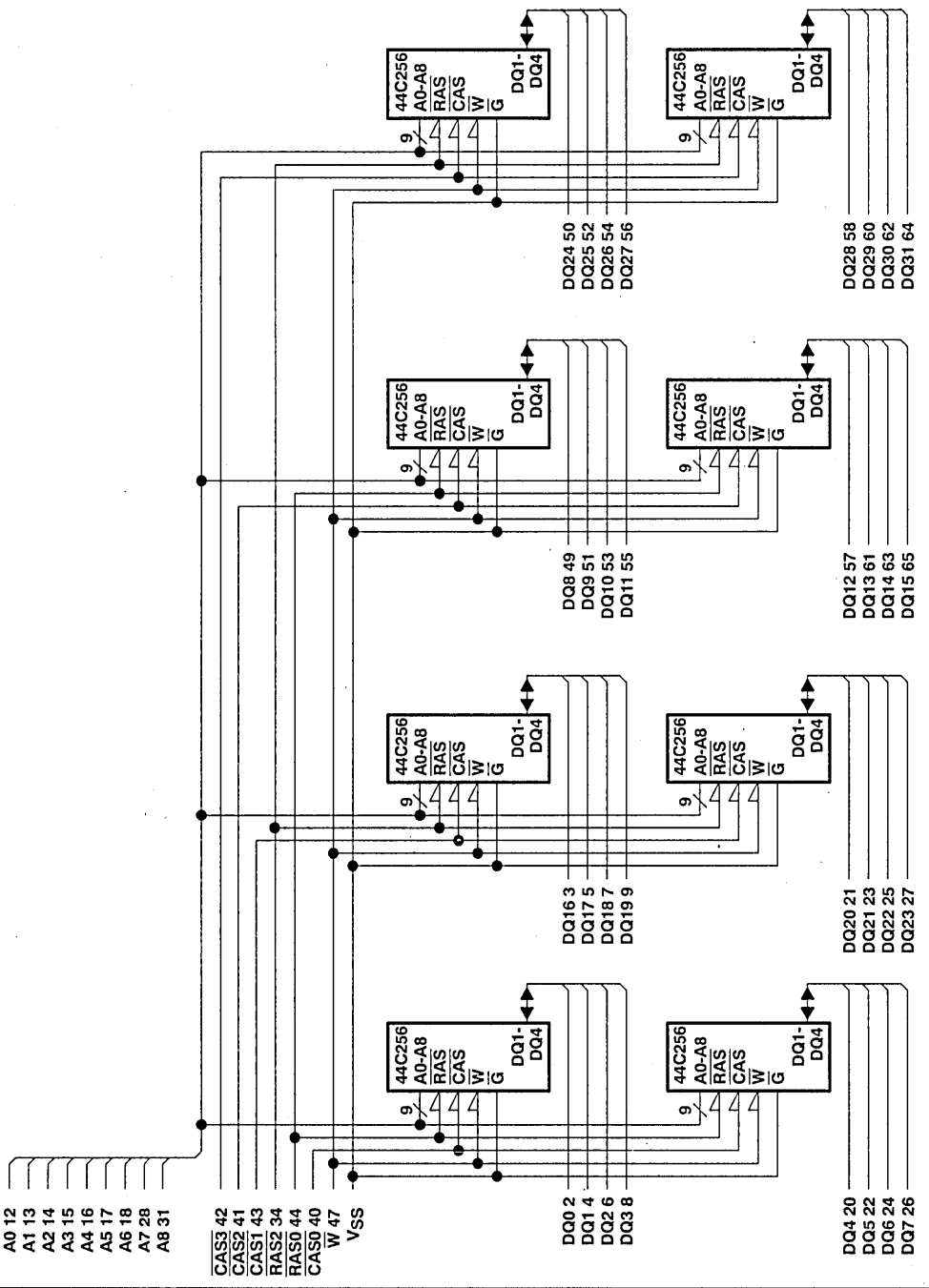
TM256BBK32† (Side View)

TM512CBK32† (Side View)

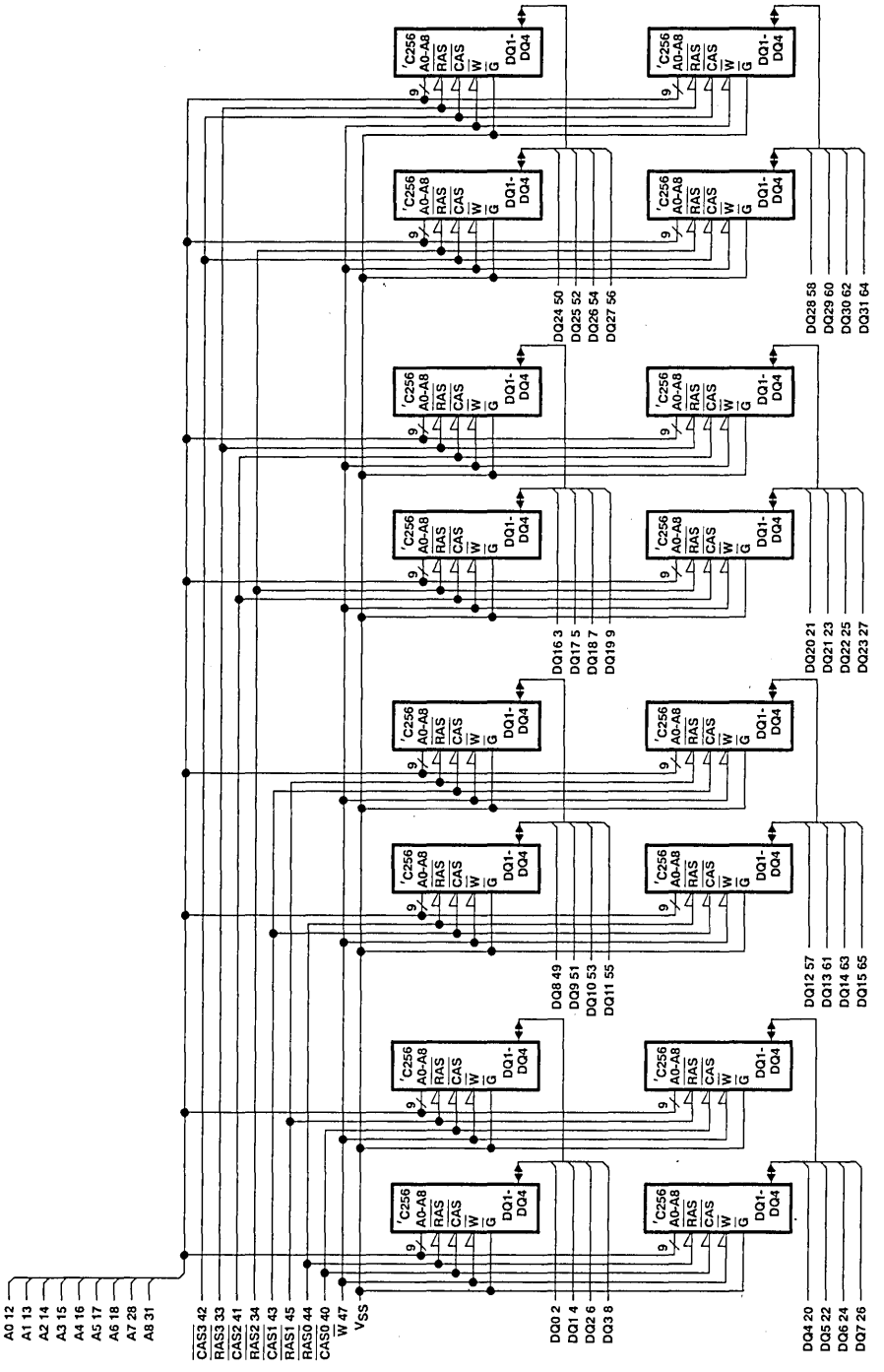
PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS0}$-$\overline{CAS3}$	Column-Address Strobe
DQ0-DQ31	Data In/Data Out
NC	No Connection
$\overline{RAS0}$-$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

† The packages shown here are for pinout reference only and are not drawn to scale. Parts locations may vary.

functional block diagram (for TM256BBK32)



functional block diagram (TM512CBK32)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 8 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (TM256BBK32-6 and TM512CBK32-6)	4.75	5	5.25	V
V_{CC}	Supply voltage (TM256BBK32-70/-80/-10 and TM512CBK32-70/-80/-10)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'256BBK32-6		'256BBK32-70		'256BBK32-80		'256BBK32-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 to V_{CC}		±10		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10		±10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		760		640		600		520	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		16		16		16		16	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		8		8		8		8	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		720		640		560		480	mA
I_{CC4}	Average page current (see Note 4)	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		560		480		400		360	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'512CBK32-6		'512CBK32-70		'512CBK32-80		'512CBK32-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 to V_{CC}		±10		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10		±10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		776		656		616		536	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		32		32		32		32	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		16		16		16		16	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high, ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		736		656		576		496	mA
I_{CC4}	Average page current (see Note 4)	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		576		496		416		376	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4 Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		TM256BBK32		TM512CBK32		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		40		80	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ input		10		20	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ input		20		20	pF
$C_{i(W)}$	Input capacitance, write-enable input		40		80	pF
$C_{o(DQ)}$	Output capacitance on DQ pins		7		14	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	'256BBK32-6 '512CBK32-6		'256BBK32-70 '512CBK32-70		'256BBK32-80 '512CBK32-80		'256BBK32-10 '512CBK32-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	t_{CAC}		15		18		20		25	ns
$t_{a(CA)}$	Access time from column-address	t_{CAA}		30		35		40		45	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns
$t_{a(CP)}$	Access time from column precharge	t_{CAP}		35		40		40		50	ns
$t_{d(CLZ)}$	$\overline{CAS}$ to output in low Z	t_{CLZ}	0		0		0		0		ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 6)	t_{OFF}	0	15	0	18	0	20	0	25	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	'256BBK32-6 '512CBK32-6		'256BBK32-70 '512CBK32-70		'256BBK32-80 '512CBK32-80		'256BBK32-10 '512CBK32-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 7)	t_{RC}	110		130		150		180		ns
$t_{c(W)}$	Write cycle time	t_{WC}	110		130		150		180		ns
$t_{c(P)}$	Page-mode read or write cycle time	t_{PC}	40		45		50		55		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	15	10 000	18	10 000	20	10 000	25	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	40		50		60		70		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low	t_{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low	t_{RASP}	60	100 000	70	100 000	80	100 000	100	100 000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		15		15		15		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		0		ns
$t_{su(D)}$	Data setup time before $\overline{CAS}$ low	t_{DS}	0		0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low	t_{WCS}	0		0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	15		18		20		25		ns
$t_{su(WRH)}$	$\overline{W}$-command setup time before $\overline{RAS}$ high	t_{RWL}	15		18		20		25		ns

NOTE 7: All cycle times assume t_t = 5 ns.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

PARAMETER		ALT. SYMBOL	'256BBK32-6 '512CBK32-6		'256BBK32-70 '512CBK32-70		'256BBK32-80 '512CBK32-80		'256BBK32-10 '512CBK32-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(CA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	10		15		15		20		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	10		10		12		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 8)	t_{AR}	50		55		60		70		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 8)	t_{DHR}	50		55		60		70		ns
$t_{h(D)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	10		15		15		20		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 9)	t_{RCH}	0		0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 9)	t_{RRH}	0		0		0		0		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	15		15		15		20		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low	t_{WCR}	50		55		60		70		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	60		70		80		100		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	15		18		20		25		ns
$t_{d(RLCL)}$	Delay time $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	t_{RCD}	20	45	20	52	22	60	25	75	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address	t_{RAD}	15	30	15	35	17	40	20	55	ns
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	30		35		40		45		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	30		35		40		45		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 11)	t_{CHR}	15		15		20		25		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 11)	t_{CSR}	10		10		10		10		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 11)	t_{RPC}	0		0		0		0		ns
t_{rf}	Distribution refresh time interval	t_{REF}		8		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	3	50	ns

NOTES: 8. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
9. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for the read cycle.
10. Maximum value specified only to guarantee access time.
11. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

device symbolization

The specifications contained in the data sheet are applicable to all TM256BBK32s and TM512CBKs symbolized as shown in Figure 1. Please note that the location of the part number may vary.

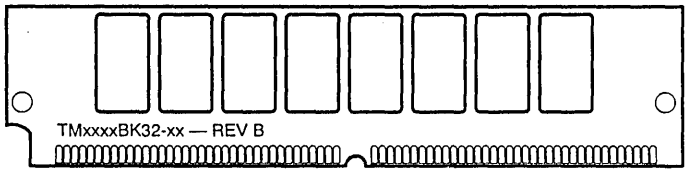


Figure 1. Device Symbolization

This Data Sheet is Applicable to All TM024EAD9s Manufactured With TMS4C1024s Symbolized With Revision "D" and Subsequent Revisions.

- **TM024EAD9 . . . 1 048 576 × 9 Organization**
- **Single 5-V Supply (10% Tolerance)**
- **30-pin Single-In-Line Package (SIP)**
  – Leadless Module for Use with Sockets
- **Utilizes Nine 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period . . . 8 ms (512 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Performance of Unmounted RAMs:**

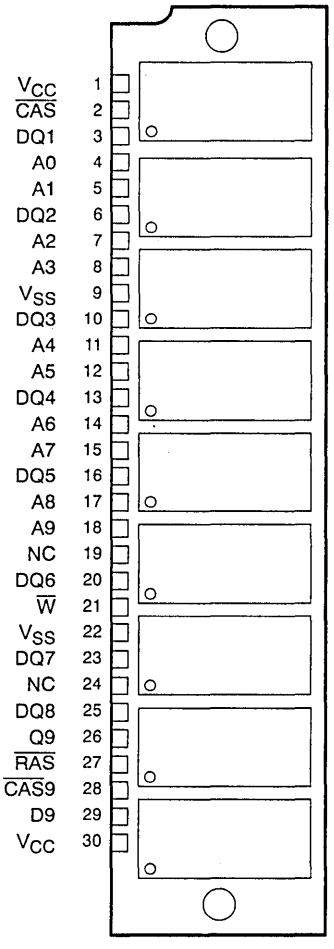
	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)	V_{CC} TOLERANCE
TMS4C1024-6	60 ns	15 ns	110 ns	5%
TMS4C1024-70	70 ns	18 ns	130 ns	10%
TMS4C1024-80	80 ns	20 ns	150 ns	10%
TMS4C1024-10	100 ns	25 ns	180 ns	10%

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free Air Temperature . . . 0°C to 70°C**

description

The TM024EAD9 is a 9216K (dynamic) random-access memory module, organized as 1 048 576 × 9 bits [bit nine (D9, Q9) is generally used for parity and is controlled by $\overline{CAS9}$] in a 30-pin single-in-line (SIP) Package.

AD Single-In-Line Package
(Top View)



PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS}$, $\overline{CAS9}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
D9	Data In
NC	No Internal Connection
Q9	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

The TM024EAD9 is composed of nine TMS4C1024DJ, 1 048 576 × 1-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead package (SOJ), mounted on a substrate together with decoupling capacitors.

The TMS4C1024DJ is described in the TMS4C1024 data sheet and is fully electrically tested and processed according to TI MIL-STD-883B flows (as ammended for commercial applications) prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed.

The TM024EAD9 SIP is available in the AD single-sided, leadless module for use with sockets.

The TM024EAD9 SIP is rated for operation from 0°C to 70°C.

operation

The TM024EAD9 operates as nine TMS4C1024DJs shown in the functional block diagram. Refer to the TMS4C1024 data sheet for details of its operation. The common I/O feature of the TM024EAD9 dictates the use of early write cycles to prevent contention on D and Q.

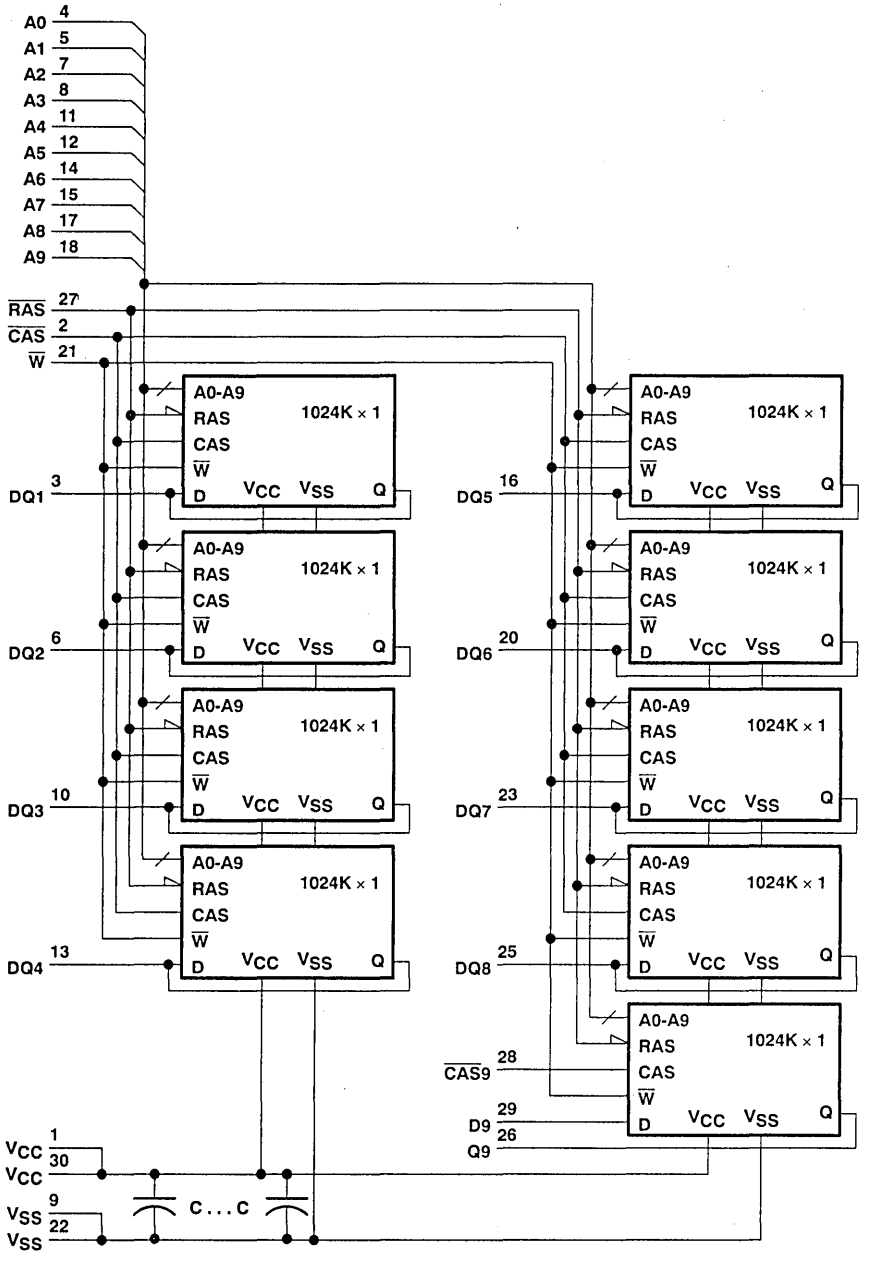
specifications

For TMS4C1024DJ electrical specifications, refer to the TMS4C1024 data sheet.

single-in-line package and components

PC substrate: 1,27 (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate (or coat) on top of copper

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation: ..... 9 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (TM024EAD9-6)	4.75	5	5.25	V
V_{CC}	Supply voltage (TM024EAD9-70/-80/-10)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

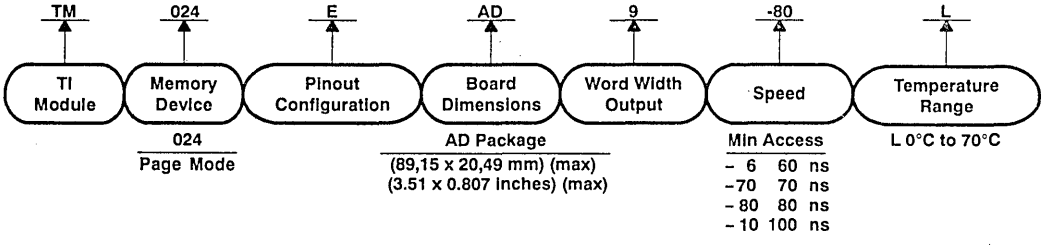
PARAMETER		TEST CONDITIONS	TM024EAD9-6		TM024EAD9-70		TM024EAD9-80		TM024EAD9-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 to V_{CC}		±10		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10		±10	µA
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.5 V		855		720		675		585	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		18		18		18		18	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		810		720		630		540	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		630		540		450		405	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		45	pF
$C_{i(D)}$	Input capacitance, data input (D9 only)		5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		45	pF
$C_{i(W)}$	Input capacitance, write-enable input		45	pF
$C_{o(DQ)}$	Output capacitance (DQ1-DQ8)		10	pF
C_o	Output capacitance (Q9 only)		7	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

TI single-in-line package nomenclature



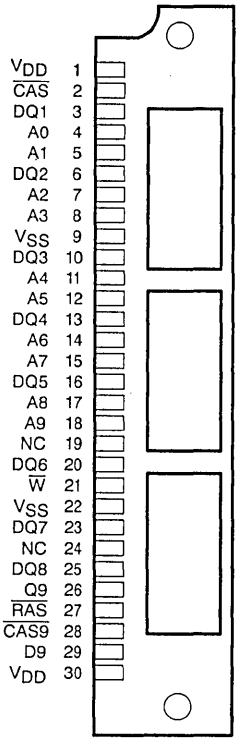
This Data Sheet is Applicable to All TM124EAD9Bs and TM124EAD9Cs Symbolized with Revision "B" and Subsequent Revisions as Described on Page 6-44.

- **1 048 576 × 9 Organization**
- **Single 5-V Power Supply**
- **30-Pin Single-In-Line Package (SIP)**
- **TM124EAD9B . . . Utilizes Two 4-Megabit and One 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **TM124EAD9C . . . Utilizes Three 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **Long Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Outputs**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)	V_{CC} TOLERANCE
'124EAD9B/C-6	60 ns	30 ns	110 ns	±5%
'124EAD9B/C-70	70 ns	35 ns	130 ns	±10%
'124EAD9B/C-80	80 ns	40 ns	150 ns	±10%
'124EAD9B/C-10	100 ns	45 ns	180 ns	±10%

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**

AD Single-In-Line Package (Top View)



PIN NOMENCLATURE	
A0-A9	Address Inputs
CAS, CAS9	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
D9	Data In
NC	No Connect
Q9	Data Out
RAS	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
W	Write Enable

description

The TM124EAD9B and TM124EAD9C are 9216K, dynamic random-access memory modules organized as 1048 576 × 9 [bit nine is generally used for parity] in 30-pin single-in-line packages.

The TM124EAD9B is composed of two TMS44400, 1048 576 × 4-bit dynamic RAMs in 20/26-lead plastic small-outline J-lead packages (SOJs), and one TMS4C1024, 1048 576 × 1-bit dynamic RAM in a 20/26-lead plastic small-outline J-lead package (SOJ).

The TM124EAD9C is composed of two TMS44400, 1 048 576 × 4-bit dynamic RAMs in 20/26-lead plastic small-outline J-lead packages (SOJs), and one TMS44100, 4 194 304 × 1-bit dynamic RAM in a 20/26-lead plastic small-outline J-lead package (SOJ).

The TM124EAD9B and TM124EAD9C are both mounted on a substrate together with three 0.2 μF decoupling capacitors. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated through-holes, a cost savings can be realized.

The TM124EAD9B and TM124EAD9C each feature $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM124EAD9B and TM124EAD9C are characterized for operation from 0°C to 70°C.

operation

The TM124EAD9B operates as two TMS44400s and one TMS4C1024 connected as shown in the functional block diagram.

The TM124EAD9C operates as two TMS44400s and one TMS44100 connected as shown in the functional block diagram.

The common I/O features of the TM124EAD9B and TM124EAD9C dictate the use of early write cycles to prevent contention on the DQ lines.

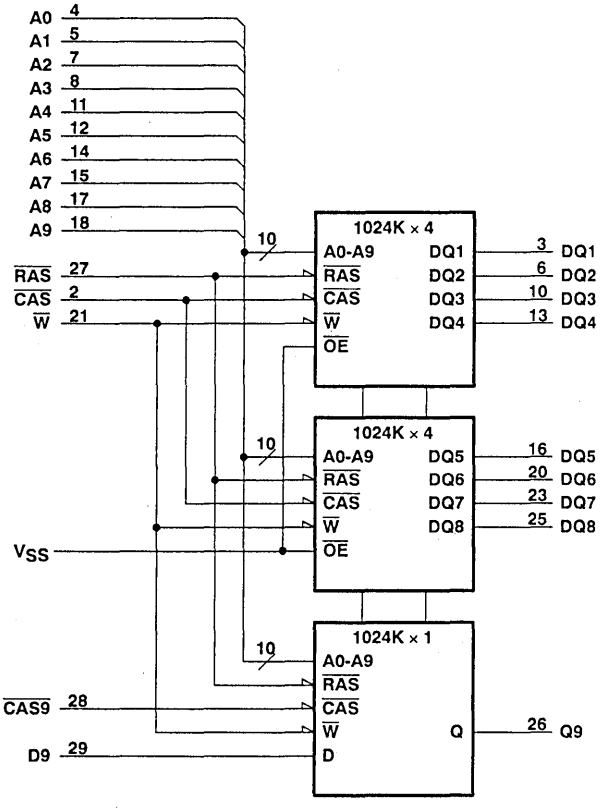
specifications

The refresh period is extended to 16 milliseconds and, during this period, each of the 1024 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power. For the TM124EAD9B, the nine least significant row addresses (A0-A8) must be refreshed every 8 ms as required by the TMS4C1024.

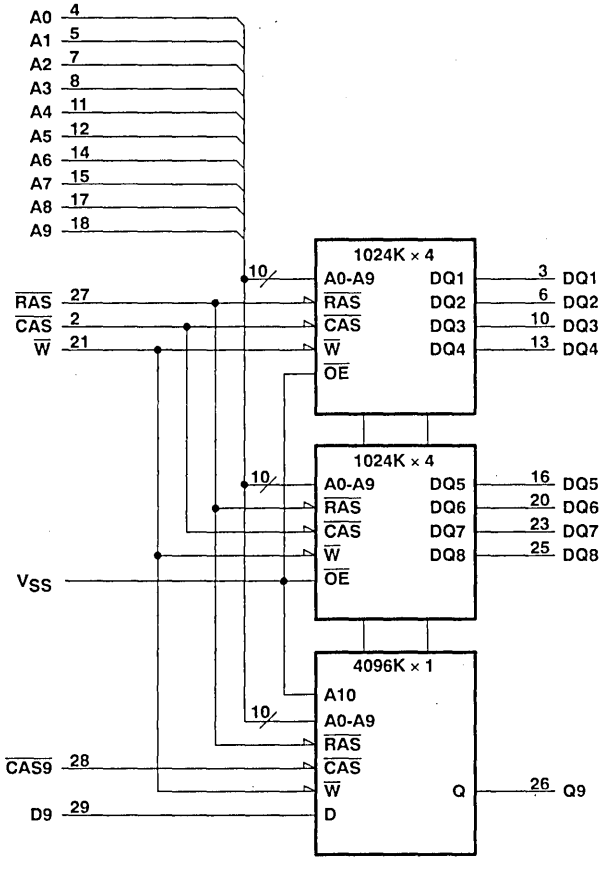
single-in-line package and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness on contact area
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

functional block diagram (TM124EAD9B)



functional block diagram (TM124EAD9C)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 3 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (TM124EAD9B-6 and TM124EAD9C-6)	4.75	5	5.75	V
V_{CC}	Supply voltage (TM124EAD9B-70/-80/-10 and TM124EAD9C-70/-80/-10)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124EAD9B-6 '124EAD9C-6		'124EAD9B-70 '124EAD9C-70		'124EAD9B-80 '124EAD9C-80		'124EAD9B-10 '124EAD9B-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I=0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 30		± 30		± 30		± 30	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		285		255		225		195	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		6		6		6		6	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		3		3		3		3	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		285		255		225		195	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		210		180		150		120	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		TM124EAD9B TM124EAD9C		UNIT
		MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		15	pF
$C_{i(DQ)}$	Input capacitance, data inputs/outputs		12	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		21	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		21	pF
$C_{i(CAS9)}$	Input capacitance, $\overline{CAS9}$ input		7	pF
$C_{i(D9)}$	Input capacitance on D9		5	pF
$C_{o(Q9)}$	Output capacitance on Q9		7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124EAD9B-6 '124EAD9C-6		'124EAD9B-70 '124EAD9C-70		'124EAD9B-80 '124EAD9C-80		'124EAD9B-10 '124EAD9C-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	0	25	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124EAD9B-6 '124EAD9C-6		'124EAD9B-70 '124EAD9C-70		'124EAD9B-80 '124EAD9C-80		'124EAD9B-10 '124EAD9C-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		180		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		55		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		75		ns
t_{DH}	Data hold time	10		15		15		20		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		75		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 10)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 10)	0		0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 10)	50		55		60		75		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns

Continued next page.

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'124EAD9B-6 '124EAD9C-6		'124EAD9B-70 '124EAD9C-70		'124EAD9B-80 '124EAD9C-80		'124EAD9B-10 '124EAD9C-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 11)	15	30	15	35	15	40	20	50	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 11)	20	45	20	52	20	60	25	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{REF}	Distributed refresh time interval		16		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	2	50	ns

NOTE 11: The maximum value is specified only to guarantee access time.

device symbolization

The specifications contained in this data sheet are applicable to all TM124EAD9Bs and TM124EAD9Cs symbolized as shown in Figure 1. Please note that the location of the part number may vary.

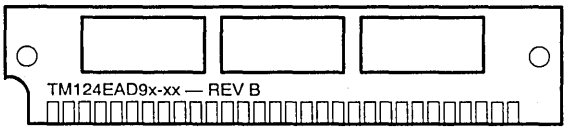


Figure 1. Device Symbolization

SMMS236 — JANUARY 1991

- TM256KBK36B . . . 262 144 × 36 Organization
- TM512LBK36B . . . 524 288 × 36 Organization
- Single 5-V Power Supply
- 72-pin Single-In-Line Package (SIP) – Leadless Module for Use With Sockets
- TM256KBK36B . . . Utilizes Eight 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages and One 1-Megabit Quad-$\overline{CAS}$ Dynamic RAM in a Plastic Small-Outline J-Lead (SOJ) Package
- TM512LBK36B . . . Utilizes Sixteen 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Two 1-Megabit Quad-$\overline{CAS}$ Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages
- Long Refresh Period . . . 8 ms (512 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$, $\overline{RAS}$-Only, and Hidden Refresh
- 3-State Output
- Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines, in Four Blocks
- Performance Ranges:

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)	V_{CC} TOLERANCE
'256KBK36B-6	60 ns	15 ns	110 ns	±5%
'256KBK36B-70	70 ns	18 ns	130 ns	±10%
'256KBK36B-80	80 ns	20 ns	150 ns	±10%
'256KBK36B-10	100 ns	25 ns	180 ns	±10%
'512LBK36B-6	60 ns	15 ns	110 ns	±5%
'512LBK36B-70	70 ns	18 ns	130 ns	±10%
'512LBK36B-80	80 ns	20 ns	150 ns	±10%
'512LBK36B-10	100 ns	25 ns	180 ns	±10%

- Low Power Dissipation
- Operating Free-Air Temperature Range . . . 0°C to 70°C

description

TM256KBK36B

The TM256KBK36B is a 9437K (dynamic) random-access memory module organized as four times 262 144 × 9 [bit nine is generally used for parity] in a 72-pin single-in-line package (SIP). The SIP is composed of eight TMS44C256DJ, 262 144 × 4-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs) and one TMS44C260DJ, 262 144 × 4-bit Quad-$\overline{CAS}$ dynamic RAM in a 24/26-lead plastic small-outline J-lead package (SOJ), mounted on a substrate together with decoupling capacitors. Each TMS44C256DJ and TMS44C260DJ is described in the TMS44C256 or TMS44C260 data sheets (repectively).

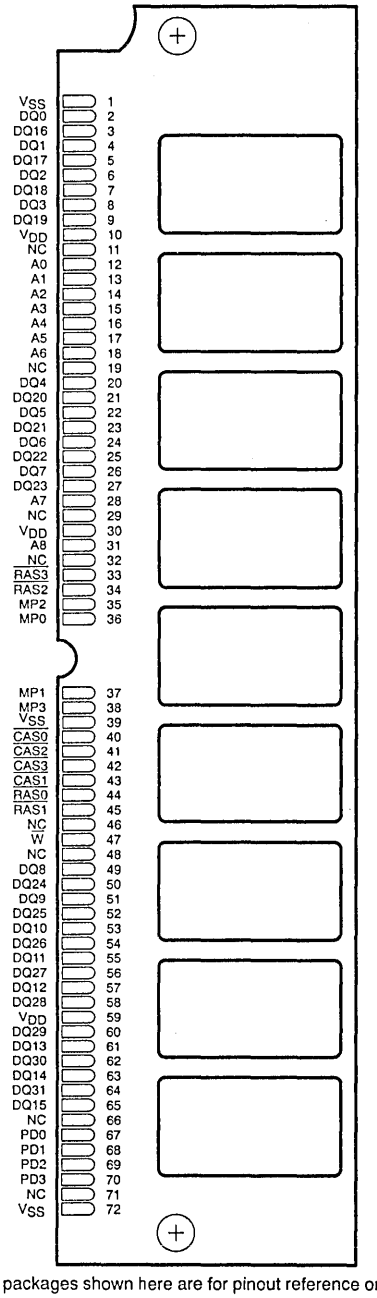
The TM256KBK36B is available in a single-sided BK leadless module for use with sockets.

The TM256KBK36B features $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns. This device is rated for operation from 0°C to 70°C.

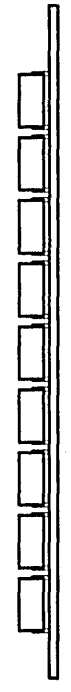
TM512LBK36B

The TM512LBK36B is a 18 874K (dynamic) random-access memory module organized as four times 524 288 × 9 [bit nine is generally used for parity] in a 72-pin single-in-line package (SIP). The SIP is composed of sixteen TMS44C256DJ, 262 144 × 4-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs) and two TMS44C260DJ, 262 144 × 4-bit Quad-$\overline{CAS}$ dynamic RAMs in a 24/26-lead plastic small-outline J-lead package (SOJ), mounted on a substrate together with decoupling capacitors. Each TMS44C256DJ and TMS44C260DJ is described in the TMS44C256 or TMS44C260 data sheets (repectively).

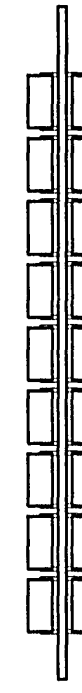
BK Single-In-Line Package† (Top View)



TM256KBK36B† (Side View)



TM512LBK36B† (Side View)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS0}$-$\overline{CAS3}$	Column-Address Strobe
DQ0-DQ31	Data In/Data Out
MP0-MP3	Parity
NC	No Connection
PD0-PD3	Presence Detects
$\overline{RAS0}$-$\overline{RAS3}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

† The packages shown here are for pinout reference only and are not drawn to scale.

The TM512LBK36B is available in a double-sided BK leadless module for use with sockets.

The TM512LBK36B features $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns. This device is rated for operation from 0°C to 70°C.

operation

TM256KBK36B

The TM256KBK36B operates as eight TMS44C256DJs and one TMS44C260DJ connected as shown in the functional block diagram and Table 1. The parity bits MP0-MP3 are provided by the TMS44C260DJ and are controlled by $\overline{RAS2}$. To ensure proper parity bit operation all memory accesses must include a $\overline{RAS2}$ pulse. Refer to the TMS44C256 and TMS44C260 data sheets for details of operation. The common I/O feature of the TM256KBK36B dictates the use of early write cycles to prevent contention on D and Q.

TM512LBK36B

The TM512LBK36B operates as sixteen TMS44C256DJs and two TMS44C260DJs connected as shown in the functional block diagram and Table 1. The parity bits MP0-MP3 are provided by the TMS44C260DJs and are controlled by $\overline{RAS2}$ and $\overline{RAS3}$ on side 1 and side 2 respectively. To ensure proper parity bit operation all memory accesses to side 1/side 2 must include a $\overline{RAS2}/\overline{RAS3}$ pulse. Refer to the TMS44C256 and TMS44C260 data sheets for details of operation. The common I/O feature of the TM512LBK36B dictates the use of early write cycles to prevent contention on D and Q.

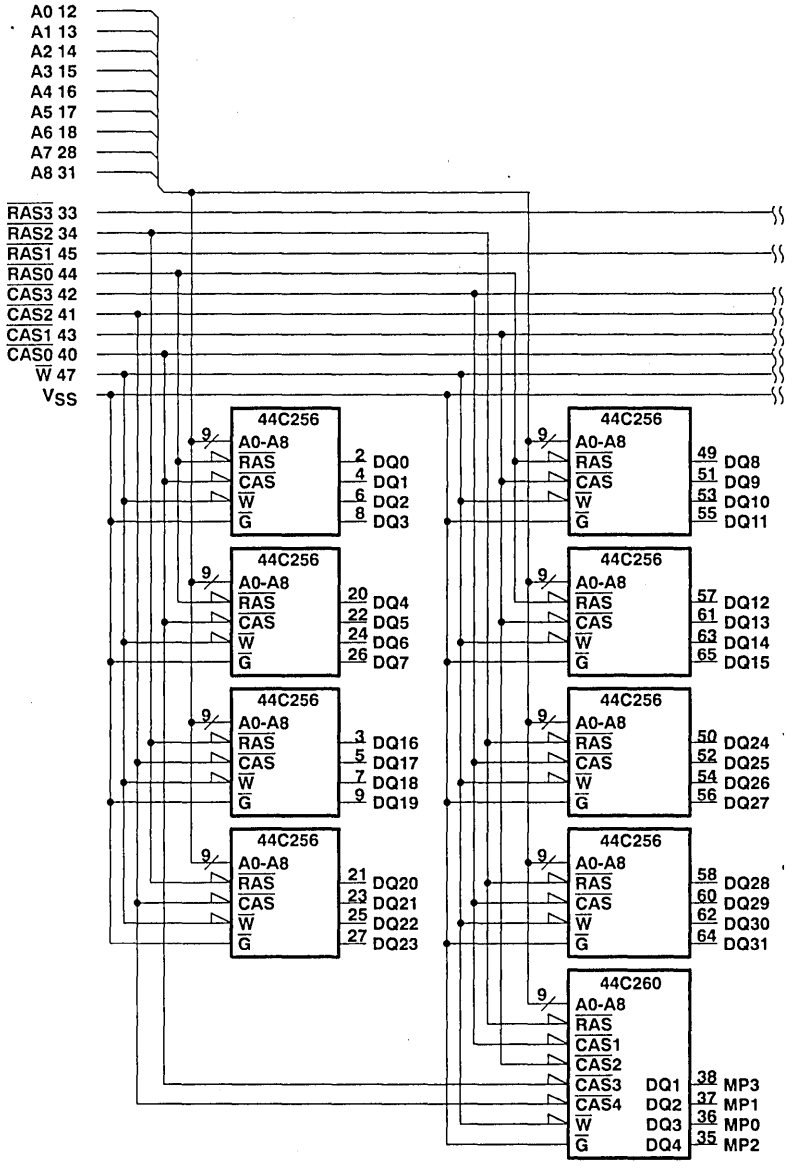
single-in-line package and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and gold plate on top of copper

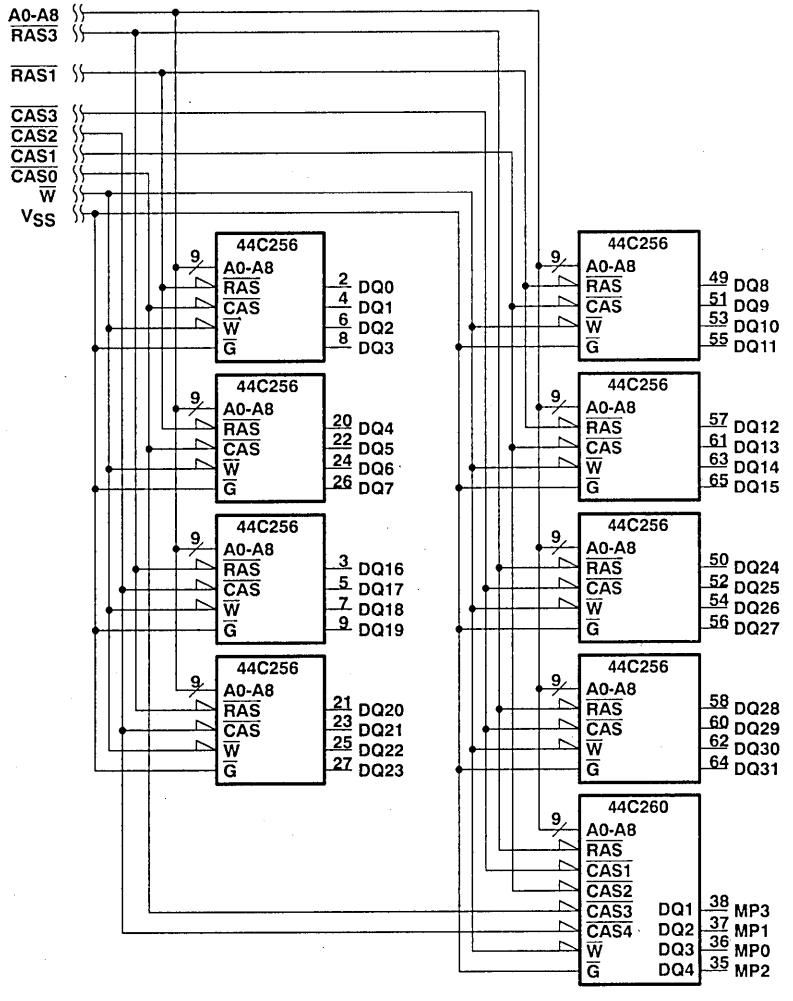
Table 1. Connection Table

DATA BLOCK	$\overline{RASx}$		$\overline{CASx}$
	SIDE 1	SIDE 2	
DQ0-DQ7 MP0	$\overline{RAS0}$ $\overline{RAS2}$	$\overline{RAS1}$ $\overline{RAS3}$	$\overline{CAS0}$ $\overline{CAS0}$
DQ8-DQ15 MP1	$\overline{RAS0}$ $\overline{RAS2}$	$\overline{RAS1}$ $\overline{RAS3}$	$\overline{CAS1}$ $\overline{CAS1}$
DQ16-DQ23 MP2	$\overline{RAS2}$ $\overline{RAS2}$	$\overline{RAS3}$ $\overline{RAS3}$	$\overline{CAS2}$ $\overline{CAS2}$
DQ24-DQ31 MP3	$\overline{RAS2}$ $\overline{RAS2}$	$\overline{RAS3}$ $\overline{RAS3}$	$\overline{CAS3}$ $\overline{CAS3}$

functional block diagram (for TM256KBK36B and TM512LBK36B)



functional block diagram (for TM512LBK36B)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 9 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (TM256KBK36B-6 and TM512LBK36B-6)	4.75	5	5.25	V
V_{CC}	Supply voltage (TM256KBK36B-70/-80/-10 and TM512LBK36B-70/-80/-10)	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'256KBK36B-6		'256KBK36B-70		'256KBK36B-80		'256KBK36B-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 90		± 90		± 90		± 90	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.5 V		855		720		675		585	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		18		18		18		18	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		810		720		630		540	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		630		540		450		405	mA

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'512LBK36B-6		'512LBK36B-70		'512LBK36B-80		'512LBK36B-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 180		± 180		± 180		± 180	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 20		± 20		± 20		± 20	µA
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.5 V		873		738		693		603	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		36		36		36		36	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		828		738		648		558	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		648		558		468		423	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		TM256KBK36B		TM512LBK36B		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		45		90	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs		25		25	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs		15		30	pF
$C_{i(W)}$	Input capacitance, write-enable input		45		90	pF
$C_{o(DQ)}$	Output capacitance on DQ pins		7		14	pF
$C_{o(MP)}$	Output capacitance on MP pins		7		14	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	'256KBK36B-6 '512LBK36B-6		'256KBK36B-70 '512LBK36B-70		'256KBK36B-80 '512LBK36B-80		'256KBK36B-10 '512LBK36B-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	t_{CAC}		15		18		20		25	ns
$t_{a(CA)}$	Access time from column-address	t_{CAA}		30		35		40		45	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns
$t_{a(CP)}$	Access time from column precharge	t_{CAP}		35		40		40		50	ns
$t_{d(CLZ)}$	$\overline{CAS}$ to output in low Z	t_{CLZ}	0				0		0		ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)	t_{OFF}	0	15	0	18	0	20	0	25	ns

NOTE 4: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	'256KBK36B-6 '512LBK36B-6		'256KBK36B-70 '512LBK36B-70		'256KBK36B-80 '512LBK36B-80		'256KBK36B-10 '512LBK36B-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 5)	t_{RC}	110		130		150		180		ns
$t_{c(W)}$	Write cycle time	t_{WC}	110		130		150		180		ns
$t_{c(P)}$	Page-mode read or write cycle time	t_{PC}	40		45		50		55		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	15	10 000	18	10 000	20	10 000	25	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	40		50		60		70		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low	t_{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low	t_{RASP}	60	100 000	70	100 000	80	100 000	100	100 000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		15		15		15		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		0		ns
$t_{su(D)}$	Data setup time before $\overline{CAS}$ low	t_{DS}	0		0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low	t_{WCS}	0		0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	15		18		20		25		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	15		18		20		25		ns

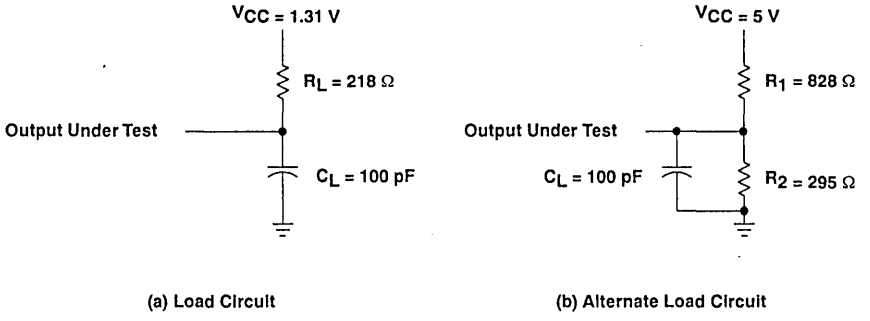
NOTE 5: All cycle times assume t_t = 5 ns.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

PARAMETER		ALT. SYMBOL	'256KBK36B-6 '512LBK36B-6		'256KBK36B-70 '512LBK36B-70		'256KBK36B-80 '512LBK36B-80		'256KBK36B-10 '512LBK36B-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(CA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	10		15		15		20		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	10		10		12		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 6)	t_{AR}	50		55		60		70		ns
$t_{h(CLCH)}$	Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high (see Note 7)	t_{AR}	50		55		60		70		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 6)	t_{DHR}	50		55		60		70		ns
$t_{h(D)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	10		15		15		20		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 8)	t_{RCH}	0		0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 8)	t_{RRH}	0		0		0		0		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	15		15		15		20		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low	t_{WCR}	50		55		60		70		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	60		70		80		100		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	15		18		20		25		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ (see Note 9)	t_{RCD}	20	45	20	52	22	60	25	75	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address	t_{RAD}	15	30	15	35	17	40	20	55	ns
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	30		35		40		45		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	30		35		40		45		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 10)	t_{CHR}	15		15		20		25		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 10)	t_{CSR}	10		10		10		10		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 10)	t_{RPC}	0		0		0		0		ns
t_{rf}	Distribution refresh time interval	t_{REF}		8		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	3	50	ns

NOTES: 6. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
7. Reference TMS44C260 data sheet.
8. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for the read cycle.
9. Maximum value specified only to guarantee access time.
10. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit

(b) Alternate Load Circuit

Figure 1. Load Circuits for Timing Parameters

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- TM256KBK36C . . . 262 144 × 36-Bit Organization
- TM512LBK36C . . . 524 288 × 36-Bit Organization
- Single 5-V Power Supply
- 72-pin Single-In-Line Package (SIP)
  – Leadless Module for Use With Sockets
- TM256KBK36C . . . Utilizes Eight 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Two 1-Megabit Quad-$\overline{CAS}$ Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages
- TM512LBK36C . . . Utilizes Sixteen 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Four 1-Megabit Quad-$\overline{CAS}$ Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages
- Long Refresh Period . . . 8 ms (512 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Output

- Performance Ranges:

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)	V_{CC} TOLERANCE
'256KBK36C-6	60 ns	15 ns	110 ns	±5%
'256KBK36C-70	70 ns	18 ns	130 ns	±10%
'256KBK36C-80	80 ns	20 ns	150 ns	±10%
'256KBK36C-10	100 ns	25 ns	180 ns	±10%
'512LBK36C-6	60 ns	15 ns	110 ns	±5%
'512LBK36C-70	70 ns	18 ns	130 ns	±10%
'512LBK36C-80	80 ns	20 ns	150 ns	±10%
'512LBK36C-10	100 ns	25 ns	180 ns	±10%

- Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines
- Separate $\overline{RAS}$ Control for Eighteen Data-In and Data-Out Lines in Two Blocks
- Low Power Dissipation
- Operating Free-Air Temperature Range . . . 0°C to 70°C
- Enhanced Page Mode Operation with $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, and Hidden Refresh

description

TM256KBK36C

The TM256KBK36C is a 9216K dynamic random-access memory module organized as four times 262 144 × 9 [bit nine is generally used for parity] in a 72-pin single-in-line package (SIP). The SIP is composed of eight TMS44C256DJ, 262 144 × 4-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs) and two TMS44C260DJ, 262 144 × 4-bit Quad-$\overline{CAS}$ dynamic RAMs in 24/26-lead plastic small-outline J-lead packages (SOJs), mounted on a substrate together with decoupling capacitors. Each TMS44C256DJ and TMS44C260DJ is described in the TMS44C256 or TMS44C260 data sheets (respectively).

The TM256KBK36C SIP is available in a single-sided BK leadless module for use with sockets.

The TM256KBK36C SIP features $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns and 100 ns. This device is rated for operation from 0°C to 70°C.

TM512LBK36C

The TM512LBK36C is a 18 432K dynamic random-access memory module organized as four times 524 288 × 9 [bit nine is generally used for parity] in a 72-pin single-in-line package (SIP). The SIP is composed of sixteen TMS44C256DJ, 262 144 × 4-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs) and four TMS44C260DJ, 262 144 × 4-bit Quad-$\overline{CAS}$ dynamic RAMs in 24/26-lead plastic small-outline J-lead packages (SOJs), mounted on a substrate together with decoupling capacitors. Each TMS44C256DJ and TMS44C260DJ is described in the TMS44C256 or TMS44C260 data sheets (respectively).

The TM512LBK36C is available in a double-sided BK leadless module for use with sockets.

The TM512LBK36C features $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns and 100 ns. This device is rated for operation from 0°C to 70°C.

operation

TM256KBK36C

The TM256KBK36C operates as eight TMS44C256DJs and two TMS44C260DJs connected as shown in the functional block diagram and Table 1. Refer to the TMS44C256 and TMS44C260 data sheets for details of operation. The common I/O feature of the TM256KBK36C dictates the use of early write cycles to prevent contention on D and Q.

TM512LBK36C

The TM512LBK36C operates as sixteen TMS44C256DJs and four TMS44C260DJs connected as shown in the functional block diagram and Table 1. Refer to the TMS44C256 and TMS44C260 data sheets for details of operation. The common I/O feature of the TM512LBK36C dictates the use of early write cycles to prevent contention on D and Q.

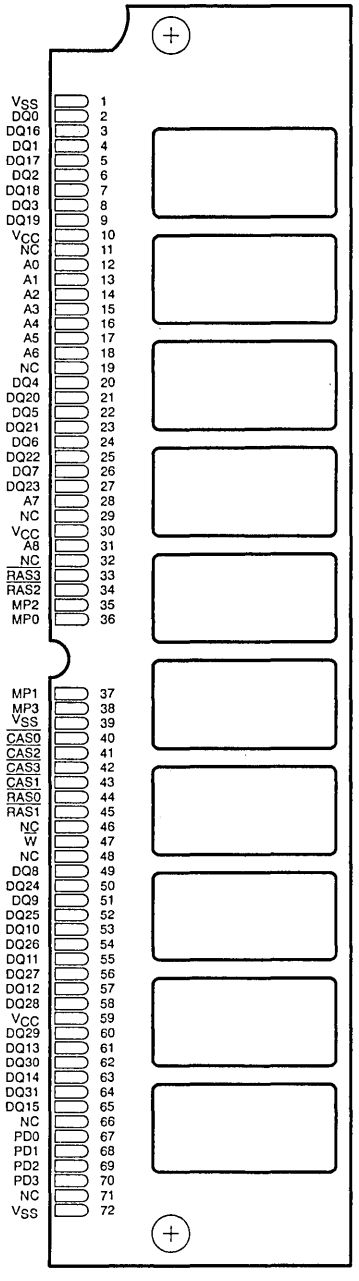
single-in-line package and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and gold plate on top of copper

Table 1. Connection Table

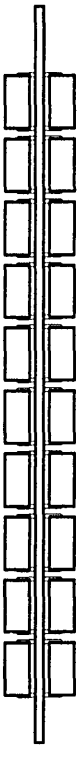
DATA BLOCK	$\overline{RASx}$		$\overline{CASx}$
	Side 1	Side 2	
DQ0-DQ7 MP0	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ8-DQ15 MP1	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ16-DQ23 MP2	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ24-DQ31 MP3	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$

BK Single-in-line Package† (Top View)



TM256KBK36C
BK Single-in-line Package† (Side View)

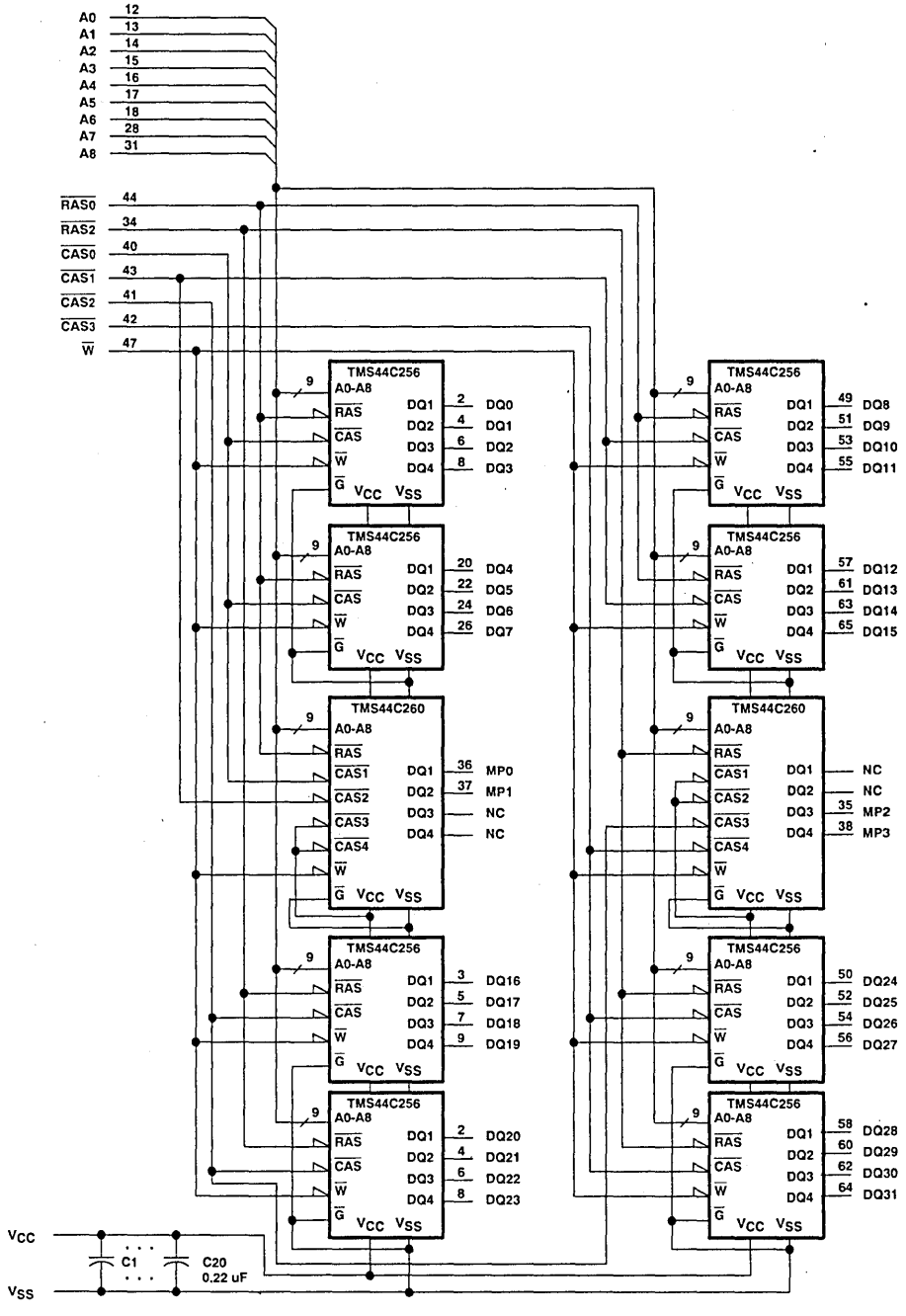
TM512LBK36C
BK Single-in-line Package† (Side View)



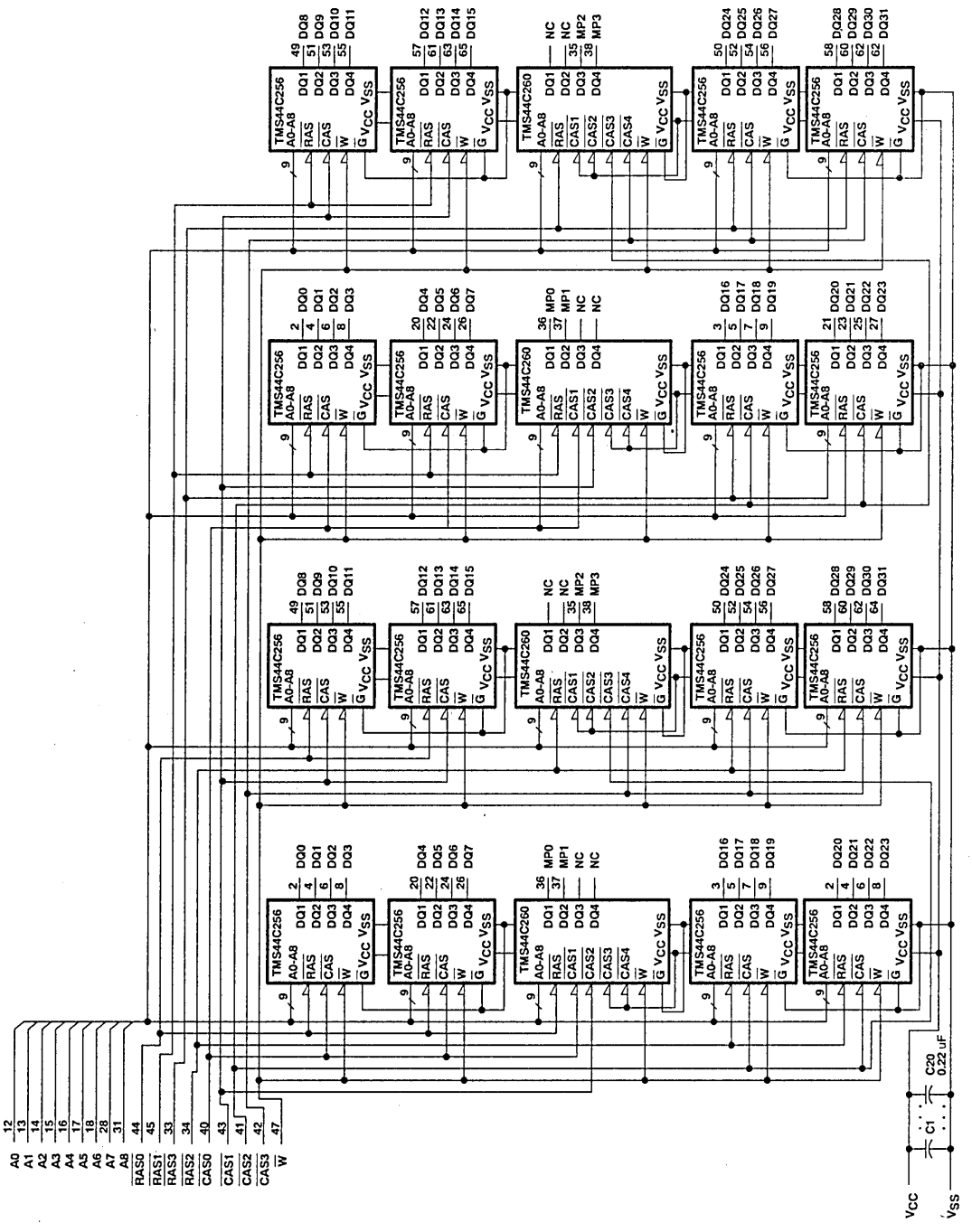
PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS0}$-$\overline{CAS3}$	Column-Address Strobe
$\overline{RAS0}$-$\overline{RAS3}$	Row-Address Strobe
DQ0-DQ31	Data In/Data Out
$\overline{W}$	Write Enable
NC	No External Connection
V_{CC}	5-V Supply
V_{SS}	Ground
PD0-PD3	Presence Detects
MP0-MP3	Parity

† The packages shown here are for pinout reference only and are not drawn to scale.

functional block diagram (TM256KBK36C)



functional block diagram (TM512LBK36C)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 10 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (TM256KBK36C-6 and TM512LBK36C-6)	4.75	5	5.25	V
V_{CC}	Supply voltage (TM256KBK36C-70/-80/-10 and TM512LBK36C-70/-80/-10)	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'256KBK36C-6		'256KBK36C-70		'256KBK36C-80		'256KBK36C-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±100		±100		±100		±100	µA
I_O	Output current (leakage)	V_O = 0 to 6.5 V, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10		±10	µA
I_{CC1}	Read or write cycle current	t_{RWC} = minimum, V_{CC} = 5.5 V		950		800		750		650	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		20		20		20		20	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR)	t_{RWC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		900		800		700		600	mA
I_{CC4}	Average page current	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		700		600		500		450	mA

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'512LBK36C-6		'512LBK36C-70		'512LBK36C-80		'512LBK36C-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±200		±200		±200		±200	µA
I_O	Output current (leakage)	V_O = 0 to 6.5 V, V_{CC} = 5.5 V, $\overline{CAS}$ high		±20		±20		±20		±20	µA
I_{CC1}	Read or write cycle current	t_{RWC} = minimum, V_{CC} = 5.5 V		970		820		770		670	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		40		40		40		40	mA
I_{CC3}	Average refresh current (RAS-only or CBR)	t_{RWC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high (RAS-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		920		820		720		620	mA
I_{CC4}	Average page current	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		720		620		520		470	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		TM256KBK36C		TM512LBK36C		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		50		100	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs		25		25	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs		15		30	pF
$C_{i(W)}$	Input capacitance, write-enable input		50		100	pF
$C_{o(DQ)}$	Output capacitance, DQ		7		14	pF
$C_{o(MP)}$	Output capacitance on MP pins		7		14	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TM256KBK36C-6 TM512LBK36C-6		TM256KBK36C-70 TM512LBK36C-70		TM256KBK36C-80 TM512LBK36C-80		TM256KBK36C-10 TM512LBK36C-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CAA}	Access time from column-address		30		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{CAP}	Access time from column precharge		35		40		40		50	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 4)	0	15	0	18	0	20	0	25	ns

NOTE 4: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'256KBK36C-6 '512LBK36C-6		'256KBK36C-70 '512LBK36C-70		'256KBK36C-80 '512LBK36C-80		'256KBK36C-10 '512LBK36C-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time (see Note 6)	110		130		150		180		ns
t_{WC}	Write cycle time	110		130		150		180		ns
t_{PC}	Page-mode read or write cycle time (see Note 7)	40		45		50		55		ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{WP}	Write pulse duration	15		15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time before $\overline{W}$ low	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		20		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		12		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 8)	50		55		60		70		ns

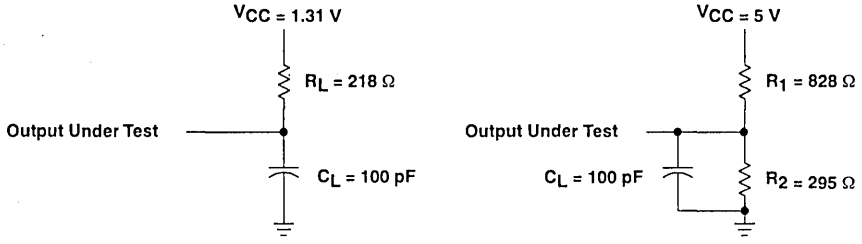
NOTES: 5. Timing measurements are referenced to V_{IL} max or V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. $t_{PC} > t_{CP}$ min + t_{CAS} min + $2t_T$.
8. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

PARAMETER		'256KBK36C-6 '512LBK36C-6		'256KBK36C-70 '512LBK36C-70		'256KBK36C-80 '512LBK36C-80		'256KBK36C-10 '512LBK36C-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CLCH}	Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high (see Note 12)	5		5		5		5		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	10		15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 8)	50		55		60		70		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 9)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 9)	0		0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 8)	50		55		60		70		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	22	60	25	75	ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 10)	15	30	15	35	17	40	20	55	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 11)	15		15		20		25		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 11)	10		10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 11)	0		0		0		0		ns
t_{REF}	Refresh time interval		8		8		8		8	ms
t_T	Transitiion time	3	50	3	50	3	50	3	50	ns

NOTES: 8. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
9. Either t_{RRH} or t_{RCH} must be satisfied for the read cycle.
10. Maximum value specified only to guarantee access time.
11. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
12. See TMS44C260 data sheet.

PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit

(b) Alternate Load Circuit

Figure 1. Load Circuits for Timing Parameters

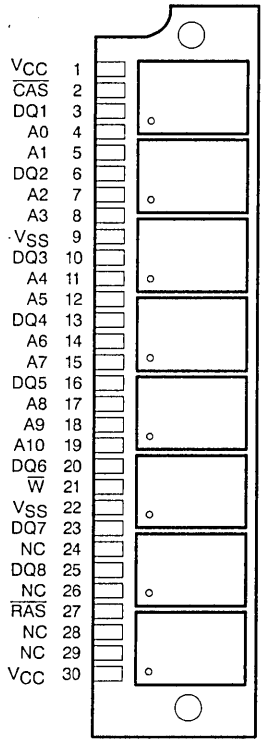
This Data Sheet is Applicable to All TM4100GBD8s Symbolized with Revision "B" and Subsequent Revisions as Described on Page 6-71.

- **4 194 304 × 8 Organization**
- **Single 5-V Power Supply**
- **30-Pin Single-In-Line Package (SIP) — Leadless Module for Use with Sockets**
- **Utilizes Eight 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **Long Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'4100GBD8-6	60 ns	30 ns	15 ns	110 ns
'4100GBD8-70	70 ns	35 ns	18 ns	130 ns
'4100GBD8-80	80 ns	40 ns	20 ns	150 ns
'4100GBD8-10	100 ns	50 ns	25 ns	180 ns

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Seperate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**

BD Single-In-Line Package† (Top View)



† The package shown is for pinout reference only.

PIN NOMENCLATURE	
A0-A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4100GBD8 is a 36 864K (dynamic) random-access memory module organized as 4 194 304 × 8-bits in a 30-pin single-in-line package (SIP).

The SIP is composed of eight TMS44100DM or TMS44100DJ, 4 194 304 × 1-bit dynamic RAMs in 20/26-lead plastic small-outline J-lead packages (SOJ), mounted on a substrate with decoupling capacitors.

The TMS4100GBD8 SIP is available in the BD single-sided, leadless module for use with sockets.

The TMS4100GBD8 SIP is characterized for operation from 0°C to 70°C.

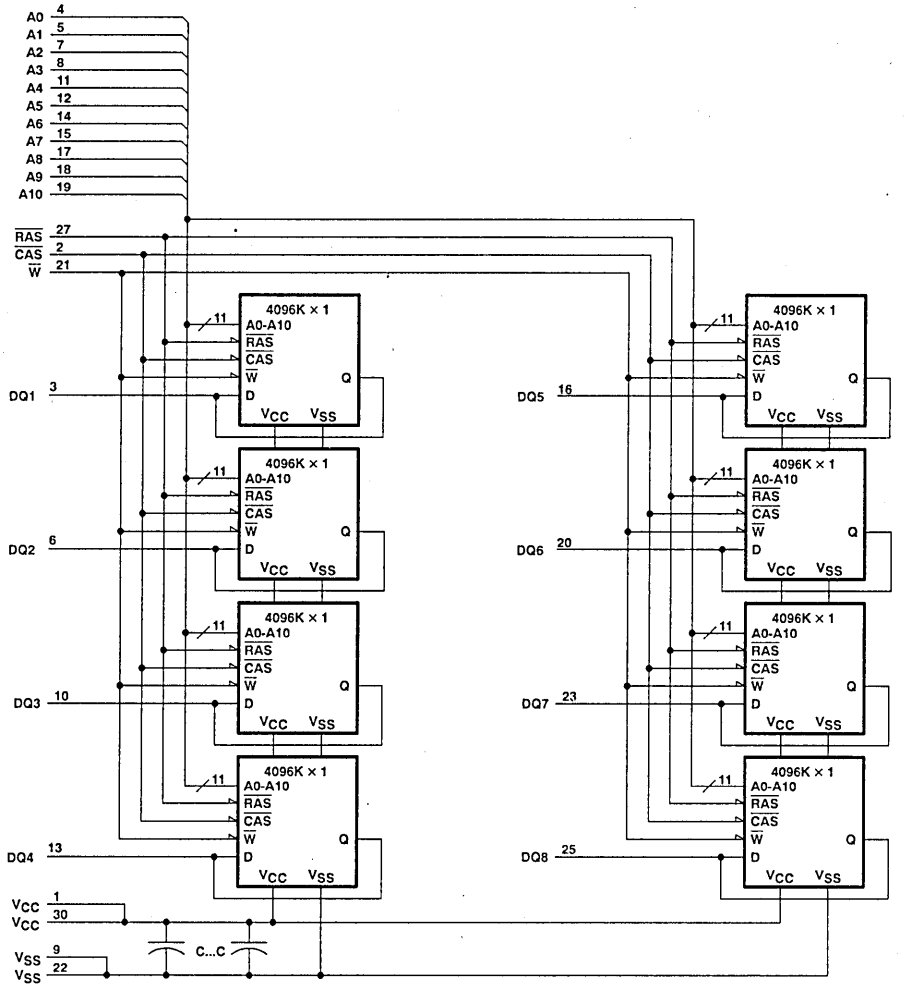
operation

The TMS4100GBD8 operates as eight TMS44100DMs or TMS44100DJs connected as shown in the functional block diagram. Refer to the TMS44100 data sheet for details of its operation. The common I/O feature of the TM4100GBD8 dictates the use of early write cycles to prevent contention on D and Q.

single-in-line package and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate on top of copper

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1)	−1 V to 7 V
Voltage range on V_{CC}	−1 V to 7 V
Short circuit output current	50 mA
Power dissipation	8 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (TM4100GBD8-6)	4.75	5	5.25	V
V_{CC}	Supply voltage (TM4100GBD8-70/-80/-10)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'4100GBD8-6		'4100GBD8-70		'4100GBD8-80		'4100GBD8-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10		±10	μA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		760		680		600		520	mA
I_{CC2}	Standby Current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		16		16		16		16	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} − 0.2 V (CMOS)		8		8		8		8	mA
I_{CC3}	Average refresh current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high		760		680		600		520	mA
I_{CC4}	Average page current (see Note 4)	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		560		480		400		320	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		40	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		56	pF
$C_{i(W)}$	Input capacitance, write-enable input		56	pF
C_o	Output capacitance (pins DQ1-DQ8)		12	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on the pin under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'4100GBD8-6		'4100GBD8-70		'4100GBD8-80		'4100GBD8-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	0	25	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4100GBD8-6		'4100GBD8-70		'4100GBD8-80		'4100GBD8-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		180		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		55		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTS}	$\overline{W}$-low setup time (test mode only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		75		ns
t_{DH}	Data hold time	10		15		15		20		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		75		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 10)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 10)	0		0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 10)	50		55		60		75		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		10		ns

Continued next page.

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'4100GBD8-6		'4100GBD8-70		'4100GBD8-80		'4100GBD8-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 11)	15	30	15	35	15	40	20	50	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 11)	20	45	20	52	20	60	25	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{TAA}	Access time from address (test mode)	35		40		45		50		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		55		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		105		ns
t_{REF}	Refresh time interval		16		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	2	50	ns

NOTE 11: The maximum value is specified only to guarantee access time.

device symbolization

The specifications contained in this data sheet are applicable to all TM4100GBD8s symbolized as shown in Figure 1. Please note that the location of the part number may vary.

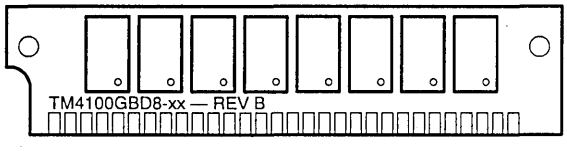


Figure 1. Device Symbolization

This Data Sheet is Applicable to All TM124BBK32s Symbolized with Revision "B" and Subsequent Revisions as Described on Page 6-79.

- **TM124BBK32 . . . 1 048 576 × 32 Organization**
- **Single 5-V Power Supply**
- **72-pin Single-In-Line Package (SIP) – Leadless Module for Use With Sockets**
- **Utilizes Eight 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Distributed Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines, In Four Blocks**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)	V_{CC} TOLERANCE
'124BBK32-6	60 ns	15 ns	110 ns	±5%
'124BBK32-70	70 ns	18 ns	130 ns	±10%
'124BBK32-80	80 ns	20 ns	150 ns	±10%
'124BBK32-10	100 ns	25 ns	180 ns	±10%

- **Low Power Dissipation**
- **Operating Free-Air-Temperature Range . . . 0°C to 70°C**

description

The TM124BBK32 is a 33 526K (dynamic) random-access memory organized as four times 1 048 576 × 8 in a 72-pin single-in-line package (SIP). The SIP is composed of eight TMS44400, 1 048 576 × 4-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), mounted on a substrate with decoupling capacitors mounted beneath the SOJs. Each TMS44400 is described in the TMS44400 data sheet.

The TM124BBK32 SIP is available in the single-sided BK leadless module for use with sockets.

The TM124BBK32 SIP features $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns. This device is rated for operation from 0°C to 70°C

operation

The TM124BBK32 operates as eight TMS44400DMs connected as shown in the functional block diagram. Refer to the TMS44400 data sheet for details of operation. The common I/O feature of the TM124BBK32 dictates the use of early write cycles to prevent contention on D and Q.

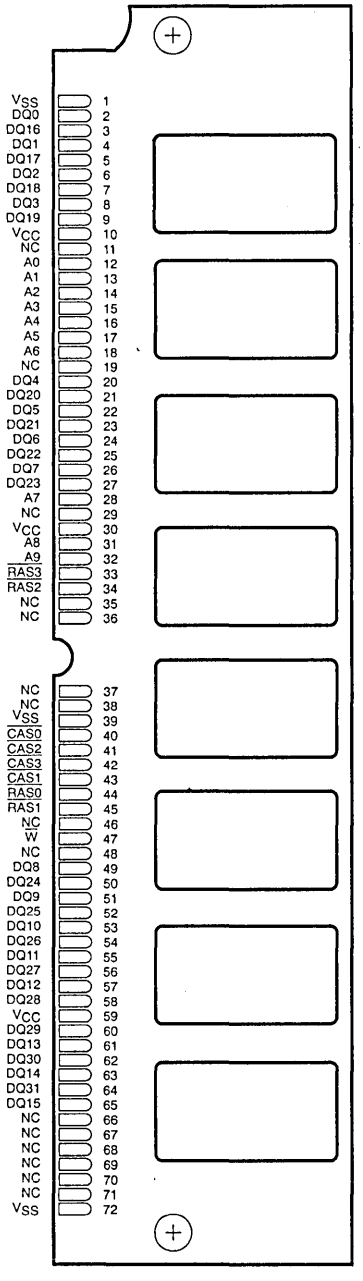
specifications

Refresh period is extended to 16 milliseconds and, during this period, each of the 1024 rows must be strobed with $\overline{RAS}$ in order to retain data. A0-A9 address lines must be refreshed every 16 ms as required by the TMS44400 DRAM. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

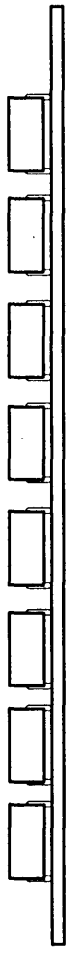
single-in-line package and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and gold plate on top of copper

BK Single-In-Line Package†
(Top View)



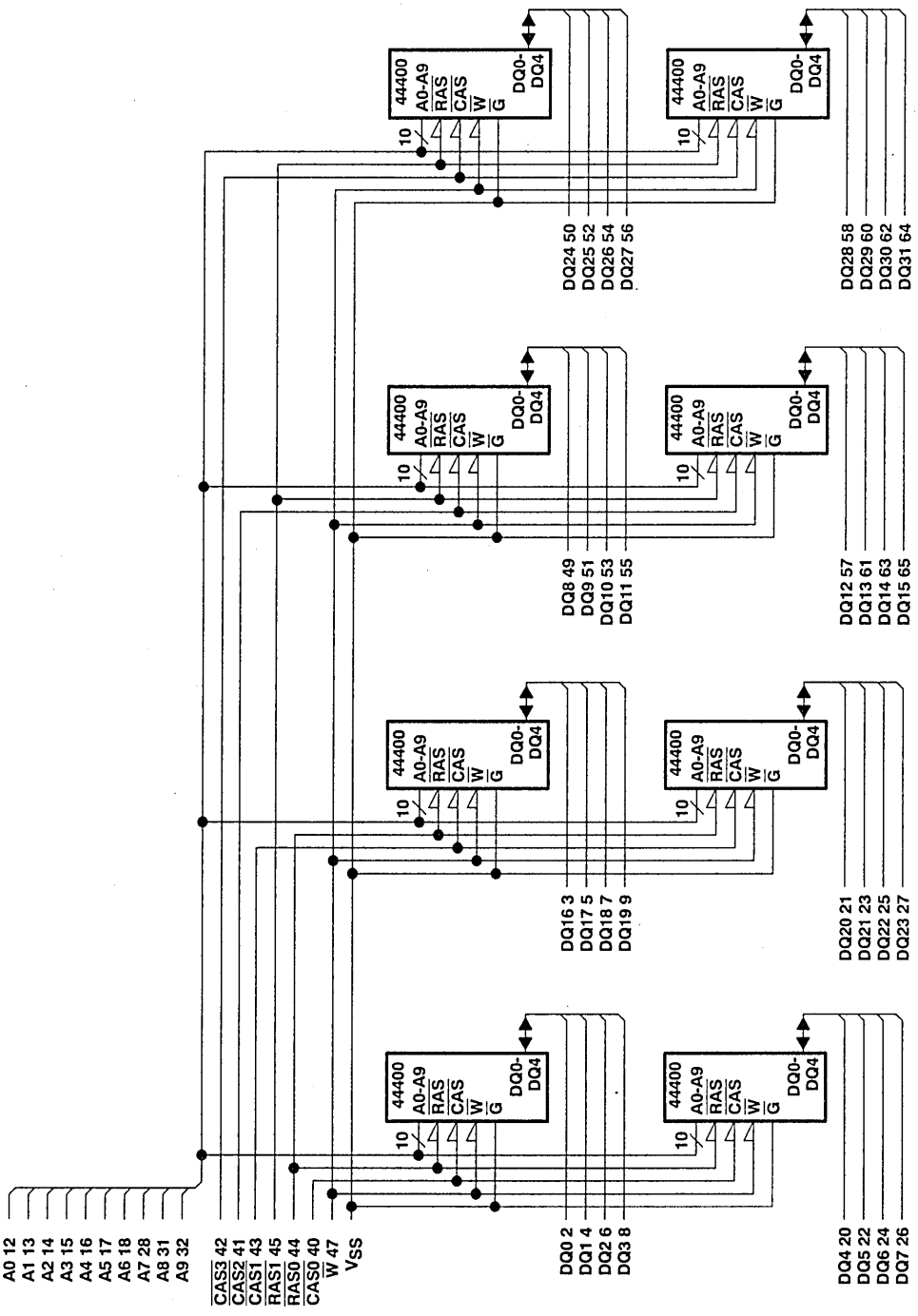
TM124BBK32†
(Side View)



PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS0}$-$\overline{CAS3}$	Column-Address Strobe
DQ0-DQ31	Data In/Data Out
NC	No Internal Connection
$\overline{RAS0}$-$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

† The packages shown here are for pinout reference only and are not drawn to scale.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 8 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (TM124BBK32-6)	4.75	5	5.25	V
V_{CC}	Supply voltage (TM124BBK32-70/-80/-10)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124BBK32-6		'124BBK32-70		'124BBK32-80		'124BBK32-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 to V_{CC}		±10		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10		±10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		760		680		600		520	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		16		16		16		16	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		8		8		8		8	
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ · high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		760		680		600		520	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		560		480		400		320	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature f = 1 MHz (see Note 5)

		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		40	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$		28	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$		14	pF
$C_{i(W)}$	Input capacitance, write-enable input		56	pF
$C_{o(DQ)}$	Output capacitance on DQ pins		7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124BBK32-6		'124BBK32-70		'124BBK32-80		'124BBK32-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	0	25	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended range of supply voltage and operating free-air temperature

		'124BBK32-6		'124BBK32-70		'124BBK32-80		'124BBK32-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle	110		130		150		180		ns
t_{PC}	Page-mode read or write cycle time	40		45		50		55		ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{WP}	Write pulse duration	15		15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		20		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 7)	50		55		60		75		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 7)	50		55		60		75		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	10		15		15		20		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 8)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 8)	0		0		0		0		ns

NOTES: 7. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended range of supply voltage and operating free-air temperature (concluded)

		'124BBK32-6		'124BBK32-70		'124BBK32-80		'124BBK32-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		20		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low	50		55		60		75		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		0		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 9)	20	45	20	52	20	60	25	75	ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 10)	15		15		20		20		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 10)	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address	15	30	15	35	15	40	20	50	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 10)	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{WTS}	$\overline{W}$-low setup time (test mode only)	10		10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		10		ns
t_{TAA}	Access time from address (test mode)	35		40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		105		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		55		ns
t_{REF}	Refresh time interval		16		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	2	50	ns

NOTES: 9. Maximum value specified only to guarantee access time.
10. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

device symbolization

The specifications contained in the data sheet are applicable to all TM124BBK32s symbolized as shown in Figure 1. Please note that the location of the part number may vary.

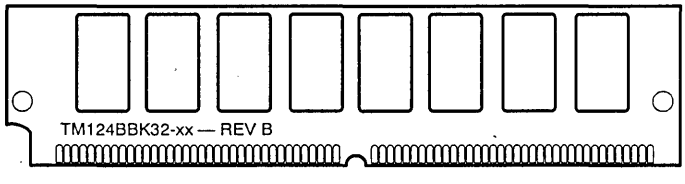


Figure 1. Device Symbolization

REV A — SMMS409A — JANUARY 1990 — REVISED JANUARY 1991

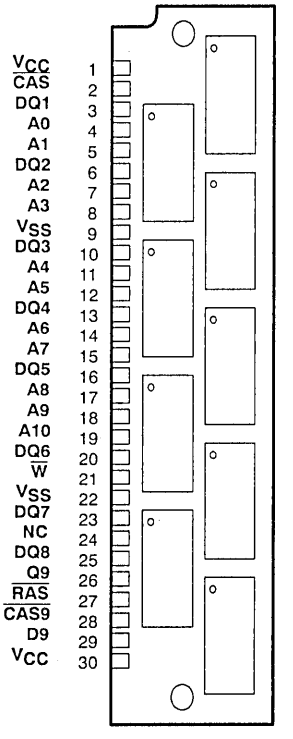
This Data Sheet is Applicable to All TM4100EBD9s Symbolized with Revision "B" and Subsequent Revisions as Described on Page 6-87.

- **4 194 304 × 9 Organization**
- **30-Pin Single-In-Line Package (SIP) — Leadless Module for Use with Sockets**
- **Utilizes Nine 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Single 5-V Power Supply**
- **Long refresh period . . . 16 ms (1024) cycles**
- **All Inputs, Outputs, and Clocks Fully TTL Compatible**
- **3-State Output**
- **Performance of Unmounted RAMs:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
TMS44100-6	60 ns	15 ns	110 ns
TMS44100-70	70 ns	18 ns	130 ns
TMS44100-80	80 ns	20 ns	150 ns
TMS44100-10	100 ns	25 ns	180 ns

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free Air Temperature . . . 0°C to 70°C**

BD Single-In-Line Package†
(Top View)



†The package shown is for pinout reference only.

PIN NOMENCLATURE	
A0-A10	Address Inputs
$\overline{CAS}$, $\overline{CAS9}$	Column-Address Strobe
DQ1-DQ8	Data In / Data Out
D9	Data In
NC	No Connection
Q9	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4100EBD9 is 36 864K dynamic random-access memory module organized as 4 194 304 bits [bit nine (D9, Q9) is generally used for parity and is controlled by $\overline{CAS9}$] in a 30-pin single-in-line (SIP) package.

The SIP is composed of nine TMS44100, 4 194 304 × 1 bit dynamic RAMs, each in a 20/26-lead plastic small-outline J-lead package (SOJ), mounted on a substrate with decoupling capacitors.

The TM4100EBD9 SIP is available in the BD single-sided, leadless module for use with sockets.

The TM4100EBD9 SIP is characterized for operation from 0°C to 70°C.

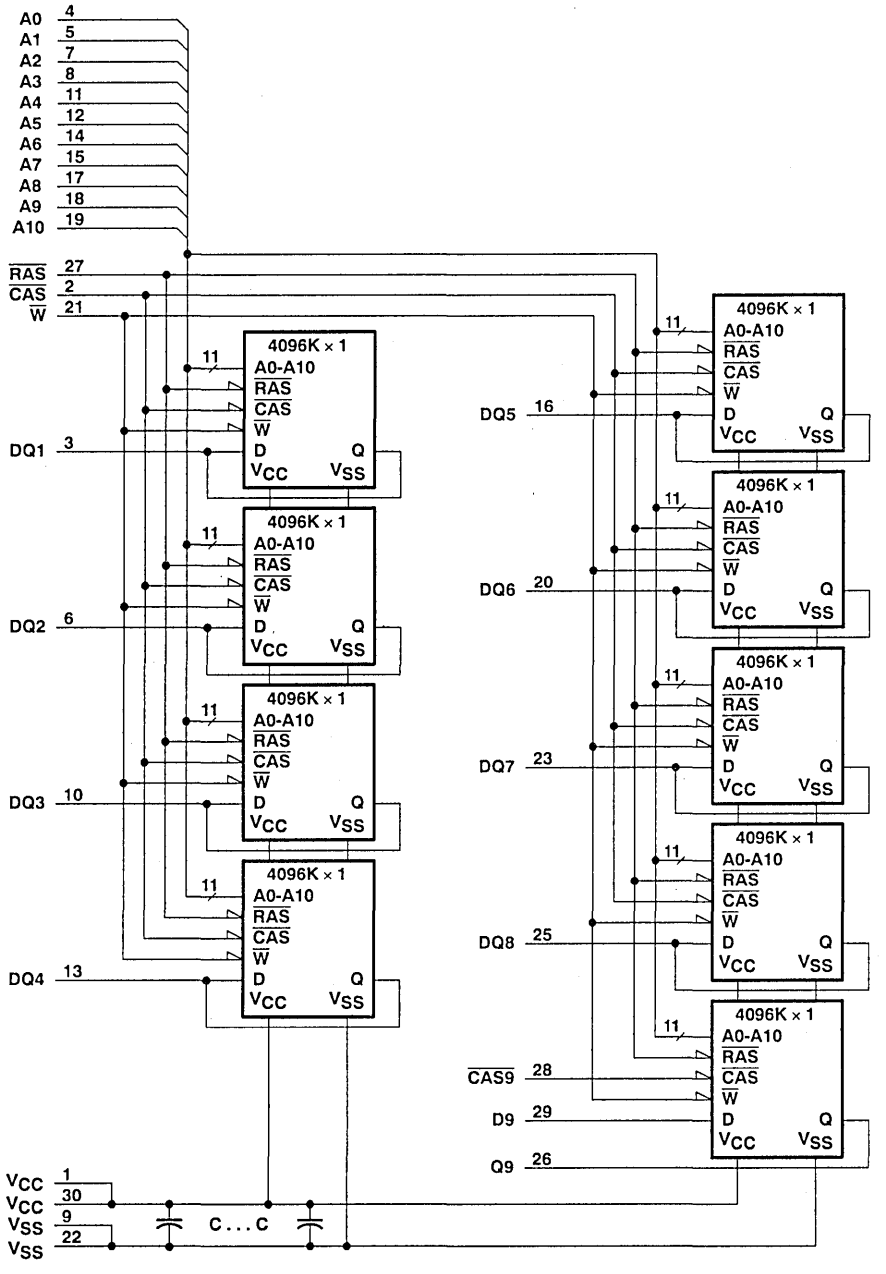
operation

The TM4100EBD9 operates as nine TMS44100s connected as shown in the functional block diagram. Refer to the TMS4100 data sheet for details of its operation. The common I/O feature of the TM4100EBD9 dictates the use of early write cycles to prevent contention on D and Q.

single-in-line package and components

PC substrate: 1,27 (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate (or coat) on top of copper

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation: ..... 9 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (TM4100EBD9-6)	4.75	5	5.25	V
V_{CC}	Supply voltage (TM4100EBD0-70/-80/-10)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'4100EBD9-6		'4100EBD9-70		'4100EBD9-80		'4100EBD9-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10		±10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		855		765		675		585	mA
I_{CC2}	Standby Current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		18		18		18		18	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		9		9		9		9	
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		855		765		675		585	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		630		540		450		360	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		45	pF
$C_{i(D)}$	Input capacitance, data input (D9 only)		5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		63	pF
$C_{i(W)}$	Input capacitance, write-enable input		63	pF
$C_{o(DQ)}$	Output capacitance (DQ1-DQ8)		12	pF
C_o	Output capacitance (Q9 only)		7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'4100EBD9-6		'4100EBD9-70		'4100EBD9-80		'4100EBD9-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 5)	0	15	0	18	0	20	0	25	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4100EBD9-6		'4100EBD9-70		'4100EBD9-80		'4100EBD9-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		180		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		55		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns

Continued next page.

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'4100EBD9-6		'4100EBD9-70		'4100EBD9-80		'4100EBD9-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTS}	$\overline{W}$-low setup time (test mode only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		75		ns
t_{DH}	Data hold time (see Note 10)	10		15		15		20		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		75		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	0		0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		75		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	30	15	35	15	40	20	50	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	52	20	60	25	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{TAA}	Access time from address (test mode)	35		40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		105		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		55		ns
t_{REF}	Refresh time interval		16		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	2	50	ns

NOTES: 10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
12. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. The maximum value is specified only to guarantee access time.

device symbolization

The specifications contained in this data sheet are applicable to all TM4100EBD9s symbolized as shown in Figure 1. Please note that the location of the part number may vary.

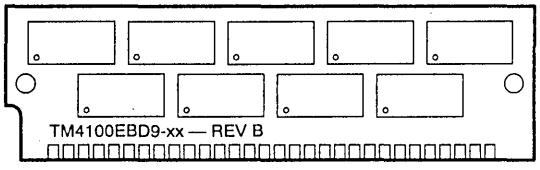


Figure 1. Device Symbolization

This Data Sheet is Applicable to All TM124MBK36As Symbolized with Revision "B" and Subsequent Revisions as Described on Page 6-95.

- **TM124MBK36A . . . 1 048 576 × 36 Organization**
- **Single 5-V Power Supply (±5% Tolerance)**
- **72-pin Single-In-Line Package (SIP)**
  – Leadless Module for Use With Sockets
- **Utilizes Eight 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Four 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines, in Four Blocks**
- **Separate $\overline{RAS}$ Control for Eighteen Data-In and Data-Out Lines, in Two Blocks**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
TM124MBK36A-6	60 ns	15 ns	30 ns	110 ns
TM124MBK36A-7	70 ns	18 ns	35 ns	130 ns
TM124MBK36A-8	80 ns	20 ns	40 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**
- **Presence Detect**

ADVANCE INFORMATION

description

The TM124MBK36A is a 37 748K (dynamic) random-access memory organized as four times 1 048 576 × 9 [bit 9 is generally used for parity] in a 72-pin single-in-line package (SIP). The SIP is composed of eight TMS44400DM or TMS44400DJ, 1 048 576 × 4-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), and four TMS4C1024DJ, 1 048 576 × 1-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs) mounted on a substrate with decoupling capacitors. Each TMS44400DM or TMS44400DJ and TMS4C1024DJ is described in the TMS44400 and TMS4C1024 data sheets (respectively).

The TM124MBK36A SIP is available in a double-sided BK leadless module for use with sockets.

The TM124MBK36A SIP features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is rated for operation from 0°C to 70°C

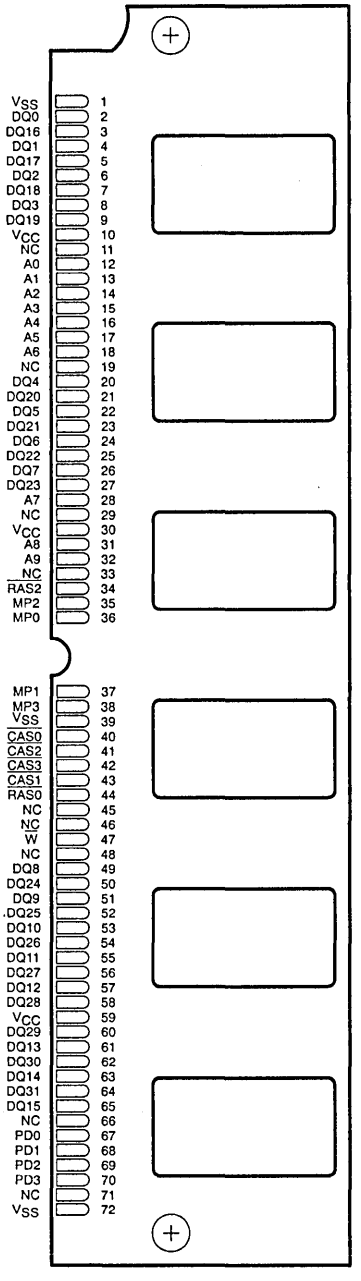
operation

The TM124MBK36A operates as eight TMS44400DMs or TMS44400DJs and four TMS4C1024DJs connected as shown in the functional block diagram and Table 1. Refer to the TMS44400 and TMS4C1024 data sheets for details of operation. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

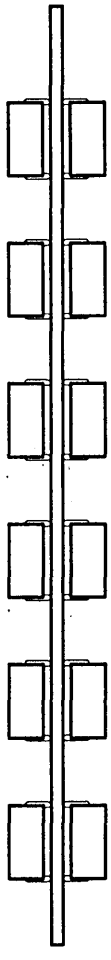
specifications

Refresh period is extended to 16 milliseconds and, during this period, each of the 1024 rows must be strobed with $\overline{RAS}$ in order to retain data. Address line A9 must be used as most significant refresh address line (lowest frequency) to assure correct refresh for both TMS44400 and TMS4C1024. A0-A8 address lines must be refreshed every 8 ms as required by the TMS4C1024 DRAM. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

BK Single-In-Line Package†
(Top View)



TM124MBK36A†
(Side View)



PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS0}$-$\overline{CAS3}$	Column-Address Strobe
DQ0-DQ31	Data In/Data Out
MP0-MP3	Parity
NC	No Connection
PD0-PD3	Presence Detects
$\overline{RAS0}$, $\overline{RAS2}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

† The package shown here is for pinout reference only and is not drawn to scale.

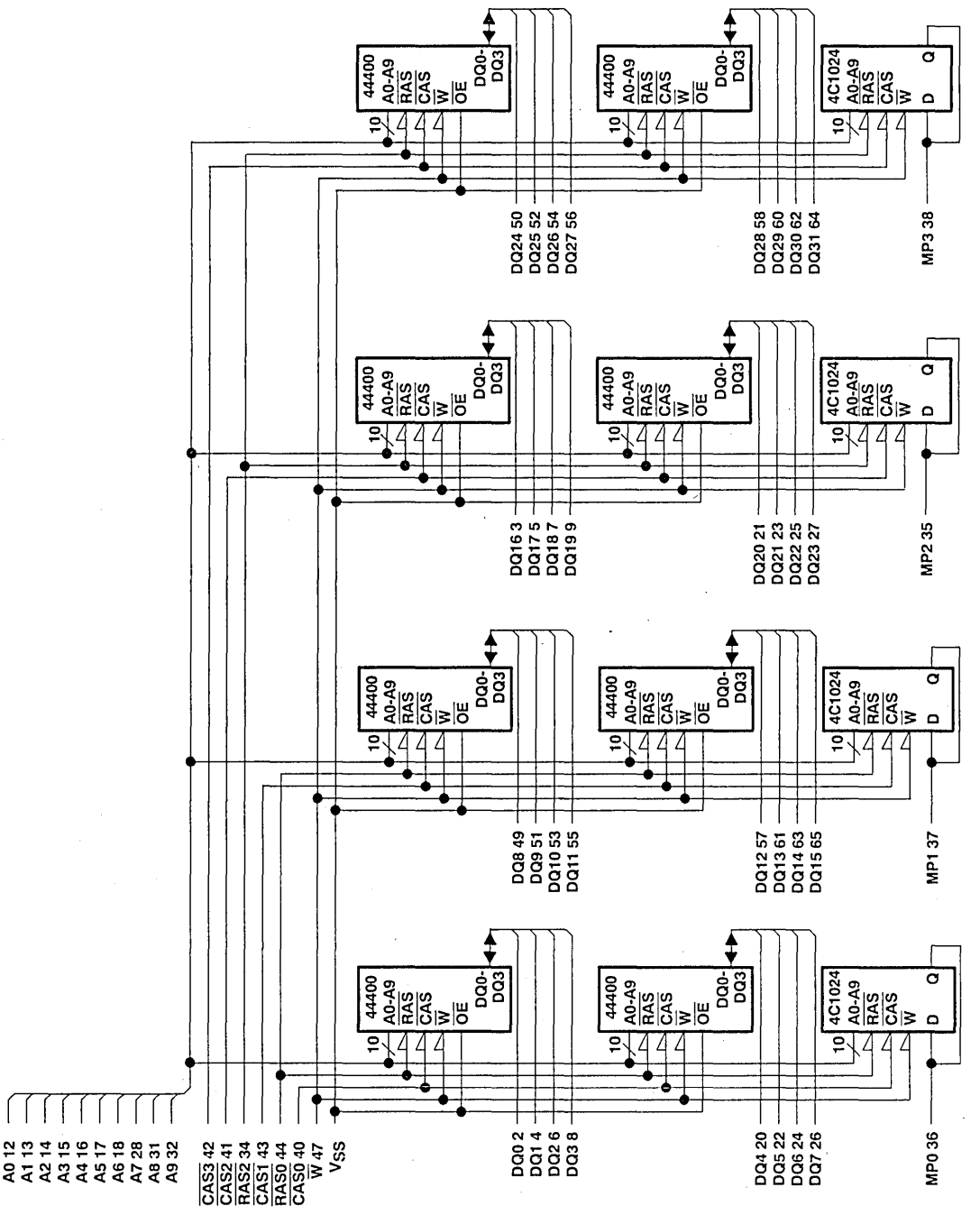
Table 1. Connection Table

DATA BLOCK	$\overline{RASx}$	$\overline{CASx}$
DQ-DQ7 MP0	$\overline{RAS0}$	$\overline{CAS0}$
DQ8-DQ15 MP1	$\overline{RAS0}$	$\overline{CAS1}$
DQ16-DQ23 MP2	$\overline{RAS2}$	$\overline{CAS2}$
DQ24-DQ31 MP3	$\overline{RAS2}$	$\overline{CAS3}$

single-in-line package and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and gold plate on top of copper

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 12 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124MBK36A-6		'124MBK36A-7		'124MBK36A-8		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 120		± 120		± 120	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		1140		1000		900	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		24		24		24	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		12		12		12	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1120		1000		880	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		840		720		600	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			60	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs			19	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs			38	pF
$C_{i(W)}$	Input capacitance, write-enable input			76	pF
$C_{o(DQ)}$	Output capacitance on DQ pins			7	pF
$C_{o(MP)}$	Output capacitance on MP pins			12	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124MBK36A-6		'124MBK36A-7		'124MBK36A-8		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124MBK36A-6		'124MBK36A-7		'124MBK36A-8		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns

NOTES: 7. All cycles assume t_T = 5 ns.
8. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'124MBK36A-6		'124MBK36A-7		'124MBK36A-8		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{DH}	Data hold time	10		15		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		12		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 10)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 10)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 11)	15	30	15	35	17	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 11)	20	45	20	52	22	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	3	50	3	50	3	50	ns

NOTES: 9. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. The maximum value is specified only to guarantee access time.

device symbolization

The specifications contained in this data sheet are applicable to all TM124MBK36As symbolized as shown in Figure 1. Please note that the location of the part number may vary.

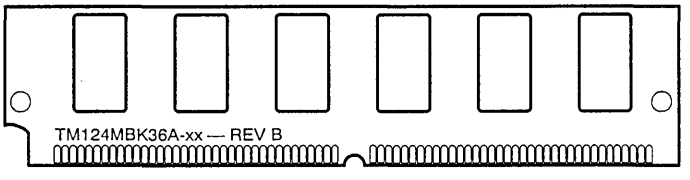


Figure 1. Device Symbolization

ADVANCE INFORMATION

This Data Sheet is Applicable to All TM124MBK36Bs Symbolized with Revision "B" and Subsequent Revisions as Described on Page 6-103.

- **TM124MBK36B . . . 1 048 576 × 36 Organization**
- **Single 5-V Power Supply (5% Tolerance)**
- **72-pin Single-In-Line Package (SIP)**
  – Leadless Module for Use With Sockets
- **Utilizes Eight 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages and One 4-Megabit Quad-$\overline{CAS}$ Dynamic RAM in a Plastic Small-Outline J-Lead (SOJ) Package**
- **Long Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines, in Four Blocks**
- **Enhanced Page Mode Operation with $\overline{CAS}$-Before-$\overline{RAS}$, $\overline{RAS}$-Only, and Hidden Refresh**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'124MBK36B-6	60 ns	30 ns	15 ns	110 ns
'124MBK36B-7	70 ns	35 ns	18 ns	130 ns
'124MBK36B-8	80 ns	40 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air-Temperature Range . . . 0°C to 70°C**
- **Presence Detect**

ADVANCE INFORMATION

description

The TM124MBK36B is a 37 748K (dynamic) random-access memory organized as four times 1 048 576 × 9 [bit 9 is generally used for parity] in a 72-pin single-in-line package (SIP). The SIP is composed of eight TMS44400DM or TMS44400DJ, 1 048 576 × 4-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), and one TMS44460DJ, 1 048 576 × 4-bit Quad-$\overline{CAS}$ dynamic RAM, in a 24/26-lead plastic small-outline J-lead package (SOJ) mounted on a substrate with decoupling capacitors. Each TMS44400DM or TMS44400DJ and TMS44460DJ is described in the TMS44400 and TMS44460 data sheets (respectively).

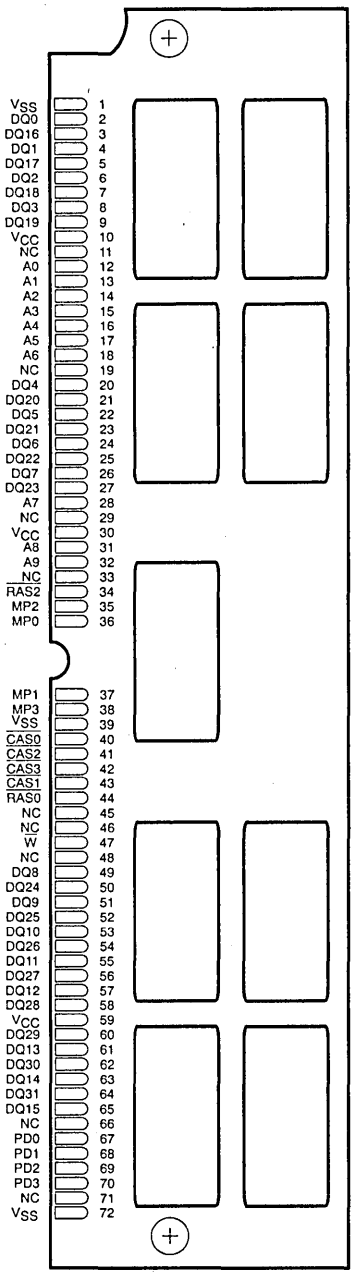
The TM124MBK36B SIP is available in the single-sided BK leadless module for use with sockets.

The TM124MBK36B SIP features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is rated for operation from 0°C to 70°C

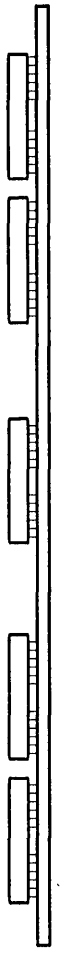
operation

The TM124MBK36B operates as eight TMS44400DMs or TMS44400DJs and one TMS44460DJ connected as shown in the functional block diagram and Table 1. The parity bits MP0-MP3 are provided by the TMS44460DJ and are controlled by $\overline{RAS2}$. To ensure proper parity bit operation all memory accesses should include a $\overline{RAS2}$ pulse. Refer to the TMS44400 and TMS44460 data sheets for details of operation. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

BK Single-In-line Package† (Top View)



TM124MBK36B† (Side View)



PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS0}$-$\overline{CAS3}$	Column-Address Strobe
DQ0-DQ31	Data In/Data Out
MP0-MP3	Parity
NC	No Connection
PD0-PD3	Presence Detects
$\overline{RAS0}$, $\overline{RAS2}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

† The package shown here is for pinout reference only and is not drawn to scale.

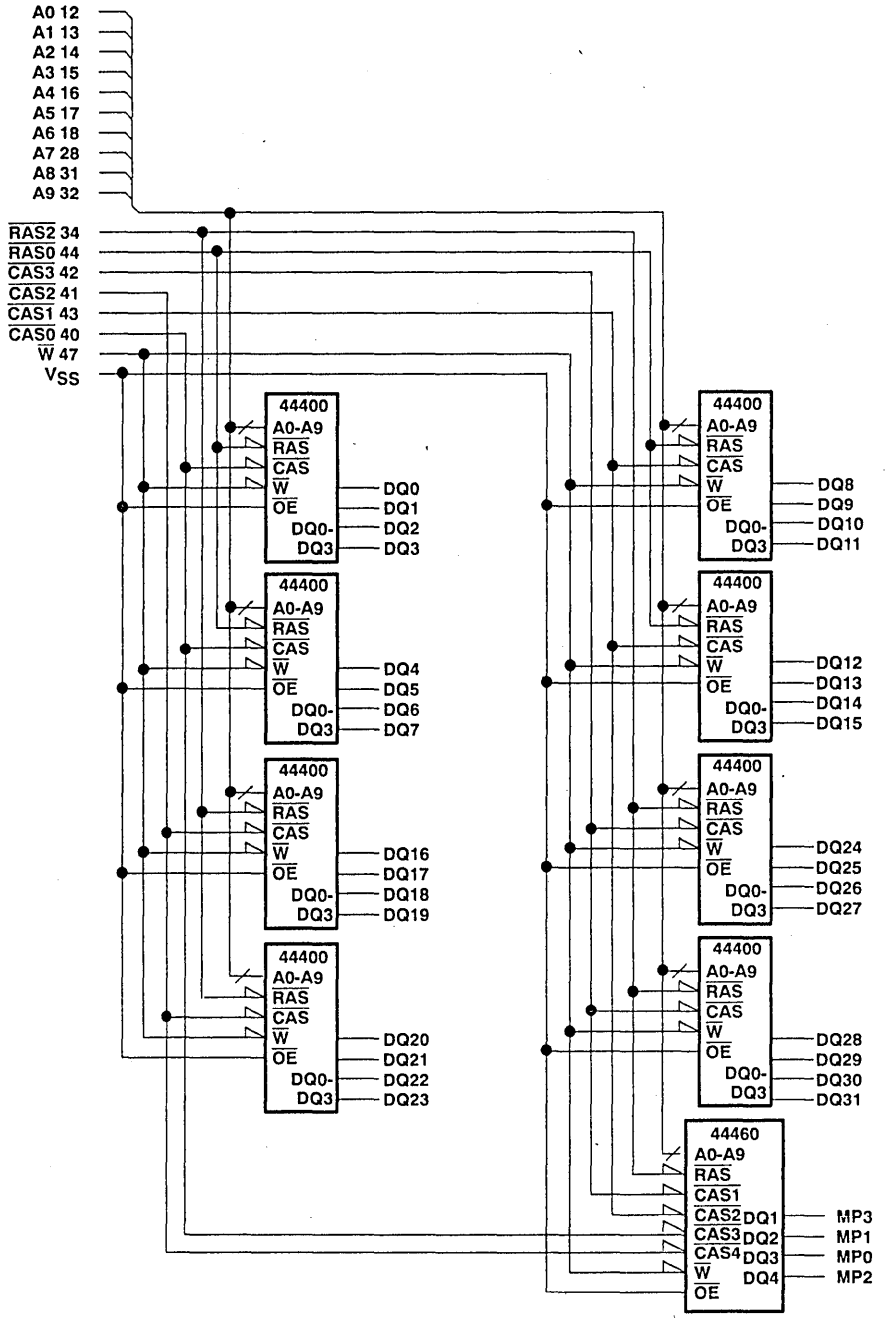
Table 1. Connection Table

DATA BLOCK	$\overline{RAS}x$	$\overline{CAS}x$
DQ0-DQ7	$\overline{RAS0}$	$\overline{CAS0}$
MP0	$\overline{RAS2}$	$\overline{CAS0}$
DQ8-DQ15	$\overline{RAS0}$	$\overline{CAS1}$
MP1	$\overline{RAS2}$	$\overline{CAS1}$
DQ16-DQ23	$\overline{RAS2}$	$\overline{CAS2}$
MP2	$\overline{RAS2}$	$\overline{CAS2}$
DQ24-DQ31	$\overline{RAS2}$	$\overline{CAS3}$
MP3	$\overline{RAS2}$	$\overline{CAS3}$

single-in-line package and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and gold plate on top of copper

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 9 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124MBK36B-6		'124MBK36B-7		'124MBK36B-8		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 90		± 90		± 90	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		855		765		675	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		18		18		18	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		9		9		9	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		855		765		675	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		630		540		450	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			45	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs			35	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs			21	pF
$C_{i(W)}$	Input capacitance, write-enable input			63	pF
$C_{o(DQ)}$	Output capacitance on DQ pins			7	pF
$C_{o(MP)}$	Output capacitance on MP pins			7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124MBK36B-6		'124MBK36B-7		'124MBK36B-8		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{AA}	Access time from column-address		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124MBK36B-6		'124MBK36B-7		'124MBK36B-8		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{WC}	Write cycle time	110		130		150		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns

NOTES: 7. All cycles assume t_T = 5 ns.
8. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'124MBK36B-6		'124MBK36B-7		'124MBK36B-8		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{DH}	Data hold time	10		15		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{CLCH}	Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high	5		5		5		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 10)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 10)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 11)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 11)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

NOTES: 9. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. The maximum value is specified only to guarantee access time.

ADVANCE INFORMATION

device symbolization

The specifications contained in this data sheet are applicable to all TM124MBK36Bs symbolized as shown in Figure 1. Please note that the location of the part number may vary.

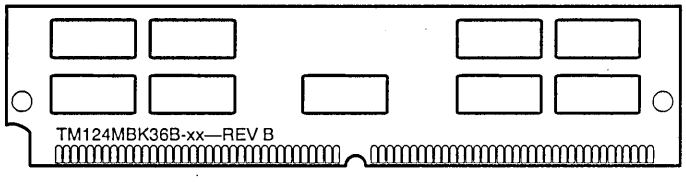


Figure 1. Device Symbolization

TEXAS INSTRUMENTS MEMORY CARDS

Overview

With smaller and more dense end-equipment systems emerging in the marketplace, the needs of memory customers are changing. Memories need to be smaller and more dense to fit in these systems. To meet this need, Texas Instruments has developed a compact "memory card".

This new packaging technology allows several memory devices to be surface-mounted together on a memory card substrate with a two-piece pin-and-socket edge connector. The finished card is about the size of a credit card. Current versions can hold as many as 12 devices, offering customers high-density memory in a small package.

Memory Card Evolution

Texas Instruments began working on the memory card concept a few years ago when a need arose for compact font storage solution using one-time-programmable PROMs (OTPs). Since then, the needs and applications for memory cards have expanded, creating the need for an industry standard. TI participates as a member of various standards organizations to try to meet this need.

Both the Japan Electronic Industry Development Association (JEIDA) and the Personal Computer Memory Card International Association (PCMCIA) have agreed to accept the same standard to encourage the use of IC memory cards. Their guidelines propose that the standard IC card be 85.6 mm × 54 mm in size with a two-row 68-pin connector that will transfer data in an MS-DOS format. The Type I memory card guideline is 3.3 mm thick. This standard was needed so that memory cards can be interchanged between systems (i.e., desktop PC to laptop PC).

JEDEC format also is 85.6 mm × 54 mm in size, but uses a 60-pin, two-piece connector with 3.4 mm or 3.5 mm card thickness.

Texas Instruments offers standard memory cards that follow the JEIDA and PCMCIA Type I memory card standards or the JEDEC format.

Individual device packaging improvements were needed to allow for the evolution of memory cards. Thin and light-weight packages that did not compromise device functionality had to be developed. To meet these requirements, TI developed the ThinSOJ, ThinSOP, QFP, and SQFP (small quad-flat package) packages to surface mount the individual devices in the compact memory card.

Applications

There are many potential applications for memory cards. These credit-card size storage devices are often used in place of floppy-disk drives in portable and hand-held computers since they reduce the cost and bulk. Below are a few of the other applications for memory cards:

– ***Computers***
- Personal Computers
- Notebook/Pocket Computers
- Pocket Diaries

– ***Office Equipment/Peripherals***
- Facsimile and Copy Machines (Usage Control)
- Printer and Typewriter Fonts
- Word Processors (Text Storage)

– ***Sales Automation***
- Hand-held terminals (Inventory Control)
- Electronic Cash Register

– ***Factory Automation***
- Machinery Control
- Programmable Controllers (Process Control Data Storage)

Not only are there several segmented applications for memory cards, but some card technologies are better suited for different applications. OTP memory cards are ideal for font storage; DRAM memory cards are good for PC, facsimile machine, and printer applications; and Flash EEPROMs can be used in "solid-state" disk applications.

Product Offering

TI has the capability to produce many standard and custom memory cards to meet the needs of our customers.

Currently, TI offers standard cards made with OTPs and DRAMs. Flash EEPROM versions are in development. Drivers or decoders, as applicable, are included on these memory cards to simplify system design. The table below lists a few of TI's most popular OTP memory cards.

OTP PROM MEMORY CARD SELECTION GUIDE

DENSITY (KB)	BIT WIDTH (BITS)	ACCESS TIME	CARD SIZE	CONNECTOR TYPE
64	16	200 ns	85.6 mm × 54 mm × 3.5 mm	60-pin, two-piece
128	16	200 ns	85.6 mm × 54 mm × 3.5 mm	60-pin, two-piece
256	16	200 ns	85.6 mm × 54 mm × 3.5 mm	60-pin, two-piece
512	16	200 ns	85.6 mm × 54 mm × 3.5 mm	60-pin, two-piece
32	8	200 ns	85.6 mm × 54 mm × 3.5 mm	60-pin, two-piece
64	8	200 ns	85.6 mm × 54 mm × 3.5 mm	60-pin, two-piece
128	8	200 ns	85.6 mm × 54 mm × 3.5 mm	60-pin, two-piece
256	8	200 ns	85.6 mm × 54 mm × 3.5 mm	60-pin, two-piece

Custom memory cards can be designed and developed for customers with a high-volume specific application. These cards can contain additional IC circuitry to further enhance the memory card functionality.

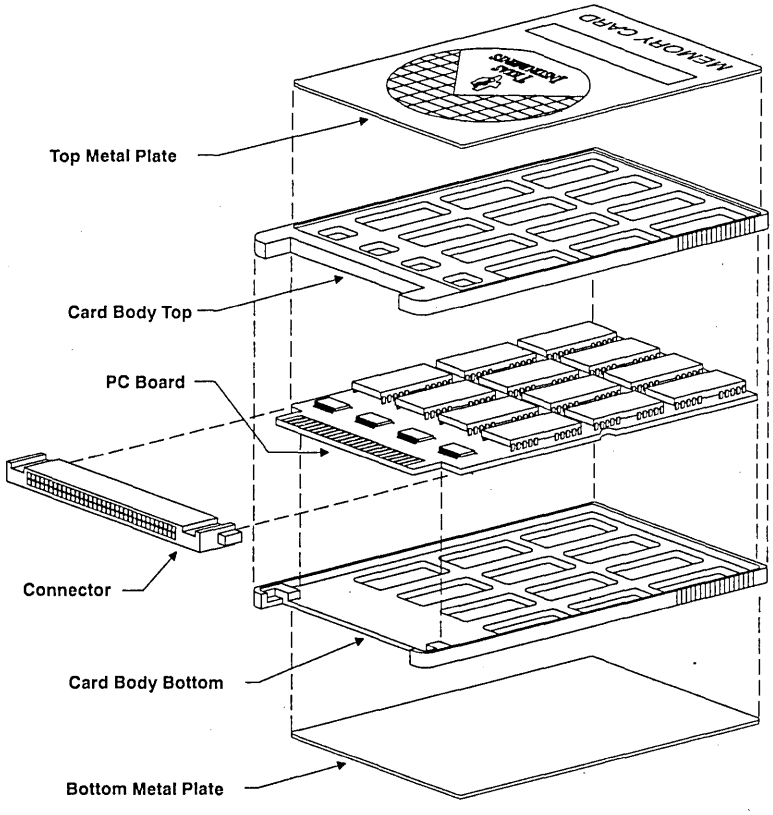
The figure on the next page illustrates the typical construction of a memory card.

Quality and Reliability

TI is committed to total quality control. There are quality checks at every step of the design and production processes to make sure that TI memory products meet or exceed TI and industry quality standards.

All individual components are carefully tested as standard TI product prior to assembly on the memory card. After assembly, the memory card is then tested as a complete memory array.

Figure 1. Memory Card Construction



TMS27C128 131 072-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC128 131 072-BIT PROGRAMMABLE READ-ONLY MEMORY

REV A — SMLS128D — OCTOBER 1984 — REVISED JANUARY 1991

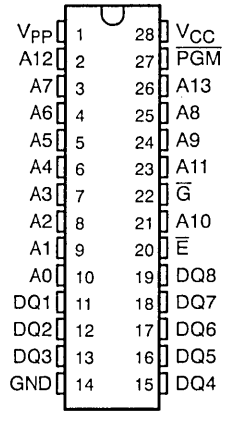
This Data Sheet is Applicable to All TMS27C128s and TMS27PC128s Symbolized with Code "B" as Described on Page 7-12.

- **Organization . . . 16K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 128K MOS ROMs, PROMs, and EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**

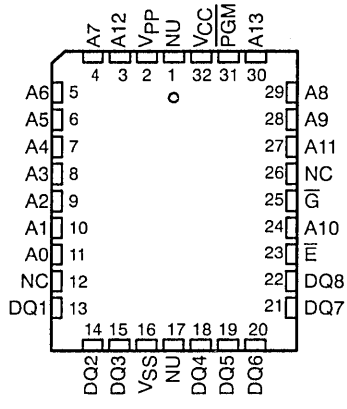
V_{CC} ± 5%	V_{CC} ± 10%	
'27C128-100		100 ns
'27C128-120	'27C128-12	120 ns
'27C/PC128-1	'27C/PC128-15	150 ns
'27C/PC128-2	'27C/PC128-20	200 ns
'27C/PC128	'27C/PC128-25	250 ns

- **Power Saving CMOS Technology**
- **Very High-Speed SNAP! Pulse Programming**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation (V_{CC} = 5.25 V)**
  - **— Active . . . 158 mW Worst Case**
  - **— Standby . . . 1.4 mW Worst Case (CMOS Input Levels)**
- **PEP4 Version Available With 168 Hour Burn-in and Choices of Operating Temperature Ranges**
- **128K EPROM Available With MIL-STD-883C Class B High-Reliability Processing (SMJ27C128)**

J and N Packages
(Top View)



FM Package
(Top View)



description

The TMS27C128 series are 131 072-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC128 series are 131 072-bit, one-time, electrically programmable read-only memories.

PIN NOMENCLATURE	
A0-A13	Address Inputs
$\overline{E}$	Chip Enable/Powerdown
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
NU	Make No External Connection
$\overline{PGM}$	Program
DQ1-DQ8	Inputs (programming)/Outputs
V_{CC}	5-V Power Supply
V_{PP}	12-13 V Programming Power Supply

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

REV A — SMLS128D — OCTOBER 1984 — REVISED JANUARY 1991

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C128 and the TMS27PC128 are pin compatible with 28-pin 128K MOS ROMs, PROMs, and EPROMs.

The TMS27C128 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C128 is offered with two operating temperature ranges of 0°C to 70°C and – 40°C to 85°C (TMS27C128-_ _JL and TMS27C128-_ _JE, respectively). The TMS27C128 is also offered with 168-hour burn-in temperature ranges (TMS27C128-_ _JL4 and TMS27C128-_ _JE4, respectively). (See table below).

The TMS27PC128 PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC128 is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix). The TMS27PC128 is also offered with two operating temperature ranges of 0°C to 70°C and – 40°C to 85°C (TMS27PC128-_ _NL, TMS27PC128-_ _NE and TMS27PC128-_ _FML, TMS27PC128-_ _FME respectively). The TMS27PC128 is also offered with 168 hour burn-in temperature ranges (TMS27PC128-_ _NL4, TMS27PC128-_ _NE4 and TMS27PC128-_ _FML4, TMS27PC128-_ _FME4, respectively). (See table below).

All package styles conform to JEDEC standards.

EPROM AND PROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR OPERATING TEMPERATURE RANGES WITH PEP4 168 HR. BURN-IN	
	0°C TO 70°C	– 40°C TO 85°C	0°C TO 70°C	– 40°C TO 85°C
TMS27C128-XXX	JL	JE	JL4	JE4
TMS27PC128-XXX	NL	NE	NL4	NE4
TMS27PC128-XXX	FML	FME	FML4	FME4

These EPROMs and PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 12-13 V supply is needed for programming . All programming signals are TTL level. These devices are programmable by using the SNAP! Pulse programming algorithm.The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of two seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation listed in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X	V_{IH}	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ1-DQ8	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	83

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C128s or TMS27PC128s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ1 through DQ8.

latchup immunity

Latchup immunity on the TMS27C128 and TMS27PC128 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family"*, available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL or CMOS signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure (TMS27C128)

Before programming, the TMS27C128 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). EPROM erasure before programming is necessary to assure that all bits are at the logic high level. Logic lows are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light. The recommended minimum ultraviolet light exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C128, the window should be covered with an opaque label.

initializing (TMS27PC128)

The one-time programmable TMS27PC128 PROM is provided with all bits at the logic high level. The logic lows are programmed into the desired locations. Logic lows programmed into a PROM cannot be erased.

SNAP! Pulse programming

The 128K EPROM and PROM are programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which programs in a nominal time of two seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins DQ1 to DQ8. Once addresses and data are stable, $\overline{PGM}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., A0 = V_{IL} accesses the manufacturer code, which is output on DQ1-DQ8; A0 = V_{IH} accesses the device code, which is output on DQ1-DQ8. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit DQ8. The manufacturer code for these devices is 97, and the device code is 83.

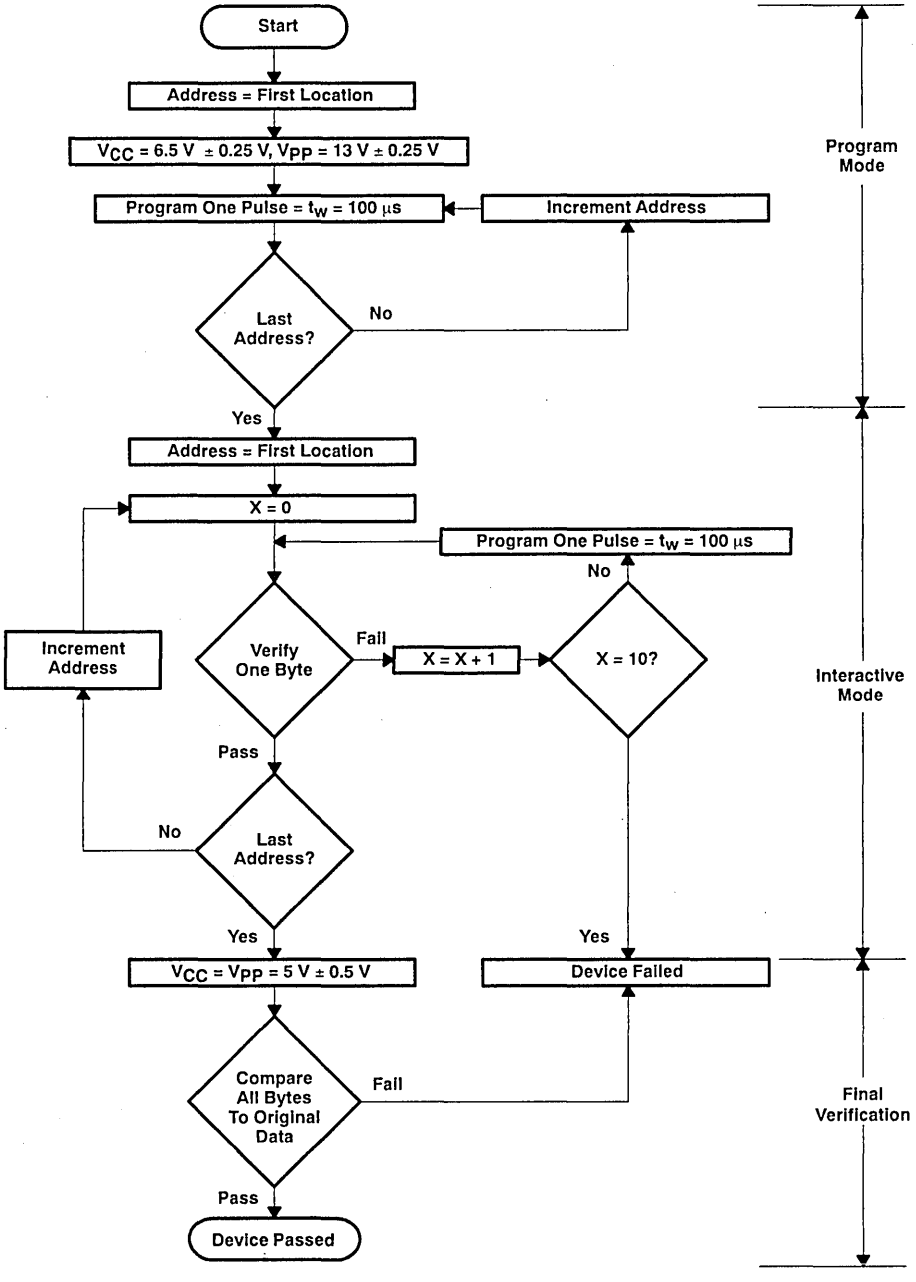
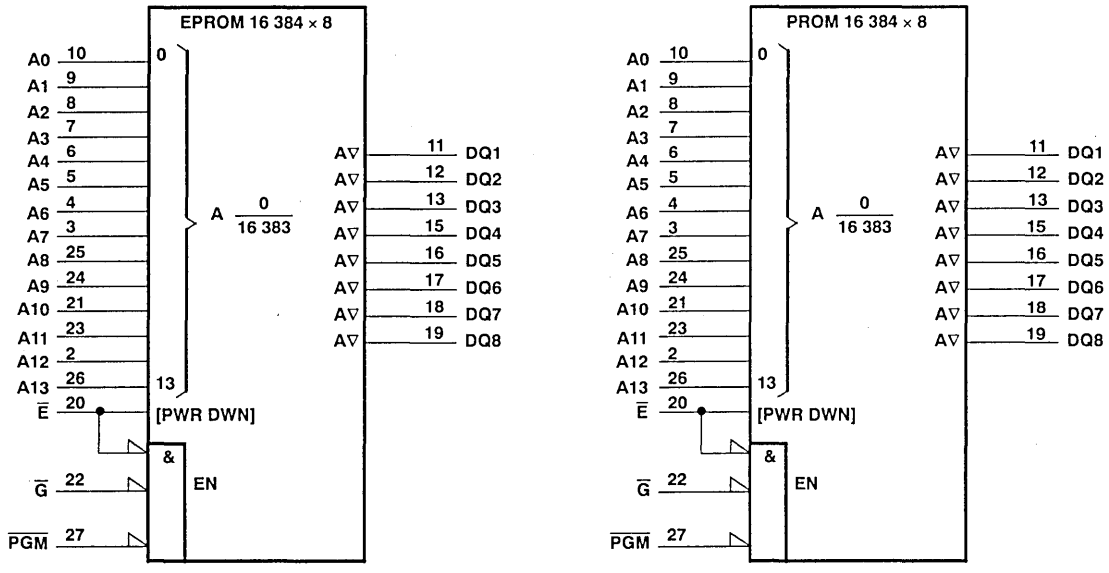


Figure 1. SNAP! Pulse Programming Flowchart

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... – 0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... – 0.6 V to 6.5 V
A9 ..... – 0.6 V to 13.5 V
Output voltage range (see Note 1) ..... – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C128-_ _JL and JL4, '27PC128-_ _NL, and NL4
FML, and FML4) ..... 0°C to 70°C
Operating free-air temperature range ('27C128-_ _JE and JE4, '27PC128-_ _NE, NE4,
FME, and FME4) ..... – 40°C to 85°C
Storage temperature range ..... – 65°C to 150°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			'27C128-100 '27C128-120 '27C/PC128-1 '27C/PC128-2 '27C/PC128			'27C128-12 '27C/PC128-15 '27C/PC128-20 '27C/PC128-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply Voltage	Read mode (see Note 2)		4.75	5	5.25	4.5	5	5.5	V
	SNAP! Pulse programming algorithm		6.25	6.5	6.75	6.25	6.5	6.75	
V_{PP} Supply voltage	Read mode (see Note 3)		$V_{CC}-0.6$		$V_{CC}+0.6$	$V_{CC}-0.6$		$V_{CC}+0.6$	V
	SNAP! Pulse programming algorithm		12.75	13	13.25	12.75	13	13.25	
V_{IH} High-level input voltage		TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	
V_{IL} Low-level input voltage		TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		0.2	−0.5		0.2	V
T_A Operating free-air temperature		'27C128-_ _JL,JL4 '27PC128-_ _NL,NL4 FML, FML4	0		70	0		70	°C
T_A Operating free-air temperature		'27C128-_ _JE,JE4 '27PC128-_ _NE,NE4 FME, FME4	−40		85	−40		85	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = -2.5$ mA	3.5			V
			$I_{OH} = -20$ μA	$V_{CC}-0.1$			V
V_{OL}	Low-level output voltage		$I_{OL} = 2.1$ mA			0.4	V
			$I_{OL} = 20$ μA			0.1	V
I_I	Input current (leakage)		$V_I = 0$ to 5.5 V			±1	μA
I_O	Output current (leakage)		$V_O = 0$ to V_{CC}			±1	μA
I_{PP1}	V_{PP} supply current		$V_{PP} = V_{CC} = 5.5$ V		1	10	μA
I_{PP2}	V_{PP} supply current (during program pulse)		$V_{PP} = 13$ V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{IH}$		250	500	μA
		CMOS-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{CC}$		100	250	μA
I_{CC2}	V_{CC} supply current (active)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open		15	30	mA

† Typical values are at $T_A = 25°C$ and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	$V_I = 0$, f = 1 MHz		6	10	pF
C_O	Output capacitance	$V_O = 0$, f = 1 MHz		10	14	pF

† Typical values are at $T_A = 25°C$ and nominal voltages.
‡ Capacitance measurements are made on sample basis only.

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C128-100		'27C128-120 '27C128-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		100		120	ns
$t_{a(E)}$	Access time from chip enable			100		120	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		55	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	40	0	45	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C/PC128-1 '27C/PC128-15		'27C/PC128-2 '27C/PC128-20		'27C/PC128 '27C/PC128-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		150		200		250	ns
$t_{a(E)}$	Access time from chip enable			150		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

† Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} =13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

			MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference page 7-10).
5. Common test conditions apply for t_{dis} except during programming.

PARAMETER MEASUREMENT INFORMATION

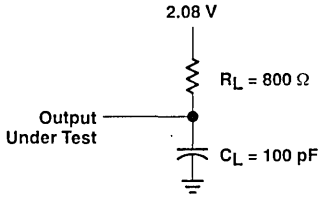
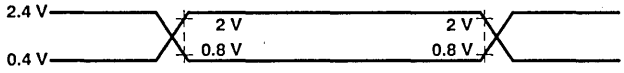


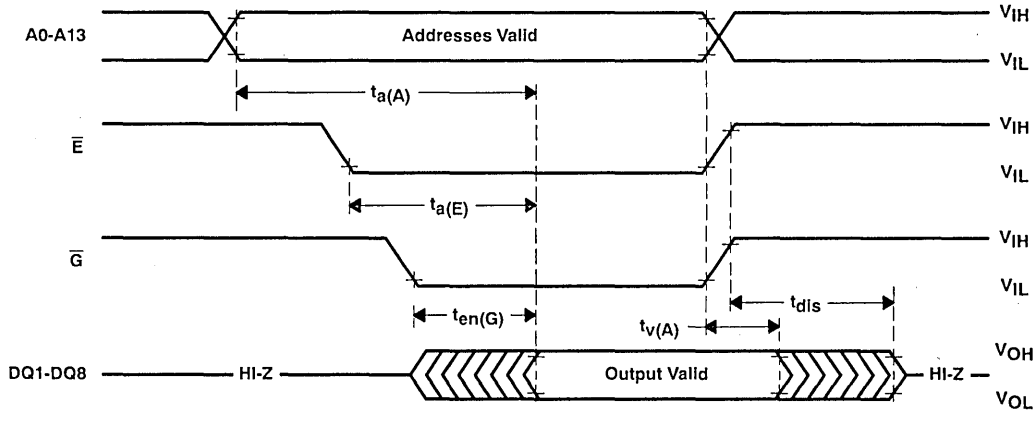
Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms

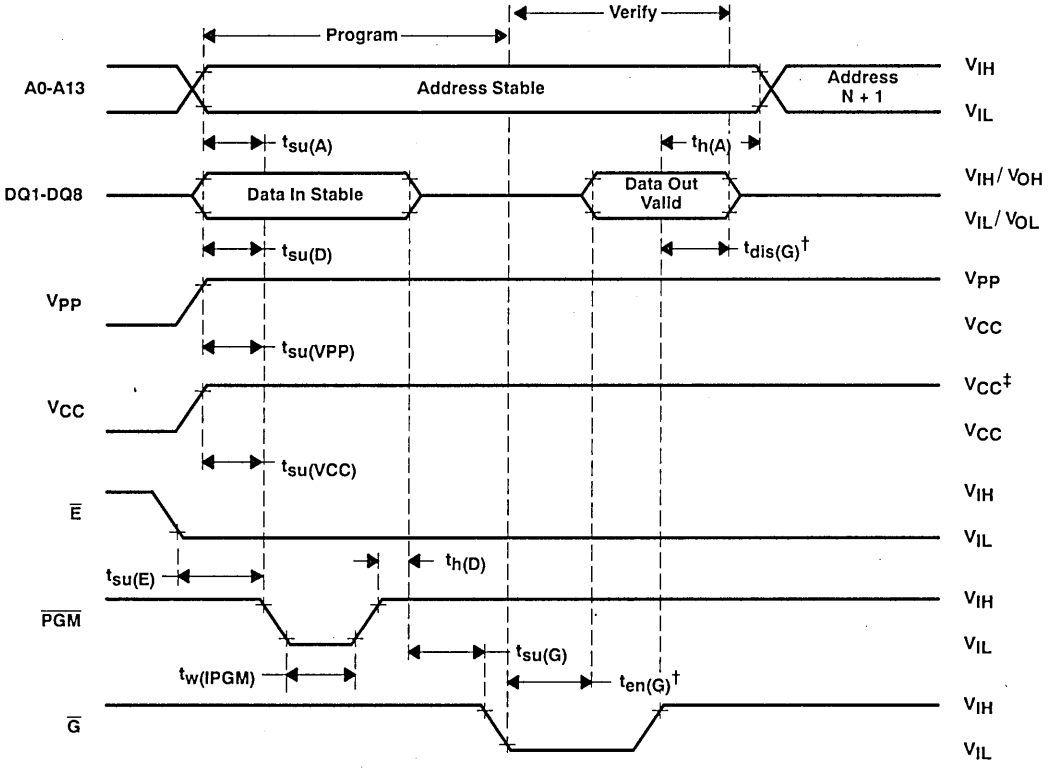


AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

read cycle timing



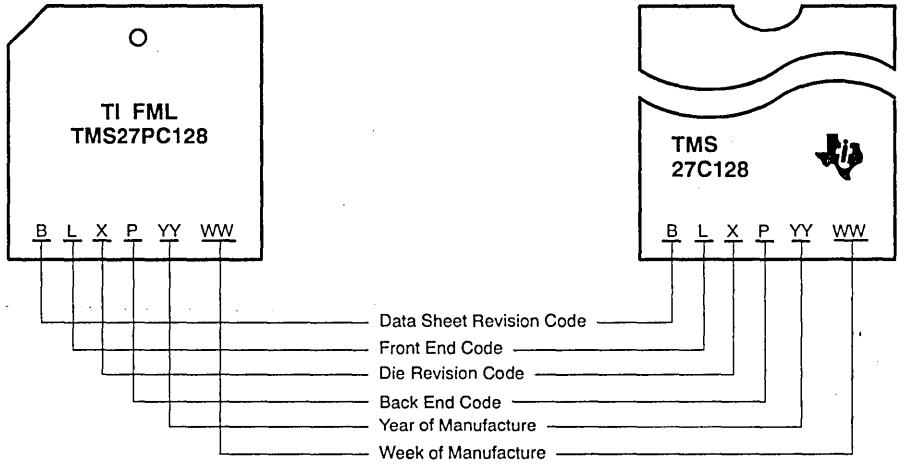
program cycle timing



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

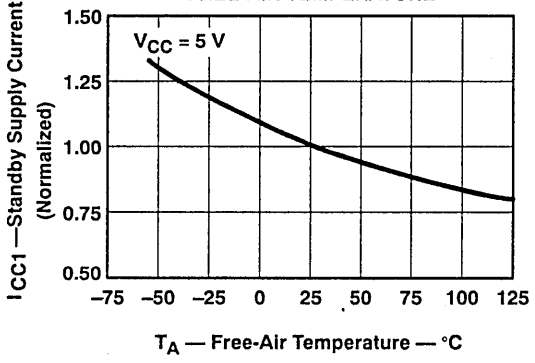
device symbolization

This data sheet is applicable to all TI TMS27C128 CMOS EPROMs and TMS27PC128 PROMs with the data sheet revision code "A" as shown below.

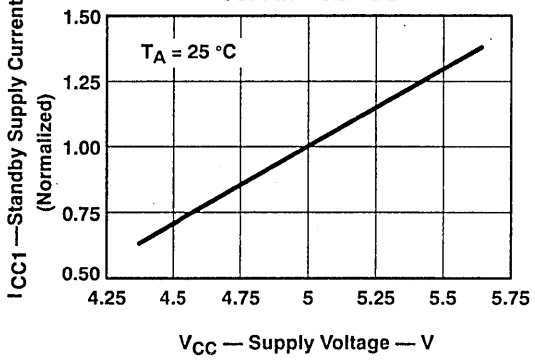


TYPICAL TMS27C/PC128 CHARACTERISTICS

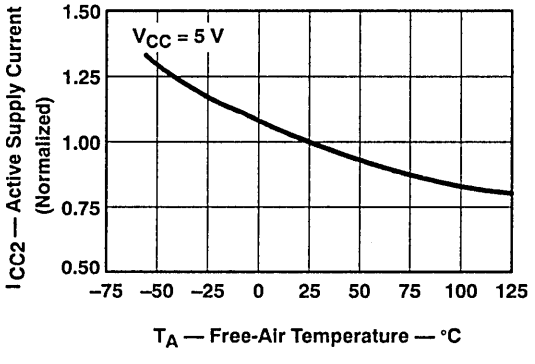
STANDBY SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



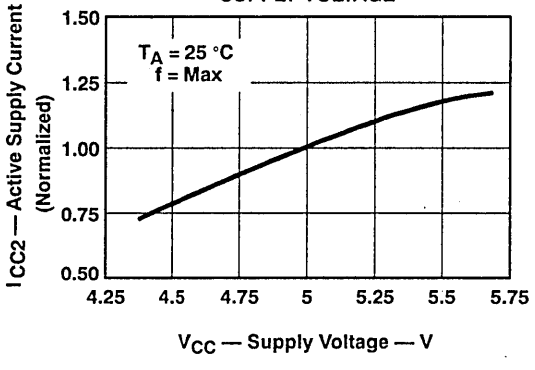
STANDBY SUPPLY CURRENT
vs
SUPPLY VOLTAGE



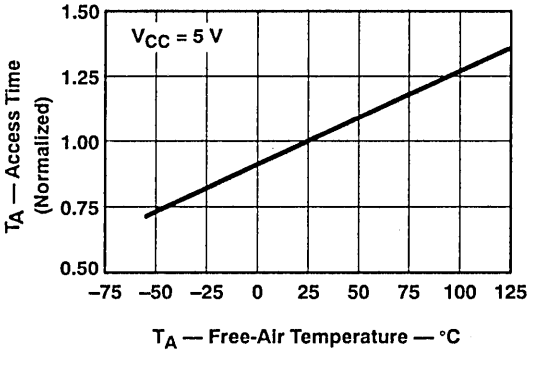
ACTIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



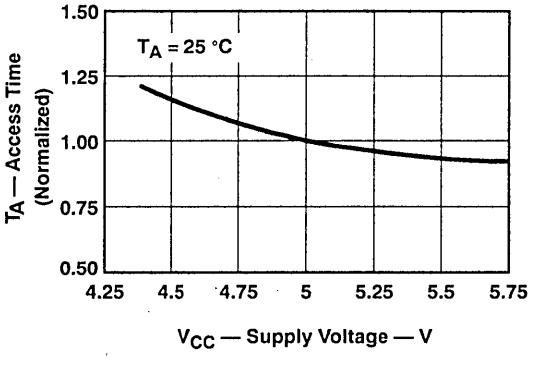
ACTIVE SUPPLY CURRENT
vs
SUPPLY VOLTAGE



ACCESS TIME
vs
FREE-AIR TEMPERATURE



ACCESS TIME
vs
SUPPLY VOLTAGE



REV A — SMLS128D — OCTOBER 1984 — REVISED JANUARY 1991

TMS27C256 262 144-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC256 262 144-BIT PROGRAMMABLE READ-ONLY MEMORY

REV A — SMLS256E — SEPTEMBER 1984 — REVISED JANUARY 1991

This Data Sheet is Applicable to All TMS27C256s and TMS27PC256s Symbolized with Code "B" as Described on Page 7-25.

- **Organization . . . 32K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 256K MOS ROMs, PROMs, and EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**

V_{CC} ± 5%	V_{CC} ± 10%	
'27C/PC256-100	'27C/PC256-10	100 ns
'27C/PC256-120	'27C/PC256-12	120 ns
'27C/PC256-150	'27C/PC256-15	150 ns
'27C/PC256-1	'27C/PC256-17	170 ns
'27C/PC256-2	'27C/PC256-20	200 ns
'27C/PC256	'27C/PC256-25	250 ns

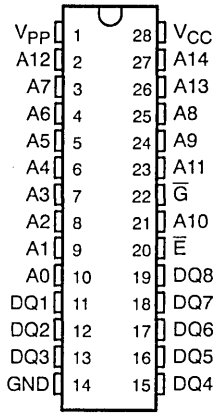
- **Power Saving CMOS Technology**
- **Very High-Speed SNAP! Pulse Programming**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **— Active . . . 165 mW Worst Case**
  - **— Standby . . . 1.4 mW Worst Case (CMOS Input Levels)**
- **PEP4 Version Available With 168 Hour Burn-in, and Choices of Operating Temperature Ranges**
- **256K EPROM Available With MIL-STD-883C Class B High Reliability Processing (SMJ27C256)**

description

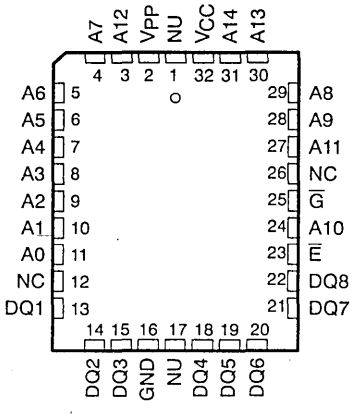
The TMS27C256 series are 262 144-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC256 series are 262 144-bit, one-time, electrically programmable read-only memories.

J and N Packages
(Top View)



FM Package
(Top View)



PIN NOMENCLATURE	
A0-A14	Address Inputs
$\overline{E}$	Chip Enable/Powerdown
$\overline{G}$	Output Enable
GND	Ground
NC	No Internal Connection
NU	Make No External Connection
DQ1-DQ8	Inputs (programming)/Outputs
V_{CC}	5-V Power Supply
V_{PP}	13 V Programming Power Supply

REV A — SMLS256E — SEPTEMBER 1984 — REVISED JANUARY 1991

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C256 and the TMS27PC256 are pin compatible with 28-pin 256K MOS ROMs, PROMs, and EPROMs.

The TMS27C256 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC256 OTP PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC256 OTP PROM is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix).

The TMS27C256 and TMS27PC256 are offered with two choices of temperature ranges of 0°C to 70°C and – 40°C to 85°C (TMS27C256-_ _JL and TMS27C256-_ _JE; TMS27PC256-_ _NL and TMS27PC256-_ _NE; TMS27PC256-_ _FML and TMS27PC256-_ _FME, respectively). The TMS27C256 and the TMS27PC256 are also offered with 168-hour burn-in on both temperature ranges (TMS27C256-_ _JL4 and TMS27C256-_ _JE4; TMS27PC256-_ _FML4 and TMS27PC256-_ _FME4, respectively); see table below.

All package styles conform to JEDEC standards.

EPROM AND OTP PROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C TO 70°C	– 40°C TO 85°C	0°C TO 70°C	– 40°C TO 85°C
TMS27C256-XXX	JL	JE	JL4	JE4
TMS27PC256-XXX	NL	NE	NL4	NE4
TMS27PC256-XXX	FML	FME	FML4	FME4

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 13-V supply is needed for programming . All programming signals are TTL level. These devices are programmable by the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13-V and a V_{CC} of 6.5-V for a nominal programming time of four seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13-V for SNAP! Pulse) and 12-V on A9 for signature mode.

FUNCTION	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	V_{IH}	V_{IL}	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ1-DQ8	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	04

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C256s or TMS27PC256s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ1 through DQ8.

latchup immunity

Latchup immunity on the TMS27C256 and TMS27PC256 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family"*, available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL or CMOS signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure (TMS27C256)

Before programming, the TMS27C256 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). EPROM erasure before programming is necessary to assure that all bits are in the logic high state. Logic lows are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light. The recommended minimum exposure dose (UV intensity × exposure time) is 15-W•s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C256, the window should be covered with an opaque label.

initializing (TMS27PC256)

The one-time programmable TMS27PC256 PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The 256K EPROM and OTP PROM are programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which programs in a nominal time of four seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins DQ1 to DQ8. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V.

program inhibit

Programming may be inhibited by maintaining a high level inputs on the $\overline{E}$ and $\overline{G}$ pins.

program verify

Programmed bits may be verified with V_{PP} = 13 V when $\overline{G}$ = V_{IL} and $\overline{E}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., A0 = V_{IL} accesses the manufacturer code, which is output on DQ1-DQ8; A0 = V_{IH} accesses the device code, which is output on DQ1-DQ8. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit DQ8. The manufacturer code for these devices is 97, and the device code is 04.

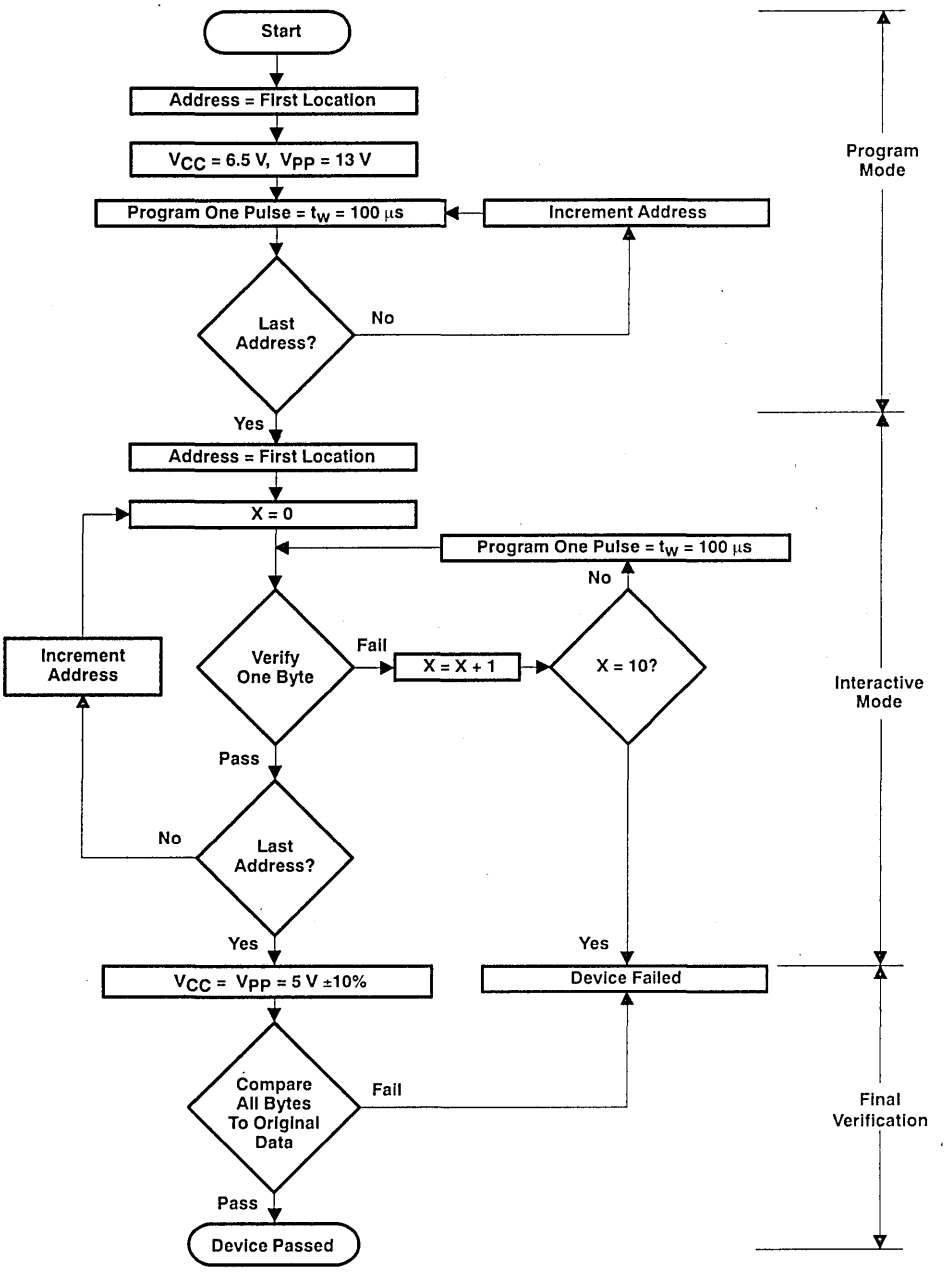
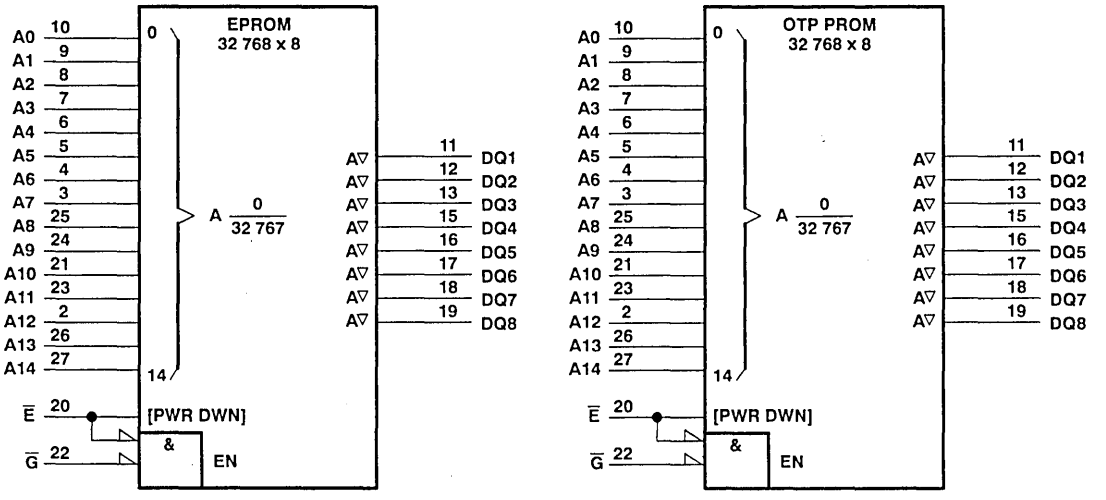


Figure 1. SNAP! Pulse Programming Flowchart

REV A — SMLS256E — SEPTEMBER 1984 — REVISED JANUARY 1991

logic symbol†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} ..... – 0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 ..... – 0.6 V to 6.5 V
A9 ..... – 0.6 V to 13.5 V
Output voltage range (see Note 1) ..... – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C256-_ _JL and JL4, '27PC256-_ _NL, NL4, FML, and FML4) ..... 0° C to 70°C
Operating free-air temperature range ('27C256-_ _JE and JE4, '27PC256-_ _NE, NE4, FME, and FME4) ..... – 40° C to 85°C
Storage temperature range ..... – 65°C to 150°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			TMS27C/PC256-100, TMS27C/PC256-120, TMS27C/PC256-150, TMS27C/PC256-1, TMS27C/PC256-2, TMS27C/PC256			TMS27C/PC256-10, TMS27C/PC256-12, TMS27C/PC256-15, TMS27C/PC256-17, TMS27C/PC256-20, TMS27C/PC256-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.75	5	5.25	4.5	5	5.5	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode (see Note 3)	$V_{CC}-0.6$		$V_{CC}+0.6$	$V_{CC}-0.6$		$V_{CC}+0.6$	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	12.75	13	13.25	
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		0.2	−0.5		0.2	
T_A	Operating free-air temperature	'27C256-_ _JL, JL4 '27PC256-_ _NL, NL4, FML, FML4	0		70	0		70	°C
T_A	Operating free-air temperature	'27C256-_ _JE, JE4 '27PC256-_ _NE, NE4, FME, FME4	−40		85	−40		85	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = -2.5$ mA	3.5			V
			$I_{OH} = -20$ µA	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 2.1$ mA			0.4	V
			$I_{OL} = 20$ µA			0.1	
I_I	Input current (leakage)		$V_I = 0$ to 5.5 V			±1	µA
I_O	Output current (leakage)		$V_O = 0$ to V_{CC}			±1	µA
I_{PP1}	V_{PP} supply current		$V_{PP} = V_{CC} = 5.5$ V		1	10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		$V_{PP} = 13$ V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{IH}$		250	500	µA
		CMOS-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{CC}$		100	250	
I_{CC2}	V_{CC} supply current (active)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open		15	30	mA

†Typical values are at $T_A = 25°C$ and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	$V_I = 0$, f = 1 MHz		6	10	pF
C_O	Output capacitance	$V_O = 0$, f = 1 MHz		10	14	pF

†Typical values are at $T_A = 25°C$ and nominal voltages.
‡ Capacitance measurements are made on a sample basis only.

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (see Notes 4 and 5)	'27C256-100 '27PC256-100 '27C256-10 '27PC256-10		'27C256-120 '27PC256-120 '27C256-12 '27PC256-12		'27C256-150 '27PC256-150 '27C256-15 '27PC256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		55		75	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	45	0	45	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

PARAMETER		TEST CONDITIONS (see Notes 4 and 5)	'27C256-1 '27PC256-1 '27C256-17 '27PC256-17		'27C256-2 '27PC256-2 '27C256-20 '27PC256-20		'27C256 '27PC256 '27C256-25 '27PC256-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		170		200		250	ns
$t_{a(E)}$	Access time from chip enable			170		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

†Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6.50 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low). (Reference page 7-23.)

5. .Common test conditions apply for the t_{dis} except during programming.

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V, T_A = 25°C (see Note 4)

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	95	100	105	µs
$t_{su(A)}$	Address setup time	2			µs
$t_{su(G)}$	$\overline{G}$ setup time	2			µs
$t_{su(E)}$	$\overline{E}$ setup time	2			µs
$t_{su(D)}$	Data setup time	2			µs
$t_{su(VPP)}$	V_{PP} setup time	2			µs
$t_{su(VCC)}$	V_{CC} setup time	2			µs
$t_{h(A)}$	Address hold time	0			µs
$t_{h(D)}$	Data hold time	2			µs

NOTE 4: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low). (Reference page 7-23.)

PARAMETER MEASUREMENT INFORMATION

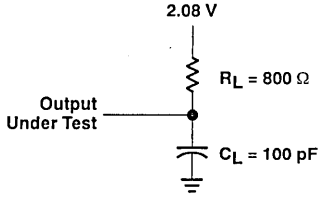
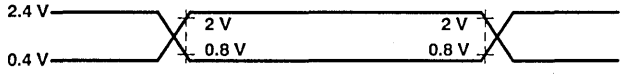


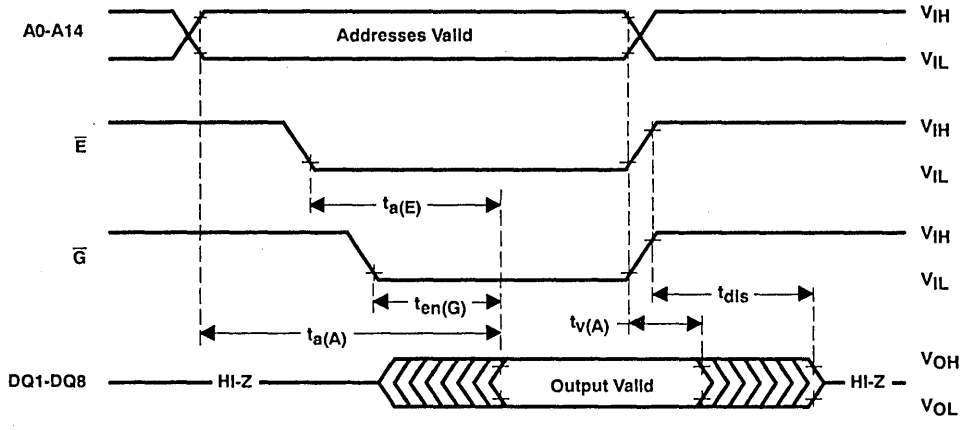
Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms

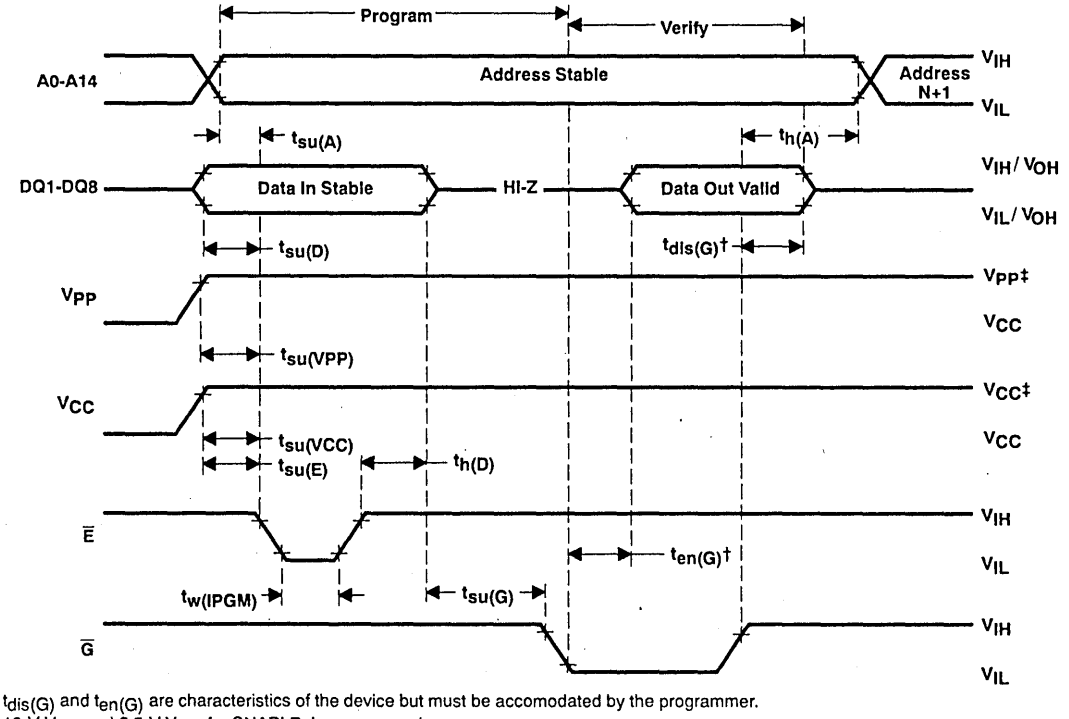


A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

read cycle timing



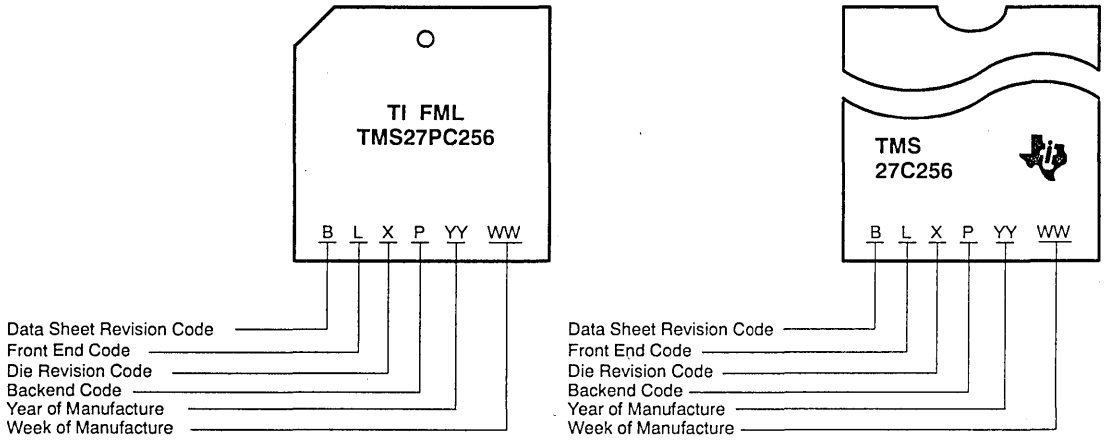
program cycle timing (SNAP! Pulse programming)



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accomodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

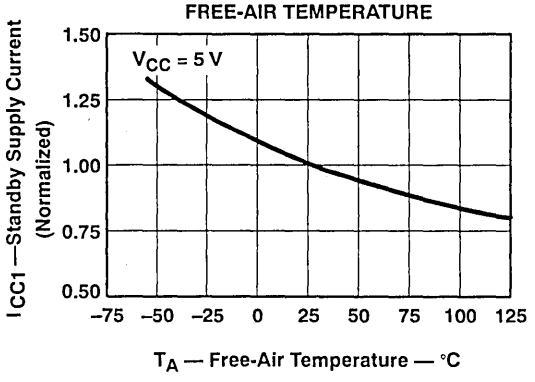
device symbolization

This data sheet is applicable to all TI TMS27C256 CMOS EPROMs and TMS27PC256 CMOS OTP PROMs with the data sheet revision code "B" as shown below.

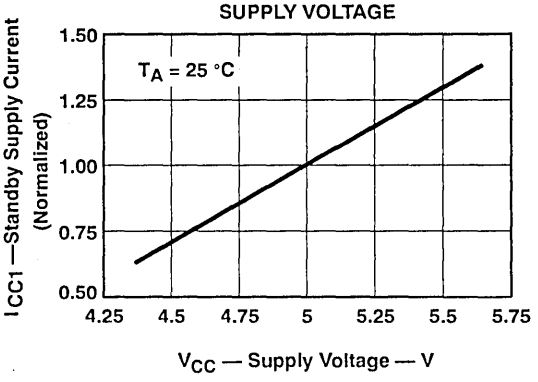


TYPICAL TMS27C/PC256 CHARACTERISTICS

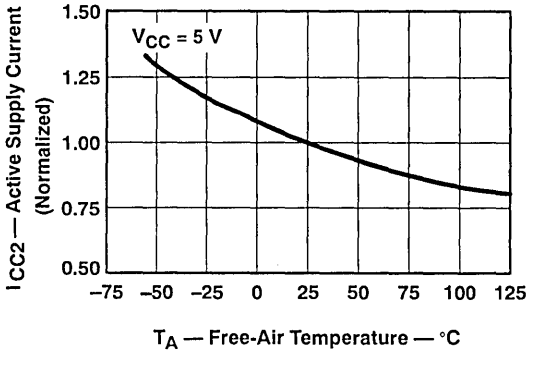
STANDBY SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



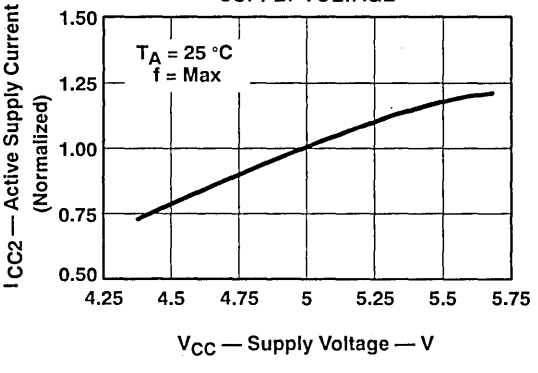
STANDBY SUPPLY CURRENT
vs
SUPPLY VOLTAGE



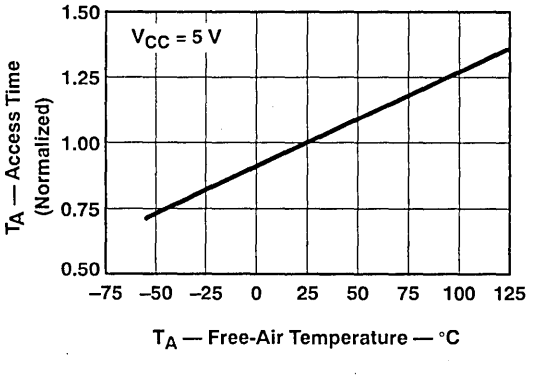
ACTIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



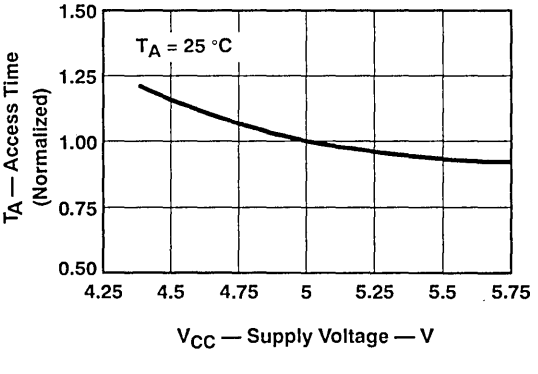
ACTIVE SUPPLY CURRENT
vs
SUPPLY VOLTAGE



ACCESS TIME
vs
FREE-AIR TEMPERATURE



ACCESS TIME
vs
SUPPLY VOLTAGE



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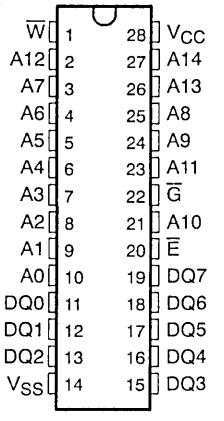
- Organization 32K × 8
- Single 5-V Power Supply
- HVCMOS Technology
- All Inputs/Outputs TTL Compatible
- Max Access/Min Cycle Time

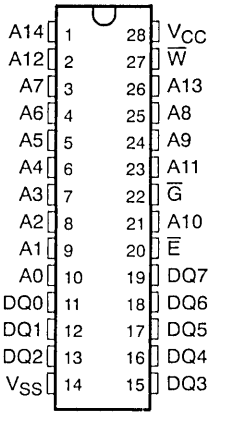
V_{CC} ± 5%	V_{CC} ± 10%	
'29F256/8/9-170		170 ns
'29F256/8/9-200	'29F256/8/9-20	200 ns
'29F256/8/9-250	'29F256/8/9-25	250 ns
'29F256/8/9-300	'29F256/8/9-30	300 ns

- Self-Timed Erasure of the Entire Memory Before any Reprogramming (15 ms MAX)
- Single Byte and Page (64 Bytes) Program:
  - Latched Address and Data
  - Self-Timed Programming Operation (15 ms MAX)
  - Data Polling Verification
- 100, 1000, and 10000 Cycles Endurance Versions
- Software Inadvertent Write Protection
- Software Erase Mode Entry
- TMS29F256 Pinout Compatible With EPROM JEDEC Standard
- TMS29F258 Pinout Compatible With EEPROM JEDEC Standard
- Choice of Operating Temperature Ranges

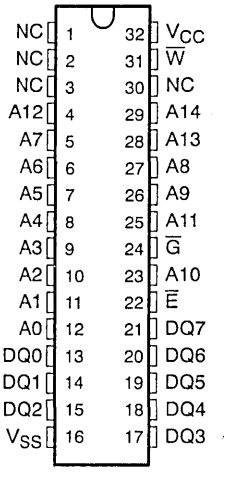
TMS29F256 . . . N Package
TMS29F256 . . . J Package
(Top View)



TMS29F258 . . . N Package
TMS29F258 . . . J Package
(Top View)



TMS29F259 . . . N Package
TMS29F259 . . . J Package
(Top View)



PIN NOMENCLATURE	
A0-A14	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Internal Connection
$\overline{W}$	Write Enable
DQ0-DQ7	Data In/Data Out
V_{CC}	5-V Power Supply
V_{SS}	Ground

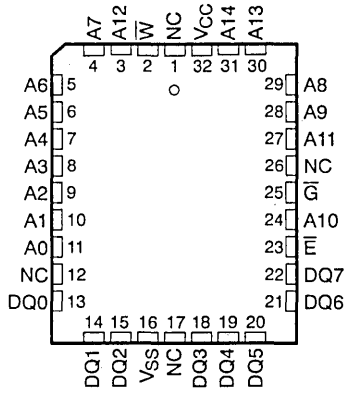
description

The TMS29F256, TMS29F258, and TMS29F259 are 262 144-bit, programmable read-only memories that can be electrically bulk-erased and reprogrammed. These devices are fabricated using HVCMOS flotox technology for high reliability and very low power dissipation. They perform the erase/program operations automatically with a single 5-V supply, and they can program a single byte or any number of bytes between 1 and 64.

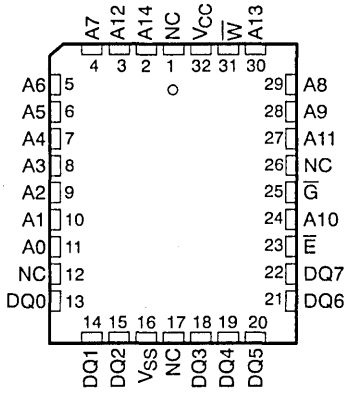
The TMS29F256, TMS29F258, and TMS29F259 Flash EEPROMs are offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting-hole rows on 15,2-mm (600-mil) centers. The TMS29F256, TMS29F258, and TMS29F259 in

the ceramic package are each offered with three guaranteed temperature ranges of 0°C to 70°C, – 40°C to 85°C, and – 40°C to 125°C (TMS29F256-_ _JL, TMS29F258-_ _JL, and TMS29F259-_ _JL for 0°C to 70°C; TMS29F256-_ _JE, TMS29F258-_ _JE, and TMS29F259-_ _JE for – 40°C to 85°C; and TMS29F256-_ _JQ, TMS29F258-_ _JQ, and TMS29F259-_ _JQ for – 40°C to 125°C).

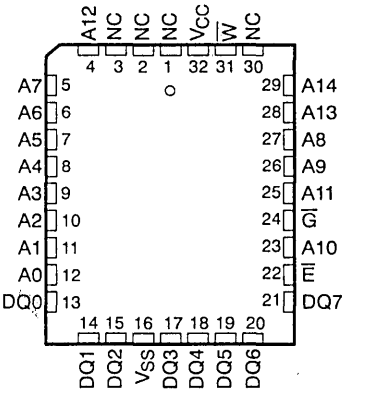
TMS29F256
FM PACKAGE
(TOP VIEW)



TMS29F258
FM PACKAGE
(TOP VIEW)



TMS29F259
FM PACKAGE
(TOP VIEW)



The TMS29F256, TMS29F258, and TMS29F259 are also offered with 168 hour burn-in temperature ranges (TMS29F256-_ _JL4, JE4, and JQ4; TMS29F258-_ _JL4, JE4, and JQ4; TMS29F259-_ _JL4, JE4, and JQ4, respectively). (See table on page 7-29.)

The TMS29F256, TMS29F258, and TMS29F259 are also offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2-mm (600-mil) centers. The TMS29F256, TMS29F258, and TMS29F259 are offered in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix). These packages are guaranteed from 0°C to 70°C (NL or FML suffix).

The TMS29F256, TMS29F258, and TMS29F259 are organized as 32K × 8 bits. They feature internal circuitry to minimize the external hardware interface that provides latched address and data, self-timed programming, and data polling verification. In the erased state all bits are at a logic high. To reprogram, all memory bits are erased first, then those bits that should be logic lows are programmed accordingly. During programming, the data polling function is enabled, causing the memory to respond with the last data read except that the most significant bit is inverted to inform the host microprocessor that the memory is busy until the programming is completed.

The TMS29F256, TMS29F258, and TMS29F259 are available in 100 cycle endurance versions and will be available in 1000 and 10 000 cycle endurance versions.

FUNCTION (PINS)	MODE					
	Read	Output Disable	Standby and Write Inhibit	Write	Signature Mode	
$\overline{E}$ (20)§	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	
$\overline{G}$ (22)§	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	
A0 (10)§	X	X	X	X	V_{IL}	V_{IH}
A9 (24)§	X	X	X	X	V_H‡	
$\overline{W}$ (1)§	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	
DQ0-DQ7 (11-13, 15-19)§	Data Out	HI-Z	HI-Z	Data In	MFG	DEVICE
					97	F1

† X = Don't care for V < V_{CC}.
‡ 12.5 V < V_H < 15 V.
§ TMS29F256 J and N package pins.

operation

read/output disable

When the outputs of two or more TMS29F256s, TMS29F258s, and TMS29F259s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices.

To read the output of the TMS29F256, TMS29F258, or TMS29F259 a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

power down

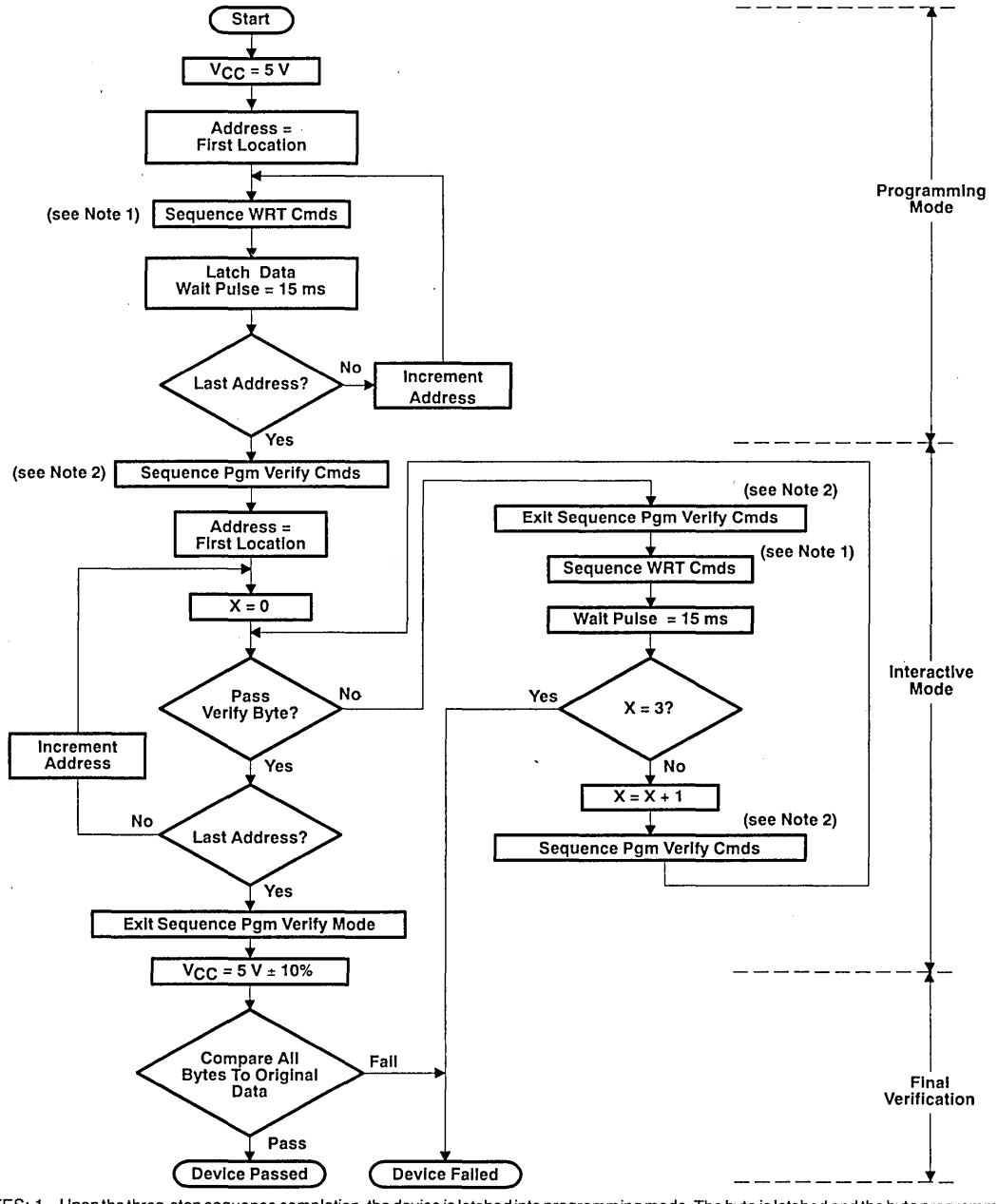
Active I_{CC} current can be reduced from 20 mA to 2 mA typically, by applying a high TTL signal to the $\overline{E}$ pin. In this mode all the outputs are in the high-impedance state.

single-byte program

The single-byte program initiates with $\overline{W}$ low and $\overline{G}$ high applied to a selected device. The addresses on the address pins will be latched on the falling edge of $\overline{E}$ or $\overline{W}$, whichever comes first. Figure 1 illustrates the single-byte programming flow.

After the latching operations are completed, the device starts automatically programming the data in the addressed location within the memory array. This internal programming operation is completed in 15 ms maximum.

FLASH EEPROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN			SUFFIX FOR PEP4 168 HR. BURN-IN vs TEMPERATURE RANGES		
	0°C to 70°C	– 40°C to 85°C	– 40°C to 125°C	0°C to 70°C	– 40°C to 85°C	– 40°C to 125°C
TMS29F256-xxx	JL,NL,FML	JE	JQ	JL4	JE4	JQ4
TMS29F258-xxx	JL,NL,FML	JE	JQ	JL4	JE4	JQ4
TMS29F259-xxx	JL,NL,FML	JE	JQ	JL4	JE4	JQ4



NOTES: 1. Upon the three-step sequence completion, the device is latched into programming mode. The byte is latched and the byte programming operation starts if a subsequent rising edge of $\overline{W}$ is not detected within 100 μs.
2. Similar to the page programming mode.

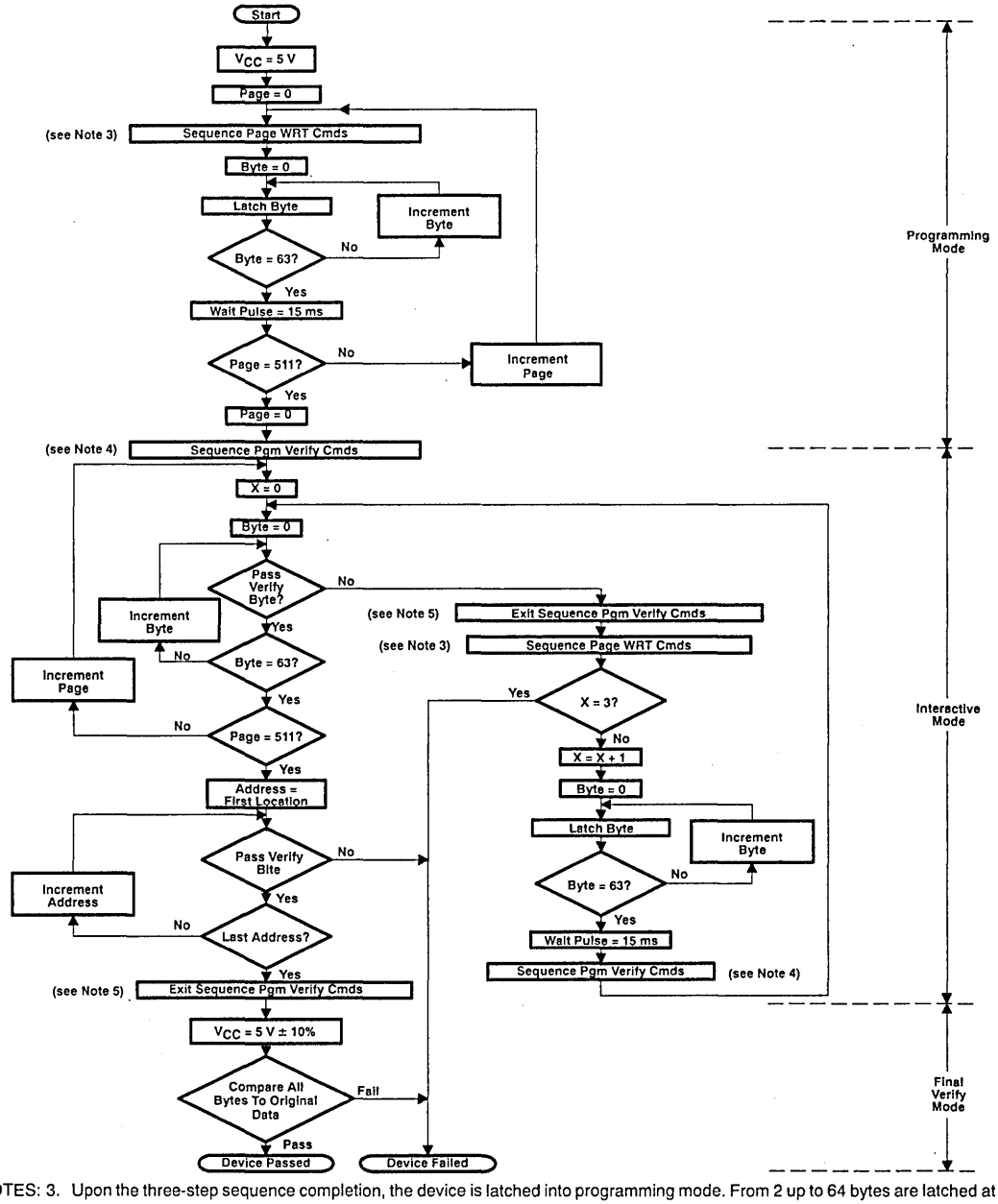
Figure 1. Single-byte Programming Flowchart

automatic page program

The page mode of the '29F256, '29F258, and '29F259 allow the user to program 2 to 64 bytes at a time. These bytes are initially loaded in the internal device register and then automatically stored in the addressed memory locations within the memory array. The internal programming operation is completed in 15 ms maximum, regardless of the number of bytes (64 maximum) loaded. During the page loading, the page address (A6 to A14) must be the same as the initial page address. Figure 2 illustrates the automatic page programming flow.

The page mode operation initiates in the same way as the single byte mode. After the first byte has been loaded, the '29F256, '29F258, and '29F259 can be loaded with 1 to 63 additional bytes. Each byte load cycle starts with the falling edge of $\overline{W}$, or $\overline{E}$, whichever comes last. A successive byte must be loaded within 100 μs from the rising edge of the previous byte load cycle. If a subsequent rising edge of $\overline{W}$ is not detected within 100 μs, the internal programming operation starts automatically and subsequent attempts to load additional bytes are ignored until the operation is completed.

Note that both the single byte and the automatic page programs can be entered after a proper "dummy" sequence of bytes has been loaded (see inadvertent write protection).



NOTES: 3. Upon the three-step sequence completion, the device is latched into programming mode. From 2 up to 64 bytes are latched at a rate of 1 μs up to 100 μs per byte.

4. Upon the three-step sequence completion, the device is latched into the program verify mode. All the bytes are read with a sense voltage of: (internal V_{sense} volt) + (program margin voltage).

5. Upon the three-step sequence completion, the device exits the program verify mode and returns to the page write setup.

Figure 2. Page Programming Flowchart — Entire Memory Algorithm

data polling

During a programming operation, the data polling software function is enabled to notify the host microcomputer that the memory is busy with programming and ignores any command until the programming operation is completed. If an attempt to read any byte occurs during the programming cycle, the device answers with the last loaded byte, but with the inverted logical value of DQ7. (See page 7-44 for data polling timing diagram.)

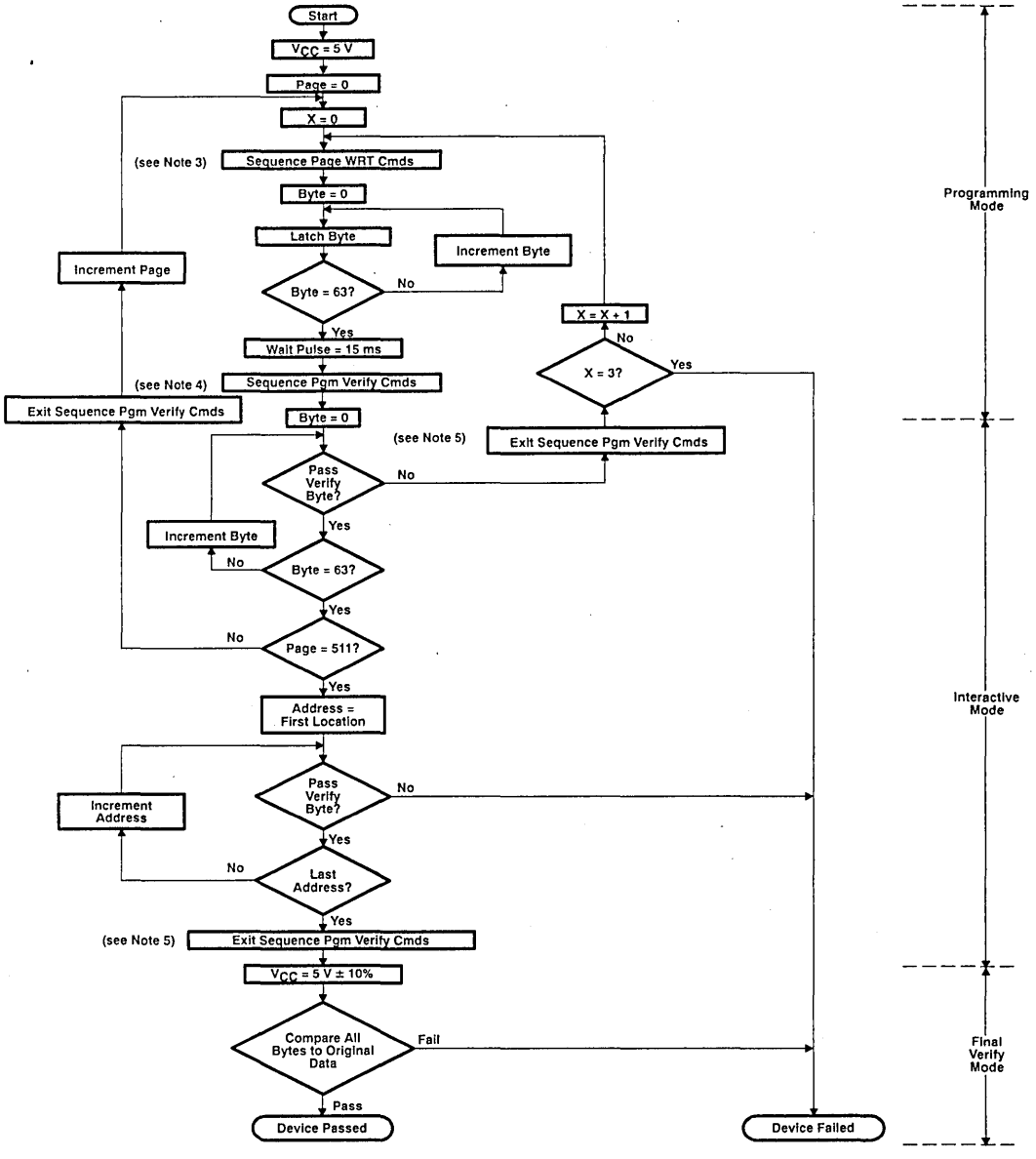
flash erase mode

The flash erase operation can be activated via software by loading a dummy sequence of data/address strings. The timing characteristics of this sequence are the same as those used for the page mode. The device detects this particular sequence and automatically starts the self-timed erase. If the sequence load cycle is longer than 100 μs, the device ignores it. This sequence should not be used in the actual software program to prevent inadvertent flash erase operations.

The specified dummy sequence to initiate the flash erase mode is:

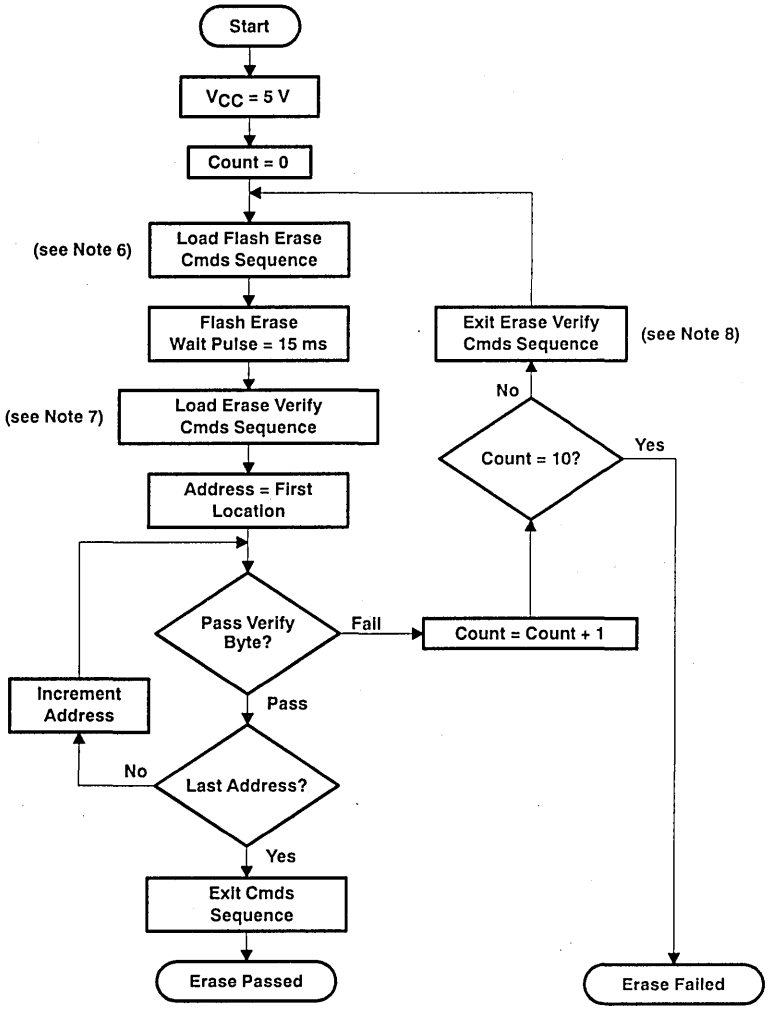
STEP	MODE	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	80
4	Access Write	5555	AA
5	Access Write	2AAA	55
6	Access Write	5555	10

The self-timed flash erase mode starts automatically.



NOTES: 3. Upon the three-step sequence completion, the device is latched into programming mode. From 2 up to 64 bytes are latched at a rate of 1 μs up to 100 μs per byte.
4. Upon the three-step sequence completion, the device is latched into the program verify mode. All the bytes are read with a sense voltage of: (internal V_{sense} volt) + (program margin voltage).
5. Upon the three-step sequence completion, the device exits the program verify mode and returns to the page write setup.

Figure 3. Page Programming Flowchart — Standard Algorithm



NOTES: 6. The bulk-erase operation starts automatically once the six-step sequence is completed.
7. The device is latched into the Erase Verify mode once the three-step sequence is completed. All bytes are read with a sense voltage of: (internal V_{sense} voltage) — (erase margin voltage).
8. Upon the three-step sequence completion, the device is de-latched and returns to Flash operating setup.

Figure 4. Flash Erase Flowchart

signature mode

The signature mode provides access to two bytes contained in a spare row. One byte designates the manufacturer, the other byte designates the device code. The signature mode can be entered through either a hardware or a software operation.

The hardware entry mode is specified in the mode table in the description section. Setting the device in the read mode and applying V_H on pin A9 produces the manufacturer byte code at the I/O pins if A0 = V_{IL}, or the device identifier byte code if A0 = V_{IH}. The information provided by these two bytes helps the programmer select the proper programming algorithm.

The signature mode software entry sequence is specified as follows:

STEP	MODE	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	90

exit mode

The software exit sequence for any mode is specified as follows:

STEP	MODE	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	F0

program verify mode

The program verify mode allows the programmer to verify the adequacy of the programming.

STEP	MODE	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	B0

Upon completion of the three-step sequence, the device is latched into the program verify mode. All the bytes are read with a sense voltage of:

(internal V_{sense} voltage) + (program margin voltage)

The three access write (steps 1-3) are used only to enable the program verify mode: no data will actually be written to the device.

The software exit sequence must be applied to exit this program verify mode.

erase verify mode

The erase verify mode allows the programmer to verify the extent of erasure.

The device provides the following software sequence to access the erase verify mode:

STEP	MODE	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	D0

Upon completion of the three-step sequence, the device is latched into erase verify mode. All the bytes are read with a sense voltage of:

(internal V_{sense} voltage) – (erase margin voltage)

The software exit sequence must be applied to exit this program verify mode.

inadvertent write protection

The device is protected against write commands during power-up and power down. The protection is released only if V_{CC} is higher than 3 V. Moreover, the device provides a hardware and a software protection against inadvertent write commands that may occur even with a stable V_{CC}.

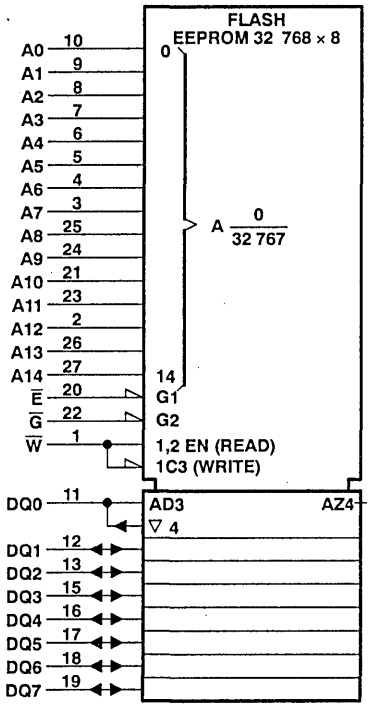
The hardware protection consists of noise immunity to a pulse on $\overline{W}$ shorter than 20 ns, which is unable to start a program cycle, and of a logic inhibit that prevents starting the program cycle unless the conditions of $\overline{W}$ low, $\overline{E}$ low, and $\overline{G}$ high are satisfied simultaneously.

The software protection is such that no program operation is enabled unless preceded by a sequence of three dummy write operations. Should the specified sequence not be loaded before any program operation or the sequence load cycle is longer than 100 μs, the device ignores the program commands.

The inadvertent write protection software sequence is specified as follows:

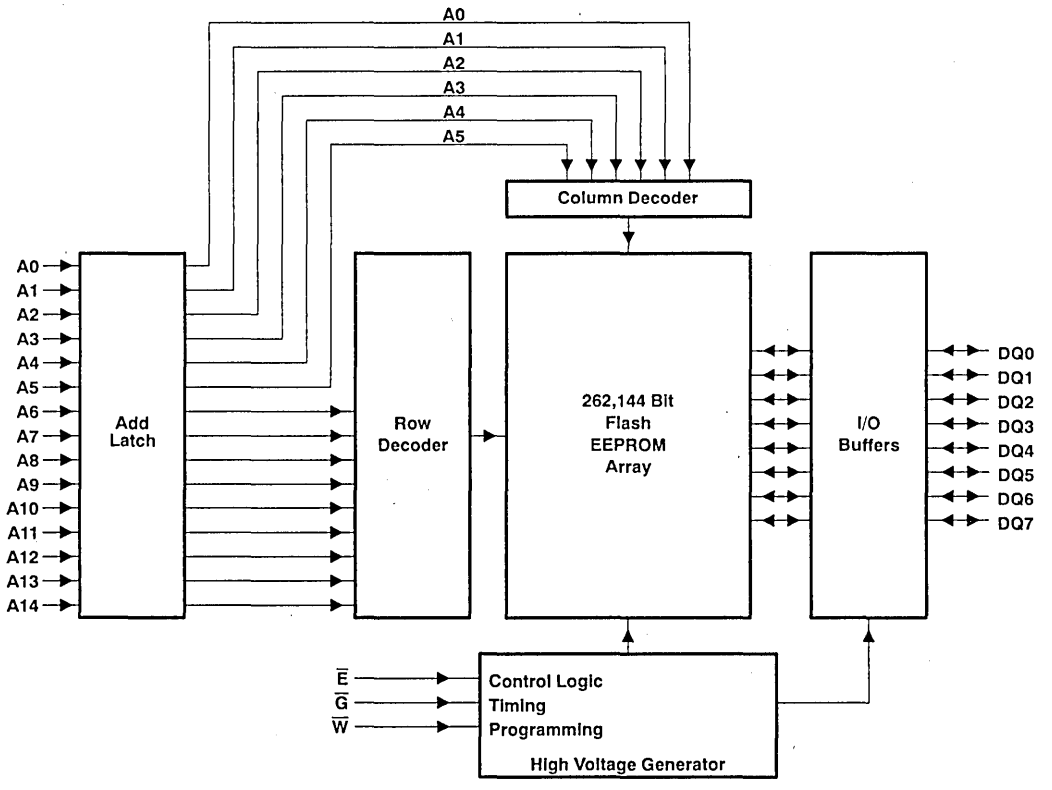
STEP	MODE	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	A0
4	Page Program	page address + 1st byte address up to the 64th	1st data up to the 64th

logic symbol†



† This symbol is in accordance with ANSI/EEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the TMS29F256 J and N packages.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 9) ..... – 0.6 V to 7 V
Input voltage range: All except $\overline{G}$ and A9 ..... – 0.6 V to 6.5 V
$\overline{G}$ and A9 ..... 0.6 V to 15 V
Output voltage (see Note 9) ..... – 0.6 V to V_{CC} + 0.6 V
Operating free-air temperature range ('29F256-_ _ JL, JL4, NL, and FML;
'29F258-_ _ JL, JL4, NL, and FML; '29F259-_ _ JL, JL4, NL, and FML) ..... 0°C to 70°C
Operating free-air temperature range ('29F256-_ _ JE and JE4;
'29F258-_ _ JE and JE4; '29F259-_ _ JE and JE4) ..... – 40°C to 85°C
Operating free-air temperature range ('29F256-_ _ JQ and JQ4;
'29F258-_ _ JQ and JQ4; '29F259-_ _ JQ and JQ4) ..... – 40°C to 125°C
Storage temperature range ..... – 65°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 9: All voltage values are with respect to the most negative supply voltage V_{SS} (substrate).

recommended operating conditions

			'29F256-170 '29F258-170 '29F259-170 '29F256-200 '29F258-200 '29F259-200		'29F256-250 '29F258-250 '29F259-250 '29F256-300 '29F258-300 '29F259-300	'29F256-20 '29F258-20 '29F259-20 '29F256-25 '29F258-25 '29F259-25		'29F256-30 '29F258-30 '29F259-30	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	4.5	5	5.5	V
V_{IH}	High-level input voltage	TTL	2		V_{CC}+1	2		V_{CC}+1	V
		CMOS	V_{CC} – 0.2		V_{CC}+1	V_{CC} – 0.2		V_{CC}+1	
V_{IL}	Low-level input voltage	TTL	– 0.5		0.8	– 0.5		0.8	V
		CMOS	– 0.5		GND+0.2	– 0.5		GND+0.2	
T_A	Operating free-air temperature	'29F256-_ _JL,JL4,NL,FML '29F258-_ _JL,JL4,NL,FML '29F259-_ _JL,JL4,NL,FML	0		70	0		70	°C
T_A	Operating free-air temperature	'29F256-_ _JE,JE4 '29F258-_ _JE,JE4 '29F259-_ _JE,JE4	– 40		85	– 40		85	°C
T_A	Operating free-air temperature	'29F256-_ _JQ,JQ4 '29F258-_ _JQ,JQ4 '29F259-_ _JQ,JQ4	– 40		125	– 40		125	°C

electrical characteristics over full range of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 400 μA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)	All except A9	V_I = 0 to 5.5 V			±1	μA
		A9	V_I = 0 to 15 V			±50	
I_O	Output current (leakage)		V_O = 0.1 V to V_{CC}			±10	μA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		2	3.5	mA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		1.5	3	
I_{CC2}	V_{CC} average supply current (active read)		t_{cycle} = minimum cycle time, outputs open			15	mA
I_{CC3}	V_{CC} average supply current (active write)		t_{cycle} = 15 ms			10	mA

† Typical values are at T_A = 25° C and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		4	6	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz		8	12	pF

† Typical values are at T_A = 25°C and nominal voltage.
‡ Capacitance measurements are made on sample basis only.

PARAMETER MEASUREMENT INFORMATION

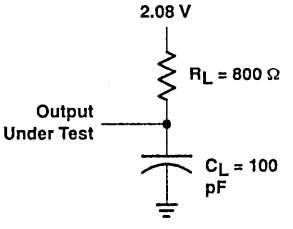
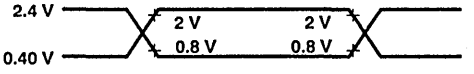


Figure 5. Output Load Circuit

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for both inputs and outputs. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and V_{SS} as close as possible to the device pins.

switching characteristics over full ranges of recommended operating conditions†

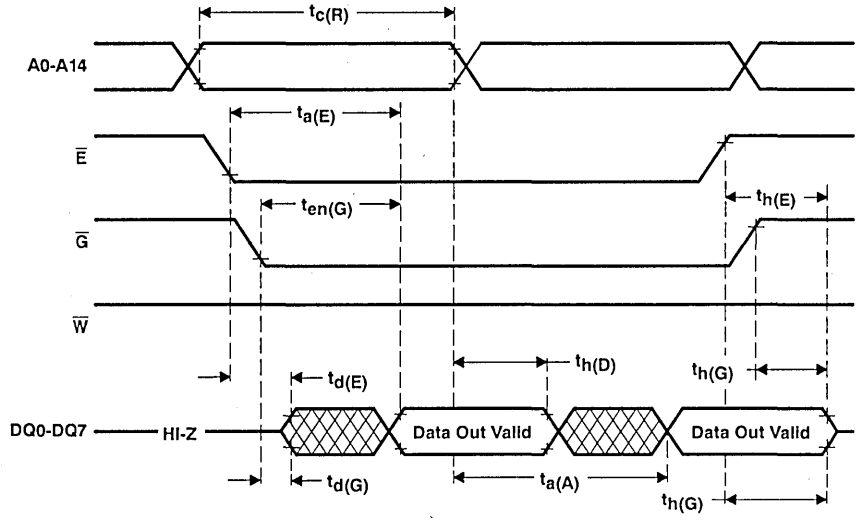
PARAMETER		'29F256-170 '29F258-170 '29F259-170		'29F256-200 '29F258-200 '29F259-200 '29F256-20 '29F258-20 '29F259-20		'29F256-250 '29F258-250 '29F259-250 '29F256-25 '29F258-25 '29F259-25		'29F256-300 '29F258-300 '29F259-300 '29F256-30 '29F258-30 '29F259-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		170		200		250		300	ns
$t_{a(E)}$	Access time from chip enable		170		200		250		300	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		75		85		100		120	ns
$t_{c(R)}$	Read cycle time	170		200		250		300		ns
$t_{d(E)}$	Delay time, chip enable low to output	10	40	15	50	20	60	25	70	ns
$t_{d(G)}$	Delay time, output enable low to output	10	40	15	50	20	60	25	70	ns
$t_{h(E)}$	Hold time, chip enable to HI-Z output	10	40	15	50	20	60	25	70	ns
$t_{h(G)}$	Hold time, output enable to HI-Z output	10	40	15	50	20	60	25	70	ns
$t_{h(D)}$	Hold time, data valid to address	20	40	30	50	40	60	50	70	ns

† These parameters are guaranteed in regular read mode only.

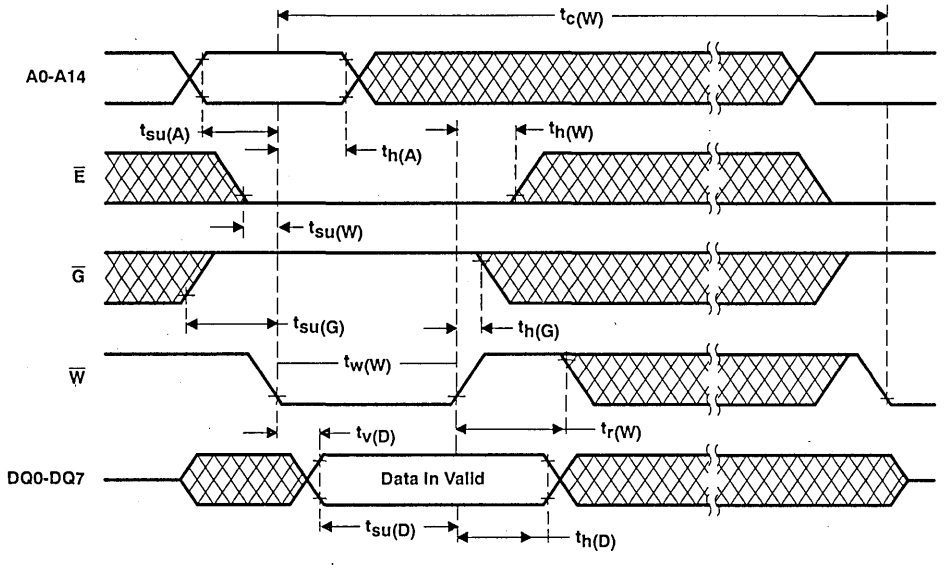
timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
$t_{c(W)}$	Write cycle time		15	ms
$t_{c(W)B}$	Byte load cycle time	1	100	µs
$t_{su(A)}$	Address setup time	10		ns.
$t_{su(W)}$	Write setup time	0		ns
$t_{su(D)}$	Data setup time	80		ns
$t_{su(G)}$	Output enable setup time	10		ns
$t_{h(A)}$	Address hold time	150		ns
$t_{h(W)}$	Write hold time	0		ns
$t_{h(G)}$	Output enable hold time	10		ns
$t_{h(D)}$	Data hold time	10		ns
$t_{w(W)}$	Write pulse duration	200		ns
$t_{r(W)}$	Write high recovery time	800		ns
$t_{rec(W)}$	Write high recovery time in page mode	800		ns
$t_{r(E)}$	Chip enable high recovery time	800		ns
$t_{v(D)}$	Data valid time		300	µs
$t_{w(E)}$	Chip enable pulse duration	200		ns

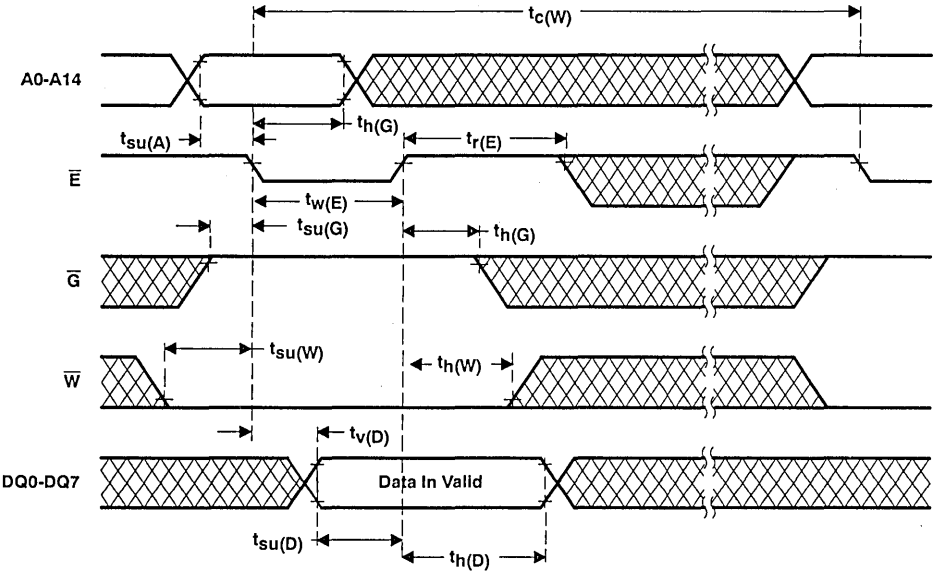
read cycle



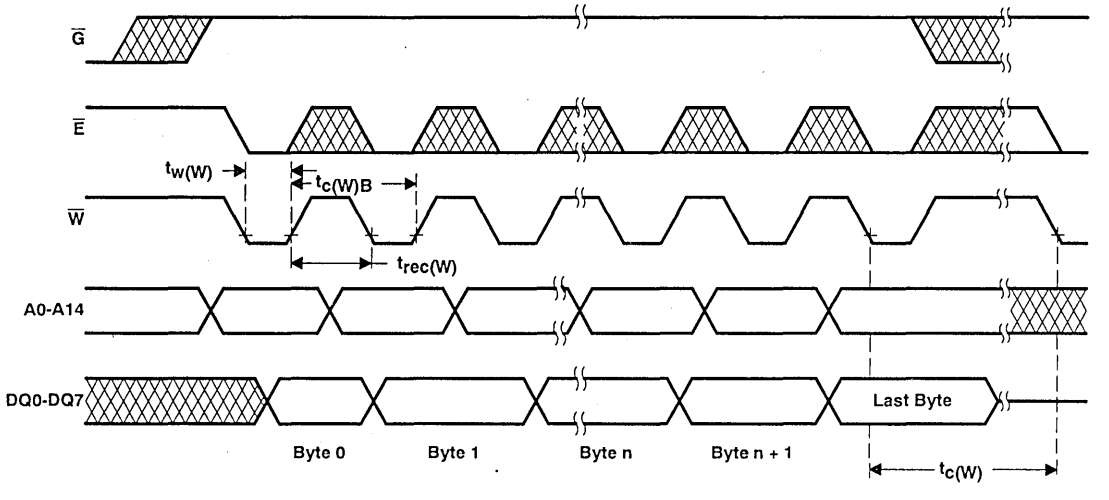
$\overline{W}$ controlled write cycle



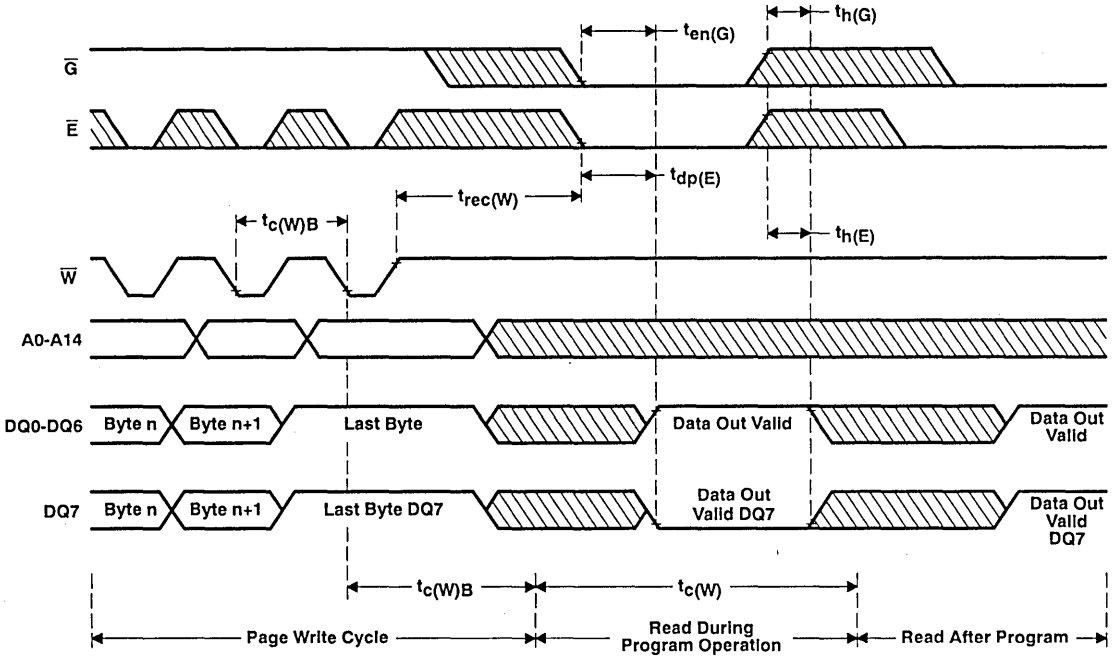
$\overline{E}$ controlled write cycle



page write cycle

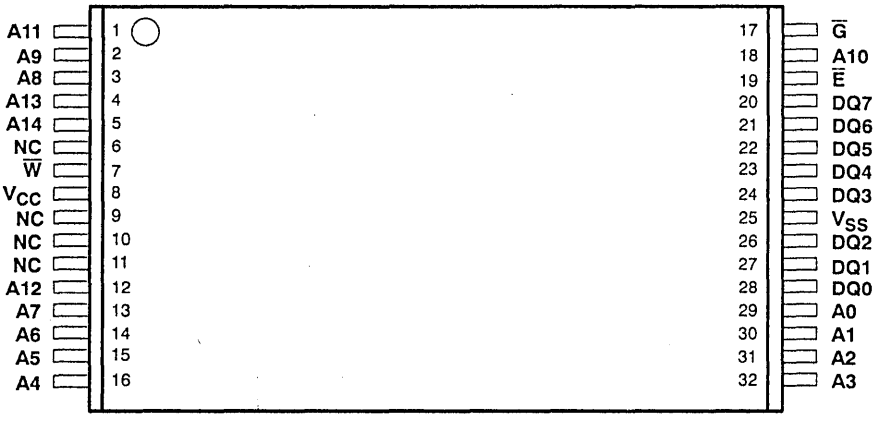


data polling



The following 32-pin Thin Small-Outline Package (TSOP) is under developement by Texas Instruments for the TMS29F259. Please see *Chapter 14, Mechanical Data* for complete package specifications.

DD Package†
Top View



† The package shown is for pinout reference only.

ADVANCE INFORMATION

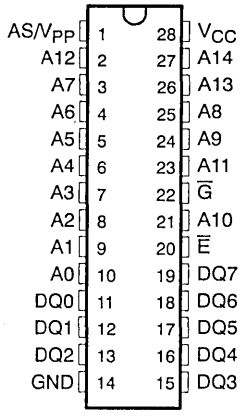
SMLS857 — NOVEMBER 1990

- **Organization . . . 32K × 8**
- **Single 5-V Power Supply**
- **Intergrated Address Latch**
- **Max Access/Min Cycle Time (V_{CC} ± 5%)**

TMS87C257-150	**150 ns**
TMS87C257-1	**170 ns**
TMS87C257-2	**200 ns**
TMS87C257	**250 ns**

- **Power-Saving CMOS Technology**
- **Very High-Speed SNAP! Pulse Programming**
- **3-State Output Buffers**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **— Active . . . 263 mW Worst Case**
  - **— Standby . . . 1.4 mW Worst Case (CMOS Input Levels)**

J Package
(Top View)



PIN NOMENCLATURE	
A0-A14	Address Inputs
$\overline{E}$	Chip Enable/Powerdown
$\overline{G}$	Output Enable
GND	Ground
NC	No Internal Connection
NU	Make No External Connection
DQ0-DQ7	Inputs (programming)/Outputs
V_{CC}	5-V Power Supply
AS/V_{PP}	Address Strobe/13-V Programming Power Supply

description

The TMS87C257 series are 262 144-bit, ultra-violet-light erasable, electrically programmable read-only memories.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs(including program data inputs) can be driven by Series 74 TTL circuits without the use of external pullup resistors. Each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus.

The TMS87C257 incorporates internal address latches on address inputs A0-A7. The internal address latch allows address and data pins to be tied directly to the processor's multiplexed address/data pins which can simplify design, reduce chip connect, and lower the cost of multiplexed bus systems.

The TMS87C257 is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS87C257 is characterized for operation from – 40°C to 85°C (E suffix).

These EPROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 13 V supply is needed for programming . All programming signals are TTL level. These devices are programmable by the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of four seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation listed in the following table. The read mode requires a single 5-V supply. AS/V_{PP} during programming requires 13 V for SNAP! Pulse and 12 V on A9 for signature mode.

FUNCTION	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
AS/V_{PP}	V_{IL}§	X	X	V_{PP}	V_{PP}	V_{PP}	V_{IH}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0-DQ7	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	C2

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.
§ V_{IL} latches the address inputs A0-A7, V_{IH} unlatches those inputs.

read/output disable

When the outputs of two or more TMS87C257s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to the $\overline{G}$ pin while the device is powered up ($\overline{E}$ is low). Output data is accessed at pins DQ0 through DQ7.

latchup immunity

Latchup immunity on the TMS87C257 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family"*, available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 30 mA to 250 μA (CMOS-level inputs) by applying a high-level (CMOS) signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state, independent of $\overline{G}$. Data and address inputs are at static CMOS levels.

erasure

Before programming, the TMS87C257 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). EPROM erasure before programming is necessary to assure that all bits are in the logic high state. Logic lows are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light. The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS87C257, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed zero low can be erased only by ultraviolet light.

SNAP! Pulse programming

The 256K latched CMOS EPROM is programmed using the TI SNAP! Pulse programming algorithm as illustrated by the flowchart in Figure 1, which can reduce time to a nominal of four seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins DQ0 to DQ7. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when AS/V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{G} = V_{IH}$, and $\overline{E} = V_{IL}$. During the programming mode, the address latch becomes effectively transparent. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP}$ = 5 V.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified with AS/V_{PP} = 13 V when $\overline{G} = V_{IL}$ and $\overline{E} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., $A0 = V_{IL}$ accesses the manufacturer code, which is output on DQ0-DQ7; $A0 = V_{IH}$ accesses the device code, which is output on DQ0-DQ7. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit DQ7. The manufacturer code for these devices is 97, and the device code is C2.

memory address lines

Fifteen memory address lines (A0-A14) are provided on the device and are used in conjunction with $\overline{G}$ and $\overline{E}$ to select one of 32 768 eight bit locations in the memory array. Addresses A0 through A7 are latched on the negative edge of the address strobe signal.

address strobe line

The address strobe (AS) input is multiplexed with V_{PP} on pin 1. The negative edge of AS latches the low order address lines (A0-A7) to demultiplex the address/data bus while the positive edge of AS unlatches these address lines.

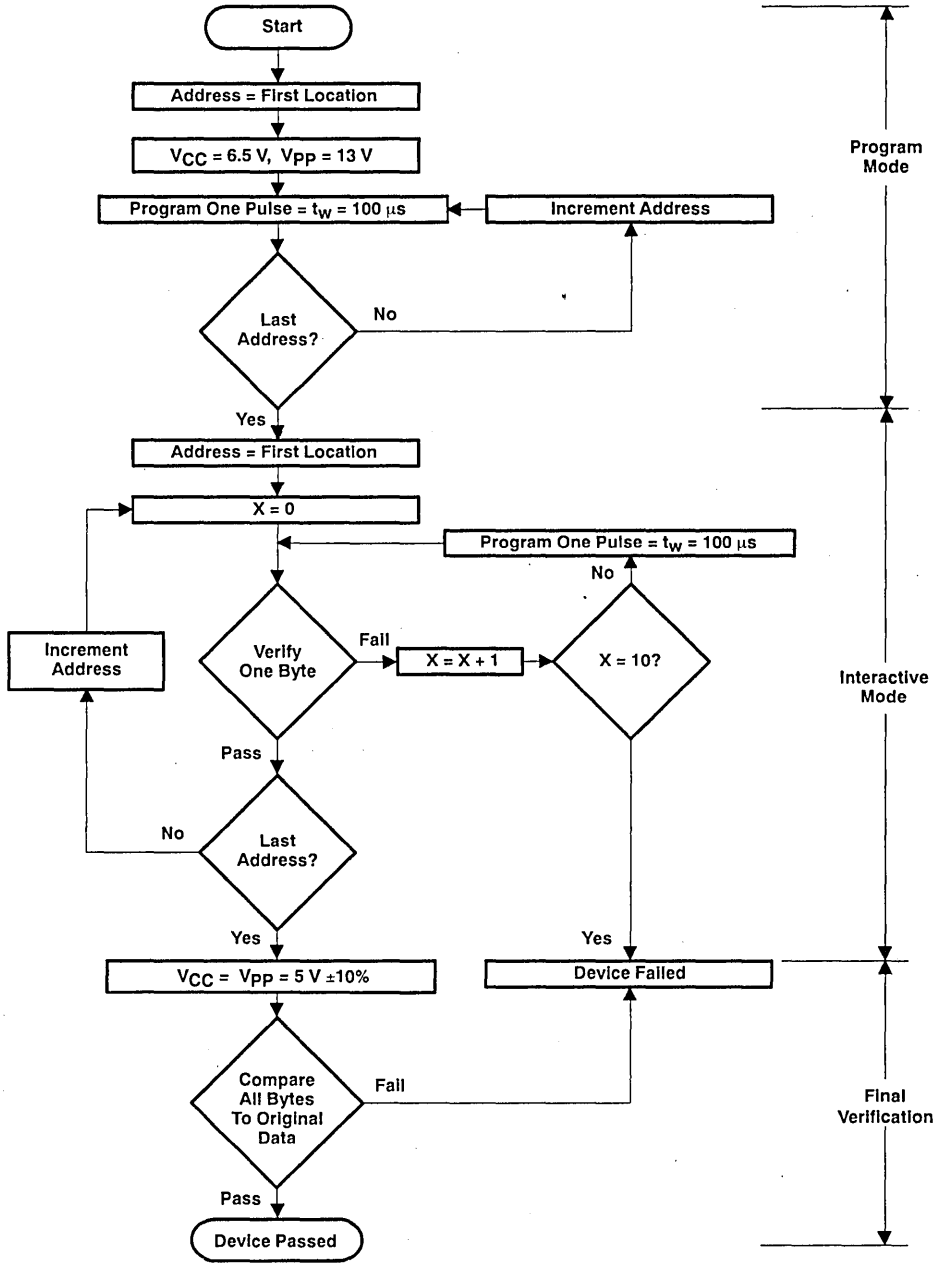
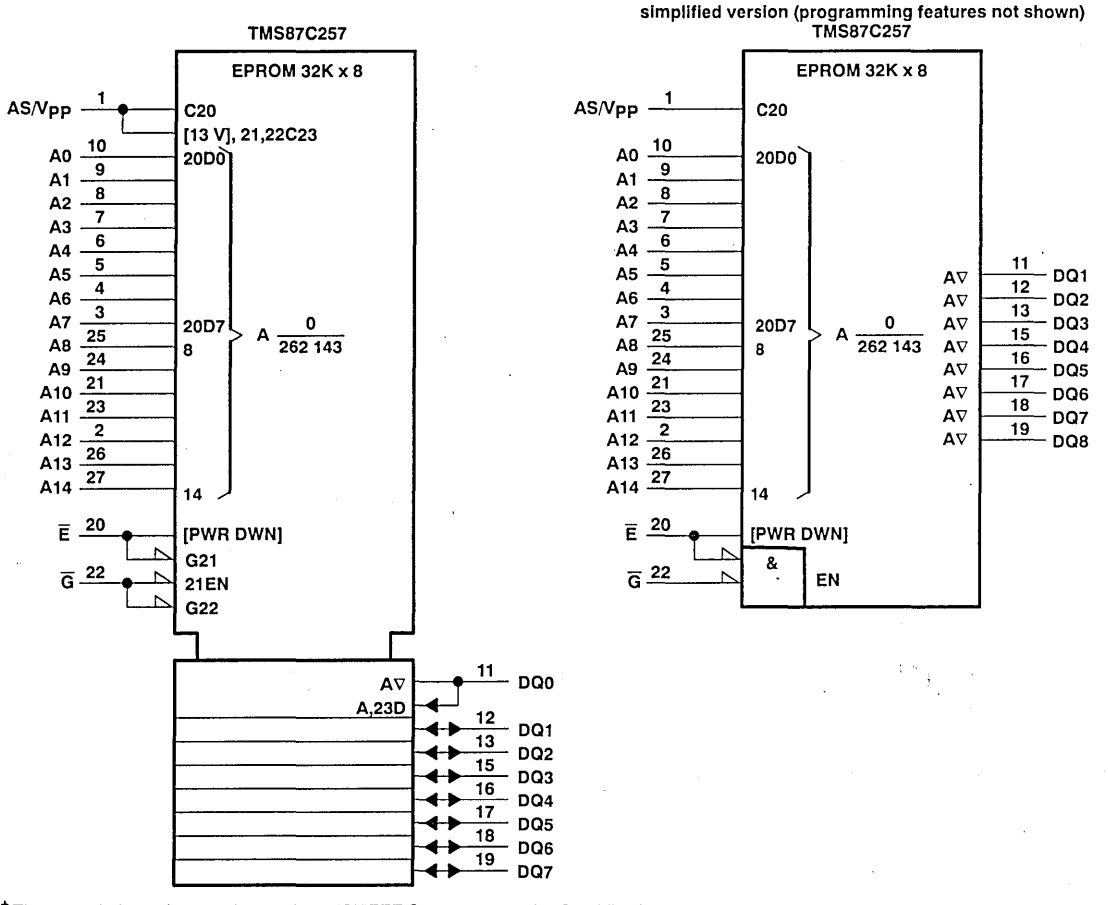


Figure 1. SNAP! Pulse Programming Flowchart

logic symbol†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} ..... – 0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 ..... – 0.6 V to 6.5 V
A9 ..... – 0.6 V to 13.5 V
Output voltage range (see Note 1) ..... – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('87C257-_ _JE ..... – 40° C to 85°C
Storage temperature range ..... – 65°C to 150°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			TMS87C257-150 TMS87C257-1 TMS87C257-2 TMS87C257			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.75	5	5.25	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode (see Note 3)	VCC – 0.6		VCC + 0.6	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	
V_{IH}	High-level input voltage (CMOS)		VCC × 0.7		VCC + 1	V
V_{IL}	Low-level input voltage (CMOS)		– 0.5		0.8	V
T_A	Operating free-air temperature		– 40		85	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 2.5 mA	3.5			V
			I_{OH} = – 20 μA	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
			I_{OL} = 20 μA			0.1	
I_I	Input current (leakage)		V_I = 0 to 5.5 V			±1	μA
I_O	Output current (leakage)		V_O = 0 to V_{CC}			±1	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		1	10	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	250	μA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		15	30	mA

†Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance §	V_I = 0, f = 1 MHz		6	10	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz		10	14	pF

†Typical values are at T_A = 25°C and nominal voltages.
‡ Capacitance measurements are made on a sample basis only.
§ AS/V_{PP} is not included in input capacitance.

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 & 5)	'87C257-150		'87C257-1		'87C257-2		'87C257		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq$ 20 ns, Input $t_f \leq$ 20 ns		150		170		200		250	ns
$t_{a(E)}$	Access time from chip enable			150		170		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		0		ns
$t_{su(AS)}$	Address to AS/V_{PP} fall		20		20		20		20		ns
$t_{w(AS)}$	Address strobe pulse width		90		90		90		90		ns
$t_{h(AS)}$	Address hold from AS/V_{PP} fall		30		30		30		30		ns

†Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V, T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to V_{CC} × 0.7 V. Timing measurements are made at 3 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)

5. Common test conditions apply for the t_{dis} except during programming.

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V, T_A = 25°C (see Note 4)

		MIN	NOM	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	95	100	105	µs
$t_{su(A)}$	Address setup time	2			µs
$t_{su(G)}$	$\overline{G}$ setup time	2			µs
$t_{su(E)}$	$\overline{E}$ setup time	2			µs
$t_{su(D)}$	Data setup time	2			µs
$t_{su(VPP)}$	V_{PP} setup time	2			µs
$t_{su(VCC)}$	V_{CC} setup time	2			µs
$t_{h(A)}$	Address hold time	0			µs
$t_{h(D)}$	Data hold time	2			µs

NOTE 4: For all switching characteristics the input pulse levels are 0.4 V to V_{CC} × 0.7 V. Timing measurements are made at 3 V for logic high and 0.8 V for logic low). (reference AC Testing Waveform)

PARAMETER MEASUREMENT INFORMATION

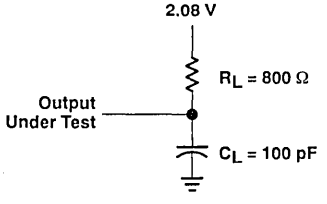
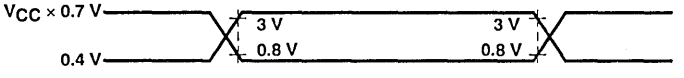


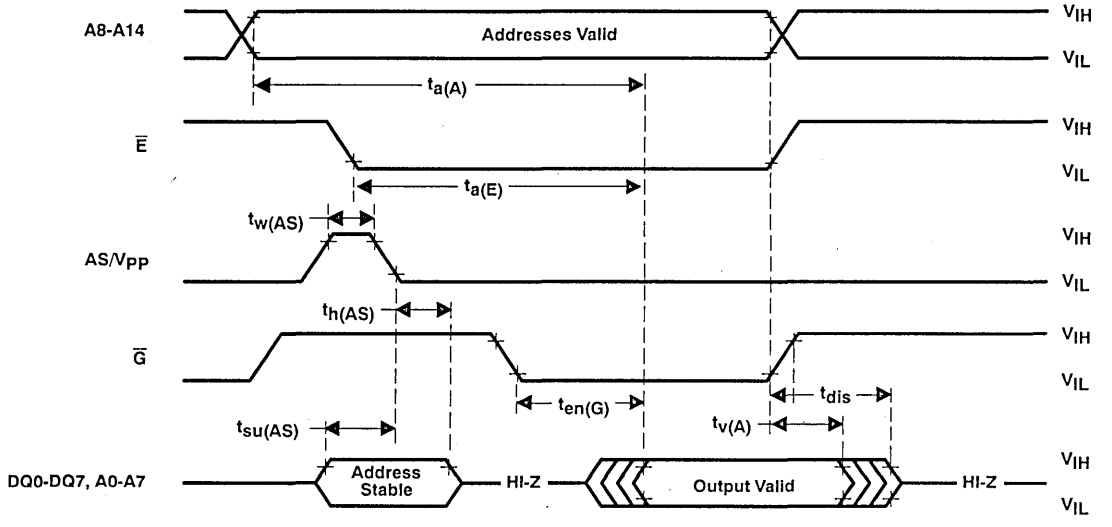
Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms

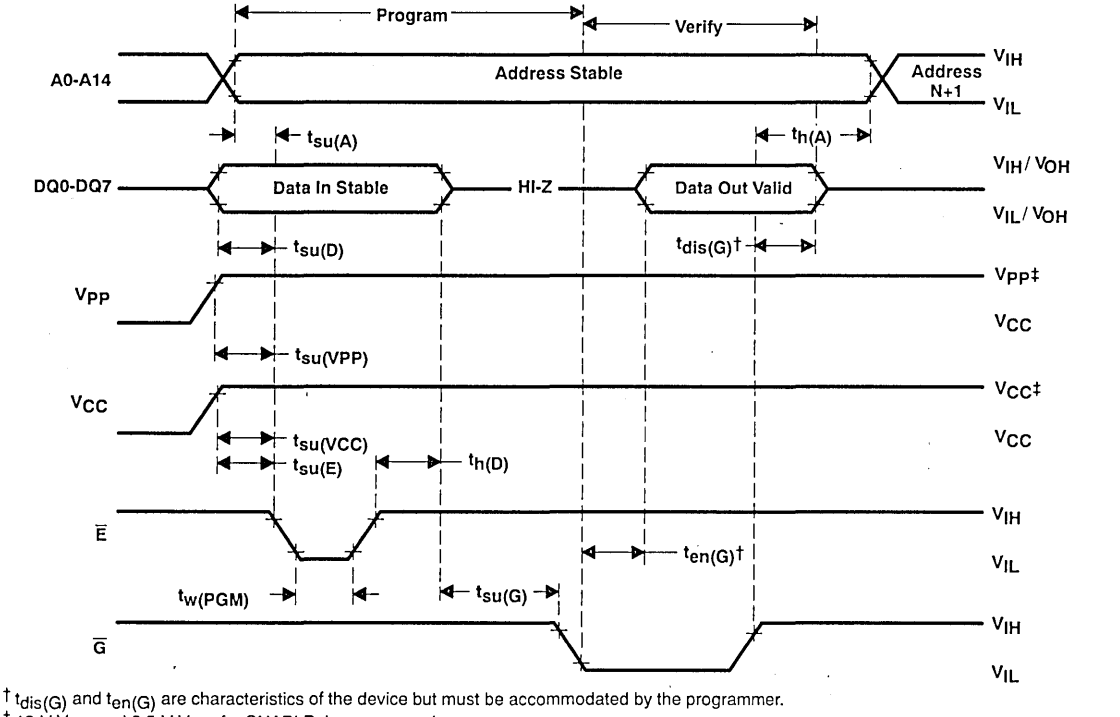


A.C. testing inputs are driven at V_{CC} × 0.7 V for logic high and 0.4 V for logic low. Timing measurements are made at 3 V for logic high and 0.8 V for logic low for both inputs and outputs.

read cycle timing



program cycle timing (SNAP! Pulse programming)



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

TMS27C510 524 288-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC510 524 288-BIT PROGRAMMABLE READ-ONLY MEMORY

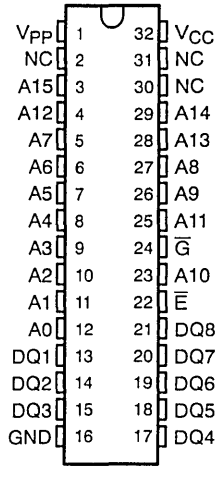
SMLS510 — AUGUST 1990

- Organization . . . 64K × 8
- Single 5-V Power Supply
- Pin Compatible With Existing 1 Meg MOS ROMs, PROMs, and EPROMs
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Times

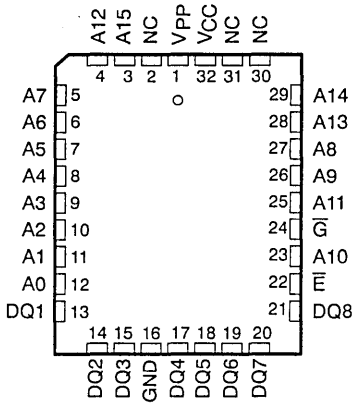
V_{CC} ± 5%	V_{CC} ± 10%	
'27C/PC510-120	'27C510-12	120 ns
'27C/PC510-150	'27C/PC510-15	150 ns
'27C/PC510-170	'27C/PC510-17	170 ns
'27C/PC510-200	'27C/PC510-20	200 ns
'27C/PC510-250	'27C/PC510-25	250 ns

- Power Saving CMOS Technology
- Very High Speed SNAP! Pulse Programming
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity With Standard TTL Loads
- Latchup Immunity of 250 mA on All Input and Output Lines
- Low Power Dissipation (V_{CC} = 5.25 V)
  - Active . . . 158 mW Worst Case
  - Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)
- PEP4 Version Available With 168 Hour Burn-In, and Choices of Operating Temperature Range
- 512K EPROM Available with MIL-STD-883C Class B High Reliability Processing (SMJ27C510)

J and N Packages
(Top View)



FM Package
(Top View)



PIN NOMENCLATURE	
A0-A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
DQ1-DQ8	Inputs (programming)/Outputs
V_{CC}	5-V Power Supply
V_{PP}	12-13 V Programming Power Supply

description

The TMS27C510 series are 524 288-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC510 series are 524 288-bit, one-time, electrically programmable read-only memories.

These devices are fabricated using power saving CMOS technology for high speed and simple inter-

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face with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C510 and the TMS27PC510 are pin compatible with 32-pin 1M MOS ROMs, PROMs, and EPROMs.

The TMS27C510 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C510 is available with two choices of temperature ranges of 0°C to 70°C and – 40°C to 85°C (TMS27C510-_ _ JL and TMS27C510- _ _ JE, respectively). The TMS27C510 is also offered with 168 hour burn-in on both temperature ranges (TMS27C510-_ _ JL4 and TMS27C510- _ _ JE4, respectively). (See table below).

The TMS27PC510 PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC510 is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix). The TMS27PC510 is specified for operation from 0°C to 70°C, and – 40°C to 85°C.

All package styles conform to JEDEC standards.

EPROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C TO 70°C	– 40°C TO 85°C	0°C TO 70°C	– 40°C TO 85°C
TMS27C510-XXX	JL	JE	JL4	JE4
TMS27PC510-XXX	NL, FML	NE, FME	—	NE4, FME4

These EPROMs and PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 12-13 V supply is needed for programming. All programming signals are TTL level. These devices are programmable by a SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13.0 V and a V_{CC} of 6.5 V for a nominal programming time of seven seconds. For programming outside the system, existing EPROM programers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13.0 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ1-DQ8	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	15

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C510s or TMS27PC510s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ1 to DQ8.

latchup immunity

Latchup immunity on the TMS27C510 and TMS27PC510 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001; *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family."*

powerdown

Active I_{CC} current can be reduced from 30 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure (TMS27C510)

Before programming, the TMS27C510 EPROM is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is 15 watt-seconds per square centimeter. A typical 12-milliwatt-per-square-centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C510, the window should be covered with an opaque label. After erasure (all bits in logic 1 state), logic 0s are programmed into the desired locations. A programmed zero can be erased only by ultraviolet light.

initializing (TMS27PC510)

The one-time programmable TMS27PC510 PROM is provided with all bits in logic 1 state, then logic 0s are programmed into the desired locations. Logic 0s programmed into a PROM cannot be erased.

SNAP! Pulse programming

The 512K EPROM and PROM can be programmed using the TI SNAP! Pulse programming algorithm as illustrated by the flowchart of Figure 1, which can reduce programming time to a nominal of 7 seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins DQ1 to DQ8. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13.0 V, V_{CC} = 6.5 V, $\overline{G} = V_{IH}$, and $\overline{E} = V_{IL}$. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP}$ = 5 V.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 13.0 V when $\overline{G} = V_{IL}$ and $\overline{E} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., A0 = V_{IL} accesses the manufacturer code which is output on DQ1-DQ8; A0 = V_{IH} accesses the device code which is output on DQ1-DQ8. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit DQ8. The manufacturer code for these devices is 97, and the device code is 15.

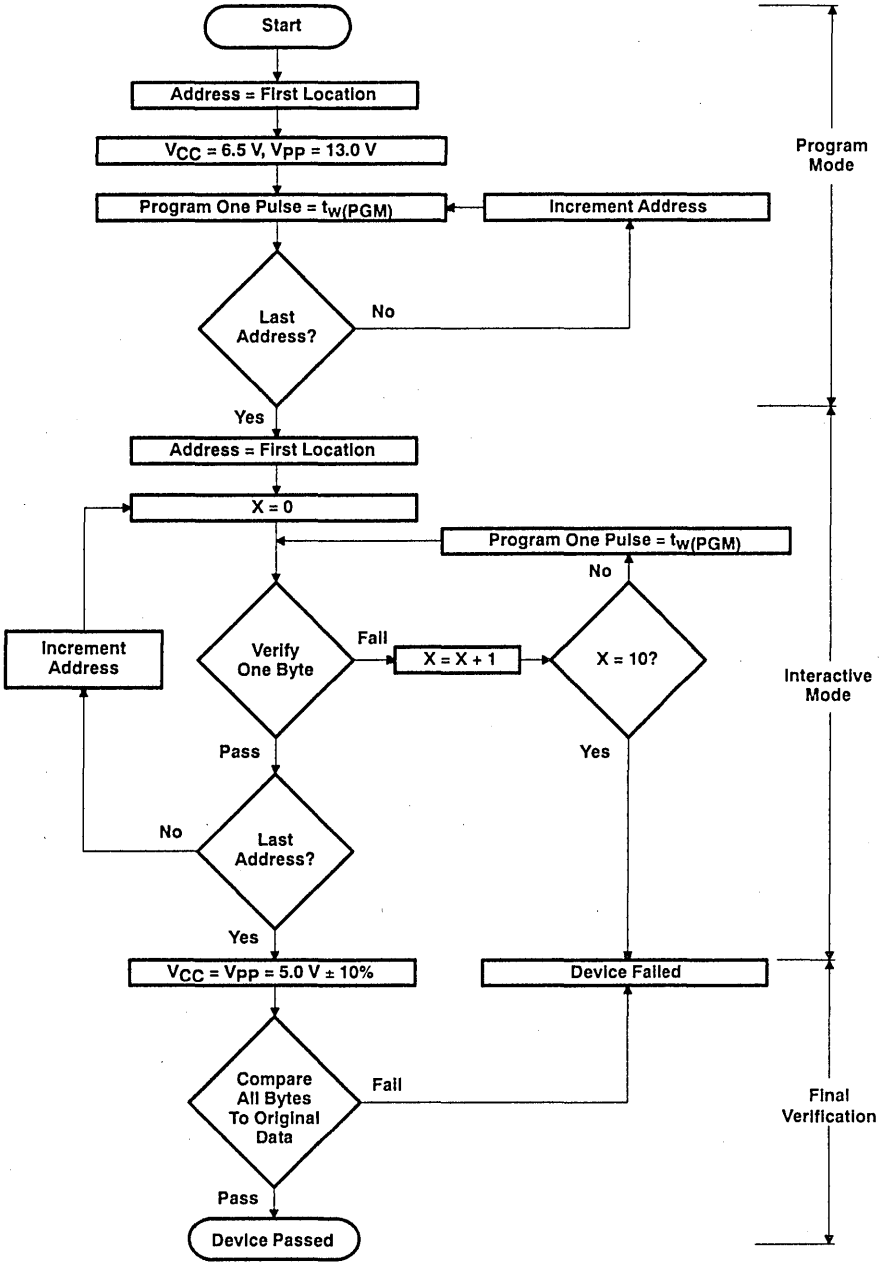
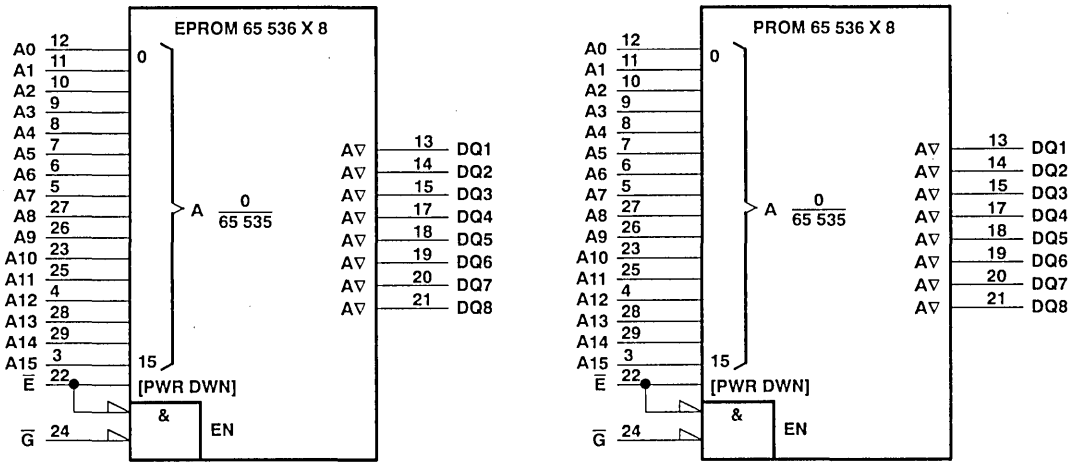


Figure 1. SNAP! Pulse Programming Flowchart

ADVANCE INFORMATION

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
J and N packages illustrated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... – 0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 ..... – 0.6 V to 6.5 V
A9 ..... – 0.6 V to 13.5 V
Output voltage range (see Note 1) ..... – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C510- _ _ JL and JL4;
'27PC510- _ _ NL, FML, NE, and FME) ..... 0°C to 70°C
Operating free-air temperature range ('27C510- _ _ JE, JE4, NE4, and FME4) ..... – 40°C to 85°C
Storage temperature range ..... – 65°C to 150°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			'27C510-120, '27C510-150, '27PC510-150, '27C510-170, '27PC510-170, '27C510-200, '27PC510-200, '27C510-250, '27PC510-250			'27C510-12, '27C510-15, '27PC510-15, '27C510-17, '27PC510-17, '27C510-20, '27PC510-20, '27C510-25, '27PC510-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.75	5	5.25	4.5	5	5.5	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode (see Note 3)	$V_{CC}-0.6$		$V_{CC}+0.6$	$V_{CC}-0.6$		$V_{CC}+0.6$	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	12.75	13	13.25	
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		0.2	−0.5		0.2	
T_A	Operating free-air temperature (see Table, page 2)		(see Table, page 2)			(see Table, page 2)			°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −2.5 mA	3.5			V
			I_{OH} = −20 µA	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
			I_{OL} = 20 µA			0.1	
I_I	Input current (leakage)		V_I = 0 to 5.5 V			±1	µA
I_O	Output current (leakage)		V_O = 0 to V_{CC}			±1	µA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		1	10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		250	500	µA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	250	
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		15	30	mA

† Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		6	10	pF
C_o	Output capacitance	V_O = 0, f = 1 MHz		10	14	pF

† Typical values are at T_A = 25°C and nominal voltages.
‡ Capacitance measurements are made on sample basis only.

ADVANCE INFORMATION

ADVANCE INFORMATION

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C510-120 '27C510-12		'27C510-150 '27PC510-150 '27C510-15 '27PC510-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		120		150	ns
$t_{a(E)}$	Access time from chip enable			120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		75	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	45	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C510-170 '27PC510-170 '27C510-17 '27PC510-17		'27C510-200 '27PC510-200 '27C510-20 '27PC510-20		'27C510-250 '27PC510-250 '27C510-25 '27PC510-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		170		200		250	ns
$t_{a(E)}$	Access time from chip enable			170		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

† Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming, V_{CC} = 6.5 V and V_{PP} = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 4)

			MIN	NOM	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTES: 4. For all switching characteristics, the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic 1 and 0.8 V for logic 0. (Reference page 7-65.)
5. Common test conditions apply for the t_{dis} except during programming.

PARAMETER MEASUREMENT INFORMATION

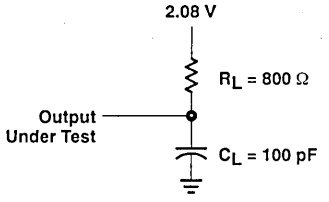
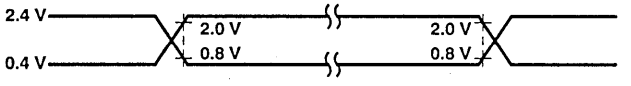


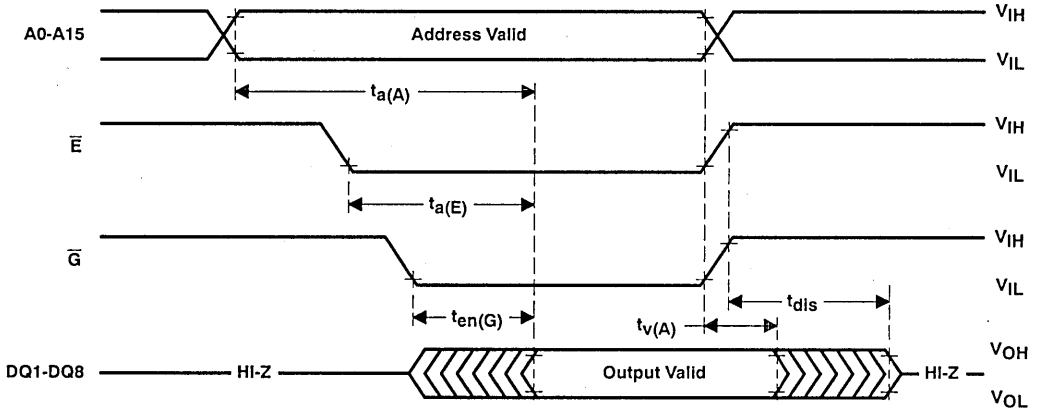
Figure 3. Output Load Circuit

AC testing input/output wave forms



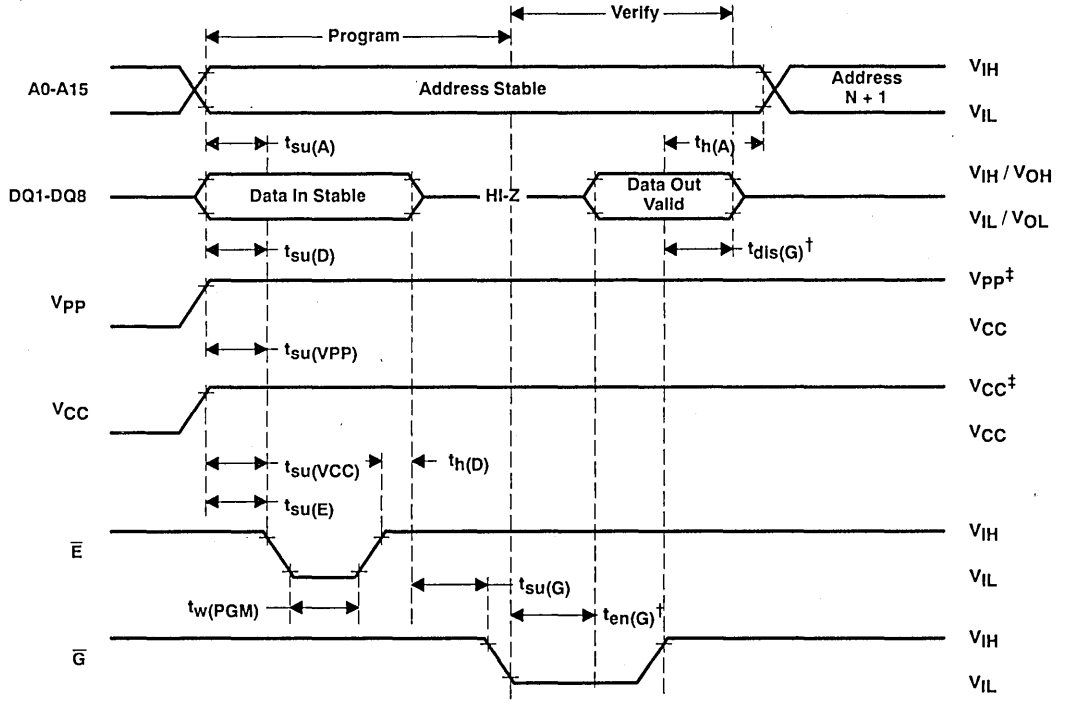
AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

read cycle timing



ADVANCE INFORMATION

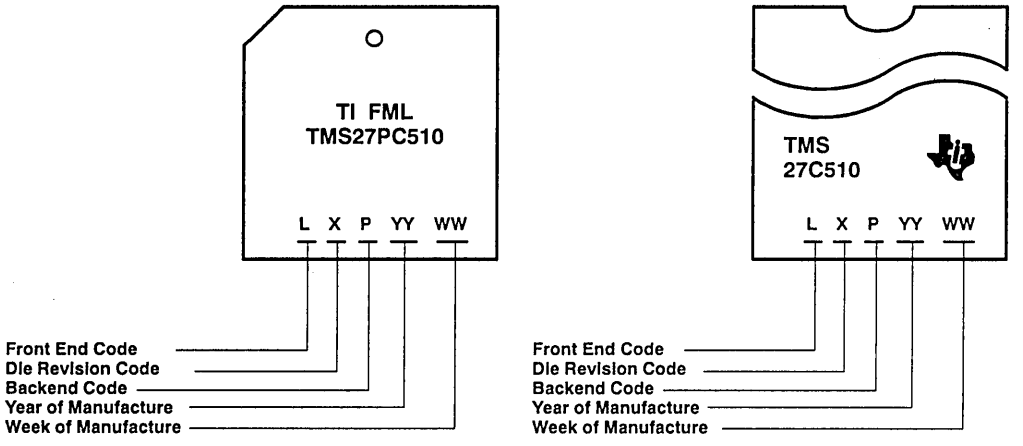
program cycle timing



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13.0-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

ADVANCE INFORMATION

device symbolization

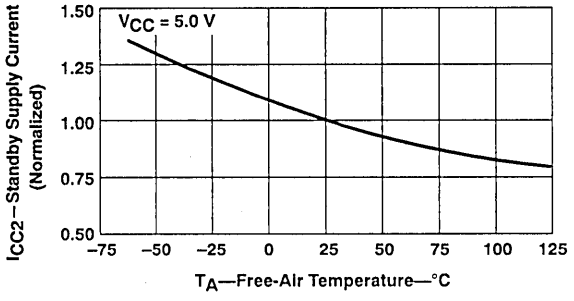


ADVANCE INFORMATION

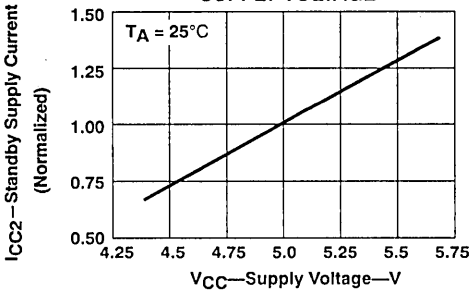
ADVANCE INFORMATION

TYPICAL TMS27C/PC510 CHARACTERISTICS

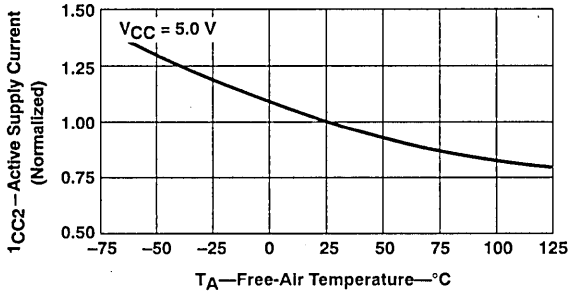
STANDBY SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



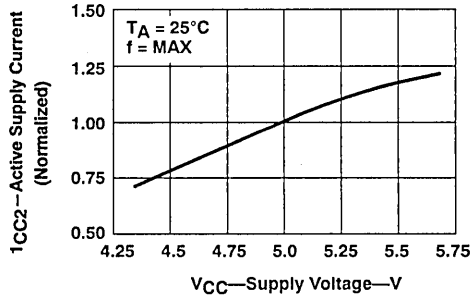
STANDBY SUPPLY CURRENT
vs
SUPPLY VOLTAGE



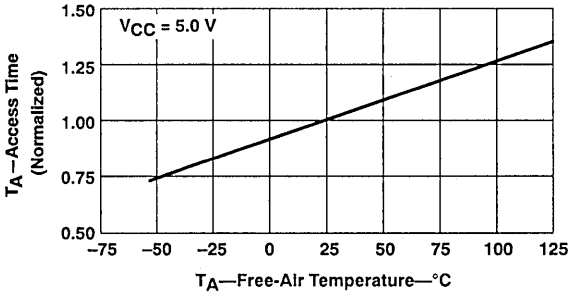
ACTIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



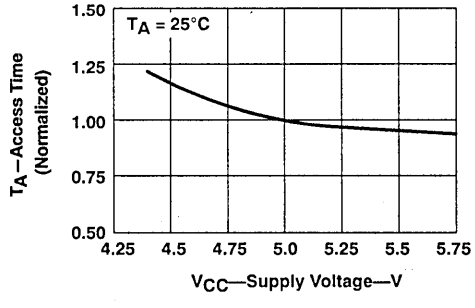
ACTIVE SUPPLY CURRENT
vs
SUPPLY VOLTAGE



ACCESS TIME
vs
FREE-AIR TEMPERATURE



ACCESS TIME
vs
SUPPLY VOLTAGE



TMS27C512 524 288-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC512 524 288-BIT PROGRAMMABLE READ-ONLY MEMORY

SMLS512D – NOVEMBER 1985 – REVISED OCTOBER 1990

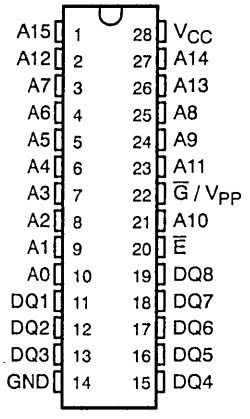
This Data Sheet is Applicable to All TMS27C512s and TMS27PC512s Symbolized with Code "B" as Described on Page 7-79.

- **Organization . . . 64K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 512K MOS ROMs, PROMs, and EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**

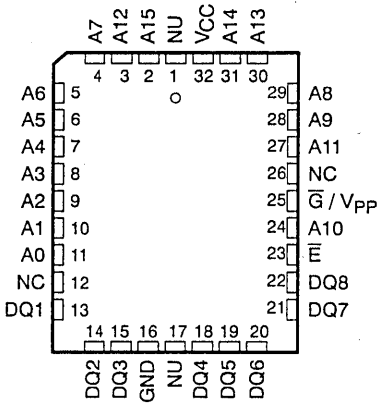
V_{CC} ± 5%	V_{CC} ± 10%	
'27C/PC512-100	'27C/PC512-10	100 ns
'27C/PC512-120	'27C/PC512-12	120 ns
'27C/PC512-150	'27C/PC512-15	150 ns
'27C/PC512-2	'27C/PC512-20	200 ns
'27C/PC512	'27C/PC512-25	250 ns

- **Power Saving CMOS Technology**
- **Very High-Speed SNAP! Pulse Programming**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation (V_{CC} = 5.25 V)**
  - **— Active . . . 158 mW Worst Case**
  - **— Standby . . . 1.4 mW Worst Case (CMOS Input Levels)**
- **PEP4 Version Available With 168 Hour Burn-in, and Choices of Operating Temperature Ranges**
- **512K EPROM Available With MIL-STD-883C Class B High Reliability Processing (SMJ27C512)**

J and N Packages
(Top View)



FM Package
(Top View)



PIN NOMENCLATURE	
A0-A15	Address Inputs
$\overline{E}$	Chip Enable/Powerdown
$\overline{G}$ / V_{PP}	13 V Programming Power Supply
GND	Ground
NC	No Internal Connection
NU	Make No External Connection
DQ1-DQ8	Inputs (Programming) / Outputs
V_{CC}	5-V Power Supply

description

The TMS27C512 series are 524 288-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC512 series are 524 288-bit, one-time, electrically programmable read-only memories.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C512 and the TMS27PC512 are pin compatible with 28-pin 512K MOS ROMs, PROMs, and EPROMs.

The TMS27C512 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC512 OTP PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC512 OTP PROM is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix).

The TMS27C512 and TMS27PC512 are offered with two choices of temperature ranges of 0°C to 70°C and – 40°C to 85°C (TMS27C512-_ _JL and TMS27C512-_ _JE; TMS27PC512-_ _NL and TMS27PC512-_ _NE; TMS27PC512-_ _FML and TMS27PC512-_ _FME respectively). The TMS27C512 and TMS27PC512 are also offered with 168-hour burn-in on both temperature ranges (TMS27C512-_ _JL4 and TMS27C512-_ _JE4; TMS27PC512-_ _NL4 and TMS27PC512-_ _NE4; TMS27PC512-_ _FML4 and TMS27PC512-_ _FME4, respectively); see table below.

All package styles conform to JEDEC standards.

EPROM AND OTP PROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C TO 70°C	– 40°C TO 85°C	0°C TO 70°C	– 40°C TO 85°C
TMS27C512-XXX	JL	JE	JL4	JE4
TMS27PC512-XXX	NL	NE	NL4	NE4
TMS27PC512-XXX	FML	FME	FML4	FME4

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 13-V supply is needed for programming. All programming signals are TTL level. The device is programmed using TI's SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13-V and a V_{CC} of 6.5-V for a nominal programming time of seven seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$ / V_{PP}	V_{IL}	V_{IH}	X†	V_{PP}	V_{IL}	V_{PP}	V_{IL}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ1-DQ8	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	85

† X can be V_{IL} or V_{IH}.
‡ VH = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C512s or TMS27PC512s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ / V_{PP} pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 through Q8.

latchup immunity

Latchup immunity on the TMS27C512 and TMS27PC512 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family"*, available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL / CMOS signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure (TMS27C512)

Before programming, the TMS27C512 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 angstroms). EPROM erasure before programming is necessary to assure that all bits are in the logic high state. Logic lows are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light. The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C512, the window should be covered with an opaque label.

initializing (TMS27PC512)

The one-time programmable TMS27PC512 PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into a PROM cannot be erased.

SNAP! Pulse programming

The 512K EPROM and OTP PROM is programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which programs in a nominal time of seven seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins DQ1 to DQ8. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved with $\overline{G}$ / V_{PP} = 13 V, V_{CC} = 6.5 V, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = 5 V, $\overline{G}$ / V_{PP} = V_{IL}, and $\overline{E}$ = V_{IL}.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified when $\overline{G}$ / V_{PP} and $\overline{E}$ = V_{IL}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., A0 = V_{IL} accesses the manufacturer code, which is output on DQ1-DQ8; A0 = V_{IH} accesses the device code, which is output on DQ1-DQ8. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit DQ8. The manufacturer code for these devices is 97, and the device code is 85.

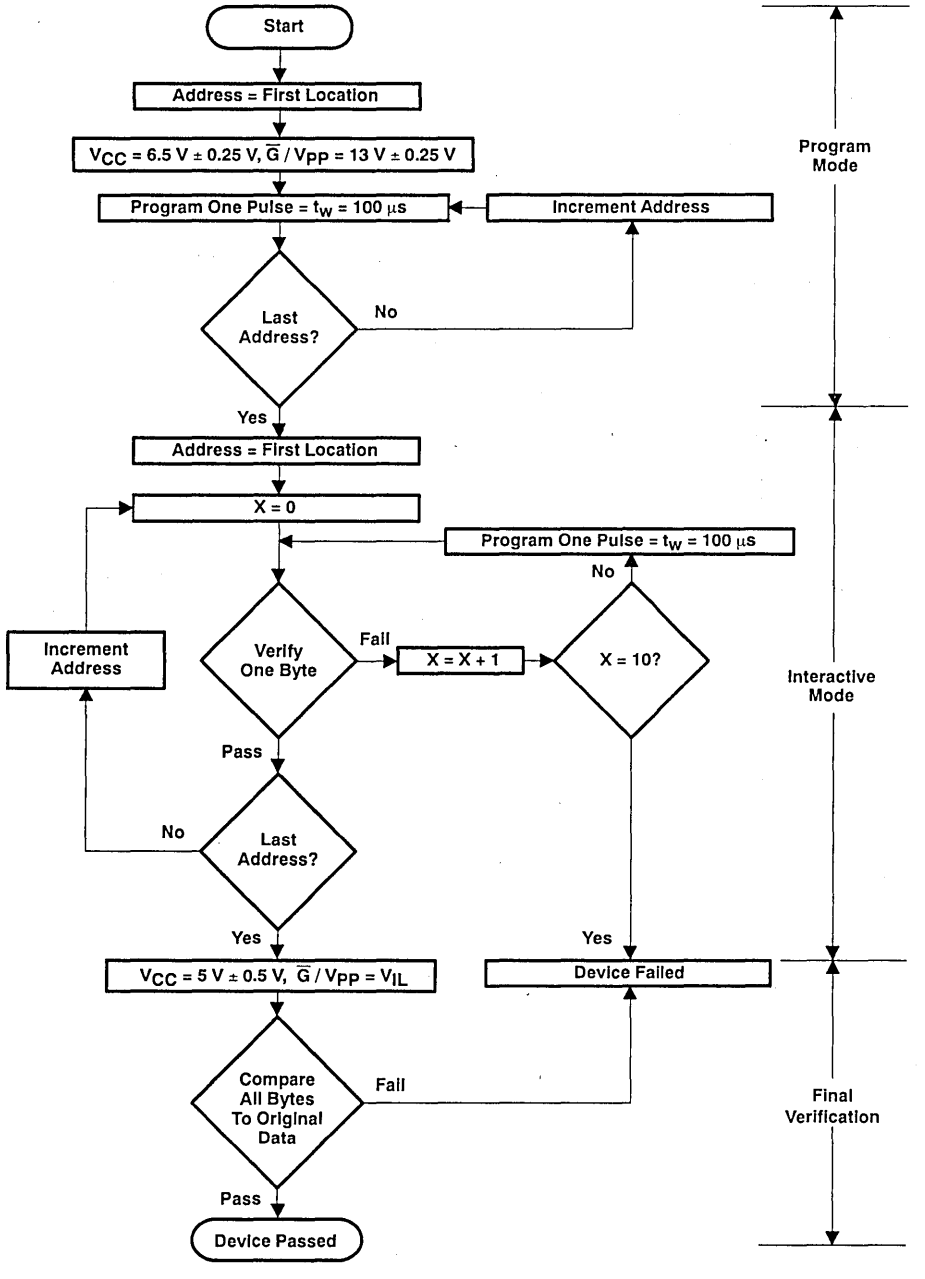
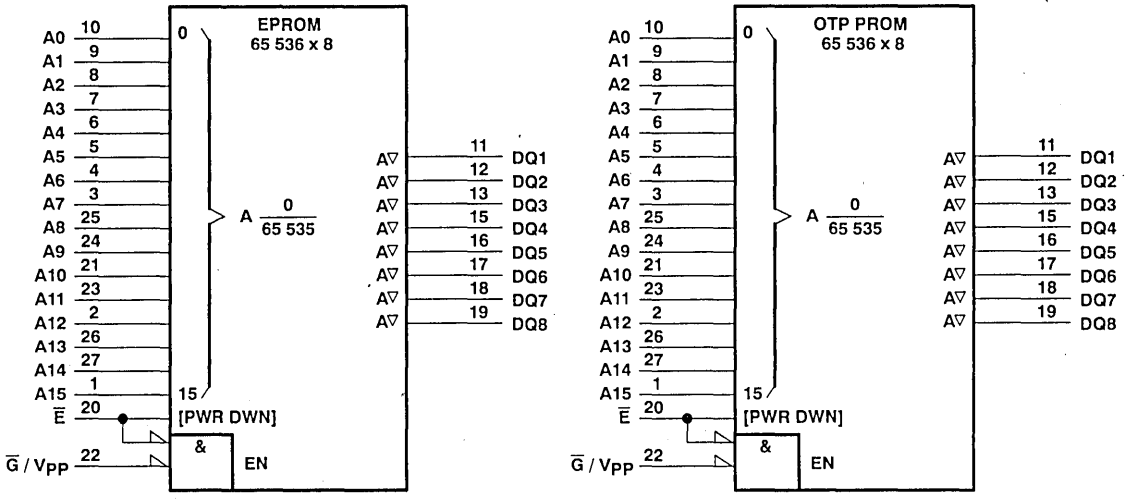


Figure 1. SNAP! Pulse Programming Flowchart

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} ..... – 0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 ..... – 0.6 V to 6.5 V
A9 ..... – 0.6 V to 13.5 V
Output voltage range (see Note 1) ..... – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C512-_ _JL and JL4, '27PC512-_ _NL and NL4, and FML and FML4) ..... 0°C to 70°C
Operating free-air temperature range ('27C512-_ _JE and JE4, '27PC512-_ _NE and NE4, and FME and FME4) ..... – 40°C to 85°C
Storage temperature range ..... – 65°C to 150°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			TMS27C/PC512-100 TMS27C/PC512-120 TMS27C/PC512-150 TMS27C/PC512-2 TMS27C/PC512			TMS27C/PC512-10 TMS27C/PC512-12 TMS27C/PC512-15 TMS27C/PC512-20 TMS27C/PC512-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.75	5	5.25	4.5	5	5.5	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	6.25	6.5	6.75	
$\overline{G}$ / V_{PP}	Supply voltage	SNAP! Pulse programming algorithm	12.75	13	13.25	12.75	13	13.25	V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	
V_{IL}	High-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		0.2	−0.5		0.2	
T_A	Operating free-air temperature	'27C512-_ _JL, JL4 '27PC512-_ _NL, NL4, FML, FML4	0		70	0		70	°C
T_A	Operating free-air temperature	'27C512-_ _JE, JE4 '27PC512-_ _NE, NE4, FME, FME4	−40		85	−40		85	°C

NOTE 2: V_{CC} must be applied before or at the same time as $\overline{G}$ / V_{PP} and removed after or at the same time as $\overline{G}$ / V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −2.5 mA	3.5			V
			I_{OH} = −20 μA	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
			I_{OL} = 20 μA			0.1	
I_I	Input current (leakage)		V_I = 0 to 5.5 V			±1	μA
I_O	Output current (leakage)		V_O = 0 to V_{CC}			±1	μA
I_{PP}	$\overline{G}$ / V_{PP} supply current (during program pulse)		$\overline{G}$ / V_{PP} = 13 V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		250	500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	250	
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		15	30	mA

† Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		6	10	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz		10	14	pF
$C_{G\,/\,VPP}$	$\overline{G}$ / V_{PP} input capacitance	$\overline{G}$ / V_{PP} = 0, f = 1 MHz		20	25	pF

† Typical values are at T_A = 25°C and nominal voltages.
‡ Capacitance measurements are made on a sample basis only.

switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	TMS27C/PC512-100 TMS27C/PC512-10		TMS27C/PC512-120 TMS27C/PC512-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns		100		120	ns
$t_{a(E)}$	Access time from chip enable			100		120	ns
$t_{en(G)}$	Output enable time from $\overline{G}$ / V_{PP}			55		55	ns
t_{dis}	Output disable time from $\overline{G}$ / V_{PP} or $\overline{E}$, whichever occurs first†		0	45	0	45	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$ / V_{PP}, whichever occurs first†		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	TMS27C/PC512-150 TMS27C/PC512-15		UNIT
			MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns		150	ns
$t_{a(E)}$	Access time from chip enable			150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$ / V_{PP}			75	ns
t_{dis}	Output disable time from $\overline{G}$ / V_{PP} or $\overline{E}$, whichever occurs first†		0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$ / V_{PP}, whichever occurs first†		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	TMS27C/PC512-2 TMS27C/PC512-20		TMS27C/PC512 TMS27C/PC512-25		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns		200		250	ns
$t_{a(E)}$	Access time from chip enable			200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$ / V_{PP}			75		100	ns
t_{dis}	Output disable time from $\overline{G}$ / V_{PP} or $\overline{E}$, whichever occurs first†		0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$ / V_{PP}, whichever occurs first†		0		0		ns

† Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6.50 V and $\overline{G}$ / V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$ / V_{PP}	0		130	ns

NOTES: 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (Reference page 7-77).
4. Common test conditions apply for t_{dis} except during programming.

recommended timing requirements for programming: V_{CC} = 6.50 and $\overline{G}/V_{PP}$ = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

		MIN	TYP	MAX	UNIT
$t_{w(IPGM)}$	Inital program pulse duration	95	100	105	µs
$t_{su(A)}$	Address setup time	2			µs
$t_{su(D)}$	Data setup time	2			µs
$t_{su(VPP)}$	$\overline{G}$ / V_{PP} setup time	2			µs
$t_{su(VCC)}$	V_{CC} setup time	2			µs
$t_{h(A)}$	Address hold time	0			µs
$t_{h(D)}$	Data hold time	2			µs
$t_{h(VPP)}$	$\overline{G}$ / V_{PP} hold time	2			µs
$t_{rec(PG)}$	$\overline{G}$ / V_{PP} recovery time	2			µs
t_{EHD}	Data valid from $\overline{E}$ low			1	µs
$t_{r(PG)G}$	$\overline{G}$ / V_{PP} rise time	50			ns

NOTE 3: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (Reference below).

PARAMETER MEASUREMENT INFORMATION

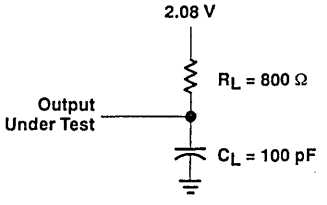
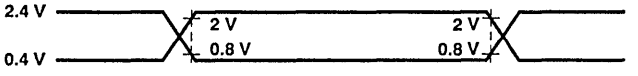


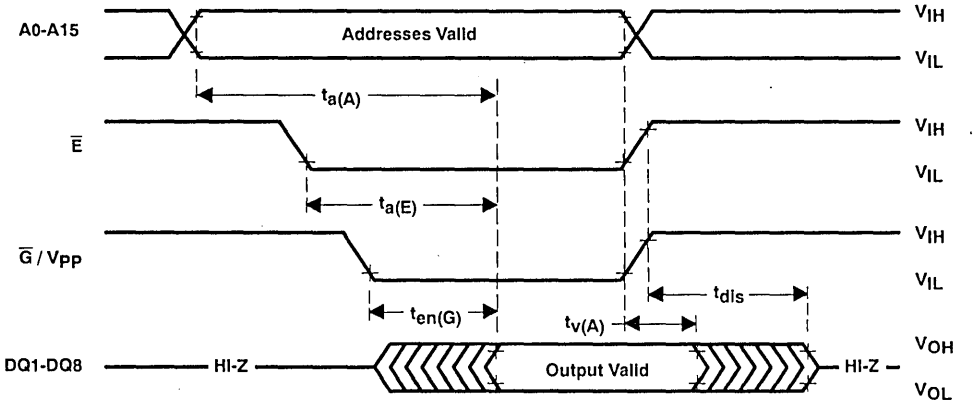
Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms

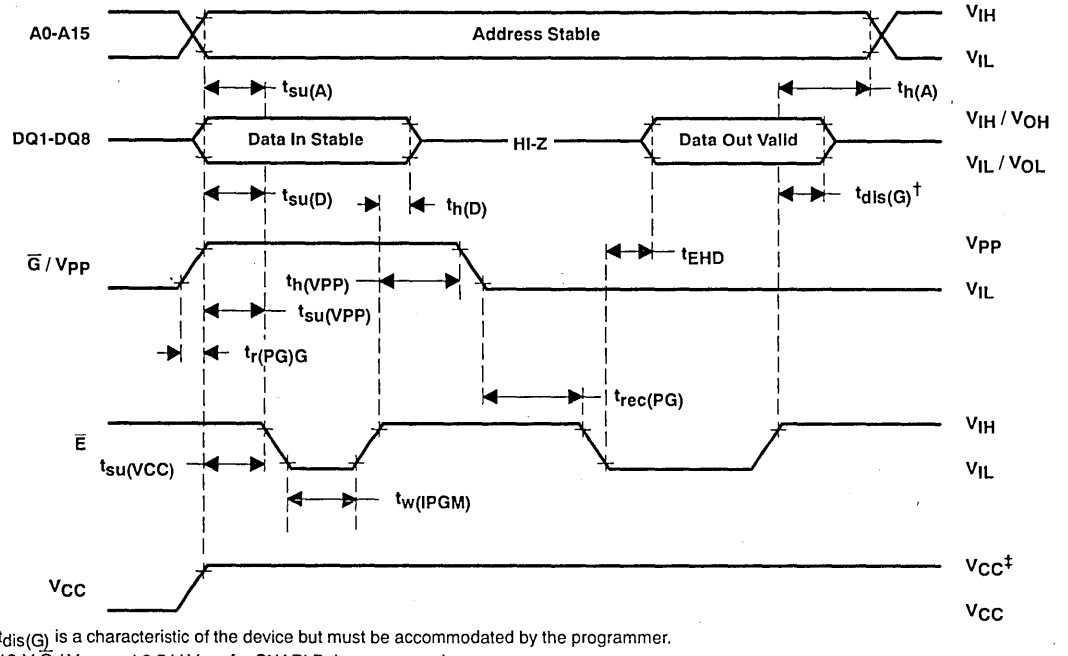


A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

read cycle timing



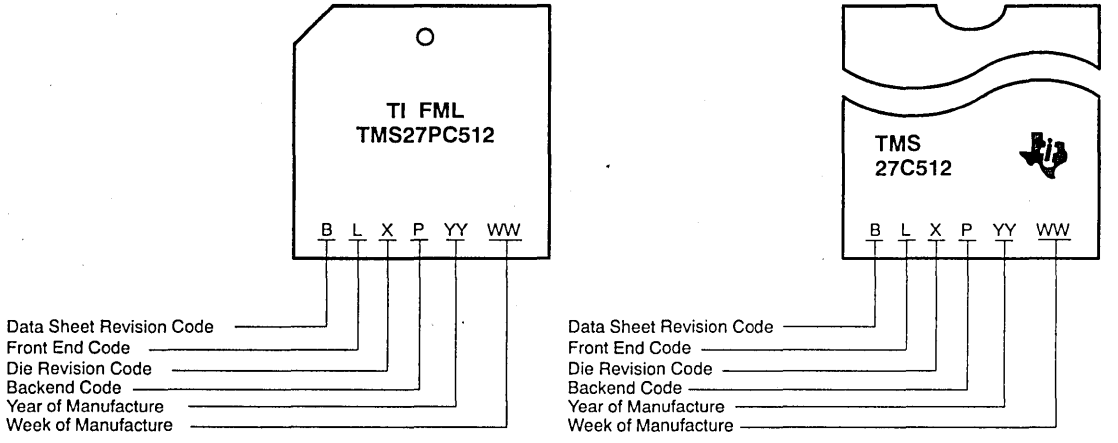
program cycle timing (SNAP! Pulse programming)



† $t_{dis(G)}$ is a characteristic of the device but must be accommodated by the programmer.
‡ 13-V $\overline{G}$ / V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

device symbolization

This data sheet is applicable to all TI TMS27C512 CMOS EPROMs and TMS27PC512 CMOS OTP PROMs with the data sheet revision code "B" as shown below.

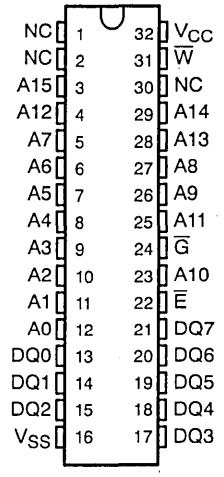


- Organization 64K × 8 or 2 Blocks of 32K × 8 Each
- Single 5-V Power Supply
- HVCMOS Technology
- All Inputs/Outputs TTL Compatible
- Max Access/Min Cycle Time

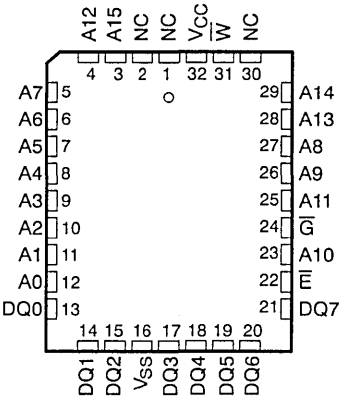
V_{CC} ± 5%	V_{CC} ± 10%	
'29F512-100		100 ns
'29F512-120	'29F512-12	120 ns
'29F512-150	'29F512-15	150 ns
'29F512-200	'29F512-20	200 ns

- Self-Timed Erasure of the Entire Memory or Block-Erase Option (2 Blocks) Before any Reprogramming (20 ms Max)
- Single Byte and Page (128 Bytes) Program:
  - — Latched Address and Data
  - — Self-Timed Programming Operation (10 ms Max)
  - — Data Polling Verification
- 1000- and 10 000-Cycle Endurance Versions
- Software Inadvertent Write Protection
- Software Erase Mode Entry
- Operating Free-Air Temperature Range . . . 0°C to 70°C

N and J Packages
(Top View)



FM Package
(Top View)



description

The TMS29F512 is a 524 288-bit, programmable read-only memory that can be electrically bulk-erased or block erased and reprogrammed. The device is fabricated using HVCMOS flotox technology for high reliability and very low power dissipation. It performs the erase/program operations automatically with a single 5-V supply voltage, and it can program a single byte or any number of bytes between 1 and 128.

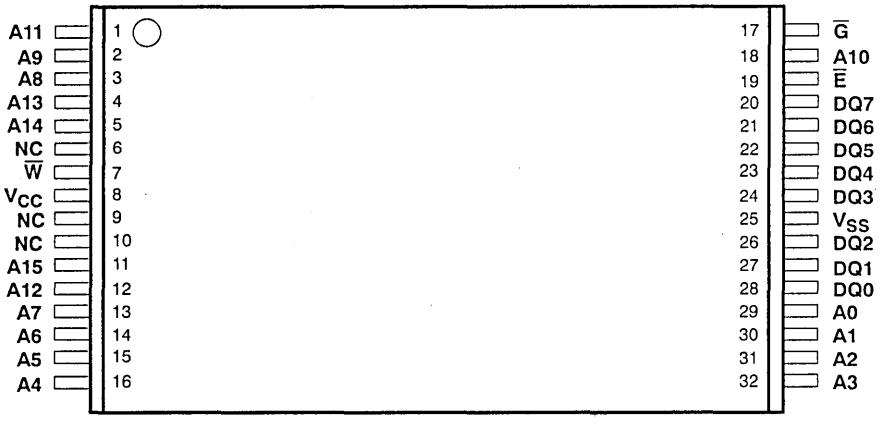
PIN NOMENCLATURE	
A0-A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Internal Connection
$\overline{W}$	Write Enable
DQ0-DQ7	Data In/Data Out
V_{CC}	5-V Power Supply
V_{SS}	Ground

The TMS29F512 Flash/Block EEPROM is offered in a dual-in-line ceramic package (J suffix) and a dual-in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2-mm (600-mil) centers. The TMS29F512 is also offered in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix). These packages are characterized for operation from 0°C to 70°C.

ADVANCE INFORMATION

The following 32-pin Thin Small-Outline Package (TSOP) is under developement by Texas Instruments for the TMS29F512. Please see *Chapter 14, Mechanical Data* for complete package specifications.

DD Package†
Top View



† The package shown is for pinout reference only.

ADVANCE INFORMATION

TMS27C010A 1 048 576-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC010A 1 048 576-BIT PROGRAMMABLE READ-ONLY MEMORY

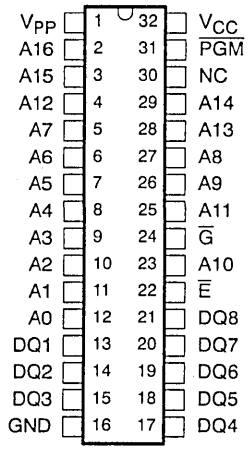
SMLS110 — NOVEMBER 1990

- Organization . . . 128K × 8
- Single 5-V Power Supply
- Operationally Compatible With Existing Megabit EPROMs
- Industry Standard 32-Pin Dual-In-line Package and 32-Lead Plastic Chip Carrier
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

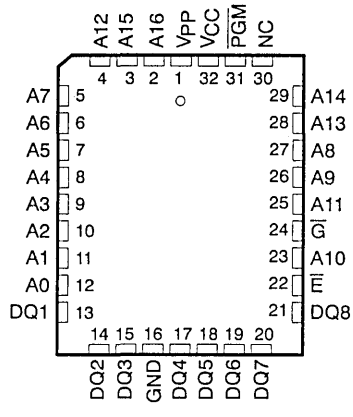
V_{CC} ± 5%	V_{CC} ± 10%	
'27C010A-100		100 ns
'27PC010A-100		100 ns
'27C010A-120	'27C010A-12	120 ns
'27PC010A-120	'27PC010A-12	120 ns
'27C010A-150	'27C010A-15	150 ns
'27PC010A-150	'27PC010A-15	150 ns
'27C010A-200	'27C010A-20	200 ns
'27PC010A-200	'27PC010A-20	200 ns

- 8-Bit Output For Use in Microprocessor-Based Systems
- Very High-Speed SNAP! Pulse Programming
- Power-Saving CMOS Technology
- 3-State Output Buffers
- 400-mV Minimum DC Noise Immunity With Standard TTL Loads
- Latchup Immunity of 250 mA on All Input and Output Pins
- No Pullup Resistors Required
- Low Power Dissipation (V_{CC} = 5.5 V)
  - —Active . . . 165 mW Worst Case
  - —Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)
- PEP4 Version Available With 168 Hour Burn-In and Choices of Operating Temperature Ranges

J Package
(Top View)



FM Package
(Top View)



PIN NOMENCLATURE	
A0-A16	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Internal Connection
$\overline{PGM}$	Program
DQ1-DQ8	Inputs (programming)/Outputs
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply†

†Only in program mode.

description

The TMS27C010A series are 1 048 576-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC010A series are 1 048 576-bit, one-time, electrically programmable read-only memories.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the the use of external pullup resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS27C010A EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C010A is also offered with two choices of temperature ranges of 0°C to 70°C and – 40°C to 85°C (TMS27C010A-_ _JL and TMS27C010A-_ _JE, respectively). The TMS27C010A is also offered with 168 hour burn-in on both temperature ranges (TMS27C010A-_ _JL4 and TMS27C010A-_ _JE4, respectively). (See table below).

The TMS27PC010A OTP PROM is offered in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix). The TMS27PC010A is offered with two choices of temperature ranges of 0°C to 70°C and – 40°C to 85°C (TMS27PC010A-_ _FML and TMS27PC010A-_ _FME, respectively). (See table below).

EPROM AND OTP PROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HOUR BURN-IN VS TEMPERATURE RANGES	
	0°C to 70°C	– 40°C to 85°C	0°C to 70°C	– 40°C to 85°C
TMS27C010A-xxx	JL	JE	JL4	JE4
TMS27PC010A-xxx	FML	FME		

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 13-V supply is needed for programming. All programming signals are TTL level. These devices are programmable using the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of thirteen seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	X	X	X	V_{IL}	V_{IH}	X	X	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ1-DQ8	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	D6

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C010As or TMS27PC010As are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C010A and TMS27PC010A is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family"*, available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 μA for a high TTL input on $\overline{E}$ and to 100 μA for a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27C010A)

Before programming, the TMS27C010A EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C010A, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

initializing (TMS27PC010A)

The one-time programmable TMS27PC010A PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C010A and TMS27PC010A are programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which programs in a nominal time of thirteen seconds. Actual programming time will vary as a function of the programmer used.

The SNAP! Pulse programming algorithm uses an initial pulse of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$. Data is presented in parallel (eight bits) on pins DQ1 through DQ8. Once addresses and data are stable, $\overline{PGM}$ is pulsed low.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP} = 5\ V \pm 10\%$.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pins.

program verify

Programmed bits may be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

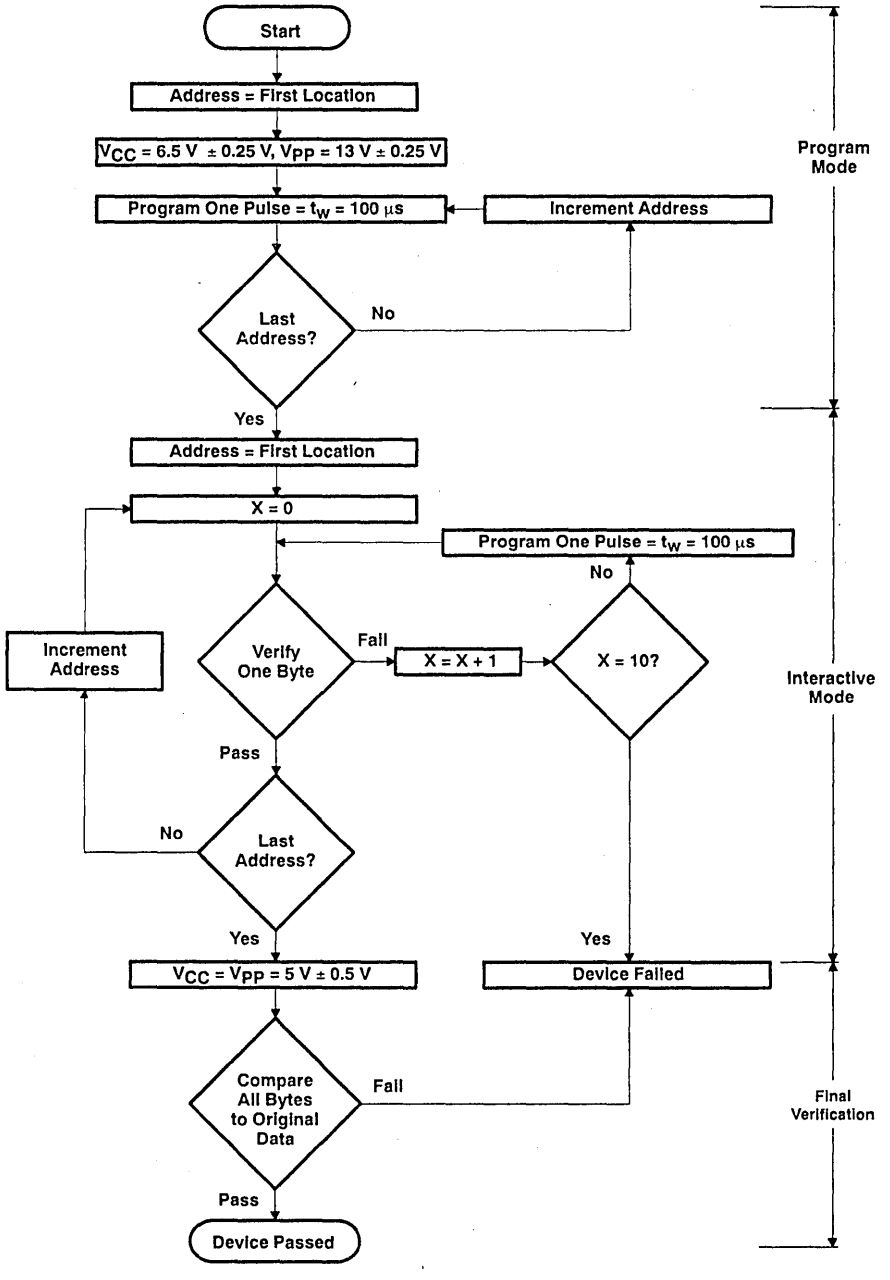


Figure 1. SNAP! Pulse Programming Flowchart

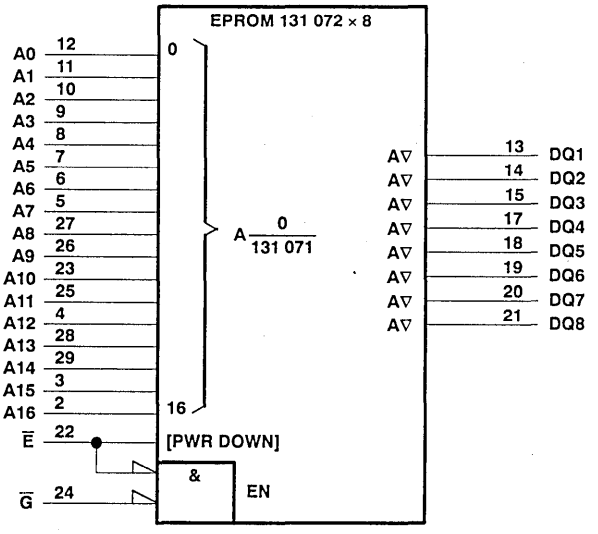
signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12 V. Two identifier bytes are accessed by toggling A0. All addresses must be held low. The signature code for these devices is 97D6. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code D6 (Hex), as shown by the signature mode table below.

IDENTIFIER†	PINS									
	A0	DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	1	1	0	1	0	1	1	0	D6

† $\overline{E} = \overline{G} = V_{IL}$, A1-A8 = V_{IL}, A9 = V_H, A10-A16 = V_{IL}, $V_{PP} = V_{CC}$.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
J package illustrated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} ..... – 0.6 V to 14 V
Input voltage range, All inputs except A9 ..... – 0.6 V to V_{CC} + 1 V
A9 ..... – 0.6 V to 13.5 V
Output voltage range, with respect to V_{SS} (see Note 1) ..... – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C010A-_ _JL and JL4, '27PC010A-_ _FML) ..... 0°C to 70°C
Operating free-air temperature range ('27C010A-_ _JE and JE4, '27PC010A-_ _FME) .... – 40°C to 85°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			'27C010A/PC010A-100, '27C010A/PC010A-120, '27C010A/PC010A-150, '27C010A/PC010A-200			'27C010A/PC010A-12, '27C010A/PC010A-15, '27C010A/PC010A-20			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC} Supply voltage	Read mode (see Note 2)		4.75	5	5.25	4.5	5	5.5	V
	SNAP! Pulse programming algorithm		6.25	6.5	6.75	6.25	6.5	6.75	V
V_{PP} Supply voltage	Read mode (see Note 3)		V_{CC} – 0.6	V_{CC}	V_{CC} + 0.6	V_{CC} – 0.6	V_{CC}	V_{CC} + 0.6	V
	SNAP! Pulse programming algorithm		12.75	13	13.25	12.75	13	13.25	V
V_{IH} High-level input voltage		TTL	2.0		V_{CC} + 0.5	2.0		V_{CC} + 0.5	V
		CMOS	V_{CC} – 0.2		V_{CC} + 0.5	V_{CC} – 0.2		V_{CC} + 0.5	
V_{IL} Low-level input voltage		TTL	– 0.5		0.8	– 0.5		0.8	V
		CMOS	– 0.5		GND + 0.2	– 0.5		GND + 0.2	
T_A Operating free-air temperature		'27C010A-_ _JL,JL4 '27PC010A-_ _FML	0		70	0		70	°C
T_A Operating free-air temperature		'27C010A-_ _JE,JE4 '27PC010A-_ _FME	– 40		85	– 40		85	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}. During programming, V_{PP} must be maintained at 13 V ± 0.25 V.

electrical characteristics over full range of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −20 μA	V_{CC} − 0.2		V
			I_{OH} = −2.5 mA	3.5		
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA		0.4	V
			I_{OL} = 20 μA		0.1	
I_I	Input current (leakage)		V_I = 0 to 5.5 V		±1	μA
I_O	Output current (leakage)		V_O = 0 to V_{CC}		±1	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		10	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$\overline{E}$ = V_{IH}, V_{CC} = 5.5 V		500	μA
		CMOS-input level	$\overline{E}$ = V_{CC} ± 0.2 V, V_{CC} = 5.5 V		100	
I_{CC2}	V_{CC} supply current (active) (output open)		$\overline{E}$ = V_{IL}, V_{CC} = 5.5 V, t_{cycle} = minimum cycle time†, outputs open		30	mA

† Minimum cycle time = maximum access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		4	8	pF
C_o	Output capacitance	V_O = 0, f = 1 MHz		6	10	pF

‡ Capacitance measurements are made on sample basis only.

§ All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 & 5)	'27C010A-100 '27PC010A-100		'27C010A-120 '27PC010A-120 '27C010A-12 '27PC010A-12		'27C010A-150 '27PC010A-150 '27C010A-15 '27PC010A-15		'27C010A-200 '27PC010A-200 '27C010A-20 '27PC010A-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \leq$ 20 ns, Input $t_f \leq$ 20 ns		100		120		150		200	ns
$t_{a(E)}$	Access time from chip enable			100		120		150		200	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		55		75		75	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first¶		0	50	0	50	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first		0		0		0		0		ns

¶ Value calculated from 0.5-V delta to measured output level.

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2.V for logic high and 0.8 V for logic low (reference AC Testing Wave Form).

5. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 4)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference AC Testing Wave Form).

PARAMETER MEASUREMENT INFORMATION

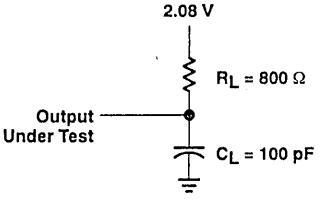
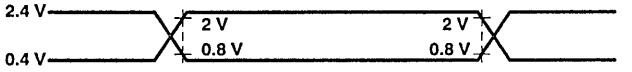


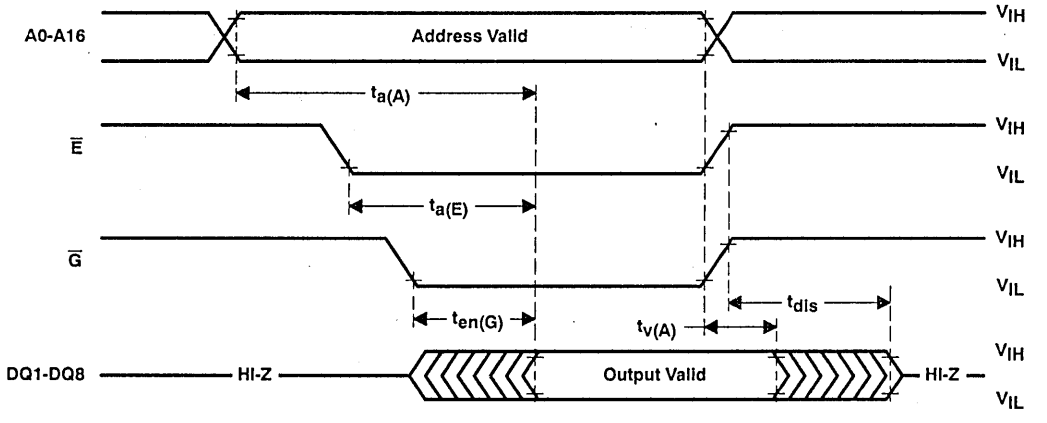
Figure 2. AC Test Output Load Circuit

AC testing input/output wave forms

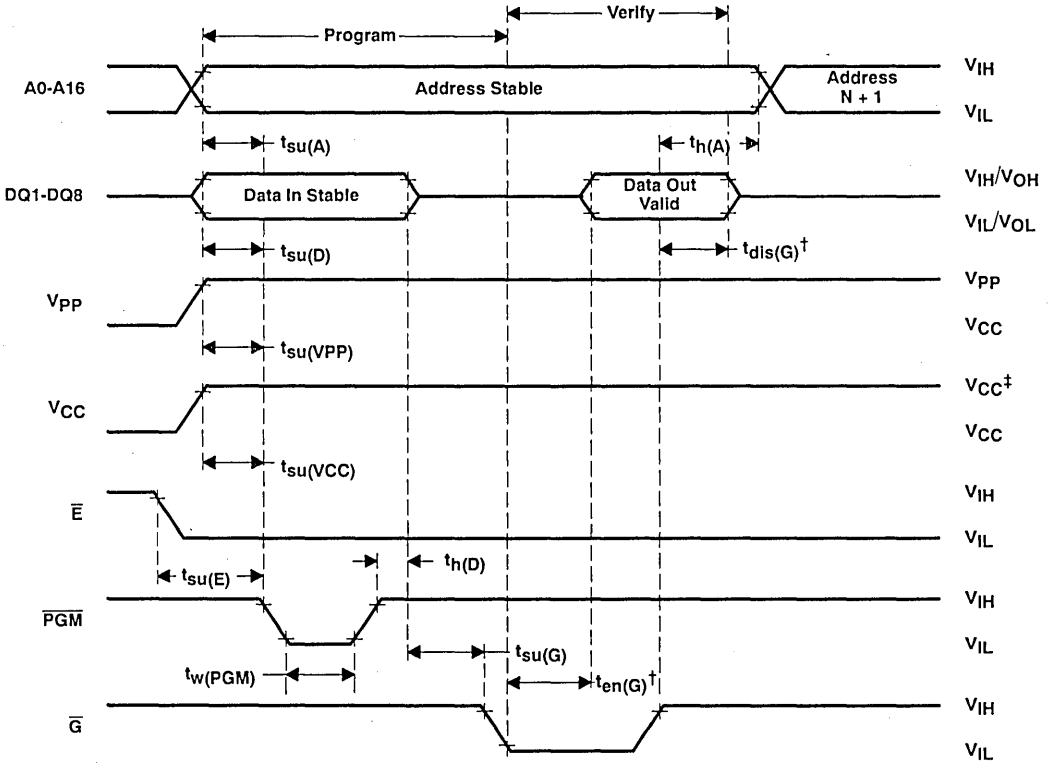


AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

read cycle timing



program cycle timing (SNAP! Pulse programming)



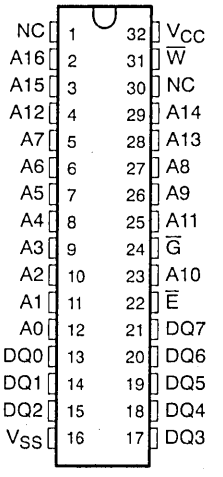
† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

- Organization 128K × 8 or 4 Blocks of 32K × 8 Each
- Single 5-V Power Supply
- HVCMOS Technology
- All Inputs/Outputs TTL Compatible
- Max Access/Min Cycle Time

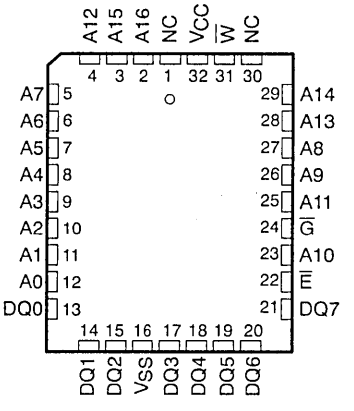
V_{CC} ± 5%	V_{CC} ± 10%	
'29F010-100		100 ns
'29F010-120	'29F010-12	120 ns
'29F010-150	'29F010-15	150 ns
'29F010-200	'29F010-20	200 ns

- Self-Timed Erasure of the Entire Memory Or Block-Erase Option (4 Blocks) Before any Reprogramming (20 ms Max)
- Single Byte and Page (128 Bytes) Program:
  - — Latched Address and Data
  - — Self-Timed Programming Operation (10 ms Max)
  - — Data Polling Verification
- 10K Cycles Endurance
- Software Inadvertent Write Protection
- Software Erase Mode Entry
- Pinout Compatible With EPROM JEDEC Standard
- Low Power Dissipation (V_{CC} = 5.25 V)
  - — Active Write . . . 52.5 mW
  - — Active Read . . . 82.5 mW
  - — Standby . . . 5.25 mW (CMOS-Input Levels)
- PEP4 Version Available With 168 Hour Burn-In, and Choices of Operating Temperature Ranges

N and J Packages
(Top View)



FM Package
(Top View)



PIN NOMENCLATURE	
A0-A16	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Connection
$\overline{W}$	Write Enable
DQ0-DQ7	Data In/Data Out
V_{CC}	5-V Power Supply
V_{SS}	Ground

description

The TMS29F010 is a 1 048 576-bit, programmable read-only memory that can be electrically bulk-erased or block-erased and reprogrammed. The device is fabricated using HVCMOS flotox technology for high reliability and very low power dissipation.

ADVANCE INFORMATION

It performs the erase/program operations automatically with a single 5-V supply, and it can program a single byte or any number of bytes between 1 and 128.

The TMS29F010 Flash/Block EEPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting-hole rows on 15,2-mm (600-mil) centers. The TMS29F010 in the ceramic package is offered with three choices of operating temperature ranges of 0°C to 70°C, – 40°C to 105°C, and – 40°C to 125°C (TMS29F010-_ _ JL, TMS29F010-_ _ JE, and TMS29F010-_ _ JQ, respectively). The TMS29F010 in the ceramic package is also offered with 168 hour burn-in on all temperature ranges (TMS29F010-_ _ JL4, TMS29F010-_ _ JE4, and TMS29F010-_ _ JQ4, respectively); see table.

The TMS29F010 is also offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2-mm (600-mil) centers, and a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix). The plastic-packaged TMS29F010s operating free-air temperature range is from 0°C to 70°C (NL or FML suffix). This temperature range is also offered with 168 hour burn-in (NL4 or FML4 suffix); see table.

The TMS29F010 is organized as 128K × 8 bits or as 4 blocks of 32K × 8 bits each. It features internal circuitry to minimize the external hardware interface that provides latched address and data, self-timed programming, and data polling verification. In the erased state all bits are logic high. To reprogram, all memory bits are erased first, and then those bits that should be logic low are programmed accordingly. During programming the data polling function is enabled to inform the host microprocessor that the memory is busy until the programming is completed.

The TMS29F010 is available in 1 000- and 10 000-cycle endurance versions.

FUNCTION (PINS)§	MODE					
	READ	OUTPUT DISABLE	STANDBY AND WRITE INHIBIT	WRITE	SIGNATURE MODE	
$\overline{E}$ (22)§	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	
$\overline{G}$ (24)§	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	
A0 (12)§	X	X	X	X	V_{IL}	V_{IH}
A9 (26)§	X	X	X	X	V_H‡	
$\overline{W}$ (31)§	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	
DQ0-DQ7 (13-15, 17-21)§	Data Out	HI-Z	HI-Z	Data In	MFG 97	DEVICE F4

† X = V_{IL} or V_{IH}.
‡ 12.5 V < V_H < 15 V.
§ N and J packages.

In the flash-erase operating mode, all memory bits are erased before reprogramming. In the block-erase operating mode, all the bits of a particular block are erased before reprogramming, whereas all the bits of the other three blocks remain unchanged.

FLASH/BLOCK EEPROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN			SUFFIX FOR PEP4 168 ± 8 HR. BURN-IN VS TEMPERATURE RANGES		
	0°C to 70°C	– 40°C to 105°C	– 40°C to 125°C	0°C to 70°C	– 40°C to 105°C	– 40°C to 125°C
TMS29F010-xxx	JL	JE	JQ	JL4	JE4	JQ4
TMS29F010-xxx	NL			NL4		
TMS29F010-xxx	FML			FML4		

operation

read/output disable

When the outputs of two or more TMS29F010s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices.

To read the output of the TMS29F010, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

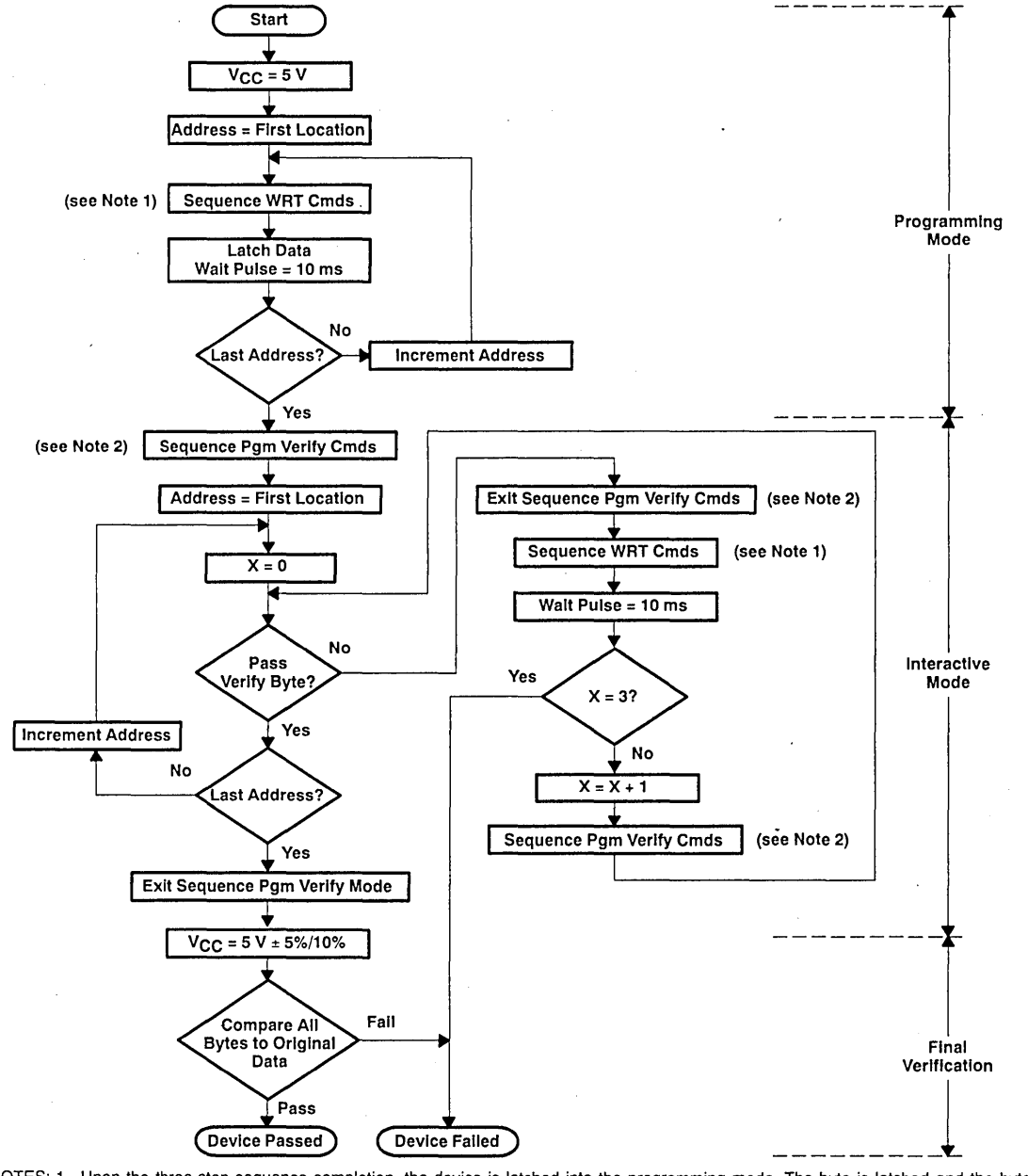
power down

Active I_{CC} current can be reduced from 15 mA to 1 mA typical by applying a high TTL signal to the $\overline{E}$ pin. In this mode all the outputs are in the high-impedance state.

single-byte program

The single-byte program initiates with $\overline{W}$ low and $\overline{G}$ high applied to a selected device. The addresses on the address pins will be latched on the falling edge of $\overline{E}$ or $\overline{W}$, whichever comes last. Figure 1 illustrates the single-byte programming flow.

After the latching operations are completed, the device starts automatically programming the data in the addressed location within the memory array. This internal programming operation is completed in 10 ms maximum.



NOTES: 1. Upon the three-step sequence completion, the device is latched into the programming mode. The byte is latched and the byte programming operation starts if a subsequent rising edge of $\overline{W}$ is not detected within 100 µs.
2. Similar to the page programming mode.

Figure 1. Single-Byte Programming Flowchart

automatic page program (entire array program only)

The page mode of the TMS29F010 allows the user to program 2 to 128 bytes at a time. These bytes are initially loaded in the internal device register and then automatically stored in the addressed memory locations within the memory array. The internal programming operation is completed in 10 ms maximum, regardless of the number of bytes (128 maximum) loaded. During the page loading, the page address (A5 to A14) must be the same as the initial page address whereas A0, A1, A2, A3, A4, A15, and A16 can change with the byte location. Figure 1 illustrates the automatic page programming flow.

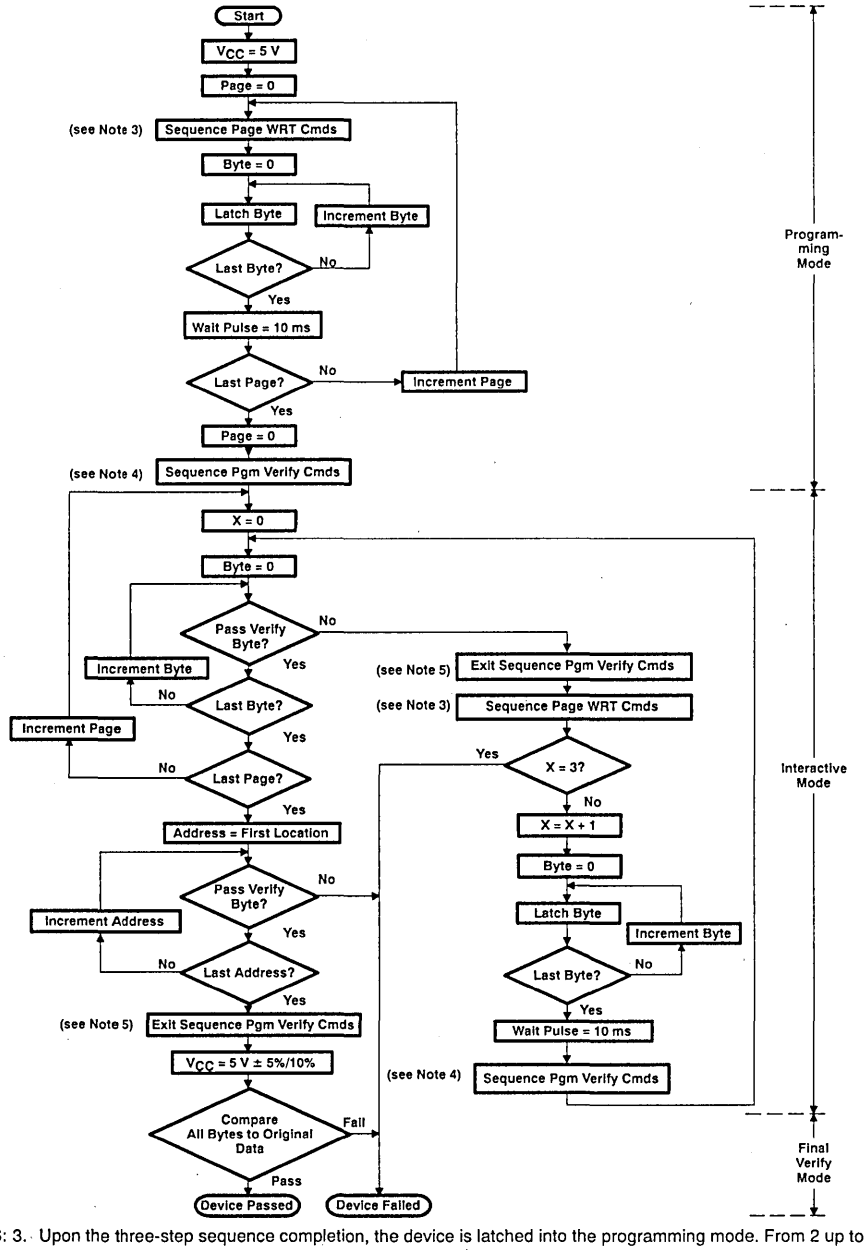
The page mode operation initiates in the same way as the single byte mode. After the first byte has been loaded, the TMS29F010 can be loaded with 1 to 127 additional bytes. Each byte load cycle starts with the falling edge of $\overline{W}$, or $\overline{E}$, whichever comes last. A successive byte must be loaded within 100 μs from the rising edge of the previous byte load cycle. If a subsequent rising edge of $\overline{W}$ is not detected within 100 μs, the internal programming operation starts automatically and subsequent attempts to load additional bytes are ignored until the operation is completed.

Note that both the single byte and the automatic page programs can be entered after a proper "dummy" sequence of bytes has been loaded (see sequence write commands).

Note that if only a single block is required to be programmed at a time, then the page mode allows the user to program 2 to 32 bytes in a specified block. During the page loading, the page address (A5 to A16) must be the same as the initial page address whereas A0, A1, A2, A3, and A4 can change with the byte location. Figure 2 illustrates the automatic page programming flow within a block.

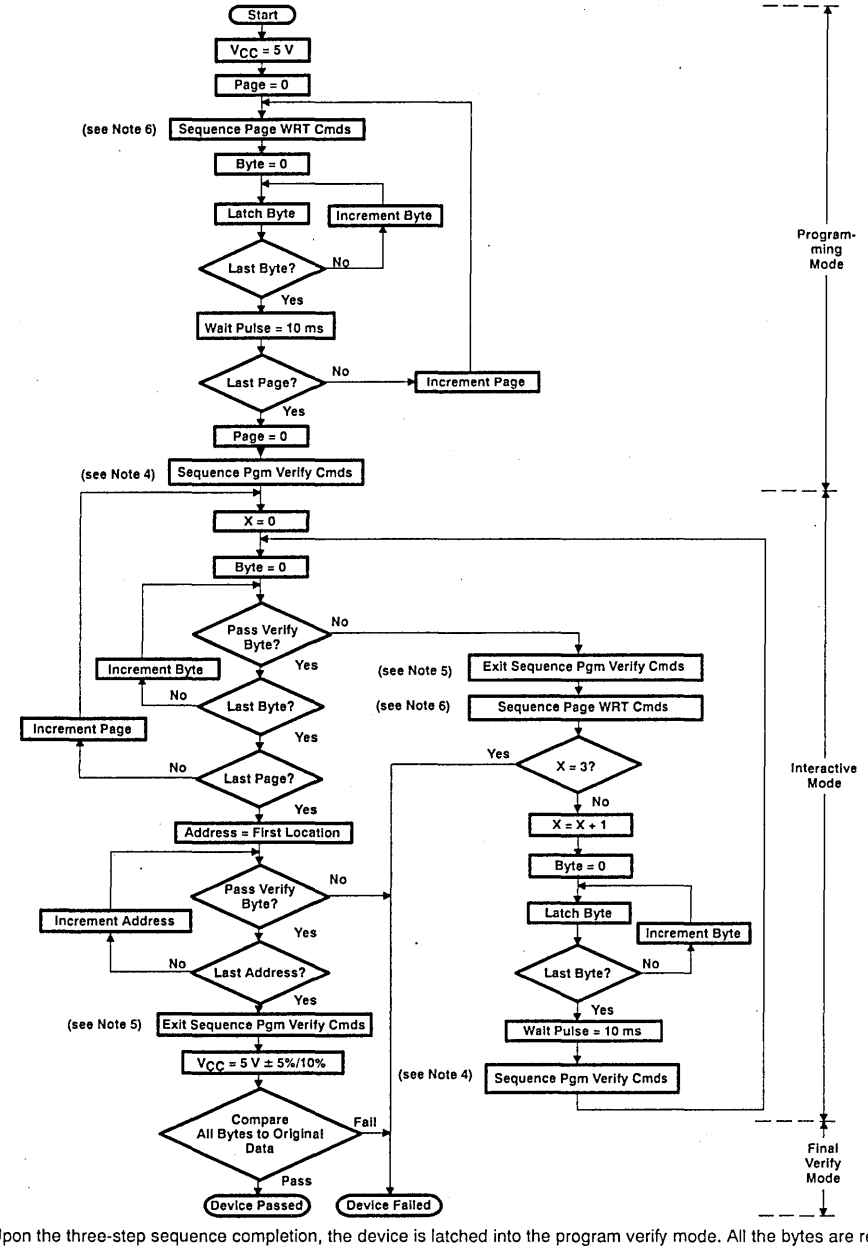
NOTE: The whole memory array is divided in 4 blocks that are identified with addresses A15 and A16. The logic table is as follows:

Block Name	A15	A16
Top left	0	0
Top right	0	1
Bottom left	1	0
Bottom right	1	1



NOTES: 3. Upon the three-step sequence completion, the device is latched into the programming mode. From 2 up to 32 bytes are latched at a rate of 1 μs up to 100 μs per byte. There are 1024 pages.
4. Upon the three-step sequence completion, the device is latched into the program verify mode. All the bytes are read with a sense voltage of: (internal V_{sense} volt) + (program margin voltage).
5. Upon the three-step sequence completion, the device exits the program verify mode and returns to the page write setup.

Figure 2. Page Programming Flowchart — Block Memory Algorithm



NOTES: 4. Upon the three-step sequence completion, the device is latched into the program verify mode. All the bytes are read with a sense voltage of: (internal V_{sense} volt) + (program margin voltage).
5. Upon the three-step sequence completion, the device exits the program verify mode and returns to the page write setup.
6. Upon the three-step sequence completion, the device is latched into the programming mode. From 2 up to 128 bytes are latched at a rate of 1 μs up to 100 μs per byte.There are 1024 pages.

Figure 3. Page Programming Flowchart — Entire Memory Algorithm

data polling

During a programming operation, the data polling software function is enabled to notify the host microcomputer that the memory is busy with programming and ignores any command until the programming operation is completed. If an attempt to read the last loaded byte occurs during the programming cycle, the device answers with the inverted logic value of DQ7. (See data polling diagram.)

flash-erase mode

The flash-erase operation can be activated via software by loading a dummy sequence of data/address strings. The timing characteristics of this sequence are the same as those used for the page mode. The device detects this particular sequence and automatically starts the self-timed erase. If the sequence is different from that specified (see table below) or the sequence load cycle is longer than 100 μs, the device ignores it. This sequence should not be used in the actual software program to prevent inadvertent flash-erase operations.

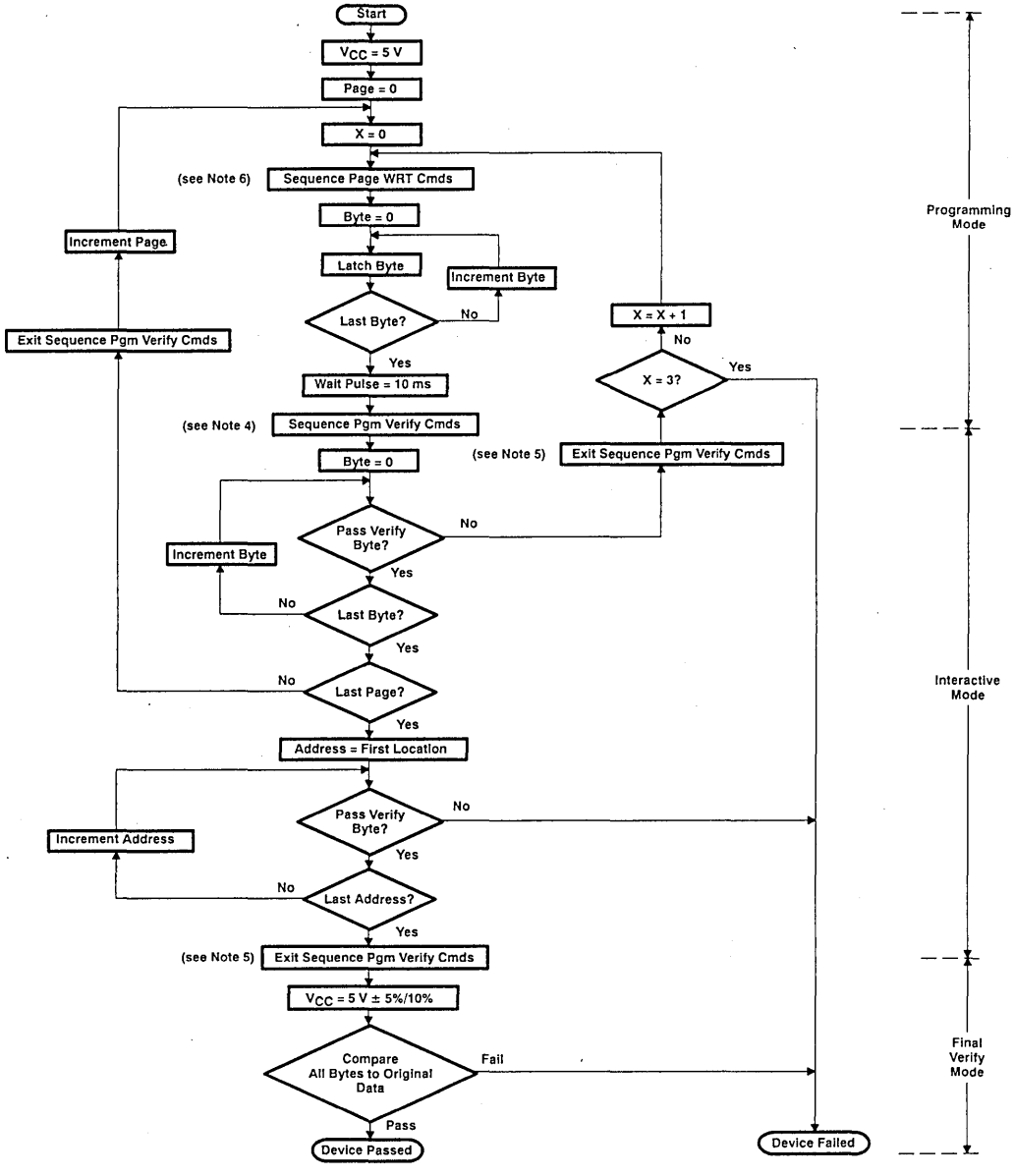
The specified dummy sequence to initiate the flash-erase mode is:

Step	Mode	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	80
4	Access Write	5555	AA
5	Access Write	2AAA	55
6	Access Write	5555	10

block-erase mode

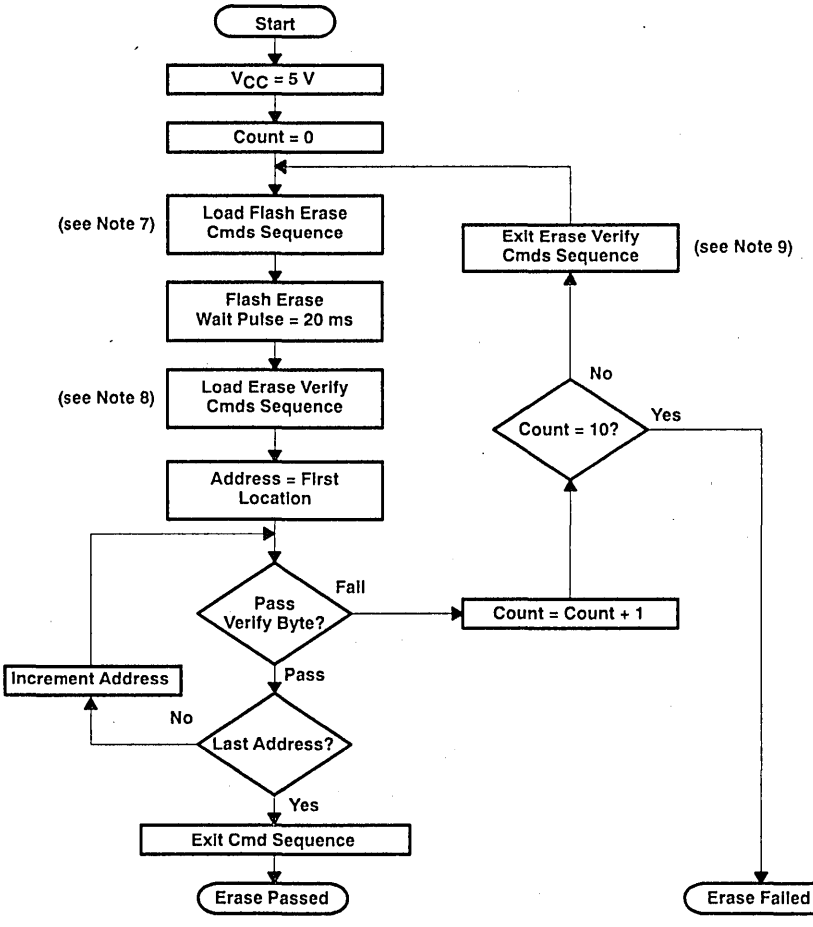
Each of the four 32K-byte blocks can be activated via software by loading a dummy sequence of data/address strings. The timing characteristics of this sequence are the same as those used for the page mode. The device detects this particular sequence and automatically starts the self-timed erase. If the sequence is different from that specified (see the table below) or the sequence load cycle is longer than 100 μs, the device ignores it. This sequence should not be used in the actual software program to prevent inadvertent flash-erase operations.

Step	Mode	A14-A0	Top Left DQ7-DQ0	Top Right DQ7-DQ0	Bottom Left DQ7-DQ0	Bottom Right DQ7-DQ0
1	Access Write	5555	AA	AA	AA	AA
2	Access Write	2AAA	55	55	55	55
3	Access Write	5555	80	80	80	80
4	Access Write	5555	AA	AA	AA	AA
5	Access Write	2AAA	55	55	55	55
6	Access Write	5555	13	15	16	19



NOTES: 4. Upon the three-step sequence completion, the device is latched into the program verify mode. All the bytes are read with a sense voltage of: (internal V_{sense} volt) + (program margin voltage).
5. Upon the three-step sequence completion, the device exits the program verify mode and returns to the page write setup.
6. Upon the three-step sequence completion, the device is latched into the programming mode. From 2 up to 128 bytes are latched at a rate of 1 μs up to 100 μs per byte.There are 1024 pages.

Figure 4. Page Programming Flowchart — Standard Algorithm



NOTES: 7. The bulk-erase operation starts automatically once the six-step sequence is completed. If any block-erase is selected, the specified dummy sequences need to be accessed. (see Page 7-102)
8. The device is latched into the Erase Verify mode once the three-step sequence is completed. All bytes are read with a sense voltage of: (internal V_{sense} voltage) — (erase margin voltage).
9. Upon the three-step sequence completion, the device is de-latched and returns to Flash operating setup.

Figure 5. Flash-Erase Flowchart

signature mode

The signature mode provides access to two bytes contained in a spare row. One byte designates the manufacturer, the other byte designates the device code. The signature mode can be entered through either a hardware or a software operation.

The hardware entry mode is specified in the mode table in the description section. Setting the device in the read mode and applying V_H on pin A9 produces the manufacturer byte code at the I/O pins if A0 = V_{IL}, or the device identifier byte code if A0 = V_{IH}. The information provided by these two bytes helps the programmer select the proper programming algorithm.

The signature mode software entry sequence is specified as follows:

Step	Mode	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	90

exit mode

The software exit sequence for any mode is specified as follows:

Step	Mode	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	F0

program verify mode

The program verify mode allows the programmer to verify the adequacy of the programming.

Step	Mode	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	B0

Upon completion of the three-step sequence, the device is latched into the program verify mode. All the bytes are read with a sense voltage of:

(internal V_{sense} voltage) + (program margin voltage)

The three access write (steps 1-3) are used only to enable the program verify mode: no data will actually be written to the device.

The software exit sequence must be applied to exit this program verify mode.

erase verify mode

The erase verify mode allows the programmer to verify the extent of erasure.

The device provides the following software sequence to access the erase verify mode:

Step	Mode	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	D0

Upon completion of the three-step sequence, the device is latched into erase verify mode. All the bytes are read with a sense voltage of:

(internal V_{sense} voltage) – (erase margin voltage)

The software exit sequence must be applied to exit this program verify mode.

sequence write commends

The device is protected against write commands during power-up and powerdown. The protection is released only if V_{CC} is higher than 3 V. Moreover, the device provides a hardware and a software protection against inadvertent write commands that may occur even with a stable V_{CC}.

The hardware protection consists of *noise immunity* to a pulse on $\overline{W}$ shorter than 20 ns, which is unable to start a program cycle, and of a logic inhibit that prevents starting the program cycle unless the conditions of $\overline{W}$ low, $\overline{E}$ low, and $\overline{G}$ high are satisfied simultaneously.

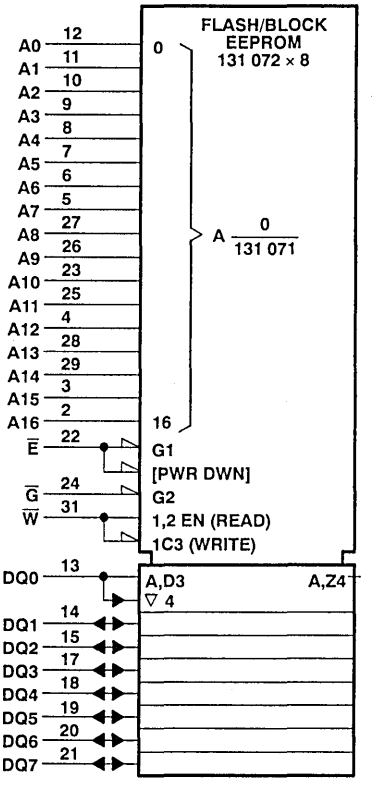
The software protection is such that no program operation is enabled unless preceded by a sequence of three "dummy" write operations. Should the specified sequence not be loaded before any program operation or the sequence load cycle is longer than 100 μs, the device ignores the program commands.

The inadvertent write protection software sequence is specified as follows:

Step	Mode	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	A0
4	Page Program	page address + 1st byte address up to the last (see automatic page program on page 7-99)	1st data up to the last byte

After step three is completed, the data polling operation can be used.

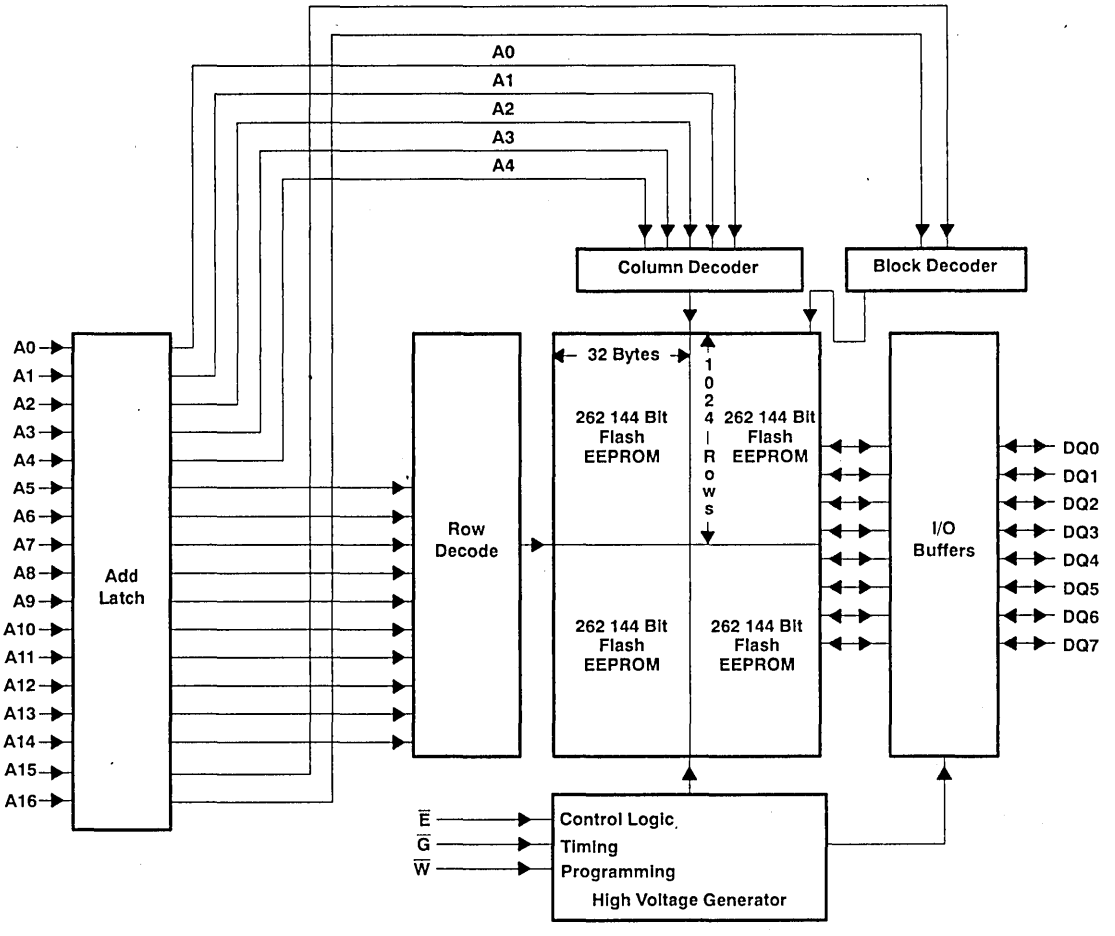
logic symbol†



† This symbol is in accordance with ANSI/EEE Std 91-1984 and IEC Publication 617-12.
J and N packages shown.

ADVANCE INFORMATION

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 10)	– 0.6 V to 7 V
Input voltage range: All except A9	– 0.6 V to 6.5 V
A9	– 0.6 V to 15 V
Output voltage (see Note 10)	– 0.6 V to V_{CC} + 0.6 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	– 65°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 10: Under absolute maximum ratings, voltage values are with respect to the most negative supply voltage V_{SS} (substrate).

recommended operating conditions

			'29F010-100 '29F010-120 '29F010-150 '29F010-200		'29F010-12 '29F010-15 '29F010-20		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.75	5.25	4.5	5.5	V
V_{IH}	High-level input voltage	TTL	2	$V_{CC}+1$	2	$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$	$V_{CC}+0.2$	$V_{CC}-0.2$	$V_{CC}+0.2$	
V_{IL}	Low-level input voltage	TTL	−0.5	0.8	−0.5	0.8	V
		CMOS	GND − 0.2	GND+0.2	GND − 0.2	GND+0.2	
T_A	Operating free-air temperature	'29F010-_ _ JL and JL4 '29F010-_ _ NL and NL4 '29F010-_ _ FML and FML4	0	70	0	70	°C
T_A	Operating free-air temperature	'29F010-_ _ JE and JE4	−40	105	−40	105	°C
T_A	Operating free-air temperature	'29F010-_ _ JQ and JQ4	−40	125	−40	125	°C

electrical characteristics over full range of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)	All except A9	V_I = 0 to 5.5 V			±1	μA
		A9	V_I = 0 to 15 V			±50	
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±10	μA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		1	1.5	mA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		0.5	1	
I_{CC2}	V_{CC} average supply current (active read)		t_{cycle} = minimum cycle time, outputs open			15	mA
I_{CC3}	V_{CC} average supply current (active write)		t_{cycle} = 10 ms			10	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		6	10	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz		10	14	pF

† Capacitance measurements are made on sample basis only.
‡ Typical values are at T_A = 25° and nominal voltages.

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

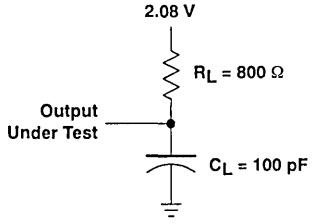
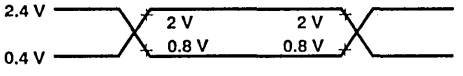


Figure 5. Output Load Circuit

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low on both inputs and outputs. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and V_{SS} as close as possible to the device pins.

switching characteristics over full ranges of recommended operating conditions†

PARAMETER		TEST CONDITIONS	'29F010-100		'29F010-120 '29F010-12		'29F010-150 '29F010-15		'29F010-200 '29F010-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF 1 Series 74 TTL Load Input $t_r \le$ 20 ns Input $t_f \le$ 20 ns		100		120		150		200	ns
$t_{a(E)}$	Access time from chip enable			100		120		150		200	ns
$t_{dp(E)}$	Access time from chip enable in data polling			75		85		100		120	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		85		100		120	ns
$t_{c(R)}$	Read cycle time		100		120		150		200		ns
$t_{d(E)}$	Delay time, chip enable low to output		0		0		0		0		ns
$t_{d(G)}$	Delay time, output enable low to output		0		0		0		0		ns
$t_{h(E)}$	Hold time, chip enable to HI-Z output		0	40	0	50	0	60	0	70	ns
$t_{h(G)}$	Hold time, output enable to HI-Z output		0	40	0	50	0	60	0	70	ns
$t_{h(D)}$	Hold time, data valid from address, $\overline{E}$, or $\overline{G}$		0		0		0		0		ns

† These parameters are guaranteed in regular read mode only.

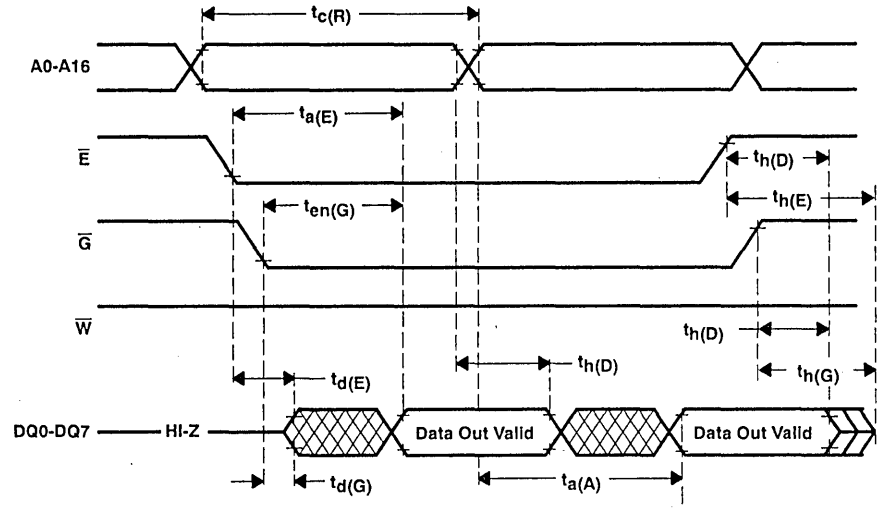
ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature

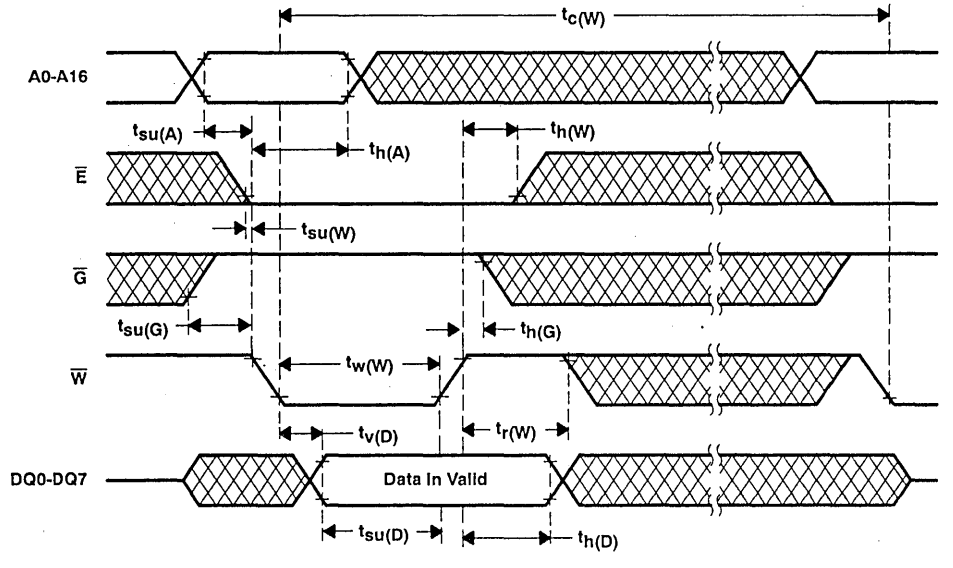
		MIN	MAX	UNIT
$t_{c(W)}$	Write cycle time		10	ms
$t_{c(W)B}$	Byte load cycle time	1	100	µs
$t_{su(A)}$	Address setup time	10		ns
$t_{su(W)}$	Write setup time	0		ns
$t_{su(D)}$	Data setup time	80		ns
$t_{su(G)}$	Output enable setup time	10		ns
$t_{h(A)}$	Address hold time	150		ns
$t_{h(W)}$	Write hold time	0		ns
$t_{h(G)}$	Output enable hold time	10		ns
$t_{h(D)}$	Data hold time	10		ns
$t_{w(W)}$	Write pulse duration	200		ns
$t_{r(W)}$	Write high recovery time	800		ns
$t_{rec(W)}$	Write high recovery time in page mode	800		ns
$t_{r(E)}$	Chip enable high recovery time	800		ns
$t_{v(D)}$	Data valid time		300	ns
$t_{w(E)}$	Chip enable pulse duration	200		ns
$t_{c(E)}$	Flash erase cycle time		20	ms

ADVANCE INFORMATION

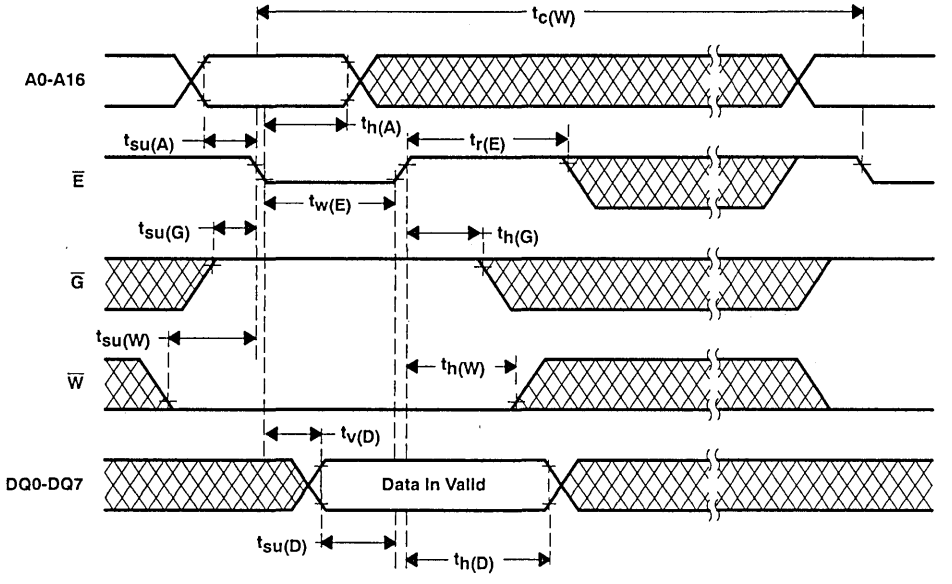
read cycle



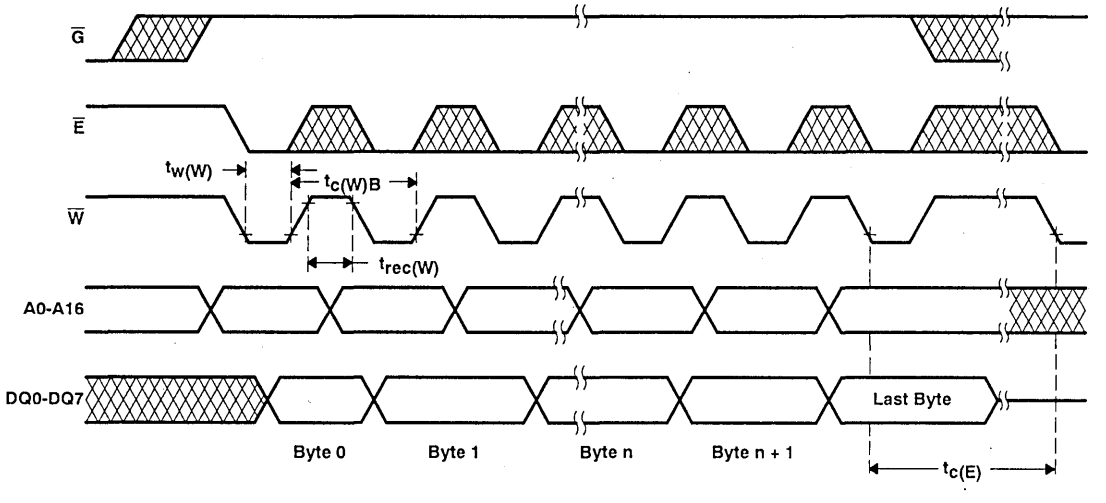
$\overline{W}$ controlled write cycle



$\overline{E}$ controlled write cycle

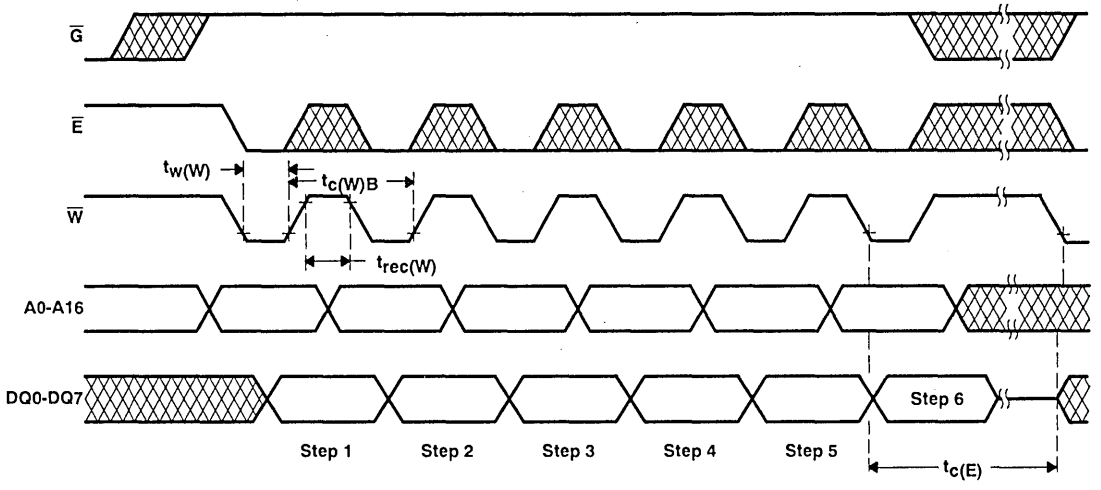


page write cycle

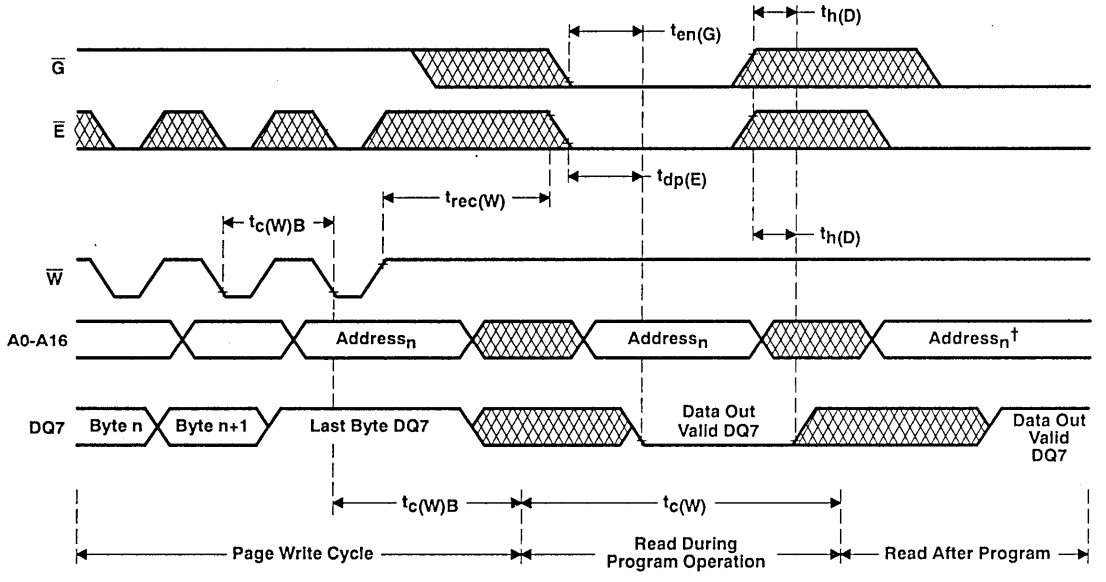


ADVANCE INFORMATION

flash erase cycle



data polling

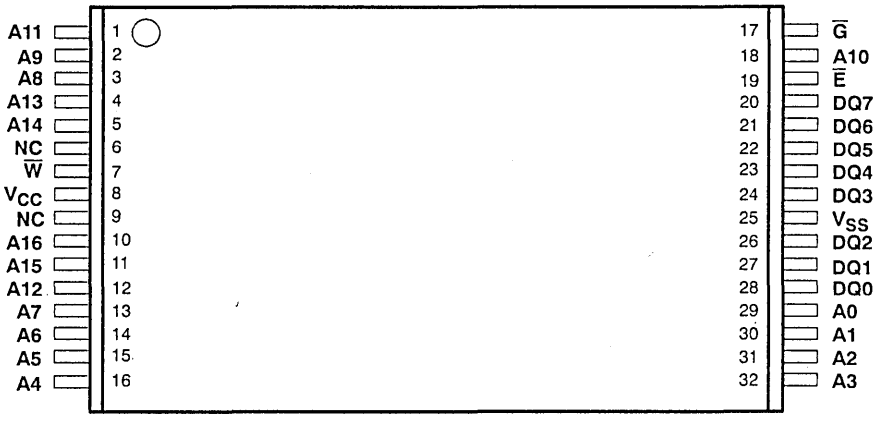


† Same address

ADVANCE INFORMATION

The following 32-pin Thin Small-Outline Package (TSOP) is under developement by Texas Instruments for the TMS29F010. Please see *Chapter 14, Mechanical Data* for complete package specifications.

DD Package†
Top View



† The package shown is for pinout reference only.

ADVANCE INFORMATION

TMS27C210A 1 048 576-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC210A 1 048 576-BIT PROGRAMMABLE READ-ONLY MEMORY

SMLS310 — NOVEMBER 1990

ADVANCE INFORMATION

- Wide-Word Organization . . . 64K × 16
- Single 5-V Power Supply
- Operationally Compatible With Existing Megabit EPROMs
- 40-Pin Dual-In-Line Package and 44-Lead Plastic Leaded Chip Carrier
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

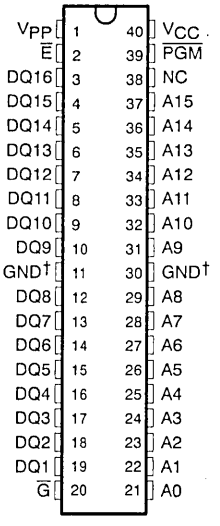
V_{CC} ± 5%	V_{CC} ± 10%	
'27C210A-120	'27C210A-12	120 ns
'27PC210A-120	'27PC210A-12	120 ns
'27C210A-150	'27C210A-15	150 ns
'27PC210A-150	'27PC210A-15	150 ns
'27C210A-200	'27C210A-20	200 ns
'27PC210A-200	'27PC210A-20	200 ns
'27C210A-250	'27C210A-25	250 ns
'27PC210A-250	'27PC210A-25	250 ns

- 16-Bit Output For Use in Microprocessor-Based Systems
- Very High-Speed SNAP! Pulse Programming
- Power-Saving CMOS Technology
- 3-State Output Buffers
- 400-mV Minimum DC Noise Immunity With Standard TTL Loads
- Latchup Immunity of 250 mA on All Input and Output Pins
- No Pullup Resistors Required
- Low Power Dissipation
  - —Active . . . 165 mW Worst Case
  - —Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)
- PEP4 Version Available With 168 Hour Burn-In and Choices of Operating Temperature Ranges

description

The TMS27C210A series are 1 048 576-bit, ultraviolet-light erasable, electrically programmable read-only memories.

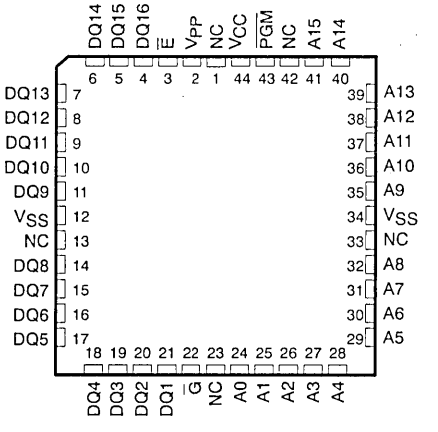
J Package
(Top View)



PIN NOMENCLATURE	
A0-A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
DQ1-DQ16	Inputs (programming)/Outputs
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply‡

† Pins 11 and 30 must be connected externally to ground.
‡ Only in program mode.

FN Package
(Top View)



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

The TMS27PC210A series are 1 048 576-bit, one-time, electrically programmable read-only memories.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS27C210A EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C210A is also offered with two guaranteed temperature ranges of 0°C to 70°C and – 40°C to 85°C (TMS27C210A-_ _JL and TMS27C210A-_ _JE, respectively). The TMS27C210A is also offered with 168 hour burn-in on both temperature ranges (TMS27C210A-_ _JL4and TMS27C210A-_ _JE4, respectively). (See table below).

The TMS27PC210A OTP PROM is offered in a 44-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FN suffix). The TMS27PC210A is offered with a temperature range of 0°C to 70°C.

EPROM AND OTP PROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HOUR BURN-IN VS TEMPERATURE RANGES	
	0°C to 70°C	– 40°C to 85°C	0°C to 70°C	– 40°C to 85°C
TMS27C210A-xxx	JL	JE	JL4	JE4
TMS27PC210A-xxx	FNL			

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor based systems. One other (13 V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

There are seven modes of operation for the TMS27C210A and TMS27PC210A which are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V) and 12 V on A9 for signature mode.

FUNCTION	MODE							
	READ	Output Disable	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	X	X	X	V_{IL}	V_{IH}	X	X	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ1-DQ16	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	AB

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C210As or TMS27PC210As are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C210A and TMS27PC210A is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family"*, available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 μA for a high TTL input on $\overline{E}$ and to 100 μA for a high CMOS input on $\overline{E}$. In this mode all outputs are in the high impedance state.

erasure (TMS27C210A)

Before programming, the TMS27C210A is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W•s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C210A the window should be covered with an opaque label.

initializing (TMS27PC210A)

The one-time programmable TMS27PC210A PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C210A and TMS27PC210A are programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which can program in a nominal time of seven seconds. Actual programming time will vary as a function of the programmer used.

The SNAP! Pulse programming algorithm uses an initial pulse of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}. Data is presented in parallel (sixteen bits) on pins DQ1 through DQ16. Once addresses and data are stable, $\overline{PGM}$ is pulsed low.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V ± 10%.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pins.

program verify

Programmed bits may be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V. Two identifier bytes are accessed by toggling A0. DQ1-DQ8 contain the valid codes. All other addresses must be held low. The signature code for these devices is 97AB. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code AB (Hex), as shown by the signature mode table below.

signature mode†

IDENTIFIER†	PINS									
	A0	DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	1	0	1	0	1	0	1	1	AB

† $\overline{E} = \overline{G} = V_{IL}$, A9 = V_H, A1-A8 = V_{IL}, A10-A15 = V_{IL}, $V_{PP} = V_{CC}$, $\overline{PGM} = V_{IH}$ or V_{IL}.

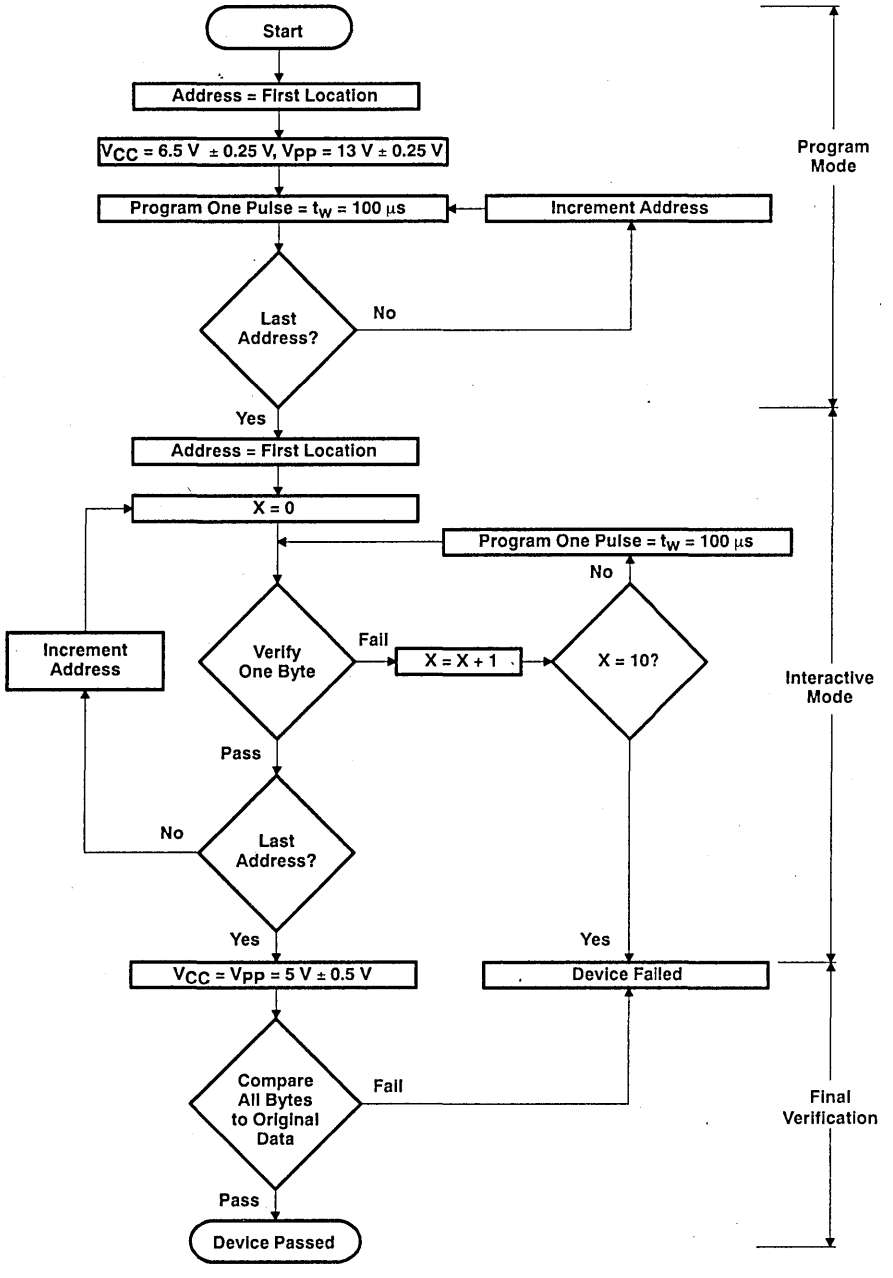
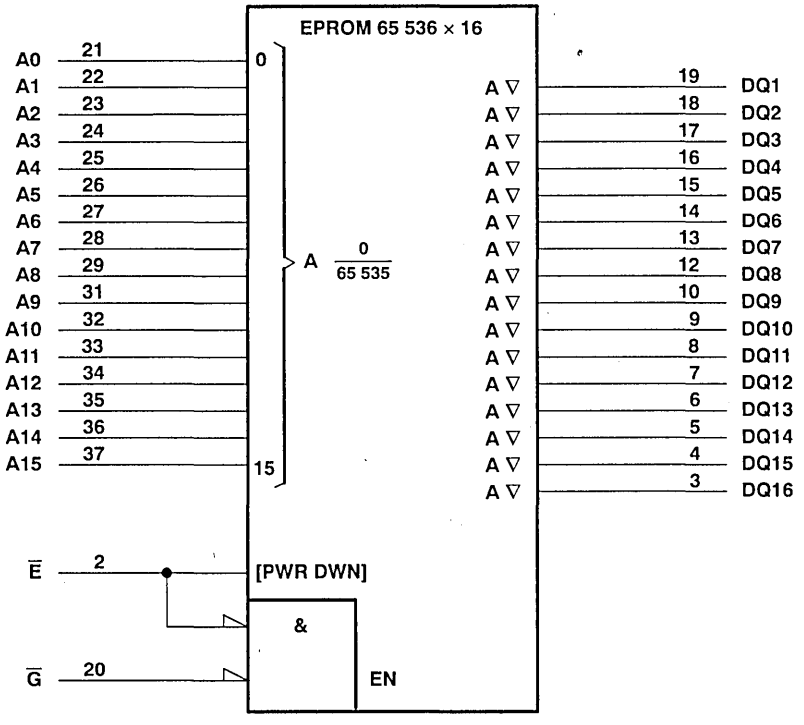


Figure 1. SNAP! Pulse Programming Flowchart

ADVANCE INFORMATION

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91–1984 and IEC Publication 617–12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} ..... – 0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 ..... – 0.6 V to V_{CC} + 1 V
A9 ..... – 0.6 V to 13.5 V
Output voltage range (see Note 1) ..... – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C210A-_ _JL and JL4, '27PC210A-_ _FNL) ..... 0° C to 70°C
Operating free-air temperature range ('27C210A-_ _JE and JE4) ..... – 40° C to 85°C
Storage temperature range ..... – 65°C to 150°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			TMS27C/PC210A-120, TMS27C/PC210A-150, TMS27C/PC210A-200, TMS27C/PC210A-250			TMS27C/PC210A-12, TMS27C/PC210A-15, TMS27C/PC210A-20, TMS27C/PC210A-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.75	5	5.25	4.5	5	5.5	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode (see Note 3)	V_{CC} –0.6	V_{CC}	V_{CC}+0.6	V_{CC}– 0.6	V_{CC}	V_{CC}+0.6	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	12.75	13	13.25	
V_{IH}	High-level input voltage	TTL	2		V_{CC}+0.5	2		V_{CC}+0.5	V
		CMOS	V_{CC} – 0.2		V_{CC}+0.5	V_{CC} – 0.2		V_{CC}+0.5	
V_{IL}	Low-level input voltage	TTL	– 0.5		0.8	– 0.5		0.8	V
		CMOS	– 0.5		GND+0.2	– 0.5		GND+0.2	
T_A	Operating free-air temperature	'27C210A-_ _JL, JL4 '27PC210A-_ _FNL	0		70	0		70	°C
T_A	Operating free-air temperature	'27C210A-_ _JE, JE4	– 40		85	– 40		85	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 20 μA	V_{CC} – 0.2		V
			I_{OH} = – 2 mA	2.4		
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA		0.4	V
			I_{OL} = 20 μA		0.1	
I_I	Input current (leakage)		V_I = 0 to 5.5 V		±1	μA
I_O	Output current (leakage)		V_O = 0 to V_{CC}		±1	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		10	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open†		30	mA

† Minimum cycle time = maximum address access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		8	12	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz		12	15	pF

‡ Capacitance measurements are made on a sample basis only.

§ Typical values are at T_A = 25°C and nominal voltages.

ADVANCE INFORMATION

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 & 5)	'27C210A-120 '27PC210A-120 '27C210A-12 '27PC210A-12		'27C210A-150 '27PC210A-150 '27C210A-15 '27PC210A-15		'27C210A-200 '27PC210A-200 '27C210A-20 '27PC210A-20		'27C210A-250 '27PC210A-250 '27C210A-25 '27PC210A-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \leq$ 20 ns, Input $t_f \leq$ 20 ns		120		150		200		250	ns
$t_{a(E)}$	Access time from chip enable			120		150		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	50	0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		0		ns

† Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)

5. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 4)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low). (reference AC Testing Wave Form)

ADVANCE INFORMATION

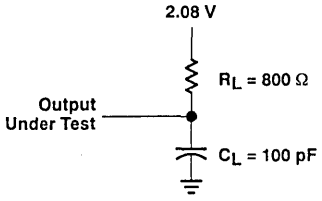
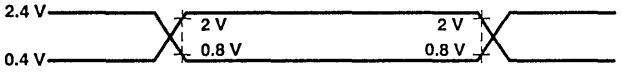


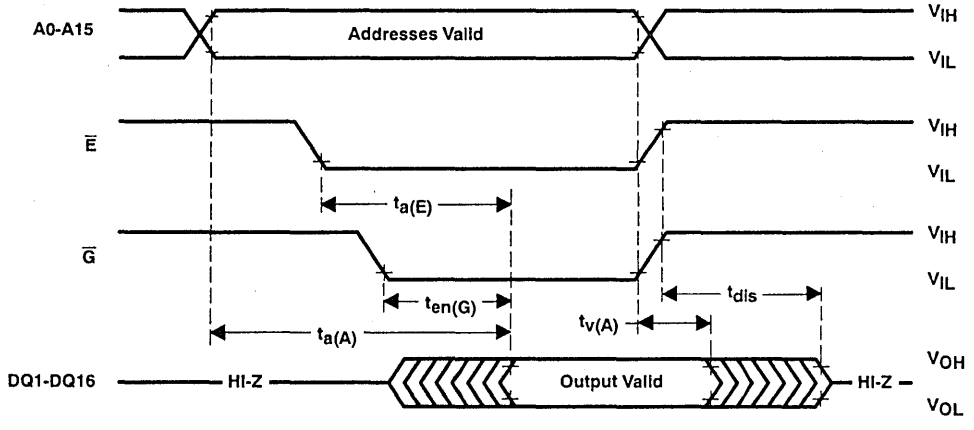
Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



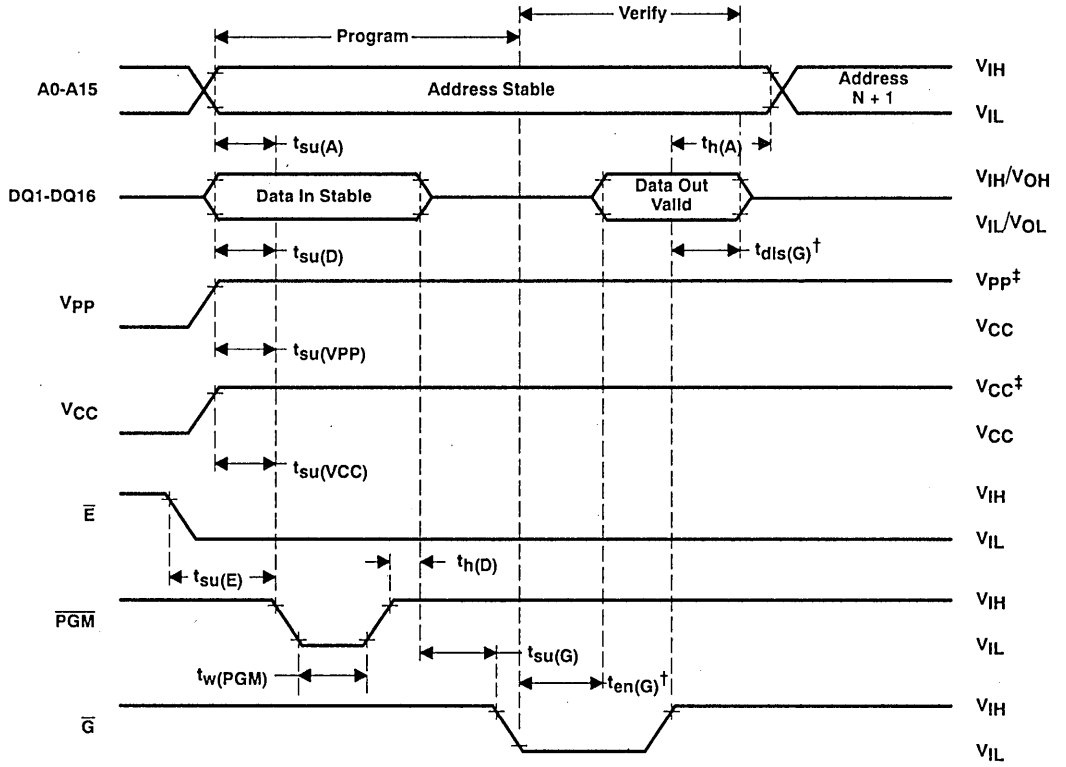
A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

read cycle timing



ADVANCE INFORMATION

program cycle timing (SNAP! Pulse programming)



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accomodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

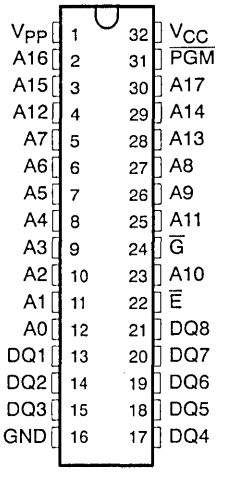
ADVANCE INFORMATION

- Organization . . . 256K × 8
- Single 5-V Power Supply
- Operationally Compatible With Existing Megabit EPROMs
- Industry Standard 32-Pin Dual-In-line Package
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

V_{CC} ± 5%	V_{CC} ± 10%	
'27C020-100		100 ns
'27C020-120	'27C020-12	120 ns
'27C020-150	'27C020-15	150 ns
'27C020-200	'27C020-20	200 ns
'27C020-250	'27C020-25	250 ns

- 8-Bit Output For Use in Microprocessor-Based Systems
- Very High-Speed SNAP! Pulse Programming
- Power Saving CMOS Technology
- 3-State Output Buffers
- 400 mV Minimum DC Noise Immunity With Standard TTL Loads
- Latchup Immunity of 250 mA on All Input and Output Pins
- No Pullup Resistors Required
- Low Power Dissipation (V_{CC} = 5.5 V)
  - — Active . . . 165 mW Worst Case
  - — Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)

J Package
(Top View)



PIN NOMENCLATURE	
A0-A17	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
$\overline{PGM}$	Program
DQ1-DQ8	Inputs (programming)/Outputs
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply†

† Only in program mode.

- PEP4 Version Available With 168 Hour Burn-In, and Choices of Operating Temperature Ranges

ADVANCE INFORMATION

description

The TMS27C020 series are 2 097 152-bit, ultraviolet-light erasable, electrically programmable read-only memories.

This device is fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pullup resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS27C020 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C020 is also offered with two choices of temperature ranges of 0° to 70°C and – 40°C to 85°C (TMS27C020-__JL and TMS27C020-__JE, respectively). The TMS27C020 is also offered with 168 hour burn-in on both temperature ranges (TMS27C020-__JL4 and TMS27C020-__JE4, respectively). (See table on next page).

EPROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS. TEMPERATURE RANGES	
	0°C to 70°C	– 40°C to 85°C	0°C to 70°C	– 40°C to 85°C
TMS27C020-XXX	JL	JE	JL4	JE4

These EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (13 V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

There are seven modes of operation for the TMS27C020, which are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V) and V_H (12 V) on A9 for signature mode.

FUNCTION	MODE							
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	X	X	X	V_{IL}	V_{IH}	X	X	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ1-DQ8	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	32

† X can be V_{IL} or V_{IH}
‡ V_H = 12 V ± 0.5 V

read/output disable

When the outputs of two or more TMS27C020s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C020 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family"*, available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 μA for a high TTL input on $\overline{E}$ and to 100 μA for a high CMOS input on $\overline{E}$. In this mode all outputs are in the high impedance state.

erasure

Before programming, the TMS27C020 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C020, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

SNAP! Pulse programming

The TMS27C020 is programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1 which programs in a nominal time of twenty-six seconds. Actual programming time will vary as a function of the programmer used.

The SNAP! Pulse programming algorithm uses an initial pulse of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}. Data is presented in parallel (eight bits) on pins DQ1 through DQ8. Once addresses and data are stable, $\overline{PGM}$ is pulsed low.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V ± 10%.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pins.

program verify

Programmed bits may be verified with V_{PP} = 13 V when $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL}, and $\overline{PGM}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12 V. Two identifier bytes are accessed by toggling A0. All addresses must be held low. The signature code for the TMS27C020 is 9732. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code 32 (Hex), as shown by the signature mode table below.

IDENTIFIER†	PINS									
	A0	DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	0	0	1	1	0	0	1	0	32

† $\overline{E}$ = $\overline{G}$ = V_{IL}, A1-A8 = V_{IL}, A9 = V_H, A10-A17 = V_{IL}, V_{PP} = V_{CC}.

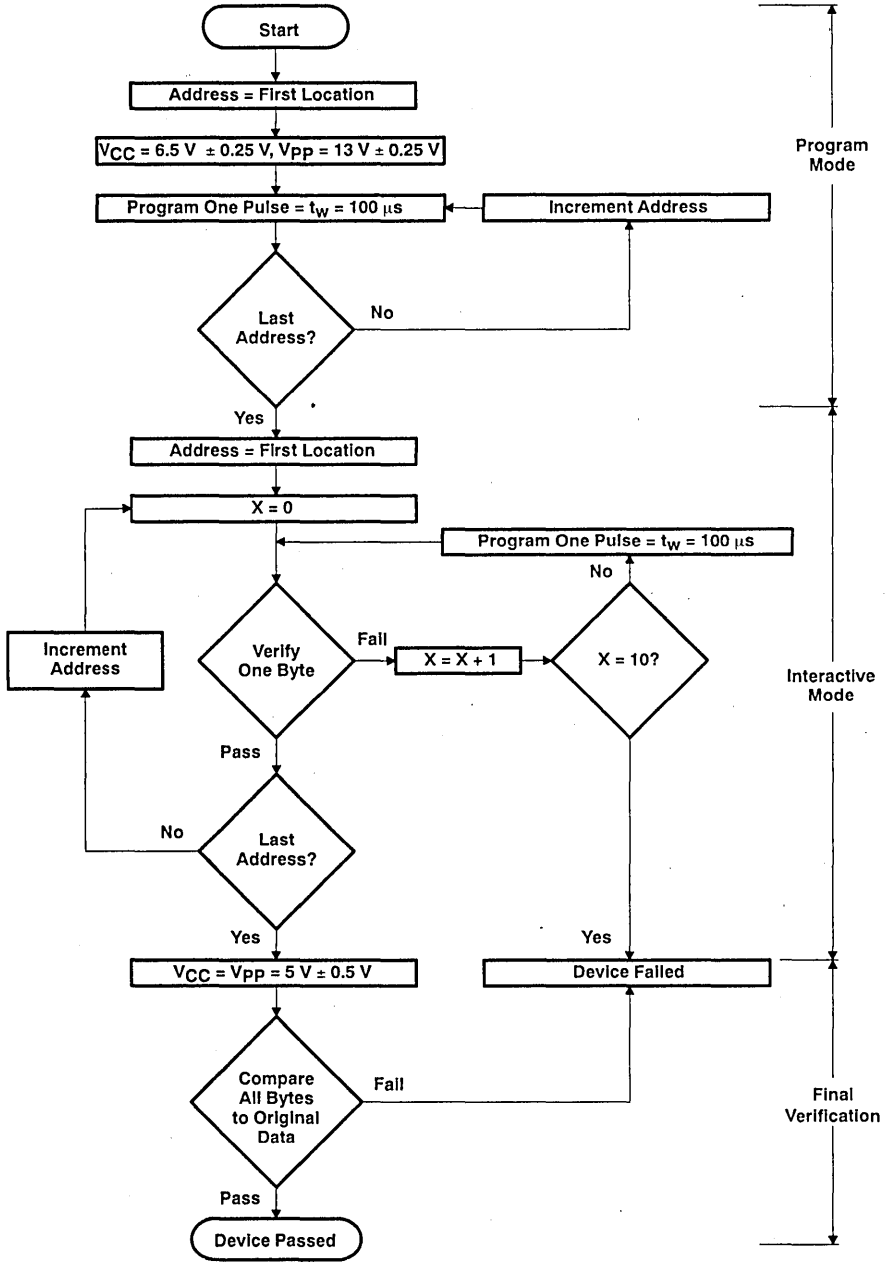
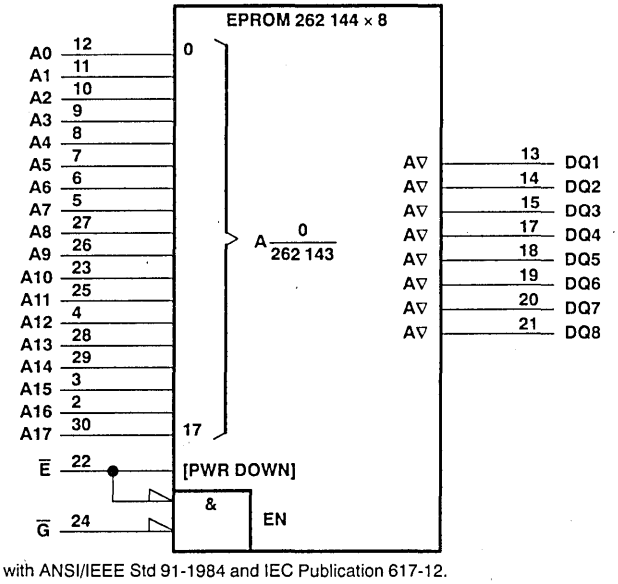


Figure 1. SNAP! Pulse Programming Flowchart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} ..... – 0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... – 0.6 V to V_{CC} + 1 V
A9 ..... – 0.6 V to 13.5 V
Output voltage range, with respect to V_{SS} (see Note 1) ..... – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C020-_ _ JL and JL4) ..... 0°C to 70°C
Operating free-air temperature range ('27C020-_ _JE and JE4) ..... – 40°C to 85°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			'27C020-100 '27C020-120 '27C020-150 '27C020-200 '27C020-250			'27C020-12 '27C020-15 '27C020-20 '27C020-25			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.75	5	5.25	4.5	5	5.5	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode (see Note 3)	V_{CC} – 0.6	V_{CC}	V_{CC} + 0.6	V_{CC} – 0.6	V_{CC}	V_{CC} + 0.6	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	12.75	13	13.25	V
V_{IH}	High-level input voltage	TTL	2		V_{CC} + 0.5	2		V_{CC} +0.5	V
		CMOS	V_{CC} – 0.2		V_{CC} + 0.5	V_{CC} – 0.2		V_{CC} + 0.5	
V_{IL}	Low-level input voltage	TTL	– 0.5		0.8	– 0.5		0.8	V
		CMOS	– 0.5		GND + 0.2	– 0.5		GND + 0.2	
T_A	Operating free-air temperature	'27C020-_ _JL, JL4	0		70	0		70	°C
T_A	Operating free-air temperature	'27C020-_ _JE, JE4	– 40		85	– 40		85	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}. During programming, V_{PP} must be maintained at 13 V ± 0.25 V.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −20 μA	V_{CC} − 0.2		V
			I_{OH} = −2 mA	2.4		
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA		0.4	V
			I_{OL} = 20 μA		0.1	
I_I	Input current (leakage)		V_I = 0 to 5.5 V		±1	μA
I_O	Output current (leakage)		V_O = 0 to V_{CC}		±1	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		10	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$\overline{E}$ = V_{IH}, V_{CC} = 5.5 V		500	μA
		CMOS-input level	$\overline{E}$ = V_{CC} ± 0.2 V, V_{CC} = 5.5 V		100	
I_{CC2}	V_{CC} supply current (active)		$\overline{E}$ = V_{IL}, V_{CC} = 5.5 V, t_{cycle} = minimum cycle time, outputs open†		30	mA

† Minimum cycle time = maximum access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		4	8	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz		6	10	pF

‡ Capacitance measurements are made on sample basis only.
§ All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 & 5)	'27C020-100		'27C020-120 '27C020-12		'27C020-150 '27C020-15		'27C020-200 '27C020-20		'27C020-250 '27C020-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input t_r ≤ 20 ns, Input t_f ≤ 20 ns		100		120		150		200		250	ns
$t_{a(E)}$	Access time from chip enable			100		120		150		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		55		75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first¶		0	50	0	50	0	60	0	60	0	80	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first		0		0		0		0		0		ns

¶ Value calculated from 0.5-V delta to measured output level. This parameter is sampled and not 100% tested.

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)
5. Common test conditions apply for t_{dis} except during programming.

ADVANCE INFORMATION

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 4)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 4: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic logic low. (reference AC Testing Wave Form)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

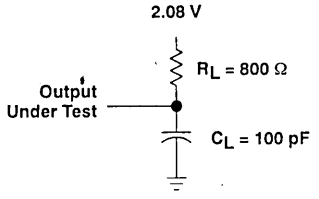
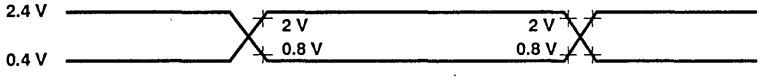


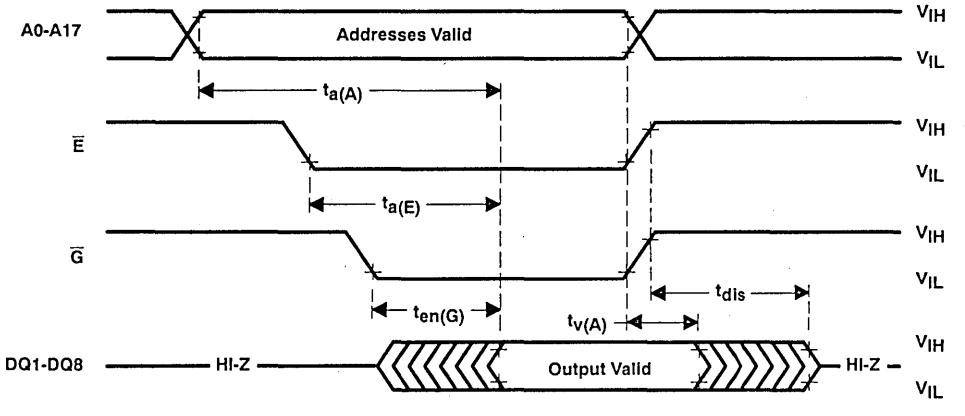
Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



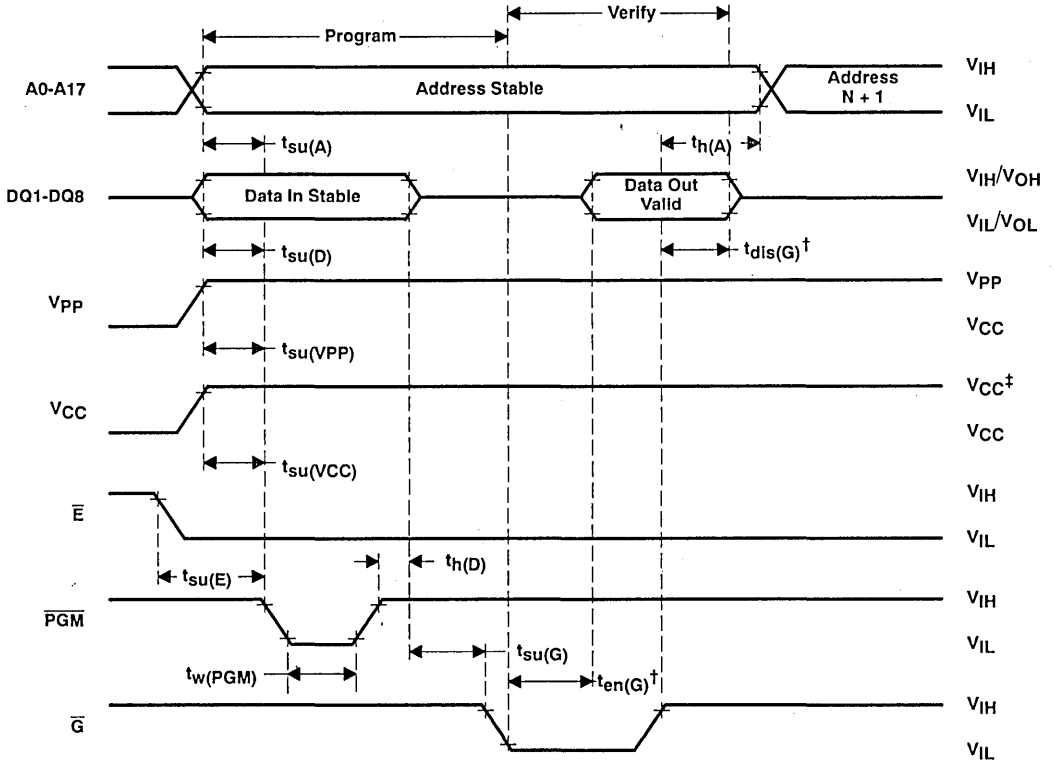
AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

read cycle timing



ADVANCE INFORMATION

program cycle timing (SNAP! Pulse programming)



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

ADVANCE INFORMATION

TMS27C040 4 194 304-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC040 4 194 304-BIT PROGRAMMABLE READ-ONLY MEMORY

SMLS040 — NOVEMBER 1990

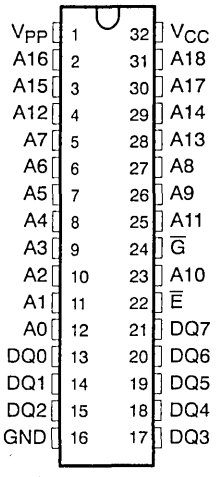
ADVANCE INFORMATION

- Organization . . . 512K × 8
- Single 5-V Power Supply
- Industry Standard 32-Pin Dual-In-line Package and 32-Lead Plastic Chip Carrier
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time

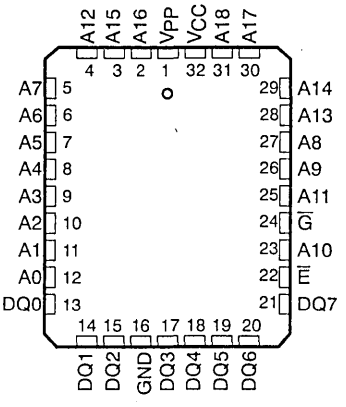
V_{CC} ± 5%	V_{CC} ± 10%	
'27C/PC040-8	'27C/PC040-80	80 ns
'27C/PC040-100	'27C/PC040-10	100 ns
'27C/PC040-120	'27C/PC040-12	120 ns
'27C/PC040-150	'27C/PC040-15	150 ns

- 8-Bit Output For Use in Microprocessor-Based Systems
- Power-Saving CMOS Technology
- 3-State Output Buffers
- 400-mV Guaranteed DC Noise Immunity With Standard TTL Loads
- Latchup Immunity of 250 mA on All Input and Output Pins
- No Pullup Resistors Required
- Low Power Dissipation (V_{CC} = 5.5 V)
  - — Active . . . 275 mW Worst Case
  - — Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)
- Choice of Two Operating Temperature Ranges

TMS27C040
J Package
(Top View)



TMS27PC040
FM Package
(Top View)



PIN NOMENCLATURE	
A0-A18	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
DQ0-DQ7	Inputs (programming)/Outputs
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply†

† Only in program mode.

description

The TMS27C040 series are 4 194 304-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC040 series are 4 194 304-bit, one-time electrically programmable read-only memories.

These devices are fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits. Each output can drive one Series 74

TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus.

The TMS27C040 is offered in a 600-mil dual-in-line cerdip package (J suffix). The TMS27C040 is offered with two choices of temperature ranges of 0°C to 70°C and −40°C to 85°C (TMS27C040-_ _JL and TMS27C040-_ _JE, respectively). The TMS27C040 is also offered with 168 hour burn-in on both temperature ranges (TMS27C040-_ _JL4 and TMS27C040-_ _JE4 respectively). (See table below.)

The TMS27PC040 is offered in a 32-lead plastic leaded chip carrier package (FM suffix). The TMS27PC040 is characterized for operation from 0°C to 70°C (TMS27PC040-_ _FML).

	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR OPERATING TEMPERATURE RANGES WITH PEP4 168 HR. BURN-IN	
	0°C TO 70°C	− 40°C TO 85°C	0°C TO 70°C	− 40°C TO 85°C
TMS27C040-XXX	JL	JE	JL4	JE4
TMS27PC040-XXX	FML			

These EPROMs and PROMS operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (13 V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

There are seven modes of operation listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V) and V_H (12 V) on A9 for signature mode.

MODE	FUNCTION						
	$\overline{E}$	$\overline{G}$	V_{PP}	V_{CC}	A9	A0	DQ0-DQ7
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	X	X	Data Out
Output Disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	X	X	HI-Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	X	X	HI-Z
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	X	Data In
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	X	X	HI-Z
Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	X	Data Out
Signature Mode	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H	V_{IL}	MFG Code 97
						V_{IH}	Device Code 50

† X can be V_{IL} or V_{IH}

‡ V_H = 12 V ± 0.5 V

read/output disable

When the outputs of two or more TMS27C040s or TMS27PC040s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C040 and TMS27PC040 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family"*, available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 50 mA to 1 mA for a high TTL input on $\overline{E}$ and to 100 μA for a high CMOS input on $\overline{E}$. In this mode all outputs are in the high impedance state.

erasure (TMS27C040)

Before programming, the TMS27C040 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet-light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2 . A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C040, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

initializing (TMS27PC040)

The one-time programmable TMS27PC040 PROM is provided with all bits in logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C040 and TMS27PC040 are programmed by using the SNAP! Pulse programming algorithm. The programming sequence is shown in the SNAP! Pulse programming flow chart (Figure 1).

The initial setup is V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IH}$. Once the initial location is selected, the data is presented in parallel (eight bits) on pins DQ0 through DQ7. Once addresses and data are stable, the programming mode is achieved when $\overline{E}$ is pulsed low (V_{IL}) with a pulse duration of $t_{w(PGM)}$. Every location is programmed only once before going to interactive mode.

In the interactive mode, the word is verified at V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IL}$. If the correct data is not read, the programming is performed by pulling $\overline{E}$ low with a pulse duration of $t_{w(PGM)}$. This sequence of verification and programming is performed up to a maximum of 10 times. When the device is fully programmed, all bytes are verified with $V_{CC} = V_{PP} = 5\ V \pm 10\%$.

program inhibit

Programming may be inhibited by maintaining high level inputs on the $\overline{E}$ and $\overline{G}$ pins.

program verify

Programmed bits may be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$, and $\overline{E} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12 V. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. The signature code for the TMS27C040 is 9750. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code 50 (Hex), as shown by the signature mode table below.

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	0	1	0	1	0	0	0	0	50

† $\overline{E} = \overline{G} = V_{IL}$, A1-A8 = V_{IL}, A9 = V_H, A10-A18 = V_{IL}, $V_{PP} = V_{CC}$.

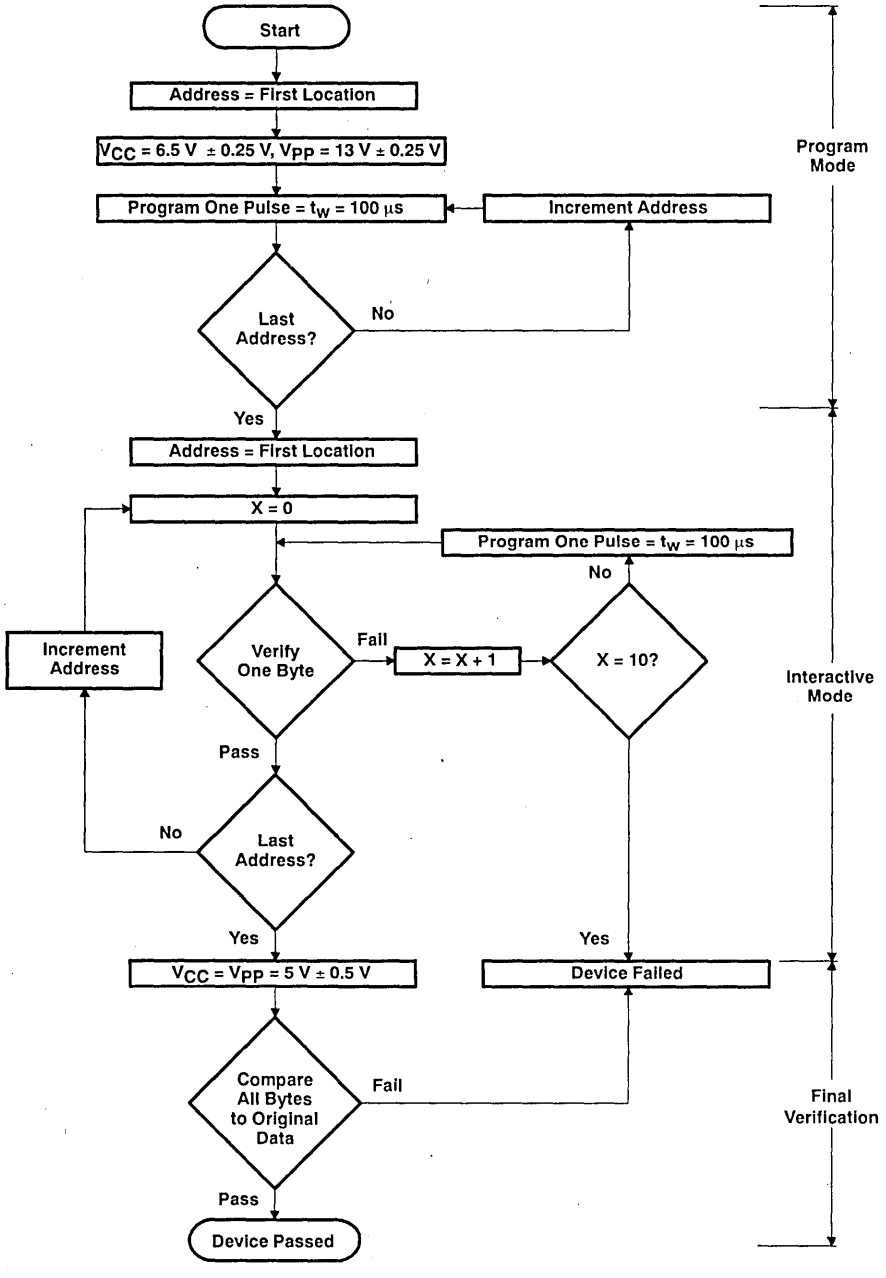
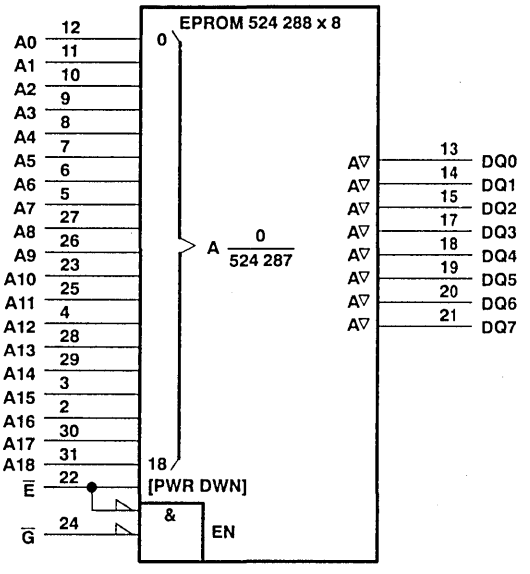


Figure 1. SNAP! Pulse Programming Flow Chart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . – 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) . . . . . – 0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 . . . . . – 0.6 V to 6.5 V
A9 . . . . . – 0.6 V to 13 V
Output voltage range, with respect to V_{SS} (see Note 1) . . . . . – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C040-_ _JL and JL4; '27PC040-_ _FML) . . . . . 0°C to 70°C
Operating free-air temperature range ('27C040-_ _JE and JE4) . . . . . – 40°C to 85°C
Storage temperature range . . . . . – 65°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			'27C/PC040-8 '27C/PC040-100 '27C/PC040-120 '27C/PC040-150			'27C/PC040-80 '27C/PC040-10 '27C/PC040-12 '27C/PC040-15			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.75	5	5.25	4.5	5	5.5	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode (see Note 3)	V_{CC} – 0.7		V_{CC}	V_{CC} – 0.7		V_{CC}	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	12.75	13	13.25	V
V_{IH}	High-level input voltage		2		V_{CC}+0.5	2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage		– 0.5		0.8	– 0.5		0.8	V
T_A	Operating free-air temperature	'27C040-_ _JL and JL4 '27PC040-_ _FML	0		70	0		70	°C
T_A	Operating free-air temperature	'27C040-_ _JE and JE4	– 40		85	– 40		85	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}. During programming, V_{PP} must be maintained at 13 V ± 0.25 V.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 400 µA	2.4		V
			I_{OH} = – 20 µA	V_{CC} – 0.1		
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA		0.4	V
			I_{OL} = 20 µA		0.1	
I_I	Input current (leakage)		V_I = 0 to 5.5 V		±1	µA
I_O	Output current (leakage)		V_O = 0 to V_{CC}		±1	µA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 12.75 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		1	mA
		CMOS-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	µA
I_{CC2}	V_{CC} supply current (active)		$\overline{E}$ = V_{IL}, V_{CC} = 5.5 V t_{cycle} = minimum cycle time, outputs open‡		50	mA

‡ Minimum cycle time = maximum access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	$V_I = 0$		4	8	pF
C_O	Output capacitance	$V_O = 0$		8	12	pF

† Capacitance measurements are made on sample basis only.
‡ All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 & 5)	'27C/PC040-8 '27C/PC040-80		'27C/PC040-100 '27C/PC040-10		'27C/PC040-120 '27C/PC040-12		'27C/PC040-150 '27C/PC040-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		80		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			80		100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		50		50		50	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first§		0	50	0	50	0	50	0	50	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first§		0		0		0		0		ns

§ Value calculated from 0.5-V delta to measured output level.

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)
5. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 4)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 4: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic logic low. (reference AC Testing Wave Form)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

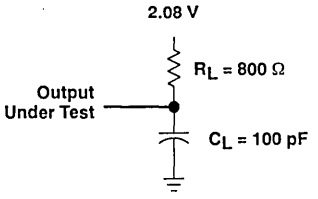
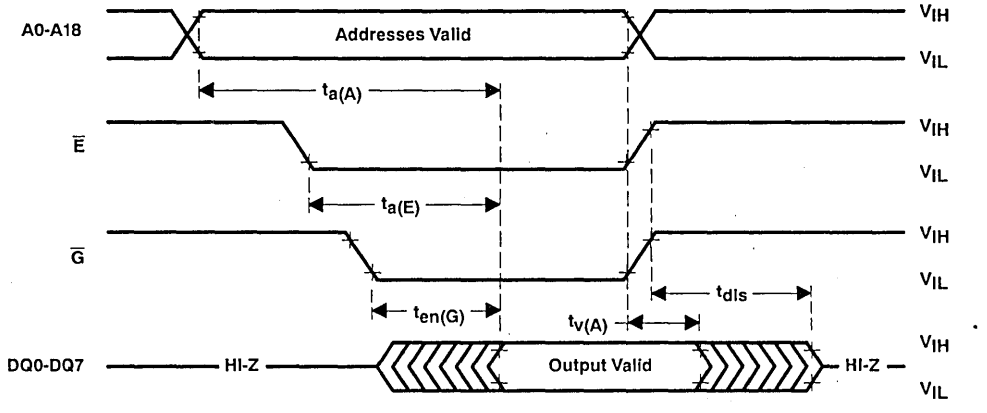


Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms

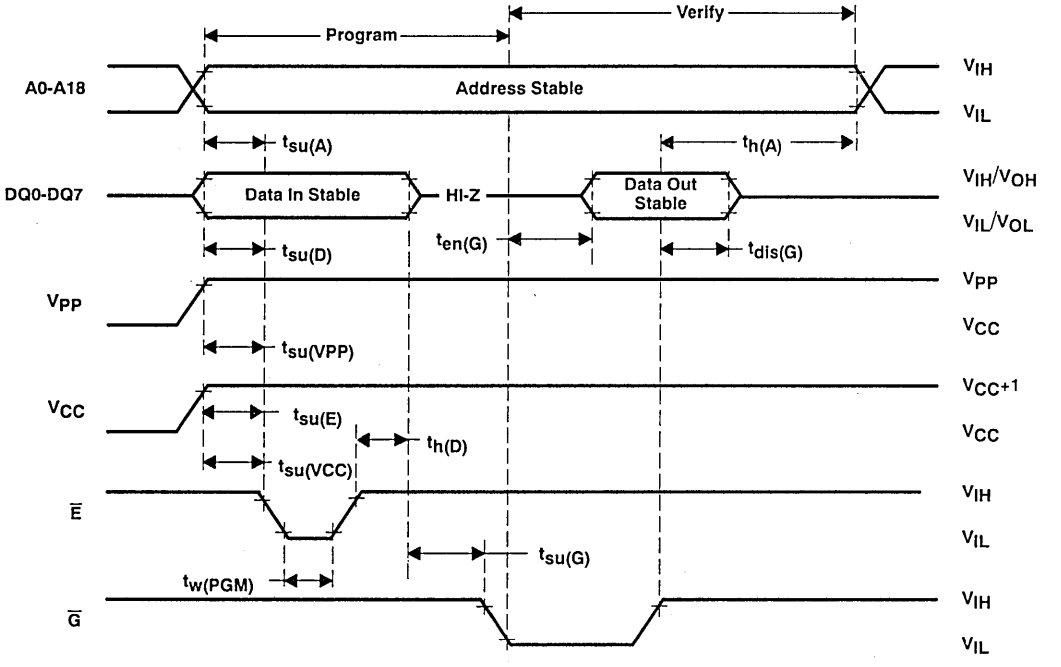
AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

read cycle timing



ADVANCE INFORMATION

program cycle timing (SNAP! Pulse programming)



ADVANCE INFORMATION

TMS27C240 4 194 304-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC240 4 194 304-BIT PROGRAMMABLE READ-ONLY MEMORY

SMLS240 — NOVEMBER 1990

ADVANCE INFORMATION

- Wide-Word Organization . . . 256K × 16
- Single 5-V Power Supply
- All Inputs/Outputs Fully TTL Compatible
- Static Operations (No Clocks, No Refresh)
- Max Access/Min Cycle Time

V_{CC} ± 5%	V_{CC} ± 10%	
'27C/PC240-8	'27C/PC240-80	80 ns
'27C/PC240-100	'27C/PC240-10	100 ns
'27C/PC240-120	'27C/PC240-12	120 ns
'27C/PC240-150	'27C/PC240-15	150 ns

- 16-Bit Output For Use in Microprocessor–Based Systems
- Very High Speed SNAP! Pulse Programming
- Power-Saving CMOS Technology
- 3-State Output Buffers
- 400-mV Minimum DC Noise Immunity With Standard TTL Loads
- Latchup Immunity of 250 mA on All Input and Output Lines
- No Pullup Resistors Required
- Low Power Dissipation (V_{CC} = 5.5 V)
  - — Active . . . 275 mW Worst Case
  - — Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)
- PEP4 Version Available With 168 Hour Burn-In, and Choices of Operating Temperature Ranges

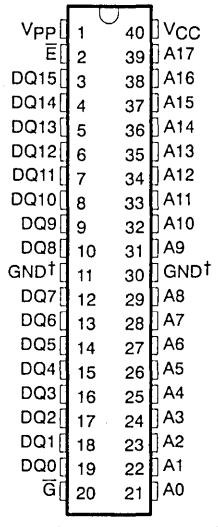
description

The TMS27C240 series are 4 194 304-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC240 series are 4 194 304-bit, one-time, electrically programmable read-only memories.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by

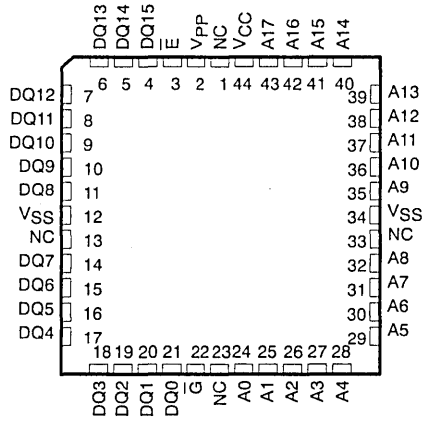
TMS27C240
J Package
(Top View)



PIN NOMENCLATURE	
A0-A17	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
DQ0-DQ15	Inputs (programming)/Outputs
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply‡

† Pins 11 and 30 must be connected externally to ground.
‡ Only in program mode.

TMS27PC240
FN Package
(Top View)



Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS27C240 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C240 is also offered with two choices of temperature ranges of 0°C to 70°C and – 40°C to 85°C (TMS27C240-_ _JL and TMS27C240-_ _JE, respectively). The TMS27C240 is also offered with 168 hour burn-in on both temperature ranges (TMS27C240-_ _JL4 and TMS27C240-_ _JE4, respectively). (See table below).

The TMS27PC240 OTP PROM is offered in a 44-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FN suffix). The TMS27PC240 is characterized for a temperature range of 0°C to 70°C.

	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C TO 70°C	– 40°C TO 85°C	0°C TO 70°C	– 40°C TO 85°C
TMS27C240-XXX	JL	JE	JL4	JE4
TMS27PC240-XXX	FNL	N/A	N/A	N/A

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), it is ideal for use in microprocessor-based systems. One other (13 V) supply is needed for programming . All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

There are eight modes of operation for the TMS27C240 and TMS27PC240 which are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse) and 12 V on A9 for signature mode.

	FUNCTION						
	$\overline{E}$	$\overline{G}$	V_{PP}	V_{CC}	A9	A0	I/O
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	X	X	DQ0-DQ7 DQ8-DQ15
Output Disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	X	X	HI-Z
Standby	V_{IH}	X†	V_{CC}	V_{CC}	X	X	HI-Z
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	X	Data In
Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	X	Data Out
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	X	X	HI-Z
Signature Mode (Mfg)	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H‡	V_{IL}	Mfg Code 0097
Signature Mode (Device)	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H‡	V_{IH}	Device Code 0030

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C240s or TMS27PC240s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C240 and TMS27PC240 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family"*, available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 50 mA to 1 mA for a high TTL input on $\overline{E}$ and to 100 μA for a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27C240)

Before programming, the TMS27C240 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C240, the window should be covered with an opaque label.

initializing (TMS27PC240)

The one-time programmable TMS27PC240 PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C240 and TMS27PC240 are programmed by using the SNAP! Pulse programming algorithm. The programming sequence is shown in the SNAP! Pulse programming flow chart (Figure 1).

The initial setup is V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IH}$. Once the initial location is selected, the data is presented in parallel (eight bits) on pins DQ0 through DQ15. Once addresses and data are stable, the programming mode is achieved when $\overline{E}$ is pulsed low (V_{IL}) with a pulse duration of $t_{w(PGM)}$. Every location is programmed only once before going to interactive mode.

In the interactive mode, the word is verified at V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IL}$. If the correct data is not read, the programming is performed by pulling $\overline{E}$ low with a pulse duration of $t_{w(PGM)}$. This sequence of verification and programming is performed up to a maximum of 10 times. When the device is fully programmed, all bytes are verified with $V_{CC} = V_{PP} = 5\ V \pm 10\%$.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ and $\overline{G}$ pins.

program verify

Programmed bits may be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$ and $\overline{E} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 31 for the J package) is forced to 12 V. Two identifier bytes are accessed by toggling A0. DQ0-DQ7 contain the valid codes. Each byte possesses odd parity on bit DQ7. All other addresses must be held low. The signature code for these devices is 9730. A0 low selects the manufacturer's code 97 (HEX), and A0 high selects the device code 30 (HEX), as shown by the signature mode table below.

signature mode†

IDENTIFIER†	PINS									
	A0	DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	HEX
MANUFACTURER CODE	1	0	0	1	0	0	1	1	1	97
DEVICE CODE	1	0	0	0	0	0	1	1	0	30

† $\overline{E} = \overline{G} = V_{IL}$, A9 = V_H, A1-A8 = V_{IL}, A10-A17 = V_{IL}, $V_{PP} = V_{CC}$, $\overline{PGM} = V_{IH}$ or V_{IL}.

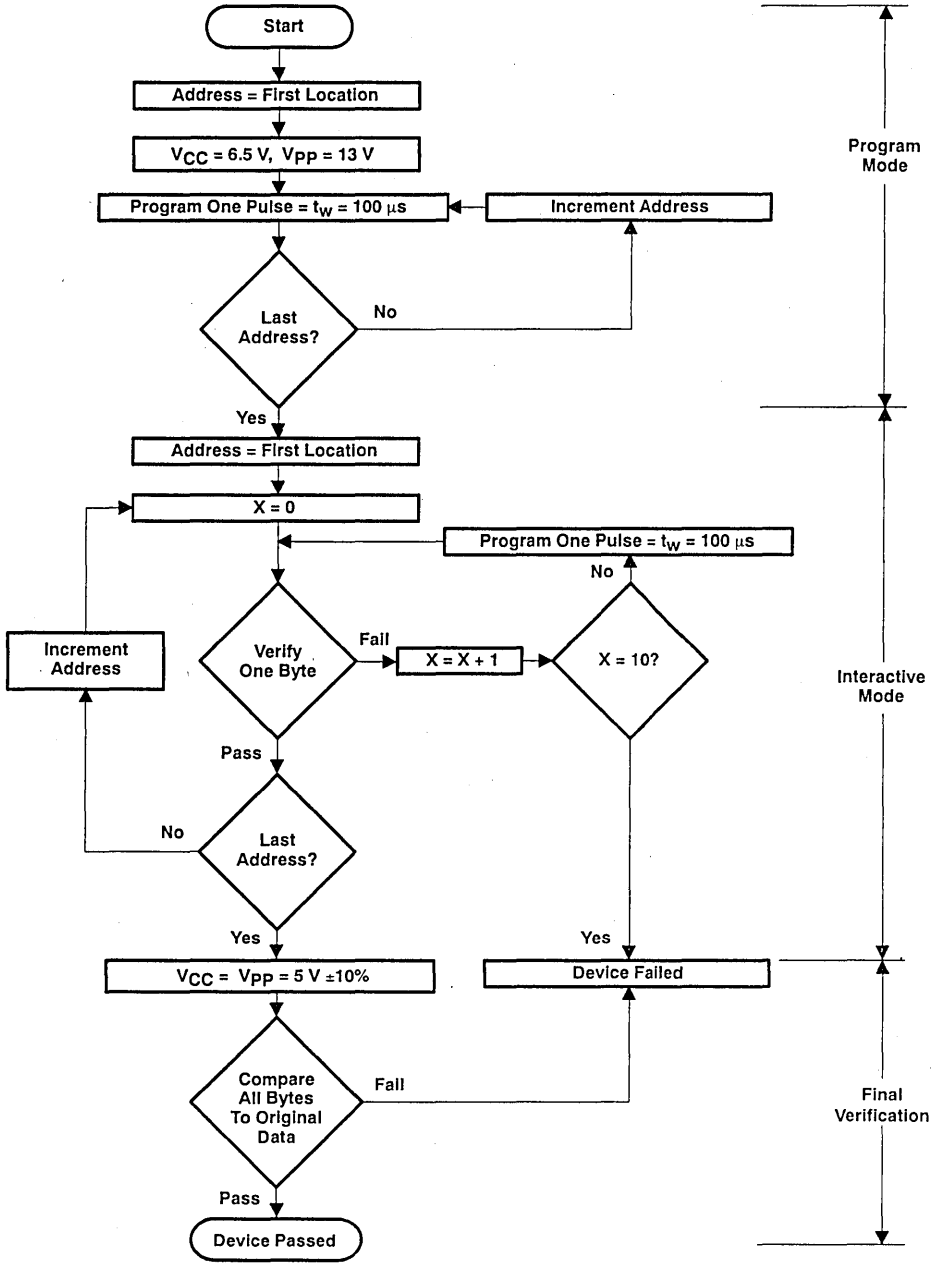
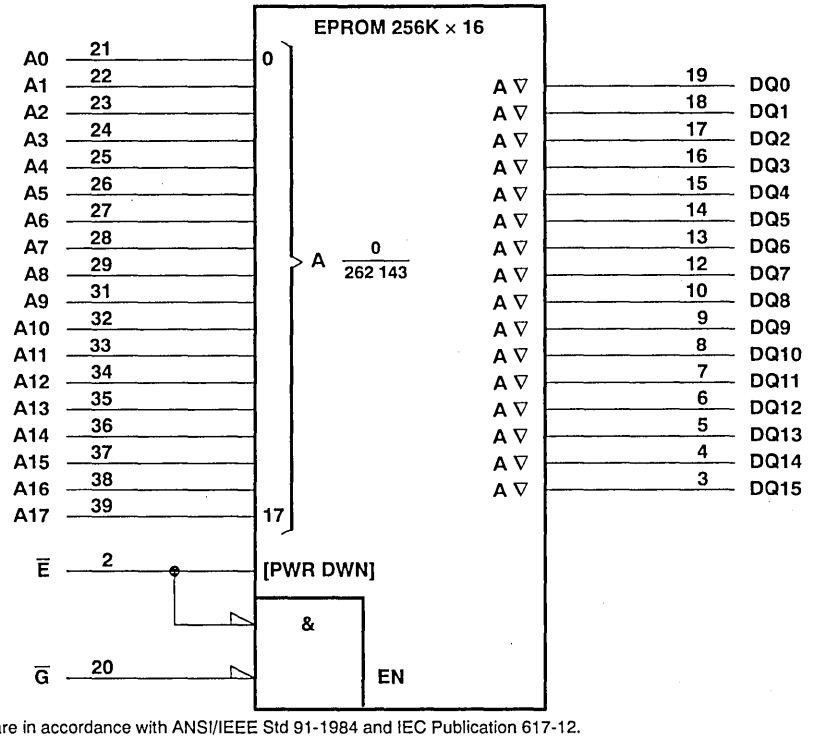


Figure 1. SNAP! Pulse Programming Flowchart

ADVANCE INFORMATION

logic symbol†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} ..... – 0.6 V to 13 V
Input voltage range (see Note 1): All inputs except A9 ..... – 0.6 V to 6.5 V
A9 ..... – 0.6 V to 13.5 V
Output voltage range (see Note 1) ..... – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C240-_ _JL and JL4,
'27PC240-_ _FNL) ..... 0° C to 70°C
Operating free-air temperature range ('27C240-_ _JE and JE4) ..... – 40° C to 85°C
Storage temperature range ..... – 65°C to 150°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			TMS27C/PC240-8, TMS27C/PC240-100, TMS27C/PC240-120, TMS27C/PC240-150			TMS27C/PC240-80, TMS27C/PC240-10, TMS27C/PC240-12, TMS27C/PC240-15			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.75	5	5.25	4.5	5	5.5	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode (see Note 3)	$V_{CC}-0.6$		$V_{CC}+0.6$	$V_{CC}-0.6$		$V_{CC}+0.6$	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	12.75	13	13.25	
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+0.5$	2		$V_{CC}+0.5$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+0.5$	$V_{CC}-0.2$		$V_{CC}+0.5$	
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		0.2	−0.5		0.2	
T_A	Operating free-air temperature	'27C240-_ _JL, JL4 '27PC240-_ _FNL	0		70	0		70	°C
T_A	Operating free-air temperature	'27C240-_ _JE, JE4	−40		85	−40		85	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, VPP must be maintained at 13 V ± 0.25 V.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = -2.5$ mA	2.4		V
			$I_{OH} = -20$ µA	$V_{CC}-0.1$		
V_{OL}	Low-level output voltage		$I_{OL} = 2.1$ mA		0.4	V
			$I_{OL} = 20$ µA		0.1	
I_I	Input current (leakage)		$V_I = 0$ to 5.5 V		±1	µA
I_O	Output current (leakage)		$V_O = 0$ to V_{CC}		±1	µA
I_{PP1}	V_{PP} supply current		$V_{PP} = V_{CC} = 5.5$ V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		$V_{PP} = 13$ V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{IH}$		1	mA
		CMOS-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{CC}$		100	µA
I_{CC2}	V_{CC} supply current (active)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open		50	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	$V_I = 0$		4	8	pF
C_O	Output capacitance	$V_O = 0$		8	12	pF

†Capacitance measurements are made on a sample basis only.
‡ Typical values are at $T_A = 25°C$ and nominal voltages.

ADVANCE INFORMATION

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 & 5)	'27C/PC240-8 '27C/PC240-80		'27C/PC240-100 '27C/PC240-10		'27C/PC240-120 '27C/PC240-12		'27C/PC240-150 '27C/PC240-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		80		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			80		100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		50		50		50	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first§		0	50	0	50	0	50	0	50	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first§		0		0		0		0		ns

†Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)

5. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 4)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 4: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)

ADVANCE INFORMATION

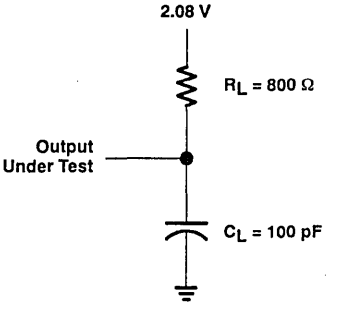
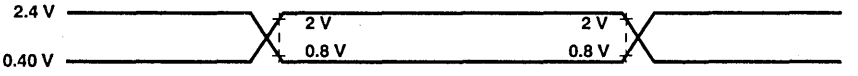


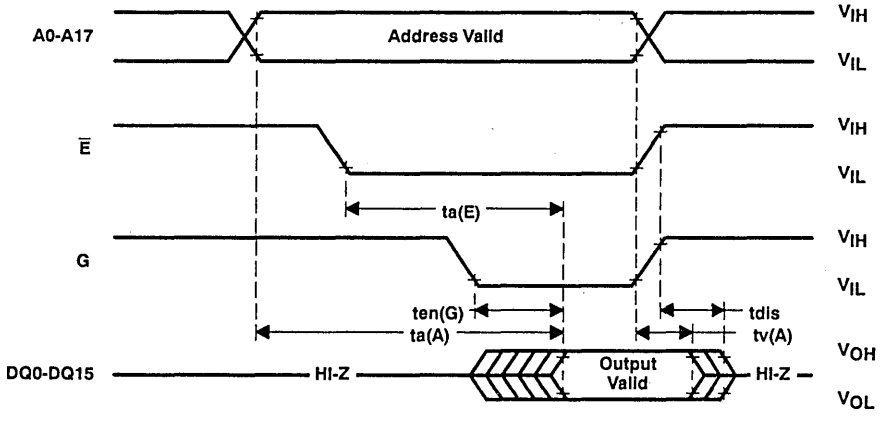
Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



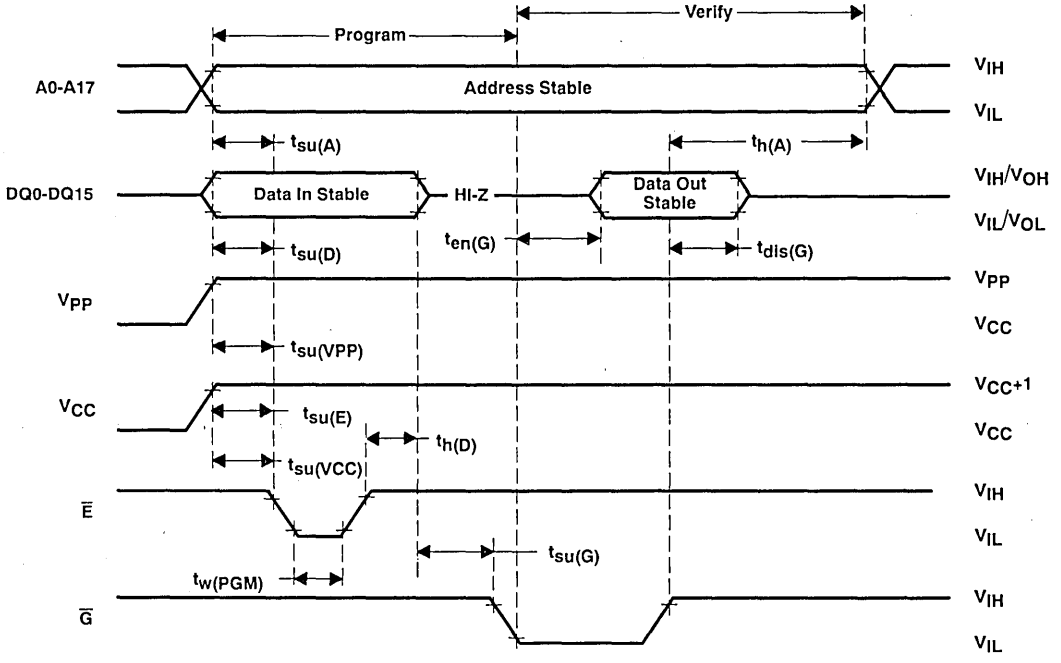
A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

read cycle timing



ADVANCE INFORMATION

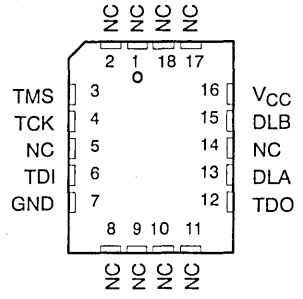
programming cycle timing (SNAP! Pulse programming)



ADVANCE INFORMATION

- Device is a Member of Texas Instruments SCOPE™ Family of Testability Products
- IEEE 1149.1 Serial Test Bus Compatible
- Embedded 2048 × 8-Bit Flash Memory
- 5-Volt Program/Erase/Read Operation
- 4 Flash Erasable Blocks (128, 384, 512, and 1024 Byte Size)
- Software Sequence Write/Erase Protection
- Write-Once Protection Bits
- Self-Timed Write/Erase Cycles
- Data Flow Read Mode
- 32-Byte Page Programming Mode
- CMOS Technology
- Single 5-V Power Supply (±10% Tolerance)
- 18-Pin Plastic Leaded Chip Carrier Package (FM Sufix)
- Operating Free-Air Temperature Range . . . 0°C to 70°C

FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
TMS	Test Mode Select
TCK	Test Clock
TDI	Test Data In
TDO	Test Data Out
DLA	Disable Lock A
DLB	Disable Lock B
V_{CC}	5-V Power Supply
GND	Ground
NC	No Connect

PRODUCT PREVIEW

description

The TMS29F816 SCOPE™ Diary is a 16 384-bit, programmable storage device that can be electrically bulk-erased and reprogrammed. All device operations are accomplished via a 4-wire Test Access Port (TAP) interface. This interface complies with the IEEE 1149.1 Serial Test Bus standard (JTAG). The interface consists of two control signals; Test Mode Select (TMS) and Test Clock (TCK); and two test data pins, Test Data In (TDI) and Test Data Out (TDO). The JTAG Test Access Protocol defines how this 4-wire test bus is used to scan-in instructions and data, to execute instructions, and to scan-out the resulting data.

All test information is serially loaded into the chip via TDI and out of the chip via TDO. The Diary has the three JTAG mandatory components, a Test Access Port (TAP) controller, a set of Test Data Registers, and an Instruction Register. The TAP controller interfaces the Test Data Registers and the Instruction Register to the 4-wire test bus. The Test Data Registers apply and/or capture test data. The Instruction Register selects the Test Data Register to be accessed and the test to be performed.

The Test Data Registers consists of three different types: the Data Scan Registers (DSR), the Bypass Register (BR), and the Device Identification Register (DIR).

The TMS29F816 SCOPE Diary features an embedded Flash EEPROM array, internal circuitry for self-timed programming/erasing, and completion polling. In the erased state all bits are at a logic 1. To reprogram, all memory bits in a selected block are erased first, and then those bits that should be logic zeroes are programmed accordingly. The device is fabricated using HVCMOS flotox technology for high-reliability and very low power dissipation. It performs the erase/program operations automatically with a single 5-V supply, and it can program a single byte or any number of bytes between 1 and 32 within the same page. During programming and erasing, the completion status is available, allowing the system to maximize throughput.

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The TMS29F816 is divided into four independently flash erasable blocks. These block are configured as 128, 384, 512, and 1024 bytes in size. Four write-once, lock-bits can be programmed to prevent erasure and programming of each block.

The device is protected against write and erase commands during power-up and power down by an on-chip power supply reference comparator. Software sequences are used to protect against inadvertent program and erase commands during normal operation.

The TMS29F816 is available in a 1000 cycle endurance version, and is characterized for operation from 0°C to 70°C.

The TMS29F816 is offered in an 18-pin plastic leaded chip carrier package (FM suffix).

pin descriptions

PIN NO.	I/O	DESCRIPTION
TMS	I	Test Mode Select. Controls transition of TAP finite state machine. This input is sampled on the rising edge of TCK.
TCK	I	Test Clock. Input clock to TAP finite state machine. All changes in state are synchronous to the test clock TCK.
TDI	I	Test Data In. Data input to the internal register scan path. Data on this pin is sampled on the rising edge of TCK.
TDO	O	Test Data Out. Data output from the internal register scan path. Data is updated on this pin on the falling edge of TCK.
DLA	I	Disable Lock A. Controls lock-bit functionally for memory array bank 0. When DLA = V_{IL}, the state of lock-bit 0 (LCK0) determines whether bank 0 can be erased or programmed. When DLA = V_{IH}, bank 0 can be erased or programmed irrespective of the state of lock-bit 0. (When DLA = V_H (V_H >> V_{CC}), the device enters a special manufacturing test mode.
DLB	I	Disable Lock B. Input that controls lock bit functionality for memory banks 1, 2 and 3. When DLB = V_{IL}, the states of lock-bits 1, 2 and 3 (LCK1, LCK2, LCK3) determine whether their respective banks (1, 2 and 3) can be erased or programmed. When DLB = V_{IH}, banks 1, 2 and 3 can be erased or programmed, irrespective of the state of their associated lock-bits.
V_{CC}	I	5-V Power Supply. 5-V ± 10% operating power supply connection.

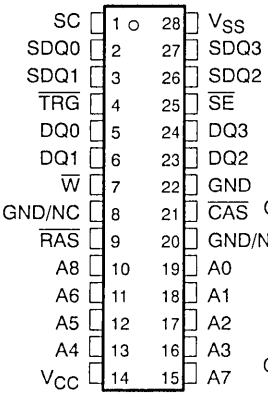
PRODUCT PREVIEW

REV A — SMVS250 — JUNE 1990 — REVISED JANUARY 1991

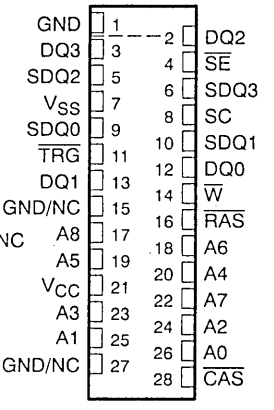
- DRAM: 262 144 Words × 4 Bits
  SAM: 512 Words × 4 Bits
- Dual Port Accessibility — Simultaneous and Asynchronous Access from the DRAM and SAM Ports
- Bidirectional Data Transfer Function Between the DRAM and the Serial Data Register
- Write Per Bit Feature for Selective Write to Each RAM I/O.
- Enhanced Page Mode Operation for Faster Access
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ and Hidden Refresh Modes
- RAM Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design
- Long Refresh Period . . . Every 8 ms (Max)
- DRAM Port Is Compatible with the TMS44C256
- Up to 33 MHz Uninterrupted Serial Data Streams
- 3-State Serial I/Os Allow Easy Multiplexing of Video Data Streams
- 512 Selectable Serial Register Starting Locations
- All Inputs and Outputs TTL Compatible
- Performance Ranges: V_{CC} ± 10%

	ACCESS TIME ROW ADDRESS (MAX) $t_{a(R)}$	ACCESS TIME COLUMN ENABLE (MAX) $t_{a(C)}$	ACCESS TIME SERIAL DATA (MAX) $t_{a(SC)}$	ACCESS TIME SERIAL ENABLE (MAX) $t_{a(SE)}$
TMS44C250-10	100 ns	25 ns	30 ns	20 ns
TMS44C250-12	120 ns	30 ns	35 ns	25 ns

DZ Package
(Top View)



SD Package
(Top View)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{\text{CAS}}$	Column Enable
DQ0-DQ3	DRAM Data In-Out/Write Mask Bit
$\overline{\text{SE}}$	Serial Enable
$\overline{\text{RAS}}$	Row Enable
SC	Serial Data Clock
SDQ0-SDQ3	Serial Data In-Out
$\overline{\text{TRG}}$	Transfer Register/Q Output Enable
$\overline{\text{W}}$	Write Mask Select/Write Enable
GND/NC	No Connect or Ground Only
V_{CC}	5-V Supply
V_{SS}	Ground
GND	Ground (Important: not connected to internal V_{SS})

- Performance Ranges: V_{CC} ± 5%

	ACCESS TIME ROW ADDRESS (MAX) $t_{a(R)}$	ACCESS TIME COLUMN ENABLE (MAX) $t_{a(C)}$	ACCESS TIME SERIAL DATA (MAX) $t_{a(SC)}$	ACCESS TIME SERIAL ENABLE (MAX) $t_{a(SE)}$
TMS44C250-1	100 ns	25 ns	30 ns	20 ns

- Texas Instruments EPIC™ CMOS Process

description

The TMS44C250 Multiport Video RAM is a high speed, dual ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 4 bits each, interfaced to a serial data register, or Serial Access Memory (SAM), organized as 512 words of 4 bits each. The TMS44C250 supports three basic types of operation: random access to and from the DRAM, serial access to and from the serial register, and bidirectional transfer of data between any row in the DRAM and the serial register. Except during transfer

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operations, the TMS44C250 can be accessed simultaneously and asynchronously from the DRAM and SAM ports. During transfer operation, the 512 columns of the DRAM are connected to the 512 positions in the serial data register. The 512 × 4 bit serial data register can be loaded from the memory row (transfer read) or else the contents of the 512 × 4 bit serial data register can be written to the memory row (transfer write).

The SAM can also be configured in input mode, accepting serial data from an external device. Once the serial register within the SAM is loaded, its contents can be transferred to the corresponding column positions in any row in memory in a single memory cycle. The SAM port is designed for maximum performance. Data can be input to or accessed from the SAM at serial rates up to 33 MHz.

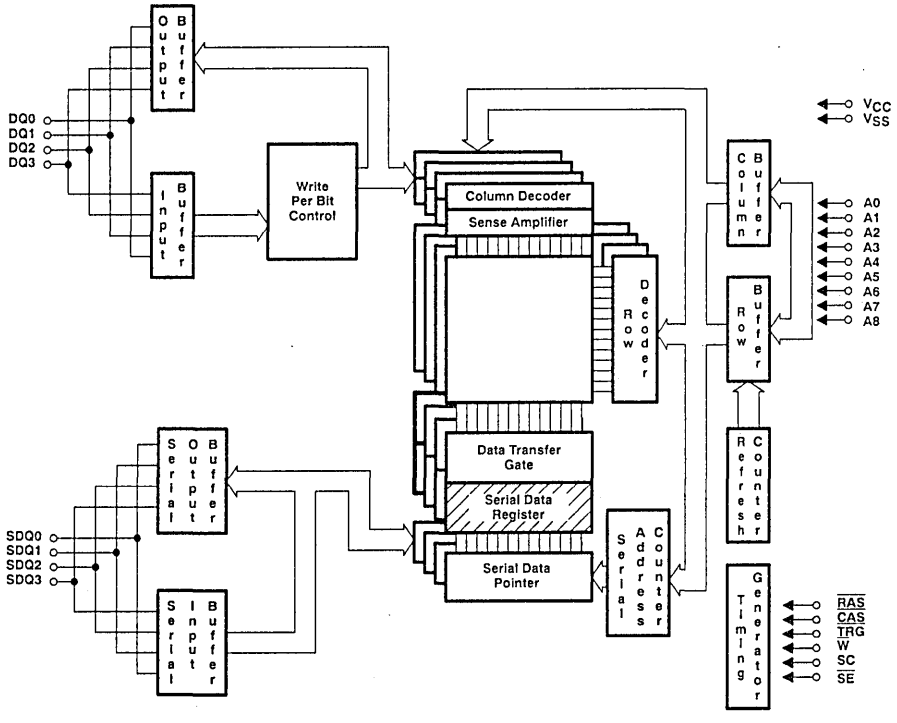
All inputs, outputs, and clock signals on the TMS44C250 are compatible with Series 74 TTL. All address lines and data-in are latched on-chip to simplify system design. All data-outs are unlatched to allow greater system flexibility.

The TMS44C250 employs state-of-the-art Texas Instruments EPIC™ scaled-CMOS, double level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The TMS44C250 is offered in a 28-pin small-outline J-leaded package (DZ suffix) for direct surface mounting in rows on 400-mil (5,08-mm) centers. It is also offered in a 400-mil, 28-pin zig-zag in-line package (SD suffix). Both packages are characterized for operation from 0°C to 70°C (L suffix).

The TMS44C250 and other Multiport Video RAMs are supported by a broad line of graphics processor and control devices from Texas Instruments.

functional block diagram



Detailed Pin Description vs Operational Mode

PIN	DRAM	TRANSFER	SAM
A0-A8	Row, Column Address	Row, Tap Address	
$\overline{CAS}$	Column Enable, Output Enable	Tap Address Strobe	
DQi	DRAM Data I/O, Write Mask Bits		
$\overline{SE}$		Serial-In Mode Enable	Serial Enable
$\overline{RAS}$	Row Enable	Row Enable	
SC			Serial Clock
SDQi			Serial Data I/O
$\overline{TRG}$	Q Output Enable	Transfer Enable	
$\overline{W}$	Write Enable, Write per Bit Select	Transfer Write Enable	
V_{CC}	5-V Supply (typical)		
V_{SS}	Device Ground		
GND/NC	No Connect or Ground Only		
GND	System Ground		

operation

random access operation

Refer to Table 1, Functional Table, for Random Access and Transfer Operations. Random access operations are denoted by the designator "R" and transfer operations are denoted by a " T."

transfer register select and DQ enable ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either register or random access operation as $\overline{RAS}$ falls. For random access (DRAM) mode, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. Asserting $\overline{TRG}$ high as $\overline{RAS}$ falls causes the 512 storage elements of each data register to remain disconnected from the corresponding 512-bit lines of the memory array. (Asserting $\overline{TRG}$ low as $\overline{RAS}$ falls connects the 512-bit positions in the serial register to the bit lines and indicates that a transfer will occur between the data registers and the selected memory row. See "Transfer Operation" for details.)

During random access operations, $\overline{TRG}$ also functions as an output enable for the random (Q) outputs. Whenever $\overline{TRG}$ is held high, the Q outputs are in the high-impedance state to prevent an overlap between the address and DRAM data. This organization allows the connection of the address lines to the data I/O lines but prohibits the use of the early write cycle. It also allows read-modify-write cycles to be performed by providing a three-state condition to the common I/O pins so that write data can be driven onto the pins after output read data has been externally latched.

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Then, the nine column address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

$\overline{RAS}$ and $\overline{CAS}$ address strobes and device control clocks

$\overline{RAS}$ is a control input that latches the states of the row address, $\overline{W}$, $\overline{TRG}$, $\overline{SE}$, and $\overline{CAS}$, onto the chip to invoke the various DRAM and Transfer functions of the TMS44C250. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is a control input that latches the states of the column address. $\overline{CAS}$ also acts as an output enable for the DRAM output pins.

write enable, write-per-bit enable ($\overline{W}$)

The $\overline{W}$ pin enables data to be written to the DRAM and is also used to select the DRAM write per bit mode of operation. A logic high level on the $\overline{W}$ input selects the read mode and logic low level selects the write mode. In an early write cycle, $\overline{W}$ is brought low before $\overline{CAS}$ and the DRAM output pins (DQ) remain in the high-impedance state for the entire cycle. During DRAM write cycles, holding $\overline{W}$ low on the falling edge of $\overline{RAS}$ will invoke the write per bit operation.

A four-bit binary code (the write-per-bit mask) is input to the device via the random DQ pins and is latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the four random I/Os are written and which are not. After $\overline{RAS}$ has latched the write mask on-chip, input data is driven onto the DQ pins and is latched on the falling edge of the later of $\overline{CAS}$ or $\overline{W}$. If a 0 was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will not be written to that I/O. If a 1 was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will be written to that I/O.

See the corresponding timing diagrams for details. IMPORTANT: The write-per-bit operation is invoked only if $\overline{W}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{W}$ is held high on the falling edge of $\overline{RAS}$, write per bit is not enabled and the write operation is identical to that of standard × 4 DRAMs.

data I/O (DQ0-DQ3)

DRAM data is written during a write or read-modify-write cycle. The falling edge of $\overline{W}$ strobes data into the on-chip data latches. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with data setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low. Thus, the data will be strobed-in by $\overline{W}$ with data setup and hold times referenced to this signal.

The three-state output buffers provide direct TTL compatability (no pullup resistors required) with a fanout of two Series 74 TTL loads. Data-out is the same polarity as data-in. The outputs are in the high impedance (floating) state as long as $\overline{CAS}$ or $\overline{TRG}$ is held high. Data will not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low. Once the outputs are valid, they remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. $\overline{CAS}$ and $\overline{TRG}$ going high returns the outputs to a high-impedance state. In an early write cycle, the outputs are always in the high-impedance state. In a register transfer operation (memory to register or register to memory), the outputs remain in the high-impedance state for the entire cycle.

enhanced page mode

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows theTMS44C250 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as "enhanced page mode." Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

Enhanced page mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row address setup, row address hold, and address multiplex is thus eliminated, and a memory cycle time reduction of up to 3 × can be achieved, compared to minimum $\overline{RAS}$ cycle times. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and page mode cycle time used. The TMS44C250 allows a full page (512 cycles) of information to be accessed in read, write, or read-modify-write mode during a single $\overline{RAS}$ low period using relatively conservative page mode cycle times.

refresh

A refresh operation must be performed to each row at least once every eight milliseconds to retain data. Since the output buffer is in the high-impedance state (unless $\overline{CAS}$ is applied), the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$. The external row address is ignored and the refresh address is generated internally.

GND

This pin is reserved for the manufacturer's test operation. It is an input and should be tied to system ground or left floating (no connection) to ensure proper device operation.

IMPORTANT: GND is not connected internally to V_{SS}.

Table 1. Functional Table

TYPE†	RAS FALL				ADDRESS		DQ0-DQ3		FUNCTION
	CAS	TRG	W	SE	RAS	CAS	RAS	CAS‡ W	
R	L	X§	X	X	X	X	X	X	CAS-Before-RAS Refresh
T	H	L	L	L	Row Addr	Tap Point	X	X	Register to Memory Transfer (Transfer Write)
T	H	L	L	H	Refresh Addr	Tap Point	X	X	Serial Write-mode Enable (Pseudo-Transfer Write)
T	H	L	H	X	Row Addr	Tap Point	X	X	Memory to Register Transfer (Transfer Read)
R	H	H	L	X	Row Addr	Col Addr	Write Mask	Valid Data	Load and use Write Mask, Write Data to Dram
R	H	H	H	X	Row Addr	Col Addr	X	Valid Data	Normal Dram Read/Write (Non Masked)

† R = Random access operation; T = Transfer operation.
‡ DQ0-3 are latched on the later of W or CAS falling edge.
§ X = Don't care.
WRITE MASK = 1 write to I/O enabled.

random port to serial port interface

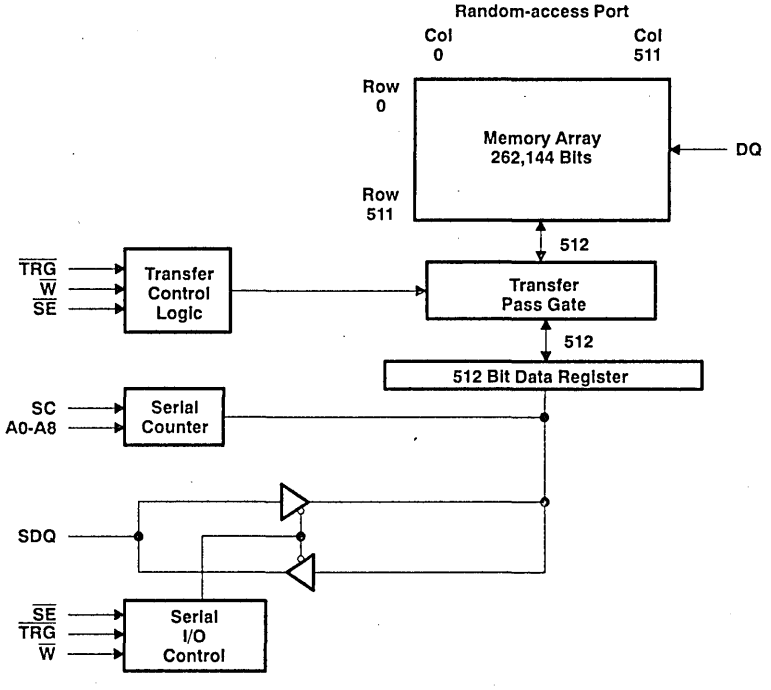


Figure 1. Block Diagram Showing One Random and One Serial I/O Interface

random address space to serial address space mapping

The 512 bits in each of the four data registers of the SAM are connected to the 512 column locations of each of the four random I/Os. Data can be accessed in or out of the SAM starting at any of the 512 data bit locations. This start location is selected by addresses A0 through A8 on the falling edge of $\overline{CAS}$ during any transfer cycle. The SAM is accessed starting from the selected start address, proceeding from the lowest to the highest significant bits. After the most significant bit position (511) is accessed, the serial counter wraps around such that bit 0 is accessed on the next clock pulse. The selected start address is stored and used for all subsequent transfer cycles until $\overline{CAS}$ is again brought low during any transfer cycle. Thus, the start address can be set once and $\overline{CAS}$ held high during all subsequent transfer cycles and the start address point will not change regardless of data present on A0 through A8.

transfer operations

As illustrated in Table 1, the TMS44C250 supports three basic transfer modes of operation:

1. Write Transfer (SAM to DRAM)
2. Pseudo Write Transfer (Switches serial port from serial out mode to serial in mode. No actual data transfer takes place between the DRAM and the SAM.)
3. Read Transfer (Transfer entire contents of DRAM to SAM)

transfer register select ($\overline{TRG}$)

Transfer operations between the memory array and the data registers are invoked by bringing $\overline{TRG}$ low before $\overline{RAS}$ falls. The states of $\overline{W}$ and $\overline{SE}$, which are also latched on the falling edge of $\overline{RAS}$, determine which transfer operation will be invoked. (See Table 2.)

During read transfer cycles, $\overline{TRG}$ going high causes the addressed row of data to be transferred into the data register. Although the previous data in the data register is overwritten, the last bit of data appearing at SDQ before $\overline{TRG}$ goes high will remain valid until the first positive transition of SC after $\overline{TRG}$ goes high. The data at SDQ will then switch to new data beginning from the selected start, or "tap," position.

transfer write enable ($\overline{W}$)

In register transfer mode, $\overline{W}$ determines whether a read or a write transfer will occur. To perform a write transfer, $\overline{W}$ and $\overline{SE}$ are held low as $\overline{RAS}$ falls. If $\overline{SE}$ is high during this transition, no transfer of data from the data register to the memory array occurs, but the SDQs are put into the input mode. This allows serial data to be input into the SAM. To perform a read transfer operation, $\overline{W}$ is held high and $\overline{SE}$ is a Don't Care as $\overline{RAS}$ falls. This cycle also puts the SDQs into the read mode, allowing serial data to be shifted out of the data register. (See Table 2.)

column enable ($\overline{CAS}$)

If $\overline{CAS}$ is brought low during a control cycle, the address present on the pins A0 through A8 will become the new register start location. If $\overline{CAS}$ is held high during a control cycle, the previous tap address will be retained from the last transfer cycle in which $\overline{CAS}$ went low to set the tap address.

addresses (A0 through A8)

Nine address bits are required to select one of the 512 possible rows involved in the transfer of data to or from the data registers. The states of A0-A8 are latched on the fallling edge of $\overline{RAS}$ to select one of 512 rows for the transfer operation.

To select one of the 512 positions in the SAM from which the first serial data will be accessed, the appropriate 9-bit column address (A0-A8) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and start (tap) position need not be supplied every cycle, only when changing to a different start position.

serial access operation

Refer to Tables 2 and 3 for the following discussion on serial access operation.

serial clock (SC)

Data (SDQ) is accessed in or out of data registers on the rising edge of SC. The TMS44C250 is designed to work with a wide range of clock duty cycles to simplify system design. Since the data registers comprising the SAM are of static design, there are no SAM refresh requirements and there is no minimum SC clock operating frequency.

serial data input/output (SDQ0-SDQ3)

SD and SQ share a common I/O pin. Data is input to the device when $\overline{SE}$ is low during write mode and data is output from the device when $\overline{SE}$ is low during read mode. The data in the SAM will be accessed in the direction from least significant bit to most significant bit. The data registers operate modulo 512. Thus, after bit 511 is accessed, the next bits to be accessed will be bits 00, 01, 02, and so on.

serial enable ($\overline{SE}$)

The Serial Enable pin has two functions: first, it is latched on the falling edge of $\overline{RAS}$, with both $\overline{TRG}$ and $\overline{W}$ low to select one of the transfer functions (see Table 3.) If $\overline{SE}$ is low during this transition, then a transfer write occurs. If $\overline{SE}$ is high as $\overline{RAS}$ falls, then a write mode control cycle is performed. The function of this cycle is to switch the SDQs from the output mode to the input mode, thus allowing data to be shifted into the data register. NOTE: All transfer read and serial mode enable (pseudo transfer write) operations will perform a memory refresh operation on the selected row.

Second, during serial access operations, $\overline{SE}$ is used as an SDQ enable/disable. In the write mode, $\overline{SE}$ is used as an input enable. $\overline{SE}$ high disables the input and $\overline{SE}$ low enables the input. To take the device out of the write mode and into the read mode, a transfer read cycle must be performed. The read mode allows data to be accessed from the data register. While in the read mode, $\overline{SE}$ high disables the output and $\overline{SE}$ low enables the output.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is NOT disabled. Thus, external SC pulses will increment the internal serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low since the serial clock input buffer and the serial address counter are not disabled by $\overline{SE}$.

Table 2. Transfer Operation Logic

$\overline{TRG}$	$\overline{W}$	$\overline{SE}$	MODE
L	L	L	Register to memory (write) transfer
L	L	H	Serial write mode enable
L	H	X	Memory to register (read) transfer

NOTE: Above logic states are assumed valid on the falling edge of $\overline{RAS}$.

Table 3. Serial Operation Logic

LAST TRANSFER CYCLE	$\overline{SE}$	SDQ
Serial write mode enable†	L	Input enable
Serial write mode enable†	H	Input disable
Memory to register	L	Output enabled
Memory to register	H	Hi-Z

†Pseudo transfer write

power up

To achieve proper device operation, an initial pause of 200 μs is required after power up, followed by a minimum of eight $\overline{RAS}$ cycles or eight $\overline{CAS}$-before-$\overline{RAS}$ cycles, a memory-to-register transfer cycle and two SC cycles.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage on any pin except DQ and SDQ (see Note 1) ..... – 1 V to 7 V
Voltage on DQ and SDQ (see Note 1) ..... – 1 V to V_{CC}
Voltage range on V_{CC} (see Note 1) ..... 0 V to 7 V
Short circuit output current (per output) ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	TMS44C250-1	4.75	5	5.25	V
		TMS44C250-10, TMS44C250-12	4.5	5	5.5	
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage		2.4		V_{CC}	V
V_{IL}	Low-level input voltage (see Note 2)		– 1.0		0.8	V
V_{OH}	High-level output voltage		2.4		V_{CC}	V
V_{OL}	Low-level output volage		– 1		0.4	V
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	TMS44C250-1 TMS44C250-10		TMS44C250-12		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High level output voltage		I_{OH} = – 5.0 mA	2.4		2.4		V
V_{OL}	Low level output voltage		I_{OL} = 4.2 mA		0.4		0.4	V
I_L	Input leakage current	TMS44C250-10, TMS44C250-12	V_I = 0 V to 5.8 V, V_{CC} = 5.5 V All other pins = 0 V to V_{CC}		±10		±10	µA
		TMS44C250-1	V_I = 0 V to 5.55 V, V_{CC} = 5.25 V All other pins = 0 V to V_{CC}		±10		±10	µA
I_O	Output leakage current (see Note 3)	TMS44C250-10, TMS44C250-12	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V		±10		±10	µA
I_O	Output leakage current (see Note 3)	TMS44C250-1	V_O = 0 V to V_{CC}, V_{CC} = 5.25 V		±10		±10	µA

PARAMETER		SAM PORT	TMS44C250-1 TMS44C250-10		TMS44C250-12		UNIT
			MIN	MAX	MIN	MAX	
I_{CC1}	Operation current $t_{c(RW)}$ = Minimum	Standby		90		80	mA
I_{CC1A}	$t_{c(SC)}$ = Minimum	Active		110		95	
I_{CC2}	Standby current, All clocks = V_{CC}	Standby		10		10	
I_{CC2A}	$t_{c(SC)}$ = Minimum	Active		35		35	
I_{CC3}	$\overline{RAS}$-only refresh current, $t_{c(RW)}$ = Minimum	Standby		90		80	
I_{CC3A}	$t_{c(SC)}$ = Minimum	Active		110		95	
I_{CC4}	Page mode current, $t_{c(P)}$ = Minimum	Standby		50		45	
I_{CC4A}	$t_{c(SC)}$ = Minimum	Active		60		55	
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ current, $t_{c(RW)}$ = Minimum	Standby		90		80	
I_{CC5A}	$t_{c(SC)}$ = Minimum	Active		110		95	
I_{CC6}	Data transfer current, $t_{c(RW)}$ = Minimum	Standby		90		80	
I_{CC6A}	$t_{c(SC)}$ = Minimum	Active		110		95	

NOTE 3: $\overline{SE}$ is disabled for SDQ output leakage tests.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 4)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write enable input		7	pF
$C_{i(SC)}$	Input capacitance, serial clock		7	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		7	pF
$C_{o(O)}$	Output capacitance, SDQ and DQ		7	pF

NOTE 4: V_{CC} equal to 5 V ± 0.5 V for TMS44C250-10, and TMS44C250-12; 5 V ± 0.25 V for TMS44C250-1, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS44C250-1 TMS44C250-10		TMS44C250-12		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{d(RLCL)}$ = MAX	t_{CAC}	0	25		30	ns
$t_{A(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{CAA}		50		60	ns
$t_{a(CP)}$	Access time from $\overline{CAS}$ high	$t_{d(RLCL)}$ = MAX	t_{CAP}		55		65	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MAX	t_{RAC}		100		120	ns
$t_{a(G)}$	Access time of Q from $\overline{TRG}$ low		t_{OEA}		25		30	ns
$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 50 pF	t_{SCA}		30		35	ns
$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 50 pF	t_{SEA}		20		25	ns
$t_{dis(CH)}$	Random output disable time from $\overline{CAS}$ high	C_L = 100 pF	t_{OFF}	0	20	0	20	ns
$t_{dis(G)}$	Random output disable time from $\overline{TRG}$ high	C_L = 100 pF	t_{OEZ}	0	20	0	20	ns
$t_{dis(SE)}$	Serial output disable time from $\overline{SE}$ high	C_L = 50 pF	t_{SEZ}	0	20	0	20	ns

NOTE 5: Switching times assume C_L = 100 pF unless otherwise noted (see Figure 2).

timing requirements over recommended ranges of supply voltage and operating free-air temperature†

		ALT. SYMBOL	TMS44C250-1 TMS44C250-10		TMS44C250-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	190		220		ns
$t_{c(W)}$	Write cycle time	t_{WC}	190		220		ns
$t_{c(rdW)}$	Read-modify-write cycle time	t_{RWC}	250		290		ns
$t_{c(P)}$	Page-mode read, write cycle time	t_{PC}	60		70		ns
$t_{c(RDWP)}$	Page-mode read-modify-write cycle time	t_{RWC}	105		125		ns
$t_{c(TRD)}$	Transfer read cycle time	t_{RC}	190		220		ns
$t_{c(TW)}$	Transfer write cycle time	t_{WC}	190		220		ns
$t_{c(SC)}$	Serial clock cycle time (see Note 7)	t_{SCC}	30		35		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		15		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	25	75 000	30	75 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	80		90		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	100	75 000	120	75 000	ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	t_{WP}	25		25		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		25		35		ns
$t_{w(SCH)}$	Pulse duration, SC high	t_{SC}	10		12		ns
$t_{w(SCL)}$	Pulse duration, SC low	t_{SCP}	10		12		ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(WMR)}$	$\overline{W}$ setup time before $\overline{RAS}$ low	t_{WSR}	0		0		ns
$t_{su(DQR)}$	DQ setup time before $\overline{RAS}$ low	t_{MS}	0		0		ns
$t_{su(TRG)}$	$\overline{TRG}$ setup time before $\overline{RAS}$ low	t_{TLS}	0		0		ns
$t_{su(SE)}$	$\overline{SE}$ setup time before $\overline{RAS}$ low	t_{ESR}	0		0		ns
$t_{su(DCL)}$	Data setup time before $\overline{CAS}$ low	t_{DSC}	0		0		ns
$t_{su(DWL)}$	Data setup time before $\overline{W}$ low	t_{DSW}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
$t_{su(WCH)}$	Write setup time before $\overline{CAS}$ high	t_{CWL}	25		30		ns
$t_{su(WRH)}$	Write setup time before $\overline{RAS}$ high with $\overline{TRG}$ = $\overline{W}$ = low	t_{RWL}	25		30		ns
$t_{su(SDS)}$	SD setup time before SC high	t_{SDS}	3		3		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		ns
$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		ns

Continued next page.

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 6. All cycle times assume t_t = 5 ns.

7. When the odd tap is used (tap address can be 0-511, and odd taps are 1,3,5, etc.), the cycle time for SC in serial data out cycle needs to be 50 ns minimum.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

		ALT. SYMBOL	TMS44C250-1 TMS44C250-10		TMS44C250-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(TRG)}$	$\overline{TRG}$ hold time after $\overline{RAS}$ low	t_{TLH}	15		15		ns
$t_{h(SE)}$	$\overline{SE}$ hold time after $\overline{RAS}$ low with $\overline{TRG}$ = $\overline{W}$ = low	t_{REH}	15		15		ns
$t_{h(RWM)}$	Write mask, transfer enable hold time after $\overline{RAS}$ low	t_{RWH}	15		15		ns
$t_{h(RDQ)}$	DQ hold time after $\overline{RAS}$ low (write mask operation)	t_{MH}	15		15		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low (see Note 9)	t_{AR}	45		45		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	20		25		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 10)	t_{DHR}	45		50		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	20		25		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ (see Note 11)	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ (see Note 11)	t_{RRH}	10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 10)	t_{WCR}	50		55		ns
$t_{h(WLG)}$	$\overline{TRG}$ hold time after $\overline{W}$ low (see Note 12)	t_{OEH}	25		30		ns
$t_{h(SDS)}$	SD hold time after SC high	t_{SDH}	5		5		ns
$t_{h(SHSQ)}$	SQ hold time after SC high	t_{SOH}	10		10		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	30		35		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Notes 13 and 14)	t_{CWD}	55		65		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Notes 15 and 16)	t_{RCD}	25	75	25	90	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	50		60		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)	t_{RWD}	130		155		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 13)	t_{AWD}	85		100		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 11)	t_{CHR}	25		25		ns
$t_{d(CLRL)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 17)	t_{CSR}	10		10		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 17)	t_{RCP}	5		5		ns
$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high	t_{CTH}	25		35		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ		25		30		ns
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high	t_{RTH}	90		95		ns

Continued next page.

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].
10. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
11. Either $t_{h(RHrd)}$ or $t_{(CHrd)}$ must be satisfied for a read cycle.
12. Output enable controlled write. Output remains in the high-impedance state for the entire cycle.
13. Read-modify-write operation only.
14. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
15. Read cycles only.
16. Maximum value specified only to guarantee $\overline{RAS}$ access time.
17. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only.

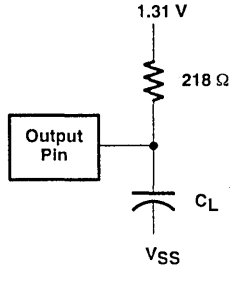
timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)†

		ALT. SYMBOL	TMS44C250-1 TMS44C250-10		TMS44C250-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 18)	t_{RSD}	130		135		ns
$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 18)	t_{CSD}	40		45		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 18 and 19)	t_{TSL}	10		15		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 18)	t_{TRD}	−10		−10		ns
$t_{d(SCRL)}$	Delay time, SC high to $\overline{RAS}$ low with $\overline{TRG}$ = $\overline{W}$ = low (see Notes 20 and 21)	t_{SRS}	10		10		ns
$t_{d(SCSE)}$	Delay time, SC high to $\overline{SE}$ high in serial input mode		20		20		ns
$t_{d(RHSC)}$	Delay time, $\overline{RAS}$ high to SC high (see Note 21)	t_{SRD}	25		30		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 22)	t_{TRP}	$t_{w(RH)}$		$t_{w(RH)}$		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 22)	t_{TSD}	35		40		ns
$t_{d(SESC)}$	Delay time, $\overline{SE}$ low to SC high (see Note 23)	t_{SWS}	10		15		ns
$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8	ms
t_t	Transition time	t_T	3	50	3	50	ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 18. Memory to register (read) transfer cycles only.
19. In a transfer read cycle, the state of SC when $\overline{TRG}$ rises is a Don't Care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{TRG}$ goes high.
20. In a transfer write cycle, the state of SC when $\overline{RAS}$ falls is a Don't Care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{RAS}$ goes low.
21. Register to memory (write) transfer cycles reserved only.
22. Memory to register (read) and register to memory (write) transfer cycles only.
23. Serial data-in cycles only.

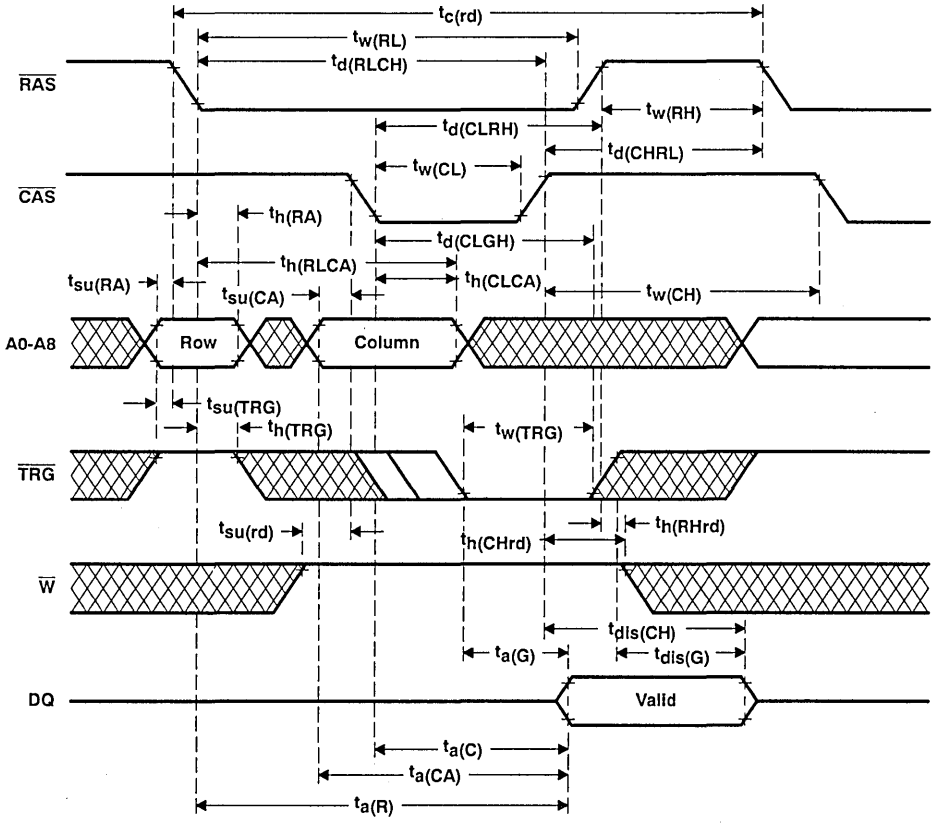
PARAMETER MEASUREMENT INFORMATION



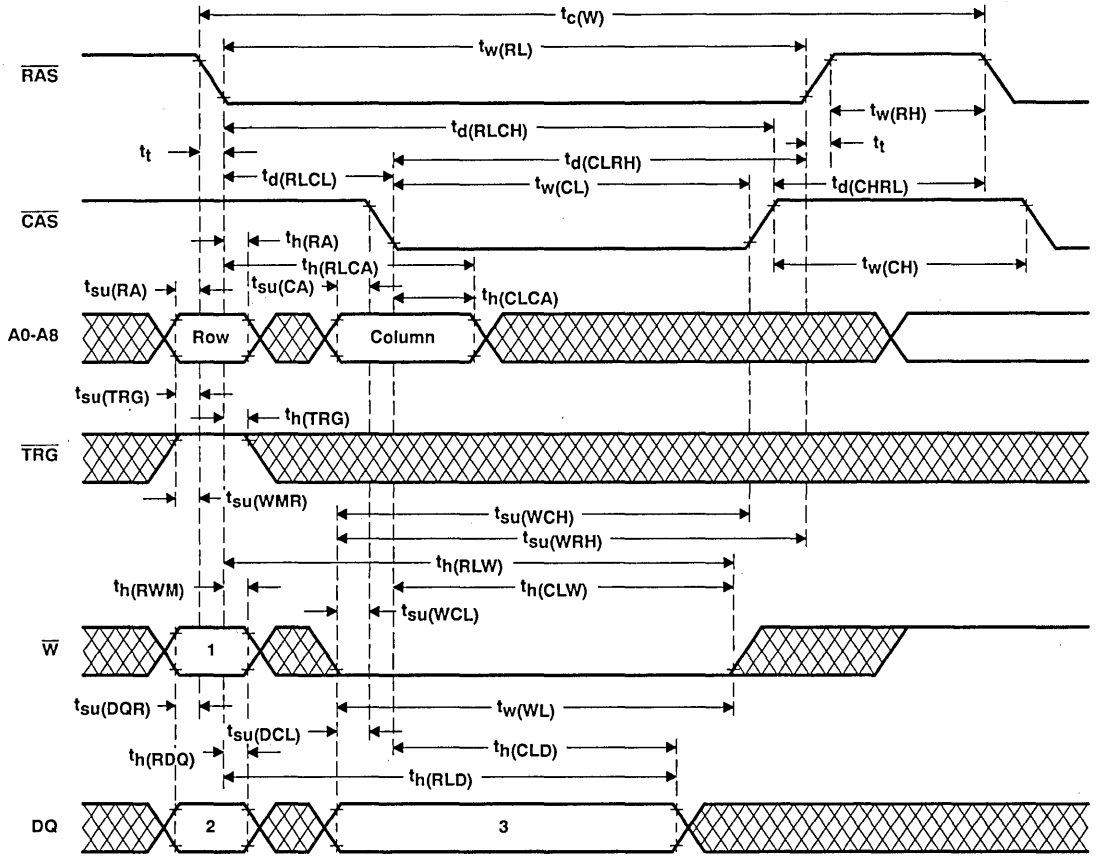
Load Circuit

Figure 2. Load Circuit

read cycle timing

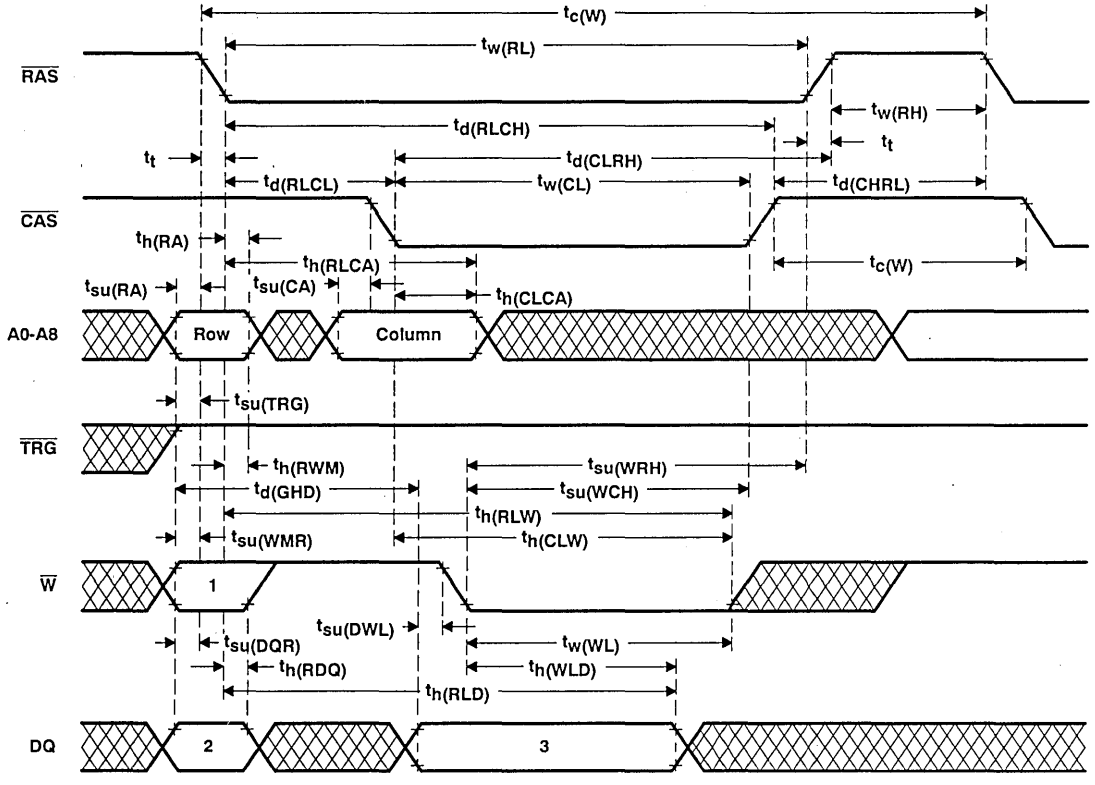


early write cycle timing



NOTE 24: See "Write Cycle State Table" for the logic state of "1", "2", and "3".

delayed write cycle timing

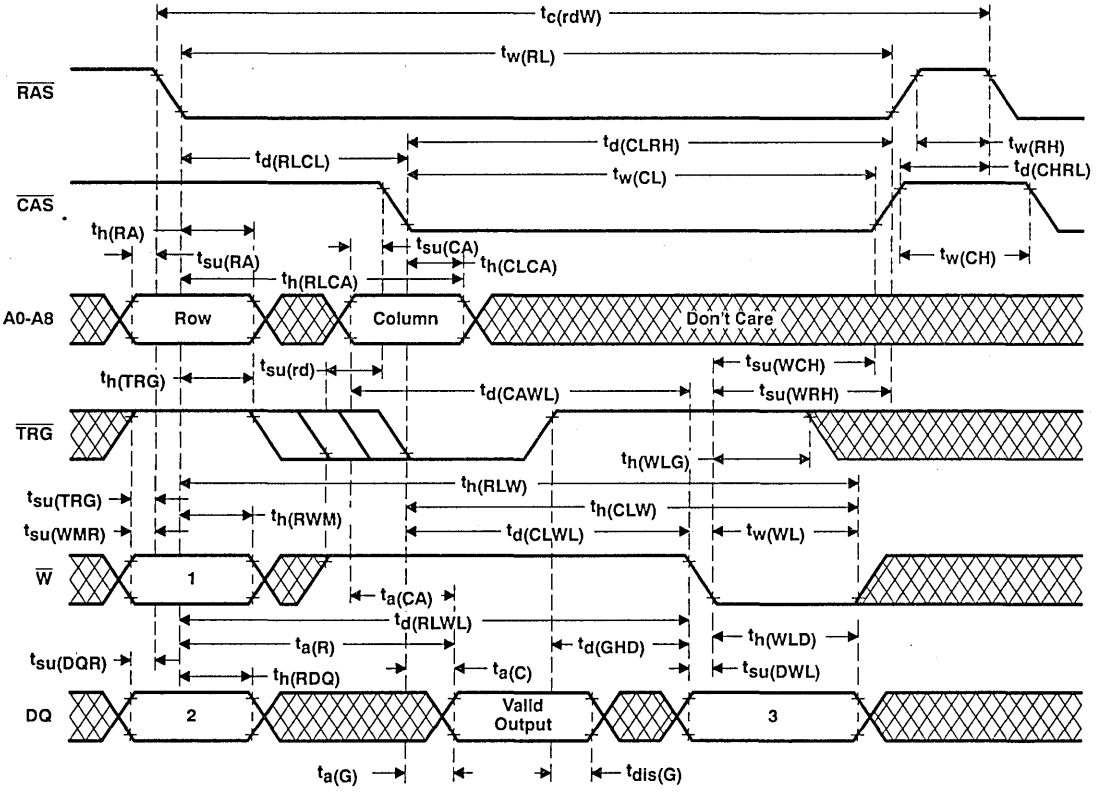


NOTE 24: See "Write Cycle State Table" for the logic state of "1", "2", and "3".

write cycle state table

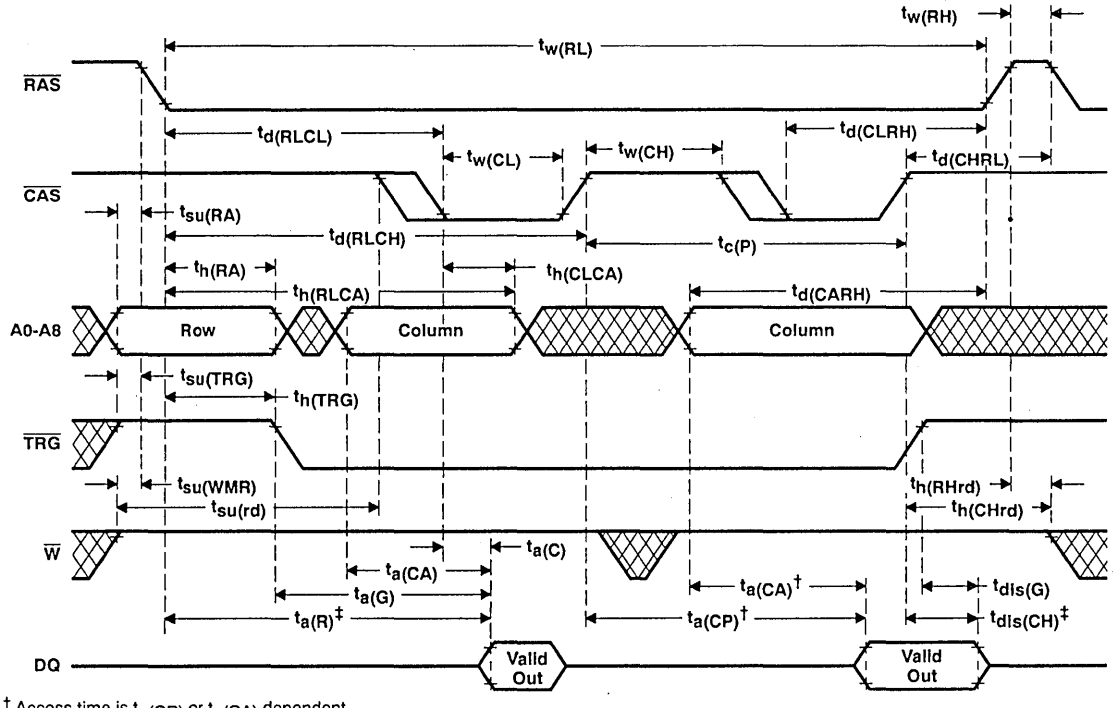
CYCLE	STATE		
	1	2	3
Write mask load/use Write DQs to I/Os	L	Write Mask	Valid Data
Normal early or late Write operation	H	Don't Care	Valid Data

read-write/read-modify-write cycle timing



NOTE 24: See "Write Cycle State Table" for the logic state of "1", "2", and "3". Same logic as delayed write cycle.

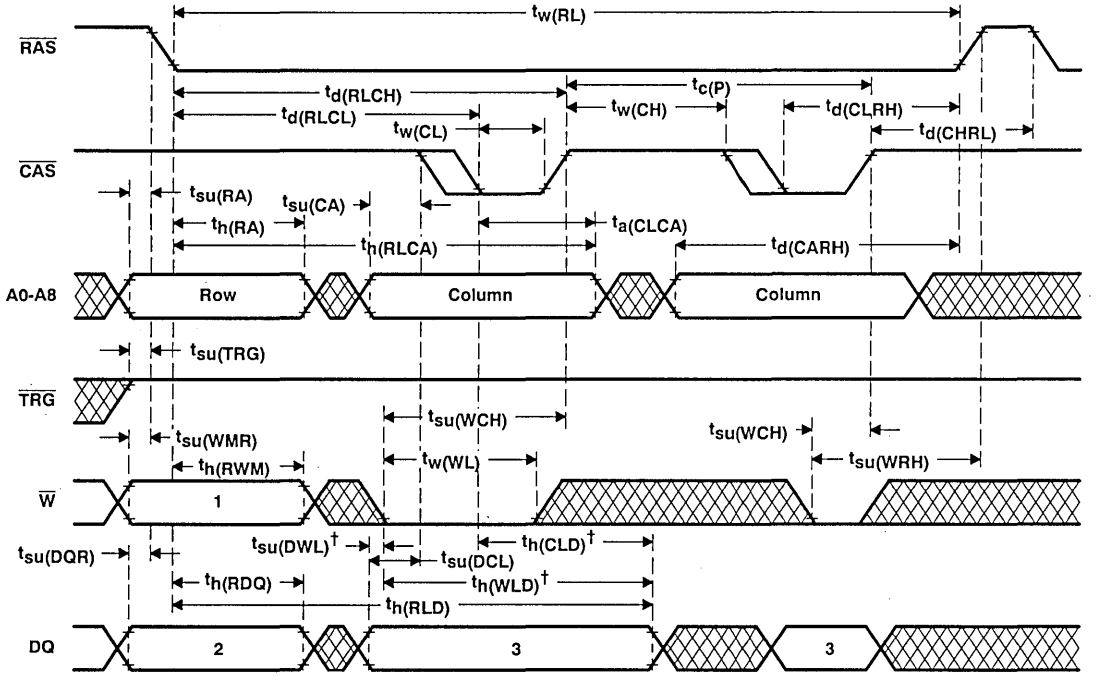
enhanced page-mode read cycle timing



† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
‡ Output may go from high-impedance state to an invalid data state prior to the specified access time.

NOTE 25: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.

enhanced page mode write cycle timing

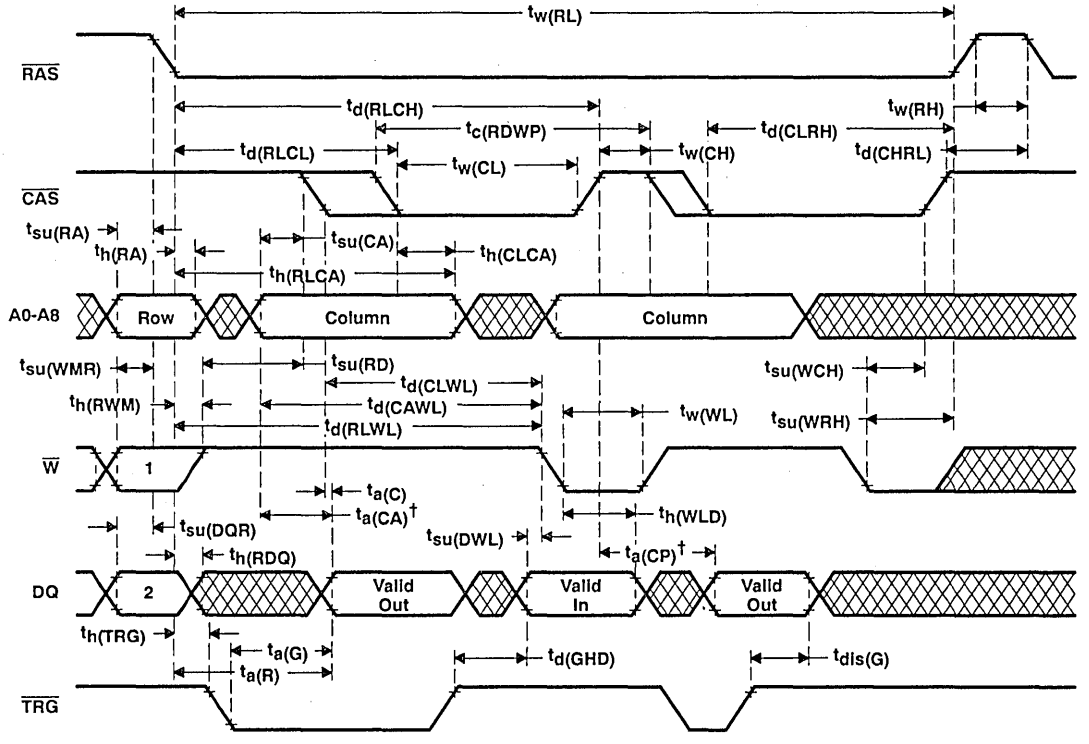


† Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

NOTES: 24. See "Write Cycle State Table" for the logic state of "1", "2", and "3".

26. A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used, to guarantee page-mode cycle time. If the early write cycle timing is used, the state of $\overline{TRG}$ is a Don't Care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

enhanced page-mode read-modify-write cycle timing

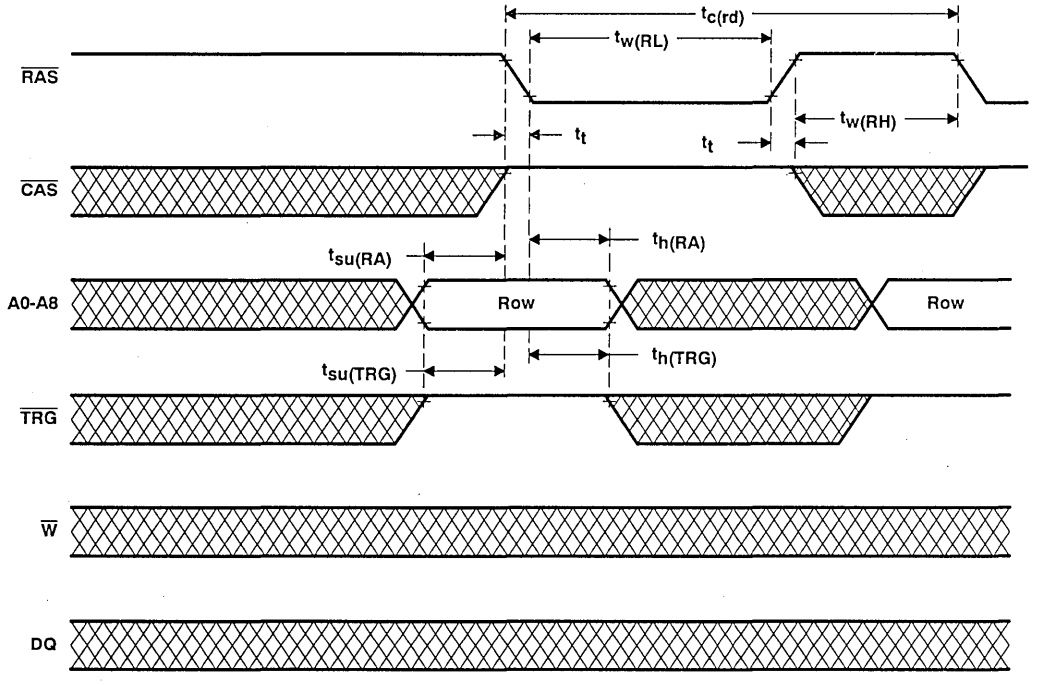


† Output may go from the high-impedance state to an invalid data state prior to the specified access time.

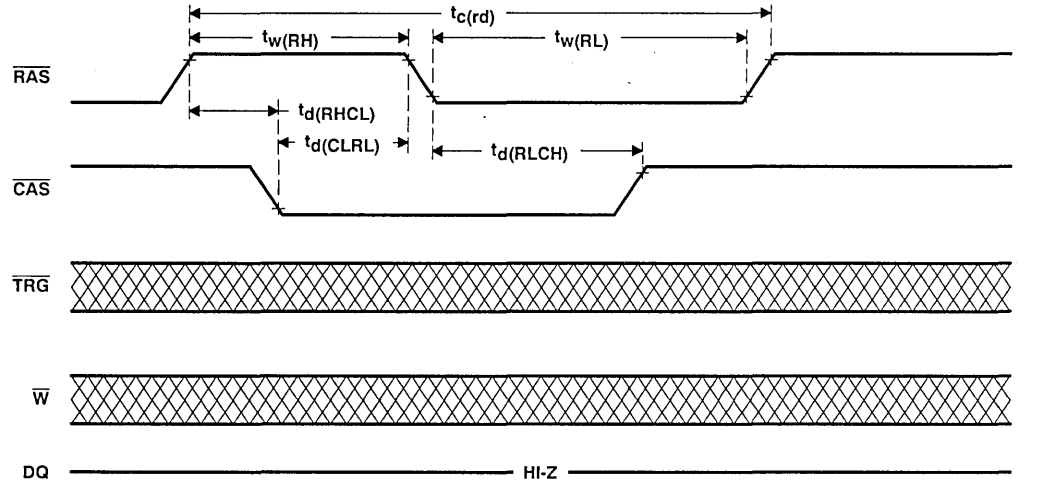
NOTES: 24. See "Write Cycle State Table" for the logic state of "1", "2", and "3".

27. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

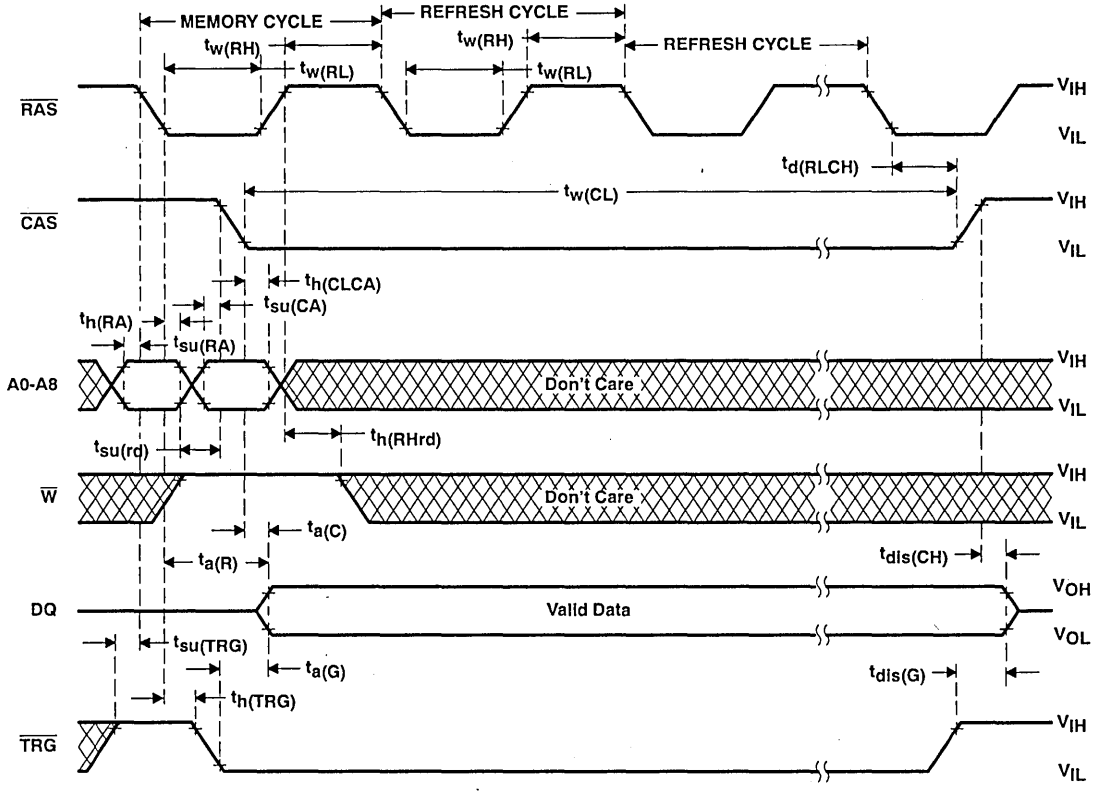
$\overline{\text{RAS}}$-only refresh timing



$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh

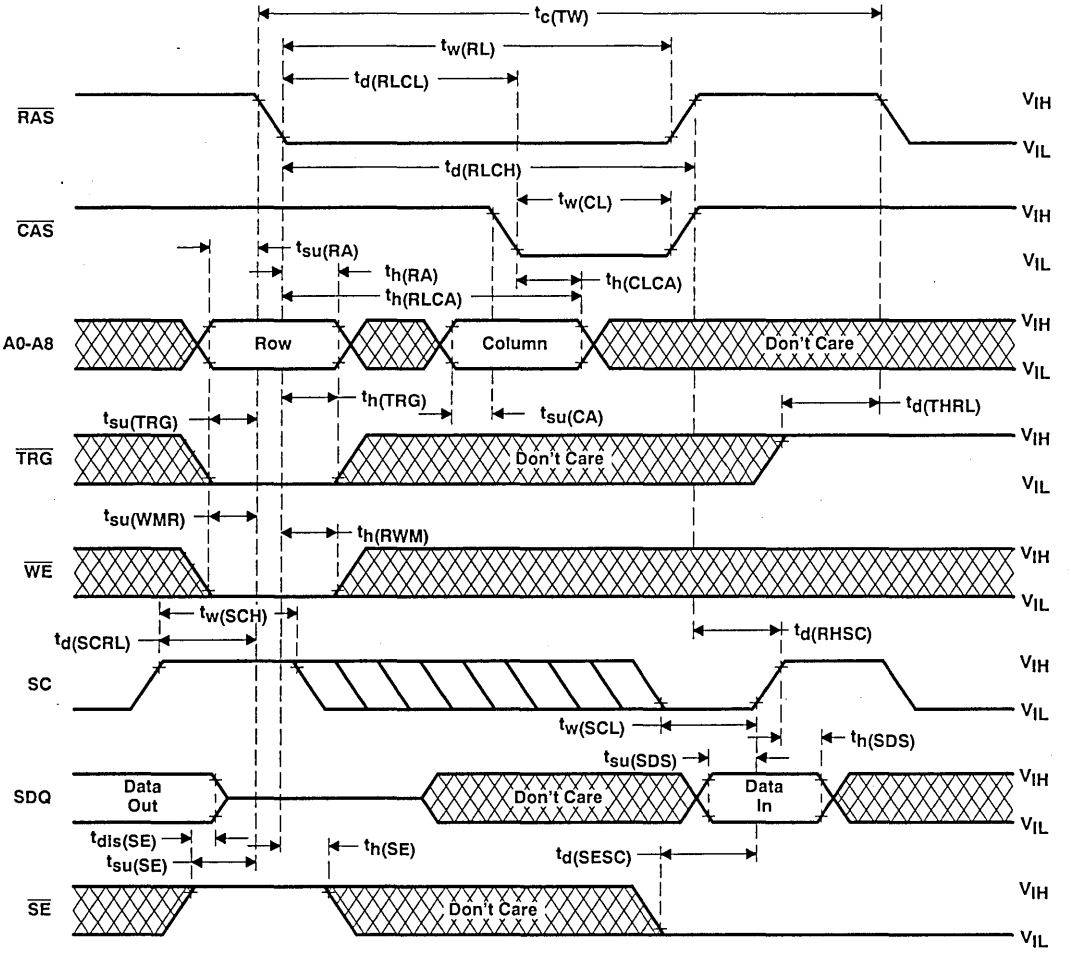


hidden refresh cycle timing



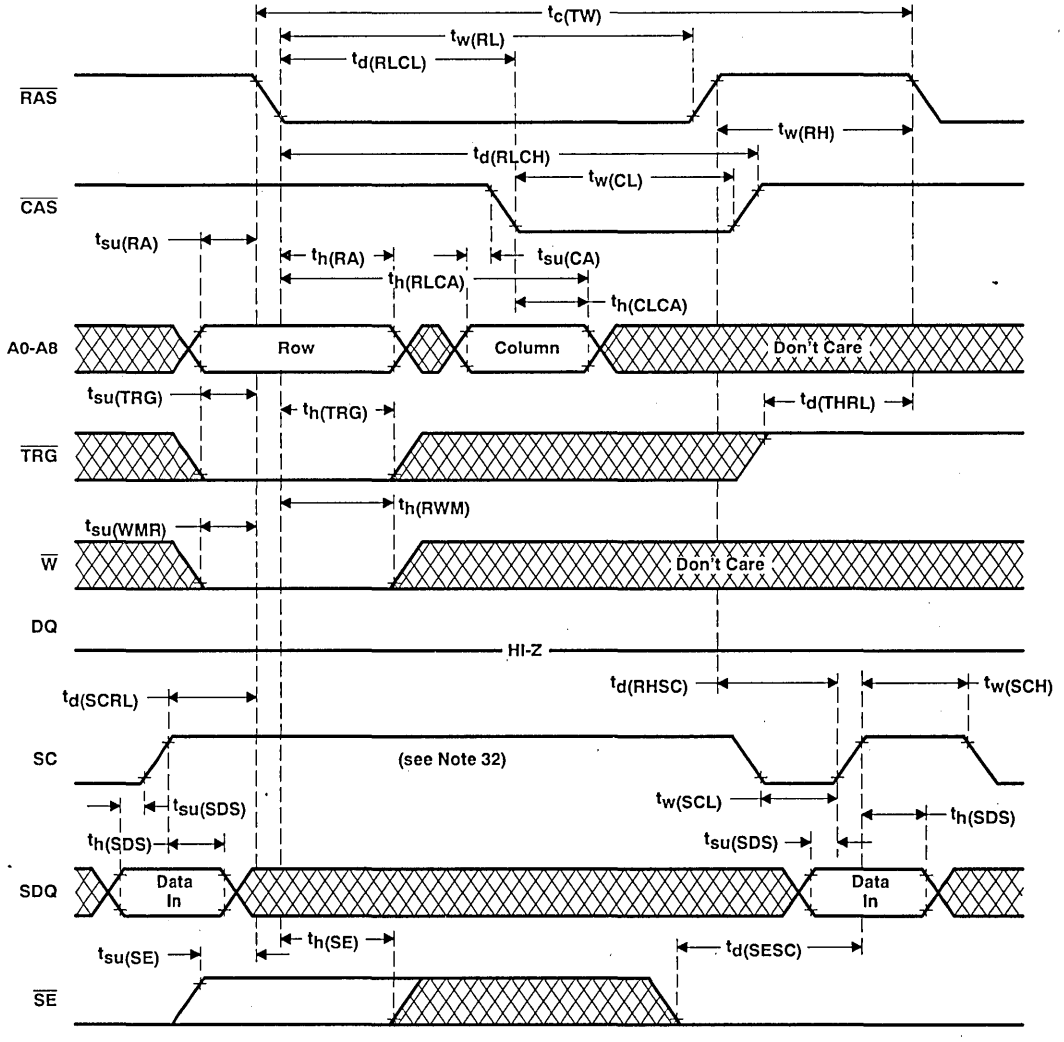
write-mode control pseudo write transfer timing

The write-mode control cycle is used to change the SDQs from the output mode to the input mode. This allows serial data to be written into the data register. The diagram below assumes that the device was originally in the serial read mode.



NOTES: 28. Random-mode Q outputs remain in the high-impedance state for the entire write-mode control.
29. $\overline{SE}$ must be high as $\overline{RAS}$ falls in order to perform a write-mode control cycle.

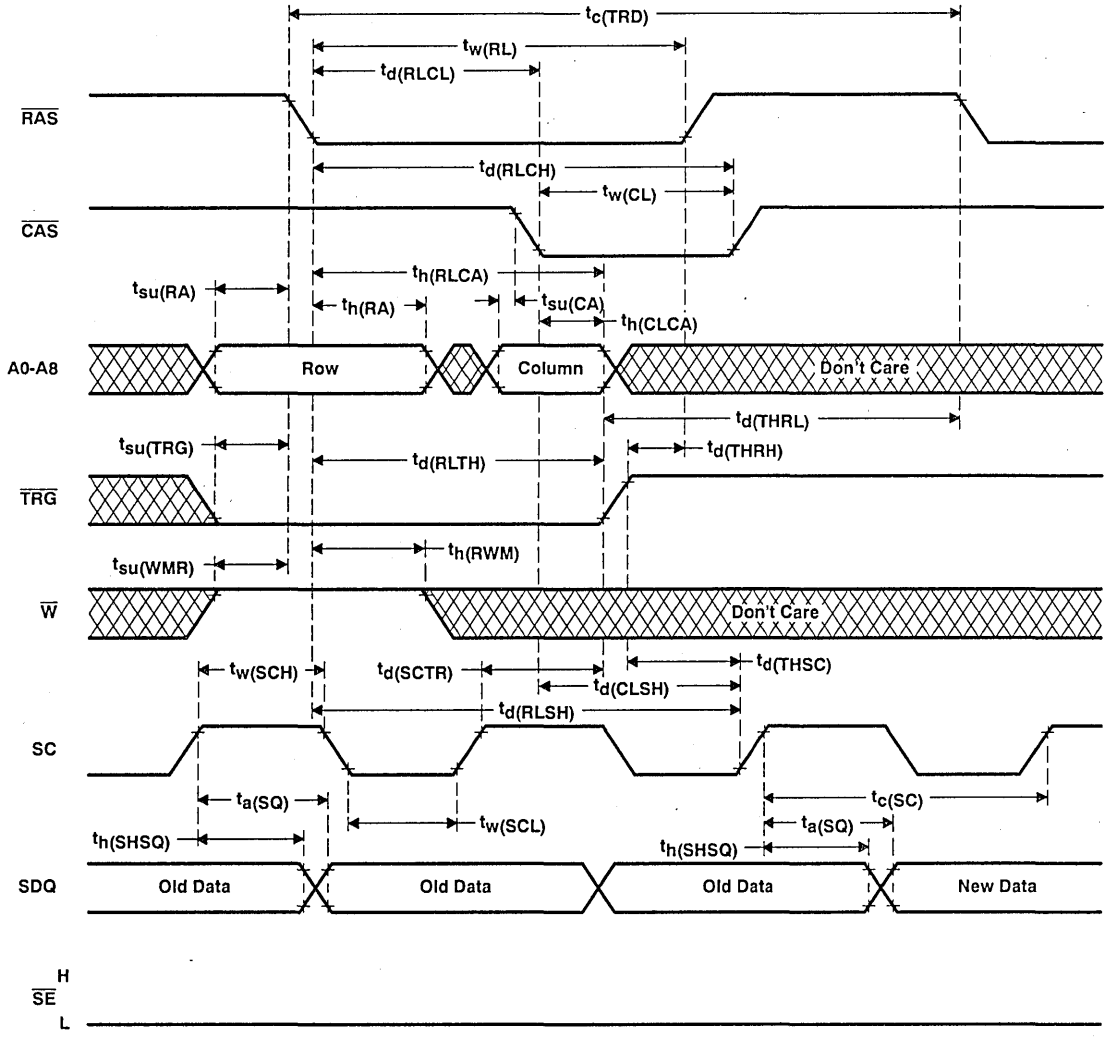
data register to memory timing, serial input enabled



NOTES: 30. Random mode Q outputs remain in the high-impedance state for the entire data register to memory transfer cycle. This cycle is used to transfer data from the data register to the memory array. Every one of the 512 locations in each data register is written into the corresponding 512 columns of the selected row. Data in the data register may proceed from a serial shift-in or from a parallel load from one of the memory array rows. The above diagram assumes that the device is in the serial write mode (i.e., SD is enabled by a previous write mode control cycle, thus allowing data to be shifted-in).

31. Successive transfer writes can be performed without serial clocks for applications requiring fast memory array clears.
32. SC transitions are not allowed between $\overline{RAS}$ low and $\overline{TRG}$ high.
33. For multiple transfer write operation; a transfer read cycle needs to be done from the same row after the first transfer write is carried out, then do multiple transfer write for subsequent rows.

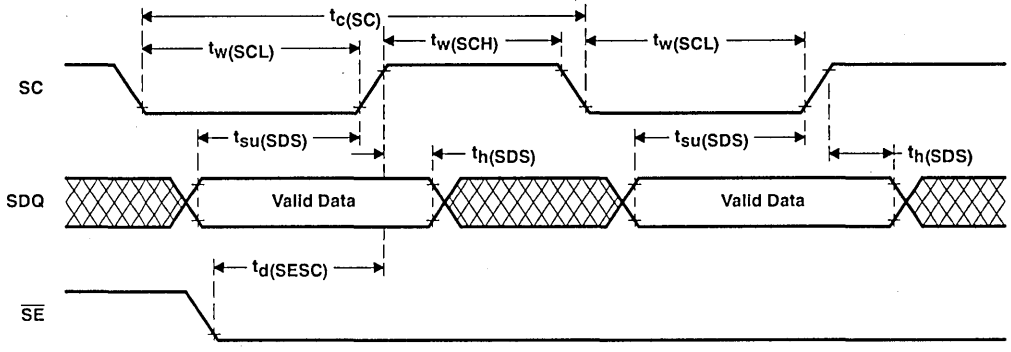
memory to data register transfer timing



NOTES: 34. Random mode (Q outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written into from the 512 corresponding columns of the selected row. The data that is transferred into the data registers may be either shifted out or transferred back into another row.

35. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

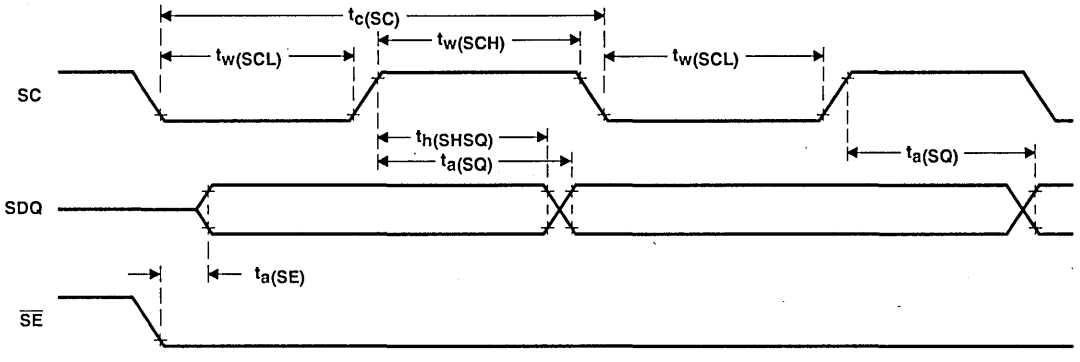
serial data-in timing



The serial data-in cycle (SD) is used to input serial data into the data registers. Before data can be written into the data registers via SD, the device must be put into the write mode by performing a write mode control, or pseudo-transfer, cycle. Transfer write cycles occurring between the write mode control cycle and the subsequent writing of data will take the device out of the write mode. However, a transfer read cycle during that time will take the device out of the write mode and put it into the read mode, thus disabling the input of data. Data will be written starting at the location specified by the input address loaded on the previous transfer cycle.

While accessing data in the serial data registers, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.

serial data-out timing



NOTES: 7. When the odd tap is used (tap addresses can be 0-511, and odd taps are 1,3,5 ... etc.), the cycle time for SC in serial data out cycle needs to be 50 ns minimum.

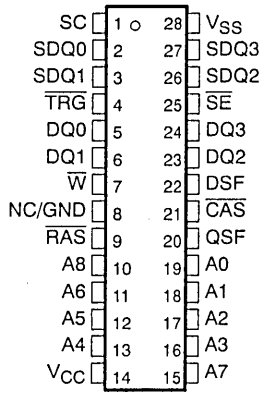
36. While reading data through the serial data register, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register to memory or memory to register data transfer operation.

The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle. Transfer write cycles occurring between the transfer read cycle and the subsequent shifting out of data will not take the device out of the read mode. But a write mode control cycle at that time will take the device out of the read mode and put it in the write mode, thus not allowing the reading of data.

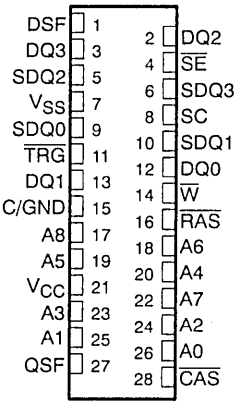
This Data Sheet Is Applicable to All TMS44C251s Symbolized With Revision "I" and Subsequent Revisions as Described on Page 8-71.

- **DRAM: 262 144 Words × 4 Bits**
  SAM: 512 Words × 4 Bits
- **Dual Port Accessibility — Simultaneous and Asynchronous Access from the DRAM and SAM Ports**
- **Bidirectional Data Transfer Function Between the DRAM and the Serial Data Register**
- **4 × 4-Block Write Feature for Fast Area Fill Operations. As Many as Four Memory Address Locations Written Per Cycle From an On-Chip Color Register**
- **Write-Per-Bit Feature for Selective Write to Each RAM I/O. Two Write-Per-Bit Modes to Simplify System Design**
- **Enhanced Page Mode Operation for Faster Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ and Hidden Refresh Modes**
- **RAM Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design**
- **Long Refresh Period . . . Every 8 ms (Max)**
- **DRAM Port Is Compatible with the TMS44C256**
- **Up to 33 MHz Uninterrupted Serial Data Streams**
- **Split Serial Data Register for Simplified Realtime Register Reload**
- **3-State Serial I/Os Allow Easy Multiplexing of Video Data Streams**
- **512 Selectable Serial Register Starting Locations**
- **All Inputs and Outputs TTL Compatible**
- **Texas Instruments EPIC™ CMOS Process**

DZ Package†
(Top View)



SD Package†
(Top View)



†The packages shown here are for pinout reference only and are not drawn to scale.

PIN NOMENCLATURE

A0-A8	Address Inputs
$\overline{CAS}$	Column Enable
DQ0-DQ3	DRAM Data In-Out/Write Mask Bit
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row Enable
SC	Serial Data Clock
SDQ0-SDQ3	Serial Data In-Out
$\overline{TRG}$	Transfer Register/Q Output Enable
$\overline{W}$	Write Mask Select/Write Enable
DSF	Special Function Select
QSF	Split-Register Activity Status
V_{CC}	5-V Supply
V_{SS}	Ground
NC/GND	No Connect/Ground (Important: not connected to internally to V_{SS})

- **Performance Ranges:**

V_{CC} ± 5%

	ACCESS TIME ROW ADDRESS (MAX) $t_{a(R)}$	ACCESS TIME COLUMN ENABLE (MAX) $t_{a(C)}$	ACCESS TIME SERIAL DATA (MAX) $t_{a(SQ)}$	ACCESS TIME SERIAL ENABLE (MAX) $t_{a(SE)}$
TMS44C251-1	100 ns	25 ns	30 ns	20 ns

V_{CC} ± 10%

TMS44C251-10	100 ns	25 ns	30 ns	20 ns
TMS44C251-12	120 ns	30 ns	35 ns	25 ns

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description

The TMS44C251 multiport video RAM is a high speed, dual ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 4 bits each interfaced to a serial data register, or Serial Access Memory (SAM), organized as 512 words of 4 bits each. The TMS44C251 supports three basic types of operation: random access to and from the DRAM, serial access to and from the serial register, and bidirectional transfer of data between any row in the DRAM and the serial register. Except during transfer operations, the TMS44C251 can be accessed simultaneously and asynchronously from the DRAM and SAM ports. During transfer operations, the 512 columns of the DRAM are connected to the 512 positions in the serial data register. The 512 × 4 bit serial data register can be loaded from the memory row (transfer read), or else the contents of the 512 × 4 bit serial data register can be written to the memory row (transfer write).

The TMS44C251 is equipped with several features designed to provide higher system-level bandwidth and simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's 4 × 4 Block Write mode. The Block Write mode allows four bits of data present in an on-chip color data register to be written to any combination of four adjacent column address locations. As many as 16 bits of data can be written to memory during each $\overline{CAS}$ cycle time. Also on the DRAM port, a write mask register provides a persistent write-per-bit mode without repeated mask loading.

On the serial register, or SAM port, the TMS44C251 offers a split-register transfer read (DRAM to SAM) option, which enables realtime register reload implementation for truly continuous serial data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. This new realtime register reload implementation allows truly continuous serial data. For applications not requiring realtime register reload (for example, reloads done during CRT retrace periods), the single register mode of operation is retained to simplify design. The SAM can also be configured in input mode, accepting serial data from an external device. Once the serial register within the SAM is loaded, its contents can be transferred to the corresponding column positions in any row in memory in a single memory cycle.

The SAM port is designed for maximum performance. Data can be input to or accessed from the SAM at serial rates up to 33 MHz. During a split-register mode of operation, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate open-drain output, designated QSF, is included to indicate which half of the serial register is active at any given time in the split register mode.

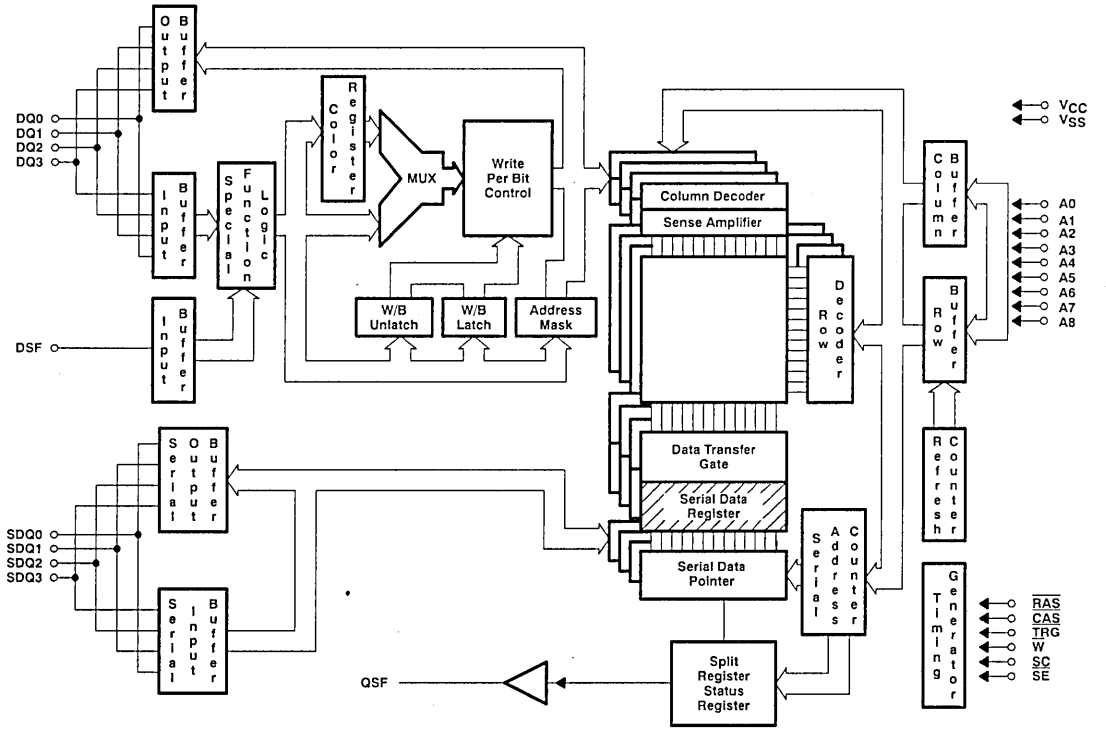
All inputs, outputs, and clock signals on the TMS44C251 are compatible with Series 74 TTL. All address lines and data-in are latched on-chip to simplify system design. All data-outs are unlatched to allow greater system flexibility.

The TMS44C251 employs state-of-the-art Texas Instruments EPIC™ scaled-CMOS, double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The TMS44C251 is offered in a 28-pin small-outline J-lead package (DZ suffix) for direct surface mounting in rows on 400-mil (5,08-mm) centers. It is also offered in a 400-mil, 28-pin zig-zag in-line package (SD suffix). Both packages are characterized for operation from 0°C to 70°C (L suffix).

The TMS44C251 and other Multiport Video RAMs are supported by a broad line of graphics processor and control devices from Texas Instruments, including the TMS34020 Graphics System Processor.

functional block diagram



Detailed Pin Description vs Operational Mode

PIN	DRAM	TRANSFER	SAM
A0-A8	Row, Column Address	Row, Tap Address	
$\overline{CAS}$	Column Enable, Output Enable	Tap Address Strobe	
DQi	DRAM Data I/O, Write Mask Bits		
DSF	Block Write Enable	Split-Register Enable	
	Persistent Write-per-Bit Enable	Alternate Write Transfer Enable	
	Color Register Load Enable		
	Write-per-Bit Mask Load Enable		
$\overline{RAS}$	Row Enable	Row Enable	
$\overline{SE}$		Serial-In Mode Enable	Serial Enable
SC			Serial Clock
SDQi			Serial Data I/O
$\overline{TRG}$	Q Output Enable	Transfer Enable	
$\overline{W}$	Write Enable, Write-per-Bit Select	Transfer Write Enable	
QSF			Split Register Active Status
V_{CC}	5-V Supply (typical)		
V_{SS}	Device Ground		
NC/GND	Make No External Connection or Tie to System Ground		

operation

random-access operation

Refer to Table 1, Function Table, for Random-Access and Transfer Operations. Random-access operations are denoted by the designator "R" and transfer operations are denoted by a "T".

transfer register select and DQ enable ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either register or random-access operation as $\overline{RAS}$ falls. For the random-access (DRAM) mode, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. Asserting $\overline{TRG}$ high as $\overline{RAS}$ falls causes the 512 storage elements of each data register to remain disconnected from the corresponding 512-bit lines of the memory array. (Asserting $\overline{TRG}$ low as $\overline{RAS}$ falls connects the 512-bit positions in the serial register to the bit lines and indicates that a transfer will occur between the data registers and the selected memory row. See "Transfer Operation" for details.)

During random-access operations, $\overline{TRG}$ also functions as an output enable for the random (Q) outputs. Whenever $\overline{TRG}$ is held high, the Q outputs are in the high-impedance state to prevent an overlap between the address and DRAM data. This organization allows the connection of the address lines to the data I/O lines but prohibits the use of the early write cycle. It also allows read-modify-write cycles to be performed by providing a three-state condition to the common I/O pins so that write data can be driven onto the pins after output read data has been externally latched.

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Then, the nine column address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

$\overline{RAS}$ and $\overline{CAS}$ address strobes and device control clocks

$\overline{RAS}$ is a control input that latches the states of the row address, $\overline{W}$, $\overline{TRG}$, $\overline{SE}$, $\overline{CAS}$, and DSF onto the chip to invoke the various DRAM and Transfer functions of the TMS44C251. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is a control input that latches the states of the column address and DSF to control various DRAM and Transfer functions. $\overline{CAS}$ also acts as an output enable for the DRAM output pins.

special function select (DSF)

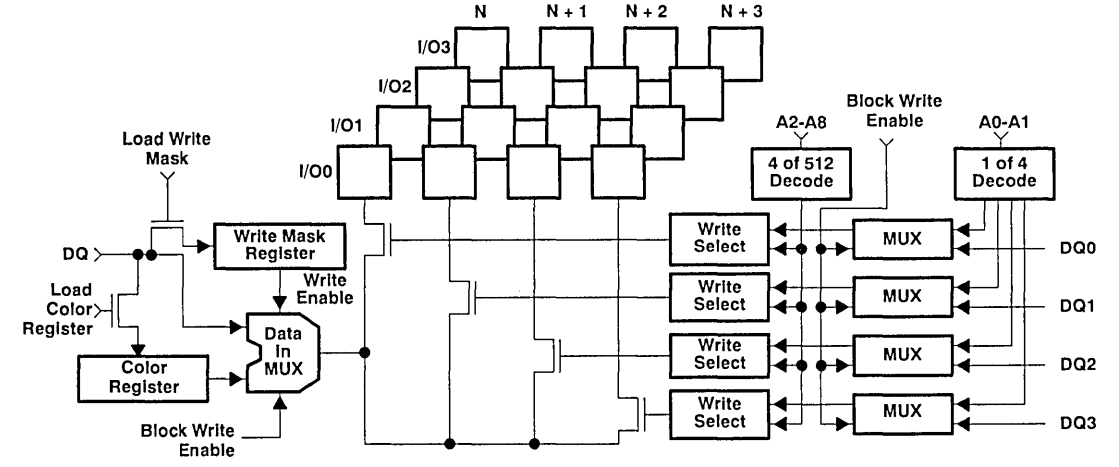
The Special Function Select input is latched on the falling edges of $\overline{RAS}$ and $\overline{CAS}$, similarly to an address, and serves four functions. First, during write cycles DSF invokes persistent write-per-bit operation. If $\overline{TRG}$ is high, $\overline{W}$ is low, and DSF is low on the falling edge of $\overline{RAS}$, the write mask will be reloaded with the data present on the DQ pins. If DSF is high, the mask will not be reloaded but will retain the data from the last mask reload cycle.

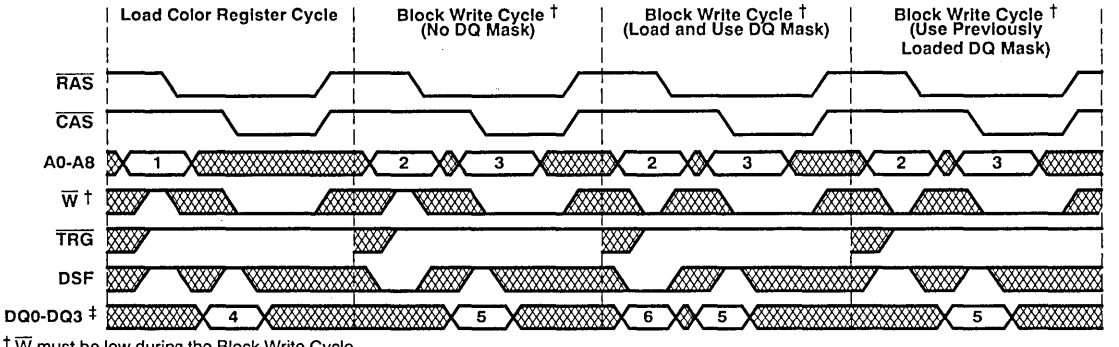
Second, DSF is used to change the internally stored write-per-bit mask register (or write mask) via the load write mask cycle. The data present on the DQ pins when $\overline{W}$ falls is written to the write mask rather than to the addressed memory location. See "Delayed Write Cycle Timing" and the accompanying "Write Cycle State Table" in the timing diagram section. Once the write mask is loaded, it can be used on subsequent masked write-per-bit cycles. This feature allows systems with a common address and data bus to use the write-per-bit feature, eliminating the time needed for multiplexing the write mask and input data on the data bus.

Third, DSF is used to load an on-chip four-bit data, or "color", register via the Load Color Register cycle. The contents of this register can subsequently be written to any combination of four adjacent column memory locations using the 4 × 4-Block Write feature. The load color register cycle is performed using normal write cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Once the color register is loaded, it retains data until power is lost or until another load color register cycle is performed.

After loading the color register, the block write cycle can be enabled by holding DSF high on the falling edge of $\overline{CAS}$. During block write cycles, only the seven most significant column addresses (A2-A8) are latched on the falling edge of $\overline{CAS}$. The two least significant addresses (A0-A1) are replaced by the four DQ bits, which are also latched on the later of $\overline{CAS}$ or $\overline{W}$ falling. These four bits are used as an address mask and indicate which of the four column address locations addressed by A2-A8 will be written with the contents of the color register during the write cycle, and which ones will not. DQ0 enables a write to column address A1 is low, A0 is low; DQ1 enables a write to A1 is low, A0 is high; DQ2 enables a write to A1 is high, A0 is low; and DQ3 enables a write to A1 is high, A0 is high. A logic high level enables a write and a logic low level disables the write. A maximum of 16 bits can be written to memory during each $\overline{CAS}$ cycle (see Figure 1, Block Write Diagram).

Fourth, the DSF pin is used to invoke the split-register transfer and serial access operation, described in the sections "Transfer Operation" and "Serial Operation".





† $\overline{W}$ must be low during the Block Write Cycle.
‡ DQ0-DQ3 ($\overline{CAS}$) are latched on the later of $\overline{W}$ or $\overline{CAS}$ falling edge. DQ0-DQ3 ($\overline{RAS}$) are latched on $\overline{RAS}$ falling edge.
Legend:

1. Refresh Address
2. Row Address
3. Block Address (A2-A8)
4. Color Register Data
5. Column Mask Data
6. DQ Mask Data

= Don't Care

Figure 1. Block Write Diagram

write enable, write-per-bit enable ($\overline{W}$)

The $\overline{W}$ pin enables data to be written to the DRAM and is also used to select the DRAM write-per-bit mode of operation. A logic level high on the $\overline{W}$ input selects the read mode and a logic low level selects the write mode. In an early write cycle, $\overline{W}$ is brought low before $\overline{CAS}$, and the DRAM output pins (DQ) remain in the high-impedance state for the entire cycle. During DRAM write cycles, holding $\overline{W}$ low on the falling edge of $\overline{RAS}$ will invoke the write-per-bit operation. Two modes of write-per-bit operation are supported.

Case 1. If DSF is low on the falling edge of $\overline{RAS}$, the write mask is reloaded. Accordingly, a four-bit binary code (the write-per-bit mask) is input to the device via the random DQ pins and is latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the four random I/Os are written and which are not. After $\overline{RAS}$ has latched the write mask on-chip, input data is driven onto the DQ pins and is latched on the falling edge of the later of $\overline{CAS}$ or $\overline{W}$. If a low was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will not be written to that I/O. If a high was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will be written to that I/O.

Case 2. If DSF is high on the falling edge of $\overline{RAS}$, the mask is not reloaded from the DQ pins but instead retains the value stored during the last write-per-bit mask reload. This mode of operation is known as Persistent Write-per-Bit, since the write-per-bit mask is persistent over an arbitrary number of cycles.

See the corresponding timing diagrams for details.

IMPORTANT: The write-per-bit operation is invoked only if $\overline{W}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{W}$ is held high on the falling edge of $\overline{RAS}$, write-per-bit is not enabled and the write operation is identical to that of standard × 4 DRAMs.

data I/O (DQ0-DQ3)

DRAM data is written during a write or read-modify-write cycle. The falling edge of $\overline{W}$ strobes data into the on-chip data latches. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with data setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low. Thus, the data will be strobed-in by $\overline{W}$ with data setup and hold times referenced to this signal.

The three-state output buffers provide direct TTL compatibility (no pullup resistors required) with a fanout of two Series 74 TTL loads. Data-out is the same polarity as data-in. The outputs are in the high impedance (floating) state as long as $\overline{CAS}$ or $\overline{TRG}$ is held high. Data will not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low. Once the outputs are valid, they remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. $\overline{CAS}$ or $\overline{TRG}$ going high returns the outputs to a high-impedance state. In an early write cycle, the outputs are always in the high-impedance state. In a register transfer operation (memory to register or register to memory), the outputs remain in the high-impedance state for the entire cycle.

enhanced page mode

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows theTMS44C251 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

Enhanced page mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row address setup, row address hold, and address multiplex is thus eliminated, and a memory cycle time reduction of up to 3 × can be achieved, compared to minimum $\overline{RAS}$ cycle times. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and page mode cycle time used. The TMS44C251 allows a full page (512 cycles) of information to be accessed in read, write, or read-modify-write mode during a single $\overline{RAS}$ low period using relatively conservative page mode cycle times.

During write-per-bit operations, the DQ pins are used to load the write-per-bit mask register using either mode of write-per-bit operation described above under the $\overline{W}$ pin description.

During block write operations, the DQ pins are used to load the on-chip color register during the load color register cycle and are also used as a write enable during block write cycles.

refresh

A refresh operation must be performed to each row at least once every eight milliseconds to retain data. Since the output buffer is in the high-impedance state (unless $\overline{CAS}$ is applied), the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$. The external row address is ignored and the refresh address is generated internally.

NC/GND

This pin is reserved for the manufacturer's test operation. It is an input and should be tied to system ground or left floating for proper device operation.

IMPORTANT: NC/GND is not connected internally to V_{SS}.

Table 1. Function Table

TYPE†	RAS FALL					CAS FALL	ADDRESS		DQ0-3		FUNCTION
	CAS	TRG	W¶	DSF	SE	DSF	RAS	CAS	RAS	CAS‡ W	
R	L	X§	X	X	X	X	X	X	X	X	CAS-Before-RAS Refresh
T	H	L	L	X	L	X	Row Addr	Tap Point	X	X	Register to Memory Transfer (Transfer Write)
T	H	L	L	H	X	X	Row Addr	Tap Point	X	X	Alternate Transfer Write (Independent of SE)
T	H	L	L	L	H	X	Refresh Addr	Tap Point	X	X	Serial Write-Mode Enable (Pseudo-Transfer Write)
T	H	L	H	L	X	X	Row Addr	Tap Point	X	X	Memory To Register Transfer (Transfer Read)
T	H	L	H	H	X	X	Row Addr	Tap Point	X	X	Split Register Transfer Read (Must Reload Tap)
R	H	H	L	L	X	L	Row Addr	Col Addr	Write Mask	Valid Data	Load and Use Write Mask, Write Data to DRAM
R	H	H	L	L	X	H	Row Addr	Col A2-A8	Write Mask	Addr Mask	Load and Use Write Mask, Block Write to DRAM
R	H	H	L	H	X	L	Row Addr	Col Addr	X	Valid Data	Persistent Write-per-Bit, Write Data to DRAM
R	H	H	L	H	X	H	Row Addr	Col A2-A8	X	Addr Mask	Persistent Write-per-Bit, Block Write to DRAM
R	H	H	H	L	X	L	Row Addr	Col Addr	X	Valid Data	Normal DRAM Read/Write (Non-Masked)
R	H	H	H	L	X	H	Row Addr	Col A2-A8	X	Addr Mask	Block Write to DRAM (Non-Masked)
R	H	H	H	H	X	L	Refresh Addr	X	X	Write Mask	Load Write Mask
R	H	H	H	H	X	H	Refresh Addr	X	X	Color Data	Load Color Register

† R = Random access operation; T = Transfer operation.
‡ DQ0-3 are latched on the later of W or CAS falling edge.
§ X = Don't care.
¶ In persistent write-per-bit function, W must be high during the refresh cycles.
Addr Mask = 1; write to address location enabled.
Write Mask = 1; write to I/O enabled.

random port to serial port interface

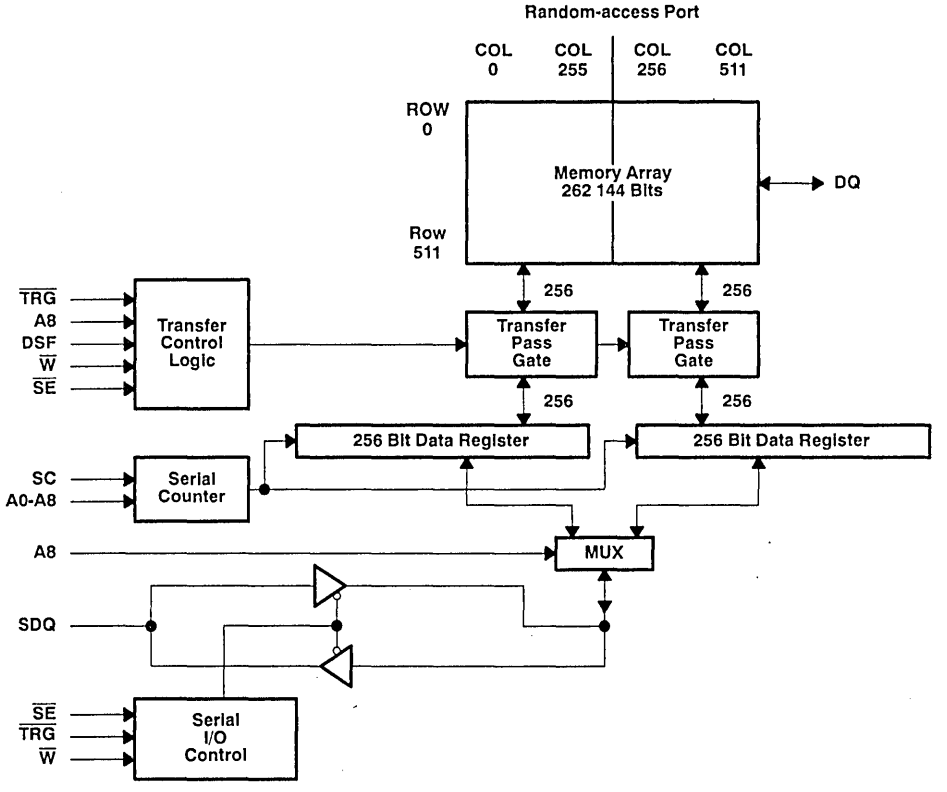


Figure 2. Block Diagram Showing One Random and One Serial I/O Interface

random-address space to serial-address space mapping

The 512 bits in each of the four data registers of the SAM are connected to the 512 column locations of each of the four random I/Os. Data can be accessed in or out of the SAM starting at any of the 512 data bit locations. This start location is selected by addresses A0 through A8 on the falling edge of $\overline{CAS}$ during any transfer cycle. The SAM is accessed starting from the selected start address, proceeding from the lowest to the highest significant bits. After the most significant bit position (511) is accessed, the serial counter wraps around such that bit 0 is accessed on the next clock pulse. The selected start address is stored and used for all subsequent transfer cycles until $\overline{CAS}$ is again brought low during any transfer cycle. Thus, the start address can be set once and $\overline{CAS}$ held high during all subsequent transfer cycles and the start address point will not change regardless of data present on A0 through A8.

split-register mode random-address to serial address-space mapping

In split-register transfer operations, the serial data register is split into halves, the low half containing bits 0 through 255 and the high half containing bits 256 through 511. When a split-register transfer cycle is performed, the tap address must be strobed in on the falling edge of $\overline{CAS}$. The most significant column address bit (A8) determines which register half will be reloaded from the memory array. The eight remaining column address bits (A0-A7) are used to select the SAM starting location for the register half selected by A8.

To insure proper operation when using the split-register read transfer feature, a non-split-register transfer must precede any split-register sequence. The serial start address must be supplied for every split-register transfer. (See Split Register Operating Sequence on page 8-69.)

transfer operations

As illustrated in Table 1, the TMS44C251 supports five basic transfer modes of operation:

1. Normal Write Transfer (SAM to DRAM)
2. Alternate Write Transfer (independent of the state of $\overline{SE}$)
3. Pseudo Write Transfer (Switches serial port from serial-out mode to serial-in mode. No actual data transfer takes place between the DRAM and the SAM.)
4. Normal Read Transfer (Transfer entire contents of DRAM to SAM)
5. Split-Register Read Transfer (Divides the SAM into a high and a low half. Only one half is transferred to the SAM while the other half is read from the serial I/O port.)

NOTES: A. All transfer write operations will switch the SDQ pins into the input (write) mode. Before data can be clocked into the serial port via the SDQ pins and SC serial clock, it is necessary to switch the SDQ pins into input mode via a previous transfer write operation.

B. *Pseudo Transfer Write Mode* has the same meaning as the term "Write Mode Control Cycle" as used in some VRAM data sheets. Both modes, or control cycles, serve to switch the direction of the SDQs without an actual data transfer taking place.

C. All transfer read operations will switch the SDQ pins into the output (read) operation

D. All transfer read operations and the pseudo transfer write operation perform a memory refresh on the selected row.

Table 2. Transfer Operation Logic

$\overline{TRG}$	$\overline{W}$	$\overline{SE}$	DSF	MODE
L	L	L	X	Register to memory (write) transfer, serial write mode enable
L	L	X	H	Alternate register to memory transfer, serial write mode enable
L	L	H	L	Pseudo write transfer, serial write mode enable
L	H	X	L	Memory to register (read) transfer
L	H	X	H	Split-register read transfer

NOTE: Above logic states are assumed valid on the falling edge of $\overline{RAS}$.

transfer register select ($\overline{TRG}$)

Transfer operations between the memory array and the data registers are invoked by bringing $\overline{TRG}$ low before $\overline{RAS}$ falls. The states of $\overline{W}$, $\overline{SE}$, and DSF, which are also latched on the falling edge of $\overline{RAS}$, determine which transfer operation will be invoked. (See Table 2.)

During read transfer cycles, $\overline{TRG}$ going high causes the addressed row of data to be transferred into the data register. Although the previous data in the data register is overwritten, the last bit of data appearing at SDQ before $\overline{TRG}$ goes high will remain valid until the first positive transition of SC after $\overline{TRG}$ goes high. The data at SDQ will then switch to new data beginning from the selected start, or *tap*, position.

transfer write enable ($\overline{W}$)

In any transfer operation, the state of $\overline{W}$ while $\overline{RAS}$ falls determines whether a read or write transfer will occur. To invoke any of the three possible write transfer operations, modes 1, 2, or 3 above, $\overline{W}$ must be low when $\overline{RAS}$ falls. If $\overline{W}$ is high when $\overline{RAS}$ falls, the transfer operation will be a read transfer (mode 4 or 5 above).

serial enable ($\overline{SE}$)

The serial enable pin has two functions, one that controls the transfer operations and one that controls the serial access operation.

For transfer operation, $\overline{SE}$ is latched together with DSF on the falling edge of $\overline{RAS}$ during any transfer write operation, i.e. when $\overline{TRG}$ and $\overline{W}$ are low when $\overline{RAS}$ falls (see Table 2):

- If $\overline{SE}$ is low at that time, a regular transfer write operation will occur.
- If $\overline{SE}$ is high and DSF is low at that time, a pseudo write transfer will occur, i.e. the SDQ pins will be switched from output to input mode without any data transfer from register to memory.
- If DSF is high, then an alternate register to memory transfer will occur, i.e. the state of $\overline{SE}$ is don't care.

column enable ($\overline{CAS}$)

If $\overline{CAS}$ is brought low during a transfer cycle, the address present on the pins A0 through A8 will become the new register start location. If $\overline{CAS}$ is held high during a control cycle, the previous tap address will be retained from the last transfer cycle in which $\overline{CAS}$ went low to set the tap address.

addresses (A0 through A8)

Nine address bits are required to select one of the 512 possible rows involved in the transfer of data to or from the data registers. The states of A0-A8 are latched on the fallling edge of $\overline{RAS}$ to select one of 512 rows for the transfer operation.

If $\overline{CAS}$ makes a high-to-low transition during any transfer cycle, the 9-bit address present on A0-A8 selects one of the 512 possible positions in the SAM from which the first serial data will be read or into which the first serial data will be written. This is also referred to as *setting the tap point*. During the very first transfer cycle, the tap point must be set. In subsequent transfer cycles, $\overline{CAS}$ need not go low, in which case the previously set tap point will be used.

In the split-register transfer mode, the most significant column address bit (A8) selects which half of the register will be reloaded from the memory array. The remaining eight addresses (A0-A7) determine the register starting location for the register to be reloaded.

special function input (DSF)

In the read transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ selects the split-register mode transfer operation. This mode divides the serial data register into a high order half and a low order half; one active, and one inactive. When the cycle is initiated, a transfer occurs between the memory array and either the high half or the low half register, depending on the state of the most significant column address bit (A8) that is strobed in on the falling edge of $\overline{CAS}$. If A8 is high, the transfer is to the high half of the register. If A8 is low, the transfer is to the low half of the register. Use of the split-register mode read transfer feature allows on-the-fly read transfer operation without synchronizing $\overline{TRG}$ to the serial clock.

In the write transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ permits use of an alternate mode of transfer write. This mode allows $\overline{SE}$ to be high on the falling edge of $\overline{RAS}$ without permitting a pseudo write transfer, with the serial port disabled during the entire transfer write cycle.

serial access operation

Refer to Table 2 for the following discussion on serial access operation.

serial clock (SC)

Data (SDQ) is accessed in or out of data registers on the rising edge of SC. The TMS44C251 is designed to work with a wide range of clock duty cycles to simplify system design. Since the data registers comprising the SAM are of static design, there are no SAM refresh requirements and there is no minimum SC clock operating frequency.

serial data input/output (SDQ0-SDQ3)

SD and SQ share a common I/O pin. Data is input to the device when $\overline{SE}$ is low during write mode, and data is output from the device when $\overline{SE}$ is low during read mode. The data in the SAM will be accessed in the direction from least significant bit to most significant bit. The data registers operate modulo 512. Thus, after bit 511 is accessed, the next bits to be accessed will be bits 00, 01, 02, and so on.

serial enable ($\overline{SE}$)

For serial access operation, $\overline{SE}$ enables or disables the SDQ pins. If the SDQ pins have been switched into input mode (write) by a previous transfer operation, $\overline{SE}$ high disables input and $\overline{SE}$ low enables input. If a previous transfer operation has switched the SDQ pins into output mode (read), $\overline{SE}$ high disables output and $\overline{SE}$ low enables output.

IMPORTANT NOTE: While $\overline{SE}$ is held high, the serial clock is NOT disabled. Thus, any SC pulses applied will increment the internal serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low since the serial clock input buffer and the serial address counter are not disabled by $\overline{SE}$.

QSF active status output for revision "I" and subsequent revision devices

During the split-register mode of serial access operation, QSF indicates which half of the serial register in the SAM is being accessed. If QSF is low, then the serial address pointer is accessing the lower (least significant) 256 bits of the SAM. If QSF is high, then the pointer is accessing the higher (most significant) 256 bits of the SAM. QSF changes state upon completing a transfer cycle, and the state of QSF is determined by the tap point loaded in that transfer cycle. QSF also changes state upon crossing the boundary between the two register halves in split-register mode. QSF is not an open-drain output pin.

QSF active status output for revision "H" devices

QSF is an open-drain output pin. During the split register mode of serial access operation, QSF indicates which half of the serial register in the SAM is being accessed. If QSF is low, then the serial address pointer is accessing the lower (least significant) 256 bits of the SAM. IF QSF is high, then the pointer is accessing the higher (most significant) 256 bits of the SAM.

QSF changes state upon crossing the boundary between the two register halves. When the SAM is not operating in split-register mode, the QSF output remains in the high-impedance state.

QSF is designed as an open drain output to allow OR-tying of QSF outputs from several chips. Thus, an external pullup resistor is required for the zero to one transition on QSF and the output rise time is determined by the load-capacitance and the value of the pullup resistor. The specification for QSF switching time assumes a pullup resistor of 820 ohms and a load capaticance of 50 picofarads illustrated as follows.

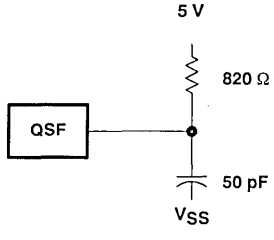


Figure 3. QSF Load Circuit (Revision "H" only)

power-up

To achieve proper device operation, an initial pause of 200 μs is required after power-up, followed by a minimum of eight $\overline{RAS}$ cycles or eight $\overline{CAS}$-before-$\overline{RAS}$ cycles, a memory-to-register transfer cycle, and two SC cycles.

absolute maximum ratings over operating free-air temperature†

Voltage on any pin except DQ and SDQ (see Note 1) ..... – 1 V to 7 V
Voltage on DQ and SDQ (see Note 1) ..... – 1 V to V_{CC} + 1
Voltage range on V_{CC} (see Note 1) ..... –1 V to 7 V
Short circuit output current (per output) ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	TMS44C251-1	4.75	5	5.25	V
		TMS44C251-10, TMS44C251-12	4.5	5	5.5	
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage		2.4		V_{CC}+1	V
V_{IL}	Low-level input voltage (see Note 2)		– 1		0.8	V
V_{OH}	High-level output voltage		2.4		V_{CC}	V
V_{OL}	Low-level output volage		– 1		0.4	V
T_A	Operating free-air temperature		0	25	70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	TMS44C251-1 TMS44C251-10		TMS44C251-12		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage		I_{OH} = –2 mA	2.4		2.4		V
V_{OL}	Low-level output voltage		I_{OL} = 2 mA		0.4		0.4	V
I_L	Input leakage current	TMS44C251-10, TMS44C251-12	V_I = 0 to 5.8 V, V_{CC} = 5.5 V, All other pins = 0 to V_{CC}		±10		±10	μA
		TMS44C251-1	V_I = 0 to 5.55 V, V_{CC} = 5.25 V, All other pins = 0 to V_{CC}		±10		±10	μA
I_O	Output leakage current (see Note 3)	TMS44C251-10, TMS44C251-12	V_O = 0 to V_{CC}, V_{CC} = 5.5 V		±10		±10	μA
		TMS44C251-1	V_O = 0 to V_{CC}, V_{CC} = 5.25 V		±10		±10	μA

PARAMETER		SAM PORT	TMS44C251-1 TMS44C251-10		TMS44C251-12		UNIT
			MIN	MAX	MIN	MAX	
I_{CC1}	Operation current, $t_{c(RW)}$ = Minimum	Standby		90		80	mA
I_{CC1A}	$t_{c(SC)}$ = Minimum	Active		110		95	
I_{CC2}	Standby current, All clocks = V_{CC}	Standby		10		10	
I_{CC2A}	$t_{c(SC)}$ = Minimum	Active		35		35	
I_{CC3}	$\overline{RAS}$-only refresh current, $t_{c(RW)}$ = Minimum	Standby		90		80	
I_{CC3A}	$t_{c(SC)}$ = Minimum	Active		110		95	
I_{CC4}	Page mode current, $t_{c(P)}$ = Minimum	Standby		50		45	
I_{CC4A}	$t_{c(SC)}$ = Minimum	Active		60		55	
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ current, $t_{c(RW)}$ = Minimum	Standby		90		80	
I_{CC5A}	$t_{c(SC)}$ = Minimum	Active		110		95	
I_{CC6}	Data transfer current, $t_{c(RW)}$ = Minimum	Standby		90		80	
I_{CC6A}	$t_{c(SC)}$ = Minimum	Active		110		95	

NOTE 3: $\overline{SE}$ is disabled for SDQ output leakage tests.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 4)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write enable input		7	pF
$C_{i(SC)}$	Input capacitance, serial clock		7	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	pF
$C_{i(DSF)}$	Input capacitance, special function		7	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		7	pF
$C_{o(O)}$	Output capacitance, SDQ and DQ		7	pF
$C_{o(QSF)}$	Output capacitance, QSF		10	pF

NOTE 4: V_{CC} equal to 5 V ± 0.5 V for TMS44C251-10 and TMS44C251-12, 5 V ± 0.25 V for TMS44C251-1, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS44C251-1 TMS44C251-10		TMS44C251-12		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{d(RLCL)}$ = MAX	t_{CAC}		25		25	ns
$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{AA}		50		25	ns
$t_{a(CP)}$	Access time from $\overline{CAS}$ high	$t_{d(RLCL)}$ = MAX	t_{CPA}		55		25	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MAX	t_{RAC}		100		25	ns
$t_{a(G)}$	Access time of Q from $\overline{TRG}$ low		t_{OEA}		25		30	ns
$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 30 pF	t_{SCA}		30		35	ns
$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 30 pF	t_{SEA}		20		25	ns
$t_{a(QSF)}$	Access time of QSF from SC low	C_L = 30 pF			60		60	ns
$t_{dis(CH)}$	Random output disable time from $\overline{CAS}$ high (See Note 6)	C_L = 100 pF	t_{OFF}	0	20	0	20	ns
$t_{dis(G)}$	Random output disable time from $\overline{TRG}$ high (See Note 6)	C_L = 100 pF	t_{OEZ}	0	20	0	20	ns
$t_{dis(SE)}$	Serial output disable time from $\overline{SE}$ high (See Note 6)	C_L = 30 pF	t_{SEZ}	0	20	0	20	ns

NOTES: 5. Switching times for RAM port output are measured with a load equivalent to 1TTL load and 100 pF, data out reference level is V_{OH}/V_{OL} = 2.4 V/0.8 V. Switching times for SAM port output are measured with a load equivalent to 1TTL load and 30 pF, serial data out reference level is V_{OH}/V_{OL} = 2 V/0.8 V.

6. $t_{dis(CH)}$, $t_{dis(G)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature †

		ALT. SYMBOL	TMS44C251-1 TMS44C251-10		TMS44C251-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 7)	t_{RC}	180		210		ns
$t_{c(W)}$	Write cycle time	t_{WC}	180		210		ns
$t_{c(rdW)}$	Read-modify-write cycle time	t_{RMW}	240		280		ns
$t_{c(P)}$	Page-mode read, write cycle time	t_{PC}	60		70		ns
$t_{c(RDWP)}$	Page-mode read-modify-write cycle time	t_{PRMW}	105		125		ns
$t_{c(TRD)}$	Transfer read cycle time	t_{RC}	180		210		ns
$t_{c(TW)}$	Transfer write cycle time	t_{WC}	180		210		ns
$t_{c(SC)}$	Serial clock cycle time (see Note 8)	t_{SCC}	30		35		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CPN}	10		15		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 9)	t_{CAS}	25	75 000	30	75 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	70		80		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 10)	t_{RAS}	100	75 000	120	75 000	ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	t_{WP}	25		25		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		25		30		ns
$t_{w(SCH)}$	Pulse duration, SC high	t_{SC}	10		12		ns
$t_{w(SCL)}$	Pulse duration, SC low	t_{SCP}	10		12		ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
$t_{su(SFC)}$	DSF setup time before $\overline{CAS}$ low	t_{FSC}	0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(WMR)}$	$\overline{W}$ setup time before $\overline{RAS}$ low	t_{WSR}	0		0		ns
$t_{su(DQR)}$	DQ setup time before $\overline{RAS}$ low	t_{MS}	0		0		ns
$t_{su(TRG)}$	$\overline{TRG}$ setup time before $\overline{RAS}$ low	t_{THS}	0		0		ns
$t_{su(SE)}$	$\overline{SE}$ setup time before $\overline{RAS}$ low with $\overline{TRG}$ = $\overline{W}$ = low	t_{ESR}	0		0		ns
$t_{su(SFR)}$	DSF setup time before $\overline{RAS}$ low	t_{FSR}	0		0		ns
$t_{su(DCL)}$	Data setup time before $\overline{CAS}$ low	t_{DSC}	0		0		ns
$t_{su(DWL)}$	Data setup time before $\overline{W}$ low	t_{DSW}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
$t_{su(WCH)}$	Write setup time before $\overline{CAS}$ high	t_{CWL}	25		30		ns
$t_{su(WRH)}$	Write setup time before $\overline{RAS}$ high	t_{RWL}	25		30		ns
$t_{su(SDS)}$	SD setup time before SC high	t_{SDS}	3		3		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		ns
$t_{h(SFC)}$	DSF hold time after $\overline{CAS}$ low	t_{CFH}	20		20		ns
$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		ns

Continued next page.

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 7. All cycle times assume t_t = 5 ns.

8. For mid-line load, $t_{c(SC)}$ = 50 ns for Revision I and subsequent revisions; $t_{c(SC)}$ = 55 ns for Revision H only. For split-register, $t_{c(SC)}$ = 40 ns for Revision H only.
9. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].
10. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

		ALT. SYMBOL	TMS44C251-1 TMS44C251-10		TMS44C251-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(TRG)}$	$\overline{TRG}$ hold time after $\overline{RAS}$ low	t_{THH}	15		15		ns
$t_{h(SE)}$	$\overline{SE}$ hold time after $\overline{RAS}$ low with $\overline{TRG}$ = $\overline{W}$ = low	t_{REH}	15		15		ns
$t_{h(RWM)}$	Write mask, transfer enable hold time after $\overline{RAS}$ low	t_{RWH}	15		15		ns
$t_{h(RDQ)}$	DQ hold time after $\overline{RAS}$ low (write mask operation)	t_{MH}	15		15		ns
$t_{h(SFR)}$	DSF hold time after $\overline{RAS}$ low	t_{RFH}	15		15		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low (see Note 10)	t_{AR}	45		45		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	20		25		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 11)	t_{DHR}	45		50		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	20		25		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ (see Note 12)	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ (see Note 12)	t_{RRH}	10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 11)	t_{WCR}	50		55		ns
$t_{h(WLG)}$	$\overline{TRG}$ hold time after $\overline{W}$ low (see Note 13)	t_{OEH}	25		30		ns
$t_{h(SDS)}$	SD hold time after SC high	t_{SDH}	5		5		ns
$t_{h(SHSQ)}$	SQ hold time after SC high	t_{SOH}	5		5		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Notes 14 and 15)	t_{CWD}	55		65		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 16)	t_{RCD}	25	75	25	90	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	50		60		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)	t_{RWD}	130		155		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 14)	t_{AWD}	85		100		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 17)	t_{CHR}	25		25		ns
$t_{d(CLRL)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 17)	t_{CSR}	10		10		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 17)	t_{RPC}	5		5		ns

Continued next page.

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 10. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].
11. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
12. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
13. Output Enable controlled write. Output remains in the high-impedance state for the entire cycle.
14. Read-modify-write operation only.
15. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
16. Maximum value specified only to guarantee $\overline{RAS}$ access time.
17. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only.

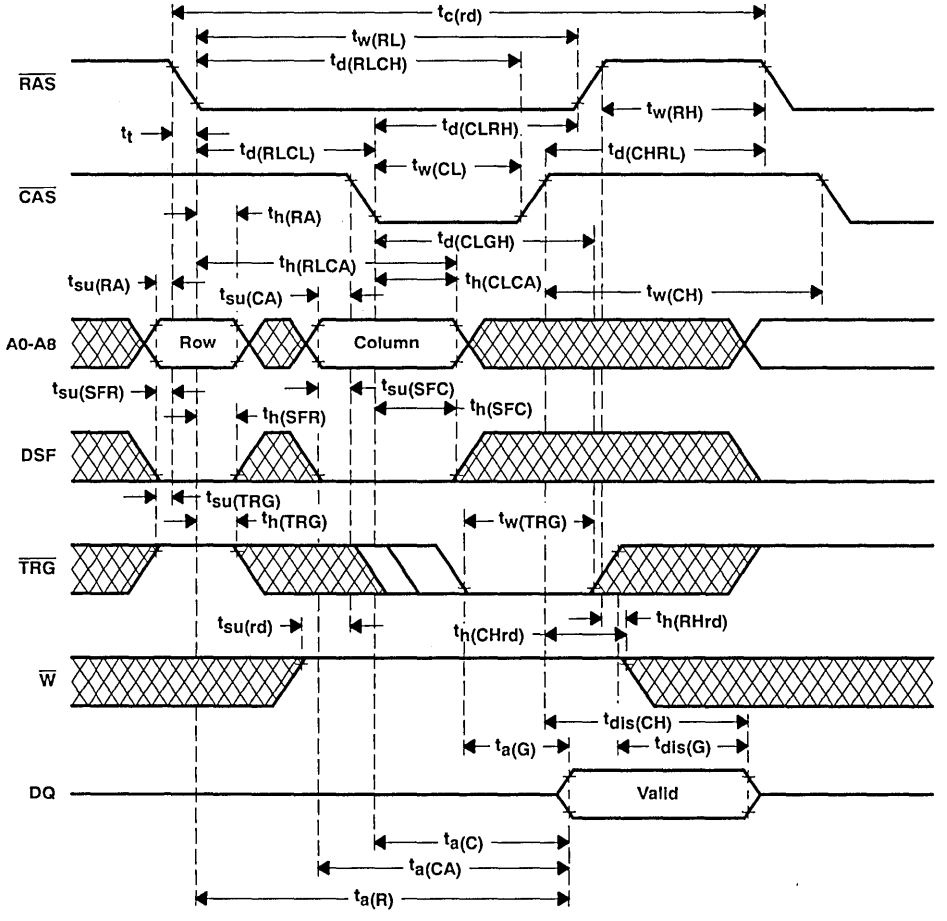
timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)†

			ALT. SYMBOL	TMS44C251-1 TMS44C251-10		TMS44C251-12		UNIT
				MIN	MAX	MIN	MAX	
$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high		t_{CTH}	25		35		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ		t_{OED}	25		30		ns
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high	Early load	t_{RTH}	$t_{h(TRG)}$		$t_{h(TRG)}$		ns
		Mid-line load		85		90		
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 18)	Revision H	t_{RSD}	125		135		ns
		Revision I		105		115		
$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 18)		t_{CSD}	35		40		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 18 and 19)		t_{TSL}	10		15		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 18)		t_{TRD}	−10		−10		ns
$t_{d(SCRL)}$	Delay time, SC high to $\overline{RAS}$ low with $\overline{TRG}$ = $\overline{W}$ = low (see Notes 20 and 21)		t_{SRS}	10		10		ns
$t_{d(SCSE)}$	Delay time, SC high to $\overline{SE}$ high in serial input mode			20		20		ns
$t_{d(RHSC)}$	Delay time, $\overline{RAS}$ high to SC high (see Note 21)		t_{SRD}	25		30		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 22)		t_{TRP}	$t_{w(RH)}$		$t_{w(RH)}$		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 22)	Revision H	t_{TSD}	35		40		ns
		Revision I		30		35		
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 22)		t_{TSD}	35		40		ns
$t_{d(SESC)}$	Delay time, $\overline{SE}$ low to SC high (see Note 23)		t_{SWS}	10		15		ns
$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split read transfer cycles			25		30		ns
$t_{d(TPRL)}$	Delay time, first (TAP) rising edge of SC after boundary switch to $\overline{RAS}$ low during split read transfer cycles			20		25		ns
$t_{rf(MA)}$	Refresh time interval, memory		t_{REF}		8		8	ms
t_t	Transition time		t_T	3	50	3	50	ns

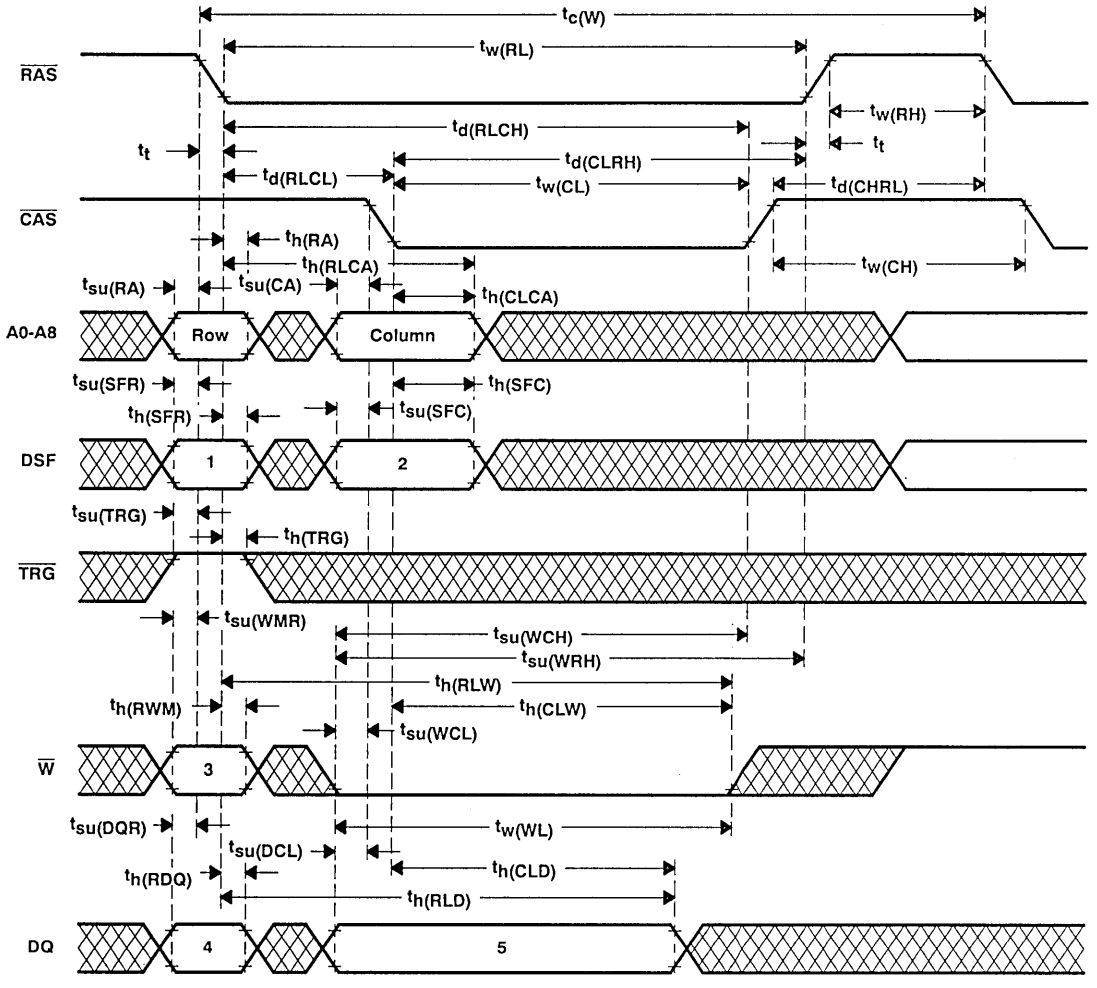
† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 18. Memory to register (read) transfer cycles only.
19. In a transfer read cycle, the state of SC when $\overline{TRG}$ rises is a Don't Care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{TRG}$ goes high.
20. In a transfer write cycle, the state of SC when $\overline{RAS}$ falls is a Don't Care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{RAS}$ goes low.
21. Register to memory (write) transfer cycles only.
22. Memory to register (read) and register to memory (write) transfer cycles only.
23. Serial data-in cycles only.

read cycle timing

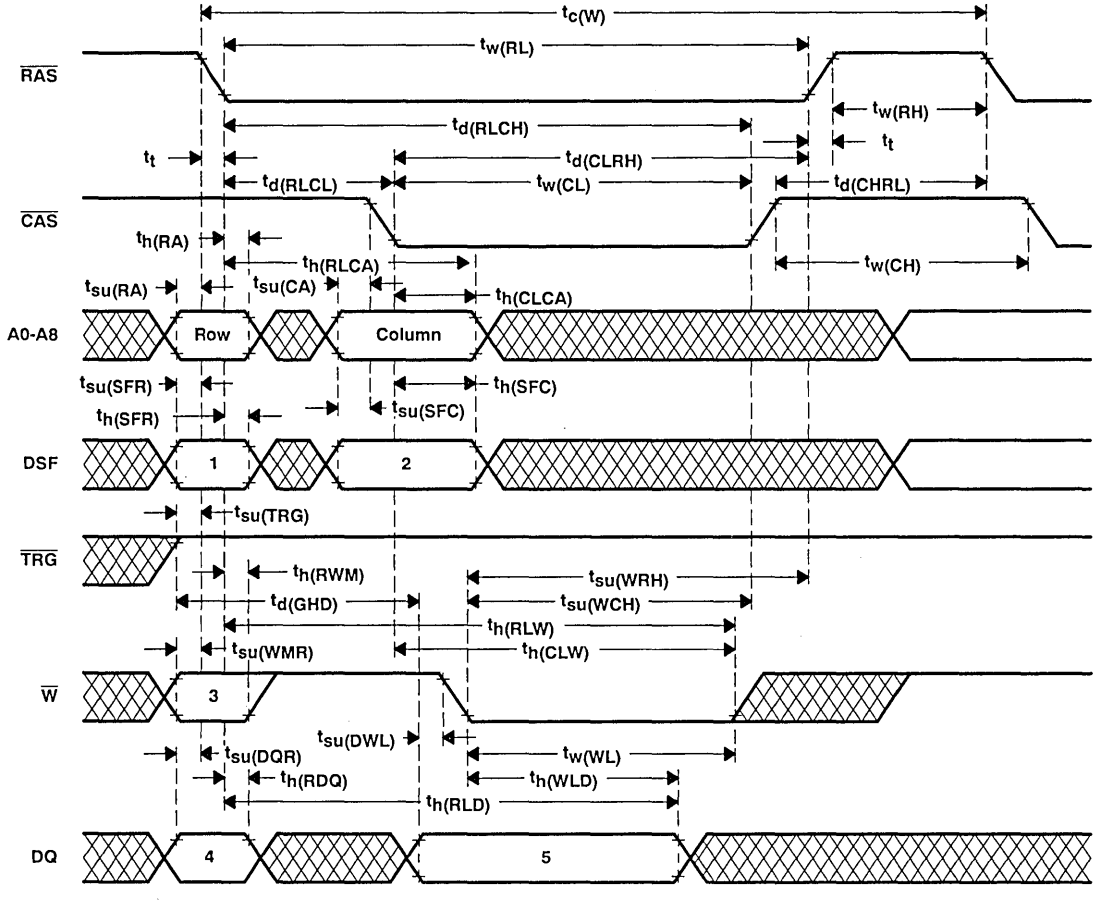


early write cycle timing



NOTE 24: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

delayed write cycle timing

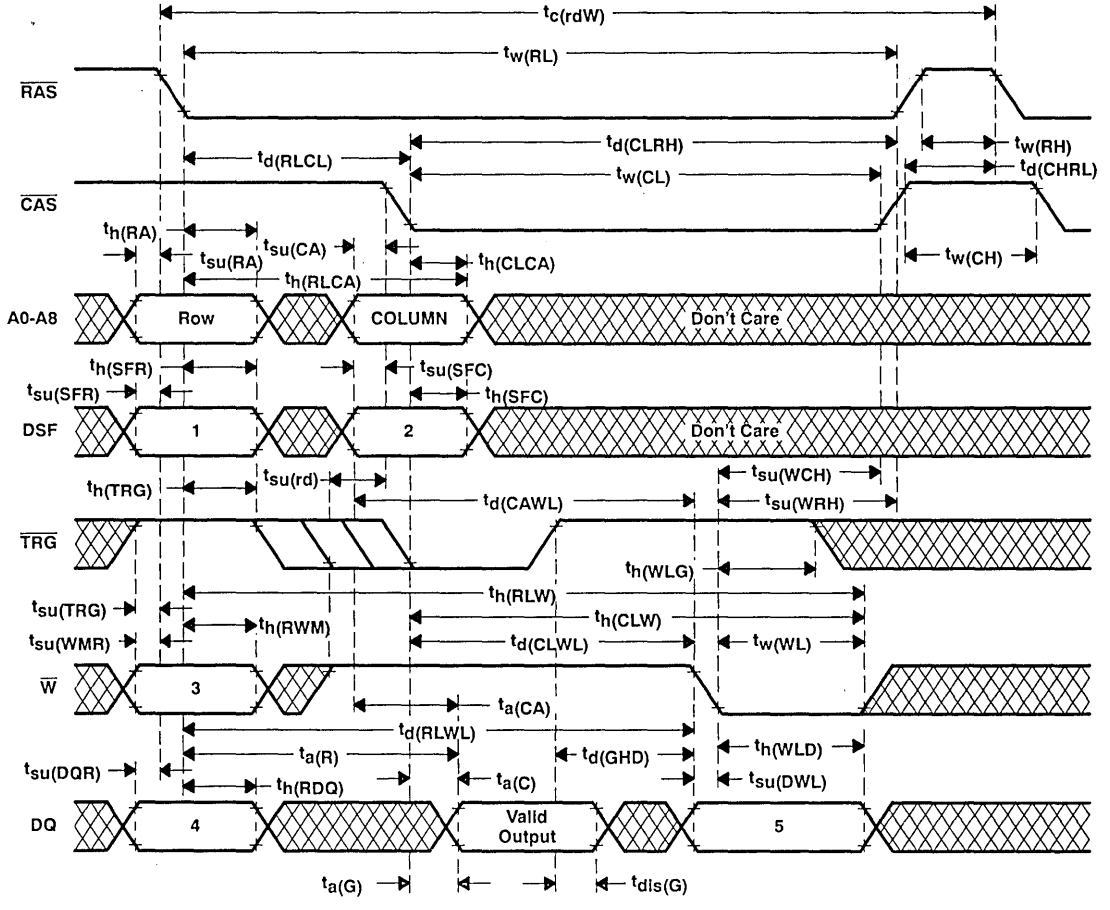


NOTE 24: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

write cycle state table

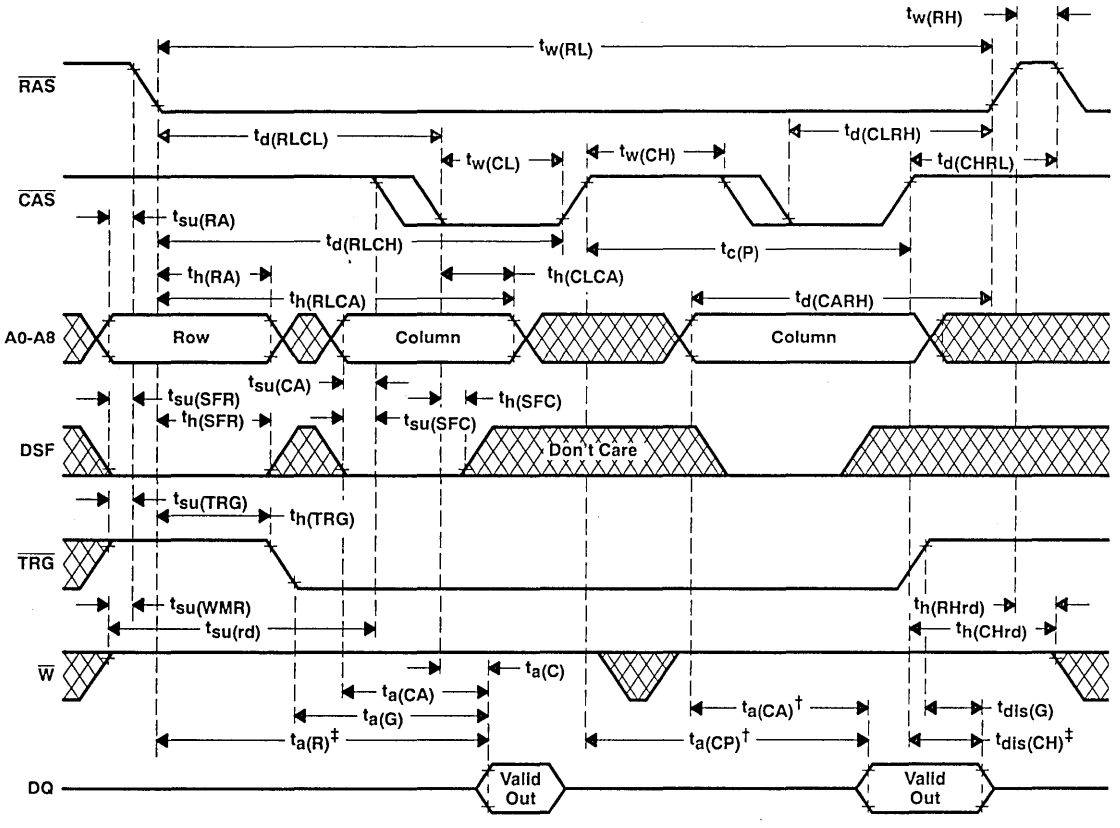
CYCLE	STATE				
	1	2	3	4	'5
Write mask load/use write DQs to I/Os	L	L	L	Write Mask	Valid Data
Write mask load/use block write	L	H	L	Write Mask	Addr Mask
Use previous write mask, write DQs to I/Os	H	L	L	Don't Care	Valid Data
Use previous write mask, block write	H	H	L	Don't Care	Addr Mask
Load write mask on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	L	H	Don't Care	Write Mask
Load color register on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	H	H	Don't Care	Color Data
Write mask disabled, block write to all I/Os	L	H	H	Don't Care	Addr Mask
Normal early or late write operation	L	L	H	Don't Care	Valid Data

read-write/read-modify-write cycle timing



NOTE 25: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5". Same logic as delayed write cycle.

enhanced page-mode read cycle timing

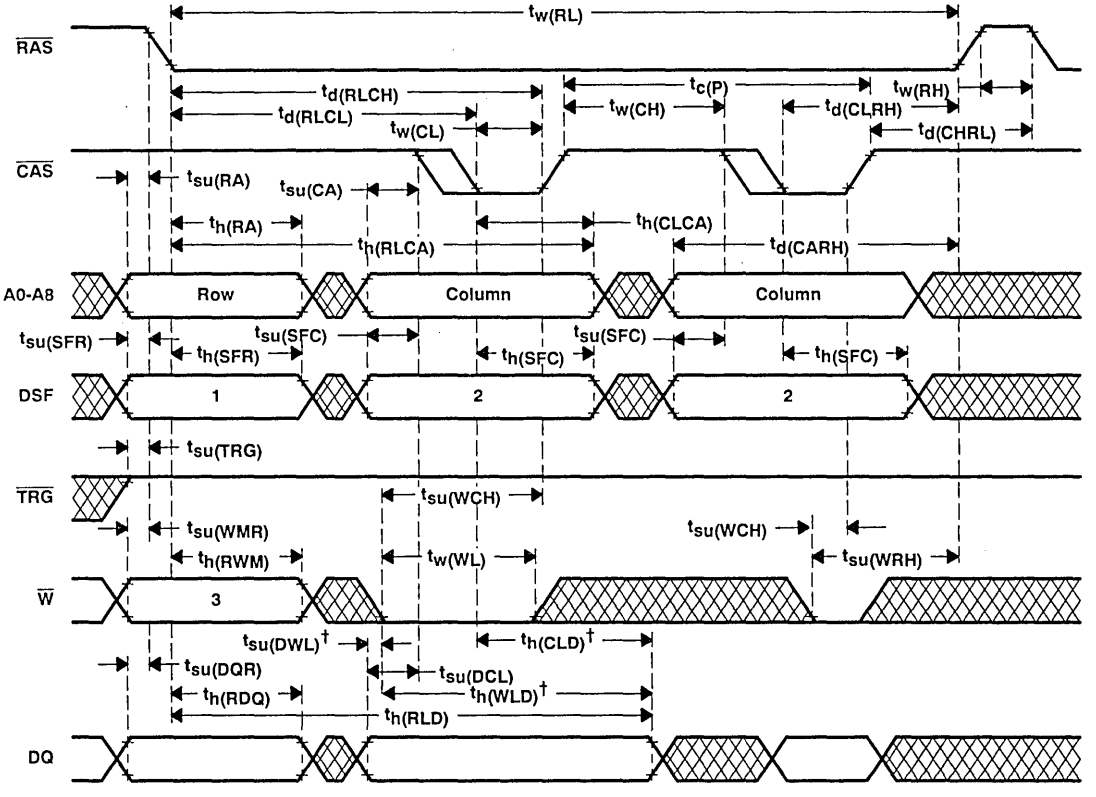


† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

‡ Output may go from high-impedance state to an invalid data state prior to the specified access time.

NOTE 26: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edges of $\overline{RAS}$ and $\overline{CAS}$ to select the desired write mode (normal, block write, etc.).

enhanced page-mode write cycle timing

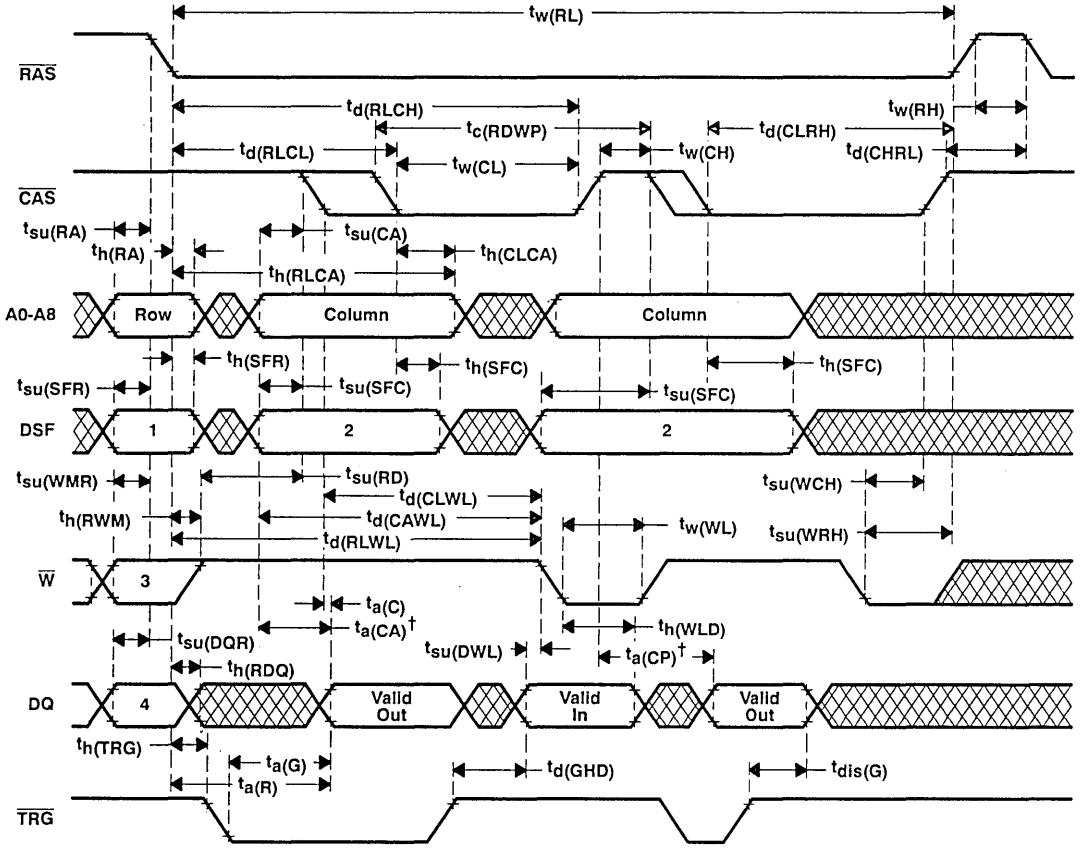


† Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

NOTES: 24. See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

27. A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used, to guarantee page-mode cycle time. If the early write cycle timing is used, the state of $\overline{TRG}$ is a Don't Care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

enhanced page-mode read-modify-write cycle timing

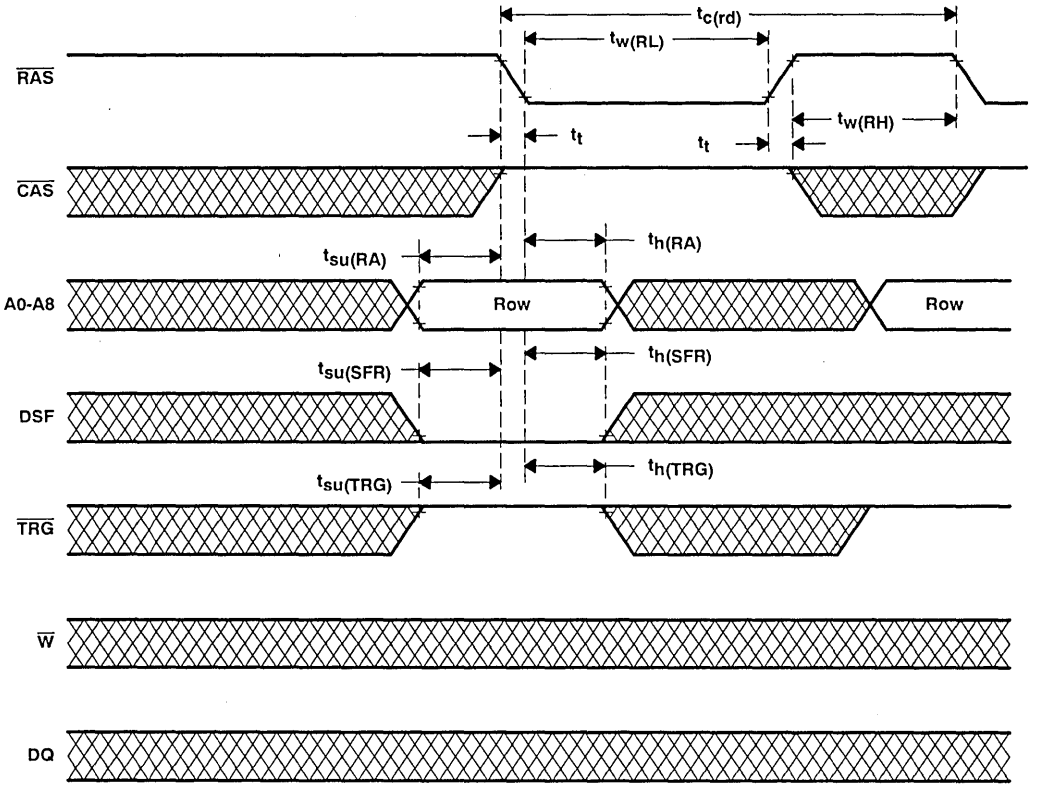


† Output may go from the high-impedance state to an invalid data state prior to the specified access time.

NOTES: 24. See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

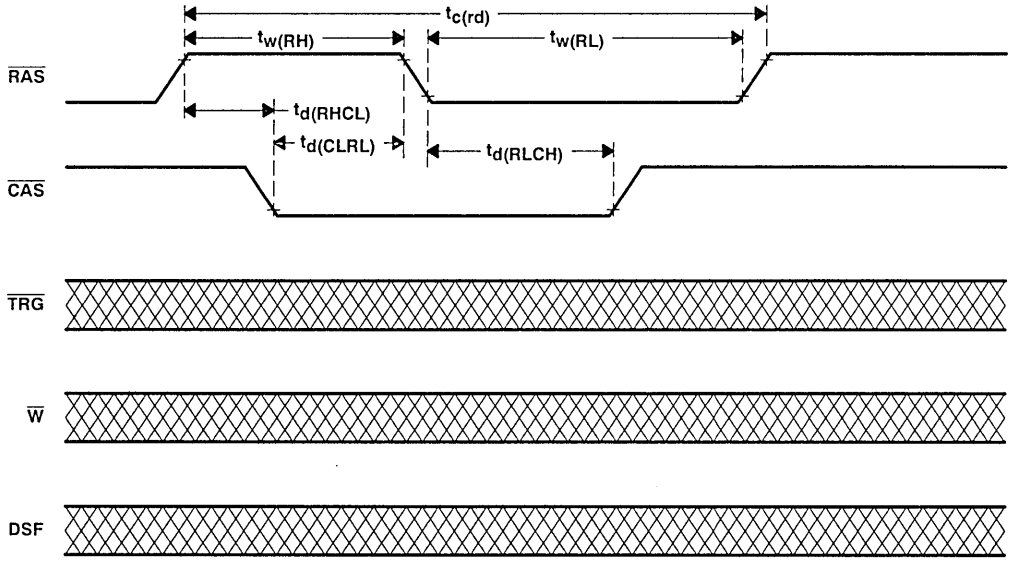
28. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing



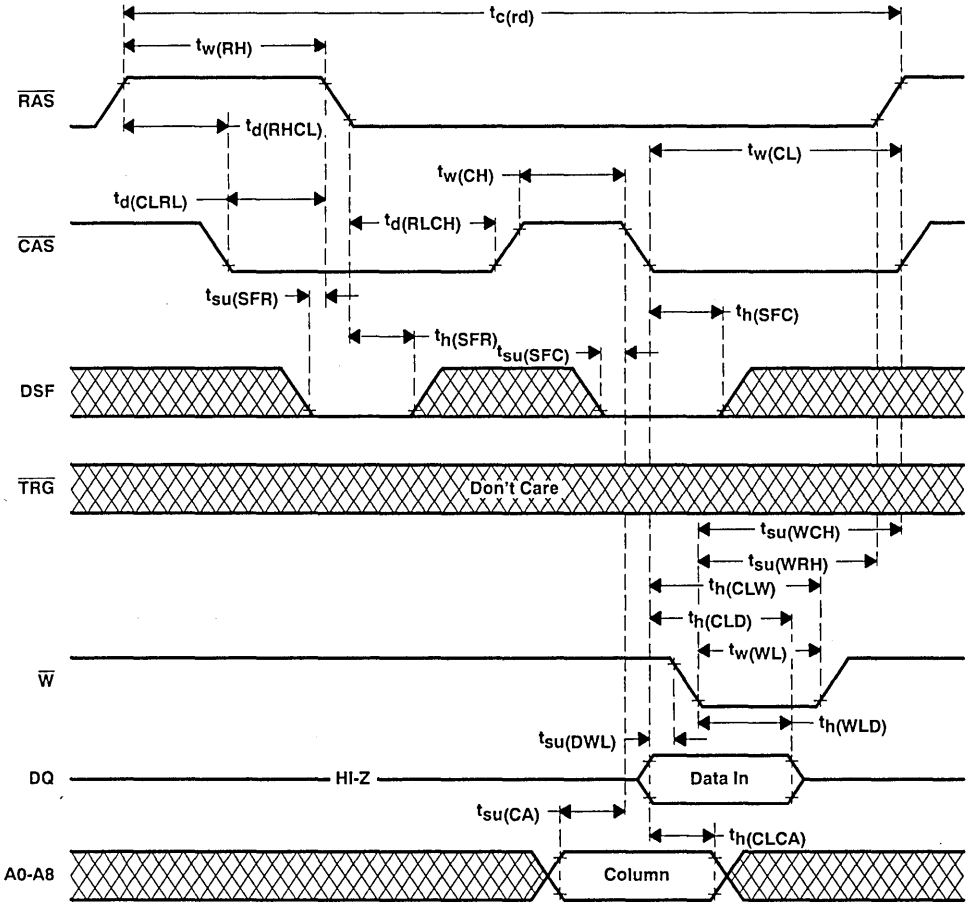
NOTE 29: In persistent write-per-bit function, $\overline{W}$ must be high during the refresh cycles.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh

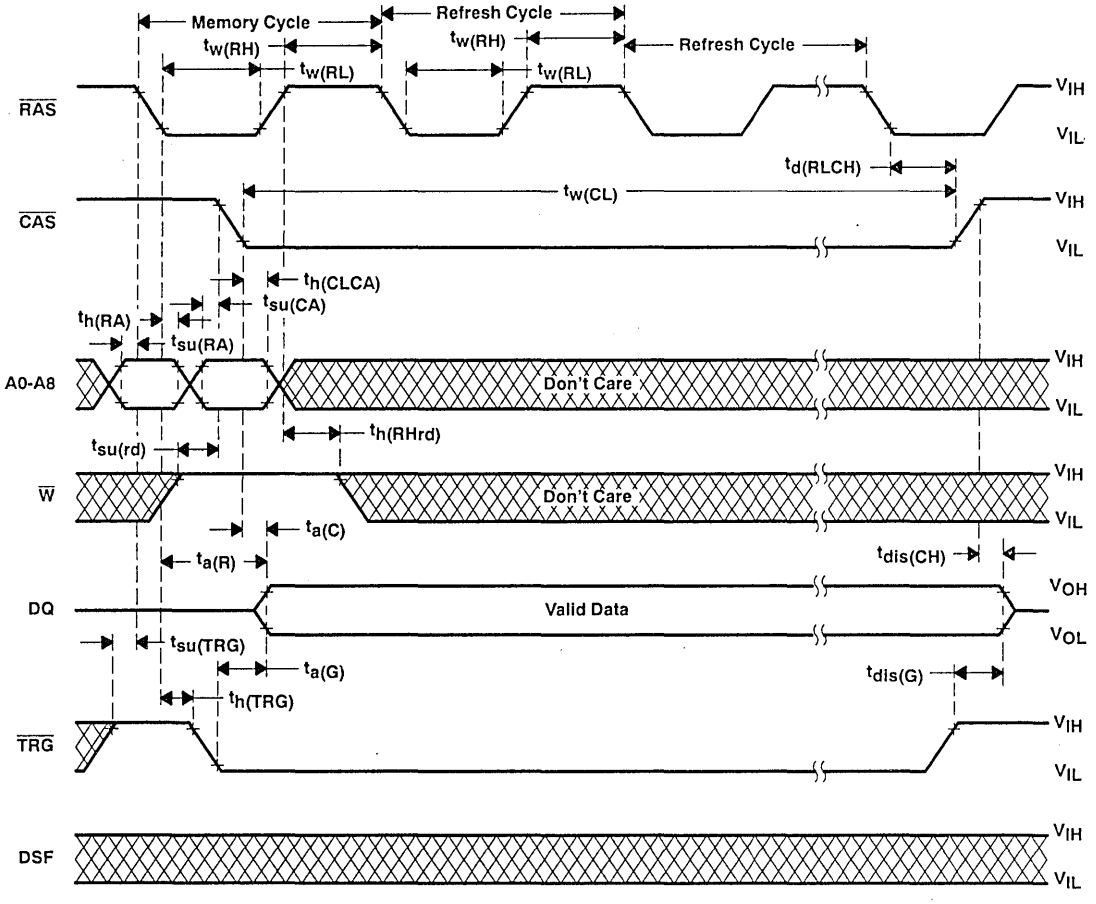


NOTE 29: In persistent write-per-bit function, $\overline{W}$ must be high during the refresh cycles.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test timing

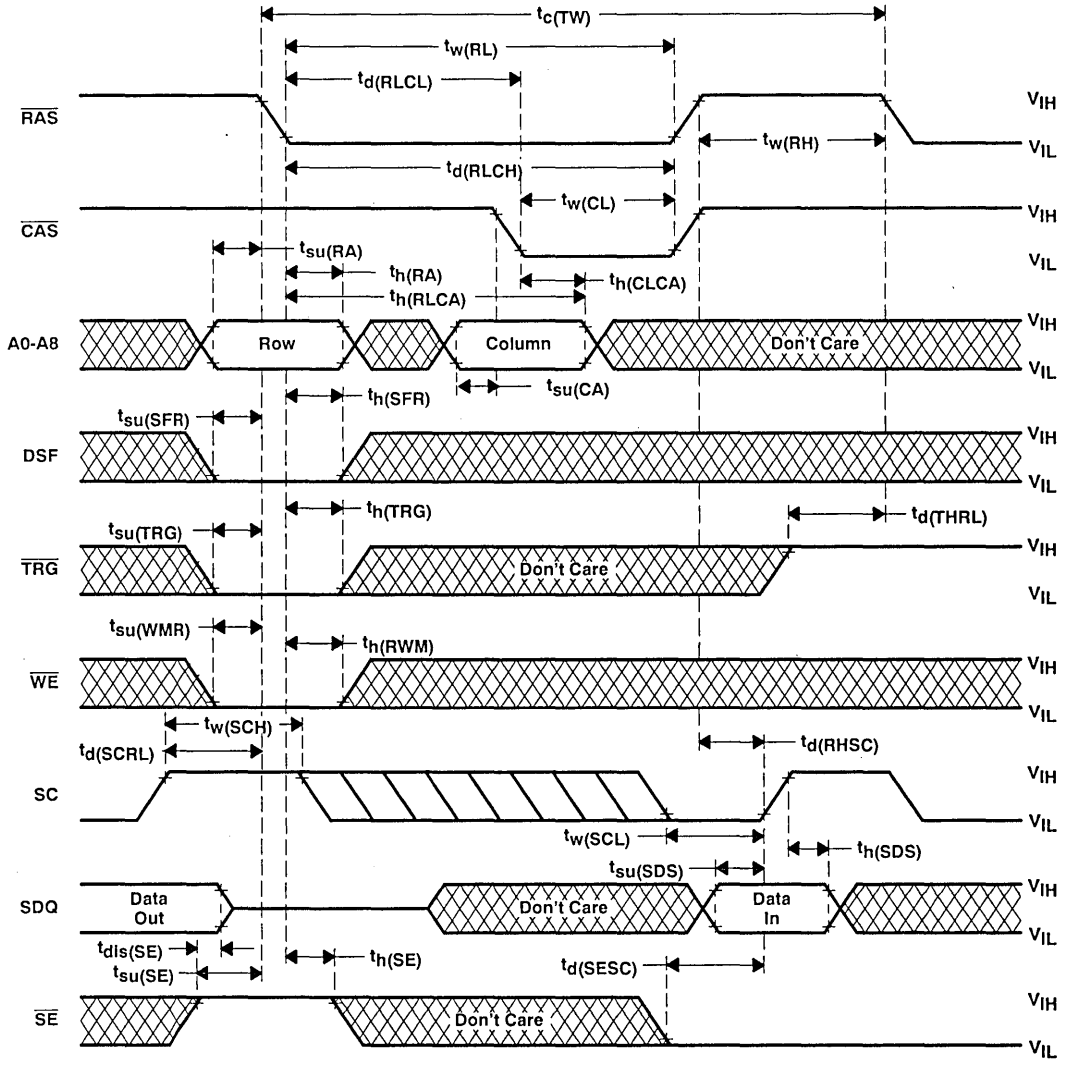


hidden refresh cycle timing



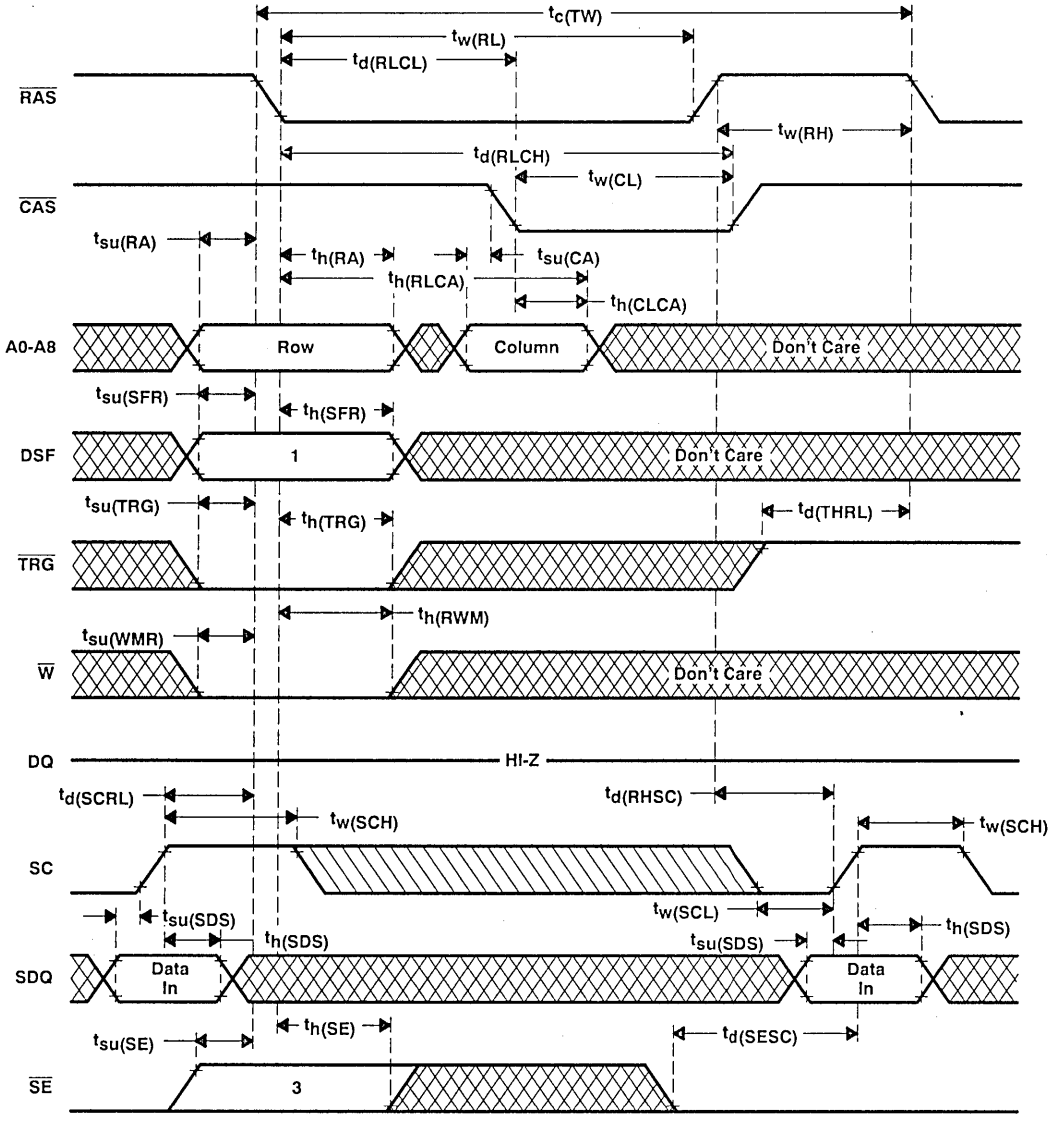
write-mode control pseudo write transfer timing

The write-mode control cycle is used to change the SDQs from the output mode to the input mode. This allows serial data to be written into the data register. The diagram below assumes that the device was originally in the serial read mode.



NOTES: 30. Random-mode Q outputs remain in the high-impedance state for the entire write-mode control.
31. $\overline{SE}$ must be high as $\overline{RAS}$ falls in order to perform a write-mode control cycle.

data register to memory timing, serial input enabled



NOTES: 32. Random mode Q outputs remain in the high-impedance state for the entire data register to memory transfer cycle. This cycle is used to transfer data from the data register to the memory array. Every one of the 512 locations in each data register is written into the corresponding 512 columns of the selected row. Data in the data register may proceed from a serial shift-in or from a parallel load from one of the memory array rows. The above diagram assumes that the device is in the serial write mode (i.e., SD is enabled by a previous write mode control cycle, thus allowing data to be shifted-in).

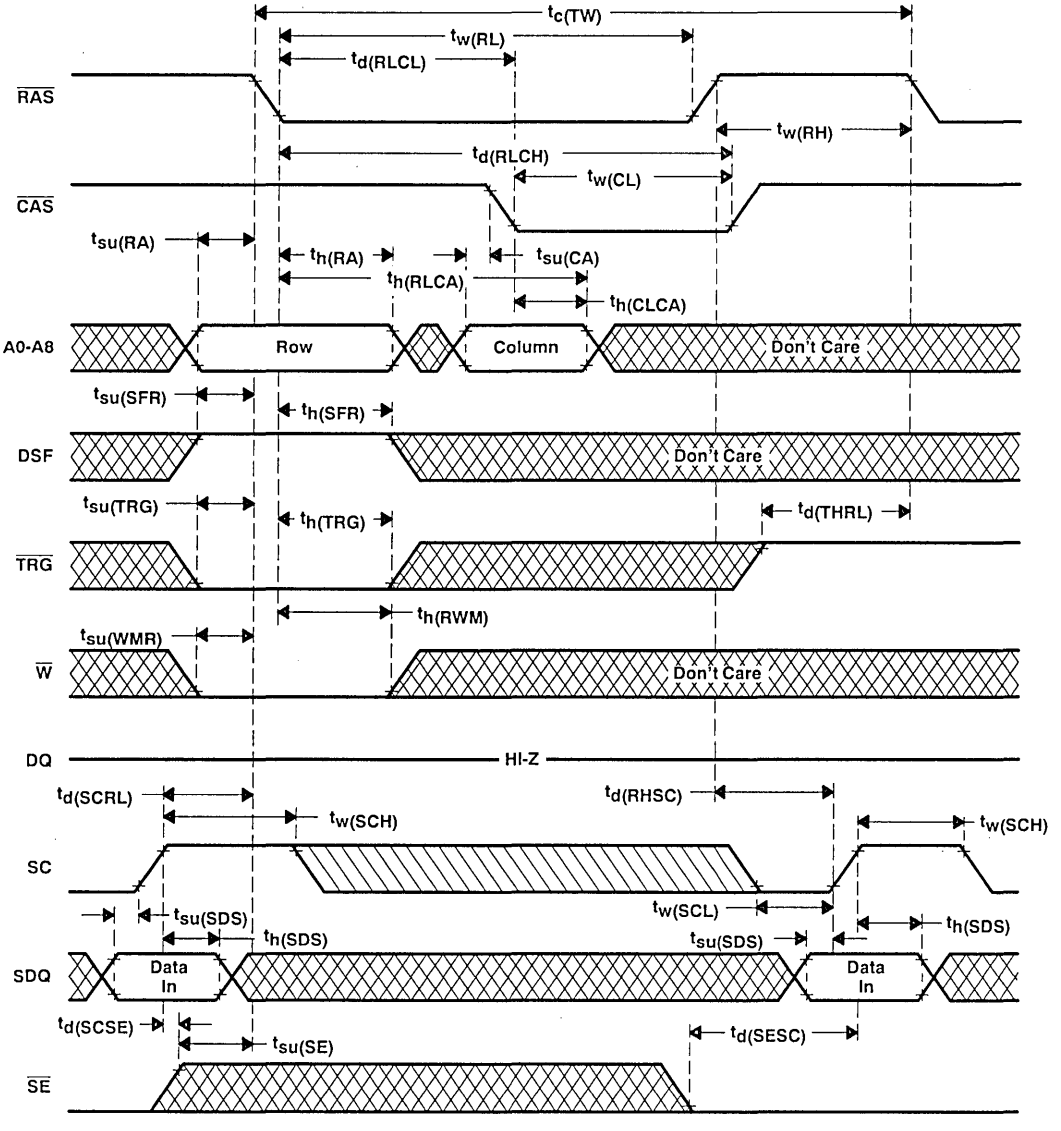
33. See "Register Transfer Function Table" for logic state of "1" and "3".

34. Successive transfer writes can be performed without serial clocks for applications requiring fast memory array clears.

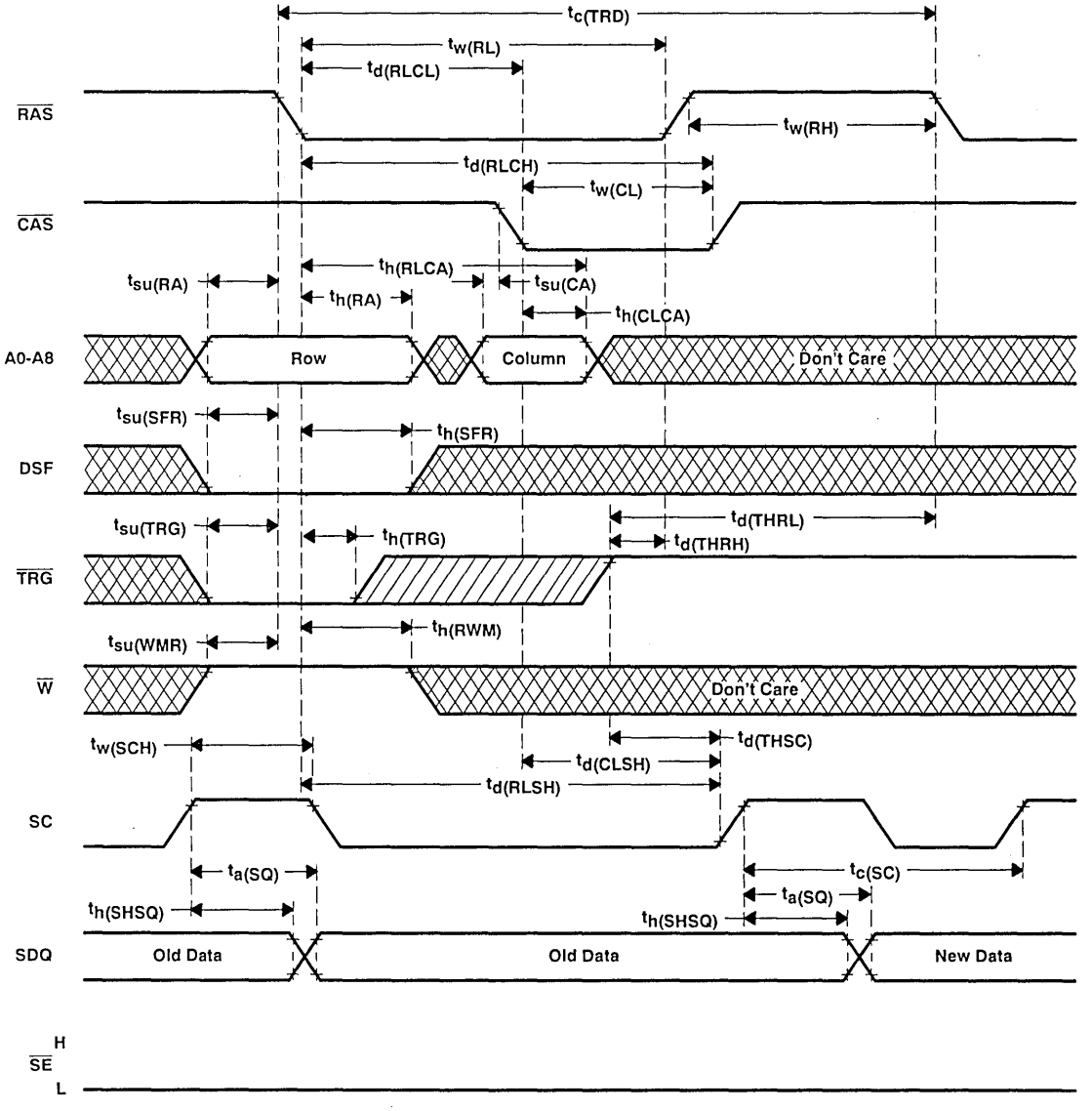
register transfer function table

FUNCTION	$\overline{RAS}$ FALL			
	$\overline{TRG}$	$\overline{W}$	DSF (1)	$\overline{SE}$ (3)
Register to memory transfer, serial input enabled, serial write mode enable	L	L	X	L
Register to memory transfer, alternate transfer write, serial write mode enable	L	L	H	X
Pseudo-transfer SDQ control, serial write mode enable	L	L	L	H
Memory to register transfer	L	H	L	X
Split-register transfer	L	H	H	X

alternate data register to memory timing



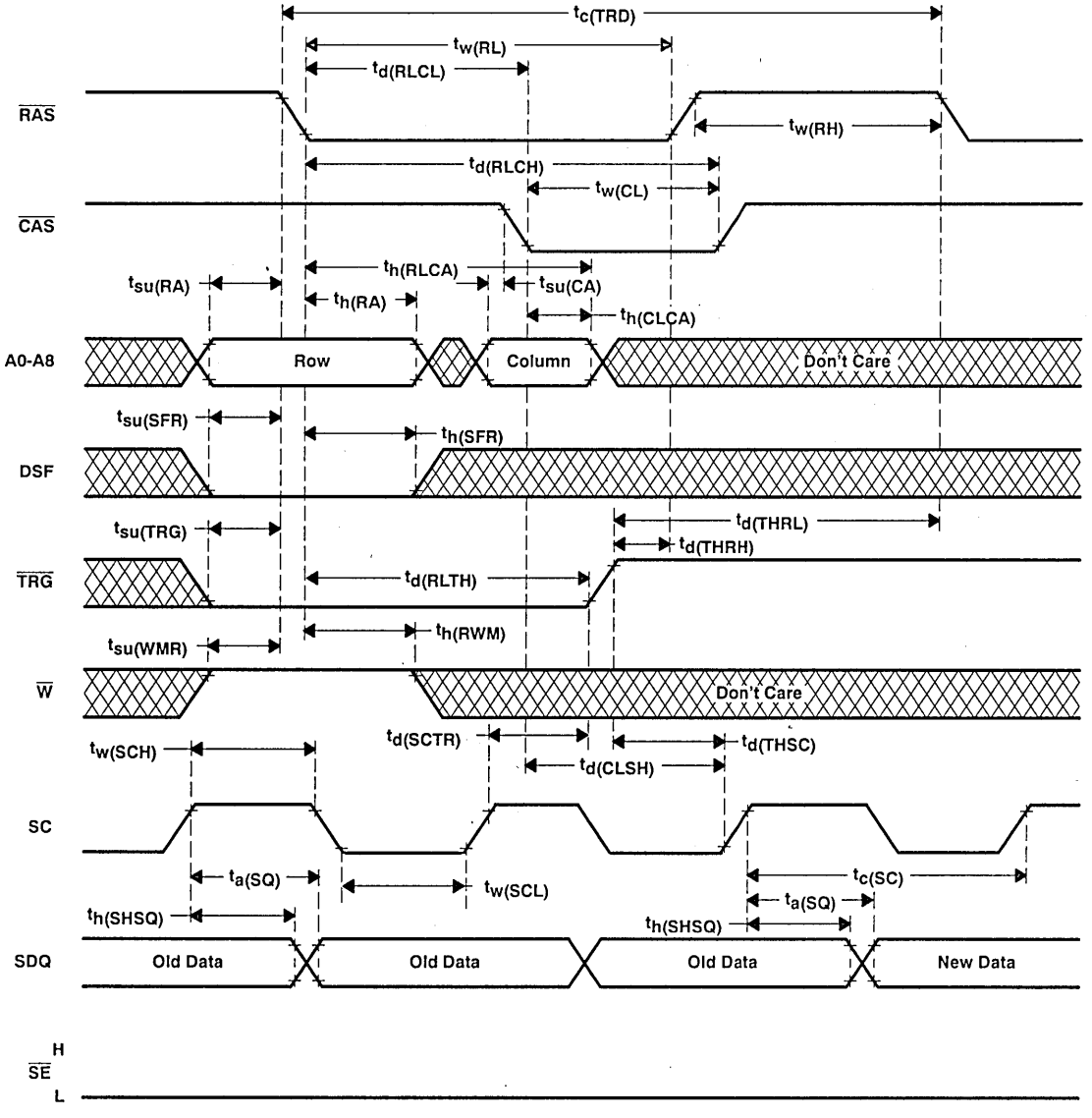
memory to data register transfer timing, early load operation



NOTES: 35. Random mode (Q outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written into from the 512 corresponding columns of the selected row. The data that is transferred into the data registers may be either shifted out or transferred back into another row.

36. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

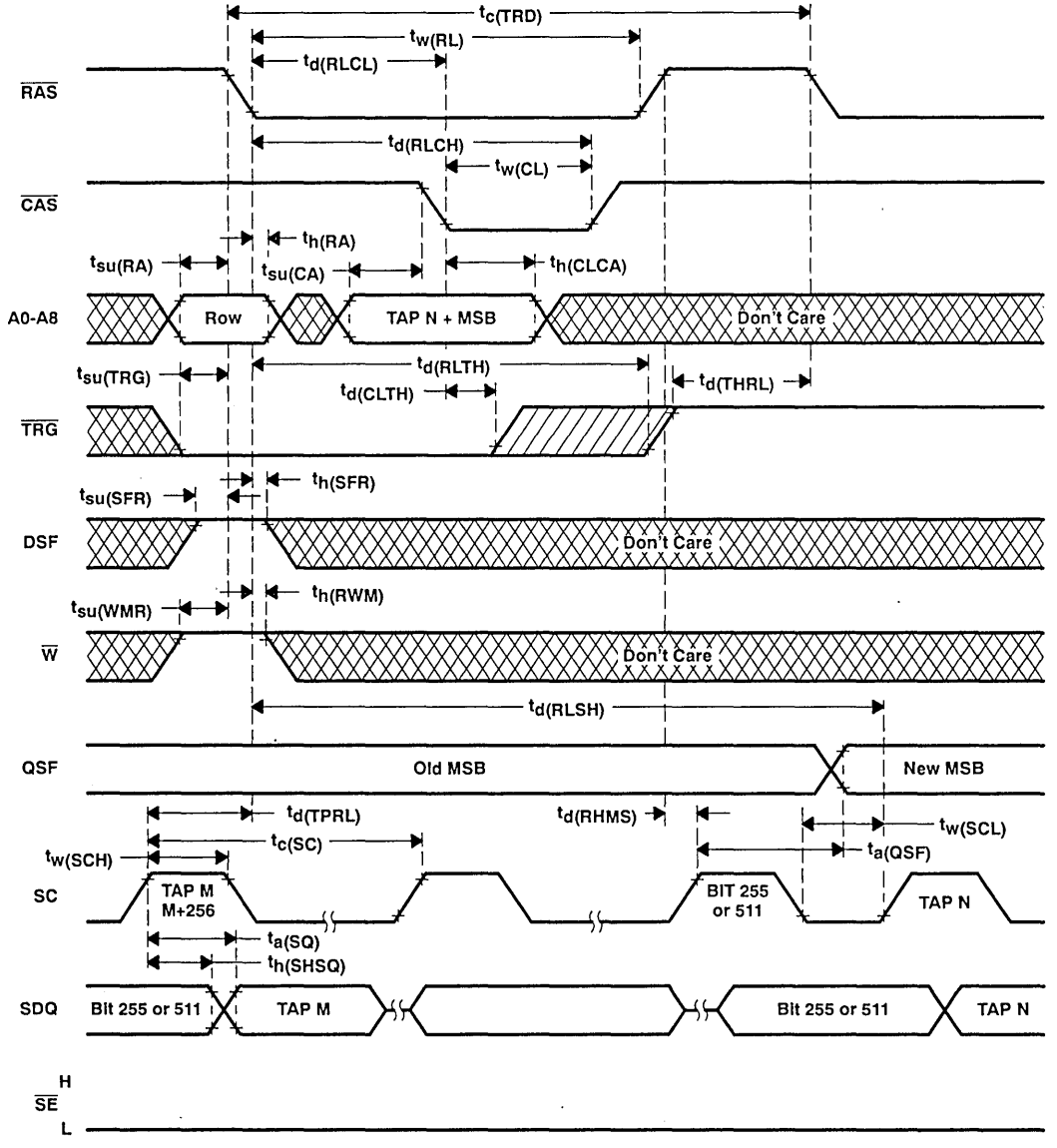
memory to data register transfer timing, mid-line load operation



NOTES: 35. Random mode (Q outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written into from the 512 corresponding columns of the selected row. The data that is transferred into the data registers may be either shifted out or transferred back into another row.

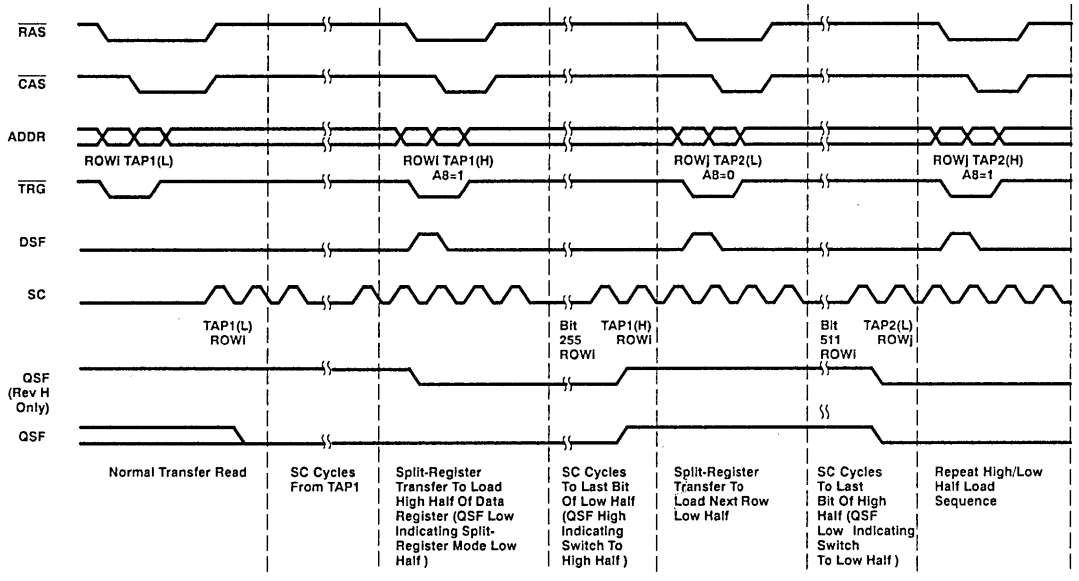
36. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

split-register mode read transfer timing



NOTE 37: There must be a minimum of two SC clocks cycle between any two split-register reload cycles, and a minimum of one SC clock cycle between a transfer read cycle and a split-register cycle.

split-register operating sequence

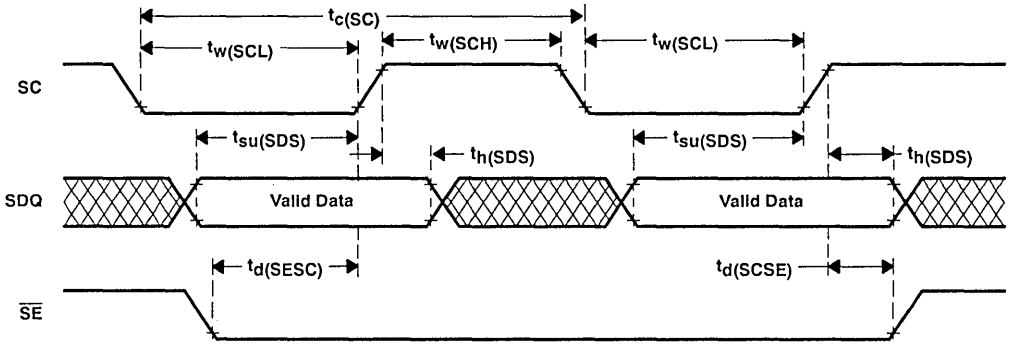


NOTES: 38. In the split-register mode, data can be transferred from different rows to the low and high halves of the data register.
39. When enabling or disabling the split-register mode, $t_{a(QSF)}$ is measured from $\overline{RAS}$ low in the transfer cycle.

application notes

1. In order to achieve proper split-register operation, a normal read transfer, followed by a minimum of one serial clock cycle should be performed before the first split-register transfer cycle. This is necessary to initialize the data register and the starting tap location. Serial access can then begin after the normal transfer cycle.
2. A split-register transfer into the inactive half is not allowed until $t_{d(TPRL)}$ is met. $t_{d(TPRL)}$ is the minimum delay time between the rising edge of the serial clock (SC) of the previously loaded tap point and the falling edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half.
3. After $t_{d(TPRL)}$ is met, the split-register transfer into the inactive half must also satisfy the $t_{d(RHMS)}$ condition. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half and the rising edge of the last serial clock (SC 255 or 511) of the active half.

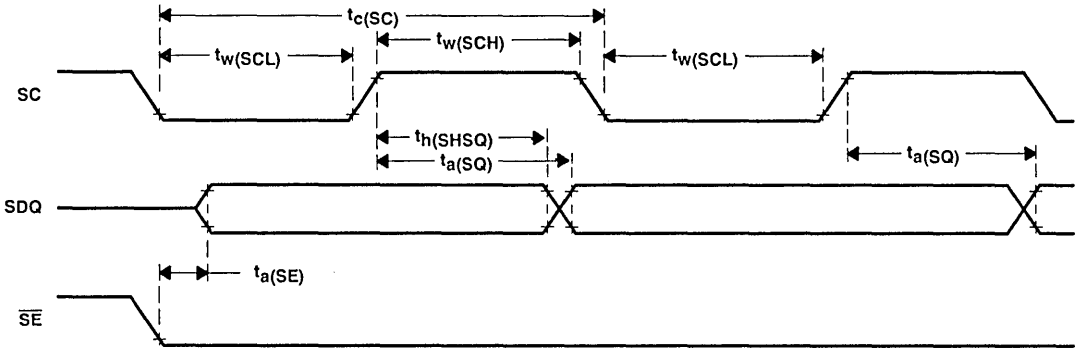
serial data-in timing



The serial data-in cycle is used to input serial data into the data registers. Before data can be written into the data registers via SD, the device must be put into the write mode by performing a write mode control (pseudo-transfer) or any transfer write cycle. A transfer read cycle is the only cycle that will take the device out of the write mode and put it into the read mode, thus disabling the input of data. Data will be written starting at the location specified by the input address loaded on the previous transfer cycle.

While accessing data in the serial data registers, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.

serial data-out timing

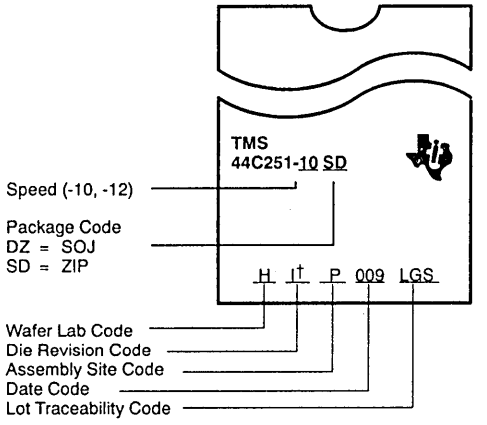


NOTES: 8. For mid-line load, $t_{c(SC)}$ = 50 ns for Revision I and subsequent revisions; $t_{c(SC)}$ = 55 ns for Revision H only. For split-register, $t_{c(SC)}$ = 40 ns for Revision H only.

40. While reading data through the serial data register, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register to memory or memory to register data transfer operation.

The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle. Transfer write cycles occurring between the transfer read cycle and the subsequent shifting out of data will not take the device out of the read mode. But a write mode control cycle at that time will take the device out of the read mode and put it in the write mode, thus not allowing the reading of data.

device symbolization



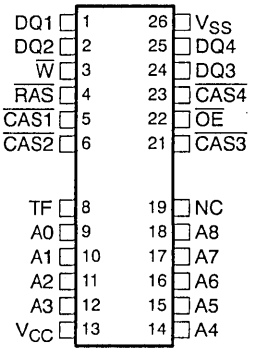
† For information on Revision "H" devices, refer to page 8-43.

- 262 144 × 4 Organization
- Single 5-V Supply (10% Tolerance)
- Performance Ranges:

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{CAA} (MAX)	READ OR WRITE CYCLE (MAX)
TMS44C260-60	60 ns	15 ns	30 ns	110 ns
TMS44C260-70	70 ns	18 ns	35 ns	130 ns
TMS44C260-80	80 ns	20 ns	40 ns	150 ns
TMS44C260-10	100 ns	25 ns	45 ns	180 ns

- Four Separate $\overline{CAS}$ Pins Provide for Separate I/O Operation
- Parity Mode and Enhanced Page Mode Operation
- 512-Cycle Refresh in 8 ms (Max)
- 3-State Unlatched Output
- Lower Power Dissipation
- Texas Instruments EPIC™ CMOS Process
- All Inputs, Outputs and Clocks are TTL Compatible
- High-Reliability Plastic 24/26-Lead 300-Mil-Wide Surface Mount (SOJ) Package
- Operating Free-Air Temperature . . . 0°C to 70°C

DJ Package†
(Top View)



†The package shown here is for pinout reference only and is not drawn to scale.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS1}$-$\overline{CAS4}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
TF	Test Function
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS44C260 is a high-speed, 1 048 576-bit dynamic random access memory organized as 262 144 words of four bits each. It employs state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at low cost.

This device features maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 413 mW operating and 11 mW standby on 80 ns devices.

Four separate $\overline{CAS}$ pins ($\overline{CAS1}$-$\overline{CAS4}$) provide for separate I/O operation allowing this device to operate in parity mode. The TMS44C260 also functions in enhanced page mode, similar to the TMS44C256.

The EPIC™ technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{CC} peaks are 140 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS44C260 is offered in a 300-mil wide 24/26 J-lead plastic surface mount SOJ (DJ suffix) package. This device is characterized for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

operation

parity mode

Four $\overline{CAS}$ pins ($\overline{CAS1}$-$\overline{CAS4}$) are provided to give independent control of the four data I/O pins (DQ1-DQ4). For read or write cycles, the column address is latched on the first $\overline{CASx}$ falling edge. Each $\overline{CASx}$ pin going low enables its corresponding DQ pin with data coming from the column address latched on the first falling $\overline{CASx}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{CASx}$ edge.The delay time from $\overline{CASx}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{CAS}$ to its corresponding DQx pin.

In order to latch in a new column address, all four $\overline{CASx}$ pins must be brought high. The column precharge time (see parameter t_{CP}) is measured from the last $\overline{CASx}$ rising edge to the first falling $\overline{CASx}$ edge of the new cycle. In order for a column address to remain valid while toggling $\overline{CASx}$, there exists a minimum setup time (t_{CLCH}) where at least one $\overline{CASx}$ must be brought low before all other $\overline{CASx}$ pins are taken high.

For early write cycles, the data is latched on the first falling $\overline{CASx}$ edge. Only the DQs that have the corresponding $\overline{CASx}$ low will be written into. Each $\overline{CASx}$ will have to meet t_{CAS} minimum in order to ensure writing into the storage cell. In order to latch a new address and new data, all $\overline{CASx}$ pins need to come high and meet t_{CP}.

This DQ independence allows the TMS44C260 to provide four parity bits in memory designs which normally require the use of four 256k × 1 DRAMs.

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CASx}$ page-mode cycle time used. With minimum $\overline{CASx}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CASx}$ is high. The falling edge of the first $\overline{CASx}$ latches the column addresses. This feature allows the TMS44C260 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CASx}$ transitions low. This performance improvement is referred to as "enhanced page mode". Valid column address may be presented immediately after t_{RAH} (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CASx}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CASx}$ low) if t_{CAA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CASx}$ goes high, minimum access time for the next cycle is determined by t_{CAP} (access time from rising edge of the last $\overline{CASx}$).

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the first column-address strobe ($\overline{CASx}$). All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CASx}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. The TMS44C260 $\overline{CASx}$ is used as a chip select activating its corresponding output buffer, as well as latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CASx}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation with $\overline{OE}$ grounded.

data in (DQ1-DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CASx}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CASx}$ and the data is strobed in by the first occurring $\overline{CASx}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CASx}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CASx}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins with the negative transition of $\overline{CASx}$ as long as t_{RAC} and t_{CAA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CASx}$ to be brought low for the output buffers to go into low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{CASx}$ is brought high.

refresh

A refresh operation must be performed at least once every eight milliseconds to retain data. This can be achieved by strobing each of the 512 rows (A0-A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding all $\overline{CASx}$ at the high (inactive) level, thus conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CASx}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

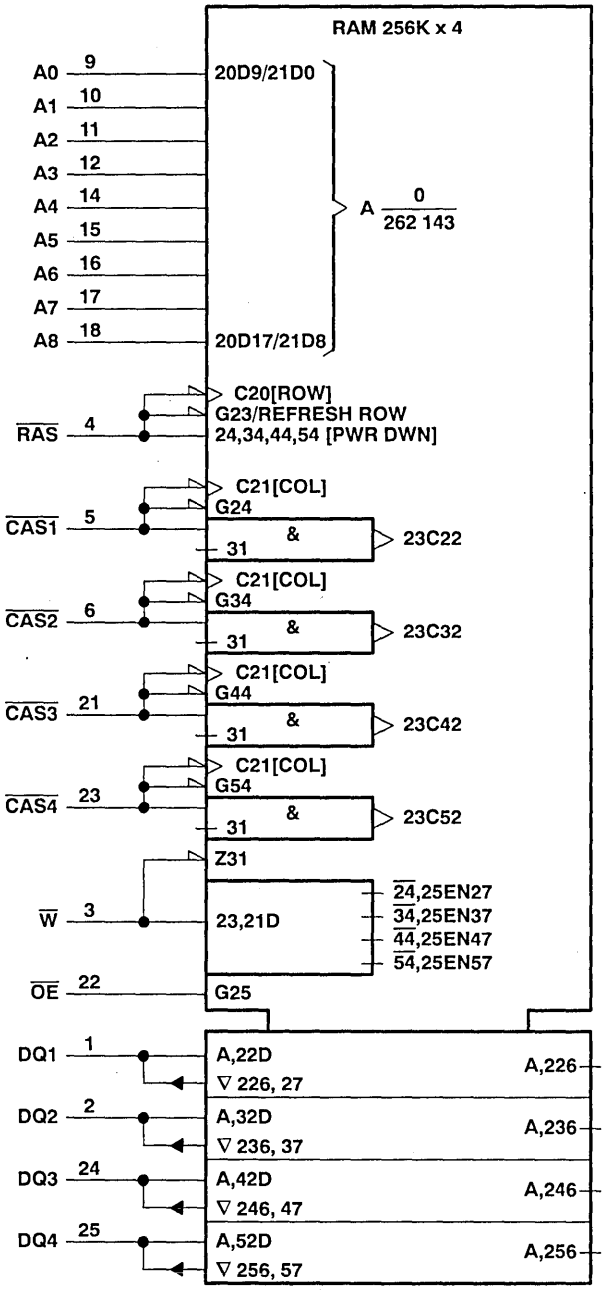
$\overline{CASx}$-before-$\overline{RAS}$ refresh

$\overline{CASx}$-before-$\overline{RAS}$ refresh is utilized by bringing at least one $\overline{CASx}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CASx}$-before-$\overline{RAS}$ refresh cycles, $\overline{CASx}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

power-up

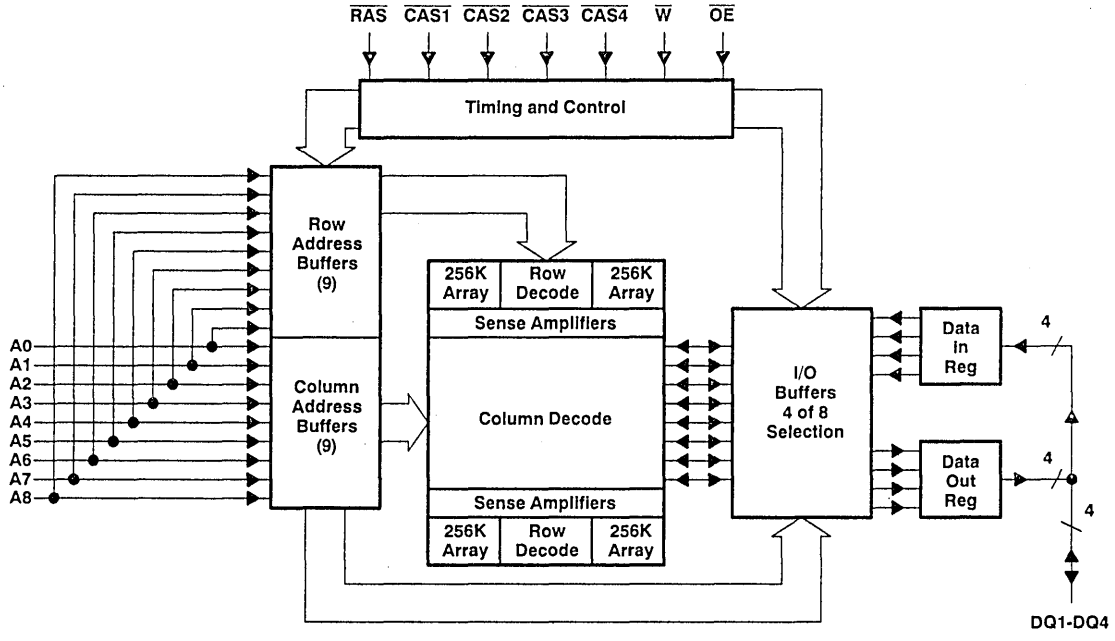
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after power-up to the full V_{CC} level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS44C260-60		TMS44C260-70		TMS44C260-80		TMS44C260-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	μA
I_O	Output current (leakage)	V_O = 0 to 6.5 V, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	μA
I_{CC1}	Read/write cycle current	t_{RWC} = minimum, V_{CC} = 5.5 V		95		80		75		65	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		2		2		2		2	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR)	t_{RWC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low, after $\overline{CAS}$ low (CBR)		90		80		70		60	mA
I_{CC4}	Average page current	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60		50		45	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)†

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			5	pF
$C_{i(W)}$	Input capacitance, write-enable input			5	pF
$C_{i(OE)}$	Input capacitance, output-enable input			5	pF
C_O	Output capacitance			7	pF

† Capacitance measurements are made on a sample basis only.

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER		TMS44C260-60		TMS44C260-70		TMS44C260-80		TMS44C260-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CAA}	Access time from column address		30		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20		25	ns
t_{CAP}	Access time from column precharge		35		40		40		50	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 4)	0	15	0	18	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 4)	0	15	0	18	0	20	0	25	ns

NOTE 4: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

		TMS44C260-60		TMS44C260-70		TMS44C260-80		TMS44C260-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time (see Note 6)	110		130		150		180		ns
t_{WC}	Write cycle time	110		130		150		180		ns
t_{RWC}	Read-write/read-modify-write cycle time	155		181		205		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 7)	40		45		50		55		ns
t_{PCM}	Page-mode read-modify-write cycle time	85		96		100		120		ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 8)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{WP}	Write pulse duration	15		15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time before $\overline{W}$ low (see Note 10)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low (see Note 10)	10		15		15		20		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		12		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		70		ns
t_{CLCH}	Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high	5		5		5		5		ns
t_{DH}	Data hold time after $\overline{CAS}$ low (see Note 10)	10		15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		70		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	0		0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (see Note 11)	15		15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		70		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		25		ns

Continued next page.

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_T = 5 ns.
7. $t_{PC} > t_{CP}$ min + t_{CAS} min + $2t_T$.
8. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time (t_{CAS}).
9. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5) (concluded)

		TMS44C260-60		TMS44C260-70		TMS44C260-80		TMS44C260-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 14)	40		46		50		60		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)	20	45	20	52	22	60	25	75	ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 15)	15	30	15	35	17	40	20	55	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)	85		98		110		135		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (see Note 14)	55		63		70		80		ns
t_{CLZ}	Delay time, $\overline{CAS}$ low to output low Z	0		0		0		0		ns
t_{OED}	Delay time, $\overline{OE}$ high before data at DQ	15		18		20		25		ns
t_{ROH}	Delay time, $\overline{OE}$ low to $\overline{RAS}$ high	10		10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	15		15		20		25		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	10		10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	0		0		0		0		ns
t_{REF}	Refresh time interval		8		8		8		8	ms
t_T	Transition time	3	50	3	50	3	50	3	50	ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
14. Read-modify-write operation only.
15. Maximum value specified only to guarantee access time.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

PARAMETER MEASUREMENT INFORMATION

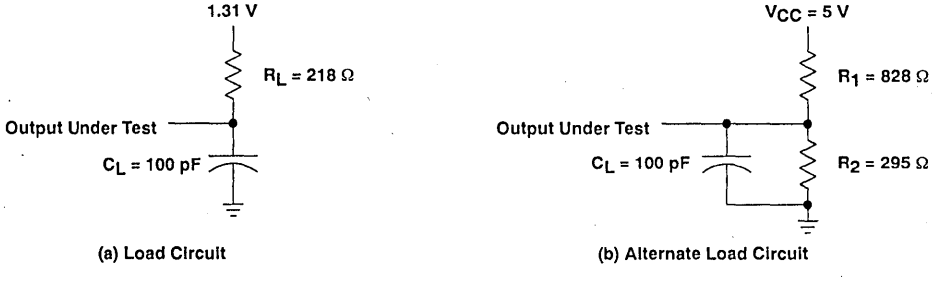
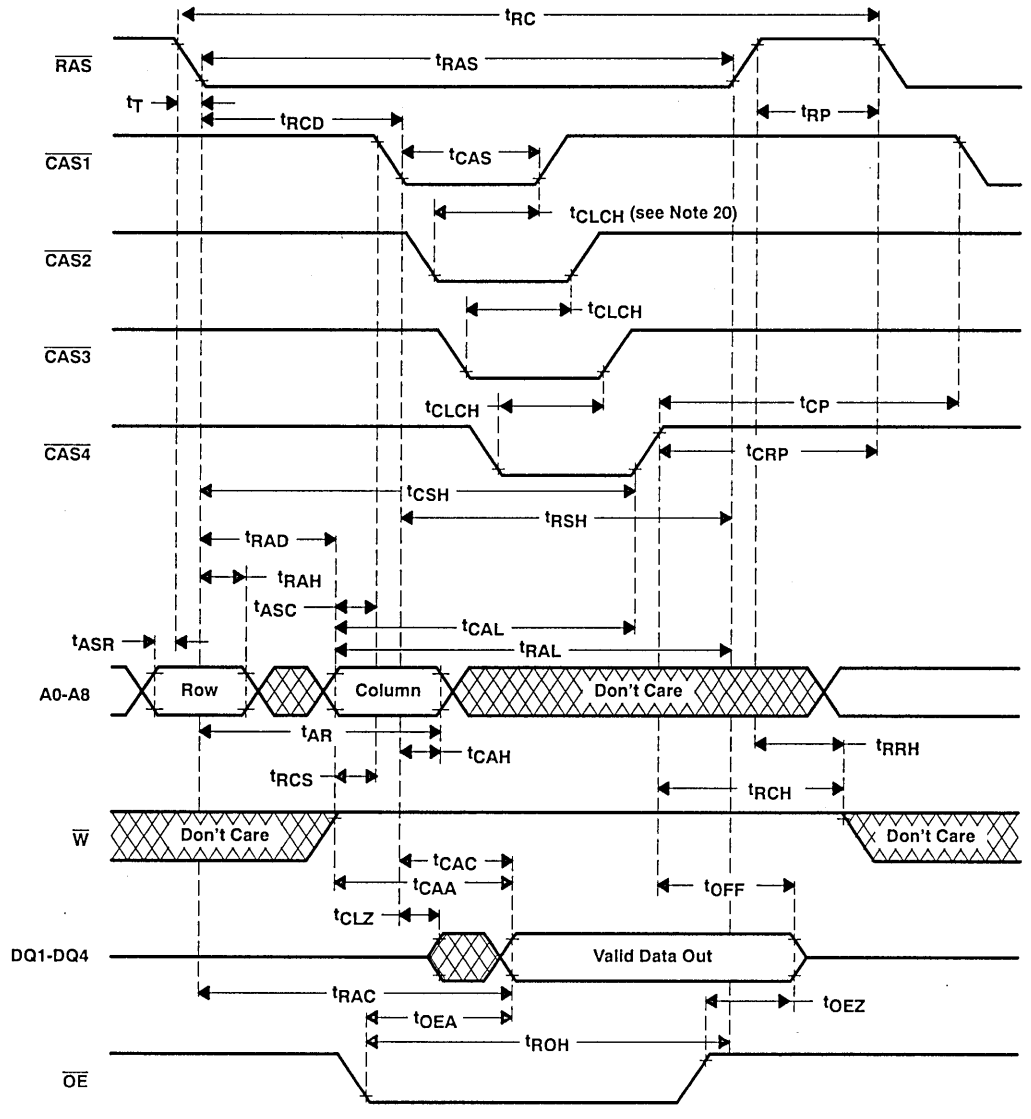


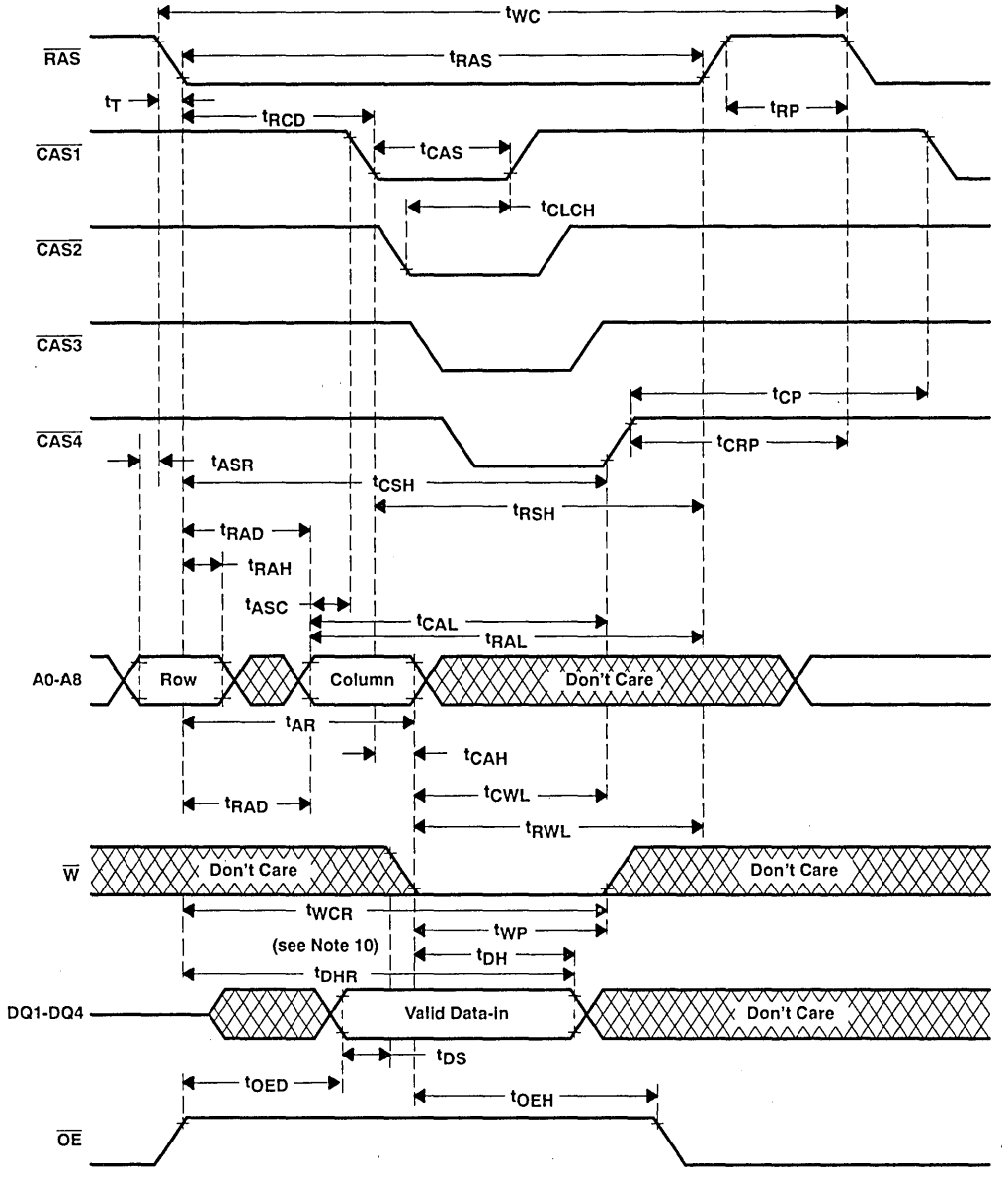
Figure 1. Load Circuits for Timing Parameters

read cycle



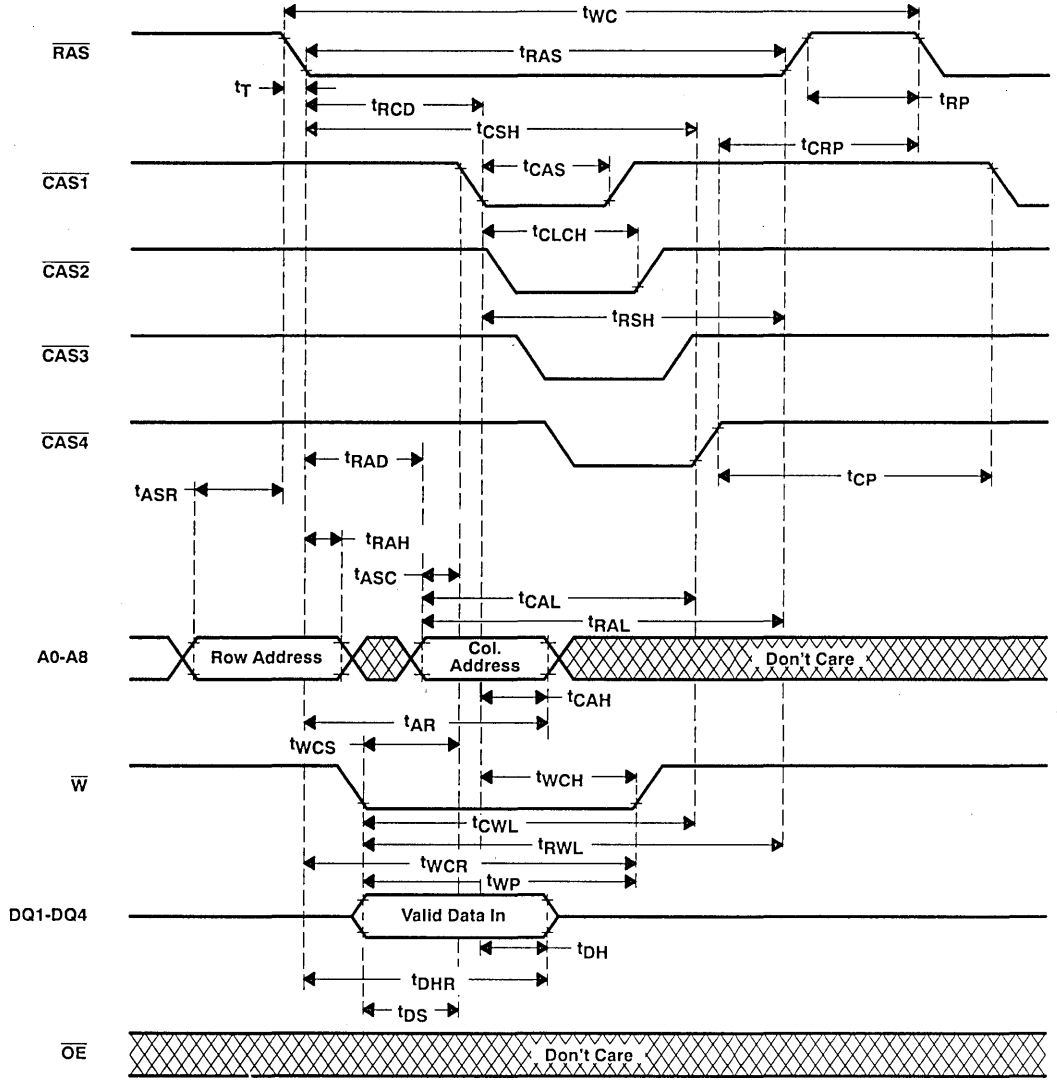
NOTES: 17. In order to hold the address latched by the first $\overline{CAS}x$ going low, the parameter t_{CLCH} must be met.
18. t_{CAC} is measured from $\overline{CAS}x$ to its corresponding DQx.
19. $\overline{CAS}x$ order is arbitrary.
20. Output may go from high-impedance to an invalid data state prior to the specified access time.

write cycle



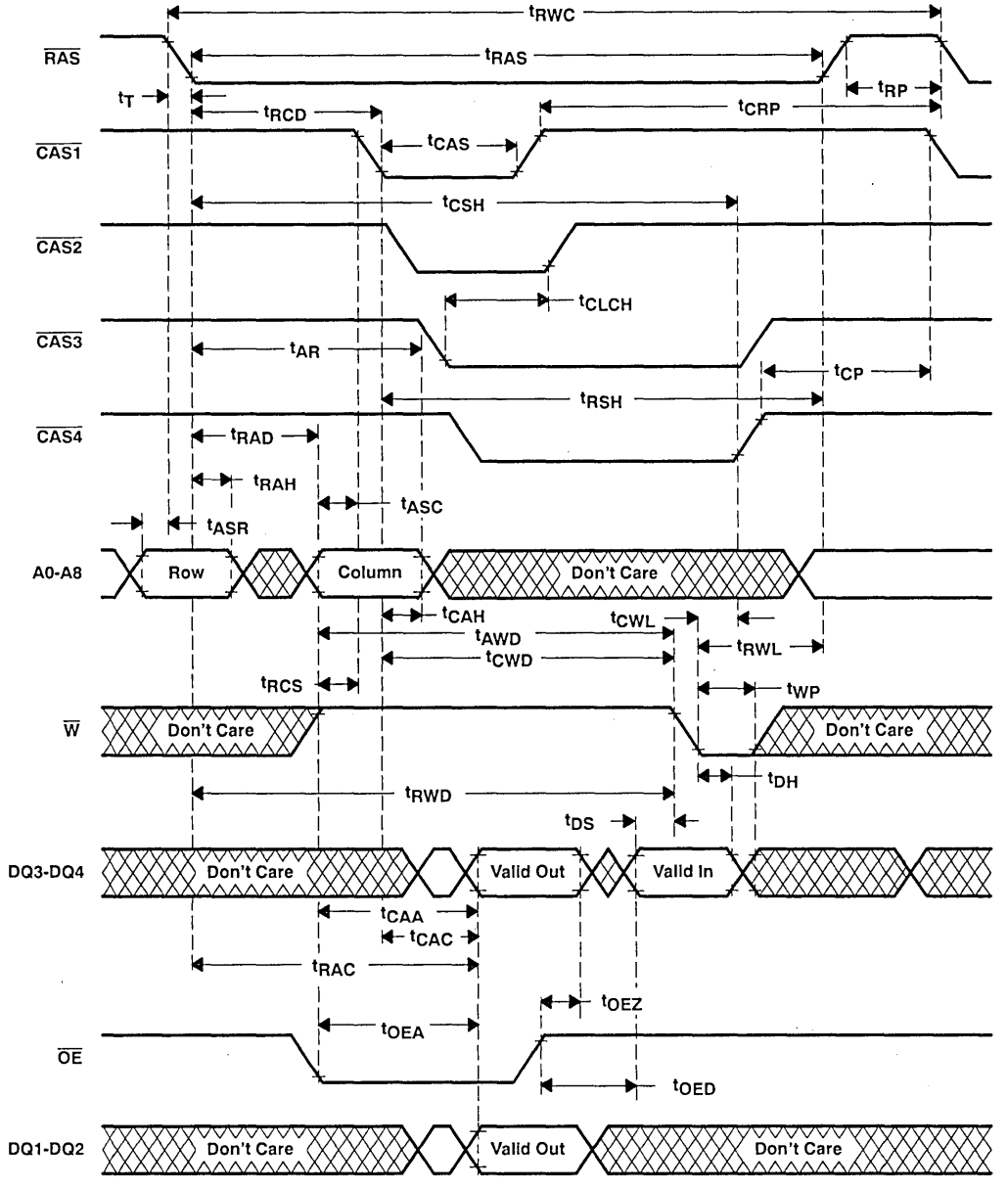
NOTES: 10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
17. In order to hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
18. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
19. $\overline{CASx}$ order is arbitrary.

early write cycle timing



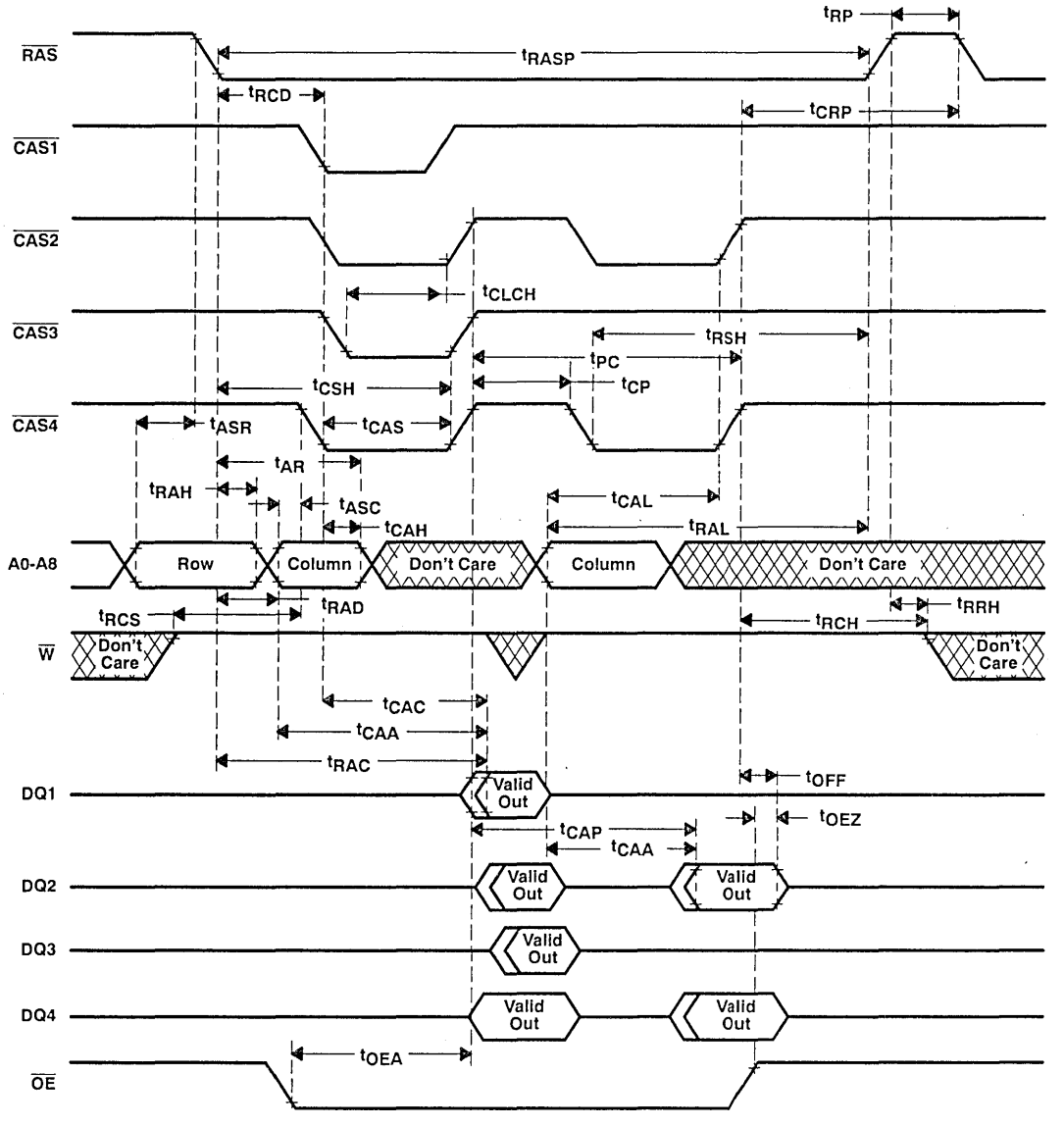
NOTES: 17. In order to hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
18. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
19. $\overline{CASx}$ order is arbitrary.

read-write/read-modify-write cycle



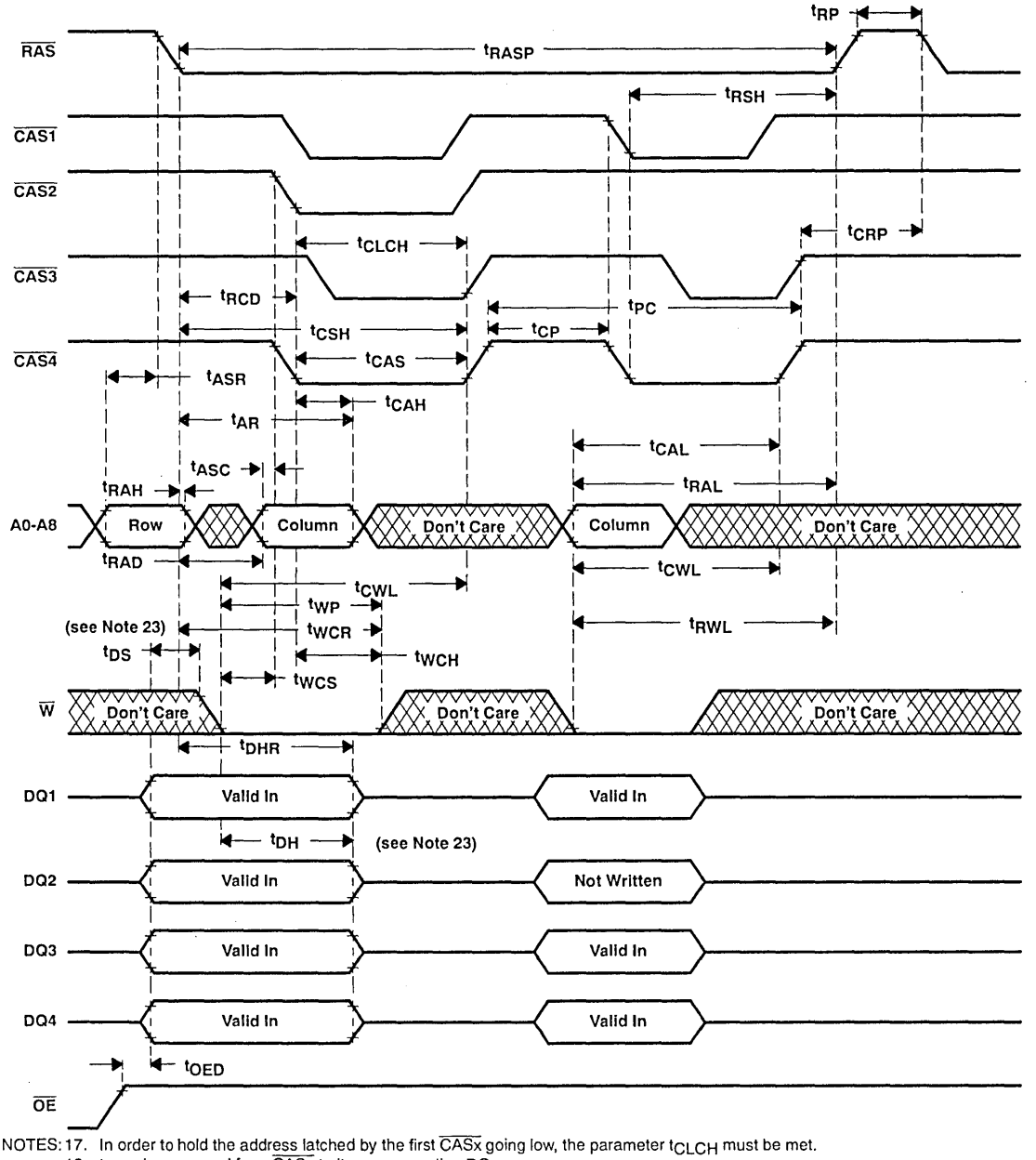
NOTES: 17. In order to hold the address latched by the first $\overline{\text{CAS}}$x going low, the parameter t_{CLCH} must be met.
18. t_{CAC} is measured from $\overline{\text{CAS}}$x to its corresponding DQx.
19. $\overline{\text{CAS}}$x order is arbitrary.

enhanced page-mode read cycle timing



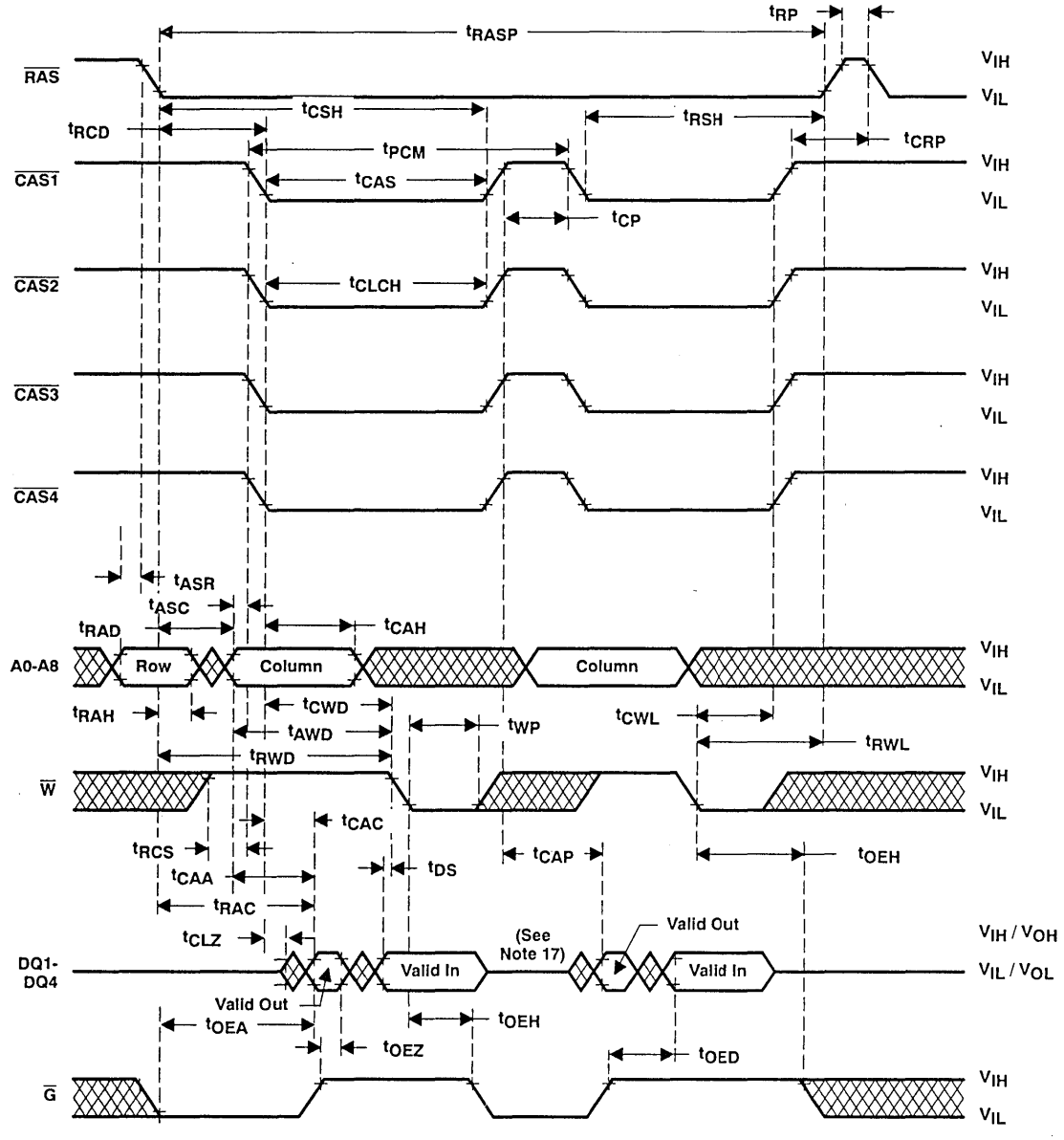
NOTES: 17. In order to hold the address latched by the first $\overline{CAS}x$ going low, the parameter t_{CLCH} must be met.
18. t_{CAC} is measured from $\overline{CAS}x$ to its corresponding DQx.
19. $\overline{CAS}x$ order is arbitrary.
20. Output may go from high-impedance to an invalid data state prior to the specified access time.
21. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
22. Access time is t_{CAP} or t_{CAA} dependent.

enhanced page-mode write cycle timing



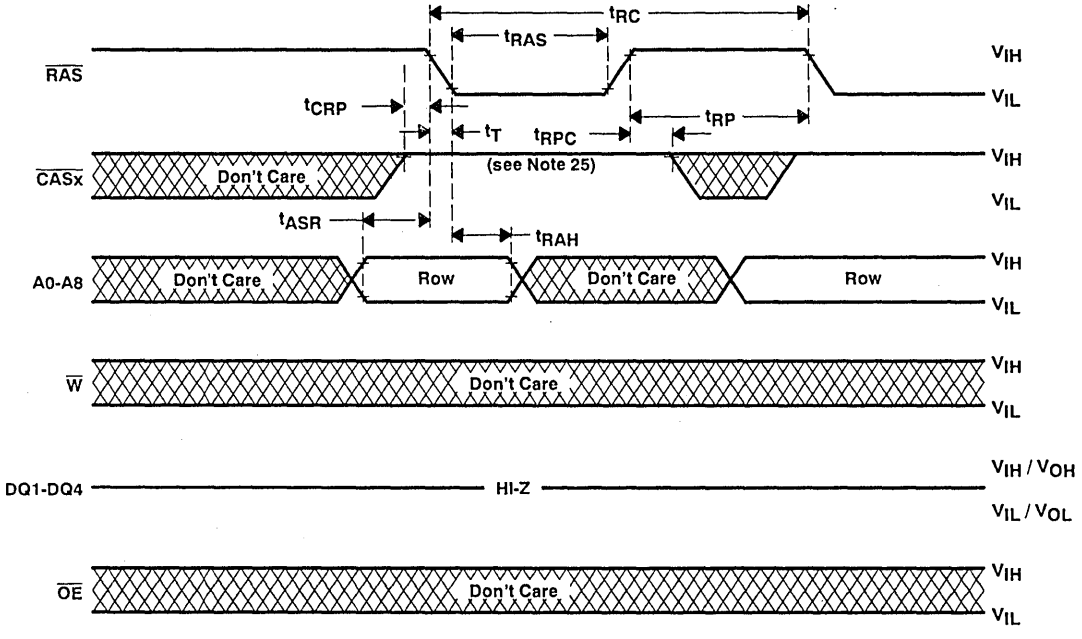
NOTES: 17. In order to hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
18. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
19. $\overline{CASx}$ order is arbitrary.
21. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
23. Referenced to $\overline{CASx}$ or $\overline{W}$, whichever occurs last.

enhanced page mode read-modify-write cycle



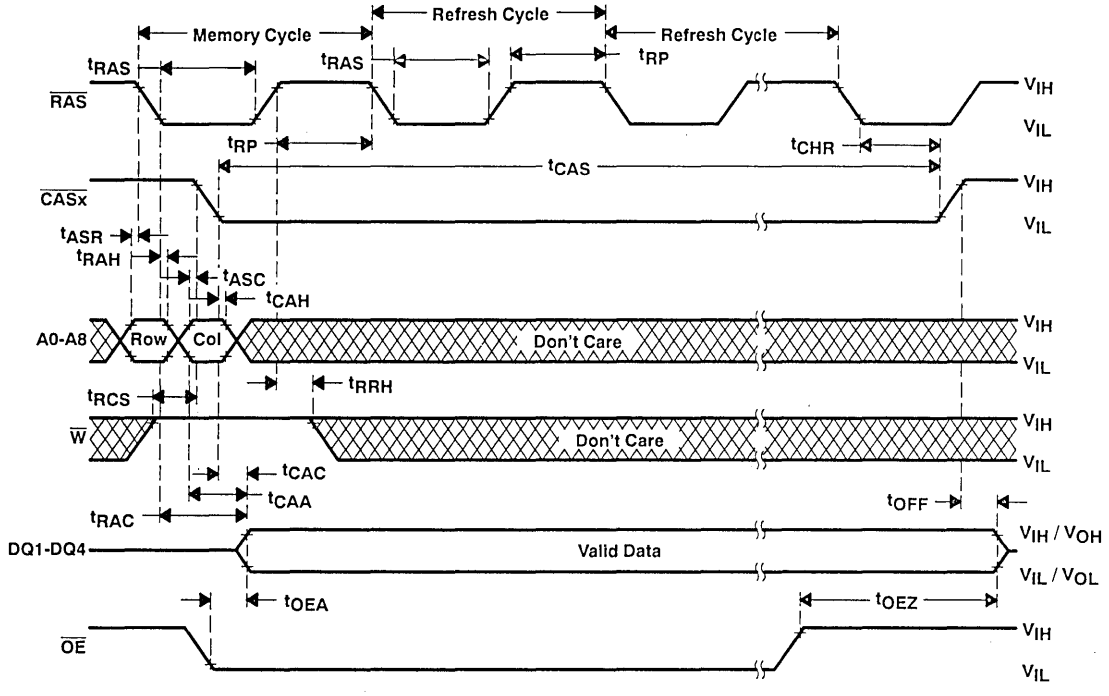
NOTES: 17. In order to hold the address latched by the first $\overline{CAS}x$ going low, the parameter t_{CLCH} must be met.
18. t_{CAC} is measured from $\overline{CAS}x$ to its corresponding DQx.
19. $\overline{CAS}x$ order is arbitrary.
24. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.

$\overline{RAS}$-only refresh timing

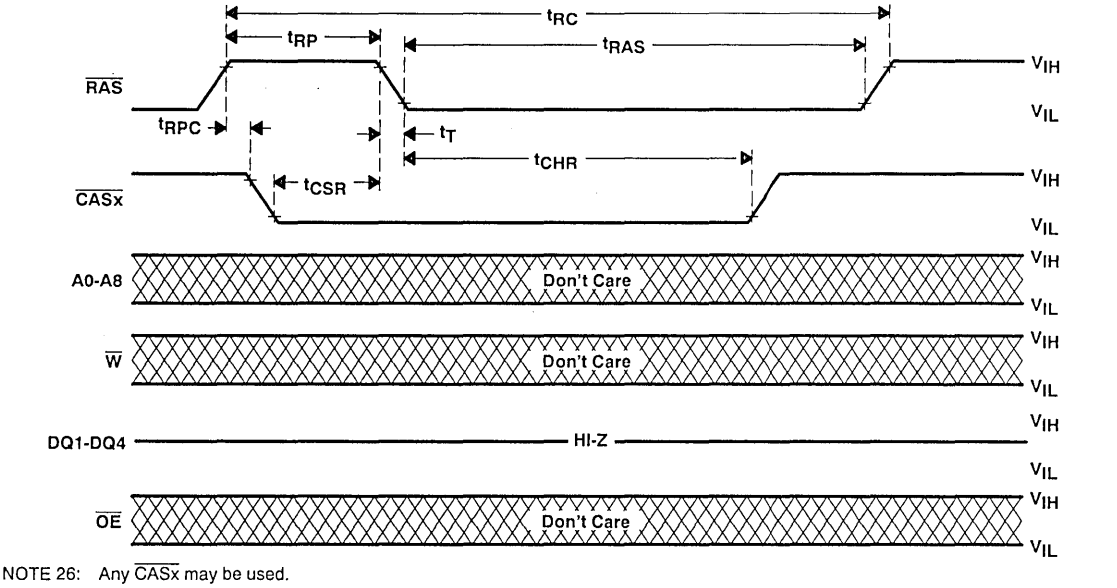


NOTE 25: All $\overline{CAS}$x must be high.

hidden refresh cycle



automatic (CAS-before-RAS) refresh cycle timing



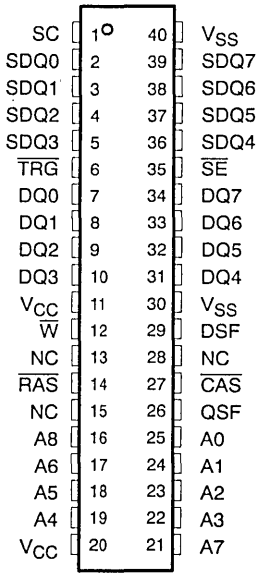
NOTE 26: Any CASx may be used.

- DRAM: 131 072 Words × 8 Bits
  SAM: 256 × 8 Bits
- Dual Port Accessibility — Simultaneous and Asynchronous Access From the DRAM and SAM Ports
- Bidirectional Data Transfer Function Between the DRAM and the Serial Data Register
- 4 × 8-Block Write Feature for Fast Area Fill Operations. As Many as Four Memory Address Locations Written Per Cycle From an On-Chip Color Register
- Write-Per-Bit Feature for Selective Write to Each RAM I/O. Two Write-Per-Bit Modes to Simplify System Design
- Enhanced Page-Mode Operation for Faster Access
- $\overline{CAS}$-before-$\overline{RAS}$ and Hidden Refresh Modes
- Long Refresh Period . . . Every 8 ms (Max)
- Up to 33 MHz Uninterrupted Serial Data Streams
- Split Serial Data Register for Simplified Realtime Register Reload
- 3-State Serial I/Os Allow Easy Multiplexing of Video Data Streams
- 256 Selectable Serial Register Starting Locations
- All Input/Outputs and Clocks TTL Compatible
- Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX) $t_{a(R)}$	ACCESS TIME COLUMN ENABLE (MAX) $t_{a(C)}$	ACCESS TIME SERIAL DATA (MAX) $t_{a(SQ)}$	ACCESS TIME SERIAL ENABLE (MAX) $t_{a(SE)}$
TMS48C121-80	80 ns	20 ns	25 ns	20 ns
TMS48C121-10	100 ns	25 ns	30 ns	20 ns
TMS48C121-12	120 ns	30 ns	35 ns	25 ns

- Texas Instruments EPIC™ CMOS Process

DZ Package
(Top View)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column Enable
DQ0-DQ7	DRAM Data In-Out/Write Mask Bit
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row Enable
SC	Serial Data Clock
SDQ0-SDQ7	Serial Data In-Out
$\overline{TRG}$	Transfer Register/Q Output Enable
$\overline{W}$	Write Mask Select/Write Enable
DSF	Special Function Select
QSF	Split-Register Activity Status
V_{CC}	5-V Supply (TYP)
V_{SS}	Ground
NC	No External Connect

ADVANCE INFORMATION

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description

The TMS48C121 multiport video RAM is a high-speed dual-ported memory device. It consists of a dynamic random-access memory (DRAM), organized as 131 072 words of 8-bits each interfaced to a serial data register, or Serial Access Memory (SAM), organized as 256 words of 8-bits each. The TMS48C121 supports three basic types of operation: random access to and from the DRAM, serial access to and from the serial register, and bidirectional transfer of data between any row in the DRAM and the serial register. Except during transfer operations, the TMS48C121 can be accessed simultaneously and asynchronously from the DRAM and SAM ports. During transfer operation, the 256 columns of the DRAM are connected to the 256 positions in the serial data register. The 256 × 8-bit serial data register can be loaded from the memory row (transfer read) or else the contents of the 256 × 8-bit serial data register can be written to the memory row (transfer write).

The TMS48C121 is equipped with several features designed to provide higher system-level bandwidth and simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's 4 × 8-Block Write mode. The Block Write mode allows eight bits of data present in an on-chip color data register to be written to any combination of four adjacent column address locations. As many as 32 bits of data can be written to memory during each $\overline{CAS}$ cycle time. Also on the DRAM port, a write mask or a write-per-bit allows masking any combination of the 8 input/outputs on any write cycle. The persistent write-per-bit feature uses a mask register which, once loaded, can be used on subsequent write cycles. The mask register eliminates having to provide mask data on every mask write cycle.

On the serial register, or SAM port, the TMS48C121 offers a split-register transfer read (DRAM to SAM) option that enables realtime register reload implementation for truly continuous serial data streams, without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. This new realtime register reload implementation allows truly continuous serial data. For applications not requiring realtime register reload (for example, reloads done during CRT retrace periods), the single-register mode of operation is retained to simplify system design. The SAM can also be configured in input mode, accepting serial data from an external device. Once the serial register within the SAM is loaded, its contents can be transferred to the corresponding column positions in any row in memory in a single memory cycle.

The SAM port is designed for maximum performance. Data can be input to or accessed from the SAM at serial rates up to 33 MHz. During the split-register mode of operation, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate output, designated QSF, is included to indicate which half of the serial register is active at any given time in the split register mode.

All inputs, outputs, and clock signals on the TMS48C121 are compatible with Series 74 TTL. All address lines and data-in are latched on-chip to simplify system design. All data-outs are unlatched to allow greater system flexibility.

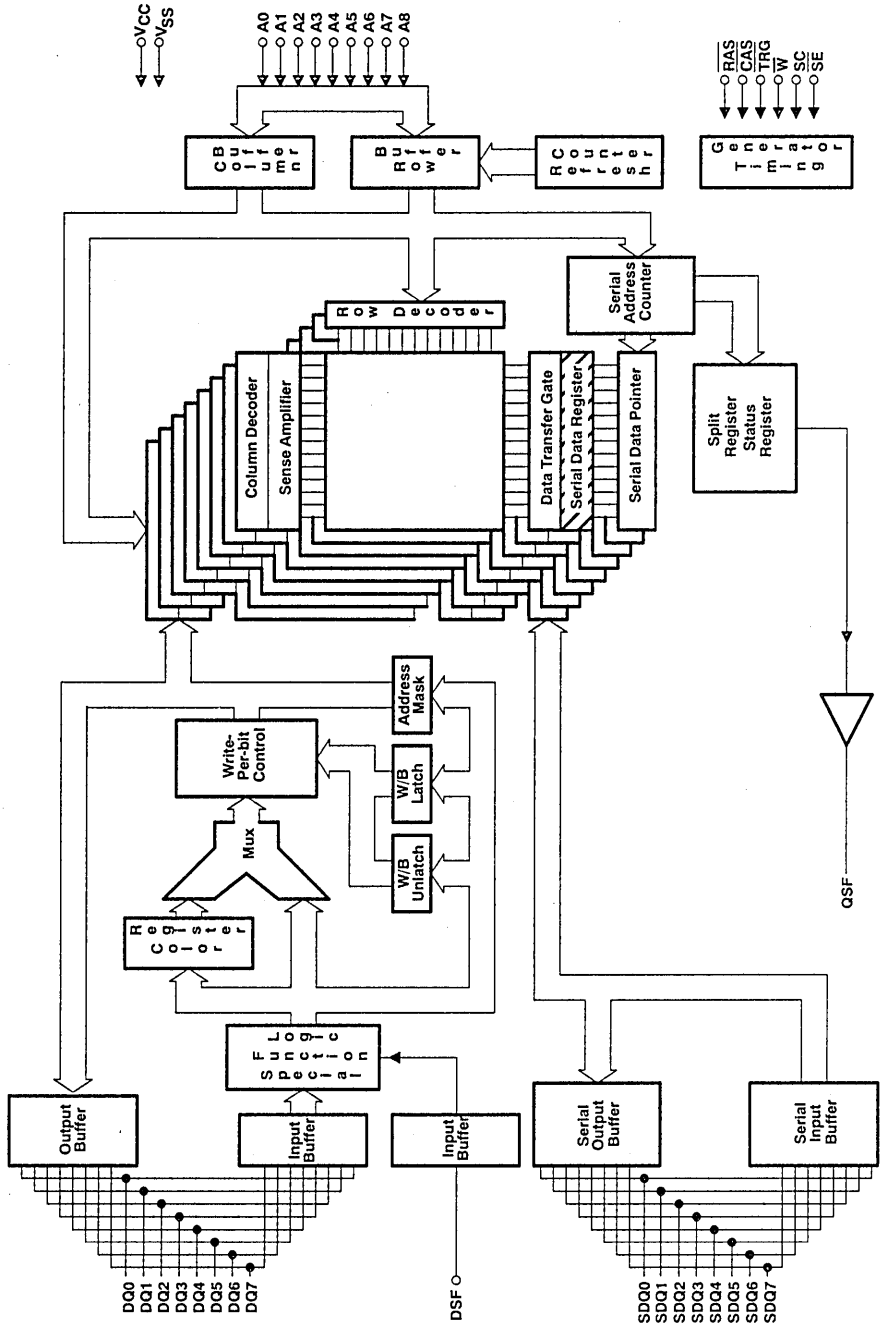
Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row address setup, row address hold, and address multiplex is thus eliminated, and a memory cycle time reduction of up to 3 × can be achieved, compared to minimum $\overline{RAS}$ cycle times. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and page-mode cycle time used. The TMS48C121 allows a full page (256 cycles) of information to be accessed in read, write, or read-modify-write mode during a single $\overline{RAS}$ low period using relatively conservative page-mode cycle times.

The TMS48C121 employs state-of-the-art Texas Instruments EPIC™ scaled-CMOS, double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The TMS48C121 is offered in a 40-pin small-outline J-lead package (DZ suffix) for direct surface mounting in rows on 400-mil (5,08-mm) centers.

The TMS48C121 and other Multiport Video RAMs are supported by a broad line of graphics processor and control devices from Texas Instruments, including the TMS34010 and TMS34020 Computer Video Products.

functional block diagram



Detailed Pin Description vs Operational Mode

PIN	DRAM	TRANSFER	SAM
A0-A8	Row, Column Address	Row, Tap Address	
$\overline{CAS}$	Column Enable, DQ Output Enable	Tap Address Strobe	
DQ	DRAM Data I/O, Write Mask Bits		
DSF	Block Write Enable	Split Register Enable	
	Persistent Write-Per-Bit Enable	Alternate Write Transfer Enable	
	Color Register Load Enable		
$\overline{RAS}$	Row Enable	Row Enable	
$\overline{SE}$		Serial-In Mode Enable	Serial Enable
SC			Serial Clock
SDQ			Serial Data I/O
$\overline{TRG}$	Q Output Enable	Transfer Enable	
$\overline{W}$	Write Enable, Write-Per-Bit Select	Transfer Write Enable	
QSF			Split Register Active Status
NC	Not Connected to External V_{SS}		
V_{CC}†	5-V Supply		
V_{SS}†	Ground		

† For proper device operation, both V_{CC} pins must be connected to a 5-V supply and both V_{SS} pins must be tied to ground.

operation

random access operation

Refer to Table 1, Functional Truth Table, for Random Access and Transfer Operations. Random access operations are denoted by the designator "R" and transfer operations are denoted by a "T".

transfer register select and DQ enable ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either register or random access operation as $\overline{RAS}$ falls. For the random access (DRAM) mode, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. Asserting $\overline{TRG}$ high as $\overline{RAS}$ falls causes the 256 storage elements of each data register to remain disconnected from the corresponding 256-bit lines of the memory array. (Asserting $\overline{TRG}$ low as $\overline{RAS}$ falls connects the 256-bit positions in the serial register to the bit lines and indicates that a transfer will occur between the data registers and the selected memory row. (See "Transfer Operation" for details.)

During random access operations, $\overline{TRG}$ also functions as an output enable for the random (Q) outputs. Whenever $\overline{TRG}$ is held high, the Q outputs are in the high-impedance state to prevent an overlap between the address and DRAM data. This organization allows the connection of the address lines to the data I/O lines but prohibits the use of the early write cycle. It also allows read-modify-write cycles to be performed by providing a three-state condition to the common I/O pins so that write data can be driven onto the pins after output read data has been externally latched.

address (A0 through A8)

Seventeen address bits are required to decode 1 of 131 072 storage cell locations. Nine row address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Then, eight column address bits are set up on pins A0 through A7 and latched onto the chip on the falling edge of $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

$\overline{RAS}$ and $\overline{CAS}$ address strobes and device control clocks

$\overline{RAS}$ is a control input that latches the states of the row address, $\overline{W}$, $\overline{TRG}$, $\overline{SE}$, $\overline{CAS}$, and DSF onto the chip to invoke the various DRAM and transfer functions of the TMS48C121. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is a control input that latches the states of the column address and DSF to control various DRAM and transfer functions. $\overline{CAS}$ also acts as an output enable for the DRAM output pins.

special function select (DSF)

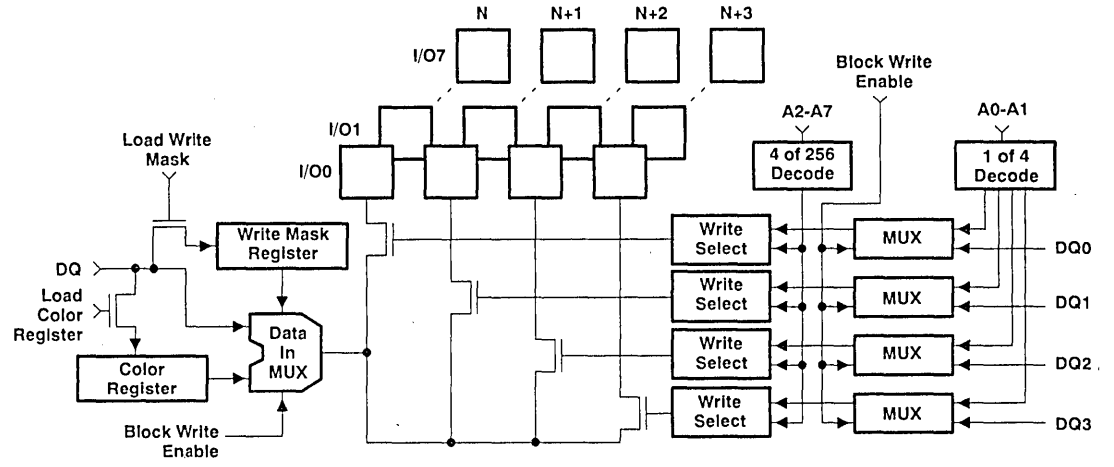
The Special Function Select input is latched on the falling edges of $\overline{RAS}$ and $\overline{CAS}$, similarly to an address, and serves four functions. First, during write cycles DSF invokes persistent write-per-bit operation. If $\overline{TRG}$ is high, $\overline{W}$ is low, and DSF is low on the falling edge of $\overline{RAS}$, the write mask will be reloaded with the data present on the DQ pins. If DSF is high, the mask will not be reloaded but will retain the data from the last mask reload cycle.

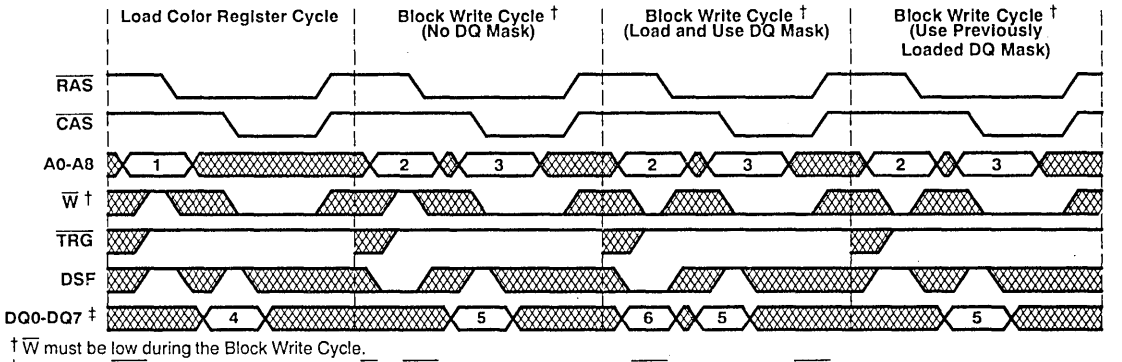
Secondly, the DSF is used to change the internally stored write per bit mask register (or write mask) via the load write mask cycle. The data present on the DQ pins when $\overline{W}$ falls is written to the write mask rather than to the addressed memory location. See "Delayed Write Cycle Timing" and the accompanying "Write Cycle State Table" in the timing diagram section. Once the write mask is loaded, it can be used on subsequent masked write per bit cycles. This feature allows systems with a common address and data bus to use the write-per-bit feature, eliminating the time needed for multiplexing the write mask and input data on the data bus.

Third, the DSF is used to load an on-chip four-bit data, or "color," register via the Load Color Register cycle. The contents of this register can subsequently be written to any combination of four adjacent column memory locations using an 4 × 8-Block Write feature. The load color register cycle is performed using normal write cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Once the color register is loaded, it retains data until power is lost or until another load register cycle is performed.

After loading the color register, the block write cycle can be enabled by holding DSF high on the falling edge of $\overline{CAS}$. During block write cycles, only the six most significant column addresses (A2-A7) are latched on the falling edge of $\overline{CAS}$. The two least significant addresses (A0-A1) are replaced by four DQ bits (DQ0, DQ1, DQ2, and DQ3), which are also latched on the later of $\overline{CAS}$ or $\overline{W}$ falling. These four bits are used as an address mask or column select and indicate which of the four column address locations addressed by A2-A7 will be written with the contents of the color register during the write cycle. DQ0 enables a write to column address A1 = 0 (A1 low), A0 = 0 (A0 low) DQ1 enables a write to column address A1 = 0 (A1 low), A0 = 1 (A0 high); DQ2 enables a write to column address A1 = 1 (A1 high), A0 = 0 (A0 low); and DQ3 enables a write to column address A1 = 1 (A1 high), A0 = 1 (A0 high). A high logic level enables a write and a low logic level disables the write. A maximum of 32 bits can be written to memory during each $\overline{CAS}$ cycle (see Figure 1, Block Write Diagram).

Fourth, the DSF pin is used to invoke the split register transfer and serial access operation described in the sections "Transfer Operation" and "Serial Operation."





† W must be low during the Block Write Cycle.
‡ DQ0-DQ7 (CAS) are latched on the later of W or CAS falling edge. DQ0-DQ7 (RAS) are latched on RAS falling edge.
Legend:

1. Refresh Address
2. Row Address
3. Column Start Address (A0-A8)
4. Color Register Data
5. Column Mask Data
6. DQ Mask Data

= Don't Care

Figure 1. Block Write Diagram

write enable, write-per-bit enable and persistent write-per-bit enable (W)

The W pin enables data to be written to the DRAM and also is used to select the DRAM write-per-bit mode of operation. A logic high level on the W input selects the read mode and logic low level selects the write mode. In an Early Write cycle, W is brought low before CAS and the DRAM output pins (DQ) remain in the high-impedance state for the entire cycle. During DRAM write cycles, holding W low on the falling edge of RAS will invoke the write-per-bit operation. Two modes of write-per-bit operation are supported.

Case 1. If DSF is low on the falling edge of $\overline{RAS}$, the write mask is reloaded. Accordingly, a four-bit binary code (the write-per-bit mask) is input to the device via the random DQ pins and is latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the four random I/Os are written and which are not. After $\overline{RAS}$ has latched the write mask on-chip, input data is driven onto the DQ pins and is latched on the falling edge of the later of $\overline{CAS}$ or $\overline{W}$. If a low was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will not be written to that I/O. If a high was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will be written to that I/O.

Case 2. If DSF is high on the falling edge of $\overline{RAS}$, the mask is not reloaded from the DQ pins but instead retains the value stored during the last write-per-bit mask reload. This mode of operation is known as *persistent write-per-bit*, since the write-per-bit mask is persistent over an arbitrary number of cycles.

See the corresponding timing diagrams for details. IMPORTANT: The write-per-bit operation is invoked only if $\overline{W}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{W}$ is held high on the falling edge of $\overline{RAS}$, write-per-bit is not enabled and the write operation will be performed to all 8 inputs.

data I/O (DQ0-DQ7)

DRAM data is written during a write or read-modify-write cycle. The falling edge of $\overline{W}$ strobes into the on-chip data latches. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by early $\overline{CAS}$ with data setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low. Thus, the data will be strobed-in by $\overline{W}$ with data setup and hold times referenced to this signal.

The three-state output buffers provide direct TTL compatibility (no pull-up resistors) with a fanout of two Series 74 TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance (floating) state as long as $\overline{CAS}$ or $\overline{TRG}$ is held high. Data will not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low. Once the outputs are valid, they remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. $\overline{CAS}$ or $\overline{TRG}$ going high returns the outputs to a high-impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a register transfer operation (memory to register or register to memory), the outputs remain in the high-impedance state for the entire cycle.

refresh

A refresh operation must be performed to each row at least once every eight milliseconds to retain data. Since the output buffer is in the high-impedance state (unless $\overline{CAS}$ is applied), the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$. The external row address is ignored and the refresh address is generated internally when using $\overline{CAS}$-before-$\overline{RAS}$ refresh. 512 cycles must be performed within eight milliseconds, but not necessarily in succession. Other cycles may be performed in between $\overline{CAS}$-before-$\overline{RAS}$ cycles without disturbing the internal address generation.

NC

The pins should be tied to system ground or left floating (no connection) for proper device operation.

IMPORTANT: NC is not connected internally to V_{SS}.

Table 1. Function Table

TYPE†	RAS FALL					CAS FALL	ADDRESS		DQ0-DQ7		FUNCTION
	CAS	TRG	W¶	DSF	SE	DSF	RAS	CAS	RAS	CAS‡ W	
R	L	X§	X	X	X	X	X	X	X	X	CAS-before-RAS refresh
T	H	L	L	X	L	X	Row Addr	Tap Point	X	X	Register to memory transfer (Transfer Write)
T	H	L	L	H	X	X	Row Addr	Tap Point	X	X	Alternate transfer write (Independent of SE)
T	H	L	L	L	H	X	Refresh Addr	Tap Point	X	X	Serial write-mode enable (Psuedo-transfer write)
T	H	L	H	L	X	X	Row Addr	Tap Point	X	X	Memory to register transfer (Transfer read)
T	H	L	H	H	X	X	Row Addr	Tap Point	X	X	Split register transfer read (Must reload tap)
R	H	H	L	L	X	L	Row Addr	Col Addr	Write Mask	Valid Data	Load and use write mask, write data to DRAM
R	H	H	L	L	X	H	Row Addr	Col A2-A7	Write Mask	Addr Mask	Load and use write mask, block write to DRAM
R	H	H	L	H	X	L	Row Addr	Col Addr	X	Valid Data	Persistent write per bit, write data to DRAM
R	H	H	L	H	X	H	Row Addr	Col A2-A7	X	Addr Mask	Persistent write per bit, block write to DRAM
R	H	H	H	L	X	L	Row Addr	Col Addr	X	Valid Data	Normal DRAM read/write (Non masked)
R	H	H	H	L	X	H	Row Addr	Col A2-A7	X	Addr Mask	Block write to DRAM (Non masked)
R	H	H	H	H	X	L	Refresh Addr	X	X	Write Mask	Load write mask
R	H	H	H	H	X	H	Refresh Addr	X	X	Color Data	Load color register

† R = Random access operation; T = Transfer operation
‡ DQ0-DQ7 are latched on the later of W or CAS falling edge.
§ X = Don't care
¶ In persistent write-per-bit function, W must be high during the refresh cycle.
Addr Mask = H: Write to address/column location enabled (DQ0, DQ1, DQ2, DQ3).
Write Mask = H: Write to I/O enabled.

random port to serial port interface

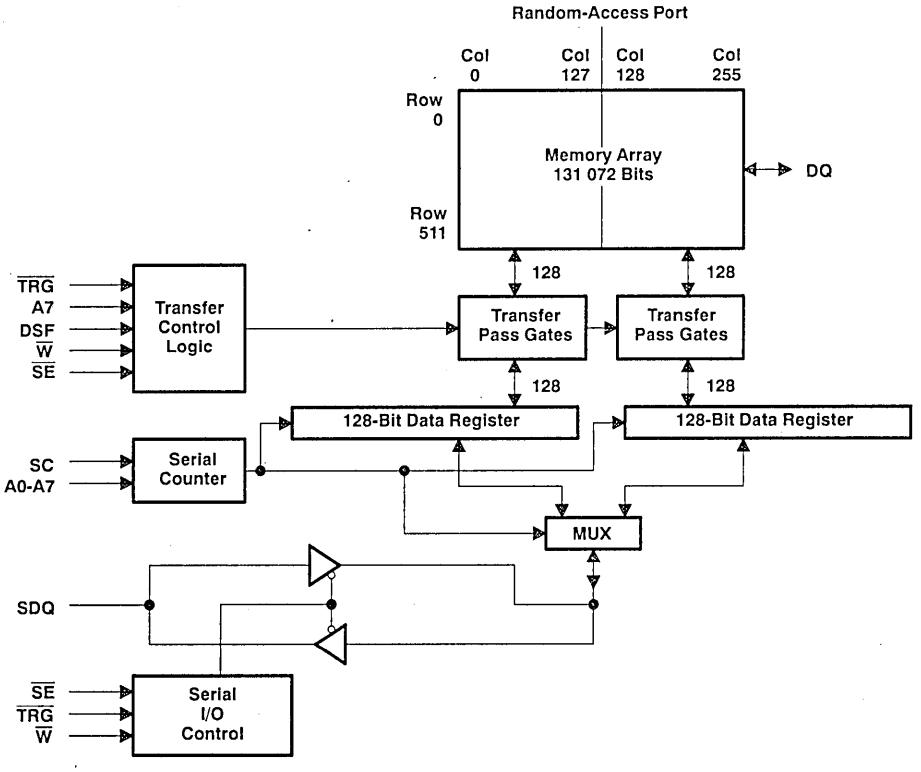


Figure 1. Block Diagram Showing One Random and One Serial I/O Interface

random-address space to serial-address space mapping

The 256 bits in each of the eight data registers of the SAM are connected to the 256 column locations of each of the eight random I/Os. Data can be accessed in or out of the SAM starting at any of the 256 data bit locations. This start location is selected by addresses A0 through A7 on the falling edge of $\overline{CAS}$ during any transfer cycle. The SAM is accessed starting from the selected start address, proceeding from the lowest to the highest significant bits. After the most significant bit position (255) is accessed, the serial counter wraps around such that bit 0 is accessed on the next clock pulse. The selected start address is stored and used for all subsequent transfer cycles until $\overline{CAS}$ is again brought low during any transfer cycle. Thus, the start address can be set once and $\overline{CAS}$ held high during all subsequent transfer cycles and the start address point will not change regardless of data present on A0 through A7.

split-register mode random-address to serial-address space mapping

In split-register transfer operation, the serial-data register is split into halves, the low half containing bits 0 through 127 and the high half containing bits 128 through 255. When a split-register transfer cycle is performed, the "tap" address must be strobed in on the falling edge of $\overline{CAS}$. The most significant column address bit A7 determines which register half will be reloaded from the memory array. The seven remaining column address bits (A0-A6) are used to select the SAM starting location for the register half selected by A7.

To insure proper operation when using the split-register read transfer feature, a non-split register transfer must precede any split register sequence. The serial start address must be supplied for every split-register transfer. (See Split-Register Operating Sequence on page 8-123.)

transfer operations

The Serial Enable pin $\overline{SE}$ has two functions: first, it is latched on the fallilng edge of $\overline{RAS}$, with both $\overline{TRG}$ and $\overline{W}$ low to select one of the transfer functions. If $\overline{SE}$ is low during this transition, then a transfer write occurs. If $\overline{SE}$ is high as $\overline{RAS}$ falls and DSF is low, then a write mode control cycle is performed. The function of this cycle is to switch the SDQs from the output mode to the input mode, thus allowing data to be shifted into the data register.

NOTE: All transfer-write modes will switch the SDQs from the output mode to the input mode. All transfer read and serial mode enable (psuedo transfer write) operations will perform a memory refresh operation on the selected row.

As illustrated in Table 1, the TMS48C121 supports five basic modes of transfer operation:

1. Normal Write Transfer (SAM to DRAM)
2. Alternate Write Transfer (independent of the state of $\overline{SE}$)
3. Pseudo Write Transfer (Switches serial port from serial out mode to serial in mode. No actual data transfer takes place between the DRAM and the SAM.)
4. Normal Read Transfer (Transfer entire contents of DRAM row to SAM)
5. Split-Register Read Transfer (Divides the SAM into a high and a low half. Only one half is transferred to the SAM while the other half is read from the serial I/O port.)

Note: All transfer write modes will switch the SDQ's from the output mode into the input mode.

transfer register select ($\overline{TRG}$)

Transfer operations between the memory array and the data registers are invoked by bringing $\overline{TRG}$ low before $\overline{RAS}$ falls. The states of $\overline{W}$, $\overline{SE}$, and DSF, which are also latched on the falling edge of $\overline{RAS}$, determine which transfer operation will be invoked.

During read transfer cycles, $\overline{TRG}$ going high causes the addressed row of data to be transferred into the data register. Although the previous data in the data register is overwritten, the last bit of data appearing at SDQ before $\overline{TRG}$ goes high will remain valid until the first positive transition of SC after $\overline{TRG}$ goes high. The data at SDQ will then switch to new data beginning from the selected start, or "tap" position.

transfer write enable ($\overline{W}$)

In the register-transfer mode, $\overline{W}$ determines whether a read or a write transfer will occur. To perfom a write transfer, $\overline{W}$ and $\overline{SE}$ are held low as $\overline{RAS}$ falls except for alternate transfer-write. If $\overline{SE}$ is high during this transition, no transfer of data from the data register to the memory array occurs, but the SDQs are put into the input mode. This allows serial data to be input into the SAM. An alternative way to perform the transfer-write cycle is by holding DSF high on the falling edge of $\overline{RAS}$. In this way, the state of $\overline{SE}$ is a don't care as $\overline{RAS}$ falls. To perform a read transfer operation, $\overline{W}$ is held high and $\overline{SE}$ is a don't care as $\overline{RAS}$ falls. This cycle also puts the SDQs into the read mode, allowing data to be shifted out of the data register.

column enable ($\overline{CAS}$)

If $\overline{CAS}$ is brought low during a pseudo write transfer cycle, the address present on the pins A0 through A7 will become the new register start location. If $\overline{CAS}$ is held high during a pseudo write transfer cycle, the previous tap address will be retained from the last transfer cycle in which $\overline{CAS}$ went low to set the tap address.

address (A0 through A8)

Nine bits are required to select one of the 512 possible rows involved in the transfer of data to or from the data registers. The states of A0-A8 are latched on the falling edge of $\overline{RAS}$ to select one of 512 rows for the transfer operation.

To select one of the 256 positions in the SAM from which the first serial data will be accessed, the appropriate 8-bit column address (A0-A7) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and start (tap) position need not be supplied every cycle, only when changing to a different start position.

In the split-register transfer mode, the most significant column address bit (A7) selects which half of the register will be reloaded from the memory array. The remaining seven addresses (A0-A6) determine the register starting location for the register to be reloaded.

special function input (DSF)

In the read-transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ selects the split-register mode transfer operation. This mode divides the serial data register into a high-order half and a low-order half; one active, and one inactive. When the cycle is initiated, a transfer occurs between the memory array and either the high-half or the low-half register, depending on the state of most significant column address bit (A7) that is strobed in on the falling edge of $\overline{CAS}$. If A7 is high, the transfer is to the high half of the register. If A7 is low, the transfer is to the low half of the register. Use of the split-register-mode read-transfer feature allows on-the-fly read transfer operation without synchronizing $\overline{TRG}$ to the serial clock.

In the write-transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ permits use of an alternate mode of transfer write. This mode allows $\overline{SE}$ to be high on the falling edge of $\overline{RAS}$ without performing a pseudo write transfer, with the serial port disabled during the entire transfer write cycle.

serial clock (SC)

Data (SDQ) is accessed in or out of the data registers on the rising edge of SC. The TMS48C121 is designed to work with a wide range of clock duty cycles to simplify system design. Since the data registers comprising the SAM are of static design, there are no SAM refresh requirements and there is no minimum SC clock operating frequency.

serial data input/output (SDQ0-SDQ7)

SD and SQ share a common I/O pin. Data is input to the device when $\overline{SE}$ is low during a write mode and data is output from the device when $\overline{SE}$ is low during read mode. The data in the SAM will be accessed in the direction from least significant bit to the most significant bit. The data registers operate modulo 256. Thus, after bit 255 is accessed, the next bits to be accessed will be bits 00, 01, 02, and so on.

serial enable ($\overline{SE}$)

During serial access operations, $\overline{SE}$ is used as an SDQ enable/disable. In the write mode, $\overline{SE}$ is used as an input enable. $\overline{SE}$ high disables the input and $\overline{SE}$ low enables the input. To take the device out of the write mode and into the read mode, a transfer read cycle must be performed. The read mode allows data to be accessed from the data register. While in the read mode, $\overline{SE}$ high disables the output and $\overline{SE}$ low enables the output.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is not disabled. Thus, external SC pulses will increment the internal serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low since the serial clock input buffer and the serial address counter are not disabled by $\overline{SE}$.

split-register active-status output (QSF)

During the split-register mode of serial access operation, QSF indicates which half of the serial register in the SAM is being accessed. If QSF is low, the serial address pointer is accessing the lower (least significant) 128 bits of the SAM. If QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM. QSF changes state upon crossing the boundary between the two register halves.

power-up

To achieve proper device operation, an initial pause of 200 μs is required after power-up, followed by a minimum of eight $\overline{RAS}$ cycles or eight $\overline{CAS}$-before-$\overline{RAS}$ cycles, a memory to register transfer cycle, and two SC cycles.

absolute maximum ratings over operating free-air temperature†

Voltage on any pin except DQ and SDQ (see Note 1) ..... – 1 V to 7 V
Voltage on DQ and SDQ (see Note 1) ..... – 1 V to 6.5 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less psoitive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions

	PARAMETER	TEST CONDITIONS	SAM PORT	TMS48C121-80		TMS48C121-10		TMS48C121-12		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 5.8, V_{CC} = 5.5 All other pins at 0 to V_{CC}			±10		±10		±10	µA
I_O	Output leakage current (see Note 3)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V			±10		±10		±10	µA
I_{CC1}	Operating current, $t_{c(RW)}$ = minimum		Standby		100		80		70	mA
I_{CC1A}	Operating current, $t_{c(SC)}$ = minimum		Active		120		95		85	
I_{CC2}	Standby current, All clocks = V_{CC}		Standby		10		10		10	
I_{CC2A}	Standby current, $t_{c(SC)}$ = minimum		Active		35		35		30	
I_{CC3}	$\overline{RAS}$-only refresh current, $t_{c(RW)}$ = minimum		Standby		100		80		70	
I_{CC3A}	$\overline{RAS}$-only refresh current, $t_{c(SC)}$ = minimum		Active		120		95		85	
I_{CC4}	Page-mode current, $t_{c(P)}$ = minimum		Standby		55		45		40	
I_{CC4A}	Page-mode current, $t_{a(SC)}$ = minimum		Active		65		55		50	
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ current, $t_{c(RW)}$ = minimum		Standby		100		80		70	
I_{CC5A}	$\overline{CAS}$-before-$\overline{RAS}$ current, $t_{c(SC)}$ = minimum		Active		120		95		85	
I_{CC6}	Data transfer current, $t_{c(RW)}$ = minimum		Standby		100		80		70	
I_{CC6A}	Data transfer current, $t_{c(SC)}$ = minimum		Active		120		95		85	

NOTE 3: $\overline{SE}$ is disabled for SDQ output leakage tests.

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 4)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write enable input		7	pF
$C_{i(SC)}$	Input capacitance, serial clock		7	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	pF
$C_{i(DSF)}$	Input capacitance, special function		7	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		7	pF
$C_{o(O)}$	Output capacitance, SDQ and DQ		7	pF
$C_{o(QSF)}$	Output capacitance, QSF		10	pF

NOTE 4: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS48C121-80		TMS48C121-10		TMS48C121-12		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{d(RLCL)}$ = Max	t_{CAC}		20		25		30	ns
$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = Max	t_{AA}		40		50		60	ns
$t_{a(CP)}$	Access time from $\overline{CAS}$ high	$t_{d(RLCL)}$ = Max	t_{CPA}		45		55		65	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = Max	t_{RAC}		80		100		120	ns
$t_{a(G)}$	Access time of Q from $\overline{TRG}$ low		t_{OEA}		20		25		30	ns
$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 30 pF	t_{SCA}		25		30		35	ns
$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 30 pF	t_{SEA}		20		20		25	ns
$t_{a(QSF)}$	Access time of QSF from SC low	C_L = 30 pF			60		60		60	ns
$t_{dis(CH)}$	Random output disable time from $\overline{CAS}$ high (see Note 6)	C_L = 30 pF	t_{OFF}	0	20	0	20	0	20	ns
$t_{dis(G)}$	Random output disable time from $\overline{TRG}$ high (see Note 6)	C_L = 30 pF	t_{OEZ}	0	20	0	20	0	20	ns
$t_{dis(SE)}$	Serial output disable time from $\overline{SE}$ high (see Note 6)	C_L = 30 pF	t_{SEZ}	0	20	0	20	0	20	ns

NOTES: 5. Switching times for RAM port output are measured with a load equivalent to 1 TTL load and 100 pF. Data out reference level: V_{OH}/V_{OL} = 2.4 V/0.8 V. Switching times for SAM port output are measured with a load equivalent to 1 TTL load and 30 pF. Serial data out reference level: V_{OH}/V_{OL} = 2 V/0.8 V.

6. $t_{dis(CH)}$, $t_{dis(G)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature†

		ALT. SYMBOL	TMS48C121-80		TMS48C121-10		TMS48C121-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 7)	t_{RC}	160		180		210		ns
$t_{c(W)}$	Write cycle time	t_{WC}	160		180		210		ns
$t_{c(rdW)}$	Read-modify-write cycle time	t_{RMW}	215		240		280		ns
$t_{c(P)}$	Page-mode read, write cycle time	t_{PC}	50		60		70		ns
$t_{c(RDWP)}$	Page-mode read-modify-write cycle time	t_{PRMW}	90		105		125		ns
$t_{c(TRD)}$	Transfer read cycle time	t_{RC}	160		180		210		ns
$t_{c(TW)}$	Transfer write cycle time	t_{WC}	160		180		210		ns
$t_{c(SC)}$	Serial clock cycle time	t_{SCC}	30		30		35		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$	t_{CPN}	10		10		15		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	20	75 000	25	75 000	30	75 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	70		70		80		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	80	75 000	100	75 000	120	75 000	ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	t_{WP}	15		25		25		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		20		25		30		ns
$t_{w(SCH)}$	Pulse duration, SC high	t_{SC}	10		10		12		ns
$t_{w(SCL)}$	Pulse duration, SC low	t_{SCP}	10		10		12		ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		0		ns
$t_{su(SFC)}$	DSF setup time before $\overline{CAS}$ low	t_{FSC}	0		0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		0		ns
$t_{su(WMR)}$	$\overline{W}$ setup time before $\overline{RAS}$ low	t_{WSR}	0		0		0		ns
$t_{su(DQR)}$	DQ setup time before $\overline{RAS}$ low	t_{MS}	0		0		0		ns
$t_{su(TRG)}$	$\overline{TRG}$ setup time before $\overline{RAS}$ low	t_{THS}	0		0		0		ns
$t_{su(SE)}$	$\overline{SE}$ setup time before $\overline{RAS}$ low	t_{ESR}	0		0		0		ns
$t_{su(SFR)}$	DSF setup time before $\overline{RAS}$ low	t_{FSR}	0		0		0		ns
$t_{su(DCL)}$	Data setup time before $\overline{CAS}$ low	t_{DSC}	0		0		0		ns
$t_{su(DWL)}$	Data setup time before $\overline{W}$ low	t_{DSW}	0		0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	Write setup time before $\overline{CAS}$ high	t_{CWL}	20		25		30		ns
$t_{su(WRH)}$	Write setup time before $\overline{RAS}$ high with $\overline{TRG}$ = $\overline{W}$ = low	t_{RWL}	20		25		30		ns
$t_{su(SDS)}$	SD setup time before SC high	t_{SDS}	3		3		3		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		20		ns
$t_{h(SFC)}$	DSF hold time after $\overline{CAS}$ low	t_{CFH}	20		20		20		ns
$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		15		ns
$t_{h(TRG)}$	$\overline{TRG}$ hold time after $\overline{RAS}$ low	t_{THH}	15		15		15		ns
$t_{h(SE)}$	$\overline{SE}$ hold time after $\overline{RAS}$ low with $\overline{TRG}$ = $\overline{W}$ = low	t_{REH}	15		15		15		ns
th(RWM)	Write mask, transfer enable hold time after $\overline{RAS}$ low	t_{RWH}	15		15		15		ns

Continued next page.

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 7. All cycle times assume t_t = 5 ns.

8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

			ALT. SYMBOL	TMS48C121-80		TMS48C121-10		TMS48C121-12		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(RDQ)}$	DQ hold time after $\overline{RAS}$ low (write mask operation)		t_{MH}	15		15		15		ns
$t_{h(SFR)}$	DSF hold time after $\overline{RAS}$ low		t_{RFH}	15		15		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 9)		t_{AR}	45		45		45		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low		t_{DH}	20		25		25		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 10)		t_{DHR}	45		50		50		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low		t_{DH}	20		25		25		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ (see Note 11)		t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ (see Note 11)		t_{RRH}	10		10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low		t_{WCH}	15		25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 10)		t_{WCR}	45		50		55		ns
$t_{h(WLG)}$	$\overline{TRG}$ hold time after $\overline{W}$ low (see Note 12)		t_{OEH}	20		25		30		ns
$t_{h(SDS)}$	SD hold time after SC high		t_{SDH}	5		5		5		ns
$t_{h(SHSQ)}$	SQ hold time after SC high		t_{SOH}	5		5		5		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high		t_{CSH}	80		100		120		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		t_{RSH}	25		25		30		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Notes 13 and 14)		t_{CWD}	45		55		65		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Notes 15 and 16)		t_{RCD}	20	60	25	75	25	90	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high		t_{RAL}	40		50		60		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)		t_{RWD}	110		130		155		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 13)		t_{AWD}	75		85		100		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 17)		t_{CHR}	20		25		25		ns
$t_{d(CLRL)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 17)		t_{CSR}	10		10		10		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 17)		t_{RPC}	5		5		5		ns
$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high		t_{CTH}	20		25		35		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ		t_{OED}	25		30		30		ns
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (see Notes 18 and 19)	Early load	t_{RTH}	$t_{h(TRG)}$		$t_{h(TRG)}$		$t_{h(TRG)}$		ns
		Mid-line real-time load		65		70		80		

Continued next page.

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].
10. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
11. Either $t_{h(RHrd)}$ or $t_{(CHrd)}$ must be satisfied for a read cycle.
12. Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.
13. Read-modify-write operation only.
14. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
15. Read cycles only.
16. The maximum value is specified only to guarantee $\overline{RAS}$ access time.
17. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only.
18. $\overline{TRG}$ may be brought high "early" when real time memory to register data transfer is not required, provided that the $t_{h(TRG)}$, $t_{d(SCTR)}$, and $t_{d(RLSH)}$ specifications are met.
19. Memory to register (read) transfer cycles only.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)†

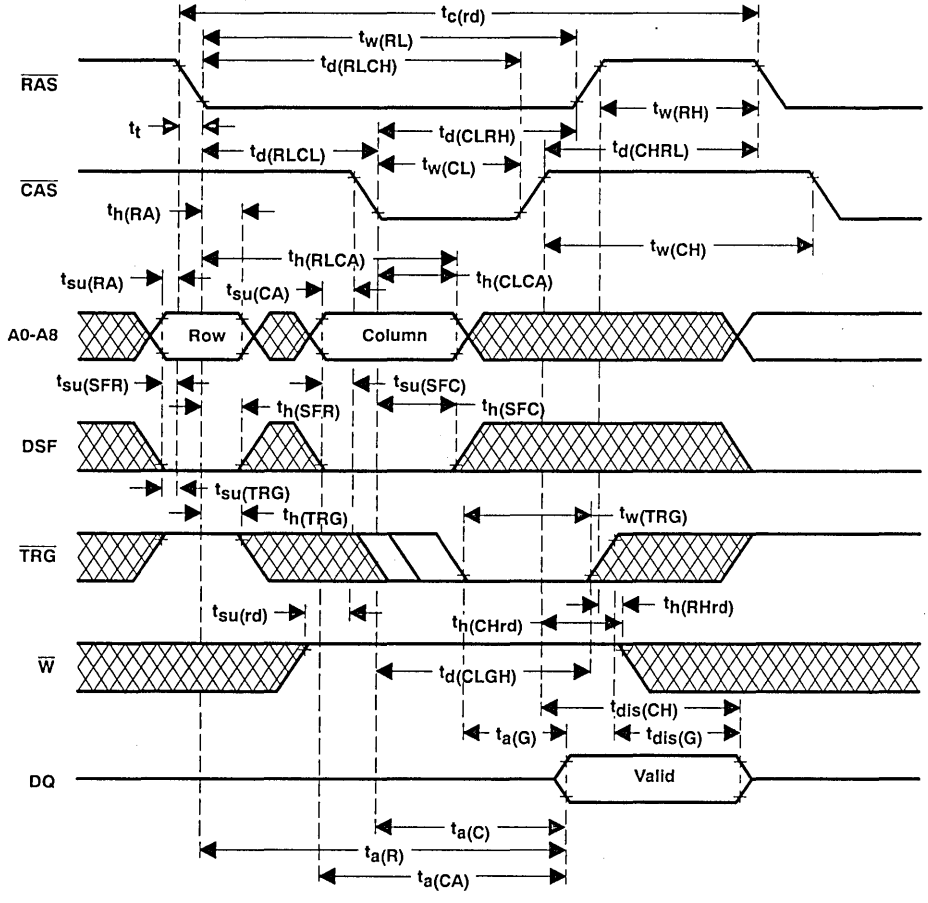
		ALT. SYMBOL	TMS48C121-80		TMS48C121-10		TMS48C121-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 19)	t_{RSD}	85		95		105		ns
$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 19)	t_{CSD}	35		40		45		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 19 and 20)	t_{TSL}	10		15		15		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 19)	t_{TRD}	– 10		– 10		– 10		ns
$t_{d(SCRL)}$	Delay time, SC high to $\overline{RAS}$ low with $\overline{TRG}$ = $\overline{W}$ = low (see Notes 21 and 22)	t_{SRS}	10		10		10		ns
$t_{d(SCSE)}$	Delay time, SC high to $\overline{SE}$ high in serial input mode		15		20		20		ns
$t_{d(RHSC)}$	Delay time, $\overline{RAS}$ high to SC high (see Note 22)	t_{SRD}	20		30		30		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 23)	t_{TRP}	$t_{w(RH)}$		$t_{w(RH)}$		$t_{w(RH)}$		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 23)	t_{TSD}	20		25		40		ns
$t_{d(SESC)}$	Delay time, $\overline{SE}$ low to SC high (see Note 24)	t_{SWS}	10		15		15		ns
$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split read transfer cycles		20		25		30		ns
$t_{d(TPRL)}$	Delay time, first (TAP) rising edge of SC after boundary switch to $\overline{RAS}$ low during split read transfer cycles		20		25		25		ns
$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 19. Memory to register (read) transfer cycles only.
20. In a transfer read cycle, the state of SC when $\overline{TRG}$ rises is a Don't Care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{TRG}$ goes high.
21. In a transfer write cycle, the state of SC when $\overline{RAS}$ falls is a Don't Care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{RAS}$ goes low.
22. Register to memory (write) transfer cycles only.
23. Memory to register (read) and register to memory (write) transfer cycles only.
24. Serial data-in cycles only.

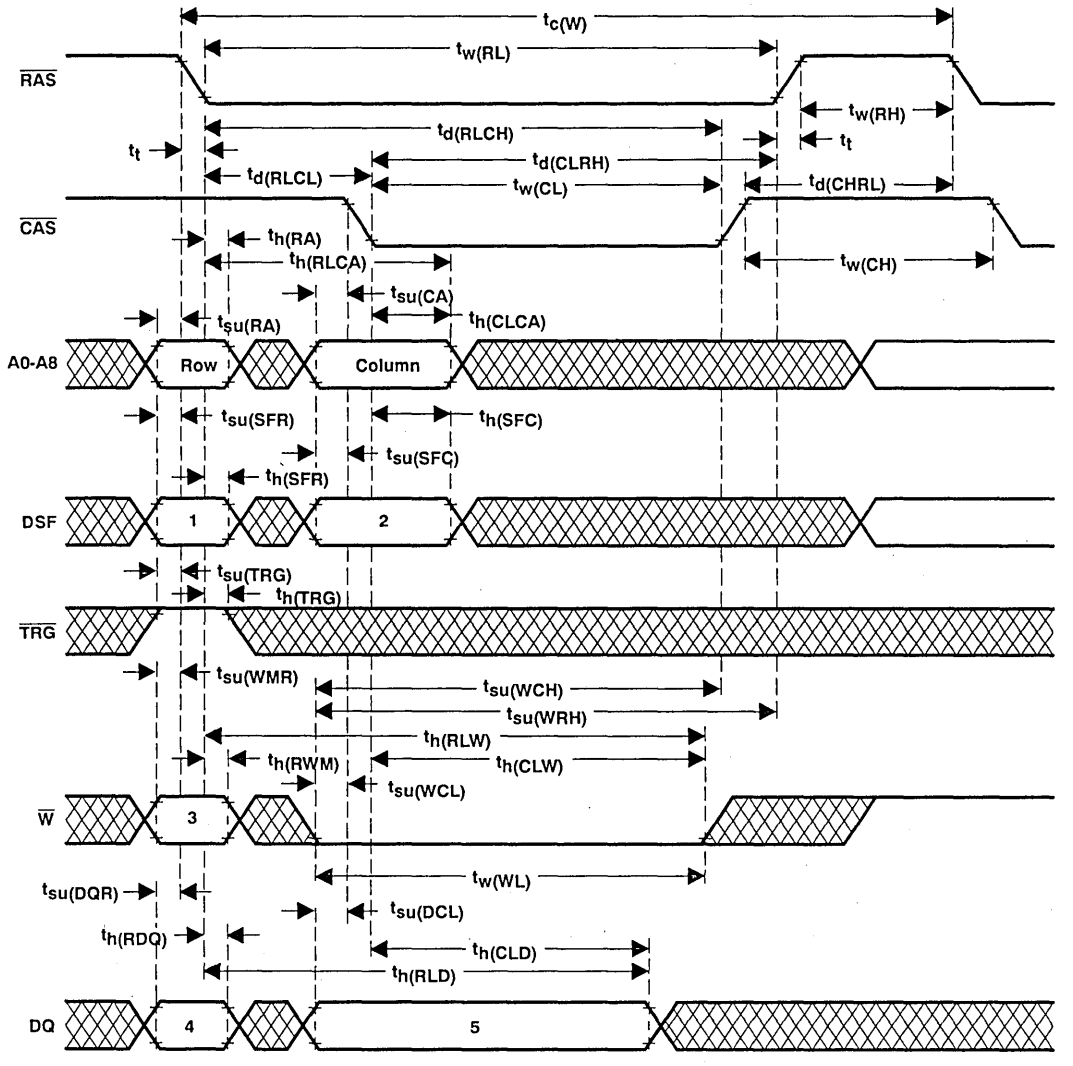
ADVANCE INFORMATION

read cycle timing



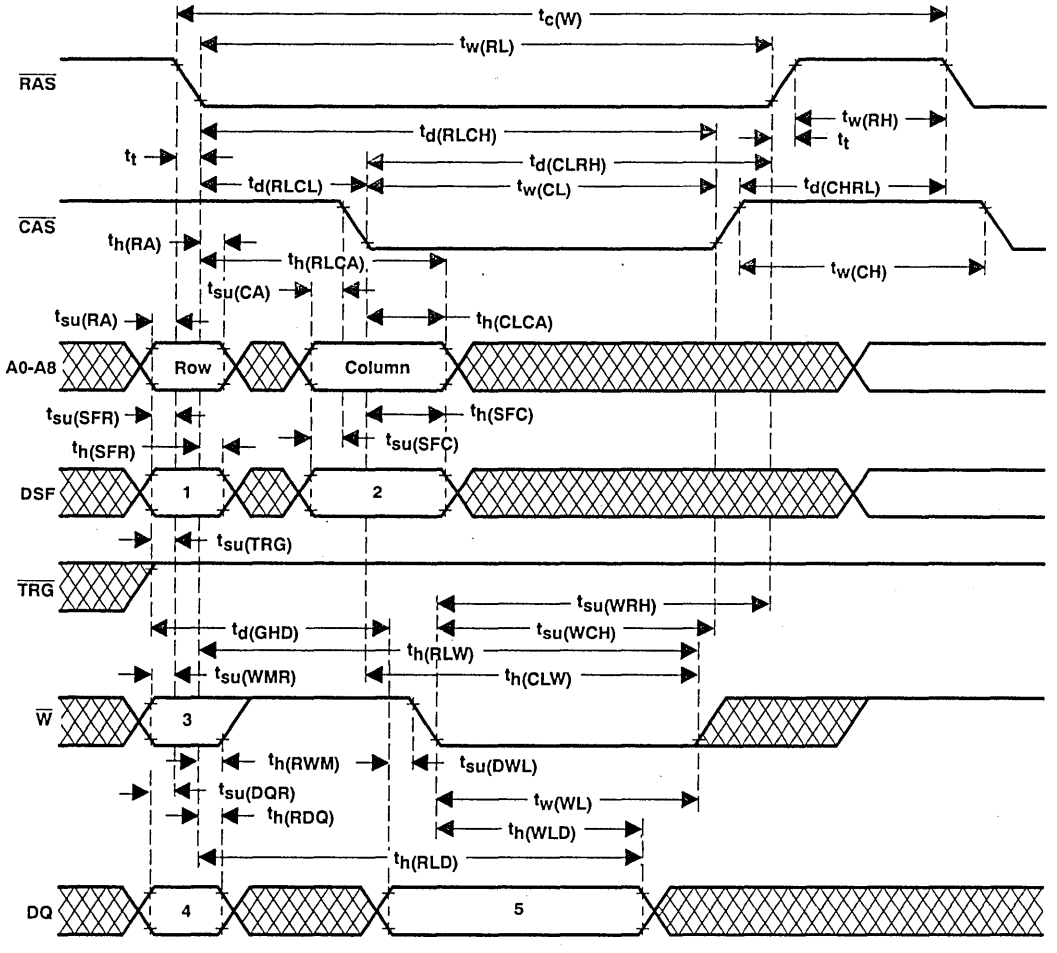
ADVANCE INFORMATION

early write cycle timing



NOTE 25: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

delayed write cycle timing



NOTE 25: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

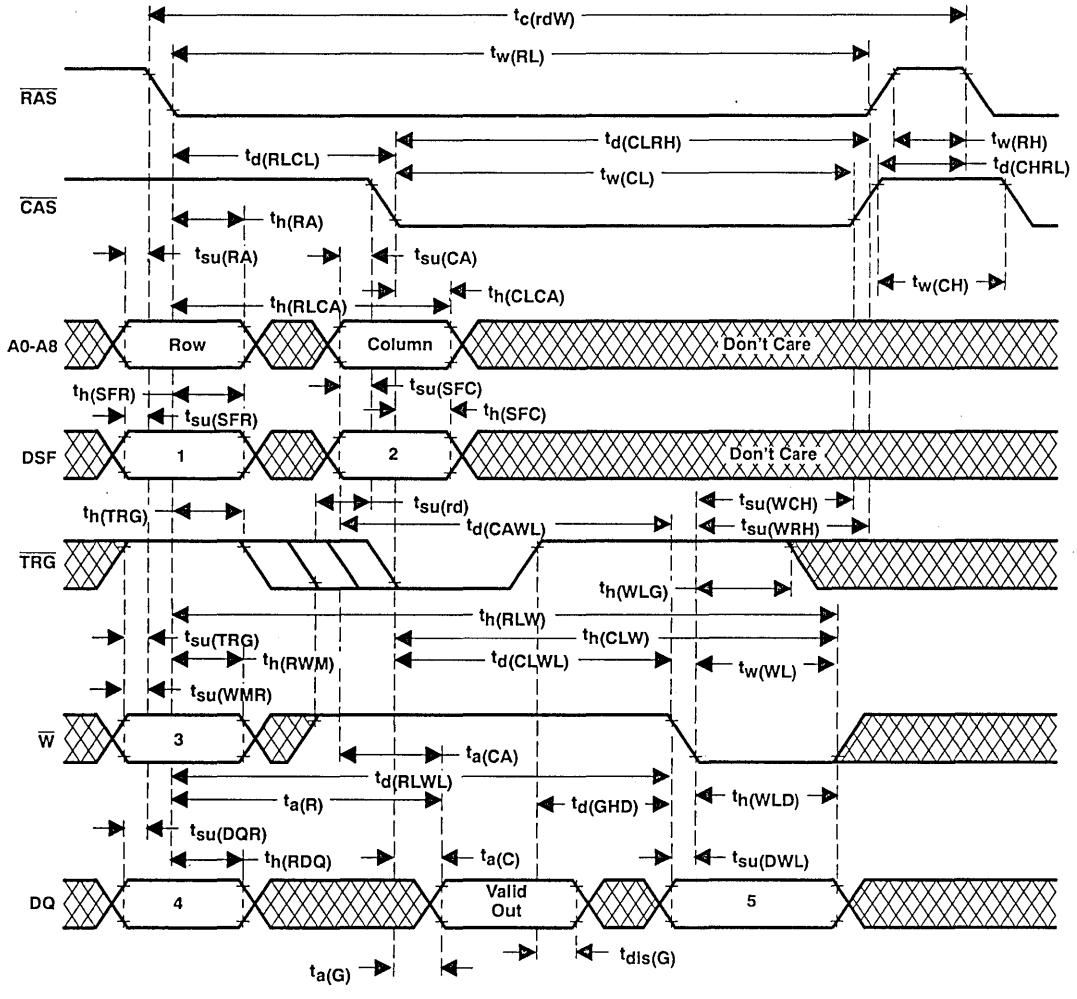
ADVANCE INFORMATION

write cycle state table

CYCLE	STATE				
	1	2	3	4	5
Write mask load/use, write DQs to I/Os	L	L	L	Write Mask	Valid Data
Write mask load/use, block write	L	H	L	Write Mask	Addr Mask
Use previous write mask, write DQs to I/Os	H	L	L	Don't Care	Valid Data
Use previous write mask, block write	H	H	L	Don't Care	Addr Mask
Load write mask on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	L	H	Don't Care	Write Mask
Load color register on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	H	H	Don't Care	Color Data
Write mask disabled, block write to all I/Os	L	H	H	Don't Care	Addr Mask
Normal early or late write operation	L	L	H	Don't Care	Valid Data

ADVANCE INFORMATION

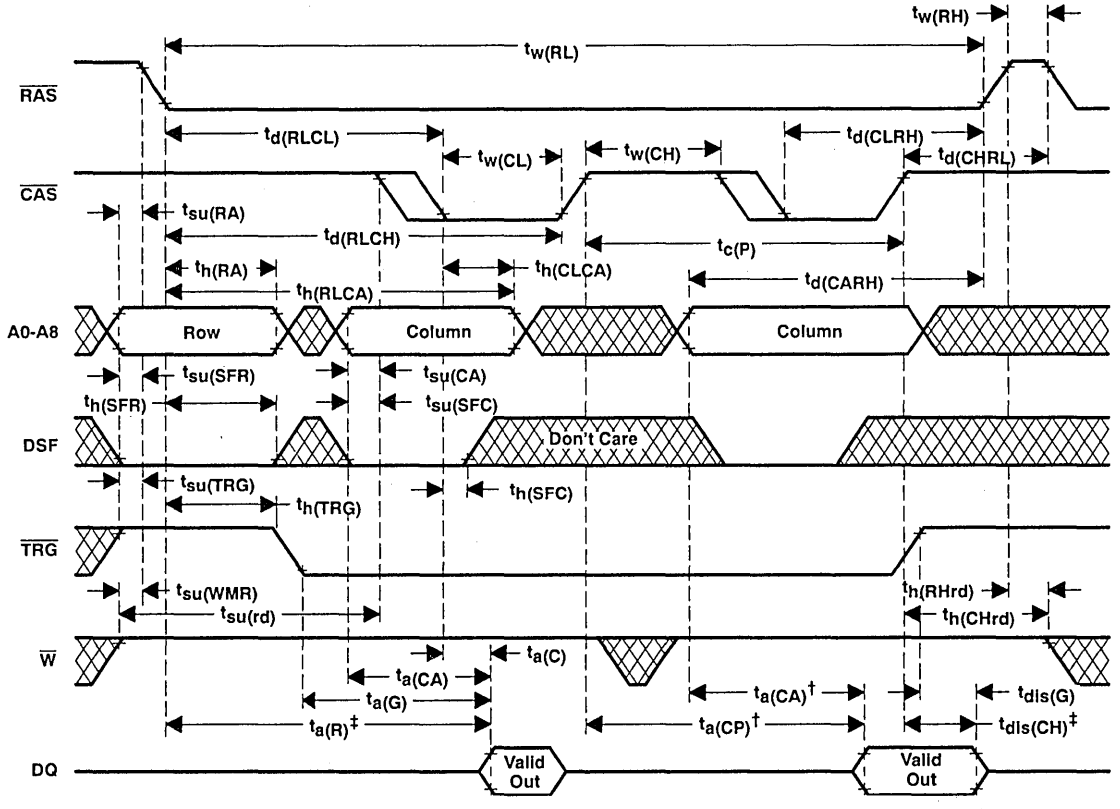
read-write/read-modify-write cycle timing



NOTE 26: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5". Same logic as delayed write cycle.

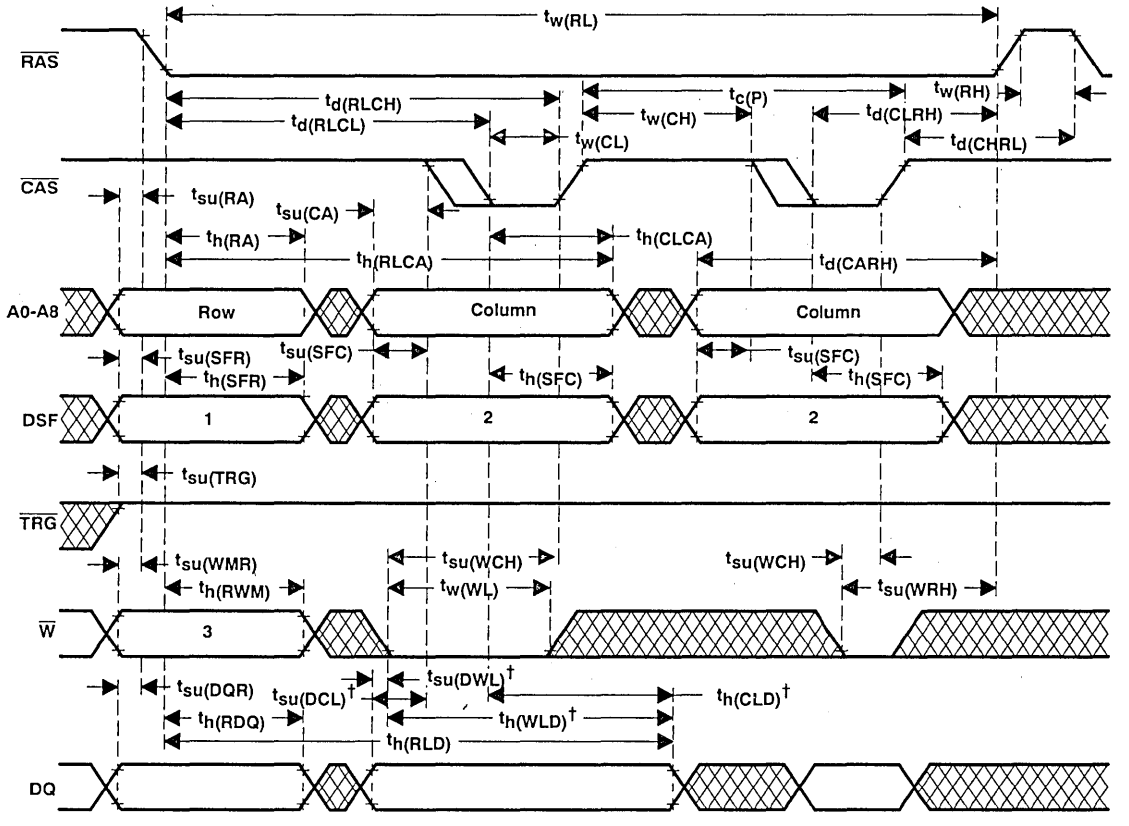
ADVANCE INFORMATION

enhanced page-mode read cycle timing



† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
‡ Output may go from the high-impedance state to an invalid data state prior to the specified access time.
NOTE 27: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to select the desired write mode (normal, block write, etc.)

enhanced page-mode write cycle timing



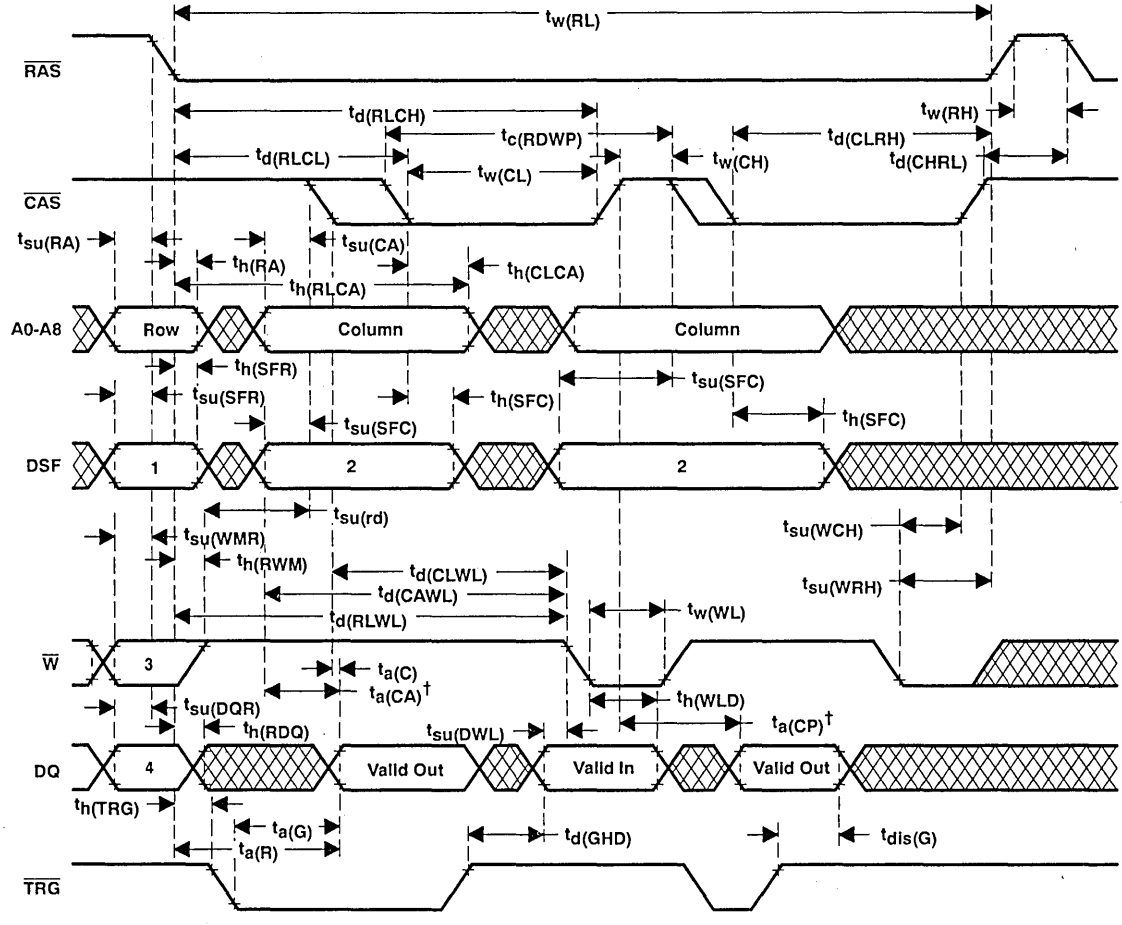
† Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

NOTES: 25. See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

28. A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write features is used, to guarantee page-mode cycle time. If the early write cycle timing is used, the state of $\overline{TRG}$ is a Don't Care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

ADVANCE INFORMATION

enhanced page-mode read-modify-write cycle timing

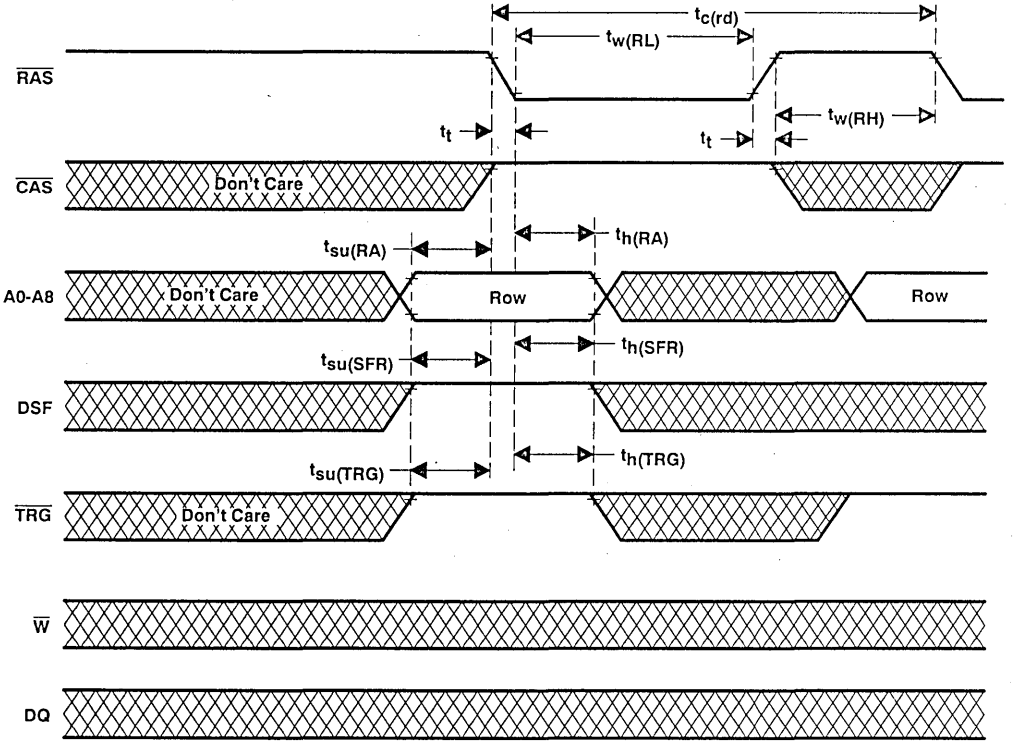


† Output may go from the high-impedance state to an invalid data state prior to the specified access time.

NOTES: 25. See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

29. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

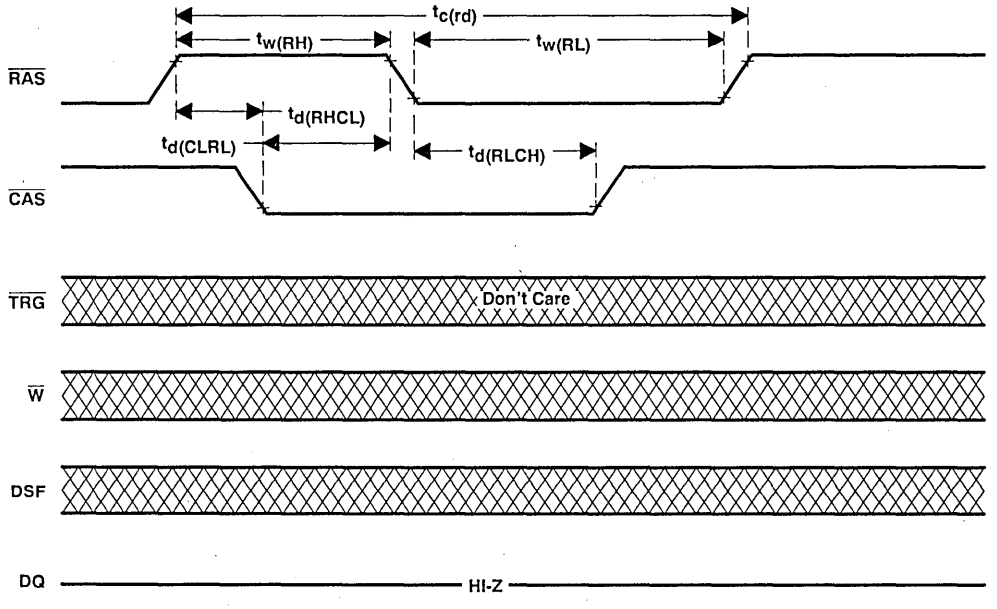
$\overline{\text{RAS}}$-only refresh timing



NOTE 30: In persistent write-per-bit function, $\overline{\text{W}}$ must be high during the refresh cycle.

ADVANCE INFORMATION

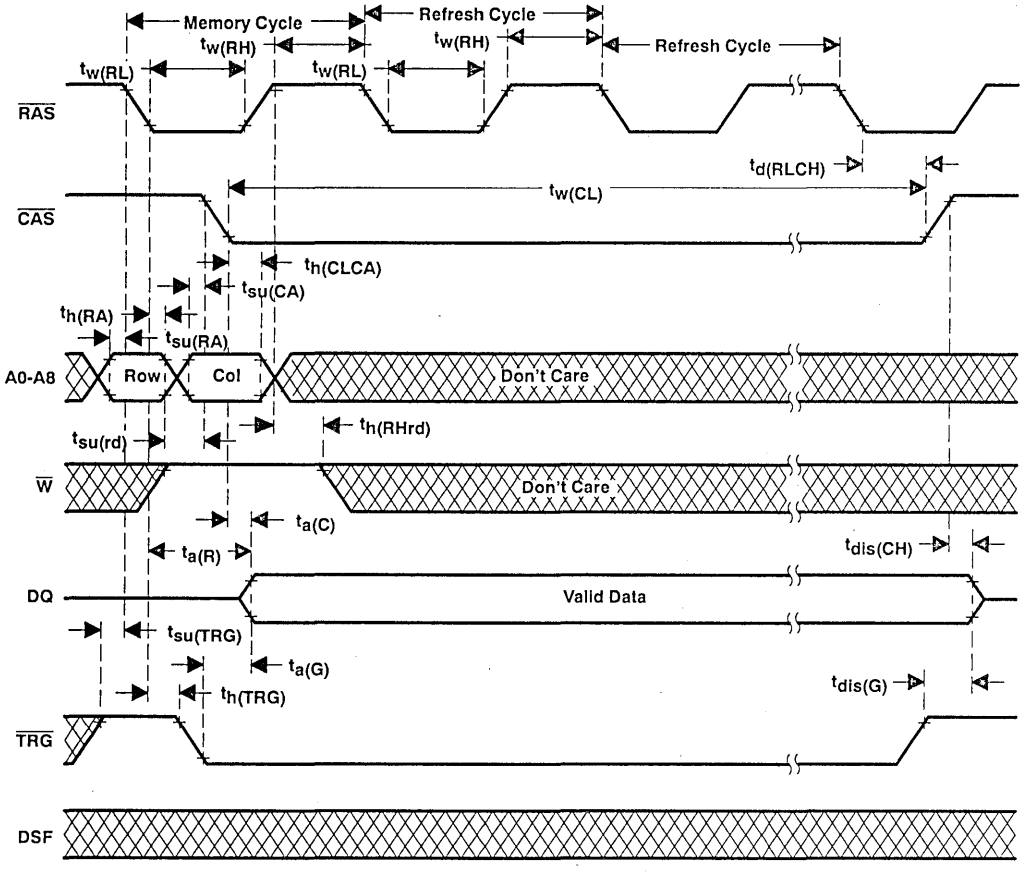
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh



NOTE 30: In persistent write-per-bit function, $\overline{\text{W}}$ must be high during the refresh cycle.

ADVANCE INFORMATION

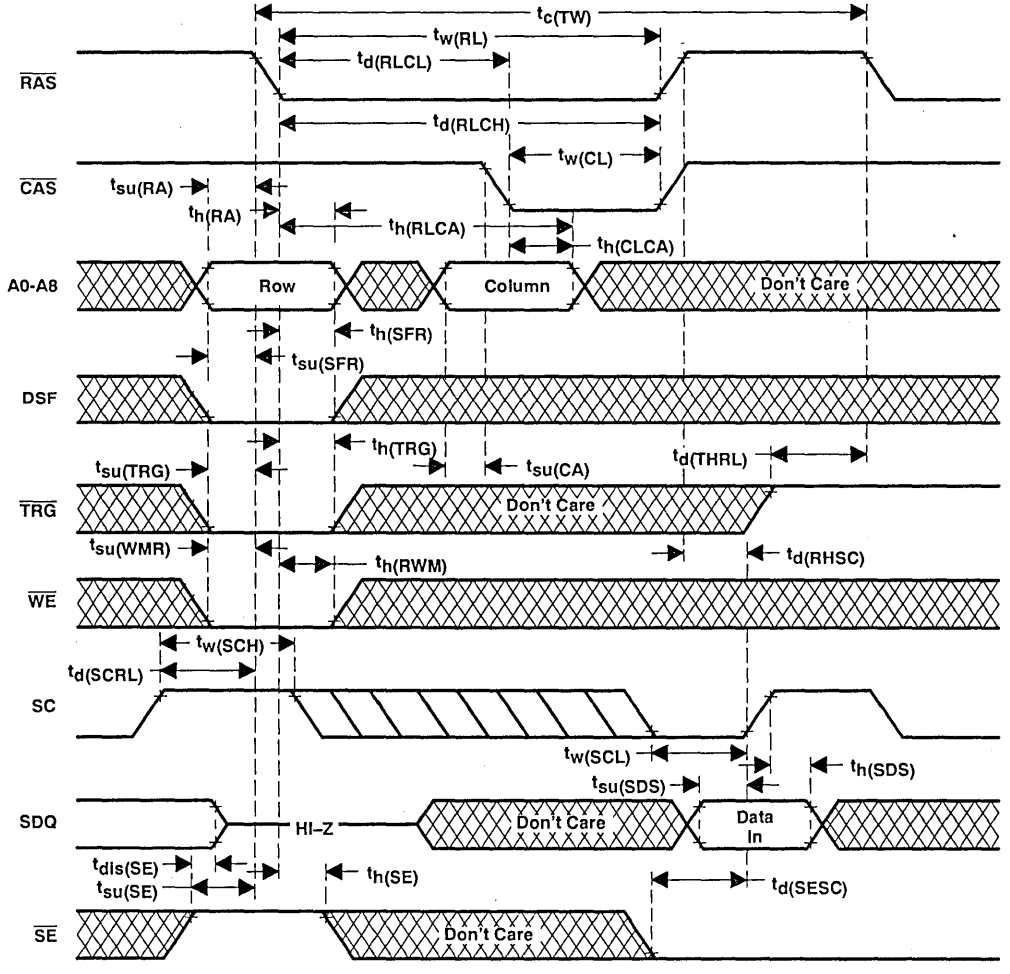
hidden refresh cycle timing



ADVANCE INFORMATION

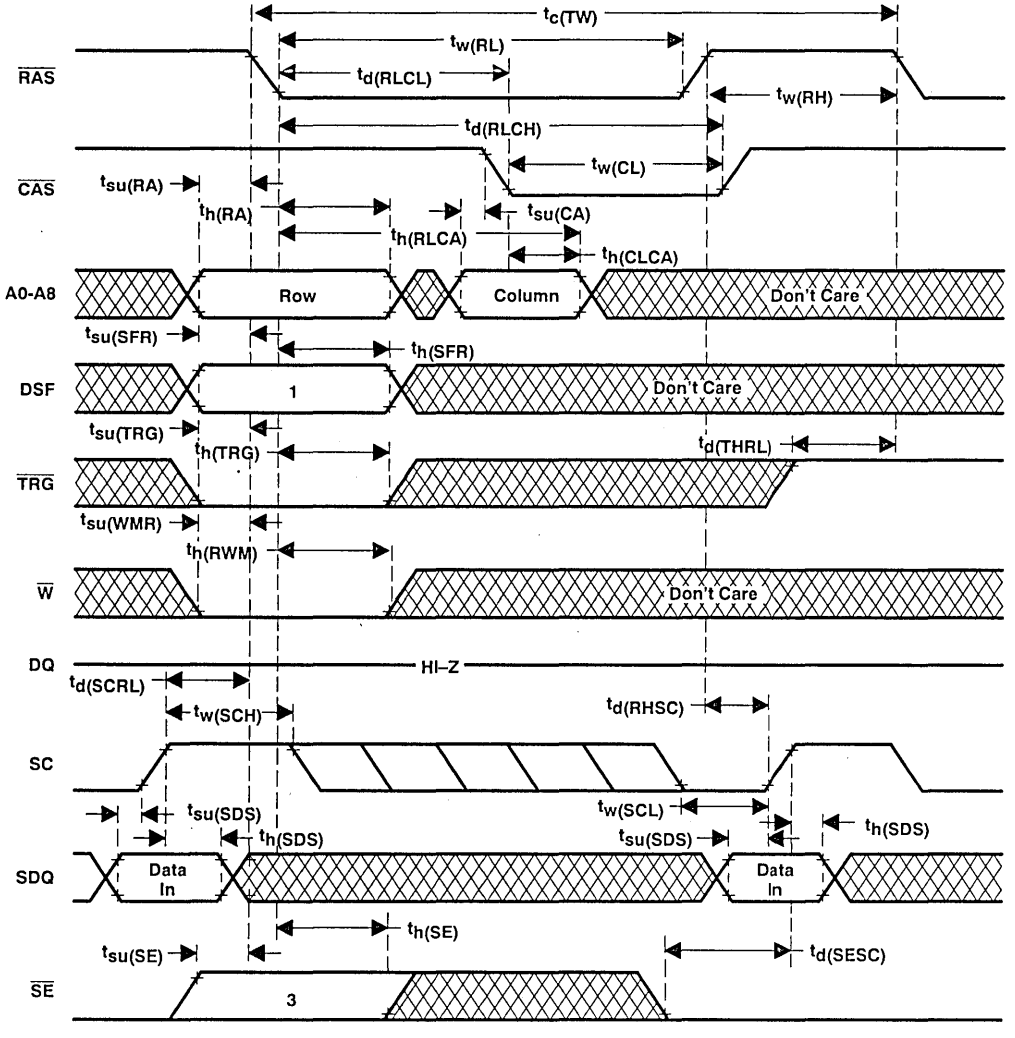
write-mode control pseudo transfer timing

The write-mode control cycle is used to change the SDQs from the output mode to the input mode. This allows serial data to be written into the data register. The diagram below assumes that the device was originally in the serial read mode.



NOTES: 31. Random-mode Q outputs remain in the high-impedance state for the entire write-mode control.
32. $\overline{SE}$ must be high as $\overline{RAS}$ falls in order to perform a write-mode control cycle.

data register to memory timing, serial input enabled



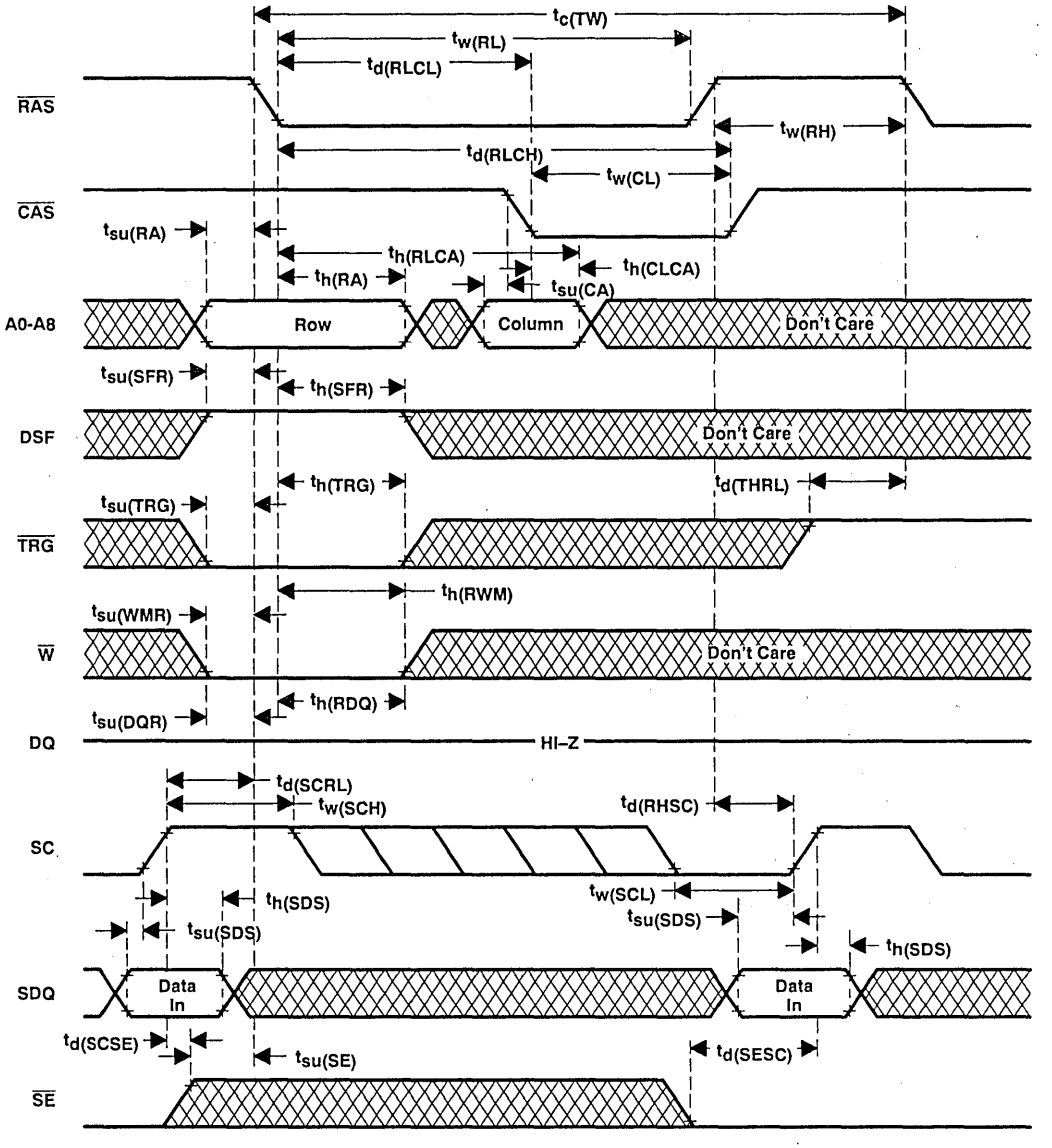
register transfer function table

FUNCTION	RAS FALL			
	TRG	W	DSF (1)	SE (3)
Register to memory transfer, serial input enabled	L	L	X	L
Register to memory transfer, alternate transfer write	L	L	H	X
Pseudo-transfer SDQ control	L	L	L	H
Memory to register transfer	L	H	L	X
Split register transfer	L	H	H	X

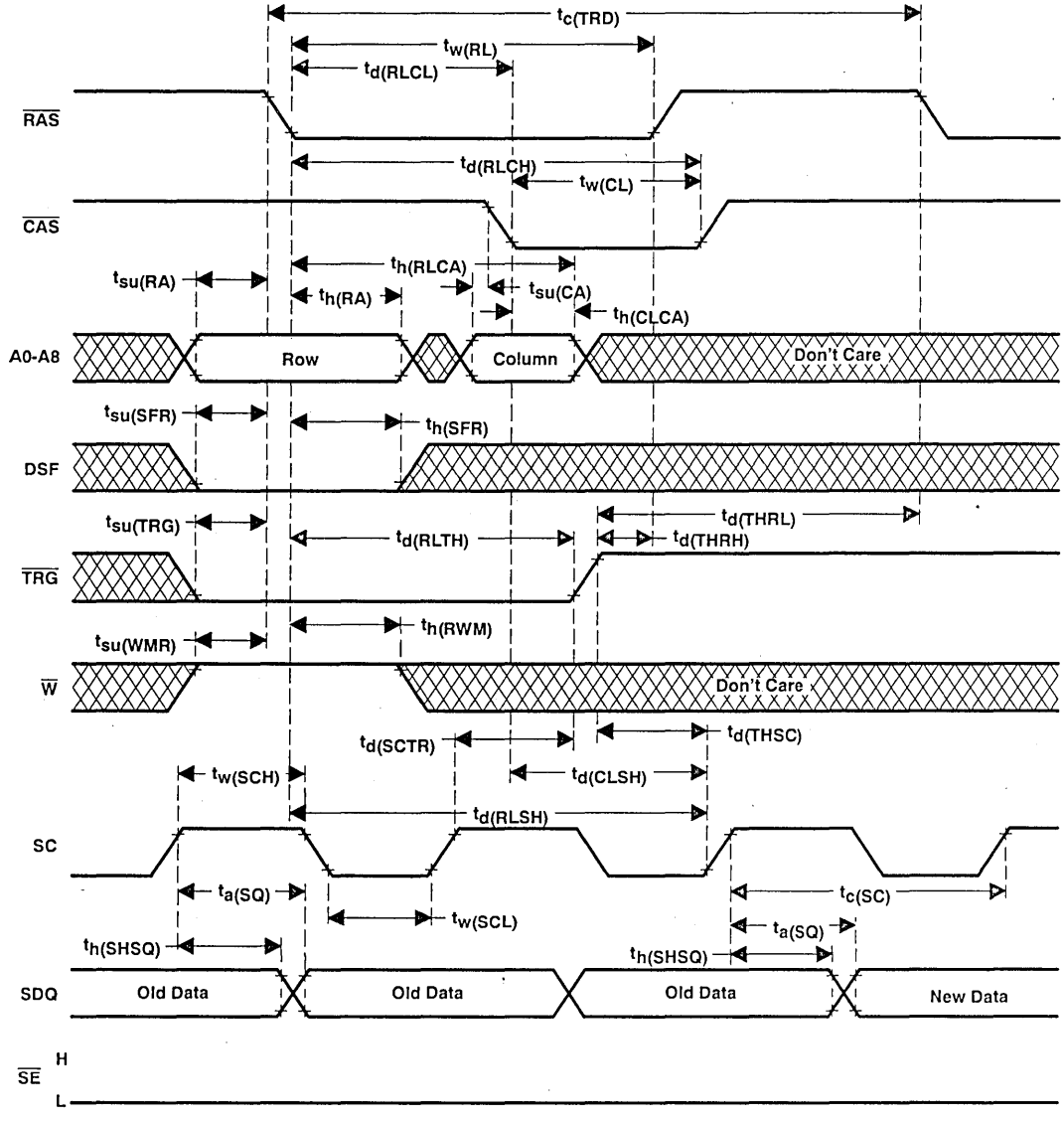
ADVANCE INFORMATION

ADVANCE INFORMATION

alternate data register to memory timing



memory to data register transfer timing

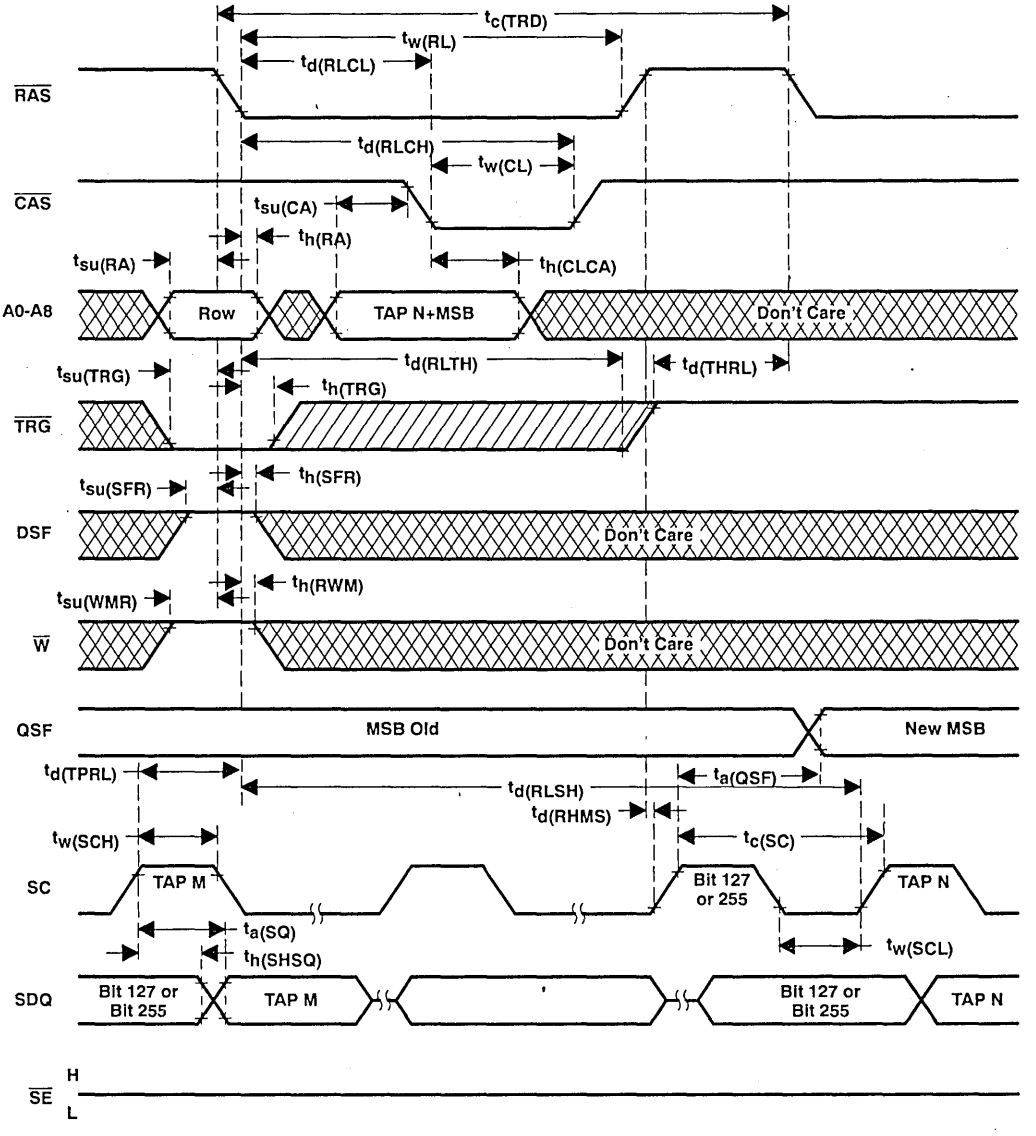


NOTES: 33. Random mode (Q outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register treansfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row. The data that is transferred into the data registers may be either shifted out or transferred back into another row.

34. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

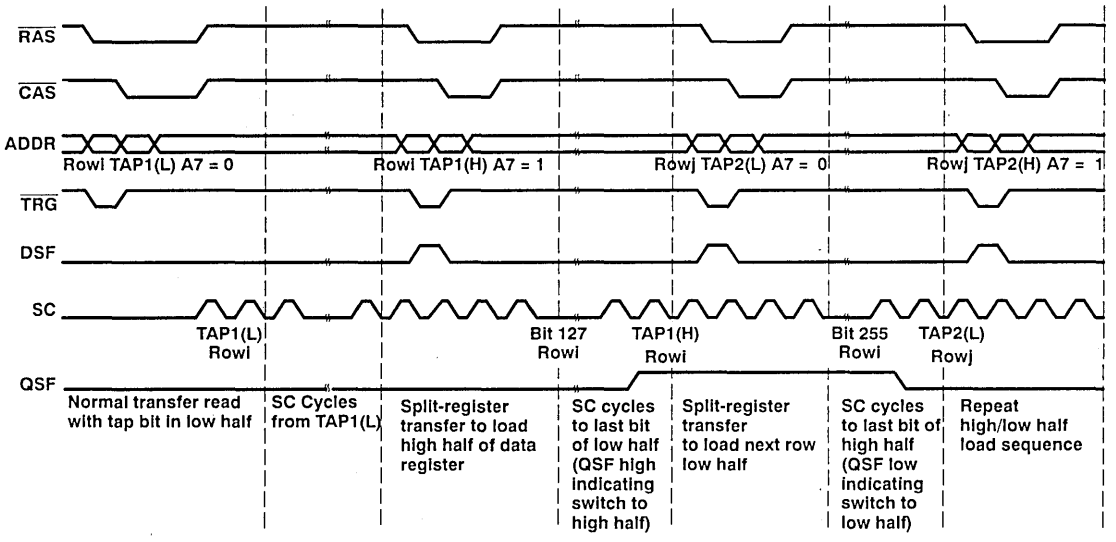
ADVANCE INFORMATION

split-register mode read transfer timing



NOTE 35: There must be a minimum of two SC clock cycle between any two split-register reload cycles, and between a transfer read cycle and a split-register cycle.

split-register operating sequence



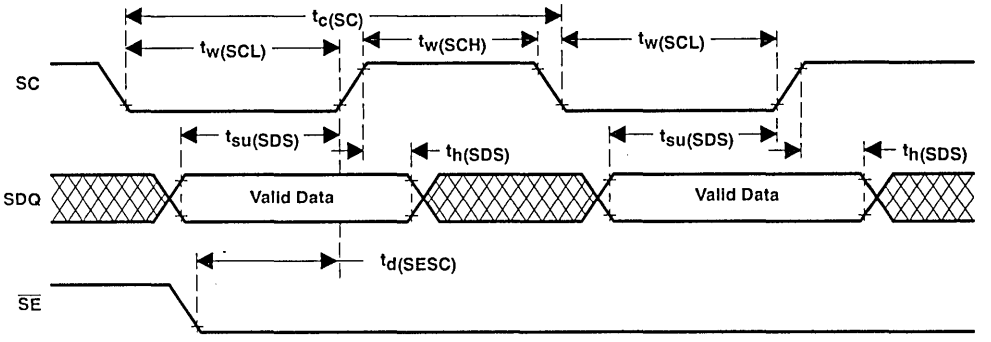
NOTES: 36. In split register mode, data can be transferred from different rows to the low and high halves of the data register.
37. When enabling or disabling split register mode, $t_{a(QSF)}$ is measured from $\overline{RAS}$ low in the transfer cycle.

In order to achieve proper split-register operation, a normal read transfer should be performed before the first split-register transfer cycle. This is necessary to initialize the data register and the starting tap location. Serial access can then begin after the normal transfer cycle.

Before reaching the data register boundary, bit 127 or 255, the first split-register transfer to the inactive register half can be performed. When the serial counter reaches the data register boundary, it will be loaded with the tap location set on the previous split-register transfer cycle, with the next serial access continuing from that tap location. (See timing diagrams on pages 8-122 and 8-123.)

ADVANCE INFORMATION

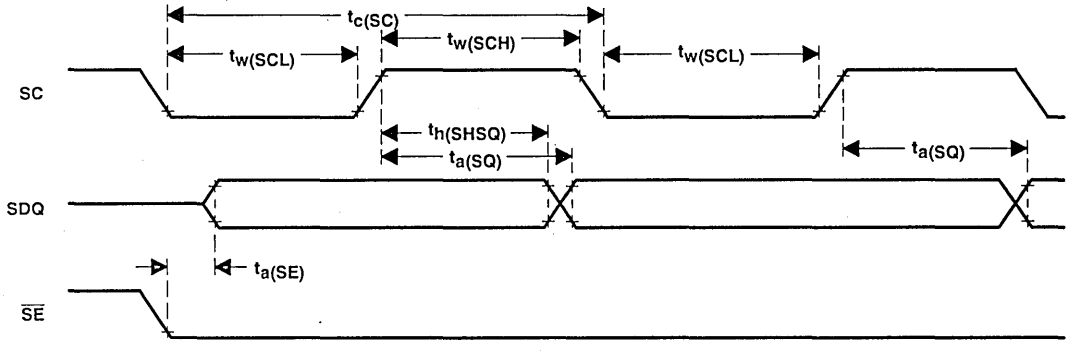
serial data-in timing



The Serial Data-in cycle is used to input serial data into the data registers. Before data can be written into the data registers via SD, the device must be put into the write mode by performing a write mode control (pseudo-transfer) cycle or any other transfer write cycle. A transfer read cycle is the only cycle that will take the serial port (SAM) out of the write mode and put it into the read mode, thus disabling the input data. Data will be written starting at the location specified by the input address loaded on the previous transfer cycle.

While accessing data in the serial data registers, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.

serial data-out timing



NOTE 38: While reading data through the serial data register, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register to memory to register data transfer operation.

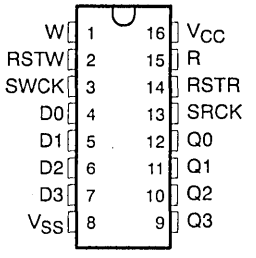
The Serial Data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle. Any transfer write cycles occurring between the transfer read cycle and the subsequent shifting out of data will take the device out of the read mode and put it in the write mode, thus not allowing the reading of data.

- 262 264 × 4 Organization
- Single 5-V Power Supply (± 10% Tolerance)
- Fast FIFO (First-In First-Out) Operation
  - Full Word Continuous Read/Write
  - Asynchronous Read/Write
- Quasi-Static (Refresh Free)
- High-Speed Read/Write Operation

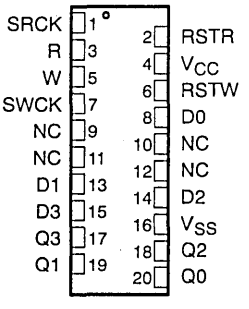
	ACCESS TIME (MAX)	CYCLE TIME READ (MIN)	CYCLE TIME WRITE (MIN)
TMS4C1050/4C1060-30	25 ns	30 ns	30 ns
TMS4C1050/4C1060-40	30 ns	40 ns	40 ns
TMS4C1050/4C1060-60	50 ns	60 ns	60 ns

- Low Power Dissipation (Average I_{DD} = 50 mA at Minimum Cycle)
- Plastic 16-Pin 300-mil-Wide DIP, 20-Pin 400-mil ZIP, or 20/26-Lead Surface-Mount (SOJ) Package
- Texas Instruments EPIC™ (Enhanced Process Implanted CMOS) Technology
- Operating Free-Air Temperature . . . 0°C to 70°C

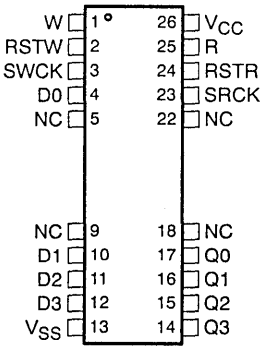
N Package
(Top View)



SD Package
(Top View)



DJ Package
(Top View)



description

The TMS4C1050 and TMS4C1060 are Field Memories (FMEM) which read and write data exclusively through serial ports, 4 bits wide. Maximum storage capacity is 262 264 words by four bits each. Addressing is controlled by write address and read address pointers, which must be reset to zero before memory access begins.

Read and write access may occur asynchronously, if desired by the user. When read access is delayed relative to write access, the TMS4C1050 and the TMS4C1060 function like a First-In First-Out (FIFO) register. The amount of delay determines the "length" of the FIFO register.

PIN NOMENCLATURE	
D0-D3	Data-In
Q0-Q3	Data-Out
R	Read Enable
RSTR	Reset Read
RSTW	Reset Write
SRCK	Serial Read Clock
SWCK	Serial Write Clock
W	Write Enable
NC	No Internal Connection
V_{CC}	5-V Power Supply
V_{SS}	Ground

Unlike in a conventional FIFO register, however, data may be read as many times as desired, after it is written into the storage array. Even if the content of the read address pointer is lost because the requirements for its integrity have been violated (i.e., at least one clock period per 1 ms while R is active), the data stored is not lost and can be recovered by resetting the read address pointer to zero again.

EPIC is a trademark of Texas Instruments Incorporated.

description (continued)

Minimum delay between writing into the device and reading out data is 600 SWCK cycles. Maximum delay is one full field (262 264 write cycles) plus another 119 SWCK cycles.

The TMS4C1050 and TMS4C1060 employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and power at a low cost.

Dynamic data storage cells are employed as the main data memory to achieve high density. Self-refresh and arbitration logic is implemented in the TMS4C1050 and TMS4C1060 supplying a refresh-free system. This logic prevents any conflict between data-saving/data-loading/memory-refresh requests.

The write address counting scheme of the TMS4C1060 has been modified relative to its read address counting scheme, to allow easy cascading of several memory devices. In this respect the TMS4C1050 and the TMS4C1060 differ. Another difference between both memories is the timing of output enabling and disabling. In the TMS4C1060, this timing is clock edge controlled, while in the TMS4C1050 enabling and disabling is level controlled.

The TMS4C1050 and TMS4C1060 are offered in a 16-pin dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 7,62-mm (300-mil) centers. These devices are also offered in a 20-pin 400-Mil ZIP package (SD suffix) and a 300-Mil 20/26 J-lead plastic surface mount SOJ package (DJ suffix). These devices are guaranteed for operation from 0°C to 70°C (L suffix).

operation

write operation

The write operation is controlled by two clocks, SWCK and RSTW, and W. It is accomplished by cycling SWCK and holding W high after write address pointer reset operation (RSTW). Each write operation, which begins with RSTW, must contain at least 120 active write cycles, i.e. SWCK cycles while W is high. To transfer the last data written into the device, which at that time is still stored in the write line buffer, to the memory array, an RSTW operation is required after the last SWCK cycle.

reset write (RSTW)

The first positive transition of SWCK after RSTW going high, resets the write address pointers to zero. RSTW setup and hold times are referenced to the rising edge of SWCK. The state of W may be high or low during any reset operation. Before RSTW may be brought high again for a futher reset operation, it must have been low for at least two SWCK cycles.

data inputs (D0-D3) and write clock (SWCK)

The SWCK input latches the data inputs on chip when W is high and also increments the internal write address pointer. Data-in setup and hold times [$t_{su(D)}$, $t_{h(D)}$] are referenced to the rising edge of SWCK.

write enable (W)

W is used as a data-in enable/disable. A logic high on the W input enables the input, and a logic low disables the input and holds the internal write address pointer. W disable time (low) can be expanded to 1 ms. In case W is held low over 1 ms, the content of the write address pointer may get lost. In this case an RSTW operation is required to re-initialize this pointer.

Note that W setup and hold times are referenced to the rising edge of SWCK.

read operation

The read operation is controlled by two clocks, SRCK and RSTR, and R. It is accomplished by cycling SRCK and holding R high after a read address pointer reset operation (RSTR). Each read operation, which begins with RSTR, must contain at least 120 active read cycles, i.e. SRCK cycles while R is high.

reset read (RSTR)

The first positive transition of SRCK after RSTR has gone high resets the read address pointers to zero. RSTR setup and hold times are referenced to the rising edge of SRCK. The state of R may be high or low during any reset operation. Before RSTR may be brought high again for a further reset operation, it must have been low for at least two SRCK cycles.

data out (Q0-Q3) and read clock (SRCK)

Data is shifted out of the data registers on the rising edge of SRCK when R is high during a read operation. The SRCK input increments the internal read address pointer when R is high.

The three-state output buffer provides direct TTL compatibility (no pullup resistor required). Data out is the same polarity as data in. The output becomes valid after the access time interval t_{AC} that begins with the positive transition of SRCK.

Output valid time [$t_{v(OUT)}$] is referenced to the rising edge of SRCK in the next cycle.

output enabling and disabling (TMS4C1050 only)

When R changes state, the outputs will become enabled or disabled. However, SRCK must go low also, before a change of the state of R can be noticed at the outputs. The state of SRCK influences the outputs only during the first SRCK cycle following each change of state of R.

In order for the outputs to become enabled, R must go high and SRCK must go low. Enable time is determined by whichever transition (R going high or SRCK going low) occurs last. In order for the outputs to become disabled, R must go low and SRCK must go low. Disable time is determined by whichever transition (R going low or SRCK going low) occurs last. See the timing diagrams under read cycle timing (output enable and disable) for an illustration of enable and disable timing.

output enabling and disabling (TMS4C1060 only)

The state of R is latched in by the read clock . SRCK determines whether the outputs will be enabled or disabled. If R is high at the rising edge of SRCK, the outputs will be enabled. If R is low at the rising edge of SRCK, the outputs will be disabled. R setup and hold times are referenced to the rising edge of SRCK.

read enable (R)

R performs a double function. First, R gates the SRCK clock, for incrementing the read pointer. When R is high before the rising edge of SRCK, the read pointer is incremented. When R is low, the read pointer is not incremented. R setup times (t_{RHSRH} and t_{RLSRH}) and R hold times [$t_{h(RE)}$] are referenced to the rising edge of the SRCK clock.

The second function of R is to enable and disable the outputs. See the appropriate section on "output enabling and disabling".

After a read operation has started, R may be brought low for a maximum of 1 ms, before the contents of the read address pointer will be lost due to the dynamic nature of the read address pointer register. In this case, information stored in the memory will not be lost, but it will be necessary to restart the read cycle at the beginning address (zero) by performing an RSTR operation.

power-up and initialization

On powering up, the device is designed to begin proper operation after at least 100 μs after V_{CC} has stabilized to a value within the range of recommended operating conditions. After this 100 μs stabilization interval, the following initialization sequence must be performed.

Because the read and write address pointers are not valid after power-up, a minimum of 130 dummy read operations (SRCK cycles) must be performed, followed by an RSTR operation, to properly initialize the read address pointer. A minimum of 130 dummy write operations (SWCK cycles) must be performed, followed by an RSTW operation, to properly initialize the write address pointer. Dummy read cycles/RSTR and dummy write cycles/RSTW may occur simultaneously.

If these dummy read and write operations start while V_{CC} and/or the substrate voltage have not stabilized, it is required to perform an RSTR operation plus a minimum of 130 SRCK cycles plus another RSTR operation, and an RSTW operation plus a minimum of 130 SRCK cycles plus another RSTW operation to properly initialize read and write address pointers.

old/new data access

There must be minimum delay of 600 SWCK cycles between writing into memory and reading out from memory. If reading from the first field starts with an RSTR operation, before the start of writing the second field, (before the next RSTW operation), then the data just written in will be read out.

The start of reading out the first field of data may be delayed past the beginning of writing in the second field of data for as many as 119 SWCK cycles. If the RSTR operation for the first field read-out occurs less than 120 SWCK cycles after the RSTW operation for the second field write-in, then the internal buffering of the device assures that the first field will still be read out. The first field of data that is read out while the second field of data is written is called old data.

In order to read out new data, i.e., the second field written in, the delay between an RSTW operation and an RSTR operation must be at least 600 SRCK cycles. If the delay between RSTW and RSTR operations is more than 120 but less than 600 cycles, then the data read out will be undetermined. It may be old data or new data or a combination of old and new data. Such a timing should be avoided.

cascade operation (TMS4C1060 only)

The TMS4C1060 has been designed to allow easy cascading of multiple memory devices, in order to obtain a higher storage depth or a longer delay than can be achieved with only one memory device. See the interconnection diagram on page 8-138 for details.

As illustrated in the timing diagram on page 8-138, the positive SRCK/SWCK edge at the beginning of a clock cycle serves to initiate read-out, whereas writing in is initiated by the positive SWCK/SRCK edge at the end of a cycle. This differs from the functionality of the TMS4C1050, in which both the read-out and the write-in are initiated at the beginning of a clock cycle.

internal operation

writing into memory

The first 120 words of data following the initial RSTW operation after power-up are written into a cache buffer (A) initially, and will never be stored elsewhere, to allow read-out of data later without the delay involved in retrieving it from the main memory array.

Starting from address 121, data is written into the write line buffer, top block, until this block (256 words long) is full. Further writing then occurs to the bottom block of the write line buffer, while the top block is transferred to the main memory array. By the time the bottom block is full, the top block has been transferred to memory and can be used again to receive new incoming data. The channelling of input data into the top or bottom block is controlled internally by the device and is transparent to the user.

After the 120-word long cache buffer has been filled with incoming data, the input line selector switches the connection of the input port over to the B line buffer to assure that the next field of data, which will arrive later after a subsequent RSTW operation, does not over write the content of the cache buffer. Each subsequent filling of the cache buffer toggles the connection of the input port between the A and the B line buffers with the 121st SWCK pulse. The A and B line buffers, as well as the input line selector, are static registers.

The connection of the output port will also be toggled between A and B line buffers by the 121st SWCK pulse, providing no read operation from a cache buffer is in progress at this time. The output port will always be connected to the line buffers opposite to the one connected to the input port. In case a read operation from a cache buffer is in progress when the 121st SWCK occurs, the toggling of the output port connection will be delayed until the cache buffer has been read out completely.

The requirement stated on page 8-126 that each write operation must contain at least 120 active SWCK cycles, exists in order to assure that the toggling of the input and output ports between the A line buffer and the B line buffer functions without errors as described above.

The serial write pointer stores the (column) address of the last input data word received, while the write counter stores the row address. The serial write pointer is a dynamic register and must be clocked at least once per 1 ms. Holding W low will inhibit clocking; thus W must not be held low for more than 1 ms, and the SWCK must not be inactive for more than 1 ms, to assure integrity of the serial write pointer. Only when the serial write pointer stores the address zero, i.e. the initial address or head address, may this value of 1 ms be exceeded.

After the last word of a full write cycle has been latched in (with a positive transition of the SWCK clock), the write line buffer most likely will be partially filled without having been transferred to the main memory array. To assure that the information contained in the write line buffer is stored also and cannot be lost, it is required that an RSTW operation be performed within 1 ms after input when write clocking has stopped.

In addition to transferring the partially filled write line buffer into the main memory array, this RSTW operation will also reset the write addresses (serial write pointer) to zero, and due to the internal construction of the dynamic serial write pointer register, this internal address of zero remains stored indefinitely. Regardless of how much later a new write cycle starts, it is not necessary to perform another RSTW operation again at that time.

reading from memory

After an RSTR operation, data from the main memory array (starting at address 121) will be transferred to a read line buffer. Because this transfer requires some time, the first 120 words will be read out of the A or B line buffers, where they had been previously stored (see writing into memory above).

If the first RSTR operation occurs after the first RSTW operation but before the second RSTW operation, read access will be to the same buffer that data had been written into during the first write cycle. Thus old data will be read out.

If the first RSTR operation occurs after the second RSTW operation, i.e. after the writing in of new data has already started, then the delay between the second RSTW and the first RSTR operation determines whether old data or new data will be read out.

If this delay is less than 120 SWCK cycles, data will be read out from the line buffer that was written into during the previous write cycle; i.e., old data will be read out. A delay of less than 120 SWCK cycles also assures that all following data bits are old data, because replacement of old data by new data in the main memory array will occur later than the respective read access to each address in the array.

If this delay is more than 600 SWCK cycles, data will be read out from the line buffer that it was written into during the current write cycle; i.e., new data will be read out. A delay of more than 600 SWCK cycles also assures that all following data bits are new data, because replacement of old data by new data in the main memory array will occur before the respective read access to each address in the array.

If this delay is more than 120 but less than 600 SWCK cycles, data read out can be either old or new or a mixture of old and new data, because it cannot be predicted accurately whether a word accessed for reading has already been replaced by new data or not. Such a situation should be avoided.

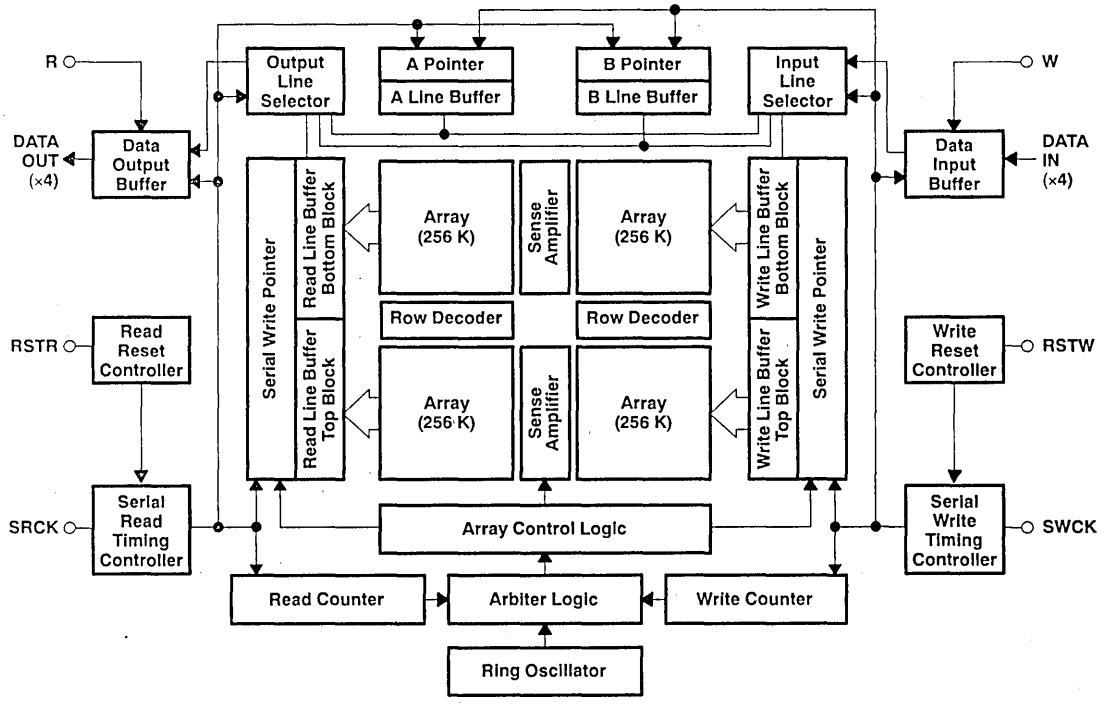
After the first 120 words bits are read out of the A or B line buffer, read transfer from the main memory array to the read line buffer is finished, and subsequent reading will occur from this buffer. Similar to the write operation, while one half of this buffer is being read out, the other half will be filled again by a new read transfer from the main memory array.

The serial read pointer stores the (column) address of the last data word read out, while the read counter stores the row address. The serial read pointer is a dynamic register and must be clocked at least once per 1 ms. Holding R low will inhibit clocking. R must not be held low for more than 1 ms, and the SRCK must not be inactive for more than 1 ms to assure integrity of the serial read pointer. Only when the serial read pointer stores the address zero; i.e., the initial address or head address, may this value be exceeded.

self-refresh and arbitration logic

The self-refresh and arbitration logic will keep the main memory information refreshed automatically without requiring any user action, control the address pointers for both read and write, and control the flow of information both into and out of the main memory.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (TMS4C1050) (see Note 1)	−1 V to 7 V
Voltage range on V_{CC}	0 V to 7 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

	PARAMETER	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		V_{CC}+1	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: V_{IL} = − 1.5 V undershoot is allowed when device is operated in the range of recommended supply voltage.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4C1050-30 TMS4C1060-30		TMS4C1050-40 TMS4C1060-40		TMS4C1050-60 TMS4C1060-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, R low		±10		±10		±10	μA
I_{DD1}	Average operating current	Minimum write/read cycle, output open		50		45		35	mA
I_{DD2}	Standby current	After 1 RSTW/RSTR cycle, W and R low		10		10		10	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz			7	pF
C_o	Output capacitance	V_I = 0, f = 1 MHz			10	pF

† V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	TMS4C1050-30 TMS4C1060-30		TMS4C1050-40 TMS4C1060-40		TMS4C1050-60 TMS4C1060-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AC}	Access time from SRCK high	see Note 3		25		30		50	ns
$t_{v(OUT)}$	Output valid time after SRCK high	see Note 3	6		6		6		ns
$t_{dis(CKL)}$	Output disable time after SRCK low	see Note 4	4	15	4	15	4	15	ns
$t_{en(CKL)}$	Output enable time after SRCK low	see Note 3	0	15	0	15	0	15	ns
$t_{en(RH)}$	Output enable time after R high	see Note 3	0	15	0	15	0	15	ns
$t_{dis(RL)}$	Output disable time after R low	see Note 4	4	15	4	15	4	15	ns

NOTES: 3. The load connected to each output is a 50-pF capacitor to ground, in parallel with a 218-Ω resistor to 1.31 V as illustrated by Figure 1.

4. Disable times are specified from the initiating timing edge until the output is no longer driven by the memory. If disable times are to be measured by observing output voltage waveforms, sufficiently low load resistors and capacitors have to be used, and the RC time constants of the load have to be taken into account.

PARAMETER MEASUREMENT INFORMATION

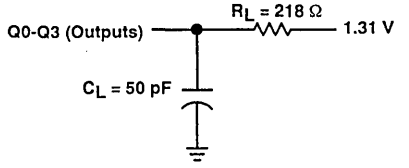


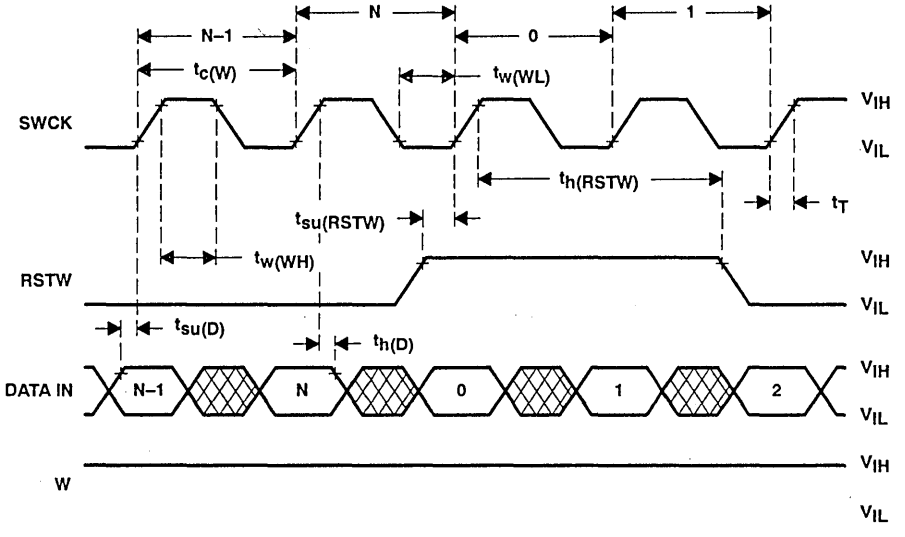
Figure 1. Load Circuit for Timing Parameters

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Notes 5 and 6)

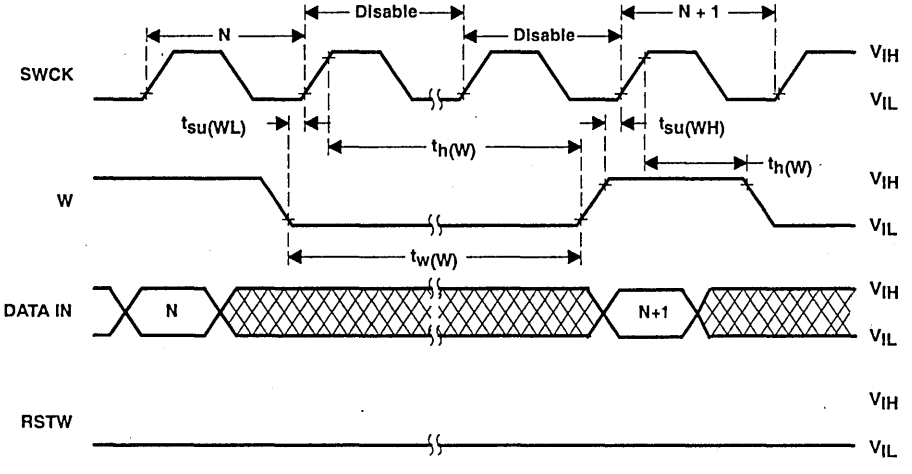
		TMS4C1050-30 TMS4C1060-30		TMS4C1050-40 TMS4C1060-40		TMS4C1050-60 TMS4C1060-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time (see Notes 5 and 6)	30	1 000 000	40	1 000 000	60	1 000 000	ns
$t_{c(R)}$	Read cycle time (see Notes 5 and 6)	30	1 000 000	40	1 000 000	60	1 000 000	ns
$t_{w(R)}$	Pulse duration, R low (see Notes 5 and 6)	10	1 000 000	10	1 000 000	10	1 000 000	ns
$t_{w(W)}$	Pulse duration, W low (see Notes 7 and 8)	10	1 000 000	10	1 000 000	10	1 000 000	ns
$t_{w(RH)}$	Pulse duration, SRCK high	12		17		20		ns
$t_{w(RL)}$	Pulse duration, SRCK low	12		17		20		ns
$t_{w(WH)}$	Pulse duration, SWCK high	12		17		20		ns
$t_{w(WL)}$	Pulse duration, SWCK low	12		17		20		ns
$t_{su(D)}$	Data setup time before SWCK high	5		5		5		ns
$t_{su(RH)}$	R-high setup time before SRCK high	0		0		0		ns
$t_{su(RL)}$	R-low setup time before SRCK high	0		0		0		ns
$t_{su(WH)}$	W-high setup time before SWCK high	0		0		0		ns
$t_{su(WL)}$	W-low setup time before SWCK high	0		0		0		ns
$t_{su(RSTR)}$	RSTR setup time before SRCK high	3		3		3		ns
$t_{su(RSTW)}$	RSTW setup time before SWCK high	3		3		3		ns
$t_{h(D)}$	Data hold time after SWCK high	6		6		6		ns
$t_{h(R)}$	R-hold time after SRCK high	6		6		6		ns
$t_{h(W)}$	W-hold time after SWCK high	6		6		6		ns
$t_{h(RSTR)}$	RSTR hold time after SRCK high	6		6		6		ns
$t_{h(RSTW)}$	RSTW hold time after SWCK high	6		6		6		ns
t_T	Transition time	3	30	3	30	3	30	ns

NOTES: 5. No restrictions apply to the maximum value, if the read and write address pointers are addressing the first address.
6. If the read and write address pointers are not addressing the first address, $t_{c(W)}$, $t_{c(R)}$, $t_{w(WH)}$, $t_{w(WL)}$, $t_{w(WE)}$, $t_{w(RH)}$, $t_{w(RL)}$, and $t_{w(R)}$ must be 1 ms or less. After improper operation (over 1 ms), an RSTW or RSTR cycle is required to initialize the read or write address pointers.
7. Timing measurements are referenced to V_{IH} (MIN) = 2.4 V and V_{IL} (MAX) = 0.8 V. t_T is measured between V_{IH} (MIN) and V_{IL} (MAX).
8. All cycle times assume t_T = 3 ns.

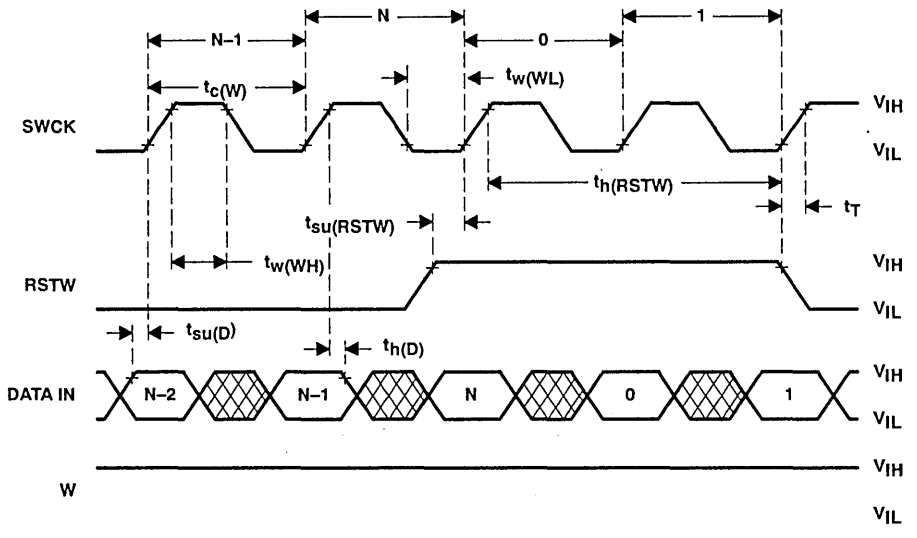
write cycle timing (reset write)



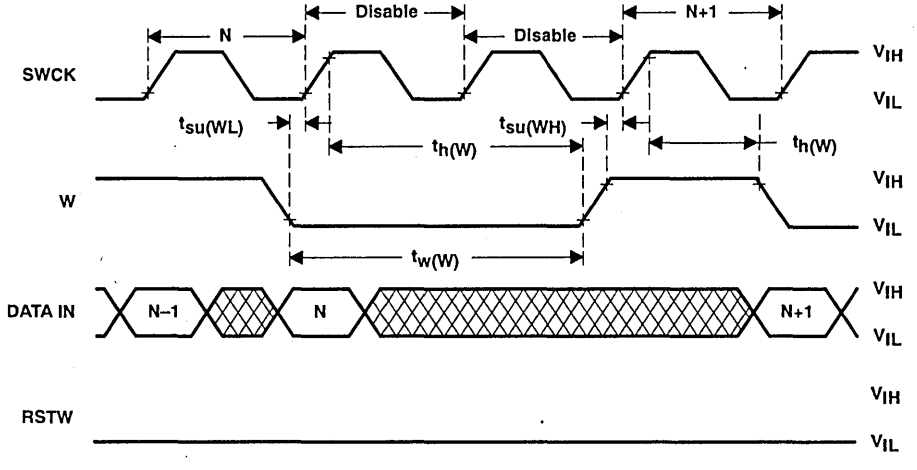
write cycle timing (write enable)



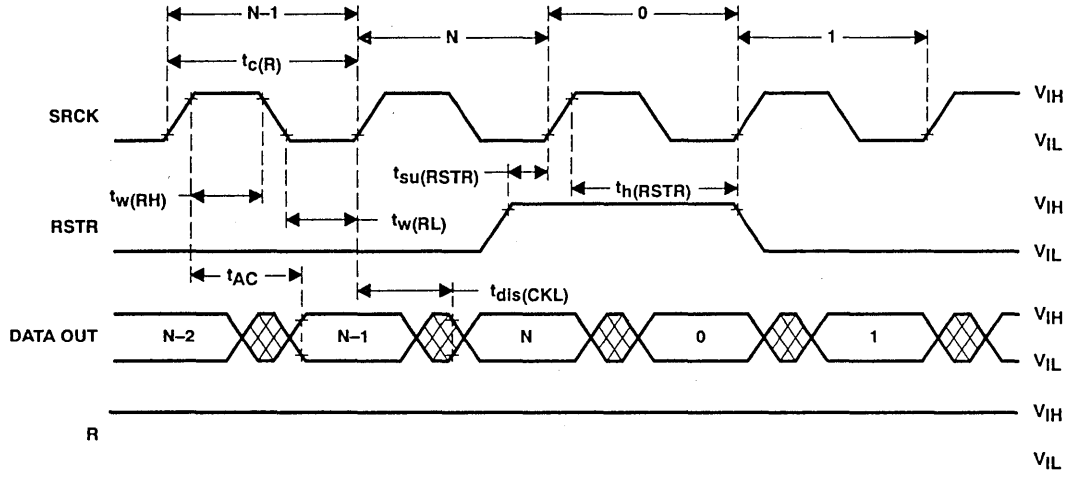
write cycle timing (reset write)



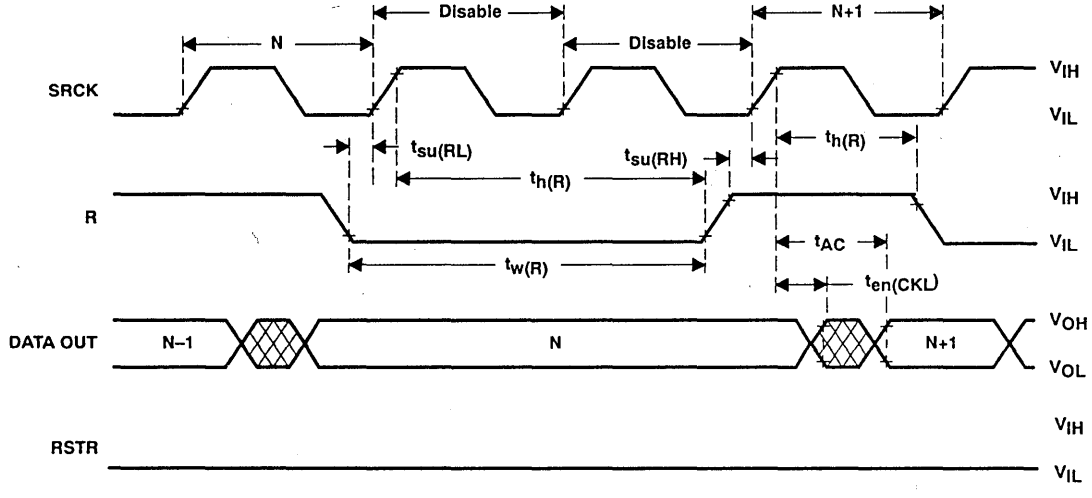
write cycle timing (write enable)



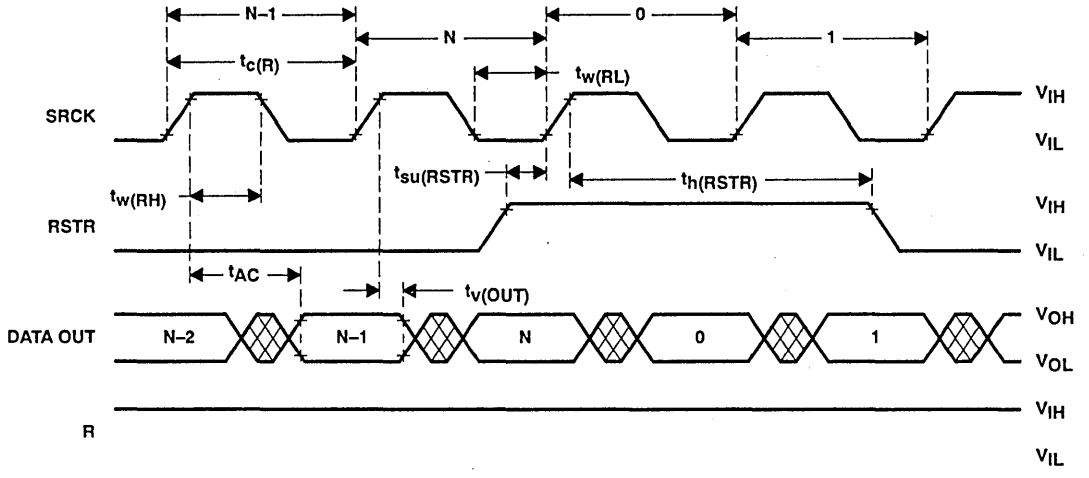
read cycle timing (reset read)



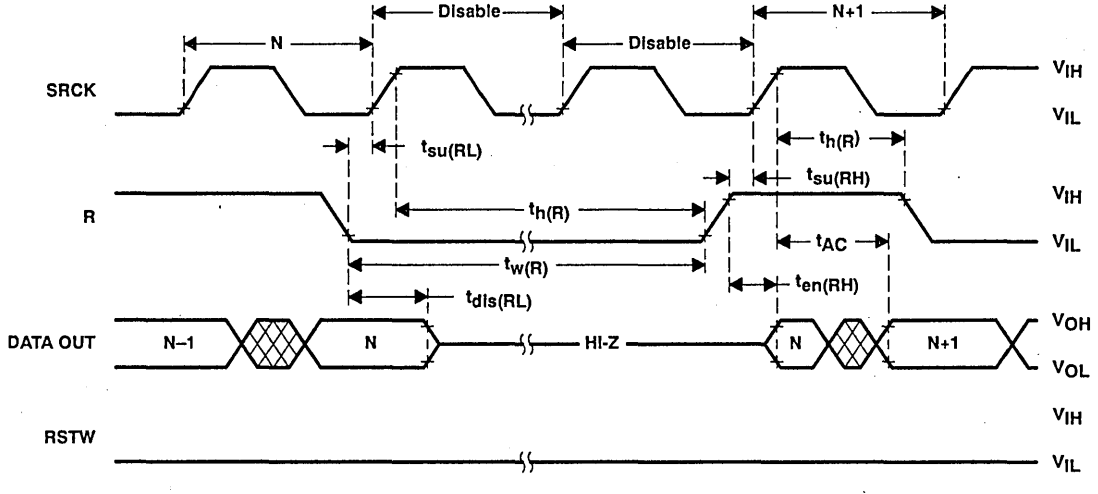
read cycle timing (read enable)



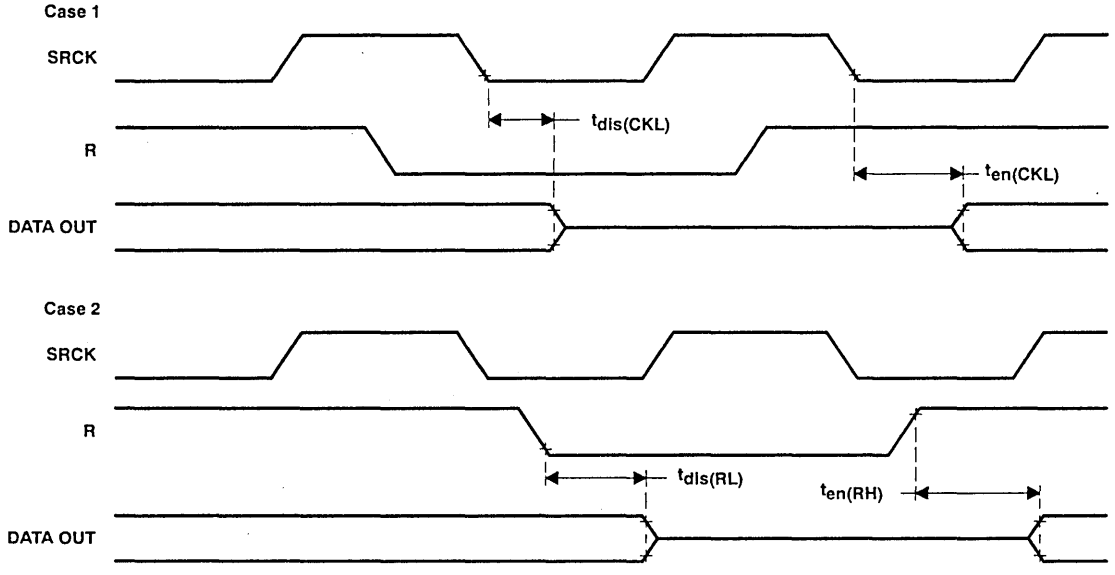
read cycle timing (reset read)



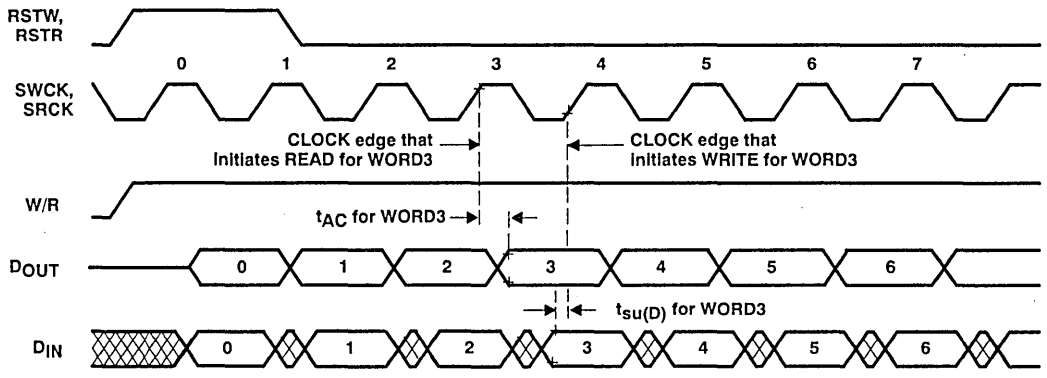
read cycle timing (read enable)



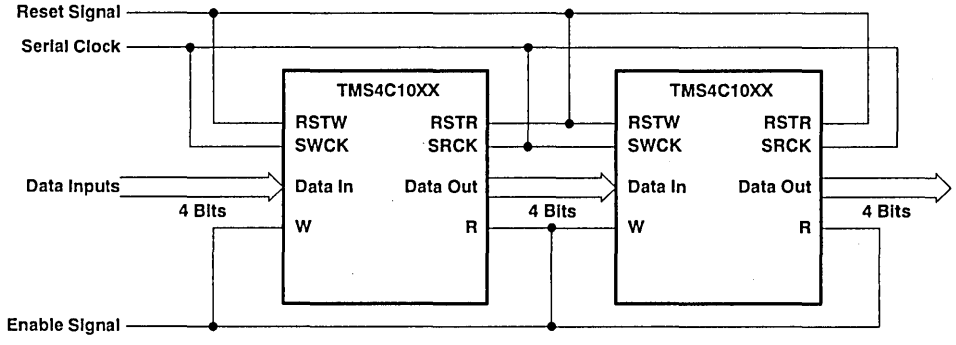
read cycle timing (output enable and disable)



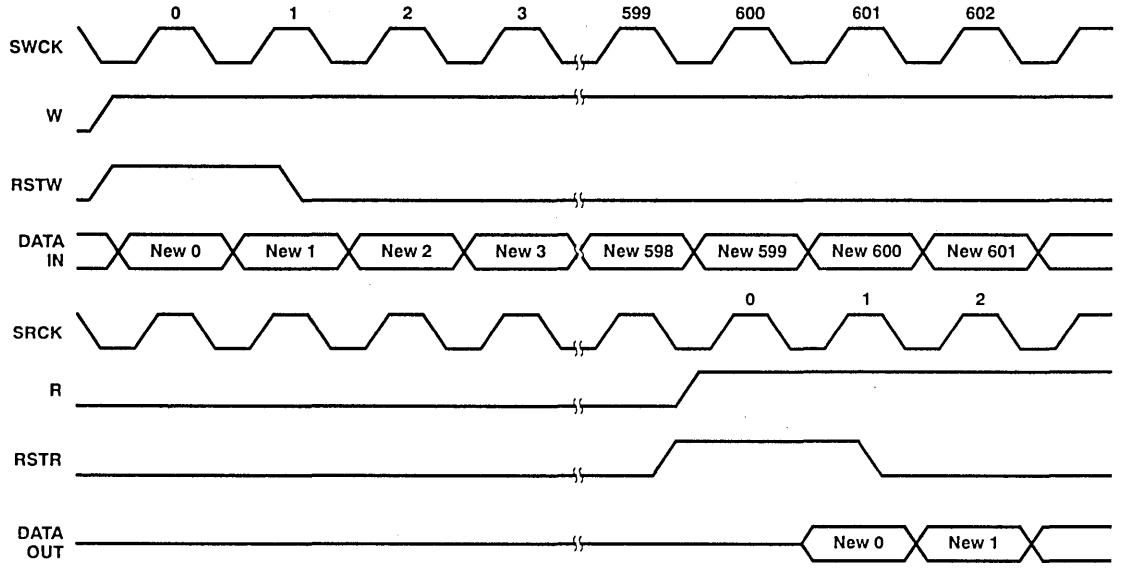
cascade mode



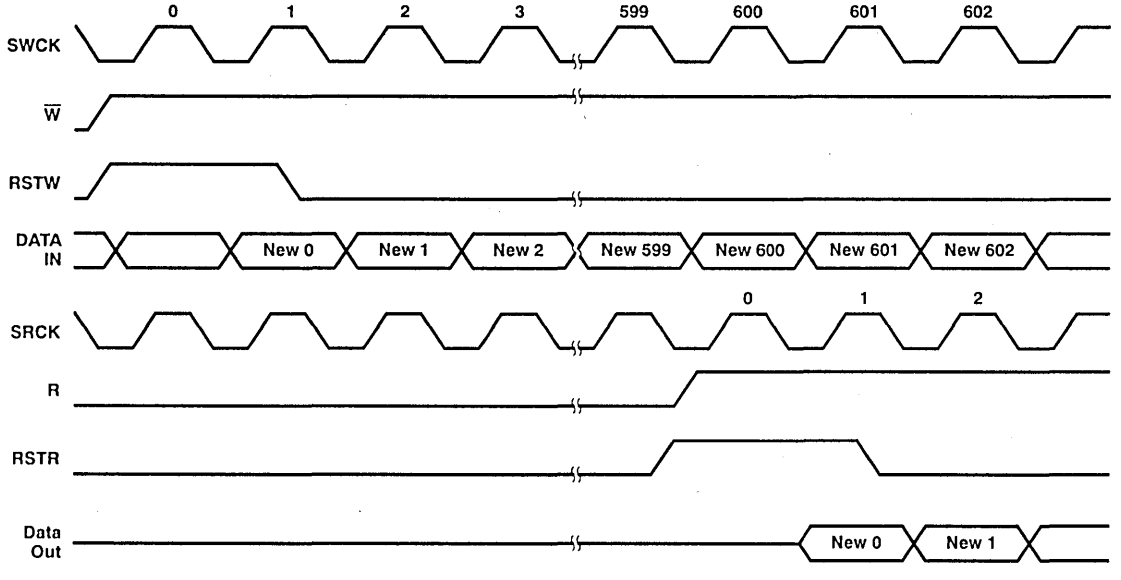
cascade operation-signal connections



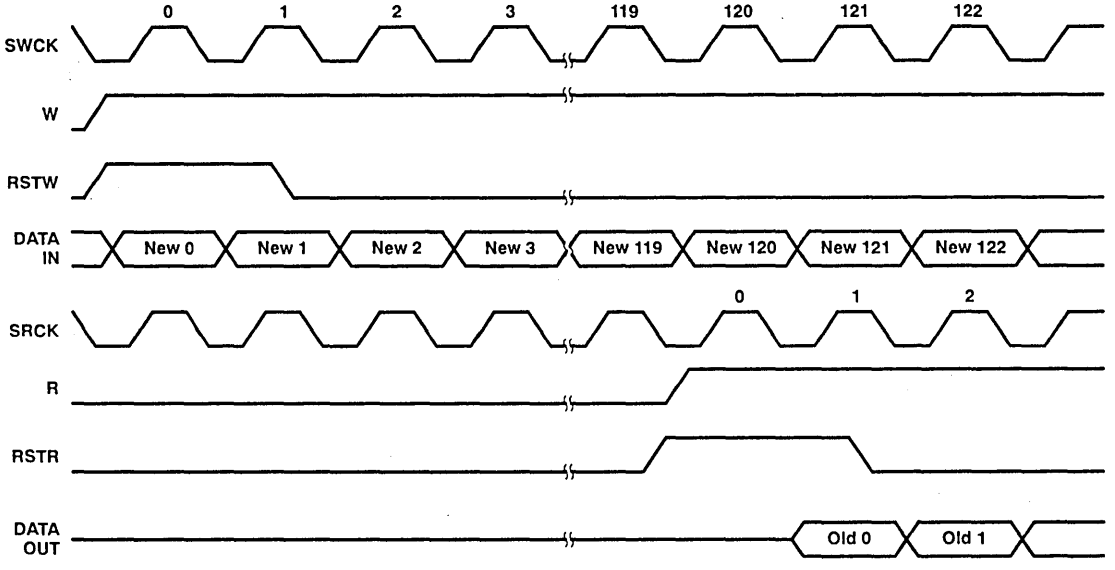
new data access mode (TMS4C1050)



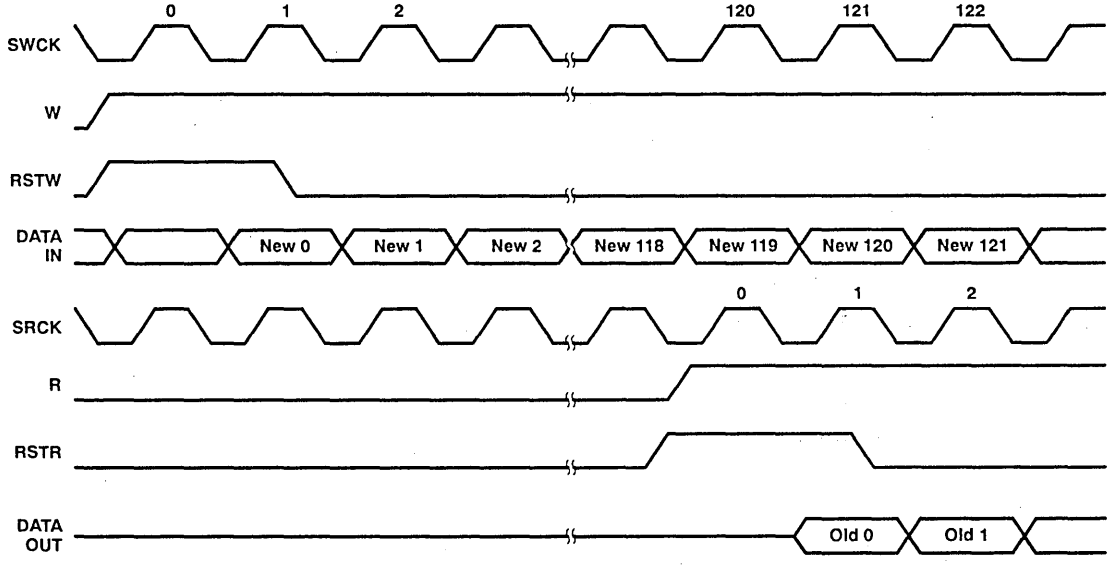
new data access mode (TMS4C1060)



old data access mode (TMS4C1050)



old data access mode (TMS4C1060)

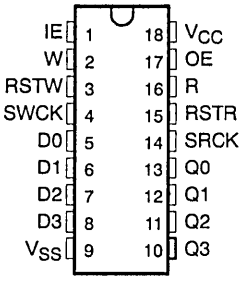


- **262 264 × 4 Organization**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Fast FIFO (First-In First-Out) Operation**
  - **Full Word Continuous Read/Write**
  - **Asynchronous Read/Write**
- **Fully Static (Refresh Free)**
- **High Speed Read/Write Operation**

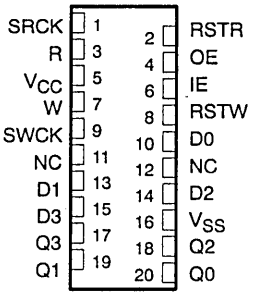
	ACCESS TIME (MAX)	READ CYCLE TIME (MIN)	WRITE CYCLE TIME (MIN)
TMS4C1070-30	25 ns	30 ns	30 ns
TMS4C1070-40	30 ns	40 ns	40 ns
TMS4C1070-60	50 ns	60 ns	60 ns

- **Write Mask Function By Input Enable**
- **Cascade Connection Capability**
- **Low Power Dissipation (Average I_{DD} = 50 mA at Minimum Cycle)**
- **1 Meg DRAM Compatible Process Technology**
- **18-Pin 300-MIL DIP, 20-Pin ZIP, 20/26-Lead Surface Mount SOJ**

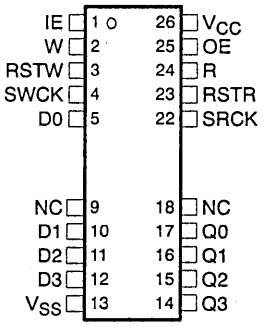
N Package
(Top View)



SD Package
(Top View)



DJ Package
(Top View)



PIN NOMENCLATURE	
D0-D3	Data Inputs
IE	Input Enable
NC	No Internal Connection
OE	Output Enable
Q0-Q3	Data Outputs
R	Read Enable
RSTR	Reset Read
RSTW	Reset Write
SRCK	Serial Read Clock
SWCK	Serial Write Clock
V_{CC}	5-V Supply
V_{SS}	Ground
W	Write Enable

description

The TMS4C1070 is a 4-bit wide dynamic Field Memory (FMEM) that refreshes its storage cells automatically, so that it appears fully static to the user. Internal arbitration logic prevents any conflict between user access to memory and internal refresh operations.

The TMS4C1070 is similar in operation and functionality to Texas Instruments original serial-access memory, the TMS4C1050. Compared to the TMS4C1050, the TMS4C1070 has the following additional functions and features:

a. The Input enable function of the '4C1070 allows the user to write into selected locations of the memory only, leaving the rest of the memory contents unchanged.

b. The serial write and read pointers of the '4C1070 are static registers. This allows the user to interrupt continuous write or read operations for an infinite length of time.

c. The '4C1070 has been designed to allow easy cascading of several memory devices, in order to obtain a larger storage depth or a longer delay.

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Maximum storage capacity is 262 264 words × 4-bits. Read and write access to the TMS4C1070 occurs serially, and normally starts at address 0, after read and write pointers are reset via RSTW and RSTR operations.

Read and write access may occur asynchronously, if desired by the user. When read access is delayed relative to write access, the TMS4C1070 functions like a First-In First-Out (FIFO) register. The amount of delay determines the "length" of this FIFO register. Unlike in a conventional FIFO register, however, data may be read as many times as desired, after it is written into the storage array.

Minimum delay between writing into the device and reading out data is 600 SWCK cycles. Maximum delay is one full field (262 144 write cycles) plus another 119 SWCK cycles.

The TMS4C1070 is offered in an 18-pin dual-in-line plastic package (N suffix), a 20-pin zig-zag in-line package (SD suffix), and a 20/26-lead surface mount SOJ package (DJ suffix). All are characterized for operation from 0°C to 70°C (L suffix).

operation

write operation

The write operation is controlled by two clocks, SWCK, RSTW, and with W, and IE. The write operation is accomplished by cycling SWCK and holding W and IE high after a write address pointer reset operation (RSTW). Each write operation must contain at least 120 write cycles, i.e. two successive RSTW operations must be separated by at least 120 active write cycles (SWCK cycles) while W is high.

To transfer the last data written into the device, which at that time is still stored in the write line buffer to the memory array, an RSTW operation is required after the last SWCK cycle.

reset write (RSTW)

The first positive transition of SWCK after RSTW has gone high resets the write address pointers to zero. RSTW setup and hold times are referenced to the rising edge of SWCK. The state of W may be high or low during any reset operation. Before RSTW may be brought high again for a further reset operation, it must have been low for at least 2 SWCK cycles.

data inputs (D0-D3) and write clock (SWCK)

The SWCK input latches the data inputs on chip when W and IE are high. SWCK also increments the internal write address pointer, when W is high, regardless of the state of IE. Data-in setup and hold times are referenced to the rising edge of SWCK.

write enable (W)

W is used to enable/disable incrementing the internal write address pointer and to enable/disable writing into the memory. A logic high on the W input serves to enable both functions and a logic low serves to disable both functions. W setup and hold times are referenced to the rising edge of SWCK.

input enable (IE)

IE is used to enable/disable writing into memory. A logic high on the IE enables writing, and a logic low disables writing. The internal write address pointer is always incremented by cycling SWCK regardless of IE logic level. Note that IE setup and hold times are referenced to the rising edge of SWCK.

Write Cycle Function Table

SWCK RISING EDGE			
W	IE	Write Address Pointer	D0-D3
H	H	Address Pointer Increment	Store Data
H	L		Not Store
L	X	Address Pointer Stop	Not Store

X = Don't Care

read operation

The read operation is controlled by four clocks, SRCK, RSTR, R, and OE. It is accomplished by cycling SRCK and holding R and OE high after a read address pointer reset operation (RSTR). Each read operation must contain at least 120 read cycles, i.e. two successive RSTR operations must be separated by at least active 120 read cycles (SRCK cycles) while R is high.

Read Cycle Function Table

SRCK RISING EDGE			
R	OE	Read Address Pointer	Q0-Q3
H	H	Address Pointer Increment	Data Out
H	L		HI-Z
L	H	Address Pointer Stop	Data Out
L	L		HI-Z

reset read (RSTR)

The first positive transition of SRCK after RSTR has gone high resets the read address pointers to zero. RSTR setup and hold times are referenced to the rising edge of SRCK. The state of R may be high or low during any reset operation. Before RSTR may be brought high again for a further reset operation, it must have been low for at least 2 SRCK cycles.

data outputs (Q0-Q3) and read clock (SRCK)

Data is shifted out of the data registers on the rising edge of SRCK when R and OE are high during a read operation. The SRCK input increments the internal read address pointer when R is high.

The three-state output buffer provides direct TTL compatibility (no pullup resistor required). Data out is the same polarity as data in. The output becomes valid after the access time interval (t_{AC}) that begins with the positive transition of SRCK. Data out valid time [$t_{V(OUT)}$] is referenced to the rising edge of SRCK in the next cycle.

read enable (R)

R is used to enable/disable incrementing the internal read address pointer. A logic high on the R input enables pointer incrementing by the next following positive SRCK transition, and a logic low disables pointer incrementing. R setup and hold times are referenced to the rising edge of SRCK. The data at the outputs will be the data read out during the SRCK cycle prior to R going low.

output enable (OE)

OE is used as a data out enable/disable. A logic high on the OE input enables the output, and a logic low disables the output. The internal read address pointer is always incremented by cycling SRCK regardless of OE logic level. The outputs will be clocked into the high-impedance (floating) state by the next positive SRCK transition following OE being low. The disable time [$t_{dis(CK)}$] applies. The outputs will be enabled by the next positive SRCK transition following OE being high. The enable time [$t_{en(CK)}$] applies.

power-up and initialization

When the device is powered-up, it is not guaranteed to function properly until at least 100 μs after V_{CC} has stabilized to a value within the range of recommended operating conditions. This time is defined as $t_{POWER-OK}$. After $t_{POWER-OK}$, the following initialization sequence must be performed.

Because the read and write address pointers are not valid after power-up, a minimum of 130 dummy read operations (SRCK cycles) must be performed, followed by an RSTR operation, to properly initialize the read address pointer, and a minimum of 130 dummy write operations (SWCK cycles) must be performed, followed by an RSTW operation, to properly initialize the write address pointer. Dummy read cycles/RSTR and dummy write cycles/RSTW may occur simultaneously.

If these dummy read and write operations start earlier than $t_{POWER-OK}$, while V_{CC} and/or the substrate voltage have not stablized yet, then it is required to perform an RSTR operation plus a minimum of 130 SRCK cycles plus another RSTR operation, and an RSTW operation plus a minimum of 130 SRCK cycles plus another RSTW operation, to properly initialize read and write address pointers.

old/new data access

There must be a minimum delay of 600 SWCK cycles between writing into memory and reading out from memory. If reading of the first field starts, with an RSTR operation, before the start of writing the second field, i.e. before the next RSTW operation, then the data just written in will be read out.

The start of reading out the first field of data may be delayed past the beginning of writing in the second field of data for as many as 119 SWCK cycles. If the RSTR operation for the first field read-out occurs less than 120 SWCK cycles after the RSTW operation for the second field write-in, then the internal buffering of the device assures that the first field will still be read out. The first field of data that is read out while the second field of data is written is called old data.

In order to read out new data, i.e. the second field written in, the delay between RSTW operation and RSTR operation must be at least 600 SWCK cycles. If the delay between RSTW and RSTR operations is more than 120 but less than 600 cycles, then the data read out will be undetermined, it may be old data or new data or a combination of old and new data. Such a timing should be avoided.

cascade operation

The TMS4C1070 has been designed to allow easy cascading of several memory devices, in order to obtain a higher storage depth or a longer delay than can be achieved with only one memory device. See the interconnection diagram on page 8-152 for details.

As illustrated in the timing diagram on page 8-152, the positive SRCK/SWCK edge at the beginning of a clock cycle serves to initiate read-out, whereas writing in is initiated by the positive SWCK/SRCK edge at the end of a clock cycle. This differs from the functionality of the TMS4C1050, in which both the read-out and the write-in are initiated at the beginning of a clock cycle.

internal operation

writing into memory

The first 120 words of data following the initial RSTW operation after power-up are written into a cache buffer, the A line buffer initially, and will never get stored elsewhere, to allow read-out of data later without the delay involved in retrieving it from the main memory array.

Starting from address 121, data is written into the write line buffer, top block, until this block (256 words long) is full. Further writing then occurs to the bottom block of the write line buffer, while the top block is transferred to the main memory array. By the time the bottom block is full, the top block has been transferred to memory and can be used again to receive new incoming data. The channelling of input data into the top or bottom block is controlled internally by the device and is transparent to the user.

After the 120-word long cache buffer has been filled with incoming data, the input line selector switches the connection of the input port over to the B line buffer, to assure that the next field of data which will arrive later, after a subsequent RSTW operation, does not over-write the content of the cache buffer. Each subsequent filling of the cache buffer toggles the connection of the input port between the A and the B line buffers with the 121st SWCK pulse. The A and B line buffers, as well as the input line selector, are static registers.

The connection of the output port will also be toggled between the A and B line buffers by the 121st SWCK pulse, providing no read operation from a cache buffer is in progress at this time. The output port will always be connected to the line buffer opposite to the one connected to the input port. In case a read operation from a cache buffer is in progress when the 121st SWCK occurs, the toggling of the output port connection will be delayed until the cache buffer has been read out completely.

The requirement stated on page 8-143 that each write operation must contain at least 120 active SWCK cycles, exists in order to assure that the toggling of the input and the output ports between the A line buffer and the B line buffer functions without errors as described above.

The serial write pointer stores the (column) address of the last input data word received, while the write counter stores the row address. The serial write pointer of the TMS4C1070 is a static register. Therefore no limit exists for the maximum period of clocking inactivity, as was the case for the TMS4C1060.

After the last word of a full write cycle has been latched in (with a positive transition of the SWCK clock), the write line buffer most likely will be partially filled without having been transferred to the main memory array. To assure that the information contained in the write line buffer is stored also and cannot be lost, it is required that an RSTW operation be performed within 1 ms after input = write clocking has stopped.

In addition to transferring the partially filled write line buffer into the main memory array, this RSTW operation will also reset the write addresses (serial write pointer) to zero, and due to the internal construction of the dynamic serial write pointer register, this initial address of zero remains stored indefinitely. So regardless of how much later a new write cycle starts, it is not necessary to perform another RSTW operation again at that time.

reading from memory

After an RSTR operation, data from the main memory array (starting at address 121) will be transferred to read line buffer. Because this transfer required some time, the first 120 words will be read out of the A or B line buffer, where they had been stored before (see writing into memory).

If the first RSTR operation occurs after the first but before the second RSTW operation, read access will be to the same buffer that data had been written into during the first write cycle. Thus old data will be read out.

If the first RSTR occurs after the second RSTW operation, i.e. after the writinging of new data has already started, then the delay between second RSTW and first RSTR operation determines, whether old data or new data will be read out.

If this delay is less than 120 SWCK cycles, then the data will be read out from the line buffer that it was written into during the previous write cycle, i.e. old data will be read out. A delay of less than 120 SWCK cycles will also assure that all following data words are old data, because replacement of old data by new data in the main memory array will occur later than the respective read access to each address in the array.

If this delay is more than 600 SWCK cycles, then the data will be read out from the line buffer that it was written into during the current write cycle, i.e. new data will be read out. A delay of more than 600 SWCK cycles will also assure that all following data words are new data, because replacement of old data by new data in the main memory array will occur before the respective read access to each address in the array.

If this delay is more than 120 but less than 600 SWCK cycles, then the data read out can be either old or new or a mixture of old and new data, because it cannot be predicted accurately, whether a word accessed for reading has already been replaced by new data or not. Such a situation should be avoided.

After the first 120 words are read out of the A or B line buffer, read transfer from the main memory array to read line buffer is finished, and subsequent reading will occur from this buffer. Similar to the write operation, while one half of this buffer is being read out, the other half will be filled again by a new read transfer from the main memory array.

The serial read pointer stores the (column) address of the last data word read out, while the read counter stores the row address. The serial read pointer of the TMS4C1070 is a static register. Therefore no limit exists for the maximum period of clocking inactivity.

self-refresh and arbitration logic

The self-refresh and arbitration logic will keep the main memory information refreshed automatically without requiring any user action, control the address pointers for both read and write, and control the flow of information both into and out of the main memory.

ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin except (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... 0 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		V_{CC}+1	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: V_{IL} = – 1.5 V undershoot is allowed when device is operated in the range of recommended supply voltage.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4C1070-30		TMS4C1070-40		TMS4C1070-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5 V, OE low		±10		±10		±10	µA
I_{DD1}	Average operating current	Minimum write/read cycle, OE low		50		45		35	mA
I_{DD2}	Average standby current	After 1 RSTW/RSTR cycle, W and R low		10		10		10	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance	V_I = 0			7	pF
C_O	Output capacitance	V_I = 0			10	pF

† V_{CC} equal to 5 V ± 0.5 V and the bias under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	TMS4C1070-30		TMS4C1070-40		TMS4C1070-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AC}	Access time from SRCK high	see Note 3		25		30		50	ns
$t_{dis(CK)}$	Output disable time after SRCK high	see Note 4	6	25	6	25	6	25	ns
$t_{en(CK)}$	Output enable time after SRCK high	see Note 3	6	25	6	25	6	25	ns
$t_{v(OUT)}$	Output valid time after SRCK high	See Note 3	6		6		6		ns

NOTES: 3. The load connected to each output is a 50 pF capacitor to ground, in parallel with a 218 Ohm resistor to 1.31 V. (See Figure 1.)
4. Disable times are specified from the initiating timing edge until the output is no longer driven by the memory. If disable times are to be measured by observing output voltage waveforms, sufficiently low load resistors and capacitors have to be used, and the RC time constants of the load have to be taken into account.

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

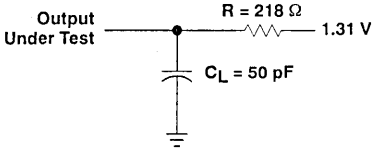


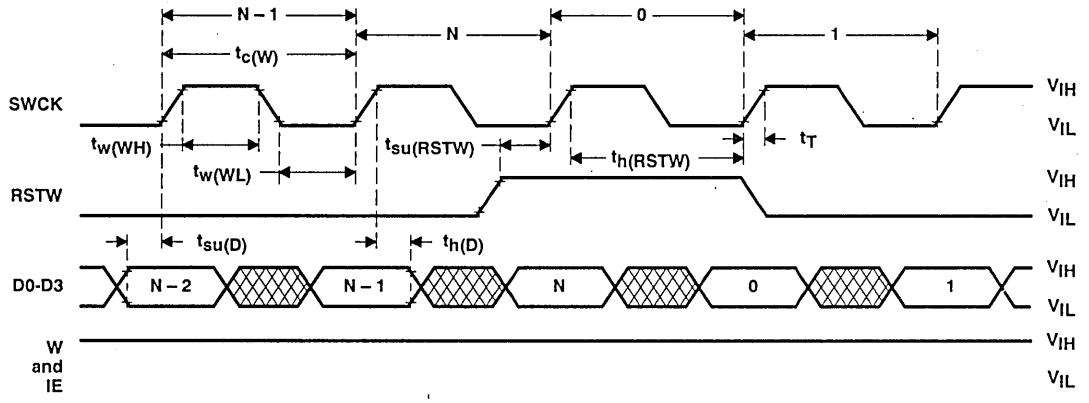
Figure 1. Output Load Circuit

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Notes 5 and 6)

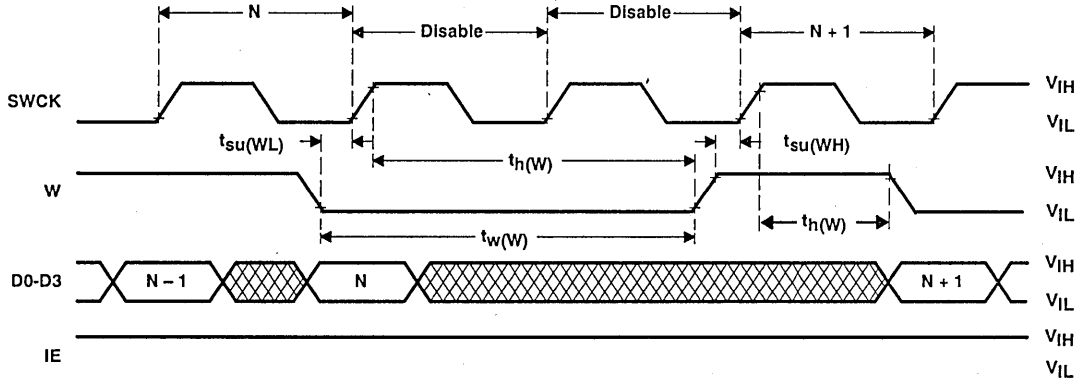
		TMS4C1070-30		TMS4C1070-40		TMS4C1070-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time	30		40		60		ns
$t_{c(R)}$	Read cycle time	30		40		60		ns
$t_{w(R)}$	Pulse duration, R-low	10		10		10		ns
$t_{w(W)}$	Pulse duration, W-low	10		10		10		ns
$t_{w(IE)}$	Pulse duration, IE low	10		10		10		ns
$t_{w(OE)}$	Pulse duration, OE low	10		10		10		ns
$t_{w(RH)}$	Pulse duration, SRCK high	12		17		20		ns
$t_{w(RL)}$	Pulse duration, SRCK low	12		17		20		ns
$t_{w(WH)}$	Pulse duration, SWCK high	12		17		20		ns
$t_{w(WL)}$	Pulse duration, SWCK low	12		17		20		ns
$t_{su(D)}$	Data setup time before SWCK high	5		5		5		ns
$t_{su(RH)}$	R-high setup time before SRCK high	0		0		0		ns
$t_{su(RL)}$	R-low setup time before SRCK high	0		0		0		ns
$t_{su(WH)}$	W-high setup time before SWCK high	0		0		0		ns
$t_{su(WL)}$	W-low setup time before SWCK high	0		0		0		ns
$t_{su(IEH)}$	IE high setup time before SWCK high	0		0		0		ns
$t_{su(IEL)}$	IE low setup time before SWCK high	0		0		0		ns
$t_{su(OEH)}$	OE high setup time before SRCK high	0		0		0		ns
$t_{su(OEL)}$	OE low setup time before SRCK high	0		0		0		ns
$t_{su(RSTR)}$	RSTR setup time before SRCK high	3		3		3		ns
$t_{su(RSTW)}$	RSTW setup time before SWCK high	3		3		3		ns
$t_{h(D)}$	Data hold time after SWCK high	6		6		6		ns
$t_{h(R)}$	R hold time after SRCK high	6		6		6		ns
$t_{h(W)}$	W hold time after SWCK high	6		6		6		ns
$t_{h(IE)}$	IE hold time after SWCK high	6		6		6		ns
$t_{h(OE)}$	OE hold time after SRCK high	6		6		6		ns
$t_{h(RSTR)}$	RSTR hold time after SRCK high	6		6		6		ns
$t_{h(RSTW)}$	RSTW hold time after SWCK high	6		6		6		ns
t_T	Input transition time	3	30	3	30	3	30	ns

NOTES: 5. Timing measurements are referenced to V_{IH} (MIN) = 2.4 V and V_{IL} (MAX) = 0.8 V. t_T is measured between V_{IH} (MIN) and V_{IL} (MAX).
6. All cycle times assume t_T = 35 ns.

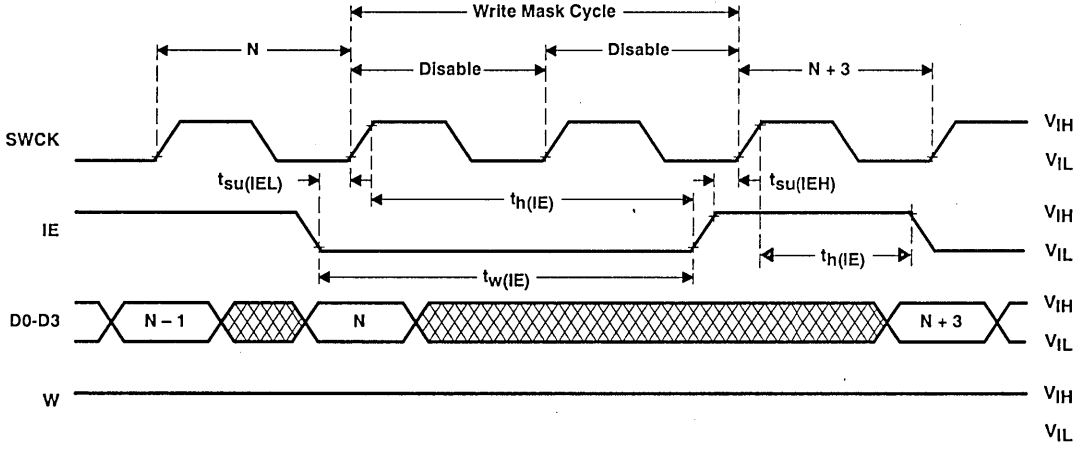
write cycle timing (reset write)



write cycle timing (write enable)

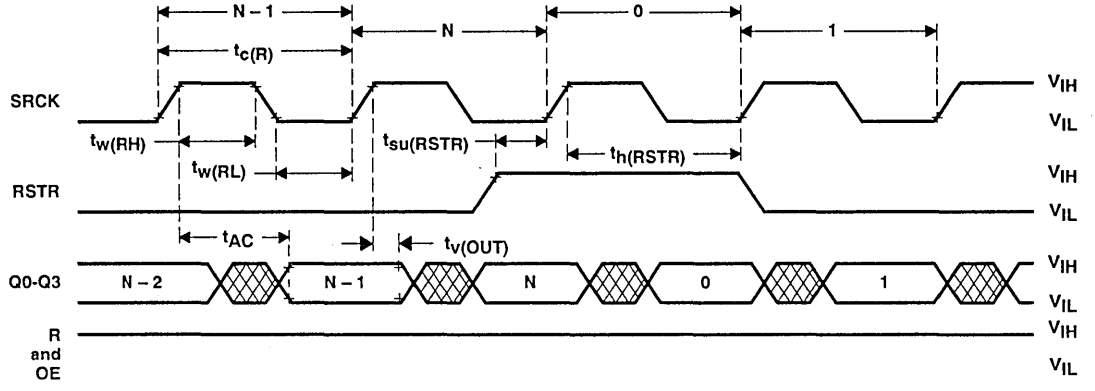


write cycle timing (input enable = write mask operation)

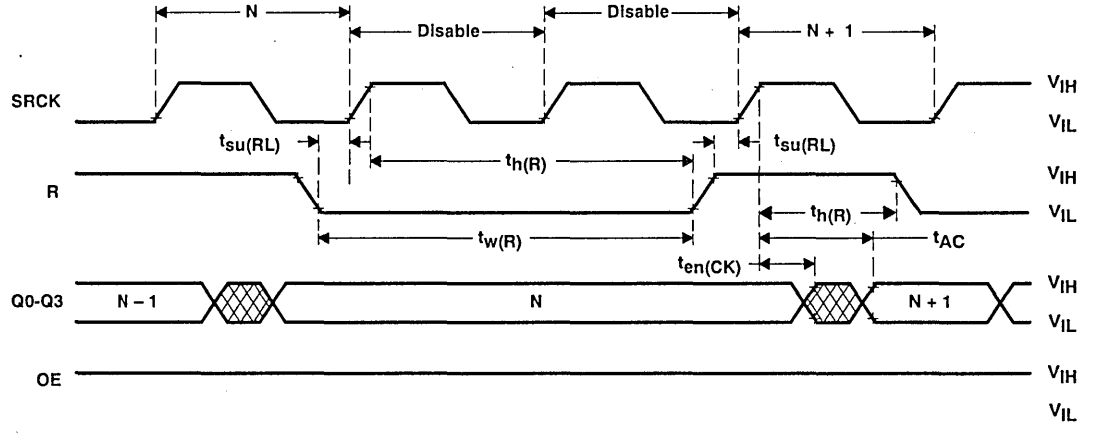


ADVANCE INFORMATION

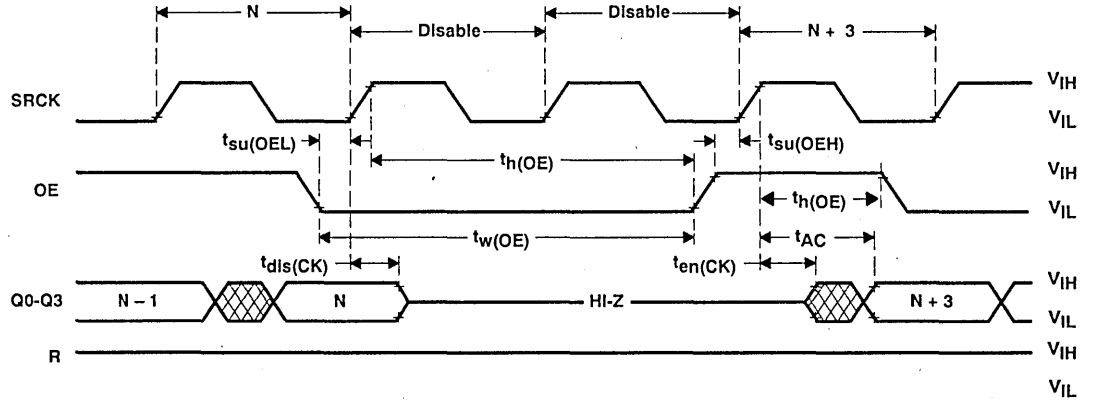
read cycle timing (reset read)



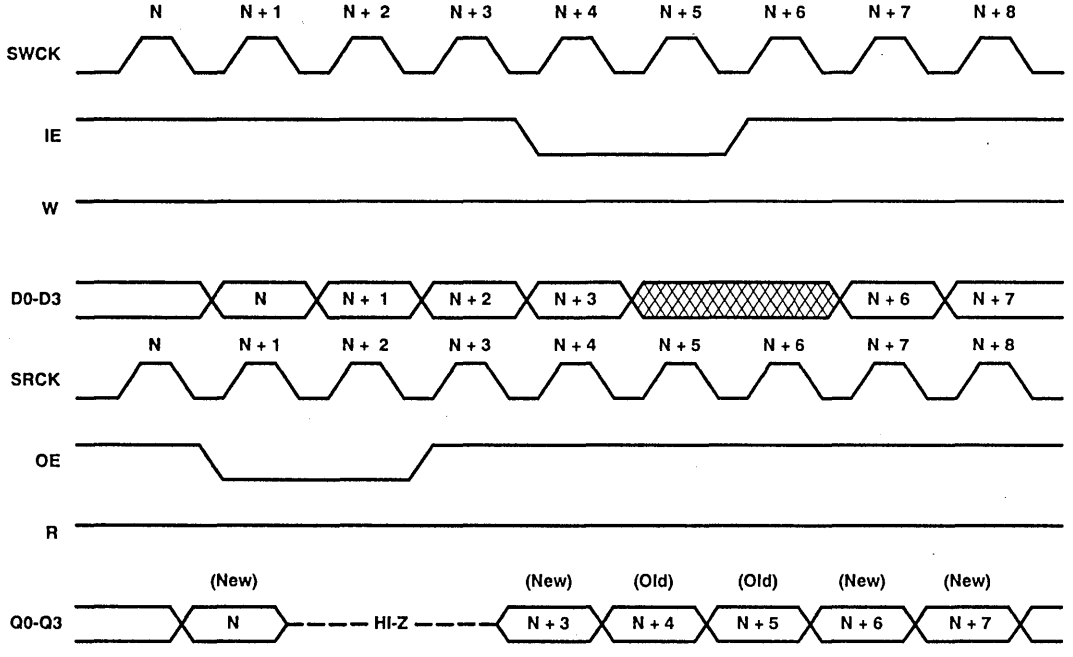
read cycle timing (read enable)



read cycle timing (output enable)



write mask operation



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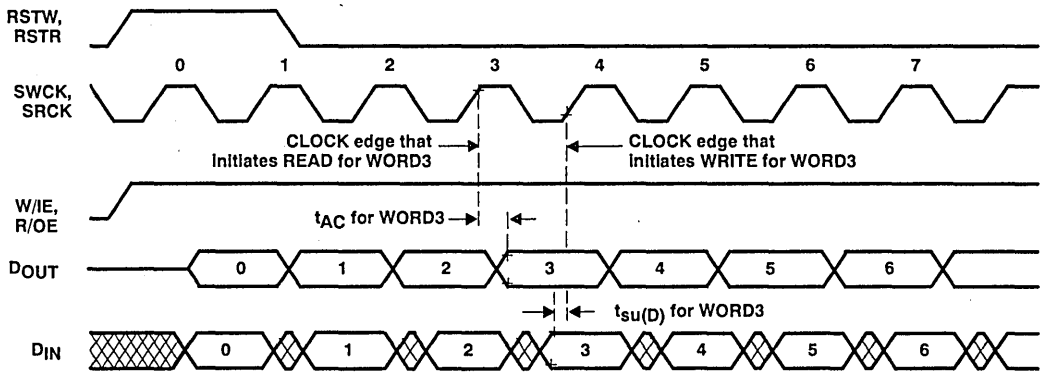
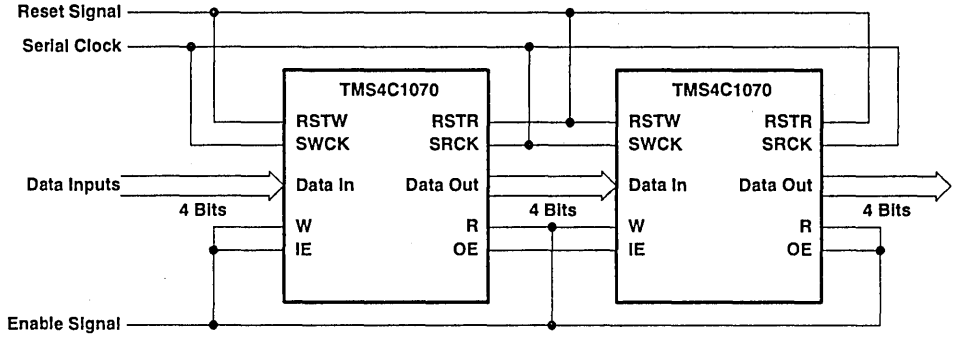
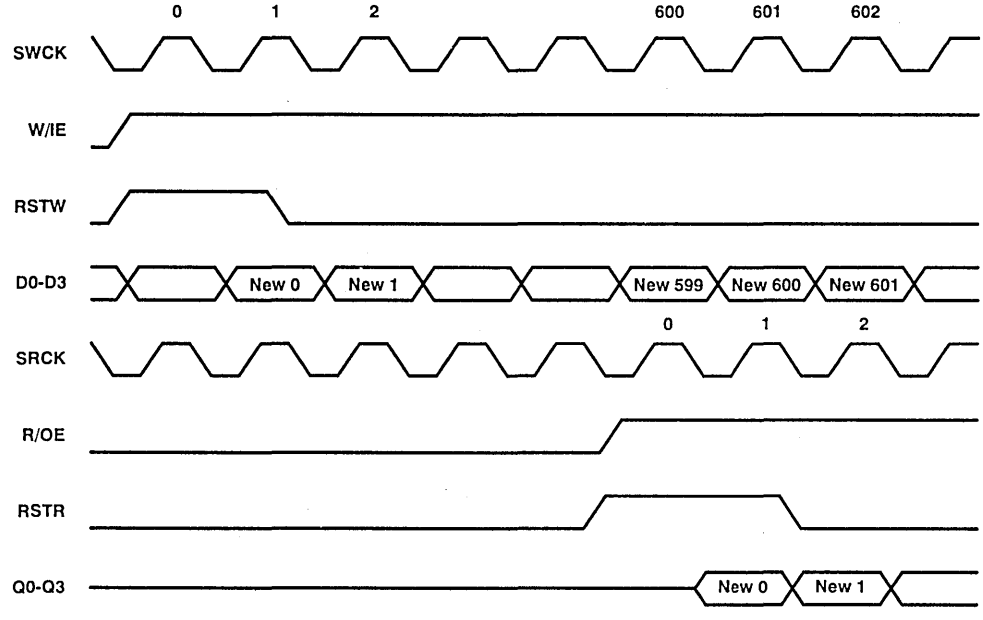
cascade mode



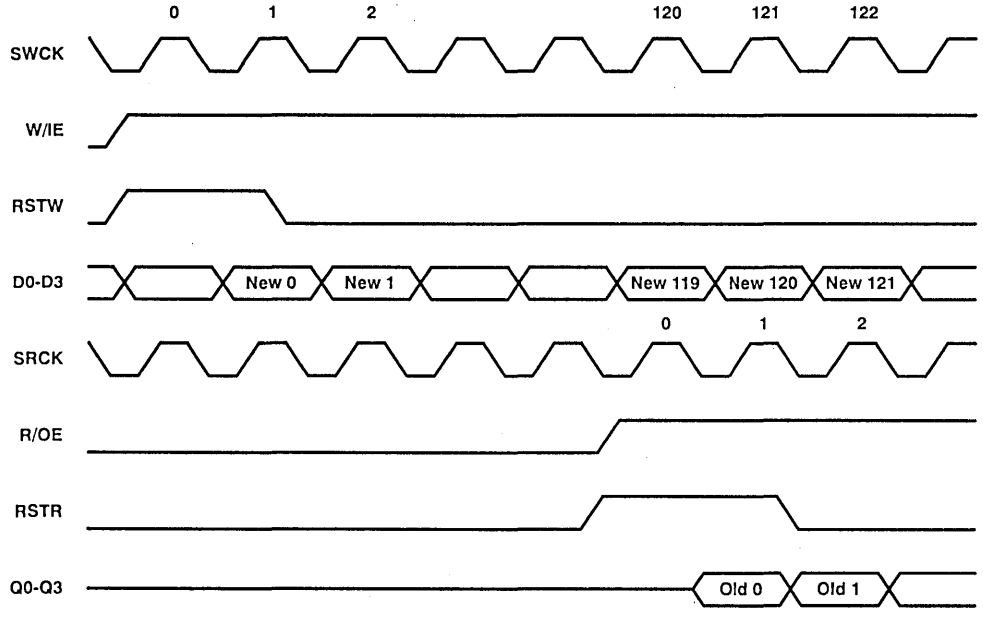
cascade operation-signal connections



new data access mode



old data access mode

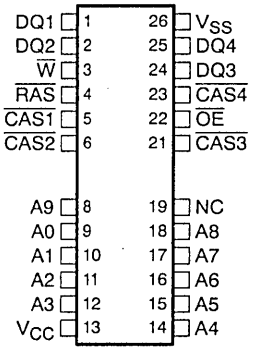


- 1 048 576 × 4 Organization
- Single 5-V Supply (10% Tolerance)
- Performance Ranges:

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{CAA} (MAX)	READ OR WRITE CYCLE (MAX)
TMS44460-60	60 ns	15 ns	30 ns	110 ns
TMS44460-70	70 ns	20 ns	35 ns	130 ns
TMS44460-80	80 ns	20 ns	40 ns	150 ns
TMS44460-10	100 ns	25 ns	45 ns	190 ns

- Four Separate $\overline{CAS}$ Pins Provide for Separate I/O Operation
- Parity Mode and Enhanced Page Mode Operation
- 1024-Cycle Refresh in 16 ms (Max)
- 3-State Unlatched Output
- Low Power Dissipation
- Texas Instruments EPIC™ CMOS Process
- All Inputs, Outputs and Clocks are TTL Compatible
- High-Reliability Plastic 24/26-Lead 300-Mil-Wide Surface Mount (SOJ) Package
- Operating Free-Air Temperature . . . 0°C to 70°C

DJ Package† (Top View)



†The package shown here is for pinout reference only and is not drawn to scale.

PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS1}$-$\overline{CAS4}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

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description

The TMS44460 is a high-speed, 4 194 304-bit dynamic random access memory organized as 1 048 576 words of four bits each. It employs state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at low cost.

This device features maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 413 mW operating and 6 mW standby on 80 ns devices.

Four separate $\overline{CAS}$ pins ($\overline{CAS1}$-$\overline{CAS4}$) provide for separate I/O operation allowing this device to operate in parity mode. The TMS44460 also functions in enhanced page mode, similar to the TMS44400.

The EPIC™ technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{CC} peaks are 140 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS44460 is offered in a 300-mil wide 24/26 J-lead plastic surface mount SOJ (DJ suffix) package. This device is characterized for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

operation

parity mode

Four $\overline{CAS}$ pins ($\overline{CAS1}$-$\overline{CAS4}$) are provided to give independent control of the four data I/O pins (DQ1-DQ4). For read or write cycles, the column address is latched on the first $\overline{CASx}$ falling edge. Each $\overline{CASx}$ pin going low enables its corresponding DQ pin with data coming from the column address latched on the first falling $\overline{CASx}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{CASx}$ edge.The delay time from $\overline{CASx}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{CAS}$ to its corresponding DQx pin.

In order to latch in a new column address, all four $\overline{CASx}$ pins must be brought high. The column precharge time (see parameter t_{CP}) is measured from the last $\overline{CASx}$ rising edge to the first falling $\overline{CASx}$ edge of the new cycle. In order for a column address to remain valid while toggling $\overline{CASx}$, there exists a minimum setup time (t_{CLCH}) where at least one $\overline{CASx}$ must be brought low before all other $\overline{CASx}$ pins are taken high.

For early write cycles, the data is latched on the first falling $\overline{CASx}$ edge. Only the DQs that have the corresponding $\overline{CASx}$ low will be written into. Each $\overline{CASx}$ will have to meet t_{CAS} minimum in order to ensure writing into the storage cell. In order to latch a new address and new data, all $\overline{CASx}$ pins need to come high and meet t_{CP}.

This DQ independence allows the TMS44460 to provide four parity bits in memory designs which normally require the use of four 1 Meg × 1 DRAMs.

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CASx}$ page-mode cycle time used. With minimum $\overline{CASx}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CASx}$ is high. The falling edge of the first $\overline{CASx}$ latches the column addresses. This feature allows the TMS44460 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CASx}$ transitions low. This performance improvement is referred to as "enhanced page mode". Valid column address may be presented immediately after t_{RAH} (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CASx}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CASx}$ low) if t_{CAA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CASx}$ goes high, minimum access time for the next cycle is determined by t_{CAP} (access time from rising edge of the last $\overline{CASx}$).

address (A0 through A9)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Ten row-address bits are set up on pins A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the first column-address strobe ($\overline{CASx}$). All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CASx}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. The TMS44460 $\overline{CASx}$ is used as a chip select activating its corresponding output buffer, as well as latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CASx}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation with $\overline{OE}$ grounded.

data in (DQ1-DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CASx}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CASx}$ and the data is strobed in by the first occurring $\overline{CASx}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CASx}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CASx}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins with the negative transition of $\overline{CASx}$ as long as t_{RAC} and t_{CAA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CASx}$ to be brought low for the output buffers to go into low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{CASx}$ is brought high.

refresh

A refresh operation must be performed at least once every sixteen milliseconds to retain data. This can be achieved by strobing each of the 1024 rows (A0-A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding all $\overline{CASx}$ at the high (inactive) level, thus conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CASx}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

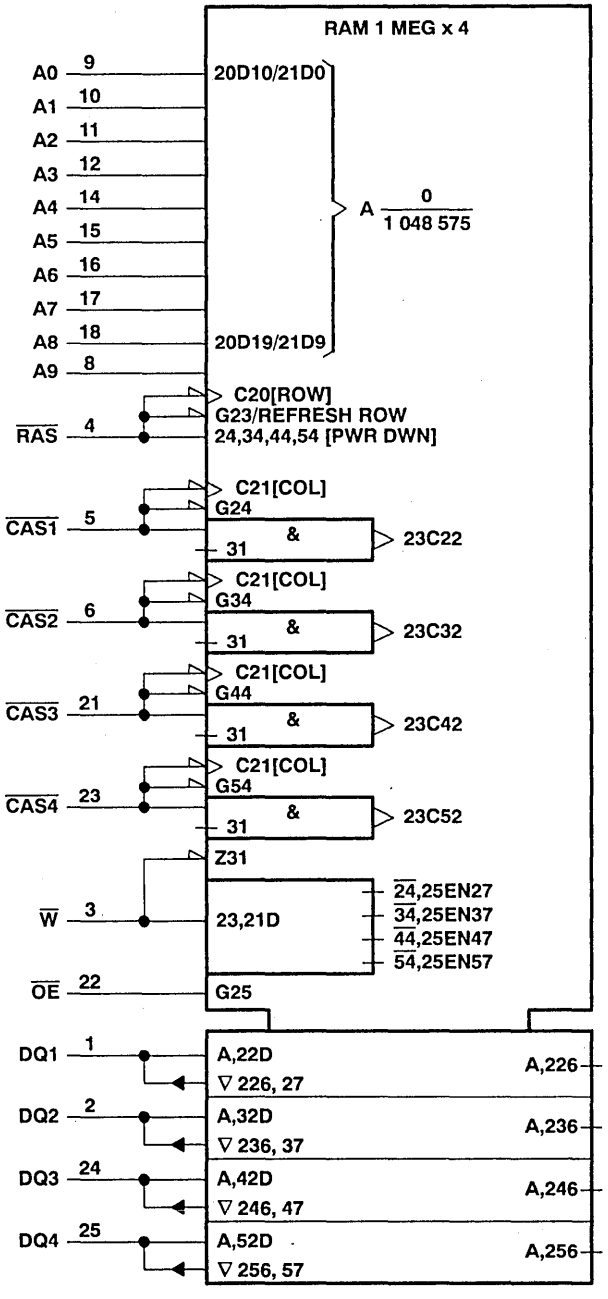
$\overline{CASx}$-before-$\overline{RAS}$ refresh

$\overline{CASx}$-before-$\overline{RAS}$ refresh is utilized by bringing write enable ($\overline{W}$) high and at least one $\overline{CASx}$ low earlier than $\overline{RAS}$ and holding it low after $\overline{RAS}$ falls (see parameters t_{WSR} and t_{CSR}) and holding $\overline{W}$ high and $\overline{CASx}$ low after $\overline{RAS}$ falls (see parameters t_{WHR} and t_{CHR}). For successive $\overline{CASx}$-before-$\overline{RAS}$ refresh cycles, write enable ($\overline{W}$) must remain high and $\overline{CASx}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

power-up

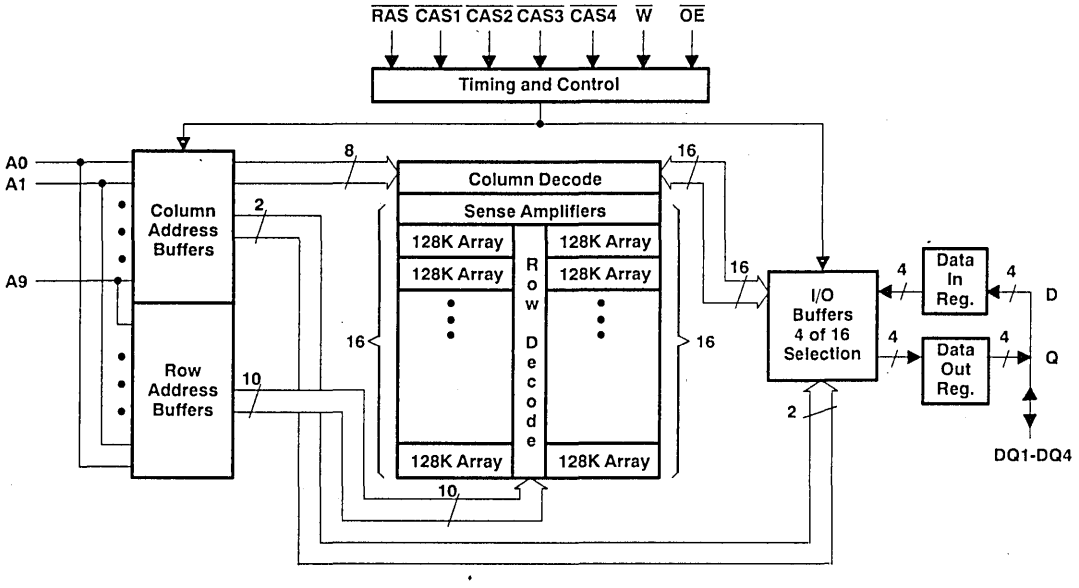
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after power-up to the full V_{CC} level. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... −1 V to 7 V
Voltage range on V_{CC} ..... −1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TMS44460-60		TMS44460-70		TMS44460-80		TMS44460-10		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to 6.5 V, V_{CC} = 5.5 V, $\overline{CAS}$ high			± 10		± 10		± 10		± 10	µA
I_{CC1}	Read/write cycle current	t_{RWC} = minimum, V_{CC} = 5.5 V			95		85		75		65	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V	TTL		2		2		2		2	mA
			CMOS		1		1		1		1	
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR)	t_{RWC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low, after $\overline{CAS}$ low (CBR)			95		85		75		65	mA
I_{CC4}	Average page current	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling			70		60		50		40	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)†

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(D)}$	Input capacitance, data inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

† Capacitance measurements are made on a sample basis only.

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER		TMS44460-60		TMS44460-70		TMS44460-80		TMS44460-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CAA}	Access time from column address		30		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20		25	ns
t_{CAP}	Access time from column precharge		35		40		45		50	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 4)	0	15	0	18	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 4)	0	15	0	18	0	20	0	25	ns

NOTE 4: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

		TMS44460-60		TMS44460-70		TMS44460-80		TMS44460-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time (see Note 6)	110		130		150		180		ns
t_{WC}	Write cycle time	110		130		150		190		ns
t_{RWC}	Read-write/read-modify-write cycle time	155		181		205		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 7)	40		45		50		55		ns
t_{PCM}	Page-mode read-modify-write cycle time	85		96		105		120		ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 8)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{WP}	Write pulse duration	15		15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time before $\overline{W}$ low (see Note 10)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time (see Note 11)	10		10		10		10		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 12)	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low (see Note 10)	10		15		15		20		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 13)	50		55		60		75		ns
t_{CLCH}	Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high	5		5		5		5		ns
t_{DH}	Data hold time after $\overline{CAS}$ low (see Note 10)	10		15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 13)	50		55		60		75		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 14)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 14)	0		0		0		0		ns
t_{WHR}	$\overline{W}$-high hold time (see Note 11)	10		10		10		10		ns

Continued next page.

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_T = 5 ns.
7. $t_{PC} > t_{CP}$ min + t_{CAS} min + $2t_T$.
8. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time (t_{CAS}).
9. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
12. Early write operation only.
13. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5) (concluded)

		TMS44460-60		TMS44460-70		TMS44460-80		TMS44460-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{WCH}	Write hold time after $\overline{CAS}$ low (see Note 12)	15		15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 13)	50		55		60		75		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		25		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 15)	40		46		50		60		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 16)	20	45	20	52	20	60	25	75	ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 16)	15	30	15	35	15	40	20	50	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 15)	85		98		110		135		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (see Note 15)	55		63		70		80		ns
t_{CLZ}	Delay time, $\overline{CAS}$ low to output low Z	0		0		0		0		ns
t_{OED}	Delay time, $\overline{OE}$ high before data at DQ	15		18		20		25		ns
t_{ROH}	Delay time, $\overline{OE}$ low to $\overline{RAS}$ high	10		10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 11)	15		15		20		20		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 11)	10		10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 11)	0		0		0		0		ns
t_{REF}	Refresh time interval		16		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	2	50	ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
11. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
12. Early write operation only.
13. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
15. Read-modify-write operation only.
16. Maximum value specified only to guarantee access time.

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

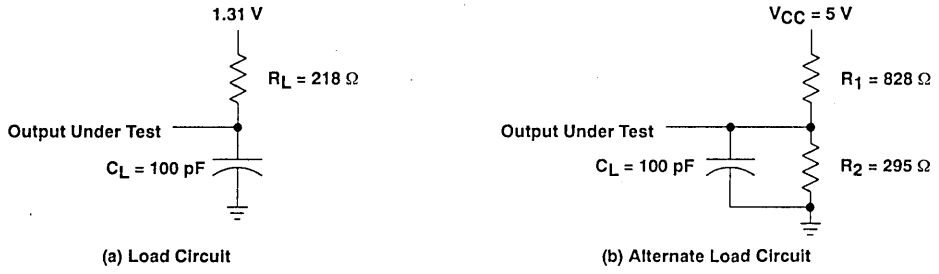
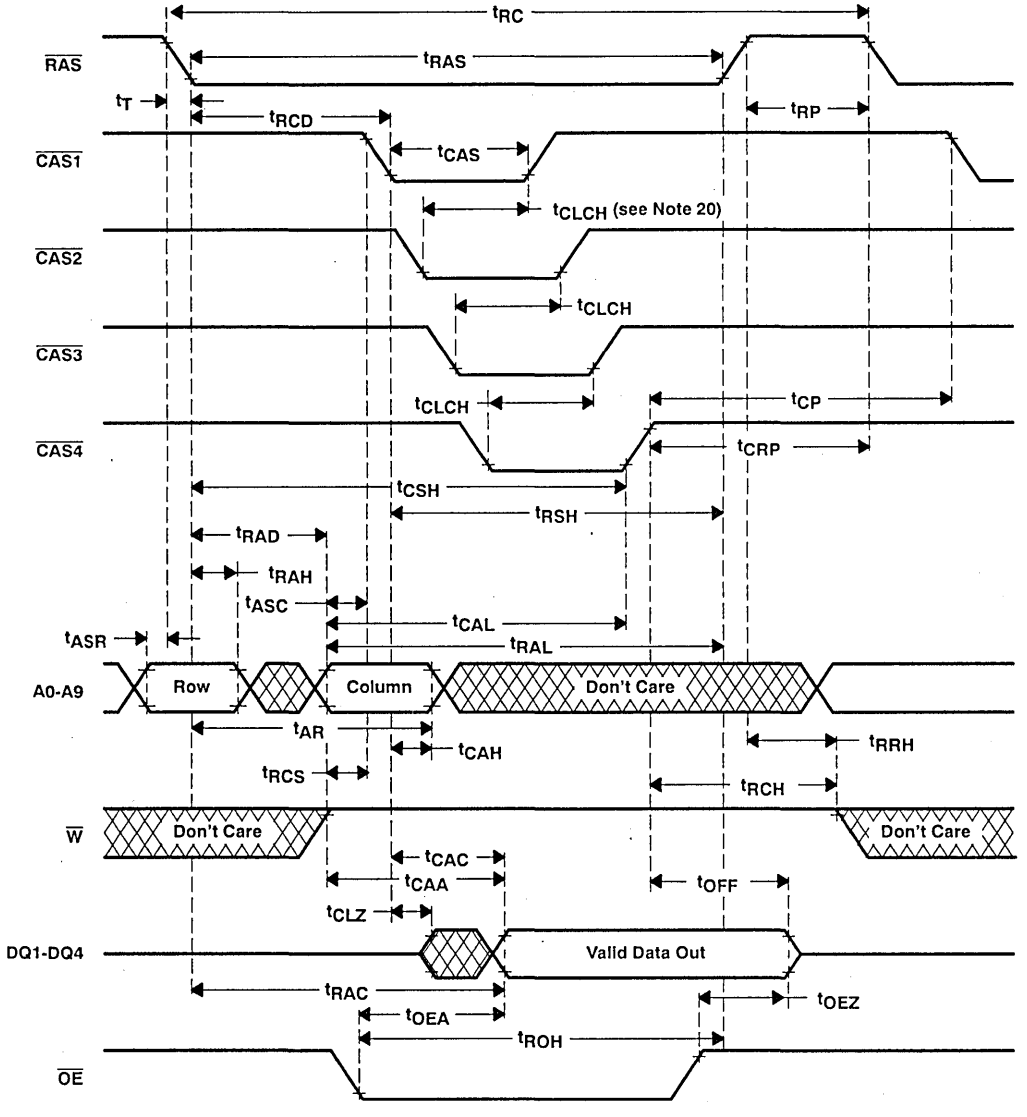


Figure 1. Load Circuits for Timing Parameters

ADVANCE INFORMATION

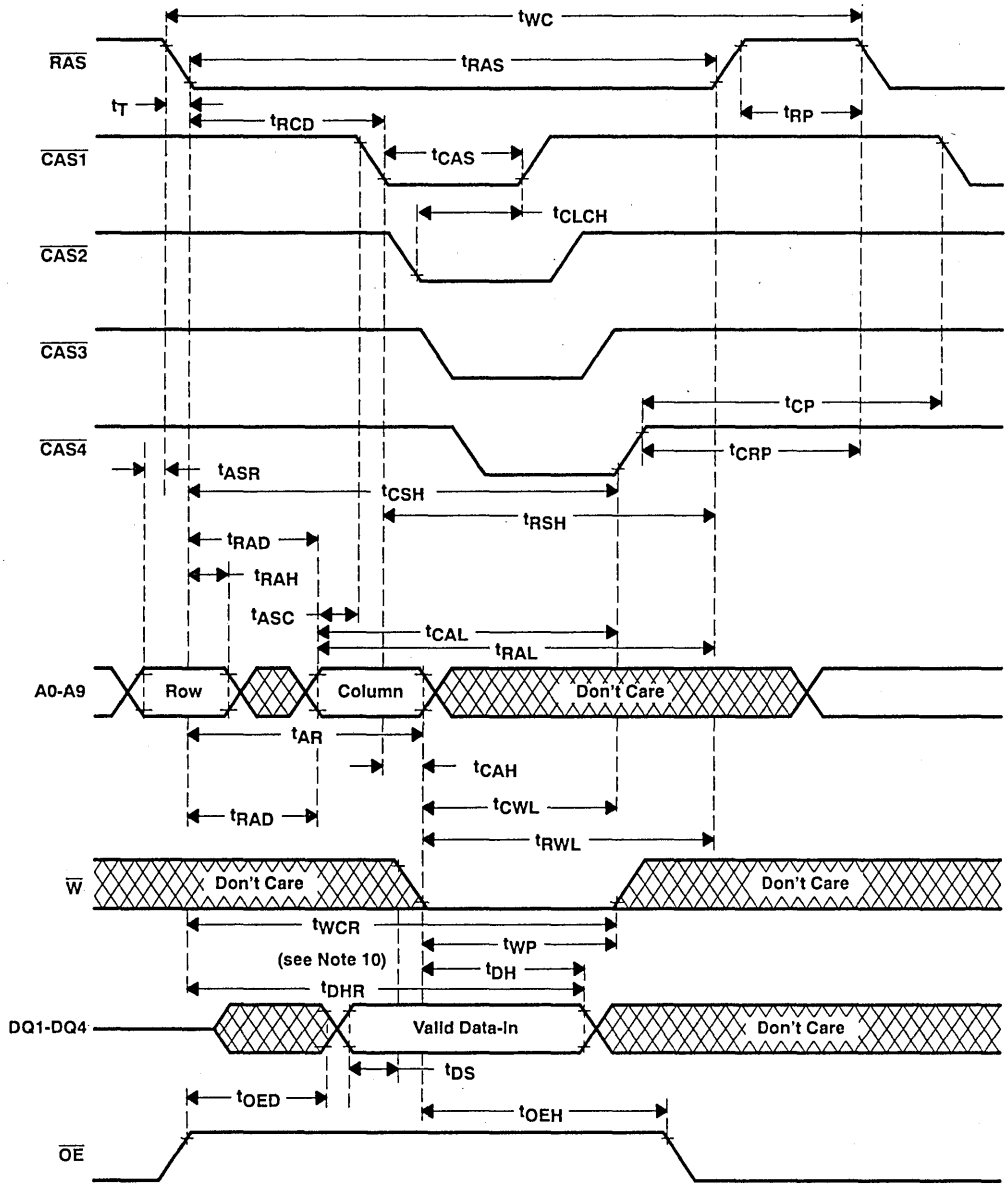
ADVANCE INFORMATION

read cycle



NOTES: 17. In order to hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
18. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
19. $\overline{CASx}$ order is arbitrary.
20. Output may go from high-impedance to an invalid data state prior to the specified access time.

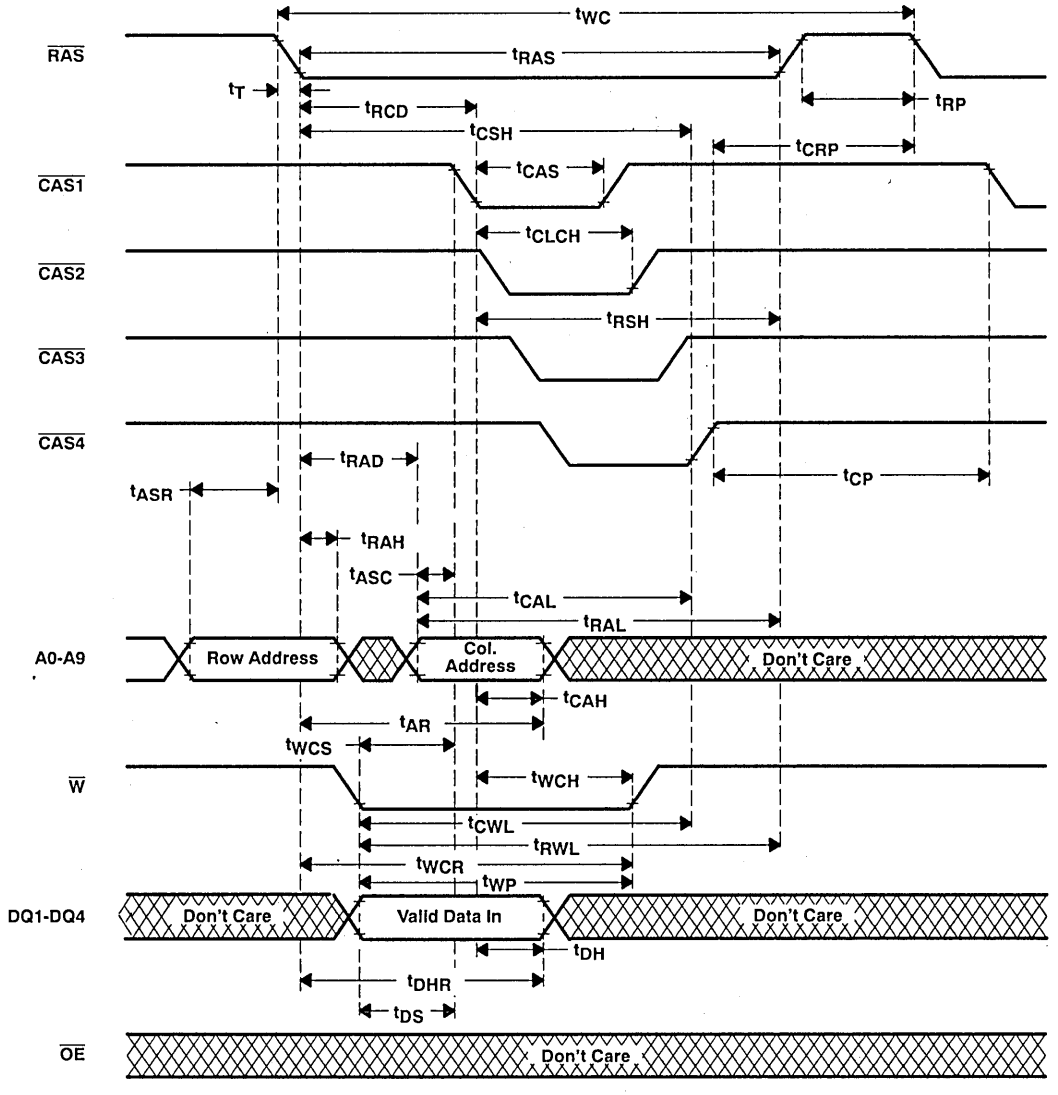
write cycle



NOTES: 10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
17. In order to hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
18. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
19. $\overline{CASx}$ order is arbitrary.

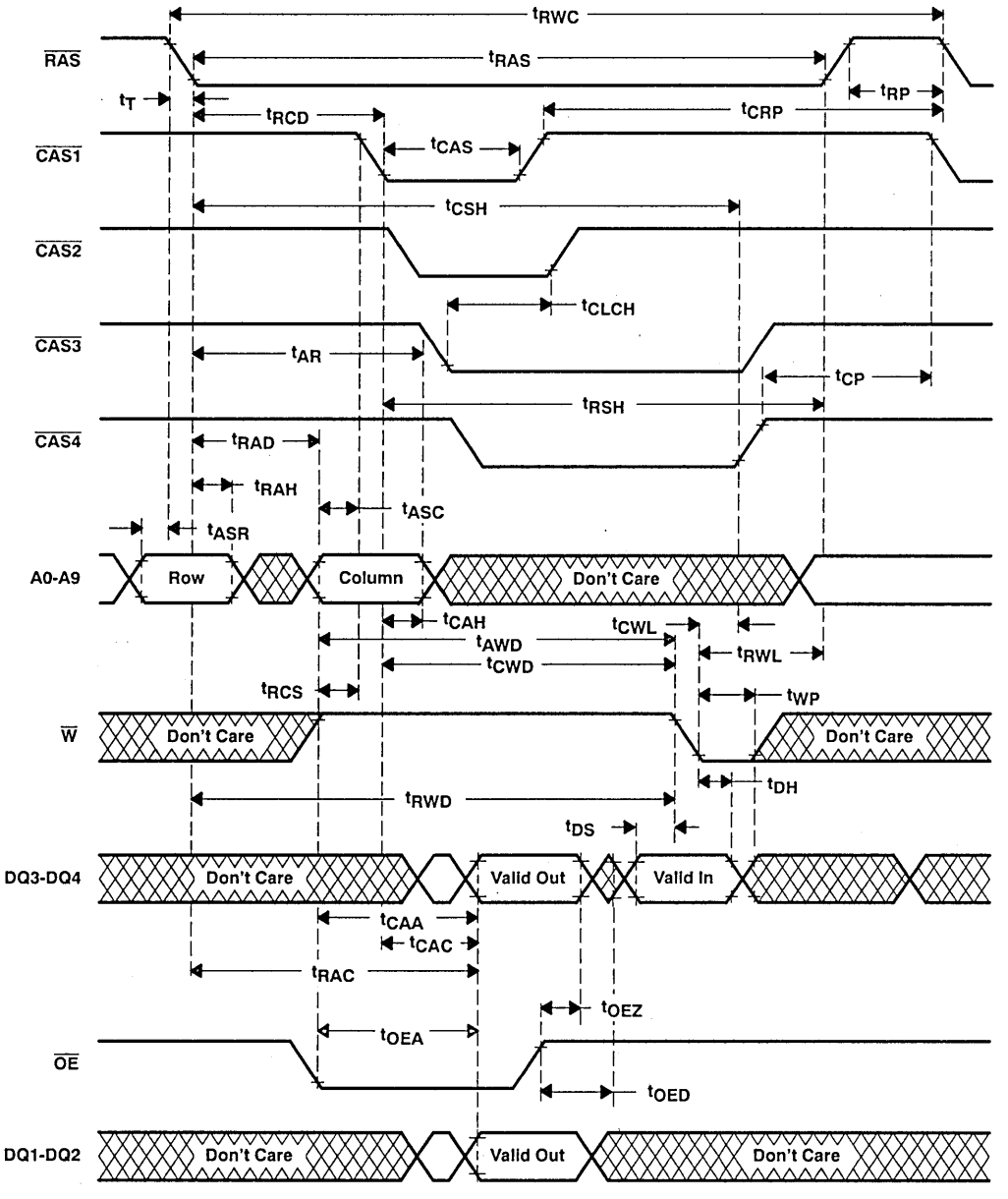
ADVANCE INFORMATION

early write cycle timing



NOTES: 17. In order to hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
18. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
19. $\overline{CASx}$ order is arbitrary.

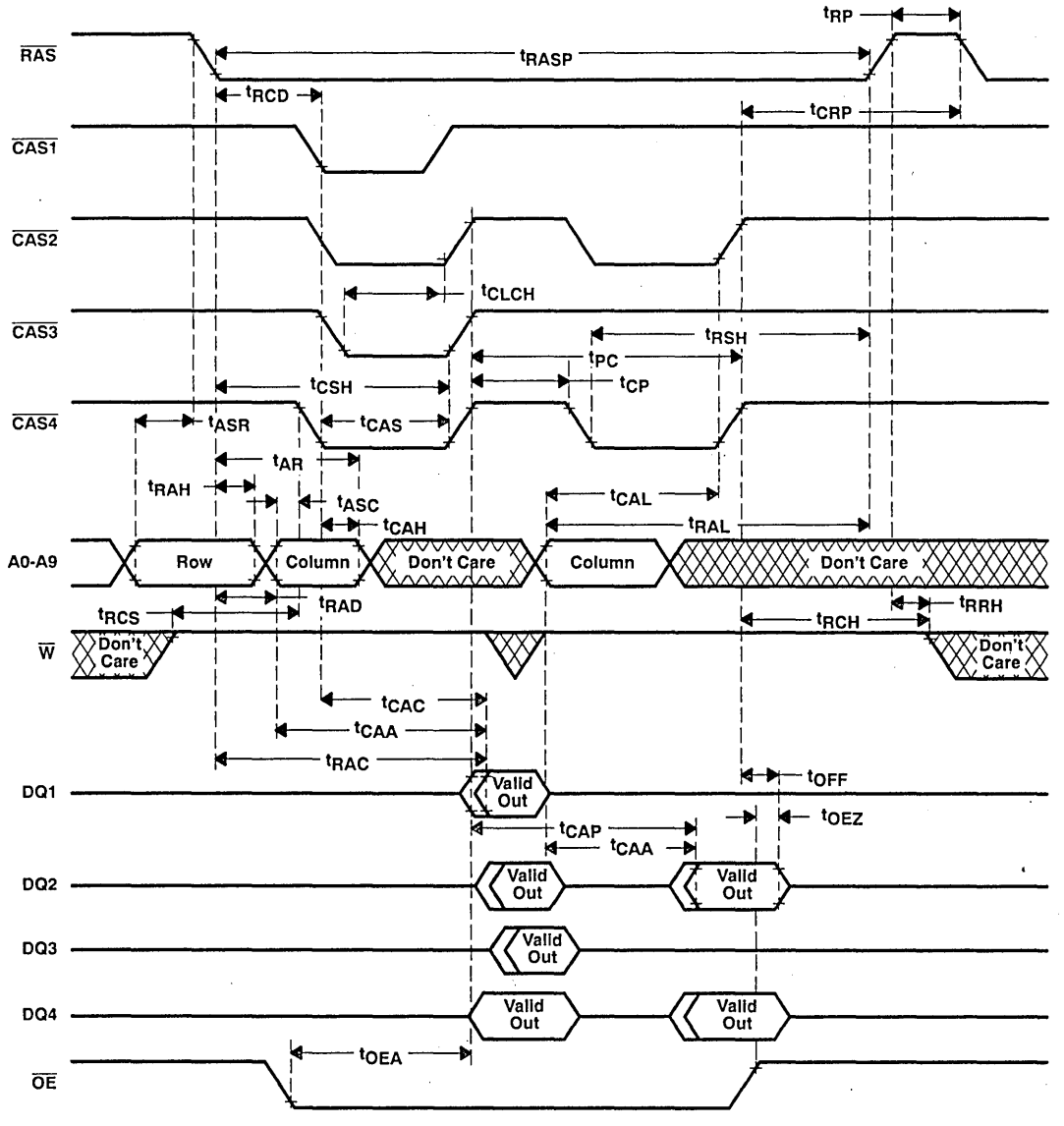
read-write/read-modify-write cycle



NOTES: 17. In order to hold the address latched by the first $\overline{CAS}x$ going low, the parameter t_{CLCH} must be met.
18. t_{CAC} is measured from $\overline{CAS}x$ to its corresponding DQx.
19. $\overline{CAS}x$ order is arbitrary.

ADVANCE INFORMATION

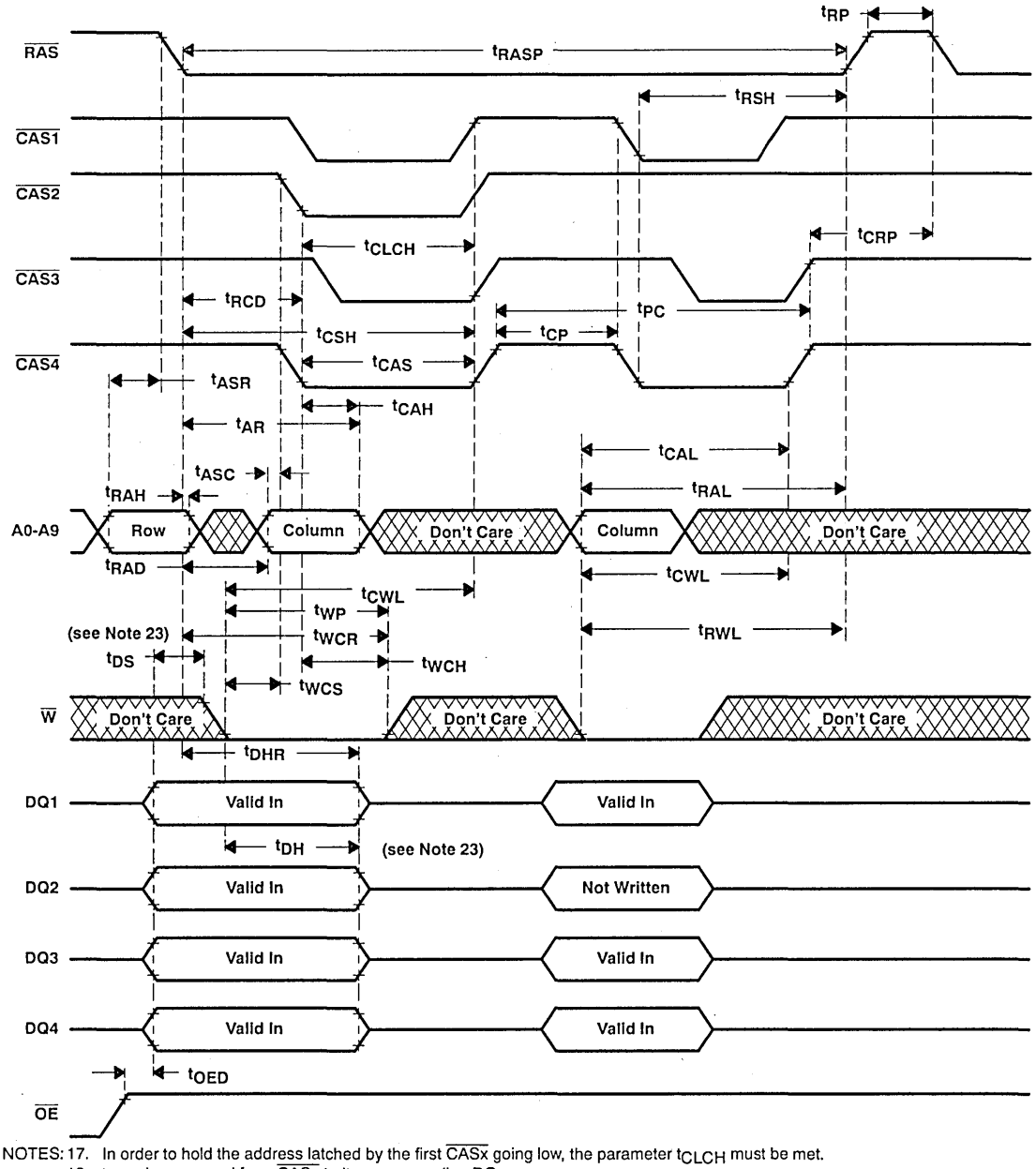
enhanced page-mode read cycle timing



NOTES: 17. In order to hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
18. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
19. $\overline{CASx}$ order is arbitrary.
20. Output may go from high-impedance to an invalid data state prior to the specified access time.
21. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
22. Access time is t_{CAP} or t_{CAA} dependent.

ADVANCE INFORMATION

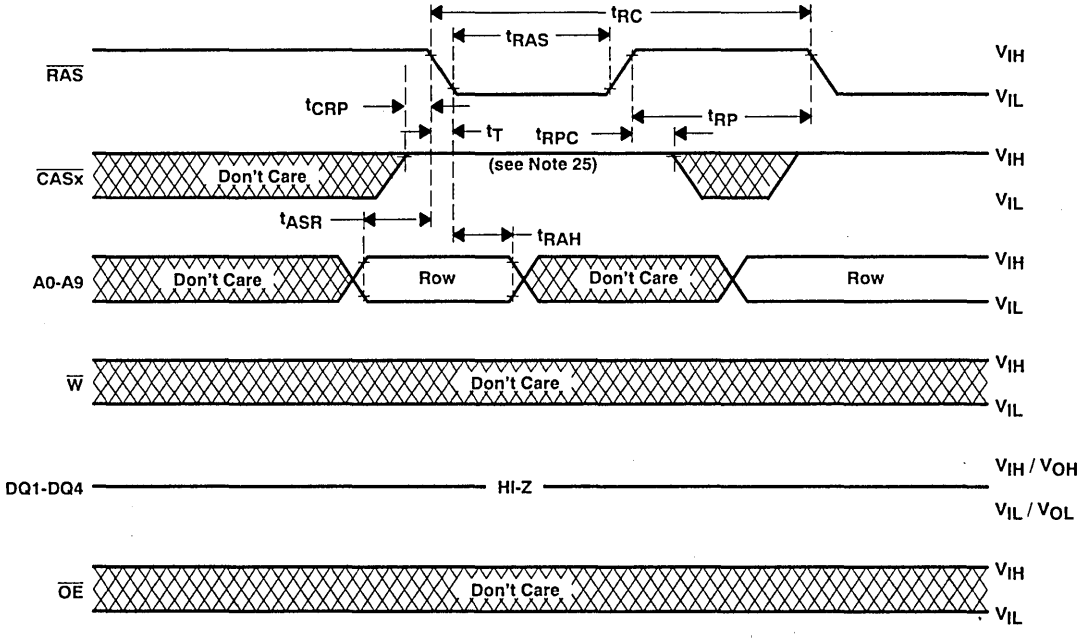
enhanced page-mode write cycle timing



NOTES: 17. In order to hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
18. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
19. $\overline{CASx}$ order is arbitrary.
21. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
23. Referenced to $\overline{CASx}$ or $\overline{W}$, whichever occurs last.

ADVANCE INFORMATION

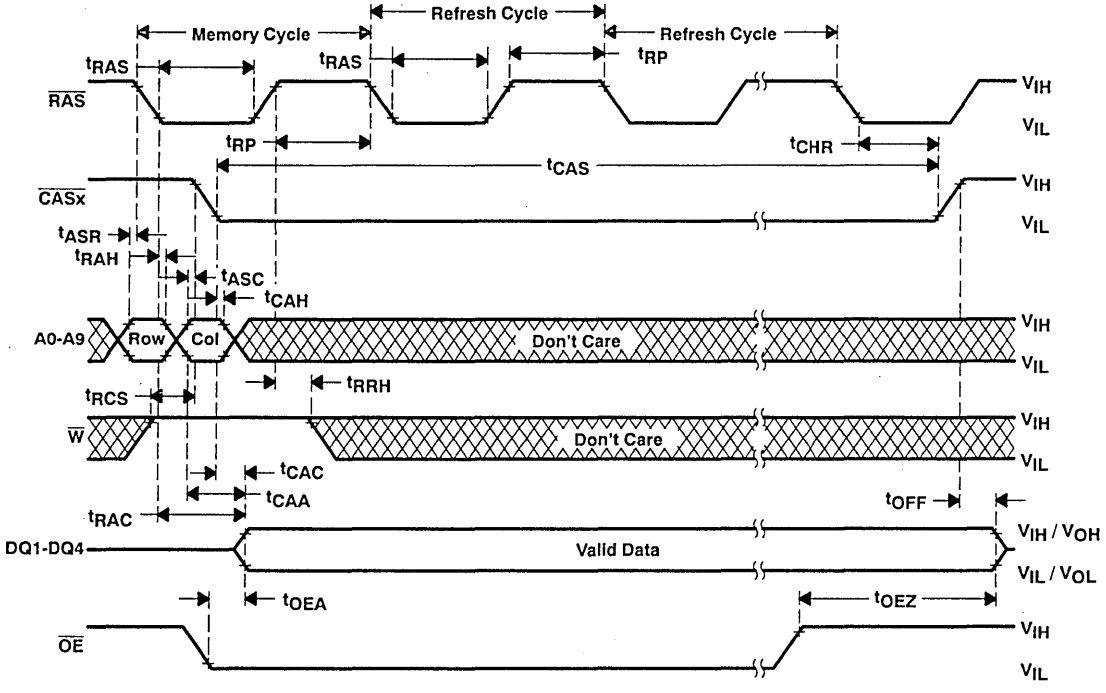
$\overline{RAS}$-only refresh timing



NOTE 24: All $\overline{CAS}$x must be high.

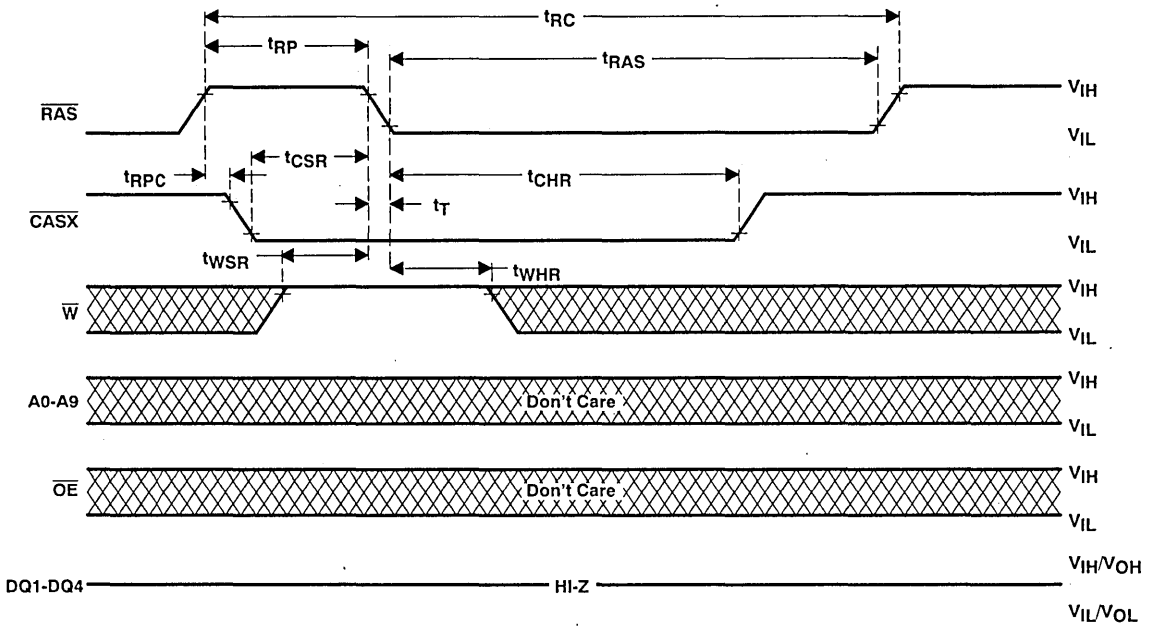
ADVANCE INFORMATION

hidden refresh cycle



ADVANCE INFORMATION

automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



NOTE 25: Any $\overline{CASx}$ may be used.

ADVANCE INFORMATION

This section contains data sheets of Military MOS Memory devices. In conformance with MIL-STD-883, all parameters listed on the appropriate data sheet are tested if a min or max limit is specified unless there are exceptions listed in the Military Products Baseline and Errata to Data Books. The errata book should be referenced for a complete errata status of all data sheets. Errata will include actual parametric limit changes, notations that indicate that a parameter is not production tested, parametric test condition changes, and clarifying notes. The Military Products Baseline and Errata to Data Books is published twice a year (2Q and 4Q) with updates published on a monthly basis. If you desire to be added to the mailing list for this publication contact:

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(915) 561-7142

Process Flows

Several process flows are available for devices manufactured by Texas Instruments Military Products. They include Class B and Class S screened devices that conform to MIL-STD-883 Method 5004, as well as special flows such as the Lockheed Monitored Line (Space Level) and the DESC Standard Military Drawing (SMD). These and other process flows are described in the *Military Products Designer's Reference Guide*, literature number SGYZ001C. The flows are typical and may vary depending on changes to applicable military standards, such as MIL-M-38510 or MIL-STD-883. Contact the factory for the processing levels available by device.

PROCESS FLOWS	DESCRIPTION
JAN S	QPL products processed to MIL-M-38510 Level S for space-level applications.
LMSC	Products processed on the Lockheed Monitored Line A program developed by the Air Force for space-level applications.
SEQ	Non-JAN products processed to Level S to negotiated electrical specifications for space-level applications.
JAN B	QPL products processed to MIL-M-8510 Level B for military applications.
DESC/SMD	Standard Military Drawing products processed to Level B with Table 1 Electricals controlled by DESC.
SNJ/SMJ	Products processed to MIL-STD-883.
SN/SM	Products processed per test flow defined in reference document.‡
SMX†/SNX	Products assembled and tested by Military Products prior to production release. No minimum screening or testing required.
SMP/SNP	Devices representative of production material with military temperature range testing. Shipped without generic coverage.

† SMX devices are experimental or have not been fully characterized and specifications are preliminary and subject to change. Notwithstanding any provisions to the contrary. TI makes no warranty, either expressed, implied or statutory (including any implied warranty of merchantability or fitness for a specific purpose) as to devices or that a final production version will be sold.

‡ Refer to *Military Products Designer's Reference Guide*, SGYZ001C.

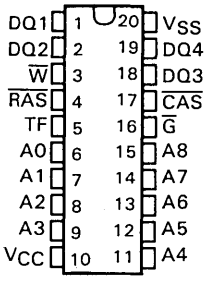
MAY 1989—REVISED FEBRUARY 1990

- 262,144 × 4 Organization
- Single 5-V Supply (10% Tolerance)
- Performances Ranges:

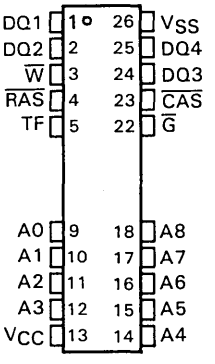
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
SMJ44C256-10	100 ns	25 ns	45 ns	190 ns
SMJ44C256-12	120 ns	30 ns	55 ns	220 ns
SMJ44C256-15	150 ns	40 ns	70 ns	260 ns

- Enhanced Page Mode Operation with $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
- Long Refresh Period . . . 512-Cycle Refresh in 8 ms (Max)
- 3-State Unlatched Output
- Lower Power Dissipation
- Texas Instruments EPIC™ CMOS Process
- All Input and Clocks Are TTL-Compatible
- −55°C to 125°C Operating Temperature Range
- Packaging Offered:
  - 20-Pin 300-Mil Ceramic DIP (JD Suffix)
  - 20-Lead Ceramic Surface Mount Package (HJ Suffix)
  - 20-Terminal Low-Profile Leadless Ceramic Surface Mount Package (HL Suffix)
  - 20-Terminal Leadless Ceramic Surface Mount Package (FQ Suffix)
- High Reliability MIL-STD-883C Processing

JD PACKAGE†
(TOP VIEW)



HJ, HL, AND FQ PACKAGES†
(TOP VIEW)



†The packages shown here are for pinout reference only.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Data-Output Enable
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The SMJ44C256 is a high-speed, 1,048,576-bit dynamic random-access memory organized as 262,144 words of four bits each. This device employs state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row-address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page-mode cycle time used. With minimum $\overline{CAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

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Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ44C256 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as "enhanced page-mode". Valid column address may be presented immediately after $t_{h(RA)}$ (row-address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low,) if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. The SMJ44C256 $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation with $\overline{G}$ grounded.

data in (DQ1-DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed or read-modify-write cycle, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatability (no pull-up resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{G}$ are brought low. In a read cycle the output becomes valid after the access timer interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying $t_{d(GHD)}$.

output enable ($\overline{G}$)

$\overline{G}$ controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{G}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every eight milliseconds to retain data. This can be achieved by strobing each of the 512 rows (A0-A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter $t_{d(CLRL)R}$] and holding it low after $\overline{RAS}$ falls [see parameter $t_{d(RLCH)R}$]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

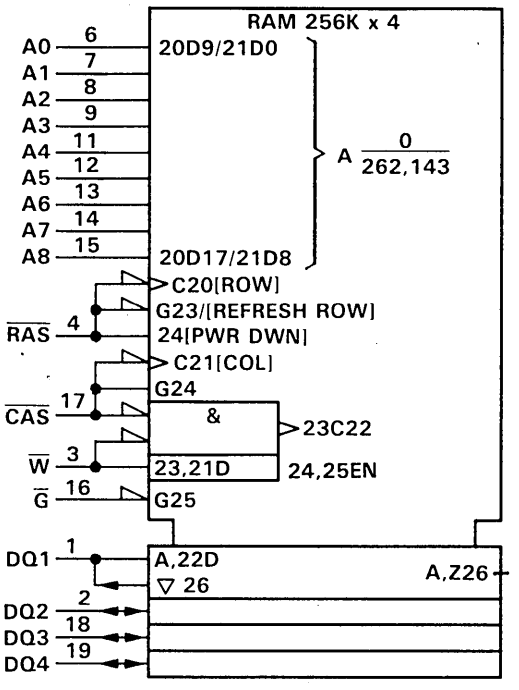
power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after power up to the full V_{CC} level.

test function pin

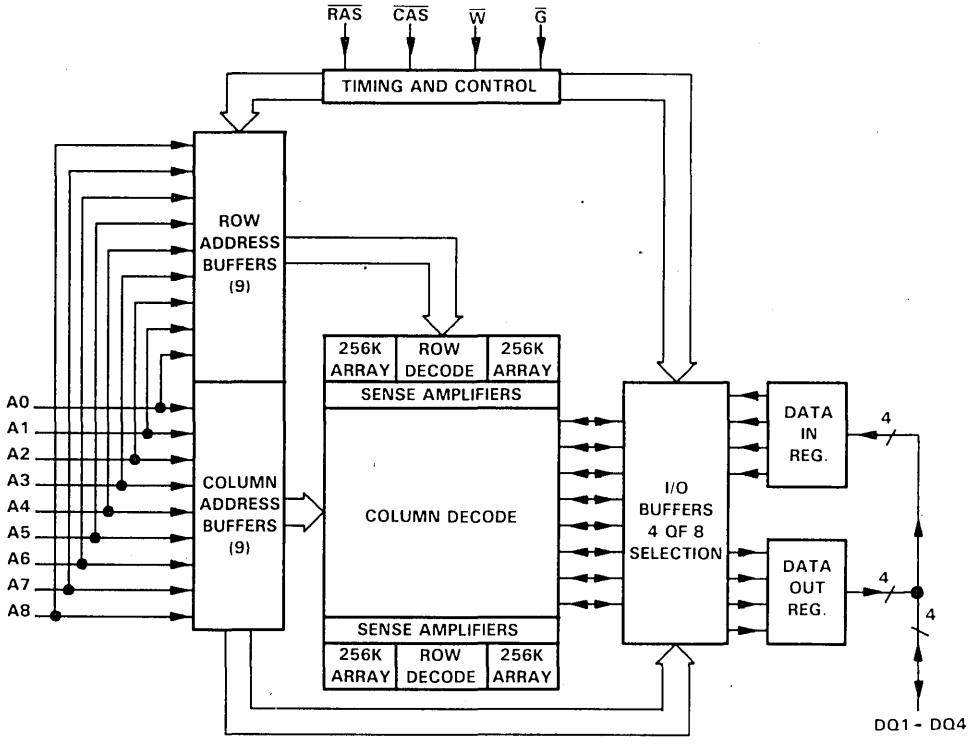
During normal device operation, the TF pin must be either disconnected or biased at a voltage less than or equal to V_{CC}.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JD package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1)	−1 V to 7 V
Voltage range on V_{CC}	0 V to 7 V
Short-circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		L VERSION			M VERSION			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{SS}	Supply voltage		0			0		V
V_{IH}	High-level input voltage	2.4		6.5	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.6	−1		0.6	V
T_A	Operating free-air temperature	0			−55			°C
T_C	Case temperature			70			125	°C

NOTE 2: The algebraic convention, where the negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ44C256-10		SMJ44C256-12		SMJ44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	μA
I_{CC1}	Read/write cycle current	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V		70		60		55	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		3		3		3	mA
I_{CC3}	Average refresh current	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high		65		55		50	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		45		35		30	mA

capacitance over recommended supply voltage range and operating temperature range, f = 1 MHz, (see Note 3)

PARAMETER†		MIN	TYP‡	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		5	7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		6	8	pF
$C_{i(W)}$	Input capacitance, write-enable input		6	8	pF
C_o	Output capacitance		6	8	pF

NOTE 3: V_{CC} equal to 5.0 V ± 0.5 V and the bias on pins under test is 0.0 V.
†Capacitance is sampled only at initial design and after any major change.
‡All typical values are at T_C = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating temperature range (see Figure 1)

PARAMETER		ALT. SYMBOL	SMJ44C256-10		SMJ44C256-12		SMJ44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}		25		30		40	ns
$t_{a(CA)}$	Access time from column address	t_{CAA}		45		55		70	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low	t_{RAC}		100		120		150	ns
$t_{a(G)}$	Access time from $\overline{G}$ low	t_{GAC}		25		30		40	ns
$t_{a(CP)}$	Access time from column precharge	t_{CAP}		50		60		75	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)	t_{OFF}	0	25	0	30	0	35	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high (see Note 4)	t_{GOFF}	0	25	0	30	0	35	ns

NOTE 4: $t_{dis(CH)}$ and $t_{dis(G)}$ are specified when the output is no longer driven.

timing requirements over recommended supply voltage range and operating temperature range

		ALT. SYMBOL	SMJ44C256-10		SMJ44C256-12		SMJ44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	190		220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	190		220		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	270		305		355		ns
$t_{c(P)}$	Page-mode read or write cycle time (see Note 7)	t_{PC}	55		65		80		ns
$t_{c(PM)}$	Page-mode read-modify-write cycle time	t_{PCM}	135		150		175		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	25	10,000	30	10,000	40	10,000	ns
$t_{w(RH)}$	Pulse duration $\overline{RAS}$ high (precharge)	t_{RP}	80		90		100		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	100	10,000	120	10,000	150	10,000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RASP}	100	100,000	120	100,000	150	100,000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		20		25		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	5		5		5		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ low (see Note 10)	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	25		30		40		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	25		30		40		ns
$t_{h(CA)}$	Column-address hold time after $\overline{CAS}$ low (see Note 10)	t_{CAH}	20		20		25		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	70		80		100		ns
$t_{h(D)}$	Data hold time after $\overline{CAS}$ low (see Note 10)	t_{DH}	20		25		30		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	70		85		110		ns

Continued next page.

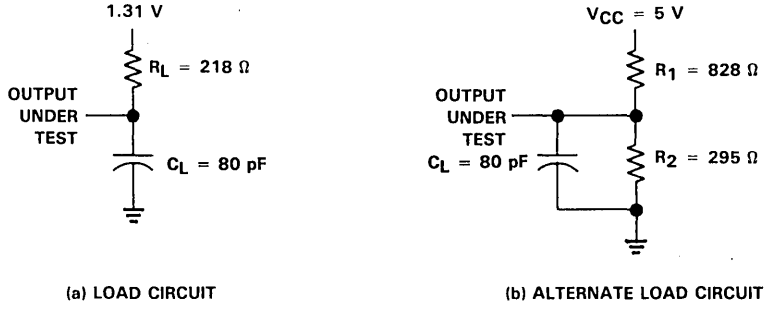
NOTES:
5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume $t_t = 5$ ns.
7. $t_{c(P)} > t_{w(CH)}$ min + $t_{w(CL)}$ min + 2 t_t.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.

timing requirements over recommended supply voltage range and operating temperature range (concluded)

		ALT. SYMBOL	SMJ44C256-10		SMJ44C256-12		SMJ44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 14)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 14)	t_{RRH}	10		10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	20		25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 12)	t_{WCR}	75		90		105		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		40		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 15)	t_{CWD}	70		80		90		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 13)	t_{RCD}	30	75	30	90	30	110	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address (see Note 13)	t_{RAD}	20	55	20	65	25	80	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	45		55		70		ns
$t_{d(CACH)}$	Delay time, column address to $\overline{CAS}$ high	t_{CAL}	45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 15)	t_{RWD}	150		170		200		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 15)	t_{AWD}	95		105		120		ns
$t_{d(GHD)}$	Delay time, $\overline{G}$ high before data at DQ	t_{GDD}	25		30		40		ns
$t_{d(GLRH)}$	Delay time, $\overline{G}$ low to $\overline{RAS}$ high	t_{GSR}	25		30		40		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		15		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms

NOTES: 11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Maximum value specified only to guarantee access time.
14. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
15. Read-modify-write operation only.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
17. System transition times (rise and fall) are to be a minimum of 3 ns and a maximum of 50 ns.

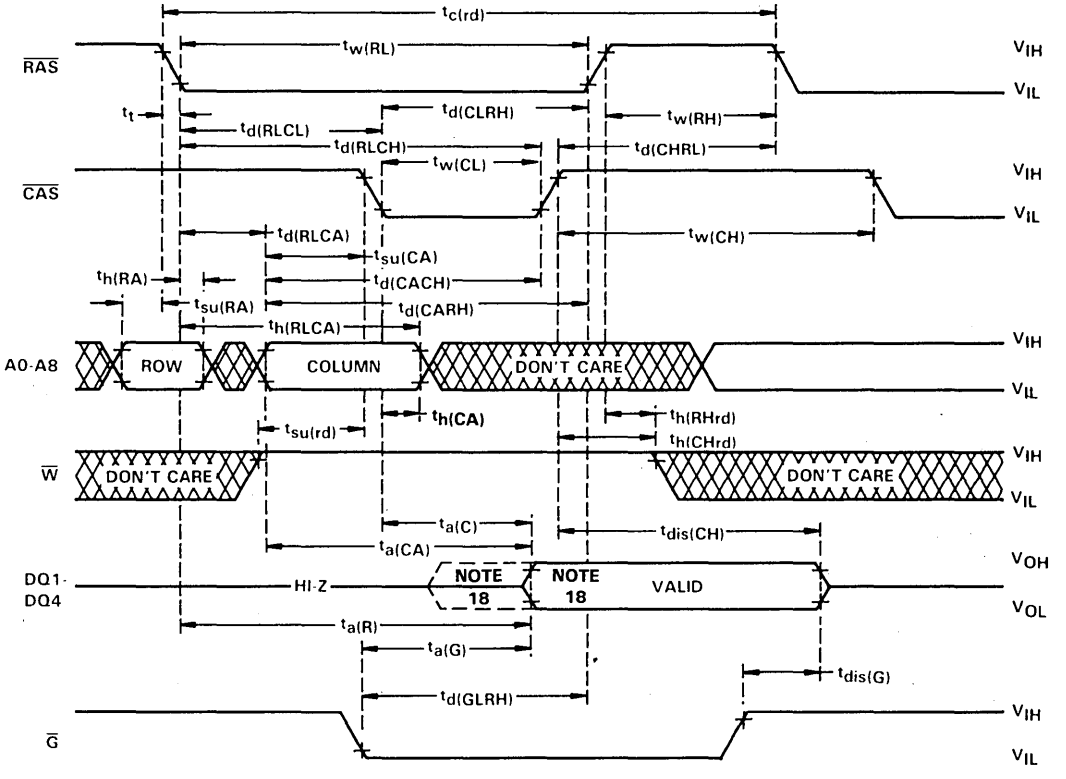
PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT (b) ALTERNATE LOAD CIRCUIT

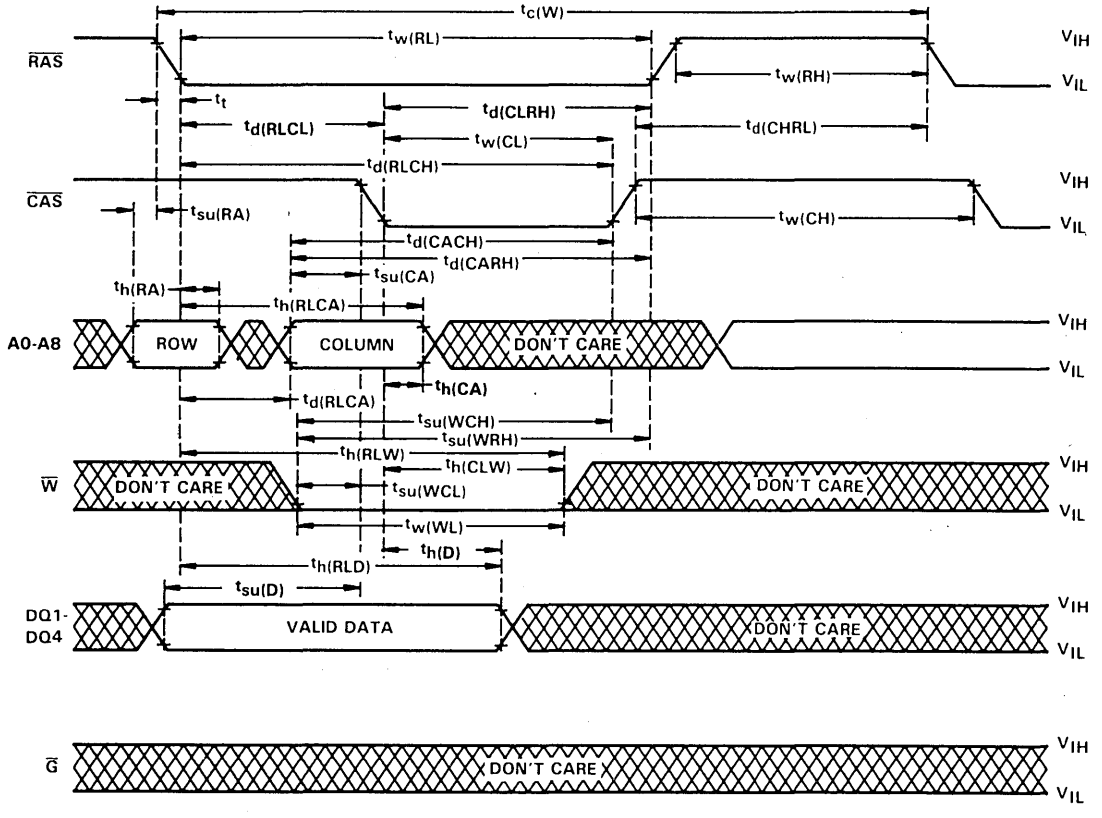
FIGURE 1. LOAD CIRCUITS FOR TIMING PARAMETERS

read cycle timing

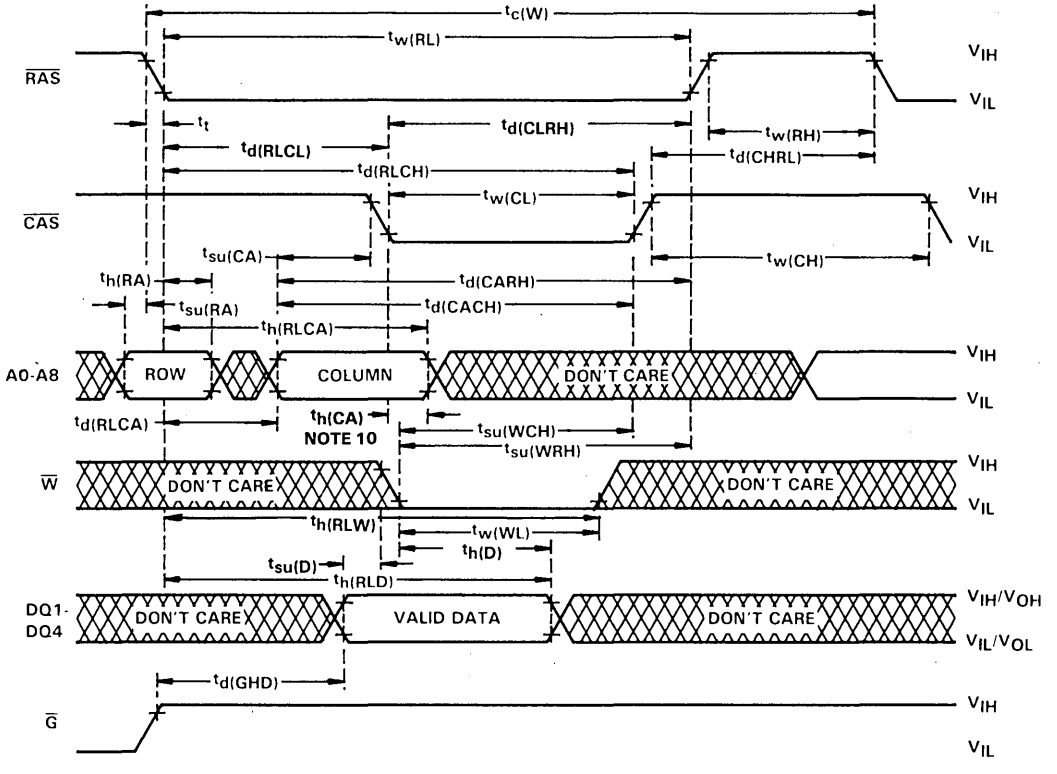


NOTE 18: Output may go from high impedance to an invalid data state prior to the specified access time.

early write cycle timing

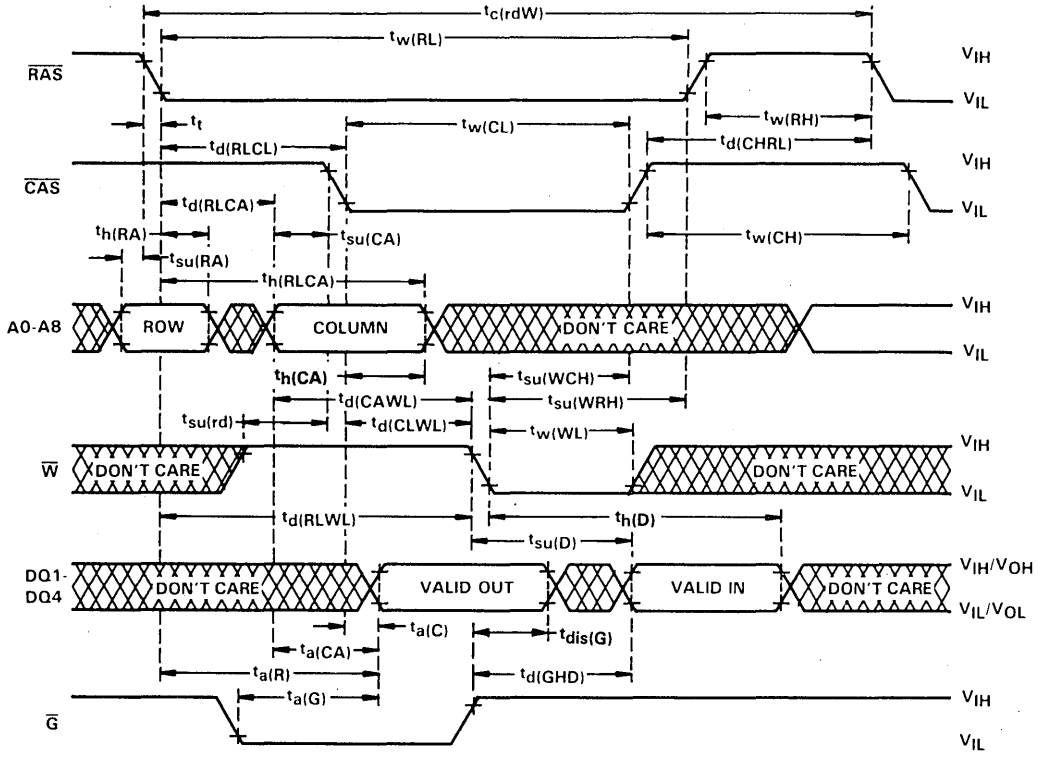


write cycle timing

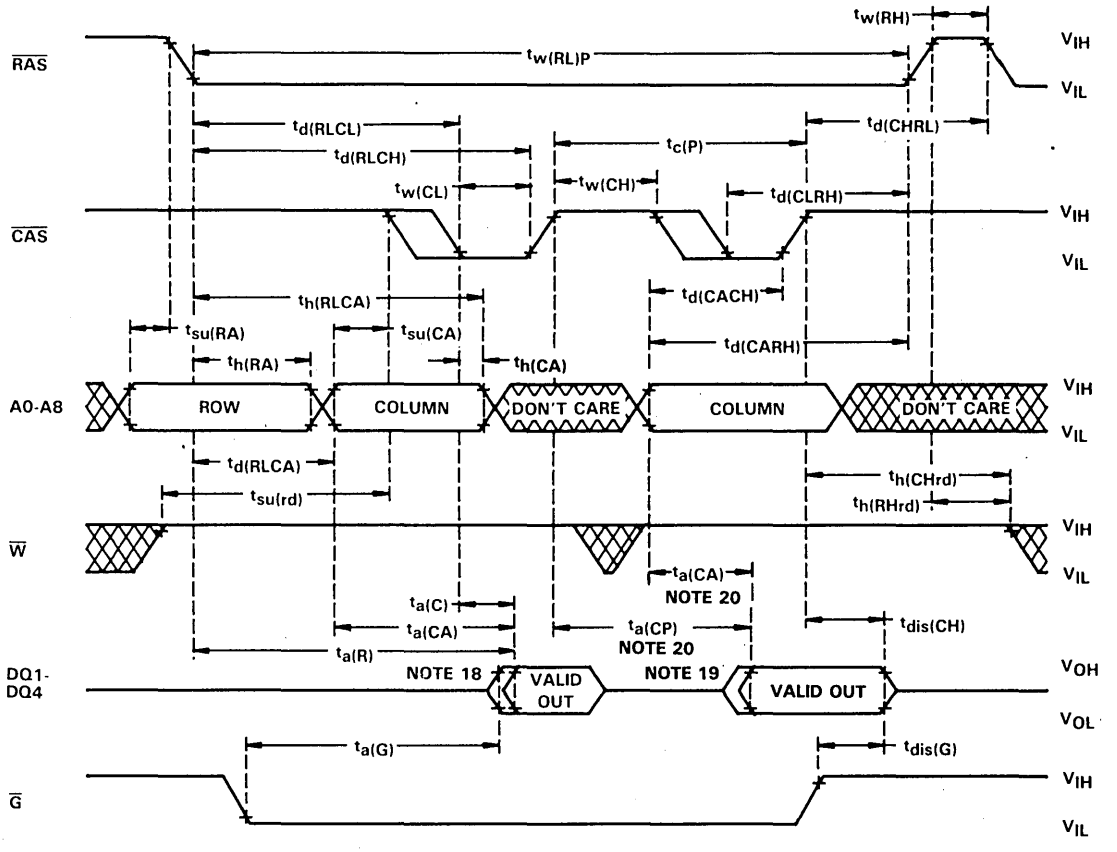


NOTE 10: Later of $\overline{CAS}$ or $\overline{W}$ in write operation.

read-write/read-modify-write cycle timing

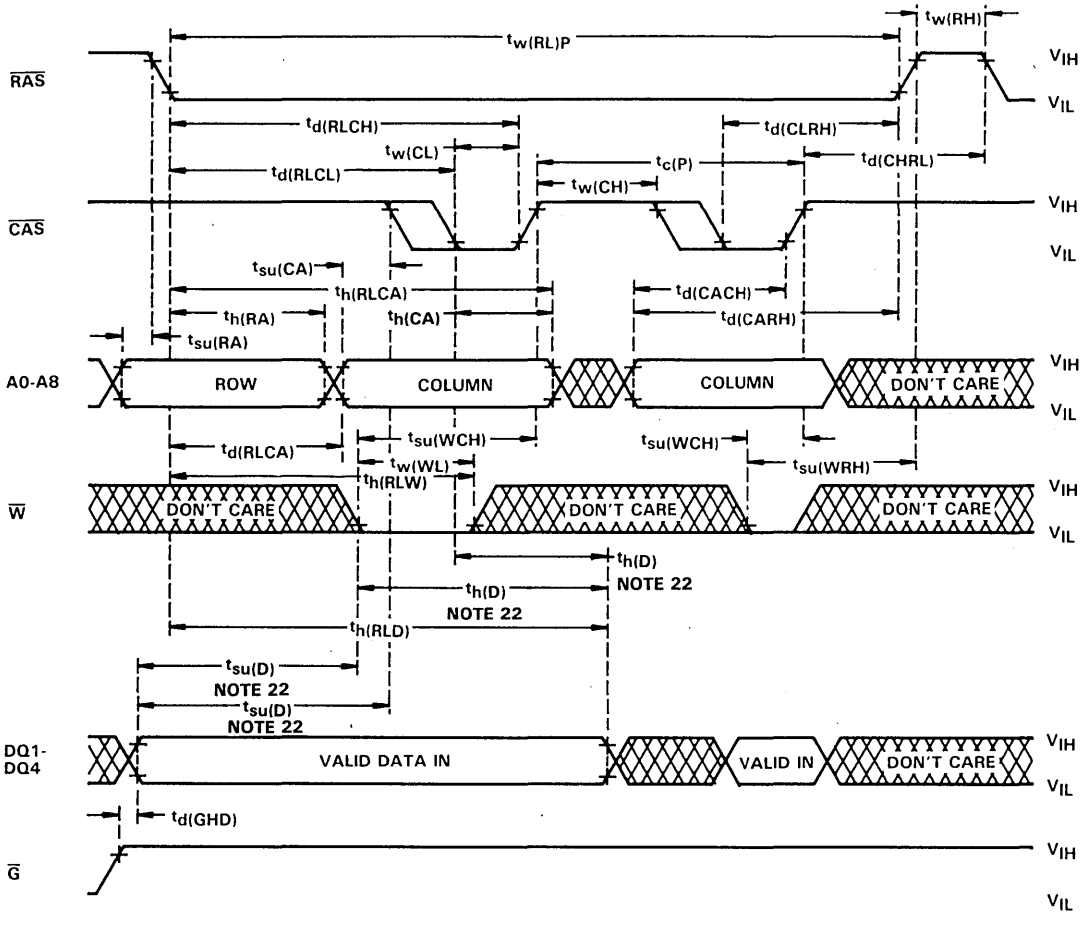


enhanced page-mode read cycle timing



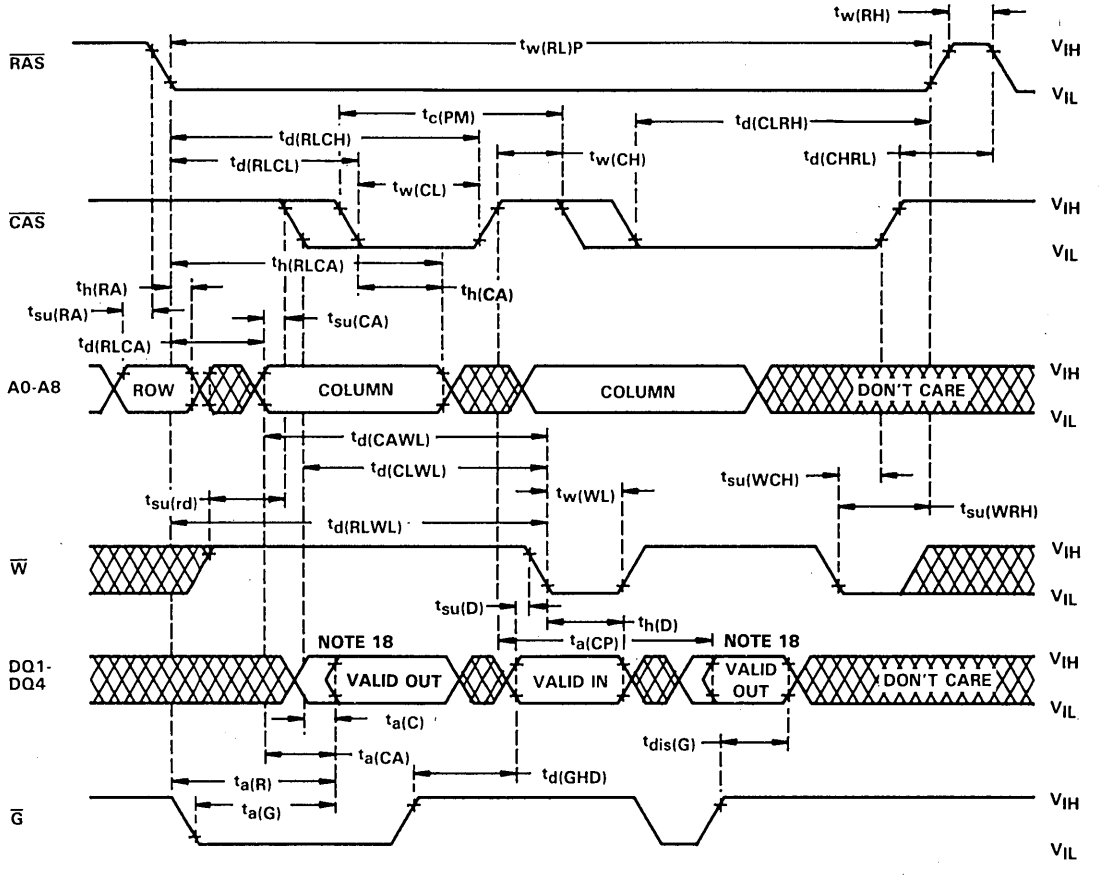
NOTES: 18. Output may go from high impedance to an invalid data state prior to the specified access time.
19. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
20. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

enhanced page-mode write cycle timing



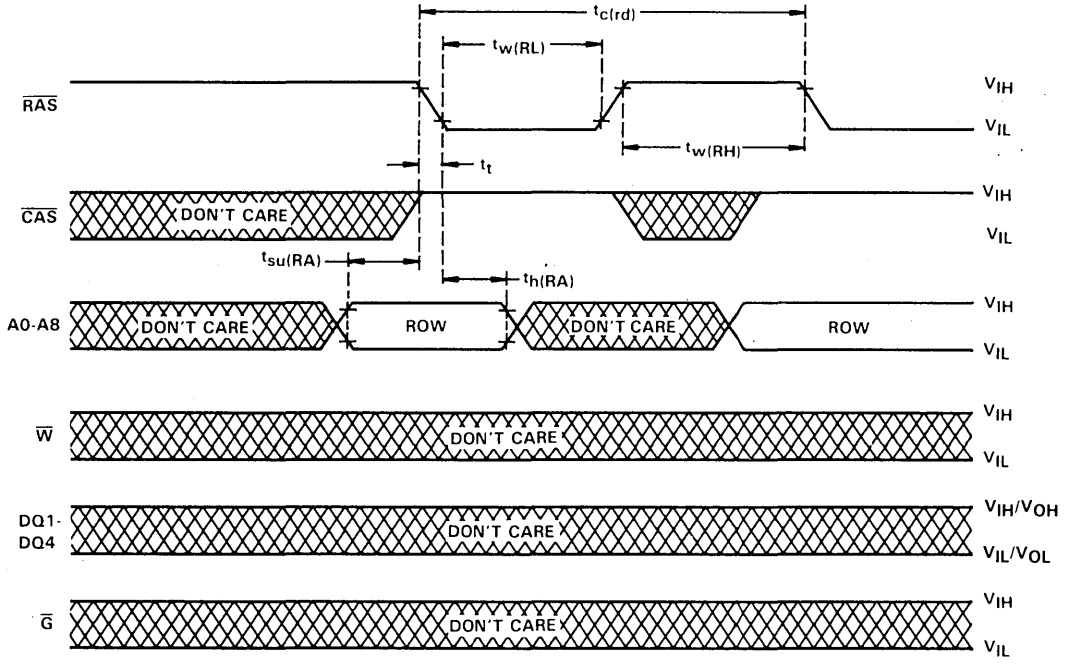
NOTES: 21. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.
22. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

enhanced page-mode read-modify-write cycle timing

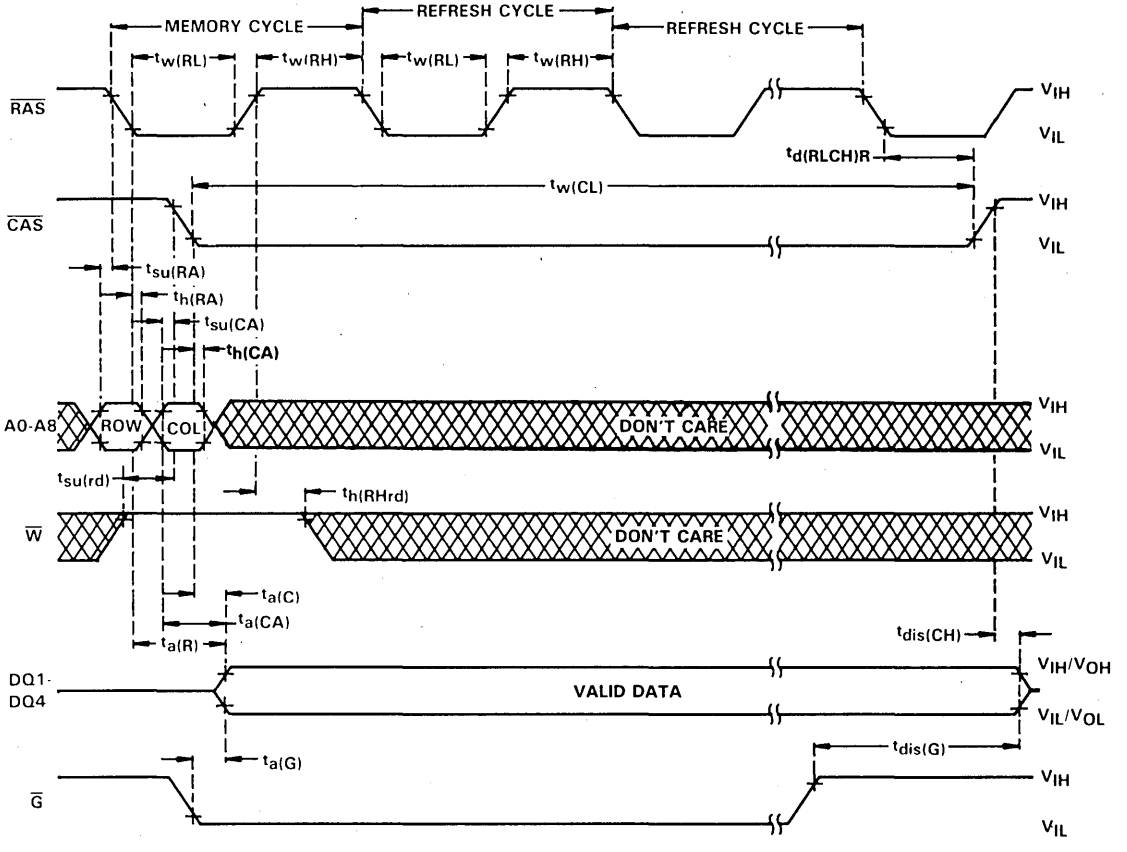


NOTES: 18. Output may go from high impedance to an invalid data state prior to the specified access time.
23. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.

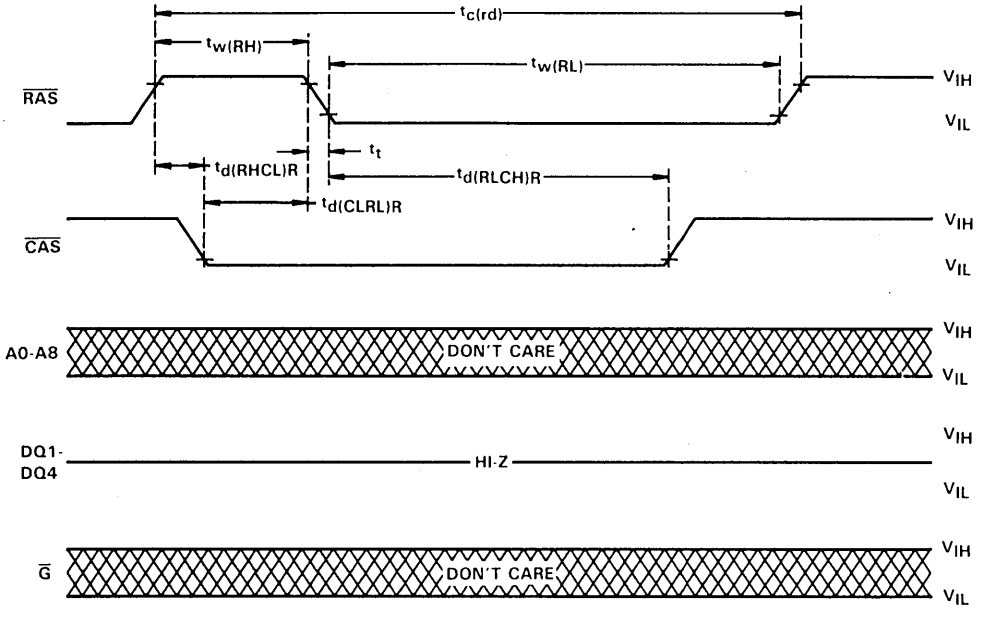
$\overline{\text{RAS}}$-only refresh timing



hidden refresh cycle (enhanced page mode)



automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



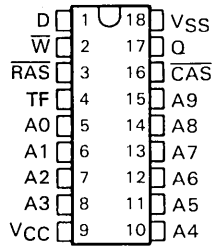
DECEMBER 1988 – REVISED DECEMBER 1989

- 1,048,576 × 1 Organization
- Single 5-V Supply (10% Tolerance)
- −55°C to 125°C Operating Temperature Range
- Performance Ranges:

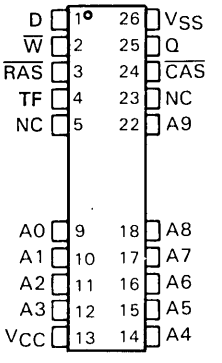
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
SMJ4C1024-10	100 ns	25 ns	45 ns	190 ns
SMJ4C1024-12	120 ns	30 ns	55 ns	220 ns
SMJ4C1024-15	150 ns	40 ns	70 ns	260 ns

- SMJ4C1024—Enhanced Page Mode Operation for Faster Memory Access
  - Higher Data Bandwidth than Conventional Page-Mode Parts
  - Random Single-Bit Access Within a Row with a Column Address
- One of TI's CMOS Megabit DRAM Family Including: SMJ44C256—256K × 4 Enhanced Page Mode
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
- Long Refresh Period . . . 512-Cycle Refresh in 8 ms (Max)
- 3-State Unlatched Output
- Low Power Dissipation
- Texas Instruments EPIC™ CMOS Process
- All Inputs and Clocks Are TTL Compatible
- Packaging Offered:
  - 18-Pin 300-Mil Ceramic DIP
  - 20-Lead Ceramic Surface Mount Package (HJ Suffix)
  - 20-Terminal Leadless Ceramic Surface Mount Package (FQ Suffix)
  - 20-Lead Flat Pack (HK Suffix)
- High-Reliability Class B Processing

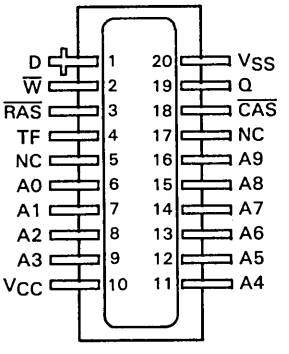
JD PACKAGE
(TOP VIEW)



HJ AND FQ PACKAGES†
(TOP VIEW)



HK PACKAGE
(TOP VIEW)



†The packages shown here are for pinout reference only. The HJ and FQ packages are actually 75% of the length of the JD package.

PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS}$	Column-Addrss Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The SMJ4C1024 is a high-speed, 1,048,576-bit dynamic random-access memory organized as 1,048,576 words of one bit each. It employs state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 100 ns, 120 ns, and 150 ns. Maximum power dissipation is as low as 385 mW operating and 16.5 mW standby on 100 ns devices.

EPIC is a trademark of Texas Instruments Incorporated.

The EPIC™ technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 140 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ4C1024 is offered in 18-pin ceramic dual-in-line (JD suffix) and 20-terminal ceramic leadless carrier, 20-pin leaded carrier, and 20-pin flatpack. They are guaranteed for operation from −55°C to 125°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ4C1024 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as "enhanced page mode." Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$.)

address (A0 through A9)

Twenty address bits are required to decode 1 of 1,048,576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every eight milliseconds to retain data. This can be achieved by strobing each of the 512 rows (A0-A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

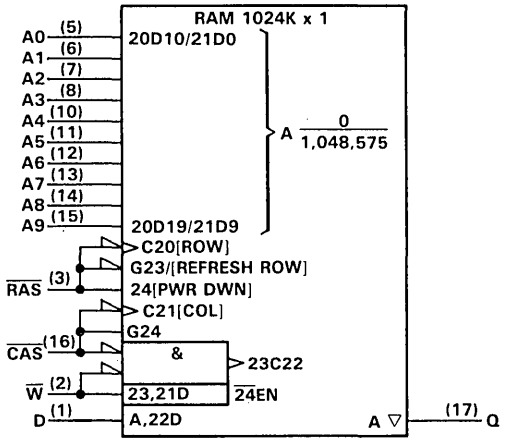
$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter $t_{d(CLRL)R}$] and holding it low after $\overline{RAS}$ falls [see parameter $t_{d(RLCH)R}$]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh cycles.

power up

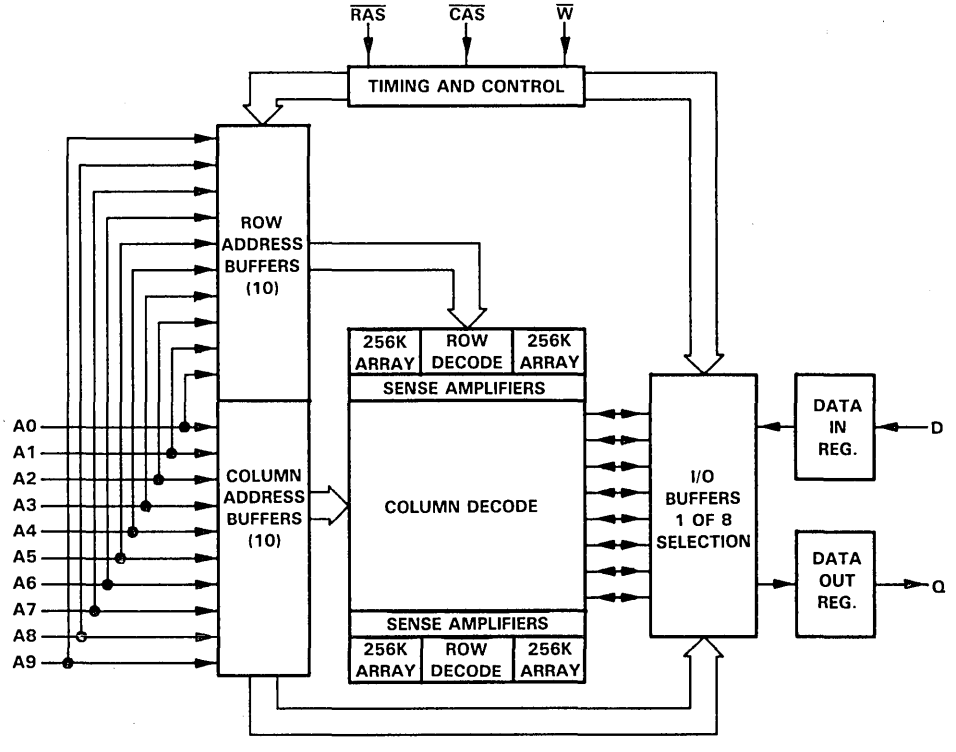
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 18-pin dual-in-line package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin . . . . . −1 V to 7 V
Voltage range on V_{CC} . . . . . −1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device relaibility.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Minimum operating free-air temperature	−55			°C
T_C	Maximum operating case temperature			125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4C1024-10		SMJ4C1024-12		SMJ4C1024-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{CC} = 5 V, All other input pins = 0 V to V_{CC}		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	μA
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.5 V		70		60		55	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		3		3		3	mA
I_{CC3}	Average refresh current	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high		65		55		50	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		45		35		30	mA

capacitance over recommended supply range and operating temperature range, f = 1 MHz (see Note 3)

PARAMETER†		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			6	pF
$C_{i(D)}$	Input capacitance, data input			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			8	pF
C_o	Output capacitance			7	pF

†Capacitance is sampled only at initial design and after any major change.
NOTE 3: V_{CC} equal to 5.0 V ± 0.5 V and the bias on the pins under test is 0.0 V

switching characteristics over recommended supply voltage range and operating temperature range (see Figure 1)

PARAMETER		ALT. SYMBOL	SMJ4C1024-10		SMJ4C1024-12		SMJ4C1024-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}		25		30		40	ns
$t_{a(CA)}$	Access time from column address	t_{CAA}		45		55		70	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low	t_{RAC}		100		120		150	ns
$t_{a(CP)}$	Access time from column precharge	t_{CAP}		50		60		75	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)	t_{OFF}	0	25	0	30	0	35	ns

NOTE 4: $t_{dis(CH)}$ is specified when the output is no longer driven.

timing requirements over recommended supply voltage range and operating temperature range

PARAMETER		ALT. SYMBOL	SMJ4C1024-10		SMJ4C1024-12		SMJ4C1024-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	190		220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	190		220		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	220		265		315		ns
$t_{c(P)}$	Page-mode read or write cycle time (see Note 7)	t_{PC}	55		65		80		ns
$t_{c(PM)}$	Page-mode read-modify-write cycle time	t_{PCM}	85		110		135		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	25	10,000	30	10,000	40	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	80		90		100		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	100	10,000	120	10,000	150	10,000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RASP}	100	100,000	120	100,000	150	100,000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		20		25		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	3		3		3		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time (see Note 10)	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	25		30		40		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	25		30		40		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		25		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	70		80		100		ns
$t_{h(D)}$	Data hold time (see Note 10)	t_{DH}	20		25		30		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	70		85		110		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 15)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 15)	t_{RRH}	10		10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	20		25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 12)	t_{WCR}	70		85		100		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		40		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 13)	t_{CWD}	25		40		50		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	28	75	28	90	33	110	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address (see Note 14)	t_{RAD}	20	55	20	65	25	80	ns

Continued next page.

NOTES:

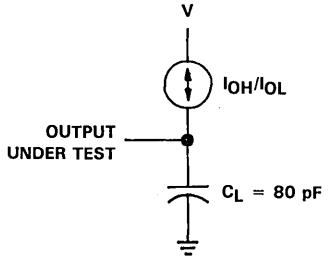
5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. To guarantee $t_{c(P)}$ min, $t_{a(CA)}$ must be observed.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed.
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed.
10. Before the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Read-modify-write operation only.
14. Maximum value specified only to guarantee access time.
15. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.

timing requirements over recommended supply voltage range and operating temperature range (concluded)

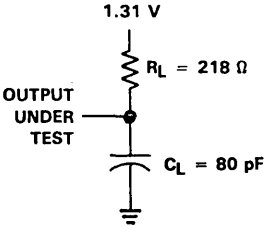
PARAMETER		ALT. SYMBOL	SMJ4C1024-10		SMJ4C1024-12		SMJ4C1024-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	45		55		70		ns
$t_{d(CACH)}$	Delay time, column address to $\overline{CAS}$ high	t_{CAL}	45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)	t_{RWD}	100		130		160		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 13)	t_{AWD}	45		65		80		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high, (see Note 16)	t_{CHR}	25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low, (see Note 16)	t_{CSR}	10		10		15		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms

NOTES: 13. Read-modify-write operation only.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
17. System transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 50 ns.

PARAMETER MEASUREMENT INFORMATION

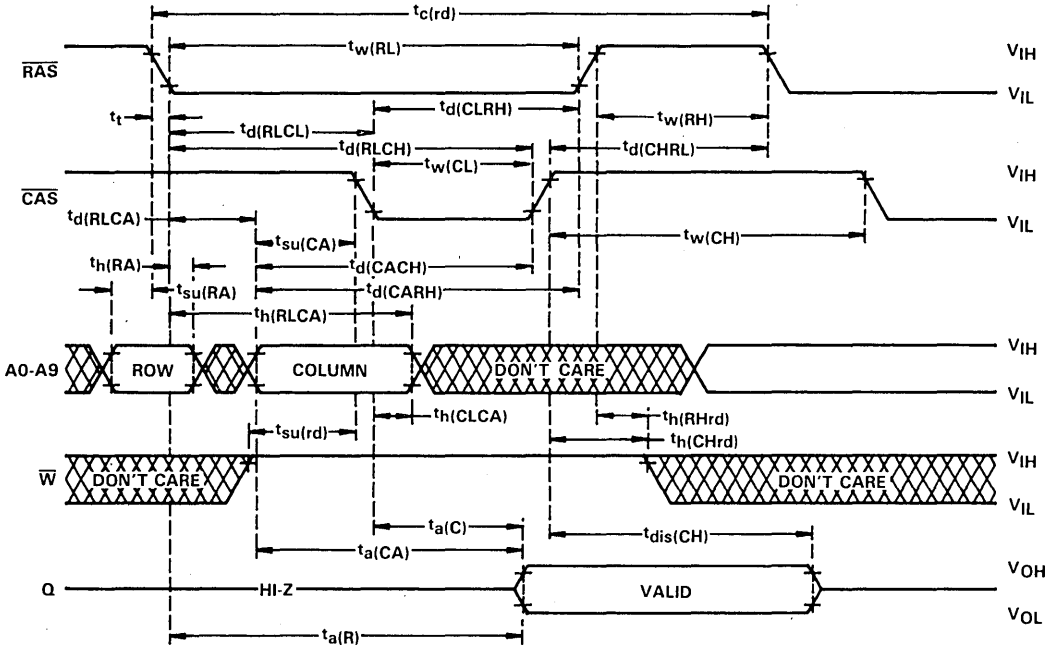


(a) LOAD CIRCUIT

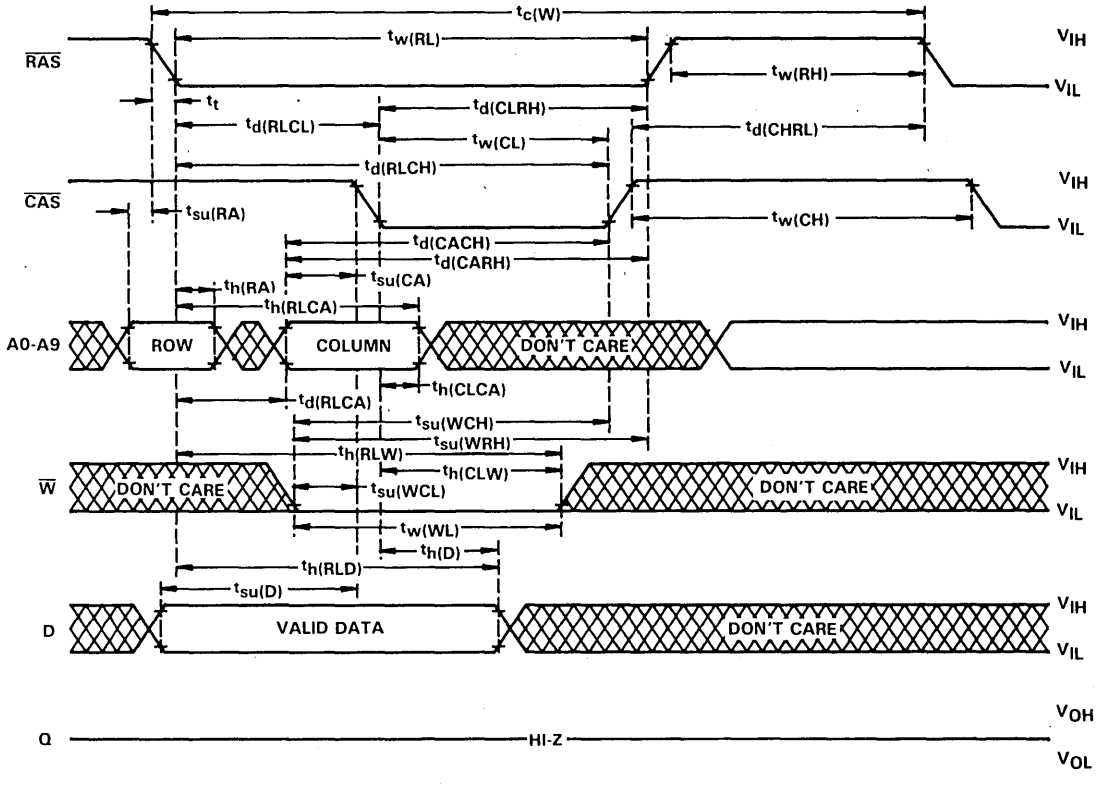


(b) ALTERNATE LOAD CIRCUIT

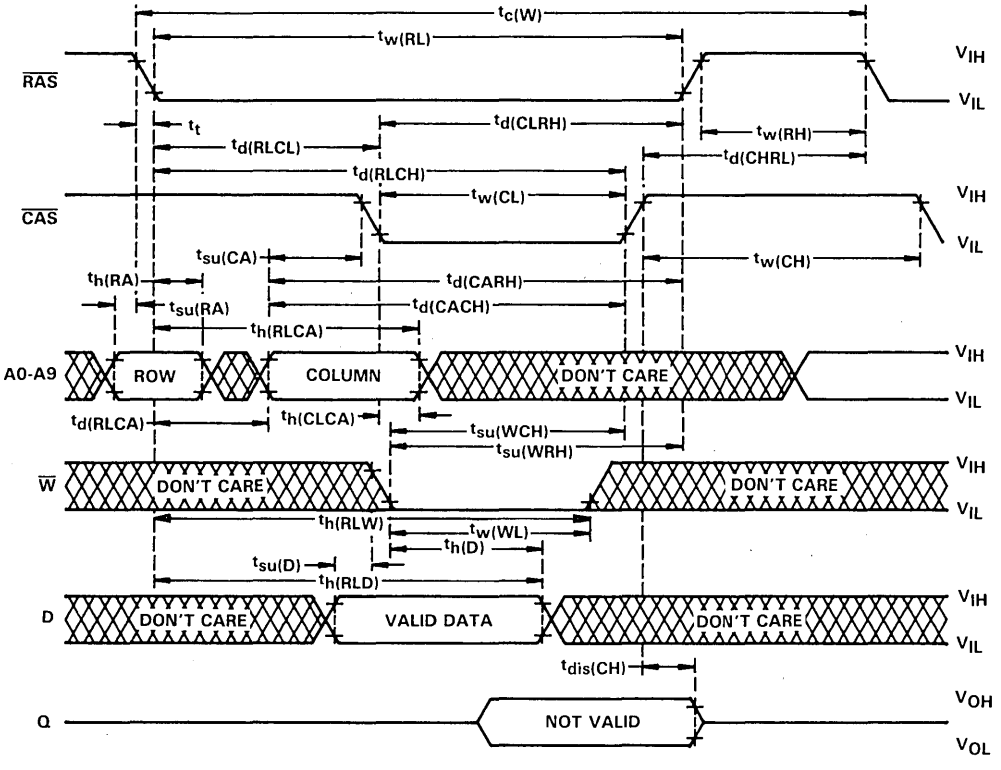
read cycle timing



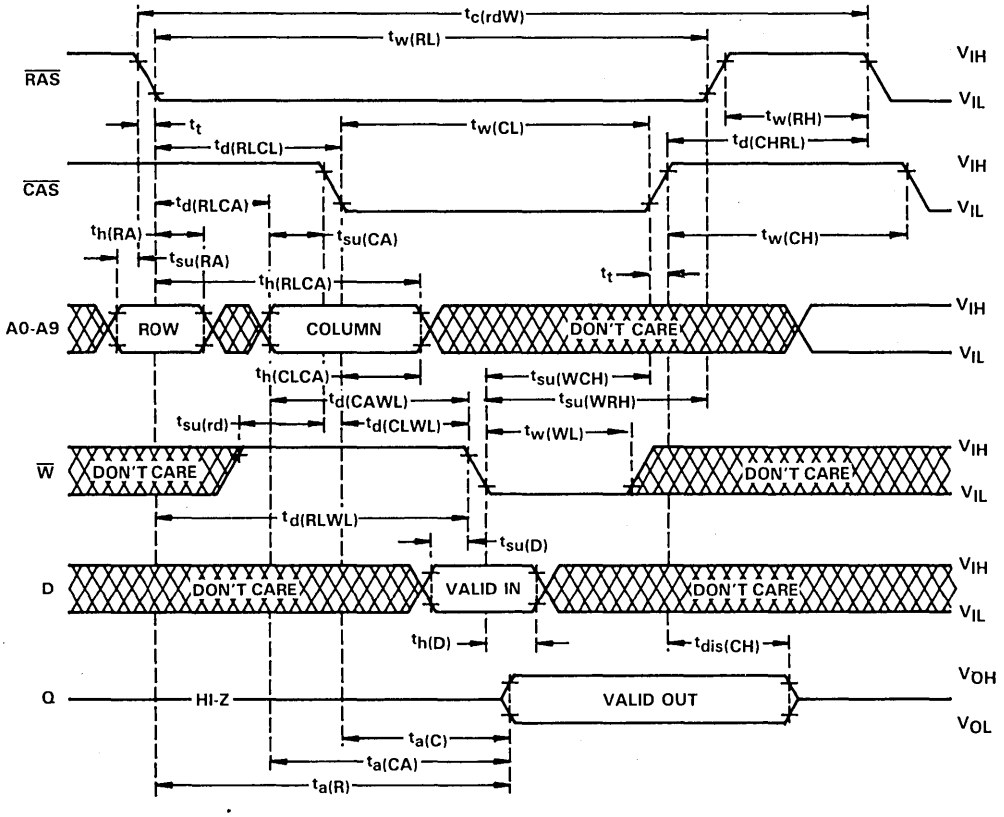
early write cycle timing



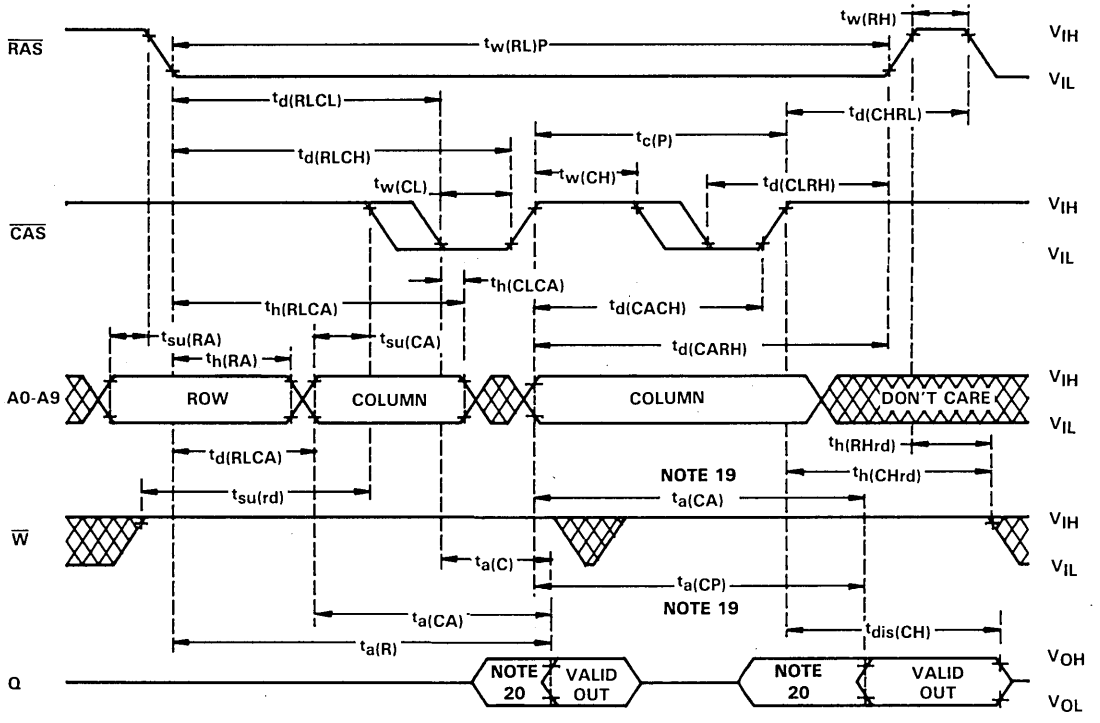
write cycle timing



read-write read-modify-write cycle timing

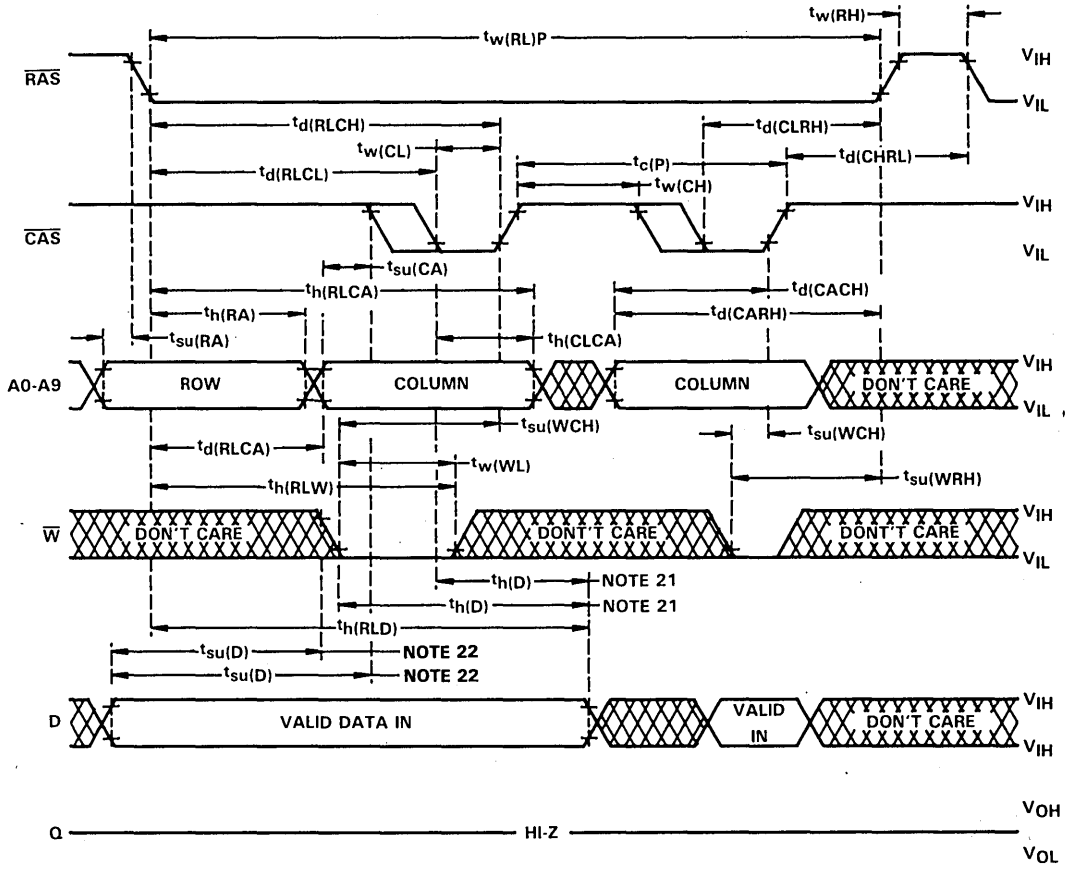


enhanced page-mode read cycle timing



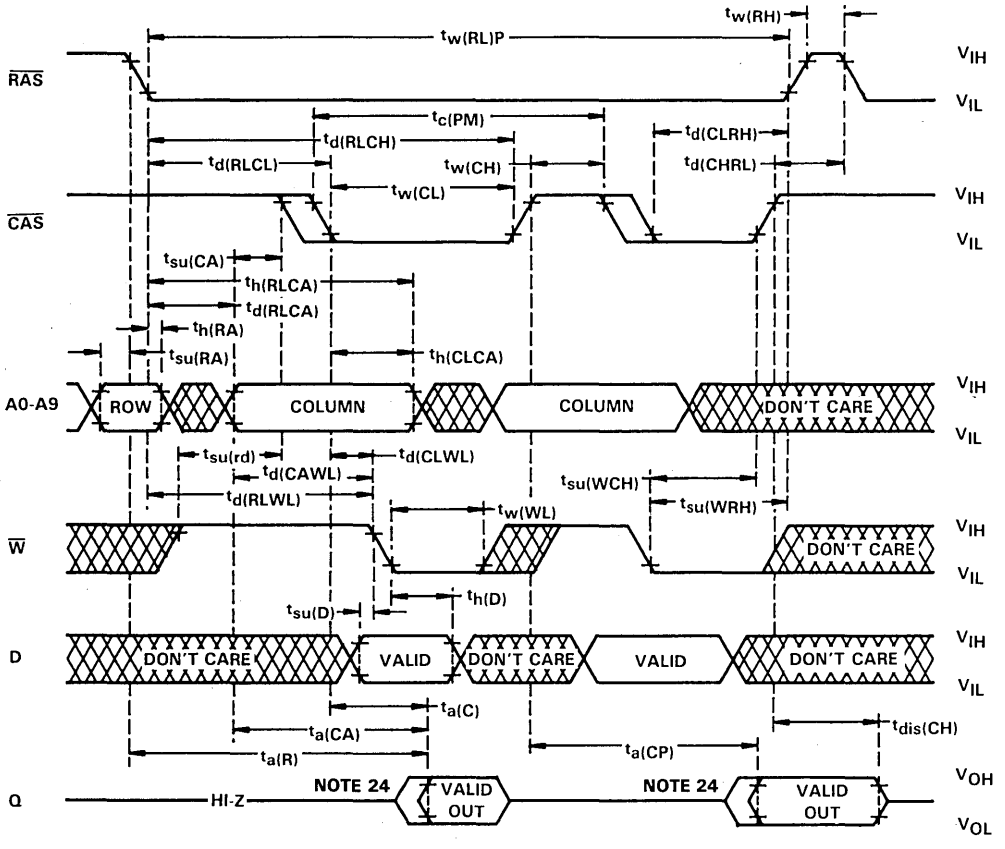
NOTES: 18. A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
19. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
20. Output may go from three-state to an invalid data state prior to the specified access time.

enhanced page-mode write cycle timing



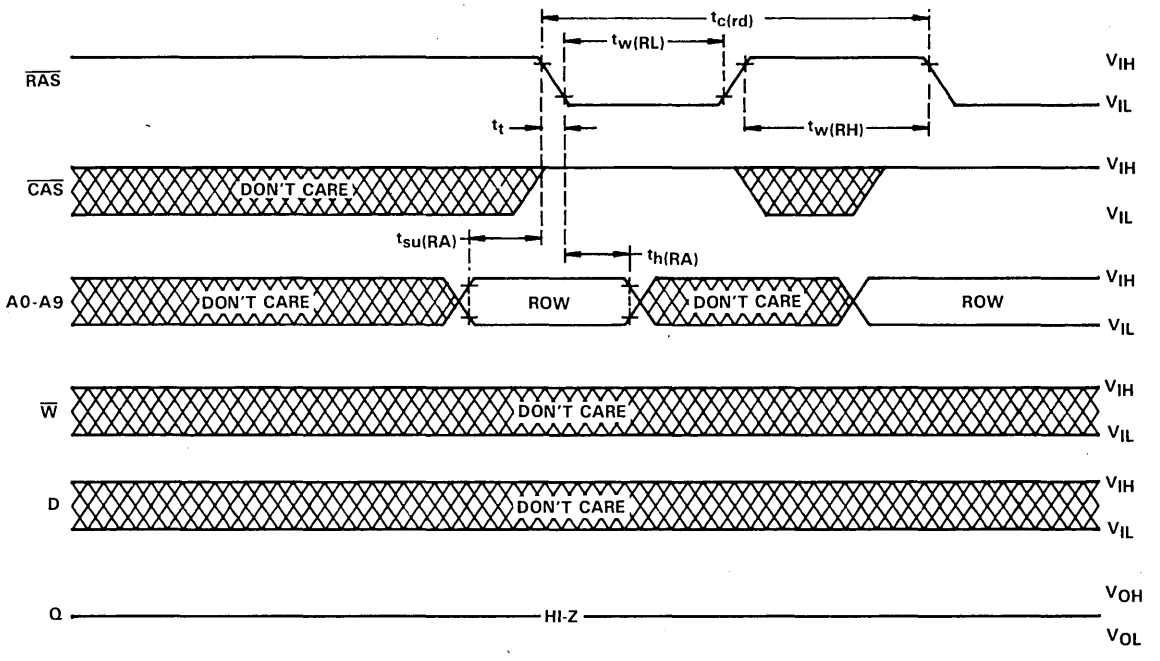
NOTES: 21. A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.
22. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

enhanced page-mode read-modify-write cycle timing

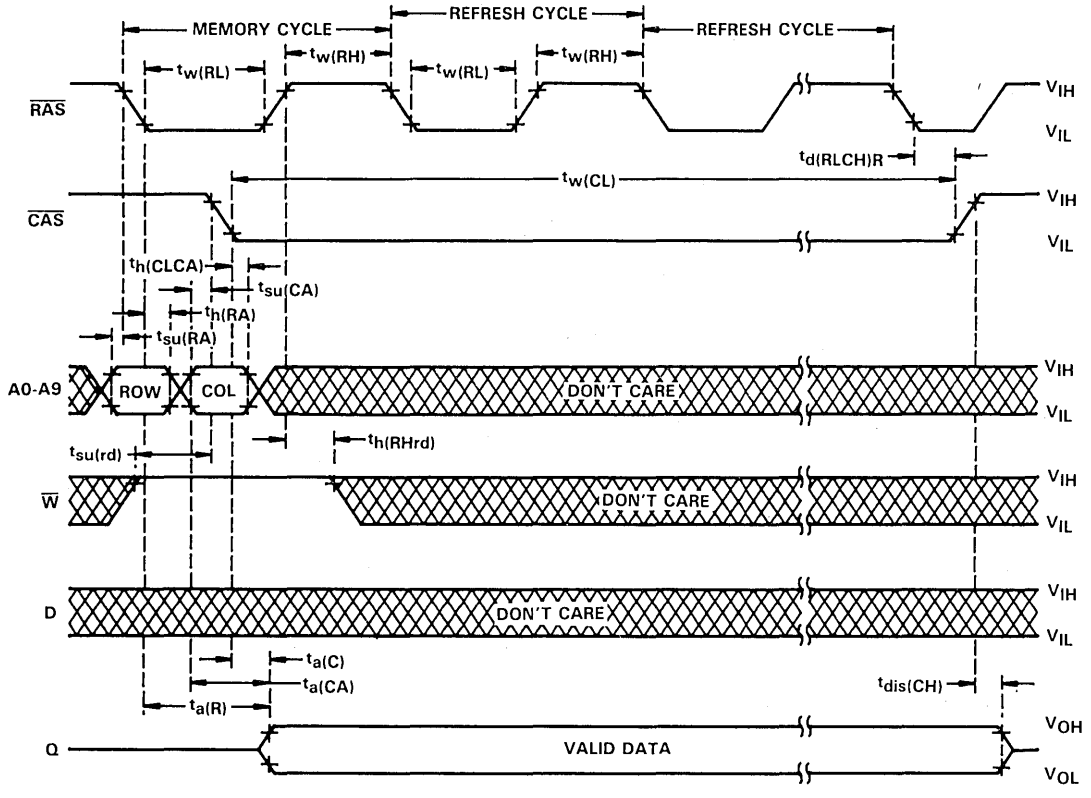


NOTES: 23. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.
24. Output may go from three-state to an invalid data state prior to the specified access time.

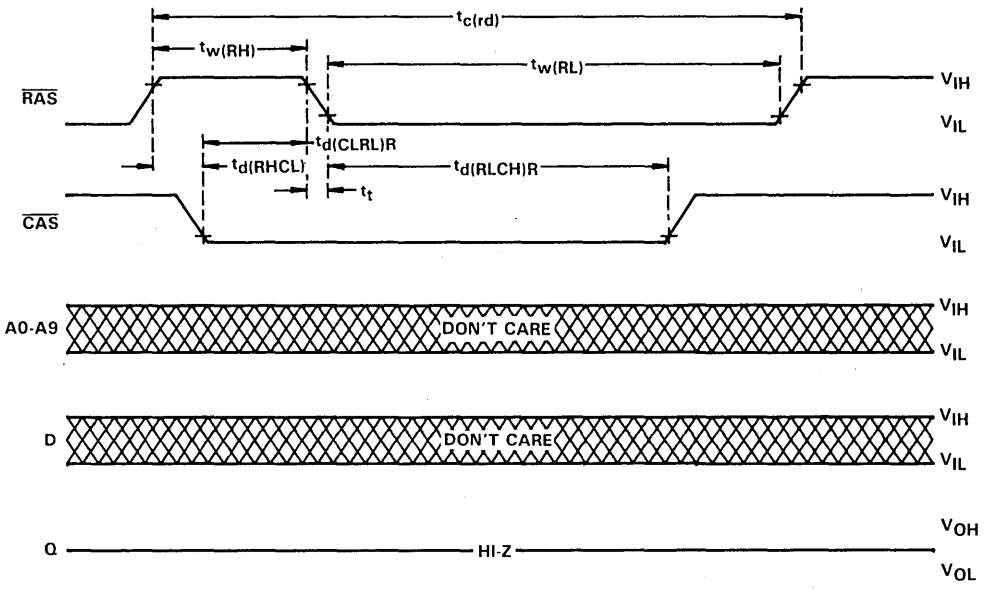
$\overline{RAS}$ only refresh timing



hidden refresh cycle



automatic ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$) refresh timing

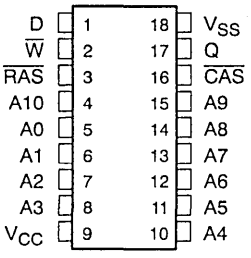


- MIL-STD-883C, Class B, High-Reliability Processing
- Military Temperature Range . . . – 55°C to 125°C
- Organization . . . 4 194 304 × 1
- Single 5-V Power Supply (±10% Tolerance)
- Performance Ranges:

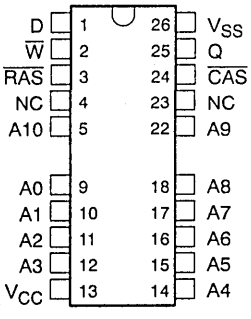
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
SMJ44100-80	80 ns	20 ns	40 ns	150 ns
SMJ44100-10	100 ns	25 ns	50 ns	180 ns
SMJ44100-12	120 ns	30 ns	55 ns	210 ns

- Enhanced Page Mode Operation for Faster Memory Access
  - — Higher Data Bandwidth than Conventional Page-Mode Parts
  - — Random Single-Bit Access Within a Row With a Column Address
- CAS-Before-RAS Refresh
- Long Refresh Period . . . 1024-Cycle Refresh in 16 ms (Max)
- 3-State Unlatched Output
- Low Power Dissipation
- Texas Instruments EPIC™ CMOS Process
- All Inputs/Outputs and Clocks are TTL Compatible
- Packaging Options:
  - — 400 mil 20/26-Leadless Ceramic SOLCC (HM Suffix)
  - — 18-Pin, 400 mil Ceramic DIP (JD Suffix)
  - — 20-Pin, Ceramic FLATPACK (HR Suffix)
  - — 20-Pin, Ceramic CSOJ
  - — Additional Package Options Planned

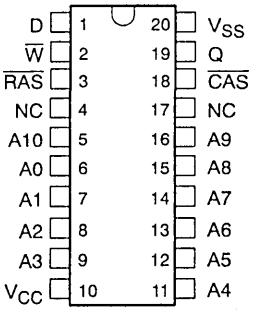
JD Package
(Top View)



HM and CSOJ Packages
(Top View)



HR Package
(Top View)



PIN NOMENCLATURE	
A0-A10	Address Inputs
CAS	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
RAS	Row-Address Strobe
W	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

ADVANCE INFORMATION

description

The SMJ44100 series are high-speed 4 194 304-bit dynamic random-access memories, organized as 4 194 304 words of one bit each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power operation.

The SMJ44100 features maximum row access time of 80 ns, 100 ns, and 120 ns. Maximum power dissipation is as low as 385 mW operating and 22 mW standby.

EPIC is a trademark of Texas Instruments Incorporated.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ44100 is offered in a 400 mil 20/26-leadless ceramic surface mount SOLCC package (HM Suffix), 18-pin ceramic dual-in-line package (JD Suffix), 20-pin ceramic flatpack (HR Suffix) and a 20-pin leaded ceramic chip carrier (CSOJ). All packages are guaranteed for operation from – 55°C to 125°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ44100 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0 through A10)

Twenty-two address bits are required to decode 1 of 4 194 304 storage cell locations. Eleven row-address bits are set up on inputs A0 through A10 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The eleven column-address bits are set up on pins A0 through A10 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{AA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every sixteen milliseconds to retain data. This can be achieved by strobing each of the1024 rows (A0-A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter t_{CSR}] and holding it low after $\overline{RAS}$ falls [see parameter t_{CHR}]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

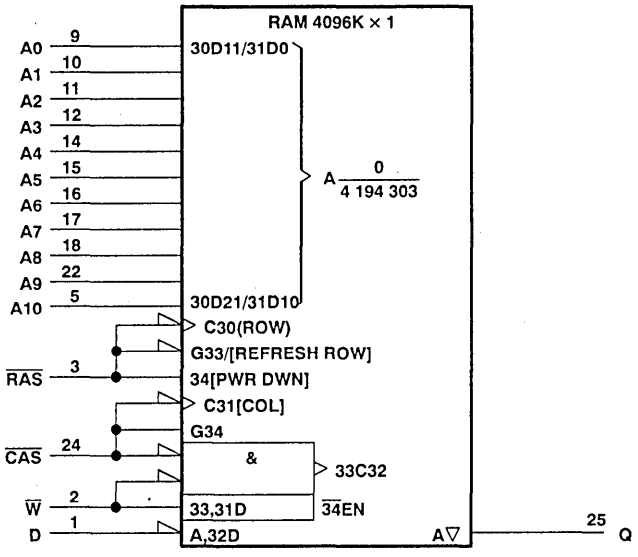
power-up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

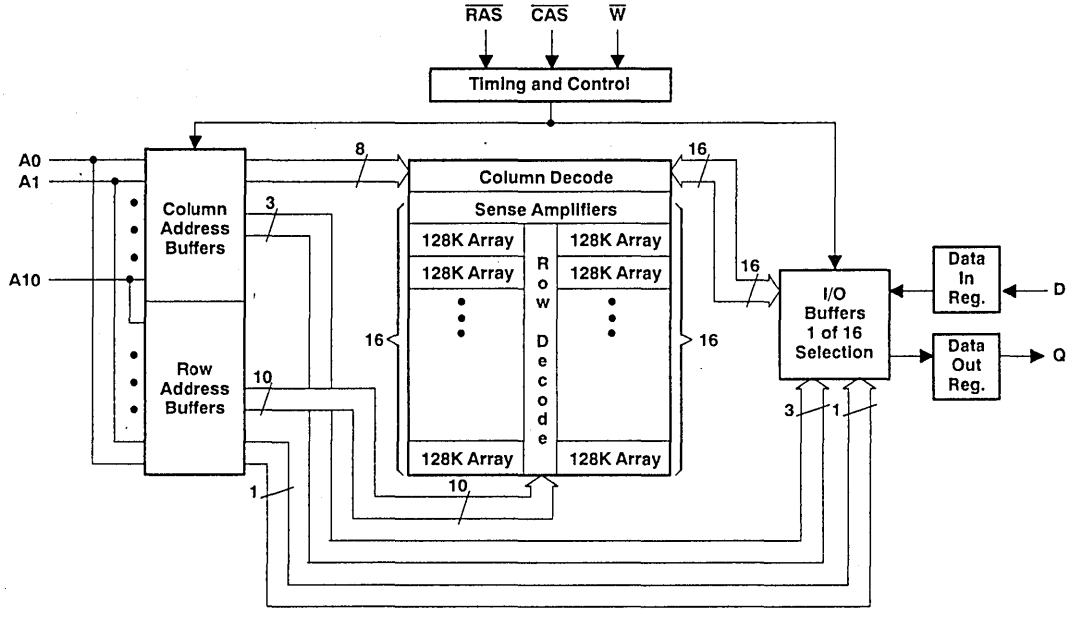
An industry standard Design For Test (DFT) mode is incorporated in the SMJ44100. A $\overline{CAS}$-before-$\overline{RAS}$ cycle with $\overline{W}$ low (WCBR) cycle is used to enter test mode. In the test mode, data is written into and read from eight sections of the array in parallel. Data is compared upon reading and if all bits are equal, the data out pin will go high. If any one bit is different, the data out pin will go low. Any combination read, write, read-write, or page-mode can be used in test mode. The test mode function reduces test times by enabling the 4 meg DRAM to be tested as if it were a 512K DRAM, where row address 10, column address 10, and also column address 0 are not used. A $\overline{RAS}$ only or CBR refresh cycle is used to exit the DFT mode.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the SOLCC(HM) package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating temperature ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Min operating temperature	– 55			°C
T_C	Max operating case temprature			125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ44100-80		SMJ44100-10		SMJ44100-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		85		80		70	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		4		4		4	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only, or $\overline{CBR}$) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low, after $\overline{CAS}$ low (CBR)		85		75		65	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		40		35	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			7	pF
$C_{i(D)}$	Input capacitance, data inputs			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			10	pF
$C_{i(W)}$	Input capacitance, write-enable input			10	pF
C_o	Output capacitance			10	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V. Capacitance is sampled only at initial design and after any major change.

switching characteristics over recommended ranges of supply voltage range and operating temperature

PARAMETER		SMJ44100-80		SMJ44100-10		SMJ44100-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		40		50		55	ns
t_{CAC}	Access time from $\overline{CAS}$ low		20		25		30	ns
t_{CPA}	Access time from column precharge		45		50		55	ns
t_{RAC}	Access time from $\overline{RAS}$ low		80		100		120	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)		20		25		30	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven. The output is disabled when $\overline{CAS}$ is brought high.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating temperature

		SMJ44100-80		SMJ44100-10		SMJ44100-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	150		180		210		ns
t_{RWC}	Read-write cycle time	175		210		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	50		60		65		ns
t_{PRWC}	Page-mode read-write cycle time	70		85		95		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	80	100 000	100	100 000	120	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	80	10 000	100	10 000	120	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	20	10 000	25	10 000	30	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		15		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	60		70		80		ns
t_{WP}	Write pulse duration	15		20		25		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	20		25		30		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	20		25		30		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	15		20		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low	60		75		90		ns
t_{DH}	Data hold time (see Note11)	15		20		25		ns
t_{AR}	Column address hold time after $\overline{RAS}$ low (see Note 13)	60		75		90		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		15		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 12)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 12)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		20		25		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 10)	60		75		90		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	40		50		55		ns

Continued next page.

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. The minimum value is measured when t_{RDC} is set to t_{RCD} min as a reference.

ADVANCE INFORMATION

timing requirements over recommended supply voltage range and operating temperature range (concluded)

		SMJ44100-80		SMJ44100-10		SMJ44100-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		25		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	80		100		120		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	20		25		30		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	40	20	50	20	65	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	40		50		55		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	40		50		55		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	60	25	75	25	90	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	20		25		30		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	80		100		120		ns
t_{CLZ}	$\overline{CAS}$ to output in low Z (see Note 15)							
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time (see Note 16)							

NOTES: 14. Maximum value specified only to assure access time.
15. Valid data is presented at the output after all access times are satisfied. The output may go from three-state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.
16. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be minimum of 3 ns and maximum of 50 ns.

PARAMETER MEASUREMENT INFORMATION

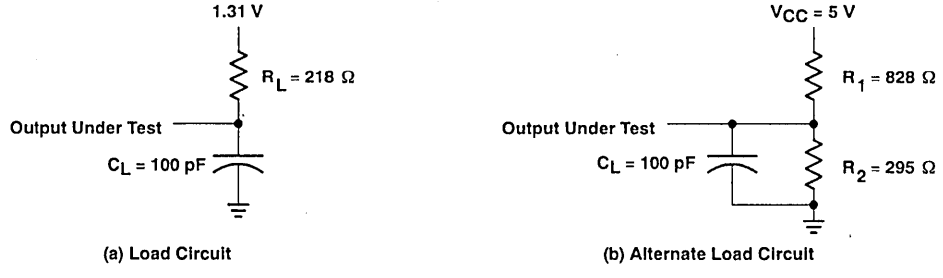
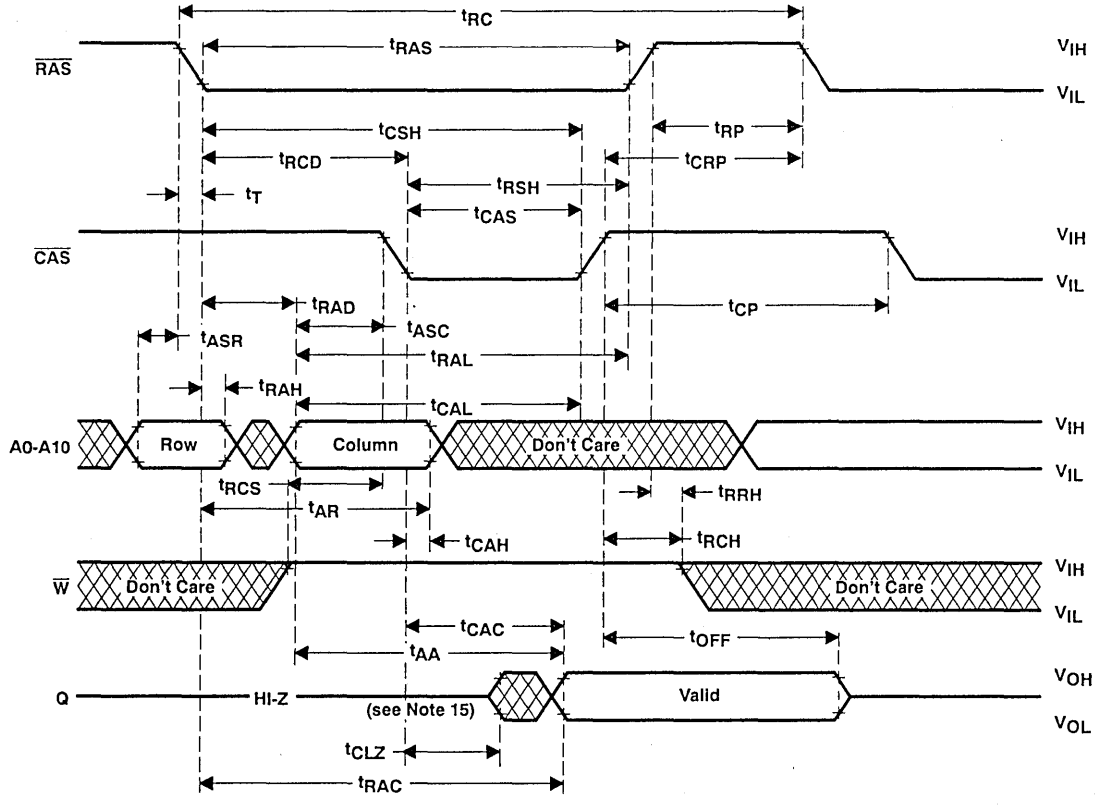


Figure 1. Load Circuits for Timing Parameters

read cycle timing

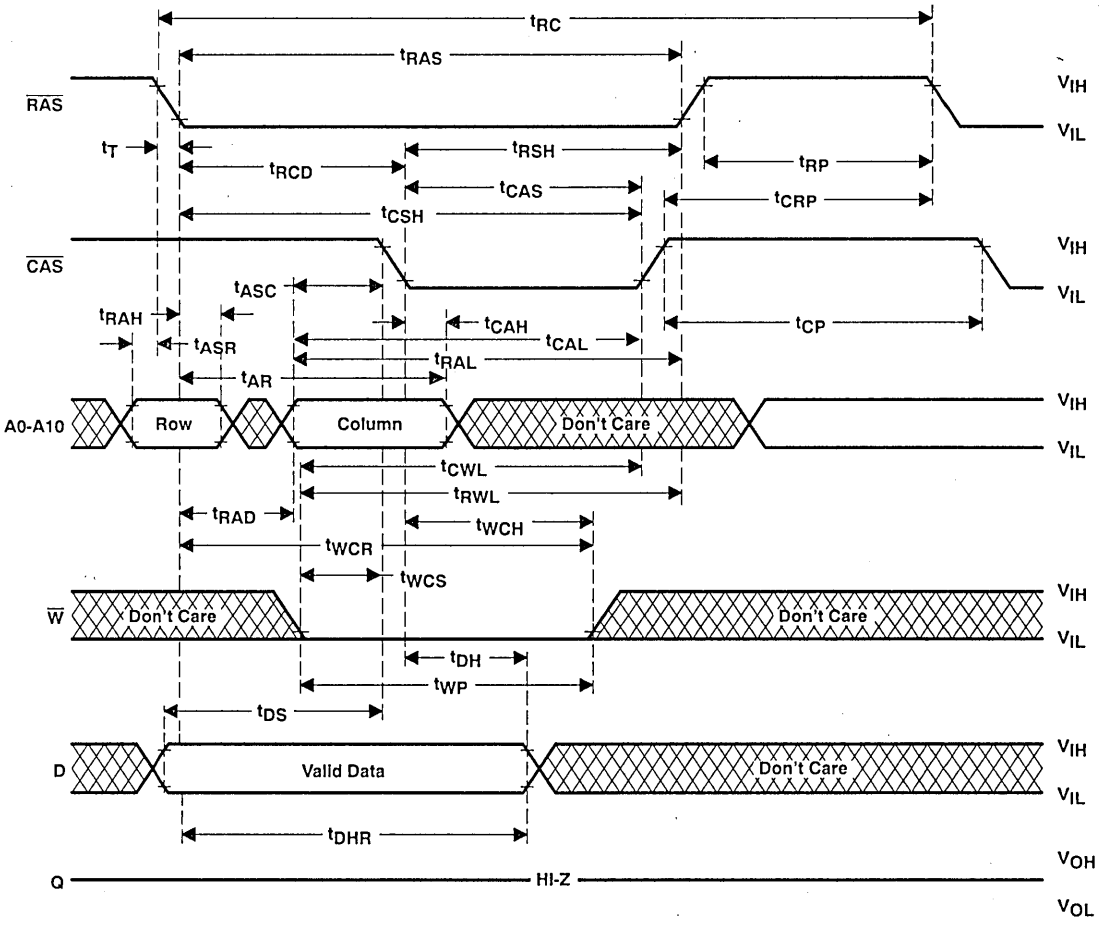


NOTE 15: Valid data is presented at the output after all access times are satisfied. The output may go from three-state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

ADVANCE INFORMATION

ADVANCE INFORMATION

early write cycle timing



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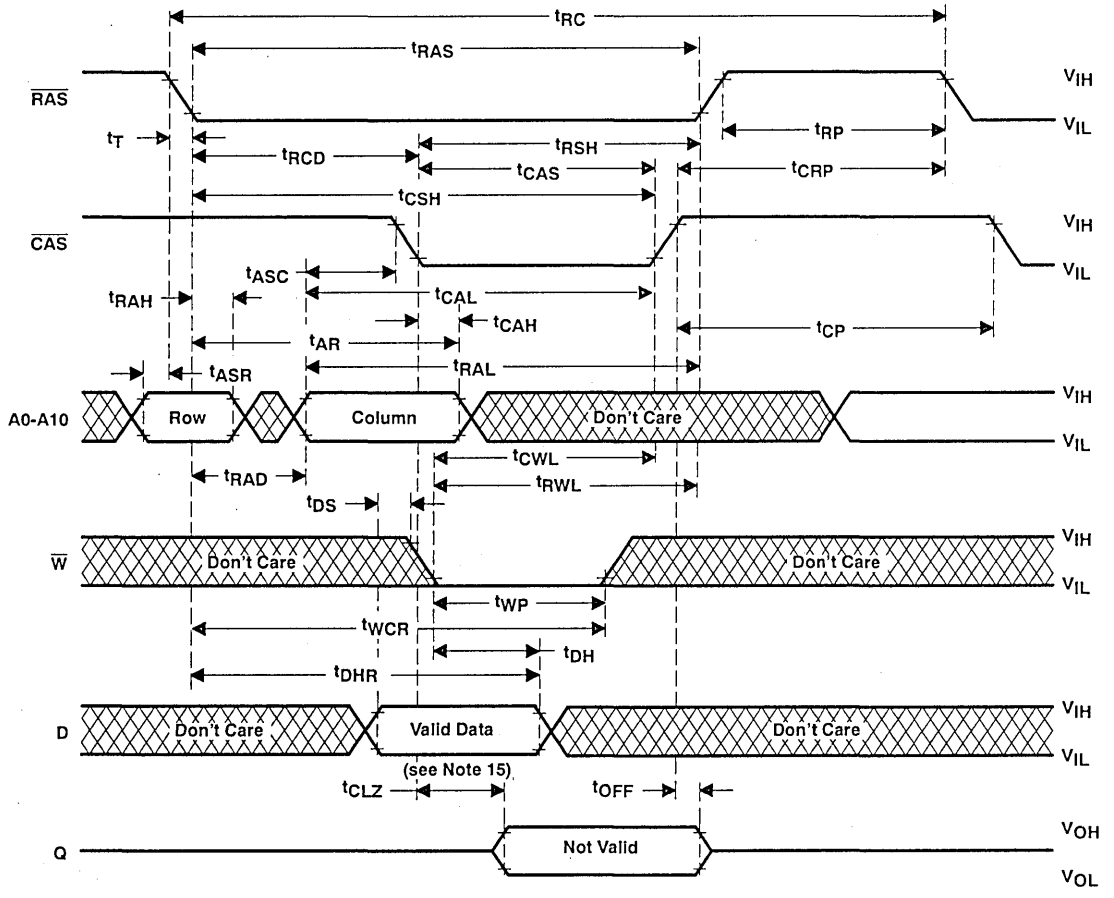
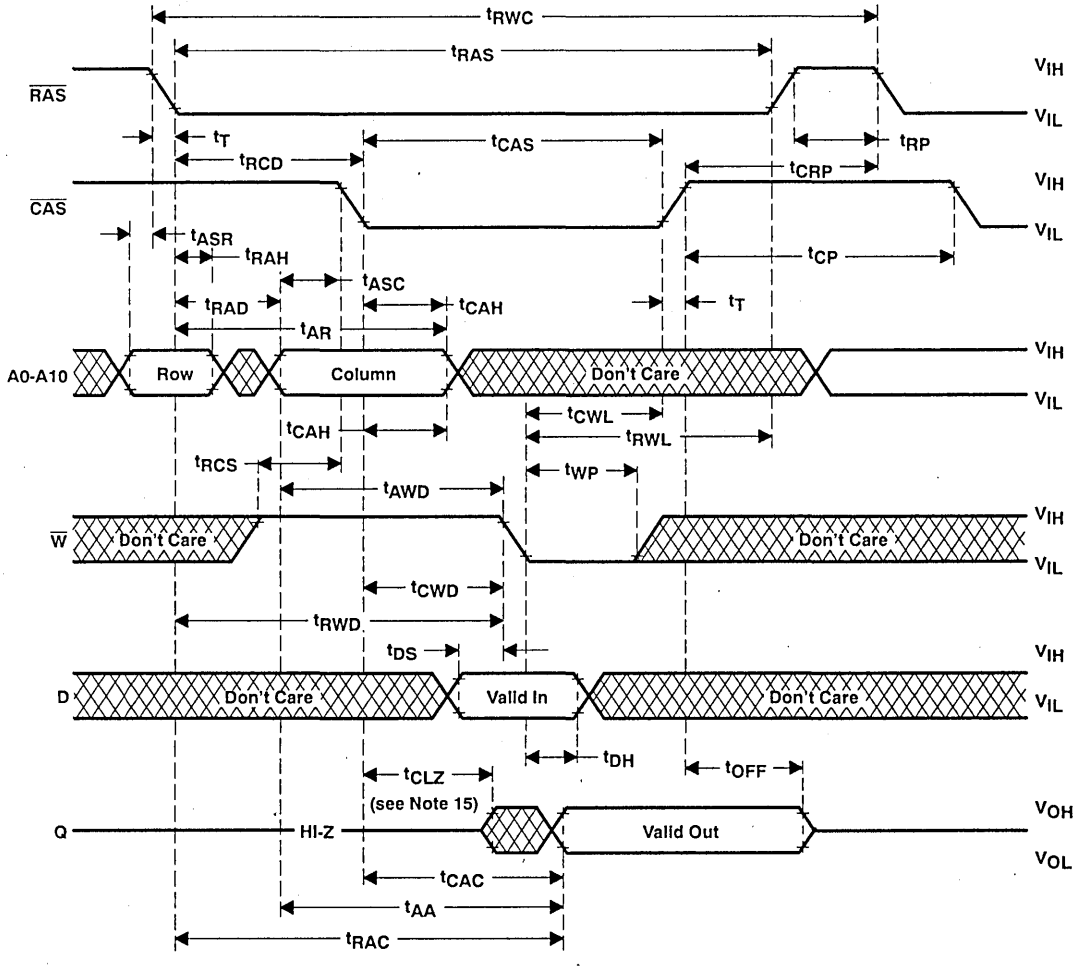
write cycle timing



NOTE 15: Valid data is presented at the output after all access times are satisfied. The output may go from three-state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

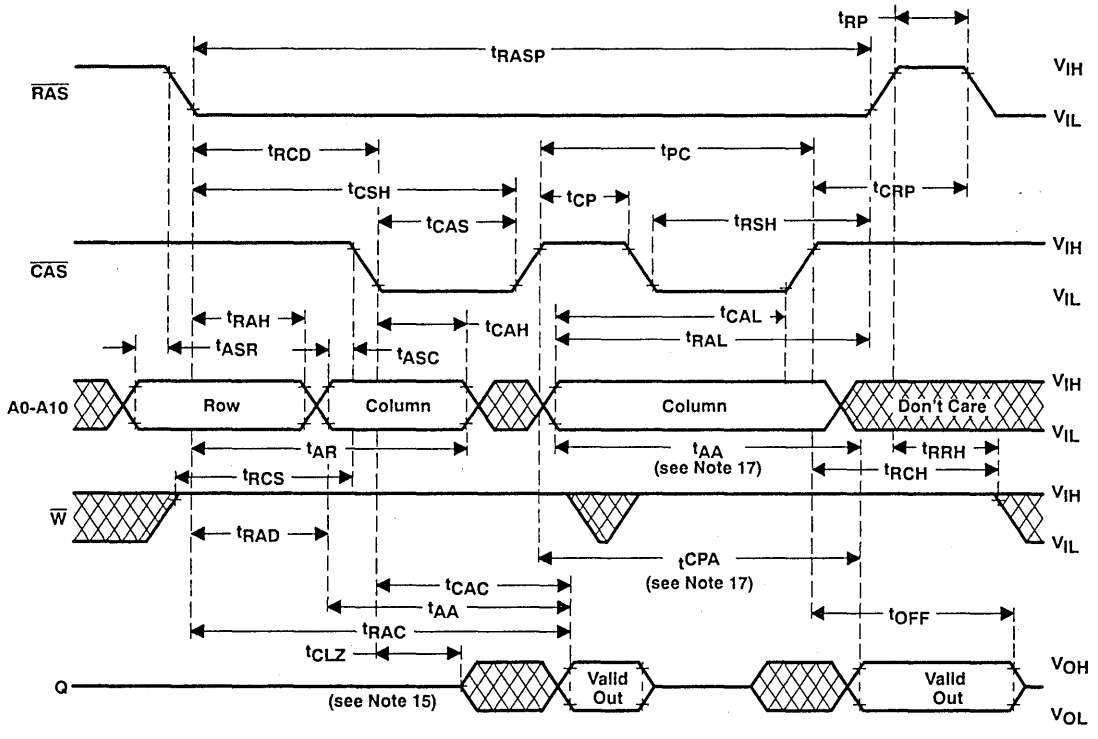
ADVANCE INFORMATION

read-write cycle timing



NOTE 15: Valid data is presented at the output after all access times are satisfied. The output may go from three-state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

enhanced page-mode read cycle timing

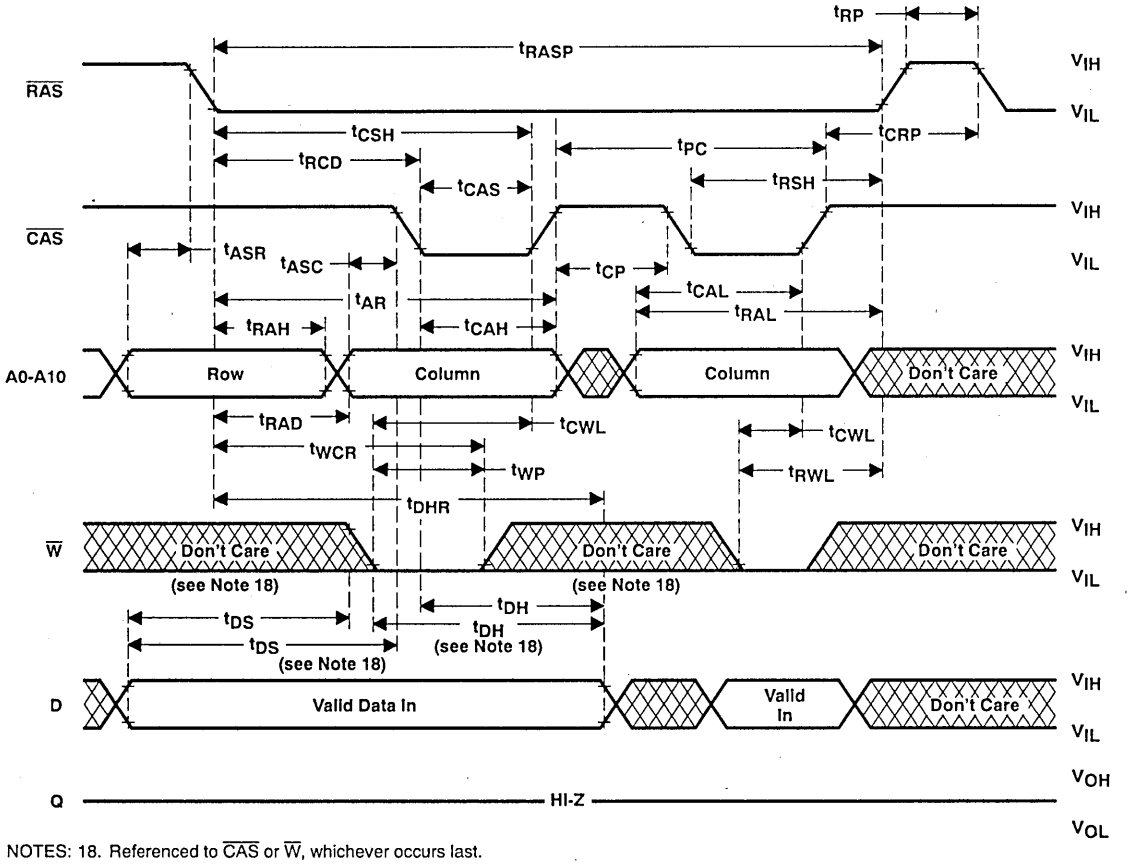


NOTES: 15. Valid data is presented at the output after all access times are satisfied. The output may go from three-state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

17. Access time is t_{CPA} or t_{AA} dependent.

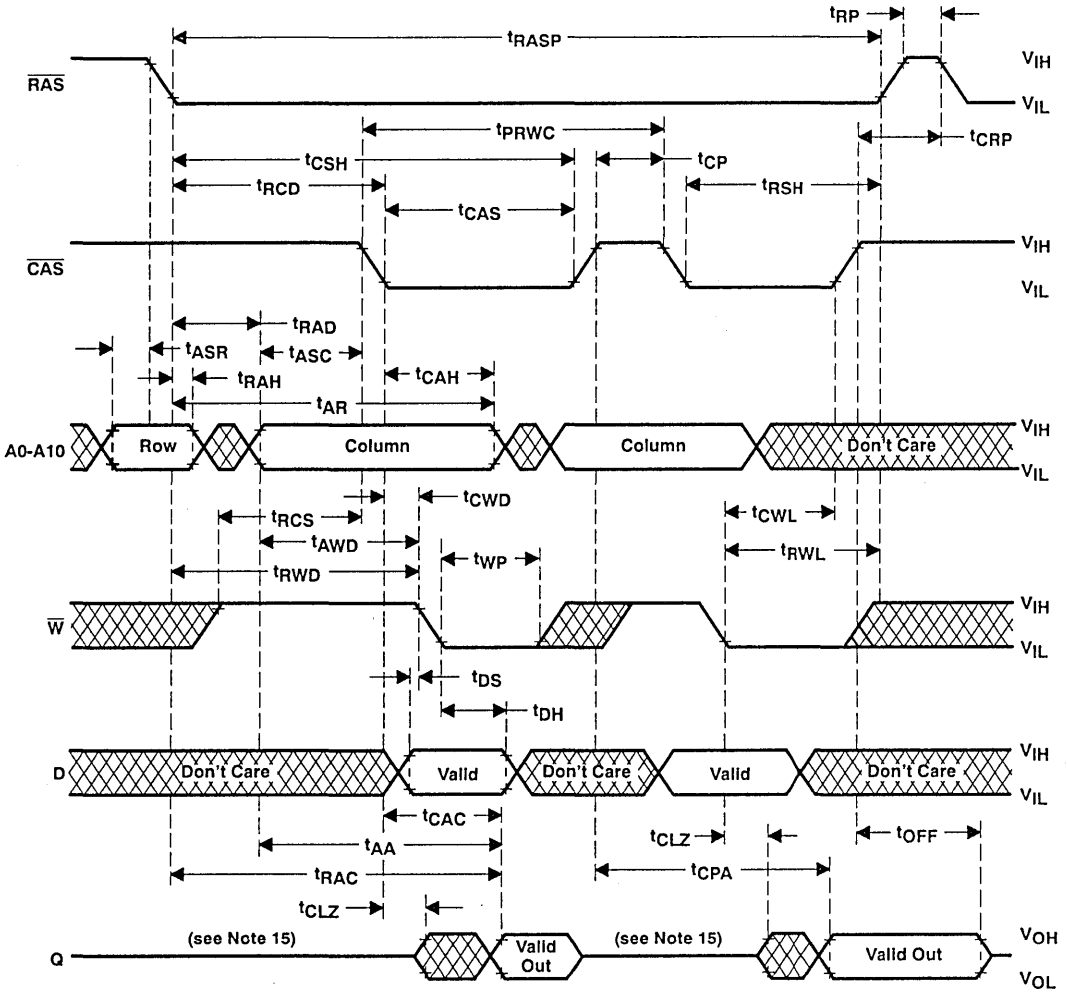
ADVANCE INFORMATION

enhanced page-mode write cycle timing (see Note 19)



NOTES: 18. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
19. A read cycle or a read-write cycle can be intermixed with a write cycle as long as read and read-write timing specifications are not violated.

enhanced page-mode read-write cycle timing (see Note 20)

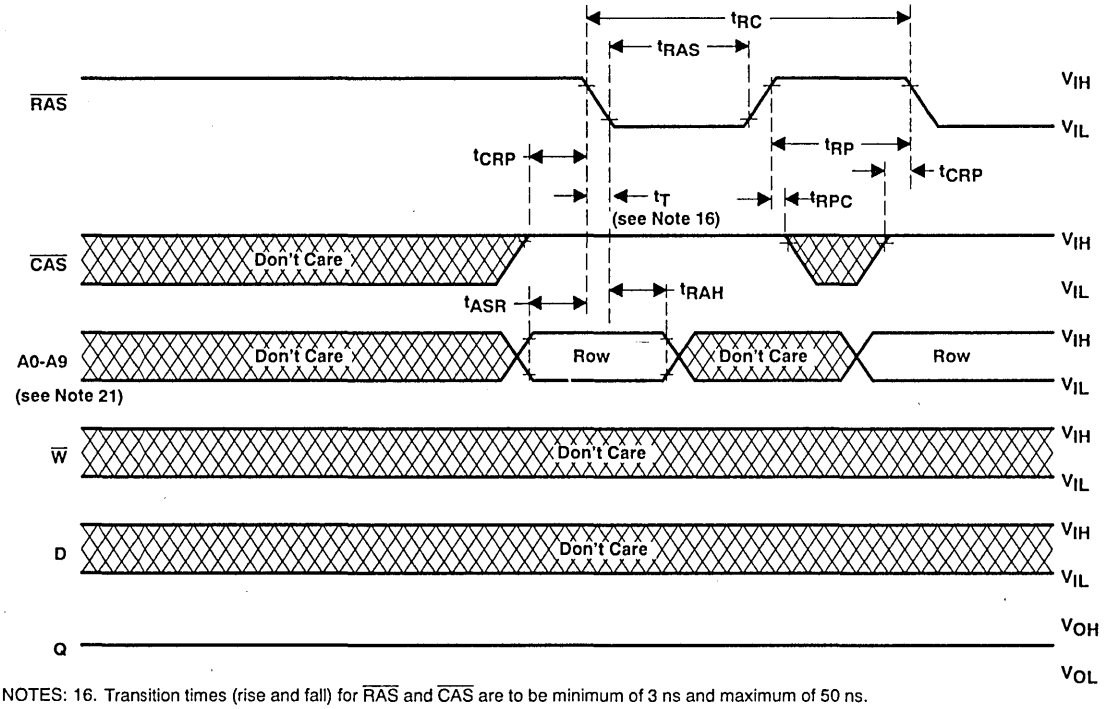


NOTES: 15. Valid data is presented at the output after all access times are satisfied. The output may go from three-state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

20. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

ADVANCE INFORMATION

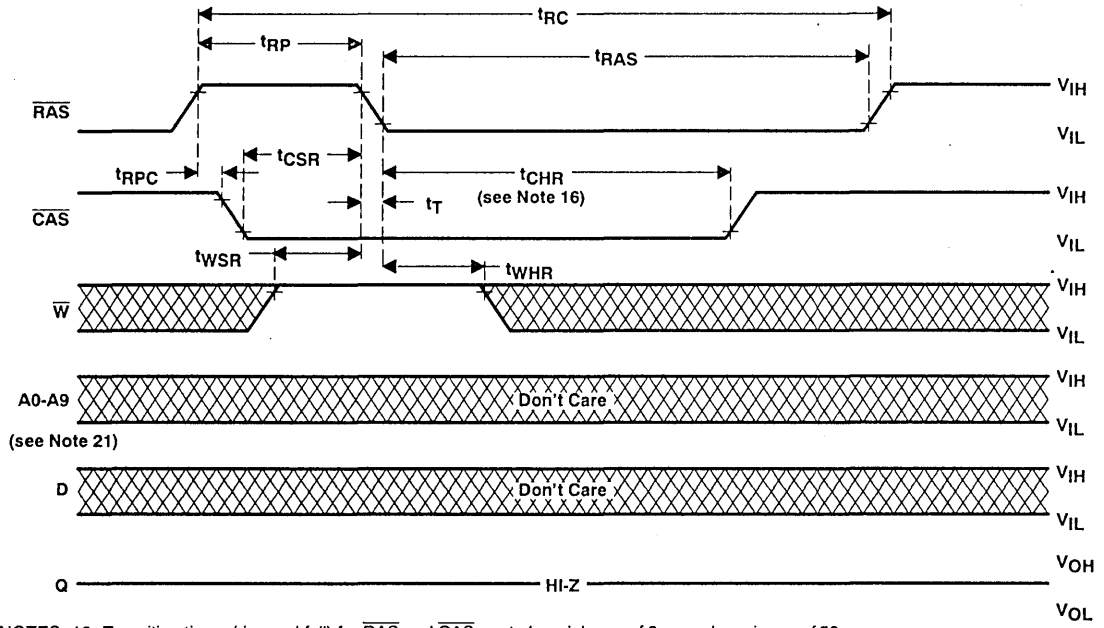
$\overline{\text{RAS}}$-only refresh timing



NOTES: 16. Transition times (rise and fall) for $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are to be minimum of 3 ns and maximum of 50 ns.
21. A10 is a don't care.

ADVANCE INFORMATION

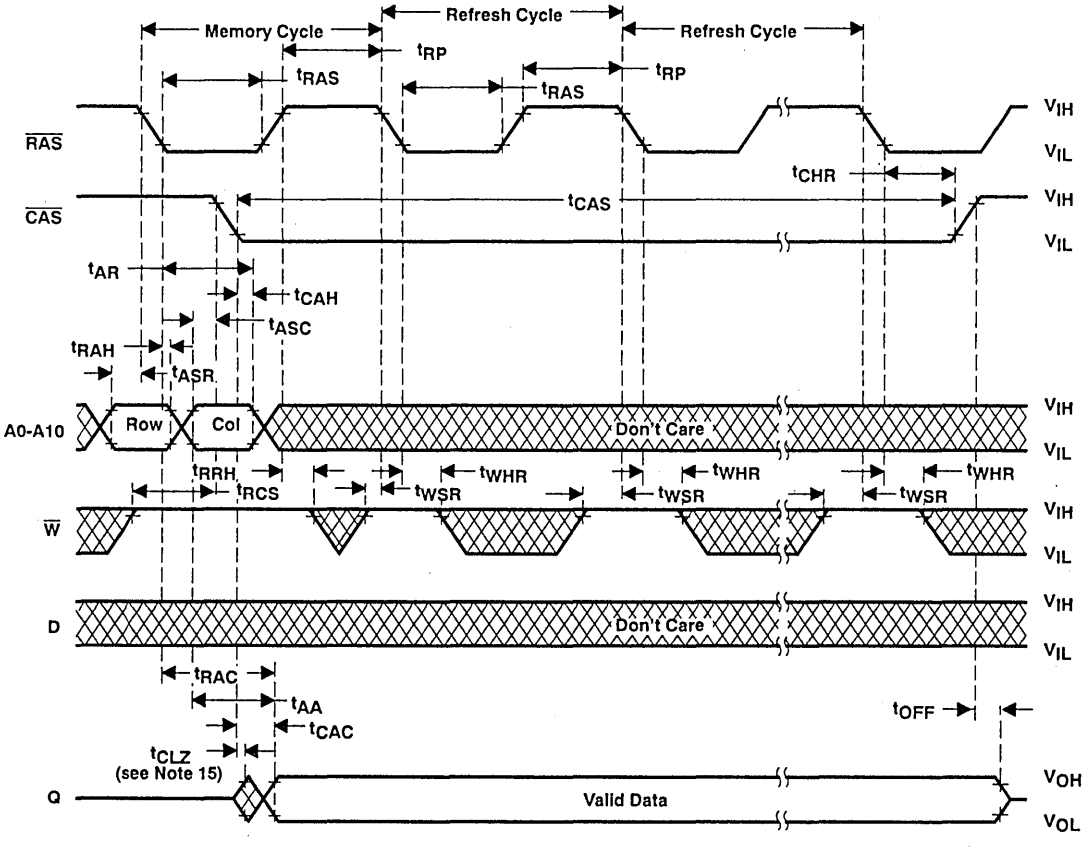
automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



NOTES: 16. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be minimum of 3 ns and maximum of 50 ns.
21. A10 is a don't care.

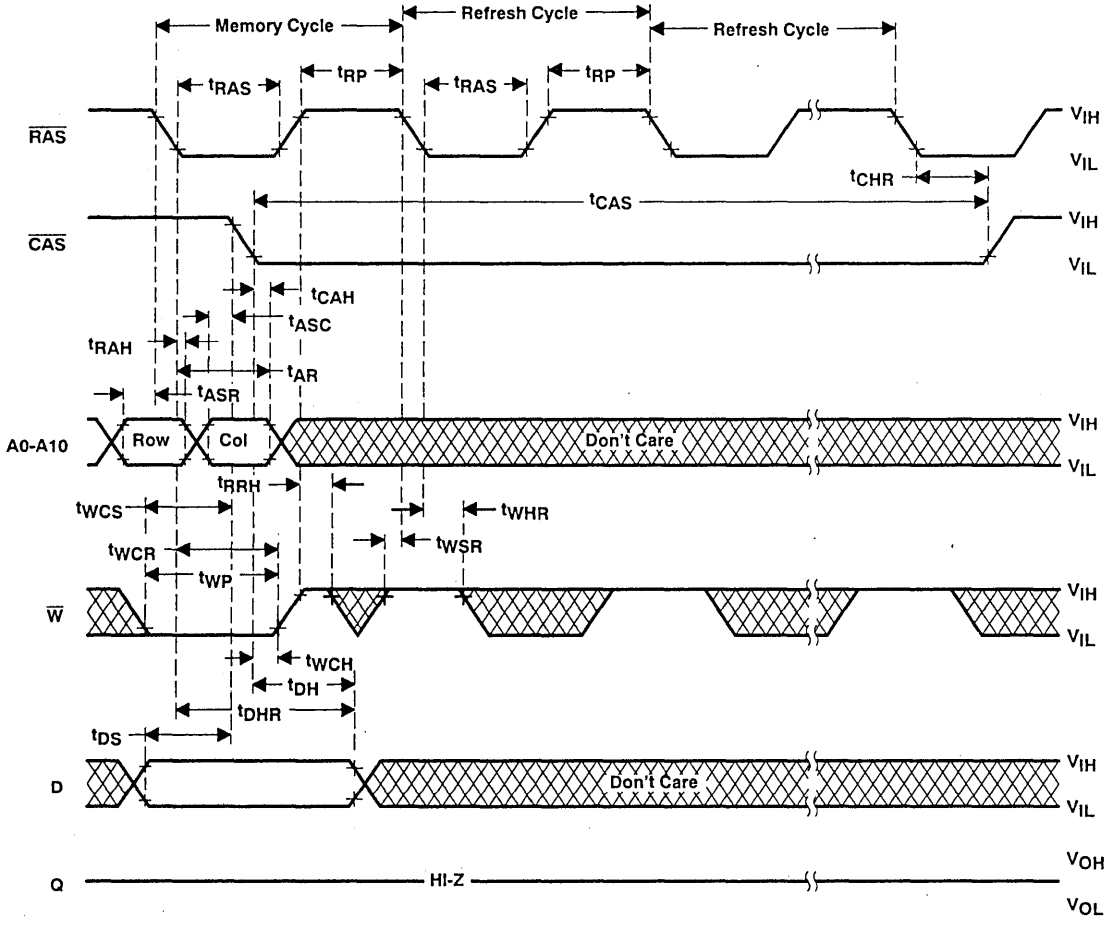
ADVANCE INFORMATION

hidden refresh cycle (read)



NOTE 15: Valid data is presented at the output after all access times are satisfied. The output may go from three-state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

hidden refresh cycle (write)



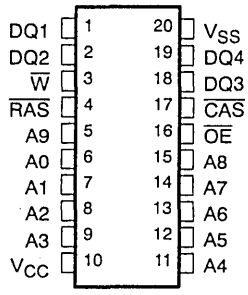
ADVANCE INFORMATION

- **Military Temperature Range . . . – 55 to 125°C**
- **MIL-STD-883C, Class B, High-Reliability Processing**
- **Organization . . . 1 048 576 × 4**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

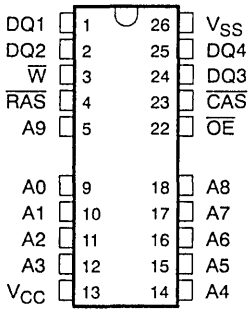
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
SMJ44400-80	80 ns	20 ns	40 ns	150 ns
SMJ44400-10	100 ns	25 ns	50 ns	180 ns
SMJ44400-12	120 ns	30 ns	55 ns	210 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
  - **— Higher Data Bandwidth than Conventional Page-Mode Parts**
  - **— Random Single-Bit Access Within a Row With a Column Address**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 1024-Cycle Refresh in 16 ms (Max)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **Packaging Options:**
  - **— 400 mil 20/26-Leadless Ceramic SOLCC (HM Suffix)**
  - **— 20-Pin, 400 mil Ceramic DIP (JD Suffix)**
  - **— 20-Pin, Ceramic FLATPACK (HR Suffix)**
  - **— 20-Pin, Ceramic CSOJ**
  - **— Additional Package Options Planned**

JD and HR Package
(Top View)



HM and CSOJ Package
(Top View)



PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

ADVANCE INFORMATION

description

The SMJ44400 series are high-speed 4 194 304-bit dynamic random-access memories, organized as 1 048 576 words of four bits each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power operation.

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The SMJ44400 features maximum row access time of 80 ns, 100 ns, and 120 ns. Maximum power dissipation is as low as 360 mW operating and 22 mW standby.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ44400 is offered in a 400-mil 20/26-leadless ceramic surface mount SOLCC package (HM suffix), a 20-pin ceramic dual-in-line package (JD suffix), a 20-pin ceramic flatpack (HR suffix), and a 20-pin leaded ceramic chip carrier (CSOJ). All packages are characterized for operation from – 55°C to 125°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ44400 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0 through A9)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data in/out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OED}.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every sixteen milliseconds to retain data. This can be achieved by strobing each of the1024 rows (A0-A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter t_{CSR}] and holding it low after $\overline{RAS}$ falls [see parameter t_{CHR}]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

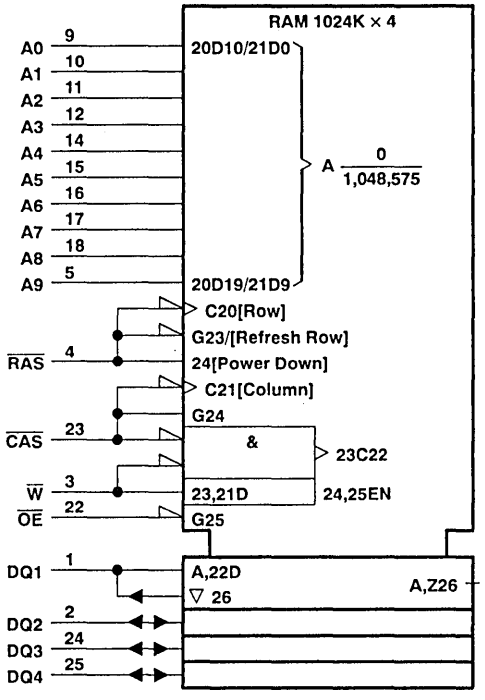
power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

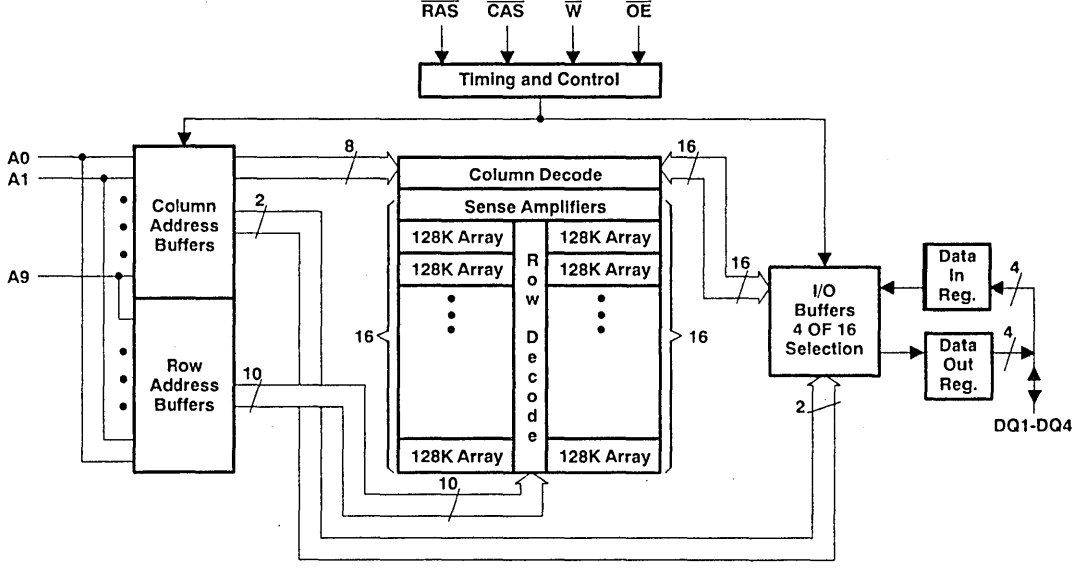
An industry standard Design For Test (DFT) mode is incorporated in the SMJ44400. A $\overline{CAS}$-before-$\overline{RAS}$ with $\overline{W}$ low (WCBR) cycle is used to enter test mode. In the test mode, data is written into and read from eight sections of the array in parallel. All data is written into the array through DQ1. Data is compared upon reading and if all bits are equal, all DQ pins will go high. If any one bit is different, all the DQ pins will go low. Any combination read, write, read-write, or page-mode can be used in the test mode. The test mode function reduces test times by enabling the 1 meg × 4 DRAM to be tested as if it were a 512K DRAM where column address 0 is not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. The pinouts illustrated are for the SOLCC package.

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating temperature ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 0.5		0.6	V
T_A	Min Operating temperature	– 55			°C
T_C	Max Operating case temperature			125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ44400-80		SMJ44400-10		SMJ44400-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		85		80		70	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		4		4		4	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only, or $\overline{CBR}$)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low, after $\overline{CAS}$ low (CBR)		85		75		65	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		40		35	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			10	pF
$C_{i(W)}$	Input capacitance, write-enable input			10	pF
C_O	Output capacitance			10	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V. Capacitance is sampled only at initial design and after any major change.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		SMJ44400-80		SMJ44400-10		SMJ44400-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		40		50		55	ns
t_{CAC}	Access time from $\overline{CAS}$ low		20		25		30	ns
t_{CPA}	Access time from column precharge		45		50		55	ns
t_{RAC}	Access time from $\overline{RAS}$ low		80		100		120	ns
t_{OEA}	Access time from $\overline{OE}$ low		20		25		30	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)		20		25		30	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)		20		25		30	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven. The outputs are disabled by bringing either $\overline{OE}$ or $\overline{CAS}$ high.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating temperature

		SMJ44400-80		SMJ44400-10		SMJ44400-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	150		180		210		ns
t_{RWC}	Read-write cycle time	205		245		285		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	50		60		65		ns
t_{PRWC}	Page-mode read-write cycle time	100		120		135		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	80	100 000	100	100 000	120	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	80	10 000	100	10 000	120	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	20	10 000	25	10 000	30	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		15		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	60		70		80		ns
t_{WP}	Write pulse duration	15		20		25		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	20		25		30		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	20		25		30		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	15		20		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low	60		75		90		ns
t_{DH}	Data hold time (see Note 11)	15		20		25		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 10)	60		75		90		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		15		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 12)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 12)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		20		25		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 10)	60		75		90		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{AWD}	Delay time, column-address to $\overline{W}$ low (Read-write operation only)	70		80		90		ns

Continued next page.

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating temperature (concluded)

		SMJ44400-80		SMJ44400-10		SMJ44400-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		25		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	80		100		120		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	50		60		70		ns
t_{OEH}	$\overline{OE}$ command hold time	20		25		30		ns
t_{OED}	$\overline{OE}$ to data delay	20		25		30		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	20		25		30		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 13)	15	40	20	50	20	65	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	40		50		55		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	40		50		55		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 13)	20	60	25	75	25	90	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	20		25		30		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	110		135		160		ns
t_{CLZ}	$\overline{CAS}$ to output in low Z (see Note 14)							
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time (see Note 15)							

NOTES: 13. Maximum value specified only to guarantee access time.
14. Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.
15. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 50 ns.

PARAMETER MEASUREMENT INFORMATION

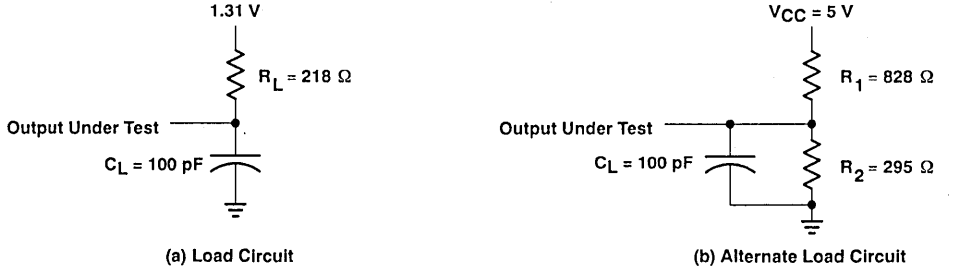
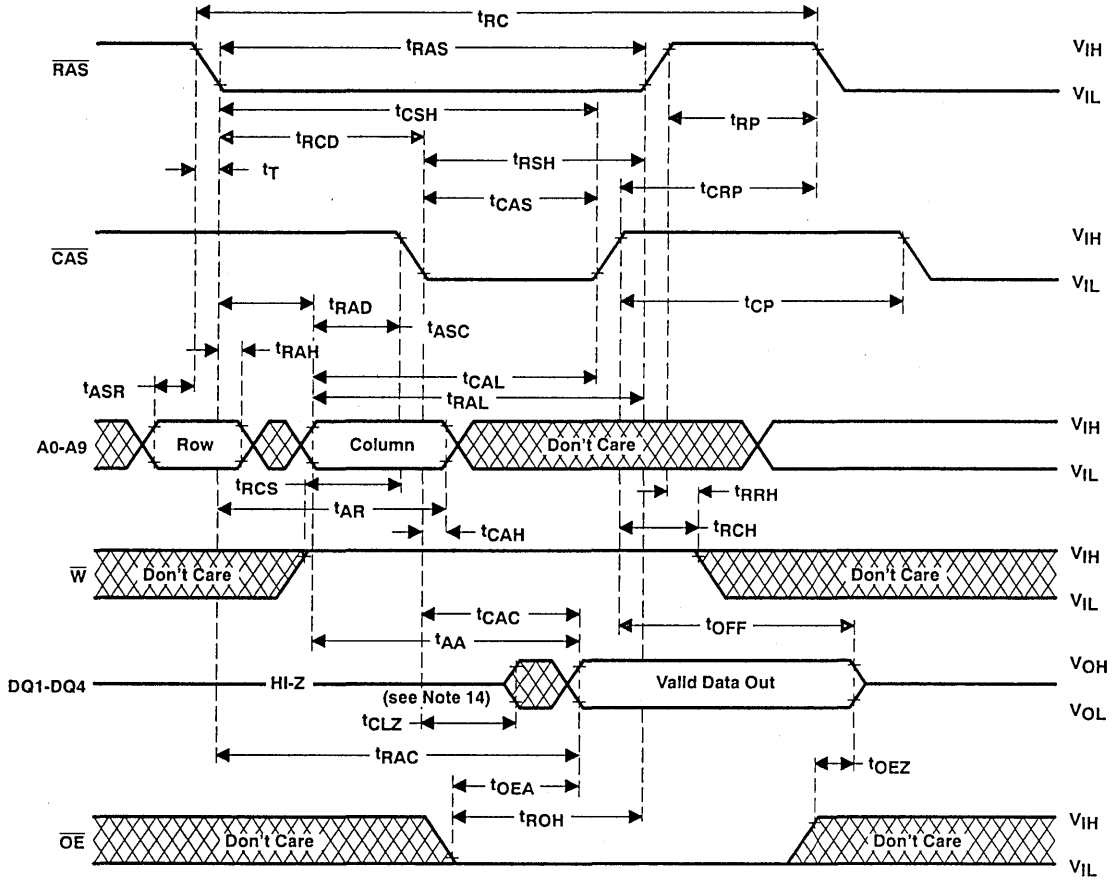


Figure 1. Load Circuits for Timing Parameters

read cycle timing

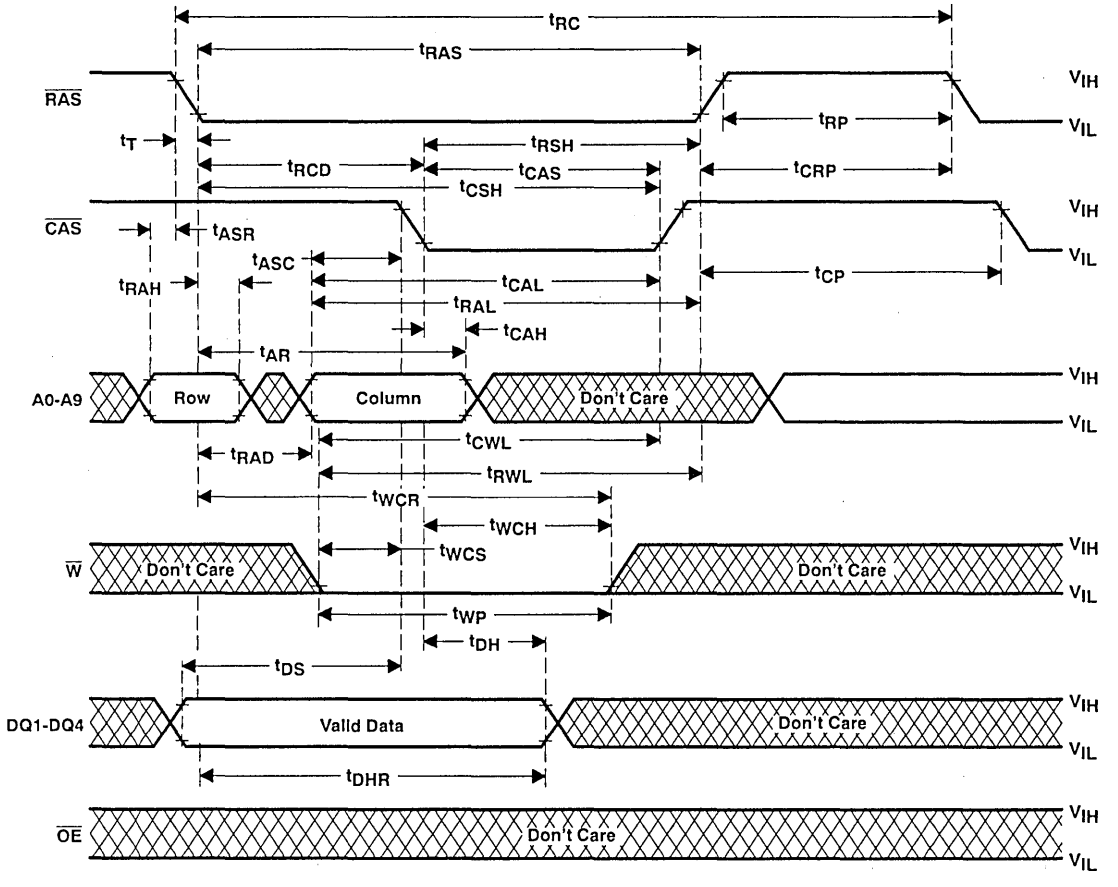


NOTE 14: Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.

ADVANCE INFORMATION

ADVANCE INFORMATION

early write cycle timing



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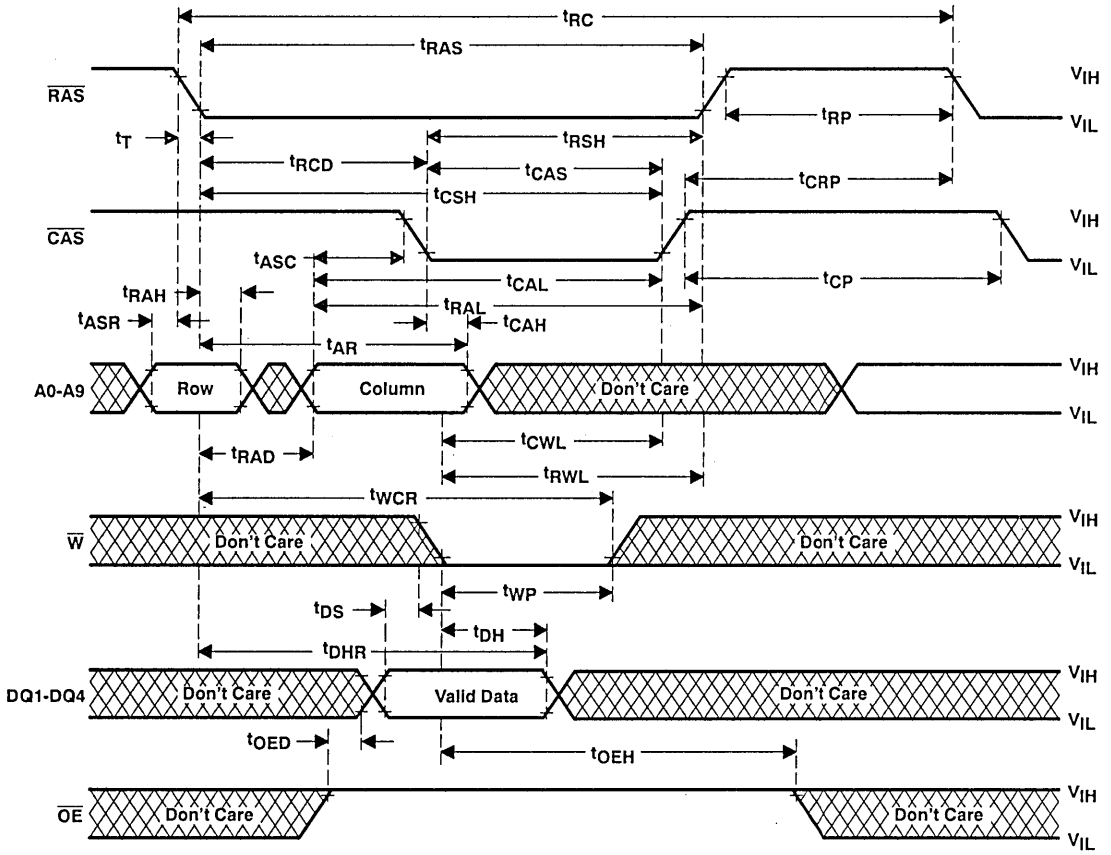
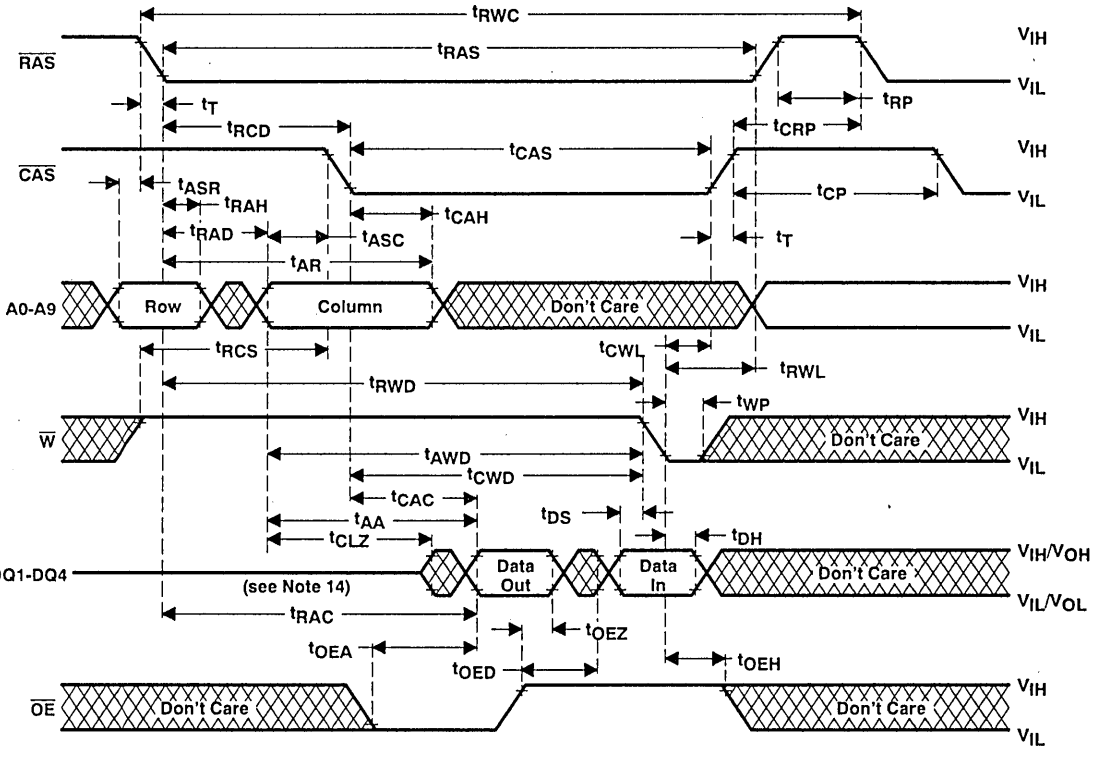
write cycle timing



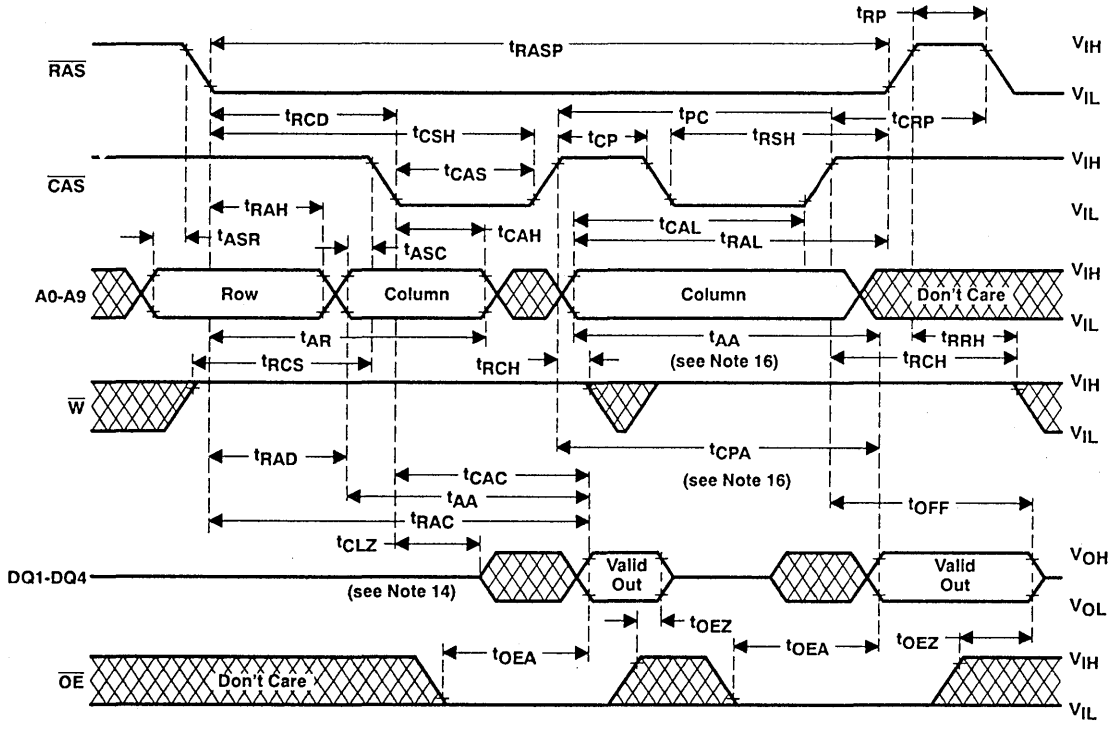
ADVANCE INFORMATION

read-write cycle timing



NOTE 14: Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.

enhanced page-mode read cycle timing

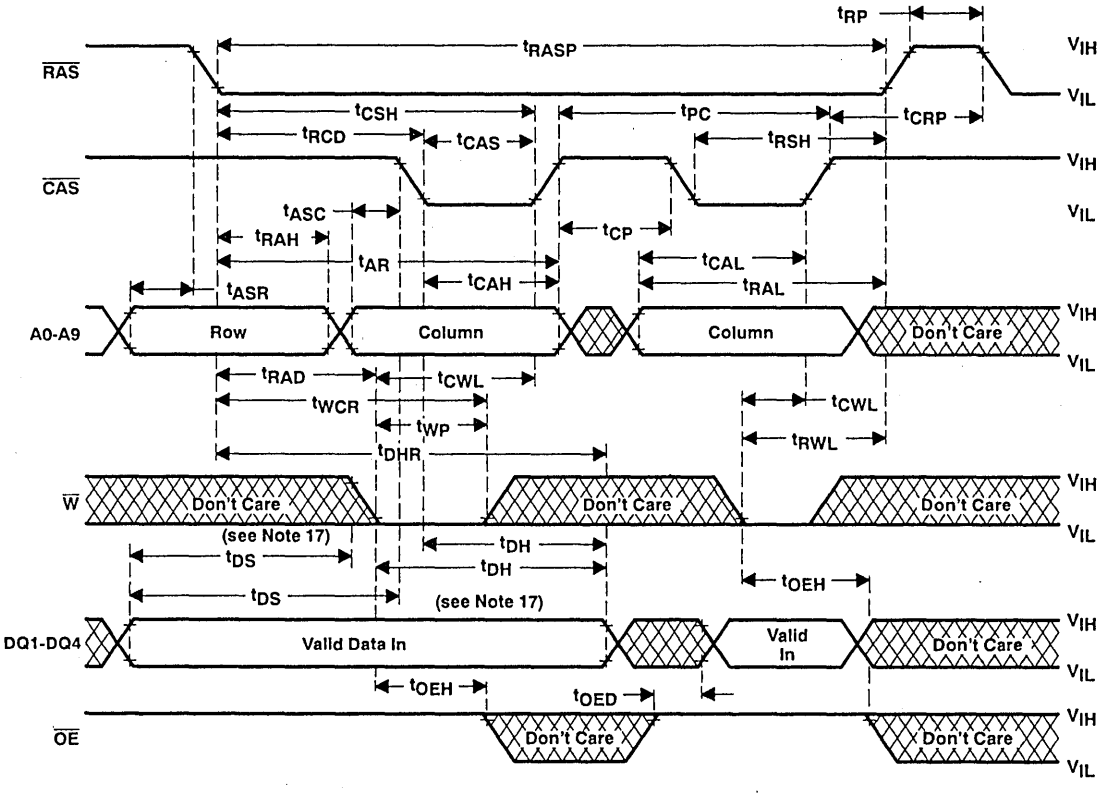


NOTES: 14. Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.

16. Access time is t_{CPA} or t_{AA} dependent.

ADVANCE INFORMATION

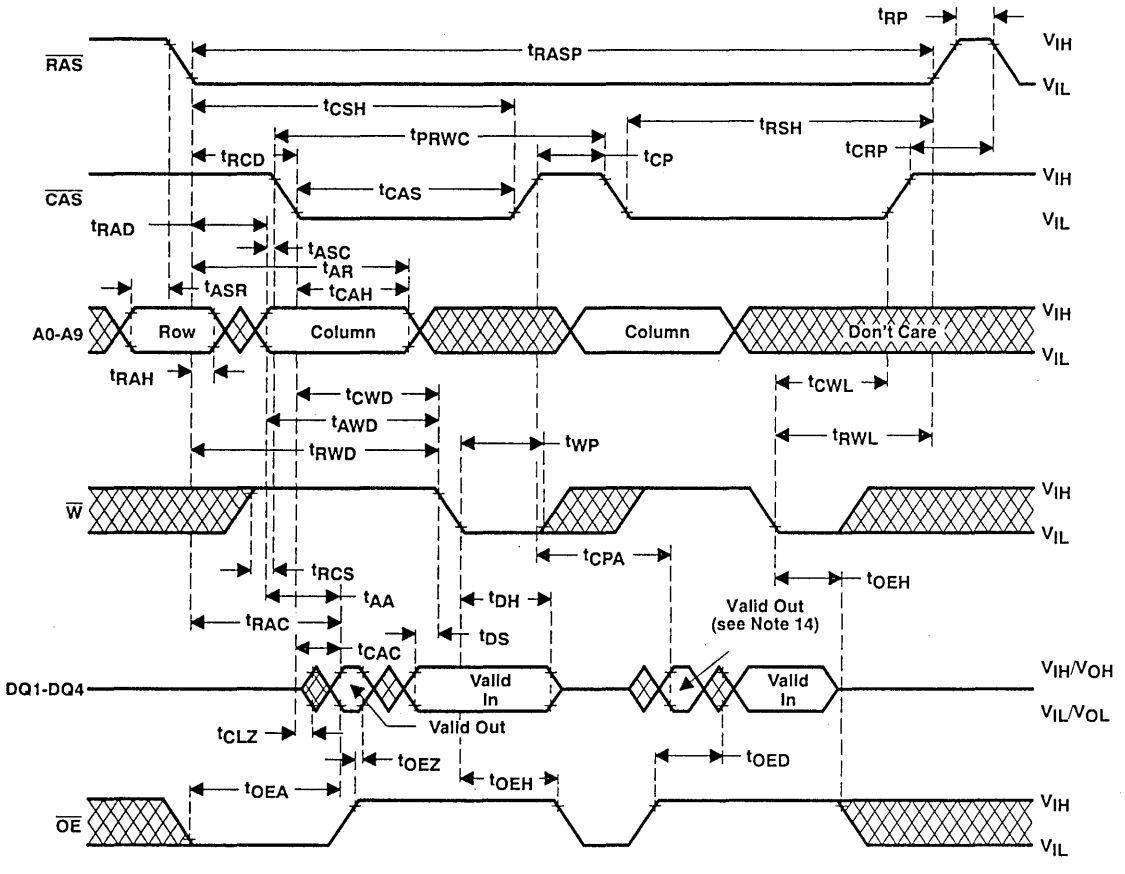
enhanced page-mode write cycle timing (see Note 18)



NOTES: 17. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

18. A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

enhanced page-mode read-write cycle timing (see Note 19)

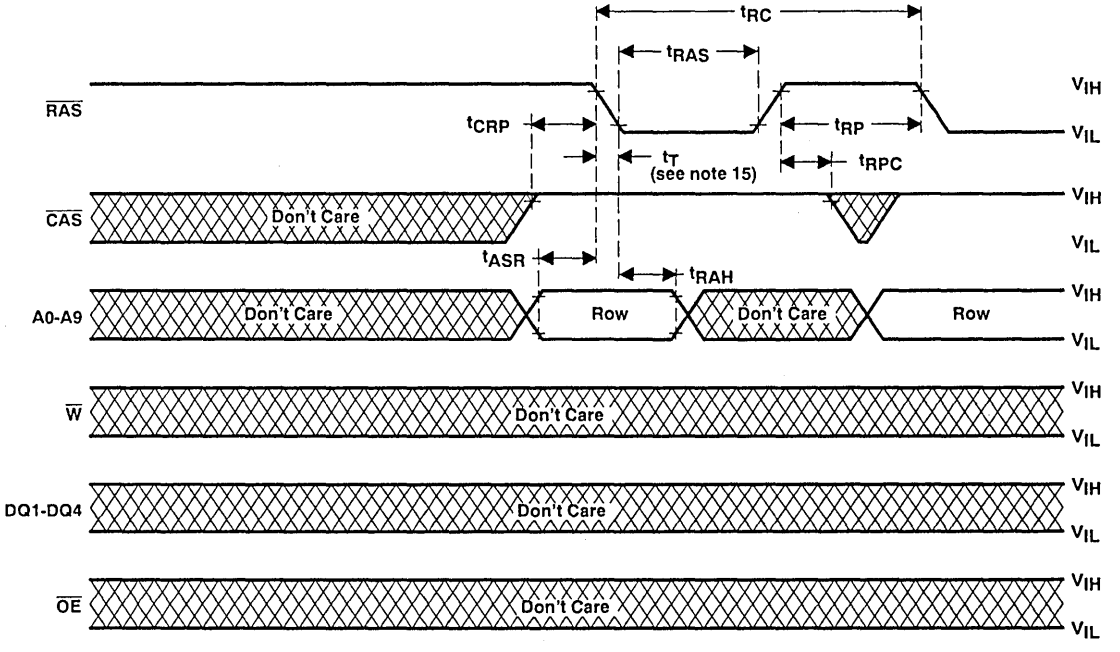


NOTES: 14. Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.

19. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

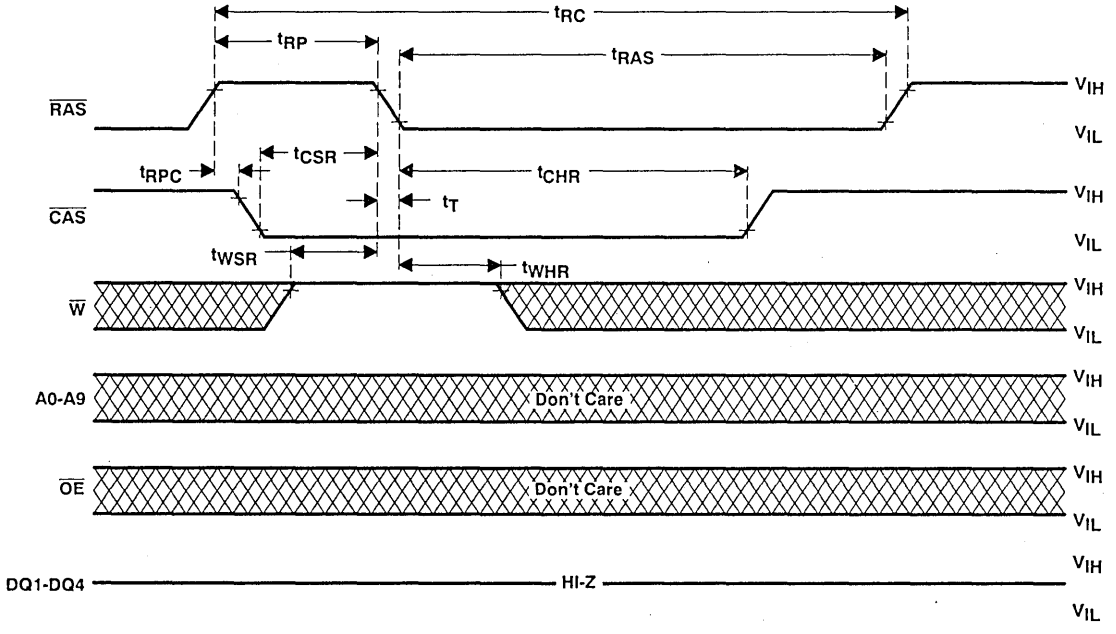
ADVANCE INFORMATION

$\overline{RAS}$-only refresh timing



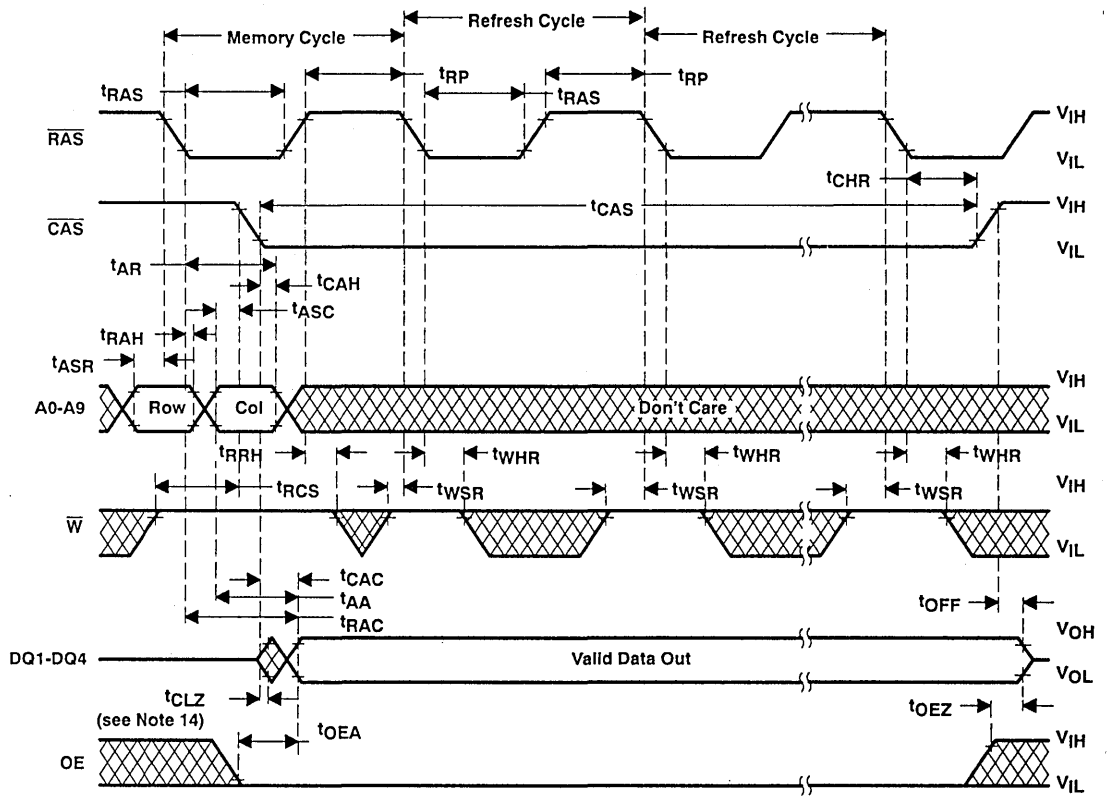
NOTE 15: Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 50 ns.

automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



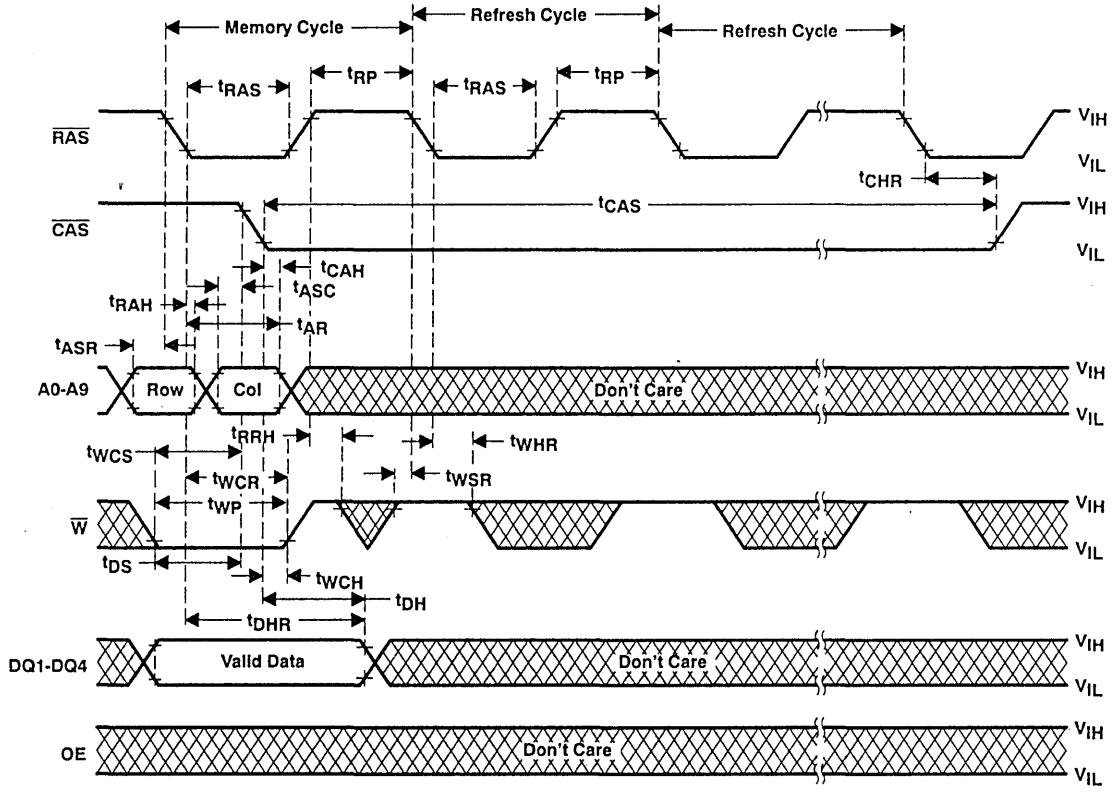
ADVANCE INFORMATION

hidden refresh cycle (read)



NOTE 14: Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.

hidden refresh cycle (write)



ADVANCE INFORMATION

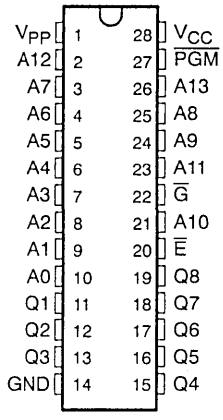
SGMS006C — AUGUST 1986 — REVISED JANUARY 1991

- **Military Operating Temperature Range . . . – 55°C to 125°C**
- **MIL-STD-883C Class B High-Reliability Processing**
- **Organization . . . 16K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 64K and 128K EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**

V_{CC} ± 5%	V_{CC} ± 10%	
'27C128-120		120 ns
	'27C128-15	150 ns
	'27C128-17	170 ns
	'27C128-20	200 ns
	'27C128-25	250 ns
	'27C128-30	300 ns

- **HVCMOS Technology**
- **3-State Output Buffer**
- **Low Power Dissipation**
  - **— Active . . . 138 mW Worst Case**
  - **— Standby . . . 1.7 mW Worst Case (CMOS-Input Levels)**

J Package
(Top View)



PIN NOMENCLATURE	
A0-A13	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12–13-V Power Supply

- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**

description

The SMJ27C128 series are 131 072-bit, ultraviolet-light erasable, electrically programmable read-only memory. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pullup resistors. The data outputs are three-state for connecting multiple devices to a common bus. The SMJ27C128 is pin compatible with 28-pin 128K ROMs and EPROMs. They are offered in a 600-mil dual-in-line ceramic package (J suffix) rated for operation from – 55°C to 125°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. These devices are programmable by either Fast or SNAP! Pulse programming algorithms. The Fast programming algorithm uses a V_{PP} of 12.5 V and a V_{CC} of 6 V for a nominal programming time of two minutes. The SNAP! Pulse programming algorithm uses a V_{PP} of 13.0 V and a V_{CC} of 6.5 V for a nominal programming time of two seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation for the SMJ27C128 listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V for Fast, or 13 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION (PINS)	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$ (22)	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X	V_{IH}	
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8 (11-13, 15-19)	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	83

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more SMJ27C128s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the selected SMJ27C128, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 through Q8.

latchup immunity

Latchup immunity on the SMJ27C128 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001; *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family,"* available through TI Field Sales Offices.

powerdown

Active I_{CC} supply current can be reduced from 25 mA to 500 μA (TTL-level inputs) or 300 μA (CMOS-level inputs) by applying a high input signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the SMJ27C128 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). EPROM erasure before programming is necessary to assure that all bits are in the logic 1 (high) state. Logic lows are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light. The recommended minimum exposure dose (UV intensity × exposure time) is 15 W•s/cm^2. A typical 12 mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SMJ27C128, the window should be covered with an opaque label.

SNAP! Pulse programming

The 128K EPROM can be programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which can reduce programming time to a nominal of two seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{PGM}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 μs followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V.

fast programming

The 128K EPROM can be programmed using the Fast programming algorithm illustrated by the flowchart in Figure 2. During Fast programming, data is presented in parallel (eight bits) on pins Q1 through Q8. Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{PGM}$ is pulsed. The programming mode is achieved when V_{PP} = 12.5 V, V_{CC} = 6 V, $\overline{G}$ = V_{IH}, $\overline{PGM}$ = V_{IL}, and $\overline{E}$ = V_{IL}. More than one SMJ27C128 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6 V and V_{PP} = 12.5 V. When the full Fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V (see Figure 2).

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL}, and $\overline{PGM}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10); i.e., A0 = V_{IL} accesses the manufacturer code, which is output on Q1-Q8; A0 = V_{IH} accesses the device code, which is output on Q1-Q8. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for these devices is 97, and the device code is 83.

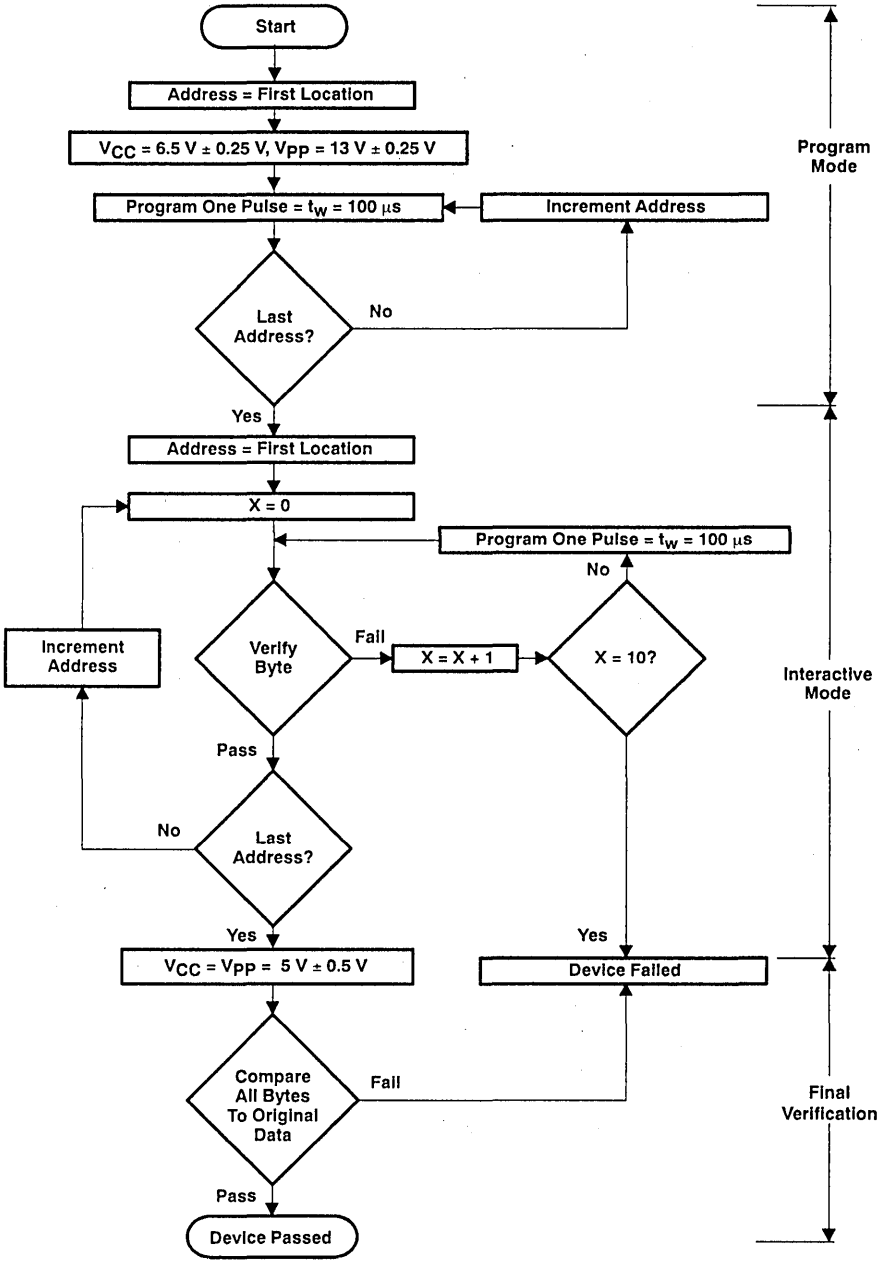


Figure 1. SNAP! Pulse Programming Flowchart

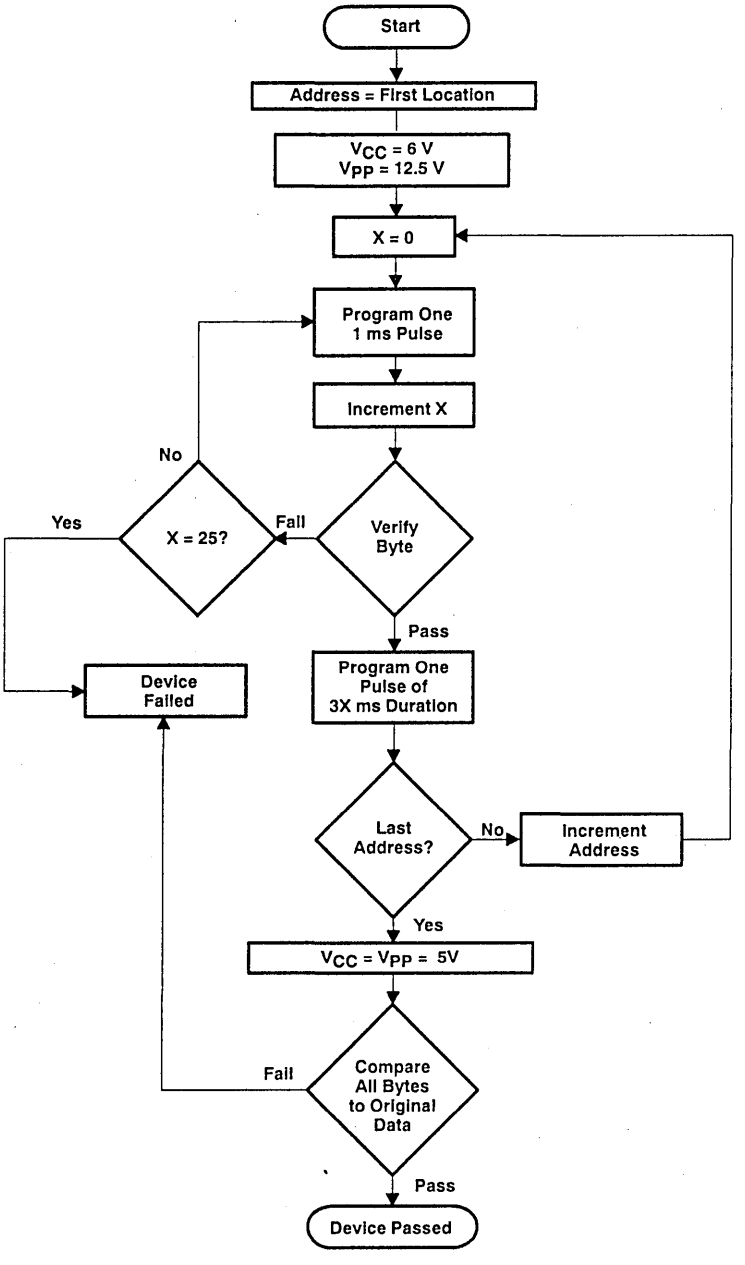
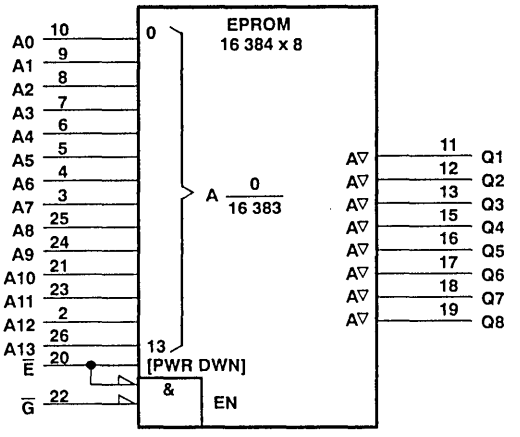


Figure 2. FAST Programming Flowchart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... – 0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... – 0.6 V to 6.5 V
A9 ..... – 0.6 V to 13.5 V
Output voltage range (see Note 1) ..... – 0.6 V to V_{CC} + 1 V
Minimum operating free-air temperature ..... – 55° C
Maximum operating case temperature ..... 125° C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				SMJ27C128-120			SMJ27C128-15 SMJ27C128-17 SMJ27C128-20 SMJ27C128-25 SMJ27C128-30			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)		4.75	5	5.25	4.5	5	5.5	V
		Fast programming algorithm		5.75	6	6.25	5.75	6	6.25	V
		SNAP! Pulse programming algorithm		6.25	6.50	6.75	6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode (see Note 3)		$V_{CC}-0.6$		$V_{CC}+0.6$	$V_{CC}-0.6$		$V_{CC}+0.6$	V
		Fast programming algorithm		12	12.5	13	12	12.5	13	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	12.75	13	13.25	V
V_{IH}	High-level input voltage		TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
			CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	V
V_{IL}	Low-level input voltage		TTL	−0.5		0.8	−0.5		0.8	V
			CMOS	−0.5		0.2	−0.5		0.2	V
T_A	Operating free-air temperature			−55			**−55**			°C
T_C	Operating case temperature					125			125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = -400\,\mu A$	2.4			V
V_{OL}	Low-level output voltage		$I_{OL} = 2.1$ mA			0.4	V
I_I	Input current (leakage)		$V_I = 0$ to 5.5 V			±1	µA
I_O	Output current (leakage)		$V_O = 0$ to V_{CC}			±1	µA
I_{PP1}	V_{PP} supply current		$V_{PP} = V_{CC} = 5.5$ V			100	µA
I_{PP2}	V_{PP} supply current‡ (during program pulse)		$V_{PP} = 13$ V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{IH}$			500	µA
		CMOS-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{CC}$			300	µA
I_{CC2}	V_{CC} supply current (active)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open		10	25	mA

† Typical values are at $T_A = 25°C$ and nominal voltages.
‡ This parameter has been characterized at 25°C and is not tested.

capacitance§

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	$V_I = 0$, f = 1 MHz		6	10	pF
C_O	Output capacitance	$V_O = 0$, f = 1 MHz		8	14	pF

† Typical values are at $T_A = 25°C$ and nominal voltages.
§ Capacitance measurements are made on sample basis only.

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C128-120		'27C128-15		'27C128-17		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	(see Figure 3)		120		150		170	ns
$t_{a(E)}$	Access time from chip enable			120		150		170	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		70		70	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	50	0	50	0	50	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C128-20		'27C128-25		'27C128-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	(see Figure 3)		200		250		300	ns
$t_{a(E)}$	Access time from chip enable			200		250		300	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		100		120	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	105	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

† Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

recommended timing requirements for programming: V_{CC} = 6 V and V_{PP} = 12.5 V (Fast) or V_{CC} = 6.5 and V_{PP} =13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

			MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	Fast programming algorithm	0.95	1	1.05	ms
		SNAP! Pulse programming algorithm	95	100	105	µs
$t_{w(FPGM)}$	Final pulse duration	Fast programming only	2.85		78.75	ms
$t_{su(A)}$	Address setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
t_{dis}	Output disable time from $\overline{G}$		0		130	ns
t_{enG}	Output enable time from $\overline{G}$				150	ns
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs

NOTES: 4. For all switching characteristics and timing measurements input pulse levels are 0.4 V to 2.4 V.
5. Common test conditions apply for t_{dis} except during programming.

PARAMETER MEASUREMENT INFORMATION

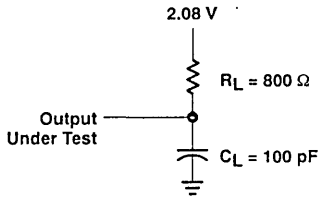
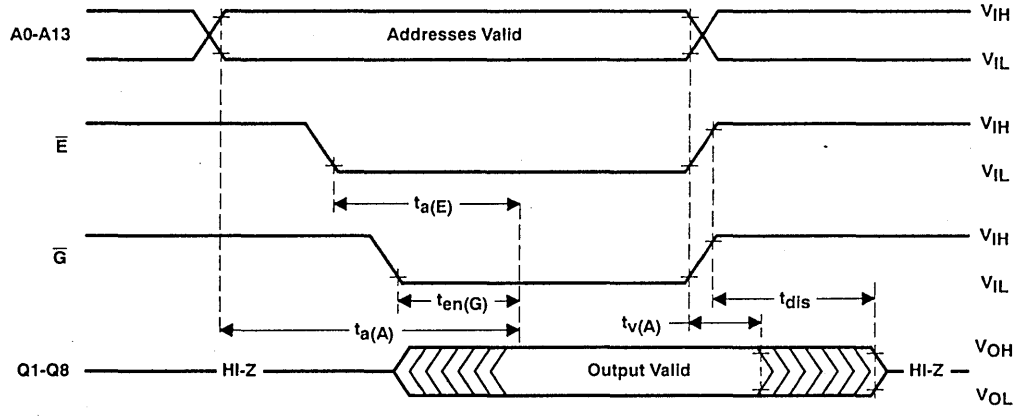
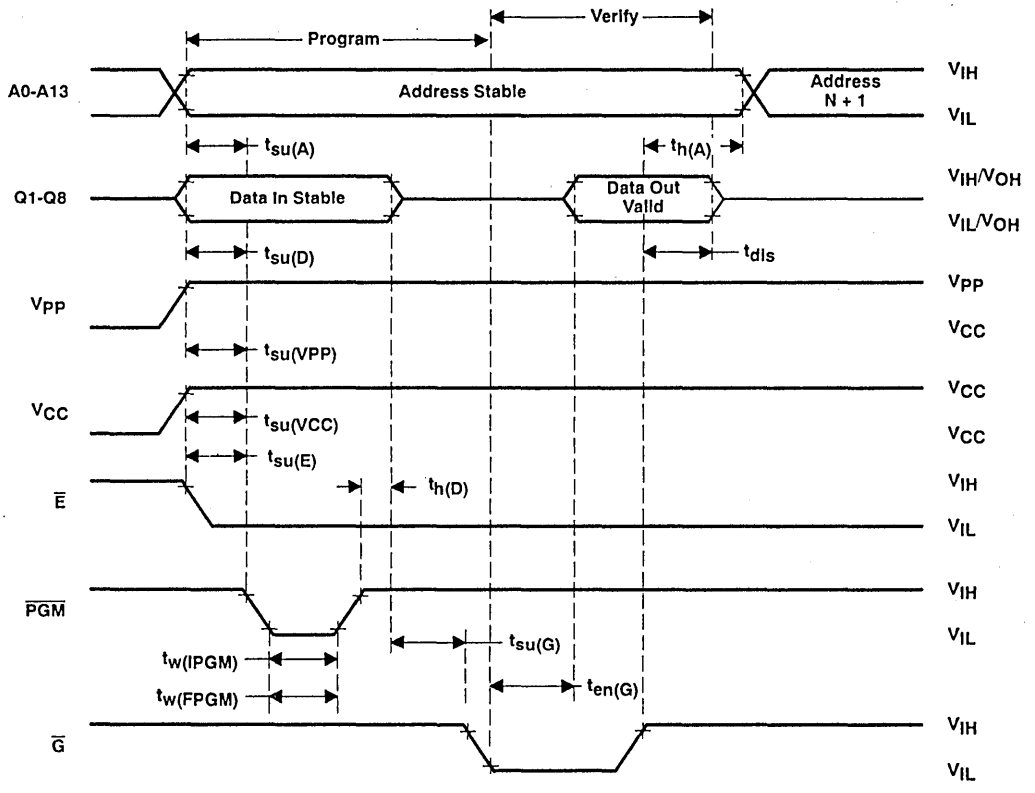


Figure 3. Output Load Circuit

read cycle timing



program cycle timing



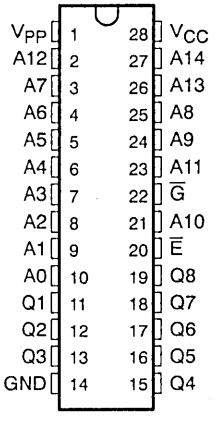
SGMS005C — MAY 1986 — REVISED JANUARY 1991

- **Military Operating Temperature Range . . . – 55°C to 125°C**
- **MIL-STD-883C Class B High-Reliabillity Processing**
- **Organization . . . 32K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 128K and 256K EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**

SMJ27C256-15	150 ns
SMJ27C256-17	170 ns
SMJ27C256-20	200 ns
SMJ27C256-25	250 ns
SMJ27C256-30	300 ns

- **HVCMOS Technology**
- **3-State Output Buffers**
- **400 mV Guaranteed DC Noise Immunity With Standard TTL Loads**
- **Low Power Dissipation**
  - **— Active . . . 138 mW Worst Case**
  - **— Standby . . . 1.7 mW Worst Case (CMOS Input Levels)**

J Package
(Top View)



PIN NOMENCLATURE	
A0-A14	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	Output Enable

description

The SMJ27C256 series are 262 144-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pullup resistors, and each output can drive one Series 54 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The SMJ27C256 is pin compatible with 28-pin 256K ROMs and EPROMs. They are offered in a 600 mil dual-in-line ceramic package (J suffix) rated for operation from – 55°C to 125°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other 12-13 V supply is needed for programming, but all programming signals are TTL level. These devices are programmable by either Fast or SNAP! Pulse programming algorithms. The Fast programming algorithm uses a V_{PP} of 12.5 V and a V_{CC} of 6 V for a nominal programming time of two minutes. The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of four seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation for the SMJ27C256 listed in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V for Fast, or 13 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION (PINS)	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$ (22)	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8 (11-13, 15-19)	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	04

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more SMJ27C256s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the selected SMJ27C256, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 through Q8.

latchup immunity

Latchup immunity on the SMJ27C256 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001; *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family."*

powerdown

Active I_{CC} supply current can be reduced from 25 mA to 500 μA (TTL-level inputs) or 300 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the SMJ27C256 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). EPROM erasure before programming is necessary to assure that all bits are in the logic 1 (high) state. Logic 0s (lows) are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light.The recommended minimum exposure dose (UV intensity × exposure time) is 15 W•s/cm^2. A typical 12 mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SMJ27C256, the window should be covered with an opaque label.

SNAP! Pulse programming

The 256K EPROM can be programmed using the TI SNAP! Pulse programming algorithm as illustrated by the flowchart in Figure 1, which can reduce programming time to a nominal of 4 seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{G}$ = V_{IH} and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V.

fast programming

The 256K EPROM can be programmed using the Fast programming algorithm illustrated by the flowchart in Figure 2. During Fast programming data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{E}$ is pulsed. The programming mode is achieved when V_{PP} = 12.5 V, V_{CC} = 6 V, $\overline{G}$ = V_{IH} and $\overline{E}$ = V_{IL}. More than one SMJ27C256 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Fast programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6 V and V_{PP} = 12.5 V. When the full Fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V (see Figure 2).

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G}$ = V_{IL}, and $\overline{E}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10); i.e., A0 = V_{IL} accesses the manufacturer code, which is output on Q1-Q8; A0 = V_{IH} accesses the device code, which is output on Q1-Q8. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for these devices is 97, and the device code is 04.

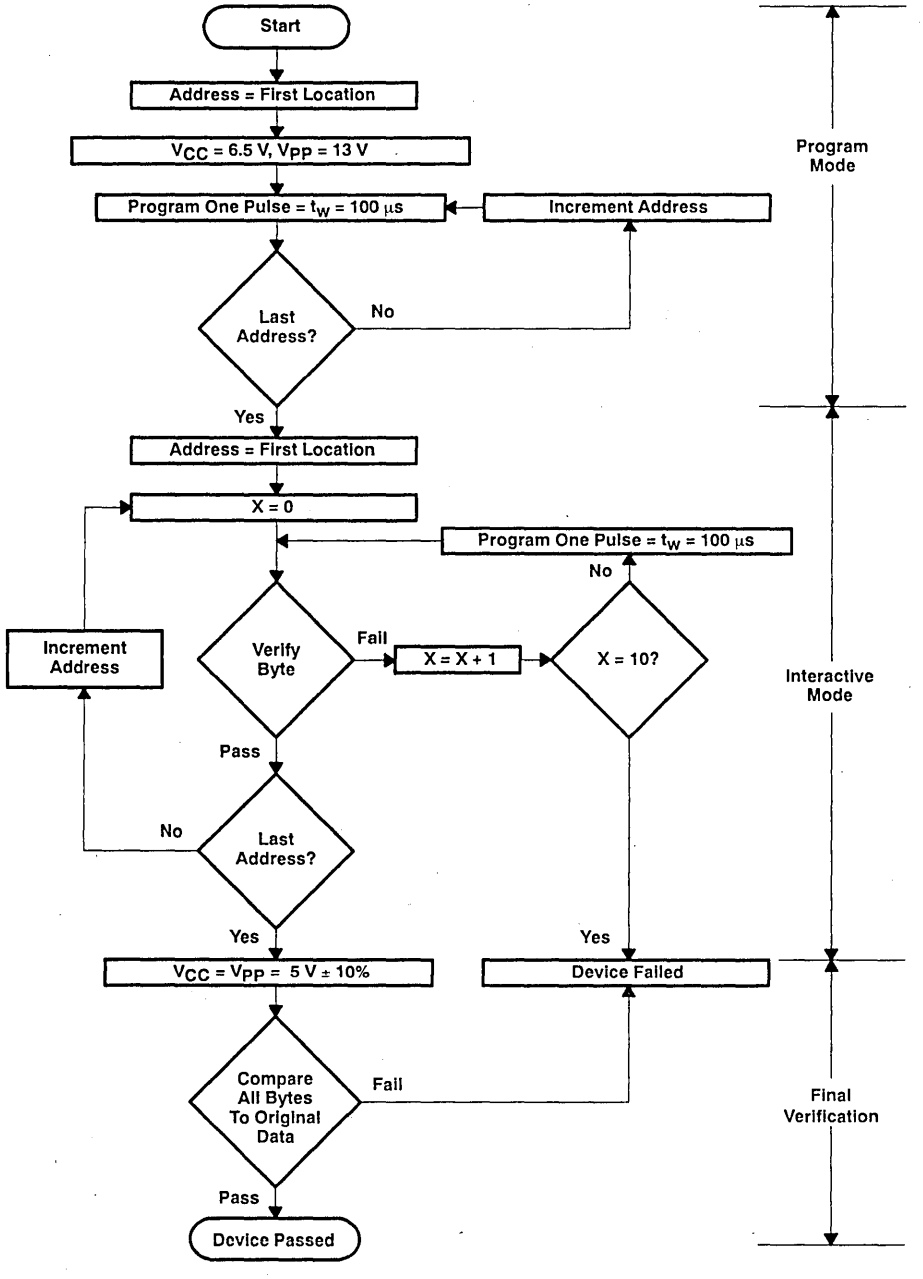


Figure 1. SNAP! Pulse Programming Flowchart

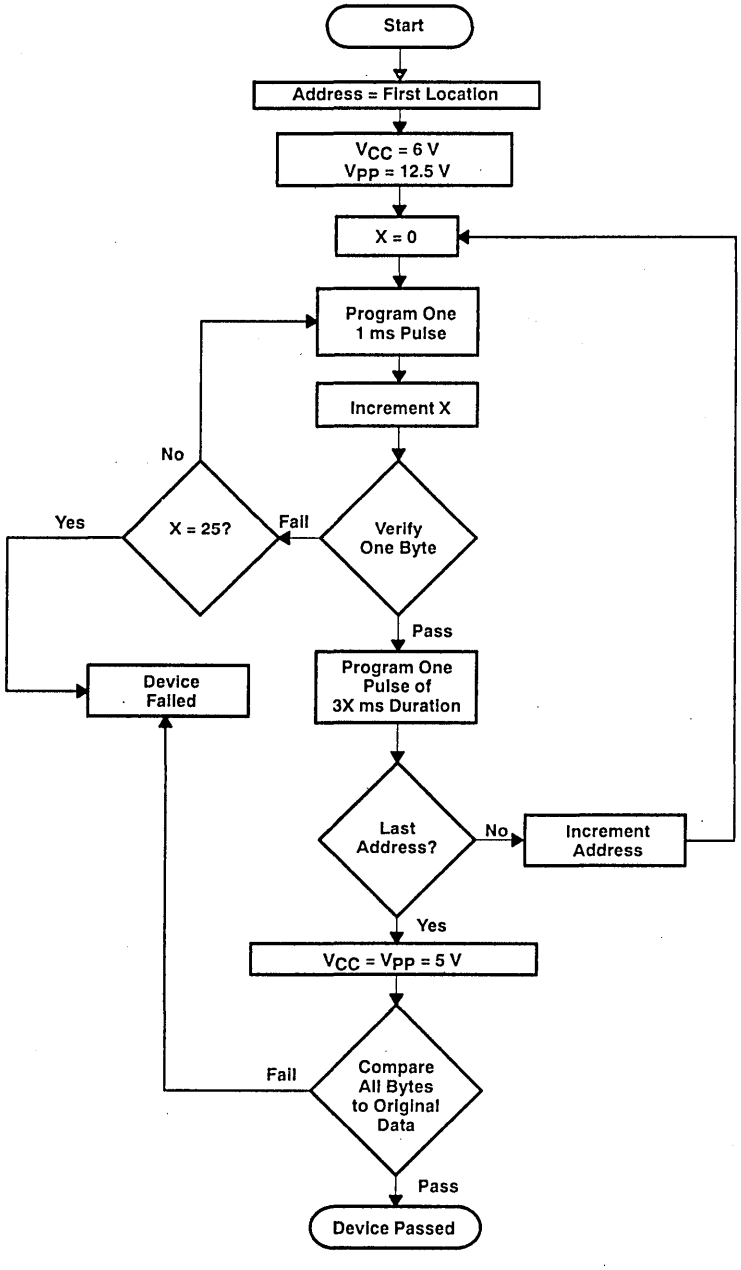
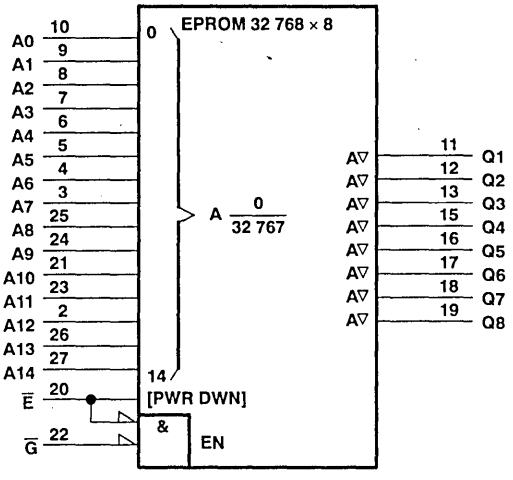


Figure 2. FAST Programming Flowchart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... – 0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... – 0.6 V to 6.5 V
A9 ..... – 0.6 V to 13.5 V
Output voltage range (see Note 1) ..... – 0.6 V to V_{CC} + 1 V
Minimum operating free-air temperature ..... – 55°C
Maximum operating case temperature ..... 125°C
Storage temperature range ..... – 65°C to 150°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	Read mode (see Note 2)	4.5	5	5.5	V
		Fast programming algorithm	5.75	6	6.25	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	V
V_{PP}	Supply Voltage	Read mode (see Note 3)	V_{CC} – 0.6		V_{CC} + 0.6	V
		Fast programming algorithm	12	12.5	13	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	V
V_{IH}	High-level input voltage (see Note 4)	TTL	2		V_{CC} + 1	V
		CMOS	V_{CC} – 0.2		V_{CC} + 0.2	V
V_{IL}	Low-level input voltage (see Note 4)	TTL	– 0.5		0.8	V
		CMOS	GND – 0.2		GND + 0.2	V
T_A	Operating free-air temperature		– 55			°C
T_C	Operating case temperature				125	°C

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (see Note 4)		I_{OH} = – 400 μA	2.4			V
V_{OL}	Low-level output voltage (see Note 4)		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage) (see Note 4)		V_I = 0 to 5.5 V			±1	μA
I_O	Output current (leakage)		V_O = 0 to V_{CC}			±1	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V			100	mA
I_{PP2}	V_{PP} supply current‡ (during program pulse) (see Note 4)		V_{PP} = 13 V		35	50	μA
I_{CC1}	V_{CC} supply curent (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			300	
I_{CC2}	V_{CC} supply current (active) (see Note 4)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		10	25	mA
I_{OS}	Output short circuit current (see Note 5)					100	mA

† Typical values are at T_A = 25°C and nominal voltages.

‡ This parameter has been characterized at 25°C and is not tested.

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}.
4. Valid during programming mode also.
5. V_{PP} may be one diode drop below V_{CC}. It may be connected to V_{CC}. Also, V_{CC} must be applied simultaneously or before V_{PP} and be removed simultaneously or after V_{PP}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		6	10	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz		10	14	pF

† Capacitance measurements are made on a sample basis only.
‡ Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 6 and 7)

PARAMETER		TEST CONDITIONS (SEE NOTES 6 AND 7)	'27C/PC256-15		'27C/PC256-17		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	(see Figure 3)		150		170	ns
$t_{a(E)}$	Access time from chip enable			150		170	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			70		70	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first §		0	55	0	55	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first §		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 6 AND 7)	'27C256-20		'27C256-25		'27C256-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	(see Figure 3)		200		250		300	ns
$t_{a(E)}$	Access time from chip enable			200		250		300	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		100		120	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first §		0	60	0	60	0	105	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first §		0		0		0		ns

§ Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

NOTES: 6. For all switching characteristics and timing measurements, input pulse levels are 0.4 V to 2.4 V.
7. Common test conditions apply to t_{dis} except during programming.

recommended timing requirements for programming: V_{CC} = 6 V and V_{PP} = 12.5 V (Fast) or V_{CC} = 6.5 and V_{PP} =13 (SNAP! Pulse), T_A = 25°C (see Note 6)

			MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	Fast programming algorithm	0.95	1	1.05	ms
		SNAP! Pulse programming algorithm	95	100	105	µs
$t_{w(FPGM)}$	Final pulse duration	Fast programming only	2.85		78.75	ms
$t_{su(A)}$	Address setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
t_{dis}	Output disable time from $\overline{G}$		0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$				150	ns
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs

NOTE 6: For all switching characteristics and timing measurements, the input pulse levels are 0.4 V to 2.4 V.

PARAMETER MEASUREMENT INFORMATION

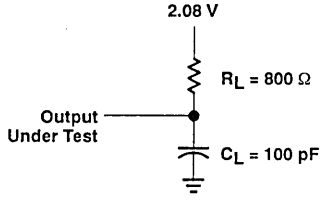
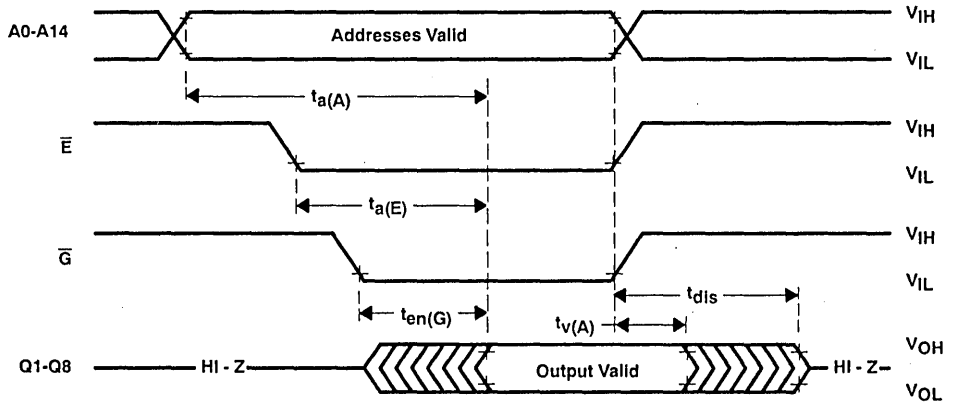
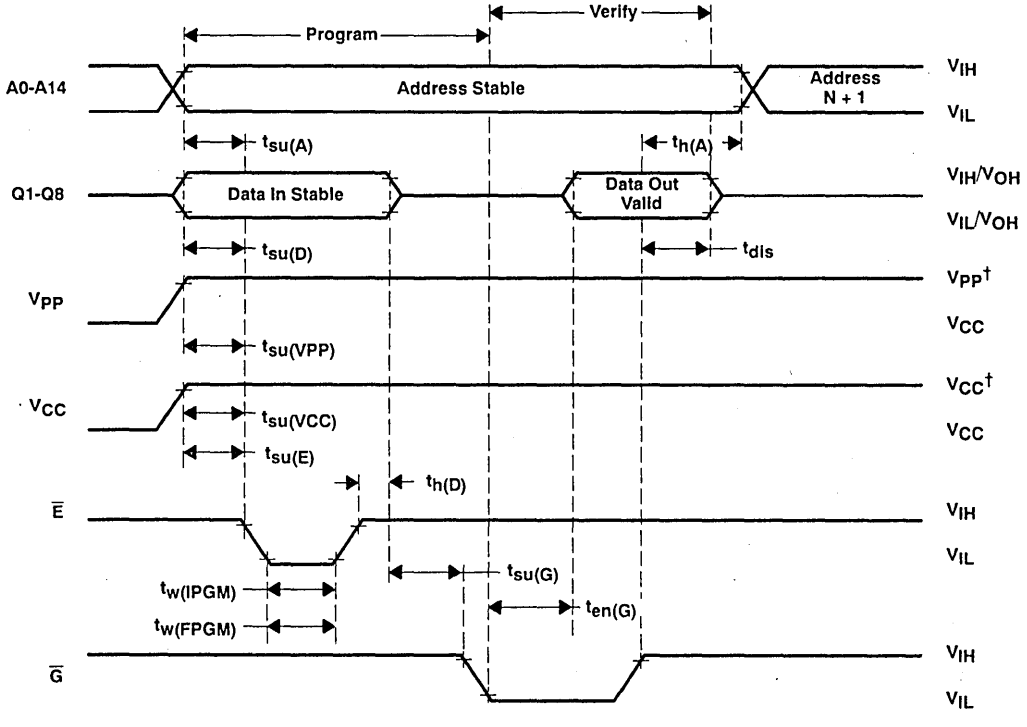


Figure 3. AC Testing Output Load Circuit

read cycle timing



program cycle timing



† 12.5-V V_{PP} and 6-V V_{CC} for Fast programming, 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

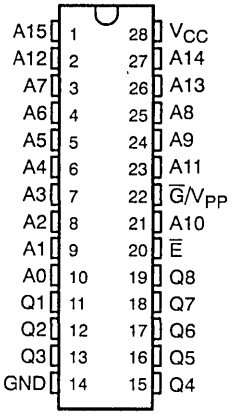
SGMS019A — SEPTEMBER 1987 — REVISED JANUARY 1991

- **Military Operating Temperature Range . . . – 55°C to 125°C**
- **MIL-STD-883C Class B High-Reliability Processing**
- **Organization . . . 64K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 512K EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**

'27C512-20	200 ns
'27C512-25	250 ns
'27C512-30	300 ns

- **HVCMOS Technology**
- **3-State Output Buffers**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Low Power Dissipation**
  - **— Active . . . 275 mW (Max)**
  - **— Standby . . . 1.9 mW (Max) (CMOS Input Levels)**

J Package
(Top View)



PIN NOMENCLATURE	
A0-A15	Address Inputs
$\overline{E}$	Chip Enable/Power Down
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
$\overline{G}/V_{PP}$	Output Enable
GND	Ground

description

The SMJ27C512 series are 524 288-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pullup resistors, and each output can drive one Series 54 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The SMJ27C512 is pin compatible with existing 28-pin 512K ROMs and EPROMs. They are offered in a 600-mil dual-in-line ceramic package (J suffix) rated for operation from –55°C to 125°C.

Since this EPROM operates from a single 5-V supply (in the read mode), it is ideal for use in microprocessor-based systems. One other 12-13 V supply is needed for programming, but all programming signals are TTL level. These devices are programmable by either Fast or SNAP! Pulse programming algorithms. Fast programming uses a V_{PP} of 12.5 V and a V_{CC} of 6 V for a nominal programming time of two minutes. SNAP! Pulse programming uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of four seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation for the SMJ27C512 listed in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V for Fast, or 13 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION (PINS)	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}/V_{PP}$ (22)	V_{IL}	V_{IH}	X†	V_{PP}	V_{IL}	V_{PP}	V_{IL}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8 (11-13, 15-19)	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	85

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more SMJ27C512s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the selected SMJ27C512, a low-level signal is applied to the $\overline{E}$ and $\overline{G}/V_{PP}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 through Q8.

power down

Active I_{CC} supply current can be reduced from 25 mA to 500 μA (TTL-level inputs) or 350 μA (CMOS-level inputs) by applying a high logic signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the SMJ27C512 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). EPROM erasure before programming is necessary to assure that all bits are in the logic 1 (high) state. Logic 0's (lows) are programmed into the desired locations. A programmed logic 0 (low) can be erased only by ultraviolet light. The recommended minimum ultraviolet light exposure dose (UV intensity × exposure time) is 15 W•s/cm^2. A typical 12 mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SMJ27C512, the window should be covered with an opaque label.

SNAP! Pulse programming

The 512K EPROM can be programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which can reduce programming time to a nominal of four seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved with $\overline{G}/V_{PP}$ = 13 V, V_{CC} = 6.5 V, and $\overline{E} = V_{IL}$. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = 5 V, $\overline{G}/V_{PP} = V_{IL}$, and $\overline{E} = V_{IL}$.

fast programming

The 512K EPROM can be programmed using the Fast programming algorithm illustrated by the flowchart in Figure 2. During Fast programming, data is presented in parallel (eight bits) on pins Q1 through Q8. Once addresses and data are stable, $\overline{E}$ is pulsed. The programming mode is achieved when $\overline{G}/V_{PP}$ = 12.5 V, V_{CC} = 6 V, and $\overline{E} = V_{IL}$. More than one SMJ27C512 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6 V. When the full Fast programming routine is complete, all bits are verified with V_{CC} = 5 V (see Figure 2).

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified with $\overline{G}/V_{PP}$ and $\overline{E} = V_{IL}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10); i.e., A0 = V_{IL} accesses the manufacturer code, which is output on Q1-Q8; A0 = V_{IH} accesses the device code, which is output on Q1-Q8. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for these devices is 97, and the device code is 85.

latchup immunity

Latchup immunity on the SMJ27C512 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family"*, available through TI Sales Offices.

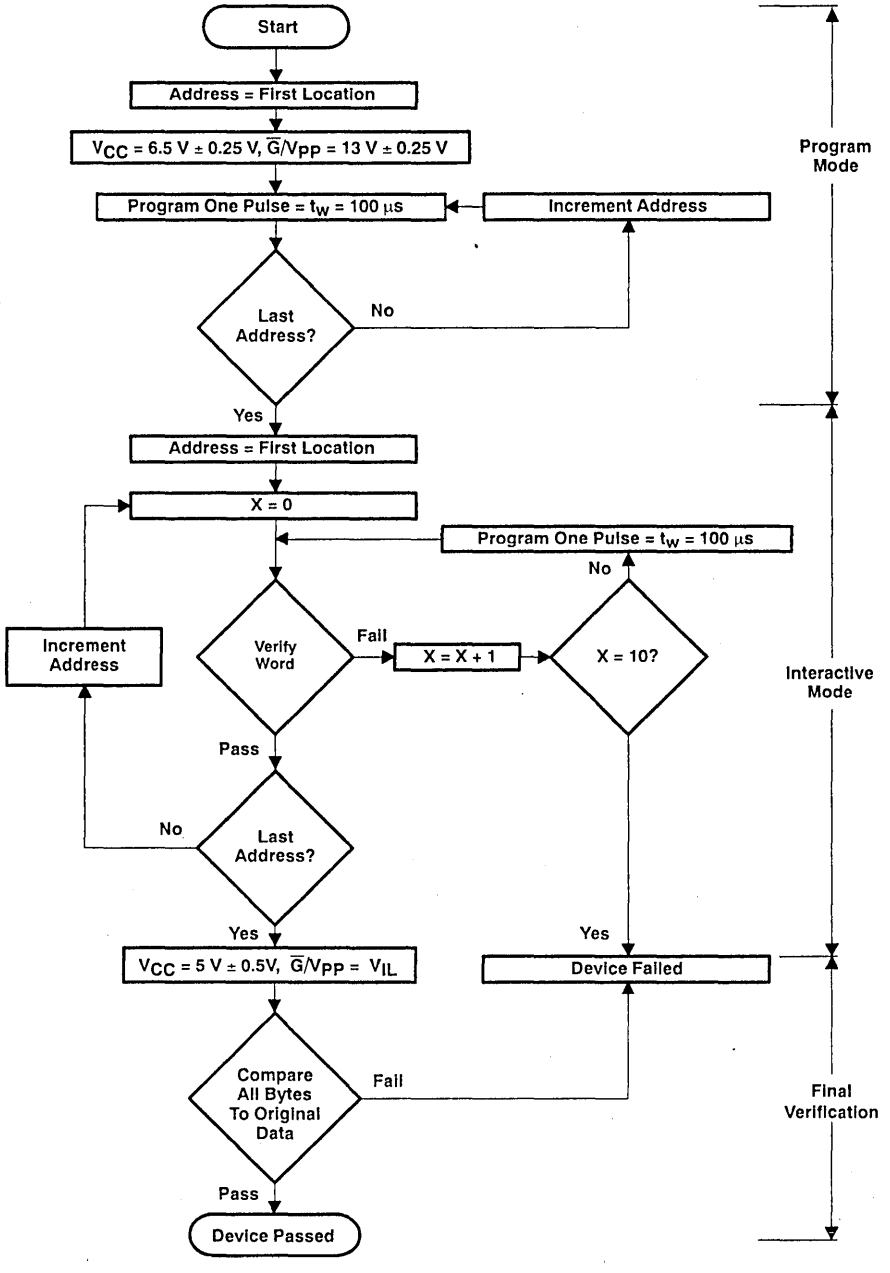


Figure 1. SNAP! Pulse Programming Flowchart

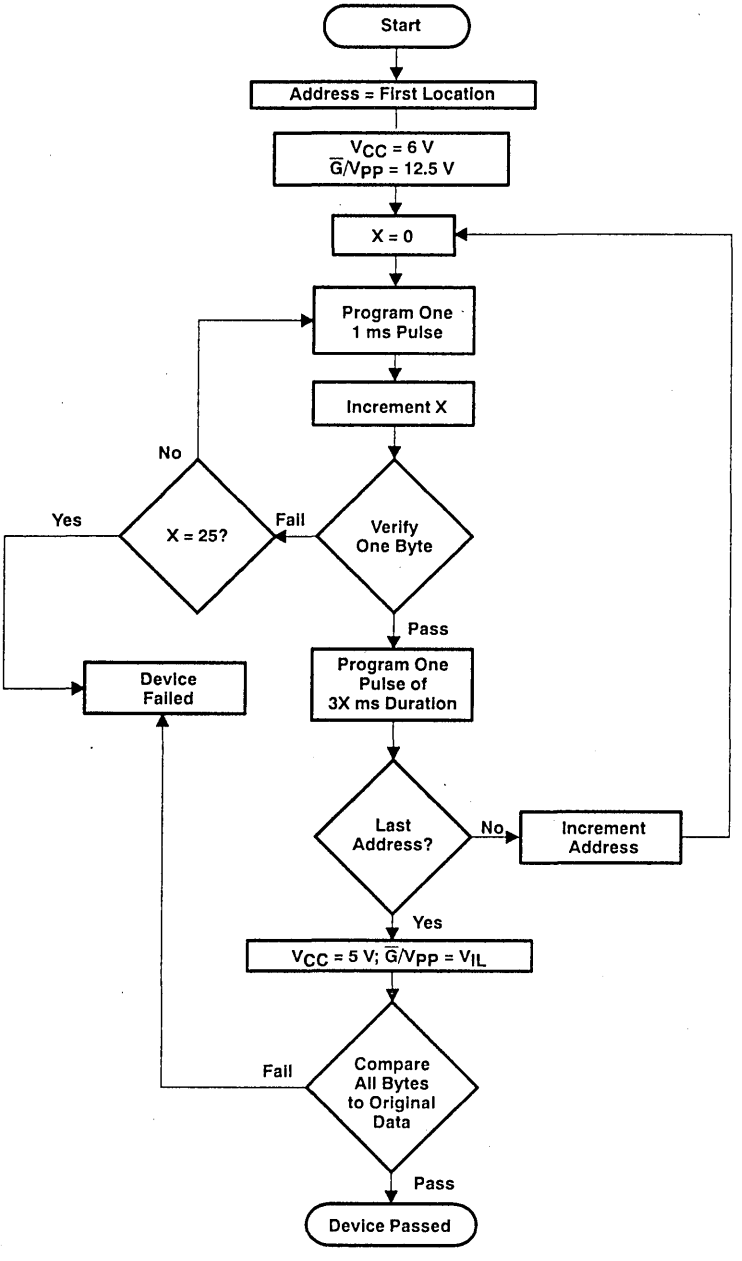
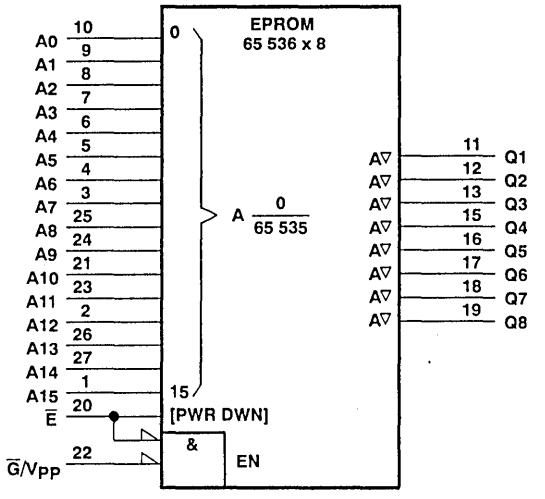


Figure 2. FAST Programming Flowchart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} ..... – 0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... – 0.6 V to 6.5 V
A9 ..... – 0.6 V to 13.5 V
Output voltage range (see Note 1) ..... – 0.6 V to V_{CC} + 1 V
Minimum operating free-air temperature ..... – 55°C
Maximum operating case temperature ..... 125°C
Storage temperature range ..... – 65°C to 150°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			SM/SMJ27C512-20 SM/SMJ27C512-25 SM/SMJ27C512-30			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)	Read mode	4.75	5	5.25	V
		Fast programming algorithm	5.75	6	6.25	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	V
$\overline{G}/V_{PP}$	Supply voltage (see Note 3)	Fast programming algorithm	12	12.5	13	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	V
		CMOS	GND − 0.2		GND + 0.2	V
T_A	Operating free-air temperature		−55			°C
T_C	Operating case temperature				125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as $\overline{G}/V_{PP}$ and removed after or at the same time as $\overline{G}/V_{PP}$. The device must not be inserted into or removed from the board when $\overline{G}/V_{PP}$ or V_{CC} is applied.

3. $\overline{G}/V_{PP}$ can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level ouput voltage		$I_{OH} = -400\mu A$	2.4			V
V_{OL}	Low-level ouput voltage		$I_{OL} = 2.1$ mA			0.4	V
I_I	Input current (leakage)		$V_I = 0$ to 5.5 V			±10	μA
I_O	Output current (leakage)		$V_O = 0$ to V_{CC}			±10	μA
I_{PP}	$\overline{G}/V_{PP}$ supply current (during program pulse)		$\overline{G}/V_{PP} = 13$ V		35	70	mA
I_{CC1}	V_{CC} supply current (standyby)	TTL-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{IH}$			500	μA
		CMOS-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{CC}$			350	μA
I_{CC2}	V_{CC} supply current (active)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open		35	50	mA

† Typical values are at $T_A = 25°C$ and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	UNIT
C_i	Input capacitance	$V_I = 0$, f = 1 MHz		6	pF
C_O	Output capacitance	$V_O = 0$, f = 1 MHz		8	pF
$C_{G/VPP}$	$\overline{G}/V_{PP}$ input capacitance	$\overline{G}/V_{PP} = 0$, f = 1 MHz		20	pF

† Typical values are at $T_A = 25°C$ and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 4)

PARAMETER		TEST CONDITIONS (SEE NOTE 4)	'27C512-20		'27C512-25		'27C512-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	(see Figure 3)		200		250		300	ns
$t_{a(E)}$	Access time from chip enable			200		250		300	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		100		120	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	105	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

† Value calculated from 0.5 V delta to measured level.

recommended timing requirements for programming: V_{CC} = 6 V and V_{PP} = 12.5 V (Fast) or V_{CC} = 6.5 and V_{PP} =13 (SNAP! Pulse), T_A = 25°C (see Note 4)

			MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	Fast programming algorithm	0.95	1	1.05	ms
		SNAP! Pulse programming algorithm	95	100	105	µs
$t_{w(FPGM)}$	Final pulse duration	Fast programming only	2.85		78.75	ms
$t_{su(A)}$	Address setup time		2			µs
$t_{dis(G)}$	Output disable time from $\overline{G}$		0		130	µs
t_{EHD}	Data valid from $\overline{E}$ low				1	µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs
$t_{r(PG)G}$	V_{PP} rise time		50			ns
$t_{h(VPP)}$	V_{PP} hold time		2			µs
$t_{rec(PG)}$	V_{PP} recovery time		2			µs

NOTE 4: For all switching characteristics and timing measurements input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference page 9-109, AC testing waveforms).

PARAMETER MEASUREMENT INFORMATION

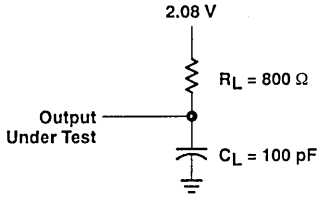
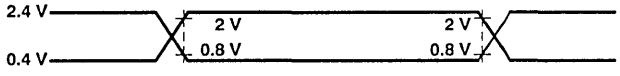


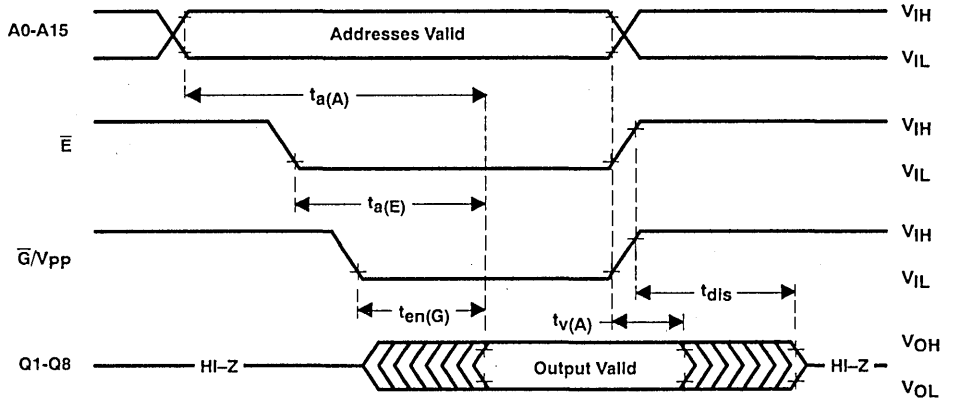
Figure 3. AC Testing Output Load Circuit

AC testing input/output wave forms

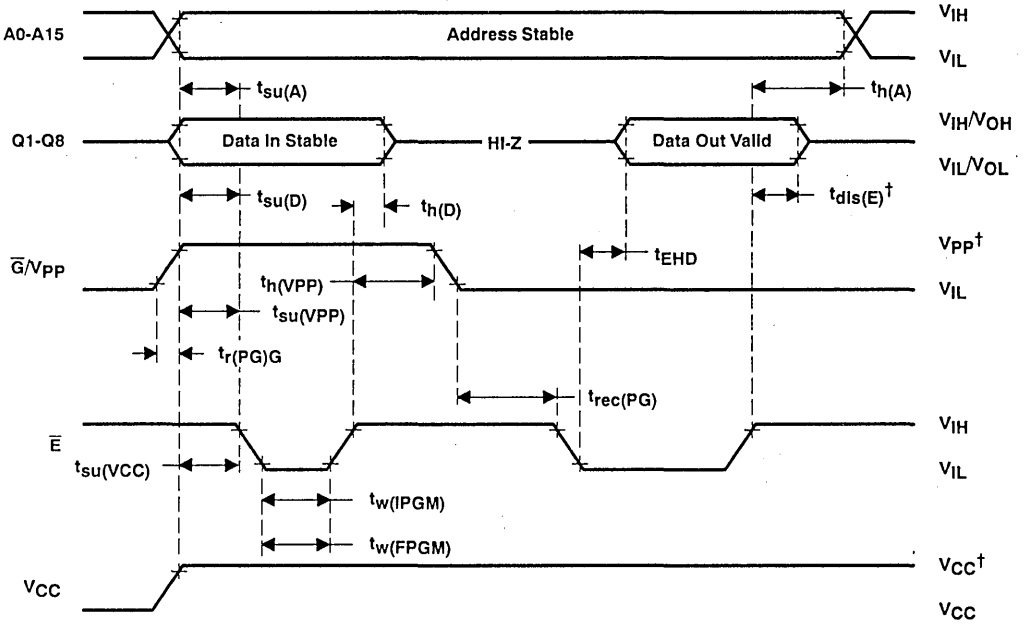


A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low.

read cycle timing



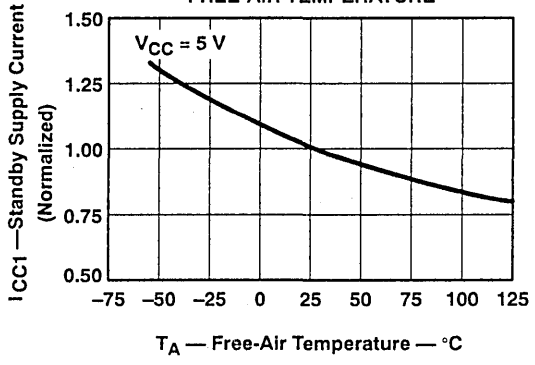
program cycle timing



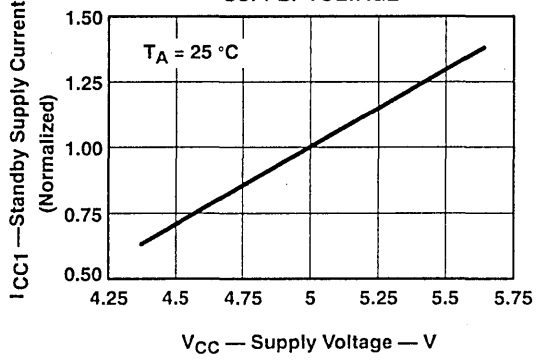
† 12.5-V V_{PP} and 6-V V_{CC} for Fast programming, 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

TYPICAL CHARACTERISTICS

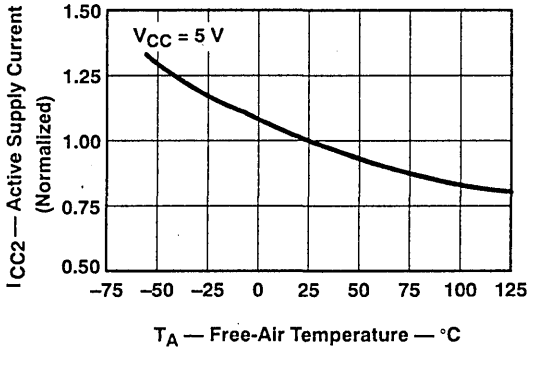
STANDBY SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



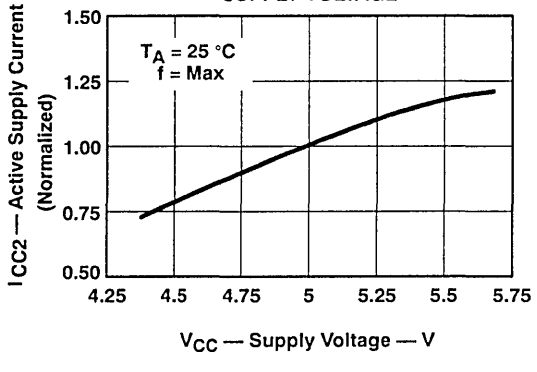
STANDBY SUPPLY CURRENT
vs
SUPPLY VOLTAGE



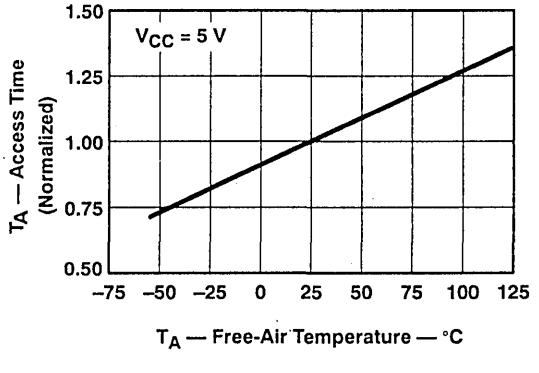
ACTIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



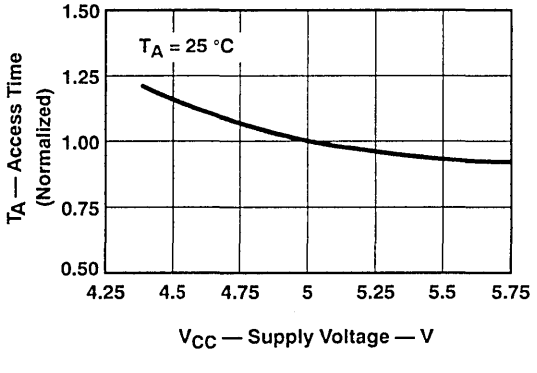
ACTIVE SUPPLY CURRENT
vs
SUPPLY VOLTAGE



ACCESS TIME
vs
FREE-AIR TEMPERATURE



ACCESS TIME
vs
SUPPLY VOLTAGE

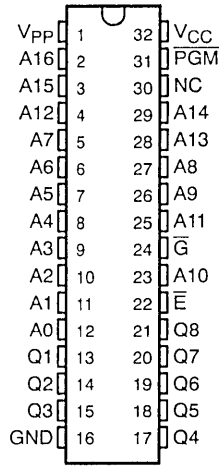


- Military Operating Temperature Range
  . . . – 55° C to 125°C
- Organization . . . 128K × 8
- Single 5-V Power Supply
- Industry Standard 32-Pin Dual-In-line Package
- All Inputs/Outputs Fully TTL Compatible
- Static Operations (No Clocks, No Refresh)
- Max Access/Min Cycle Time
  V_{CC} ± 10%

SMJ27C010-17	170 ns
SMJ27C010-20	200 ns
SMJ27C010-25	250 ns

- 8-Bit Output For Use in Microprocessor-Based Systems
- 32-Bit Programming (Four Bytes) and Standard 8-Bit Programming
- Power Saving CMOS Technology
- 3-State Output Buffers
- 400-mV Minimum DC Noise Immunity With Standard TTL Loads
- No Pullup Resistors Required

J Package
(Top View)



PIN NOMENCLATURE	
A0-A16	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No External Connection
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Supply
V_{PP}	12.5-V Supply†

† Only in program mode.

PRODUCT PREVIEW

description

The SMJ27C010 series are 1 048 576-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits. Each output can drive one Series 54 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The SMJ27C010 is offered in a 600-mil dual-in-line cerdip package (J suffix) rated for operation from – 55°C to 125°C.

Since these EPROMs operate from a single-5 V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5-V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

SMJ27C210
1 048 576-BIT UV
ERASABLE PROGRAMMABLE READ-ONLY MEMORY

SMGS028A — MARCH 1988 — REVISED NOVEMBER 1990

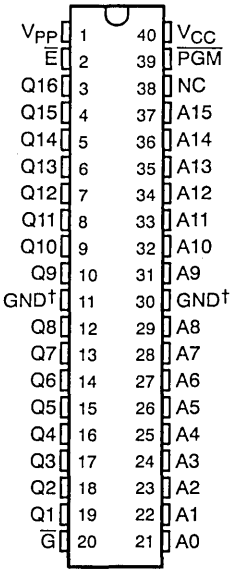
- Wide-Word Organization . . . 64K × 16
- Single 5-V Power Supply
- Operationally Compatible With Existing Megabit EPROMs
- 40-Pin Dual-In-line Package
- All Inputs and Outputs Fully TTL Compatible
- Static Operations (No Clocks, No Refresh)
- Max Access/Min Cycle Time

  V_{CC} ± 10%

SMJ27C210-12	120 ns
SMJ27C210-15	150 ns
SMJ27C210-17	170 ns
SMJ27C210-20	200 ns
SMJ27C210-25	250 ns

- 16-Bit Output For Use in Microprocessor-Based Systems
- 32-Bit Programming (Two 16-Bit Words) and 16-Bit Programming
- 16 Seconds Typical Programming Time
- Power Saving CMOS Technology
- 3-State Output Buffers
- 400-mV Minimum DC Noise Immunity With Standard TTL Loads
- Latchup Immunity of 250 mA on All Input and Output Pins
- No Pullup Resistors Required
- Low Power Dissipation
  - Active . . . 220 mW Worst Case
  - Standby . . . 1.5 mW Worst Case (CMOS-Input Levels)
- Operating Temperature Range . . . – 55° C to 125°C

J Package
(Top View)



PIN NOMENCLATURE	
A0-A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
Q1-Q16	Outputs
V_{CC}	5-V Supply
V_{PP}	12.5-V Supply‡

† Pins 11 and 30 must be connected externally to ground.
‡ Only in program mode.

PRODUCT PREVIEW

description

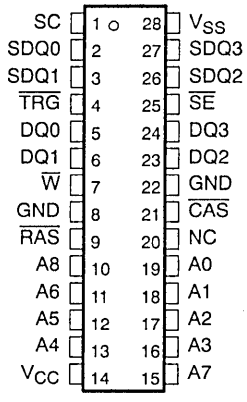
The SMJ27C210 is a 1 048 576-bit, ultraviolet-light erasable, electrically programmable read-only memory. This device is fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pullup resistors and each output can drive one Series 54 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The SMJ27C210 is offered in a 600-mil dual-in-line cerdip package (J suffix) rated for operation from – 55°C to 125°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

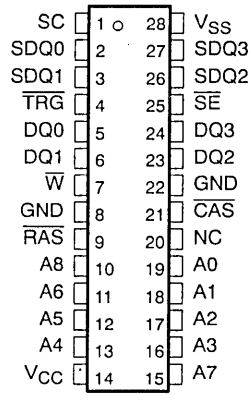
- Military Operating Temperature Range . . . – 55°C to 125°C
- Class B High-Reliability Processing
- DRAM: 262 144 Words × 4 Bits
  SAM: 512 Words × 4 Bits
- Dual Port Accessibility — Simultaneous and Asynchronous Access from the DRAM and SAM Ports
- Bidirectional Data Transfer Function Between the DRAM and the Serial Data Register
- Write Per Bit Feature for Selective Write to Each RAM I/O.
- Enhanced Page Mode Operation for Faster Access
- $\overline{CAS}$-before-$\overline{RAS}$ and Hidden Refresh Modes
- RAM Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design
- Long Refresh Period . . . Every 8 ms (Max)
- Up to 33 MHz Uninterrupted Serial Data Streams
- 3-State Serial I/Os Allow Easy Multiplexing of Video Data Streams
- 512 Selectable Serial Register Starting Locations
- Texas Instruments EPIC™ CMOS Process
- Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX) $t_{a(R)}$	ACCESS TIME COLUMN ENABLE (MAX) $t_{a(C)}$	ACCESS TIME SERIAL DATA (MAX) $t_{a(SC)}$	ACCESS TIME SERIAL ENABLE (MAX) $t_{a(SE)}$	V_{CC} TOLERANCE
'44C250-1	100 ns	25 ns	30 ns	20 ns	±5%
'44C250-2	120 ns	30 ns	35 ns	25 ns	±5%
'44C250-10	100 ns	25 ns	30 ns	20 ns	±10%
'44C250-12	120 ns	30 ns	35 ns	25 ns	±10%

JD Package† (Top View)



HJ Package† (Top View)



†The packages shown here are for pinout reference only and are not drawn to scale.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column Enable
DQ0-DQ3	DRAM Data In-Out/Write Mask Bit
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row Enable
SC	Serial Data Clock
SDQ0-SDQ3	Serial Data In-Out
$\overline{TRG}$	Transfer Register/Q Output Enable
$\overline{W}$	Write Mask Select/Write Enable
NC	No Connection
V_{CC}	5-V Supply
V_{SS}	Ground
GND	Ground (Important: not connected to internal V_{SS})

- Packaging Options
  - — 28-pin Ceramic Side Brazed DIP (JD suffix)
  - — 28-pin Ceramic Small Outline J-Leaded Chip Carrier (HJ Suffix)

NOTE: All references to the SMJ44C250-10, -1 are Advance Information Only.

EPIC is a trademark of Texas Instruments Incorporated.

description

The SMJ44C250 Multiport Video RAM is a high speed, dual ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 4 bits each, interfaced to a serial data register, or Serial Access Memory (SAM), organized as 512 words of 4 bits each. The SMJ44C250 supports three basic types of operation: random access to and from the DRAM, serial access to and from the serial register, and bidirectional transfer of data between any row in the DRAM and the serial register. Except during transfer operations, the SMJ44C250 can be accessed simultaneously and asynchronously from the DRAM and SAM ports. During a transfer operation, the 512 columns of the DRAM are connected to the 512 positions in the serial data register. The 512 × 4 bit serial data register can be loaded from the memory row (transfer read) or else the contents of the 512 × 4 bit serial data register can be written to the memory row (transfer write).

The SAM can also be configured in input mode, accepting serial data from an external device. Once the serial register within the SAM is loaded, its contents can be transferred to the corresponding column positions in any row in memory in a single memory cycle. The SAM port is designed for maximum performance. Data can be input to or accessed from the SAM at serial rates up to 33 MHz.

All address lines and data-in are latched on-chip to simplify system design. All data-outs are unlatched to allow greater system flexibility.

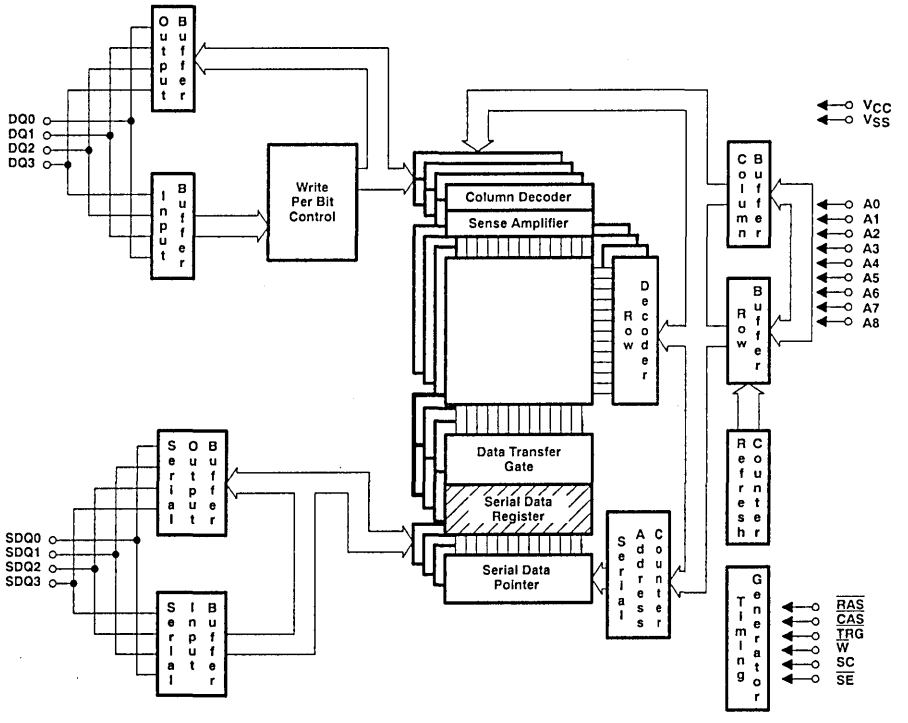
The SMJ44C250 employs state-of-the-art Texas Instruments EPIC™ scaled CMOS, double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The SMJ44C250 is offered both in a 28-pin, ceramic small-outline J-leaded package (HJ suffix) for direct surface mounting in rows on 400-mil centers. It is also offered in a 400-mil, 28-pin ceramic sidebrazed dual-in-line package (JD suffix). Both packages are characterized for operation from – 55°C to 125°C (M suffix).

The SMJ44C250 and other SMJ44C25X multiport Video RAMs are supported by a broad line of video/graphic processors from Texas Instruments, including the SMJ34010 and the SMJ34020 Graphics System Processors.

NOTE: All references to the SMJ44C250-10, -1 are Advance Information.

functional block diagram



Detailed Pin Description vs Operational Mode

PIN	DRAM	TRANSFER	SAM
A0-A8	Row, Column Address	Row, Tap Address	
$\overline{CAS}$	Column Enable, Output Enable	Tap Address Strobe	
DQi	DRAM Data I/O, Write Mask Bits		
$\overline{RAS}$	Row Enable	Row Enable	
$\overline{SE}$		Serial-In Mode Enable	Serial Enable
SC			Serial Clock
SDQi			Serial Data I/O
$\overline{TRG}$	Q Output Enable	Transfer Enable	
$\overline{W}$	Write Enable, Write per Bit Select	Transfer Write Enable	
V_{CC}	5-V Supply (typical)		
V_{SS}	Device Ground		
GND	System Ground		
NC	Make no external connection		

operation

random access operation

Refer to Table 1, Functional Table, for Random Access and Transfer Operations. Random access operations are denoted by the designator "R" and transfer operations are denoted by a " T."

transfer register select and DQ enable ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either register or random access operation as $\overline{RAS}$ falls. For random access (DRAM) mode, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. Asserting $\overline{TRG}$ high as $\overline{RAS}$ falls causes the 512 storage elements of each data register to remain disconnected from the corresponding 512-bit lines of the memory array. (Asserting $\overline{TRG}$ low as $\overline{RAS}$ falls connects the 512-bit positions in the serial register to the bit lines and indicates that a transfer will occur between the data registers and the selected memory row. See "Transfer Operation" for details.)

During random access operations, $\overline{TRG}$ also functions as an output enable for the random (Q) outputs. Whenever $\overline{TRG}$ is held high, the Q outputs are in the high-impedance state to prevent an overlap between the address and DRAM data. This organization allows the connection of the address lines to the data I/O lines but prohibits the use of the early write cycle. It also allows read-modify-write cycles to be performed by providing a three-state condition to the common I/O pins so that write data can be driven onto the pins after output read data has been externally latched.

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Then the nine column address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

$\overline{RAS}$ and $\overline{CAS}$ address strobes and device control clocks

$\overline{RAS}$ is a control input that latches the states of the row address, $\overline{W}$, $\overline{TRG}$, $\overline{SE}$, and $\overline{CAS}$, onto the chip to invoke the various DRAM and Transfer functions of the SMJ44C250. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is a control input that latches the states of the column address. $\overline{CAS}$ also acts as an output enable for the DRAM output pins.

write enable, write-per-bit enable ($\overline{W}$)

The $\overline{W}$ pin enables data to be written to the DRAM and is also used to select the DRAM write-per-bit mode of operation. A logic high level on the $\overline{W}$ input selects the read mode and logic low level selects the write mode. In an early write cycle, $\overline{W}$ is brought low before $\overline{CAS}$ and the DRAM output pins (DQ) remain in the high-impedance state for the entire cycle. During DRAM write cycles, holding $\overline{W}$ low on the falling edge of $\overline{RAS}$ will invoke the write-per-bit operation.

A four-bit binary code (the write-per-bit mask) is input to the device via the random DQ pins and is latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the four random I/Os are written and which are not. After $\overline{RAS}$ has latched the write mask on-chip, input data is driven onto the DQ pins and is latched on the falling edge of the later of $\overline{CAS}$ or $\overline{W}$. If a 0 (low) was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will not be written to that I/O. If a 1 (high) was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will be written to that I/O.

See the corresponding timing diagrams for details.

IMPORTANT: The write-per-bit operation is invoked only if $\overline{W}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{W}$ is held high on the falling edge of $\overline{RAS}$, write-per-bit is not enabled and the write operation is identical to that of standard × 4 DRAMs.

data I/O (DQ0-DQ3)

DRAM data is written during a write or read-modify-write cycle. The falling edge of $\overline{W}$ strobes data into the on-chip data latches. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with data setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low. Thus, the data will be strobed-in by $\overline{W}$ with data setup and hold times referenced to this signal.

The three-state output buffers provide direct TTL compatibility (no pullup resistors required) with a fanout of two Series 74/54 TTL loads. Data-out is the same polarity as data-in. The outputs are in the high impedance (floating) state as long as $\overline{CAS}$ or $\overline{TRG}$ is held high. Data will not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low. Once the outputs are valid, they remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. $\overline{CAS}$ or $\overline{TRG}$ going high returns the outputs to a high-impedance state. In an early write cycle, the outputs are always in the high-impedance state. In a register transfer operation (memory to register or register to memory), the outputs remain in the high-impedance state for the entire cycle.

enhanced page mode

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ44C250 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

Enhanced page mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row address setup, row address hold, and address multiplex is thus eliminated, and a memory cycle time reduction of up to 3 × can be achieved, compared to minimum $\overline{RAS}$ cycle times. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and page mode cycle time used. The SMJ44C250 allows a full page (512 cycles) of information to be accessed in read, write, or read-modify-write mode during a single $\overline{RAS}$ low period using relatively conservative page mode cycle times.

refresh

A refresh operation must be performed to each row at least once every eight milliseconds to retain data. Since the output buffer is in the high-impedance state (unless $\overline{CAS}$ is applied), the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$. The external row address is ignored and the refresh address is generated internally.

GND

This pin is reserved for the manufacturer's test operation. It is an input and should be tied to system ground.

IMPORTANT: GND is not connected internally to V_{SS}.

Table 1. Functional Table

TYPE†	RAS FALL				ADDRESS		DQ0-DQ3		FUNCTION
	CAS	TRG	W	SE	RAS	CAS	RAS	CAS‡ W‡	
R	L	X§	X	X	X	X	X	X	CAS-Before-RAS Refresh
T	H	L	L	L	Row Addr	Tap Point	X	X	Register to Memory Transfer (Transfer Write)
T	H	L	L	H	Refresh Addr	Tap Point	X	X	Serial Write-mode Enable (Pseudo-Transfer Write)
T	H	L	H	X	Row Addr	Tap Point	X	X	Memory to Register Transfer (Transfer Read)
R	H	H	L	X	Row Addr	Col Addr	Write Mask	Valid Data	Load and use Write Mask, Write Data to Dram
R	H	H	H	X	Row Addr	Col Addr	X	Valid Data	Normal Dram Read/Write (Non Masked)

† R = Random access operation; T = Transfer operation.
‡ DQ0-3 are latched on the later of W or CAS falling edge.
§ X = Don't care.
Write Mask = 1 (high) write to I/O enabled.

random port to serial port interface

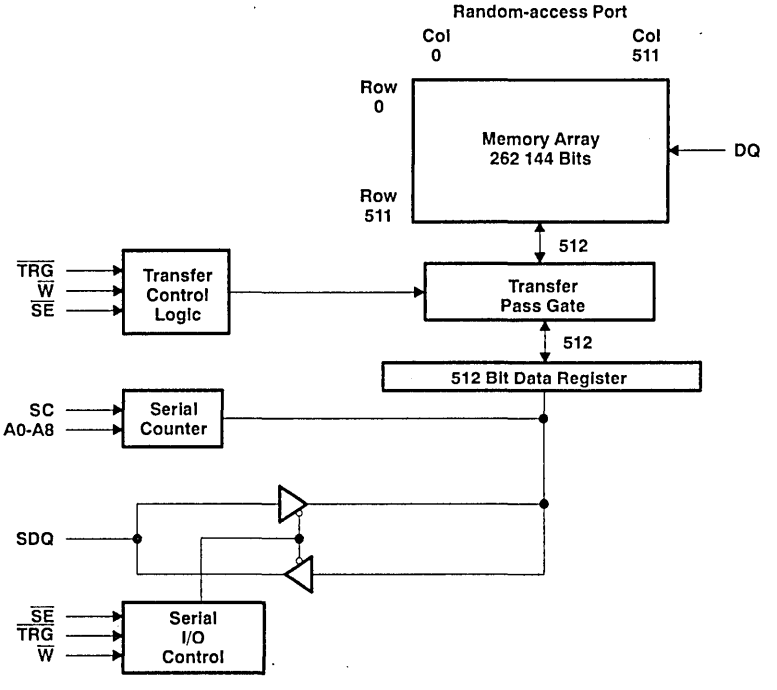


Figure 1. Block Diagram Showing One Random and One Serial I/O Interface

random address space to serial address space mapping

The 512 bits in each of the four data registers of the SAM are connected to the 512 column locations of each of the four random I/Os. Data can be accessed in or out of the SAM starting at any of the 512 data bit locations. This start location is selected by addresses A0 through A8 on the falling edge of $\overline{CAS}$ during any transfer cycle. The SAM is accessed starting from the selected start address, proceeding from the lowest to the highest significant bits. After the most significant bit position (511) is accessed, the serial counter wraps around such that bit 0 is accessed on the next clock pulse. The selected start address is stored and used for all subsequent transfer cycles until $\overline{CAS}$ is again brought low during any transfer cycle. Thus, the start address can be set once and $\overline{CAS}$ held high during all subsequent transfer cycles and the start address point will not change regardless of data present on A0 through A8.

transfer operations

As illustrated in Table 1, the SMJ44C250 supports three basic transfer modes of operation:

1. Write Transfer (SAM to DRAM)
2. Pseudo Write Transfer (Switches serial port from serial-out mode to serial-in mode. No actual data transfer takes place between the DRAM and the SAM.)
3. Read Transfer (Transfer entire contents of DRAM to SAM)

transfer register select ($\overline{TRG}$)

Transfer operations between the memory array and the data registers are invoked by bringing $\overline{TRG}$ low before $\overline{RAS}$ falls. The states of $\overline{W}$ and $\overline{SE}$, which are also latched on the falling edge of $\overline{RAS}$, determine which transfer operation will be invoked. (See Table 2.)

During read transfer cycles, $\overline{TRG}$ going high causes the addressed row of data to be transferred into the data register. Although the previous data in the data register is overwritten, the last bit of data appearing at SDQ before $\overline{TRG}$ goes high will remain valid until the first positive transition of SC after $\overline{TRG}$ goes high. The data at SDQ will then switch to new data beginning from the selected start, or *tap*, position.

transfer write enable ($\overline{W}$)

In register transfer mode, $\overline{W}$ determines whether a read or a write transfer will occur. To perform a write transfer, $\overline{W}$ and $\overline{SE}$ are held low as $\overline{RAS}$ falls. If $\overline{SE}$ is high during this transition, no transfer of data from the data register to the memory array occurs, but the SDQs are put into the input mode. This allows serial data to be input into the SAM. To perform a read transfer operation, $\overline{W}$ is held high and $\overline{SE}$ is a Don't Care as $\overline{RAS}$ falls. This cycle also puts the SDQs into the read mode, allowing serial data to be shifted out of the data register. (See Table 2.)

column enable ($\overline{CAS}$)

If $\overline{CAS}$ is brought low during a control cycle, the address present on the pins A0 through A8 will become the new register start location. If $\overline{CAS}$ is held high during a control cycle, the previous *tap* address will be retained from the last transfer cycle in which $\overline{CAS}$ went low to set the tap address.

addresses (A0 through A8)

Nine address bits are required to select one of the 512 possible rows involved in the transfer of data to or from the data registers. The states of A0-A8 are latched on the fallling edge of $\overline{RAS}$ to select one of 512 rows for the transfer operation.

To select one of the 512 positions in the SAM from which the first serial data will be accessed, the appropriate 9-bit column address (A0-A8) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and start (tap) position need not be supplied every cycle, only when changing to a different start position.

serial access operation

Refer to Tables 2 and 3 for the following discussion on serial access operation.

serial clock (SC)

Data (SDQ) is accessed in or out of data registers on the rising edge of SC. The SMJ44C250 is designed to work with a wide range of clock duty cycles to simplify system design. Since the data registers comprising the SAM are of static design, there are no SAM refresh requirements and there is no minimum SC clock operating frequency.

serial data input/output (SDQ0-SDQ3)

SD and SQ share a common I/O pin. Data is input to the device when $\overline{SE}$ is low during write mode and data is output from the device when $\overline{SE}$ is low during read mode. The data in the SAM will be accessed in the direction from least significant bit to most significant bit. The data registers operate modulo 512. Thus, after bit 511 is accessed, the next bits to be accessed will be bits 00, 01, 02, and so on.

serial enable ($\overline{SE}$)

The Serial Enable pin has two functions: first, it is latched on the falling edge of $\overline{RAS}$, with both $\overline{TRG}$ and $\overline{W}$ low to select one of the transfer functions (see Table 2.) If $\overline{SE}$ is low during this transition, then a transfer write occurs. If $\overline{SE}$ is high as $\overline{RAS}$ falls, then a write mode control cycle is performed. The function of this cycle is to switch the SDQs from the output mode to the input mode, thus allowing data to be shifted into the data register. NOTE: All transfer read and serial mode enable (pseudo transfer write) operations will perform a memory refresh operation on the selected row.

Second, during serial access operations, $\overline{SE}$ is used as an SDQ enable/disable. In the write mode, $\overline{SE}$ is used as an input enable. $\overline{SE}$ high disables the input and $\overline{SE}$ low enables the input. To take the device out of the write mode and into the read mode, a transfer read cycle must be performed. The read mode allows data to be accessed from the data register. While in the read mode, $\overline{SE}$ high disables the output and $\overline{SE}$ low enables the output.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is NOT disabled. Thus, external SC pulses will increment the internal serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low since the serial clock input buffer and the serial address counter are not disabled by $\overline{SE}$.

Table 2. Transfer Operation Logic

$\overline{TRG}$	$\overline{W}$	$\overline{SE}$	MODE
L	L	L	Register to memory (write) transfer
L	L	H	Serial write mode enable
L	H	X	Memory to register (read) transfer

NOTE: Above logic states are assumed valid on the falling edge of $\overline{RAS}$.

Table 3. Serial Operation Logic

LAST TRANSFER CYCLE	$\overline{SE}$	SDQ
Serial write mode enable†	L	Input enable
Serial write mode enable†	H	Input disable
Memory to register	L	Output enabled
Memory to register	H	HI-Z

†Pseudo transfer write.

power-up

To achieve proper device operation, an initial pause of 200 μs is required after power-up, followed by a minimum of eight $\overline{RAS}$ cycles or eight $\overline{CAS}$-before-$\overline{RAS}$ cycles, a memory-to-register transfer cycle and two SC cycles.

absolute maximum ratings over operating temperature (unless otherwise noted)†

Voltage on any pin except DQ and SDQ (see Note 1) ..... – 1 V to 7 V
Voltage on DQ and SDQ (see Note 1) ..... – 1 V to V_{CC}
Voltage range on V_{CC} (see Note 1) ..... 0 V to 7 V
Short circuit output current (per output) ..... 50 mA
Power dissipation ..... 1 W
Operating temperature range ..... –55°C to 125°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	SMJ44C250-1, SMJ44C250-2	4.75	5	5.25	V
		SMJ44C250-10, SMJ44C250-12	4.5	5	5.5	
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage		3.5		V_{CC}	V
V_{IL}	Low-level input voltage (see Note 2)		– 1.0		0.5	V
T_A	Operating free-air temperature		– 55			°C
T_C	Operating case temperature				125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = – 5.0 mA	2.4		V
V_{OL}	Low level output voltage (see Note 4)	I_{OL} = 4.2 mA		0.4	V
I_L	Input leakage current	V_I = 0 to 5.8 V, V_{CC} = 5 V, All outputs open		±1.0	µA
I_O	Output leakage current (see Note 3)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V		±10	µA

PARAMETER			SAM PORT	SMJ44C250-1 SMJ44C250-10		SMJ44C250-2 SMJ44C250-12		UNIT
				MIN	MAX	MIN	MAX	
I_{CC1}	Operation current $t_{c(RW)}$ = Minimum	(see Note 5)	Standby		100		90	mA
I_{CC1A}	$t_{c(SC)}$ = Minimum		Active		110		100	
I_{CC2}	Standby current, All clocks = V_{CC}		Standby		15		15	
I_{CC2A}	$t_{c(SC)}$ = Minimum		Active		35		35	
I_{CC3}	$\overline{RAS}$-only refresh current, $t_{c(RW)}$ = Minimum		Standby		100		90	
I_{CC3A}	$t_{c(SC)}$ = Minimum		Active		110		100	
I_{CC4}	Page mode current, $t_{c(P)}$ = Minimum		Standby		65		60	
I_{CC4A}	$t_{c(SC)}$ = Minimum		Active		70		65	
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ current, $t_{c(RW)}$ = Minimum		Standby		90		80	
I_{CC5A}	$t_{c(SC)}$ = Minimum		Active		110		100	
I_{CC6}	Data transfer current, $t_{c(RW)}$ = Minimum		Standby		100		90	
I_{CC6A}	$t_{c(SC)}$ = Minimum		Active		110		100	

NOTES: 3. $\overline{SE}$ is disabled for SDQ output leakage tests.

4. The SMJ44C250 One Mega-bit Video Ram exhibits simultaneous switching noise as described in Texas Instruments' "Advanced CMOS Logic Designer's Handbook". This phenomenon exhibits itself upon the DQ pins when the SDQ pins are switched and upon the SDQ pins when DQ pins are switched. This may cause the V_{OL} to exceed the data book limit for a short period of time, depending upon output loading and temperature. Care should be taken to provide proper termination, decoupling, and layout of the device to minimize simultaneous switching effects.

5. I_{CC} (standby) vs I_{CCA} (active) denotes the following:
   I_{CC} (standby): SAM port is inactive and the DRAM port is active (except for I_{CC2}).
   I_{CCA} (active): SAM port is active and the DRAM port is active (except for I_{CC2A}).
   I_{CC} is measured with no load on DQ or SDQ pins.

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capacitance over recommended ranges of supply voltage and operating temperature, f = 1 MHz (see Note 6)†

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		9	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		9	pF
$C_{i(W)}$	Input capacitance, write enable input		9	pF
$C_{i(SC)}$	Input capacitance, serial clock		9	pF
$C_{i(SE)}$	Input capacitance, serial enable		9	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		9	pF
$C_{o(O)}$	Output capacitance, SDQ and DQ		9	pF

† Capacitance is sampled only at initial design and after any major change.

NOTE 6: V_{CC} equal to 5 V ± 0.5 V for SMJ44C250-10 and SMJ44C250-12, 5 V ± 0.25 V for SMJ44C250-1 and SMJ44C250-2. The bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating temperature (see Note 7)

NO.†	PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ44C250-1 SMJ44C250-10		SMJ44C250-2 SMJ44C250-12		UNIT
					MIN	MAX	MIN	MAX	
1	$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{d(RLCL)}$ = MAX	t_{CAC}		25		30	ns
2	$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{CAA}		50		60	ns
3	$t_{a(CP)}$	Access time from $\overline{CAS}$ high	$t_{d(RLCL)}$ = MIN	t_{CAP}		55		65	ns
4	$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MIN	t_{RAC}		100		120	ns
5	$t_{a(G)}$	Access time of Q from $\overline{TRG}$ low		t_{OEA}		25		30	ns
6	$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 50 pF	t_{SCA}		30		35	ns
7	$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 50 pF	t_{SEA}		20		25	ns
9	$t_{dis(CH)}$	Random output disable time from $\overline{CAS}$ high (see Note 8)	C_L = 100 pF	t_{OFF}	0	20	0	20	ns
10	$t_{dis(G)}$	Random output disable time from $\overline{TRG}$ high (see Note 8)	C_L = 100 pF	t_{OEZ}	0	20	0	20	ns
11	$t_{dis(SE)}$	Serial output disable time from $\overline{SE}$ high (see Note 8)	C_L = 50 pF	t_{SEZ}	0	20	0	20	ns

† Numbering scheme intentionally skips numbers to allow for additional parameters specified in the SMJ44251A and SMJ44C251 data sheets.

NOTES: 7. Switching times assume C_L = 100 pF unless otherwise noted (see Figure 2).

8. Disable times are specified when the output is no longer driven.

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timing requirements over recommended ranges of supply voltage and operating temperature†

NO.	PARAMETER		ALT. SYMBOL	SMJ44C250-1 SMJ44C250-10		SMJ44C250-2 SMJ44C250-12		UNIT
				MIN	MAX	MIN	MAX	
12	$t_{c(rd)}$	Read cycle time (see Note 9)	t_{RC}	190		220		ns
13	$t_{c(W)}$	Write cycle time	t_{WC}	190		220		ns
14	$t_{c(rdW)}$	Read-modify-write cycle time	t_{RWC}	250		290		ns
15	$t_{c(P)}$	Page-mode read, write cycle time	t_{PC}	60		70		ns
16	$t_{c(RDWP)}$	Page-mode read-modify-write cycle time	t_{RWC}	105		125		ns
17	$t_{c(TRD)}$	Transfer read cycle time	t_{RC}	190		220		ns
18	$t_{c(TW)}$	Transfer write cycle time	t_{WC}	190		220		ns
18a	$t_{c(TW)M}$	Transfer write cycle time, multiple transfer operation		320		350		ns
19	$t_{c(SC)}$	Serial clock cycle time (see Note 10)	t_{SCC}	30		35		ns
20	$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	20		30		ns
21	$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 11)	t_{CAS}	25	75 000	30	75 000	ns
22	$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	80		90		ns
23	$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 12)	t_{RAS}	100	75 000	120	75 000	ns
23a	$t_{w(RL)M}$	Pulse duration, $\overline{RAS}$ low multiple transfer write operation		185		195		ns
24	$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	t_{WP}	25		25		ns
25	$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		25		30		ns
26	$t_{w(SCH)}$	Pulse duration, SC high	t_{SC}	10		12		ns
27	$t_{w(SCL)}$	Pulse duration, SC low	t_{SCP}	10		12		ns
28	$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
30	$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
31	$t_{su(WMR)}$	$\overline{W}$ setup time before $\overline{RAS}$ low	t_{WSR}	0		0		ns
32	$t_{su(DQR)}$	DQ setup time before $\overline{RAS}$ low (write mask operation)	t_{MS}	0		0		ns
33	$t_{su(TRG)}$	$\overline{TRG}$ setup time before $\overline{RAS}$ low	t_{TLS}	0		0		ns
34	$t_{su(SE)}$	$\overline{SE}$ setup time before $\overline{RAS}$ low (see Note 22)	t_{ESR}	0		0		ns
36	$t_{su(DCL)}$	Data setup time before $\overline{CAS}$ low	t_{DSC}	0		0		ns
37	$t_{su(DWL)}$	Data setup time before $\overline{W}$ low	t_{DSW}	0		0		ns
38	$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
39	$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
40	$t_{su(WCH)}$	Write setup time before $\overline{CAS}$ high	t_{CWL}	25		30		ns
41	$t_{su(WRH)}$	Write setup time before $\overline{RAS}$ high	t_{RWL}	25		30		ns
42	$t_{su(SDS)}$	SD setup time before SC high	t_{SDS}	3		3		ns
43	$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		ns
45	$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. All cycle times assume t_t = 5 ns.

10. When the odd tap is used (tap address can be 0-511, and odd taps are 1,3,5, etc.), the cycle time for SC in the first serial data out cycle needs to be 70 ns minimum.
11. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].
12. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

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timing requirements over recommended ranges of supply voltage and operating temperature (continued)†

NO.	PARAMETER		ALT. SYMBOL	SMJ44C250-1 SMJ44C250-10		SMJ44C250-2 SMJ44C250-12		UNIT
				MIN	MAX	MIN	MAX	
46	$t_{h(TRG)}$	$\overline{TRG}$ hold time after $\overline{RAS}$ low	t_{TLH}	15		15		ns
47	$t_{h(SE)}$	$\overline{SE}$ hold time after $\overline{RAS}$ low (see Note 22)	t_{REH}	15		15		ns
48	$t_{h(RWM)}$	$\overline{W}$ hold time after $\overline{RAS}$ low	t_{RWH}	15		15		ns
49	$t_{h(RDQ)}$	DQ hold time after $\overline{RAS}$ low (write mask operation)	t_{MH}	15		15		ns
51	$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low (see Note 13)	t_{AR}	45		45		ns
52	$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	20		25		ns
53	$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 13)	t_{DHR}	45		50		ns
54	$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	20		25		ns
55	$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ (see Note 14)	t_{RCH}	0		0		ns
56	$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ (see Note 14)	t_{RRH}	10		10		ns
57	$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	30		35		ns
58	$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 13)	t_{WCR}	50		55		ns
59	$t_{h(SDS)}$	SD hold time after SC high	t_{SDH}	5		5		ns
60	$t_{h(SHSQ)}$	SQ hold time after SC high	t_{SOH}	5		5		ns
61	$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		ns
62	$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
63	$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		ns
64	$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Notes 15 and 16)	t_{CWD}	55		65		ns
65	$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 17)	t_{RCD}	25	75	25	90	ns
66	$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	50		60		ns
67	$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 15)	t_{RWD}	130		155		ns
68	$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 15)	t_{AWD}	85		100		ns
69	$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 18)	t_{CHR}	25		25		ns
70	$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 18)	t_{CSR}	10		10		ns
71	$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 18)	t_{RPC}	10		10		ns
72	$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high	t_{CTH}	25		30		ns
73	$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ (see Note 15)		25		30		ns
74	$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high	t_{RTH}	90		95		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 13. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
14. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
15. Read-modify-write operation only.
16. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
17. Maximum value specified only to guarantee $\overline{RAS}$ access time.
18. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating temperature (concluded)†

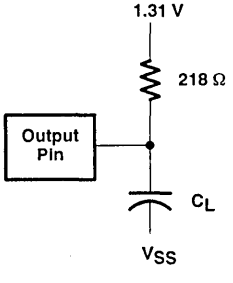
NO.	PARAMETER		ALT. SYMBOL	SMJ44C250-1 SMJ44C250-10		SMJ44C250-2 SMJ44C250-12		UNIT
				MIN	MAX	MIN	MAX	
76	$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 19)	t_{RSD}	130		140		ns
77	$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 19)	t_{CSD}	40		45		ns
78	$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 19 and 20)	t_{TSL}	15		20		ns
79	$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 19)	t_{TRD}	−10		−10		ns
80	$t_{d(SCRL)}$	Delay time, SC high to $\overline{RAS}$ (see Notes 21 and 22)	t_{SRS}	10		20		ns
81	$t_{d(SCSE)}$	Delay time, SC high to $\overline{SE}$ high in serial input mode (see Note 24)		20		20		ns
82	$t_{d(RHSC)}$	Delay time, $\overline{RAS}$ high to SC high (see Note 22)	t_{SRD}	25		30		ns
83	$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 23)	t_{TRP}	$t_{w(RH)}$		$t_{w(RH)}$		ns
84	$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 23)	t_{TSD}	35		40		ns
85	$t_{d(SESC)}$	Delay time, $\overline{SE}$ low to SC high (see Note 24)	t_{SWS}	10		15		ns
88	$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8	ms

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 19. Memory to register (read) transfer cycles only.
20. In a transfer read cycle, the state of SC when $\overline{TRG}$ rises is a Don't Care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{TRG}$ goes high.
21. In a transfer write cycle, the state of SC when $\overline{RAS}$ falls is a Don't Care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{RAS}$ goes low.
22. Register to memory (write) transfer cycles only.
23. Memory to register (read) and register to memory (write) transfer cycles only.
24. Serial data-in cycles only.
25. System transition times (rise and fall) are to be a minimum of 3 ns and a maximum of 50 ns.

ADVANCE INFORMATION

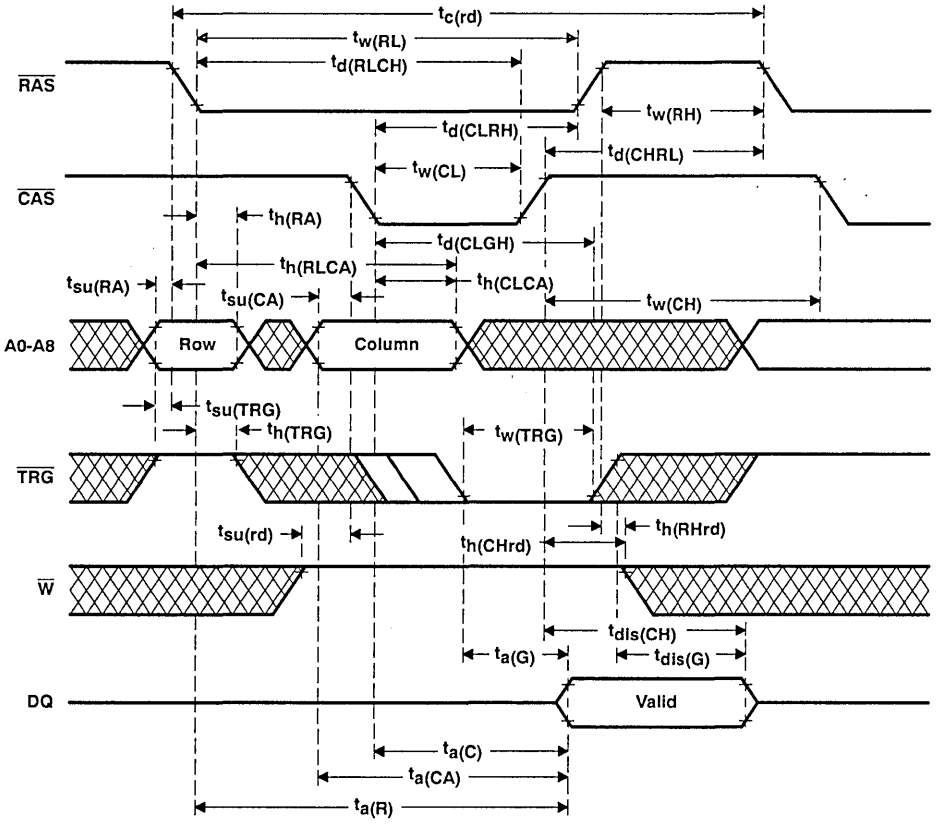
PARAMETER MEASUREMENT INFORMATION



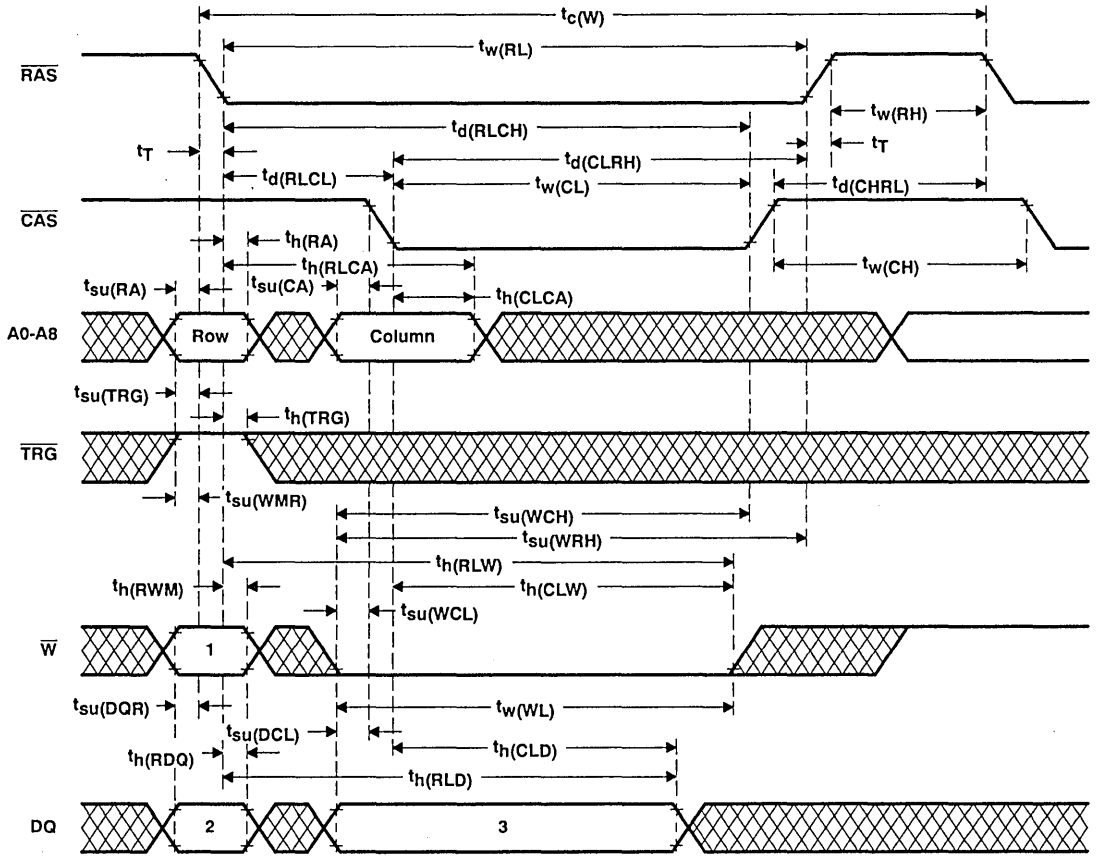
Load Circuit

Figure 2. Load Circuit

read cycle timing

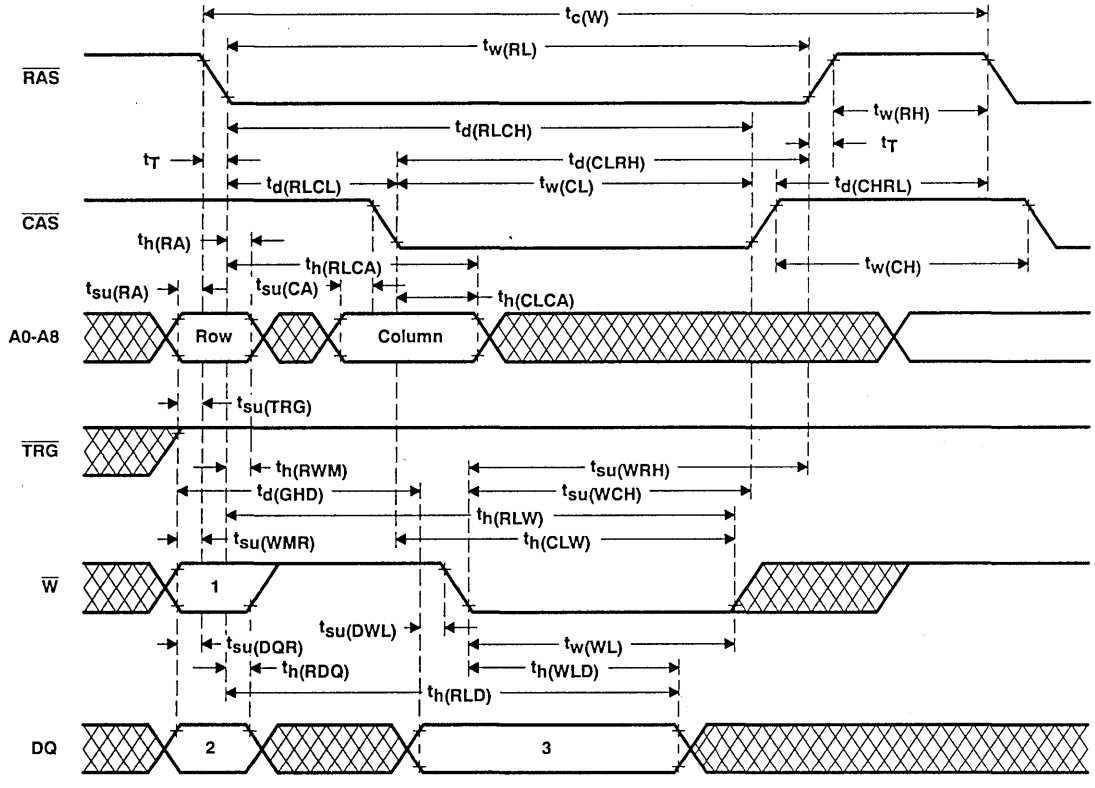


early write cycle timing



NOTE 26: See "Write Cycle State Table" for the logic state of "1", "2", and "3".

delayed write cycle timing

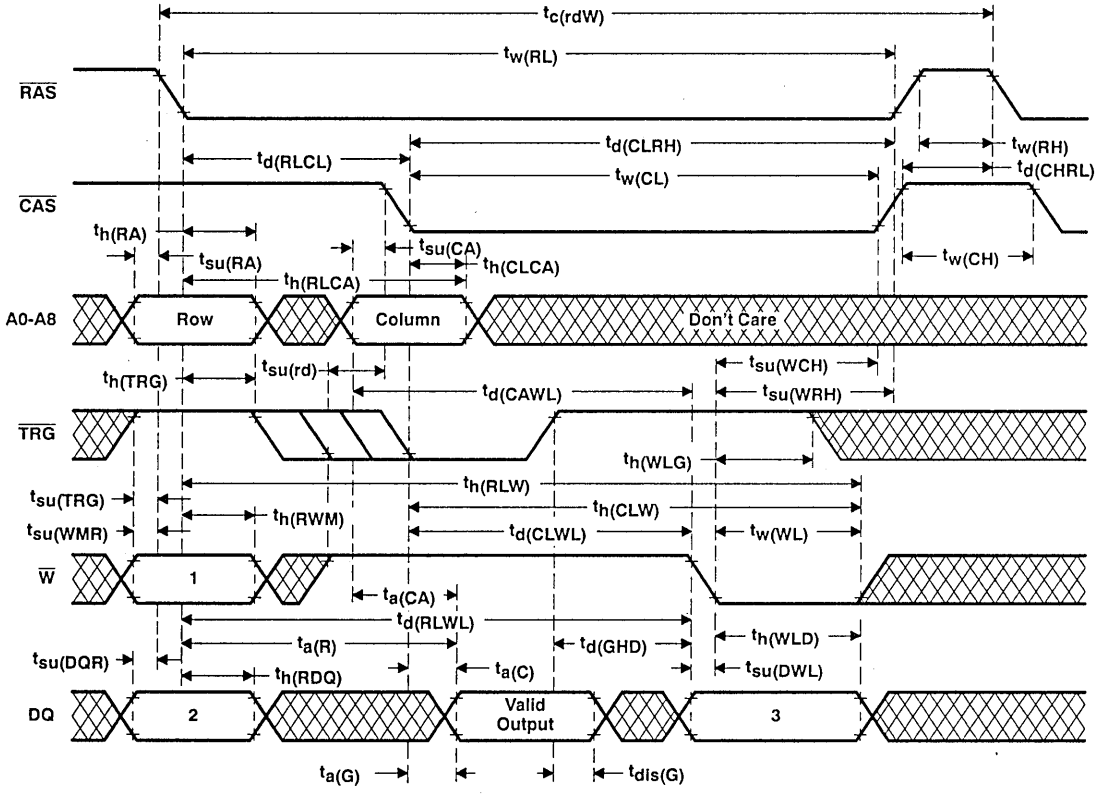


NOTE 26: See "Write Cycle State Table" for the logic state of "1", "2", and "3".

write cycle state table

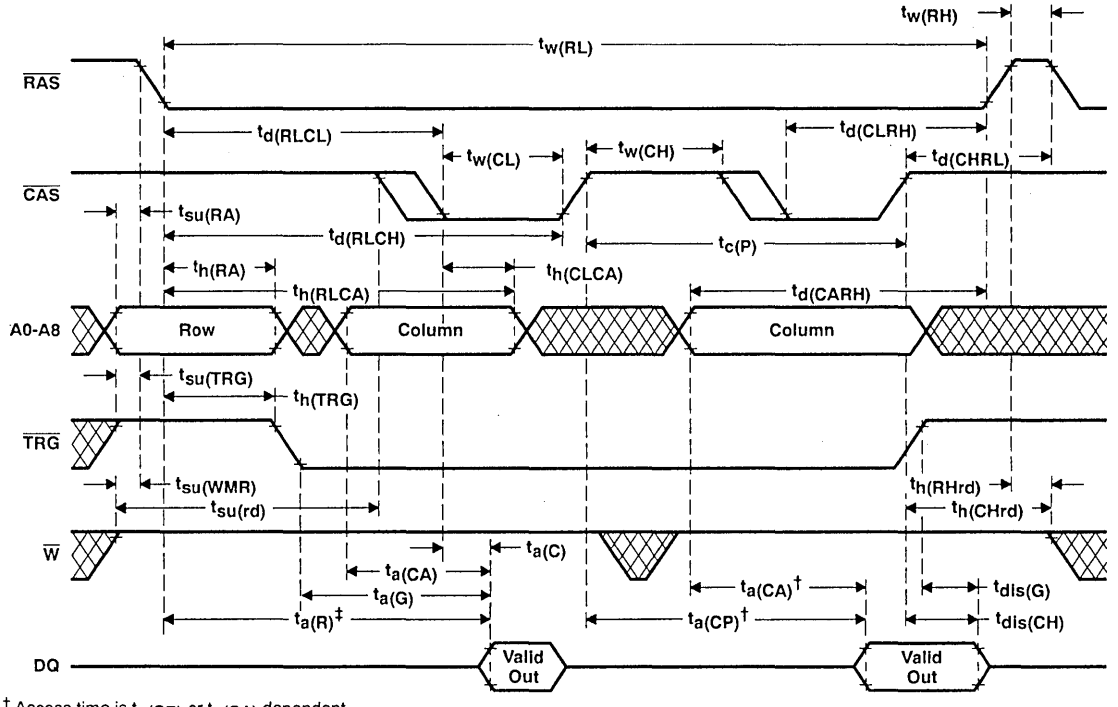
CYCLE	STATE		
	1	2	3
Write mask load/use Write DQs to I/Os	L	Write Mask	Valid Data
Normal early or late Write operation	H	Don't Care	Valid Data

read-write/read-modify-write cycle timing



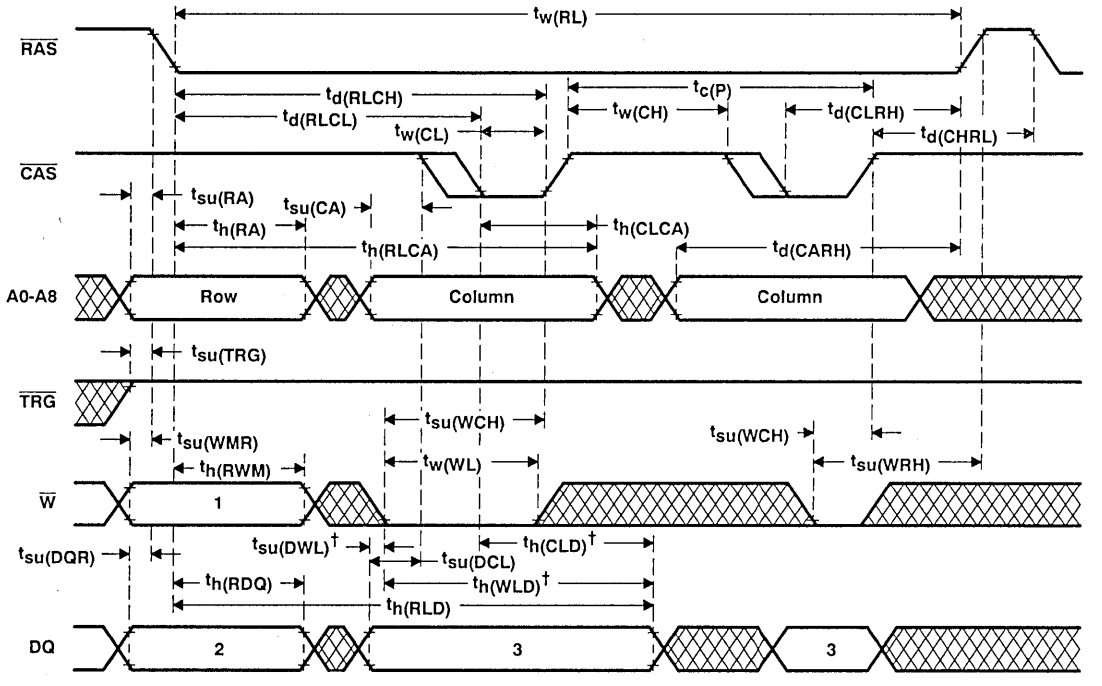
NOTE 27: See "Write Cycle State Table" for the logic state of "1", "2", and "3". Same logic as delayed write cycle.

enhanced page-mode read cycle timing



† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
‡ Output may go from high-impedance state to an invalid data state prior to the specified access time.
NOTE 28: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.

enhanced page mode write cycle timing

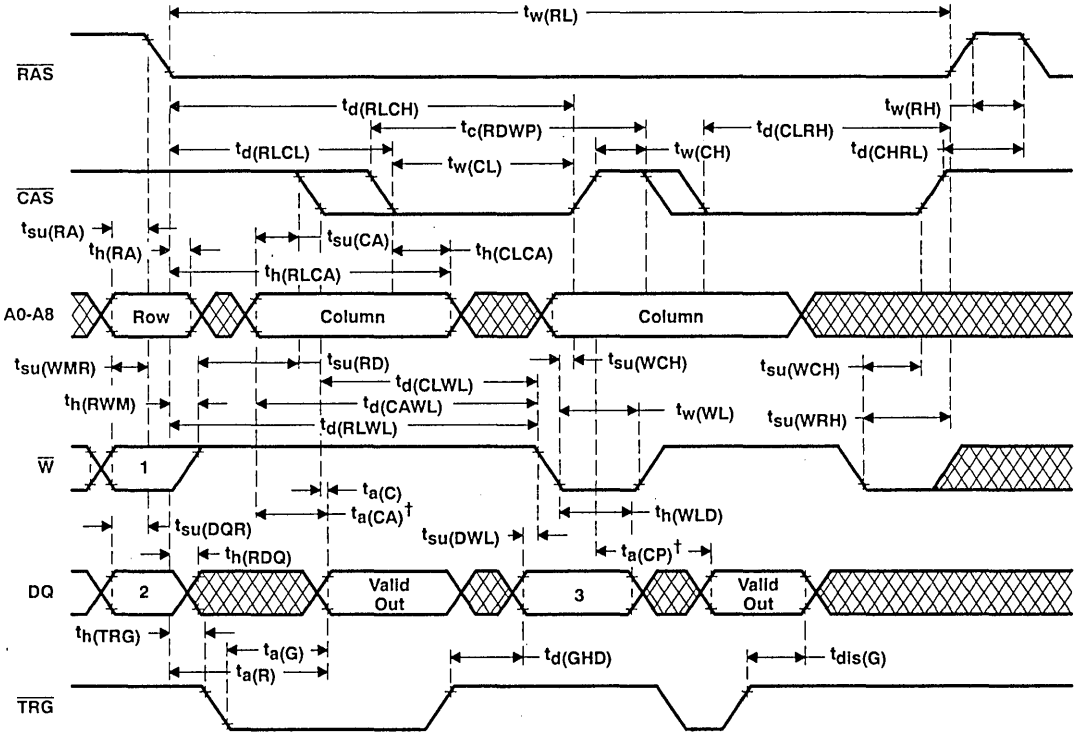


† Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

NOTES: 27. See "Write Cycle State Table" for the logic state of "1", "2", and "3". Same logic as delayed write cycle.

29. A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used, to guarantee page-mode cycle time. If the early write cycle timing is used, the state of $\overline{TRG}$ is a Don't Care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

enhanced page-mode read-modify-write cycle timing

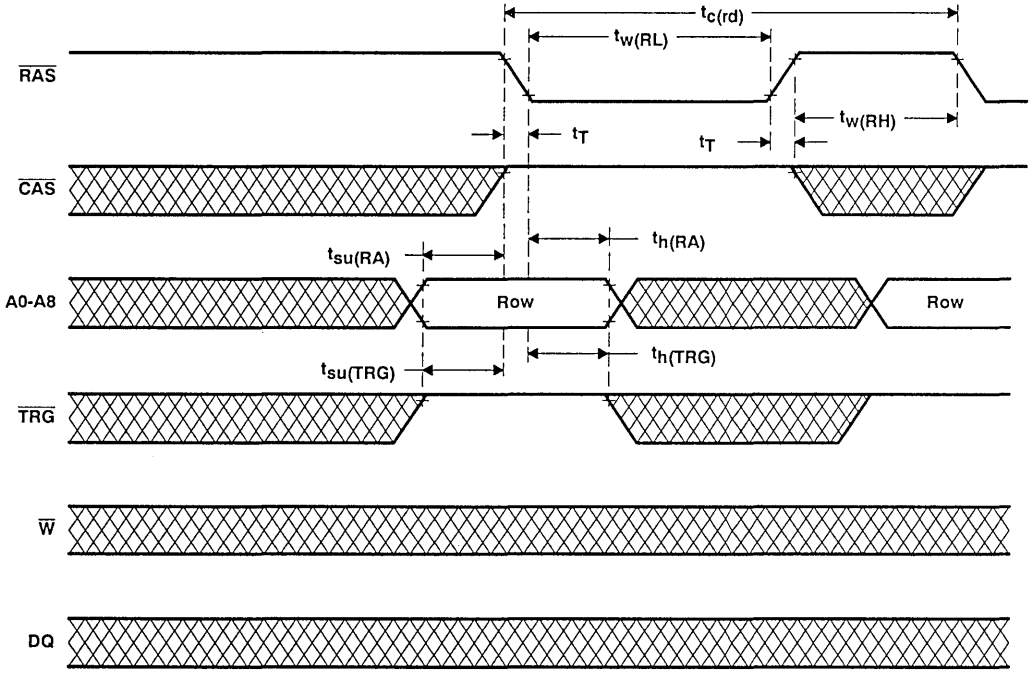


† Output may go from the high-impedance state to an invalid data state prior to the specified access time.

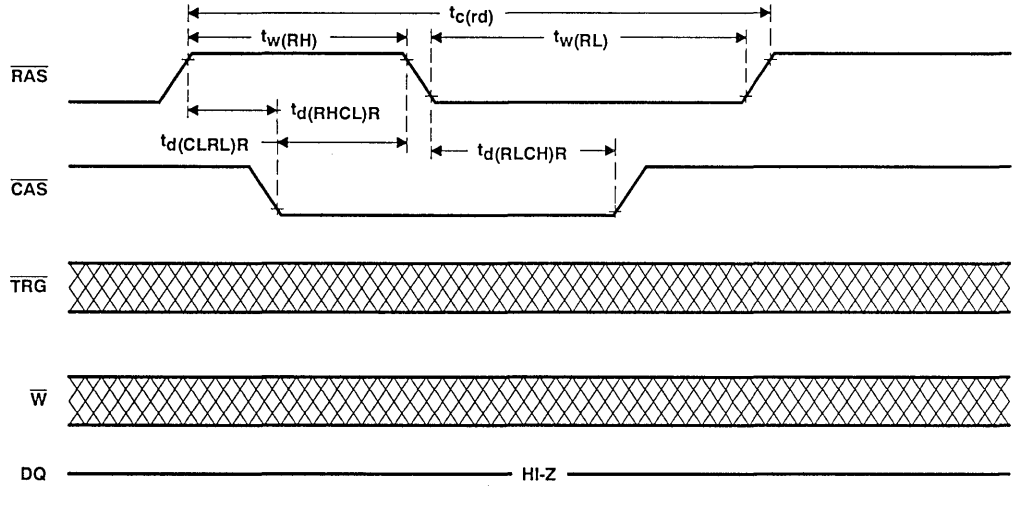
NOTES: 27. See "Write Cycle State Table" for the logic state of "1", "2", and "3". Same logic as delayed write cycle.

30. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

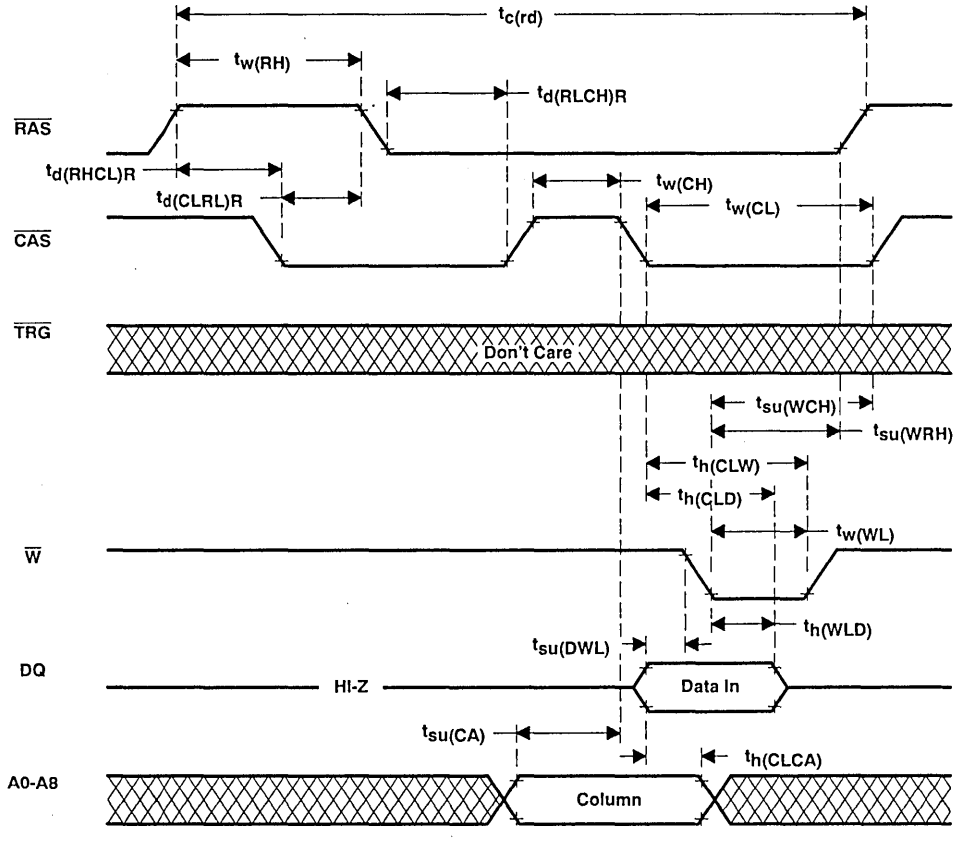
$\overline{RAS}$-only refresh timing



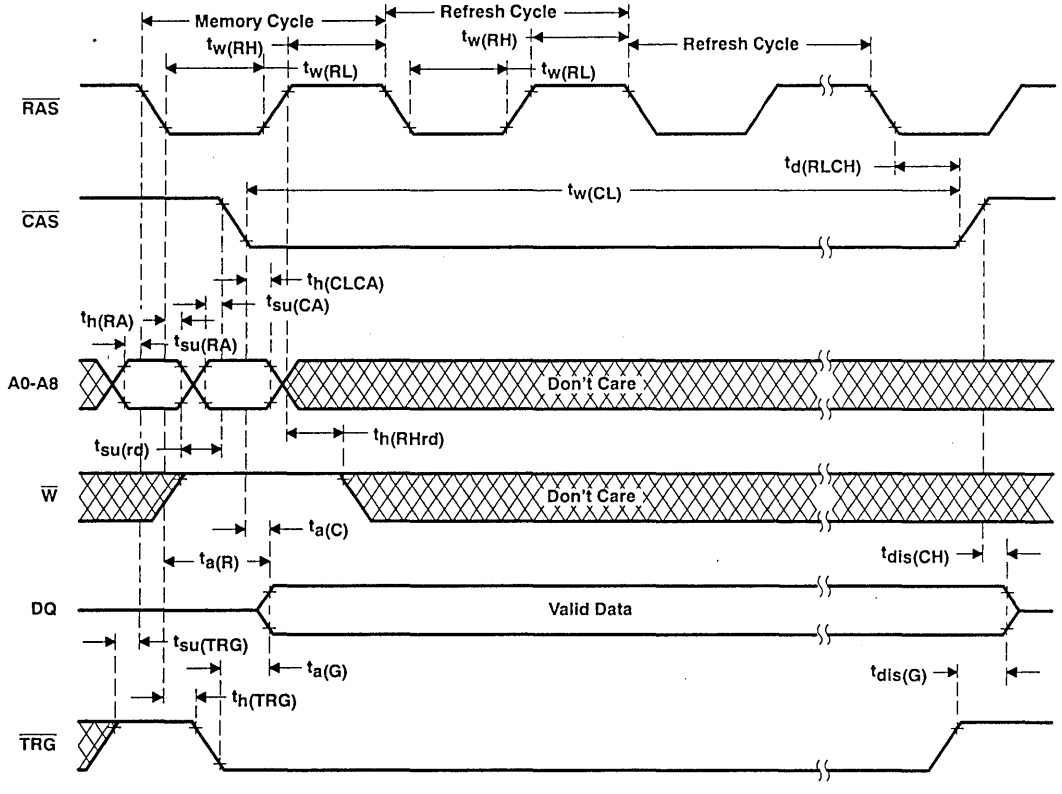
$\overline{CAS}$-before-$\overline{RAS}$ refresh



$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test timing

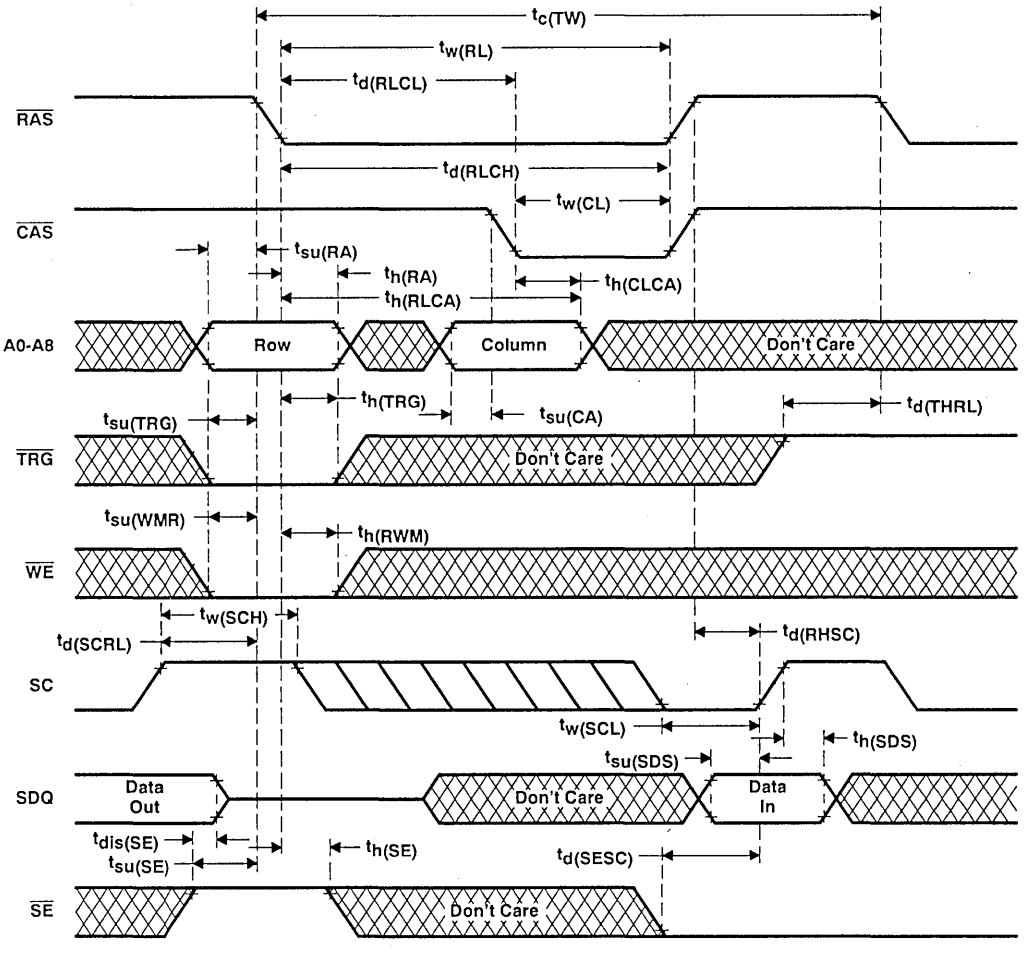


hidden refresh cycle timing



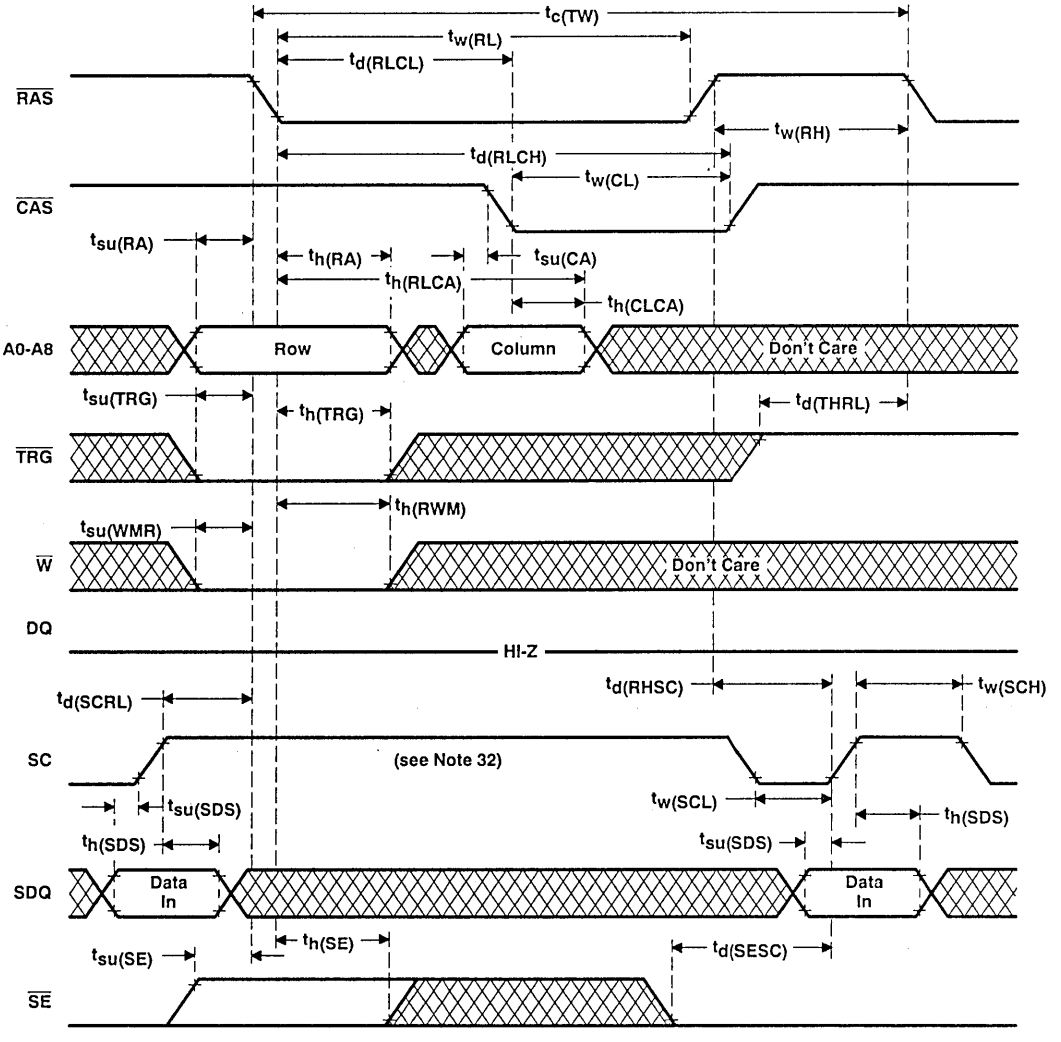
write-mode control pseudo write transfer timing

The write-mode control cycle is used to change the SDQs from the output mode to the input mode. This allows serial data to be written into the data register. The diagram below assumes that the device was originally in the serial read mode.



NOTES: 31. Random-mode Q outputs remain in the high-impedance state for the entire write-mode control.
32. $\overline{SE}$ must be high as $\overline{RAS}$ falls in order to perform a write-mode control cycle.

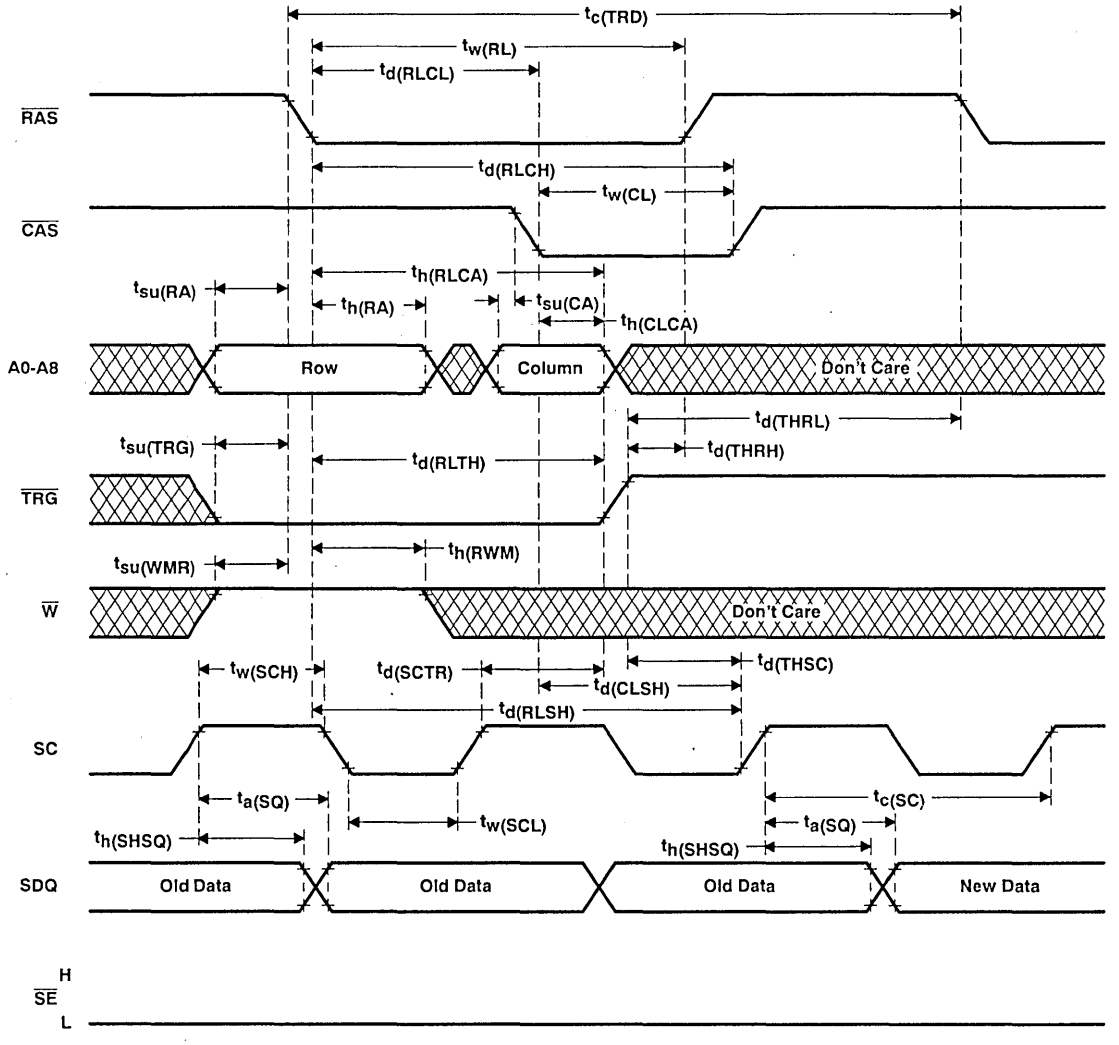
data register to memory timing, serial input enabled



NOTES: 33. Random mode Q outputs remain in the high-impedance state for the entire data register to memory transfer cycle. This cycle is used to transfer data from the data register to the memory array. Every one of the 512 locations in each data register is written into the corresponding 512 columns of the selected row. Data in the data register may proceed from a serial shift-in or from a parallel load from one of the memory array rows. The above diagram assumes that the device is in the serial write mode (i.e., SD is enabled by a previous write mode control cycle, thus allowing data to be shifted-in).

34. Successive transfer writes can be performed without serial clocks for applications requiring fast memory array clears.
35. SC transitions are not allowed between $\overline{RAS}$ low and $\overline{TRG}$ high.
36. For multiple transfer write operation; a transfer read cycle needs to be done from the same row after the first transfer write is carried out, then do multiple transfer write for subsequent rows. See parameters $t_{c(TW)M}$ and $t_{c(RL)M}$.

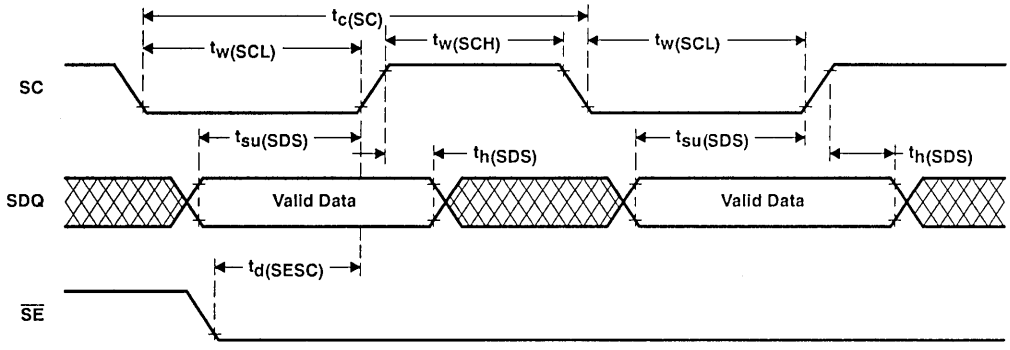
memory to data register transfer timing



NOTES: 37. Random mode (Q outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written into from the 512 corresponding columns of the selected row. The data that is transferred into the data registers may be either shifted out or transferred back into another row.

38. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

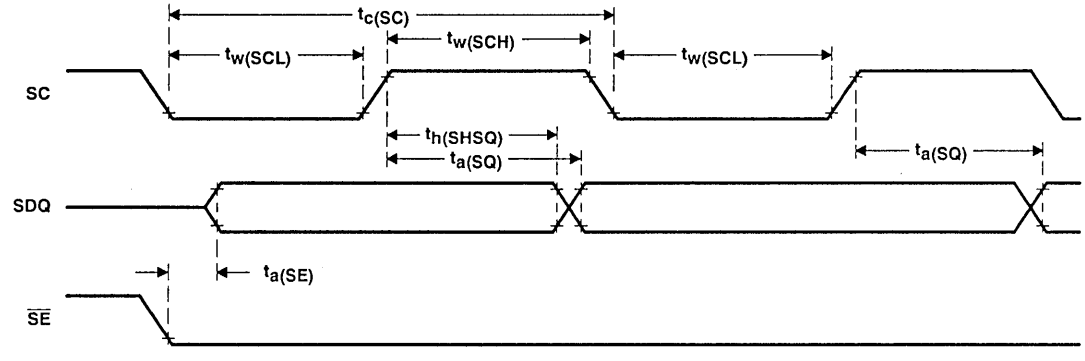
serial data-in timing



The serial data-in cycle (SD) is used to input serial data into the data registers. Before data can be written into the data registers via SD, the device must be put into the write mode by performing a write mode control, or pseudo-transfer, cycle. Transfer write cycles occurring between the write mode control cycle and the subsequent writing of data will not take the device out of the write mode. However, a transfer read cycle during that time will take the device out of the write mode and put it into the read mode, thus disabling the input of data. Data will be written starting at the location specified by the input address loaded on the previous transfer cycle.

While accessing data in the serial data registers, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.

serial data-out timing



NOTE 10: When the odd tap is used (tap addresses can be 0-511, and odd taps are 1,3,5 ... etc.), the cycle time for SC in the first serial data out cycle needs to be 70 ns minimum.

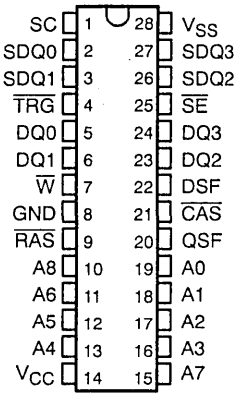
The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle. Transfer write cycles occurring between the transfer read cycle and the subsequent shifting out of data will not take the device out of the read mode. But a write mode control cycle at that time will take the device out of the read mode and put it in the write mode, thus not allowing the reading of data.

While accessing data in the serial data registers, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.

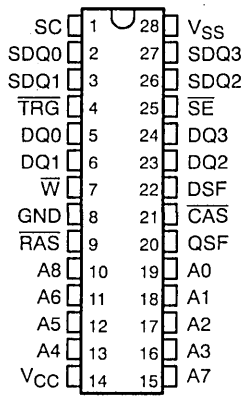
SGMS038 — JANUARY 1991

- Military Operating Temperature Range . . . –55°C to 125°C
- Class B High-Reliability Processing
- DRAM: 262 144 Words × 4 Bits
  SAM: 512 Words × 4 Bits
- Dual Port Accessibility—Simultaneous and Asynchronous Access from the DRAM and SAM Ports
- Bidirectional Data Transfer Function Between the DRAM and the Serial Data Register
- 4 × 4 Block Write Feature for Fast Area Fill Operations. As Many as Four Memory Address Locations Written Per Cycle from an On-Chip Color Register
- Write Per Bit Feature for Selective Write to Each RAM I/O. Two Write Per Bit Modes to Simplify System Design
- Enhanced Page-Mode Operation for Faster Access
- $\overline{CAS}$-before-$\overline{RAS}$ and Hidden Refresh Modes
- RAM Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design
- Long Refresh Period . . . 8 ms (Max)
- Up to 33 MHz Uninterrupted Serial Data Streams
- Split Serial Data Register for Simplified Realtime Register Reload
- 3-State Serial I/Os Allow Easy Multiplexing of Video Data Streams
- 512 Selectable Serial Register Starting Locations
- Texas Instruments EPIC™ CMOS Process
- Packaging
  —28-Pin Ceramic Sidebraze DIP (JD Suffix)
  —28-Pin Ceramic Small Outline J-Leaded Chip Carrier (HJ Suffix)

JD Package† (Top View)



HJ Package† (Top View)



†This illustration is for pinout reference only.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column Enable
DQ0-DQ3	DRAM Data In-Out / Write Mask Bit
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row Enable
SC	Serial Data Clock
SDQ0-SDQ3	Serial Data In-Out
$\overline{TRG}$	Transfer Register / Q Output Enable
$\overline{W}$	Write Mask Select / Write Enable
DSF	Special Function Select
QSF	Split Register Activity Status
V_{CC}	5-V Supply
V_{SS}	Ground
GND	Ground (Important: Not connected to internal V_{SS})

- Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX) $t_{a(R)}$	ACCESS TIME COLUMN ENABLE (MAX) $t_{a(C)}$	ACCESS TIME SERIAL DATA (MAX) $t_{a(SC)}$	ACCESS TIME SERIAL ENABLE (MAX) $t_{a(SE)}$	V_{CC} TOLERANCE
'44C251-1	100 ns	25 ns	30 ns	20 ns	±5%
'44C251-2	120 ns	30 ns	35 ns	25 ns	±5%
'44C251-10	100 ns	25 ns	30 ns	20 ns	±10%
'44C251-12	120 ns	30 ns	35 ns	25 ns	±10%

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

description

The SMJ44C251 Multiport Video RAM is a high-speed, dual-ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 4 bits each, interfaced to a serial data register, or Serial Access Memory (SAM), organized as 512 words of 4 bits each. The SMJ44C251 supports three basic types of operation: random access to and from the DRAM, serial access to and from the serial register, and bidirectional transfer of data between any row in the DRAM and the serial register. Except during transfer operations, the SMJ44C251 can be accessed simultaneously and asynchronously from the DRAM and SAM ports. During transfer operations, the 512 columns of the DRAM are connected to the 512 positions in the serial data register. The 512 × 4 bit serial data register can be loaded from the memory row (transfer read), or else the contents of the 512 × 4 bit serial data register can be written to the memory row (transfer write).

The SMJ44C251 is equipped with several features designed to provide higher system-level bandwidth and simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's novel 4 × 4 Block Write mode. The Block Write mode allows four bits of data present in an on-chip color data register to be written to any combination of four adjacent column address locations. As many as 16 bits of data can be written to memory during each $\overline{CAS}$ cycle time. Also on the DRAM port, a write mask register provides a persistent write-per-bit mode without repeated mask loading.

On the serial register, or SAM port, the SMJ44C251 offers a split register transfer read (DRAM to SAM) option that enables realtime register reload implementation for truly continuous serial data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. This new realtime register implementation allows truly continuous serial data. For applications not requiring realtime register reload (for example, reloads done during CRT retrace periods), the single-register mode of operation is retained to simplify system design. The SAM can also be configured in the input mode, accepting serial data from an external device. Once the serial register within the SAM is loaded, its contents can be transferred to the corresponding column positions in any row in memory in a single memory cycle.

The SAM port is designed for maximum performance. Data can be input to or accessed from the SAM at serial rates up to 33 MHz. During the split-register mode of operation, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate output, designated QSF, is included to designate which half of the serial register is active at any given time.

All address lines and data-in are latched on-chip to simplify system design. All data-outs are unlatched to allow greater system flexibility.

The SMJ44C251 employs state-of-the-art Texas Instruments EPIC™ scaled-CMOS, double level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The SMJ44C251 is offered in a 28-pin, ceramic small-outline J-leaded package (HJ suffix) for direct surface mounting in rows on 400-mil centers. It is also offered in a 400-mil, 28-pin, sidebrazed DIP package (JD suffix). Both packages are characterized for operation from – 55°C to 125°C (M suffix).

The SMJ44C251 and other multiport video RAMs are supported by a broad line of graphics processors and control devices from Texas Instruments, including the SMJ34010 and SMJ34020 Graphics System Processors.

PRODUCT PREVIEW

- Military Operating Temperature Range . . . – 55°C to 125°C
- Class B High-Reliability Processing
- DRAM: 262 144 Words × 4 Bits
  SAM: 512 Words × 4 Bits
- Dual Port Accessibility — Simultaneous and Asynchronous Access from the DRAM and SAM Ports
- Bidirectional Data Transfer Function Between the DRAM and the Serial Data Register
- 4 × 4 Block Write Feature for Fast Area Fill Operations. As Many as Four Memory Address Locations Written Per Cycle From an On-Chip Color Register
- Write-Per-Bit Feature for Selective Write to Each RAM I/O
- Enhanced Page Mode Operation for Faster Access
- $\overline{CAS}$-before-$\overline{RAS}$ and Hidden Refresh Modes
- RAM Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design
- Long Refresh Period . . . Every 8 ms (Max)
- Up to 33 MHz Uninterrupted Serial Data Streams
- 3-State Serial I/Os Allow Easy Multiplexing of Video Data Streams
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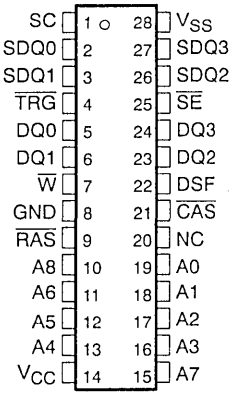
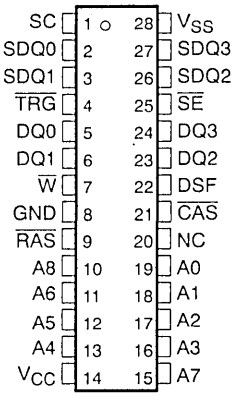
- Texas Instruments EPIC™ CMOS Process
- Packaging Options:
  — 28-pin Ceramic Sidebraze DIP (JD suffix)
  — 28-pin Ceramic Small Outline J-Leaded Chip Carrier (HJ Suffix)

JD Package
(Top View)



HJ Package
(Top View)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column Enable
DQ0-DQ3	DRAM Data In-Out/Write Mask Bit
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row Enable
SC	Serial Data Clock
SDQ0-SDQ3	Serial Data In-Out
$\overline{TRG}$	Transfer Register/Q Output Enable
$\overline{W}$	Write Mask Select/Write Enable
DSF	Special Function Select
V_{CC}	5-V Supply
V_{SS}	Ground
GND	Ground (Important: not connected internally to V_{SS})
NC	No Connection

- Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX) $t_{a(R)}$	ACCESS TIME COLUMN ENABLE (MAX) $t_{a(C)}$	ACCESS TIME SERIAL DATA (MAX) $t_{a(SC)}$	ACCESS TIME SERIAL ENABLE (MAX) $t_{a(SE)}$	V_{CC} TOLERANCE
'44C251A-1	100 ns	25 ns	30 ns	20 ns	±5%
'44C251A-2	120 ns	30 ns	35 ns	25 ns	±5%
'44C251A-10	100 ns	25 ns	30 ns	20 ns	±10%
'44C251A-12	120 ns	30 ns	35 ns	25 ns	±10%

NOTE: All references to the SMJ44C251A-10, -1 are Advance Information only.

ADVANCE INFORMATION

EPIC is a trademark of Texas Instruments Incorporated.

description

The SMJ44C251A multiport video RAM is a high speed, dual ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 4 bits each interfaced to a serial data register, or Serial Access Memory (SAM), organized as 512 words of 4 bits each. The SMJ44C251A supports three basic types of operation: random access to and from the DRAM, serial access to and from the serial register, and bidirectional transfer of data between any row in the DRAM and the serial register. Except during transfer operations, the SMJ44C251A can be accessed simultaneously and asynchronously from the DRAM and SAM ports. During a transfer operation, the 512 columns of the DRAM are connected to the 512 positions in the serial data register. The 512 × 4 bit serial data register can be loaded from the memory row (transfer read) or else the contents of the 512 × 4 bit serial data register can be written to the memory row (transfer write).

The SMJ44C251A is equipped with several features designed to provide higher system-level bandwidth and simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's 4 × 4 Block Write mode. The Block Write mode allows four bits of data present in an on-chip color data register to be written to any combination of four adjacent column address locations. As many as 16 bits of data can be written to memory during each $\overline{CAS}$ cycle time.

On the serial register, or SAM port, the SMJ44C251A offers a single register mode of operation for simplified memory design. The SAM can be configured in input mode, accepting serial data from an external device; or data can be accessed from the SAM at serial rates up to 33 MHz. Once the serial register within the SAM is loaded, it's contents can be transferred to the corresponding column positions in any row in memory in a single memory cycle.

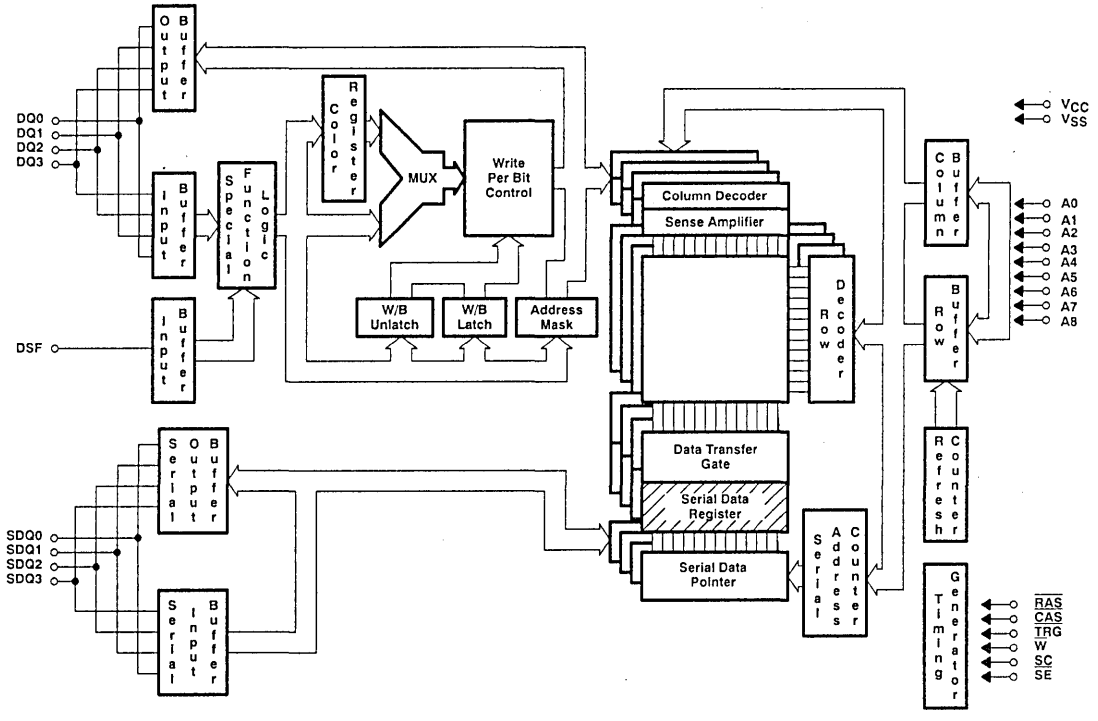
All the address lines and data-in are latched on chip to simplify design. All data-outs are unlatched to allow greater system flexibility.

The SMJ44C251A is offered both in a 28-pin 400-mil dual-in line ceramic sidebraze package (JD suffix) for through-hole row insertion, and in a 28-pin ceramic small outlline J-leaded chip carrier package (HJ suffix) for surface-mount applications. The L suffix device is tested for operation from 0°C to 70°C. The M suffix device is tested for operation from – 55°C to 125°C.

The SMJ44C251A and other SMJ44C25X multiport Video RAMs are supported by a broad line of video/graphic processors from Texas Instruments, including the SMJ34010 and SMJ34020 Graphics System Processors.

NOTE: All references to the SMJ44C251A-10, -1 are Advance Information only.

functional block diagram



Detailed Pin Description vs Operational Mode

PIN	DRAM	TRANSFER	SAM
A0-A8	Row, Column Address	Row, Tap Address	
$\overline{CAS}$	Column Enable, Output Enable	Tap Address Strobe	
DQi	DRAM Data I/O, Write Mask Bits		
DSF	Block Write Enable	Alternate Write Transfer Enable	
	Color Register Load Enable		
$\overline{RAS}$	Row Enable	Row Enable	
$\overline{SE}$		Serial-In Mode Enable	Serial Enable
SC			Serial Clock
SDQi			Serial Data I/O
$\overline{TRG}$	Q Output Enable	Transfer Enable	
$\overline{W}$	Write Enable, Write per Bit Select	Transfer Write Enable	
V_{CC}	5-V Supply (typical)		
V_{SS}	Device Ground		
GND	System Ground (Important: not connected internally to V_{SS})		
NC	Make no external connection		

operation

random access operation

Refer to Table 1, Function Table (page 9-156), for random-access and transfer operations. Random-access operations are denoted by the designator "R" and transfer operations are denoted by a " T."

transfer register select and DQ enable ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either register or random-access operation as $\overline{RAS}$ falls. For random-access (DRAM) mode, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. Asserting $\overline{TRG}$ high as $\overline{RAS}$ falls causes the 512 storage elements of each data register to remain disconnected from the corresponding 512-bit lines of the memory array. (Asserting $\overline{TRG}$ low as $\overline{RAS}$ falls connects the 512-bit positions in the serial register to the bit lines and indicates that a transfer will occur between the data registers and the selected memory row. See *Transfer Operation* for details.)

During random-access operations, $\overline{TRG}$ also functions as an output enable for the random (Q) outputs. Whenever $\overline{TRG}$ is held high, the Q outputs are in the high-impedance state to prevent an overlap between the address and DRAM data. This organization allows the connection of the address lines to the data I/O lines but prohibits the use of the early write cycle. It also allows read-modify-write cycles to be performed by providing a three-state condition to the common I/O pins so that write data can be driven onto the pins after output read data has been externally latched.

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Then, the nine column address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

$\overline{RAS}$ and $\overline{CAS}$ address strobes and device control clocks

$\overline{RAS}$ is a control input that latches the states of the row address, $\overline{W}$, $\overline{TRG}$, $\overline{SE}$, $\overline{CAS}$, and DSF onto the chip to invoke the various DRAM and Transfer functions of the SMJ44C251A. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is a control input that latches the states of the column address and DSF to control various DRAM and Transfer functions. $\overline{CAS}$ also acts as an output enable for the DRAM output pins.

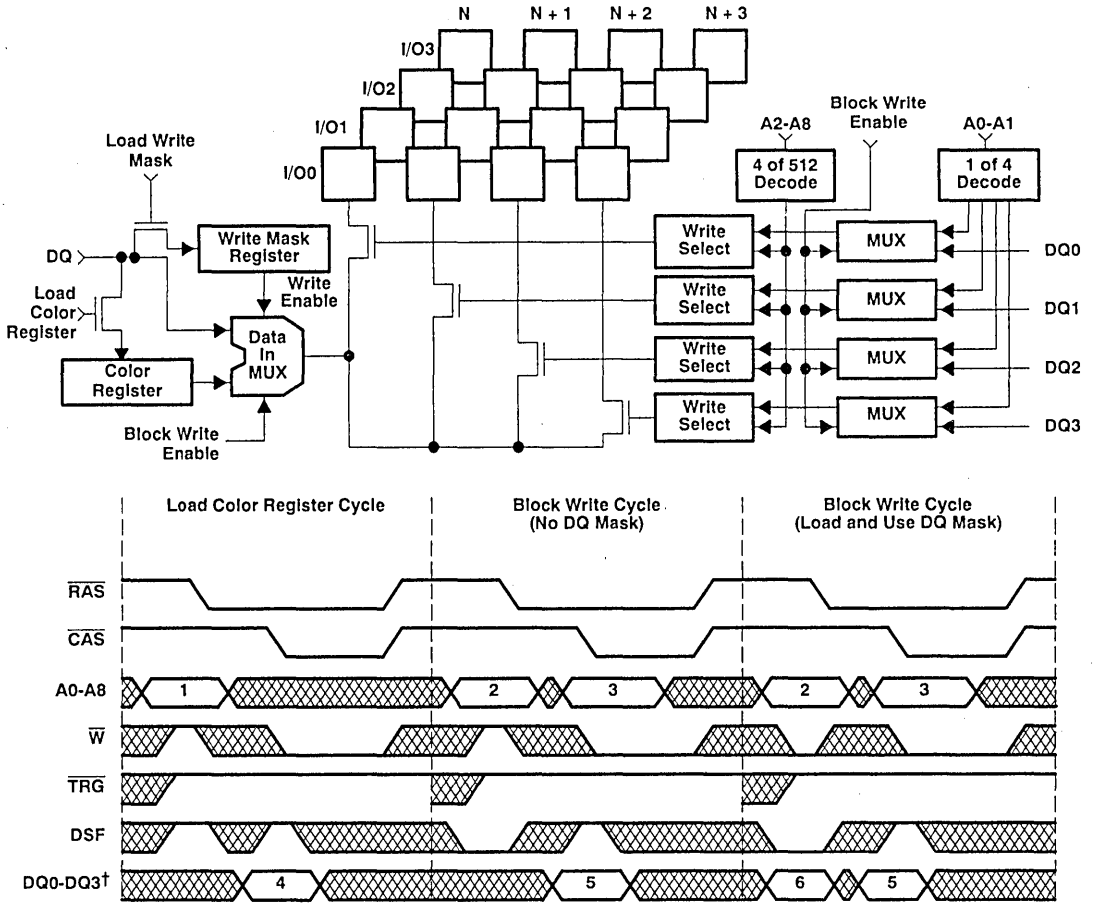
special function select (DSF)

The Special Function Select input is latched on the falling edges of $\overline{RAS}$ and $\overline{CAS}$, similarly to an address, and serves two functions.

First the DSF pin is used to load an on-chip four-bit data, or "color," register via the Load Color Register cycle. The contents of this register can subsequently be written to any combination of four adjacent column memory locations using the 4 × 4 Block Write feature. The Load Color Register cycle is performed using normal write cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Once the color register is loaded, it retains data until power is lost or until another Load Color Register cycle is performed.

After loading the color register, the Block Write cycle can be enabled by holding DSF high on the falling edge of $\overline{CAS}$. During Block Write cycles, only the seven most significant column addresses (A2-A8) are latched on the falling edge of $\overline{CAS}$. The two least significant addresses (A0-A1) are replaced by the four DQ bits, which are also latched on the later of $\overline{CAS}$ or $\overline{W}$ falling. These four bits are used as an address mask and indicate which of the four column address locations addressed by A2-A8 will be written with the contents of the color register during the write cycle, and which ones will not. DQ0 enables a write to column address A1 = low, A0 = low; DQ1 enables a write to A1 = low, A0 = high; DQ2 enables a write to A1 = high, A0 = low; and DQ3 enables a write to A1 = high, A0 = high. A logic high level enables a write and a logic low level disables the write. A maximum of 16 bits can be written to memory during each $\overline{CAS}$ cycle (see Figure 1, Block Write Diagram).

Second, the DSF pin is used to provide an alternate method of performing a transfer write. The alternate transfer write is described in the ***transfer write enable ($\overline{W}$)*** paragraph of this specification.



† DQ0-DQ3 ($\overline{CAS}$) are latched on the later of $\overline{W}$ or $\overline{CAS}$ falling edge. DQ0-DQ3 ($\overline{RAS}$) are latched on $\overline{RAS}$ falling edge.

Legend:

1. Refresh Address
2. Row Address
3. Block Address (A2-A8)
4. Color Register Data
5. Column Mask Data
6. DQ Mask Data

= Don't Care

Figure 1. Block Write Diagram

write enable, write-per-bit enable ($\overline{W}$)

The $\overline{W}$ pin enables data to be written to the DRAM and is also used to select the DRAM write per bit mode of operation. A logic level high on the $\overline{W}$ input selects the read mode and logic low level selects the write mode. In an early write cycle, $\overline{W}$ is brought low before $\overline{CAS}$ and the DRAM output pins (DQ) remain in the high-impedance state for the entire cycle. During DRAM write cycles, holding $\overline{W}$ low on the falling edge of $\overline{RAS}$ will invoke the write-per-bit operation.

When $\overline{W}$ = low on the falling edge of $\overline{RAS}$, the write mask is reloaded. Accordingly, a four-bit binary code (the write-per-bit mask) is input to the device via the random DQ pins and is latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the four random I/Os are written and which are not. After $\overline{RAS}$ has latched the write mask on-chip, input data is driven onto the DQ pins and is latched on the falling edge of the later of $\overline{CAS}$ or $\overline{W}$. If a low was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will not be written to that I/O. If a high was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will be written to that I/O.

See the corresponding timing diagrams for details. IMPORTANT: The write-per-bit operation is invoked only if $\overline{W}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{W}$ is held high on the falling edge of $\overline{RAS}$, write-per-bit is not enabled and the write operation is identical to that of standard × 4 DRAMs.

data I/O (DQ0-DQ3)

DRAM data is written during a write or read-modify-write cycle. The falling edge of $\overline{W}$ strobes data into the on-chip data latches. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with data setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, CAS will already be low. Thus, the data will be strobed-in by $\overline{W}$ with data setup and hold times referenced to this signal.

The three-state output buffers provide direct TTL compatability (no pull-up resistors required) with a fanout of two Series 74/54 TTL loads. Data-out is the same polarity as Data-in. The outputs are in the high impedance (floating) state as long as $\overline{CAS}$ or $\overline{TRG}$ is held high. Data will not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low. Once the outputs are valid, they remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. $\overline{CAS}$ or $\overline{TRG}$ going high returns the outputs to a high-impedance state. In an early write cycle, the outputs are always in the high-impedance state. In a register transfer operation (memory-to-register or register-to-memory), the outputs remain in the high-impedance state for the entire cycle.

enhanced page mode

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ44C251A to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

Enhanced page mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row address setup, row address hold, and address multiplex is thus eliminated, and a memory cycle time reduction of up to 3 × can be achieved, compared to minimum $\overline{RAS}$ cycle times. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and page mode cycle time used. The SMJ44C251A allows a full page (512 cycles) of information to be accessed in read, write, or read-modify-write modes during a single $\overline{RAS}$ low period using relatively conservative page mode cycle times.

During write-per-bit operations, the DQ pins are used to load the write-per-bit mask register described above under the $\overline{W}$ pin description.

During block write operations, the DQ pins are used to load the on-chip color register during the load color register cycle and are also used as a write enable during Block Write cycles.

refresh

A refresh operation must be performed on each row at least once every eight milliseconds to retain data. Since the output buffer is in the high-impedance state (unless $\overline{CAS}$ is applied), the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$. The external row address is ignored and the refresh address is generated internally.

GND(PIN 8)

This pin is reserved for the manufacturer's test operation. It is an input and should be tied to system ground to ensure proper device operation.

IMPORTANT: GND is not connected internally to V_{SS}.

Table 1. Function Table

TYPE†	$\overline{RAS}$ FALL					$\overline{CAS}$ FALL	ADDRESS		DQ0-3		FUNCTION
	$\overline{CAS}$	$\overline{TRG}$	$\overline{W}$	DSF	$\overline{SE}$	DSF	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$‡ $\overline{W}$	
R	L	X§	X	X	X	X	X	X	X	X	$\overline{CAS}$-before-$\overline{RAS}$ refresh
T	H	L	L	X	L	X	Row Addr	Tap Point	X	X	Register to memory transfer (Transfer Write)
T	H	L	L	H	X	X	Row Addr	Tap Point	X	X	Alternate Transfer Write (independent of $\overline{SE}$)
T	H	L	L	L	H	X	Refresh Addr	Tap Point	X	X	Serial Write-mode enable (pseudo-Transfer Write)
T	H	L	H	L	X	X	Row Addr	Tap Point	X	X	Memory to register transfer (Transfer Read)
R	H	H	L	L	X	L	Row Addr	Col Addr	Write Mask	Valid Data	Load and use write mask, write data to DRAM
R	H	H	L	L	X	H	Row Addr	Col A2-A8	Write Mask	Addr Mask	Load and use write mask, Block Write to DRAM
R	H	H	H	L	X	L	Row Addr	Col Addr	X	Valid Data	Normal DRAM read/write (non masked)
R	H	H	H	L	X	H	Row Addr	Col A2-A8	X	Addr Mask	Block Write to DRAM (non masked)
R	H	H	H	H	X	H	Refresh Addr	X	X	Color Data	Load color register

† R = Random access operation; T = Transfer operation.
‡ DQ0-3 are latched on the later of $\overline{W}$ or $\overline{CAS}$ falling edge.
§ X = Don't care.
Addr Mask = 1; write to address location enabled.
Write Mask = 1; write to I/O enabled.

random port to serial port interface

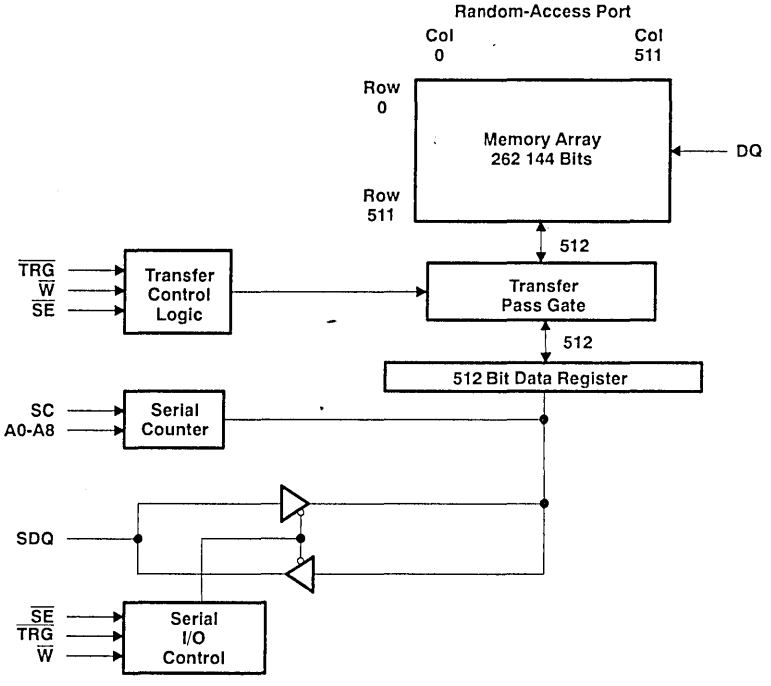


Figure 2. Block Diagram Showing One Random and One Serial I/O Interface

random-address space to serial-address space mapping

The 512 bits in each of the four data registers of the SAM are connected to the 512 column locations of each of the four random I/Os. Data can be accessed in or out of the SAM starting at any of the 512 data bit locations. This start location is selected by addresses A0 through A8 on the falling edge of $\overline{CAS}$ during any transfer cycle. The SAM is accessed starting from the selected start address, proceeding from the lowest to the highest significant bits. After the most significant bit position (511) is accessed, the serial counter wraps around such that bit 0 is accessed on the next clock pulse. The selected start address is stored and used for all subsequent transfer cycles until $\overline{CAS}$ is again brought low during any transfer cycle. Thus, the start address can be set once and $\overline{CAS}$ held high during all subsequent transfer cycles and the start address point will not change regardless of data present on A0 through A8.

transfer operations

As illustrated in Table 1, the SMJ44C251A supports four basic transfer modes of operation:

1. Normal Write Transfer (SAM to DRAM)
2. Alternate Write Transfer (independent of the state of $\overline{SE}$)
3. Pseudo Write Transfer (switches serial port from serial out mode to serial in mode. No actual data transfer takes place between the DRAM and the SAM.)
4. Normal Read Transfer (transfer entire contents of DRAM to SAM)

transfer register select ($\overline{TRG}$)

Transfer operations between the memory array and the data registers are invoked by bringing $\overline{TRG}$ low before $\overline{RAS}$ falls. The states of $\overline{W}$, $\overline{SE}$, and DSF, which are also latched on the falling edge of $\overline{RAS}$, determine which transfer operation will be invoked. (See Table 2.)

During read transfer cycles, $\overline{TRG}$ going high causes the addressed row of data to be transferred into the data register. Although the previous data in the data register is overwritten, the last bit of data appearing at SDQ before $\overline{TRG}$ goes high will remain valid until the first positive transition of SC after $\overline{TRG}$ goes high. The data at SDQ will then switch to new data beginning from the selected start, or *tap*, position.

transfer write enable ($\overline{W}$)

In the register transfer mode, $\overline{W}$ determines whether a read or a write transfer will occur. To perform a write transfer, $\overline{W}$ and $\overline{SE}$ are held low as $\overline{RAS}$ falls. If $\overline{SE}$ is high during this transition, no transfer of data from the data register to the memory array occurs, but the SDQs are put into the input mode. This allows serial data to be input into the SAM. An alternative way to perform the transfer write cycle is by holding DSF high on the falling edge of $\overline{RAS}$. In this way, the state of $\overline{SE}$ is a Don't Care as $\overline{RAS}$ falls. To perform a read transfer operation, $\overline{W}$ is held high and $\overline{SE}$ is a Don't Care as $\overline{RAS}$ falls. This cycle also puts the SDQs into the read mode, allowing serial data to be shifted out of the data register. (See Table 2.)

column enable ($\overline{CAS}$)

If $\overline{CAS}$ is brought low during a control cycle, the address present on the pins A0 through A8 will become the new register start location. If $\overline{CAS}$ is held high during a control cycle, the previous tap address will be retained from the last transfer cycle in which $\overline{CAS}$ went low to set the tap address.

addresses (A0 through A8)

Nine address bits are required to select one of the 512 possible rows involved in the transfer of data to or from the data registers. The states of A0-A8 are latched on the fallling edge of $\overline{RAS}$ to select one of 512 rows for the transfer operation.

To select one of the 512 positions in the SAM from which the first serial data will be accessed, the appropriate 9-bit column address (A0-A8) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and start (tap) position need not be supplied every cycle, only when changing to a different start position.

special function input (DSF)

In the write transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ permits use of an alternate mode of transfer write. This mode allows $\overline{SE}$ to be high on the falling edge of $\overline{RAS}$ without permitting a pseudo write transfer, with the serial port disabled during the entire transfer write cycle.

serial access operation

Refer to Tables 2 and 3 for the following discussion on serial access operation.

serial clock (SC)

Data (SDQ) is accessed in or out of data registers on the rising edge of SC. The SMJ44C251A is designed to work with a wide range of clock duty cycles to simplify system design. Since the data registers comprising the SAM are of static design, there are no SAM refresh requirements and there is no minimum SC clock operating frequency.

serial data input/output (SDQ0-SDQ3)

SD and SQ share a common I/O pin. Data is input to the device when $\overline{SE}$ is low during write mode and data is output from the device when $\overline{SE}$ is low during read mode. The data in the SAM will be accessed in the direction from least significant bit to most significant bit. The data registers operate modulo 512. Thus, after bit 511 is accessed, the next bits to be accessed will be bits 00, 01, 02, and so on.

serial enable ($\overline{SE}$)

The Serial Enable pin has two functions: first, it is latched on the falling edge of $\overline{RAS}$, with both $\overline{TRG}$ and $\overline{W}$ low to select one of the transfer functions (see Table 2). If $\overline{SE}$ is low during this transition, then a transfer write occurs. If $\overline{SE}$ is high as $\overline{RAS}$ falls and DSF is low, then a write mode control cycle is performed. The function of this cycle is to switch the SDQs from the output mode to the input mode, thus allowing data to be shifted into the data register. NOTE: All transfer read and serial mode enable (pseudo transfer write) operations will perform a memory refresh operation on the selected row.

Second, during serial access operations, $\overline{SE}$ is used as an SDQ enable/disable. In the write mode, $\overline{SE}$ is used as an input enable. $\overline{SE}$ high disables the input and $\overline{SE}$ low enables the input. To take the device out of the write mode and into the read mode, a transfer read cycle must be performed. The read mode allows data to be accessed from the data register. While in the read mode, $\overline{SE}$ high disables the output and $\overline{SE}$ low enables the output.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is NOT disabled. Thus, external SC pulses will increment the internal serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low since the serial clock input buffer and the serial address counter are not disabled by $\overline{SE}$.

Table 2. Transfer Operation Logic

$\overline{TRG}$	$\overline{W}$	$\overline{SE}$	DSF	MODE
L	L	L	X	Register to memory (write) transfer
L	L	X	H	Alternate register to memory transfer
L	L	H	L	Serial write mode enable
L	H	X	L	Memory to register (read) transfer

NOTE: Above logic states are assumed valid on the falling edge of $\overline{RAS}$.

Table 3. Serial Operation Logic

LAST TRANSFER CYCLE	$\overline{SE}$	SDQ
Alternate register to memory	H	Input Disabled
Serial write mode enable†	L	Input Enable
Serial write mode enable†	H	Input Disable
Memory to register	L	Output Enabled
Memory to register	H	Hi-Z

†Pseudo transfer write

powerup

To achieve proper device operation, an initial pause of 200 μs is required after power-up, followed by a minimum of eight $\overline{RAS}$ cycles or eight $\overline{CAS}$-before-$\overline{RAS}$ cycles, a memory-to-register transfer cycle and two SC cycles.

absolute maximum ratings over operating free-air temperature†

Voltage on any pin except DQ and SDQ (See Note 1) ..... – 1 V to 7 V
Voltage on DQ and SDQ (see Note 1) ..... – 1 V to V_{CC}
Voltage range on V_{CC} (see Note 1) ..... 0 V to 7 V
Short circuit output current (per output) ..... 50 mA
Power dissipation ..... 1 W
Operating temperature range ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	SMJ44C251A-1, SMJ44C251A-2	4.75	5	5.25	V
		SMJ44C251A-10, SMJ44C251A-12	4.5	5	5.5	
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage		3.5		V_{CC}	V
V_{IL}	Low-level input voltage (see Note 2)		– 1		0.5	V
T_A	Operating free-air temperature		– 55			°C
T_C	Operating case temperature				125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = – 5 mA	2.4		V
V_{OL}	Low level output voltage (see Note 4)	I_{OL} = 4.2 mA		0.4	V
I_L	Input leakage current	V_I = 0 to 5.8 V, V_{CC} = 5 V All other pins open		±1.0	μA
I_O	Output leakage current (see note 3)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V		±10	μA

PARAMETER			SAM PORT	SMJ44C251A-1 SMJ44C251A-10		SMJ44C251A-2 SMJ44C251A-12		UNIT
				MIN	MAX	MIN	MAX	
I_{CC1}	Operation current $t_{c(RW)}$ = Minimum	(see Note 5)	Standby		100		90	mA
I_{CC1A}	$t_{c(SC)}$ = Minimum		Active		110		100	
I_{CC2}	Standby current, All clocks = V_{CC}		Standby		15		15	
I_{CC2A}	$t_{c(SC)}$ = Minimum		Active		35		35	
I_{CC3}	$\overline{RAS}$-only refresh current, $t_{c(RW)}$ = Minimum		Standby		100		90	
I_{CC3A}	$t_{c(SC)}$ = Minimum		Active		110		100	
I_{CC4}	Page mode current, $t_{c(P)}$ = Minimum		Standby		65		60	
I_{CC4A}	$t_{c(SC)}$ = Minimum		Active		70		65	
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ current, $t_{c(RW)}$ = Minimum		Standby		90		80	
I_{CC5A}	$t_{c(SC)}$ = Minimum		Active		110		100	
I_{CC6}	Data transfer current, $t_{c(RW)}$ = Minimum		Standby		100		90	
I_{CC6A}	$t_{c(SC)}$ = Minimum		Active		110		100	

NOTES: 3. $\overline{SE}$ is disabled for SDQ output leakage tests.

4. The SMJ44C251A One Megabit Video Ram exhibits simultaneous switching noise as described in Texas Instruments' *Advanced CMOS Logic Designer's handbook*. This phenomenon exhibits itself upon the DQ pins when the SDQ pins are switched and upon the SDQ pins when DQ pin are switched. This may cause the VOL to exceed the data book limit for a short period of time, depending upon output loading and temperature. Care should be taken to provide proper termination, decoupling, and layout of the device to minimize simultaneous switching effects.

5. I_{CC} (standby) vs I_{CCA} (active) denotes the following:
I_{CC} (standby) denotes that the SAM port is inactive (standby) and the DRAM port is active (except for I_{CC2}).
I_{CCA} (active) denotes that the SAM port is active and the DRAM port is active (except for I_{CC2}).
I_{CC} is measured with no load on DQ or SDQ pins.

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capacitance over recommended ranges of supply voltage and operating temperature, f = 1 MHz (see Note 6)†

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		9	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		9	pF
$C_{i(W)}$	Input capacitance, write enable input		9	pF
$C_{i(SC)}$	Input capacitance, serial clock		9	pF
$C_{i(DSF)}$	Input capacitance, special function		9	pF
$C_{i(SE)}$	Input capacitance, serial enable		9	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		9	pF
$C_{o(O)}$	Output capacitance, SDQ and DQ		9	pF

† Capacitance is sampled only at initial design and after any major change.

NOTE 6: V_{CC} equal to 5 V ± 0.5 V for SMJ44C251A-10 and SMJ44C251A-12, 5 V ± 0.25 V for SMJ44C251A-1 and SMJ44C251A-2. The bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating temperature (see Note 7)

NO.†	PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ44C251A-1 SMJ44C251A-10		SMJ44C251A-2 SMJ44C251A-12		UNIT
					MIN	MAX	MIN	MAX	
1	$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{d(RLCL)}$ = MAX	t_{CAC}		25		30	ns
2	$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{CAA}		50		60	ns
3	$t_{a(CP)}$	Access time from $\overline{CAS}$ high	$t_{d(RLCL)}$ = MIN	t_{CAP}		55		65	ns
4	$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MIN	t_{RAC}		100		120	ns
5	$t_{a(G)}$	Access time of Q from $\overline{TRG}$ low		t_{OEA}		25		30	ns
6	$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 50 pF	t_{SCA}		30		35	ns
7	$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 50 pF	t_{SEA}		20		25	ns
9	$t_{dis(CH)}$	Random output disable time from $\overline{CAS}$ high (see Note 8)	C_L = 100 pF	t_{OFF}	0	20	0	20	ns
10	$t_{dis(G)}$	Random output disable time from $\overline{TRG}$ high (see Note 8)	C_L = 100 pF	t_{OEZ}	0	20	0	20	ns
11	$t_{dis(SE)}$	Serial output disable time from $\overline{SE}$ high (see Note 8)	C_L = 50 pF	t_{SEZ}	0	20	0	20	ns

† Numbering scheme intentionally skips numbers to allow for additional parameters specified in the SMJ44C251 data sheet.

NOTES: 7. Switching times assume C_L = 100 pF unless otherwise noted (see Figure 3).

8. Disable times are specified when the output is no longer driven.

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timing requirements over recommended ranges of supply voltage and operating temperature†

NO.	PARAMETER		ALT. SYMBOL	SMJ44C251A-1 SMJ44C251A-10		SMJ44C251A-2 SMJ44C251A-12		UNIT
				MIN	MAX	MIN	MAX	
12	$t_{c(rd)}$	Read cycle time (see Note 9)	t_{RC}	190		220		ns
13	$t_{c(W)}$	Write cycle time	t_{WC}	190		220		ns
14	$t_{c(rdW)}$	Read-modify-write cycle time	t_{RWC}	250		290		ns
15	$t_{c(P)}$	Page-mode read, write cycle time	t_{PC}	60		70		ns
16	$t_{c(RDWP)}$	Page-mode read-modify-write cycle time	t_{RWC}	105		125		ns
17	$t_{c(TRD)}$	Transfer read cycle time	t_{RC}	190		220		ns
18	$t_{c(TW)}$	Transfer write cycle time	t_{WC}	190		220		ns
18a	$t_{c(TW)M}$	Transfer write cycle time, multiple transfer operation		320		350		ns
19	$t_{c(SC)}$	Serial clock cycle time (see Note 10)	t_{SCC}	30		35		ns
20	$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	20		30		ns
21	$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 11)	t_{CAS}	25	75 000	30	75 000	ns
22	$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	80		90		ns
23	$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 12)	t_{RAS}	100	75 000	120	75 000	ns
23a	$t_{w(RL)M}$	Pulse duration, $\overline{RAS}$ low, multiple transfer write operation		185		195		ns
24	$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	t_{WP}	25		25		ns
25	$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		25		30		ns
26	$t_{w(SCH)}$	Pulse duration, SC high	t_{SC}	10		12		ns
27	$t_{w(SCL)}$	Pulse duration, SC low	t_{SCP}	10		12		ns
28	$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
29	$t_{su(SFC)}$	DSF setup time before $\overline{CAS}$ low		0		0		ns
30	$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
31	$t_{su(WMR)}$	$\overline{W}$ setup time before $\overline{RAS}$ low	t_{WSR}	0		0		ns
32	$t_{su(DQR)}$	DQ setup time before $\overline{RAS}$ low (write mask operation)	t_{MS}	0		0		ns
33	$t_{su(TRG)}$	$\overline{TRG}$ setup time before $\overline{RAS}$ low	t_{TLS}	0		0		ns
34	$t_{su(SE)}$	$\overline{SE}$ setup time before $\overline{RAS}$ low (see Note 22)	t_{ESR}	0		0		ns
35	$t_{su(SFR)}$	DSF setup time before $\overline{RAS}$ low		0		0		ns
36	$t_{su(DCL)}$	Data setup time before $\overline{CAS}$ low	t_{DSC}	0		0		ns
37	$t_{su(DWL)}$	Data setup time before $\overline{W}$ low	t_{DSW}	0		0		ns
38	$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
39	$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
40	$t_{su(WCH)}$	Write setup time before $\overline{CAS}$ high	t_{CWL}	25		30		ns
41	$t_{su(WRH)}$	Write setup time before $\overline{RAS}$ high	t_{RWL}	25		30		ns
42	$t_{su(SDS)}$	SD setup time before SC high	t_{SDS}	3		3		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. All cycle times assume t_t = 5 ns.

10. When the odd tap is used (tap address can be 0-511, and odd taps are 1,3,5, etc.), the cycle time for SC in the first serial data out cycle needs be 70 ns minimum.
11. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].
12. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

ADVANCE INFORMATION

timing requirements over recommended ranges of supply range and operating temperature (continued)†

NO.	PARAMETER		ALT. SYMBOL	SMJ44C251A-1 SMJ44C251A–10		SMJ44C251A-2 SMJ44C251A–12		UNIT
				MIN	MAX	MIN	MAX	
43	$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		ns
44	$t_{h(SFC)}$	DSF hold time after $\overline{CAS}$ low		20		20		ns
45	$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		ns
46	$t_{h(TRG)}$	$\overline{TRG}$ hold time after $\overline{RAS}$ low	t_{TLH}	15		15		ns
47	$t_{h(SE)}$	$\overline{SE}$ hold time after $\overline{RAS}$ low (see Note 22)	t_{REH}	15		15		ns
48	$t_{h(RWM)}$	$\overline{W}$ hold time after $\overline{RAS}$ low	t_{RWH}	15		15		ns
49	$t_{h(RDQ)}$	DQ hold time after $\overline{RAS}$ low (write mask operation)	t_{MH}	15		15		ns
50	$t_{h(SFR)}$	DSF hold time after $\overline{RAS}$ low		15		15		ns
51	$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low (see Note 13)	t_{AR}	45		45		ns
52	$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	20		25		ns
53	$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 13)	t_{DHR}	45		50		ns
54	$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	20		25		ns
55	$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ (see Note 14)	t_{RCH}	0		0		ns
56	$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ (see Note 14)	t_{RRH}	10		10		ns
57	$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	30		35		ns
58	$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 13)	t_{WCR}	50		55		ns
59	$t_{h(SDS)}$	SD hold time after SC high	t_{SDH}	5		5		ns
60	$t_{h(SHSQ)}$	SQ hold time after SC high	t_{SOH}	5		5		ns
61	$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		ns
62	$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
63	$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		ns
64	$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Notes 15 and 16)	t_{CWD}	55		65		ns
65	$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 17)	t_{RCD}	25	75	25	90	ns
66	$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	50		60		ns
67	$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 15)	t_{RWD}	130		155		ns
68	$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 15)	t_{AWD}	85		100		ns
69	$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 18)	t_{CHR}	25		25		ns
70	$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 18)	t_{CSR}	10		10		ns
71	$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 18)	t_{RPC}	10		10		ns
72	$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high	t_{CTH}	25		30		ns
73	$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ (see Note 15)		25		30		ns
74	$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high	t_{RTH}	90		95		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 13. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
14. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
15. Read-modify-write operation only.
16. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
17. Maximum value specified only to guarantee $\overline{RAS}$ access time.
18. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating temperature (concluded)†

NO.	PARAMETER		ALT. SYMBOL	SMJ44C251A-1 SMJ44C251A-10		SMJ44C251A-2 SMJ44C251A-12		UNIT
				MIN	MAX	MIN	MAX	
76	$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 19)	t_{RSD}	130		140		ns
77	$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 19)	t_{CSD}	40		45		ns
78	$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 19 and 20)	t_{TSL}	15		20		ns
79	$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 19)	t_{TRD}	−10		−10		ns
80	$t_{d(SCRL)}$	Delay time, SC high to $\overline{RAS}$ low (see Notes 21 and 22)	t_{SRS}	10		20		ns
81	$t_{d(SCSE)}$	Delay time, SC high to $\overline{SE}$ high in serial input mode		20		20		ns
82	$t_{d(RHSC)}$	Delay time, $\overline{RAS}$ high to SC high (see Note 22)	t_{SRD}	25		30		ns
83	$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 23)	t_{TRP}	$t_{w(RH)}$		$t_{w(RH)}$		ns
84	$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 23)	t_{TSD}	35		40		ns
85	$t_{d(SESC)}$	Delay time, $\overline{SE}$ low to SC high (see Note 24)	t_{SWS}	10		15		ns
88	$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8	ms

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 19. Memory to register (read) transfer cycles only.
20. In a transfer read cycle, the state of SC when $\overline{TRG}$ rises is a Don't Care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{TRG}$ goes high.
21. In a transfer write cycle, the state of SC when $\overline{RAS}$ falls is a Don't Care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{RAS}$ goes low.
22. Register to memory (write) transfer cycles only.
23. Memory to register (read) and register to memory (write) transfer cycles only.
24. Serial data-in cycles only.
25. System transition times (rise and fall) are to be a minimum of 3 ns and a maximum of 50 ns.

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

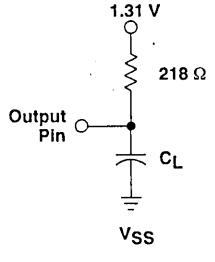
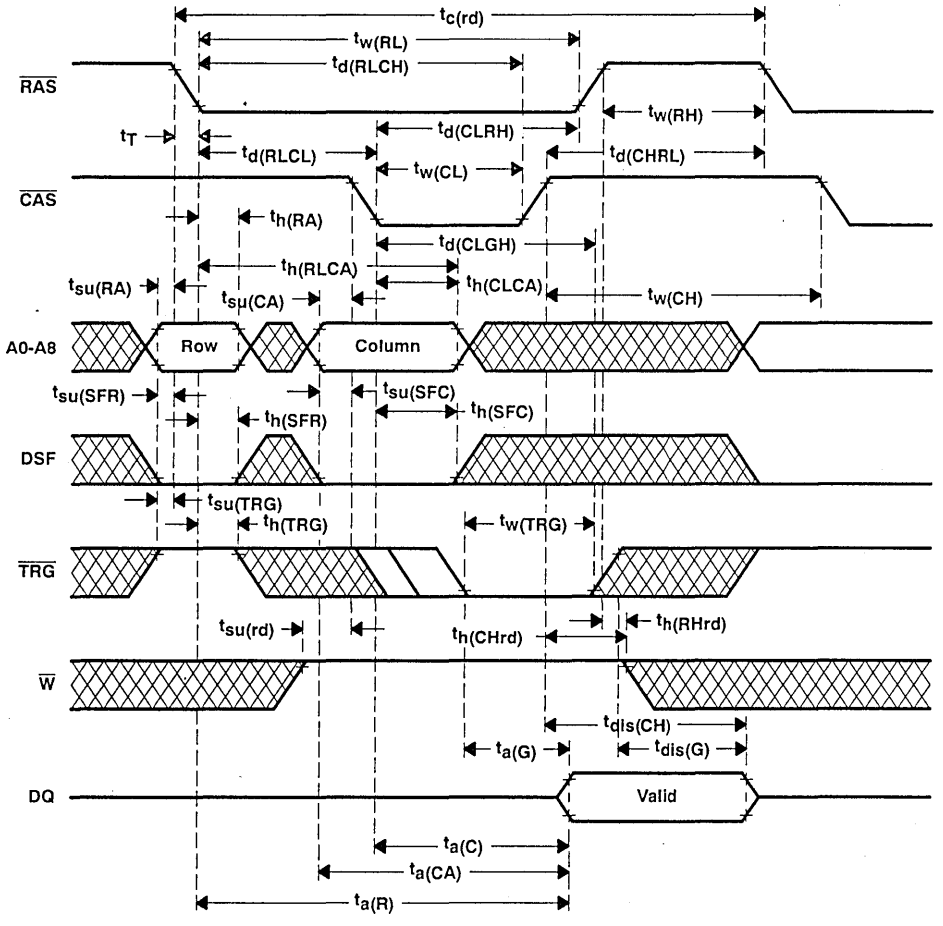
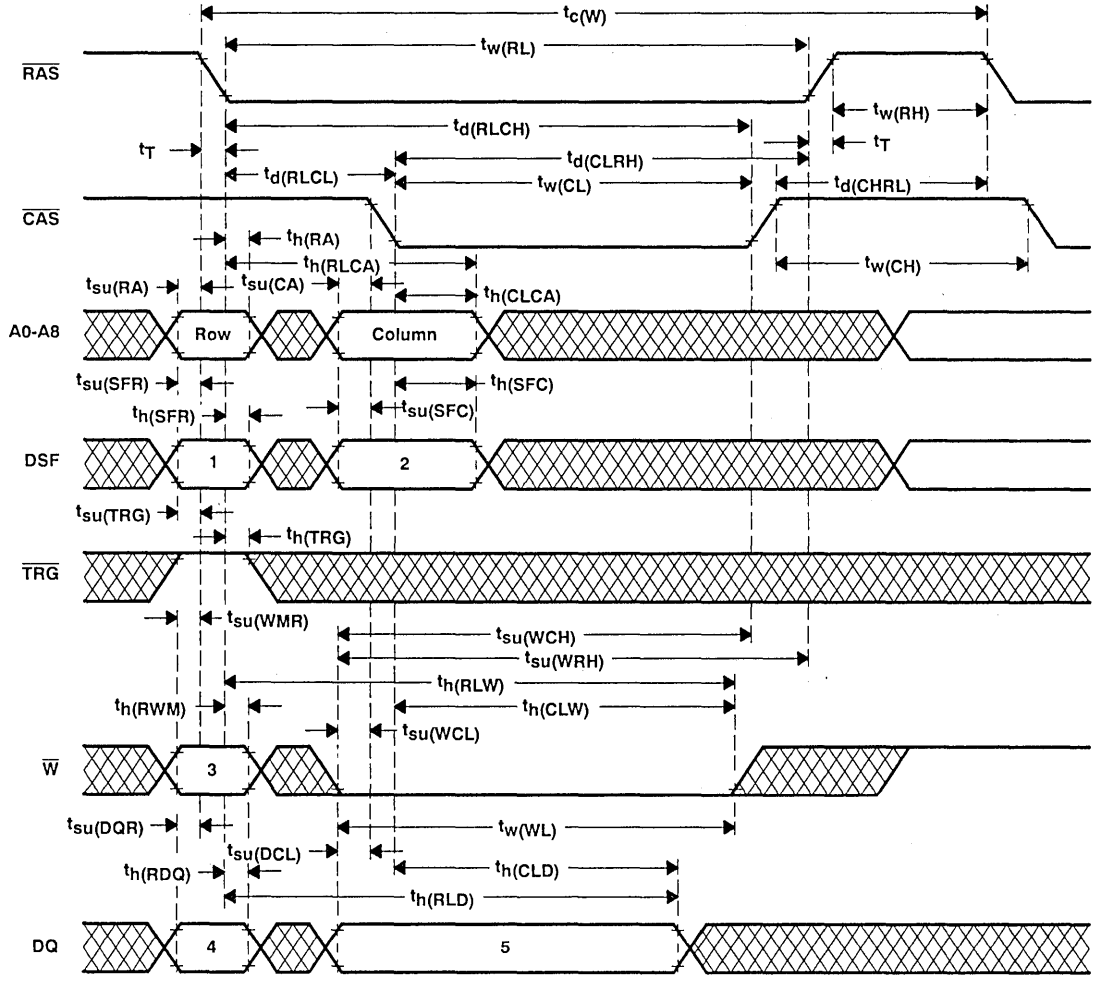


Figure 3. Load Circuit

read cycle timing

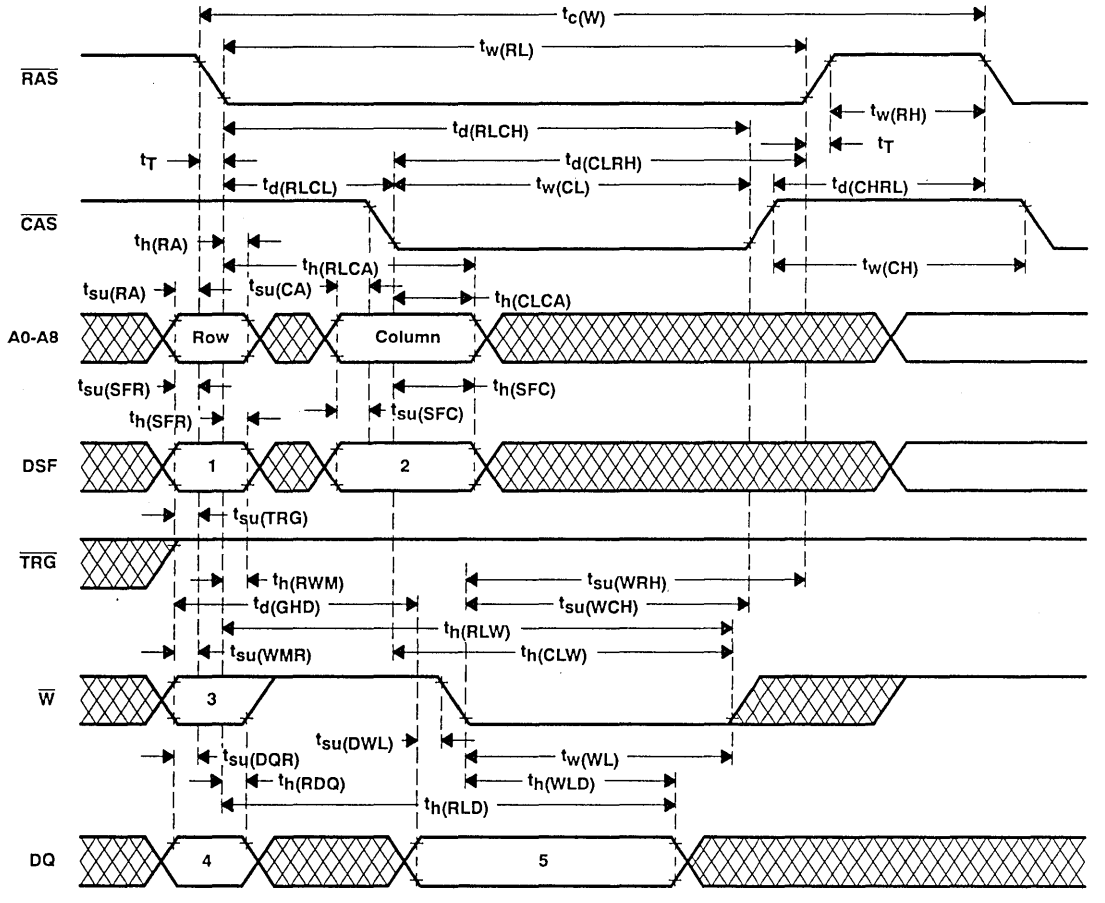


early write cycle timing



NOTE 26: See "Write Cycle State" Table for the logic state of "1", "2", "3", "4", and "5".

delayed write cycle timing

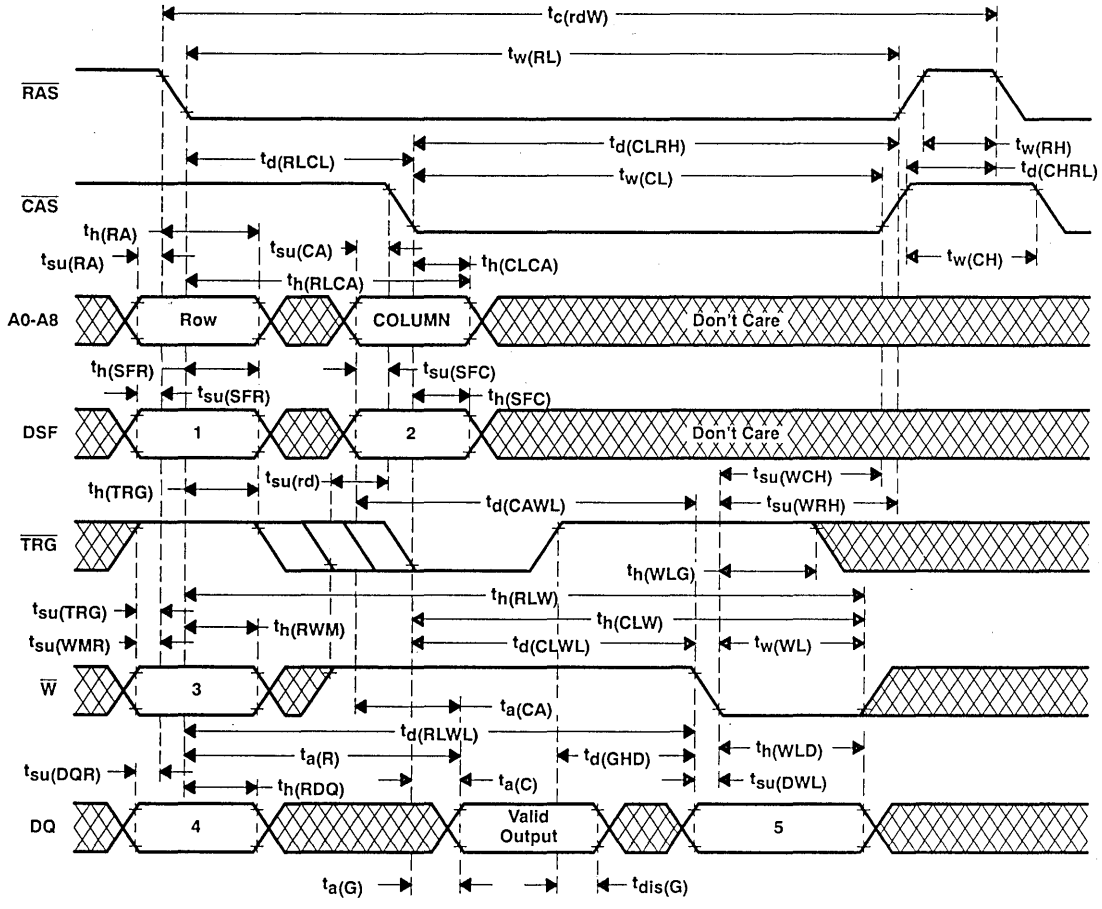


NOTE 26: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

write cycle state table

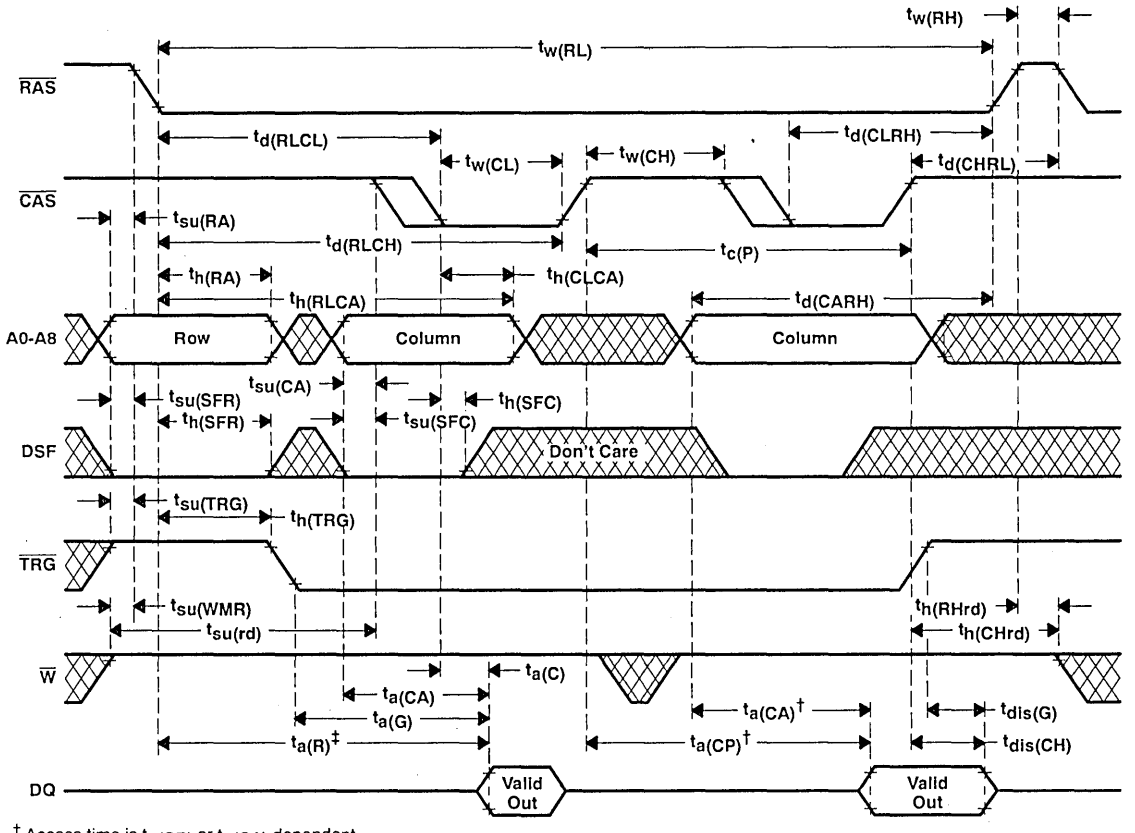
CYCLE	STATE				
	1	2	3	4	5
Write mask load/use write DQs to I/Os	L	L	L	Write Mask	Valid Data
Write mask load/use block write	L	H	L	Write Mask	ADDR Mask
Load color register on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	H	H	Don't Care	Color Data
Write mask disabled, block write to all I/Os	L	H	H	Don't Care	ADDR Mask
Normal early or late write operation	L	L	H	Don't Care	Valid Data

read-write/read-modify-write cycle timing



NOTE 27: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5". Same logic as delayed write cycle.

enhanced page-mode read cycle timing

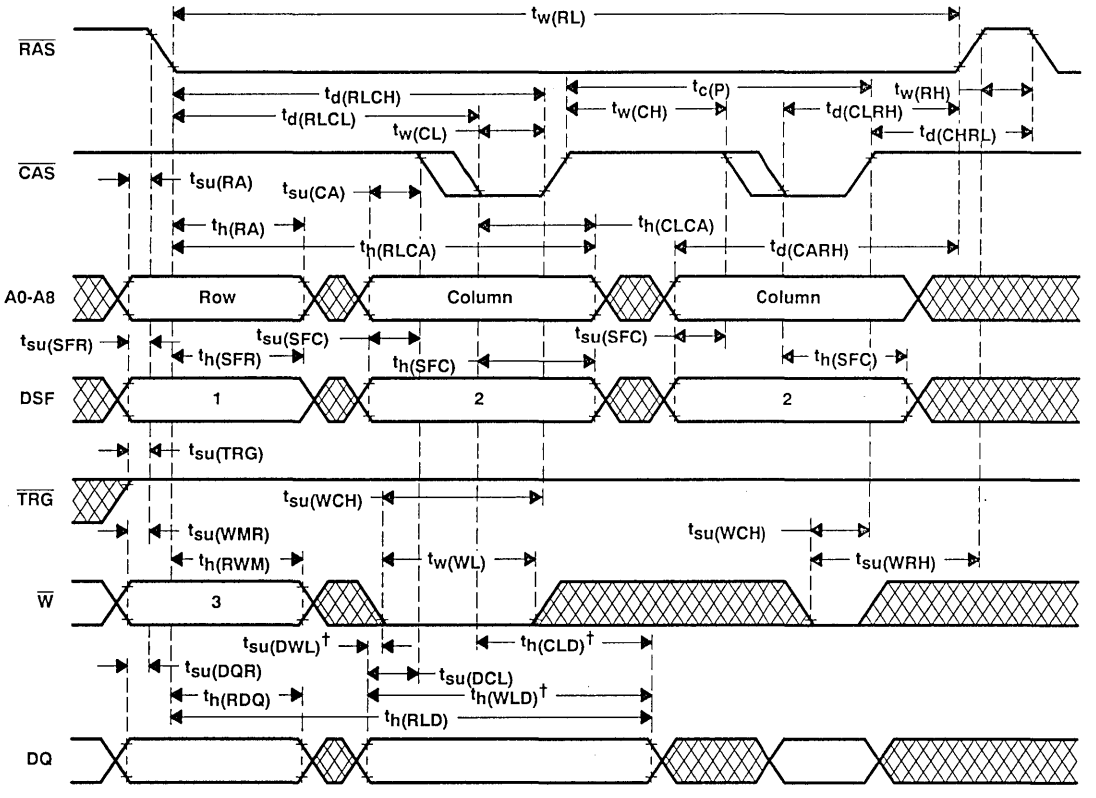


† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

‡ Output may go from high-impedance state to an invalid data state prior to the specified access time.

NOTE 28: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edges of $\overline{RAS}$ and $\overline{CAS}$ to select the desired write mode (normal, block write, etc.).

enhanced page mode write cycle timing

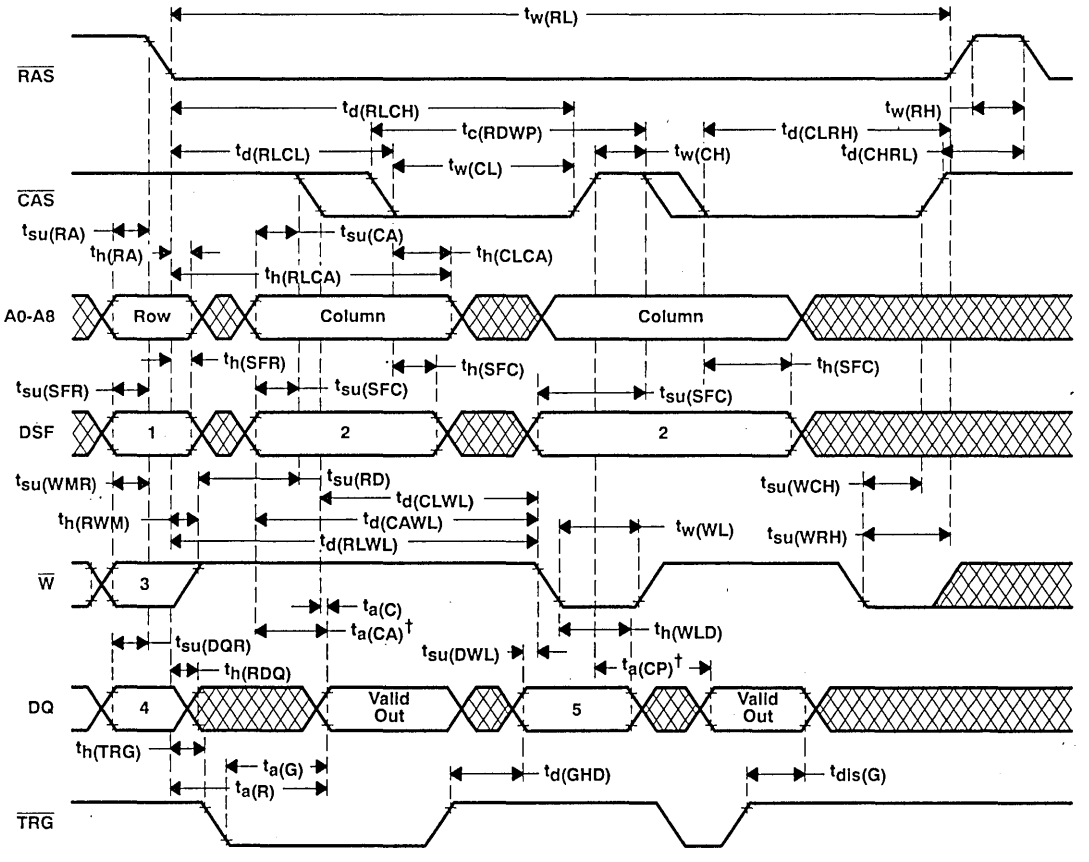


† Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

NOTES: 26. See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

29. A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used, to guarantee page-mode cycle time. If the early write cycle timing is used, the state of $\overline{TRG}$ is a Don't Care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

enhanced page-mode read-modify-write cycle timing

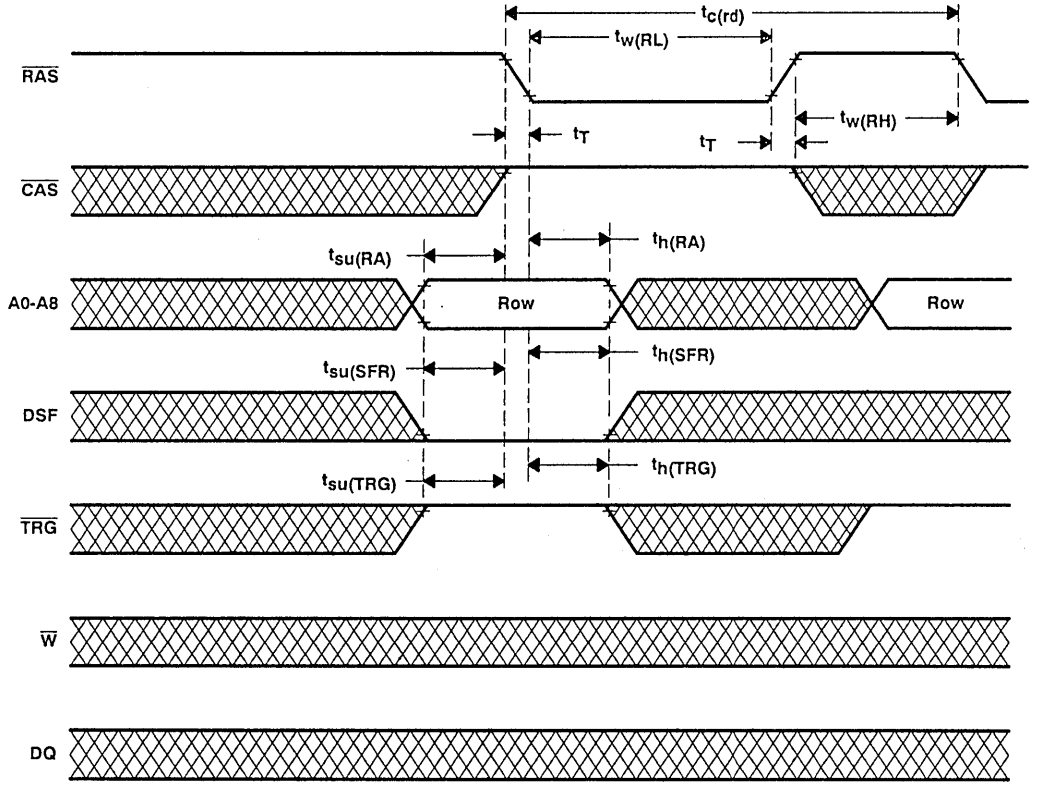


† Output may go from the high-impedance state to an invalid data state prior to the specified access time.

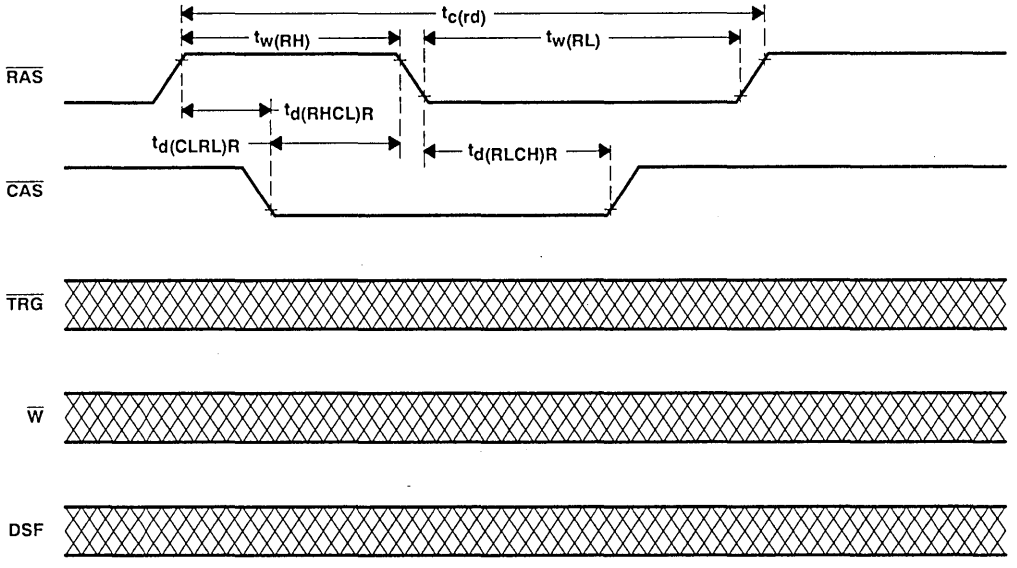
NOTES: 26. See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

30. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

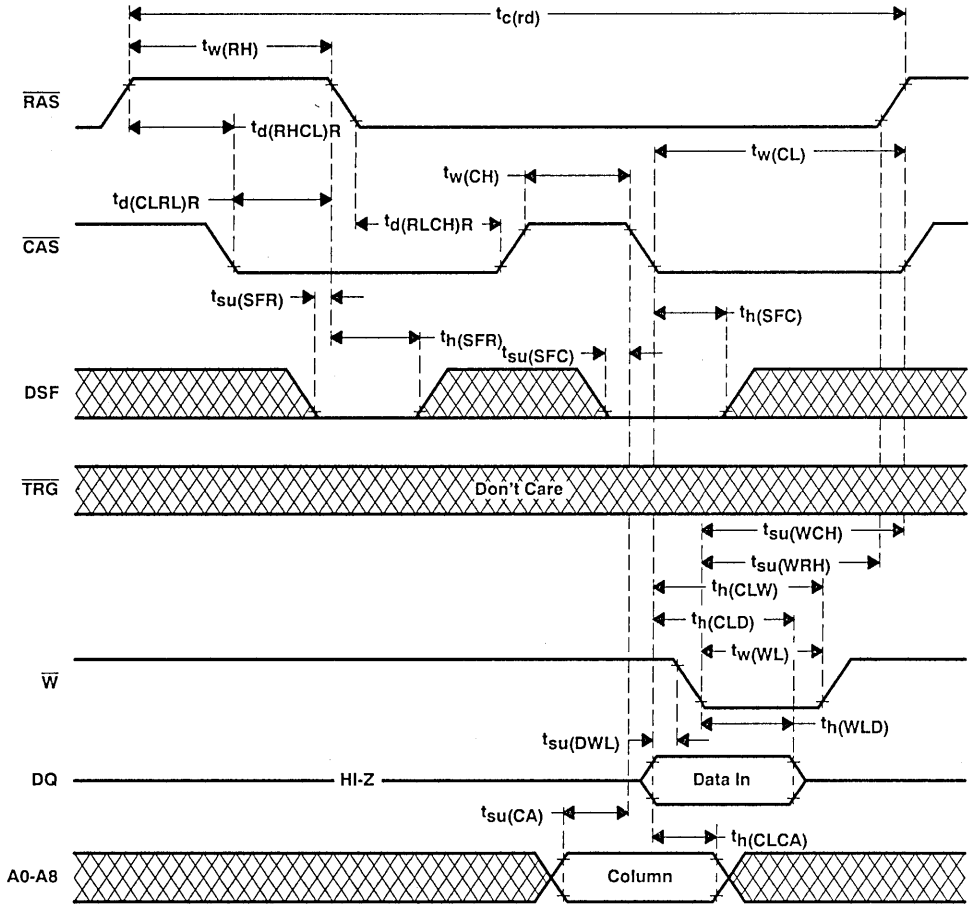
$\overline{\text{RAS}}$-only refresh timing



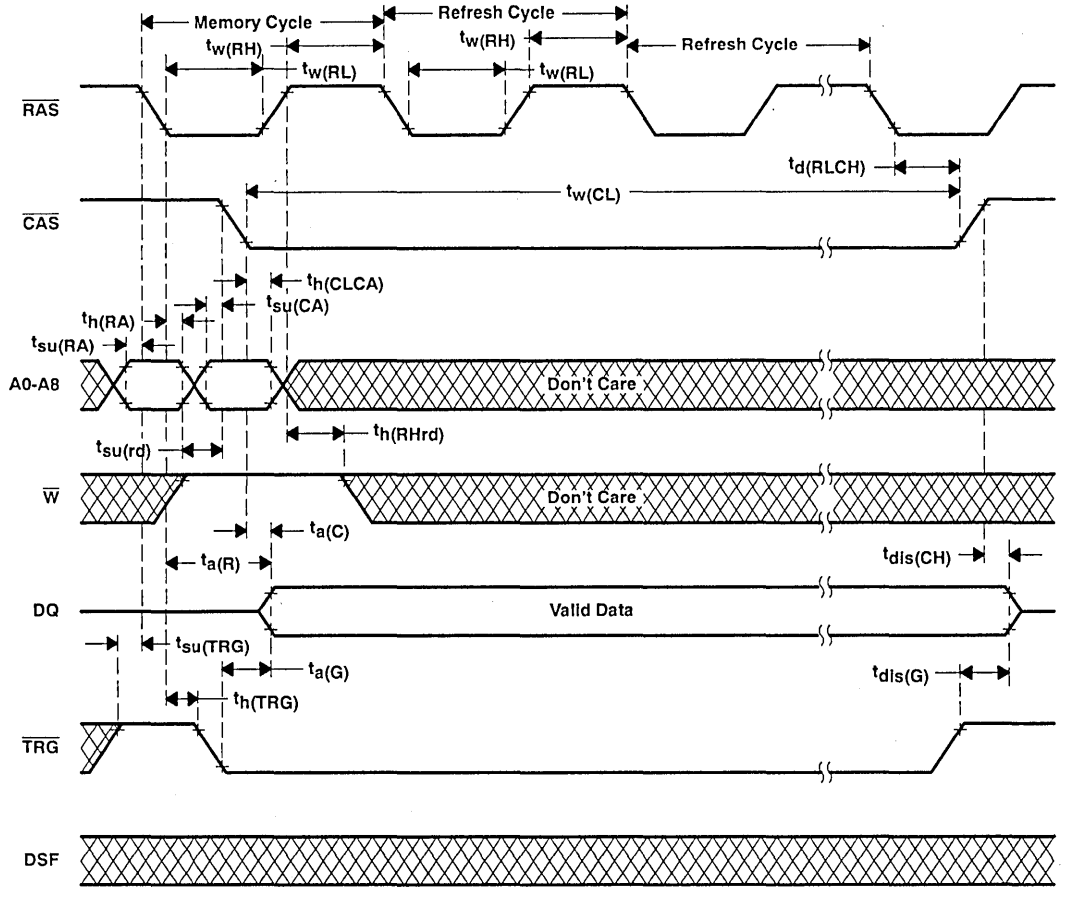
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh



$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test timing

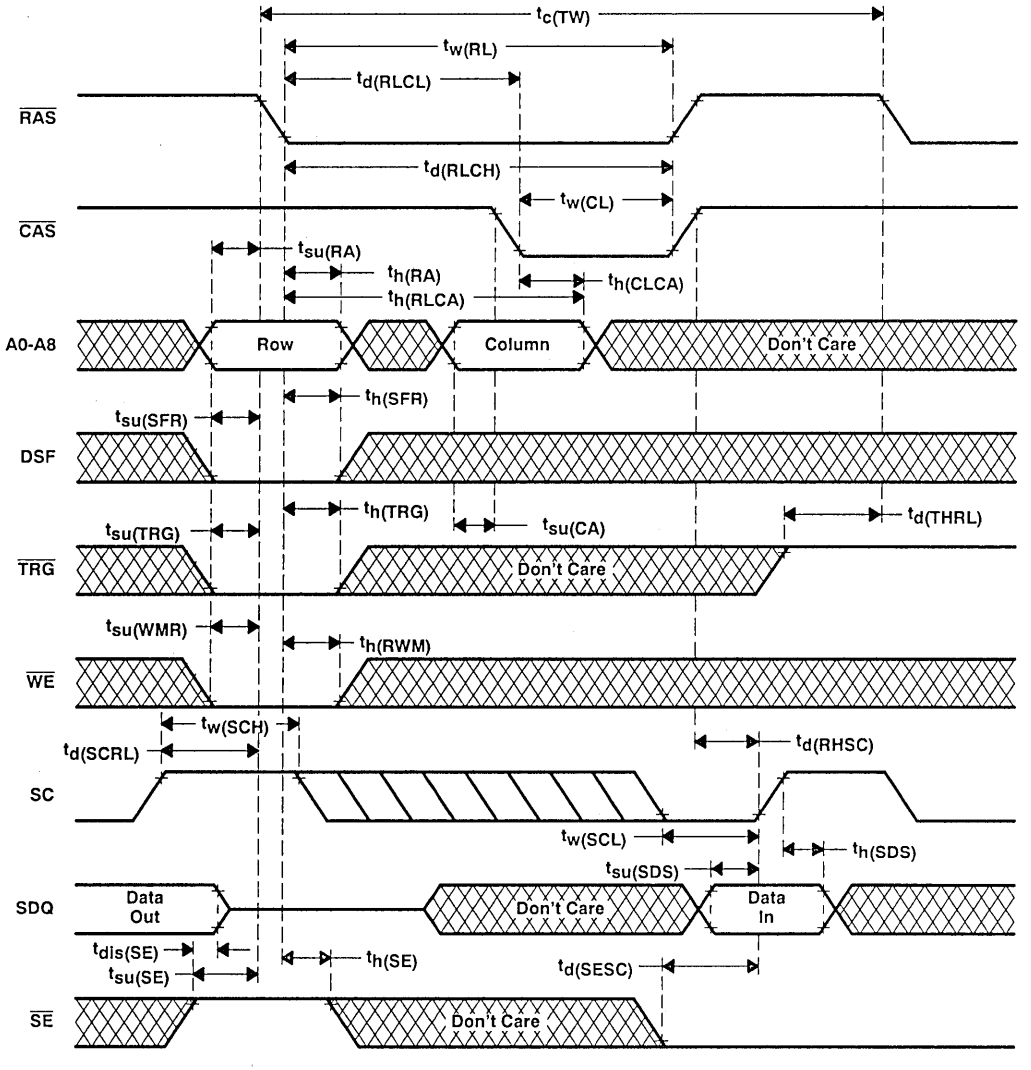


hidden refresh cycle timing



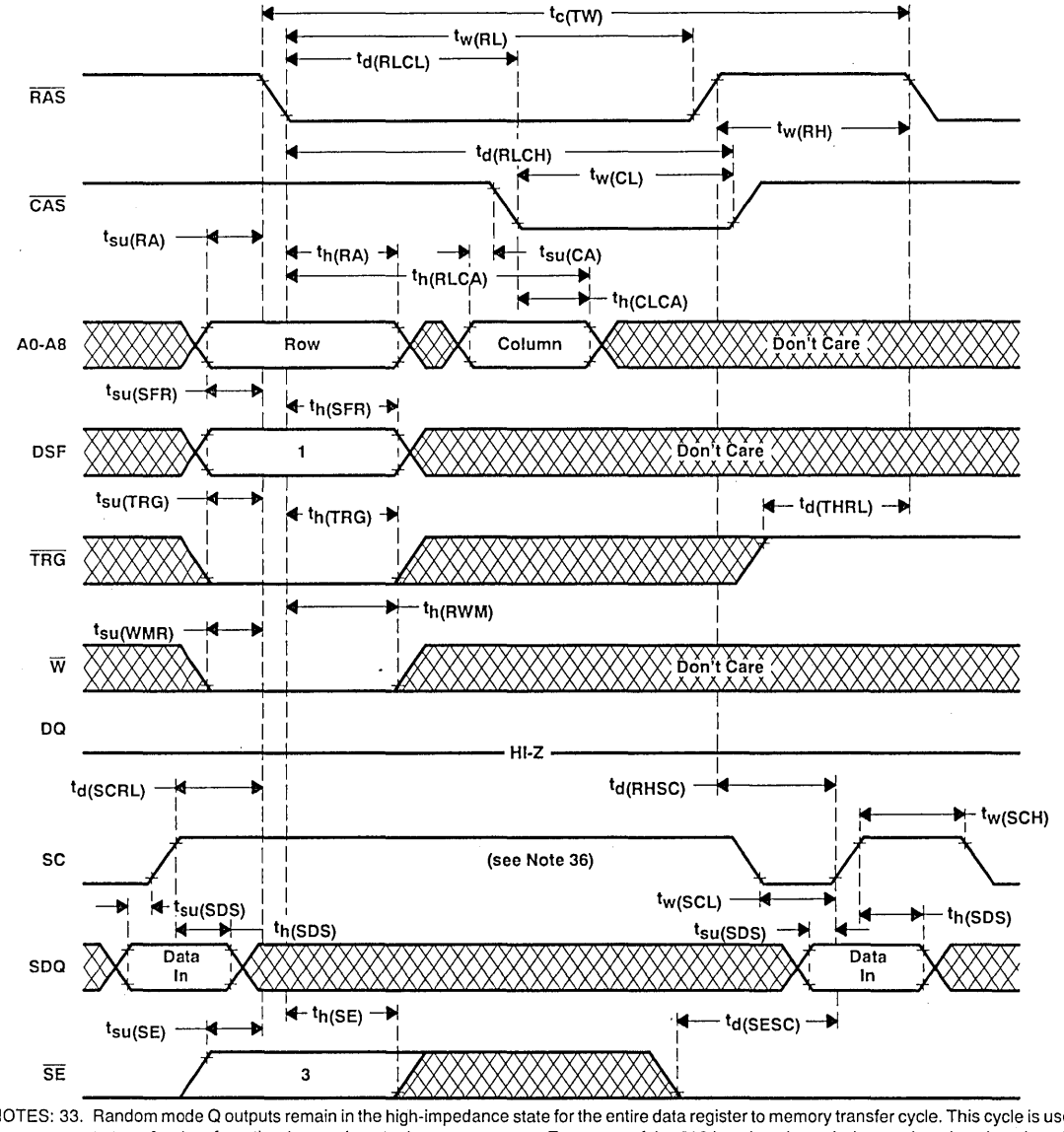
write-mode control pseudo write transfer timing

The write-mode control cycle is used to change the SDQs from the output mode to the input mode. This allows serial data to be written into the data register. The diagram below assumes that the device was originally in the serial read mode.



NOTES: 31. Random-mode Q outputs remain in the high-impedance state for the entire write-mode control.
32. $\overline{SE}$ must be high as $\overline{RAS}$ falls in order to perform a write-mode control cycle.

data register to memory timing, serial input enabled



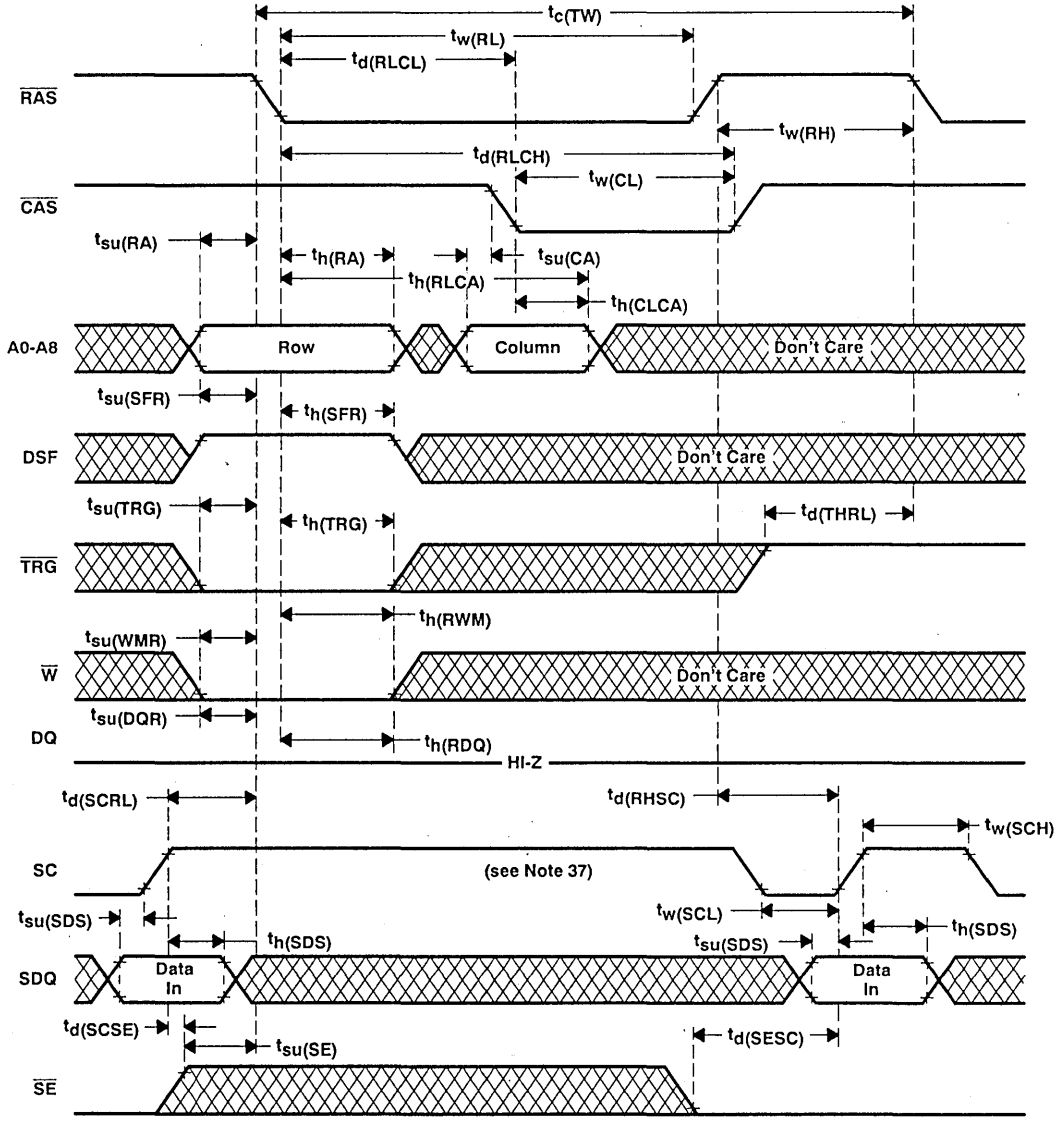
NOTES: 33. Random mode Q outputs remain in the high-impedance state for the entire data register to memory transfer cycle. This cycle is used to transfer data from the data register to the memory array. Every one of the 512 locations in each data register is written into the corresponding 512 columns of the selected row. Data in the data register may proceed from a serial shift-in or from a parallel load from one of the memory array rows. The above diagram assumes that the device is in the serial write mode (i.e., SD is enabled by a previous write mode control cycle, thus allowing data to be shifted-in).

34. See "Register Transfer Function Table" for logic state of "1" and "3".
35. Successive transfer writes can be performed without serial clocks for applications requiring fast memory array clears.
36. SC transitions are not allowed between $\overline{RAS}$ low and $\overline{TRG}$ high.
37. For a multiple transfer write operation; a transfer read cycle needs to be done from the same row after the first transfer write is carried out, then do multiple transfer write for subsequent rows. See parameters $t_{c(TW)M}$ (#18a) and $t_{w(RL)M}$ (#23a).

register transfer function table

FUNCTION	$\overline{RAS}$ FALL			
	$\overline{TRG}$	$\overline{W}$	DSF (1)	$\overline{SE}$ (3)
Register to memory transfer	L	L	X	L
Register to memory transfer, alternate transfer write	L	L	H	X
Pseudo-transfer SDQ control, serial input enabled	L	L	L	H
Memory to register transfer	L	H	L	X

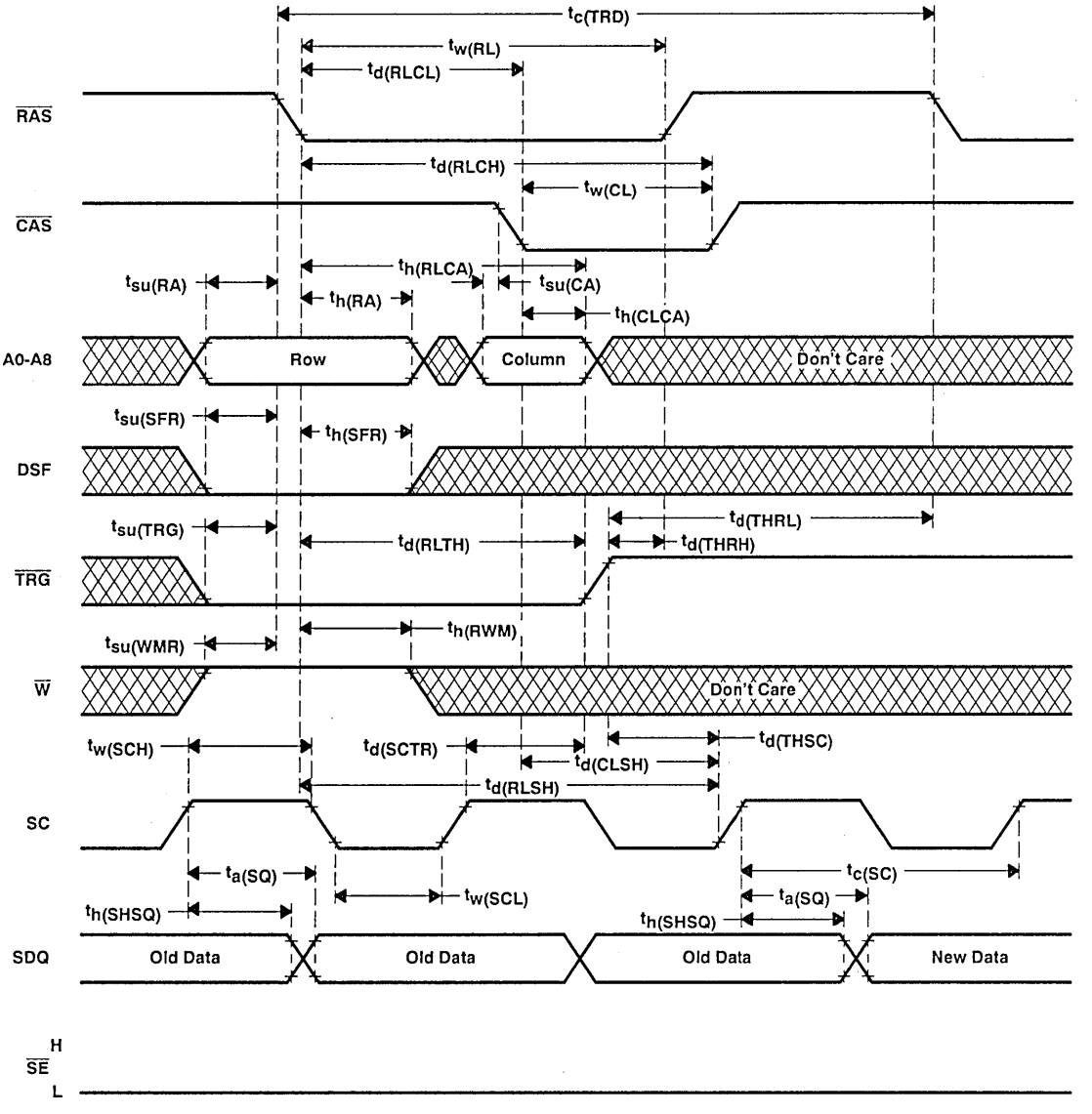
alternate data register to memory timing



NOTES: 36. SC transitions are not allowed between $\overline{RAS}$ low and $\overline{TRG}$ high.

37. For a multiple transfer write operation; a transfer read cycle needs to be done from the same row after the first transfer write is carried out, then do multiple transfer write for subsequent rows. See parameters $t_{c(TW)M}$ (#18a) and $t_{w(RL)M}$ (#23a).

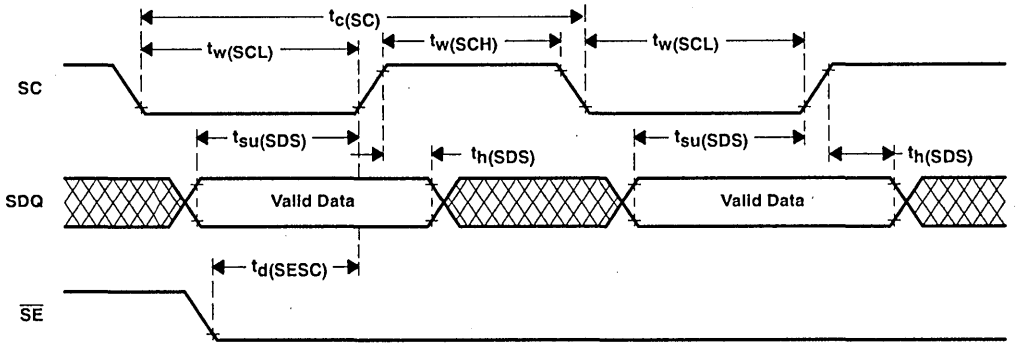
memory to data register transfer timing



NOTES: 38. Random mode (Q outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written into from the 512 corresponding columns of the selected row. The data that is transferred into the data registers may be either shifted out or transferred back into another row.

39. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

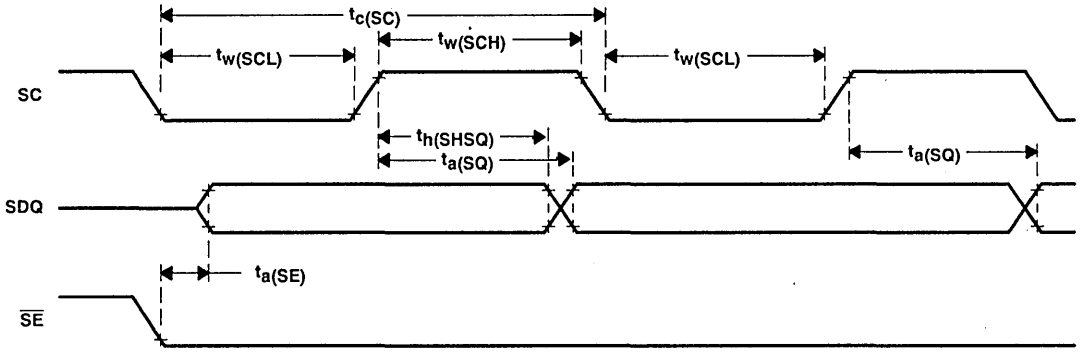
serial data-in timing



The serial data-in (SD) cycle is used to input serial data into the data registers. Before data can be written into the data registers via SD, the device must be put into the write mode by performing a write mode control, or pseudo-transfer cycle. Transfer write cycles occurring between the write mode control cycle and the subsequent writing of data will not take the device out of the write mode. However, a transfer read cycle during that time will take the device out of the write mode and put it into the read mode, thus disabling the input of data. Data will be written starting at the location specified by the input address loaded on the previous transfer cycle.

While accessing data in the serial data registers, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.

serial data-out timing



NOTE: 10. When the odd tap is used (tap addresses can be 0-511, and odd taps are 1,3,5 ... etc.), the cycle time for SC in the first serial data out cycle needs to be 40 ns minimum.

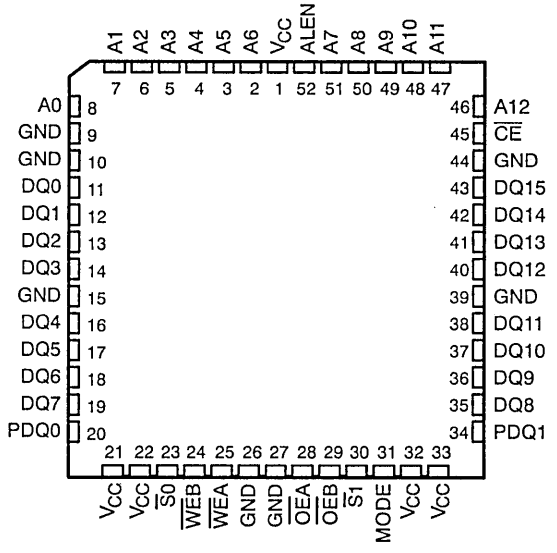
The serial data-out (SQ) cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle. Transfer write cycles occurring between the transfer read cycle and the subsequent shifting out of data will not take the device out of the read mode. But a write mode control cycle at that time will take the device out of the read mode and put it in the write mode, thus not allowing the reading of data.

While accessing data in the serial data registers, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.

D3291, NOVEMBER 1989–REVISED JUNE 1990

- **Interfaces Directly with the Intel 82385 Cache Controller**
- **Access Time . . . 25 ns Max**
- **Fast Access Time Supports 33-MHz Intel ESCA 80386 Operation**
- **Configurable for 2-Way or Direct Mapped Arrays**
- **Contains Address Latches and Byte Contol**
- **Cascadable for Larger Caches**
- **Byte Parity Storage Bits**
- **Fully TTL Compatible**

FN PACKAGE
(TOP VIEW)



description

The 'ACT2140A is a 147,456-bit static RAM with address latches and byte control that can be configured as 2-way 4K x 18 or direct mapped 8K x 18. The 'ACT2140A is fabricated using advanced silicon-gate CMOS technology for simple, high-speed interface with bipolar TTL circuits. The 'ACT2140A was designed so that it will interface directly with the Intel 82385 cache controller. Significant reductions in memory component count, board area, and power dissipation can be achieved by using this device. When using the 2-way mode, two 'ACT2140As replace 16 4K x 4 static RAMs, two latches, eight bidirectional transceivers, and one AND gate.

The MODE input of the 'ACT2140A allows the device to be used as either a 2-way set associative or direct mapped data RAM. When MODE is tied high, the 'ACT2140A is configured as two banks of 4K x 18 with common outputs as shown in logic diagram. When MODE is tied low, the 'ACT2140A is configured as one bank of 8K x 18 as shown in logic diagram.

The SN74ACT2140A is characterized for operation from 0°C to 70°C.

for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

ADVANCE INFORMATION

This device is covered by U.S. Patent 4,837,743.

ADVANCE INFORMATION

FUNCTION TABLES

TWO-WAY MODE (MODE = HIGH) 2 X 4K X 18 (see Note 1)

INPUTS							I/O		FUNCTION
$\overline{CE}$	$\overline{S0}$	$\overline{S1}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{WEA}$	$\overline{WEB}$	D0-D7, DP0	D8-D15, DP1	
X	H	H	X	X	X	X	HIGH-Z	HIGH-Z	DESELECT
X	X	X	H	H	X	X	HIGH-Z	HIGH-Z	DISABLED OUTPUTS
X	X	X	L	L	X	X	HIGH-Z	HIGH-Z	DISABLED OUTPUTS
L	L	H	L	H	H	H	OUTPUT	HIGH-Z	READ BANK A
L	L	H	H	L	H	H	OUTPUT	HIGH-Z	READ BANK B
L	H	L	L	H	H	H	HIGH-Z	OUTPUT	READ BANK A
L	H	L	H	L	H	H	HIGH-Z	OUTPUT	READ BANK B
L	L	L	L	H	H	H	OUTPUT	OUTPUT	READ BANK A
L	L	L	H	L	H	H	OUTPUT	OUTPUT	READ BANK B
L	L	H	X	X	L	H	INPUT	HIGH-Z	WRITE BANK A
L	L	H	X	X	H	L	INPUT	HIGH-Z	WRITE BANK B
L	H	L	X	X	L	H	HIGH-Z	INPUT	WRITE BANK A
L	H	L	X	X	H	L	HIGH-Z	INPUT	WRITE BANK B
L	L	L	X	X	L	H	INPUT	INPUT	WRITE BANK A
L	L	L	X	X	H	L	INPUT	INPUT	WRITE BANK B
L	L	L	X	X	L	L	HIGH-Z	HIGH-Z	INVALID WRITE
H	X	X	X	X	X	X	HIGH-Z	HIGH-Z	DESELECT

DIRECT MODE (MODE = LOW) 8K x 18 (see Note 1)

INPUTS							I/O		FUNCTION
$\overline{CE}$	$\overline{S0}$	$\overline{S1}$	$\overline{OEA}$†	$\overline{OEB}$†	$\overline{WEA}$†	$\overline{WEB}$†	D0-D7, DP0	D8-D15, DP1	
X	H	H	X	X	X	X	HIGH-Z	HIGH-Z	DESELECT
X	X	X	H	X	X	X	HIGH-Z	HIGH-Z	DISABLED OUTPUTS
X	X	X	X	H	X	X	HIGH-Z	HIGH-Z	DISABLED OUTPUTS
L	L	H	L	L	H	H	OUTPUT	HIGH-Z	READ
L	H	L	L	L	H	H	HIGH-Z	OUTPUT	READ
L	L	L	L	L	H	H	OUTPUT	OUTPUT	READ
L	L	L	L	H	H	H	OUTPUT	OUTPUT	INVALID READ
L	L	L	H	L	H	H	OUTPUT	OUTPUT	INVALID READ
L	L	H	X	X	L	X	INPUT	HIGH-Z	WRITE
L	H	L	X	X	L	X	HIGH-Z	INPUT	WRITE
L	L	L	X	X	L	X	INPUT	INPUT	WRITE
L	L	H	X	X	X	L	INPUT	HIGH-Z	WRITE
L	H	L	X	X	X	L	HIGH-Z	INPUT	WRITE
L	L	L	X	X	X	L	INPUT	INPUT	WRITE
H	X	X	X	X	X	X	HIGH-Z	HIGH-Z	DESELECT

† For compatibility with functionally equivalent devices, it may be necessary to wire $\overline{OEA}$ to $\overline{OEB}$ and $\overline{WEA}$ to $\overline{WEB}$ when MODE is tied low.

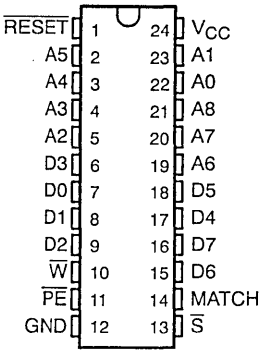
NOTE 1: Address latches for A0-A11 are latched when input signal ALEN is low and transparent when ALEN is high. A12 is functional only when MODE = low is always transparent. A12 should be grounded in the 2-way mode.

SN74ACT2150A
521 × 8 CACHE ADDRESS COMPARATOR

D3183, NOVEMBER 1988—REVISED MARCH 1990

- **Address to MATCH Valid Time**
  - **'ACT2150A 20 ns MAX**
  - **'ACT2150A 30 ns MAX**
- **300-Mil 24-Pin Ceramic Side-Brazed or Plastic Dual-In-Line or Small Outline Packages**
- **53 mA Typical Supply Current**
- **On-Chip Parity Generation and Checking**
- **Parity Error Output/Force Parity Error Input**
- **On-Chip Address/Data Comparator**
- **Asynchronous, Single-Cycle Reset**
- **Easily Expandable**
- **Fully Static**
- **Reliable Advanced CMOS Technology**
- **Fully TTL Compatible**

DW, JD, OR NT PACKAGE
(TOP VIEW)



description

This 8-bit-slice cache address comparator consists of a high-speed 512 × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. It is fabricated using N-channel silicon gate technology for high speed and simple interface with MOS and bipolar TTL circuits. The cache address comparator is easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device.

When $\overline{S}$ is low and $\overline{W}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A8 with the data on D0-D7 plus generated parity. An equality is indicated by the high level on the MATCH output. A low-level output from $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated even parity are written in the 9-bit memory location addressed by A0-A8. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

A $\overline{RESET}$ input is provided for initialization. When $\overline{RESET}$ goes low, all 512 × 9 RAM locations are cleared to zero (with valid parity) and the MATCH output is forced high. If an input word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high for every addressed memory location after reset indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless sata has been written into the addressed memeory location. When cascading in the width direction, only one bit needs to be tied high regardless of the address width.

The SN74ACT2150A operates from a single 5-V supply and is offered in a 24-pin 300-mil ceramic side-brazed or plastic dual-in-line packages and plastic "Small Outline" packages. The device is fully TTL compatible and is characterized for operation from 0°C to 70°C.

D3183, NOVEMBER 1988—REVISED MARCH 1990

MATCH OUTPUT DESCRIPTION

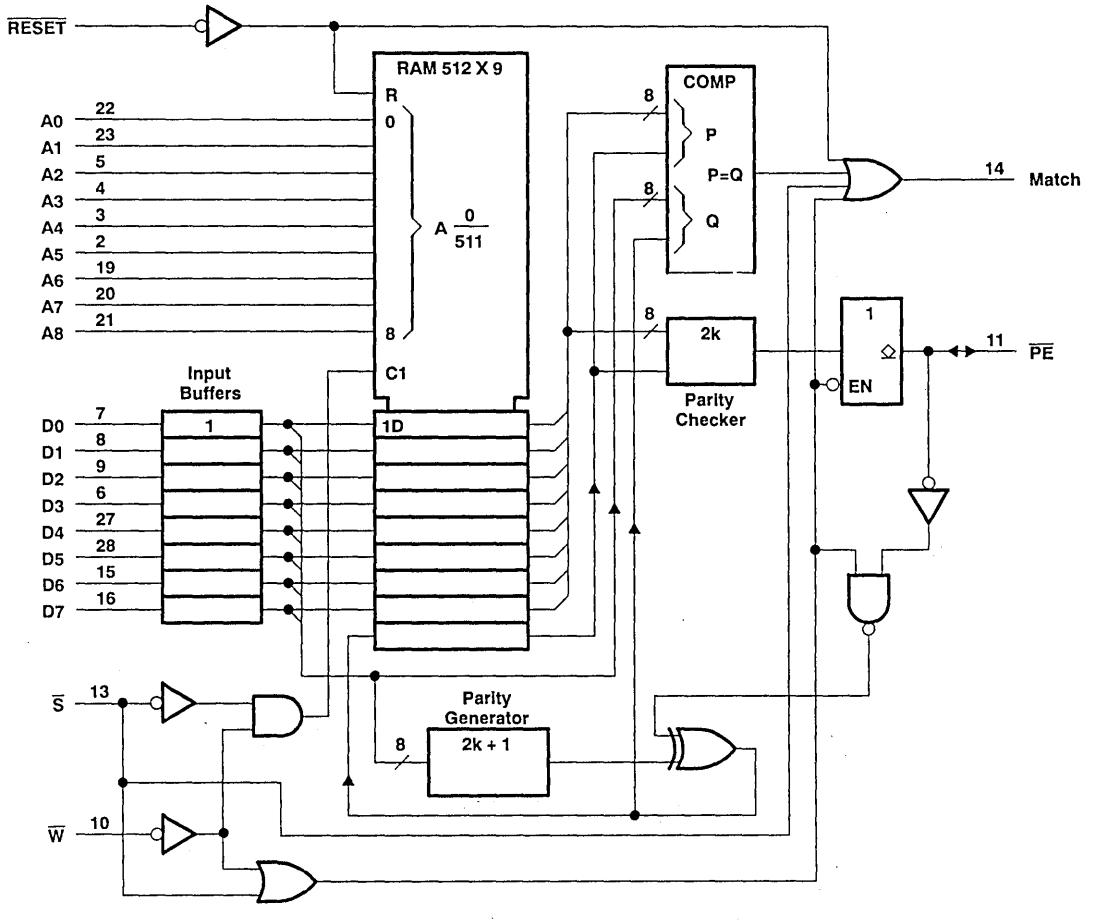
MATCH = V_{OH} if: [A0-A8] = D0-D7 + parity,
or: $\overline{RESET} = V_{IL}$,
or: $\overline{S} = V_{IH}$,
or: $\overline{W} = V_{IL}$

MATCH = V_{OL} if: [A0-A8] ≠ D0-D7 + parity,
with $\overline{RESET} = V_{IH}$,
$\overline{S} = V_{IL}$, and $\overline{W} = V_{IH}$

FUNCTION TABLE

OUTPUTS		FUNCTION DESCRIPTION
MATCH	$\overline{PE}$	
L	L	Parity Error
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

logic diagram (positive logic)



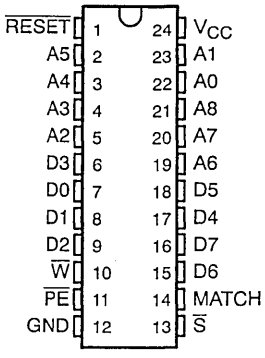
for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

D2911, MARCH 1982–REVISED SEPTEMBER 1990

- 'ACT2150A is Recommended for New Designs
- Fast Address to Match Valid Delay – Two Speed Ranges: 35 ns and 45 ns
- 512 × 9 Internal RAM
- 300-Mil 24-Pin Ceramic Side-Brazed or Plastic Dual-In-Line or Small Outline Packages
- Max Power Dissipation: 660 mW
- On-Chip Parity Generation and Checking
- Parity Error Output/Force Parity Error Input
- On-Chip Address/Data Comparator
- Asynchronous, Single-Cycle Reset
- Easily Expandable
- Fully Static
- Reliable SMOS (Scaled NMOS) Technology
- TTL- and CMOS Compatible Inputs and Outputs

DW, JD, OR NT PACKAGE
(TOP VIEW)



description

This 8-bit-slice cache address comparator consists of a high-speed 512 × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. It is fabricated using N-channel silicon gate technology for high speed and simple interface with MOS and bipolar TTL circuits. The cache address comparator is easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device.

When $\overline{S}$ is low and $\overline{W}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A8 with the data on D0-D7 plus generated parity. An equality is indicated by the high level on the MATCH output. A low-level output from $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated even parity are written in the 9-bit memory location addressed by A0-A8. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

A $\overline{RESET}$ input is provided for initialization. When $\overline{RESET}$ goes low, all 512 × 9 RAM locations are cleared and the MATCH output is forced high.

The cache address comparator operates from a single 5-V supply and is offered in a 24-pin 300-mil ceramic side-brazed or plastic dual-in-line packages and plastic "Small Outline" packages. The device is fully TTL compatible and is characterized for operation from 0°C to 70°C.

for complete data sheet

The complete version of this data sheet and application information can be obtained by calling the DVP Applications Group at 214-997-5762.

MATCH OUTPUT DESCRIPTION

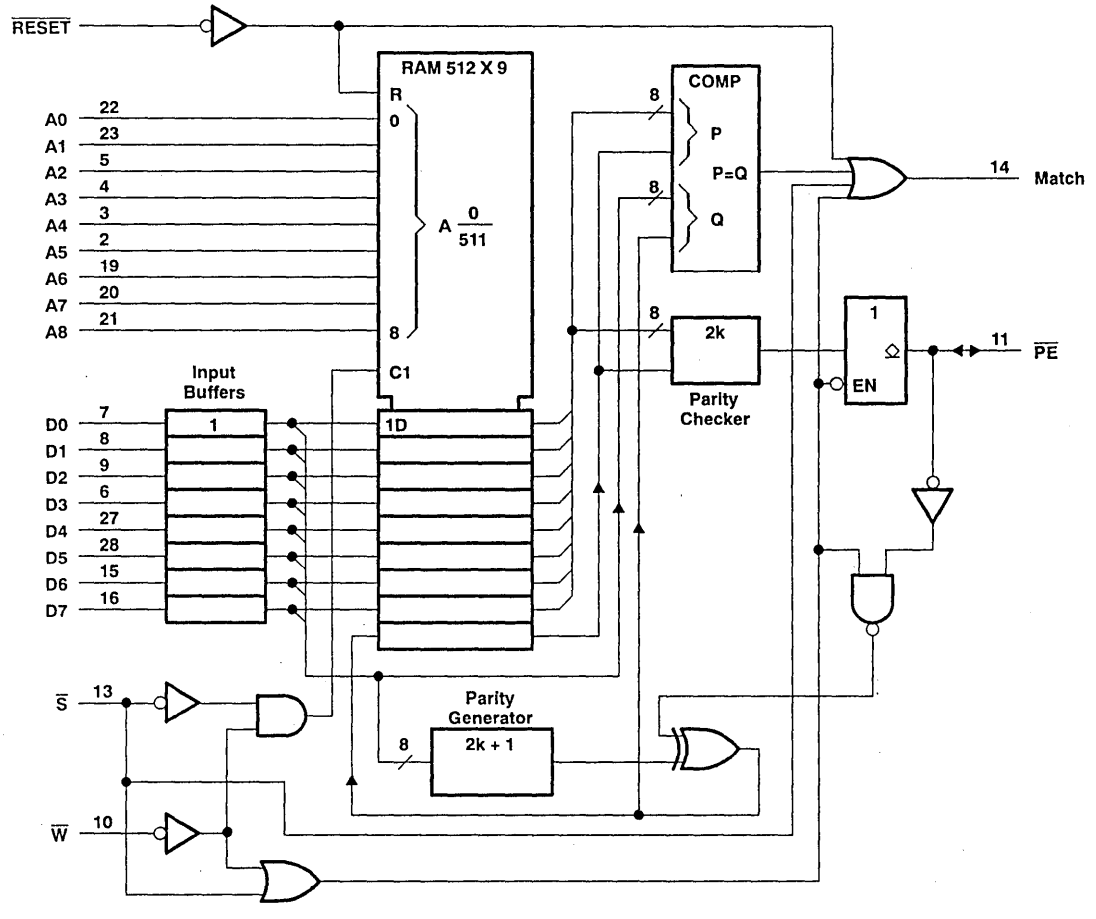
MATCH = V_{OH} if: [A0-A8] = D0-D7 + parity,
or: $\overline{RESET} = V_{IL}$,
or: $\overline{S} = V_{IH}$,
or: $\overline{W} = V_{IL}$

MATCH = V_{OL} if: [A0-A8] ≠ D0-D7 + parity,
with $\overline{RESET} = V_{IH}$,
$\overline{S} = V_{IL}$, and $\overline{W} = V_{IH}$

FUNCTION TABLE

OUTPUTS		FUNCTION DESCRIPTION
MATCH	$\overline{PE}$	
L	L	Parity Error
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

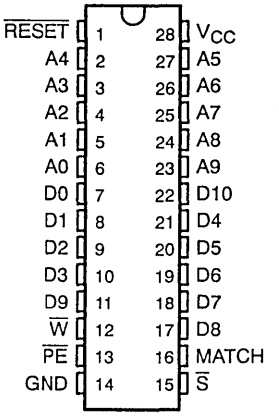
logic diagram (positive logic)



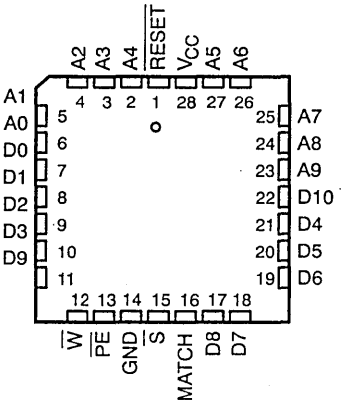
D3105, SEPTEMBER 1987–REVISED MARCH 1990

- **Fast Address to Match Delay . . . 22 ns Max**
- **On-Chip Address/Data Comparator**
- **On-Chip Parity Generator and Checking**
- **Parity Error Output, Force Parity Error Input**
- **Easily Expandable**
- **Choice of Totem-Pole ('ACT2151) or Open-Drain ('ACT2153) MATCH Output**
- **EPIC™ (Enhanced Performance Implanted CMOS) 1 μm Process**
- **Fully TTL-Compatible**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The 'ACT2151 and 'ACT2153 cache address comparators consist of a high-speed 1K × 11 static RAM array, parity generator, parity checker, and 12-bit high-speed comparator. They are fabricated using advanced silicon-gate CMOS technology for high speed and simple interface with bipolar TTL circuits. These cache address comparators are easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with these devices. The 'ACT2151 has a totem-pole match output while the 'ACT2153 has an open-drain MATCH output for easy AND-tying.

If $\overline{S}$ is low and $\overline{W}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A9 with the data D0-D10 plus generated parity. An equality is indicated by a high level on the MATCH output. A low-level output on $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D10 plus generated odd parity are written in the 12-bit memory location addressed by A0-A10. ALso during write, a parity error may be forced by holding $\overline{PE}$ low.

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 1K × 11 RAM locations are cleared to zero (with valid parity) and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high after reset for every addressed memory location, indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit must be tied high regardless of the address width.

EPIC is a trademark of Texas Instruments Incorporated.
These devices are covered by U.S. Patents 4,831,625 and 4,884,270.

These cache address comparators operate from a single 5-V supply and are offered in 28-pin 600-mil plastic dual-in-line or PLCC packages.

The SN74ACT2151 and SN74ACT2153 are characterized for operation from 0°C to 70°C.

MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: (A0-A9) = D0-D10 + parity,
or: $\overline{RESET} = V_{IL}$,
or: $\overline{S} = V_{IH}$,
or: $\overline{W} = V_{IL}$
MATCH = V_{OL} if: (A0-A9) ≠ D0-D10 + parity,
with $\overline{RESET} = V_{IH}$,
$\overline{S} = V_{IL}$, and $\overline{W} = V_{IH}$

FUNCTION TABLE

INPUTS			OUTPUTS		FUNCTION
$\overline{W}$	$\overline{S}$	$\overline{RESET}$	MATCH	$\overline{PE}$	
H	L	H	L	L	Parity error
			L	H	Not equal
			H	L	Undefined error
			H	H	Equal
L	L	H	H	IN	Write
X	H	H	H	H	Device disabled
X	X	L	H	†	Memory reset

† The state of $\overline{PE}$ is dependent on inputs $\overline{W}$ and $\overline{S}$.

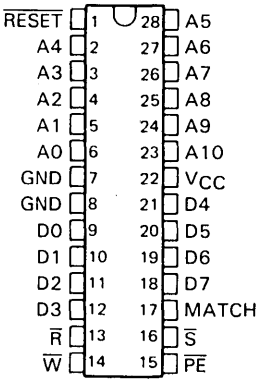
for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

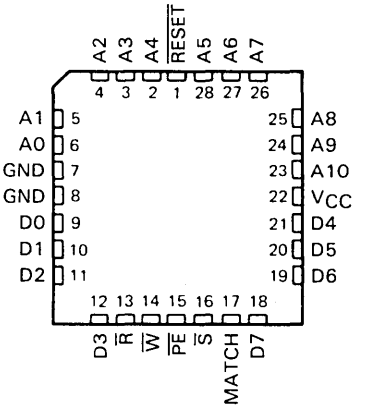
D3156, DECEMBER 1988—REVISED MARCH 1990

- Fast Address to Match Delay 25 or 25 ns Max
- Common I/O with Read Feature
- On-Chip Address/Data Comparator
- On-Chip Parity Generator and Checking
- Parity Error Output, Force Parity Error Input
- Easily Expandable
- Choice of Open-Drain or Totem-Pole MATCH Output
- EPIC™ (Enhanced Performance Implanted CMOS) 1-μm Process
- Fully TTL-Compatible

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The 'ACT2152A and 'ACT2154A cache address comparators consist of a high-speed 2K × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. They are fabricated using advanced silicon-gate CMOS technology for high speed and simple interface with bipolar TTL circuits. These cache address comparators are easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with these devices. The 'ACT2152A has a totem-pole MATCH output while the 'ACT2154A has an open-drain MATCH output for easy AND-tying.

If $\overline{S}$ is low and $\overline{W}$ and $\overline{R}$ are high, the cache address comparator compares the contents of the memory location addressed by A0-A10 with the data D0-D7 plus generated parity. An equality is indicated by a high level on the MATCH output. A low-level output on $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated odd parity are written in the 9-bit memory location addressed by A0-A10. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

EPIC is a trademark of Texas Instruments Incorporated.

A read mode is provided with the 'ACT2152 and 'ACT2154, which allows the contents of RAM to be read at the D0-D7 pins. The read mode is selected when $\overline{R}$ and $\overline{S}$ are low, and $\overline{W}$ is high.

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 2K × 9 RAM locations are cleared to zero (with valid parity) and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high after reset for every addressed memory location, indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit must be tied high regardless of the address width.

These cache address comparators operate from a single +5-V supply and are offered in 28-pin 600-mil ceramic side-brazed, plastic dual-in-line, or PLCC packages.

The 'ACT2152 and 'ACT2154 are characterized for operation from 0°C to 70°C.

MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: [A0-A10] = D0-D7 + parity,
or: $\overline{RESET}$ = V_{IL},
or: $\overline{S}$ = V_{IH},
or: $\overline{W}$ = V_{IL}

MATCH = V_{OL} if: [A0-A10] ≠ D0-D7 + parity,
with $\overline{RESET}$ = V_{IH},
$\overline{S}$ = V_{IL}, and $\overline{W}$ = V_{IH}

FUNCTION TABLE

INPUTS				OUTPUTS		I/O	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{RESET}$	MATCH	$\overline{PE}$	D0-D7	
H	L	L	H	L	H	Output	Read
H	H	L	H	L	L	Input	Parity error
				L	H		Not equal
				H	L		Undefined error
				H	H		Equal
L	X	L	H	H	IN	Input	Write
X	X	H	H	H	H	Hi-Z	Device disabled
X	X	X	L	H	†	†	Memory reset

†The state of these pins is dependent on inputs $\overline{W}$, $\overline{R}$, and $\overline{S}$.

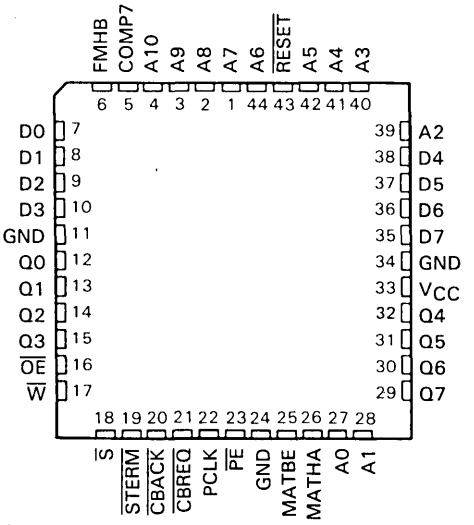
for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

D3076, NOVEMBER 1988—REVISED JUNE 1990

- Address to MATCH Time . . . 22 ns Max
- Supports Motorola MC68030 Cache Burst Fill with No Added Wait States
- Upward Compatibility for Motorola MC68030 Speed Upgrades
- Cache Data RAM with Parity and Internal Burst Counter
- Dirty Bit Storage Capability for Use in Copy-Back Caches
- Separate I/O Supports Copy-Back
- Easily Expandable in Depth and Width
- Reliable Advanced CMOS Technology
- Fully TTL Compatible

FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The 'ACT2155 burst cache address comparator/data RAM consists of a high-speed 2K × 9 static RAM array, 2-bit burst counter and control circuitry, parity generator, parity checker, and 8-bit high-speed comparator. The 'ACT2155 is fabricated using advanced silicon-gate CMOS technology for high speed and simple interface with bipolar TTL circuits. The 'ACT2155 provides a valuable building block for building fast, efficient caches. By combining this device with programmable logic, a cache can be constructed that specifically addresses the individual system requirements. Significant reductions in cache memory component count, board area, and power dissipation can be achieved by using this device.

The 'ACT2155 was designed to be used as the tag comparator and data RAM necessary to provide a cache that supports the burst-fill requirement of the Motorola MC68030 microprocessor. The 'ACT2155 directly interfaces with the Motorola MC68030 providing four long words to the processor in four clock cycles. By interfacing directly with the processor, at least 10 ns in delay time is saved when comparing this solution with discrete designs. Even though the 'ACT2155 is designed for use with the Motorola MC68030 processor, it can be used with other processors to implement write-through or copy-back class caches.

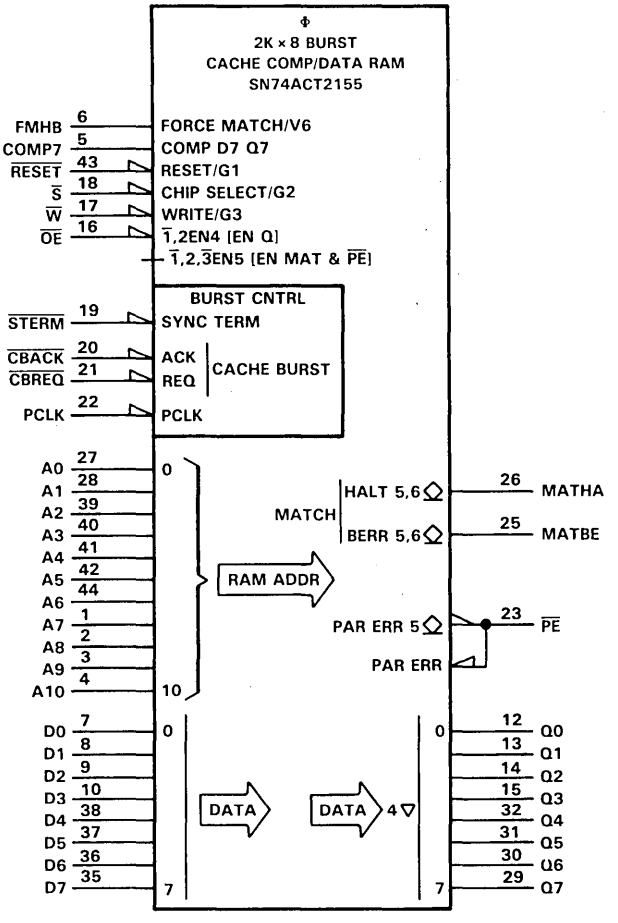
PARTIAL FUNCTION TABLE

INPUTS					OUTPUTS				FUNCTION
$\overline{S}$	$\overline{W}$	$\overline{RESET}$	$\overline{OE}$	FMHB	MATHA†	MATBE	$\overline{PE}$/(I/O)	Q0-Q7	
X	X	X	X	H	H	H	‡	‡	Force MATHA and MATBE unconditionally high
H	X	X	X	X	H	H	Disabled	Hi-Z	Deselect. Inhibits write, read, and compare.
L	H	H	X	L	H or L	H or L	L	‡	Parity error
					L	L	H		Not equal
					H	H	H		Equal
X	H	L	X	X	H	H	Disabled	Hi-Z	Memory reset unconditionally
L	L	H	H	X	H	H	Input	Hi-Z	Write, Low on $\overline{PE}$ forces parity error.
L	L	H	L	X	H	H	Input	Low	Write. Low on $\overline{PE}$ forces parity error.
L	H	H	L	X	‡	‡	Enabled	Enabled	Read

†During the burst mode, MATHA is forced high.
‡The state of these pins is dependent on inputs shown as irrelevant (X).

These devices are covered by U.S. Patents 4,831,625; 4,858,182; 4,884,270; and additional patents pending.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

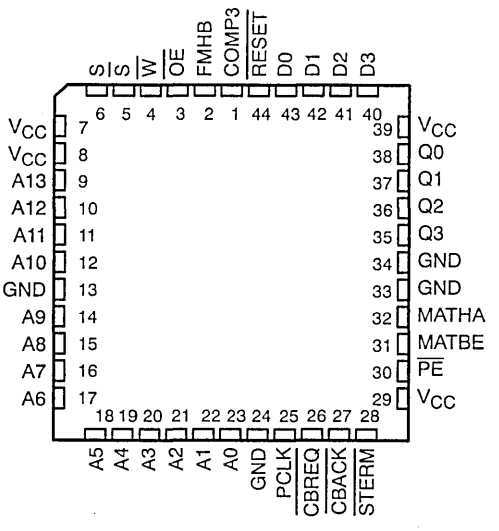
for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

D3412, APRIL 1990–REVISED JUNE 1990

- **Address to MATCH Time . . . 20 ns Max**
- **Supports Motorola MC68030 Cache Burst Fill with Direct Interface**
- **Cache Data RAM with Parity and Internal Burst Counter**
- **Dirty Bit Storage Capability for Use in Copy-Back Caches**
- **Separate I/O Supports Copy-Back**
- **Easily Expandable in Depth and Width**
- **Reliable Advanced CMOS Technology**
- **Fully TTL Compatible**

FN PACKAGE
(TOP VIEW)



description

The 'ACT2156 burst cache address comparator/ data RAM consists of a high-speed 16K x 5 static RAM array, 2-bit burst counter and control circuitry, parity generator, parity checker, and 4-bit high-speed comparator. The 'ACT2156 is fabricated using advanced silicon gate CMOS technology for high speed and simple interface with bipolar TTL circuits. The 'ACT2156 provides a valuable building block for building fast efficient caches. By combining this device with programmable logic, a cache can be constructed that specifically addresses the individual system requirements. Significant reductions in cache memory component count, board area, and power dissipation can be achieved by using this device.

The 'ACT2156 was designed to be used as the tag comparator and data RAM necessary to provide a cache that supports the burst fill requirement of the Motorola MC68030 microprocessor. The 'ACT2156 directly interfaces with the MC68030 providing four long words to the processor in four clock cycles. By interfacing directly with the processor, about 10 ns in delay time is saved when comparing this solution with discrete designs. Even though the 'ACT2156 is designed for use with the MC68030 processor, it can also be used with other processors to implement write-through or copy-back class caches.

The SN74ACT2156 is characterized for operation from 0°C to 70°C.

operation as an address comparator

The 'ACT2156 compares the contents of the memory location addressed by A0-A13 with the address bits applied at D0-D3. An equality is indicated by a high level on the MATBE and MATHA outputs. A low-level output on $\overline{PE}$ signifies a parity error in the addressed internal RAM data. During a write cycle, address bits on D0-D3 plus generated odd parity are written in the 5-bit memory location addressed by A0-A13. Also during write, a parity error may be forced for diagnostic purposes by holding $\overline{PE}$ low.

operation in the burst mode

The 'ACT2156 contains burst control circuitry consisting of a 2-bit wrap-around counter, a mux, and a Burst Control Register (BCR). The BCR controls a mux which selects A0 and A1 from either the input terminals or the 2-bit counter. When $\overline{CBREQ}$ or $\overline{CBACK}$ is high, the BCR is asynchronously reset and inputs A0 and A1 drive the RAM. On the next falling edge of PCLK after $\overline{STERM}$ is taken low, the BCR is set and the counter bits (CA0

and CA1) drive the RAM. At the same time that the BCR is set ($\overline{\text{STERM}}$ low and a PCLK falling edge), the binary value of A0 and A1 in the counter is incremented. The counter can be held at any count by taking $\overline{\text{STERM}}$ high as long as BCR remains set. When the BCR is set, MATHA is forced high.

operation as a data RAM

The 'ACT2156 can be used as a 16K x 4 data RAM with separate I/O, a four-word burst mode and parity generation and checking. When using this device as a data RAM, the FMHB input should be tied high to prevent MATHA and MATBE from switching.

using the 'ACT2156 with the MC68030

The 'ACT2156 interfaces with the Motorola MC68030 through use of 'ACT2156 input signals, $\overline{\text{STERM}}$, $\overline{\text{CBREQ}}$, PCLK, and $\overline{\text{CBACK}}$, and output signals MATBE and MATHA. Match outputs MATBE and MATHA can be tied directly to processor inputs $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$, respectively. As long as the requested information is in cache, the $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ signals remain high. When a miss occurs (MATBE and MATHA low), $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ are driven low simultaneously causing the bus cycle to be retried (rerun). A high level applied at the FMHB input forces MATBE and MATHA high to prevent continuous rerun.

The 'ACT2156 was designed to be used as the tag comparator and data RAM necessary to provide a cache that meets the Motorola MC68030 internal cache burst fill requirement by supplying four long words to the processor in four clock cycles. When the MC68030 requests a burst fill, a single address is supplied. If the requested information is in the external cache, the 'ACT2156 will indicate a hit. If $\overline{\text{STERM}}$ is low, address bits A1-A0 (A3-A2 from the processor) will be incremented on each PCLK falling edge and the MATBE output will indicate a hit or a miss. If a miss occurs, MATBE will drive $\overline{\text{BERR}}$ low causing the MC68030 to abort the burst cycle and to run with the data it received. MATHA is held high during a burst by the BCR. The timing diagram in Figure 9 shows burst mode operation.

The 'ACT2156 internal counter can also be used when writing tag and data into the cache, when the burst fill is done from main memory. When $\overline{\text{STERM}}$ is taken high (inserting processor wait states), the 2-bit counter is held at the present count. The counter will continue to increment on the first PCLK falling edge after $\overline{\text{STERM}}$ returns low. When $\overline{\text{CBACK}}$ or $\overline{\text{CBREQ}}$ returns high, the mux will select input pins A0 and A1 to drive the RAM. Figure 10 shows a MC68030 burst request with data in main memory. For more information on using the 'ACT2156 with the MC68030, see the *"SN74ACT2155/56 Cache Enhances MC68030 Processor Performance"* applications note.

cascading the 'ACT2156

The 'ACT2156 is easily cascaded in width and depth. Wider addresses can be compared by driving the A0-A13 inputs of each device with the same index and applying the additional address bits to the D0-D3 inputs. The chip select inputs allow the 'ACT2156 to be cascaded in depth. When a device is deselected, the MATHA and MATBE outputs are driven high. It should be noted that a decoder can be used to drive the select inputs, since the propagation delay from select to match is much faster than from address to match. MATHA and MATBE are open-drain outputs for easy wired logic. Through the use of the chip select inputs, the 'ACT2156 can also be cascaded for a deeper cache data buffer. Figure 12 shows the 'ACT2156 cascaded.

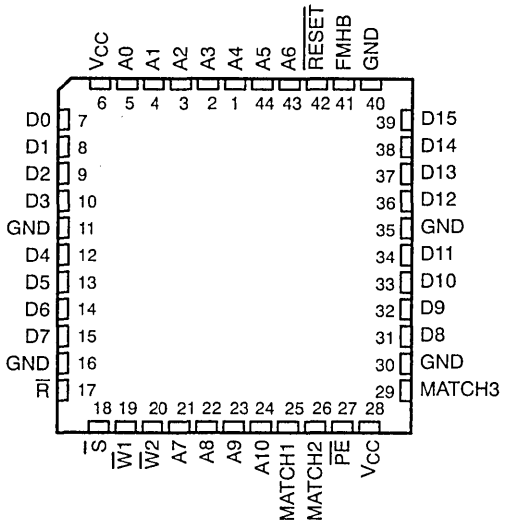
for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

D3326, JANUARY 1990–REVISED JUNE 1990

- **Fast Address to Match Delay . . . 20 ns Max**
- **Totem-Pole and Open-Drain Match Outputs**
- **On-Chip Address/Data Comparator**
- **On-Chip Parity Generation and Checking**
- **Direct 68030 Interface**
- **Reliable Advanced CMOS Technology**
- **Fully TTL Compatible**

FN PACKAGE
(TOP VIEW)



description

The 'ACT2157 cache address comparator consists of a high-speed 2K x 18 static RAM array, parity generators, parity checkers, and 18-bit high-speed comparator. It is fabricated using advanced silicon-gate CMOS technology for high-speed and simple interface with bipolar TTL circuits. This cache address comparator is easily cascaded for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device.

When $\overline{S}$ is low and $\overline{W}1$, $\overline{W}2$, and $\overline{R}$ are high, the cache address comparator compares the contents of the memory location addressed by A0-A10 with the applied D0-D15 plus generated byte parity. An equality is indicated by a high level on the MATCH1, MATCH2, and MATCH3 outputs.

The 'ACT2157 is provided with two write inputs, $\overline{W}1$ and $\overline{W}2$. When $\overline{S}$ is low, bytes D0-D7 are written into the addressed location by asserting $\overline{W}1$ (low) and bytes D8-D15 are written by asserting $\overline{W}2$ (low). By asserting both $\overline{W}1$ and $\overline{W}2$ at the same time, D0-D15 is written into the addressed memory location. During a write cycle, parity is generated and stored for each byte written.

'ACT2157 parity protection

Byte parity protection is included in the 'ACT2157 to provide a highly reliable cache directory. For any memory location addressed by A0-A10, $\overline{PE}$ will be low if a parity error occurs in either D0-D7 or D8-D15. $\overline{PE}$ is an open-drain output for easy OR-tying. For test purposes, a parity error can be forced in byte D0-D7 or D8-D15 by forcing $\overline{PE}$ low when $\overline{W}1$ or $\overline{W}2$ are low, respectively. A parity error is forced in both bytes by forcing $\overline{PE}$ low when both $\overline{W}1$ and $\overline{W}2$ are asserted.

reading the data RAM

A read mode is provided with the 'ACT2157 and allows the contents of RAM to be read at the D0-D15 pins. The read mode is selected when $\overline{R}$ and $\overline{S}$ are low and $\overline{W}1$ and $\overline{W}2$ are high. When using the 'ACT2157 as a data RAM, the FMHB input should be tied high to provide better noise immunity.

initialization

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 2K x 18 RAM locations are cleared to zero (with valid parity) and the match outputs are forced high. If an input at D0-D15 of zero is compared to any memory location that has not been written into since reset, MATCH1, MATCH2, and MATCH3 will be high

indicating that D0-D15 plus generated parity is equal to the reset memory location. $\overline{PE}$ will be high for every addressed memory location after reset indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction only, one bit needs to be tied high regardless of the address width.

cascading the 'ACT2157

The 'ACT2157 is easily cascaded in width and depth. Wider addresses can be compared by driving the A0-A10 inputs of each device with the same index and applying the additional address bits to the D0-D15 inputs. The select ($\overline{S}$) input allows these devices to be cascaded in depth. When a device is deselected, the match outputs are driven high. It should be noted that a fast decoder can be used to drive the select inputs since the propagation delay from select to match is much faster than from address to match. MATCH1 and MATCH2 are open-drain outputs for easy wire tying. Figure 11 shows the 'ACT2157 cascaded.

cache coherency through bus watching

When implementing cache designs, the problem of cache coherency is usually a concern. One solution to this problem is to implement bus watching using the 'ACT2157. By storing the same tags in the bus watcher RAM as is stored in the cache tag RAM, the bus watcher will indicate a hit every time a cached address passes down the main address bus. If cached data is being modified in main memory, the index can be passed to the cache tag and bus watcher RAM for invalidation. Figure 12 shows a typical bus watcher implementation.

using the 'ACT2157 with the MC68030

The 'ACT2157 has two open-drain match outputs for direct interface with the Motorola MC68030. By tying the outputs MATCH1 and MATCH2 directly to MC68030 inputs BERR and HALT, a two-cycle synchronous read may be easily achieved. A two-cycle access can be accomplished by using control logic that assumes a cache hit will occur every time an access is started for cacheable data. This is accomplished by asserting the MC68030 input signal STERM at the beginning of the access cycle. As long as the requested information is in cache, the BERR and HALT signals remain high. When a miss occurs (MATCH1 and MATCH2 low), BERR and HALT are driven low simultaneously causing the bus cycle to be retried (rerun). The FMHB input of the 'ACT2157 is provided so that MATCH1 and MATCH2 can be forced high. This function is used to prevent continuous rerun when the processor retries an access. FMHB could also be used during noncacheable accesses (see Figure 13).

copy-back caches

The 'ACT2157 can be used in write-through cache designs where writes to cache are immediately sent to main memory, or in copy-back cache designs where a cache write initially only modifies the cache and can later be copied back to main memory. Copy-back caches have an advantage in that the number of writes to main memory are reduced, thereby reducing bus traffic. To implement a copy-back cache, a dirty bit is needed that indicates whether or not the data is modified from that in main memory. The dirty bit is set to 1 when the cache data is modified. Data is only copied back if the dirty bit is set, otherwise it is simply overwritten. The read feature of the 'ACT2157 allows it to be used in copy-back cache designs. It should be noted, however, that the dirty bit must be stored in an external RAM. Figure 14 shows the 'ACT2157 in a copy-back application.

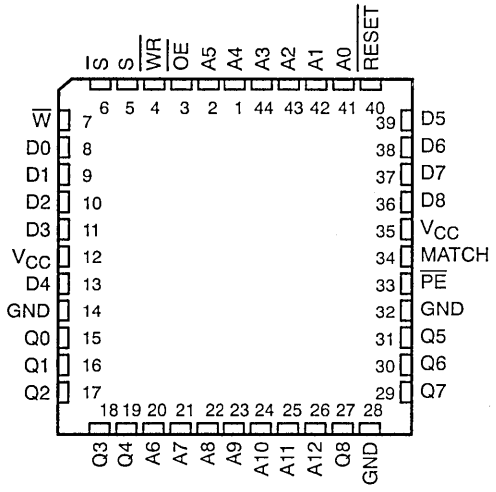
for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

D3281, MAY 1990–REVISED JUNE 1990

- Fast Address to MATCH Delay 22 ns Max
- 8K × 10 Internal Static RAM
- On-Chip Address/Data Comparator
- Read Feature with Separate I/O
- Word Reset Function for Single Entry Invalidation
- On-Chip Parity Generator and Checking
- Easily Expandable in Width and Depth
- Choice of Open-Drain ('ACT2159) or Totem-Pole ('ACT2158) MATCH Output
- Fully TTL Compatible

FN PACKAGE
(TOP VIEW)



description

The 'ACT2158 and 'ACT2159 cache address comparators consist of a high-speed 8K x 10 static RAM array, parity generator, parity checker, and 10-bit high-speed comparator. They are fabricated using advanced silicon gate CMOS technology for high speed and simple interface with bipolar TTL circuits. A single 'ACT2158 or 'ACT2159 can provide comparison for 8192 addresses of 22 bits each. In addition, these devices are easily cascaded for greater address width and/or depth.

Significant reductions in cache memory component count, board area, and power dissipation can be achieved with these devices. The 'ACT2158 has a totem-pole MATCH output while the 'ACT2159 has an open-drain MATCH output for wire AND-tying. These devices operate from a single 5-V power supply.

The SN74ACT2158 and SN74ACT2159 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

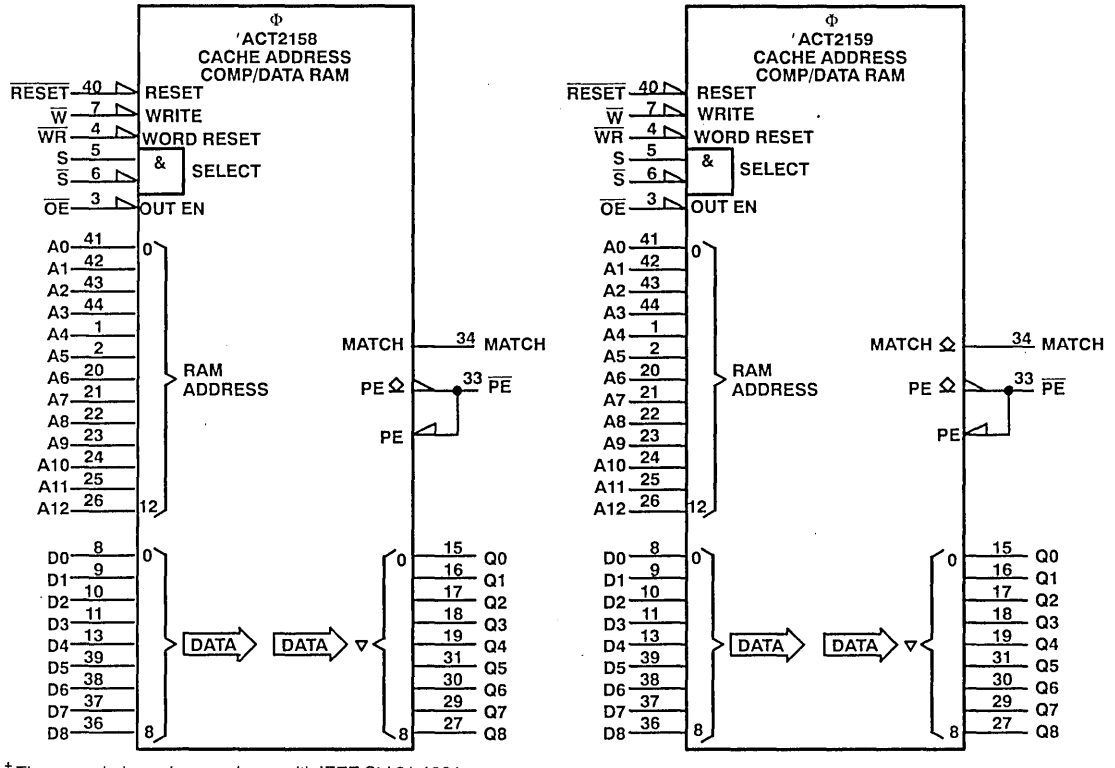
INPUTS						OUTPUTS			FUNCTION
$\overline{W}$	$\overline{OE}$	S	$\overline{S}$	$\overline{RESET}$	$\overline{WR}$	MATCH	$\overline{PE}$	Q0–Q8	
L	X	H	L	H	H	L	IN	HI-Z	Write
H	L	H	L	H	H	Active	H†	Output	Read
H	X	H	L	H	H	L	L	Hi-Z or Active	Parity Error
						L	H		Not Equal
						H	L		Undefined Error
						H	H		Equal
H	X	H	L	L	X	L	H	‡	Memory Reset (Selected)
H	X	L	X	L	X	H	H	HI-Z	Memory Reset (Deselected)
H	X	X	H	L	X	H	H	HI-Z	Memory Reset (Deselected)
H	X	H	L	H	L	L	IN	‡	Word Reset
X	X	L	X	H	X	H	H	HI-Z	Device Disabled
X	X	X	H	H	X	H	H	HI-Z	Device Disabled

† If a parity error exists in the addressed data, $\overline{PE}$ will be low.
‡ The state of these pins is dependent on input $\overline{OE}$.

These devices are covered by U.S. Patents 4,831,625; 4,858,182; 4,860,262; 4,884,270; and additional patents pending.

ADVANCE INFORMATION

logic symbols†



† These symbols are in accordance with IEEE Std 91-1984.

for complete data sheet

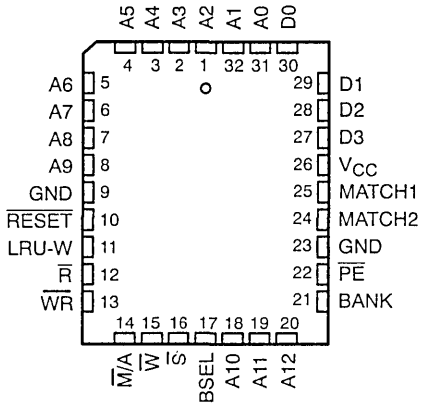
The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

ADVANCE INFORMATION

D3365, JANUARY 1990–REVISED JUNE 1990

- Address to Match Time . . . 17 ns Max
- 2-Way Architecture Significantly Improves Hit Rate
- Implements LRU Replacement Allgorithm
- Useful for Bus Watching
- On-Chip Parity Generator and Checker
- Easily Expandable in Depth and Width
- Reliable Advanced CMOS Technology
- Fully TTL Compatible

FM PACKAGE
(TOP VIEW)



description

The SN74ACT2160 is a valuable building block for implementing fast two-way set associative caches. This device consists of two separate 8K x 5 RAMs for tag and parity storage, an 8K x 1 LRU RAM, two high-speed comparators, and the control circuitry necessary to give the designer the freedom to determine how this device will be used. The SN74ACT2160 also includes single-entry invalidation circuitry and parity generation and checking for ease of design and high system reliability.

The SN74ACT2160 is fabricated using advanced silicon-gate CMOS technology for high speed and simple interface with bipolar TTL circuits. By combining the SN74ACT2160 with programmable logic, a cache can be constructed that specifically addresses the individual system requirements. Significant reductions in cache memory component count, board area, and power dissipation can be achieved by using this device.

direct-mapped versus two-way set associative caches

A cache memory is a small high-speed memory that is used to store a portion of the data found in the larger main memory to achieve optimum processor performance and to reduce main memory bus traffic. Since the cache memory is smaller than the main memory, only part of the address, the least significant bits referred to as the index, is used to address the cache memory. The most significant address bits, called the tag, are stored along with the cache data and are used to identify what data is stored in an indexed location. When the processor requests data, the index portion of the processor address points to a word of data in the cache-data RAM and to a tag in the cache tag RAM. If the upper portion of the processor address is equal to the stored tag, a cache hit is said to occur and the cached data can be immediately sent to the processor.

In a direct-mapped or one-way set associative cache, only one data word and tag exist in cache for each index. This means that when the processor requests data, only one cache memory location can contain the requested data. Also, if the requested data is not in the cache and the cache is updated, the data in the indexed cache memory location will be written over regardless of how recently it has been used.

In a two-way set associative cache, two data words and tags exist for each index. This means that the requested data can reside in one of two cache locations. When a miss occurs and the cache is updated, the least recently used data can be written over. As would be expected, studies have shown that the hit rate improves significantly when using a two-way cache design over a one-way or direct-mapped cache design. Through use of the 'ACT2160, the logic complexity and parts count usually associated with a two-way cache are greatly reduced.

ADVANCE INFORMATION

address comparison

The 'ACT2160 compares the contents of the memory location addressed by A0-A12 with the address bits (or tag) applied at D0-D3. An equality is indicated by a high level on the MATCH1 or MATCH2 outputs. MATCH1 is high when the applied tag is equal to the stored tag in bank 1. MATCH2 is high when the applied tag is equal to the stored tag in bank 2.

writing to the cache tag RAMs

The manual/auto ($\overline{M}$/A) input on the 'ACT2160 provides two methods of selecting which tag bank will be written to when the write input ($\overline{W}$) is taken low. When $\overline{M}$/A is low, the bank select input (BSEL) selects the bank to be written to. BSEL low selects bank 1 and BSEL high selects bank 2. When $\overline{M}$/A is high, the least recently used (LRU) circuitry automatically selects the bank written to when $\overline{W}$ is taken low.

writing to the cache data RAMs

When a read or a write miss occurs and the cache is updated, the BANK output will indicate which bank the data should be written to. If BANK is low, bank 1 should be written to. If BANK is high, bank 2 should be written to. When writing a tag with $\overline{M}$/A low, the BANK output will not indicate which bank is being selected by the BSEL input. BANK is the output of the internal 8K x 1 LRU RAM. When a write hit occurs, the match outputs will indicate which data bank to write to.

LRU replacement circuitry

A concept commonly referred to in cache design is the property of locality. An aspect of the property of locality says that the information currently in use is likely to be used again soon. Based on this property, it is desirable to replace the information that has not been used recently when writing to cache. With a set size of two, this is easily done using one bit to indicate which of the two addressed locations is oldest or least recently used. The 'ACT2160 contains an 8K x 1 RAM and the necessary circuitry to implement the LRU replacement algorithm.

The $\overline{M}$/A input allows the user to choose between automatic LRU and manual replacement. When $\overline{M}$/A is high, the LRU RAM output selects which bank to write to. When the LRU bit for a given address is low, a write pulse will write D0-D3 to bank 1. When the LRU bit for a given address is high, a write pulse will write D0-D3 to bank 2. The LRU RAM is updated every time a write, a match (with LRU-W signal), or a word reset occurs.

When a write occurs with $\overline{M}$/A high, the addressed LRU bit is inverted and written back in so that the next write with $\overline{M}$/A high to that address will be to the other bank. When a write occurs with $\overline{M}$/A low, the bank is selected by the BSEL input and the addressed LRU bit is adjusted so that the next write to the same address with $\overline{M}$/A high will be to the other bank.

With a match output high indicating a match, the LRU RAM will also be updated when the LRU-W input is taken low. The logic level at each match output is fed back internally to the LRU circuitry. If MATCH1 or MATCH2 are high, the LRU-W input provides an LRU write timing signal that causes an internal LRU write pulse to be generated. With MATCH1 high, the LRU bit is set high so the next write to the same address with $\overline{M}$/A high will be to bank 2. With MATCH2 high, the LRU bit is set low so the next write to the same address with $\overline{M}$/A high will be to bank 1. When cascading these devices for wider address coverage, the MATCH1 outputs must be wire-ANDed together so an LRU write will not occur unless all MATCH1 outputs are high. In the same manner, the MATCH2 outputs (in width) must be tied together. When MATCH1 and MATCH2 are forced high during deselect, write, read, word reset, or reset, and LRU-W is taken low, a false LRU write will not occur.

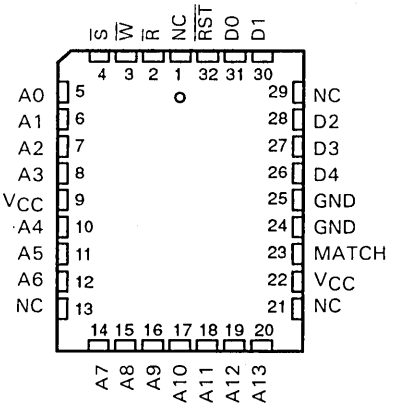
for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

D3298, SEPTEMBER 1989—REVISED JUNE 1990

- Fast Address to Match Delay
  20 ns Max — 'ACT2163
  18 ns Max — 'ACT2164
- Common I/O with Read Feature
- On-Chip Address/Data Comparator
- Easily Expanded in Depth and Width
- 'ACT2163 Has Totem-Pole Match Output
- 'ACT2164 Has Open-Drain Match Output Tested with 75-pF Load
- Reliable Advanced CMOS Technology
- Fully TTL Compatible

FM PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN74ACT2163 and SN74ACT2164 cache address comparators each consists of a high-speed 16K × 5 static RAM array and a 5-bit high-speed comparator. They are fabricated using advanced silicon-gate CMOS technology for high speed and simple interface with bipolar TTL circuits. The 'ACT2163 and 'ACT2164 cache address comparators are easily cascaded for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device.

When $\overline{S}$ is low and $\overline{W}$ and $\overline{R}$ are high, the cache address comparator compares the contents of the memory location addressed by A0-A13 with the data D0-D4. An equality is indicated by a high level on the MATCH output. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D4 is written in the 5-bit memory addressed by A0-A13.

The 'ACT2163 features a totem-pole MATCH output and the 'ACT2164 features an open-drain MATCH output. 'ACT2164 is designed to reduce the address-to-MATCH slow-down normally associated with a capacitively loaded open-drain output and is tested with a high capacitive load.

A read mode is provided with the 'ACT2163 and 'ACT2164, which allows the contents of RAM to be read at the D0-D4 pins. The read mode is selected when $\overline{R}$ and $\overline{S}$ are low and $\overline{W}$ is high.

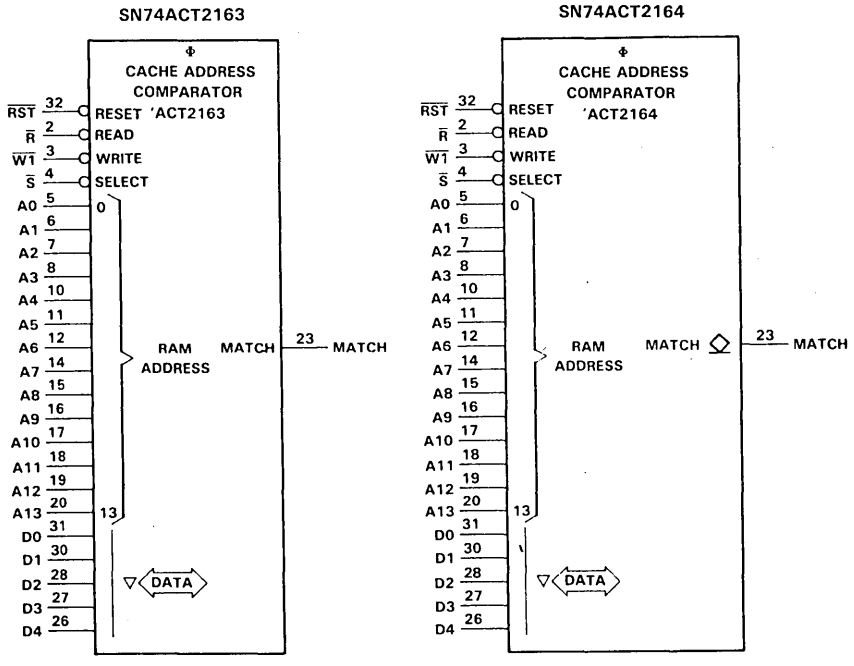
A reset input is provided for initialization. When $\overline{RST}$ is taken low, all 16K × 5 RAM locations are cleared to zero and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data is equal to the reset memory location. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction only one bit needs to be tied high regardless of the address width. These cache address comparators operate from a single 5-V supply and are offered in a 32-pin PLCC package.

The SN74ACT2163 and SN74ACT2164 are characterized for operation from 0°C to 70°C.

for complete data sheet

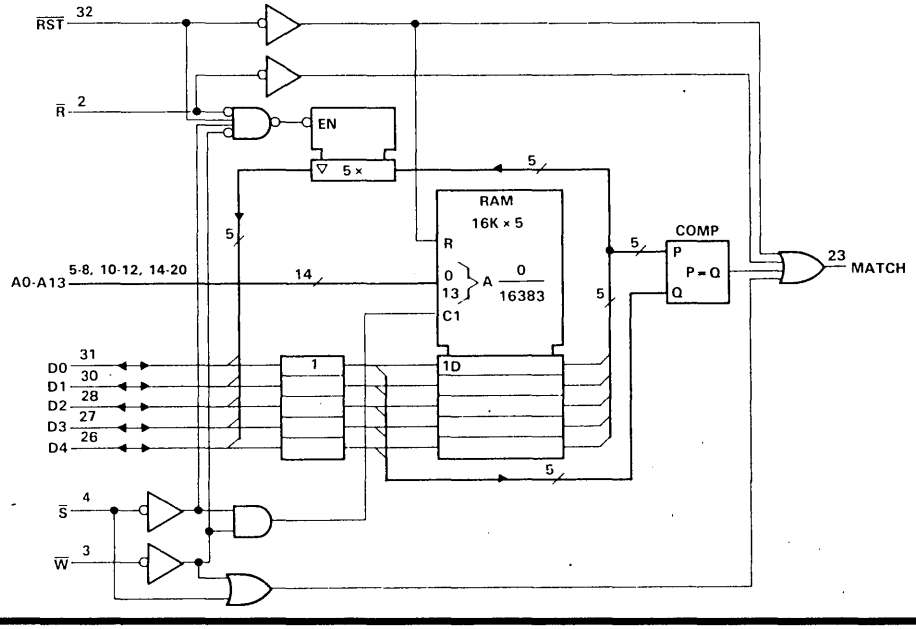
The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984.

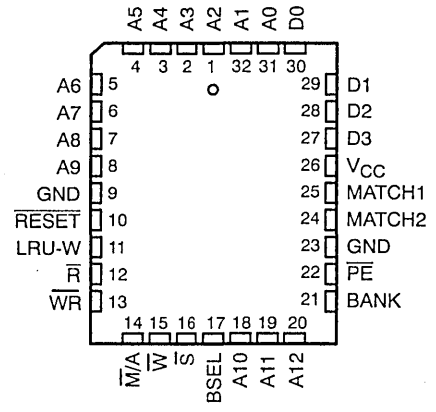
logic diagram (positive logic)



D3512, AUGUST 1990 — REVISED AUGUST 1990

- **Fast Address to Match Time . . . 12 ns Max**
- **2-Way Architecture Significantly Improves Hit Rate**
- **Implements LRU Replacement Algorithm**
- **Useful for Bus Watching**
- **On-Chip Parity Generator and Checker**
- **Easily Expandable in Depth and Width**
- **Reliable Advanced BiCMOS Technology**
- **Fully TTL Compatible**

FM PACKAGE
(TOP VIEW)



description

The SN74BCT2160 is a valuable building block for implementing fast two-way set associative caches. This device consists of two separate 8K x 5 RAMs for tag and parity storage, an 8K x 1 LRU RAM, two high-speed comparators, and the control circuitry necessary to give the designer the freedom to determine how this device will be used. The SN74BCT2160 also includes single-entry invalidation circuitry and parity generation and checking for ease of design and high system reliability.

The SN74BCT2160 is fabricated using advanced BiCMOS technology for high speed and simple interface with bipolar TTL circuits. By combining the SN74BCT2160 with programmable logic, a cache can be constructed that specifically addresses the individual system requirements. Significant reductions in cache memory component count, board area, and power dissipation can be achieved by using this device.

direct-mapped versus two-way set associative caches

A cache memory is a small high-speed memory that is used to store a portion of the data found in the larger main memory to achieve optimum processor performance and to reduce main memory bus traffic. Since the cache memory is smaller than the main memory, only part of the address, the least significant bits referred to as the index, is used to address the cache memory. The most significant address bits, called the tag, are stored along with the cache data and are used to identify what data is stored in an indexed location. When the processor requests data, the index portion of the processor address points to a word of data in the cache-data RAM and to a tag in the cache tag RAM. If the upper portion of the processor address is equal to the stored tag, a cache hit is said to occur and the cached data can be immediately sent to the processor.

In a direct-mapped or one-way set associative cache, only one data word and tag exist in cache for each index. This means that when the processor requests data, only one cache memory location can contain the requested data. Also, if the requested data is not in the cache and the cache is updated, the data in the indexed cache memory location will be written over regardless of how recently it has been used.

In a two-way set associative cache, two data words and tags exist for each index. This means that the requested data can reside in one of two cache locations. When a miss occurs and the cache is updated, the least recently used data can be written over. As would be expected, studies have shown that the hit rate improves significantly when using a two-way cache design over a one-way or direct-mapped cache design. Through use of the 'BCT2160, the logic complexity and parts count usually associated with a two-way cache are greatly reduced.

PRODUCT PREVIEW

address comparison

The 'BCT2160 compares the contents of the memory location addressed by A0-A12 with the address bits (or tag) applied at D0-D3. An equality is indicated by a high level on the MATCH1 or MATCH2 outputs. MATCH1 is high when the applied tag is equal to the stored tag in bank 1. MATCH2 is high when the applied tag is equal to the stored tag in bank 2.

writing to the 'BCT2160

The 'BCT2160 has been designed with self-timed write circuitry. A high-to-low transition at the $\overline{W}$ input initiates an internally generated write pulse. After a high-to-low transistion at $\overline{W}$, $\overline{W}$ may be held low without initiating additional write pulses. The manual/auto ($\overline{M}$/A) input on the 'BCT2160 provides two methods of selecting which tag bank will be written to when the write input ($\overline{W}$) is taken low. When $\overline{M}$/A is low, the bank select input (BSEL) selects the bank to be written to. BSEL low selects bank 1 and BSEL high selects bank 2. When $\overline{M}$/A is high, the least recently used (LRU) circuitry automatically selects the bank written to when $\overline{W}$ is taken low. The BANK output is latched when $\overline{W}$ goes low. This latch will return transparent when $\overline{W}$ returns high. When $\overline{W}$ is low the D0-D3 outputs are disabled. A high-to-low transition at the $\overline{S}$ input when $\overline{W}$ is low will not initiate a write (self-timed) pulse.

writing to the cache data RAMs

When a read or a write miss occurs and the cache is updated, the BANK output will indicate which bank the data should be written to. If BANK is low, bank 1 should be written to. If BANK is high, bank 2 should be written to. When writing a tag with $\overline{M}$/A low, the BANK output will not indicate which bank is being selected by the BSEL input. BANK is the output of the internal 8K x 1 LRU RAM. When a write hit occurs, the match outputs will indicate which data bank to write to.

LRU replacement circuitry

A concept commonly referred to in cache design is the property of locality. An aspect of the property of locality says that the information currently in use is likely to be used again soon. Based on this property, it is desirable to replace the information that has not been used recently when writing to cache. With a set size of two, this is easily done using one bit to indicate which of the two addressed locations is oldest or least recently used. The 'BCT2160 contains an 8K x 1 RAM and the necessary circuitry to implement the LRU replacement algorithm.

The $\overline{M}$/A input allows the user to choose between automatic LRU and manual replacement. When $\overline{M}$/A is high, the LRU RAM output selects which bank to write to. When the LRU bit for a given address is low, a write pulse will write D0-D3 to bank 1. When the LRU bit for a given address is high, a write pulse will write D0-D3 to bank 2. The LRU RAM is updated every time a write, a match (with LRU-W signal), or a word reset occurs.

When a write occurs with $\overline{M}$/A high, the addressed LRU bit is inverted and written back in so that the next write with $\overline{M}$/A high to that address will be to the other bank. When a write occurs with $\overline{M}$/A low, the bank is selected by the BSEL input and the addressed LRU bit is adjusted so that the next write to the same address with $\overline{M}$/A high will be to the other bank.

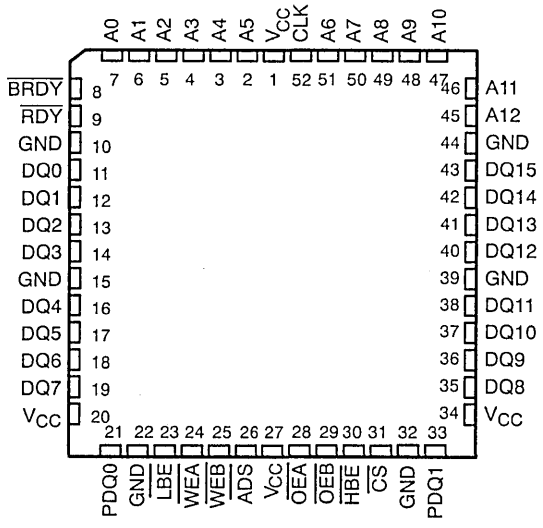
for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

D3613, AUGUST 1990

- 2-Way 8K x 18 Bit Architecture
- Designed Specifically for the i486™ Second-Level Cache
- Synchronous Read and Write Access at 50 MHz Clock Frequency
- Incorporates Burst Counter for Burst-Read (Read-Hit) Cycles or Burst-Write (Line-Fill) Cycles
- Self-Timed Write Cycle and Late Write Capability
- Fast Output Enable Time
- BiCMOS EPIC™ 0.8-μm Process

FN PACKAGE
(TOP VIEW)



description

The 'BCT2141 2-way 8K x 18-bit synchronous cache data RAM is designed to be used in the high-performance second-level cache memory system of the i486™ CPU. Synchronized read and write cycles with the 'BCT2141 can be performed at clock rates as high as 50 MHz. The 'BCT2141 is organized as two memory banks of 8K x 18. The 18-bit organization gives the designer two extra bits for byte parity storage. In addition to these features, the 'BCT2141 has address and data latches and a two-bit burst counter to support the i486™ burst operations. The on-chip self-timed write control logic completes the write cycles once the write cycle has been initiated. Bank A of the 2-way memory is enabled and written to by the $\overline{OEA}$ and $\overline{WEA}$ signals, respectively, and bank B by the corresponding $\overline{OEB}$ and $\overline{WEB}$ enable signals. The byte enable of both banks is controlled by the high-order byte enable, $\overline{HBE}$, and the lower-order byte enable, $\overline{LBE}$. Ultimately, the read and write accesses of the memory are controlled by the combination of these enable signals.

All access cycles, regardless of burst or non-burst cycles, are initiated internally with a low level at the address status signal ($\overline{ADS}$), a low-to-high transition at CLK, and a high level at $\overline{OEA}$, $\overline{OEB}$, $\overline{WEA}$, and $\overline{WEB}$. The A2-A12 address input latches are transparent when $\overline{OEA}$, $\overline{OEB}$, $\overline{WEA}$, and $\overline{WEB}$ are high. A2-A12 are latched when any of these enable signals are low. Address inputs, A0 and A1, are loaded into the burst circuitry during initialization. Once initialized, the assertion of an output enable signal will output the selected bank to the data outputs. The assertion of a write enable signal, after initialization, will cause a self-timed write pulse to be generated at the next rising clock edge provided that $\overline{RDY}$ or $\overline{BRDY}$ low, $\overline{ADS}$ high, and $\overline{LBE}$ or $\overline{HBE}$ low. Input data is latched at the same rising clock edge. The output enable and the write enable inputs also act as burst enable signals.

Initially, burst and non-burst access cycles are treated identically by the 'BCT2141. A non-burst memory access cycle is terminated by the de-assertion of the output enable or the write enable signal after one memory transfer. A burst memory access cycle, on the other hand, sequences through the memory locations on the clock rising edge with the activation of ready ($\overline{RDY}$) or burst ready ($\overline{BRDY}$) when the output enable or write enable remains active. The burst cycle is terminated either by completion of full count transfer (four read or write transfers) or by the de-assertion of the output enable or the write enable signal. Table 1 shows the 'BCT2141 burst counter sequences.

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.
i486 is a trademark of Intel Corporation.
This device is covered by patent numbers

description (continued)

A burst read cycle is initiated by either a low-going $\overline{OEA}$ or a low-going $\overline{OEB}$. Only one of the output enable signals is allowed to be low at a time. Enabling both banks simultaneously may electrically damage the device. Typically, the 'BCT2141 is capable of supplying one word of data per clock cycle after the initial T1 cycle of the i486™ during burst mode. The 'BCT2141 is designed so that each word of data is valid to meet the setup and hold times required by the i486™. A low $\overline{BRDY}$ input indicates to the data RAM to continue with the next word of the burst access. Figure 9 shows a typical non-burst and burst read cycle.

Similarly, a burst write cycle is initiated by either a low-going $\overline{WEA}$ or a low-going $\overline{WEB}$. Again only one of the write enable signals is allowed to be low at a time. Writing to both banks simultaneously will cause the data being written to be corrupted. For the burst write cycle, data must be supplied on the data inputs to meet the setup and hold time requirements of the 'BCT2141. Figure 6 illustrates a typical non-burst and burst write cycle.

Assertion of $\overline{RDY}$ during a burst cycle interrupts the burst cycle of the i486™. The 'BCT2141 responds to this interruption by ignoring the address that is supplied by the CPU since this interruption is designed for memory devices that are not able to respond to the CPU's burst requests. The burst counter of the 'BCT2141 is disabled with a low level at $\overline{ADS}$, as provided by the i486™. Upon assertion of the next $\overline{RDY}$ or $\overline{BRDY}$ signal, and the de-assertion of $\overline{ADS}$, the 'BCT2141 resumes the burst access cycle with its own internal latched address. Figure 10 shows an interrupted burst read cycle, and Figure 7 shows an interrupted burst write cycle. Figure 8 illustrates early termination of the burst write cycle with three complete write operations. Figure 11 shows early termination of the burst read cycle with three complete read operations.

The SN74BCT2141 is characterized over the commercial temperature range of 0°C to 70°C.

using the 'BCT2141 for other applications

The 'BCT2141 can also be used in applications other than i486™ based cache where the burst counter is not required. The 'BCT2141 can simply be used in the non-burst mode. The $\overline{ADS}$ signal must still be used for initialization and $\overline{RDY}$ or $\overline{BRDY}$ must be asserted for proper write operation.

Table 1 Burst Counter Sequence

ADDRESS	A1	A0	A1	A0	A1	A0	A1	A0
Starting	0	0	0	1	1	0	1	1
Second	0	1	0	0	1	1	1	0
Third	1	0	1	1	0	0	0	1
Fourth	1	1	1	0	0	1	0	0

for complete data sheet

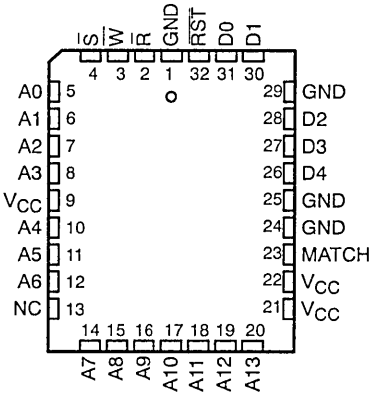
The complete version of this data sheet and application information can be obtained by calling the DVP Applications Group at 214-997-5762.

PRODUCT PREVIEW

D3513, JUNE 1990 — REVISED AUGUST 1990

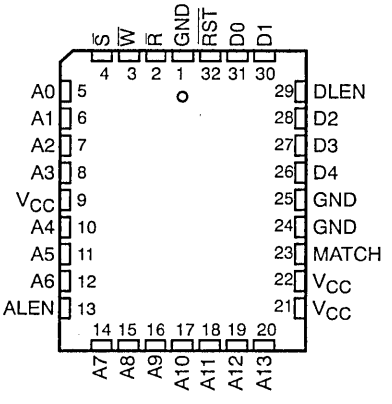
- Fast Address to MATCH Delay . . .12-ns Max
- 'BCT2163 has Totem-Pole Match Output
- 'BCT2164 and 'BCT2166 have Open-Drain Match Outputs Tested with 75-pF Load
- 'BCT2166 has Input Latches
- Self-Timed Write Circuitry
- Common I/O with Read Feature
- On-Chip Address/Data Comparator
- Easily Expanded in Depth and Width
- Reliable Advanced BiCMOS Technology
- Fully TTL Compatible

SN74BCT2163, SN74BCT2164
FM PACKAGE
(TOP VIEW)



NC – No internal connection

SN74BCT2166 . . . FM PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'BCT2163, 'BCT2164, and 'BCT2166 cache address comparators each consists of a high-speed 16K x 5 static RAM array and a 5-bit high-speed comparator. The 'BCT2166 has latches at the address, data, and select inputs. They are fabricated using advanced BiCMOS technology for high speed and simple interface with bipolar TTL circuits. The 'BCT2163, 'BCT2164, and 'BCT2166 address comparators are easily cascaded for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with these devices.

When $\overline{S}$ is low and $\overline{W}$ and $\overline{R}$ are high, the cache address comparator compares the contents of the memory location addressed by A0-A13 with the applied D0-D4. An equality is indicated by a high level on the MATCH output.

The 'BCT2163, 'BCT2164, and 'BCT2166 have been designed with self-timed write circuitry. A high-to-low transition at the $\overline{W}$ input initiates an internally generated write pulse. After a high-to-low transition at $\overline{W}$, $\overline{W}$ may be held low without initiating additional write pulses. When W is low the D0-D3 outputs are disabled. A high-to-low transition at the $\overline{S}$ input when $\overline{W}$ is low will not initiate a write (self-timed) pulse. During a write cycle the input levels on D0-D4 are written in the 5-bit memory addressed by A0-A13.

The 'BCT2163 features a totem-pole MATCH output and the 'BCT2164 and 'BCT2166 feature an open-drain MATCH output. The 'BCT2164 and 'BCT2166 are designed to reduce the address-to-MATCH slow-down normally associated with capacitively loaded open-drain outputs and are tested with a high capacitive load.

A read mode is provided with the 'BCT2163, 'BCT2164, and 'BCT2166 which allows the contents of RAM to be read at the D0-D4 pins. The read mode is selected when $\overline{R}$ and $\overline{S}$ are low and $\overline{W}$ is high.

description (continued)

A reset input is provided for initialization. When $\overline{RST}$ is taken low, all 16K x 5 RAM locations are cleared to zero and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data is equal to the reset memory location. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction only one bit needs to be tied high regardless of the address width. After power-up, these devices must be initialized by resetting the device to ensure that all memory locations are at a known state. These devices could also be initialized by writing to every memory location.

The 'BCT2166 is equipped with latches at the address, data, and select inputs. Input ALEN controls the latch at the A0-A13 and $\overline{S}$ inputs. DLEN controls the latch at the D0-D4 inputs. The latches are transparent when ALEN and DLEN are high and latched when ALEN and DLEN are low.

The SN74BCT2163, SN74BCT2164, and SN74BCT2166 are characterized for operation from 0°C to 70°C. These cache address comparators operate from a single 5-V supply and are offered in a 32-pin PLCC package.

for complete data sheet

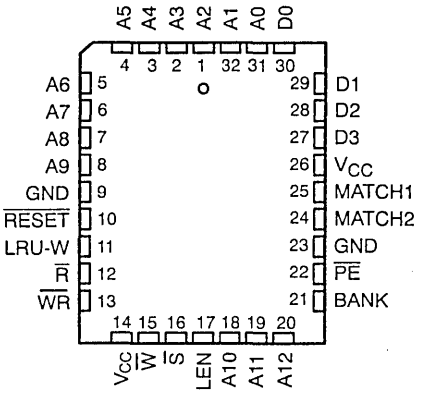
The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

PRODUCT PREVIEW

D3614, SEPTEMBER 1990

- Address to Match Time . . . 12 ns Max
- Simlar to SN74ACT2160 and SN74BCT2160 but with:
  - Latches Added
  - Integrated Invalidation and Read Cicuitry
  - No Manual Operation
- 2-Way Architecture Significantly Improves Hit Rate
- Implements LRU Replacement Algorithm
- Useful for Bus Watching
- On-Chip Parity Generator and Checker
- Easily Expandable in Depth and Width
- Reliable Advanced BiCMOS Technology
- Fully TTL Compatible

FM PACKAGE
(TOP VIEW)



description

The SN74BCT2165 is a valuable building block for implementing fast two-way set associative caches. This device consists of two separate 8K x 5 RAMs for tag and parity storage, an 8K x 1 LRU RAM, two high-speed comparators, and the control circuitry necessary to give the designer the freedom to determine how this device will be used. The SN74BCT2165 also includes single-entry invalidation circuitry and parity generation and checking for ease of design and high system reliability.

The SN74BCT2165 is fabricated using advanced BiCMOS technology for high speed and simple interface with bipolar TTL circuits. By combining the SN74BCT2165 with programmable and/or ASIC logic, a cache can be constructed that specifically addresses the individual system requirements. Significant reductions in cache memory component count, board area, and power dissipation can be achieved by using this device.

direct-mapped versus two-way set associative caches

A cache memory is a small high-speed memory that is used to store a portion of the data found in the larger main memory to achieve optimum processor performance and to reduce main memory bus traffic. Since the cache memory is smaller than the main memory, only part of the address, the least significant bits referred to as the index, is used to address the cache memory. The most significant address bits, called the tag, are stored along with the cache data and are used to identify what data is stored in an indexed location. When the processor requests data, the index portion of the processor address points to a word of data in the cache-data RAM and to a tag in the cache tag RAM. If the upper portion of the processor address is equal to the stored tag, a cache hit is said to occur and the cached data can be immediately sent to the processor.

In a direct-mapped or one-way set associative cache, only one data word and tag exist in cache for each index. This means that when the processor requests data, only one cache memory location can contain the requested data. Also, if the requested data is not in the cache and the cache is updated, the data in the indexed cache memory location will be written over regardless of how recently it has been used.

In a two-way set associative cache, two data words and tags exist for each index. This means that the requested data can reside in one of two cache locations. When a miss occurs and the cache is updated, the least recently used data can be written over. As would be expected, studies have shown that the hit rate improves significantly when using a two-way cache design over a one-way or direct-mapped cache design. Through use of the 'BCT2165, the logic complexity and parts count usually associated with a two-way cache are greatly reduced.

PRODUCT PREVIEW

address comparison

The 'BCT2165 compares the contents of the memory location addressed by A0-A12 with the address bits (or tag) applied at D0-D3. An equality is indicated by a high level on the MATCH1 or MATCH2 outputs. MATCH1 is high when the applied tag is equal to the stored tag in bank 1. MATCH2 is high when the applied tag is equal to the stored tag in bank 2.

writing to the 'BCT2165

The 'BCT2165 has been designed with self-timed write circuitry. A high-to-low transition at the $\overline{W}$ input initiates an internally generated write pulse. After a high-to-low transistion at $\overline{W}$, $\overline{W}$ may be held low without initiating additional write pulses. The bank written at the falling edge of $\overline{W}$ is automatically selected by the output of the LRU RAM. When the addressed LRU bit is low, bank 1 is selected; and when the addressed LRU bit is high, bank 2 is selected. Since the bank to be written to is selected only by the LRU bit the tag should not be rewritten during a write hit (match). The BANK output is latched when $\overline{W}$ goes low. This latch will return transparent when $\overline{W}$ returns high. When $\overline{W}$ is low the D0-D3 outputs are disabled. A high-to-low transition at the $\overline{S}$ input when $\overline{W}$ is low will not initiate a write (self-timed) pulse. During a write cycle the input levels at D0-D3 plus generated partity are written into the 5-bit memory location addressed by A0-A12 in the selected bank.

writing to the cache data RAMs

When a read or a write miss occurs and the cache is to be updated, the BANK output will indicate which bank the data should be written to. If BANK is low, bank 1 should be written to. If BANK is high, bank 2 should be written to. BANK is the output of the internal 8K x 1 LRU RAM. When a write hit occurs, the match outputs will indicate which data bank to write to.

PRODUCT PREVIEW

LRU replacement circuitry

A concept commonly referred to in cache design is the property of locality. An aspect of the property of locality says that the information currently in use is likely to be used again soon. Based on this property, it is desirable to replace the information that has not been used recently when writing to cache. With a set size of two, this is easily done using one bit to indicate which of the two addressed locations is oldest or least recently used. The 'BCT2165 contains an 8K x 1 RAM and the necessary circuitry to implement the LRU replacement algorithm.

The LRU replacement algorithm is performed automatically in the 'BCT2165. The LRU RAM output determines which bank is written to. When the LRU bit for a given address (A0-A12) is low, a write pulse will write D0-D3 to bank 1. When the LRU bit for a given address is high, a write pulse will write D0-D3 to bank 2. The LRU RAM is updated every time a write, a match (with LRU-W signal), or a word reset occurs.

When a write occurs, the addressed LRU bit is inverted and written back in so that the next write to that address will be to the other bank. When a match occurs (MATCH1 high or MATCH2 high), the LRU RAM is updated when the LRU-W input is taken low. The logic level at each match output is fed back internally to the LRU circuitry. If MATCH1 or MATCH2 are high, the LRU-W input provides an LRU write timing signal that causes an internal LRU write pulse to be generated. With MATCH1 high, the LRU bit is set high so the next write to the same address will be to bank 2. With MATCH2 high, the LRU bit is set low so the next write to the same address will be to bank 1. When cascading these devices for wider address coverage, the MATCH1 outputs must be wire-ANDed together so an LRU write will not occur unless all MATCH1 outputs are high. In the same manner, the MATCH2 outputs (in width) must be tied together. When MATCH1 and MATCH2 are forced high during deselect, write, read, word reset, or reset, and LRU-W is taken low, a false LRU write will not occur. When a word reset occurs, the addressed LRU bit is updated so that the next write to that address will be to the reset (invalidated) location.

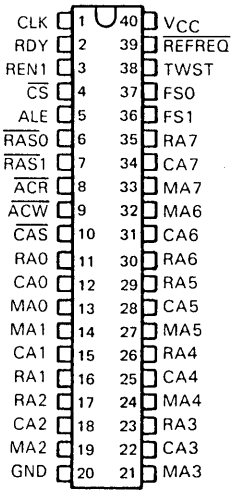
for complete data sheet

The complete version of this data sheet and application information can be obtained by calling the DVP Applications Group at 214-997-5762.

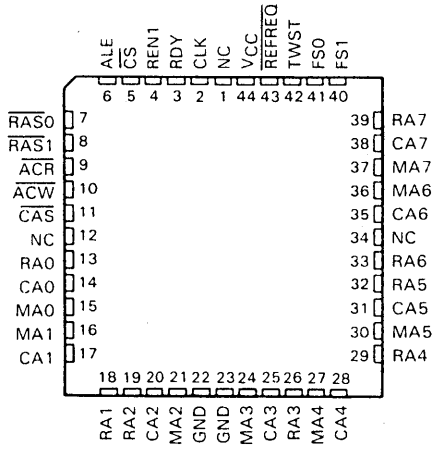
D2674, JANUARY 1982 REVISED AUGUST 1985

- Controls Operation of 8K, 16K, 32K, and 64K Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 256K Bytes of Memory Without External Devices
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
  - Strap-Selected Refresh Rate
  - Synchronous, Predictable Refresh
  - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
  - Interfaces Easily to Popular Microprocessors
- Strap-Selected Wait-State Generation for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)
- 3-State Outputs Allow Multiport Memory Configuration
- Performance Ranges of 150 ns, 200 ns, or 250 ns

TMS4500A . . . N PACKAGE
(TOP VIEW)



TMS4500A . . . FN PACKAGE
(TOP VIEW)



description

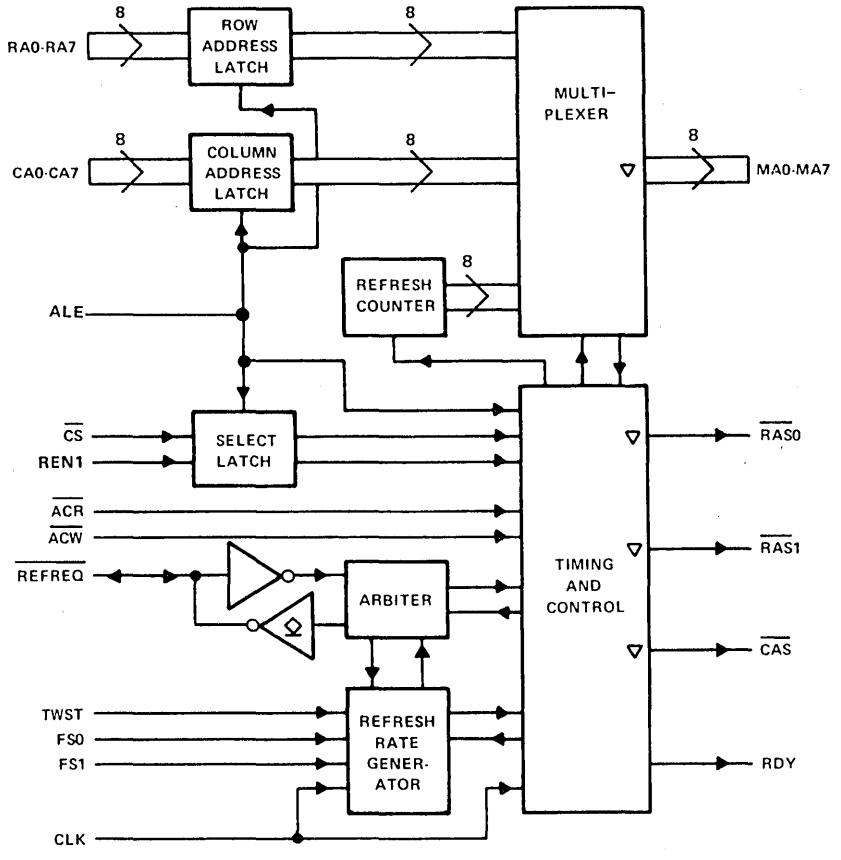
The TMS4500A is a monolithic DRAM system controller designed to provide address multiplexing, timing;, control and refresh/accesss arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

The controller contains a 16-bit multiplexer that generates the address lines for the memory device from the 16 system address bits and provides the strobe signals required by memory to decode the address. An 8-bit refresh counter generates the 256-row addresses required for refresh.

A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure date retention.

The TMS4500A also contains refresh/access arbitration circuitry to resolve conflicts between memory access requests and memory refresh cycles. The TMS4500A is offered in a 40-pin, 600-mil dual-in-line plastic package and 44-pin, 650-mil square plastic carrier package. It is characterized for operation from 0°C to 70°C.

functional block diagram



for complete data sheet

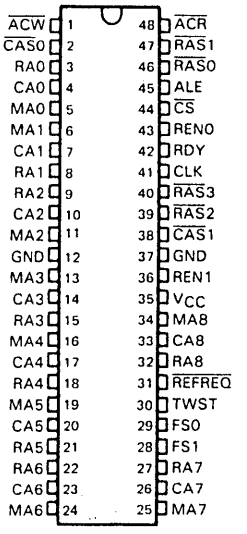
The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

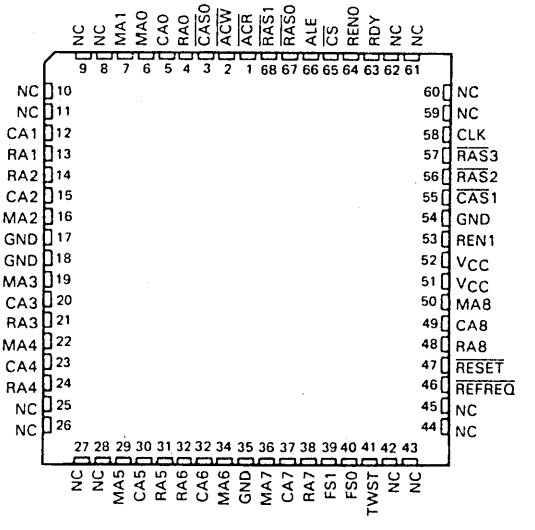
D2989, JUNE 1987—REVISED MARCH 1990

- Inputs are TTL- and CMOS-Voltage Compatible
- Controls Operation of 64K and 256K Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 2M Byte of Memory Without External Drivers
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
  - Strap-Selected Refresh Rate
  - Synchronous, Predictable Refresh
  - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
  - Interfaces Easily to Popular Microprocessors
  - Asynchronous $\overline{\text{RESET}}$ Function Provided in FK and FN Packages
- High-Performance Si-Gate CMOS Technology
- Strap-Selected Wait State Generation for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)
- 3-State Outputs Allow Multiport Memory Configuration
- Performance Range:
  115 ns ALE low to $\overline{\text{CAS}}$ low
- Functionally Equivalent to TMS4500A/B and to VTI VL4500A and VL4502
- Available in Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

JD OR N PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

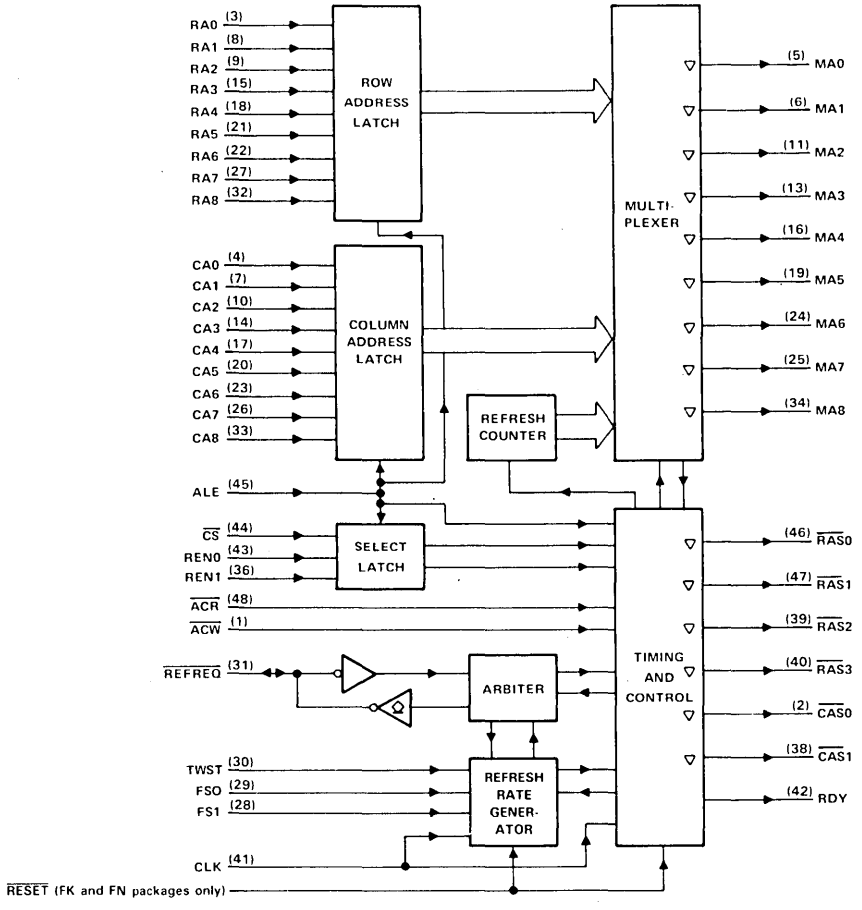
The THCT4502B is a monolithic DRAM system controller providing address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

The controller contains an 18-bit multiplexer that generates the address lines for the memory device from the 18 system address bits and provides the strobe signals required by the memory to decode the address. A 9-bit refresh counter generates up to 512 row addresses required to refresh.

for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

functional block diagram†

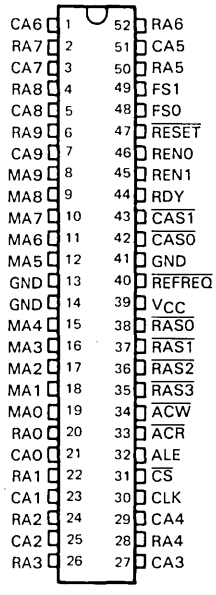


†Pin numbers shown are for JD and N packages.

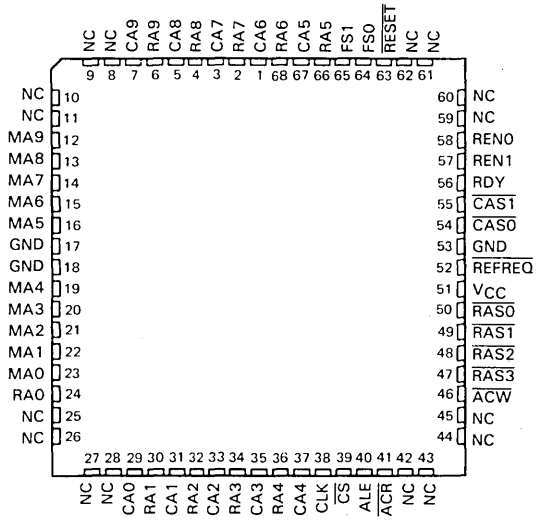
D3132, SEPTEMBER 1988—REVISED MAY 1989

- Inputs are TTL- and CMOS-Voltage Compatible
- Controls Operation of 64K, 256K, and 1M Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 4 Banks of Memory
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
  - Strap-Selected Refresh Rate
  - Synchronous, Predictable Refresh
  - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
  - Interfaces Easily to Popular Microprocessors
  - Asynchronous $\overline{\text{RESET}}$
  - Choice of CLK Polarity on Refresh/Access Arbitration
- High-Performance Si-Gate CMOS Technology
- Strap-Selected Refresh Frequencies for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)
- 3-State Outputs Allow Multiport Memory Configuration
- Performance Range:
  100 ns ALE low to $\overline{\text{CAS}}$ low
- Functionally Compatible with TMS4500A/B and with THCT4502B
- Available in Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

JD OR N PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The 'ACT4503 is a monolithic DRAM system controller providing address multiplexing, timing, control, and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

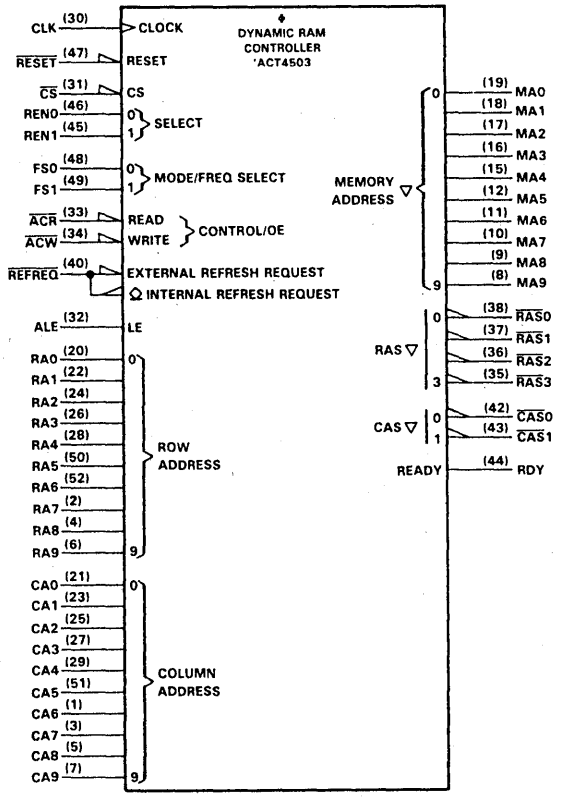
The controller contains an 20-bit multiplexer that generates the address lines for the memory device from the 20 system address bits and provides the strobe signals required by the memory to decode the address. A 10-bit refresh counter generates up to 1024 row addresses required to refresh.

A refresh timer is provided to generate the necessary timing to refresh the dynamic memories and ensure data retention.

for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

logic symbol†

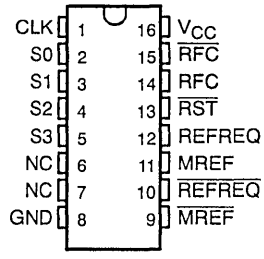


†This symbol is in accordance with ANSI/IEEE Std. 91-1984.
Pin numbers shown are for JD and N packages.

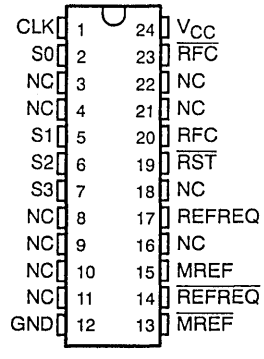
D3311, DECEMBER 1989–REVISED JULY 1990

- **Supports 16 Most Popular Microprocessor Speeds**
- **Supports Distributive- and Hidden-Refresh Operations**
- **Polarity Options Available for RFC, REFREQ, and MREF Signals**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

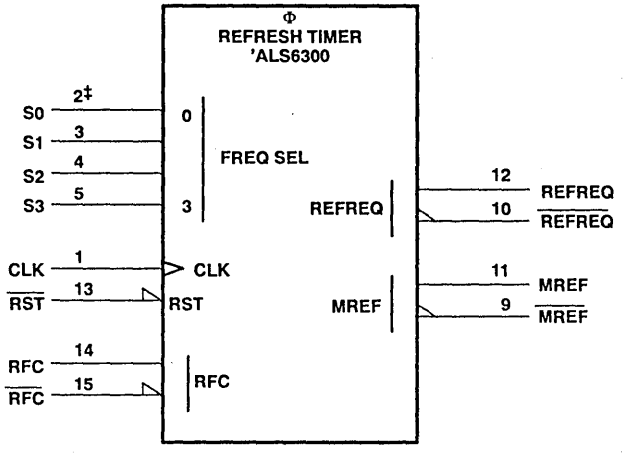
The 'ALS6300 input-selectable memory refresh timer allows the user to select one of sixteen popular divisor rates in order to generate appropriate refresh timing control signals to a memory timing control device. The flexible divide-by rates are based on the most widely used microprocessor clock frequencies and the most common dynamic RAM refresh timing requirements. In addition, this device supports both distributive- and hidden-refresh strategy by providing a refresh request signal (REFREQ) and a mandatory refresh signal (MREF). For design flexibility, the 'ALS6300 provides both active-high and active-low refresh request outputs (REFREQ and $\overline{\text{REFREQ}}$), mandatory refresh outputs (MREF and $\overline{\text{MREF}}$), and refresh-complete inputs (RFC and $\overline{\text{RFC}}$).

The DRAM memory refresh timer is basically a programmable frequency divider with special modifications to enhance its use as a refresh timer. The divisor rate is selected by applying the appropriate logic levels to the S0-S3 inputs shown in Table 1. When the internal counter reaches the selected divisor rate, REFREQ and $\overline{\text{REFREQ}}$ will go active (high and low, respectively) and stay active until an active level is seen on the RFC or $\overline{\text{RFC}}$ input. The 'ALS6300 will automatically generate a mandatory refresh signal, MREF and $\overline{\text{MREF}}$, if an active RFC or $\overline{\text{RFC}}$ is not received before 20 clock cycles before the next request. An active level on the RFC or $\overline{\text{RFC}}$ input will force REFREQ, $\overline{\text{REFREQ}}$, MREF, and $\overline{\text{MREF}}$ to their inactive states.

To achieve distributive refresh, either REFREQ, $\overline{\text{REFREQ}}$, MREF, or $\overline{\text{MREF}}$ can be used to activate the refresh cycle. When using hidden refresh, an active level on either REFREQ or $\overline{\text{REFREQ}}$ indicates that a refresh cycle should be performed immediately after the next memory access cycle. MREF or $\overline{\text{MREF}}$ is used to indicate that an access has not occurred during the given refresh period and to force the timing controller to initiate a refresh cycle within the next 20 clock periods.

A low level on the $\overline{\text{RST}}$ input clears the internal counter and sets the REFREQ, $\overline{\text{REFREQ}}$, MREF, and $\overline{\text{MREF}}$ outputs to their inactive state on the next active clock edge.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.
‡ Pin numbers are for N package.

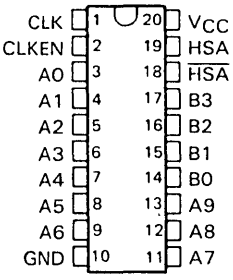
for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

D3020, JUNE 1987—REVISED DECEMBER 1989

- **Detects Present Row Equal to Last Row Address**
- **High-Performance Compare:**
  'ALS6310A CLK to HSA = 18 ns
  'ALS6311A Address to HSA = 14 ns
- **Compatible with 16K to 1M DRAMs**
- **Easily Interfaced with Microprocessor and Memory Timing Controller**
- **Dependable Texas Instruments Quality and Reliability**

DW OR N PACKAGE
(TOP VIEW)



description

The 'ALS6310A and 'ALS6311A are high-performance address comparators designed for implementing static column and page-mode access cycles.

When interfaced with the memory timing controller, these devices will detect if the present row being accessed is the same as the last row accessed. This is the fundamental requirement for implementing static column decode or page-mode access cycles.

The 'ALS6310A features two 14-bit registers and a high-speed address comparator. The first register is used to save the present row address while the second register is used to save the previous row address. On the high-to-low transition of CLK, the first register loads the new row address present on A0-A9. At the same time, the second register loads the address previously saved in the first register. The two row addresses are then compared. The High-Speed Access outputs (HSA and $\overline{\text{HSA}}$) will signal if the two addresses are equal.

The B0-B1 inputs are provided to monitor access cycles to different banks of memory. When used in conjunction with the 'ALS2968 and 'ALS6302 series DRAM controllers, the 'ALS6310A and 'ALS6311A can monitor up to 16 banks of memory. The CLK input on the 'ALS6310A can typically be interfaced with the microprocessor's Address Latch Enable (ALE) or Address Strobe (AS) outputs. This configuration simplifies the memory timing controller interface. Refer to the typical application diagram for further information.

The 'ALS6311A features one 14-bit register feeding a high-speed address comparator. This architecture offers a faster address match time, but does require the memory timing controller to generate the CLK input. Typically, the 14-bit register would only be updated if there was a change in row or bank address. Refer to the application diagram for further information.

More information on static column DRAM access can be found in the Texas Instruments application report *System Solutions for Static Column Decode*.

The SN74ALS6310A and SN74ALS6311A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE ('ALS6310A)

INPUTS				OUTPUTS	
CLKEN	CLK	A0-A9	B0-B3	HSA	$\overline{HSA}$
H	↓	P=Q	P=Q	H	L
H	↓	P=Q	P≠Q	L	H
H	↓	P≠Q	P=Q	L	H
H	↓	P≠Q	P≠Q	L	H
X	H	X	X	HSA_0	$\overline{HSA0}$
L	X	X	X	HSA_0	$\overline{HSA_0}$

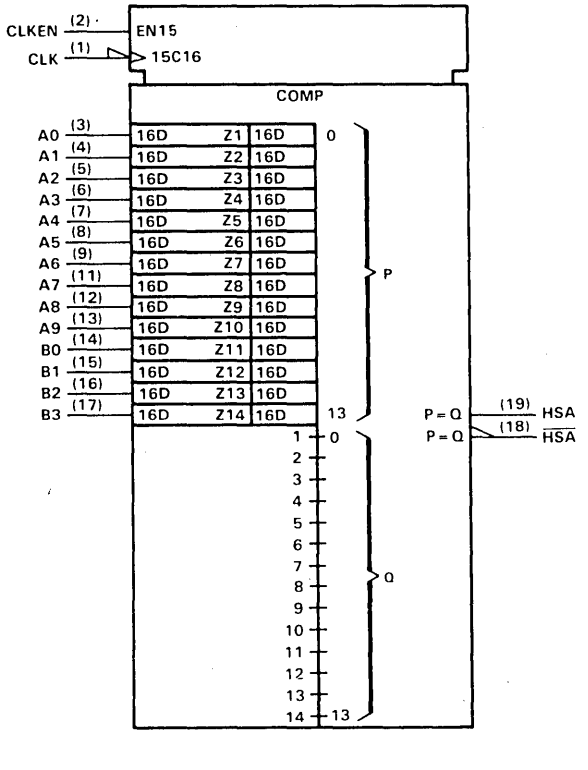
FUNCTION TABLE ('ALS6311A)

INPUTS				OUTPUTS	
CLKEN	CLK	A0-A9	B0-B3	HSA	$\overline{HSA}$
H	↑	X	X	H	L
X	X	P=Q	P=Q	H	L
X	Not↑	X	P≠Q	L	H
X	Not↑	P≠Q	X	L	H
L	X	X	P≠Q	L	H
L	X	P≠Q	X	L	H

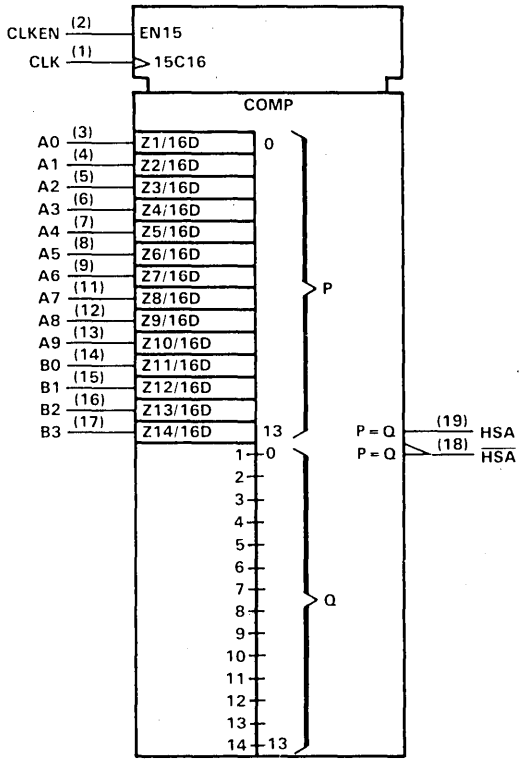
P = previous address
Q = present address

logic symbols†

'ALS6310A



'ALS6311A



†These symbols are in accordance with ANSI/IEEE Std 91 1984 and IEC Publication 617-12.

for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

D3305, JULY 1989 — REVISED AUGUST 1990

- **Multiplexed Real-Time and Latched Data**
- **Byte Control for Byte-Write Applications**
- **Useful in NuBus™ Interface Applications**
- **Useful in Memory Interleave Applications**
- **BiCMOS Design Substantially Reduces Standby Current**
- **Dependable Texas Instruments Quality and Reliability**

description

The 'BCT2423A and 'BCT2424A are a general-purpose 16-bit bidirectional transceiver with data storage latches and byte control circuitry arranged for use in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor- or bus-interface applications. This device is also useful in memory-interleaving applications. The 'BCT2423A and 'BCT2424A offer inverted data paths.

The 'BCT2423A and 'BCT2424A are designed using Texas Instruments BiCMOS process, which features bipolar drive characteristics. In addition, it greatly reduces the standby power of the device when disabled. This is valuable when the device is not performing an address or data transfer.

Three 16-bit I/O ports, A15-A0, B15-B0, and $\overline{AB}15$-$\overline{AB}0$ are available for address and/or data transfer. The $\overline{AENM}$, $\overline{AENL}$, $\overline{BENM}$, $\overline{BENL}$, $\overline{ABENM}$, and $\overline{ABENL}$ inputs control the bus transceiver functions. These control signals also allow byte-control of the most significant byte and least significant byte for each bus.

Address and/or data information can be stored using the internal storage latches. The $\overline{ALE}$, $\overline{BLE}$, $\overline{ABLEA}$, and $\overline{ABLEB}$ inputs are active low and are used to control data storage. When the latch enable input is low, the latch is transparent. When the latch enable input goes high, the data present at the inputs is latched and remains latched until the latch enable input is returned low.

Data on the 'A' bus and 'B' bus are multiplexed onto the '$\overline{AB}$' bus via the $\overline{A}$/BSEL control line. When $\overline{A}$/BSEL is low, A15-A0 is mapped to the $\overline{AB}15$-$\overline{AB}0$ outputs. When $\overline{A}$/BSEL is high, B15-B0 is mapped to the $\overline{AB}15$-$\overline{AB}0$ outputs.

The 'BCT2423A and 'BCT2424A are characterized for operation from 0°C to 70°C.

ADVANCE INFORMATION

NuBus is a trademark of Texas Instruments Incorporated.

Terminal Functions

PIN NAME	PIN NO.	DESCRIPTION
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13	5 6 7 8 10 11 12 14 15 16 17 18 19 20	Address inputs. Address 1 of 16K by 5-bit RAM memory locations. Must be stable for the duration of the write cycle.
ALEN ('BCT2166 Only)	13	Address and select latch enable input. When ALEN is high the latch is transparent. When ALEN is low A0-A13 and $\overline{S}$ are latched.
D0 D1 D2 D3 D4	31 30 28 27 26	Data (tag) inputs/outputs. D0-D4 are inputs during the compare and write modes. D0-D4 are outputs during the read mode.
DLEN ('BCT2166 Only)	29	Data latch enable input. When DLEN is high the latch is transparent. When DLEN is low D0-D4 are latched.
GND	1 24 25 29	Ground. (Pin 29 ground is for 'BCT2163 and 'BCT2164 only.)
MATCH	23	When MATCH output is high during a compare cycle, D0-D4 equals the contents of the 5-bit memory location addressed by A0-A13. MATCH is also driven high during deselect, reset, read, and write.
$\overline{R}$	2	Read input. When $\overline{R}$ and $\overline{S}$ are low and $\overline{W}$ is high, addressed data is output to the D0-D4 pins and the MATCH output is forced high.
$\overline{RST}$	32	Reset input. Aschronously clears entire RAM array to zero and forces MATCH high when $\overline{RST}$ is low.
$\overline{S}$	4	Chip select input. Enables device when $\overline{S}$ is low. Deselects device and forces MATCH high when $\overline{S}$ is high.
V_{CC}	9 21 22	Supply voltage.
$\overline{W}$	3	Write control input. Writes D0-D4 into the RAM location addressed by A0-A13 and forces MATCH high when $\overline{W}$ is low. Places selected device in compare mode when $\overline{W}$ and $\overline{R}$ are high and $\overline{S}$ is low.

PRODUCT PREVIEW

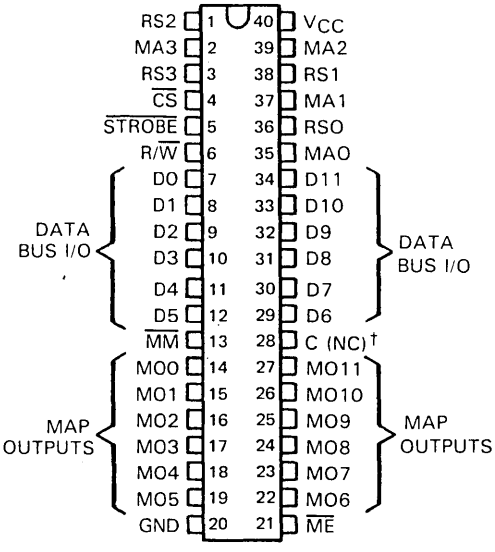
for complete data sheet

The complete version of this data sheet and application information can be obtained by calling the DVP Applications Group at 214-997-5762.

D2549, JANUARY 1981—REVISED APRIL 1990

- **Expands 4 Address Lines to 12 Address Lines**
- **Designed for Paged Memory Mapping**
- **Output Latches Provided on 'LS610**
- **3-State Map Outputs**
- **Compatible with TMS9900 and Other Microprocessors**

JD OR N PACKAGE
(TOP VIEW)



†This pin has no internal connection on the 'LS612.

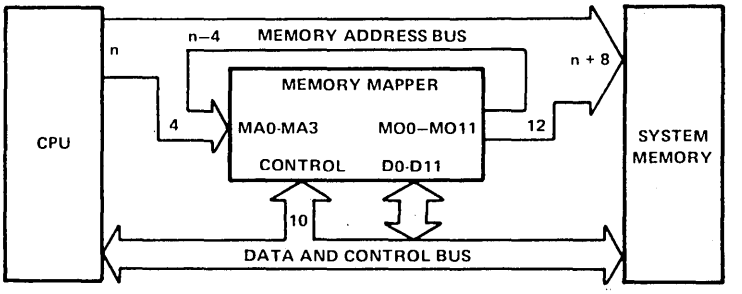
description

Each 'LS610 and 'LS612 memory-mapper integrated circuit contains a 4-line to 16-line decoder, a 16-word by 12-bit RAM, 16 channels of 2-line to 1-line multiplexers, and other miscellaneous circuitry on a monolithic chip. Each 'LS610 also contains 12 latches with an enable control.

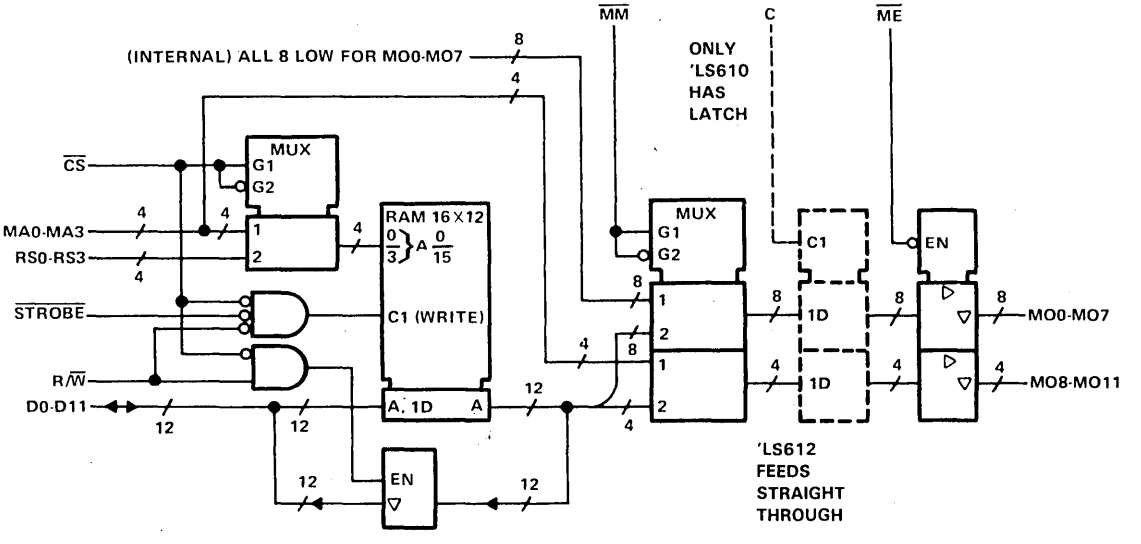
The memory mappers are designed to expand a microprocessor's memory address capability by eight bits. Four bits of the memory address bus (see System Block Diagram) can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus through the map output buffers along with the unused memory address bits from the CPU. However, addressable memory space without reloading the map registers is the same as would be available with the memory mapper left out. The addressable memory space is increased only by periodically reloading the map registers from the data bus. This configuration lends itself to memory utilization of 16 pages of $2^{(n-4)}$ registers each without reloading (n = number of address bits available from CPU).

These devices have four modes of operation: read, write, map, and pass. Data may be read from or loaded into the map register selected by the register select inputs (RSO thru RS3) under control of R/$\overline{W}$ whenever chip select ($\overline{CS}$) is low. The data I/O takes place on the data bus D0 thru D7. The map operation will output the contents of the map register selected by the map address inputs (MA0 thru MA3) when $\overline{CS}$ is high and $\overline{MM}$ (map mode control) is low. The 'LS612 output stages are transparent in this mode, while the 'LS610 outputs may be transparent or latched. When $\overline{CS}$ and $\overline{MM}$ are both high (pass mode), the address bits on MA0 thru MA3 appear at M08-M011, respectively, (assuming appropriate latch control) with low levels in the other bit positions on the map outputs.

system block diagram



logic diagram (positive logic)



for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

D3396, JANUARY 1986–REVISED JANUARY 1990

- **Detects and Corrects Single-Bit Errors**
- **Detects and Flags Dual-Bit Errors**
- **Built-In Diagnostic Capability**
- **Fast Write and Read Cycle Processing Times**
- **Byte-Write Capability**
- **Dependable Texas Instruments Quality and Reliability**

description

The 'ALS632B and 'AS632 devices are 32-bit parallel error detection and correction circuits (EDACs). The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

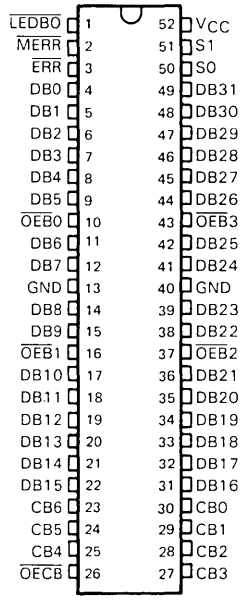
Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit data word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

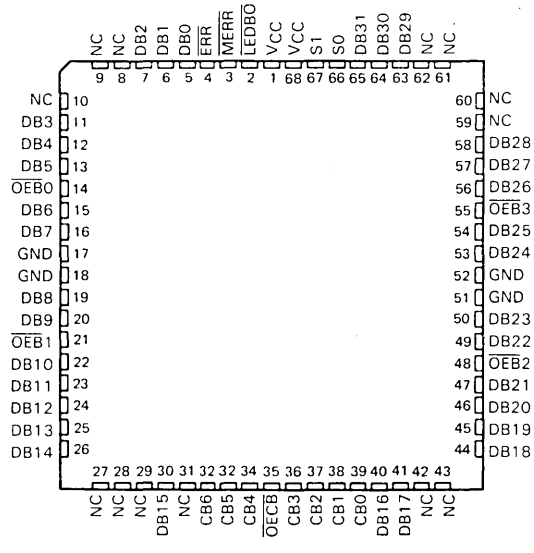
Read-modify-write (byte-control) operations can be performed by using output latch enable, $\overline{\text{LEDBO}}$, and the individual $\overline{\text{OEB0}}$ thru $\overline{\text{OEB3}}$ byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

N OR JD PACKAGE
(TOP VIEW)

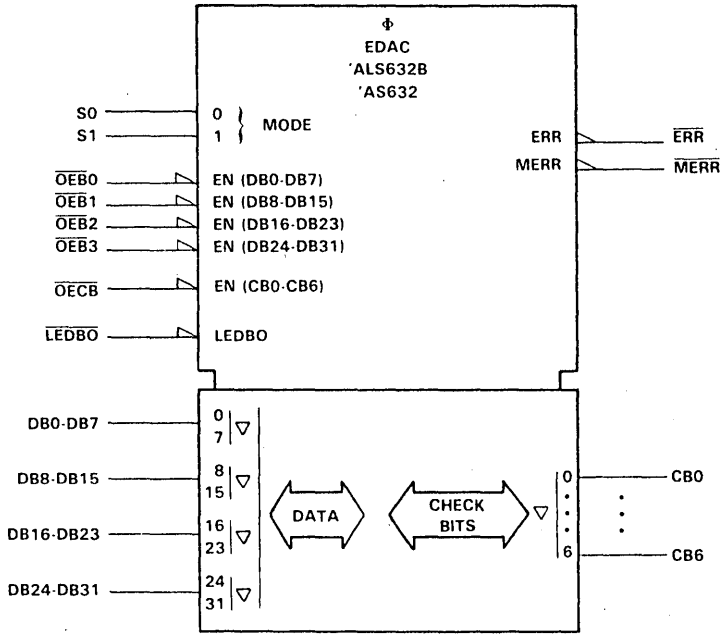


FN PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol†



TERMINAL FUNCTIONS

PIN NAME	DESCRIPTION
CB0-CB6	Check Bit data port. This 7-bit I/O port is used to output check bits during write cycles and input memory check bits during read cycles.
DB0-DB31	Data port. This 32-bit I/O port is used to input processor data during memory write cycles and used to output corrected data during memory read cycles.
$\overline{ERR}$	Single-Bit Error Flag. This active-low output signals when a single-bit error has occurred. When more than two errors occur, this output is unpredictable.
GND	Ground
$\overline{LEDBO}$	Output Latch Enable. This input controls the output data latch that stores the corrected data word. When low, data is allowed to flow through the latch. When taken high, data present at the inputs of the output data latch is stored.
$\overline{MERR}$	Multiple-Bit Error Flag. This active-low output signals when a double-bit error has occurred. When more than two errors occur, this output is unpredictable.
NC	No internal connection
$\overline{OEB0}$-$\overline{OEB31}$	Data Output Enable controls. These active-low inputs are used to enable data onto the data bus (DB0-DB31). Each input controls 8-bits for byte control operations. $\overline{OEB0}$ controls DB0-DB7, $\overline{OEB1}$ controls DB8-DB15, $\overline{OEB2}$ controls DB16-DB23, and $\overline{OEB3}$ controls DB24-DB31.
$\overline{OECB}$	Check Bit Output Enable control. This active-low input is used to enable the check bits onto the check bit bus (CB0-CB6).
S0,S1	Mode Select controls. These control inputs select the mode of the EDAC. See function tables for details.
V_{CC}	Supply voltage

for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

D3397, JANUARY 1990

- **Detects and Corrects Single-Bit Errors**
- **Detects and Flags Dual-Bit Errors**
- **Built-In Diagnostic Capability**
- **Fast Write and Read Cycle Processing Times**
- **Byte-Write Capability**
- **Dependable Texas Instruments Quality and Reliability**

description

The 'AS632A device is a 32-bit parallel error detection and correction circuit (EDAC). This EDAC uses a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDAC to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

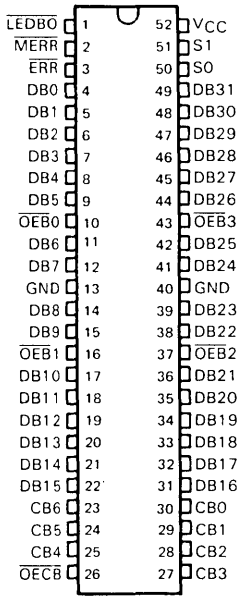
Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit data word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of this device to detect.

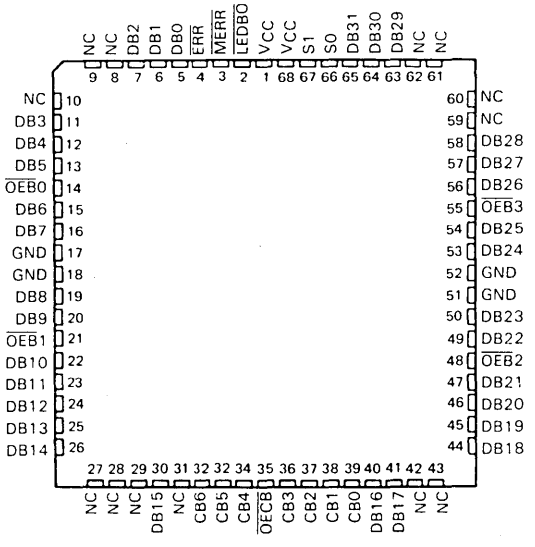
Read-modify-write (byte-control) operations can be performed by using output latch enable, $\overline{\text{LEDBO}}$, and the individual $\overline{\text{OEB0}}$ thru $\overline{\text{OEB3}}$ byte control pins.

Diagnostics are performed on the EDAC by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

N OR JD PACKAGE
(TOP VIEW)

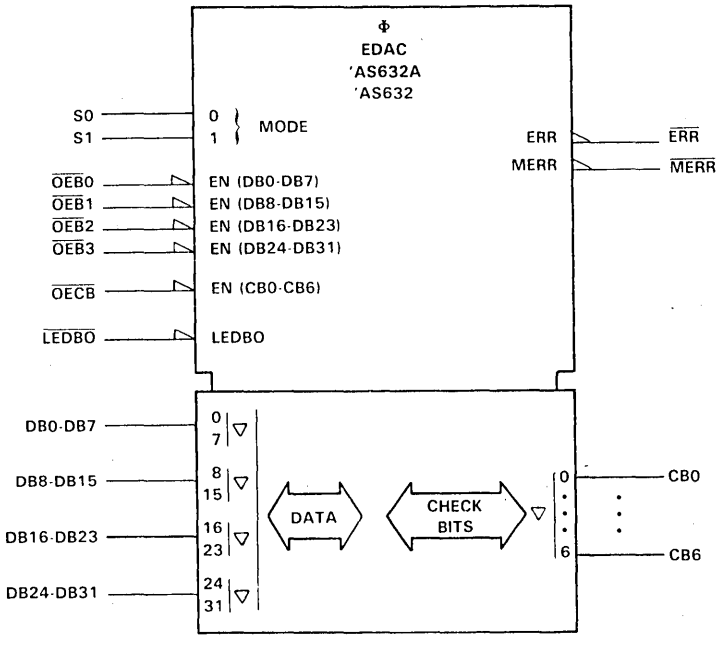


FN PACKAGE
(TOP VIEW)



NC No internal connection

logic symbol†



†This symbol is an accordance with ANSI/IEEE-Std 91-1984.

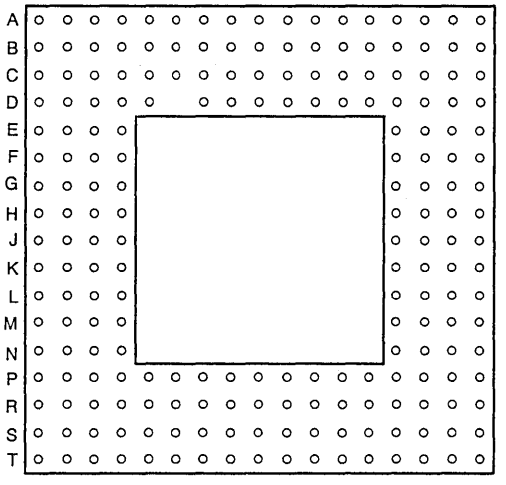
for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

D3312, FEBRUARY 1990–REVISED SEPTEMBER 1990

- 12-ns Max Pass-Thru Operation When Used in Correct-Only-On-Error Configurations
- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- Improved Performance with Flow-Thru Architecture
- Simplified Control Logic Matches Standard TTL/HCMOS '245 Bus Transceiver Logic
- Byte-Write Capability
- Built-In Diagnostic Capability
- Memory Initialization
- Heavy-Duty 48-mA Drive on Processor Data Bus
- Memory Data Bus Features Balanced Output Impedances for Safe Undershoot Characteristics

17 X 17 GA PACKAGE
(TOP VIEW)



description

The SN74AS6364 is a 64-bit Parallel Error Detection and Correction circuit (EDAC) featuring a flow-thru architecture for improved performance and ease of control. Two separate 64-bit I/O ports are provided that allow direct interface to the processor and memory data buses. The processor I/O port is designed for 48-mA drive, matching standard Advanced Schottky bus interface performance. The memory I/O port has been designed for balanced output impedances (25 Ω high and low). This feature optimizes the drive low characteristics, based on safe undershoot.

Interfacing to the 'AS6364 has been greatly simplified due to the flow-thru architecture. Data flow is handled in the same manner as used on conventional TTL/HCMOS 245 bus transceivers via a direction-control pin (DIR) and a master enable/disable pin ($\overline{G}$). In its simplest form, the direction-control pin can be driven from the processor R/$\overline{W}$ pin. When the DIR control pin is taken low (write cycle), processor data is allowed to flow through the EDAC unaltered. The 8-bit check word appears on the check word I/O bus after the specified propagation delay.

Pin locations are shown above. Pin D6 has been omitted for indexing purposes. Pin assignments for the 207 used pins are given on the following page. Pin-function descriptions are given on the page after.

When the direction-control input is taken high for a read cycle, memory data and its associated check word is allowed to flow into the EDAC. The 8-bit check word is then compared against a new check word generated from the 64-bit data word. The resulting syndrome code is decoded by the error detection logic and signals the occurrence of an error. The Single-Bit Error Flag ($\overline{ERR}$) informs the user that a single-bit error has occurred. The Multiple-Bit Error Flag ($\overline{MERR}$) informs the user that a double-bit error has occurred. The $\overline{ERR}$ flag also goes low for double-bit errors. The Correctable Error Flag ($\overline{CERR}$) lets the user know that a correctable, single-bit error has occurred ($\overline{ERR}$ low, $\overline{MERR}$ high). Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all lows or all highs on the data and check words will be flagged ($\overline{ERR}$ = low, $\overline{MERR}$ = low, and $\overline{CERR}$ = high).

PIN ASSIGNMENTS

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
A1	MD21	C2	MD14	E3	MD10	J15	GND	P1	CB6	S2	D10
A2	MD22	C3	MD15	E4	V_{CC}	J16	SYN5	P2	D4	S3	$\overline{OEB}$1
A3	MD24	C4	MD19	E14	MD54	J17	SYN6	P3	D11	S4	D16
A4	MD28	C5	MD23	E15	MD61	K1	CB1	P4	V_{CC}	S5	D17
A5	MD33	C6	GND	E16	$\overline{ERR}$	K2	CB4	P5	GND	S6	D23
A6	MD29	C7	MD27	E17	SYN3	K3	D1	P6	D18	S7	D27
A7	MD34	C8	GND	F1	MD7	K4	V_{CC}	P7	GND	S8	D25
A8	MD36	C9	GND	F2	MD5	K14	GND	P8	V_{CC}	S9	D29
A9	MD38	C10	GND	F3	MD6	K15	D63	P9	V_{CC}	S10	$\overline{OEB}$3
A10	MD41	C11	MD42	F4	GND	K16	D62	P10	GND	S11	$\overline{OEB}$4
A11	MD43	C12	MD46	F14	GND	K17	D61	P11	GND	S12	D36
A12	MD44	C13	MD48	F15	MD62	L1	$\overline{OEB}$0	P12	GND	S13	D39
A13	MD47	C14	MD52	F16	DIR	L2	D2	P13	GND	S14	D40
A14	MD50	C15	MD58	F17	SYN0	L3	GND	P14	GND	S15	D44
A15	MD55	C16	$\overline{CERR}$	G1	MD2	L4	V_{CC}	P15	D50	S16	$\overline{OEB}$5
A16	MD53	C17	LE	G2	MD3	L14	V_{CC}	P16	D51	S17	$\overline{OEB}$6
A17	MD60	D1	MD11	G3	MD4	L15	V_{CC}	P17	D55	T1	D9
B1	MD18	D2	MD12	G4	GND	L16	D60	R1	D0	T2	D12
B2	MD16	D3	MD13	G14	V_{CC}	L17	D59	R2	D7	T3	D14
B3	MD20	D4	GND	G15	$\overline{DIAG}$	M1	CB2	R3	D15	T4	D19
B4	MD25	D5	GND	G16	SYN2	M2	D5	R4	$\overline{OEB}$2	T5	D20
B5	MD26	D6		G17	SYN7	M3	GND	R5	GND	T6	D24
B6	MD31	D7	V_{CC}	H1	MD1	M4	GND	R6	D21	T7	D28
B7	MD30	D8	V_{CC}	H2	MD0	M14	V_{CC}	R7	D22	T8	D31
B8	MD32	D9	MD35	H3	CB0	M15	GND	R8	D26	T9	D33
B9	MD37	D10	V_{CC}	H4	V_{CC}	M16	D57	R9	D30	T10	D34
B10	MD39	D11	V_{CC}	H14	$\overline{INIT}$	M17	D58	R10	D38	T11	D37
B11	MD40	D12	GND	H15	SNY1	N1	CB5	R11	V_{CC}	T12	D32
B12	MD45	D13	GND	H16	SYN4	N2	D6	R12	V_{CC}	T13	D35
B13	MD49	D14	V_{CC}	H17	$\overline{OEB}$7	N3	D8	R13	D43	T14	D41
B14	MD51	D15	MD56	J1	CORR	N4	D13	R14	D47	T15	D42
B15	MD57	D16	$\overline{MERR}$	J2	CB3	N14	GND	R15	D48	T16	D45
B16	MD59	D17	$\overline{G}$	J3	GND	N15	D56	R16	D49	T17	D46
B17	MD63	E1	MD8	J4	CB7	N16	D53	R17	D52		
C1	MD17	E2	MD9	J14	V_{CC}	N17	D54	S1	D3		

for complete data sheet

The complete version of this data sheet and application information can be found in the Cache Memory Management Data Book, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

EXPLANATION OF IEEE/IEC LOGIC SYMBOLS FOR MEMORIES

Introduction

The International Electrotechnical Commission (IEC) has developed a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be partially explained below.

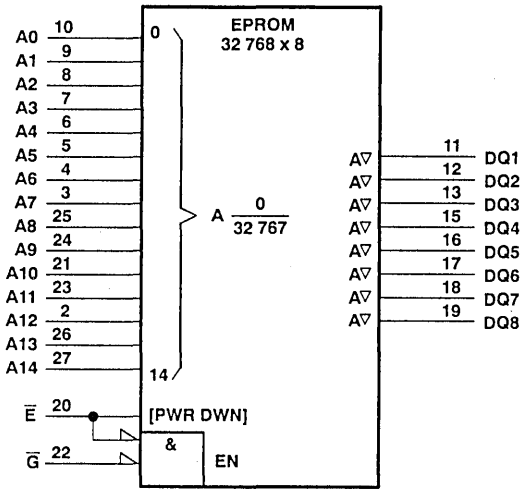
The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

The current standards are IEC Publication 617-12, 1983, and ANSI/IEEE Standard 91-1984. Most of the data sheets in this data book include symbols prepared in accordance with these standards. The explanation that follows is necessarily brief and greatly condensed from the explanation given in the standards. This is not intended to be sufficient for people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this book.

Explanation of a Typical Symbol For a Static Memory

The TMS27C256 symbol will be explained in detail. This symbol includes almost all the features found in the OTP PROMs and EPROMs.

The TMS27C256 Symbol



The address inputs are arranged in order of their assigned binary weights and the range of addresses are shown as A $\frac{m}{n}$ where m is the decimal equivalent of the lowest address and n is the highest. The outputs affected by these addresses are indicated by the letter A, as data inputs would also be if the device were a RAM.

The polarity indicator ◺ indicates that the external low level causes the internal 1-state (the active or asserted state) at an input or that the internal 1-state causes the external low level at an output. The effect is similar to specifying positive logic and using the negation symbol o.

The ▽ symbols indicate three-state outputs. Three-state outputs will always be controlled by an EN function. When EN stands at its internal 1-state, the outputs are enabled; when EN stands at its internal 0-state, the outputs stand at their high-impedance states. Sometimes the EN is a single input, but in the illustrated case, it is the output of a two-input AND gate. Both inputs (pins 20 and 22) are active low, so if either one of them goes high, the outputs will be disabled. The upper one of these two inputs (pin 20) has another function. When nonstandard labels and explanatory labels are used within symbols, they are enclosed within square brackets. Here we find the label "[PWR DWN]". This is intended to indicate that if pin 20 is high, the memory will go to a low-power standby state.

The Basics

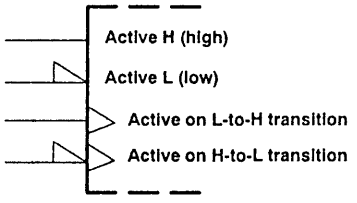
The next section illustrates the most common building blocks that are used in constructing symbols for memories. On the left are shown the symbols that specify the active levels for level-operated inputs, and the direction of active transition for dynamic inputs.

It is preferred to show all input lines on the left and all output lines on the right. When an exception is made to this left-to-right signal flow, an arrowhead is used to show the reverse signal flow. Three symbols are shown that indicate three-state, open-drain, and open-source outputs. If none of these are used, the output should be assumed to be totem-pole. The common control block is a point of replacement for inputs that affect an array of elements.

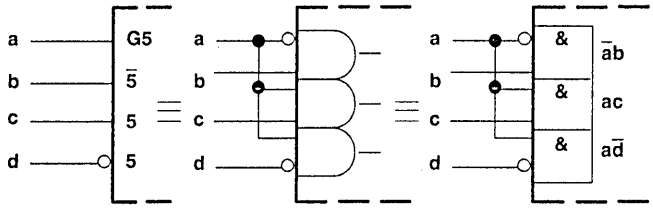
The drawings on the right define the three forms of dependency notation used in this book. At an input (or output) that affects other inputs or outputs, a letter (G, C, or Z) is placed followed by a number. That same number is placed at the affected inputs and outputs. The letter G indicates that an AND relationship exists; if the affecting input stands at the 0-state, it imposes that 0-state on the affected input or output. The letter C indicates a control relationship, usually between clock and a D (data) input. If the C input stands at its 0-state, the affected input is disabled. A D input is always an input to a storage element, which it either sets to the 1-state or resets to the 0-state, unless the D input is disabled to have no effect. Z dependency is used to transfer a signal from one place in a symbol to another, for example from the output at Z4 across to a terminal labeled "4", or from the output at Z5 back to the "5" where it serves as an input with no terminal attached.

Diagrammatic Summary

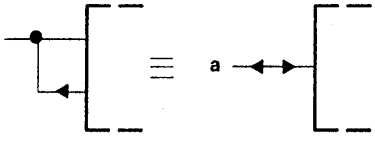
INPUTS



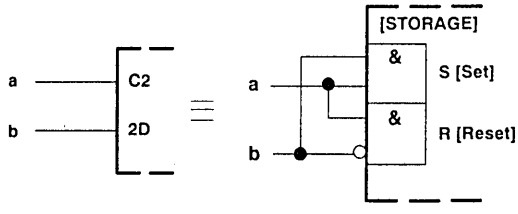
G (AND) DEPENDENCY



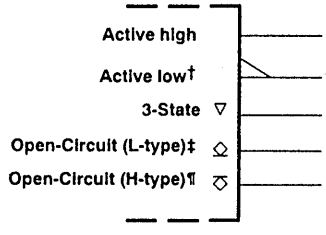
INPUT/OUTPUT



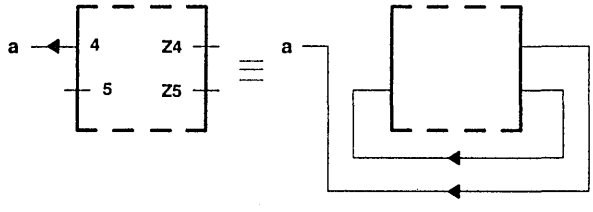
C (CONTROL) DEPENDENCY



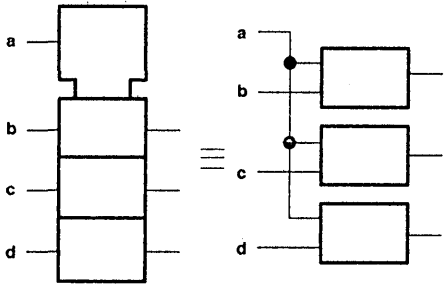
OUTPUTS



Z (INTERCONNECTION) DEPENDENCY



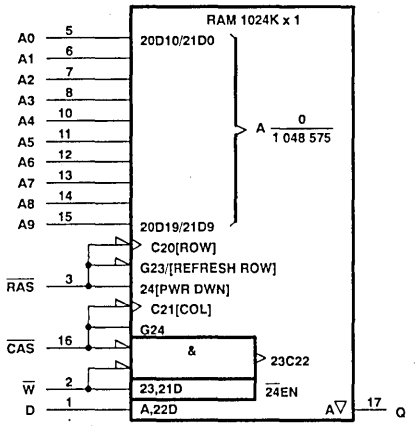
COMMON CONTROL BLOCK



† The active-low indicator may be used in combination with the 3-state and open-circuit indicators.
‡ L-types include N-channel open-drain and P-channel open-source outputs.
¶ H-types include P-channel open-drain and N-channel open-source outputs.

Explanation of a Typical Symbol for a Dynamic Memory

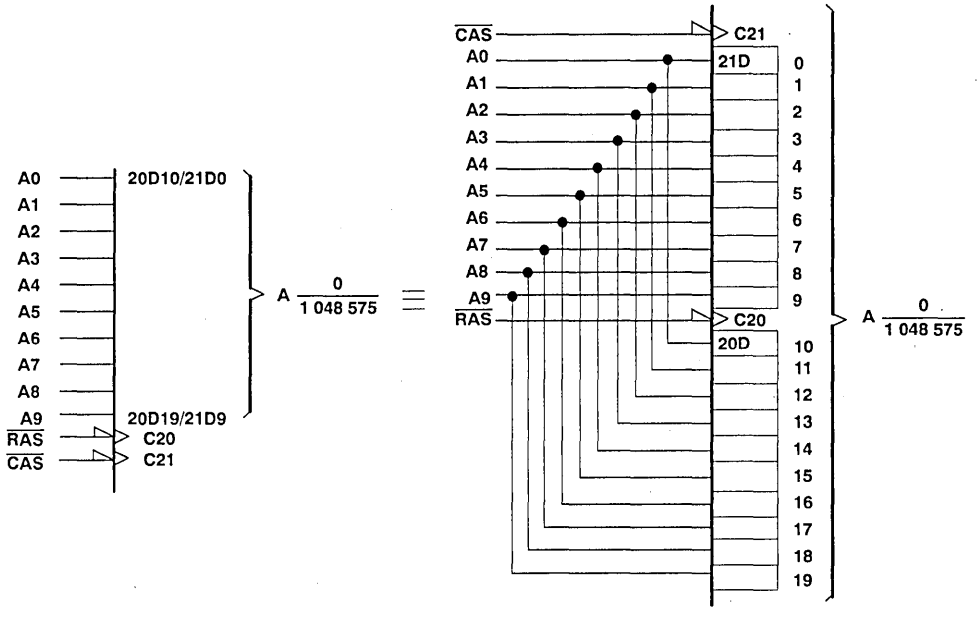
The TMS4C1024 Symbol



The TMS4C1024 symbol will be explained in detail for each operating function. The assumption is made that the previous sections have been read and understood. While this symbol is complex, so is the device it represents and the symbol shows how the part will perform depending on the sequence in which signals are applied.

Addressing

The symbol above makes use of an abbreviated from to show the multiplexed, latched addresses. The blocks representing the address latches are implied but not shown.



When $\overline{RAS}$ goes low, it momentarily enables (through C20, ▷ indicates a dynamic input) the D inputs of the ten address registers 10 through 19. When $\overline{CAS}$ goes low, it momentarily enables (through C21) the D inputs of the ten address registers 0 through 9. The outputs of the address registers are in 20 internal address lines that select 1 of 1 048 576 cells.

TEXAS INSTRUMENTS
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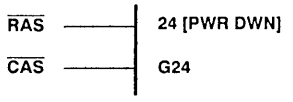
Refresh

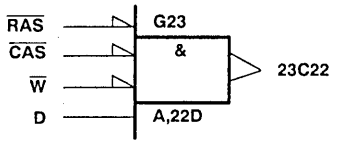
When $\overline{RAS}$ goes low, row refresh starts. It ends when $\overline{RAS}$ goes high. The other input signals required for refreshing are not indicated by the symbol.

Power Down



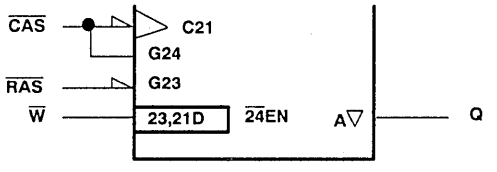
$\overline{CAS}$ is ANDed with $\overline{RAS}$ (through G24) so when $\overline{RAS}$ and $\overline{CAS}$ are both high, the device is powered down.

Write



By virture of the AND relationship between $\overline{CAS}$ and $\overline{W}$ (explicitly shown), when either one of these inputs goes low with the other one and $\overline{RAS}$ is already low ($\overline{RAS}$ is ANDed by G23), the D input is momentarily enabled (through C22). In an "early-write" cycle it is $\overline{W}$ that goes low first; this causes the output to remain off as explained below.

Read



The ANDed result of $\overline{RAS}$ and $\overline{W}$ (produced by G23) is clocked into a latch (through C21) at the instant $\overline{CAS}$ goes low. This result will be "1" if $\overline{RAS}$ is low and $\overline{W}$ is high. The complement of $\overline{CAS}$ is shown to be ANDed with the output of the latch (by G24 and 24). Therefore, as long as $\overline{CAS}$ stays low, the output is enabled. In the "early-write" cycle referred to above, a "0" was stored in the latch by $\overline{W}$ being low when $\overline{CAS}$ went low, so the output remained disabled.

If you have any questions on the Explanation of IEEE/IEC Logic Symbols, please contact:

F.A. Mann, MS 3684
Texas Instruments Incorporated
P.O. Box 655303
Dallas, Texas 75265
Telephone: (214) 997-2489

IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street
New York, New York 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, New York 10018

MOS MEMORY QUALITY AND RELIABILITY STRATEGY

Texas Instruments is committed to providing its customers with reliable, high quality memory products. MOS Memory management has applied a four point quality and reliability strategy to:

- Provide customers with the lowest cost of product ownership through quality, reliability, and service by:
  - On-time delivery to minimize customer inventory.
  - Quality performance that justifies ship-to-stock certification and eliminates the cost of component testing.
  - No system manufacturing fallout.
  - No warranty and service costs.
- Develop partnership relationships to service and solve customer problems and anticipate upcoming needs.
- Live quality improvement process from product creation and manufacturing through product sales via our total quality control approach of:
  - Quality Function Deployment.
  - Design-in and build-in quality and reliability.
  - In-control manufacturing.
  - Leadership customer service.
- Measure TI's performance by the customer's measurement and perception. The performance standard is continuous customer satisfaction.

Total Quality Control (TQC)

Total Quality Control at TI is a business management process encompassing all company functions. The goal of Total Quality Control (TQC) is continuous customer satisfaction. Utilizing a process of improvement through a positive feedback cycle, TQC is deployed in the MOS Memory Division from the initial design-in Q&R stage, in-control manufacturing, and customer service (see Figure 1).

Proper application of the concept of "PLAN-DO-CHECK-ACT" allows a positive feedback loop that creates continuous improvement and breakthrough, as opposed to the "FIX-FIX-FIX-FIX" results of a negative loop (see Figure 2).

Quality Function Deployment

Continuous customer satisfaction can be achieved only by fully understanding customer needs, then introducing innovative products that satisfy those needs. Quality Function Deployment (QFD) accomplishes both purposes at TI. QFD is a technique that systematically records the voice of the customer, identifying product and service attributes most important to the customer. QFD then blends these needs with the talents and innovations of a TI design team to define a manufacturable, reliable product solution for the customer.

Design-In Quality and Reliability

Quality and reliability improvements at TI start with the chip and package design. The objective of MOS Memory's Design-In Quality and Reliability (DIR) thrust is *first-pass qualification of new products, internally and at the customer.* The TI approach to DIR has been to understand customer requirements of a product, and to formalize this knowledge into a database that incorporates both reliability modeling knowledge, and "lessons learned" from historical problems and engineering evaluations. Before any new design is approved, the design is verified against a DIR "checklist". Design verification is planned to evolve to computer verification utilizing artificial intelligence.

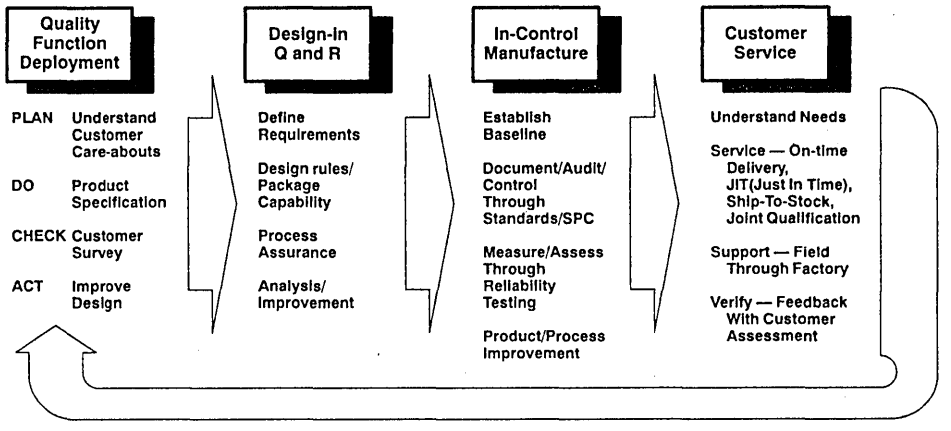


Figure 1. Total Quality Control

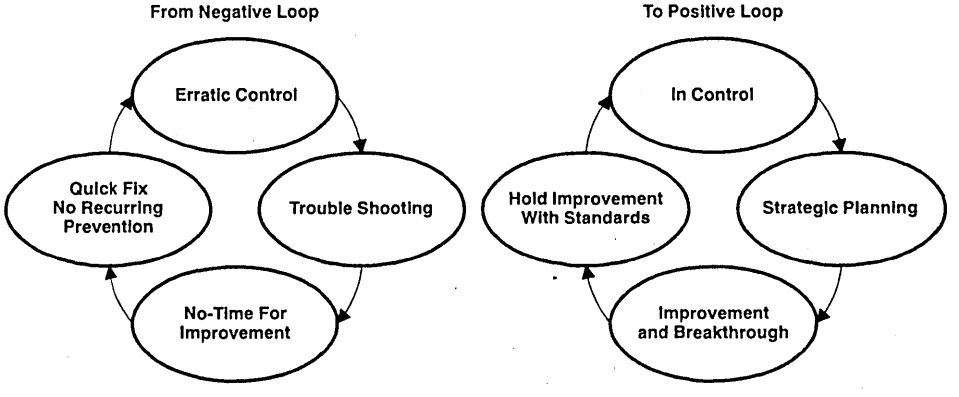


Figure 2. TQC Philosophy

In-Control Manufacturing

Documentation/Audit System

To assure in-control manufacturing, TI employs a hierarchical specification system. General specifications on all aspects of quality, reliability, and customer service are written and controlled by the central Quality and Reliability group. More detailed specifications control the operating practices of design, manufacturing, marketing, and other support organizations. These specifications follow guidelines set by the higher-level specifications, but concentrate on the type of business entity.

Regularly scheduled audits are performed within TI to ensure compliance with all specifications. The five types of audits performed are:

1. Self audit: An internal audit within each functional operation. This type of audit is conducted by persons within the operation and an additional person from outside the operation.
2. Cross-audit: An audit by persons independent of the operation being audited.
3. Group audit: An audit of an operation conducted by the Semiconductor Group audits and procedures function, which is a part of the central Quality and Reliability organization.
4. Procedures audit: An audit of lower-level specifications with respect to higher-level specifications.
5. Compliance audit: An audit of operating practices with respect to specifications.

Statistical Process Control (SPC)

Quality improvement is achieved through Statistical Process Control (SPC). SPC is applied throughout the manufacturing operations of the MOS Memory division. The objectives of SPC are:

– Control processes on a realtime basis.

– Improve process capability (CP).

– Reduce variability to target value (CPK).

– Eliminate "out-of-spec" lots.

– Achieve dependable delivery.

– Lower cost-of-quality.

Computer hardware and artificial intelligence software have been coupled to establish interactive control allowing the computer to generate realtime control charts and prompt adjustments to equipment and processes (see Figure 3).

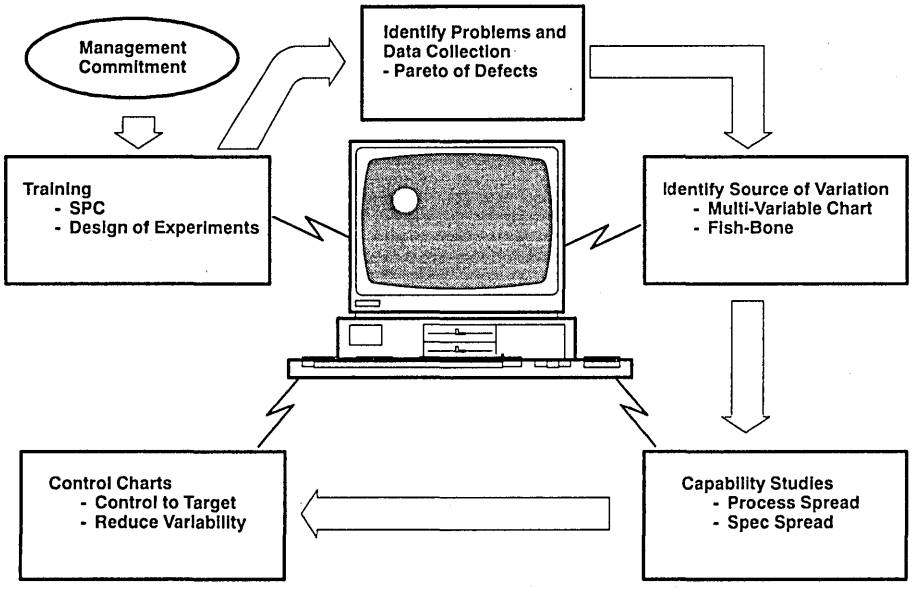


Figure 3. Computer-Aided Statistical Process Control

Die Fabrication Control

In addition to extensive SPC applications in our MOS fabrication centers, TI implements wafer-level quality and reliability controls.

Wafer-level quality control focuses on reduction of variability around target values (CPK) for key functionality parameters and controls the processes that affect these parameters. For example: Column access time (t_{CAC}) is a key DRAM parameter. One of the die manufacturing processes that affects t_{CAC} is the photo etch. To reduce variability of the target value of t_{CAC}, we control polysilicon width dimension at the photo etch process.

Wafer-level reliability controls address process control of known reliability hazards. For example: Excessive phosphorus use in die processing can lead to corrosion defects in the finished device. Wafer-level reliability controls require that phosphorus level control is built into the manufacturing process and that action is prescribed for out-of-control material. Other wafer-level reliability controls are shown in the following table.

Table 1. Wafer Reliability Controls

PARAMETER	CONTROL
Metal	Electromigration Testing, Grain Size, Silicon Nodule Monitor Step Coverage/Metal Necking Monitor Stress-Induced Metal Void Testing
Protective Overcoat	P.O. Integrity Stress Testing Thickness Monitor Refraction
Corrosion	% Phosphorus In Multilevel Oxide Monitor
Gate Oxide Integrity	Breakdown Voltage

Device Assembly Control

TI has also implemented assembly level reliability controls and SPC at critical assembly points (see Table 2) to ensure highly reliable device packaging. Each parameter has certain controls performed at appropriate frequencies to ensure that assembly processing is at qualified levels. Controls may be added or reduced after extensive testing has been performed. Results are carefully studied and fed back to preclude reliability problem introduction into the assembly process. Some of the parameters and controls are shown in Table 3.

Table 2. Major Assembly Steps Using SPC/SQC†

PLASTIC DEVICE ASSEMBLY	
Process	**Control Parameter**
Mount	% Coverage of Epoxy
Bond	Bond Strength
Mold	Temperature and Molding Parameters
Trim/Form	Lead Deflection (DIP)
CERAMIC DEVICE ASSEMBLY	
Bond	Bond Strength
Seal	Seal Furnace Temperature

†Statistical Process Control/Statistical Quality Control

Table 3. MOS Memory Assembly Level Reliability Controls

PARAMETER	CONTROL
P.O. Integrity	Contactless Wafer Mount on Tape Die Mount System Mold Compound Parameters
Chip/Crack	Visual Inspection Temp Cycle Saw Blade Conditions Poker Pin Height Wet Etch Monitor (EPROM)
Bond Integrity	Bond Strength Monitor Bond Parameters Bake/Bond Pull Monitor Capillary Change
Package Integrity	Visual Inspection Mold Press Parameters (Plastic) X-Ray Inspection (Plastic) Trim/Form (Plastic) Package Seal (Ceramic) Temp Cycle (Ceramic) Hermeticity Monitor (Ceramic)
Die Mount Integrity	Die-Shear Monitor Centrifuge Monitor X-Ray Inspect Leadframe Polyimide Pattern Inspect Pick-Up Arm Force
Contamination	Visual Inspection

Product Assessment/Improvement

Reliability Control System

The MOS Memory reliability control system (Figure 4) provides closed-loop-system feedback resulting in corrective actions and ongoing product improvements. Each new product, process, or major change to an existing product is internally qualified to industry leadership standards prior to production. This is followed by intensive monitoring during production ramp-up and routine monitoring of more than 20,000 units a month once a product achieves final production release. In 1989 almost two million memory devices were tested in all phases of the reliability control system.

Reliability Development Issues

Soft Error: TI does extensive work in all phases of device development to minimize the effects of soft errors. Soft errors are caused by alpha particles emitted by the decay of small amounts of thorium and uranium located in device packaging materials. TI maintains an aggresive program of evaluating new mold compounds to ensure low alpha emmissivity. Certain device design and processing techniques are also applied to ensure a low soft error rate. The goal of device design and processing is to maximize the cell capacitance by employing an oxide-nitride dielectric, as opposed to an oxide dielectric. Also, the cell capacitance increases as the dielectric thickness decreases. Testing has shown that the trench capacitor used in dynamic RAMs has competitive soft error rates.

Channel Hot Electron: Channel hot electrons are caused by impact ionization in the drain pinch-off region. Electrons are accelerated toward the drain, collide with positive ions, and can be trapped in the gate oxide. This trapped charge can change the characteristics of the transistor by raising the V_T (threshold voltage). One method employed to reduce the effects of hot electrons is to add a lightly doped drain to reduce the electric field at the gate. Testing for channel hot electrons is performed at a low temperature (–10°C) and a high drain voltage.

Latch-up: A CMOS device can latch-up when the gain of the parasitic PNP+NPN transistors is greater than 1. These PNP+NPN transistors act as a silicon controlled rectifier (SCR). If enough current flows through the resistors, the transistors will turn on and the device will latch-up.

To control latch-up, the SCR gain must be controlled to less than or equal to one. Methods for improving latch-up immunity include incorporating guard rings between P+ and N+ diffusions, and isolating P+ and N+ diffusions.

Latch-up testing is performed to ensure our CMOS devices meet the minimum holding current for industry standards.

Customer Service

Quality, Reliability, Service, and the Cost of Ownership

The goal of Texas Instruments is to offer the best quality, reliability, and service in the semiconductor industry. The foundation for this approach is to ship consistent quality. Consistent quality allows ship-to-stock programs that foster the elimination of the customer's incoming inspection. Ship-to-stock quality, coupled with 100% on-time delivery to narrow shipping windows means support of the customer's just-in-time manufacturing program. This combination of quality, reliability, and service can be measured by a single index called "the cost of ownership". The "cost of ownership" is defined as being composed of the purchase price, quality adders (for incoming inspection and board rework), inventory adders (for maintenance of a buffer inventory for suppliers who cannot meet just-in-time delivery), in-house reliability adders (for system burn-in and rework), and field reliability adders (for warranty and post-warranty field repairs).

For more information about the cost of ownership concept, contact your local TI sales office and request the brochure "Texas Instruments Lowers Semiconductor Cost of Ownership", SSYB057.

Quality Improvement

Significant improvement in product quality has been achieved through:

– Better definition of customer's requirements.

– Greater emphasis on quality as a design criterion.

– Improved control of incoming materials.

– Intensive training of supervisors and operators.

– Extensive use of statistical process control.

– More automation of operations to minimize operator-related defects.

QUALIFICATION

- Baseline process
- 3 – 6 diffusion lots
- Up to 7000 units tested

TEST	# OF UNITS DRAM	EPROM	OTP
125°C Op life	1100	300	200
EFR†	2000	1000	500
85/85	300	–	200
Temp. cycle	600	150	600
Press. cooker test	300	–	200
PSP/PVP‡	100	–	200
Static bias/storage	250	300	150
Soft error	2000	–	–
Data ret. bake	–	600	150
Electromigration	150	–	150
Package integrity	470	400	200
ESD	30	20	20

PRODUCTION RAMP LOT ACCEPT

- Baseline process
- 100% reliability lot acceptance concurrent with qualifications
- Review of data once sufficient lots have been sampled

TEST	# OF LOTS DRAM	EPROM	OTP
EFR†	150	100	100
High temp. rev. bias	–	50	50
Temp. cycle	50	50	50
Press. cooker test	50	–	50
Bake	–	50	50

FINAL PRODUCTION RELEASE

- Control each package/wafer fabrication site/device combination
- Ongoing reliability monitor of 125°C op life, data retention bake, temperature cycle, 85/85, autoclave, package integrity, and internal cavity moisture
- Control limits for each test
- Approximately 20,000 units tested each month
- Early failure rate monitor

† EFR (Early Failure Rate): DRAM – 125°C OPL, 80 hours
EPROM & OTP – 200°C bake, 44 hours (OTP in ceramic package)

‡ PSP: Pressure cooker, Sauter dip, Pressure cooker
PVP: Pressure cooker, Vapor phase, Pressure cooker

Figure 4. Reliability Control System

As is demonstrated in Figure 5, MOS Memory EPROM and DRAM outgoing quality has dramatically improved during the last few years. This significant improvement has occurred for all TI product lines and has been recognized publicly by many of our customers, who have given TI more than 70 major quality awards in the last three years. Included among these awards are Ford's Q-1 Award, the U.S. Naval Quality Award, and the Deming Prize, which is Japan's most prestigious quality award.

Reliability Improvement

Low IC failure rates are achieved through design-in reliability, computer aided design, stringent qualification testing prior to product release, routine monitoring of released products, and an extensive failure mode tracking and feedback system for IC failures.

Since the early '80's, MOS Memory products have exhibited a device failure rate improvement trend, which has resulted in highly reliable memory devices (see Figure 6). Even though the memory device complexity increases in an ongoing manner, TI's failure rate by function has improved at an even faster pace. TI continues to emphasize reliability improvement as a major factor in reducing the total cost of ownership for our customers. Reliability improvement is reflected as a reduction in the expected field failures during system lifetime.

Up-to-date quality and reliability data for MOS Memory products is available. Please contact your local TI sales office for information.

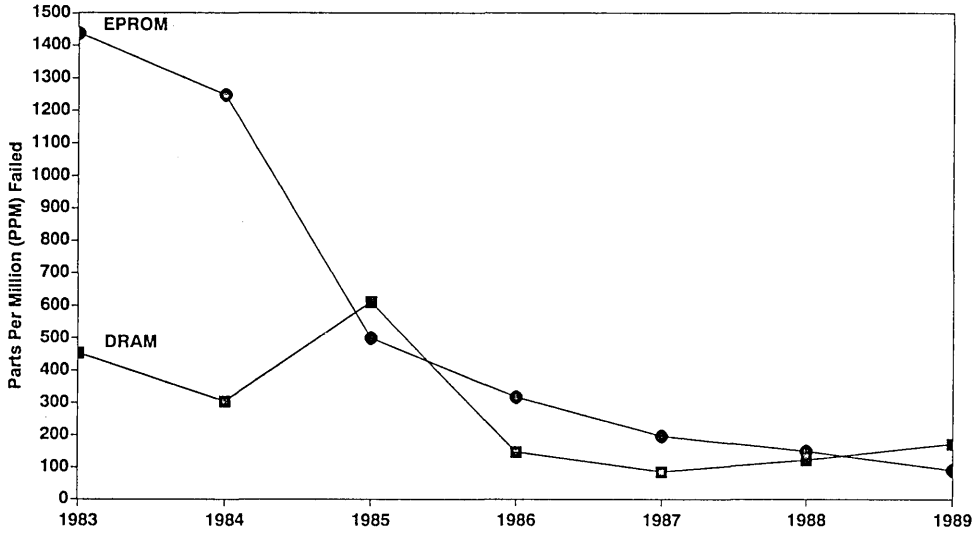


Figure 5. MOS Memory Quality Improvement

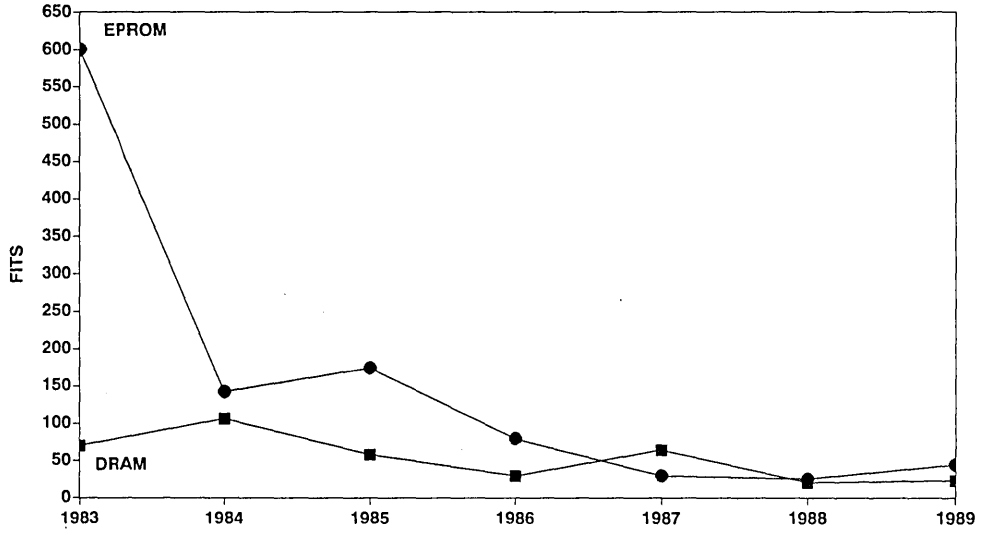


Figure 6. MOS Memory Reliability Improvement

Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies

Scope

This specification establishes the requirements for methods and materials used to protect electronic parts, devices, and assemblies (items) that are susceptible to damage or degradation from electrostatic discharge (ESD). The electrostatic charges referred to in this specification are generated and stored on surfaces of ordinary plastics, most common textile garments, ungrounded person's bodies, and many other commonly unnoticed static generators. The passage of these charges through an electrostatic-sensitive part may result in catastrophic failure or performance degradation of the part.

The part types for which these requirements are applicable include, but are not limited to, those listed:

1. All metal-oxide semiconductor (MOS) devices; e.g., CMOS, PMOS, etc.
2. Junction field-effect transistors (JFET)
3. Bipolar digital and linear circuits
4. Op-amps, monolithic microcircuits with MOS compensating networks, on-board MOS capacitors, or other MOS elements
5. Hybrid microcircuits and assemblies containing any of the types of devices listed
6. Printed circuit boards and other types of assembly containing static-sensitive devices
7. Thin-film passive devices

Definitions

1. Electrostatic Discharge (ESD): A transfer of electrostatic charges between bodies at different electrostatic potentials caused by direct contact or electrostatic field induction.
2. Conductive material: Material having a surface resistivity of 10^5 Ω/square maximum.
3. Static dissipative material: Material having a surface resistivity between 10^5 and 10^9 Ω/square.
4. Antistatic material: Material having a surface resistivity between 10^9 and 10^{14} Ω/square
5. Surface resistivity: An inverse measure of the conductivity of a material and is the resistance of unit length and unit width of a surface. Note: Surface resistivity of a material is numerically equal to the surface resistance between two electrodes forming opposite sides of a square. The size of the square is immaterial. Surface resistivity applies to both surface and volume conductive materials and has the dimension of Ω/square.
6. Volume resistivity: Also referred to as bulk resistivity. It is normally determined by measuring the resistance (R) of a square of material (surface resistivity) and multiplying this value by the thickness (T).
7. Ionizer: A blower that generates positive and negative ions, either by electrostatic means or from a radioactive energy source in an airstream, and distributes a layer of low velocity ionized air over a work area to neutralize static charges.
8. Close proximity: For the purpose of this specification, 6 inches or less.

Device Sensitivity per Test Circuit of Method 3015, MIL-STD-883C

1. Devices are categorized according to their susceptibility to damage resulting from electrostatic discharges (ESD).

Category	ESD Sensitivity
Class 1	0 V – 1999 V
Class 2	2000 V – 3999 V
Class 3	4000 V and above

2. Devices are to be protected from ESD damage from receipt at incoming inspection through assembly, test, and shipment of completed equipment.

Applicable Reference Documents

The following reference documents (of latest issue) can provide additional information on ESD controls.

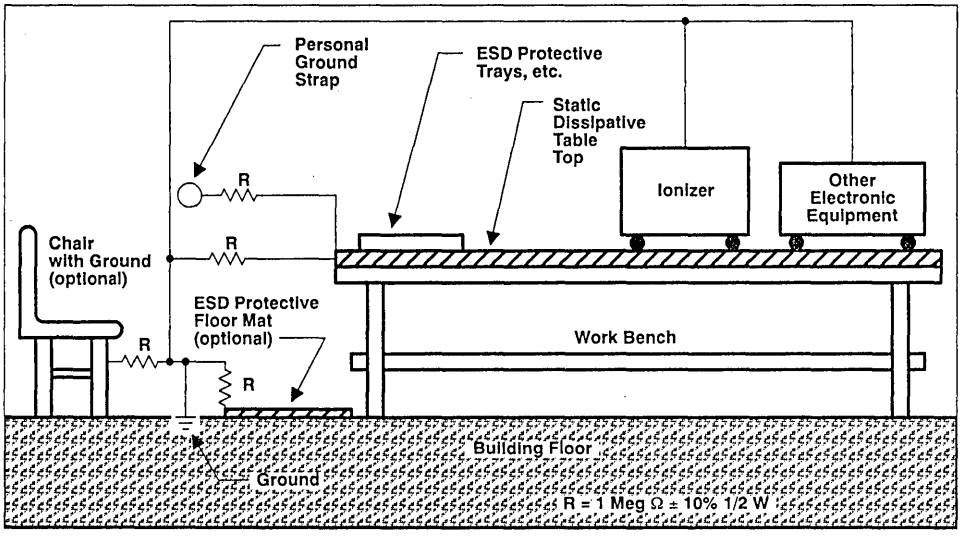
1. MIL-M-38510 Microcircuits, General Specification
2. MIL-STD-883 Test Methods and Procedures for Microelectronics
3. MIL-STD-19491 Semiconductor Devices, Packaging of
4. MIL-M-55565 Microcircuits, Packaging of
5. DOD-HDBK-263 Electrostatic Discharge Control Handbook for Protection
6. DOD-STD-1686 Electrostatic Discharge Control Program
7. NAVSEA SE 003-11-TRN-010 Electrostatic Discharge Training Manual
8. JEDEC Standard Publication 108

Facilities for Static-Free Workstation

The minimum acceptable static-free workstation shall consist of the work surface covered with static dissipative material attached to ground through a 1 MΩ ± 10% resistor, an attached grounding wrist strap with integral 1 MΩ ± 10% resistor for each operator, and air ionizer(s) of sufficient capacity for each operator. The wrist strap shall be connected to the static dissipative material. Ground shall utilize the standard building earth ground; refer to Figure 1. Conductive floor tile/carpet along with conductive shoes may be used in lieu of the conductive wrist straps for non-seated personnel. The Site Safety Engineer must review and approve all electrical connections at the static-free workstation prior to its implementation.

Air ionizers shall be positioned so that the devices at the static-free workstations are within a 4-foot arc measured by a vertical line from the face of the ionizer and 45 degrees on each side of this line.

General grounding requirements are to be in accordance with Table 1.



All electrical equipment sitting on the conductive table top must be hard grounded but must be isolated from the static disspative work surface.

NOTE: Earth ground is not computer ground or RF ground or any other limited-type ground.

Figure 1. Static-Free Workstation

Table 1. General Grounding Requirements

	Treated With Antistatic Solution or Made of Conductive Material	Grounded to Common Point	Static Dissipative Material
Handling Equipment/ Handtools	X		X
Metal Parts of Fixtures and Tools/Storage Racks		X	
Handling Trays/Tubes	X		X
Soldering Irons/Baths		X	
Table Tops/Floor Mats	X	X	X
Personnel		X Using Wrist Strap*	

* With 1 MΩ ± 10% resistor

Usage of Antistatic Solution in Areas to Control the Generation of Static Charges

The use of antistatic chemicals (antistats) should be a supplemental part of an overall organized ESD program. Any antistatic chemical application shall be considered as a means to reduce or eliminate static charge generation on nonconductive materials in the manufacturing or storage areas.

The application of any antistatic chemical in a clean room of class 10 000 or less shall not be permitted. Accordingly, any user of antistatic solutions must consider the following precautions:

1. Do not apply antistatic spray or solutions in any form to energized electrical parts, assemblies, panels, or equipment.
2. Do not perform antistatic chemical applications in any area when bare chips, raw parts, packages, and/or personnel are exposed to spray mists and evaporation vapors.

The need for initial application and frequency of reapplication can be established only through routing electrostatic voltage measurements using an electrostatic voltmeter. The following durability schedule is a reasonable expectation.

1. Soft surfaces (carpet, fabric seats, foam padding, etc.): each 6 months or after cleaning, by spraying.
2. Hard abused surfaces (floor, table tops, tools, etc.): each week (or day for heavy use) and after cleaning, by wiping or mopping.
3. Hard unabused surfaces (cabinets, walls, fixtures, etc.): each 6 months or annually and after cleaning, by wiping or spraying.
4. Company-furnished and maintained clothing and smocks: after each cleaning, by spraying or adding antistatic concentrate to final rinse water when cleaned.

The use of antistatic chemicals, their application, and compliance with all appropriate specifications, precautions, and requirements shall be the responsibility of the area supervisor where antistatic chemicals are used.

ESD Labels and Signs in Work Areas

ESD caution signs at workstations and labels on static-sensitive parts and containers shall be consistent in color, symbols class, voltage sensitivity identification, and appropriate instructions. Signs shall be posted at all workstations performing any handling operations with static-sensitive items. These signs shall contain the following information or its equivalent.

CAUTION

STATIC CAN DAMAGE COMPONENTS

Do not handle ESD-sensitive items unless grounding wrist strap is properly worn and grounded. Do not let clothing or plain plastic materials contact or come in close proximity to ESD-sensitive items.

Labels shall be affixed to all containers containing static-sensitive items at a place readily visible and proper for the intended purpose. Additionally, labels must be consistently placed on containers and packages at a standard location to eliminate mishandling. Use only QC-accepted and approved signs and labels to identify static-sensitive products and work areas. The use of ESD signs and labels, and their information content shall be the responsibility of the area supervisor to assure consistency and compatibility throughout the static-sensitive routing.

Relative Humidity Control

Since relative humidity has a significant impact on the generation of static electricity, when possible, the work area should be maintained within the 40%–60% relative humidity range.

Preparation for Working at Static-Free Workstation

A workstation with a static disspative work surface connected to ground through a 1 MΩ ± 10% resistor, a grounding wrist strap with the ground wire connected to the conductive work surface, and an ionizer constitute a static-free workstation (Figure 1). An operator is properly grounded when the wrist strap is in snug (no slack) contact with the bare skin, usually positioned on the left wrist for a right-handed operator. The wrist strap must be worn the entire time an operator is at a static-free workstation. The operator should first touch the grounded bench top before handling static-sensitive items. This precaution should be observed in addition to wearing the gounding wrist strap. If possible, the operator should avoid touching leads or contacts even though he or she is grounded.

CAUTION

Personnel shall never be attached without the presence of the 1 MΩ ± 10% series resistor in the ground wire.

An operator's clothing should never make contact or come in close proximity with static sensitive items. Operators must be especially careful to prevent any static-sensitive items (being handled) from touching their clothing. Long sleeves must be rolled up or covered with antistatic sleeve protector banded to the bare wrist, which shall "cage" the sleeve at least as far up as the elbow. Only antistatic finger cots may be used when handling static-sensitive items.

Any improperly prepared person, while at or near the work station, shall not touch or come in close proximity with any static-sensitive item. It is the responsibility of the operator and the area supervisor to ensure that the static-free work area is clear of unnecessary static hazards, including such personal items as plastic coated cups or wrappers, plastic cosmetic bottles or boxes, combs, tissue boxes, cigarette packages, and vinyl or plastic purses. All work-related items, including information sheets, fluid containers, tools, and part carriers must be approved for use at the static-free workstation.

General Handling Procedures and Requirements

1. All static-sensitive items must be received in an antistatic/conductive container and must not be removed from the container except at the static-free workstation. All protective folders or envelopes holding documentation (lot travelers, etc.) shall be made of nonstatic-generating material.

2. Each packing (outermost) container and package (internal or intermediate) shall have a bright yellow warning label attached, stating the following information or equivalent:

The warning label shall be legible and easily readable to normal vision at a distance of 3 feet.

3. Static-sensitive items are to remain in their protective containers except when actually in use at the static-free station.
4. Before removing the items from their protective container, the operator should place the container on the conductive grounded bench top and make sure the wrist strap fits snugly around the wrist and is properly plugged into the ground receptacle, then touch hands to the conductive bench top.
5. All operations on the items should be performed with the items in contact with the grounded bench top as much as possible. Do not allow conductive magazine to touch hard-grounded test gear on bench top.
6. Ordinary plastic solder-suckers and other plastic assembly aids shall not be used.
7. In cases where it is impossible or impractical to ground the operator with a wrist strap, a conductive shoe strap may be used along with conductive tile/mats.
8. When the operator moves from any other place to the static-free station, the start-up procedure shall be the same as in Preparation for Working at Static-Free Workstation.
9. The ionizer shall be in operation prior to presenting any static-sensitive items to the static-free station, and shall be in operation during the entire time period the items are at the station.
10. "Plastic snow" polystyrene foam, "peanuts," or other high-dielectric materials shall never come in contact with or be used around electrostatic sensitive items, unless they have been treated with an antistat (as evidenced by pink color and generation of less than ± 100 volts).
11. Static-sensitive items shall not be transported or stored in trays, tote boxes, vials, or similar containers made of untreated plastic material unless items are protectively packaged in conductive material.

Packaging Requirements

Packaging of static-sensitive items is to be in accordance with Device Sensitivity, item 1. The use of tape and plain plastic bags is prohibited. All outer and inner containers are to be marked as outlined in General Handling Procedures and Requirements, item 2. Conductive magazines/boxes may be used in lieu of conductive bags.

Specific Handling Procedures for Static-Sensitive Items

Stockroom Operations

1. Containers of static-sensitive items are not to be accepted into stock unless adequately identified as containing static-sensitive items.
2. Items may be removed from the protective container (magazine/bag, etc.) for the purpose of subdividing for order issue only by a properly grounded operator at an approved static-free station as defined in Facilities for and Preparation for Working at Static-Free Workstation.
3. All subdivided lots must be carefully repackaged in protective containers (magazine/bag, etc.) prior to removal from the static-free work-station and labeled to indicate that the package(s) contain static-sensitive items. If it is suspected that a static-sensitive item is not adequately protected, do not transfer it to

another container, return it to the originator for disposition unless the originator is a customer. In that case, the QC engineer should contact the customer and negotiate an appropriate disposition.

4. It is the responsibility of the stockroom supervisor to ensure that all personnel assigned to this operation are familiar with handling procedures as outlined in this specification. A copy of this specification is to be posted in the vicinity so that it is accessible to the operators. Stock handlers and all others who might have occasion to move stock are to be instructed to avoid direct contact with unprotected static-sensitive items.

Module and Subassembly Operations

1. Static-sensitive items are not to be received from a stockroom, kitting, or machine insertion area unless received in approved static-protective packaging, and properly labeled to indicate that its contents are static-sensitive.
2. All single station, progressive line manual assembly operators, and visual inspectors prior to wave soldering operations are to be properly grounded with a grounding wrist strap when handling static-sensitive items.
3. Progressive lines used as single stations where operators will be working on a mix of boards, both static-sensitive and nonstatic-sensitive, will require that all operators working on the line be properly grounded. This is necessary to accommodate the sliding of static-sensitive boards along the assembly bench or across positions not engaged in the assembly of this type board.
4. It is the responsibility of the area supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in the proper working order and to ensure that operators are wearing grounding wrist straps properly (snugly in contact with bare skin).

Soldering and Lead-Forming Operations

1. All soldering machines, conveyors, cleaning machines, and equipment shall be electrically grounded to ensure that they are at the same ground potential as the grounded operators working on their stations. No machine surfaces exposed to static-sensitive items are to be above ground potential.
2. All processing equipment shall be grounded, including all loading and unloading stations, that is, the stations before and after each piece of processing equipment.
3. All nonmetallic, static-generating components in the handling systems shall be treated to ensure protection from static.
4. All stations shall be identified by posting signs as outlined in ESD Labels and Signs in Work Areas.
5. Operators are to be properly grounded with a grounding wrist strap during any handling, loading, unloading, inspection, rework, or proximity to static-sensitive items.
6. Unloading operators working at a grounded station shall place static-sensitive items into approved static-protective bags or containers.
7. All manual soldering, repair, and touch-up work stations on the solder line are to be static protected. Operators are to wear grounding wrist straps when working on static-senstive items. Only grounded-tip soldering/desoldering irons are allowed when working on static-sensitive items.
8. It is the responsibility of the area supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that the operators are wearing grounding wrist straps properly (comfortably snug in contact with bare skin).

Electrical Testing Operations

1. All electrical test stations shall be static protected. Operators shall be properly grounded when working on these items.
2. Reused antistatic magazines must be monitored for maintenance of antistatic characteristics.

3. Devices should be in an antistatic/conductive environment except at the moment when actually under test.
4. Devices should not be inserted into or removed from circuits or tester with the power on or with signals applied to inputs to prevent transient voltages from causing permanent damage.
5. All unused input leads should be biased if possible.
6. Device or module repairs must be performed at static-free stations with the operator attached to a grounding wrist strap. Grounded-tip soldering irons shall be used when working on static-sensitive items.
7. Static-sensitive items shall be handled through all electrical inspections in static protective containers. Removal of the items from the protective containers shall be done at a static-free workstation as discussed in Preparation for Working at a Static-Free Workstation. The units must be returned to the containers before leaving the station.
8. All such items shall be shipped with an ESD warning label affixed as listed.
9. It is the responsibility of the area supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

Packing Operations

1. Static-sensitive items are not to be accepted into the packing area unless they are contained in a static-protected bag or conductive container.
2. A static-sensitive item delivered to the packer within an approved container or bag and found to be in order regarding identification shall be packed in the standard shipping carton or other regular packaging material. Containers are to be labeled in accordance with General Handling Procedures and Requirements, item 2.
3. Any void-fillers shall be made of an approved antistatic material.

Burn-In operations

1. Burn-in board loading and unloading of static-sensitive items shall be done at a static-free station.
2. Shorting clips/shorted connectors shall be installed on the board plug-in tab prior to loading any units into the board sockets. The clip/connectors shall be taken off just prior to plugging the board into the oven connector. The clip/connector shall be installed immediately upon removal of the board from the oven connector. Installation and removal of the clip/connector shall be done by a properly grounded operator.
3. All automatic or semi-automatic loading and unloading equipment shall be properly electrically grounded.
4. It is the responsibility of the area supervisor to ensure that all personnel handling static-senstive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

Customer-Returned-Item Handling Procedure

Receipt of ESD sensitive-labeled items is to be done at a static-free workstation and handled in accordance with applicable sections within this guideline.

Quality Control Provision

Sampling

Each manufacturing, stockroom, and testing operation handling ESD sensitive devices will be audited a minimum of once each quarter for compliance with all terms of this specification by the responsible process control or QRA organization. Ground continuity and the presence of uncontrolled static voltages are considered critical and shall be checked more frequently as specified below.

Ground Continuity (minimum of once a week)

Ground connections (grounding wrist strap, ground wires on cords, etc.) shall be checked for electrical continuity. The presence of a 1 MΩ ± 10% resistor in the ground connections between both the operator wrist straps to the work surface and the work surface to ground connector must be verified.

Grounded Conditions (minimum of once a week)

A visual inspection shall be made to determine full compliance with this specification at static-free workstations during handling of static-sensitive items, including operator being grounded as required, static-sensitive items not being handled in unprotected or unauthorized areas, and no static-generating materials at the grounded workstation.

Sleeve Protectors (minimum of once a week)

A visual check shall be made to determine that each operator wearing loose-fitting or long-sleeved clothing either has sleeves properly rolled or covered with sleeve protectors properly grounded to the bare skin at the wrist.

Static Voltage Levels (minimum of once a week)

In addition to the visual inspections, a sample inspection using an electrostatic voltmeter will be used to check for uncontrolled electstatic voltages at or near electrostatic-controlled work stations.

Conductive Floor Tiles (minimum of once a month)

Conductive floors must have a resistance of not less than 100 kΩ from any point on the tile to earth ground. Also, resistance from any point-to-point on the tile floor three (3) feet apart shall be not less than100 kΩ. The test methods to be used are ASTM-F-150-72 and NFPA 99.

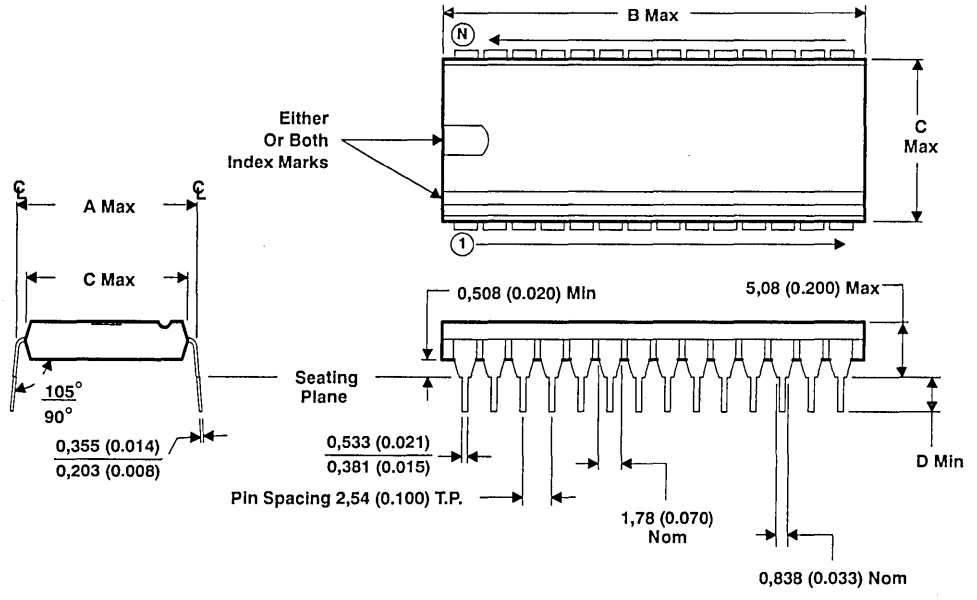
Records

Written records must be kept of all these QC audits.

Training

Training is applicable for all areas where individuals come in contact with ESD-sensitive devices. It is the responsibility of each area supervisor to make sure that his/her people receive ESD training initially and every 12 months thereafter to maintain proficiency. Training should include static fundamentals, a review of applicable parts of this specification, and actual applications in the work area.

Plastic Dual-In-Line Package (N Suffix)†



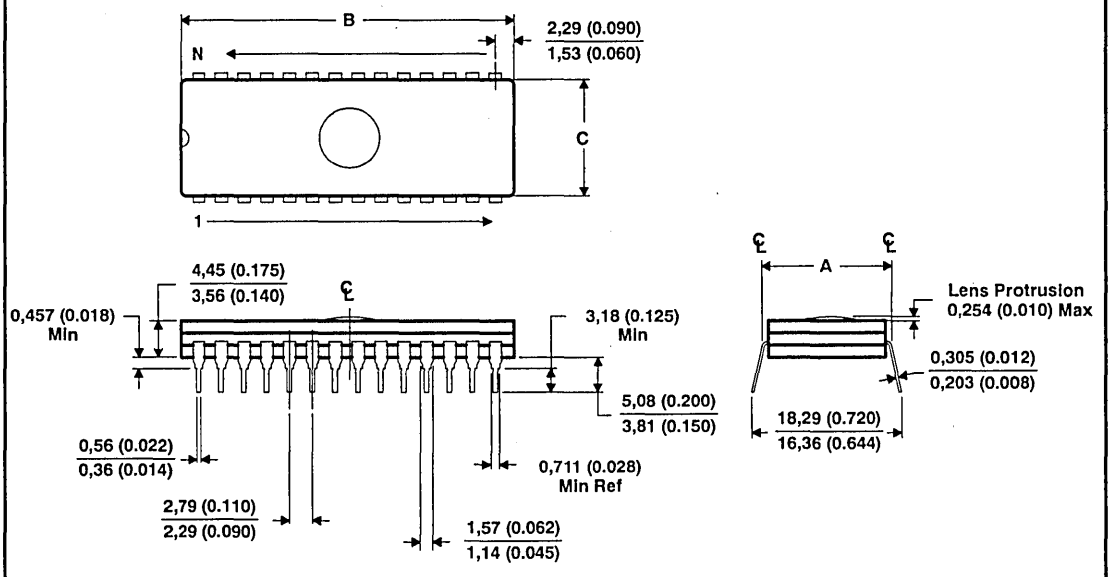
DIM \ PIN	16	18	20	28	32
A (Max)	8,26 (0.325)	8,26 (0.325)	8,26 (0.325)	15,88 (0.625)	15,88 (0.625)
B (Max)	22,10 (0.870)	22,86 (0.899)	25,40 (1.000)	37,21 (1.465)	41,94 (1.651)
C (Max)	6,86 (0.270)	6,86 (0.270)	6,86 (0.270)	13,97 (0.550)	13,97 (0.550)
D (Min)	3,18 (0.125)	3,00 (0.118)	3,00 (0.118)	2,92 (0.115)	3,18 (0.125)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

16-PIN	18-PIN	20-PIN	28-PIN	32-PIN
TMS4C1050	TMS4C1024	TMS44C256	TMS27PC128	TMS27PC510
TMS4C1060	TMS4C1025		TMS27PC256	TMS29F512
	TMS4C1027		TMS27PC512	TMS29F010
	TMS4C1070		TMS29F256	
			TMS29F258	
			TMS29F259	

Ceramic Dual-In-Line Package (J Suffix)†



DIM \ PIN	24	28	32	40
A (Max)	15,85 (0.624)	15,85 (0.624)	15,85 (0.624)	15,85 (0.624)
B (Max)	32,13 (1.265)	37,21 (1.465)	42,37 (1.668)	52,53 (2.068)
C (Max)	14,25 (0.561)	14,25 (0.561)‡ 15,19 (0.598)§	14,25 (0.561)	14,25 (0.561)

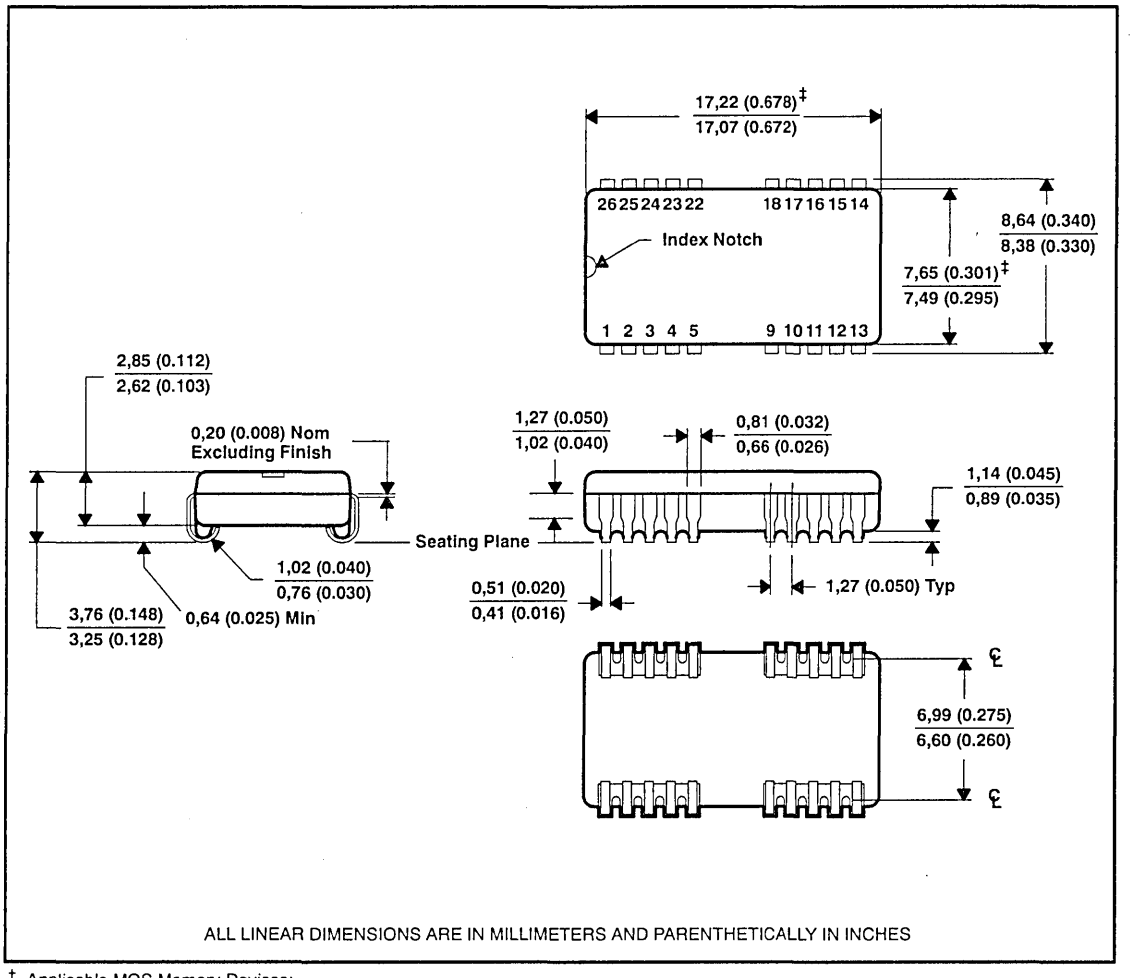
‡ This dimension pertains to TMS27C128, TMS27C256, TMS27C512, and TMS87C257 only.
§ This dimension pertains to TMS29F256, TMS29F258, and TMS29F259 only.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

28-PIN	32-PIN	40-PIN
TMS27C128	TMS27C510	TMS27C210A
TMS27C256	TMS27C010A	TMS27C240
TMS27C512	TMS27C0210A	
TMS29F256	TMS27C040	
TMS29F258	TMS29F512	
TMS29F259	TMS29F010	
TMS87C257		

20/26-Pin Plastic Small-Outline J-Lead Package (SOJ) (DJ suffix)†



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

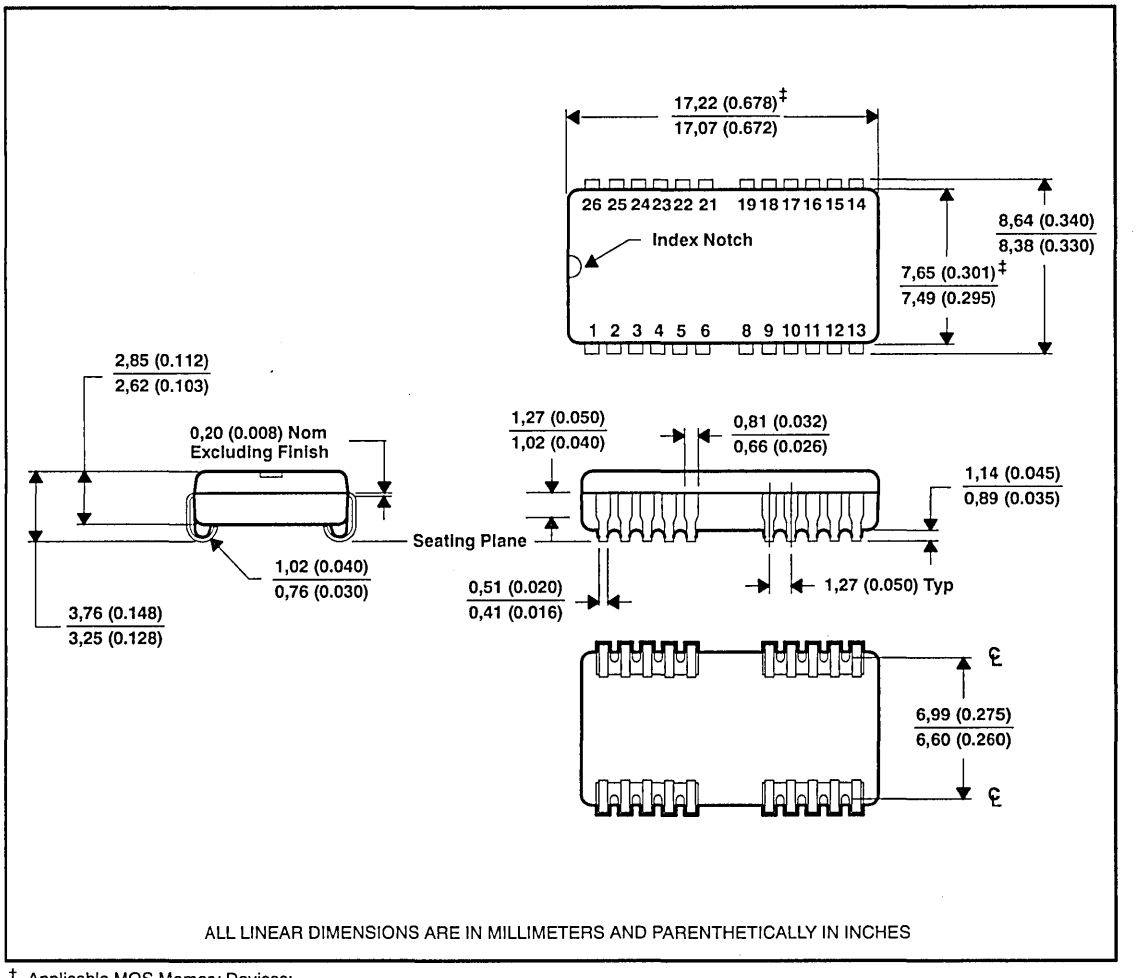
† Applicable MOS Memory Devices:

20/26-PIN§	
TMS4C1024	TMS44400
TMS4C1025	TMS44410
TMS4C1027	TMS4C1050
TMS44C256	TMS4C1060
TMS44100	TMS4C1070
TMS44101	

‡ Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0,254 mm (0.010) from the edge of the package bottom plastic.

§ The lead contact points are planar within 0,101 (0.004).

24/26-Pin Plastic Small-Outline J-Lead Package (SOJ) (DJ suffix)†



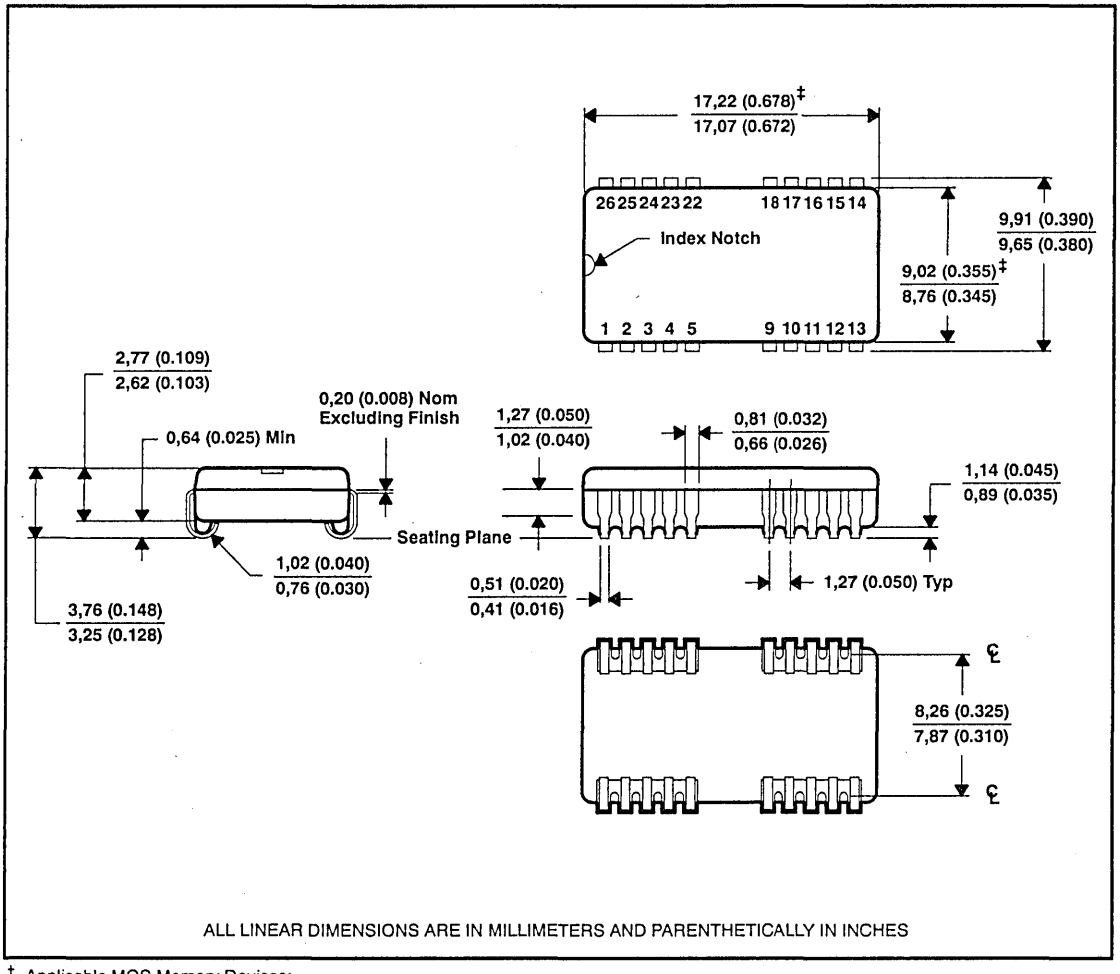
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

24/26-PIN
TMS44C260
TMS44460
TMS48C128
TMS48C138

‡ Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0,254 mm (0.010) from the edge of the package bottom plastic.

20/26-Pin Plastic Small-Outline J-Lead Package (SOJ) (DM suffix)†



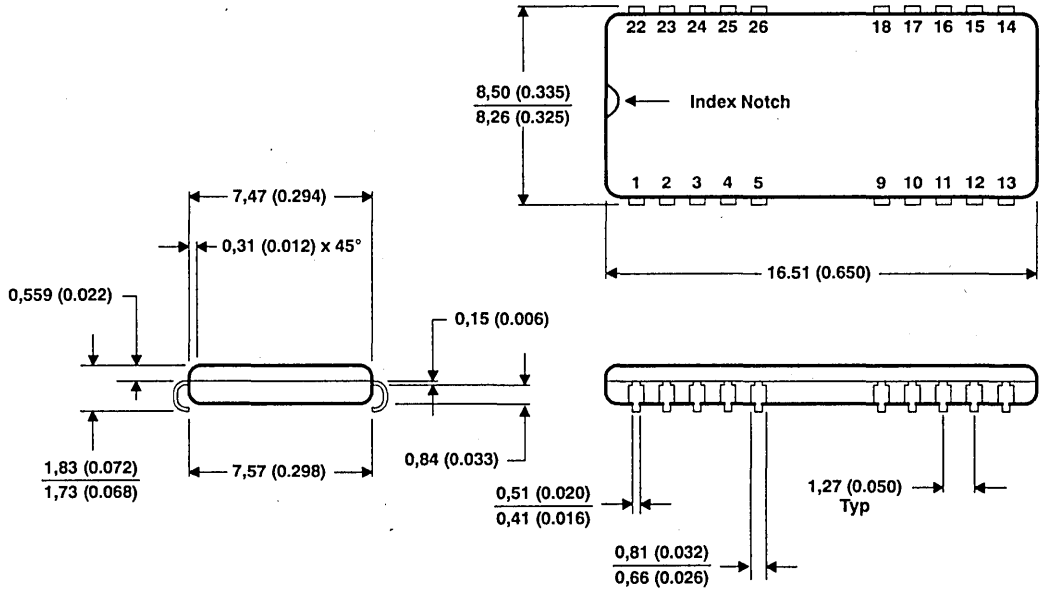
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

20/26-PIN
TMS44100
TMS44101
TMS44400
TMS44410

‡ Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0,125 (0.005).

20/26-Pin Plastic Thin Small-Outline J-Lead Package (TSOJ) (DN Suffix)†

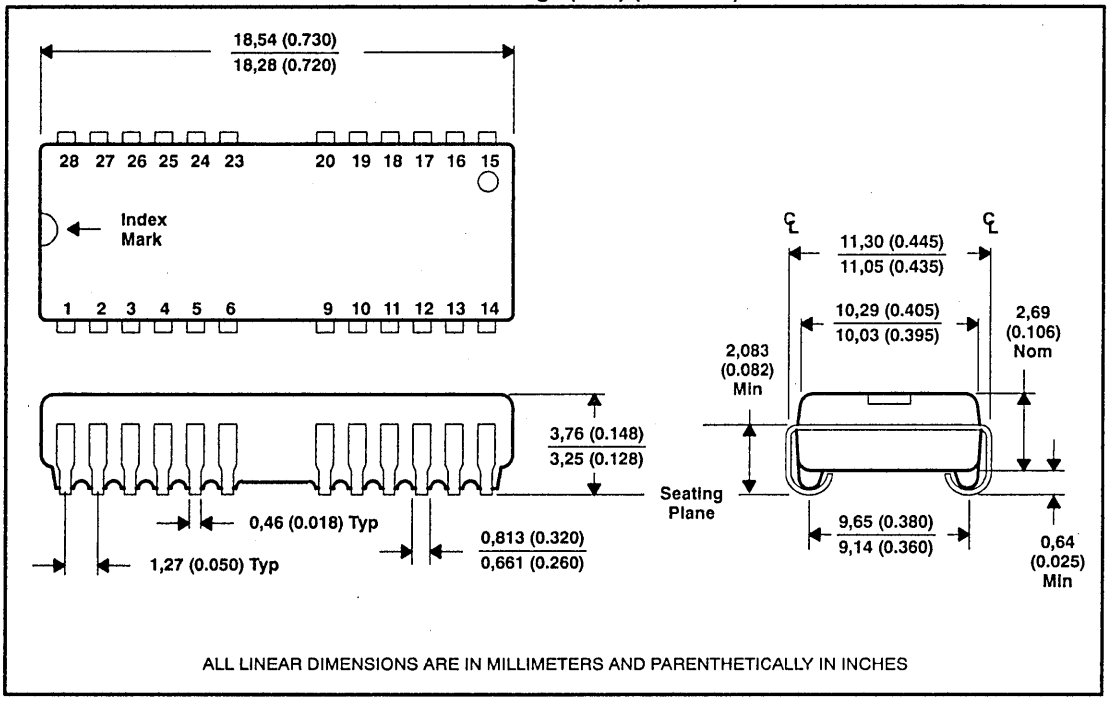


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

20/26-PIN
TMS4C1024
TMS4C1025
TMS4C1027
TMS44C256

24/28-Pin Plastic Small-Outline J-lead J-lead Package (SOJ) (DZ suffix)†

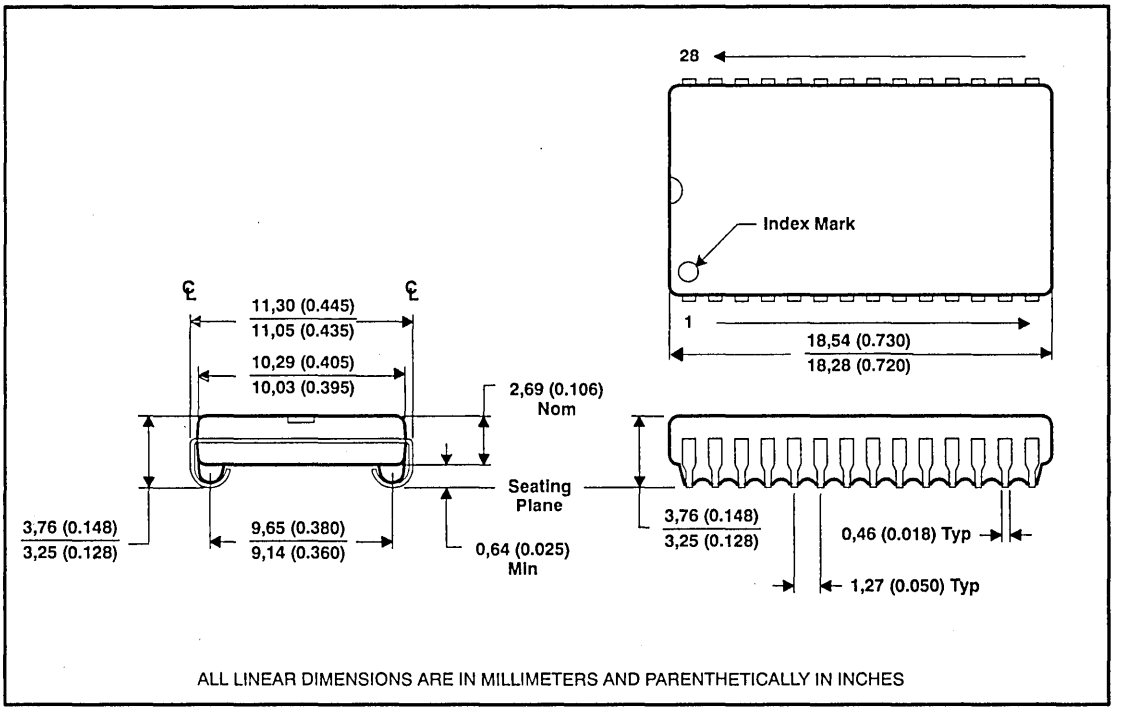


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

24/28-PIN
TMS416100
TMS416400

28-Pin Plastic Small-Outline J-Lead Package (SOJ) (DZ Suffix)†

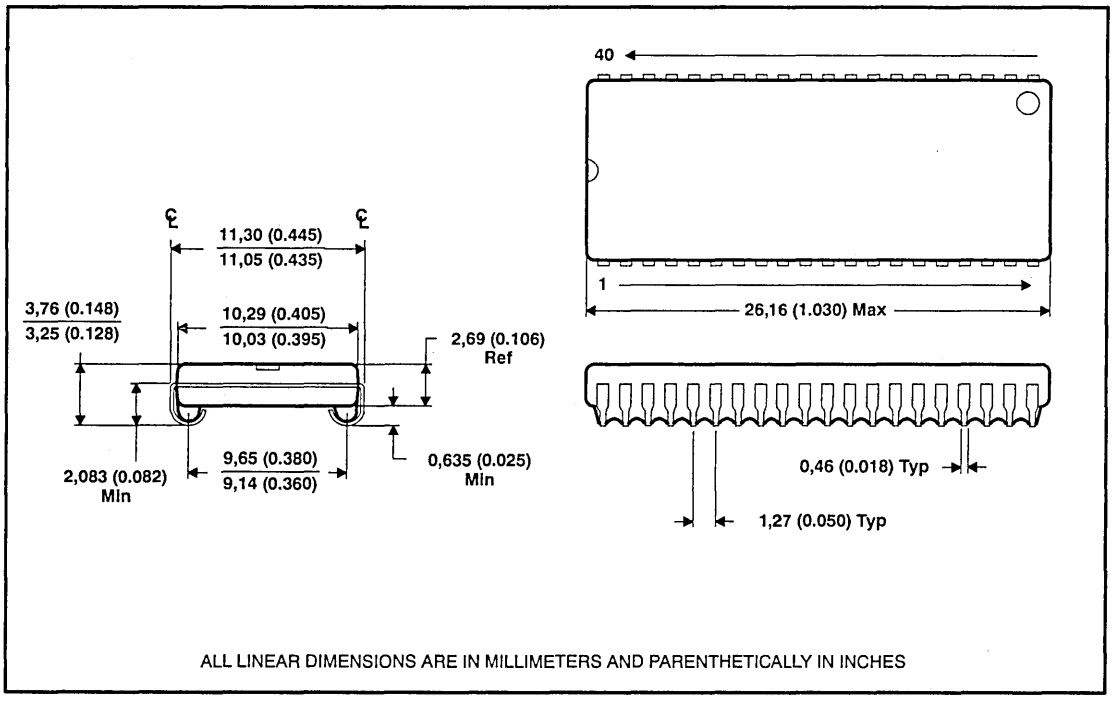


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

28-PIN
TMS44C250
TMS44C251

40-Pin Plastic Small-Outline J-Lead Package (SOJ) (DZ Suffix)†

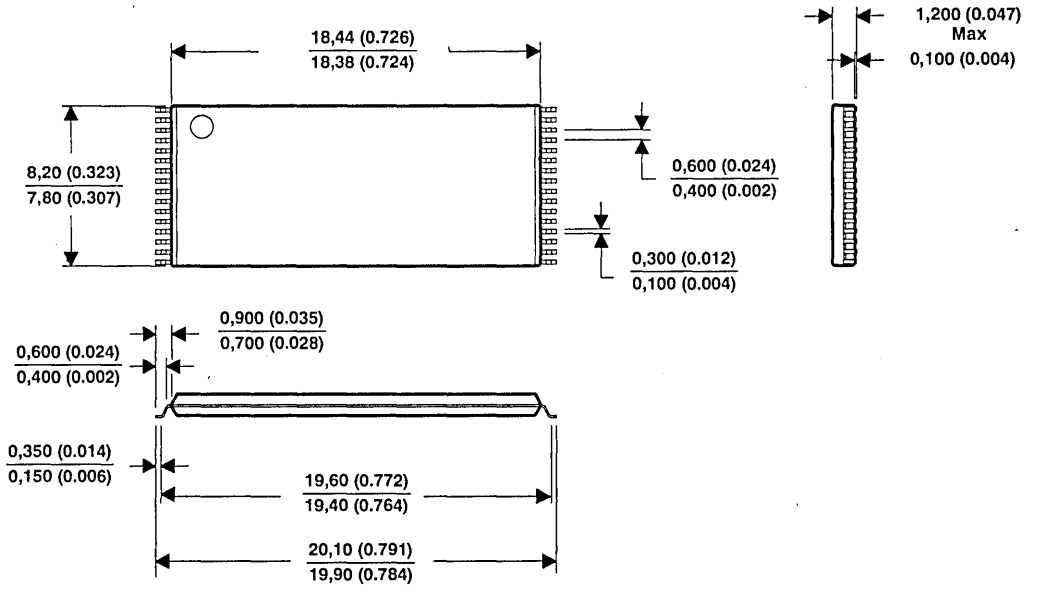


† Applicable MOS Memory Devices:

40-PIN
TMS48C121

32-Pin Plastic Thin Small-Outline J-Lead Package (TSOP) (DD Suffix)†

This package is under development.

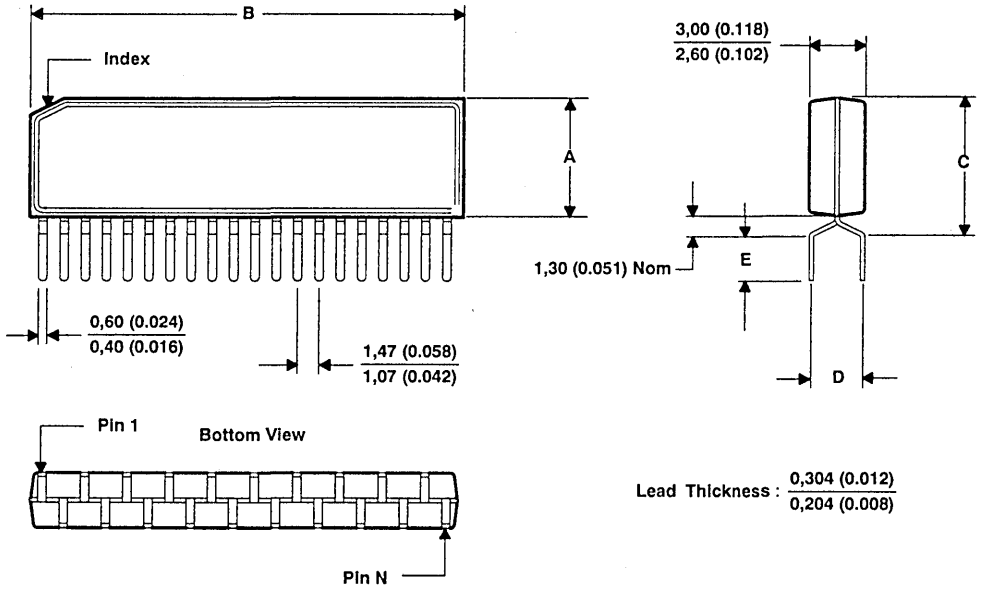


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

32-PIN‡
TMS29F259
TMS29F512
TMS29F010

Zig-Zag In-Line Plastic Package (ZIP) (SD suffix)†



DIM \ PIN	20	28
A‡	8,69 (0.342) Max	8,64 (0.340) Max
B‡	26,42 (1.040) Max	36,10 (1.420) Max
C (Max)	10,16 (0.400) Max	10,16 (0.400)
D	2,79 (0.110) 2,29 (0.090)	2,79 (0.110) 2,29 (0.090)
E	3,30 (0.130) 3,00 (0.118)	3,30 (0.130) 2,00 (0.118)

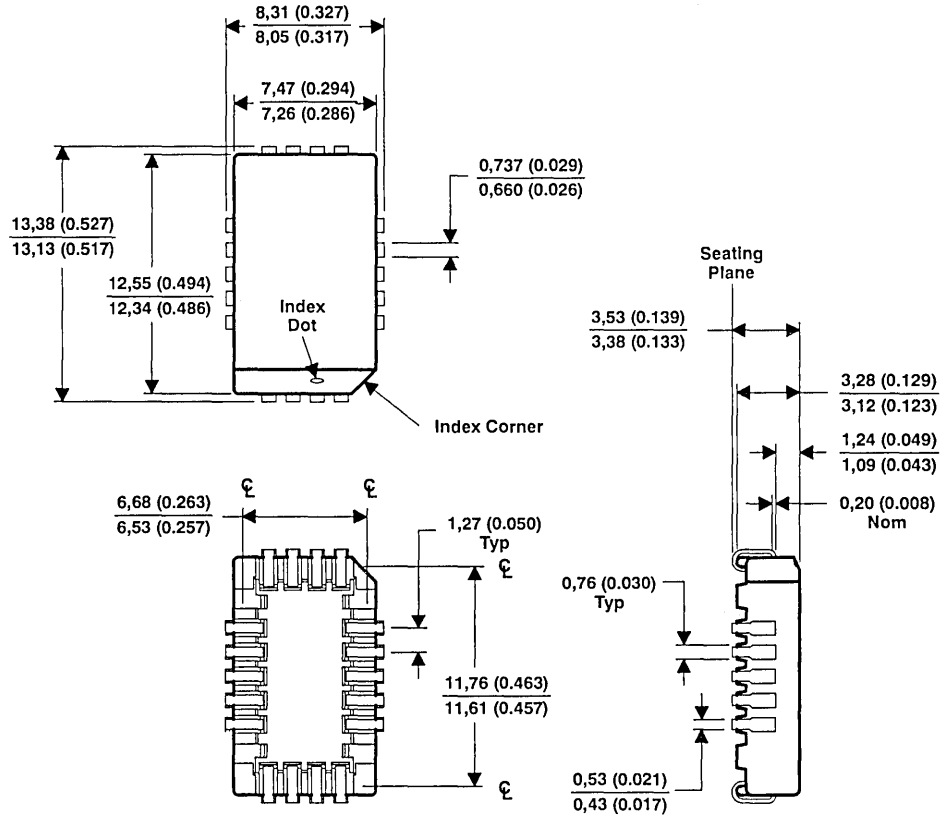
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

20-PIN	28-PIN
TMS4C1024	TMS44C250
TMS4C1025	TMS44C251
TMS4C1027	
TMS44C256	
TMS44100	
TMS44101	
TMS44400	
TMS44410	
TMS4C1050	
TMS4C1060	
TMS4C1070	

‡ Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0,125 (0.005).

18-Pin Plastic Leaded Chip Carrier (PLCC) (FM Suffix)†

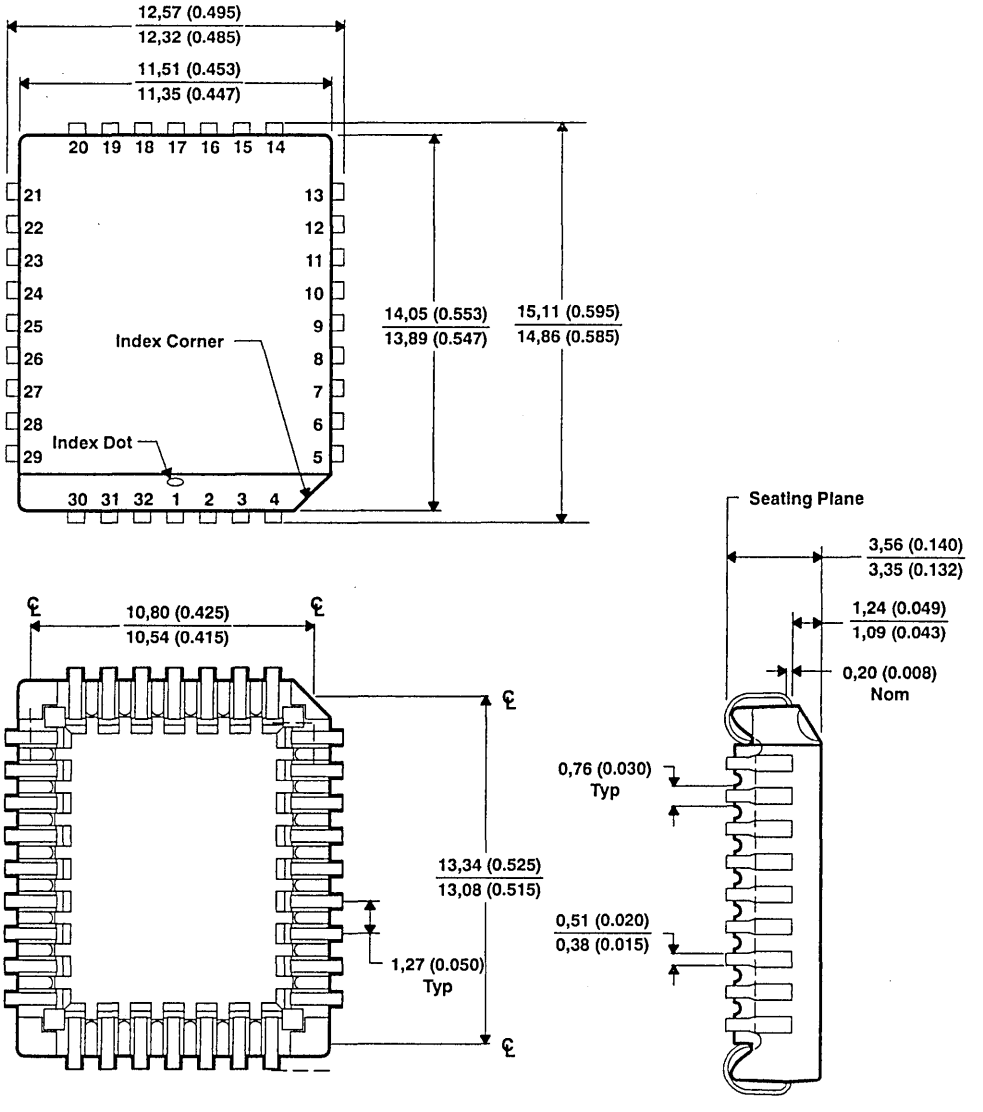


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLLY IN INCHES

† Applicable MOS Memory Devices:

18-PIN
TMS29F816

32-Pin Plastic Leaded Chip Carrier Package (PLCC) (FM suffix)†

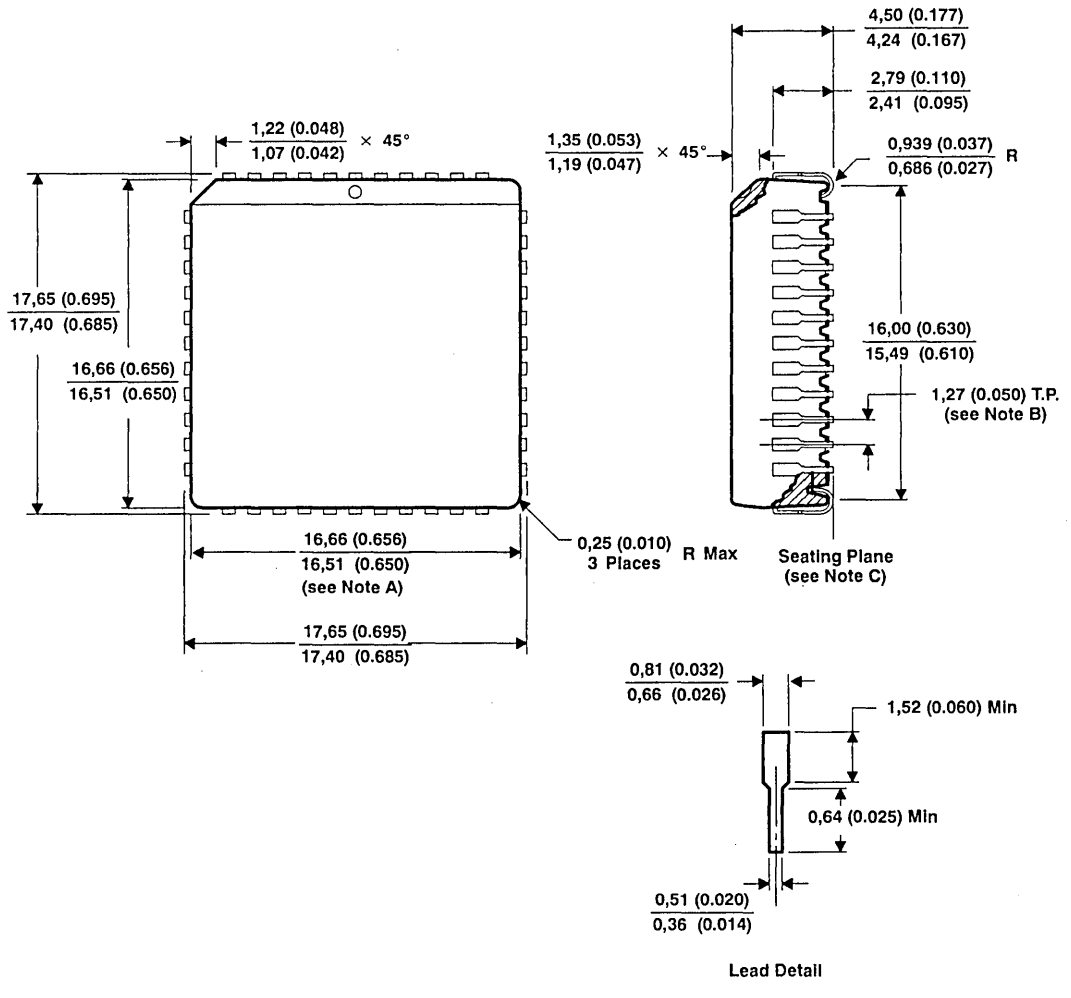


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHICALLY IN INCHES

† Applicable MOS Memory Devices:

32-PIN		
TMS27PC128	TMS27PC010A	TMS29F259
TMS27PC256	TMS27PC040	TMS29F512
TMS27PC510	TMS29F256	TMS29F010
TMS27PC512	TMS29F258	

44-Pin Plastic Leaded Chip Carrier Package (PLCC) (FN suffix)†



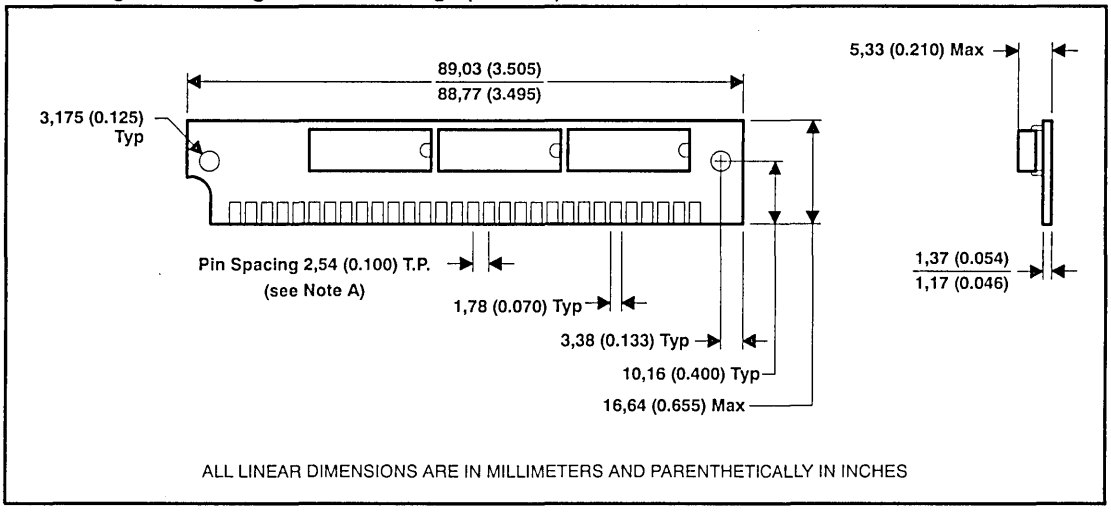
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHICALLY IN INCHES

NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by this dimension.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center of pin on each side.
C. The lead contact points are planar within 0,101 (0.004).

† Applicable MOS Memory Devices:

44-PIN
TMS27PC210A
TMS27PC240

30-Pin Single-Sided Single-In-Line Package (U Suffix)†

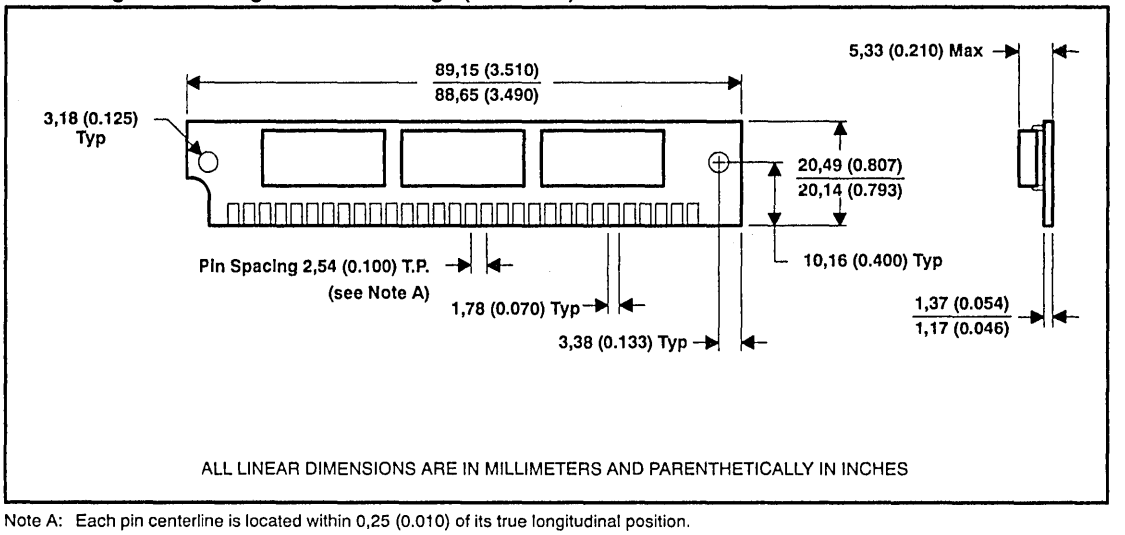


Note A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

† Applicable MOS Memory Devices:

30-PIN
TM256GU9C
TM124GU8A

30-Pin Single-Sided Single-In-Line Package (AD Suffix)†

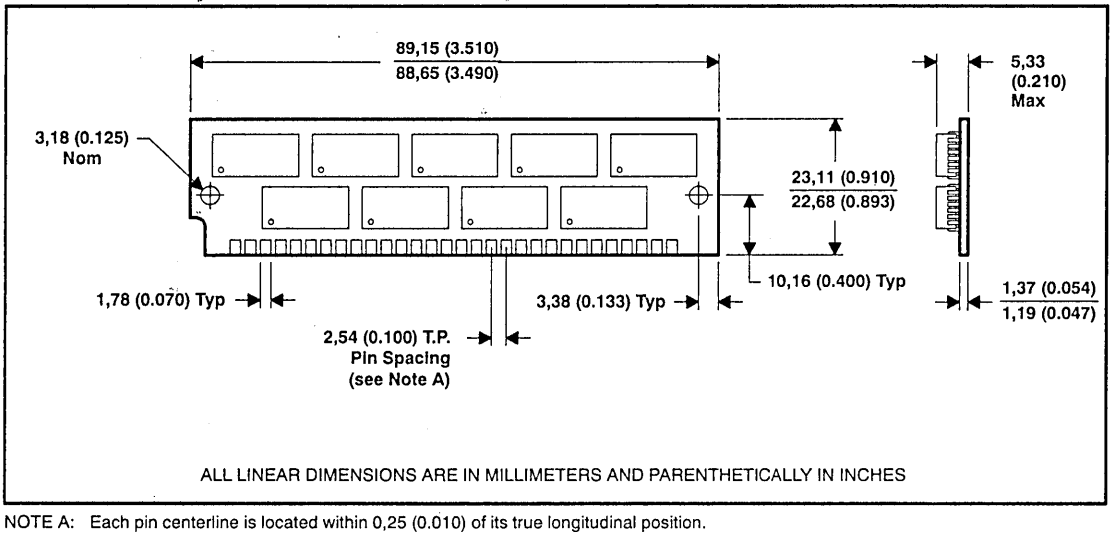


Note A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

† Applicable MOS Memory Devices:

30-PIN
TM024EAD9
TM124EAD9B
TM124EAD9C

30-Pin Single-Sided Single-In-Line Package (BD Suffix)†

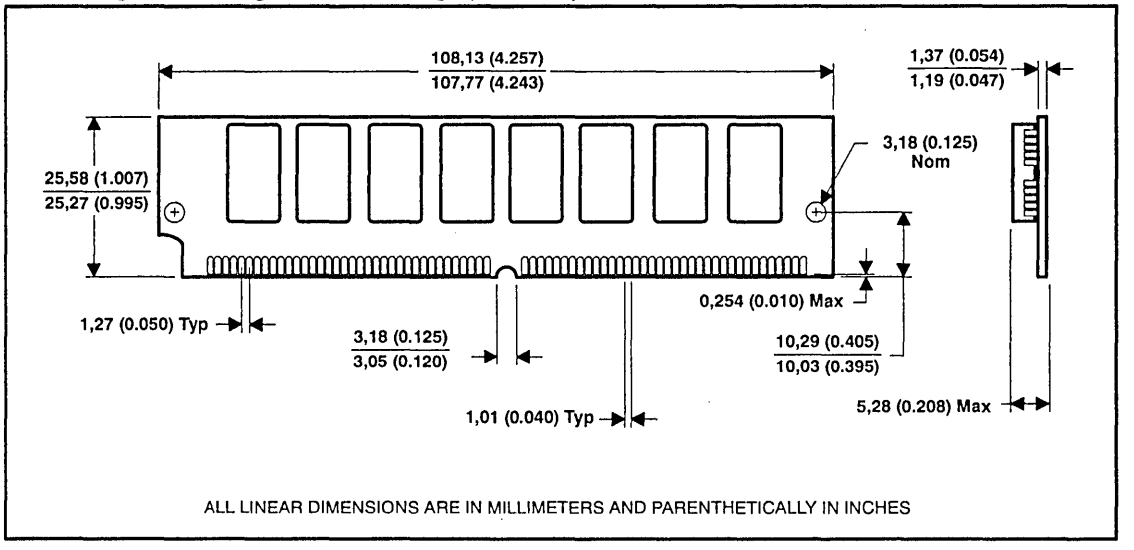


NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

† Applicable MOS Memory Devices:

30-PIN
TM4100GBD8
TM4100EBD9

72-Pin Single-Sided Single-In-Line Package (BK Suffix)†

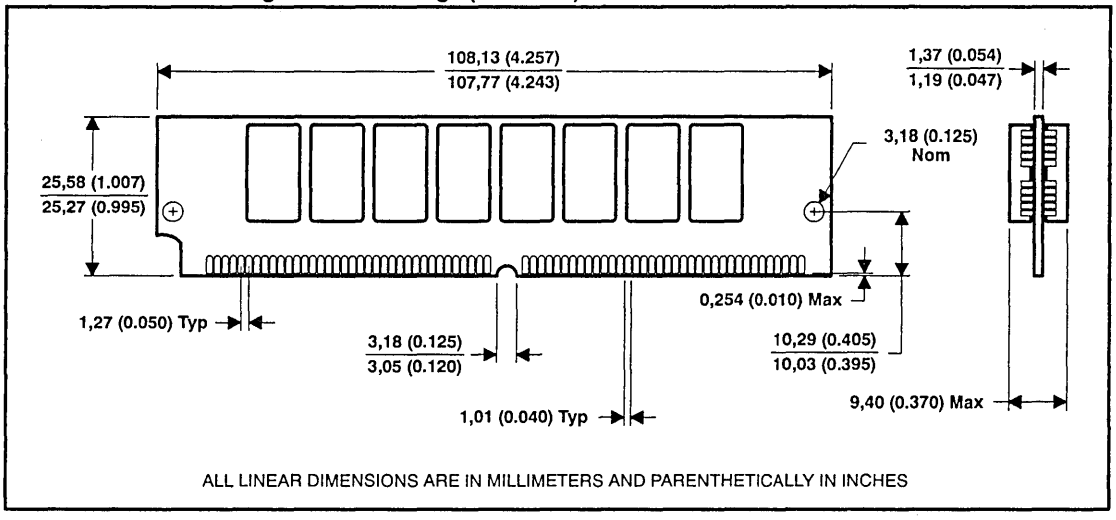


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

72-PIN
TM256BBK32
TM256KBK36B
TM256KBK36C
TM124BBK32
TM124MBK36B

72-Pin Double-Sided Single-in-line Package (BK Suffix)



NOTE A: Parts location may vary.

† Applicable MOS Memory Devices:

72-PIN
TM512CBK32
TM512LBK36B
TM512LBK36C
TM124MBK36A

MILITARY PACKAGES

The packages offered by the Military Products Division of Texas Instruments Semiconductor Group are designed to provide the most efficient and cost-effective method of meeting military system requirements. Products are offered in hermetic ceramic dual-in-line, ceramic flatpack, leadless ceramic chip carrier, and leaded ceramic chip carrier packages. All packages conform to the mechanical outlines contained in Appendix C of MIL-M-38510 except for package types that are not included in that specification. In the event of a conflict between dimensions contained in MIL-M-38510 Appendix C and other TI published mechanical outlines, MIL-M-38510 will take precedence.

Physical dimensions of the packages not contained in MIL-M-38510 Appendix C are contained in this document.

Ceramic Packages Available

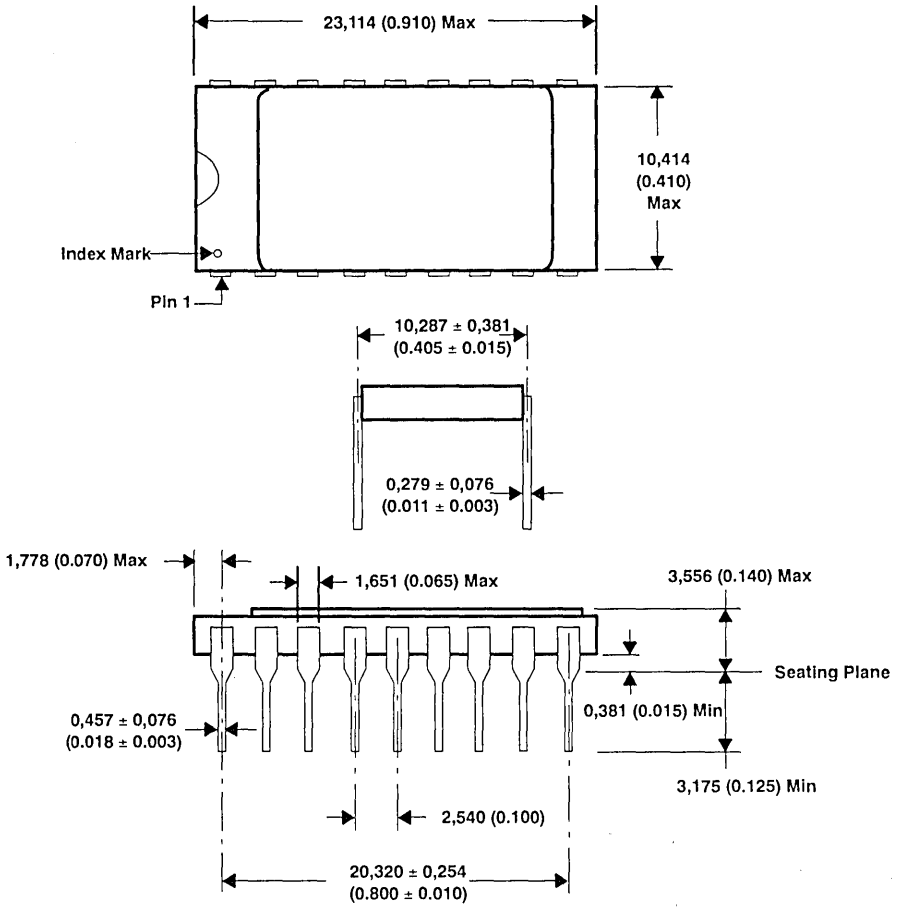
Package Designator	Description
HM, HL	Three-Layer Rectangle LCC - JEDEC Pinouts
J	Glass-Sealed CDIP
JD	Side-Brazed CDIP
HJ	Ceramic Small-Outline J-lead
HK	Side-Brazed Ceramic Flatpack
HR	Ceramic Flatpack

The TI published mechanical outlines for a given package type may vary slightly from product to product. To identify the detailed outline drawing for a particular product, refer to the specific data sheet for that product.

Mechanical Outlines

Size/Designator	Package Type	Applicable Specification	Typical Package Weight in Grams
18-pin JD	Side-Brazed Dual-In-Line	MIL-M-38510, App. C, D-6, Config 3	1.8
20-pin JD	Side-Brazed Dual-In-Line	MIL-M-38510, App. C, D-8, Config 3	2.0
20-pin HK	Side-Brazed Flatpack	TI Drawing	1.2
20-pad HL	Leadless Ceramic Chip Carrier	TI Drawing	1.1
20-pin HJ	Ceramic Small-Outline J-lead	TI Drawing	1.1
20-pad HM	Leadless Ceramic Chip Carrier	TI Drawing	1.3
20-pin HR	Ceramic Flatpack	TI Drawing	1.6
28-pin JD	Side-Brazed Dual-In-Line	MIL-M-38510, App. C, D-10, Config 3	5.3
28-pin HJ	Ceramic Small-Outline J-Lead	TI Drawing	1.5
28-pin J	Ceramic Dual-In-Line	MIL-M-38510, App. C, D-10, Config 1	7.9
32-pin J	Ceramic Dual-In-Line	TI Drawing	8.9

18-Pin Ceramic Sidebrazed Dual-In-Line Package (JD suffix)



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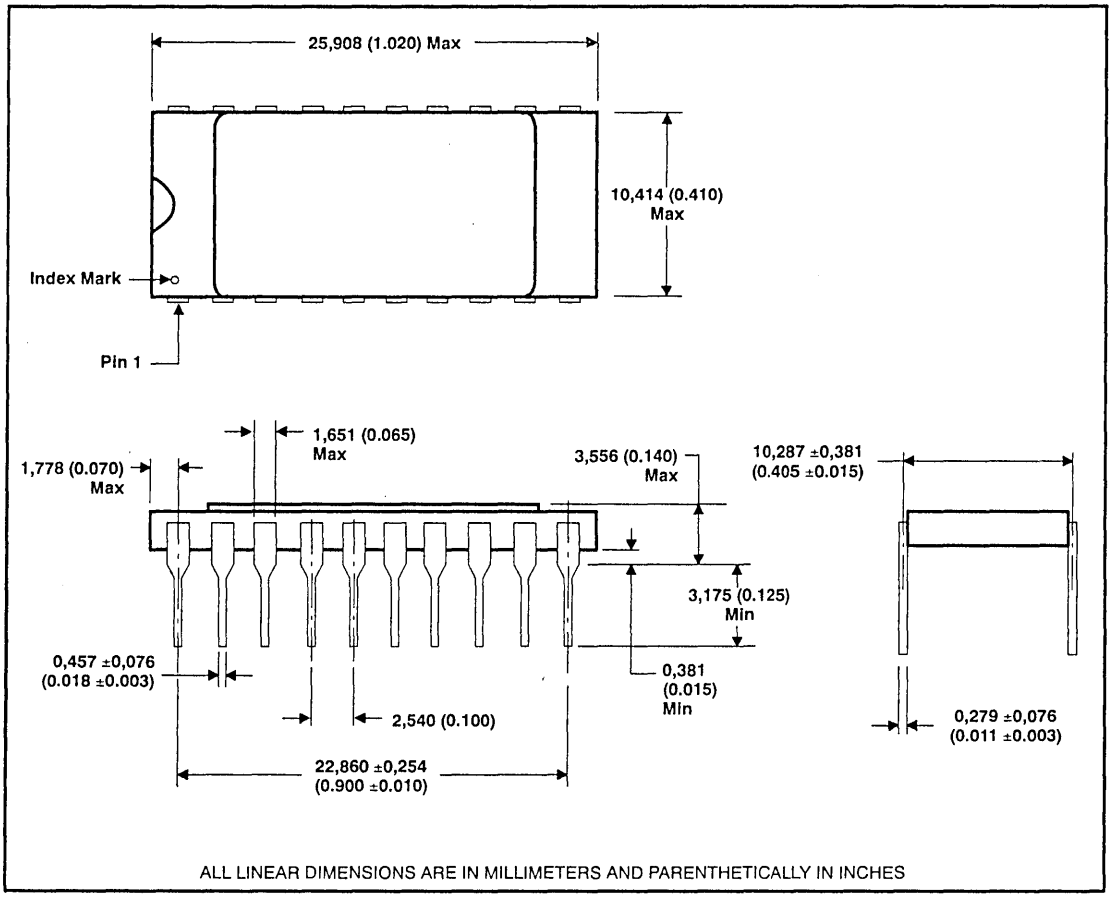
20-Pin Ceramic Sidebrazed Dual-In-Line Package (JD Suffix)



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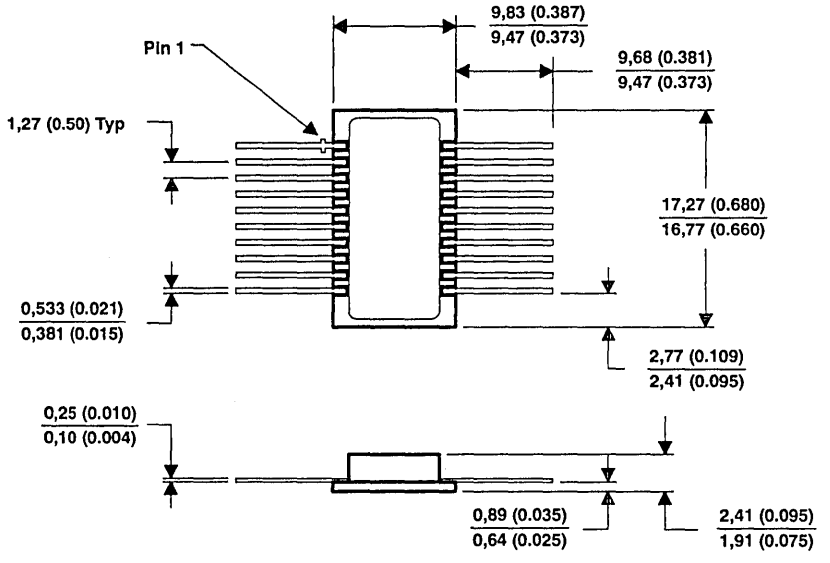
20-Pin Ceramic Flatpack (HK Suffix)



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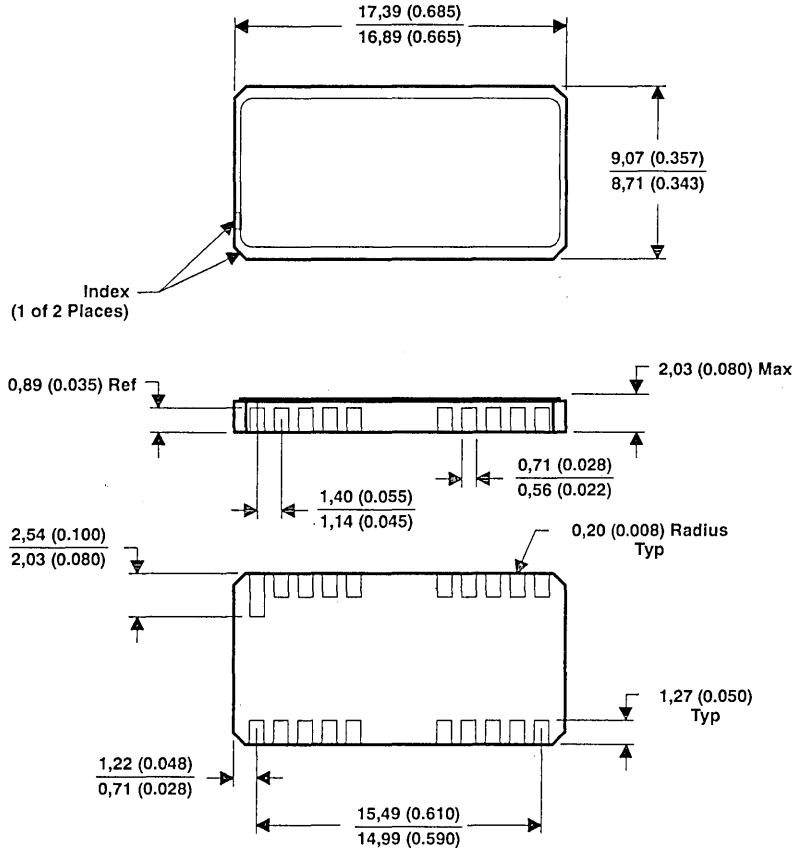
20-Pin Small-Outline Leadless Ceramic Chip (HL Suffix)



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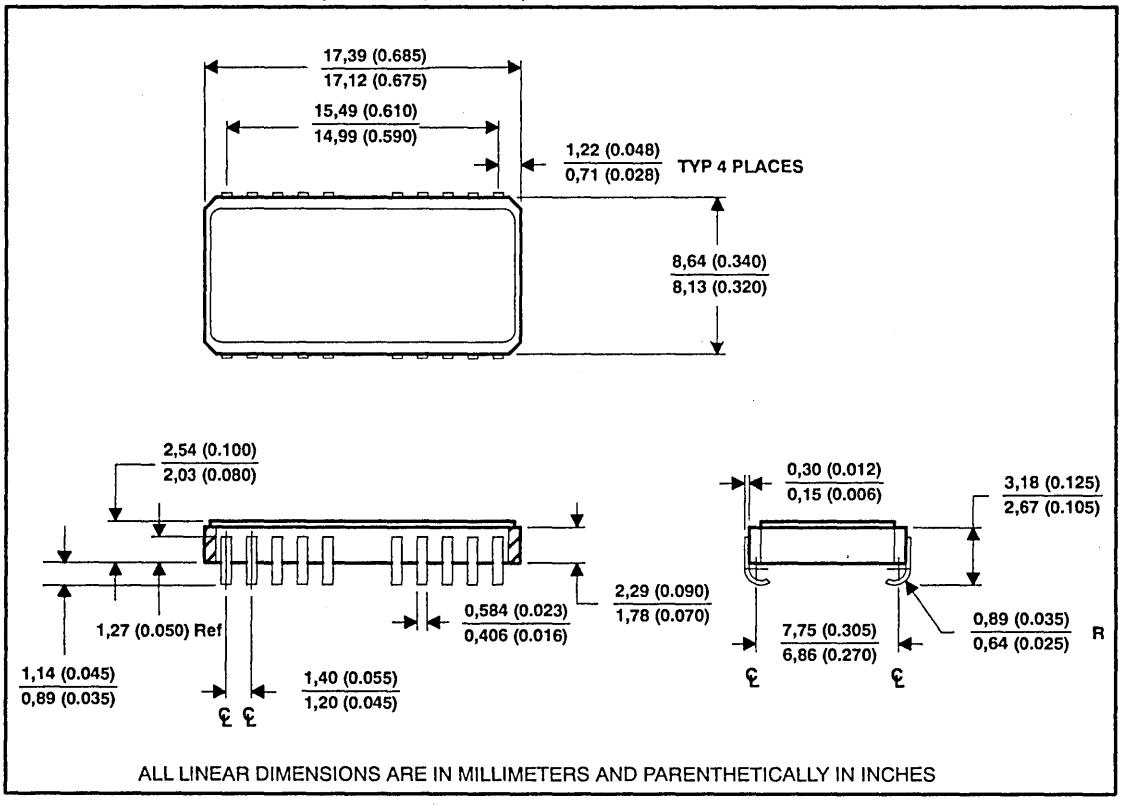
20/26-Pin Leaded Ceramic Chip Carrier (HJ Suffix)



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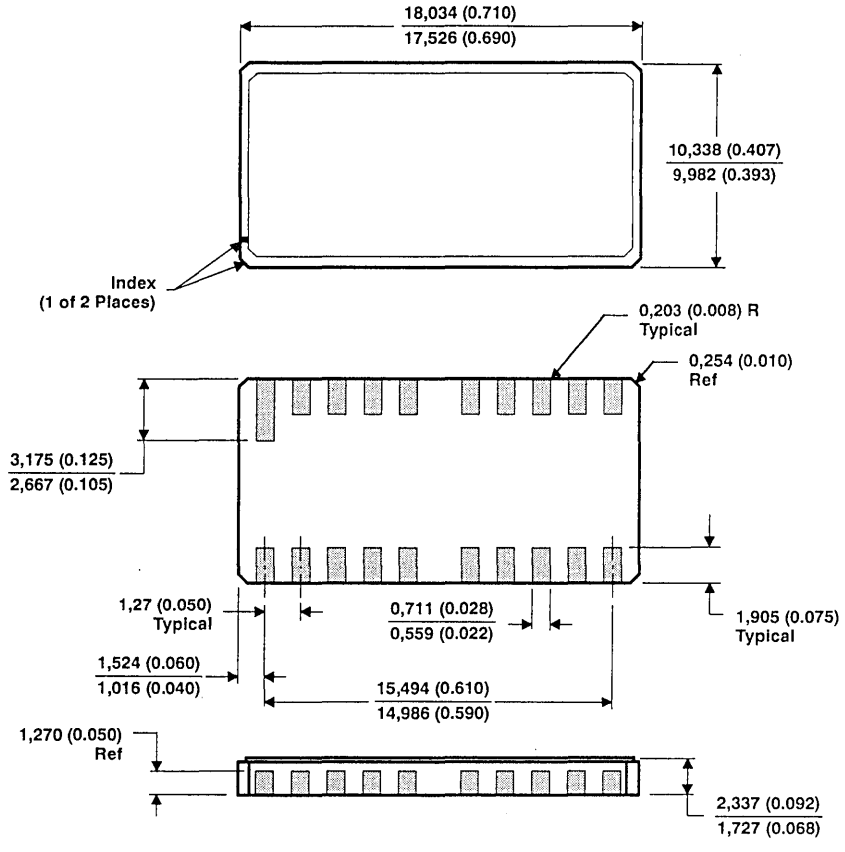
20-Pin Leadless Ceramic Chip Carrier (HM Suffix)



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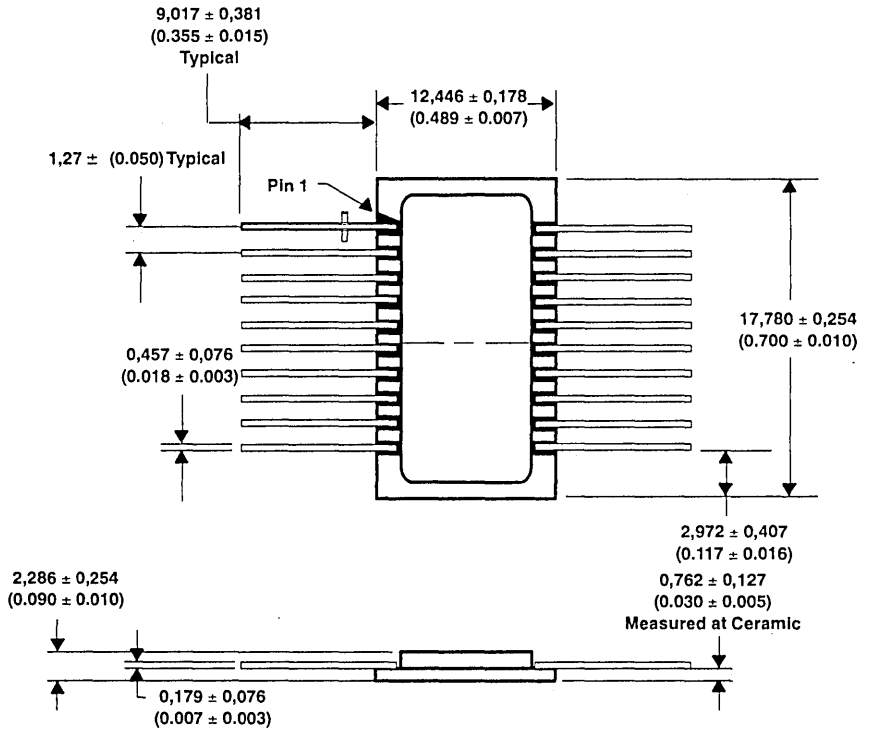
20-Pin Ceramic Flatpack (HR suffix)



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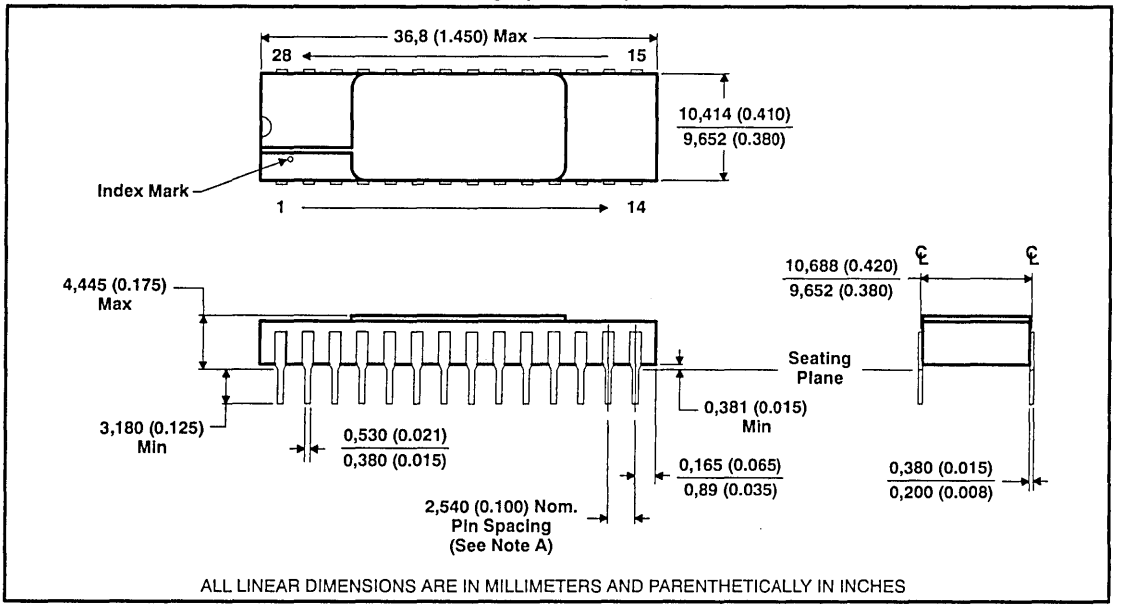
28-Pin Ceramic Sidebrazed Dual-In-Line Package (JD Suffix)



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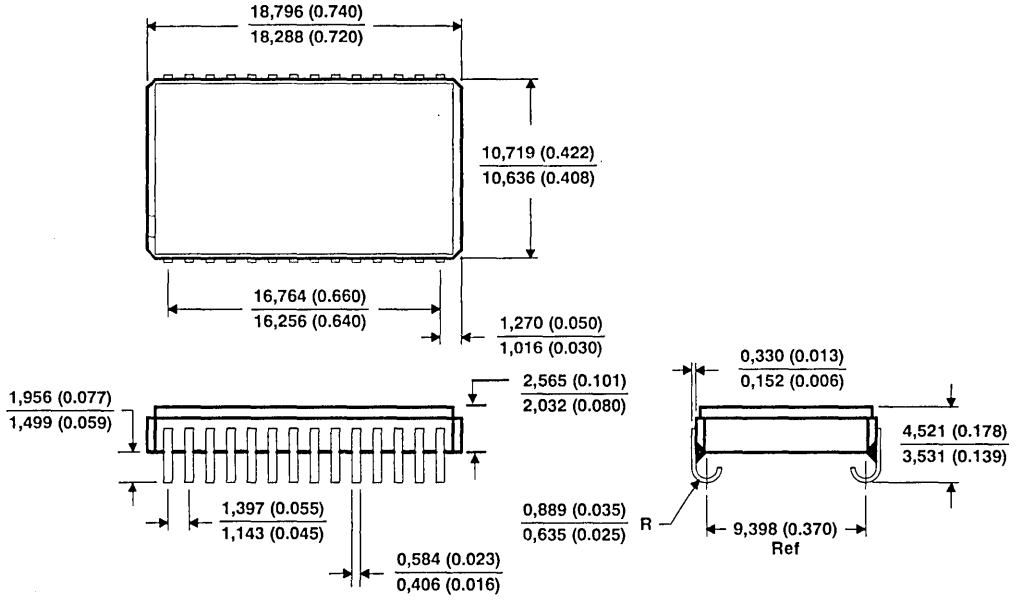
NOTE A: Each pin centerline is located within 0,250(0.010) of its true longitudinal position.

28-Pin Ceramic Small-Outline J-Lead Chip Carrier (HJ Suffix)



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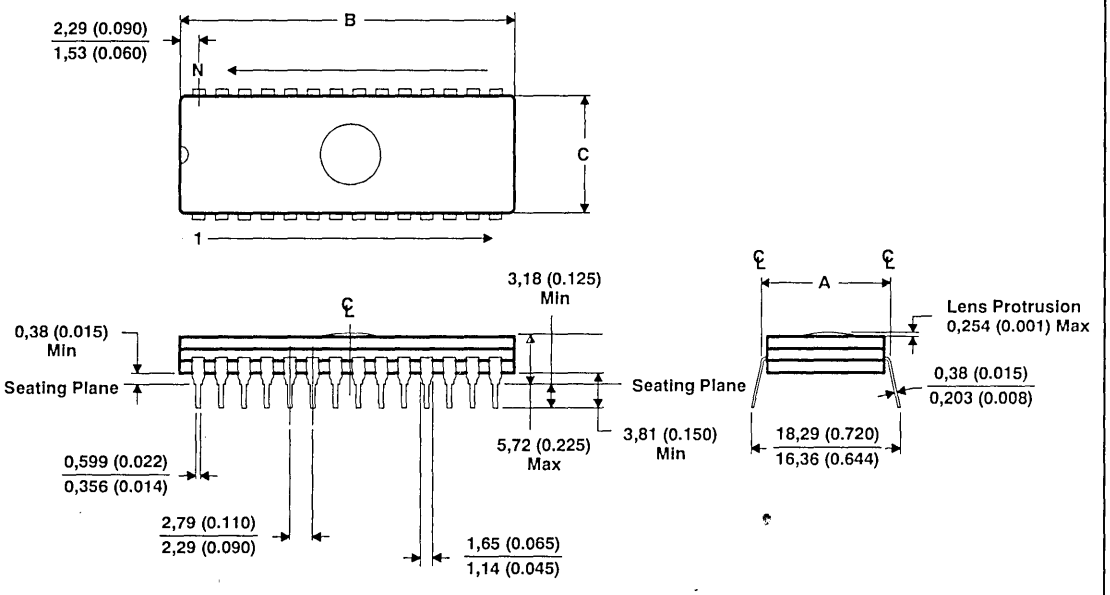
Ceramic Dual-In-Line Package (J suffix)



DIM \ PIN	28	32
A (Max)	15,75 (0.620)	15,75 (0.620)
B (Max)	37,21 (1.465)	42,37 (1.668)
C (Max)	15,49 (0.610)	15,49 (0.610)

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