TEXAS INSTRUMENTS

Linear Circuits

3-V Family

Data Book

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1994

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Linear Products

Linear Circuits Data Book

3-V Family

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INTRODUCTION

Texas Instruments offers the industry's first dedicated family of linear integrated circuits (ICs) that are specifically designed, characterized, and tested for operation at 3.3 V or less. This revised edition of the 3-V data book is expanded to include analog data converters and multichannel RS232 circuits, in addition to new offerings of operational amplifiers and comparators.

Many of the 3-V devices are available in the thin-scaled small-outline package (TSSOP), and all are available in the JEDEC-standard small-outline or through-hole packages. The TSSOP surface-mount package is just 1.1-mm (max) thick and can be a real space saver in densely packed designs.

While this manual offers information only on the 3-V analog devices available now from Texas Instruments, complete technical data for upcoming 3-V devices or any other TI semiconductor product is available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

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Dallas, Texas 75380-9066

We feel that this revised 3-V Family Data Book will be a significant addition to your library of technical literature from Texas Instruments.

operational amplifiers

DEVICE	V_{CC} (V)		V_{IO} (mV)	I_{CC} (μA)	I_{IB} (pA)	CMRR (dB)	V_n (nV/√Hz)	S/R (V/μs)	GBW (kHz)	DESCRIPTION
	MIN	MAX	MAX	MAX	TYP	TYP	TYP	TYP	TYP	
TLV2262	2.7	8	2.5	250	1	75	12	0.55	800	Dual, low noise, micropower, rail-to-rail
TLV2262A	2.7	8	0.95	250	1	77	12	0.55	800	Dual, precision, low noise, micropower, rail-to-rail
TLV2264	2.7	8	2.5	250	1	75	12	0.55	800	Quad, low noise, micropower, rail-to-rail
TLV2264A	2.7	8	0.95	250	1	77	12	0.55	800	Dual, precision, low noise, micropower, rail-to-rail
TLV2322	2	8	9	17	0.6	88	68	0.02	27	Quad, micropower
TLV2332	2	8	9	250	0.6	92	32	0.38	300	Dual, low power
TLV2342	2	8	9	1500	0.6	78	25	2.1	790	Dual, high speed
TLV2324	2	8	10	17	0.6	88	68	0.02	27	Quad, micropower
TLV2334	2	8	10	250	0.6	92	32	0.38	300	Quad, low power
TLV2344	2	8	10	1500	0.6	78	25	2.1	790	Quad, high speed
TLV2341	2	8	8	1500	0.6	78	25	2.1	790	Single, programmable power (high bias)
TLV2341	2	8	8	250	0.6	92	32	0.38	300	Single, programmable power (medium bias)
TLV2341	2	8	8	17	0.6	88	68	0.02	27	Single, programmable power (low bias)
TLV2362	±1	±2.5	6	2250	2000	75	9	2.5	6000	Dual, low noise, high-speed

comparators

DEVICE	V_{CC} (V)		V_{IO} (mV)	I_{CC} (μA)	I_{IB} (nA)	I_{OL} (mA)	t_{pd} (ns)	DESCRIPTION
	MIN	MAX	MAX	MAX	TYP	MIN	TYP	
TLV1393	2	7	5	125	40	0.5	650	Dual, low power
TLV2352	2	8	5	125	0.005	6	640	Dual, general purpose
TLV2254	2	8	5	250	0.005	6	640	Quad, general purpose
TLV2393	2	7	5	300	100	4	450	Dual, high speed

voltage regulators

DEVICE	V_O (V)	I_O (mA)	I_O (mA)	DROPOUT VOLTAGE (mV)	TOLERANCE (±%)	DESCRIPTION
	TYP	MAX	TYP	MAX		
TLV2217-33	3.3	500	2	500	1	Fixed 3.3 V, low dropout

p-channel MOSFETs

DEVICE	V_{DS} (V)	$r_{DS(on)}$ (V_{GS} = −10 V) Ω	$r_{DS(on)}$ (V_{GS} = −4.5 V) Ω	$r_{DS(on)}$ (V_{GS} = −2.7 V) Ω	I_D (A)	DESCRIPTION
	MAX	TYP	TYP	TYP	MAX	
TPS1100	−15	0.18	0.291	0.606	±1.58	Single p-channel enhancement-mode MOSFET
TPS1101	−15	0.09	0.134	0.232	±2.12	Single p-channel enhancement-mode MOSFET

data acquisition and conversion

DEVICE	ADDRESS AND DATA I/O FORMAT	ANALOG SIGNAL INPUTS	RESOLUTION (BITS)	CONVERSION SPEED (μs)	TOTAL ERROR	DESCRIPTION
TLV1543	Serial	11	10	21	±1 LSB	10-bit analog-to-digital converter
TLV1549	Serial	1	10	21	±1 LSB	10-bit analog-to-digital converter

data-transmission circuits

DEVICE	APPLICATION	BUS I/O	DRIVERS/RECEIVERS PER PACKAGE	DESCRIPTION
SN75LV4735	EIA Standard RS-232-D	Single ended	3/5	Multichannel RS232 line driver/receiver

available features

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 12 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Low Power . . . 500 μA Max**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage 950 μV Max at T_A = 25°C**
- **Wide Supply Voltage Range 2.7 V to 8 V**
- **Macromodel Included**

description

The TLV2262 and TLV2262A are dual operational amplifiers manufactured using Texas Instruments Advanced LinCMOS™ process. These devices are optimized and fully specified for single-supply 3-V and 5-V operation. For this low-voltage operation combined with μpower dissipation levels, the input noise voltage performance has been dramatically improved using optimized design techniques for CMOS-type amplifiers. Another added benefit is that these amplifiers exhibit rail-to-rail output swing. Figure 1 graphically depicts the high-level output voltage for different levels of output current for a 3-V single supply. The output dynamic range can be extended using the TLV2262 with loads referenced midway between the rails. The common-mode input voltage range is wider than typical standard CMOS-type amplifiers. To take advantage of this improvement in performance and to make this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ± 5 mV, allowing a minimum of 0 to 2-V common-mode input voltage range for a 3-V supply. Furthermore, at 200 μA (typical) of supply current per amplifier, the TLV2262 family can achieve input offset voltage levels as low as 950 μV, outperforming existing CMOS amplifiers. The Advanced LinCMOS process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input-impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

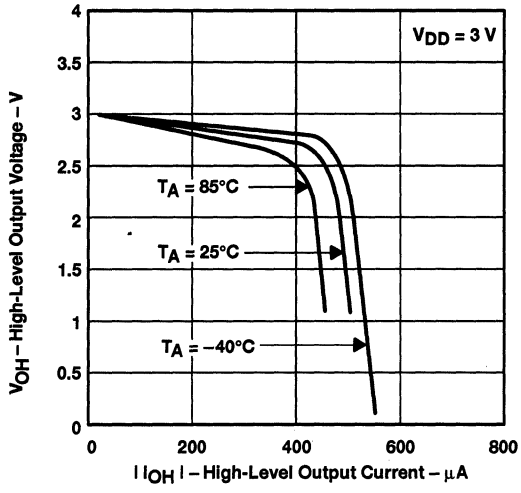

Figure 1

AVAILABLE OPTIONS

PACKAGED DEVICES					CHIP FORM (Y)
T_A	V_{IO}max AT 25°C	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 85°C	950 μV	TLV2262AID	TLV2262AIP	TLV2262AIPWLE	TLV2262Y
	2.5 mV	TLV2262ID	TLV2262IP	—	

The D packages are available taped and reeled. Add R suffix to device type, (e.g., TLV2262IDR).
The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

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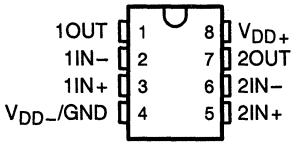
description (continued)

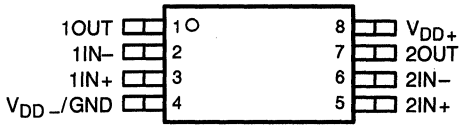
The TLV2262 and TLV2262A, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources such as piezoelectric transducers. Because of the low power dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes these devices great choices when interfacing directly to ADCs. All of these features combined with its temperature performance make the TLV2262 family ideal for remote pressure sensors, temperature control, active VR sensors, accelerometers, hand-held metering, and many other applications.

The device inputs and outputs are designed to withstand a 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD+} supply-line transients under powered conditions. Transients of greater than 20 V can trigger the ESD-protection structure, inducing a low-impedance path to V_{DD-}/GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so could result in a latched condition and device failure.

D OR P PACKAGE
(TOP VIEW)



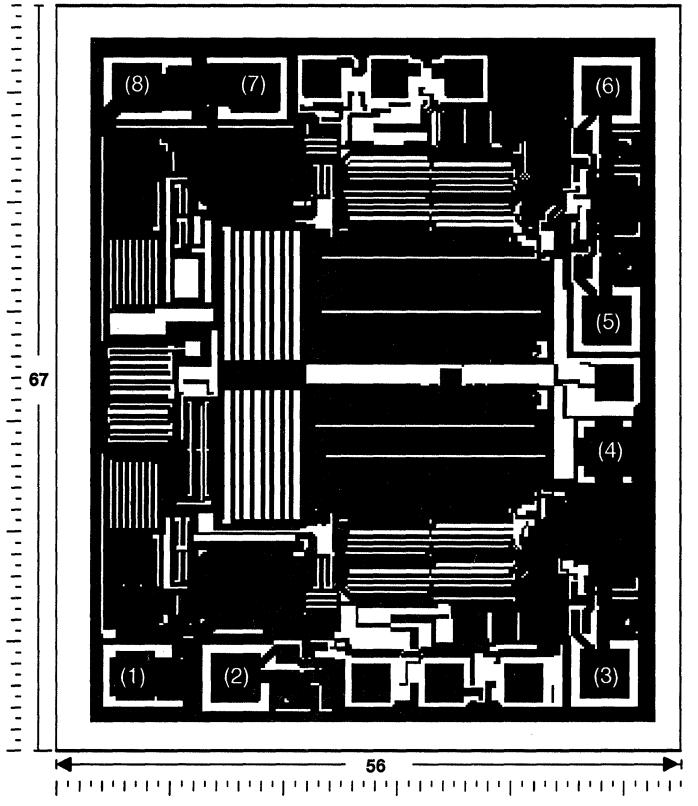
PW PACKAGE
(TOP VIEW)

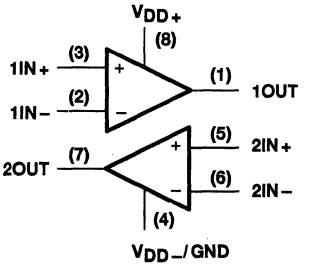


TLV2262Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2262. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

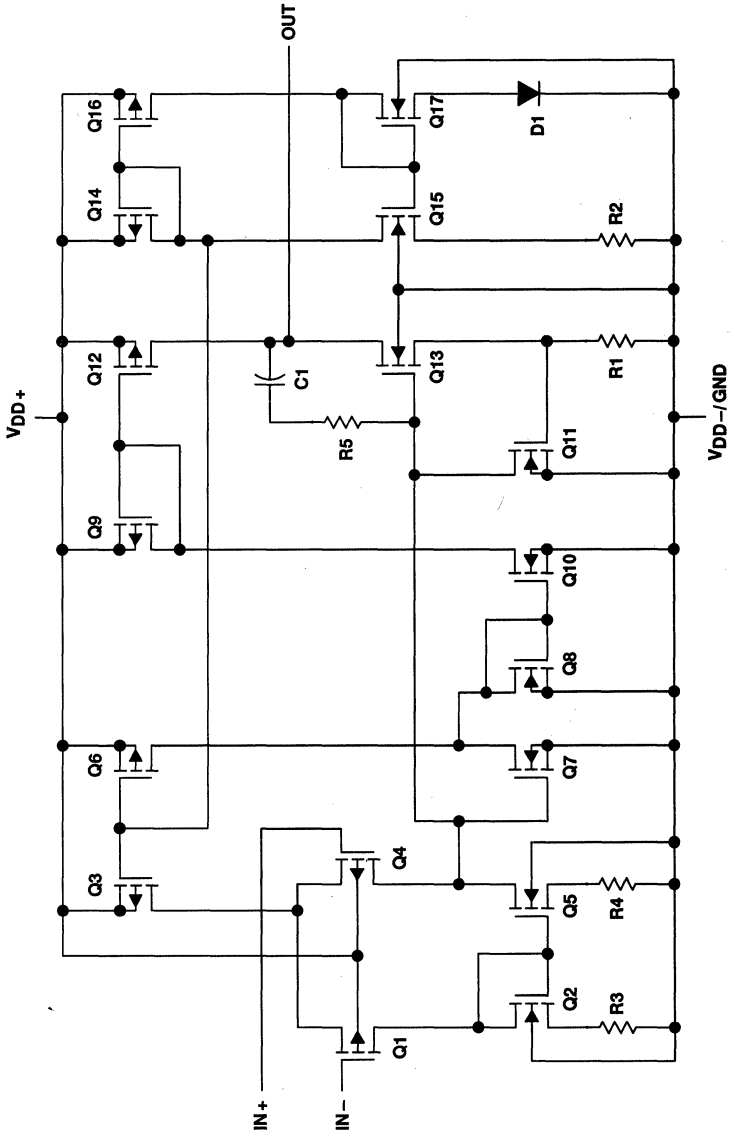
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	38
Diodes	9
Resistors	26
Capacitors	3

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... $\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1) ..... −0.3 V to V_{DD}
Input current, I_I (each input) ..... ±5 mA
Output current, I_O ..... ±50 mA
Total current into V_{DD+} ..... ±50 mA
Total current out of V_{DD-} ..... ±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows if input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{DD\pm}$ (see Note 1)	2.7	8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+}-1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+}-1.3$	V
Operating free-air temperature, T_A	−40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-}.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2262			TLV2262A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$5 mV	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		2.99			2.99		V
		I_{OH} = −100 µA		25°C	2.85			2.85			
				Full range	2.825			2.825			
		I_{OH} = −200 µA		25°C	2.7			2.7			
				Full range	2.65			2.65			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 µA	25°C		10			10		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 µA	25°C		100			100		
				Full range			150			150	
		V_{IC} = 1.5 V,	I_{OL} = 1 mA	25°C		200			200		
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 50 kΩ‡	25°C	60	100		60	100		V/mV
				Full range	30			30			
			R_L = 1 MΩ‡	25°C		100			100		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		270			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V,	R_S = 50 Ω	25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, No load,	$V_{IC} = V_{DD}/2$	25°C	80	95		80	100		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 1.5 V,	No load	25°C		400	500		400	500	µA
				Full range			500			500	

† Full range is – 40°C to 85°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2262			TLV2262A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.1 V to 1.9 V, R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.6			0.6		μV
		f = 0.1 Hz to 10 Hz		25°C		1			1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.03%			0.03%		
			A_V = 10			0.05%			0.05%		
	Gain-bandwidth product	f = 1 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.67			0.67		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		300			300		kHz
	Settling time	A_V = −1, Step = 1 V to 2 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		5.6			5.6		μs
			To 0.01%			12.5			12.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		61°			61°		
	Gain margin			25°C		14			14		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 1.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2262			TLV2262A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD}\pm$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	$|V_{IO}| \le$5 mV	R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −100 μA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_{OH} = −200 μA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.6			4.6			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	170		80	170		V/mV
				Full range	55			55			
			R_L = 1 MΩ‡	25°C		550			550		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, No load,	V_{IC} = V_{DD}/2	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		400	500		400	500	μA
				Full range			500			500	

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2262			TLV2262A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°			63°		
	Gain margin			25°C		14			14		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V

electrical characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV2262Y			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD}\pm$ = ±1.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω			300	2500	μV
I_{IO}	Input offset current					0.5	150	pA
I_{IB}	Input bias current					1	150	pA
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO}\rvert \le$ 5 mV,	R_S = 50 Ω		0 to 2	−0.3 to 2.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA				2.99		V
		I_{OH} = −200 μA			2.7	2.75		
V_{OL}	Low-level output voltage	V_{IC} = 0 V,	I_{OL} = 50 μA			10		V
		V_{IC} = 0 V,	I_{OL} = 500 μA			100	125	
		V_{IC} = 0 V,	I_{OL} = 1 mA			200	250	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V	R_L = 50 kΩ†		60	100		V/mV
			R_L = 1 MΩ†			100		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V,	V_O = 0,	R_S = 50 Ω	65	77		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V,	No load,	V_{IC} = 0	80	100		dB
I_{DD}	Supply current	V_O = 0,	No load			400	500	μA

† Referenced to 1.5 V

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV2262Y			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω			300	2500	μV
I_{IO}	Input offset current					0.5	150	pA
I_{IB}	Input bias current					1	150	pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	R_S = 50 Ω		0 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA				4.99		V
		I_{OH} = −100 μA			4.85	4.94		
		I_{OH} = −200 μA			4.7	4.85		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA			0.09	0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA			0.2	0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ†		80	170		V/mV
			R_L = 1 MΩ†			550		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V,	V_O = 2.5 V,	R_S = 50 Ω	70	83		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V,	No load,	$V_{IC} = V_{DD}/2$	80	95		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load			400	500	μA

† Referenced to 2.5 V

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	2, 3
		vs Common-mode voltage	4, 5
α_{VIO}	Input offset voltage temperature coefficient	Distribution	6, 7
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature	8
V_I	Input voltage	vs Supply voltage	9
		vs Free-air temperature	10
V_{OH}	High-level output voltage	vs High-level output current	11, 14
V_{OL}	Low-level output voltage	vs Low-level output current	12, 13, 15
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	16
I_{OS}	Short-circuit output current	vs Supply voltage	17
		vs Free-air temperature	18
V_{ID}	Differential input voltage	vs Output voltage	19, 20
A_{VD}	Differential voltage amplification	vs Load resistance	21
		vs Frequency	22, 23
		vs Free-air temperature	24, 25
z_o	Output impedance	vs Frequency	26, 27
CMRR	Common-mode rejection ratio	vs Frequency	28
		vs Free-air temperature	29
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	30, 31
		vs Free-air temperature	32
I_{DD}	Supply current	vs Free-air temperature	33
SR	Slew rate	vs Load capacitance	34
		vs Free-air temperature	35
V_O	Large-signal pulse response	vs Time	36, 37, 38, 39
V_O	Small-signal pulse response	vs Time	40, 41, 42, 43,
V_n	Equivalent input noise voltage	vs Frequency	44, 45
	Noise voltage (referred to input)	Over a 10-second period	46
	Integrated noise voltage	vs Frequency	47
THD + N	Total harmonic distortion plus noise	vs Frequency	48
	Gain-bandwidth product	vs Free-air temperature	49
		vs Supply voltage	50
ϕ_m	Phase margin	vs Frequency	22, 23
		vs Load capacitance	51
	Gain margin	vs Load capacitance	52
B_1	Unity-gain bandwidth	vs Load capacitance	53
	Overestimation of phase margin	vs Load capacitance	54

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLV2262
INPUT OFFSET VOLTAGE

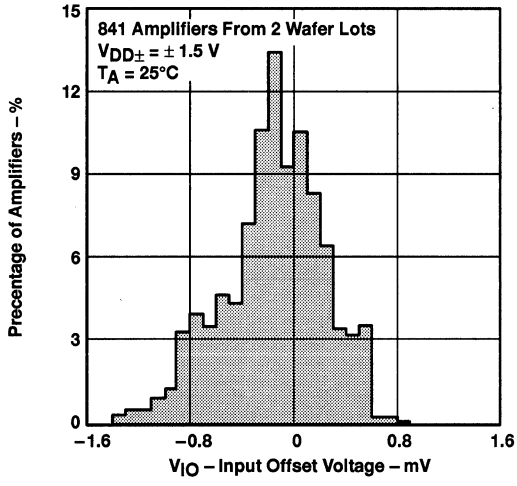


Figure 2

DISTRIBUTION OF TLV2262
INPUT OFFSET VOLTAGE

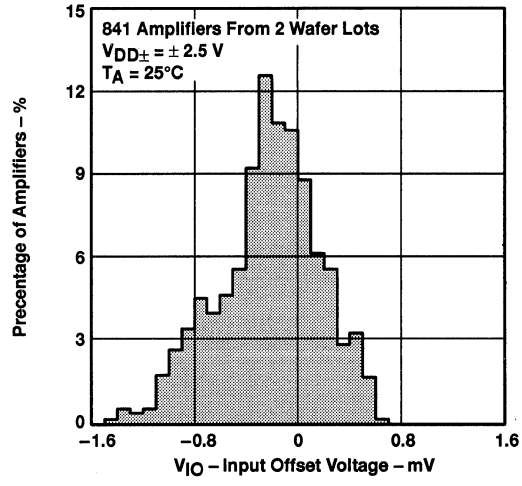


Figure 3

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

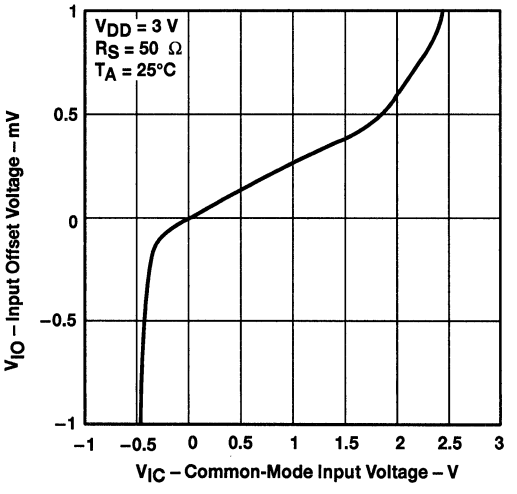


Figure 4

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

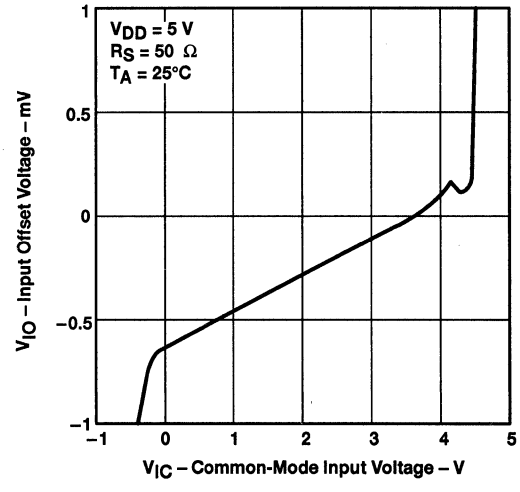


Figure 5

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLV2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

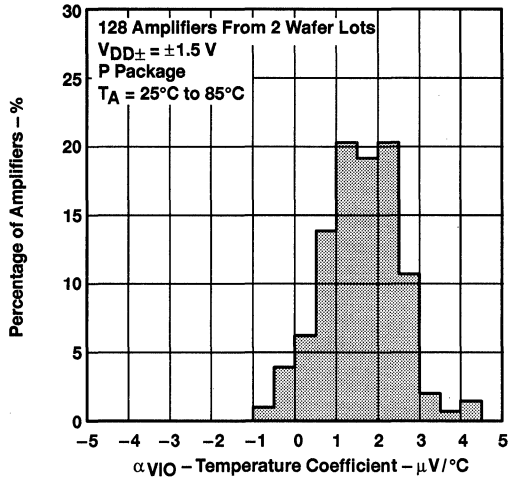


Figure 6

DISTRIBUTION OF TLV2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

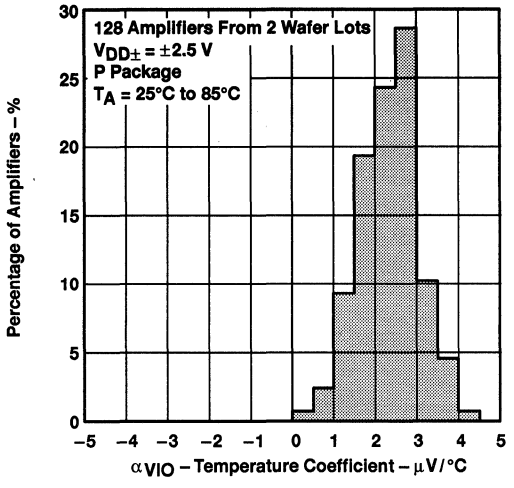


Figure 7

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

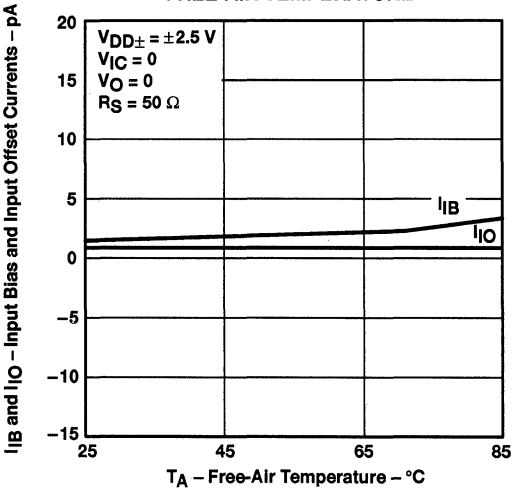


Figure 8

INPUT VOLTAGE vs SUPPLY VOLTAGE

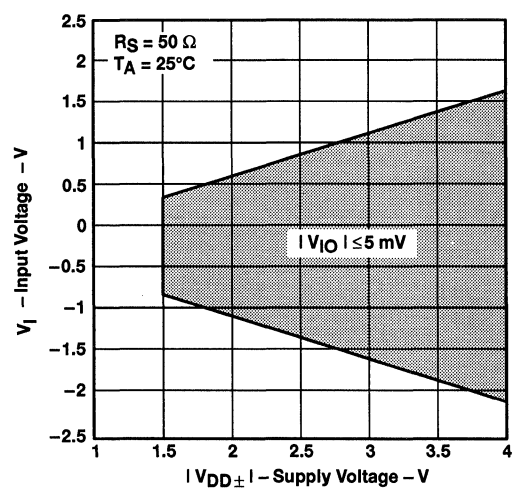


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†‡

INPUT VOLTAGE vs FREE-AIR TEMPERATURE

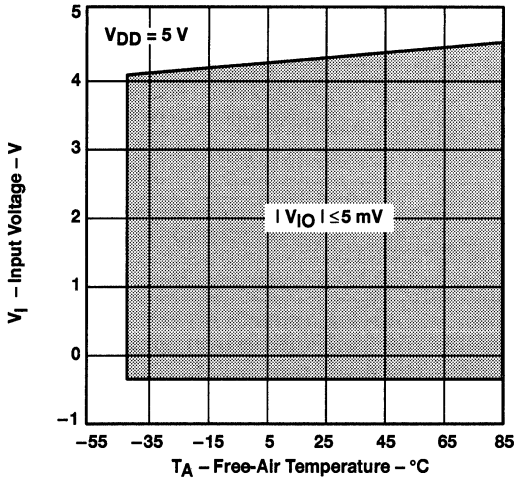


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

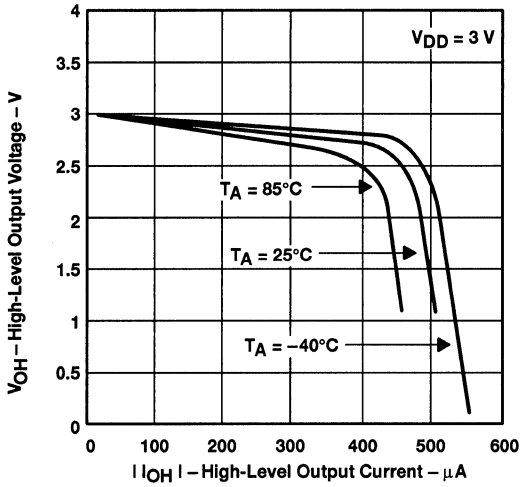


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

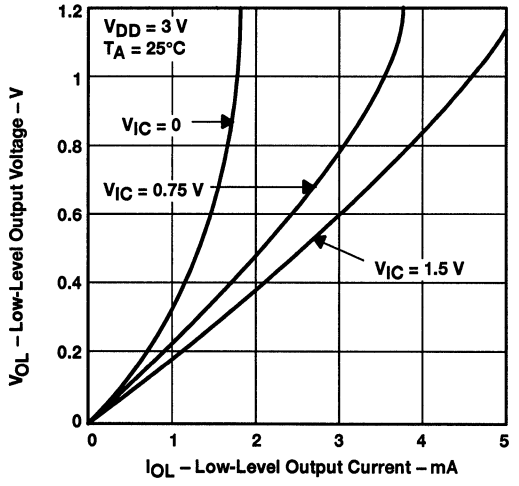


Figure 12

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

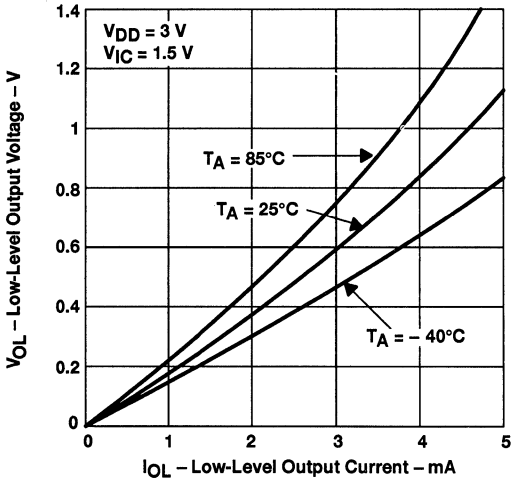


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

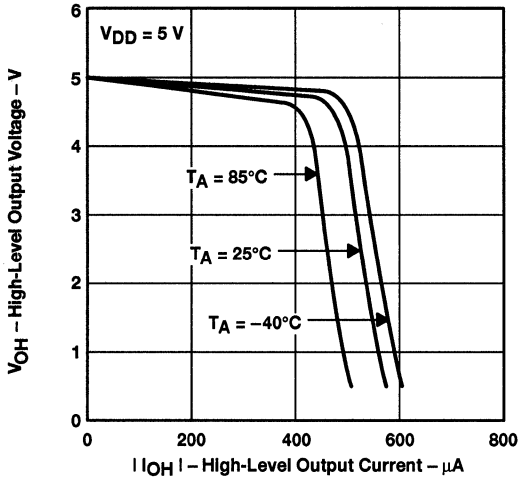


Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

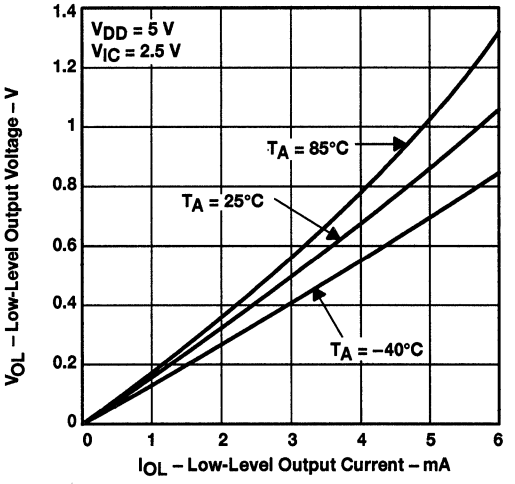


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

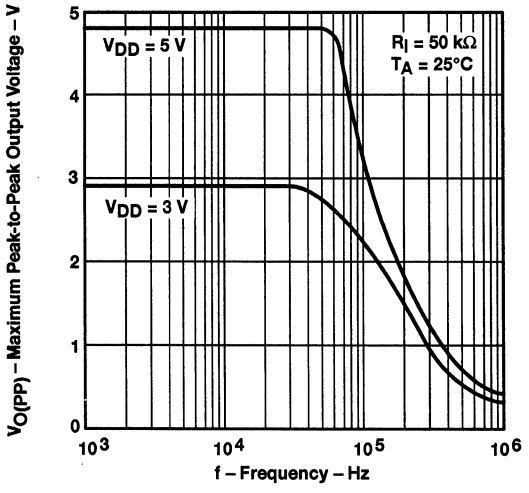


Figure 16

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

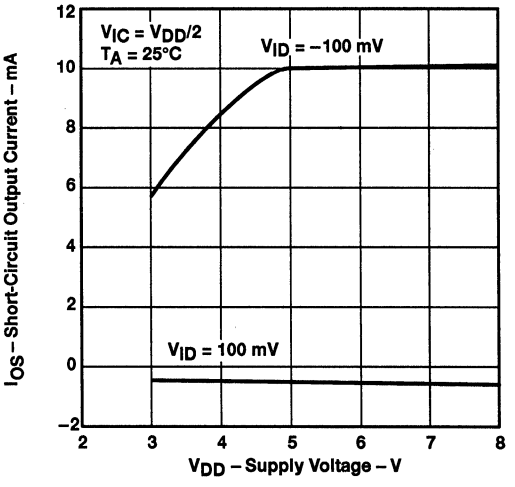


Figure 17

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

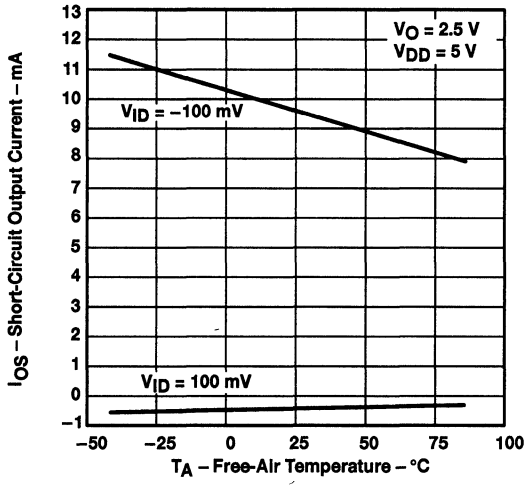


Figure 18

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

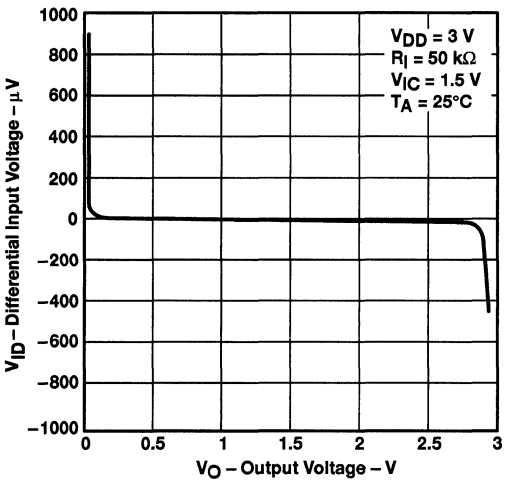


Figure 19

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

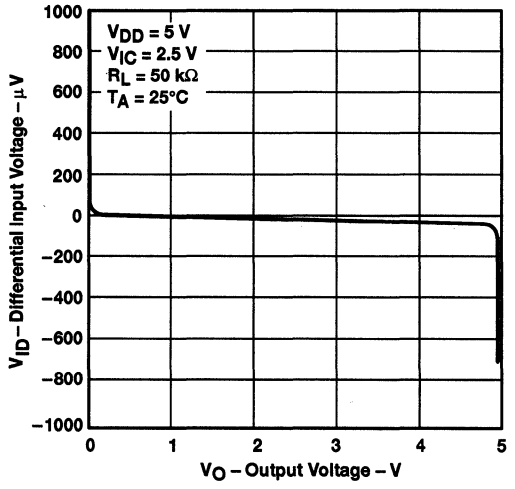


Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

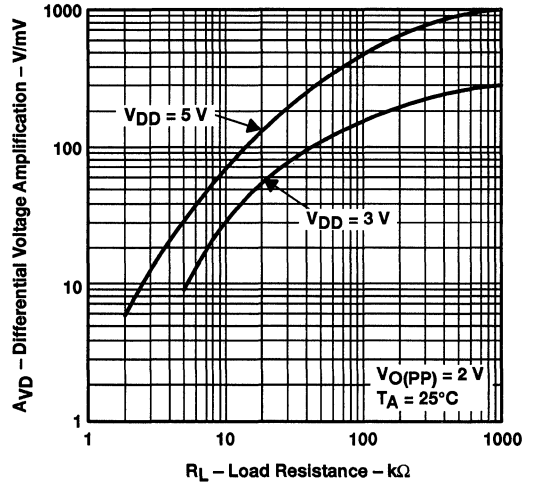


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE† AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

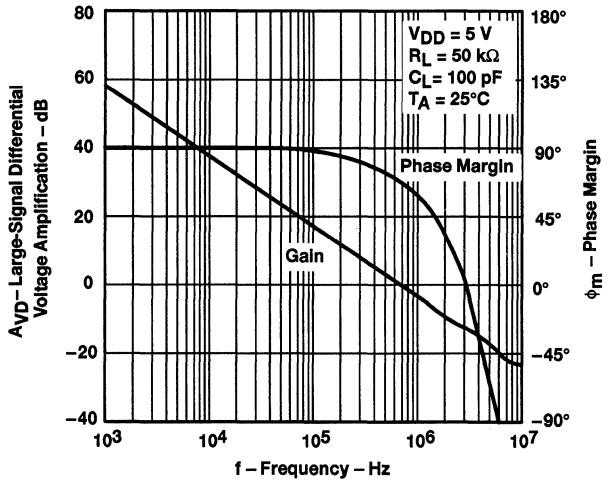


Figure 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

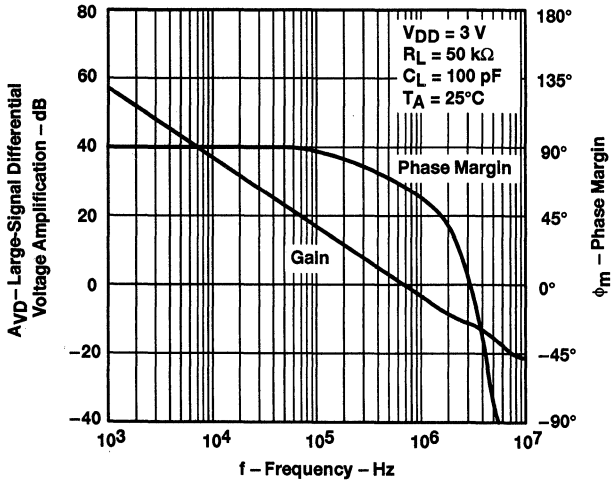


Figure 23

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

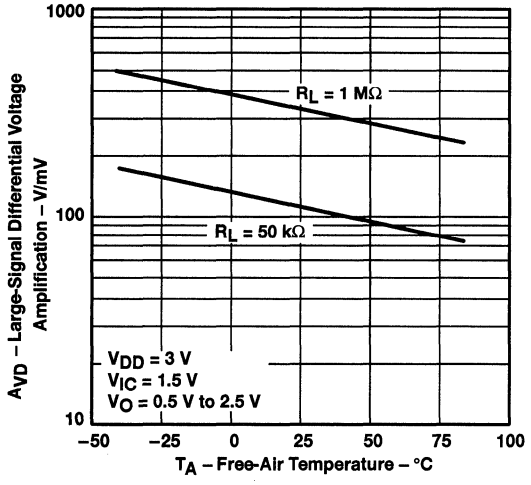


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

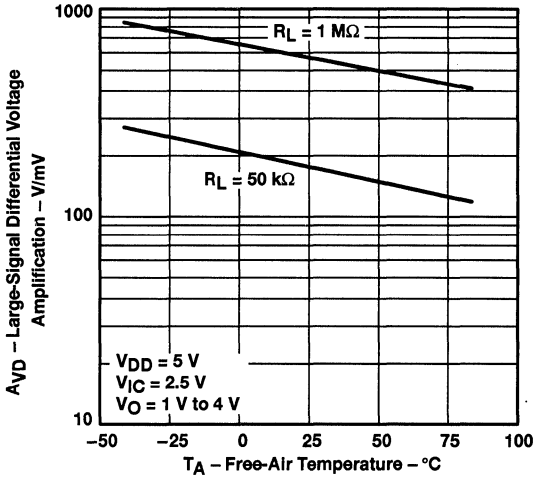


Figure 25

OUTPUT IMPEDANCE vs FREQUENCY

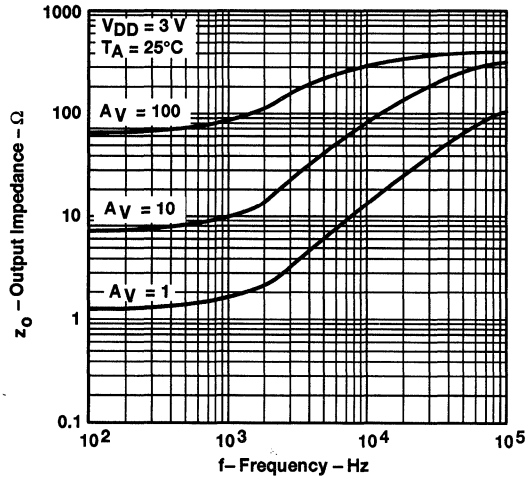


Figure 26

OUTPUT IMPEDANCE vs FREQUENCY

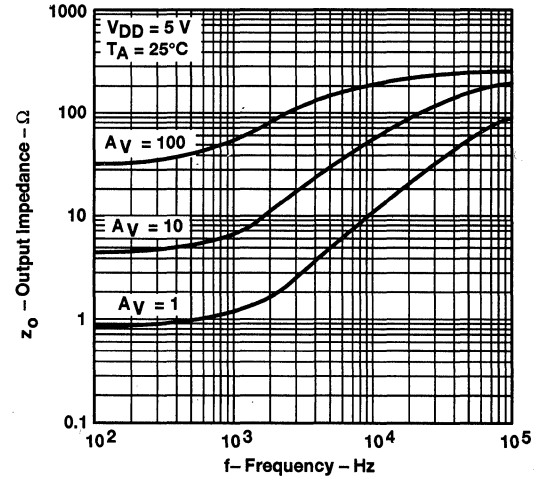


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

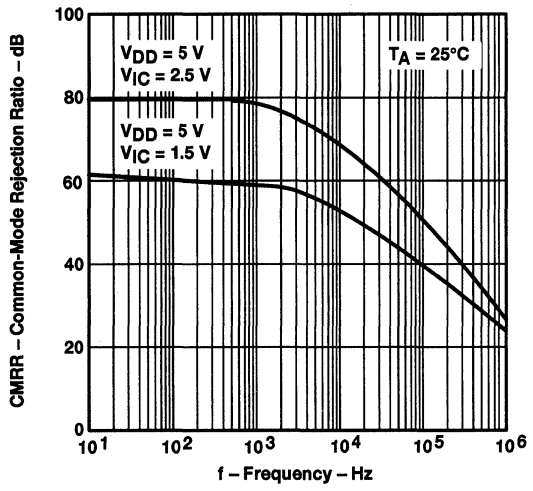


Figure 28

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

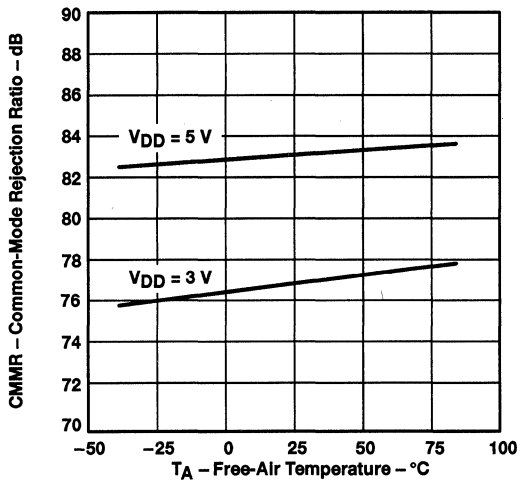


Figure 29

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

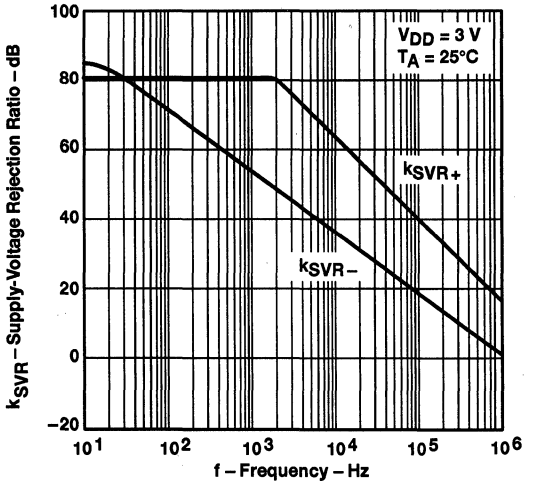


Figure 30

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

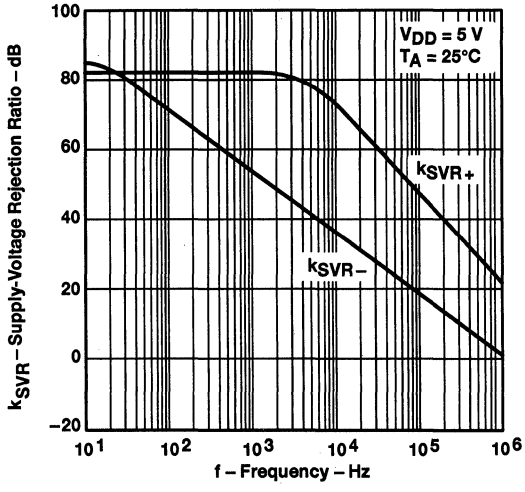


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

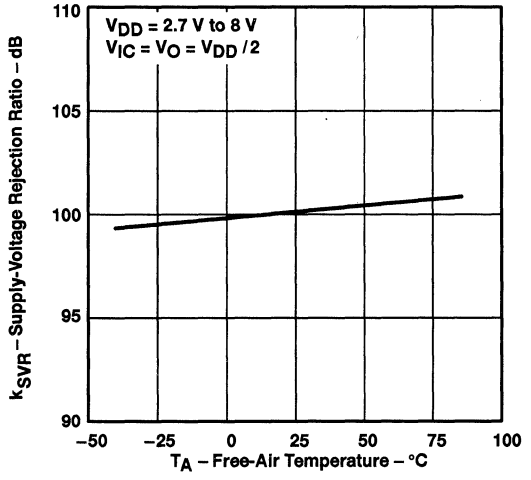


Figure 32

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

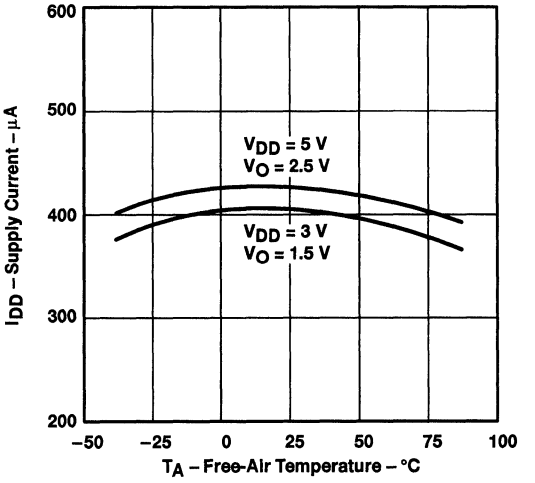


Figure 33

SLEW RATE vs LOAD CAPACITANCE

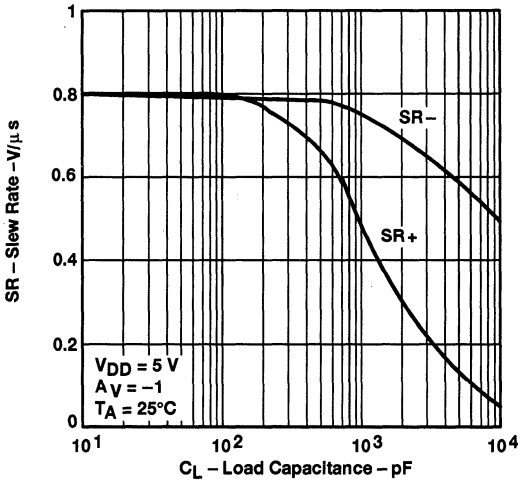


Figure 34

SLEW RATE vs FREE-AIR TEMPERATURE

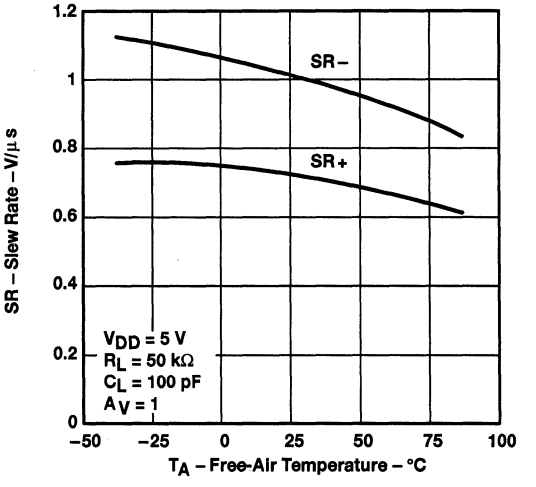


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

INVERTING LARGE-SIGNAL PULSE RESPONSE

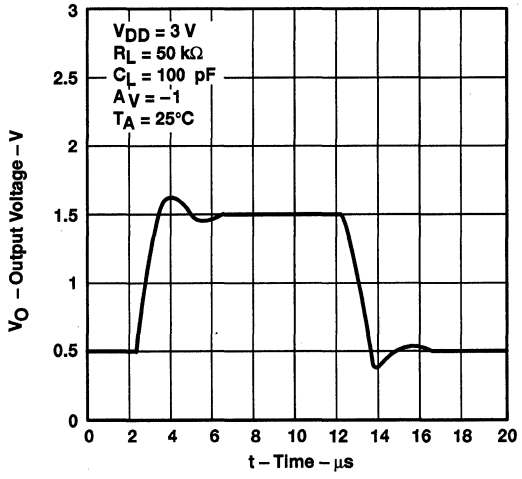


Figure 36

INVERTING LARGE-SIGNAL PULSE RESPONSE

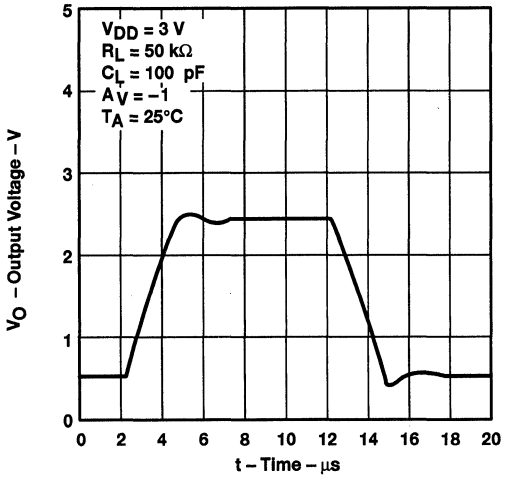


Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

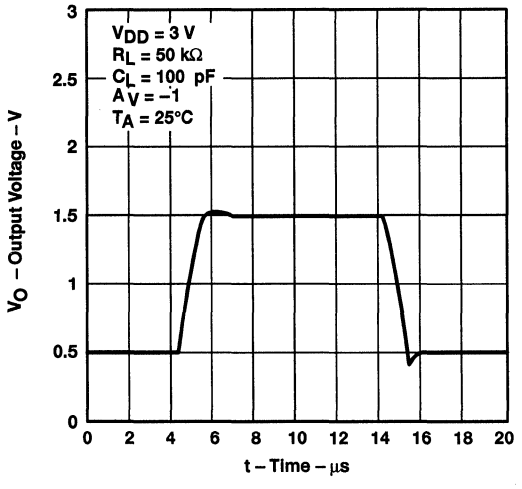


Figure 38

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

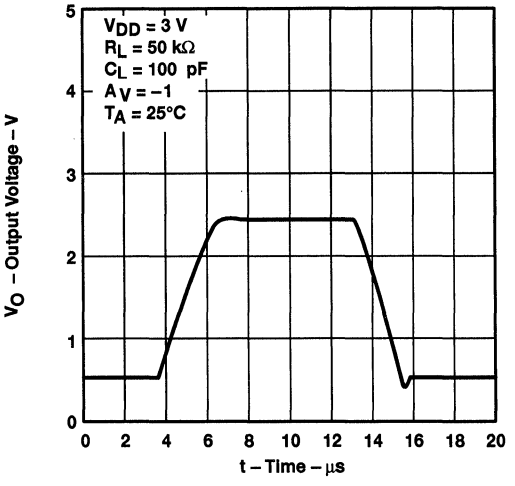


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

INVERTING SMALL-SIGNAL
PULSE RESPONSE

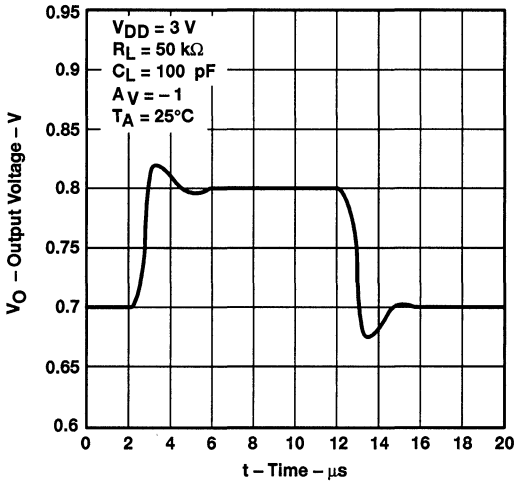


Figure 40

INVERTING SMALL-SIGNAL
PULSE RESPONSE

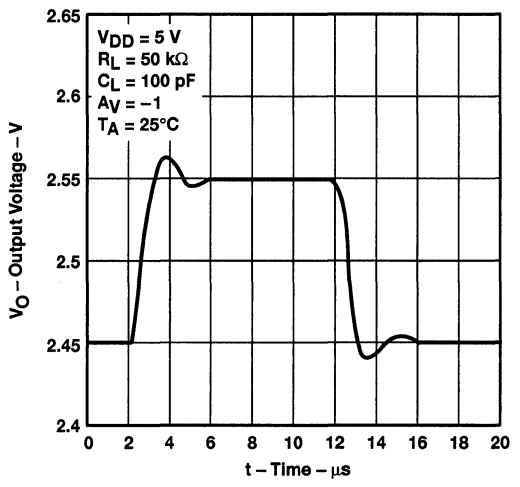


Figure 41

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE

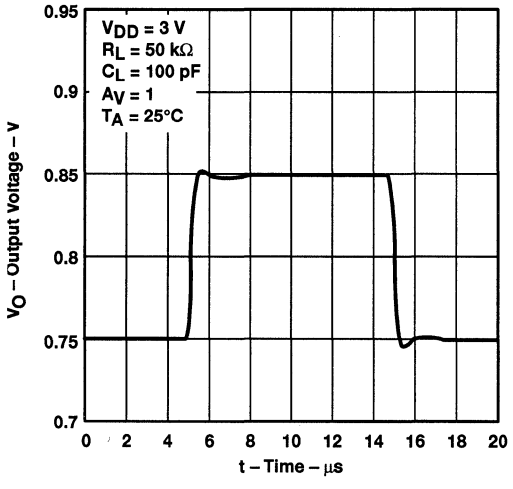


Figure 42

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE

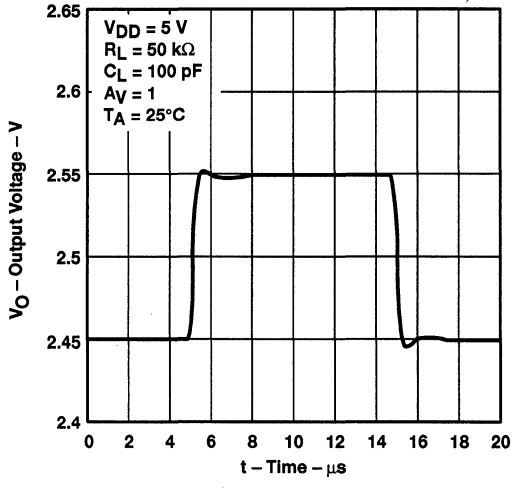


Figure 43

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

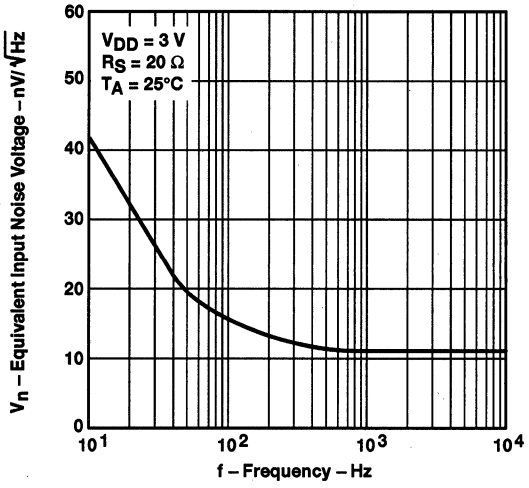


Figure 44

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

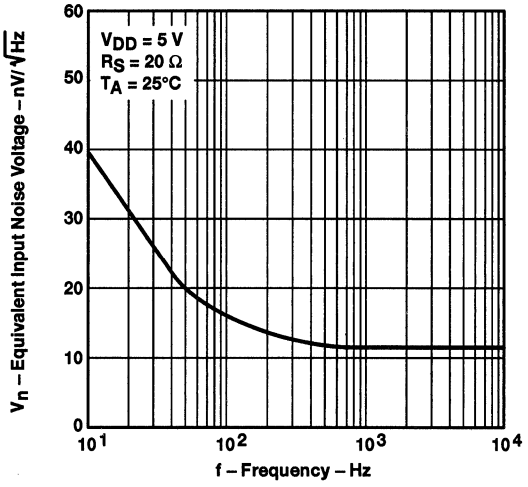


Figure 45

INPUT NOISE VOLTAGE OVER
A 10-SECOND PERIOD

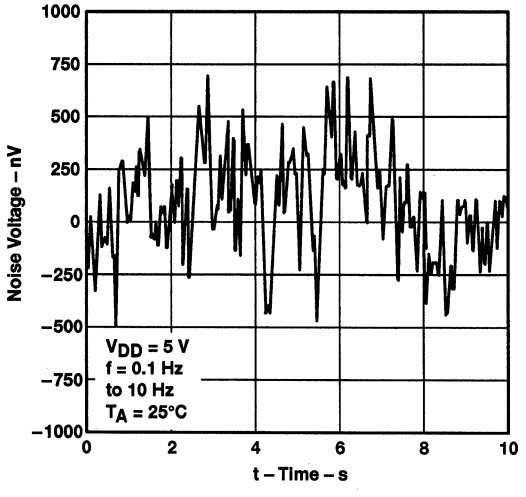


Figure 46

INTEGRATED NOISE VOLTAGE
vs
FREQUENCY

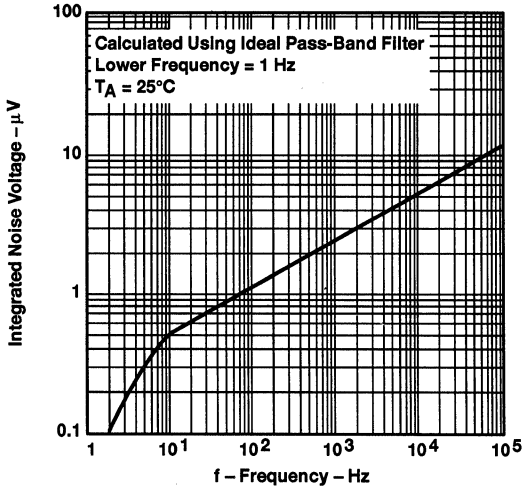


Figure 47

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

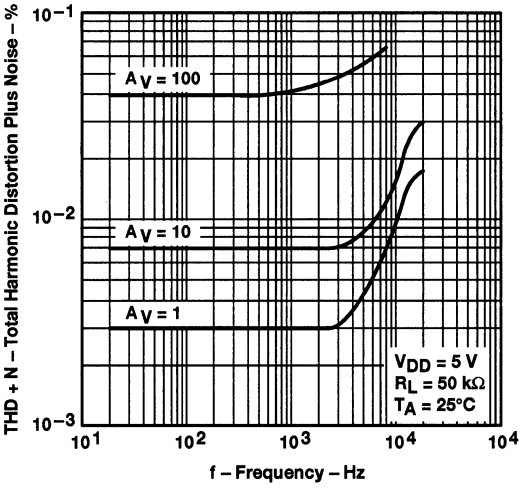


Figure 48

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

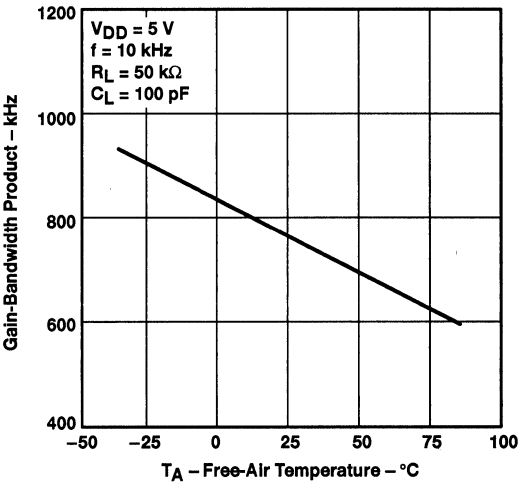


Figure 49

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

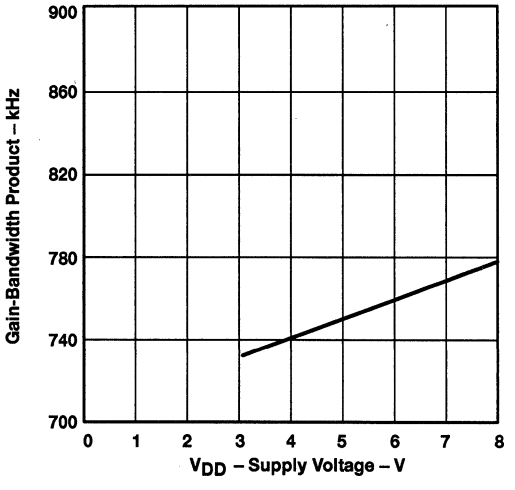


Figure 50

PHASE MARGIN
vs
LOAD CAPACITANCE

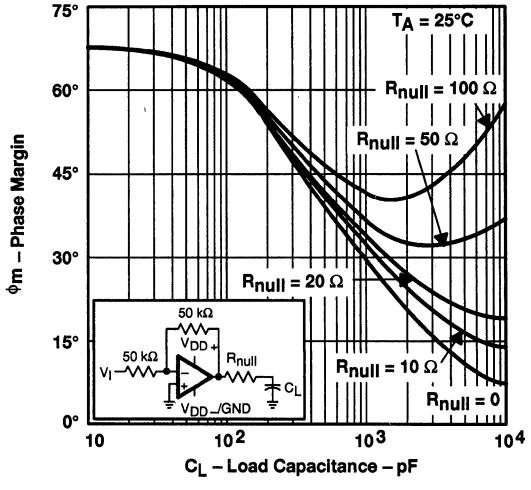


Figure 51

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

GAIN MARGIN
vs
LOAD CAPACITANCE

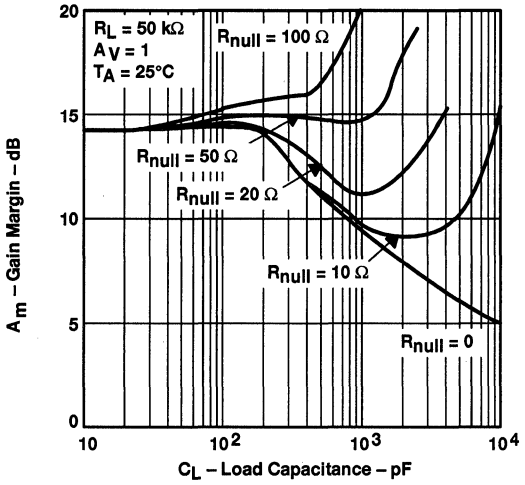


Figure 52

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

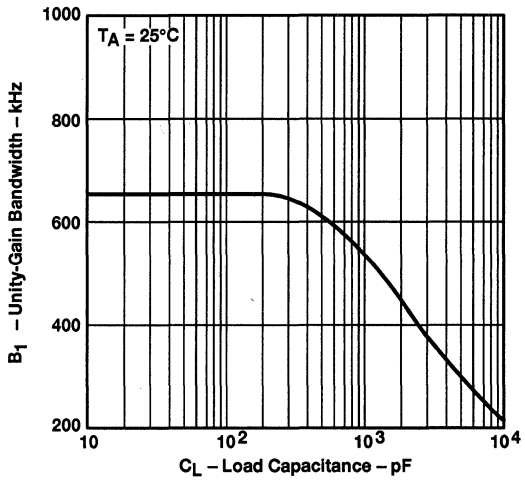
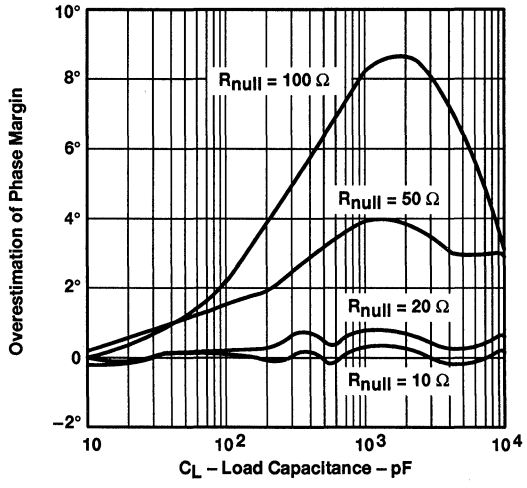


Figure 53

OVERESTIMATION OF PHASE MARGIN†
vs
LOAD CAPACITANCE



† See application information

Figure 54

APPLICATION INFORMATION

loading considerations

The TLV2262 is a low-voltage, low-power version of the TLC2272 with the appropriate design changes relative to the lower power level. The output drive performance to the negative rail for the TLV2262 is similar to the TLC2272 and is capable of driving several milliamperes.

The design topology used for the TLV2262 or the TLV2272 limits the drive to the positive rail to a value very close to the I_{DD} for the amplifier. While the TLV2272 is capable of greater than 1-mA drive from the positive rail, the TLV2262 is capable of only a few hundred microamperes. When designing with lower impedance loads (less than 50 kΩ) with the TLV2262, the lower drive capability to the positive rail needs to be taken into consideration. Although the TLV2262 topology provides lower drive to the positive rail than other high-output-drive rail-to-rail operational amplifiers, it is a more stable topology.

driving large capacitive loads

The TLV2262 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 51 and Figure 52 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see Figure 55) improves the gain and phase margins when driving large capacitive loads. Figure 51 and Figure 52 show the effects of adding series resistances of 10 Ω, 20 Ω, 50 Ω, and 100 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation (1) can be used.

$$\Delta\theta_{m1} = \tan^{-1}\left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L\right) \quad (1)$$

where : $\Delta\theta_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53). To use equation (1), UGBW must be approximated from Figure 53.

Using equation (1) alone overestimates the improvement in phase margin, as illustrated in Figure 54. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation (2).

$$F = \frac{1}{1 + g_m \times R_{null}} \quad (2)$$

where : F = factor reducing frequency of pole
g_m = small-signal output transconductance (typically 4.83×10^{-3} mhos)
R_{null} = output series resistance

APPLICATION INFORMATION

driving large capacitive loads (continued)

For the TLV2262, the pole associated with the load is typically 6 MHz with 100-pF load capacitance. This value varies inversely with C_L: at C_L = 10 pF, use 60 MHz, at C_L = 1000 pF, use 600 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone [equation (1)]. Equation (3) approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the equation (1) to better approximate the improvement in phase margin.

$$\Delta\theta_{m2} = \tan^{-1}\left[\frac{UGBW}{(F \times P_2)}\right] - \tan^{-1}\left(\frac{UGBW}{P_2}\right) \quad (3)$$

where : $\Delta\theta_{m2}$ = reduction in phase margin

UGBW = unity-gain bandwidth frequency

F = factor from equation (2)

P_2 = unadjusted pole (60 MHz @ 10 pF, 6 MHz @100 pF, etc.)

Using these equations with Figure 54 and Figure 55 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.

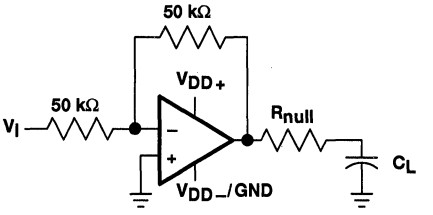


Figure 55. Series-Resistance Circuit

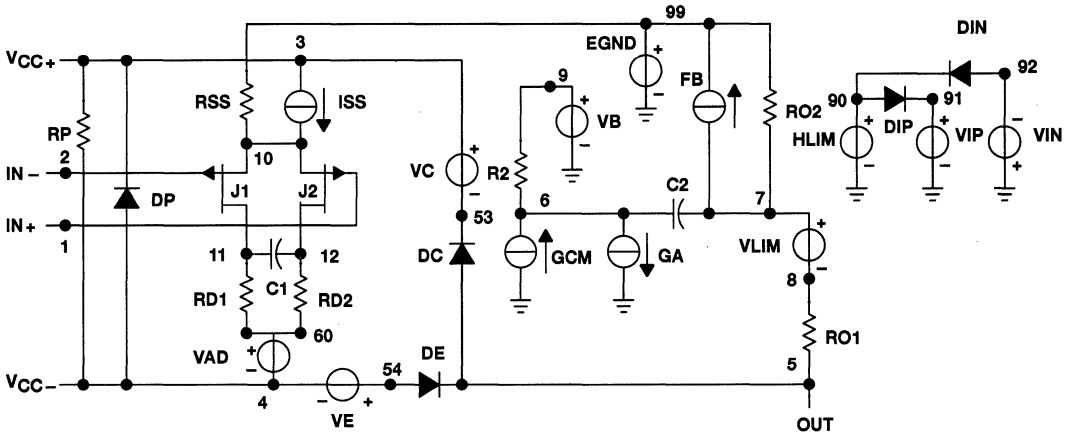
APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using *PSpice*® *Parts*™ model generation software. The Boyle macromodel and subcircuit in Figure 56 are generated using the TLV2262 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Intergrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLV2262 1 2 3 4 5
C1      11     12     5.004E–12
C2      6      7      20.00E–12
DC      5      53     DX
DE      54     5      DX
DLP     90     91     DX
DLN     92     90     DX
DP      4      3      DX
EGND    99     0      POLY (2) (3,0) (4,0) 0 .5 .5
FB      7      99     POLY (5) VB VC VE VLP
+ VLN 0 5.89E6 –10E6 10E6 10E6 –10E6
GA      6      0      11     12 62.83E–6
GCM     0      6      10     99 22.34E–9
ISS     3      10     DC 11.00E–6
HLIM    90     0      VLIM 1K
J1      11     2      10 JX
J2      12     1      10 JX
R2      6      9      100.0E3
RD1     60     11     15.92E3
RD2     60     12     15.92E3
R01     8      5      135
R02     7      99     135
RP      3      4      15.87E3
RSS     10     99     18.18E6
VAD     60     4      –.5
VB      9      0      DC 0
VC      3      53     DC .6
VE      54     4      DC .6
VLIM    7      8      DC 0
VLP     91     0      DC 0
VLN     0      92     DC 9.4
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=717.8E–6
+ VTO=–.04)
.ENDS
```

Figure 56. Boyle Macromodel and Subcircuit

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Parts is a trademark of MicroSim Corporation.

available features

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 12 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Low Power . . . 1 mA Max**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage 950 μV Max at T_A = 25°C**
- **Wide Supply Voltage Range 2.7 V to 8 V**
- **Macromodel Included**

description

The TLV2264 and TLV2264A are quad operational amplifiers manufactured using Texas Instruments Advanced LinCMOS™ process. These devices are optimized and fully specified for single-supply 3-V and 5-V operation. For this low-voltage operation combined with μpower dissipation levels, the input noise voltage performance has been dramatically improved using optimized design techniques for CMOS-type amplifiers. Another added benefit is that these amplifiers exhibit rail-to-rail output swing. Figure 1 graphically depicts the high-level output voltage for different levels of output current for a 3-V single supply. The output dynamic range can be extended using the TLV2264 with loads referenced midway between the rails. The common-mode input voltage range is wider than typical standard CMOS-type amplifiers. To take advantage of this improvement in performance and to make this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ± 5 mV, allowing a minimum of 0 to 2-V common-mode input voltage range for a 3-V supply. Furthermore, at 200 μA (typical) of supply current per amplifier, the TLV2264 family can achieve input offset voltage levels as low as 950 μV outperforming existing CMOS amplifiers. The Advanced LinCMOS process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input-impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

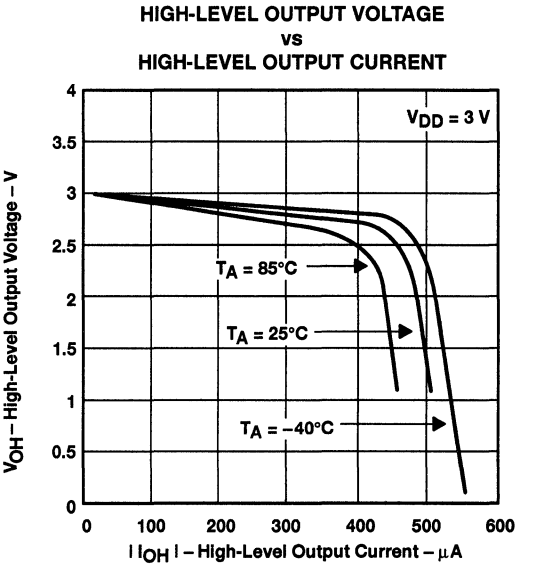


Figure 1

AVAILABLE OPTIONS

PACKAGED DEVICES					CHIP FORM (Y)
T_A	V_{IO}max AT 25°C	SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
–40°C to 85°C	950 μV 2.5 mV	TLV2264AID TLV2264ID	TLV2264AIN TLV2264IN	TLV2264AIPWLE —	TLV2264Y

The D packages are available taped and reeled. Add R suffix to device type, (e.g., TLV2264IDR).
The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

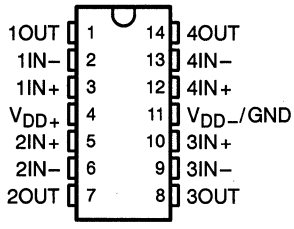
Advanced LinCMOS™ is a trademark of Texas Instruments Incorporated.

description (continued)

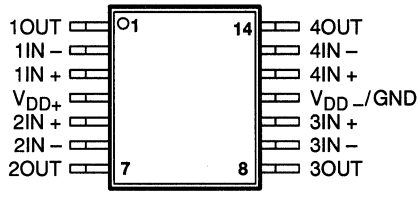
The TLV2264 and TLV2264A, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources such as piezoelectric transducers. Because of the low power-dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes these devices great choices when interfacing directly to analog-to-digital converters (ADCs). All of these features, combined with its temperature performance make the TLV2264 family ideal for remote pressure sensors, temperature control, active VR sensors, accelerometers, hand-held metering, and many other applications.

The device inputs and outputs are designed to withstand a 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD+} supply-line transients under powered conditions. Transients of greater than 20 V can trigger the ESD-protection structure, inducing a low-impedance path to V_{DD-}/GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so could result in a latched condition and device failure.

D OR N PACKAGE
(TOP VIEW)



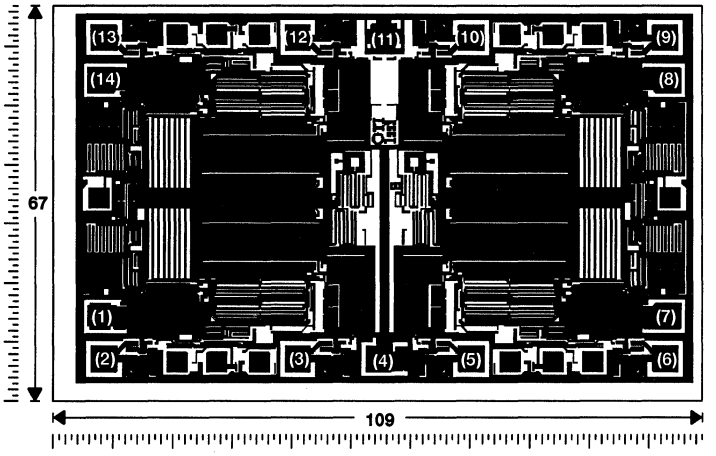
PW PACKAGE
(TOP VIEW)

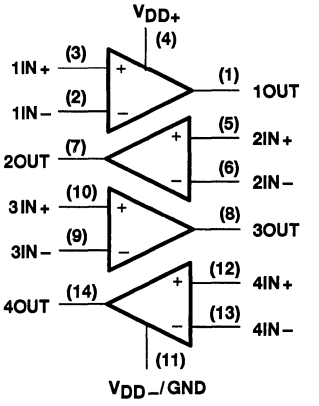


TLV2264Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2264. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

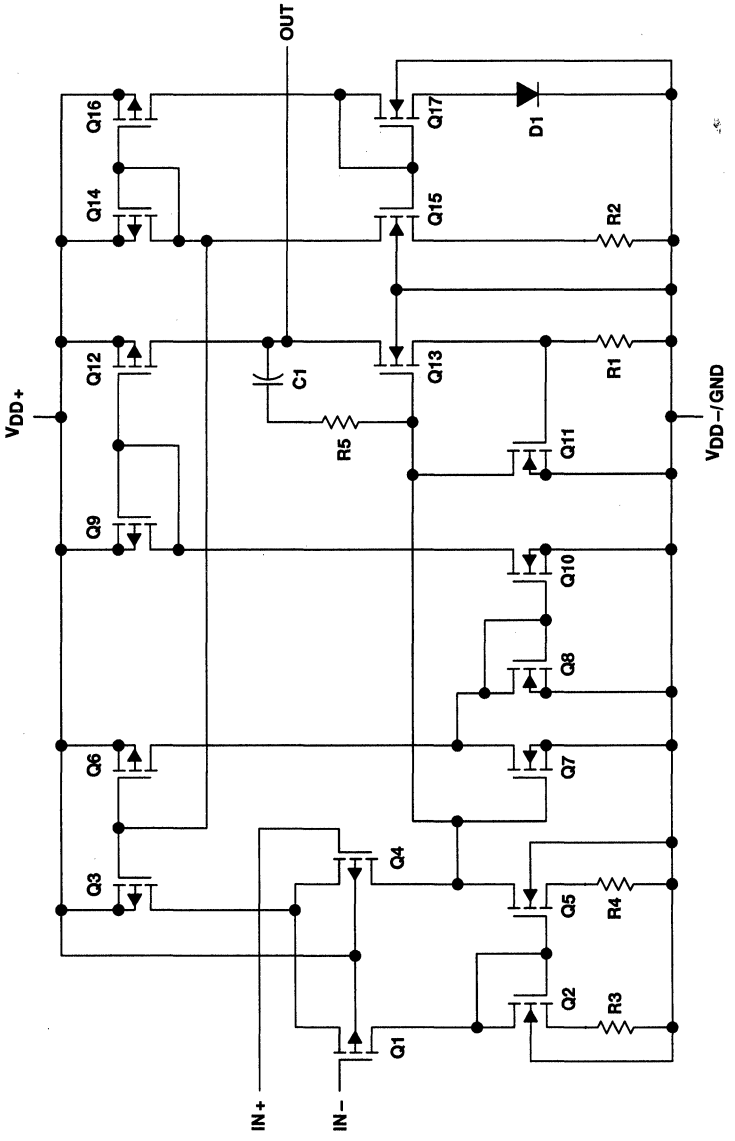
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	76
Diodes	18
Resistors	52
Capacitors	6

† Includes all amplifiers, ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... $\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1) ..... V_{DD-} −0.3 V to V_{DD+}
Input current, I_I (each input) ..... ±5 mA
Output current, I_O ..... ±50 mA
Total current into V_{DD+} ..... ±50 mA
Total current out of V_{DD-} ..... ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows if input is brought below V_{DD-} − 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW
PW	700 mW	5.6 mW/°C	364 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{DD\pm}$ (see Note 1)	2.7	8	V
Input voltage range, V_I	V_{DD-}	V_{DD+} −1.3	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} −1.3	V
Operating free-air temperature, T_A	−40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-}.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2264			TLV2264A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$5 mV	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		2.99			2.99		V
		I_{OH} = −100 μA		25°C	2.85			2.85			
				Full range	2.825			2.825			
		I_{OH} = −200 μA		25°C	2.7			2.7			
				Full range	2.65			2.65			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 μA	25°C		10			10		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 μA	25°C		100			100		
				Full range			150			150	
		V_{IC} = 1.5 V,	I_{OL} = 1 mA	25°C		200			200		
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 50 kΩ‡	25°C	60	100		60	100		V/mV
				Full range	30			30			
			R_L = 1 MΩ‡	25°C		100			100		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		270			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, R_S = 50 Ω	V_O = 1.5 V,	25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, No load,	V_{IC} = V_{DD}/2	25°C	80	95		80	100		dB
				Full range	80			80			
I_{DD}	Supply current (four amplifiers)	V_O = 1.5 V,	No load	25°C		0.8	1		0.8	1	mA
				Full range			1			1	

† Full range is – 40°C to 85°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2264			TLV2264A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.7 V to 1.7 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.6			0.6		μV
		f = 0.1 Hz to 10 Hz		25°C		1			1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.03%			0.03%		
			A_V = 10			0.05%			0.05%		
	Gain-bandwidth product	f = 1 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.67			0.67		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		300			300		kHz
t_s	Settling time	A_V = −1, Step = 1 V to 2 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		5.6			5.6		μs
			To 0.01%			12.5			12.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		61°			61°		
	Gain margin			25°C		14			14		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 1.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2264			TLV2264A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD}\pm$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	$|V_{IO}| \le$5 mV,	R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −100 μA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_{OH} = −200 μA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.6			4.6			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	170		80	170		V/mV
				Full range	55			55			
			R_L = 1 MΩ‡	25°C		550			550		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, No load,	V_{IC} = V_{DD}/2	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V,	No load	25°C		0.8	1		0.8	1	mA
				Full range			1			1	

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2264			TLV2264A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.4 V to 2.6 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°			63°		
	Gain margin			25°C		14			14		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V

electrical characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV2264Y MIN	TLV2264Y TYP	TLV2264Y MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω			300	2500	μV
I_{IO}	Input offset current					0.5	150	pA
I_{IB}	Input bias current					1	150	pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	R_S = 50 Ω		0 to 2	−0.3 to 2.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA				2.99		V
		I_{OH} = −200 μA			2.7	2.75		
V_{OL}	Low-level output voltage	V_{IC} = 0,	I_{OL} = 50 μA			10		V
		V_{IC} = 0,	I_{OL} = 500 μA			100	125	
		V_{IC} = 0,	I_{OL} = 1 mA			200	250	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V	R_L = 50 kΩ†		60	100		V/mV
			R_L = 1 MΩ†			100		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V,	V_O = 0,	R_S = 50 Ω	65	77		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V,	No load,	V_{IC} = 0	80	100		dB
I_{DD}	Supply current (four amplifiers)	V_O = 0,	No load			0.8	1	mA

† Referenced to 1.5 V

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV2264Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω		300	2500	μV
I_{IO}	Input offset current				0.5	150	pA
I_{IB}	Input bias current				1	150	pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	R_S = 50 Ω	0 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA			4.99		V
		I_{OH} = −100 μA		4.85	4.94		
		I_{OH} = −200 μA		4.7	4.85		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA		0.09	0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA		0.2	0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ†	80	170		V/mV
			R_L = 1 MΩ†		550		
r_{id}	Differential input resistance				10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10		240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V,	V_O = 2.5 V, R_S = 50 Ω	70	83		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V,	No load, V_{IC} = V_{DD}/2	80	95		dB
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V,	No load		0.8	1	mA

† Referenced to 2.5 V

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	2, 3
		vs Common-mode voltage	4, 5
α_{VIO}	Input offset voltage temperature coefficient	Distribution	6, 7
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature	8
V_I	Input voltage	vs Supply voltage	9
		vs Free-air temperature	10
V_{OH}	High-level output voltage	vs High-level output current	11, 14
V_{OL}	Low-level output voltage	vs Low-level output current	12, 13, 15
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	16
I_{OS}	Short-circuit output current	vs Supply voltage	17
		vs Free-air temperature	18
V_{ID}	Differential input voltage	vs Output voltage	19, 20
A_{VD}	Differential voltage amplification	vs Load resistance	21
		vs Frequency	22, 23
		vs Free-air temperature	24, 25
z_o	Output impedance	vs Frequency	26, 27
CMRR	Common-mode rejection ratio	vs Frequency	28
		vs Free-air temperature	29
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	30, 31
		vs Free-air temperature	32
I_{DD}	Supply current	vs Free-air temperature	33
SR	Slew rate	vs Load capacitance	34
		vs Free-air temperature	35
V_O	Large-signal pulse response	vs Time	36, 37, 38, 39
V_O	Small-signal pulse response	vs Time	40, 41, 42, 43
V_n	Equivalent input noise voltage	vs Frequency	44, 45
	Noise voltage (referred to input)	Over a 10-second period	46
	Integrated noise voltage	vs Frequency	47
THD + N	Total harmonic distortion plus noise	vs Frequency	48
	Gain-bandwidth product	vs Free-air temperature	49
		vs Supply voltage	50
ϕ_m	Phase margin	vs Frequency	22, 23
		vs Load capacitance	51
	Gain margin	vs Load capacitance	52
B_1	Unity-gain bandwidth	vs Load capacitance	53
	Overestimation of phase margin	vs Load capacitance	54

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLV2264
INPUT OFFSET VOLTAGE

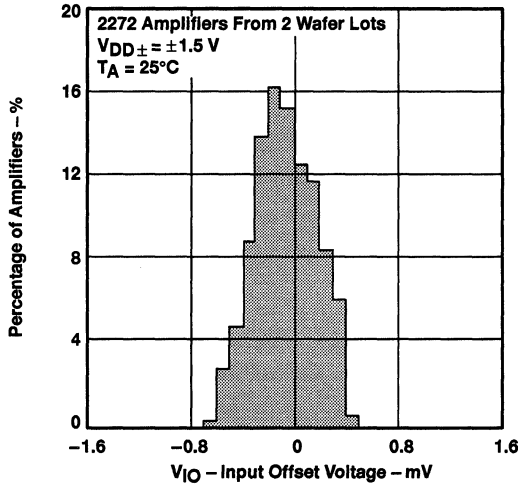


Figure 2

DISTRIBUTION OF TLV2264
INPUT OFFSET VOLTAGE

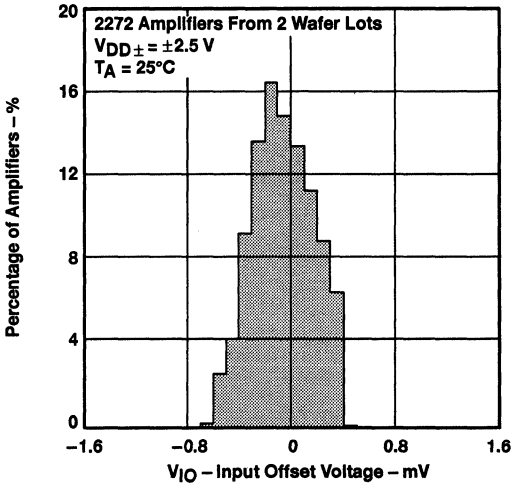


Figure 3

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

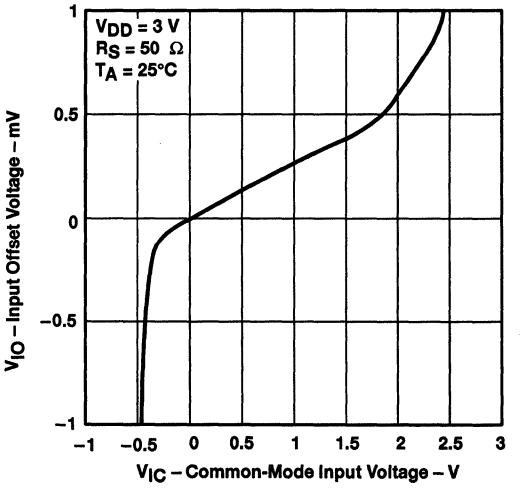


Figure 4

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

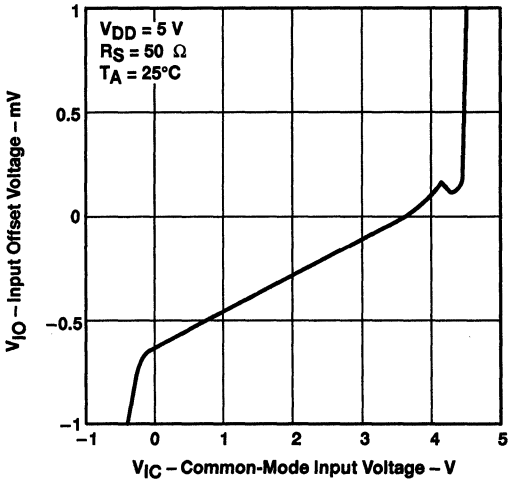


Figure 5

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLV2264 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

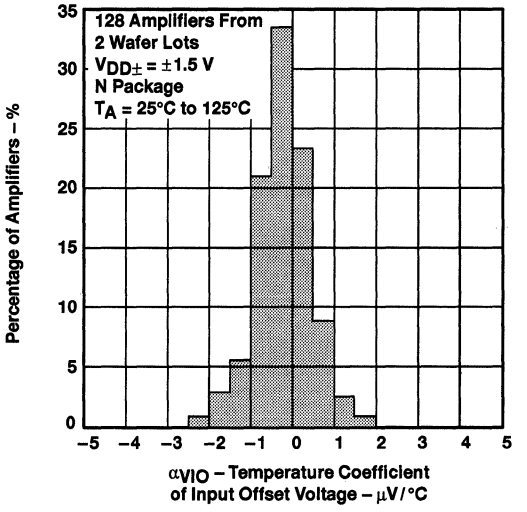


Figure 6

DISTRIBUTION OF TLV2264 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

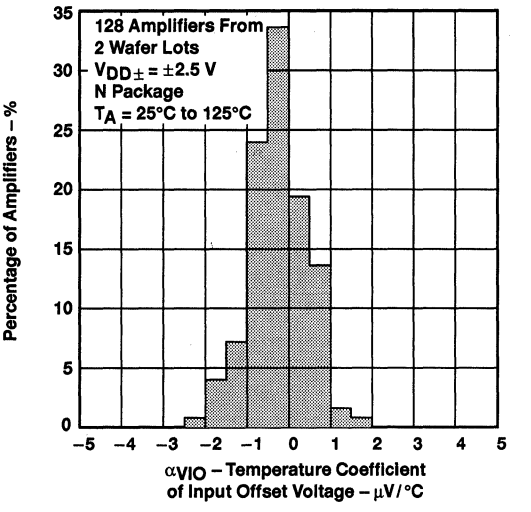


Figure 7

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

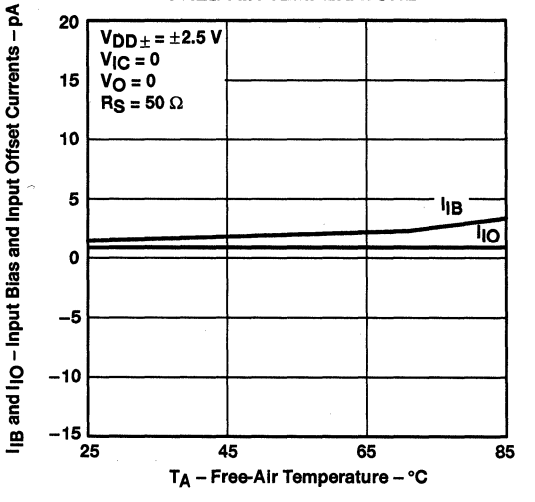


Figure 8

INPUT VOLTAGE vs SUPPLY VOLTAGE

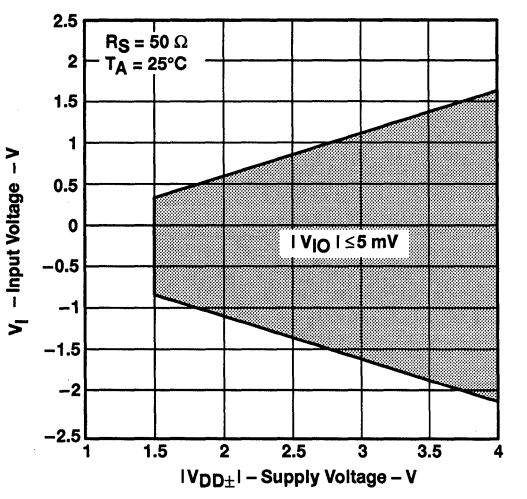


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†‡

INPUT VOLTAGE vs FREE-AIR TEMPERATURE

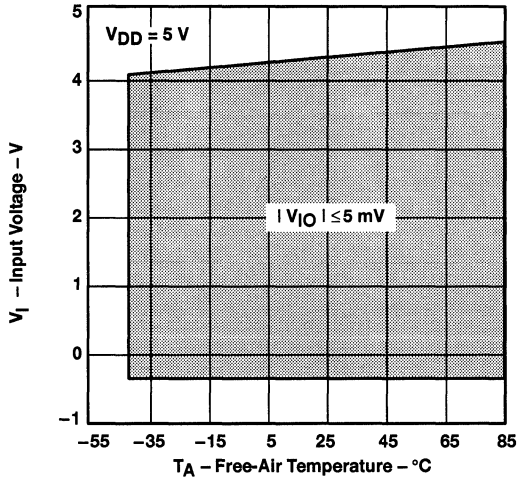


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

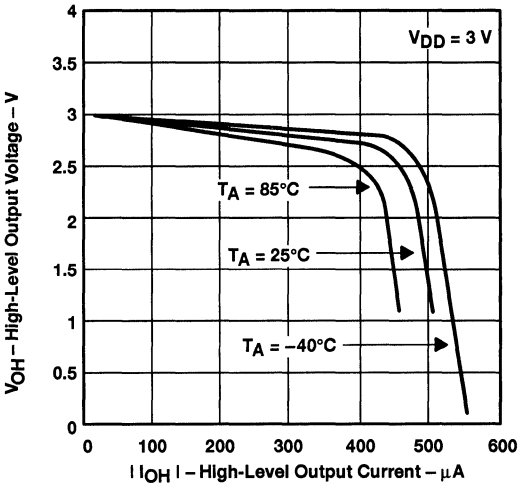


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

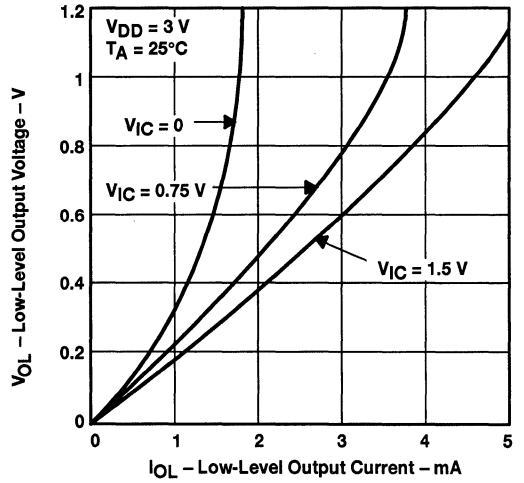


Figure 12

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

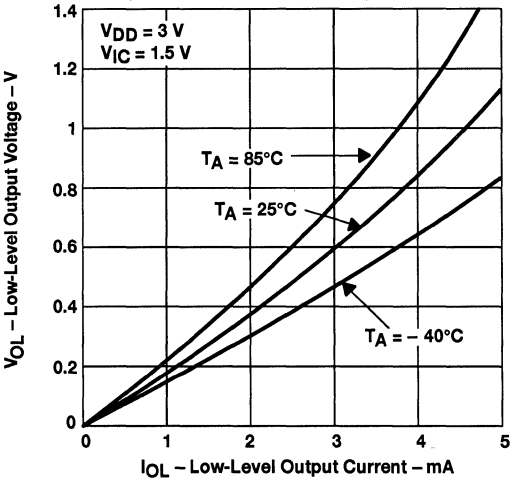


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

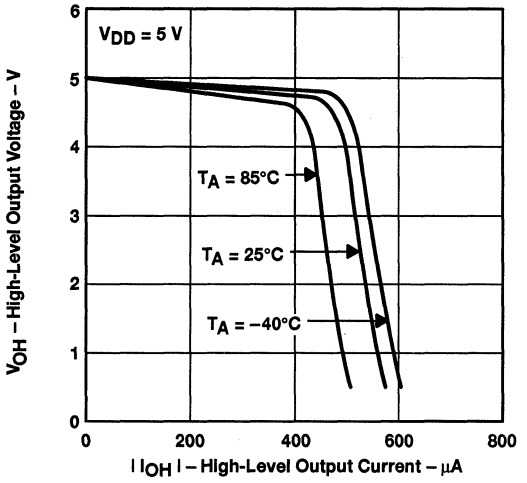


Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

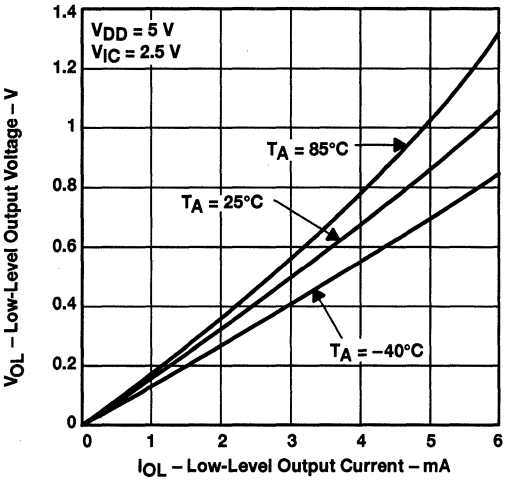


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

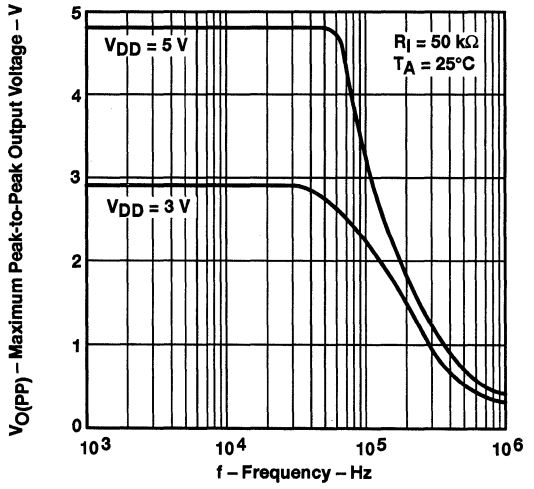


Figure 16

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

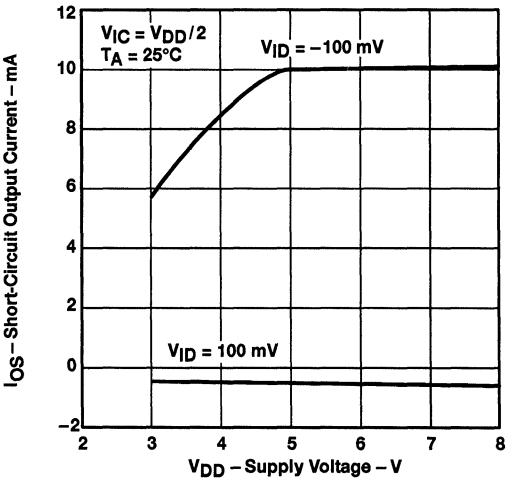


Figure 17

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

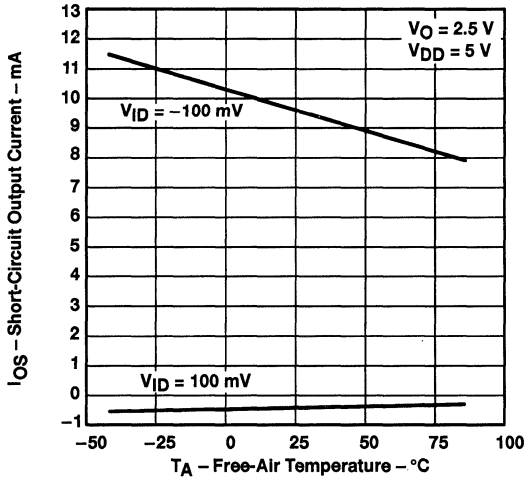


Figure 18

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

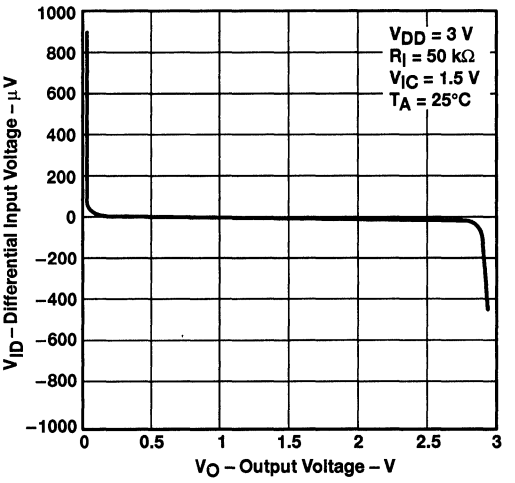


Figure 19

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

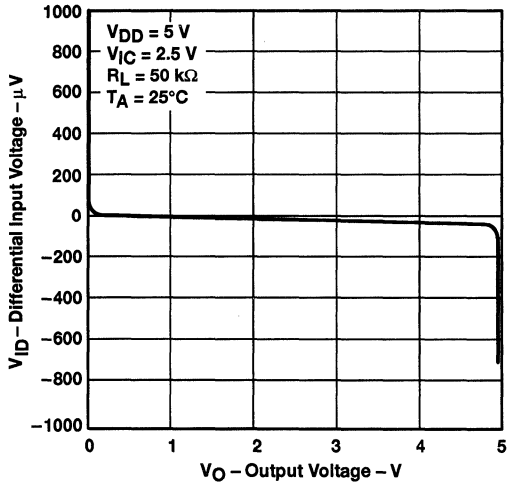


Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

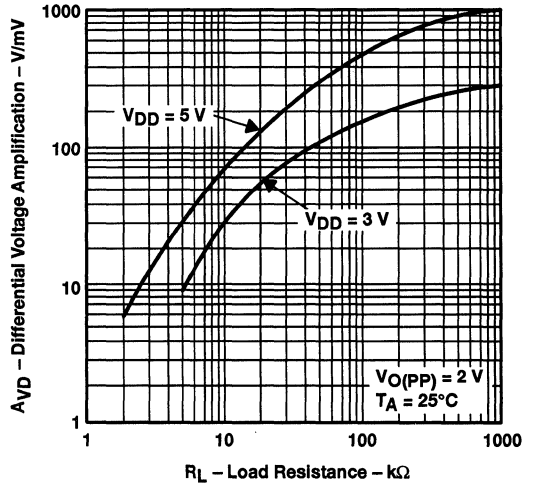


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE† AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

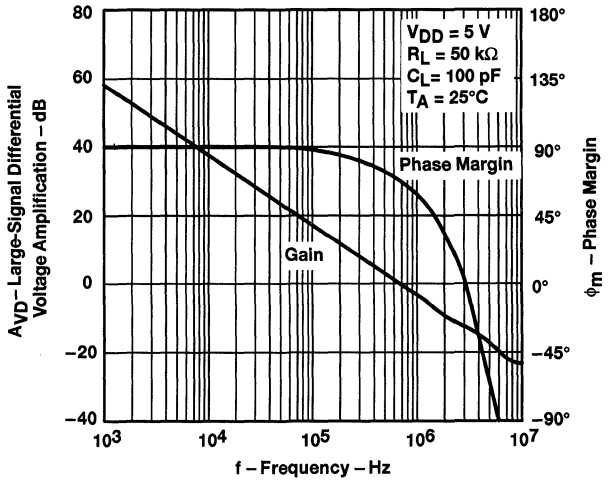


Figure 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

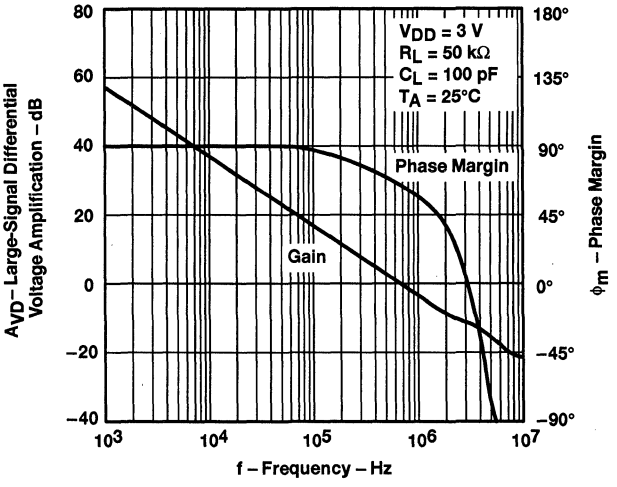


Figure 23

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

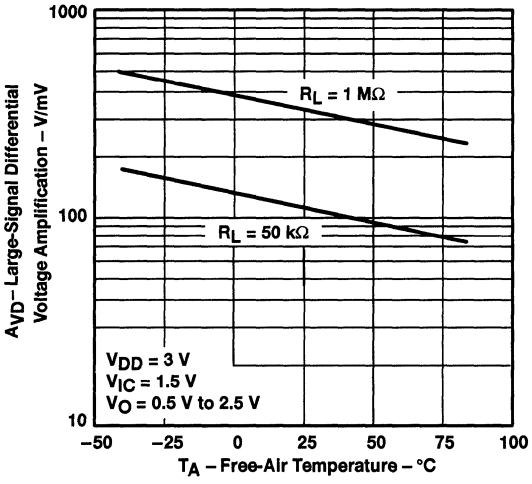


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

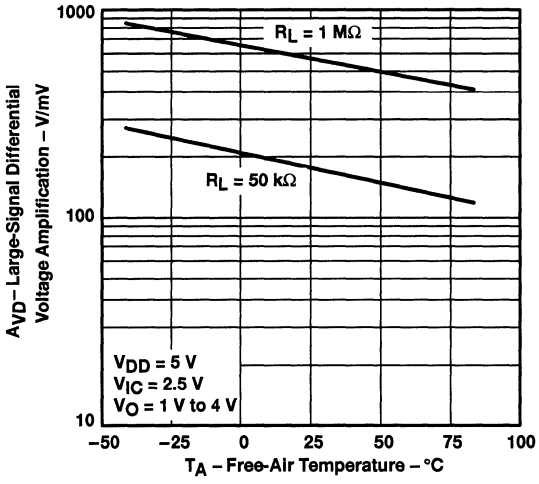


Figure 25

OUTPUT IMPEDANCE vs FREQUENCY

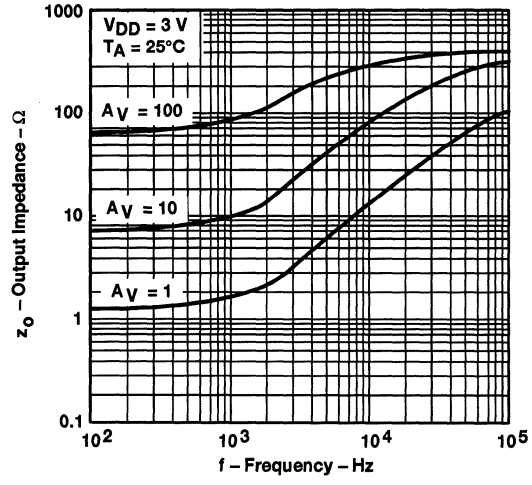


Figure 26

OUTPUT IMPEDANCE vs FREQUENCY

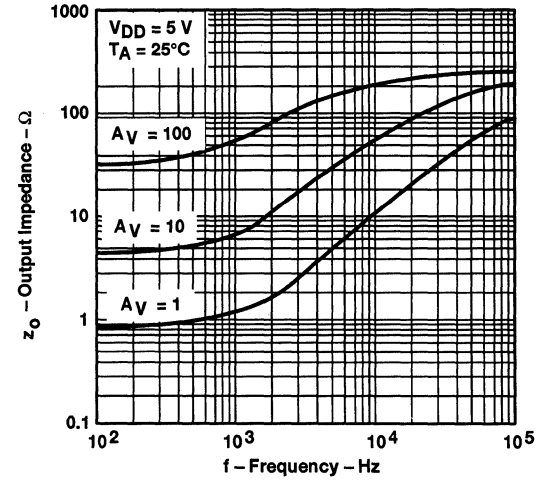


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

COMMON-MODE REJECTION RATIO vs FREQUENCY

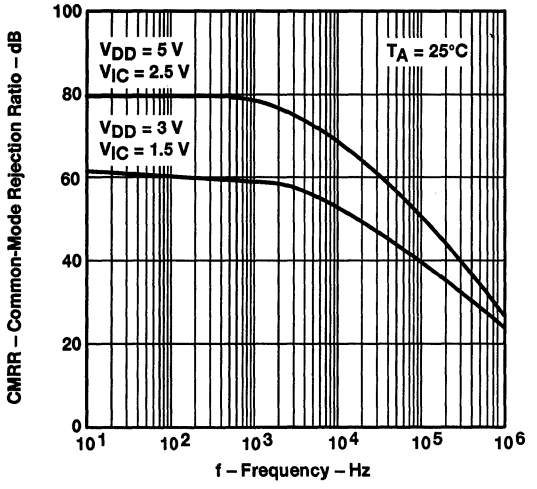


Figure 28

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

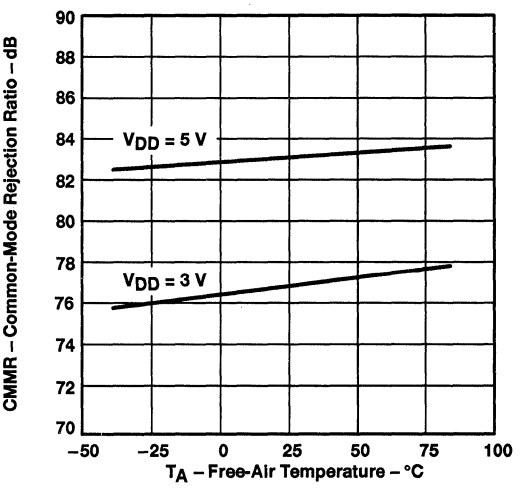


Figure 29

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

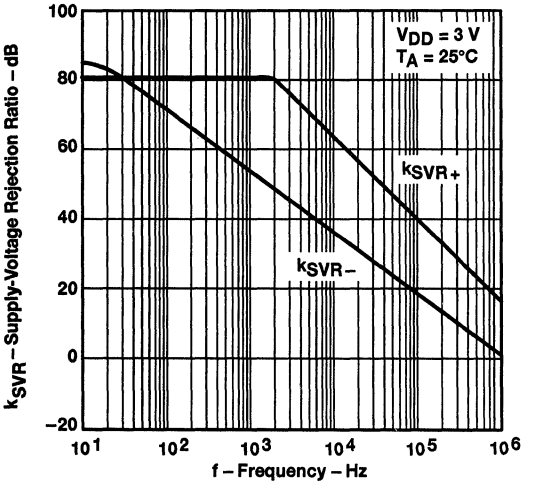


Figure 30

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

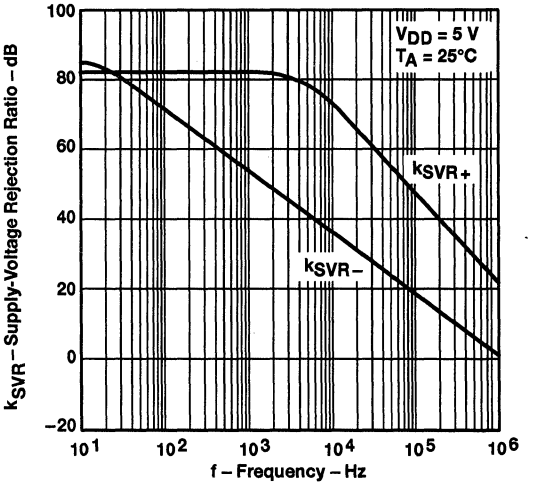


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

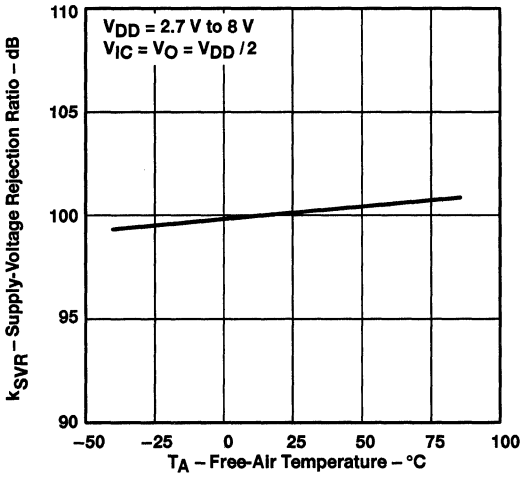


Figure 32

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

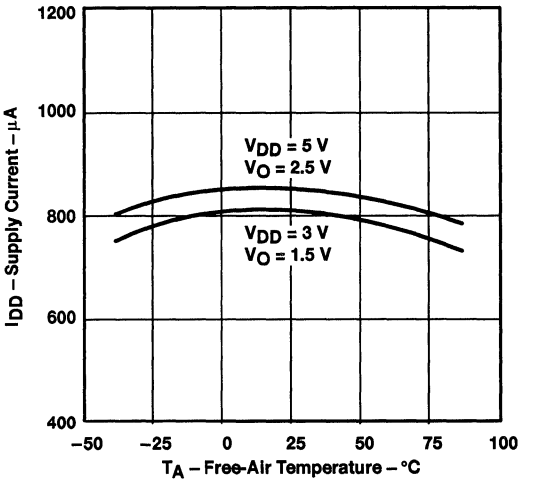


Figure 33

SLEW RATE vs LOAD CAPACITANCE

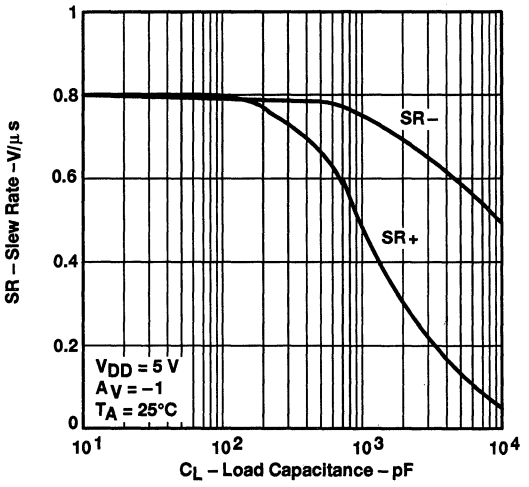


Figure 34

SLEW RATE vs FREE-AIR TEMPERATURE

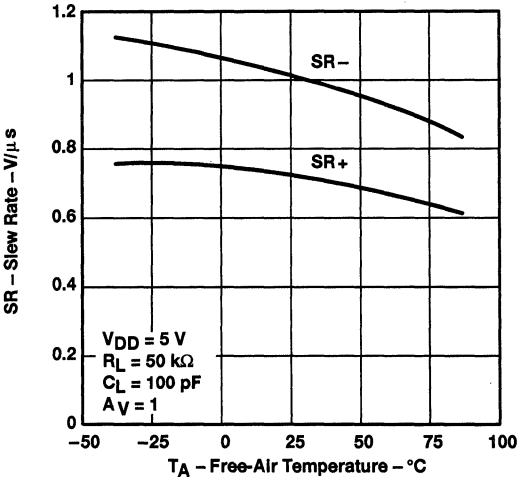


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

INVERTING LARGE-SIGNAL PULSE RESPONSE

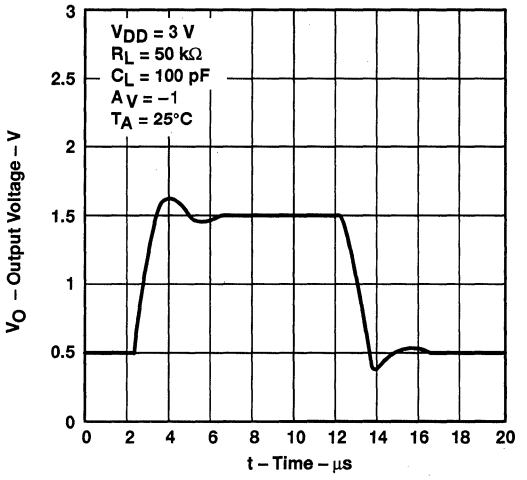


Figure 36

INVERTING LARGE-SIGNAL PULSE RESPONSE

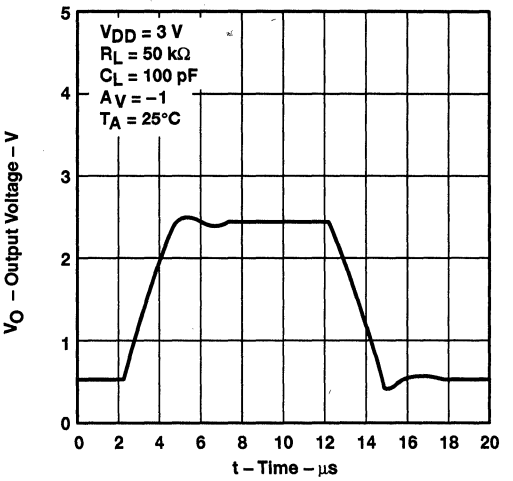


Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

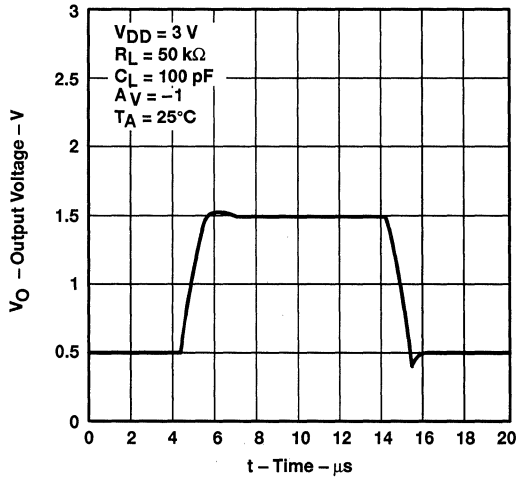


Figure 38

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

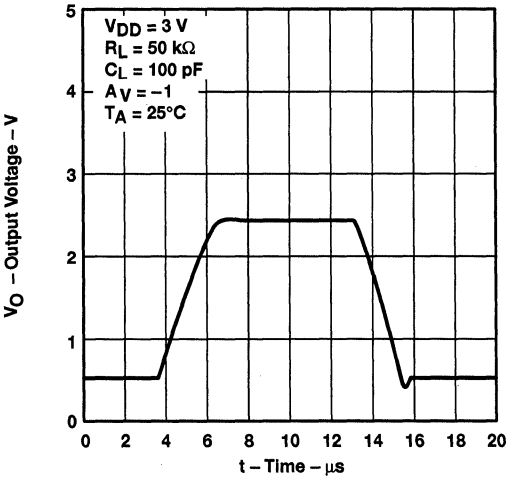


Figure 39

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

INVERTING SMALL-SIGNAL
PULSE RESPONSE

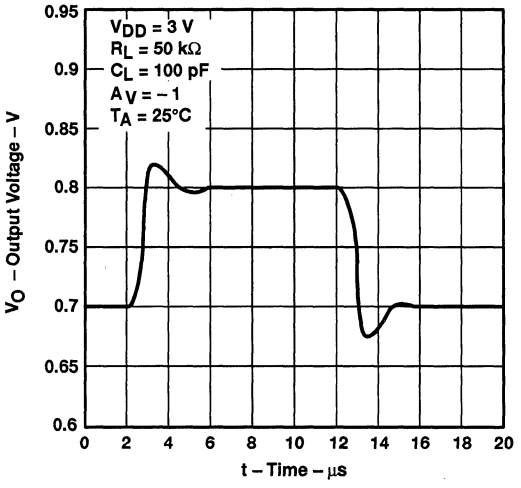


Figure 40

INVERTING SMALL-SIGNAL
PULSE RESPONSE

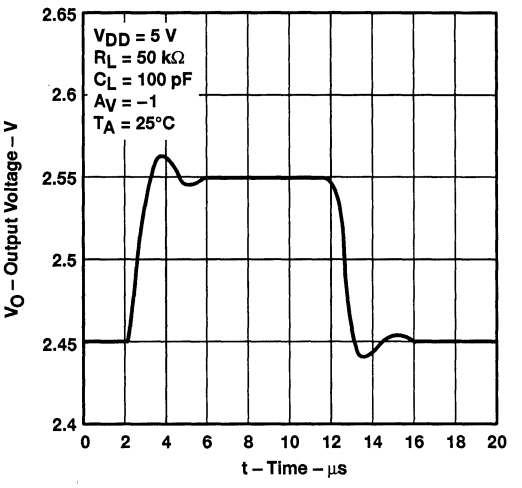


Figure 41

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE

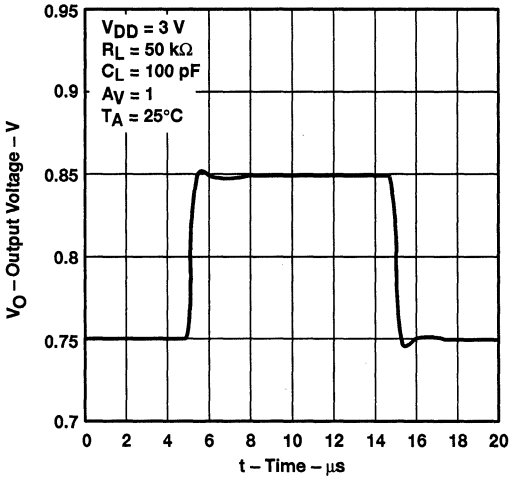


Figure 42

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE

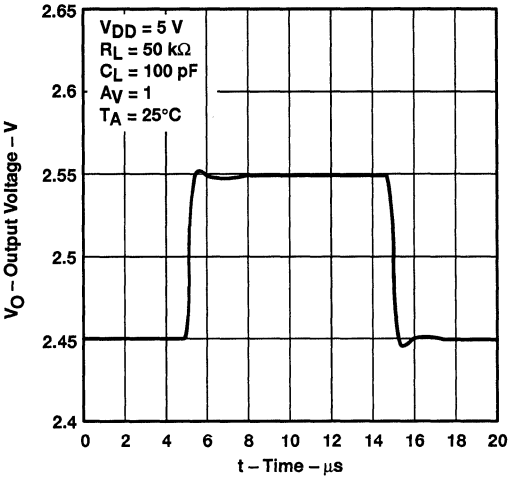


Figure 43

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

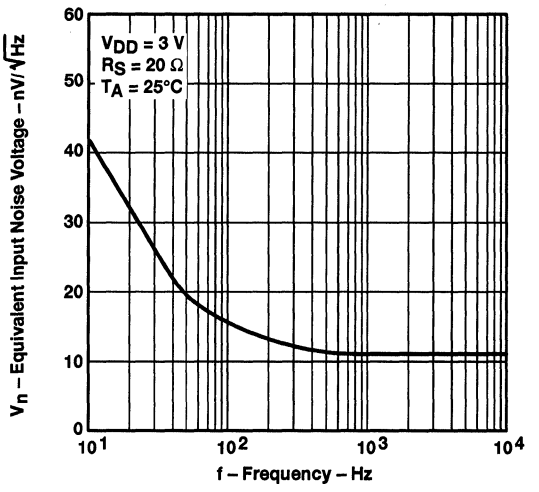


Figure 44

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

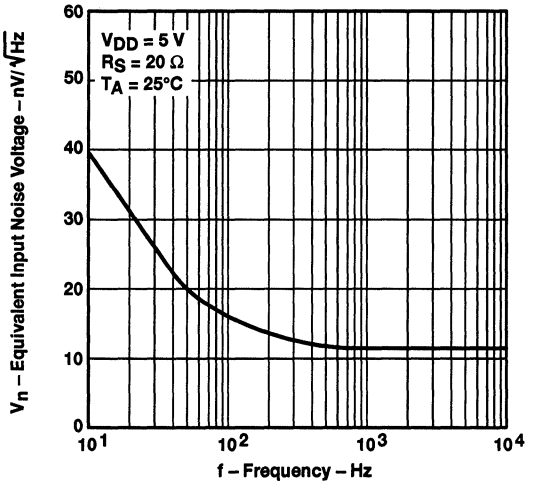


Figure 45

INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

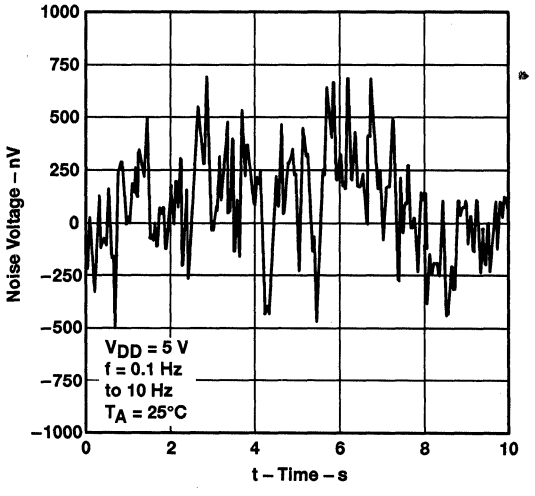


Figure 46

INTEGRATED NOISE VOLTAGE vs FREQUENCY

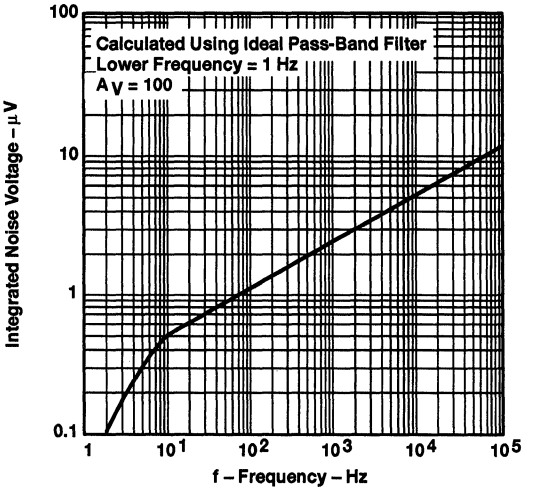


Figure 47

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

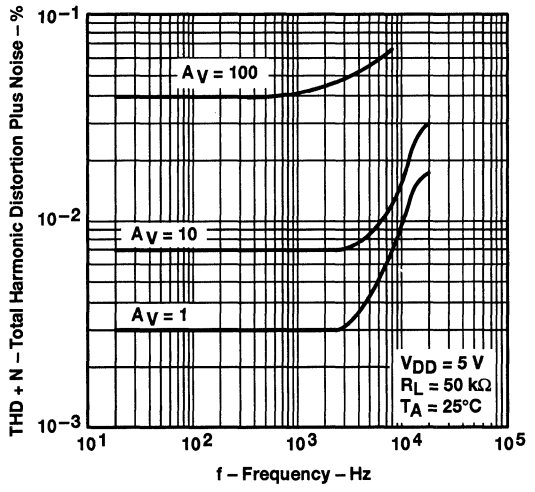


Figure 48

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

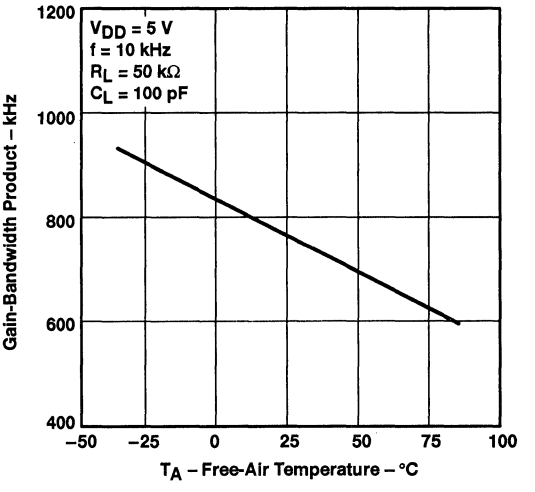


Figure 49

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

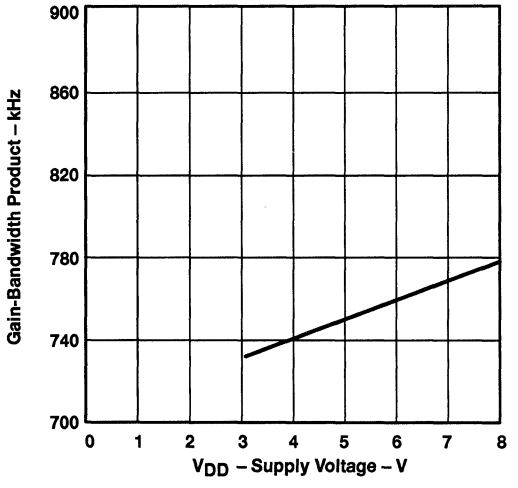


Figure 50

PHASE MARGIN vs LOAD CAPACITANCE

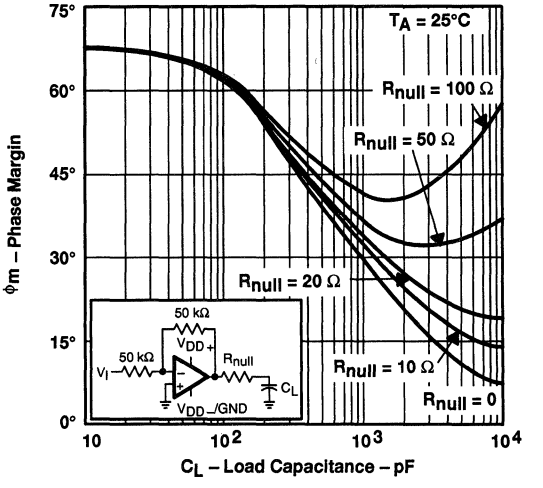


Figure 51

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

GAIN MARGIN
vs
LOAD CAPACITANCE

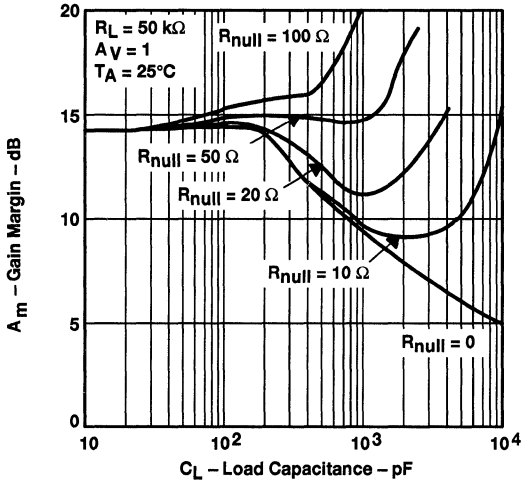


Figure 52

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

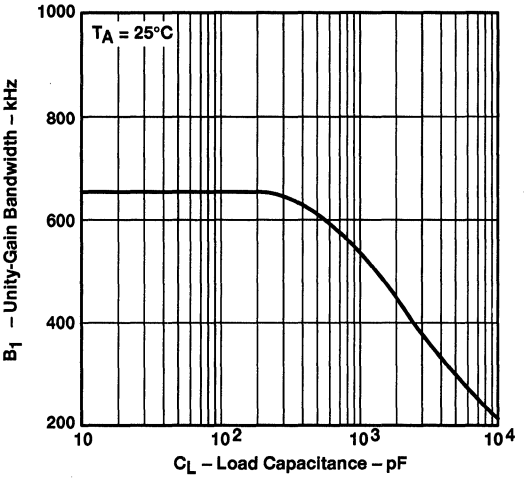
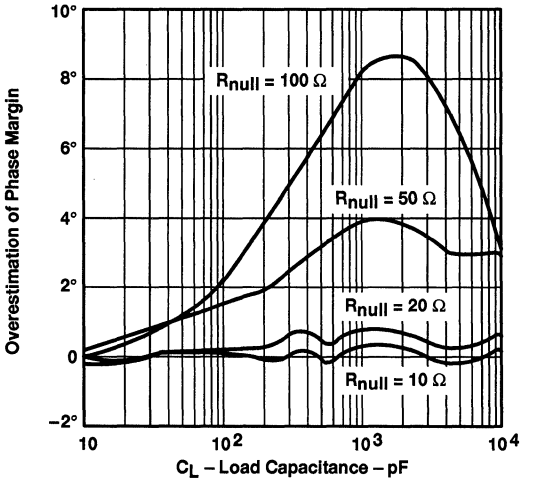


Figure 53

OVERESTIMATION OF PHASE MARGIN†
vs
LOAD CAPACITANCE



† See application information

Figure 54

APPLICATION INFORMATION

loading considerations

The TLV2264 is a low-voltage, low-power version of the TLC2274 with the appropriate design changes relative to the lower power level. The output drive performance to the negative rail for the TLV2264 is similar to the TLC2274 and is capable of driving several milliamperes.

The design topology used for the TLV2264 or the TLC2274 limits the drive to the positive rail to a value very close to the I_{DD} for the amplifier. While the TLC2274 is capable of greater than 1-mA drive from the positive rail, the TLV2264 is capable of only a few hundred microamperes. When designing with lower impedance loads (less than 50 kΩ) with the TLV2264, the lower drive capability to the positive rail needs to be taken into consideration. Although the TLV2264 topology provides lower drive to the positive rail than other high-output-drive rail-to-rail operational amplifiers, it is a more stable topology.

driving large capacitive loads

The TLV2264 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 51 and Figure 52 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see Figure 55) improves the gain and phase margins when driving large capacitive loads. Figure 51 and Figure 52 show the effects of adding series resistances of 10 Ω, 20 Ω, 50 Ω, and 100 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation (1) can be used.

$$\Delta\theta_{m1} = \tan^{-1}\left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L\right) \quad (1)$$

where : $\Delta\theta_{m1}$ = improvement in phase margin

UGBW = unity-gain bandwidth frequency

R_{null} = output series resistance

C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53). To use equation (1), UGBW must be approximated from Figure 53.

Using equation (1) alone overestimates the improvement in phase margin, as illustrated in Figure 54. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation (2).

$$F = \frac{1}{1 + g_m \times R_{null}} \quad (2)$$

where : F = factor reducing frequency of pole

g_m = small-signal output transconductance (typically 4.83×10^{-3} mhos)

R_{null} = output series resistance

APPLICATION INFORMATION

driving large capacitive loads (continued)

For the TLV2264, the pole associated with the load is typically 6 MHz with 100-pF load capacitance. This value varies inversely with C_L: at C_L = 10 pF, use 60 MHz, at C_L = 1000 pF, use 600 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone [equation (1)]. Equation (3) approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the equation (1) to better approximate the improvement in phase margin.

$$\Delta\theta_{m2} = \tan^{-1}\left[\frac{UGBW}{(F \times P_2)}\right] - \tan^{-1}\left(\frac{UGBW}{P_2}\right) \quad (3)$$

where : $\Delta\theta_{m2}$ = reduction in phase margin

UGBW = unity-gain bandwidth frequency

F = factor from equation (2)

P_2 = unadjusted pole (60 MHz @ 10 pF, 6 MHz @100 pF, etc.)

Using these equations with Figure 54 and Figure 55 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.

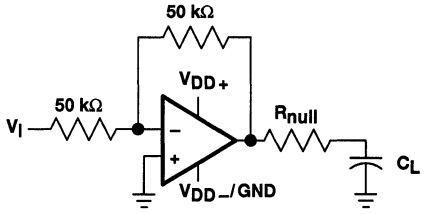


Figure 55. Series-Resistance Circuit

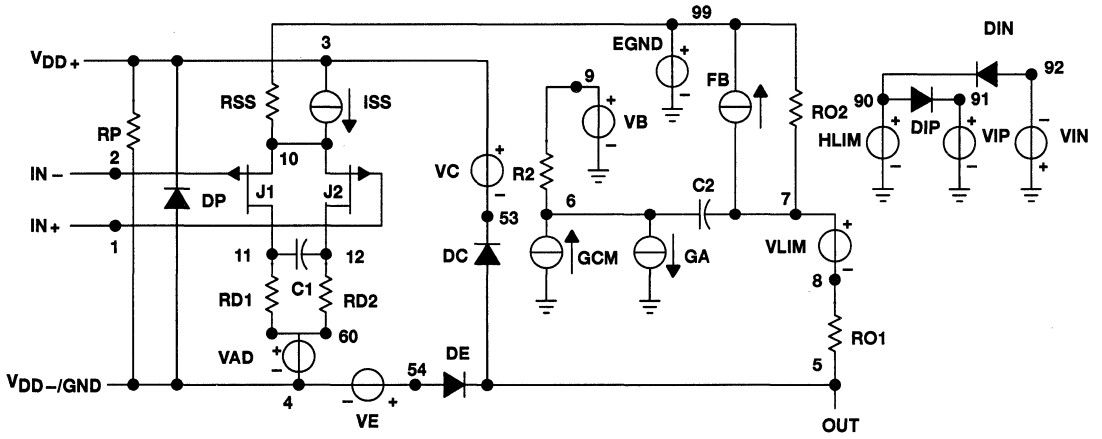
APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using *PSpice*® *Parts*™ model generation software. The Boyle macromodel and subcircuit in Figure 56 are generated using the TLV2264 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).



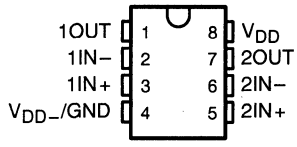

```
.SUBCKT TLV2264 1 2 3 4 5
C1      11    12    1.372E–12
C2      6     7     10.00E–12
DC      5     53    DX
DE      54    5     DX
DLP     90    91    DX
DLN     92    90    DX
DP      4     3     DX
EGND    99    0     POLY (2) (3,0) (4,0) 0 .5 .5
FB      7     99    POLY (5) VB VC VE VLP
+ VLN 0 19.79E6 –40E6 40E6 40E6 –40E6
GA      6     0     11    12 21.05E–6
GCM     0     6     10    99 7.486E–9
ISS     3     10    DC 5.500E–6
HLIM    90    0     VLIM 1K
J1      11    2     10 JX
J2      12    1     10 JX
R2      6     9     100.0E3
RD1     60    11    47.51E3
RD2     60    12    47.51E3
R01     8     5     120
R02     7     99    120
RP      3     4     15.42E3
RSS     10    99    36.36E6
VAD     60    4     –.6
VB      9     0     DC 0
VC      3     53    DC .58
VE      54    4     DC .58
VLIM    7     8     DC 0
VLP     91    0     DC 0
VLN     0     92    DC 5.4
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=161.1E–6
+ VTO=–.09)
.ENDS
```

Figure 56. Boyle Macromodel and Subcircuit

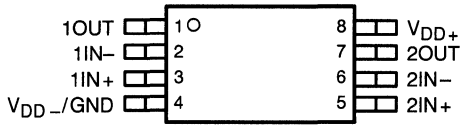
PSpice is a registered trademark of MicroSim Corporation.
Parts is a trademark of MicroSim Corporation.

- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  T_A = –40°C to 85°C . . . 2 V to 8 V
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail and up to V_{DD} –1 V at T_A = 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)

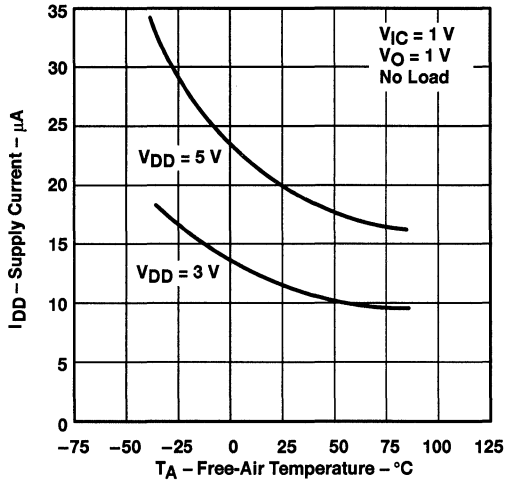


description

The TLV2322 dual operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage single-supply applications. This amplifier is especially well suited to ultra-low-power systems that require devices to consume the absolute minimum of supply currents. Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

These amplifiers are specifically targeted for use in very low-power, portable, battery-driven applications with the maximum supply current per operational amplifier specified at only 27 μA over its full temperature range of –40°C to 85°C.

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon-gate LinCMOS™ technology. The LinCMOS process also features extremely high input impedance and ultra-low bias currents making these amplifiers ideal for interfacing to high-impedance sources such as sensor circuits or filter applications.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 85°C	9 mV	TLV2322ID	TLV2322IP	TLV2322IPWLE	TLV2322Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2322IDR).
The PW package is only available left-end taped and reeled (e.g., TLV2322IPWLE).

LinCMOS™ is a trademark of Texas Instruments Incorporated.

description (continued)

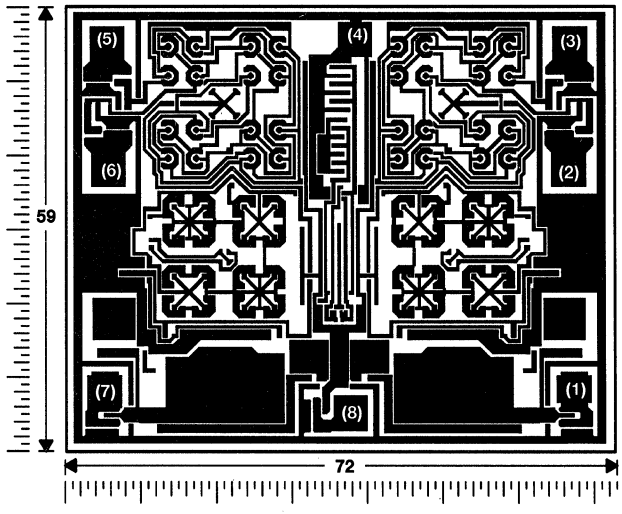
To facilitate the design of small portable equipment, the TLV2322 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

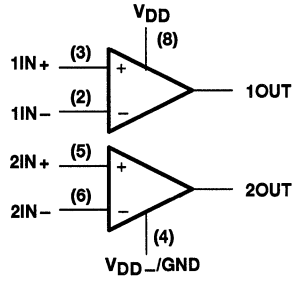
The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2322 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD can result in the degradation of the device parametric performance.

TLV2322Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2322I. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

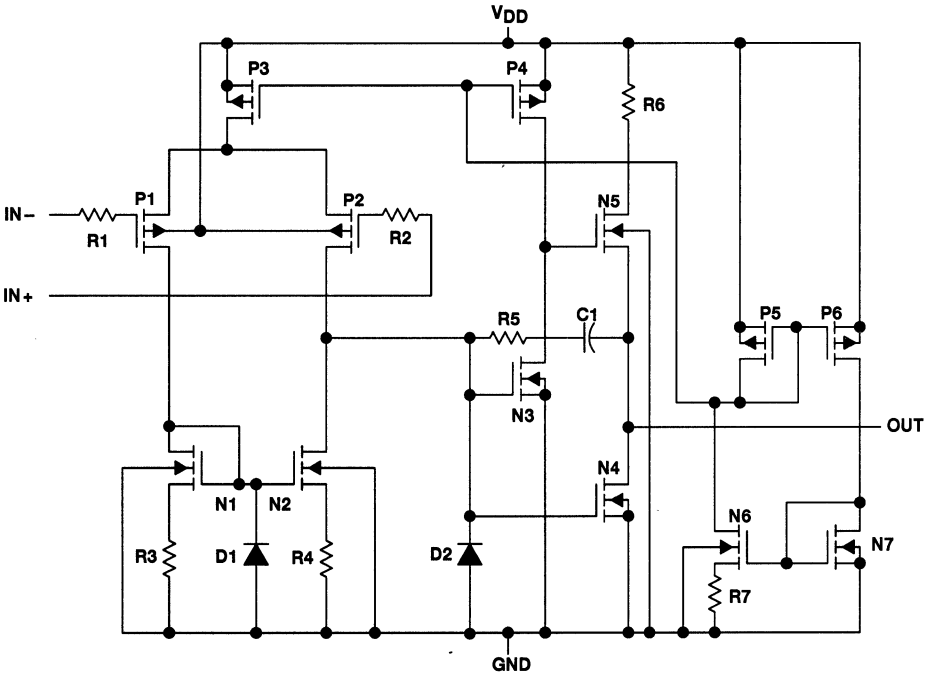
BONDING PADS:
4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES
ARE ±10%.

ALL DIMENSIONS
ARE IN MILS.

TLV2322I equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	54
Diodes	4
Resistors	14
Capacitors	2

† Includes both, amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage (see Note 2) ..... $V_{DD}\pm$
Input voltage range, V_I (any input) ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
Output current, I_O ..... ±30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	725 mV	5.8 mW/°C	377 mW
P	1000 mV	8.0 mW/°C	520 mW
PW	525 mV	4.2 mW/°C	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	−0.2	1.8	V
	V_{DD} = 5 V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2322I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	9		1.1	9	mV
			Full range			11			11	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.8		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	25°C	50	400		50	520		V/mV
			Full range	50			50			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	88		65	94		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	86		70	86		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		12	34		20	34	μA
			Full range			54			54	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, $V_{O(PP)}$ = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2322I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, See Figure 30	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		0.02		V/μs
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 30	25°C		2.5		kHz
				85°C		2		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 32	25°C		27		kHz
				85°C		21		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f= B_1, R_L = 1 MΩ,	−40°C		39°		
				25°C		34°		
				85°C		28°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2322I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, C_L = 20 pF, See Figure 30	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				85°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 30	25°C		5		kHz
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 32	25°C		85		kHz
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 1 MΩ,	−40°C		38°		
				25°C		34°		
				85°C		28°		

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2322Y						UNIT
			V_{DD} = 3 V			V_{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ		1.1	9		1.1	9	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OH} = −1 mA	1.75	1.9		3.2	3.8		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = 1 mA		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	50	400		50	520		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	88		65	94		dB
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{ID})	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω	70	86		70	86		dB
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		12	34		20	34	μA

NOTES: 4. The typical values of input bias current offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current	5
		vs Supply voltage	6
		vs Temperature	7
V_{OL}	Low-level output voltage	vs Common-mode input voltage	8
		vs Temperature	9, 11
		vs Differential input voltage	10
		vs Low-level output current	12
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage	13
		vs Temperature	14
I_{IB}/I_{IO}	Input bias and offset currents	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply voltage	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
SR	Slew rate	vs Supply voltage	19
		vs Temperature	20
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Unity-gain bandwidth	vs Temperature	22
		vs Supply voltage	23
A_{VD}	Large-signal differential voltage amplification	vs Frequency	24, 25
ϕ_m	Phase margin	vs Supply voltage	26
		vs Temperature	27
		vs Load capacitance	28
V_n	Equivalent input noise voltage	vs Frequency	29
	Phase shift	vs Frequency	24, 25

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE

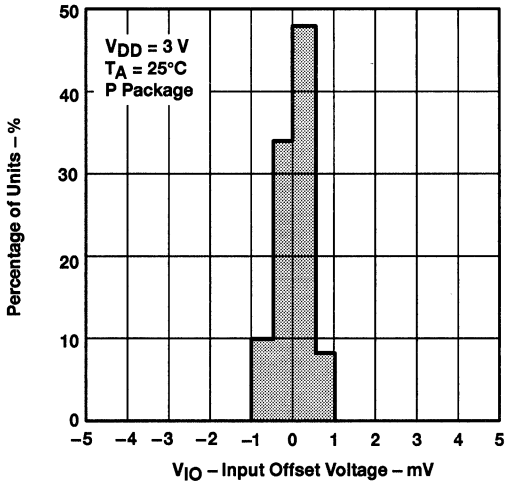


Figure 1

DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE

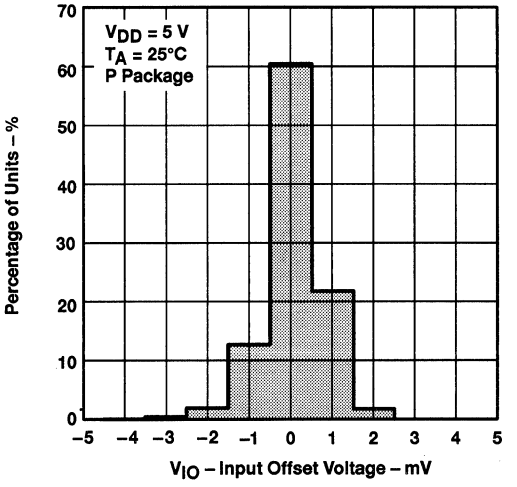


Figure 2

DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

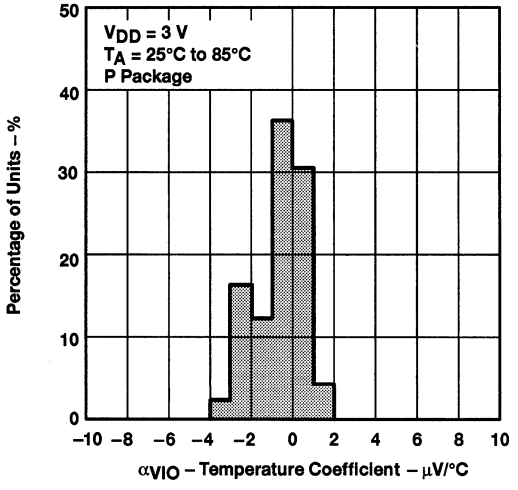


Figure 3

DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

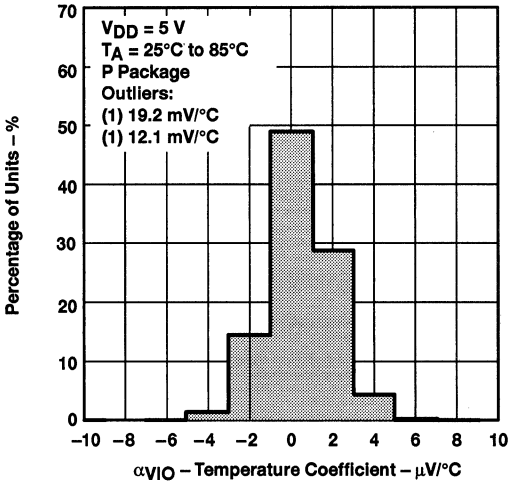


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

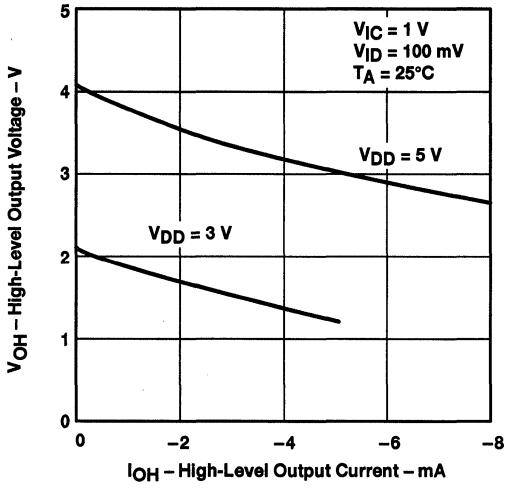


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

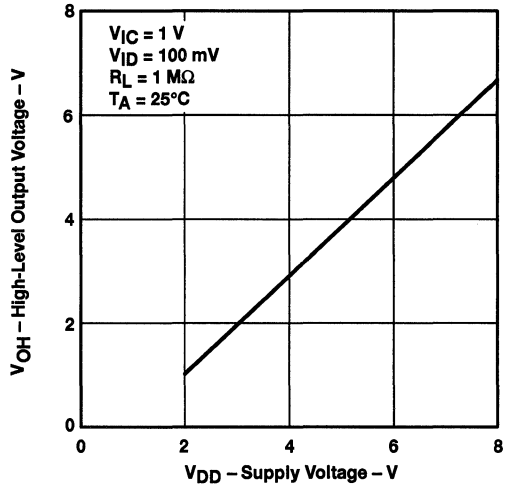


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

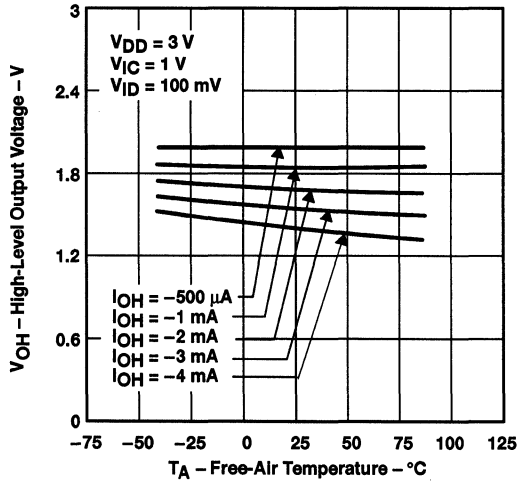


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

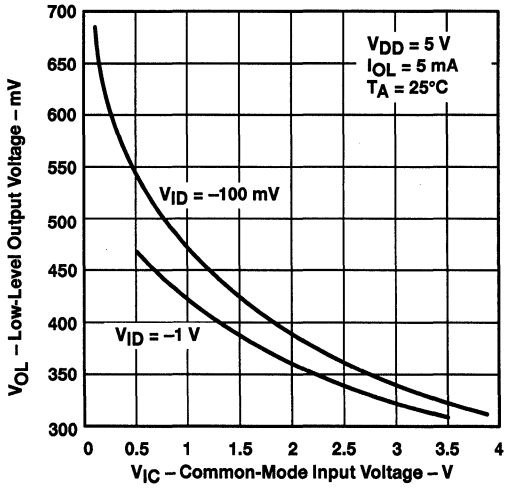


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

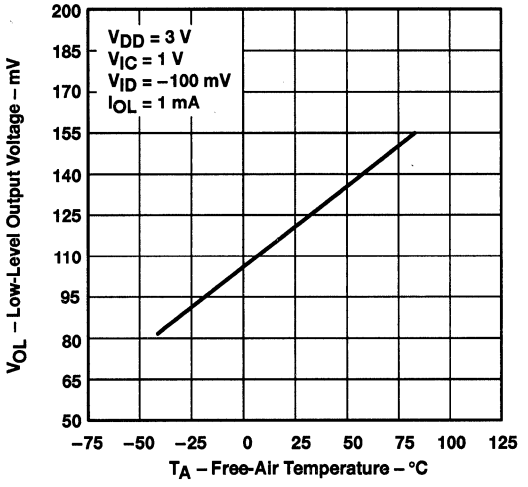


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

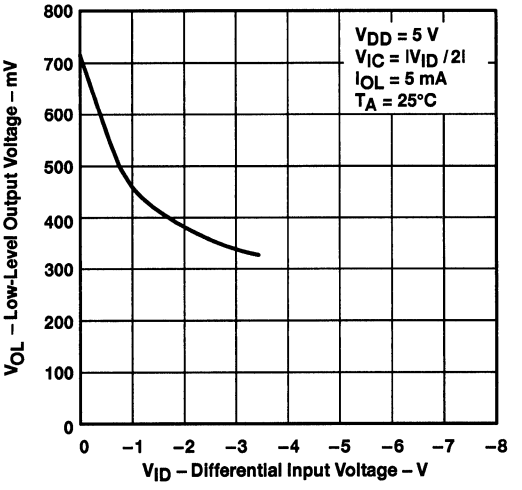


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

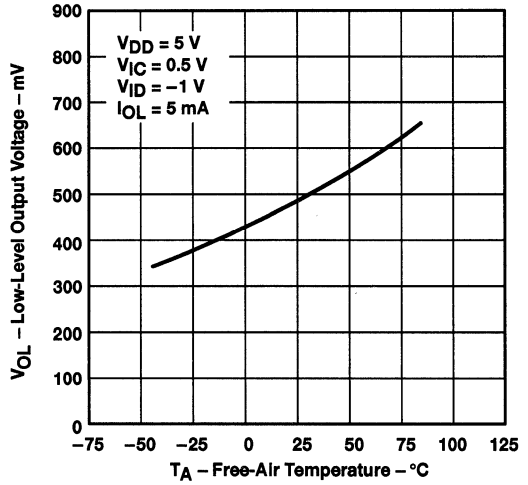


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

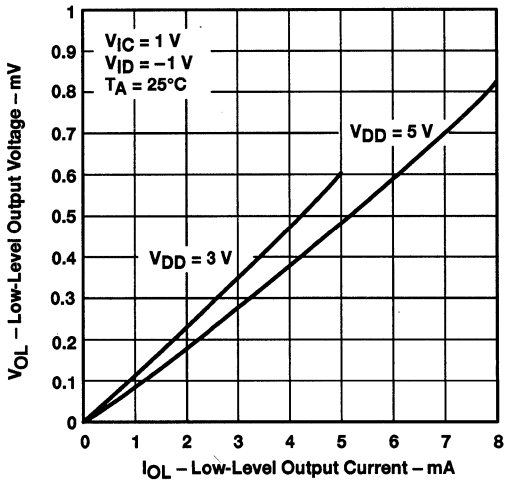


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

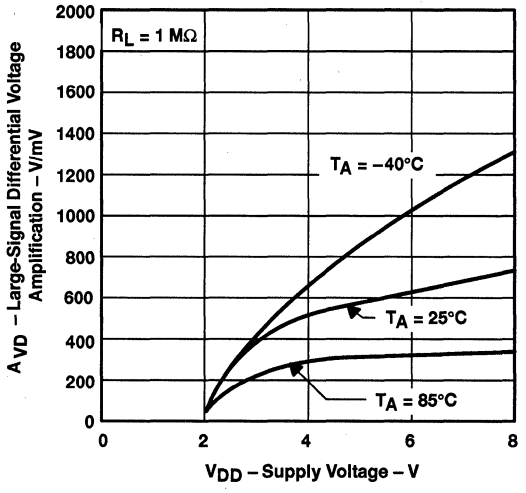


Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

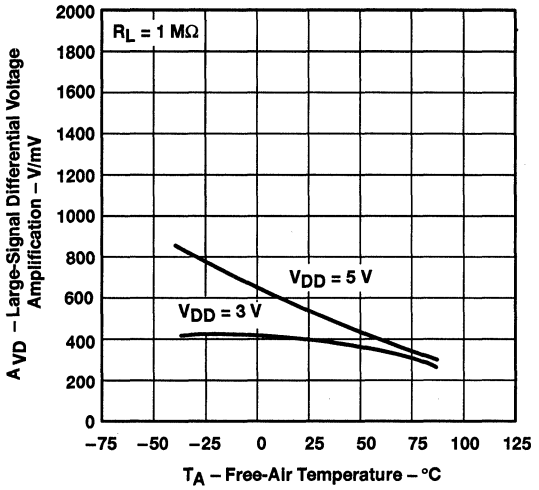
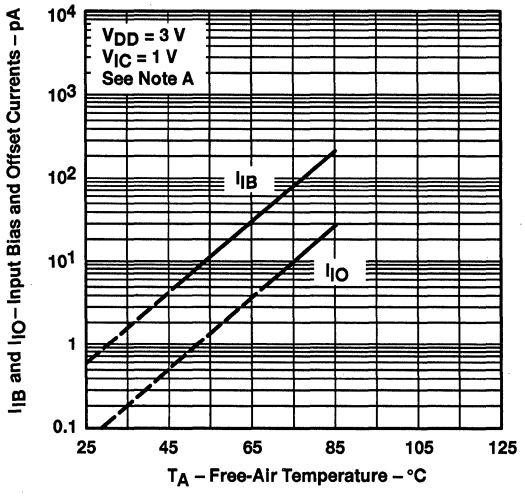


Figure 14

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 15

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE

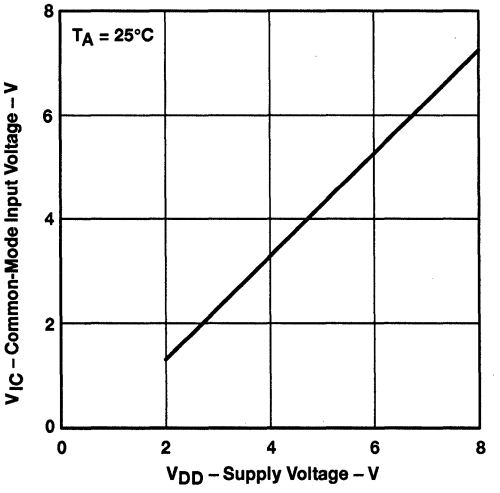


Figure 16

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

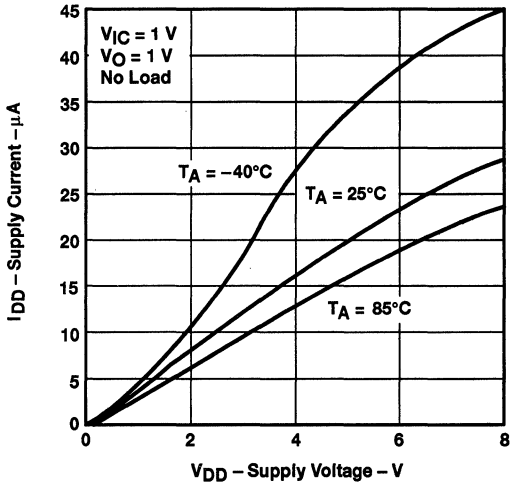


Figure 17

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

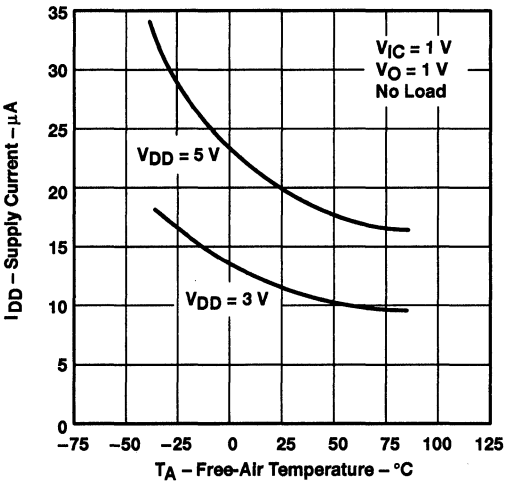


Figure 18

SLEW RATE
vs
SUPPLY VOLTAGE

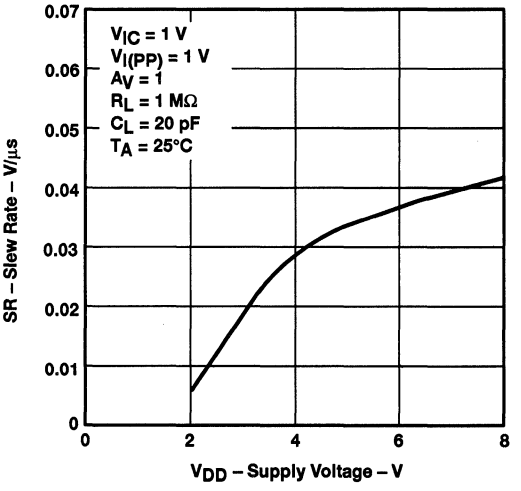


Figure 19

SLEW RATE
vs
FREE-AIR TEMPERATURE

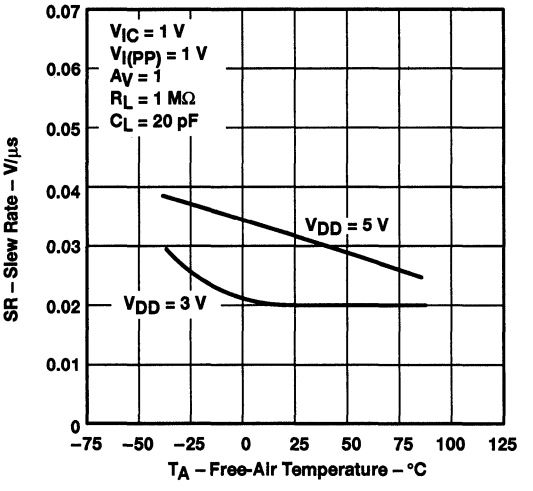


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

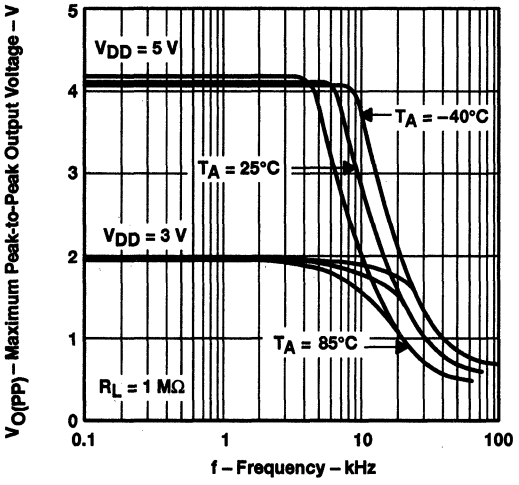


Figure 21

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

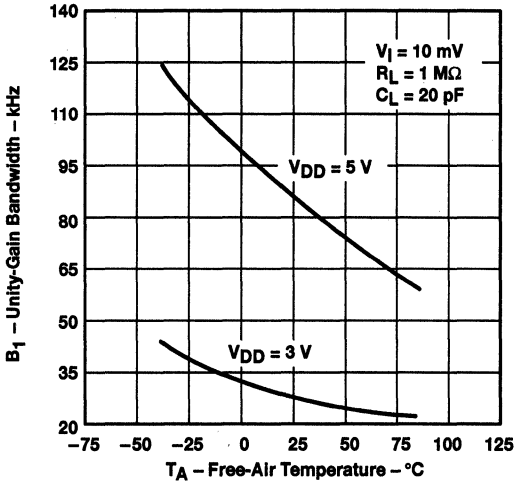


Figure 22

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

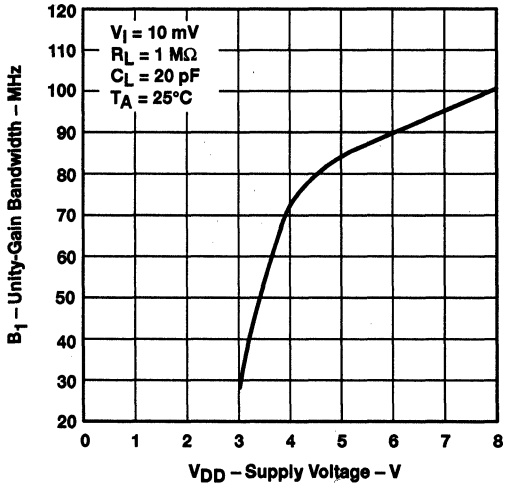


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

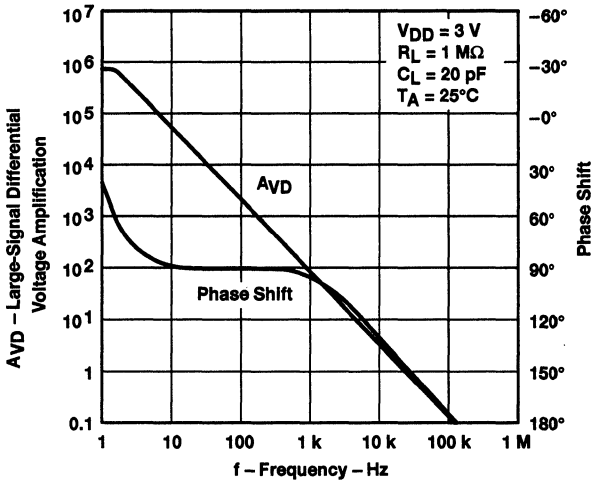


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

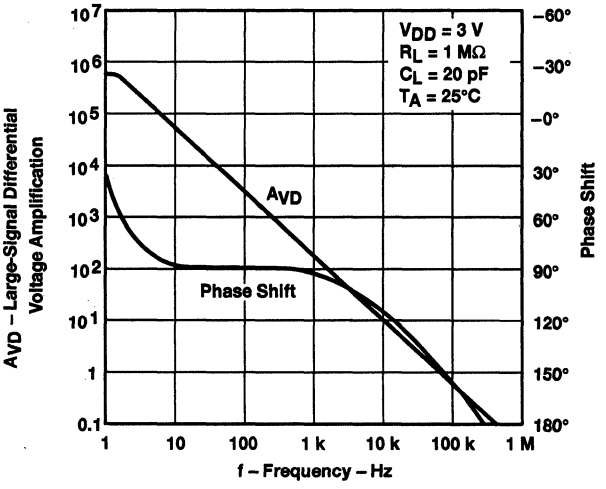


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

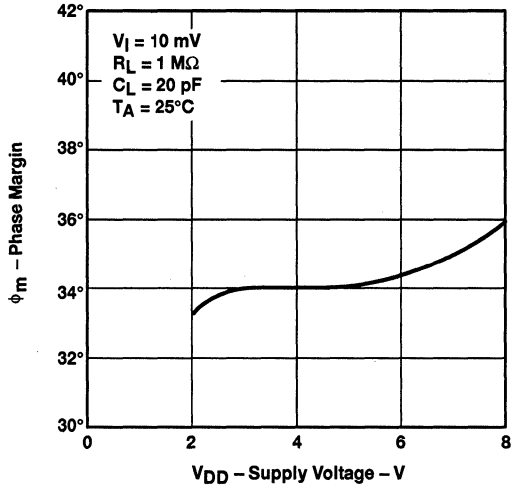


Figure 26

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

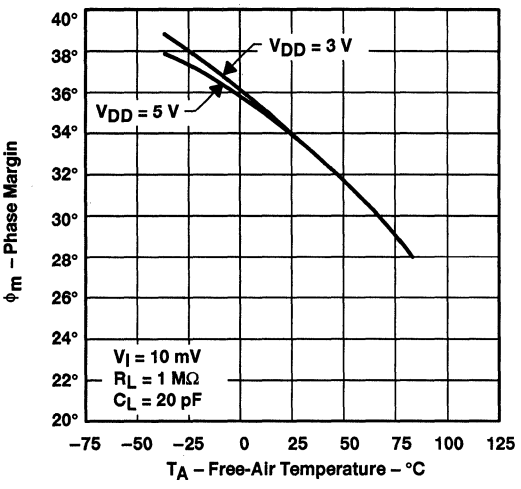


Figure 27

PHASE MARGIN
vs
LOAD CAPACITANCE

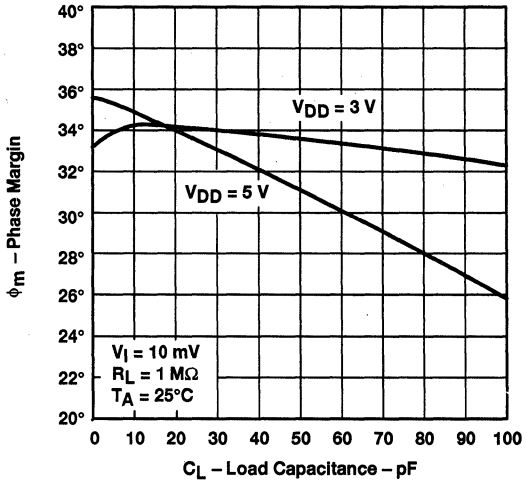


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

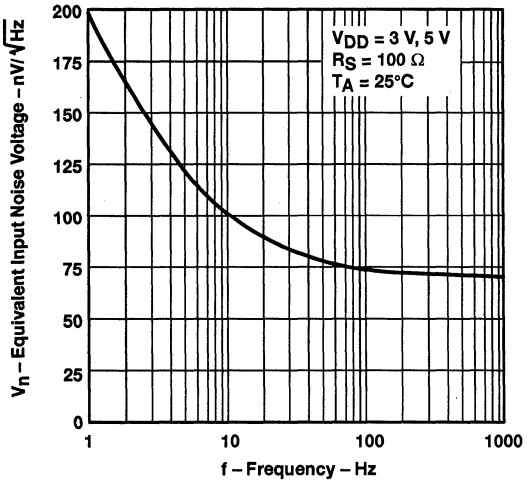


Figure 29

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2322 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

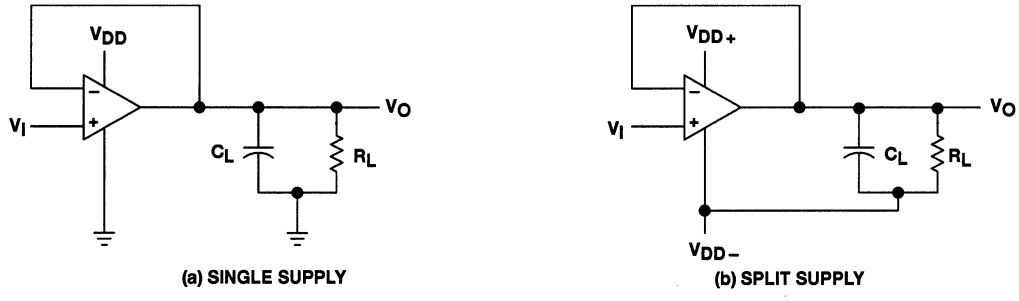


Figure 30. Unity-Gain Amplifier

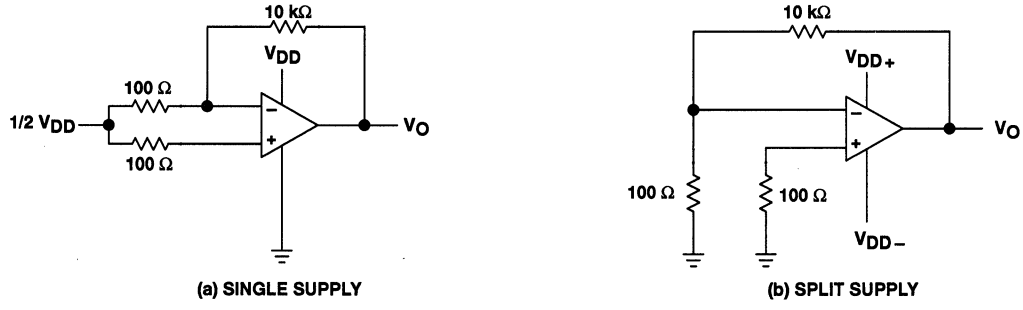


Figure 31. Noise Test Circuits

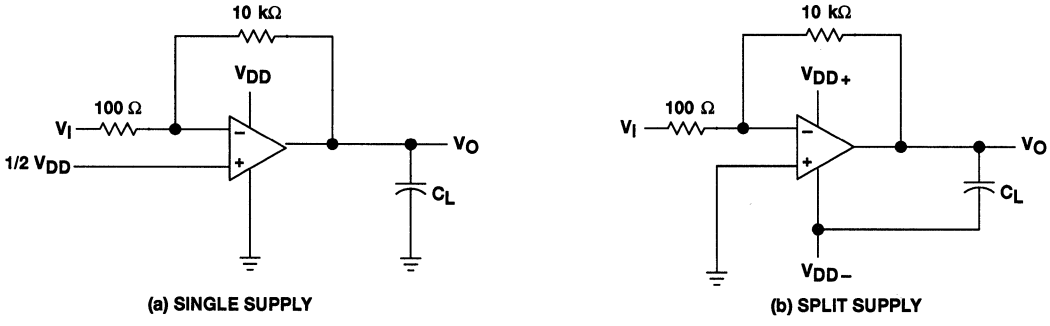


Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2322 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

  Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

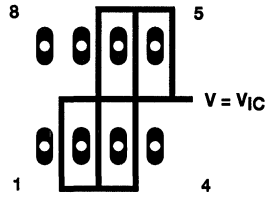


Figure 33. Isolation Metal Around Device Inputs (P Package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure the temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance that can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

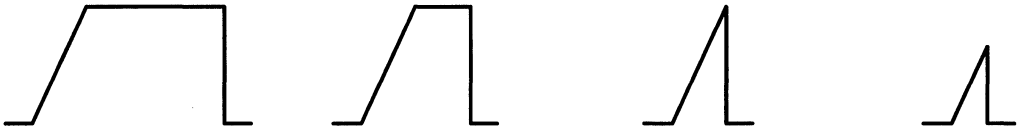


Figure 34. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2322 performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

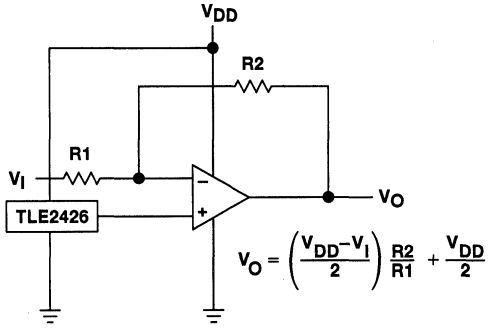


Figure 35. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)

The TLV2322 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

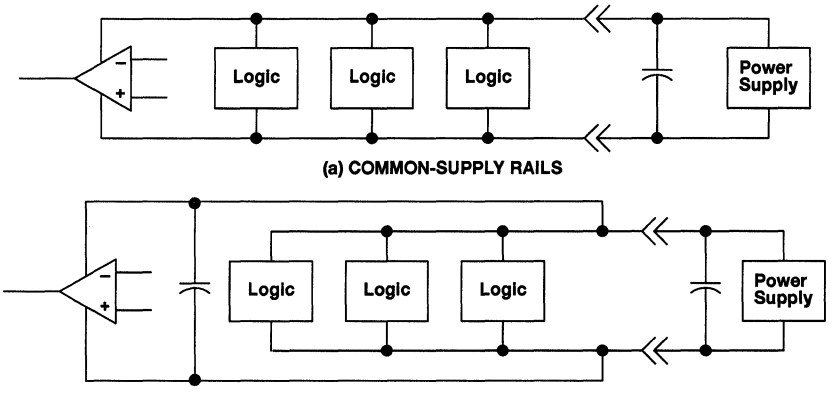


Figure 36. Common Versus Separate Supply Rails

input characteristics

The TLV2322 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower the range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.2 V at all other temperatures.

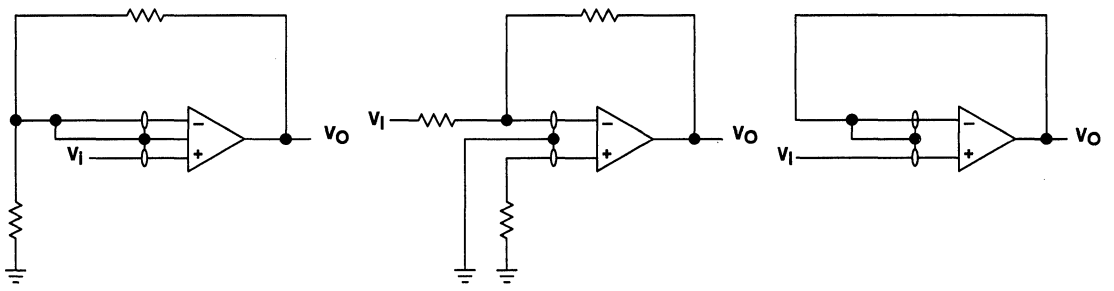
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2322 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2322 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

APPLICATION INFORMATION

input characteristics (continued)



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 37. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2322 result in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

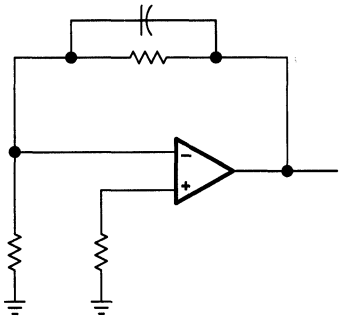


Figure 38. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV2322 incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD can result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2322 inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage

APPLICATION INFORMATION

by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2322 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2322 possesses excellent high-level output voltage and current capability methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

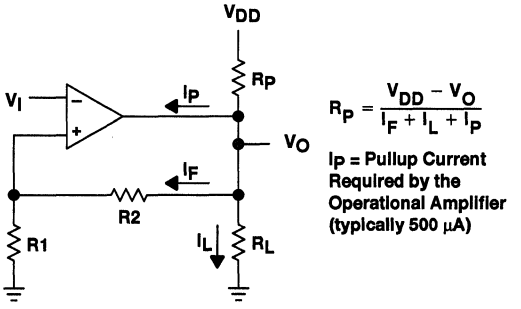


Figure 39. Resistive Pullup to Increase V_{OH}

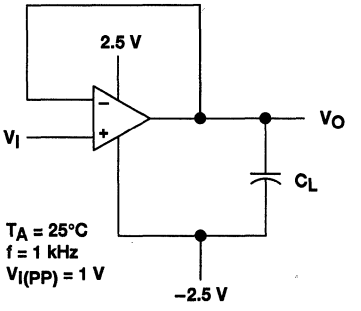
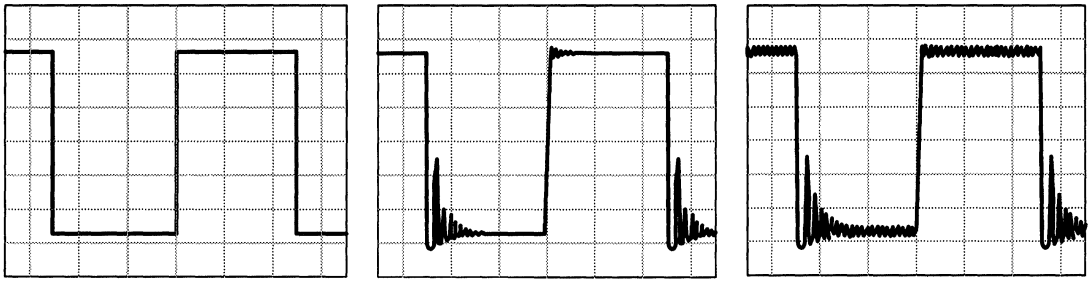


Figure 40. Test Circuit for Output Characteristics

All operating characteristics of the TLV2322 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

APPLICATION INFORMATION

output characteristics (continued)



(a) C_L = 20 pF, R_L = NO LOAD

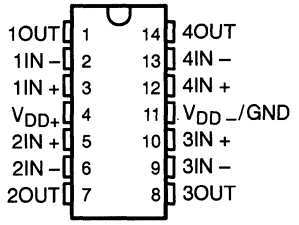
(b) C_L = 260 pF, R_L = NO LOAD

(c) C_L = 310 pF, R_L = NO LOAD

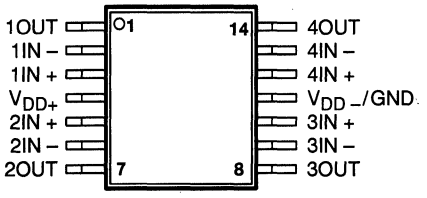
Figure 41. Effect of Capacitive Loads

- **Wide Range of Supply Voltages Over Specified Temperature Range: T_A = –40°C to 85°C . . . 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} –1 V at 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**

D OR N PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



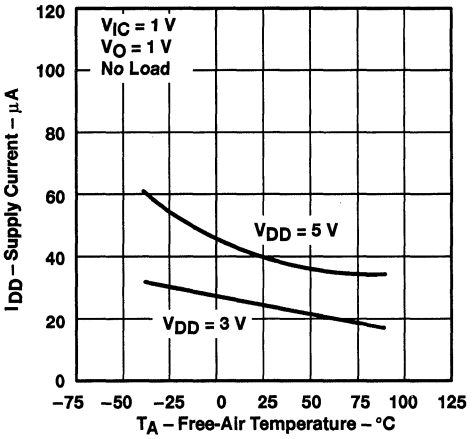
description

The TLV2324 quad operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage single-supply applications. This amplifier is especially well suited to ultra-low power systems that require devices to consume the absolute minimum of supply currents. Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies. The common-mode input-voltage range includes the negative rail and extends to within 1 V of the positive rail.

These amplifiers are specifically targeted for use in very low-power, portable, battery-driven applications with the maximum supply current per operational amplifier is specified at only 27 μA over its full temperature range of –40°C to 85°C.

Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon-gate, LinCMOS™ technology. The LinCMOS process also features extremely high input impedance and ultra-low bias currents making them ideal for interfacing to high-impedance sources such as in sensor circuits or filter applications.

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
–40°C to 85°C	10 mV	TLV2324ID	TLV2324IN	TLV2324IPWLE	TLV2324Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2324IDR).
The PW package is only available left-end taped and reeled (e.g., TLV2324IPWLE).

LinCMOS™ is a trademark of Texas Instruments Incorporated.

description (continued)

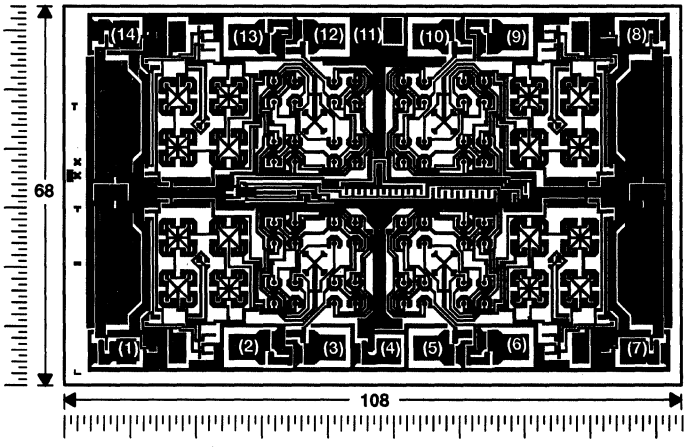
To facilitate the design of small portable equipment, the TLV2324 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline package (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

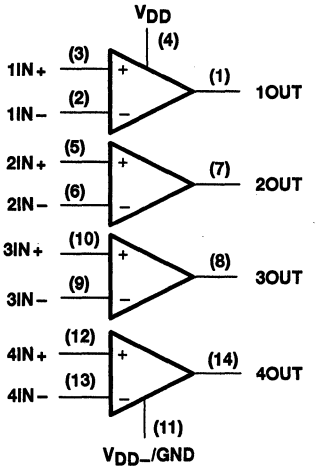
The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2324 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

TLV2324Y chip information

This chip, when properly assembled, display characteristics similar to the TLV2324I. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

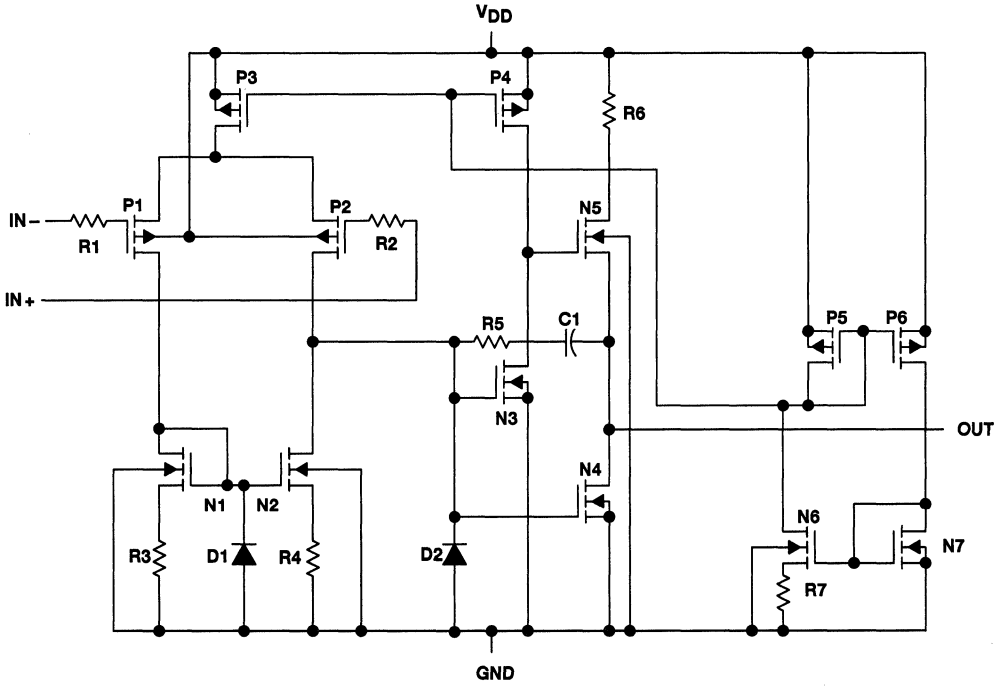
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (12) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

TLV2324I equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	108
Diodes	8
Resistors	28
Capacitors	4

† Includes all amplifiers, ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... $V_{DD\pm}$
Input voltage range, V_I (any input) ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
Output current, I_O ..... ±30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW package ..... 260°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mV	7.6 mW/°C	494 mW
N	1575 mV	12.6 mW/°C	819 mW
PW	700 mV	5.6 mW/°C	364 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	−0.2	1.8	V
	V_{DD} = 5 V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2324I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.8		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	25°C	50	400		50	520		V/mV
			Full range	50			50			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	88		65	94		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	86		70	86		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		24	68		39	68	μA
			Full range			108			108	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, $V_{O(PP)}$ = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2324I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, See Figure 30	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		0.02		V/μs
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 30	25°C		2.5		kHz
				85°C		2		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 32	25°C		27		kHz
				85°C		21		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 1 MΩ,	−40°C		39°		
				25°C		34°		
				85°C		28°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2324I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, C_L = 20 pF, See Figure 30	$V_{I(PP)}$= 1 V	25°C		0.03		V/μs
				85°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 30	25°C		5		kHz
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 32	25°C		85		kHz
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 1 MΩ,	−40°C		38°		
				25°C		34°		
				85°C		28°		

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLV2324Y						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, R_S = 50 Ω,	V_{IC} = 1 V, R_L = 1 MΩ		1.1	10		1.1	10	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)			−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, I_{OH} = −1 mA	V_{ID} = 100 mV,	1.75	1.9		3.2	3.8		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, I_{OL} = 1 mA	V_{ID} = 100 mV,		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, (see Note 6)	R_L = 1 MΩ,	50	400		50	520		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, R_S = 50 Ω	V_{IC} = V_{ICR}min,	65	88		65	94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	V_O = 1 V, R_S = 50 Ω	V_{IC} = 1 V,	70	86		70	86		dB
I_{DD}	Supply current	V_O = 1 V, No load	V_{IC} = 1 V,		24	68		39	68	μA

NOTES: 4. The typical values of input bias current offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current	5
		vs Supply voltage	6
		vs Temperature	7
V_{OL}	Low-level output voltage	vs Common-mode input voltage	8
		vs Temperature	9, 11
		vs Differential input voltage	10
		vs Low-level output current	12
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage	13
		vs Temperature	14
I_{IB}/I_{IO}	Input bias and offset currents	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply voltage	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
SR	Slew rate	vs Supply voltage	19
		vs Temperature	20
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Unity-gain bandwidth	vs Temperature	22
		vs Supply voltage	23
A_{VD}	Large-signal differential voltage amplification	vs Frequency	24, 25
ϕ_m	Phase margin	vs Supply voltage	26
		vs Temperature	27
		vs Load capacitance	28
V_n	Equivalent input noise voltage	vs Frequency	29
	Phase shift	vs Frequency	24, 25

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE

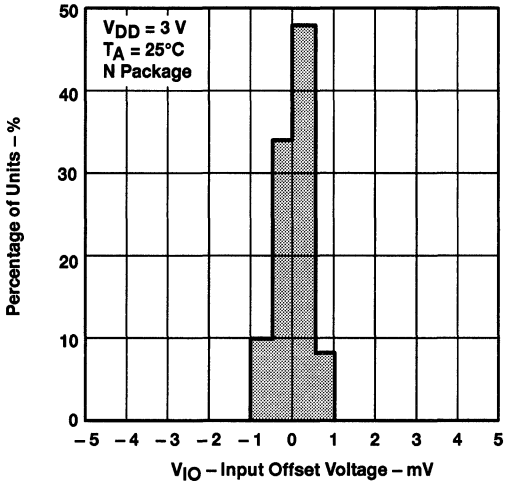


Figure 1

DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE

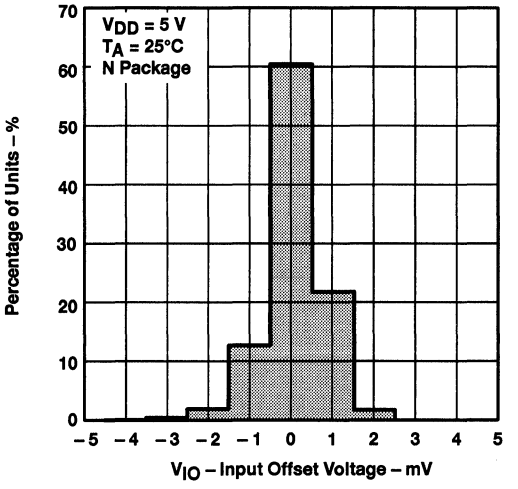


Figure 2

DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

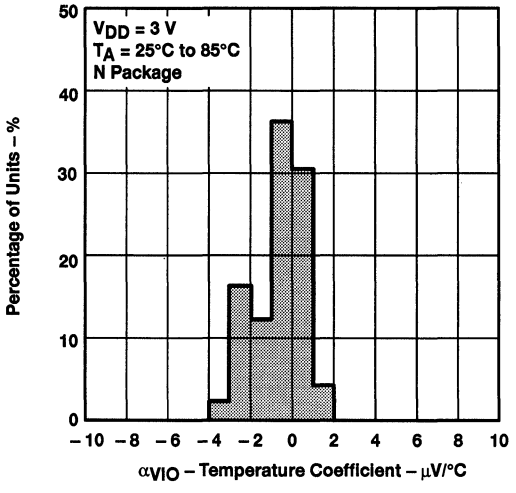


Figure 3

DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

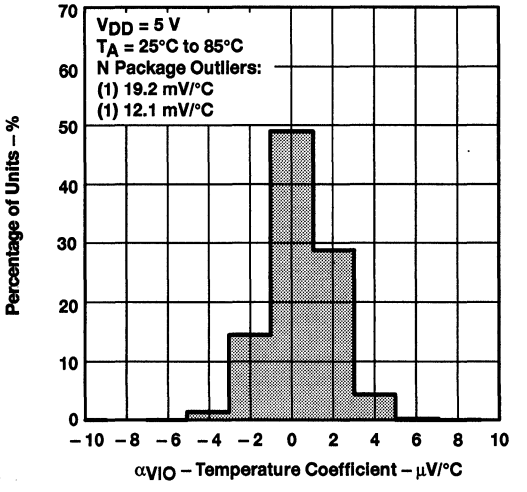


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

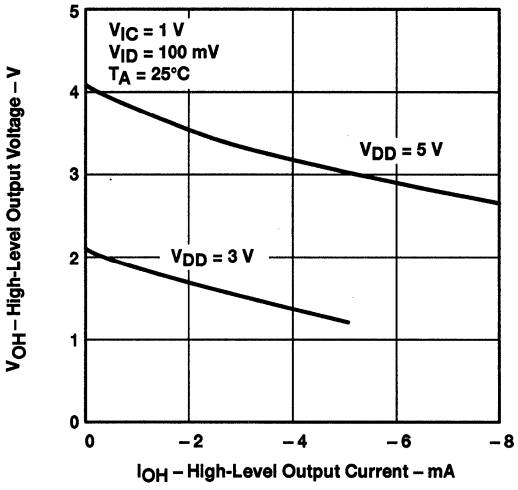


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

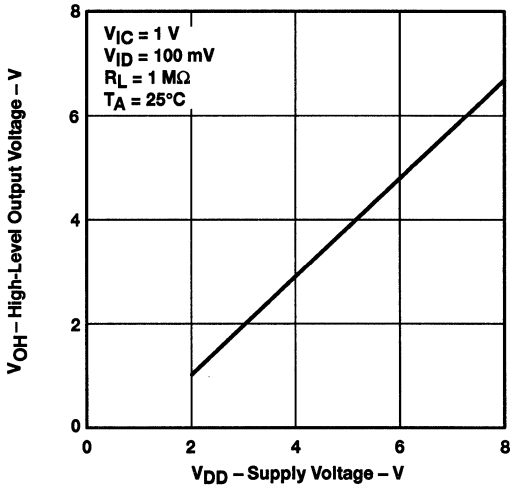


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

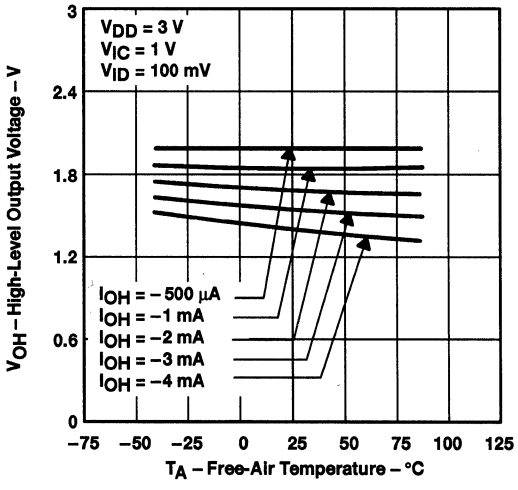


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

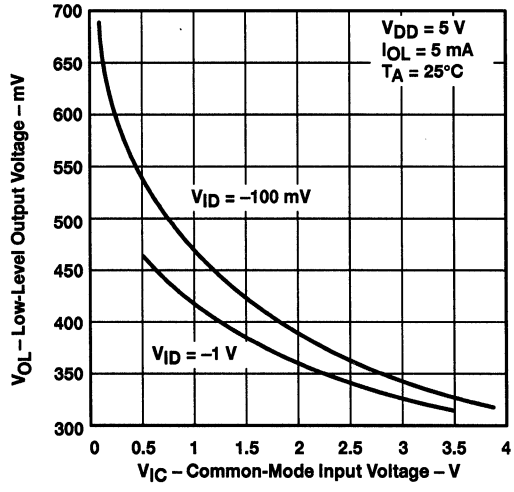


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

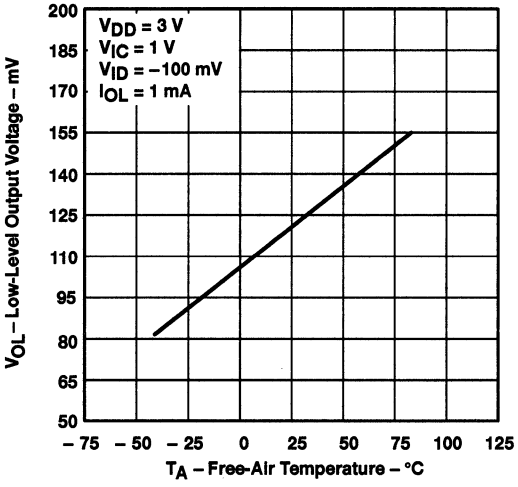


Figure 9

LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

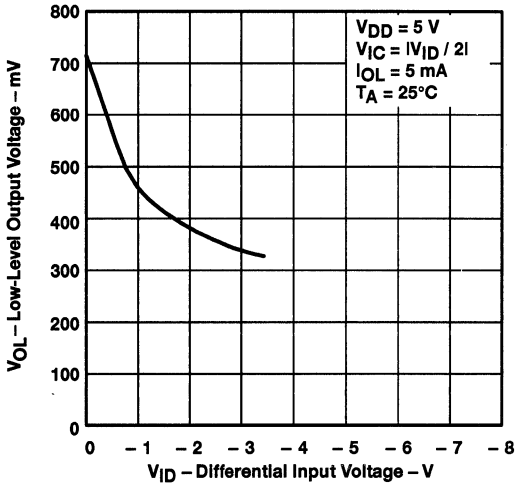


Figure 10

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

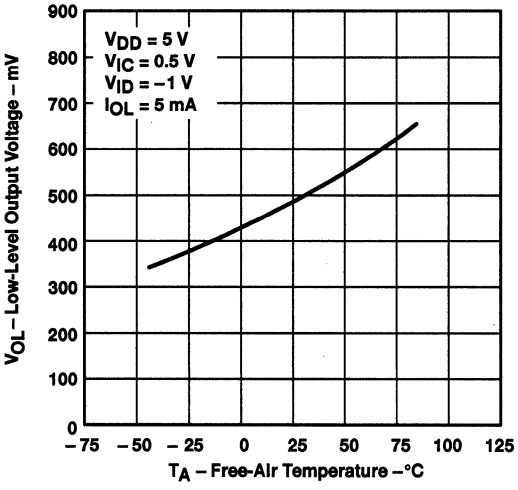


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

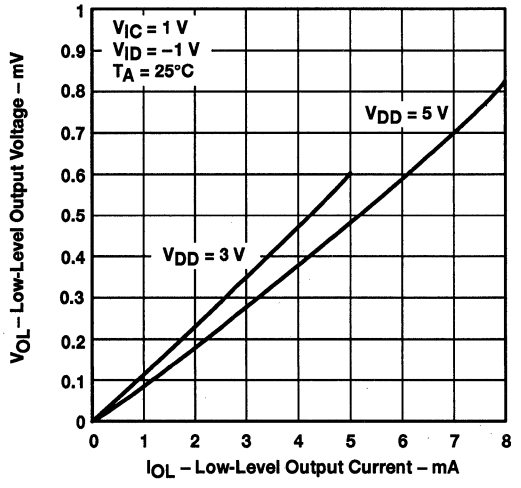


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

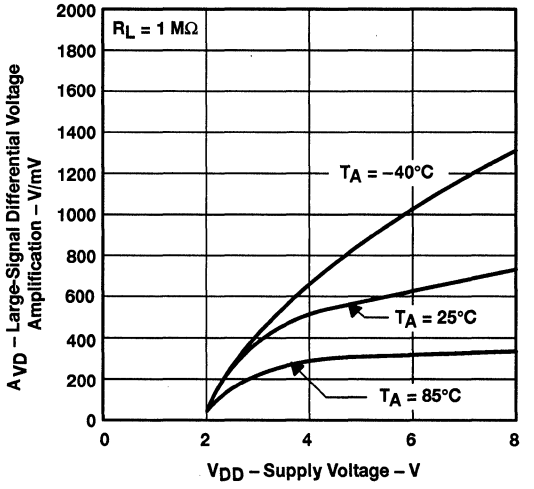


Figure 13

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

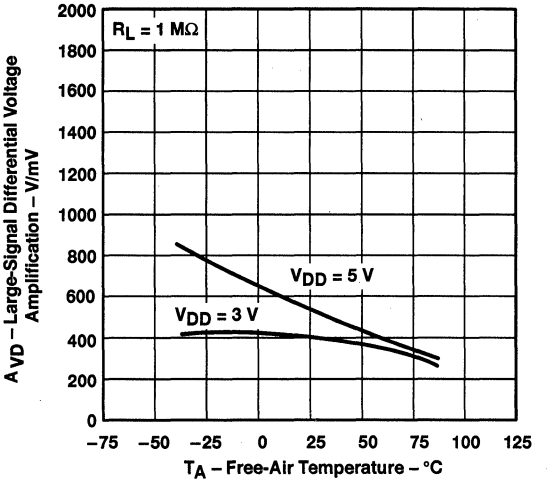
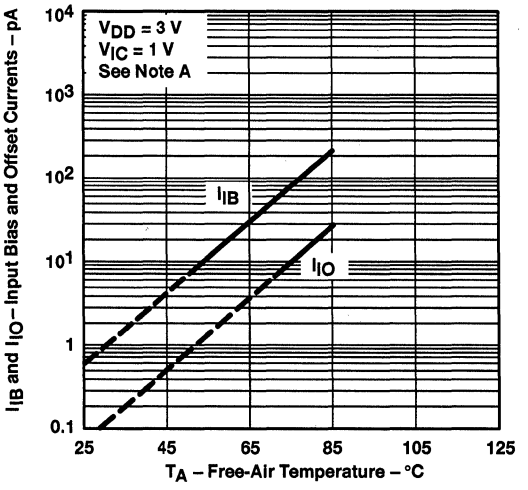


Figure 14

INPUT BIAS CURRENT AND INPUT
OFFSET CURRENT
vs
FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 15

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

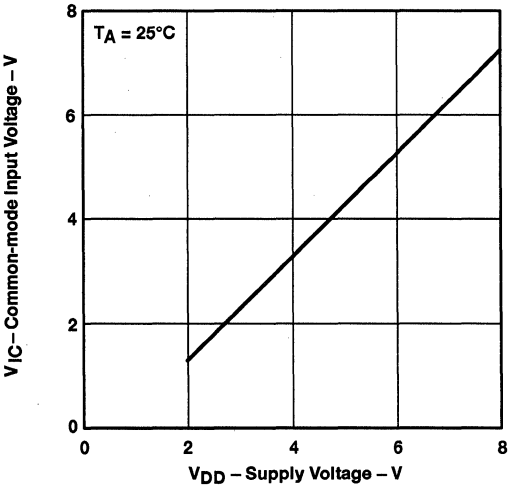


Figure 16

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

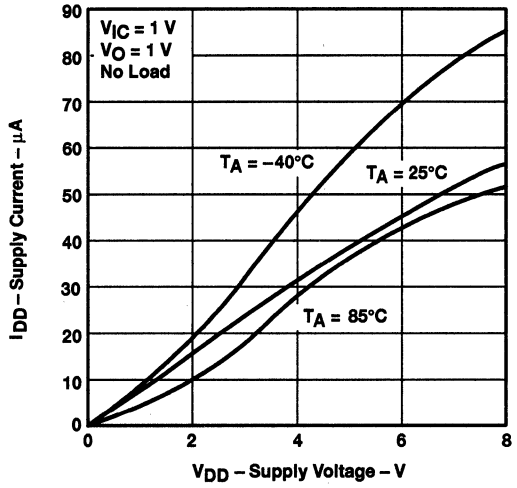


Figure 17

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

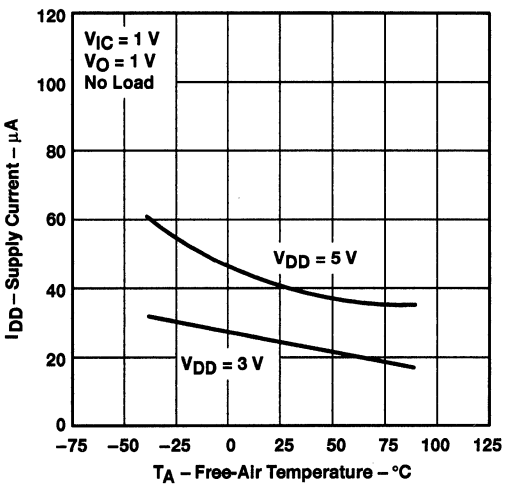


Figure 18

SLEW RATE vs SUPPLY VOLTAGE

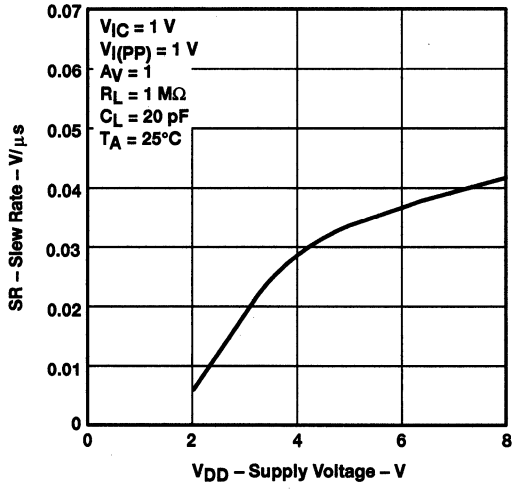


Figure 19

SLEW RATE vs FREE-AIR TEMPERATURE

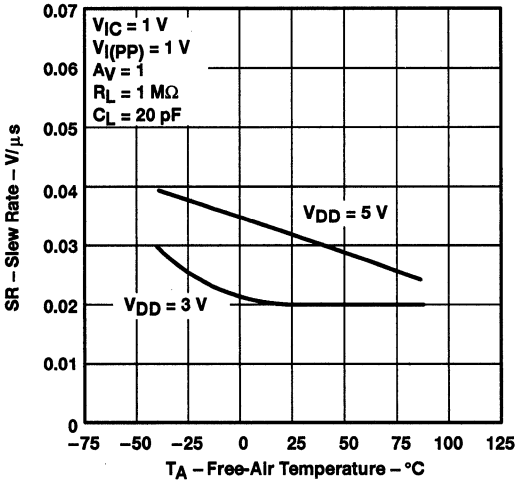


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

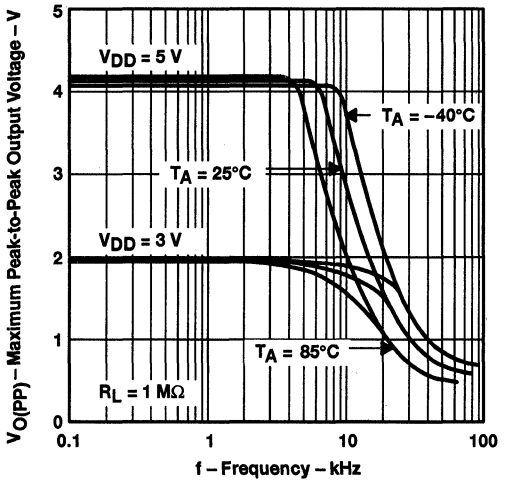


Figure 21

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

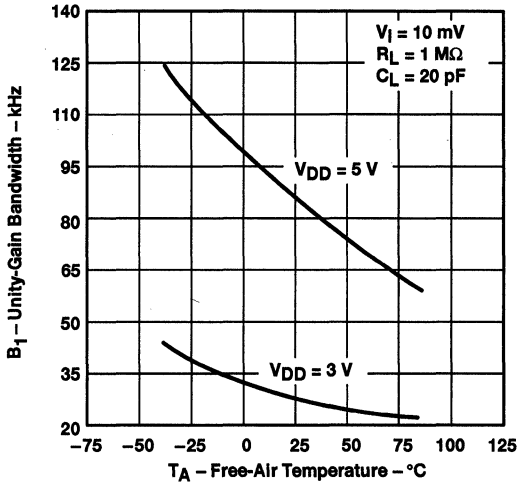


Figure 22

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

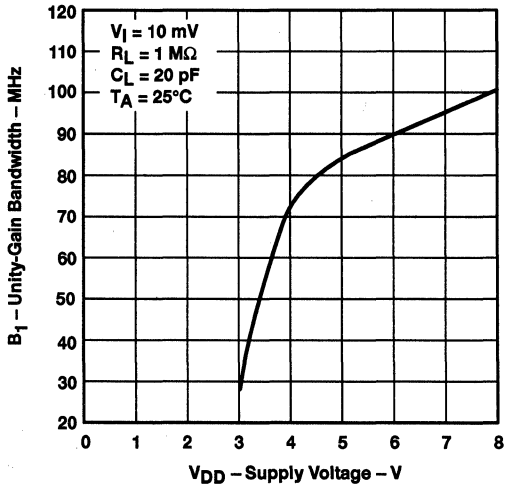


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

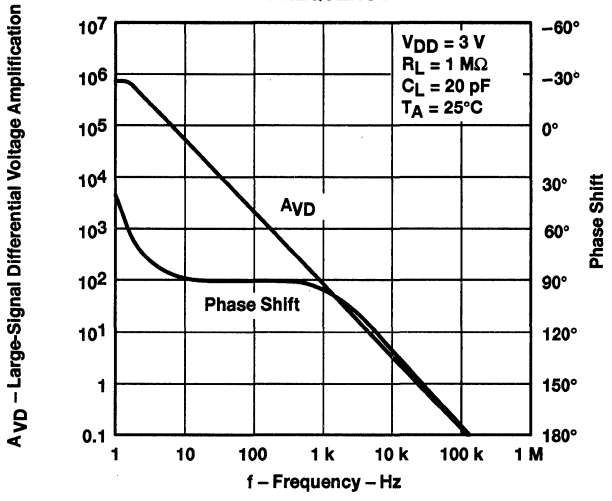


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

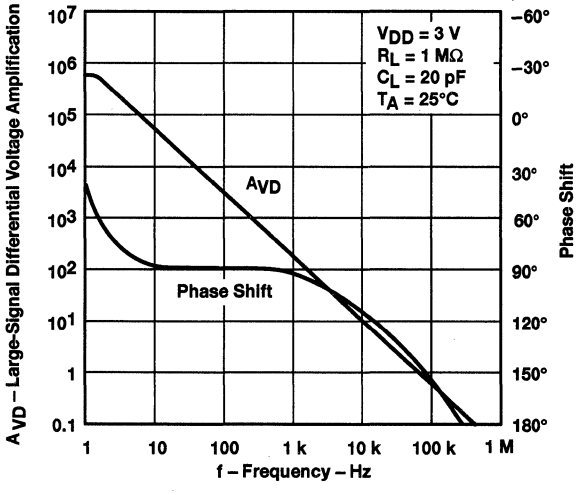


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN vs SUPPLY VOLTAGE

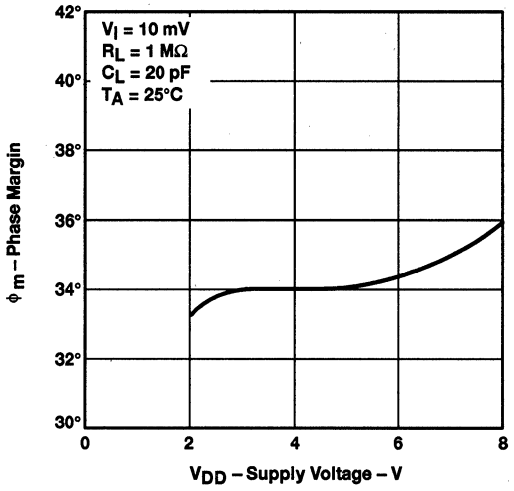


Figure 26

PHASE MARGIN vs FREE-AIR TEMPERATURE

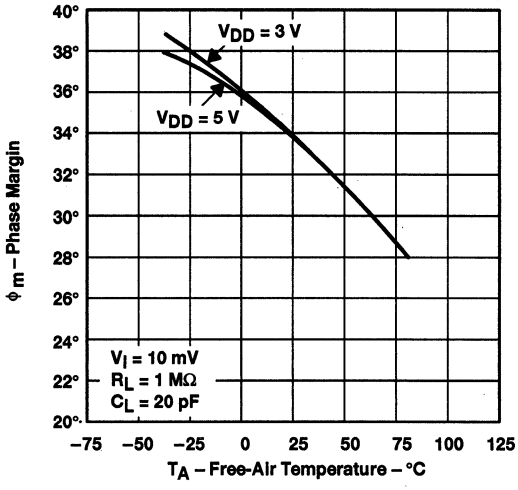


Figure 27

PHASE MARGIN vs LOAD CAPACITANCE

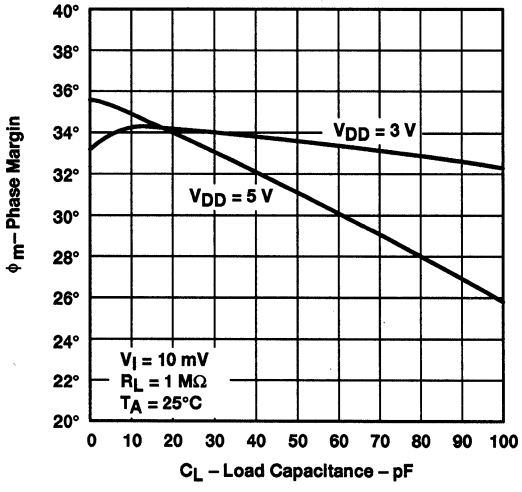


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

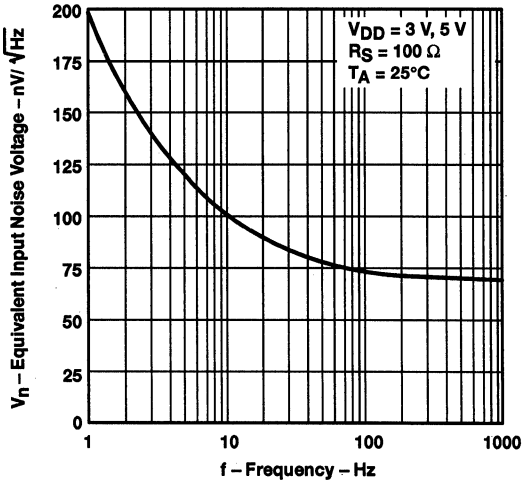
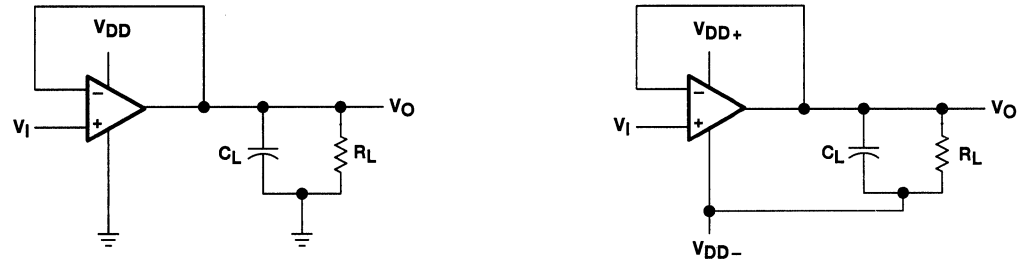


Figure 29

PARAMETER MEASUREMENT INFORMATION

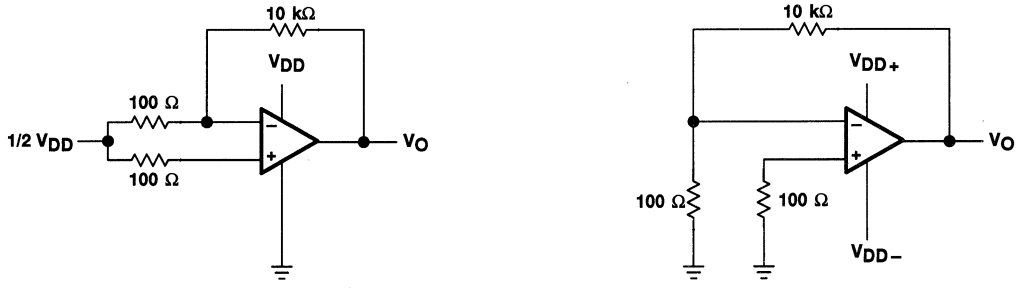
single-supply versus split-supply test circuits

Because the TLV2324 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



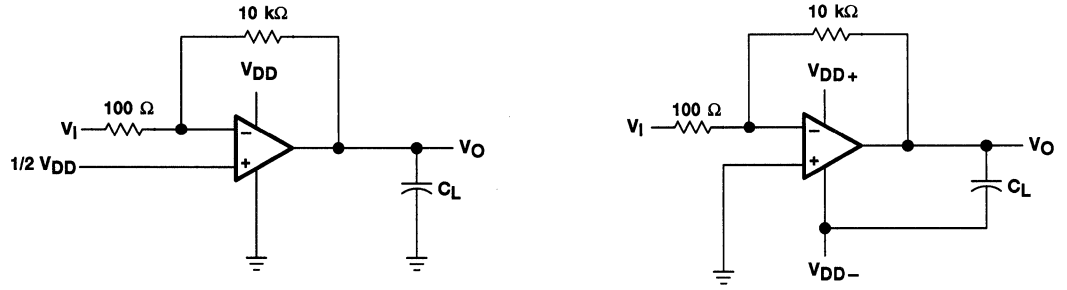
(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 30. Unity-Gain Amplifier



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 31. Noise Test Circuit



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2324 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

  Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

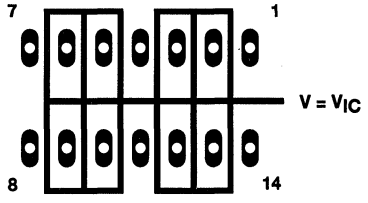


Figure 33. Isolation Metal Around Device Inputs (N Package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

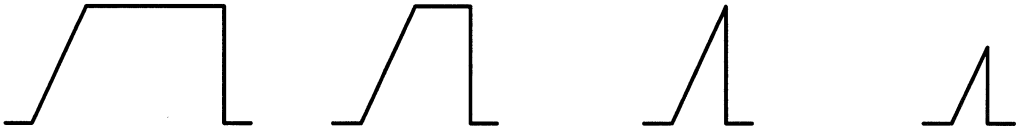


Figure 34. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2324 performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

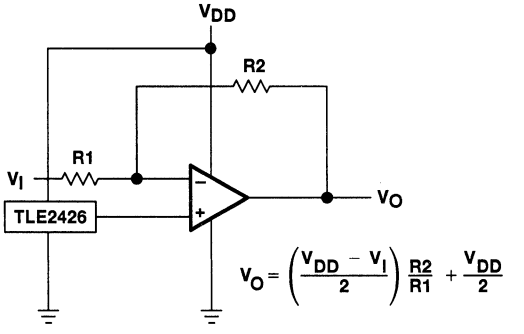


Figure 35. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)

The TLV2324 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

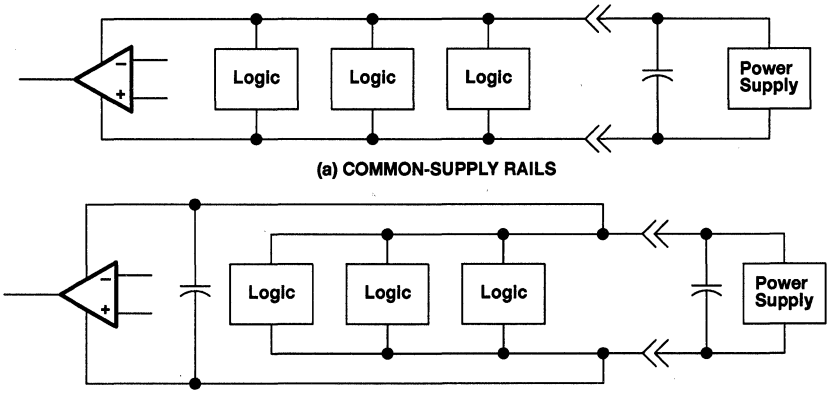


Figure 36. Common Versus Separate Supply Rails

input characteristics

The TLV2324 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.2 V at all other temperatures.

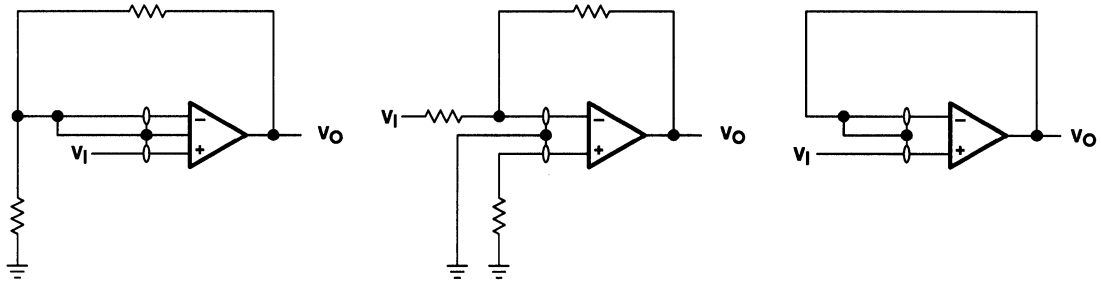
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2324 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2324 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

APPLICATION INFORMATION

input characteristics (continued)



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 37. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2324 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

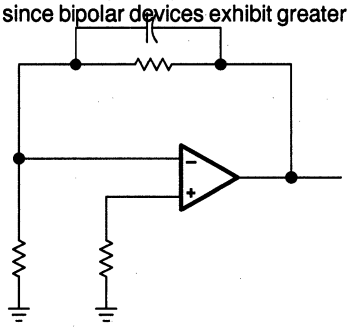


Figure 38. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV2324 incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2324 inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up; however,

APPLICATION INFORMATION

techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rail as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with the increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2324 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2324 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

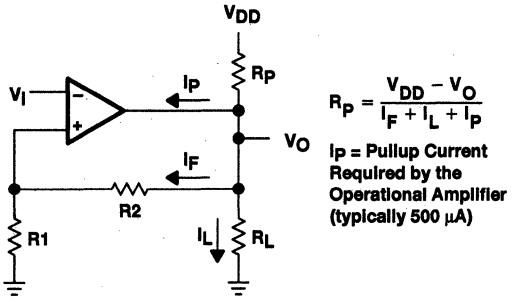


Figure 39. Resistive Pullup to Increase V_{OH}

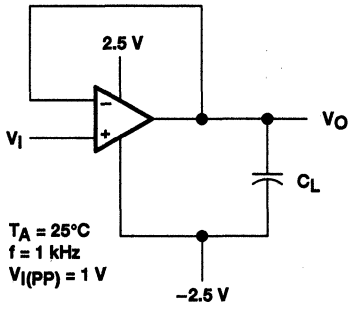
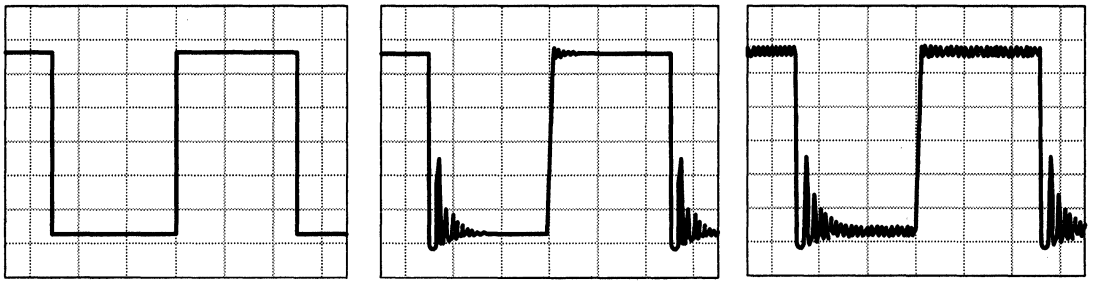


Figure 40. Test Circuit for Output Characteristics

All operating characteristics of the TLV2324 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

APPLICATION INFORMATION

output characteristics (continued)

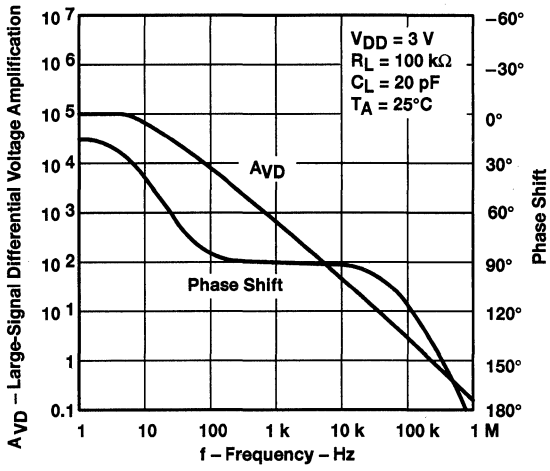


(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 260 pF, R_L = NO LOAD (c) C_L = 310 pF, R_L = NO LOAD

Figure 41. Effect of Capacitive Loads

- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  T_A = –40°C to 85°C . . . 2 V to 8 V
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} –1 V at T_A = 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY



description

The TLV2332 dual operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage single-supply applications. Unlike the TLV2322 which is optimized for ultra-low power, the TLV2332 is designed to provide a combination of low power and good ac performance. Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies. The common-mode input-voltage range includes the negative rail and extends to within 1 V of the positive rail.

Having a maximum supply current of only 310 μA per amplifier over full temperature range, the TVL2332 devices offer a combination of good ac performance and microampere supply currents. From a 3-V power supply, the amplifier's typical slew rate is 0.38 V/μs and its bandwidth is 300 kHz. These amplifiers offer a level of ac performance greater than that of many other devices operating at comparable power levels. The TLV2332 operational amplifiers are especially well suited for use in low-current or battery-powered applications.

Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon-gate LinCMOS™ technology. The LinCMOS process also features extremely high input impedance and ultra-low bias currents making these amplifiers ideal for interfacing to high-impedance sources such as sensor circuits or filter applications.

To facilitate the design of small portable equipment, the TLV2332 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline package (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 85°C	9 mV	TLV2332ID	TLV2332IP	TLV2332IPWLE	TLV2332Y

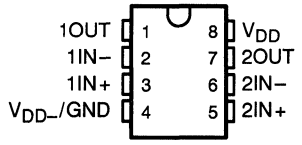
The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2332IDR).
The PW package is only available left-end taped and reeled (e.g., TLV2332IPWLE).

LinCMOS™ is a trademark of Texas Instruments Incorporated.

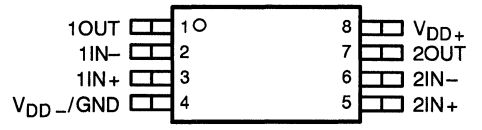
description (continued)

The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2332 incorporates internal ESD-protection circuits that prevents functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

D OR P PACKAGE
(TOP VIEW)



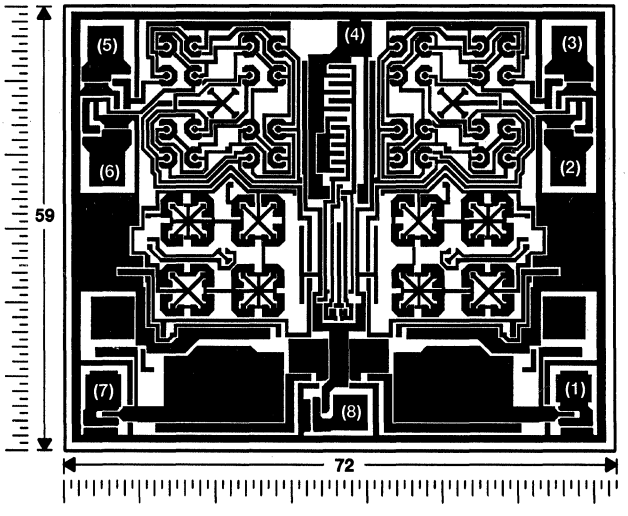
PW PACKAGE
(TOP VIEW)

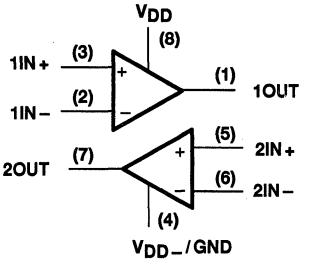


TLV2332Y chip information

This chip, when properly assembled, display characteristics similar to the TLV2332I. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

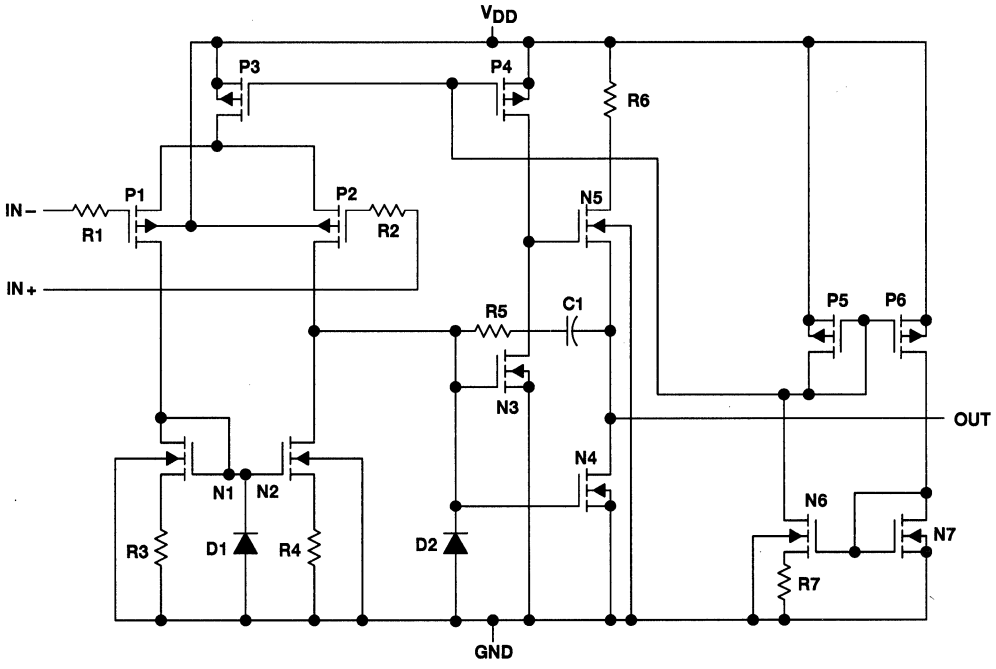
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	54
Diodes	4
Resistors	14
Capacitors	2

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... $V_{DD\pm}$
Input voltage range, V_I (any input) ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
Output current, I_O ..... ±30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	−0.2	1.8	V
	V_{DD} = 5 V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2332I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.6	9		1.1	9	mV
			Full range			11			11	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.9		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 100 kΩ, See Note 6	25°C	25	83		25	170		V/mV
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	92		65	91		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	94		70	94		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		160	500		210	560	μA
			Full range			620			800	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2332I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, See Figure 30	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		0.38		V/μs
				85°C		0.29		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 30	25°C		34		kHz
				85°C		32		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 100 kΩ,	C_L = 20 pF, See Figure 32	25°C		300		kHz
				85°C		235		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 100 kΩ,	−40°C		42°		
				25°C		39°		
				85°C		36°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2332I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, C_L = 20 pF, See Figure 30	$V_{I(PP)}$ = 1 V	25°C		0.43		V/μs
				85°C		0.35		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 30	25°C		55		kHz
				85°C		45		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 100 kΩ,	C_L = 20 pF, See Figure 32	25°C		525		kHz
				85°C		370		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 100 kΩ,	−40°C		43°		
				25°C		40°		
				85°C		38°		

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLV2332Y						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, R_S = 50 Ω,	V_{IC} = 1 V, R_L = 100 kΩ		0.6	9		1.1	9	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)			−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, I_{OH} = −1 mA	V_{ID} = 100 mV,	1.75	1.9		3.2	3.9		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, I_{OL} = 1 mA	V_{ID} = 100 mV,		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, See Note 6	R_L = 100 kΩ,	25	83		25	170		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, R_S = 50 Ω	V_{IC} = V_{ICR}min,	65	92		65	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	V_O = 1 V, R_S = 50 Ω	V_{IC} = 1 V,	70	94		70	94		dB
I_{DD}	Supply current	V_O = 1 V, No load	V_{IC} = 1 V,		160	500		210	560	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current	5
		vs Supply voltage	6
		vs Temperature	7
V_{OL}	Low-level output voltage	vs Common-mode input voltage	8
		vs Temperature	9, 11
		vs Differential input voltage	10
		vs Low-level output current	12
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage	13
		vs Temperature	14
I_{IB} /I_{IO}	Input bias and offset currents	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply voltage	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
SR	Slew rate	vs Supply voltage	19
		vs Temperature	20
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Unity-gain bandwidth	vs Temperature	22
		vs Supply voltage	23
A_{VD}	Large-signal differential voltage amplification and phase shift	vs Frequency	24, 25
ϕ_m	Phase margin	vs Supply voltage	26
		vs Temperature	27
		vs Load capacitance	28
V_n	Equivalent input noise voltage	vs Frequency	29
	Phase shift	vs Frequency	24, 25

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2332
INPUT OFFSET VOLTAGE

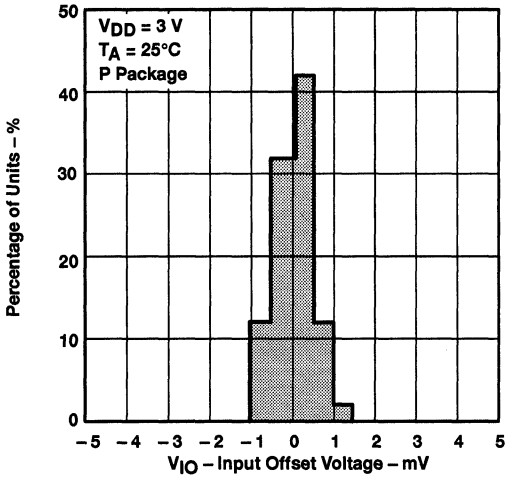


Figure 1

DISTRIBUTION OF TLV2332
INPUT OFFSET VOLTAGE

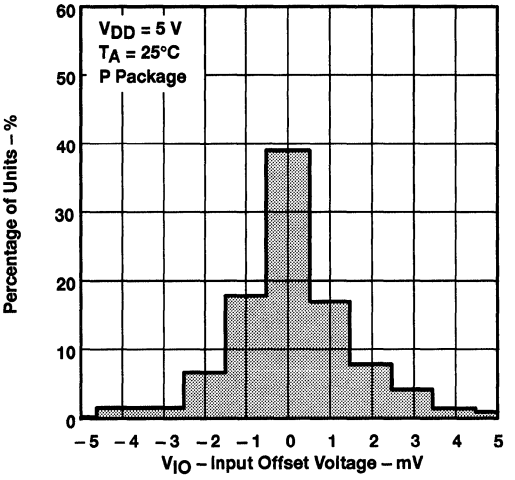


Figure 2

DISTRIBUTION OF TLV2332
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

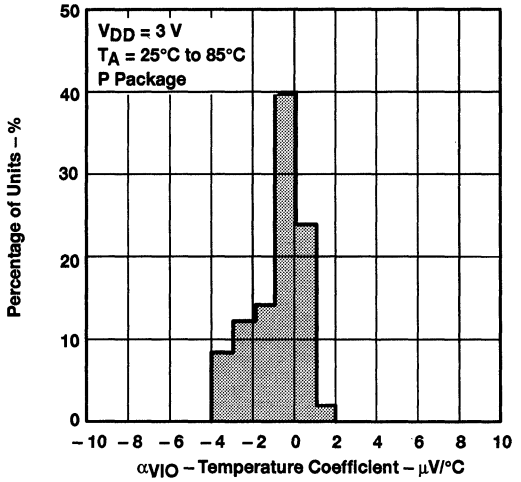


Figure 3

DISTRIBUTION OF TLV2332
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

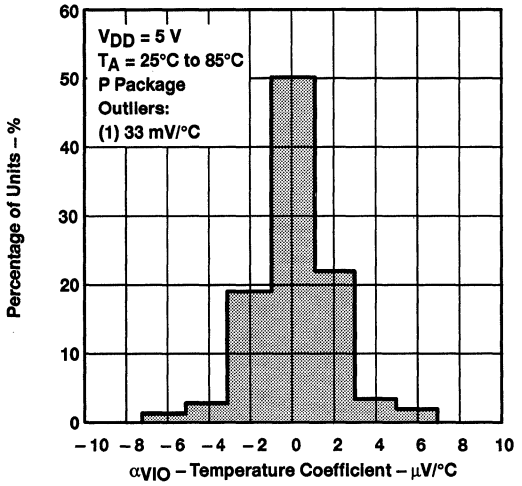


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

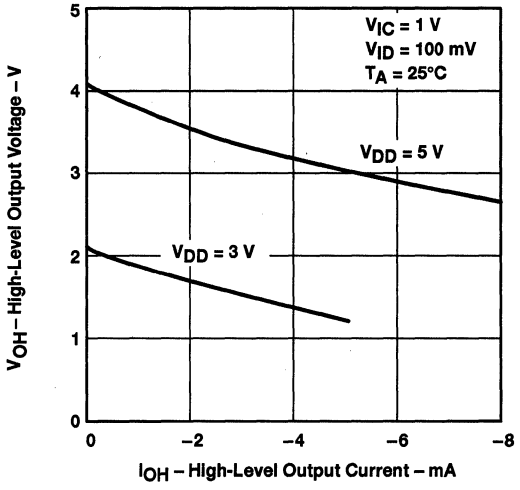


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

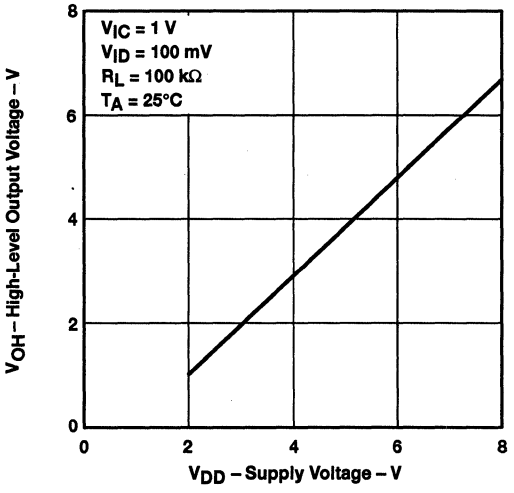


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

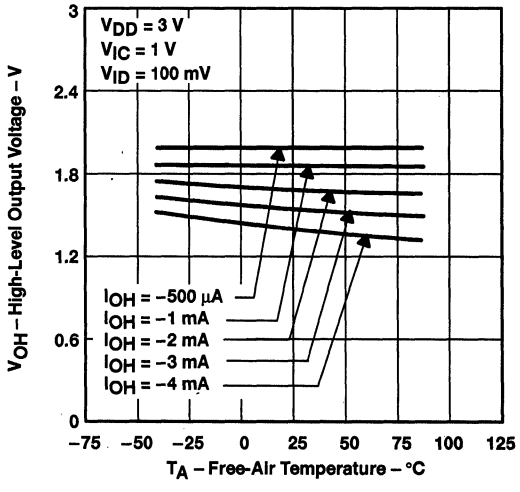


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

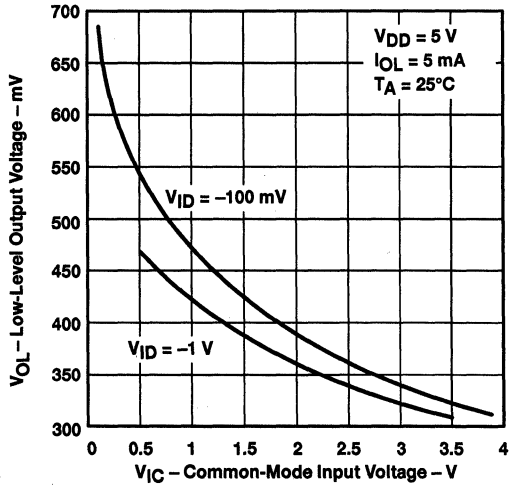


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

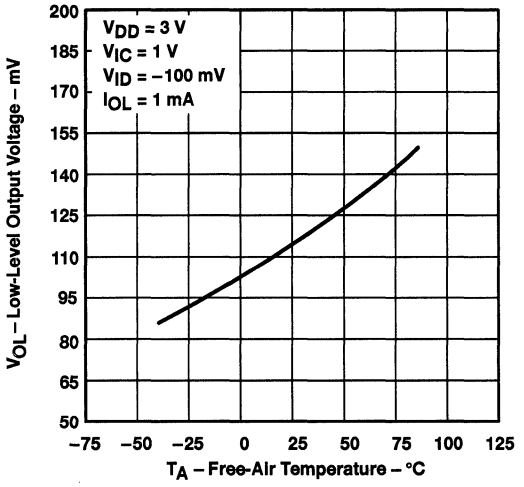


Figure 9

LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

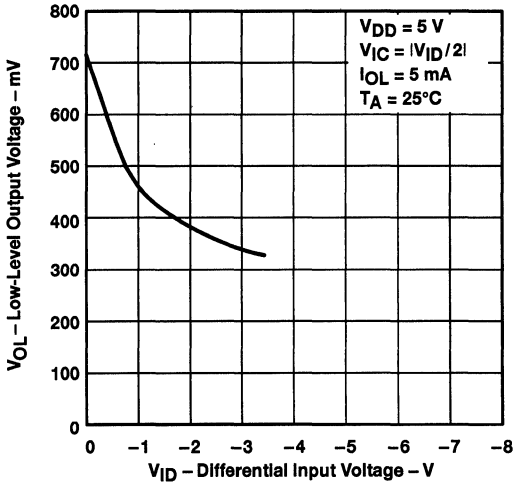


Figure 10

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

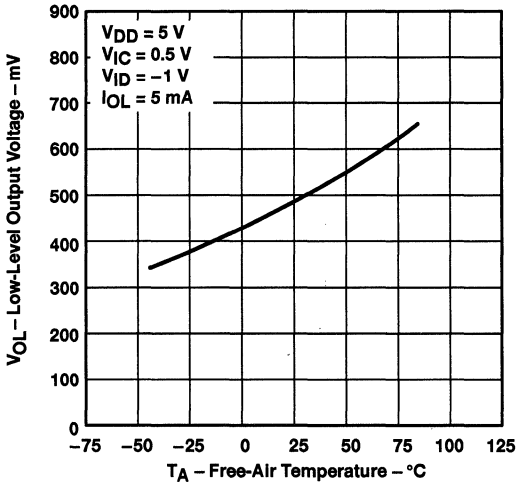


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

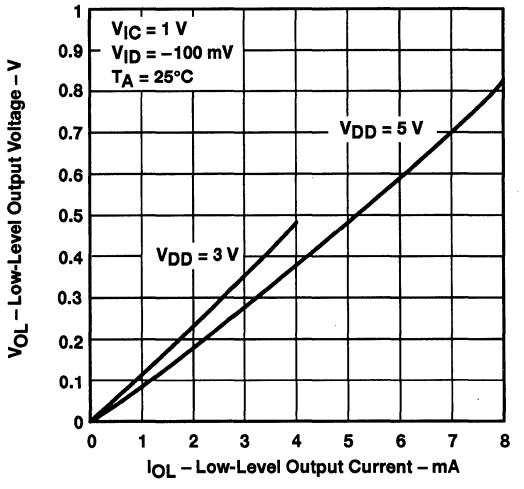


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

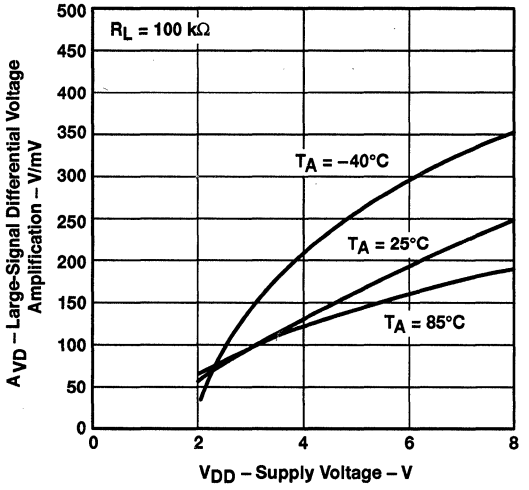


Figure 13

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

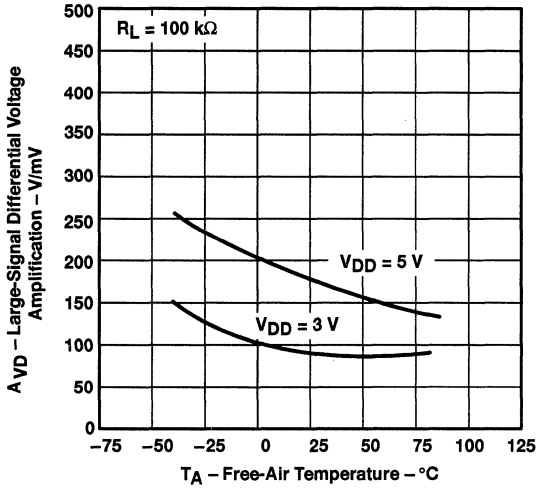
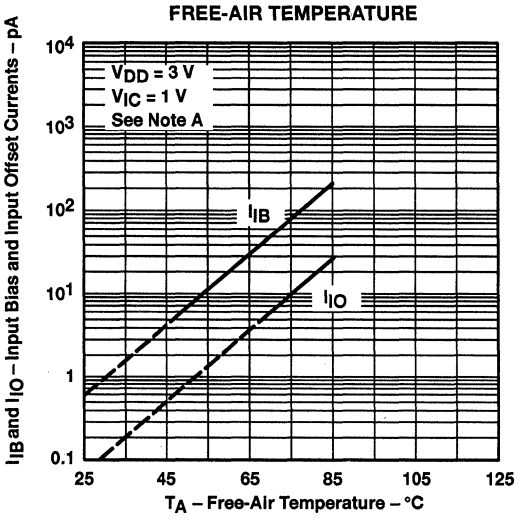


Figure 14

INPUT BIAS CURRENT AND INPUT
OFFSET CURRENT
vs
FREE-AIR TEMPERATURE



NOTE: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 15

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

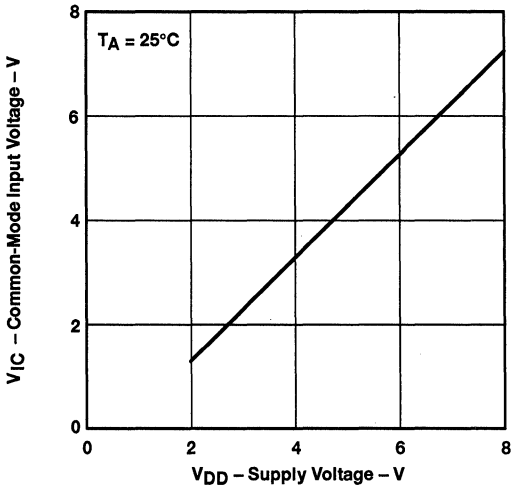


Figure 16

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

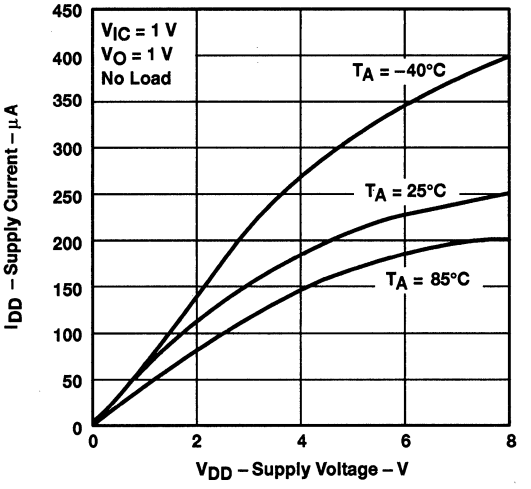


Figure 17

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

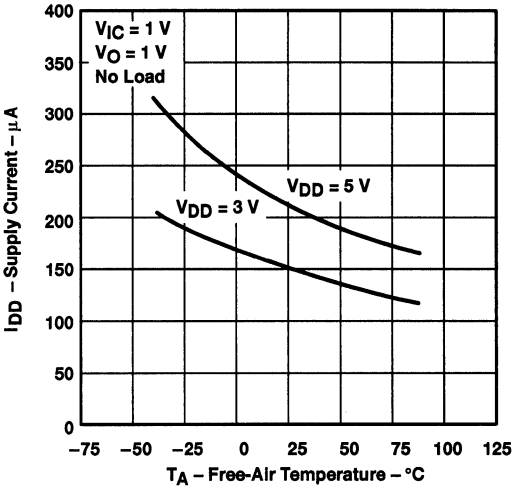


Figure 18

SLEW RATE vs SUPPLY VOLTAGE

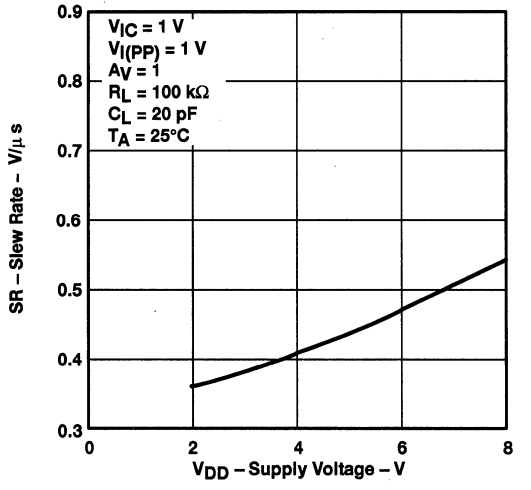


Figure 19

SLEW RATE vs FREE-AIR TEMPERATURE

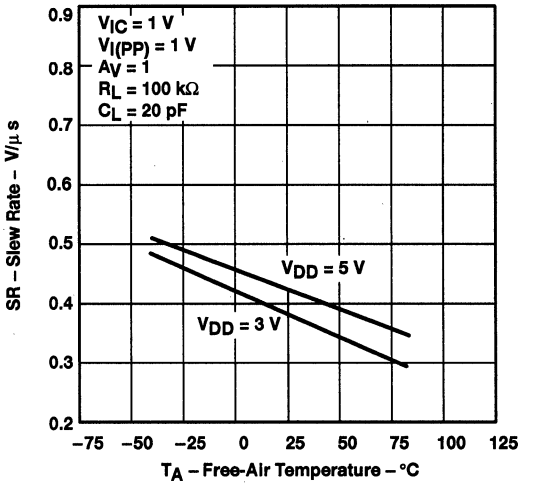


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

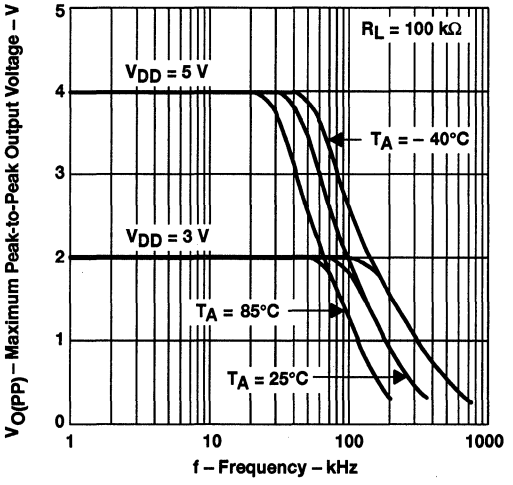


Figure 21

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

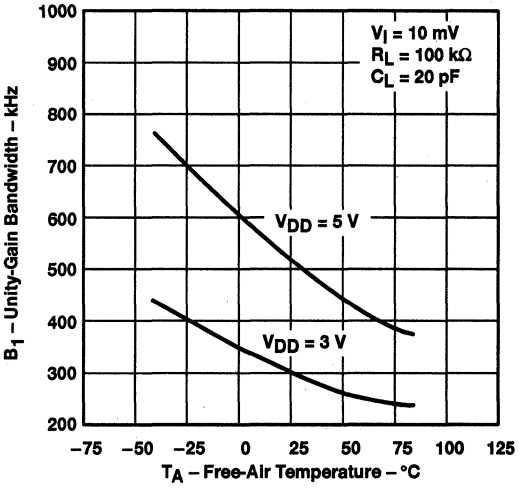


Figure 22

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

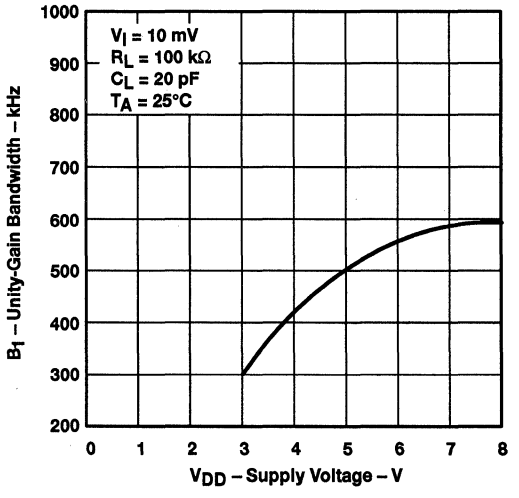


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

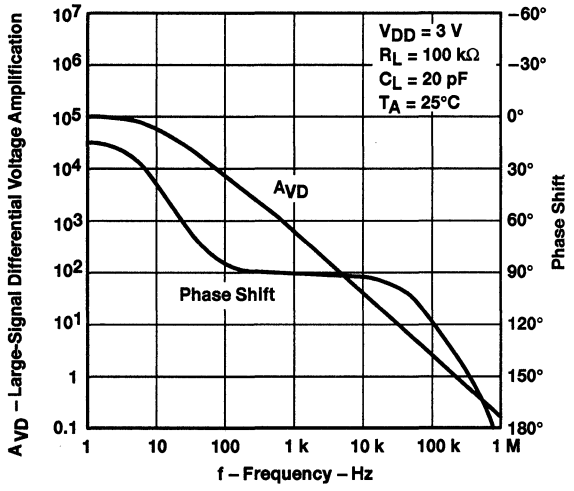


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

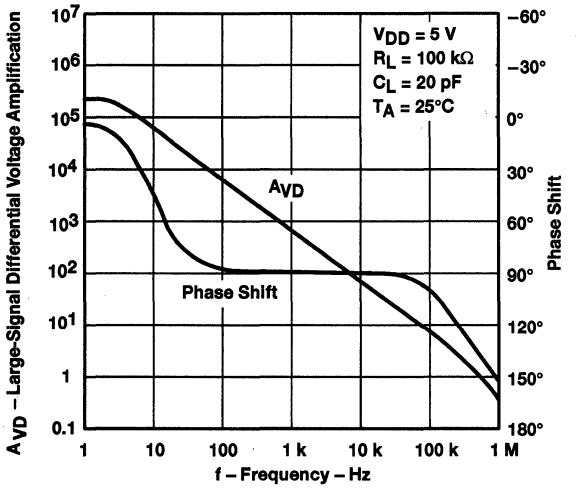


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

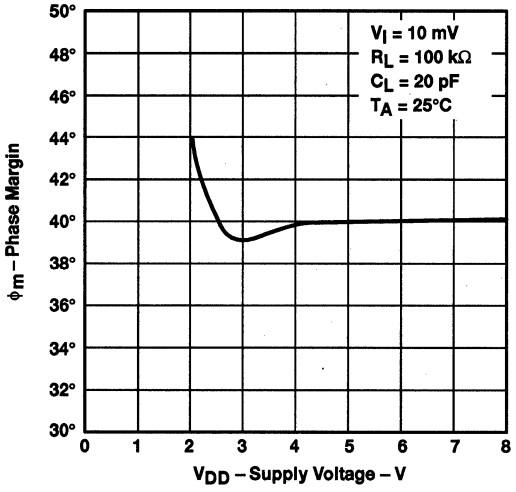


Figure 26

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

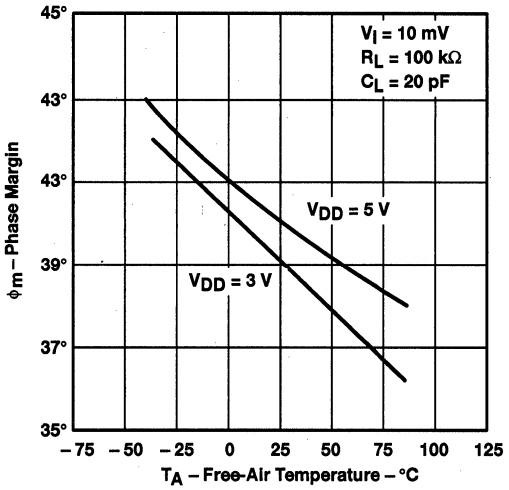


Figure 27

PHASE MARGIN
vs
LOAD CAPACITANCE

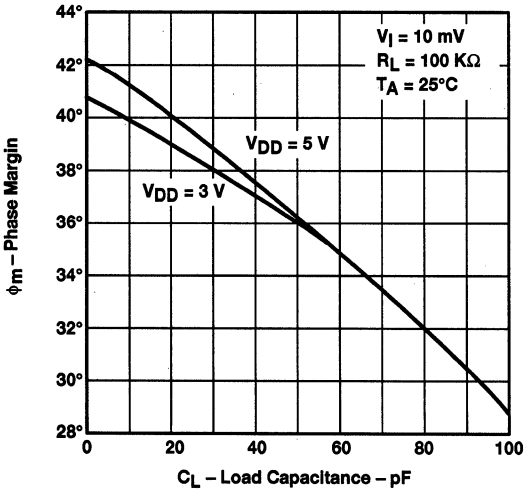


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

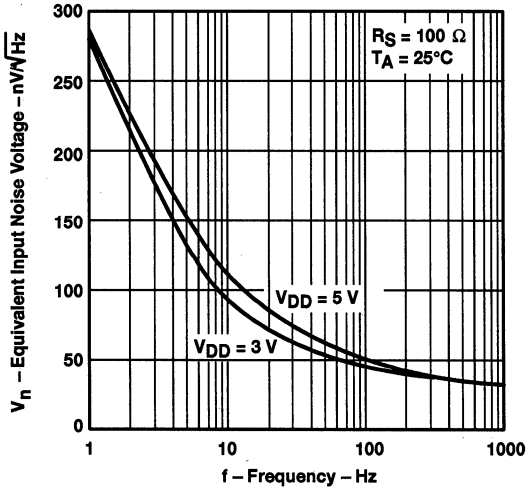
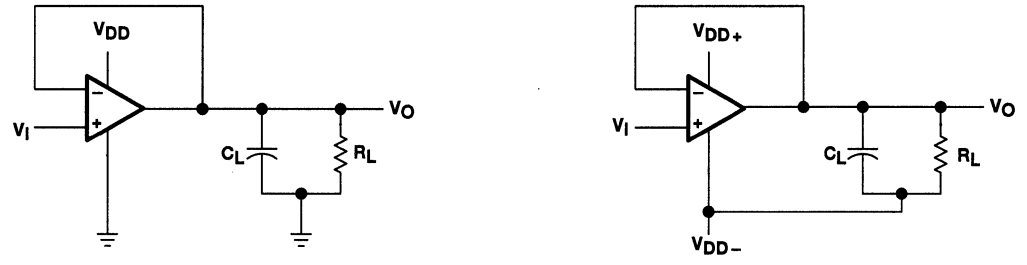


Figure 29

PARAMETER MEASUREMENT INFORMATION

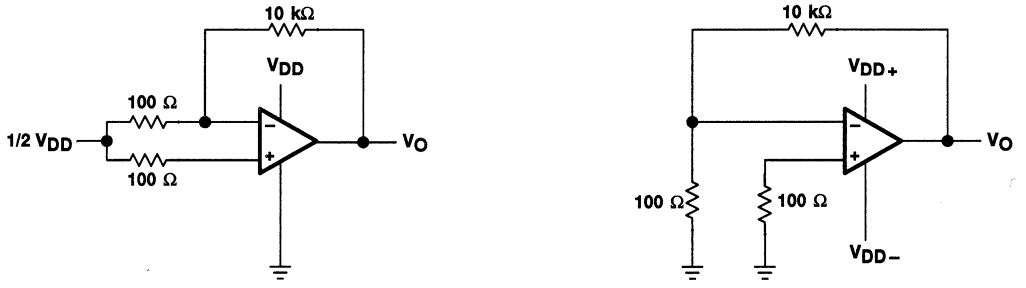
single-supply versus split-supply test circuits

Because the TLV2332 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



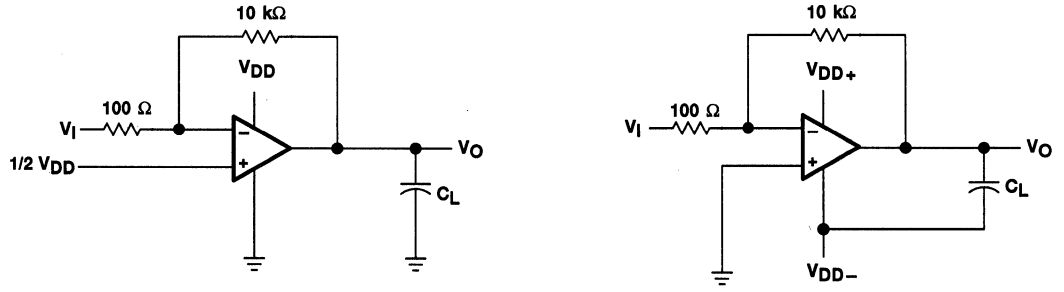
(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 30. Unity-Gain Amplifier



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 31. Noise Test Circuit



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2332 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

  Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

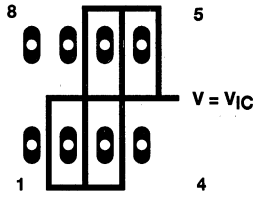


Figure 33. Isolation Metal Around Device Inputs
(P Package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

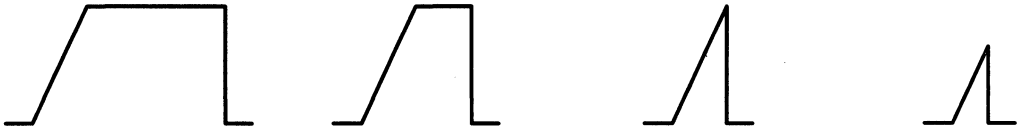


Figure 34. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2332 performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

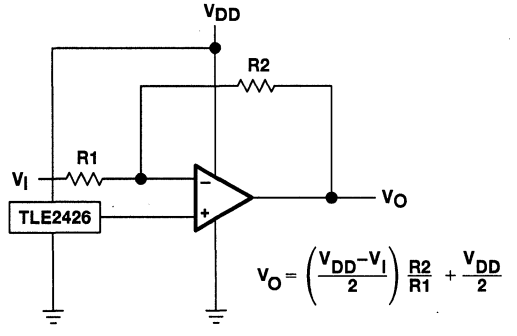


Figure 35. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)

The TLV2332 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

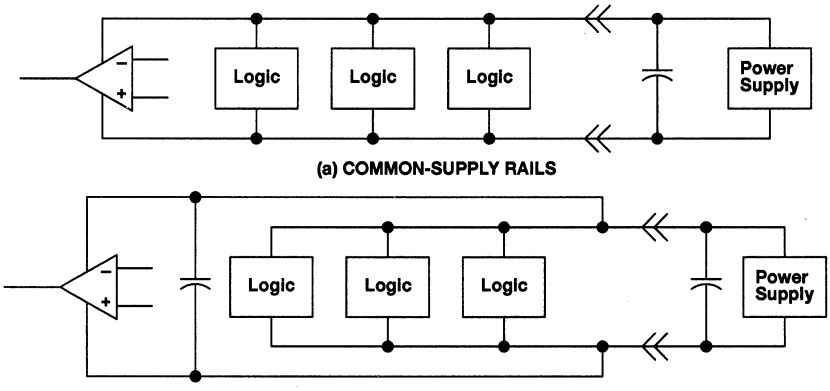


Figure 36. Common Versus Separate Supply Rails

input characteristics

The TLV2332 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower the range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.2 V at all other temperatures.

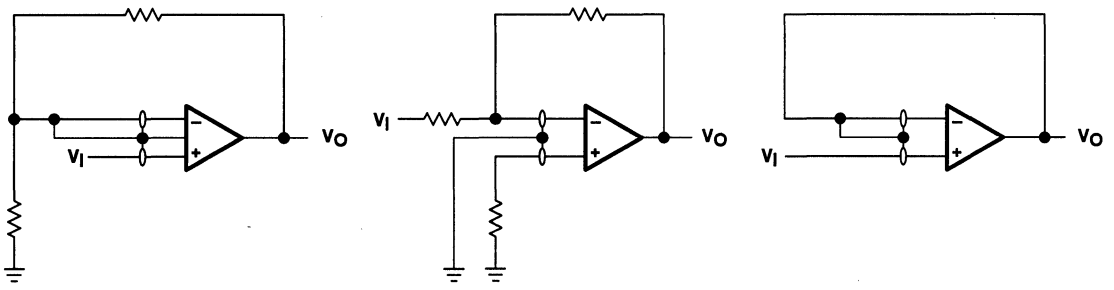
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2332 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2332 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

APPLICATION INFORMATION

input characteristics (continued)



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 37. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifiers circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2332 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifiers circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

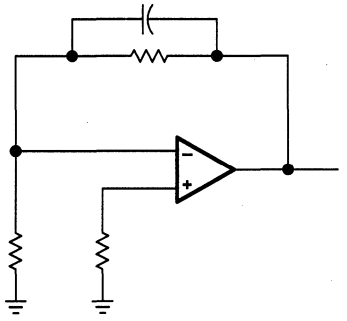


Figure 38. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV2332 incorporates an internal electro-static-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C. Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2332 inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up; however,

APPLICATION INFORMATION

techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2332 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2332 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

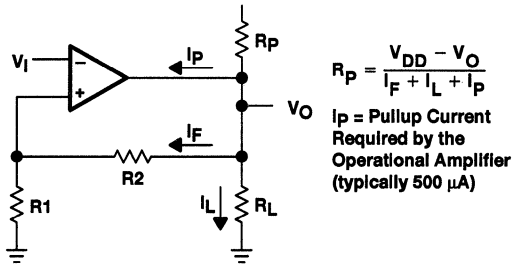


Figure 39. Resistive Pullup to Increase V_{OH}

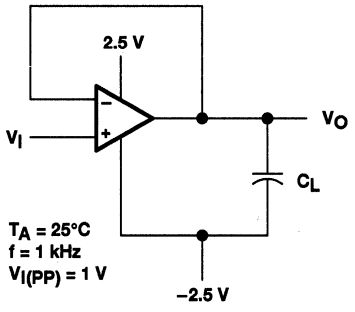
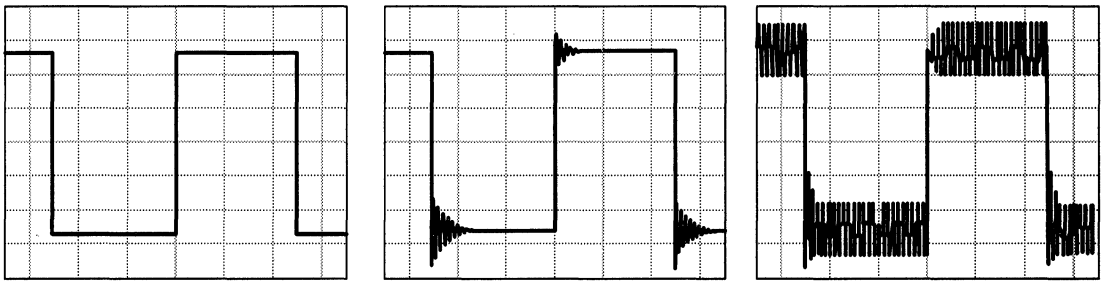


Figure 40. Test Circuit for Output Characteristics

All operating characteristics of the TLV2332 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

APPLICATION INFORMATION

output characteristics (continued)



(a) C_L = 20 pF, R_L = NO LOAD

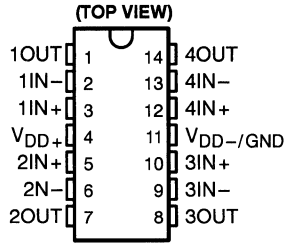
(b) C_L = 170 pF, R_L = NO LOAD

(c) C_L = 190 pF, R_L = NO LOAD

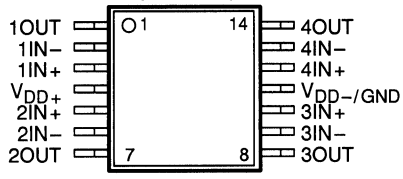
Figure 41. Effect of Capacitive Loads

- **Wide Range of Supply Voltages Over Specified Temperature Range: T_A = –40°C to 85°C . . . 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} –1 V at T_A = 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**

D OR N PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



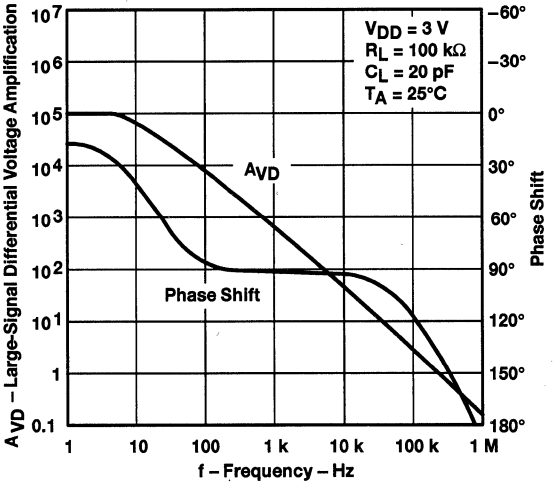
description

The TLV2344 quad operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage, single-supply applications. Unlike the TLV2324 which is optimized for ultra-low power, the TLV2334 is designed to provide a combination of low power and good ac performance. Each amplifier is fully functional down to a minimum supply voltage of 2 V and is fully characterized, tested, and specified at both 3-V and 5-V power supplies over a temperature range of –40°C to 85°C. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

Having a maximum supply current of only 300 μA per amplifier over full temperature range, the TLV2334 devices offer a combination of good ac performance and microampere supply currents. From a 3-V power supply, the amplifier's typical slew rate is 0.38 V/μs and its bandwidth is 300 kHz. These amplifiers offer a level of ac performance greater than that of many other devices operating at comparable power levels.

The TLV2334 operational amplifiers are especially well suited for use in low current or battery-powered applications.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
–40°C to 85°C	10 mV	TLV2334ID	TLV2334IN	TLV2334IPWLE	TLV2334Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2334IDR).
The PW package is only available left-end taped and reeled (e.g., TLV2334IPWLE).

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description (continued)

Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon-gate LinCMOS technology. The LinCMOS process also features extremely high input impedance and ultra-low input bias currents making them ideal for interfacing to high-impedance sources such as in sensor circuits or filter applications.

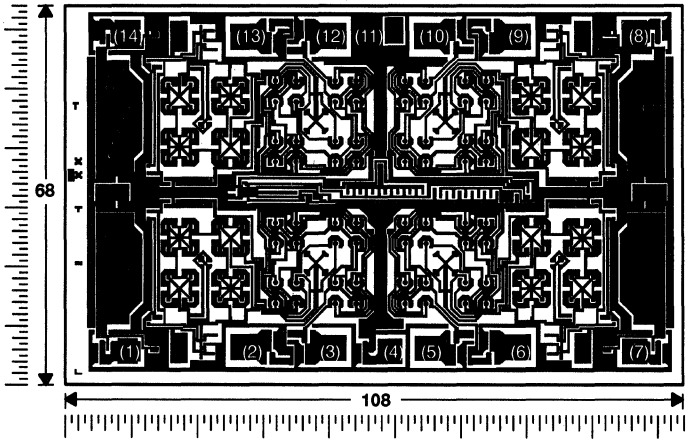
To facilitate the design of small portable equipment, the TLV2334 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

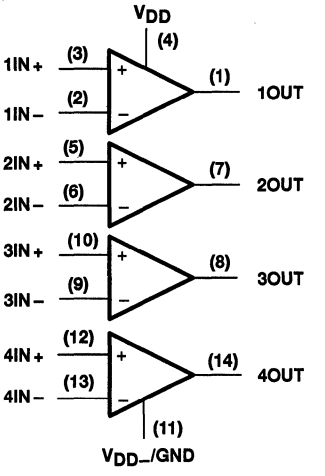
The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2334 incorporates internal ESD-protection circuits that prevents functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

TLV2334Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2334I. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

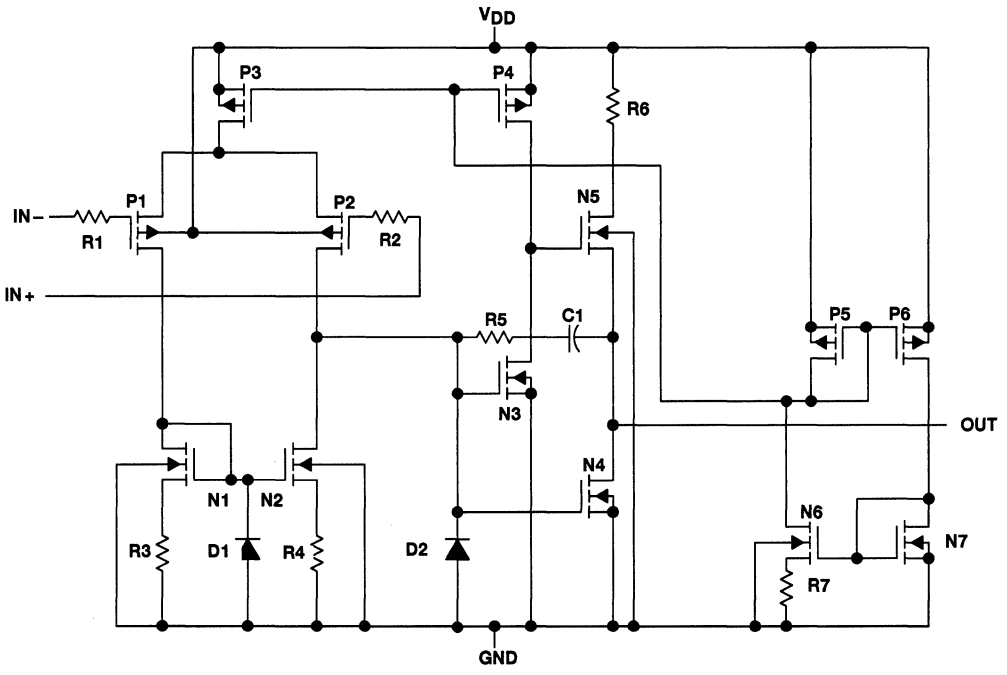
BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	108
Diodes	8
Resistors	28
Capacitors	4

† Includes all amplifiers, ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD}, (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... $V_{DD\pm}$
Input voltage, range V_I (any input) ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
Output current, I_O ..... ±30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mV	7.6 mW/°C	494 mW
N	1575 mV	12.6 mW/°C	819 mW
PW	700 mV	5.6 mW/°C	364 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	−0.2	1.8	V
	V_{DD} = 5 V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

TEXAS INSTRUMENTS
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electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2334I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.6	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.9		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 100 kΩ, See Note 6	25°C	25	83		25	170		V/mV
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	92		65	91		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	94		70	94		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		320	1000		420	1120	μA
			Full range			1200			1600	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2334I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, See Figure 30	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		0.38		V/μs
				85°C		0.29		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 30	25°C		34		kHz
				85°C		32		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 100 kΩ,	C_L = 20 pF, See Figure 32	25°C		300		kHz
				85°C		235		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 100 kΩ,	−40°C		42°		
				25°C		39°		
				85°C		36°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2334I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, C_L = 20 pF, See Figure 30	$V_{I(PP)}$ = 1 V	25°C		0.43		V/μs
				85°C		0.35		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 30	25°C		55		kHz
				85°C		45		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 100 kΩ,	C_L = 20 pF, See Figure 32	25°C		525		kHz
				85°C		370		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 100 kΩ,	−40°C		43°		
				25°C		40°		
				85°C		38°		

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLV2334Y						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, R_S = 50 Ω,	V_{IC} = 1 V R_L = 100 kΩ		0.6	10		1.1	10	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)			−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, I_{OH} = −1 mA	V_{ID} = 100 mV,	1.75	1.9		3.2	3.9		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, I_{OL} = 1 mA	V_{ID} = −100 mV,		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, See Note 6	R_L = 100 kΩ,	25	83		25	170		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, R_S = 50 Ω	V_{IC} = V_{ICR}min,	65	92		65	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	V_{IC} = 1 V, R_S = 50 Ω	V_O = 1 V,	70	94		70	94		dB
I_{DD}	Supply current	V_O = 1 V, No load	V_{IC} = 1 V,		320	1000		420	1120	μA

NOTES: 4. The typical values of input bias current offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current	5
		vs Supply voltage	6
		vs Temperature	7
V_{OL}	Low-level output voltage	vs Common-mode input voltage	8
		vs Temperature	9, 11
		vs Differential input voltage	10
		vs Low-level output current	12
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage	13
		vs Temperature	14
I_{IB}/I_{IO}	Input bias and offset currents	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply current	16
I_{DD}	Supply current	vs Supply current	17
		vs Temperature	18
SR	Slew rate	vs Supply voltage	19
		vs Temperature	20
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Unity-gain bandwidth	vs Temperature	22
		vs Supply voltage	23
A_{VD}	Large-signal differential voltage amplification	vs Frequency	24, 25
ϕ_m	Phase margin	vs Supply voltage	26
		vs Temperature	27
		vs Load capacitance	28
V_n	Equivalent input noise voltage	vs Frequency	29
	Phase shift	vs Frequency	24, 25

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2334
INPUT OFFSET VOLTAGE

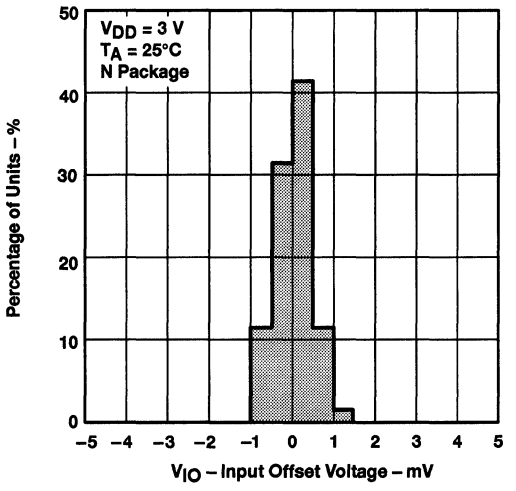


Figure 1

DISTRIBUTION OF TLV2334
INPUT OFFSET VOLTAGE

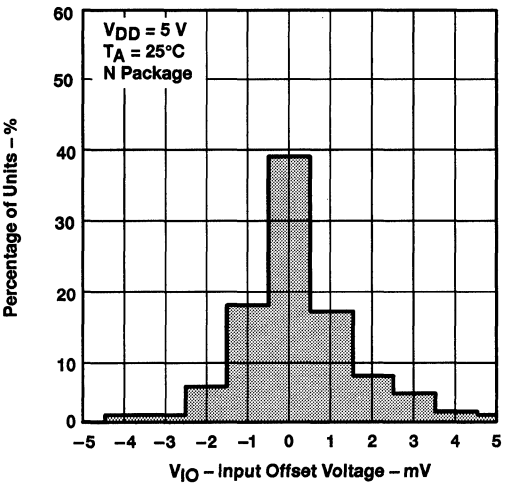


Figure 2

DISTRIBUTION OF TLV2334
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

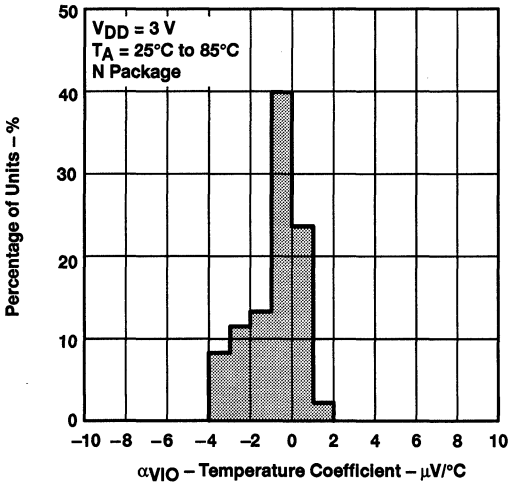


Figure 3

DISTRIBUTION OF TLV2334
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

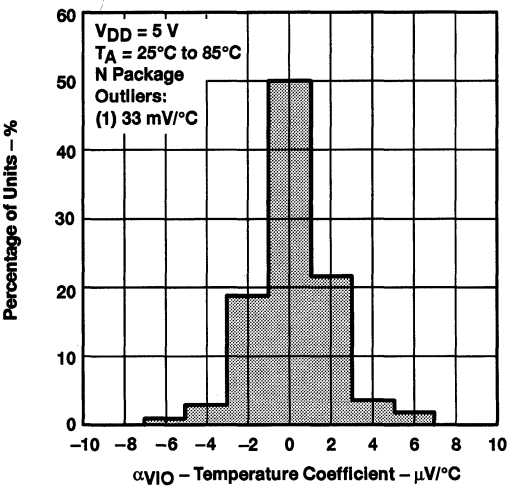


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

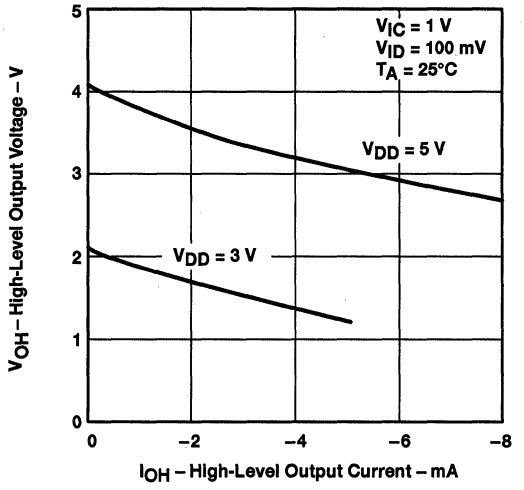


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

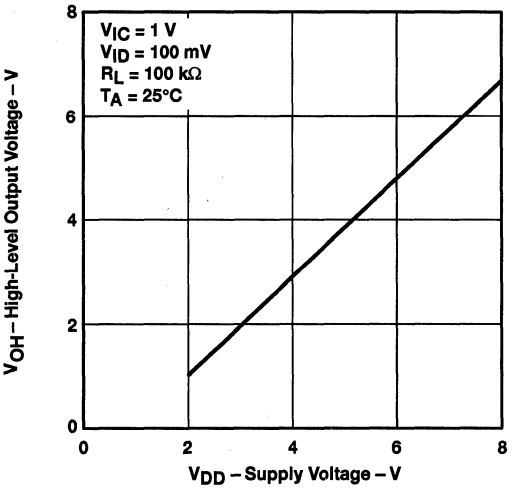


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

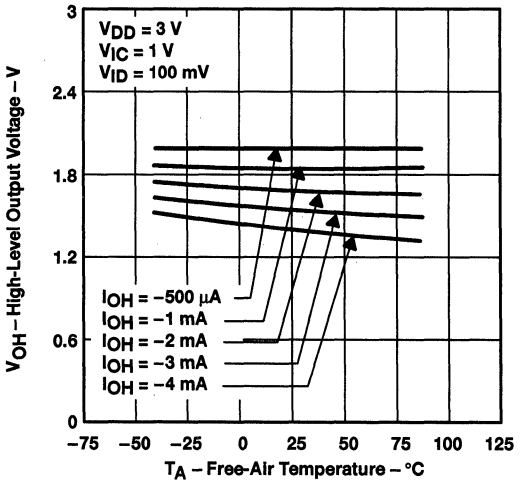


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

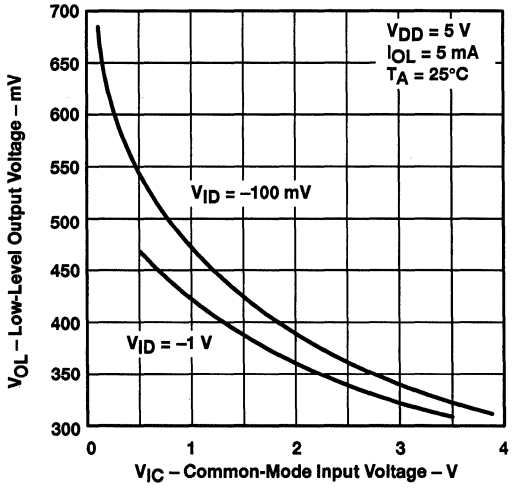


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

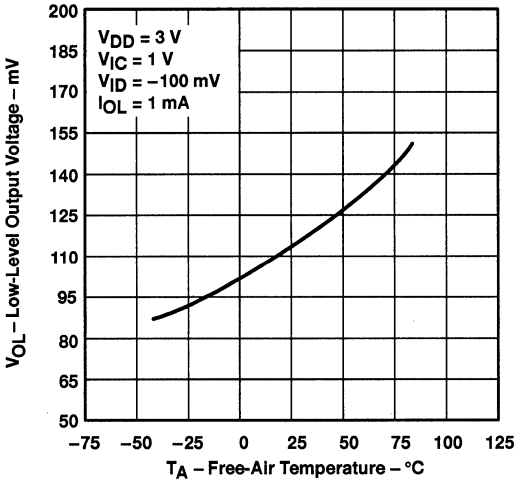


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

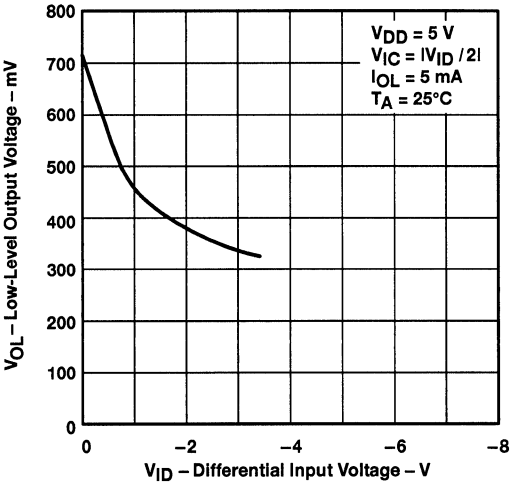


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

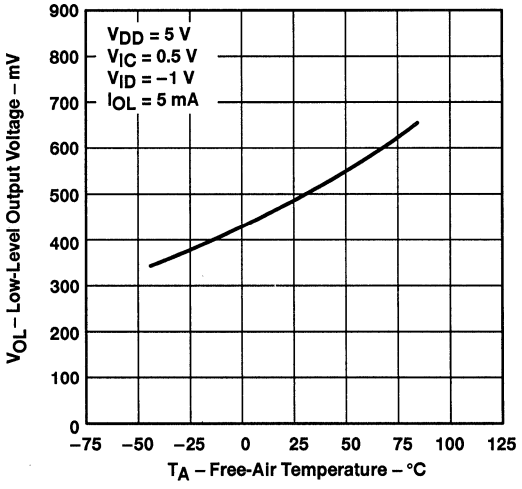


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

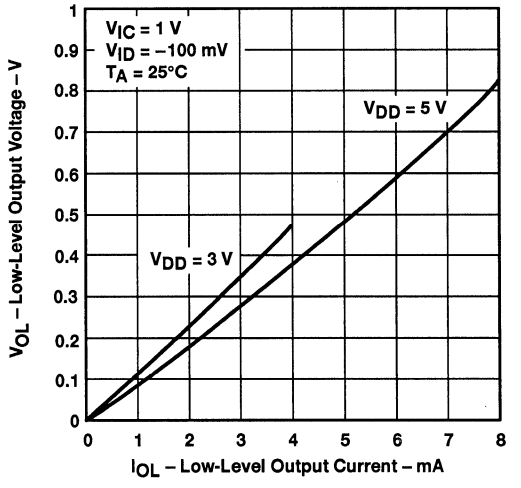


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

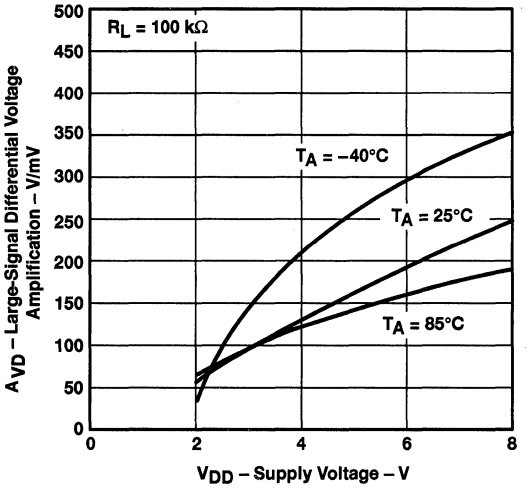


Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

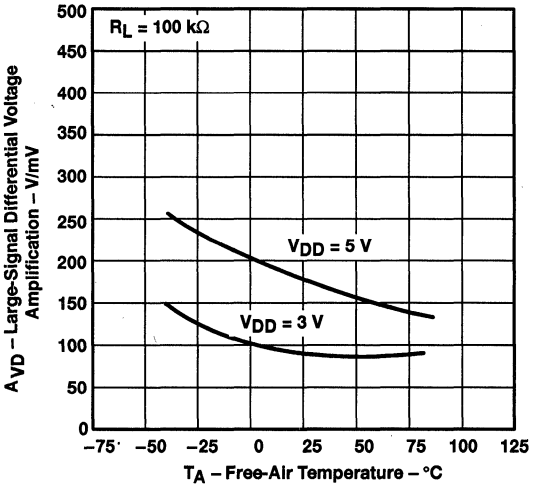


Figure 14

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

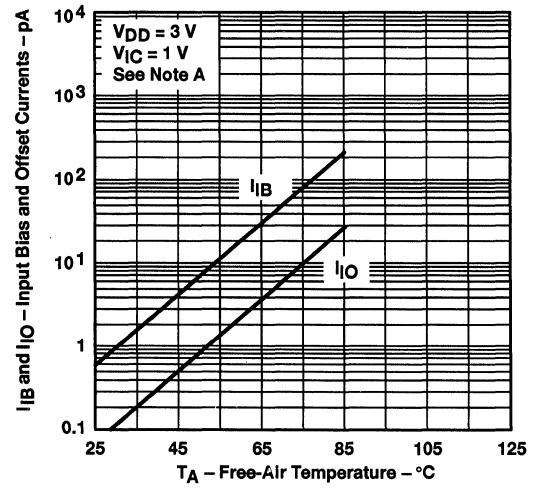


Figure 15

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE

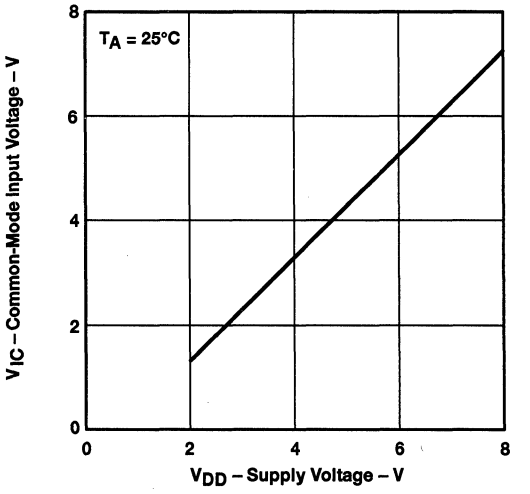


Figure 16

NOTE A: The typical values of input bias current and input offset current below 5 pA are determined mathematically.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

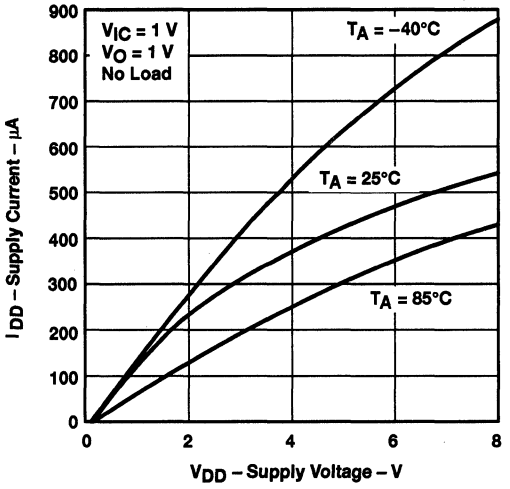


Figure 17

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

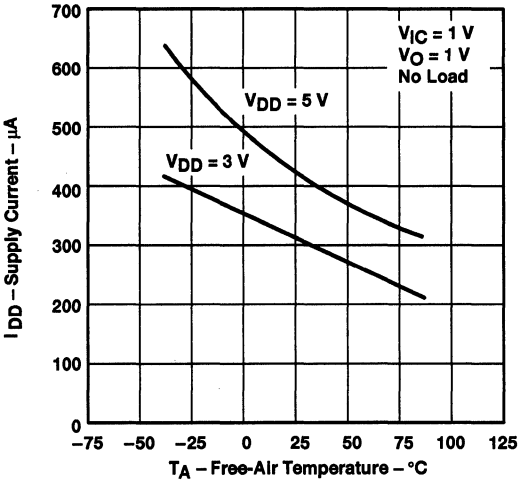


Figure 18

SLEW RATE vs SUPPLY VOLTAGE

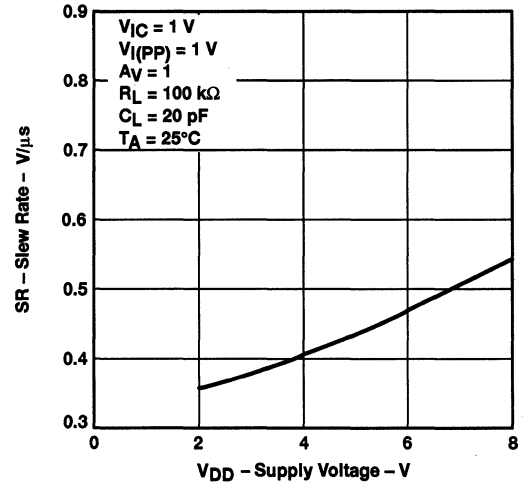


Figure 19

SLEW RATE vs FREE-AIR TEMPERATURE

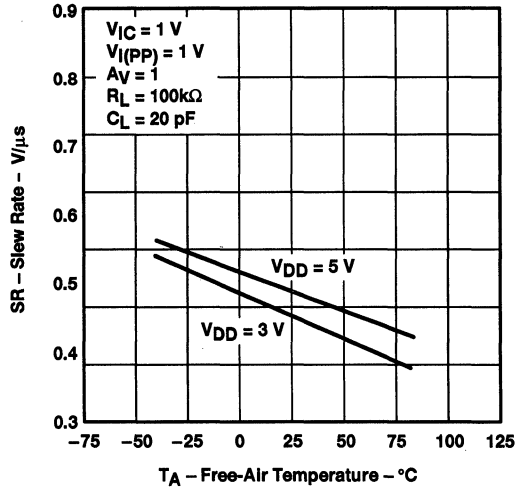


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

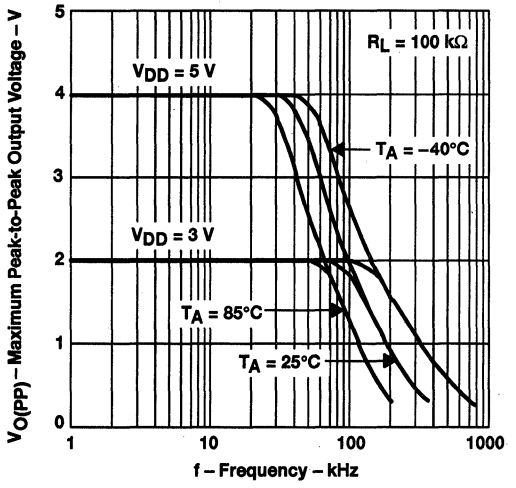


Figure 21

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

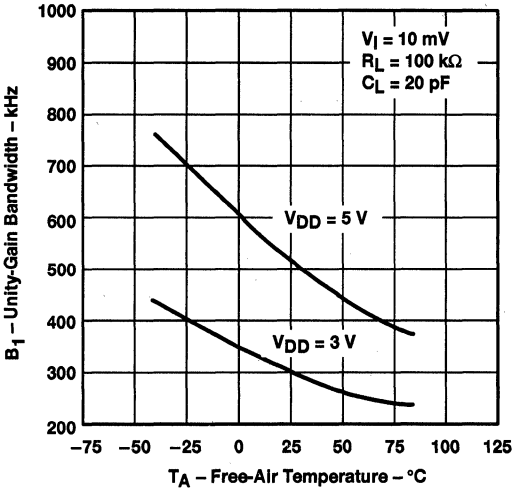


Figure 22

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

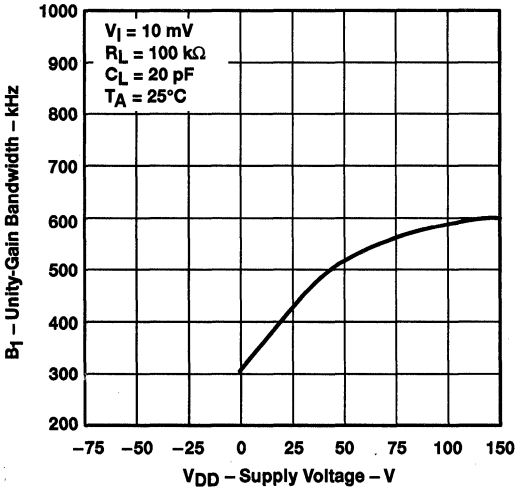


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

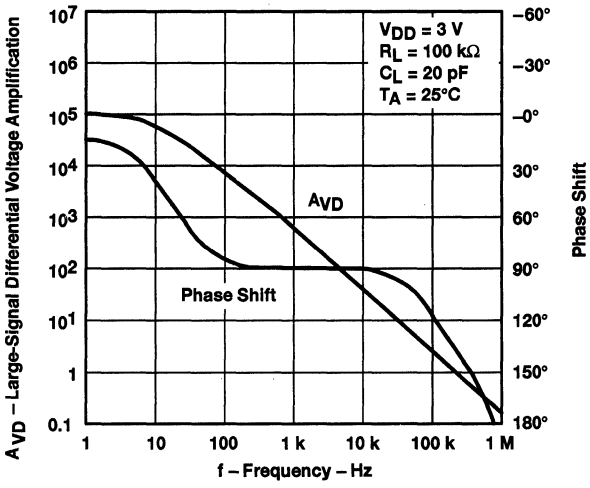


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

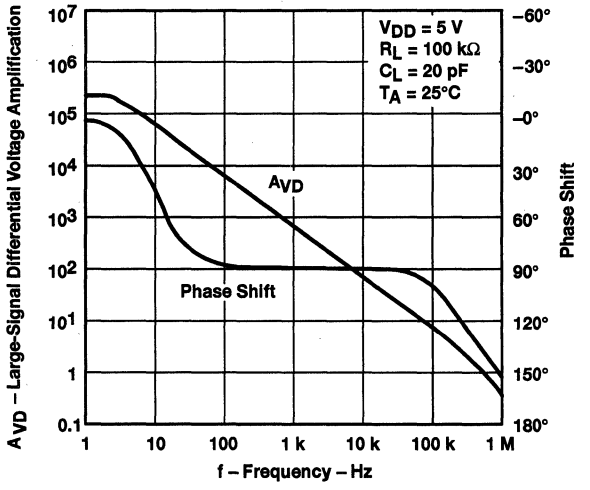


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

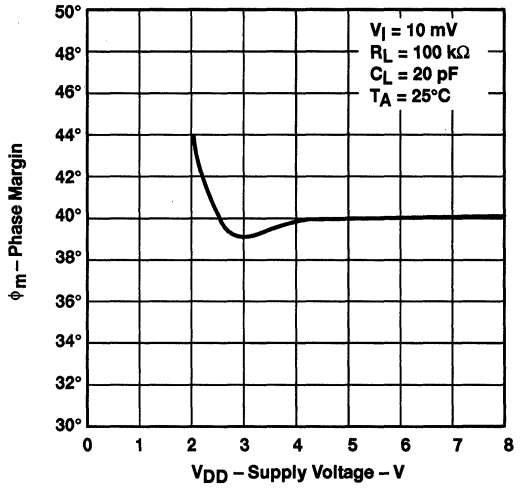


Figure 26

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

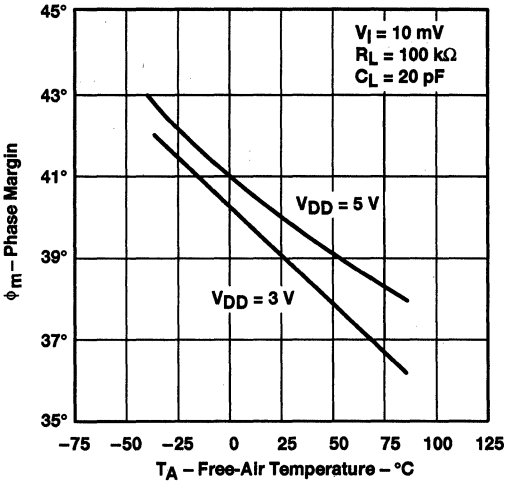


Figure 27

PHASE MARGIN
vs
LOAD CAPACITANCE

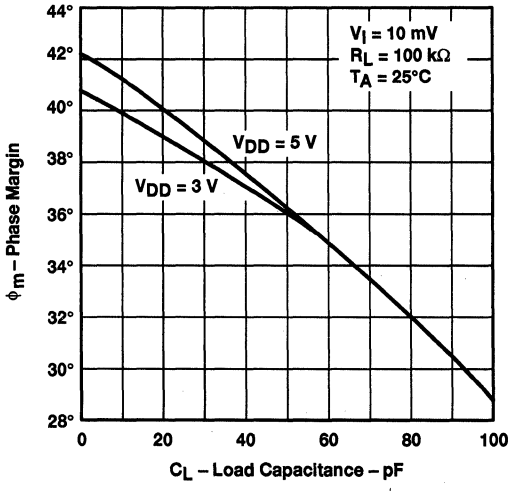


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

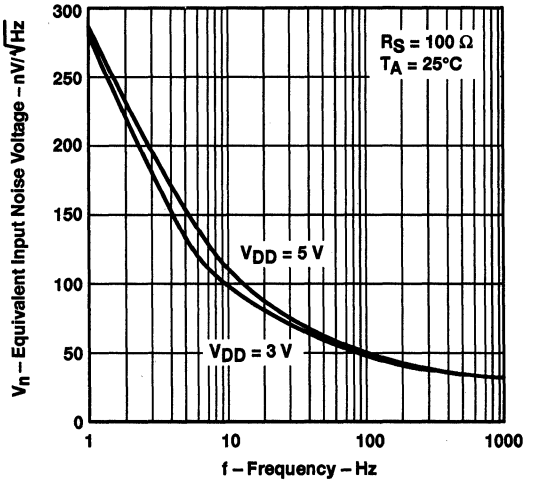


Figure 29

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2334I is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

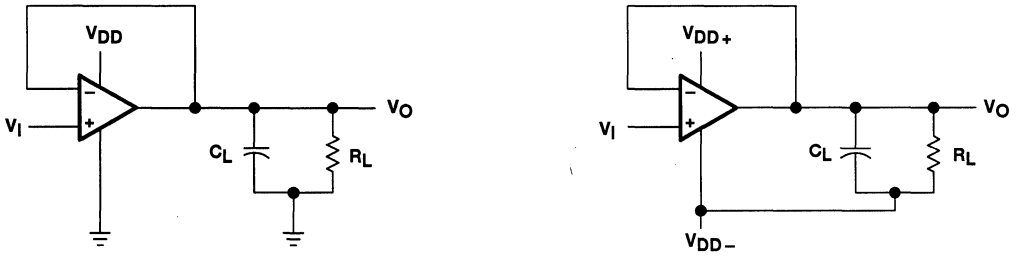


Figure 30. Unity-Gain Amplifier

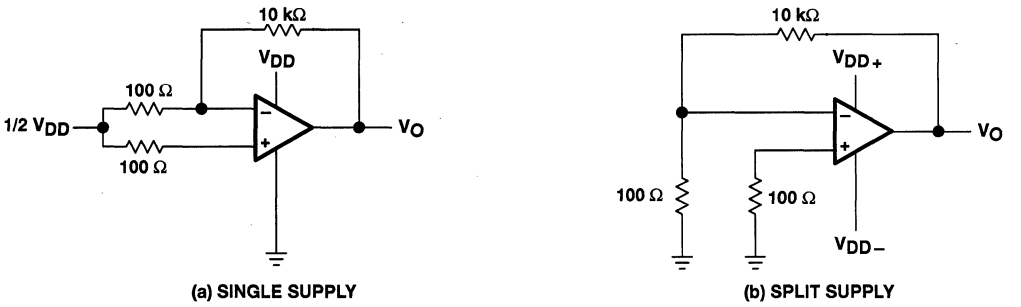


Figure 31. Noise Test Circuit

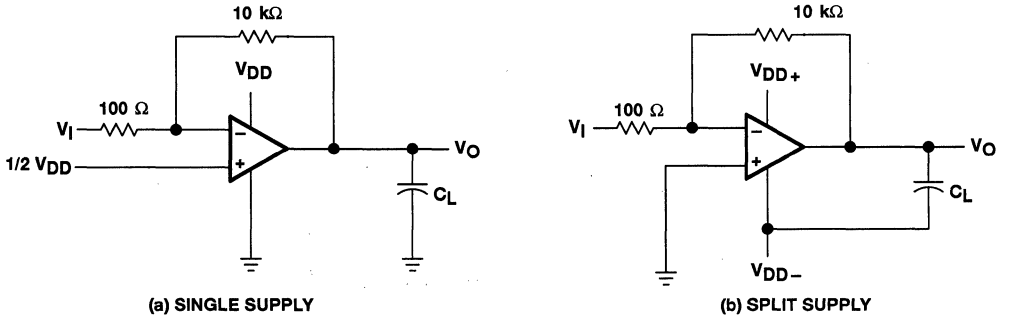


Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2334I operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

  Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading: therefore, an open-socket reading is not feasible using this method.

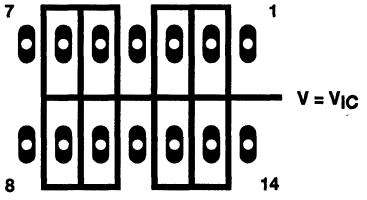


Figure 33. Isolation Metal Around Device Inputs (N Package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

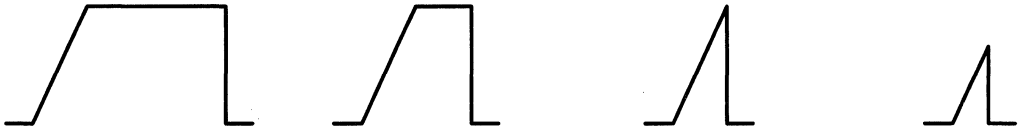


Figure 34. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2334I performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

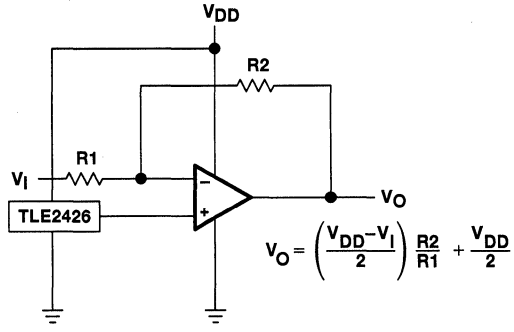


Figure 35. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)

The TLV2334I works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

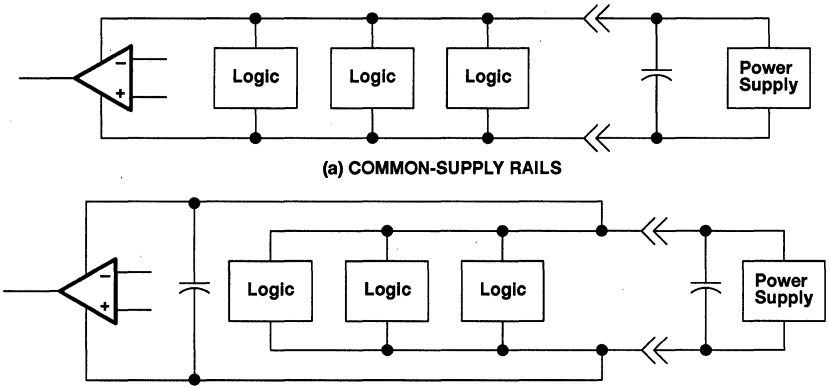


Figure 36. Common Versus Separate Supply Rails

input characteristics

The TLV2334I is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower the range limit includes the negative rail, while the upper range limit is specified at V_{DD} –1 V at T_A = 25°C and at V_{DD} –1.2 V at all other temperatures.

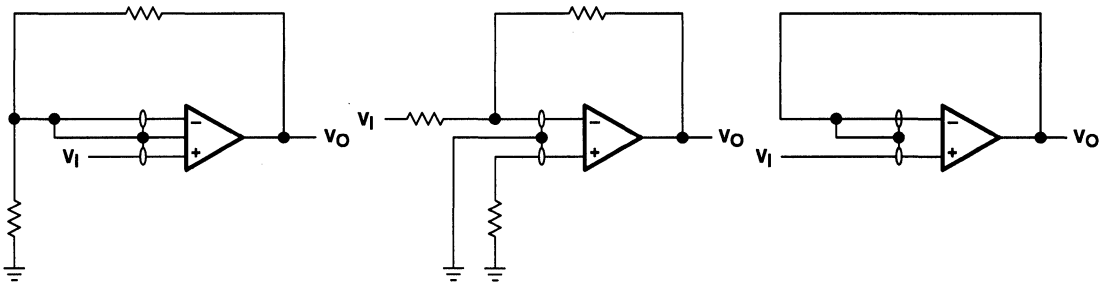
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2334I very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2334I is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level at the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

APPLICATION INFORMATION

input characteristics (continued)



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 37. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2334I results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

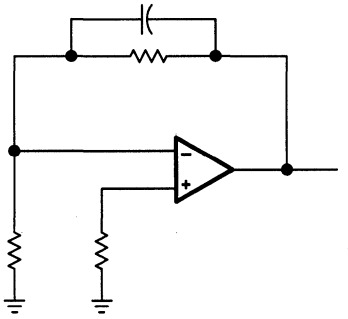


Figure 38. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV2334 incorporates an internal electro-static-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2334I inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes

APPLICATION INFORMATION

should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2334I is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2334I possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

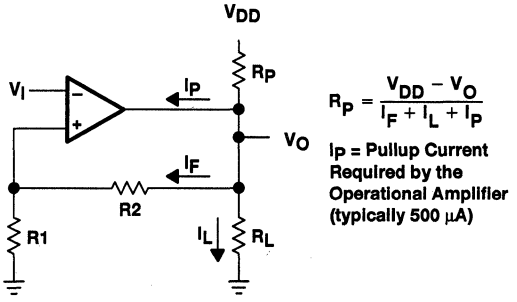


Figure 39. Resistive Pullup to Increase V_{OH}

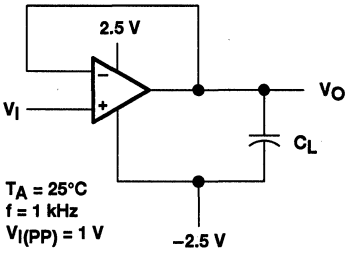
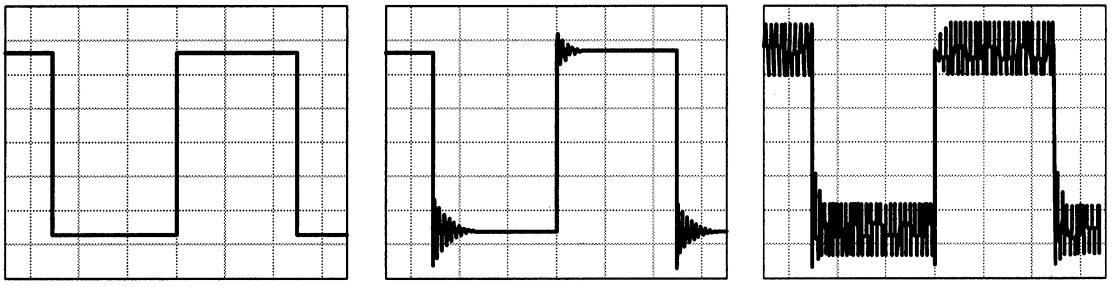


Figure 40. Test Circuit for Output Characteristics

All operating characteristics of the TLV2334I are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

APPLICATION INFORMATION

output characteristics (continued)



(a) C_L = 20 pF, R_L = NO LOAD

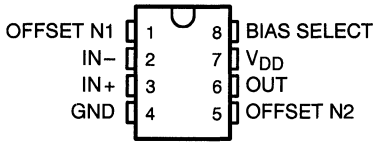
(b) C_L = 170 pF, R_L = NO LOAD

(c) C_L = 190 pF, R_L = NO LOAD

Figure 41. Effect of Capacitive Loads

- **Wide Range of Supply Voltages Over Specified Temperature Range: T_A = –40°C to 85°C . . . 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} –1 V at 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **Low Noise . . . 25 nV/√Hz Typically at f = 1 kHz (High-Bias Mode)**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**
- **Bias-Select Feature Enables Maximum Supply Current Range From 17 μA to 1.5 mA at 25°C**

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)

description

The TLV2341 operational amplifier has been specifically developed for low-voltage, single-supply applications and is fully specified to operate over a voltage range of 2 V to 8 V. The device uses the Texas Instruments silicon-gate LinCMOS™ technology to facilitate low-power, low-voltage operation and excellent offset-voltage stability. LinCMOS™ technology also enables extremely high input impedance and low bias currents allowing direct interface to high-impedance sources.

The TLV2341 offers a bias-select feature, which allows the device to be programmed with a wide range of different supply currents and therefore different levels of ac performance. The supply current can be set at 17 μA, 250 μA, or 1.5 mA, which results in slew-rate specifications between 0.02 and 2.1 V/μs (at 3 V).

The TLV2341 operational amplifiers are especially well suited to single-supply applications and are fully specified and characterized at 3-V and 5-V power supplies. This low-voltage single-supply operation combined with low power consumption makes this device a good choice for remote, inaccessible, or portable battery-powered applications. The common-mode input range includes the negative rail.

The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2341 incorporates internal ESD-protection circuits that prevents functional failures at voltages up to 2000 V as tested under MIL-STD 883 C, Methods 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 85°C	8 mV	TLV2341ID	TLV2341IP	TLV2341IPWLE	TLV2341Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2341IDR).
The PW package is only available left-end taped and reeled (e.g., TLV2341IPWLE).

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bias-select feature

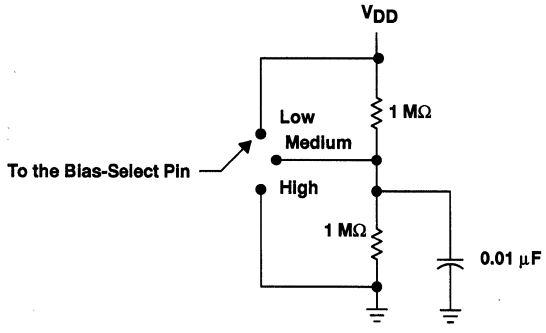
The TLV2342 offers a bias-select feature that allows the user to select any one of three bias levels, depending on the level of performance desired. The tradeoffs between bias levels involve ac performance and power dissipation (see Table 1).

Table 1. Effect of Bias Selection on Performance

TYPICAL PARAMETER VALUES T_A = 25°C, V_{DD} = 3 V		MODE			UNIT
		HIGH-BIAS R_L = 10 kΩ	MEDIUM-BIAS R_L = 100 kΩ	LOW-BIAS R_L = 1 MΩ	
P_D	Power dissipation	975	195	15	μW
SR	Slew rate	2.1	0.38	0.02	V/μs
V_n	Equivalent input noise voltage at f = 1 kHz	25	32	68	nV/√Hz
B_1	Unity-gain bandwidth	790	300	27	kHz
ϕ_m	Phase margin	46°	39°	34°	
A_{VD}	Large-signal differential voltage amplification	11	83	400	V/mV

bias selection

Bias selection is achieved by connecting the bias-select pin to one of three voltage levels (see Figure 1). For medium-bias applications, it is recommended that the bias-select pin be connected to the midpoint between the supply rails. This procedure is simple in split-supply applications since this point is ground. In single-supply applications, the medium-bias mode necessitates using a voltage divider as indicated in Figure 1. The use of large-value resistors in the voltage divider reduces the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the midpoint may be used if it is within the voltages specified in the following table.



BIAS MODE	BIAS-SELECT VOLTAGE (Single Supply)
Low	V_{DD}
Medium	1 V to V_{DD} – 1 V
High	GND

Figure 1. Bias Selection for Single-Supply Applications

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high-bias mode

In the high-bias mode, the TLV2341 series feature low offset voltage drift, high input impedance, and low noise. Speed in this mode approaches that of BiFET devices but at only a fraction of the power dissipation.

medium-bias mode

The TLV2341 in the medium-bias mode features a low offset voltage drift, high input impedance, and low noise. Speed in this mode is similar to general-purpose bipolar devices but power dissipation is only a fraction of that consumed by bipolar devices.

low-bias mode

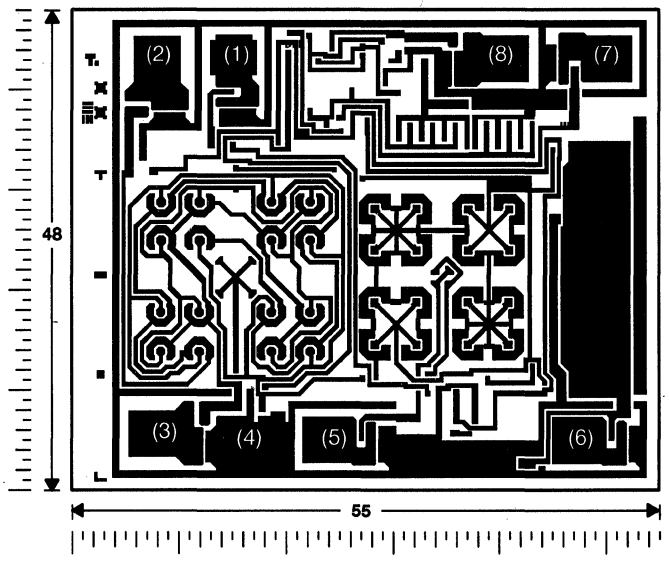
In the low-bias mode, the TLV2341 features low offset voltage drift, high input impedance, extremely low power consumption, and high differential voltage gain.

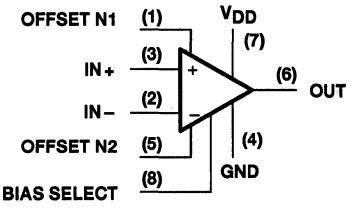
ORDER OF CONTENTS

TLV2341Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2341I. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

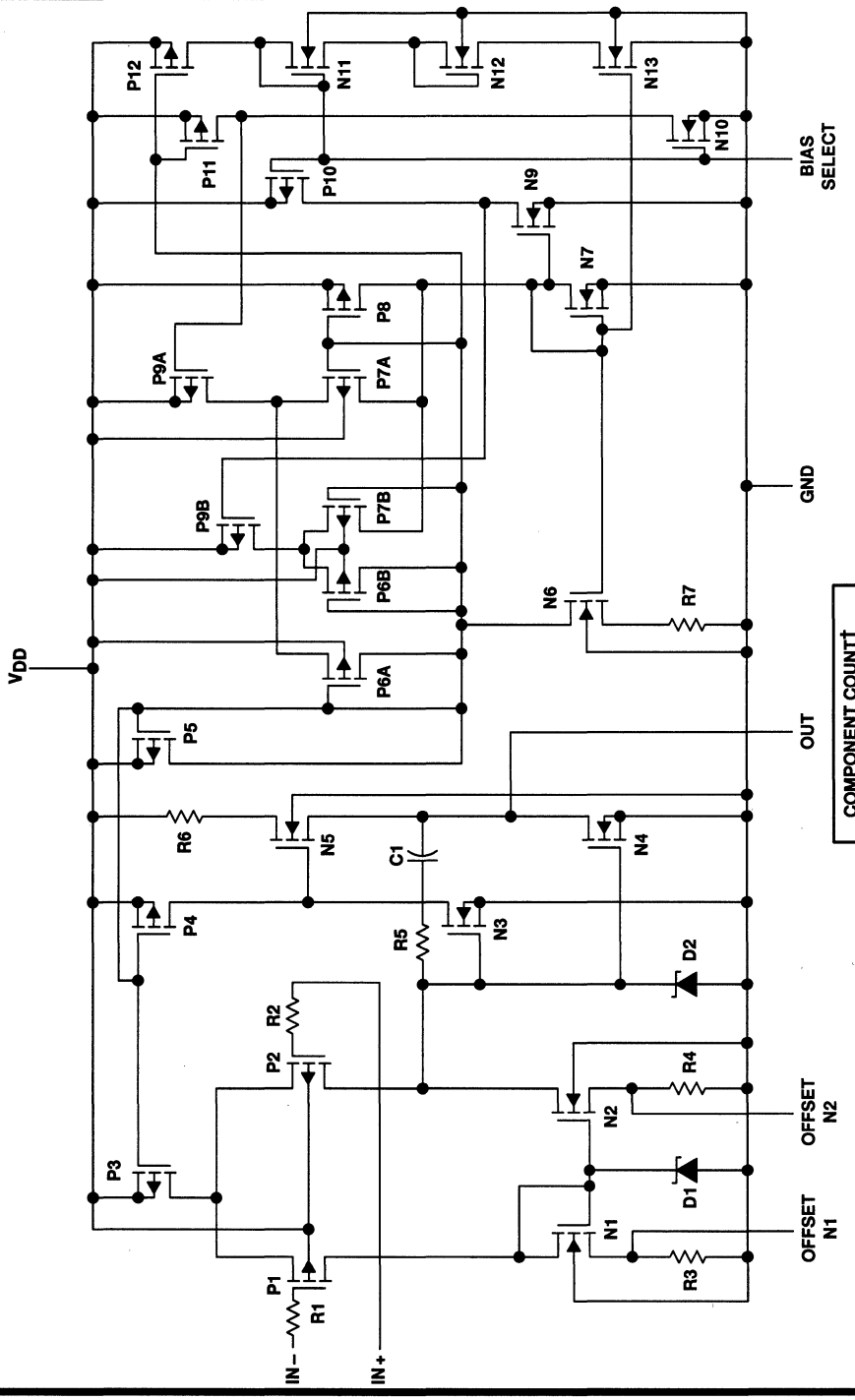
BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

equivalent schematic



COMPONENT COUNT†	
Transistors	27
Diodes	2
Resistors	7
Capacitors	1

† Includes the amplifier and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage (see Note 2) ..... $V_{DD\pm}$
Input voltage range, V_I (any input) ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
Output current, I_O ..... ±30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may effect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	−0.2	1.8	V
	V_{DD} = 5 V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

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HIGH-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2341I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.6	8		1.1	8	mV
			Full range			10			10	
α_{VIO}	Average temperature of input offset voltage		25°C to 85°C		2.7			2.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.7		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		120	150		90	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	25°C	3	11		5	23		V/mV
			Full range	2			3.5			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	78		65	80		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	95		70	95		dB
			Full range	65			65			
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0	25°C		−1.2			−1.4		μA
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		325	1500		675	1600	μA
			Full range			2000			2200	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

HIGH-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2341I MIN	TLV2341I TYP	TLV2341I MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, See Figure 92	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		2.1		V/μs
				85°C		1.7		
V_n	Equivalent input noise voltage	f = kHz, See Figure 93	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 92	25°C		170		kHz
				85°C		145		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 10 kΩ, See Figure 94	C_L = 20 pF,	25°C		790		kHz
				85°C		690		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 94	f = B_1, R_L = 1 MΩ,	−40°C		53°		
				25°C		49°		
				85°C		47°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2341I MIN	TLV2341I TYP	TLV2341I MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, C_L = 20 pF, See Figure 92	$V_{I(PP)}$ = 1 V	25°C		3.6		V/μs
				85°C		2.8		
			$V_{I(PP)}$ = 2.5 V	25°C		2.9		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 93	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 92	25°C		320		kHz
				85°C		250		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 10 kΩ,	C_L = 20 pF, See Figure 94	25°C		1.7		MHz
				85°C		1.2		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 94	f = B_1, R_L = 10 kΩ,	−40°C		49°		
				25°C		46°		
				85°C		43°		

HIGH-BIAS MODE

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2341I						UNIT
			V_{DD} = 3 V			V_{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ		0.6	8		1.1	8	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	1.75	1.9		3.2	3.7		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA		120	150		90	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	3	11		50	23		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	78		65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω	70	95		70	95		dB
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0		−1.2			−1.4		μA
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		325	1500		675	1600	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	2,3
α_{VIO}	Input offset voltage temperature coefficient	Distribution	4,5
V_{OH}	High-level output voltage	vs Output current	6
		vs Supply voltage	7
		vs Temperature	8
V_{OL}	Low-level output voltage	vs Common-mode input voltage	9
		vs Temperature	10, 12
		vs Differential input voltage	11
		vs Low-level output current	13
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage	14
		vs Temperature	15
I_{IB}/I_{IO}	Input bias and offset currents	vs Temperature	16
V_{IC}	Common-mode input voltage	vs Supply voltage	17
I_{DD}	Supply current	vs Supply voltage	18
		vs Temperature	19
SR	Slew rate	vs Supply voltage	20
		vs Temperature	21
	Bias select current	vs Supply voltage	22
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	23
B_1	Unity-gain bandwidth	vs Temperature	24
		vs Supply voltage	25
A_{VD}	Large-signal differential voltage amplification	vs Frequency	26, 27
ϕ_m	Phase margin	vs Supply voltage	28
		vs Temperature	29
		vs Load capacitance	30
V_n	Equivalent input noise voltage	vs Frequency	31
	Phase shift	vs Frequency	26, 27

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE

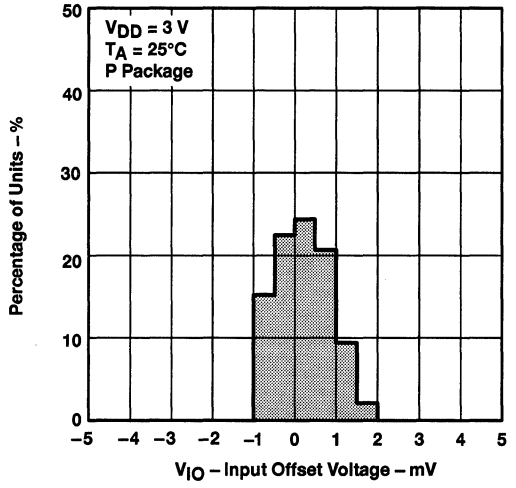


Figure 2

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE

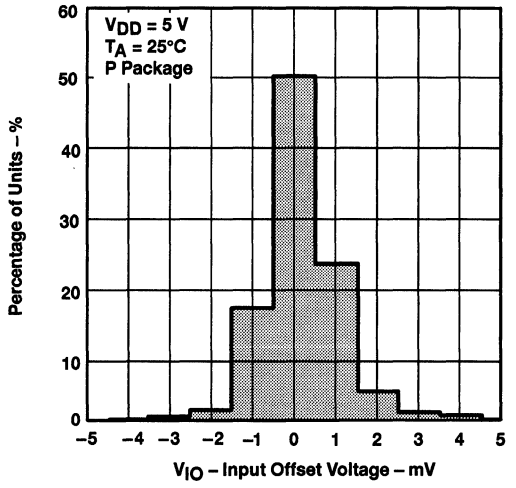


Figure 3

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

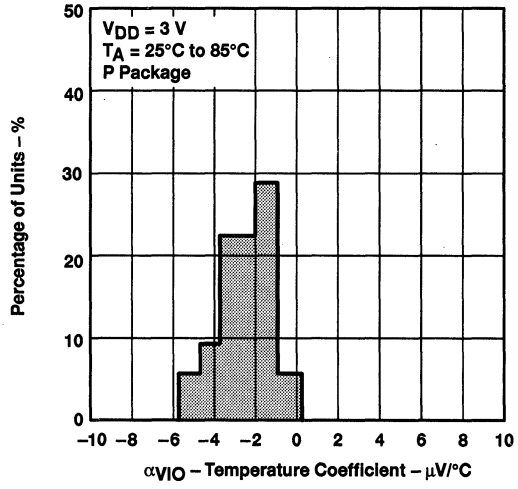


Figure 4

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

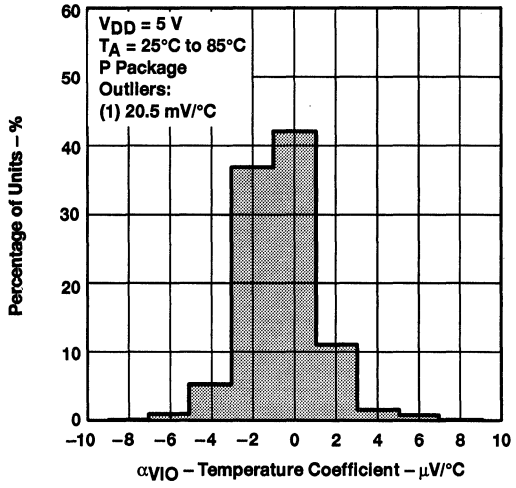


Figure 5

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

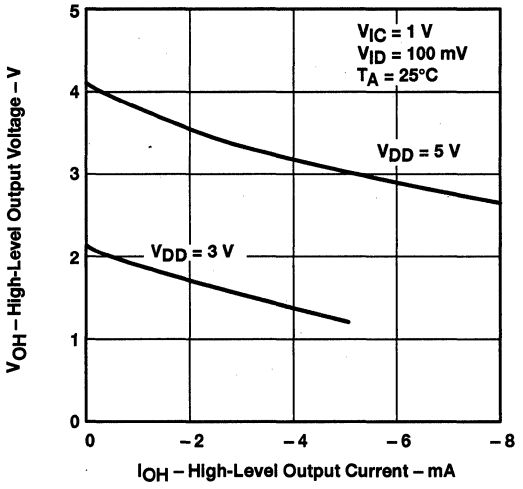


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

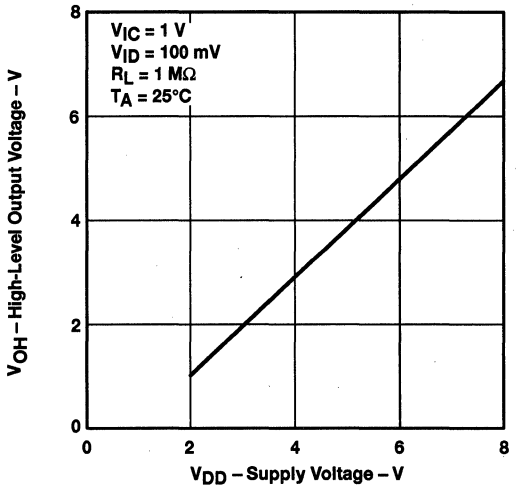


Figure 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

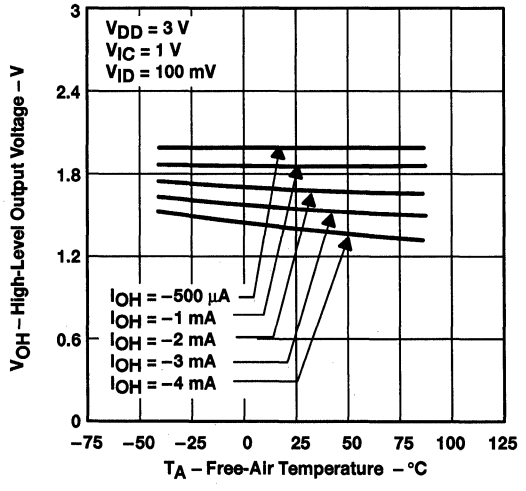


Figure 8

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

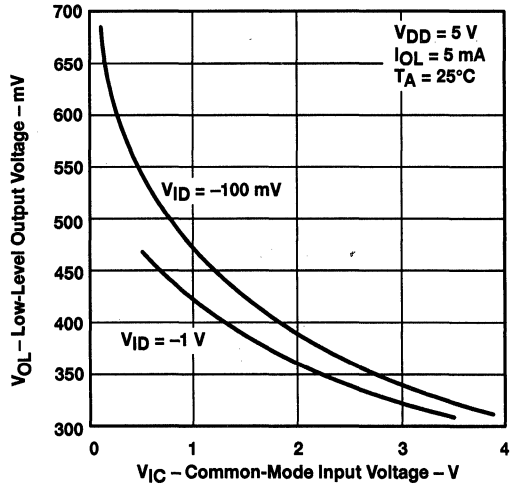


Figure 9

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

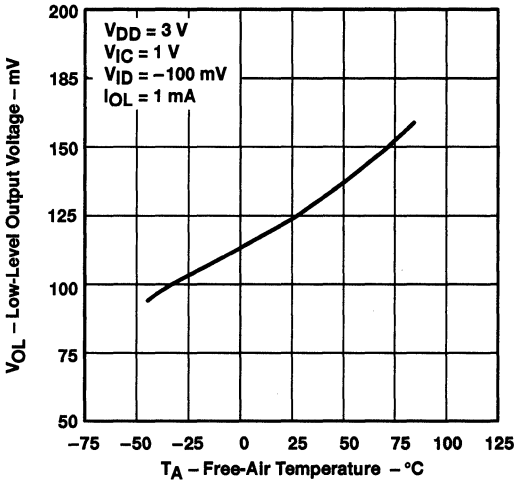


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

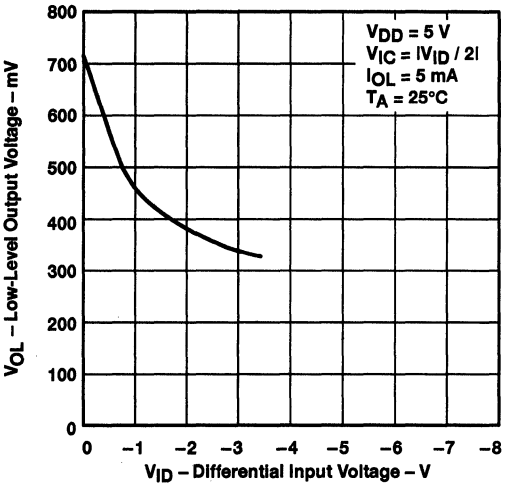


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

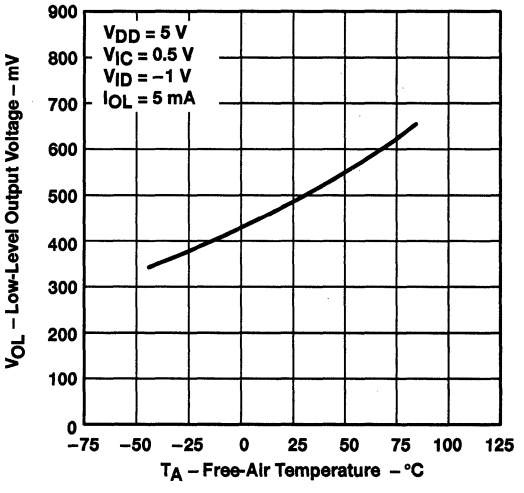


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

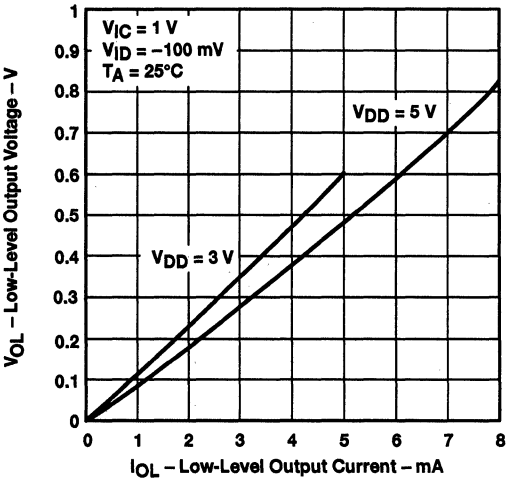


Figure 13

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

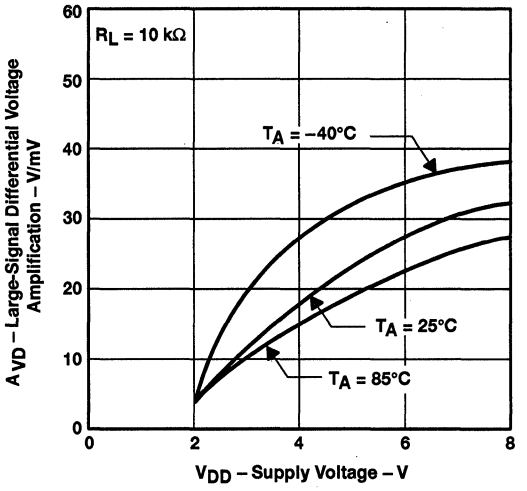


Figure 14

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

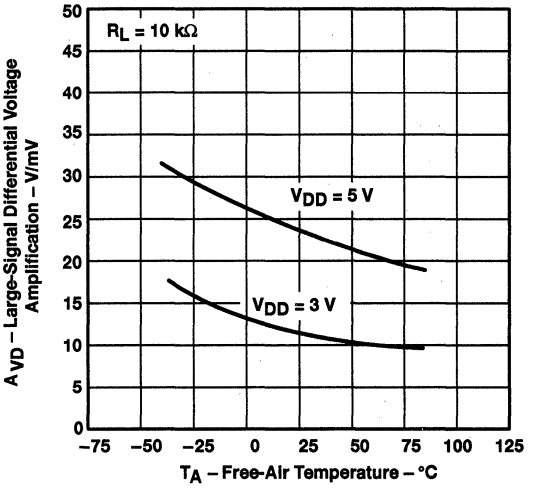
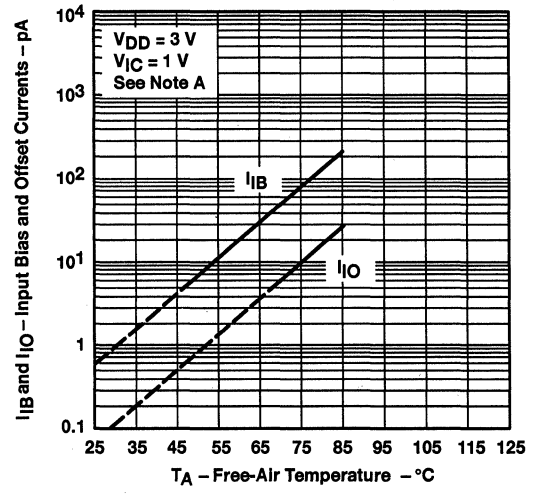


Figure 15

INPUT BIAS CURRENT AND INPUT OFFSET
CURRENT
vs
FREE-AIR TEMPERATURE



NOTE: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 16

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

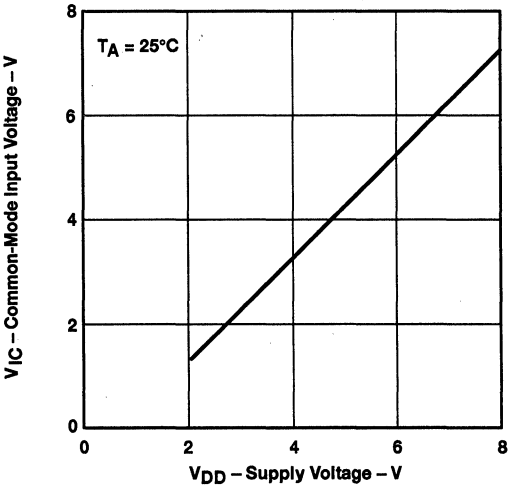


Figure 17

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

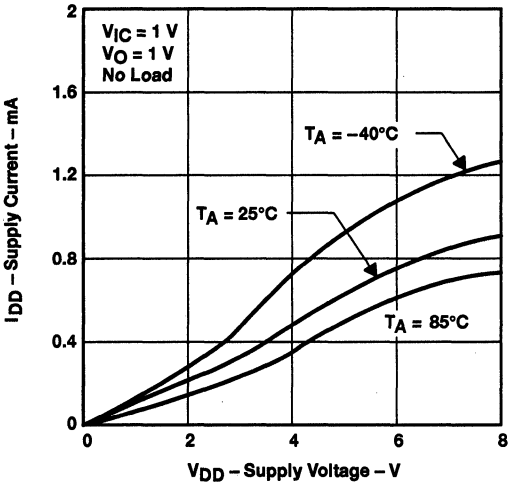


Figure 18

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

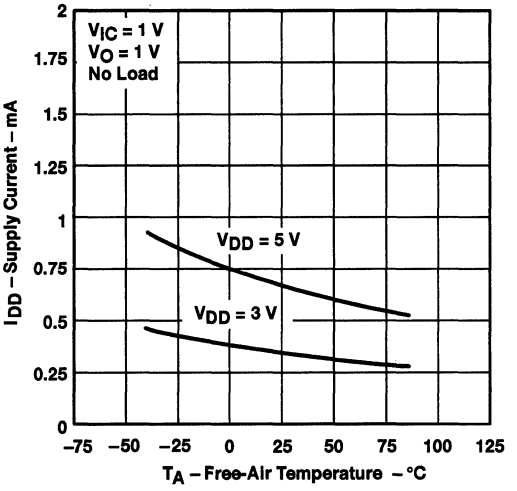


Figure 19

SLEW RATE
vs
SUPPLY VOLTAGE

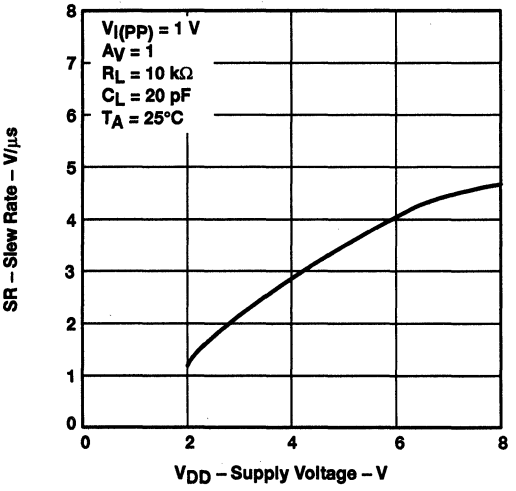


Figure 20

SLEW RATE
vs
FREE-AIR TEMPERATURE

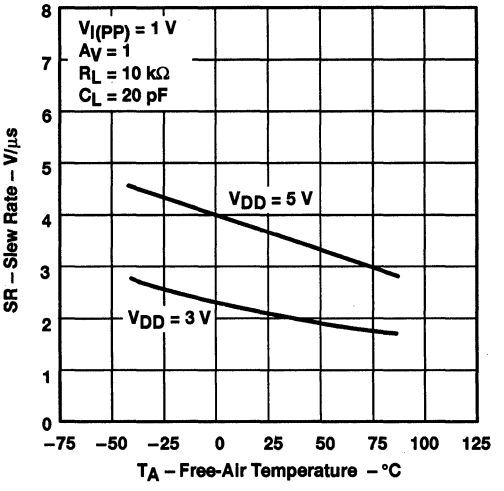


Figure 21

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

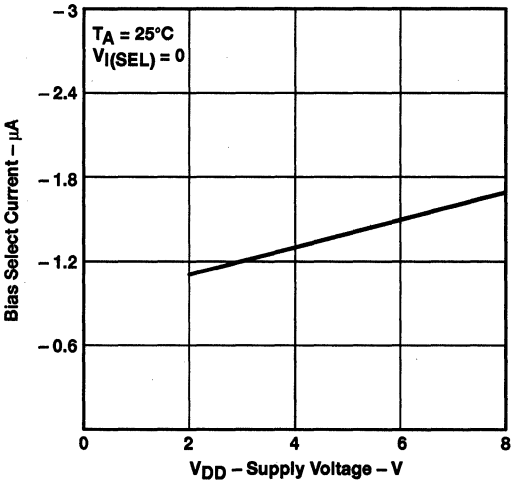


Figure 22

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

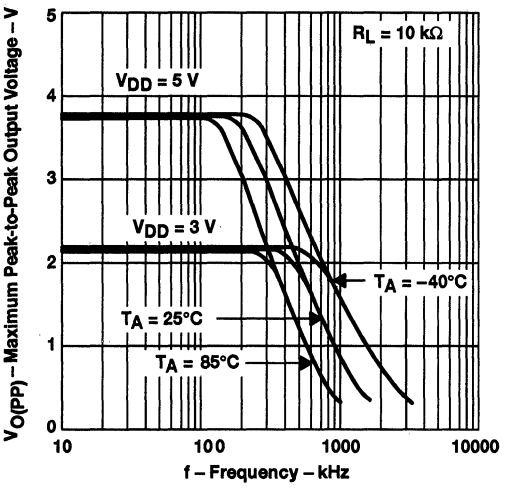


Figure 23

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

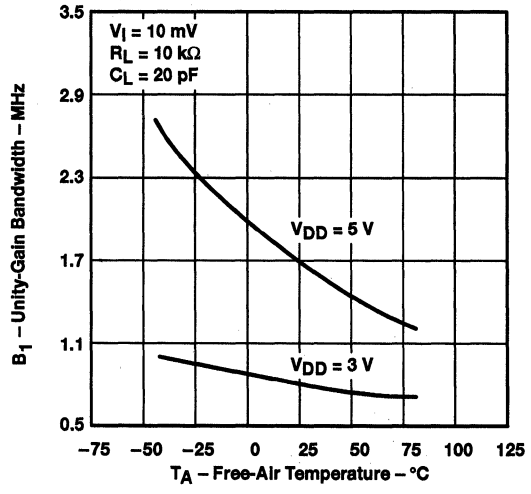


Figure 24

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

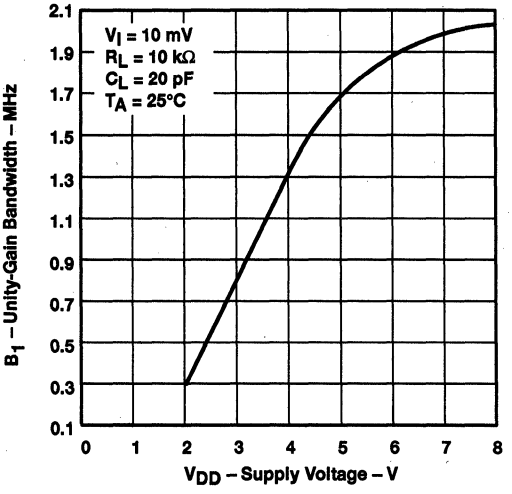


Figure 25

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

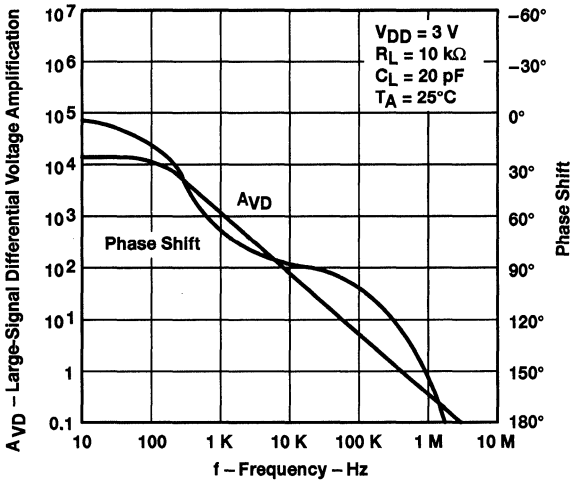


Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

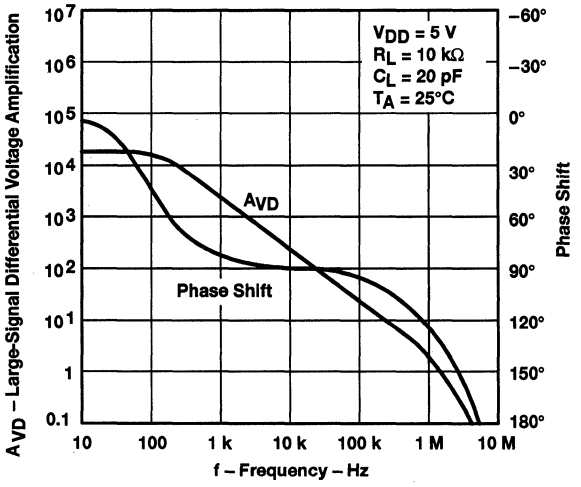


Figure 27

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

PHASE MARGIN vs SUPPLY VOLTAGE

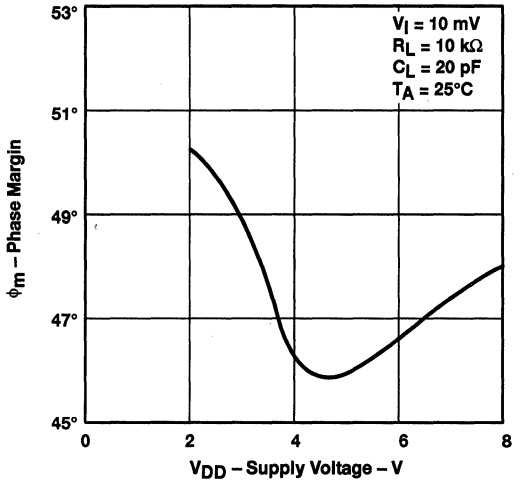


Figure 28

PHASE MARGIN vs FREE-AIR TEMPERATURE

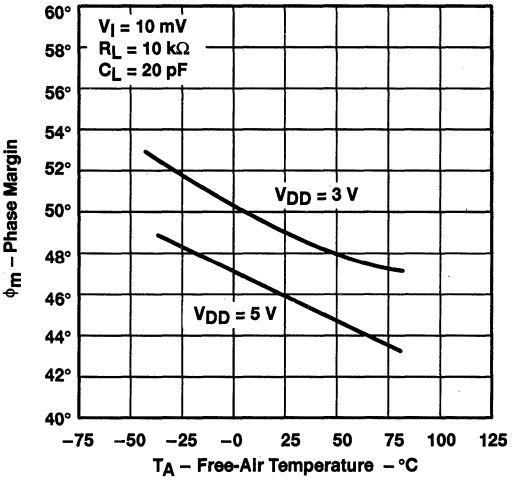


Figure 29

PHASE MARGIN vs LOAD CAPACITANCE

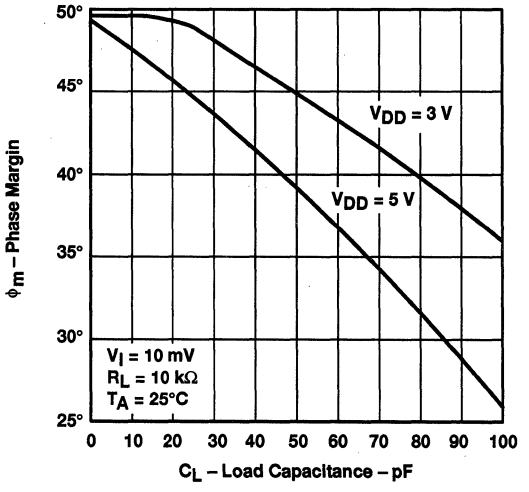


Figure 30

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

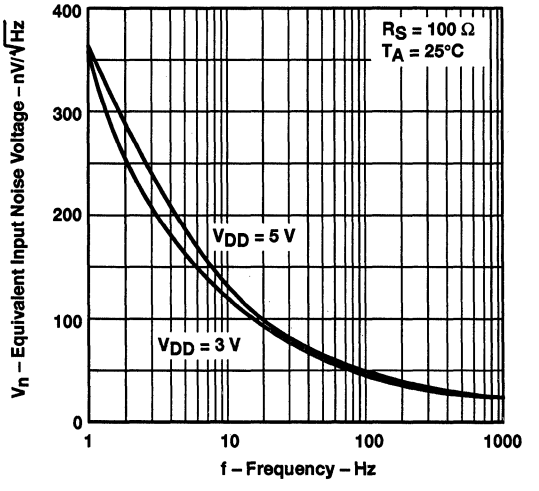


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

MEDIUM-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2341I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.6	8		1.1	8	mV
			Full range			10			10	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.9		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 100 kΩ, See Note 6	25°C	25	83		25	170		V/mV
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	92		65	91		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	94		70	94		dB
			Full range	65			65			
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0	25°C		−100			−130		nA
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		65	250		105	280	μA
			Full range			360			400	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

MEDIUM-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2341I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, See Figure 92	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		0.38		V/μs
				85°C		0.29		
V_n	Equivalent input noise voltage	f = kHz, See Figure 93	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 92	25°C		34		kHz
				85°C		32		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 100 kΩ,	C_L = 20 pF, See Figure 94	25°C		300		kHz
				85°C		235		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 94	f = B_1, R_L = 100 kΩ,	−40°C		42°		
				25°C		39°		
				85°C		36°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2341I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, C_L = 20 pF, See Figure 92	$V_{I(PP)}$ = 1 V	25°C		0.43		V/μs
				85°C		0.35		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				85°C		0.32		
V_n	Equivalent input noise voltage	f =1 kHz, See Figure 93	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 92	25°C		55		kHz
				85°C		45		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 100 kΩ,	C_L = 20 pF, See Figure 94	25°C		525		kHz
				85°C		370		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 94	f = B_1, R_L = 100 kΩ,	−40°C		43°		
				25°C		40°		
				85°C		38°		

MEDIUM-BIAS MODE

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2341I						UNIT
			V_{DD} = 3 V			V_{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 100 kΩ		0.6	8		1.1	8	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	1.75	1.9		3.2	3.9		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 100 kΩ, See Note 6	25	83		25	170		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	92		65	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω	70	94		70	94		dB
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0		−100			−130		nA
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		65	250		105	280	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	32, 33
α_{VIO}	Input offset voltage temperature coefficient	Distribution	34, 35
V_{OH}	High-level output voltage	vs Output current	36
		vs Supply voltage	37
		vs Temperature	38
V_{OL}	Low-level output voltage	vs Common-mode input voltage	39
		vs Temperature	40, 42
		vs Differential input voltage	41
		vs Low-level output current	43
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage	44
		vs Temperature	45
I_{IB}/I_{IO}	Input bias and offset currents	vs Temperature	46
V_{IC}	Common-mode input voltage	vs Supply voltage	47
I_{DD}	Supply current	vs Supply voltage	48
		vs Temperature	49
SR	Slew rate	vs Supply voltage	50
		vs Temperature	51
	Bias select current	vs Supply current	52
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	53
B_1	Unity-gain bandwidth	vs Temperature	54
		vs Supply voltage	55
A_{VD}	Large-signal differential voltage amplification	vs Frequency	56, 57
ϕ_m	Phase margin	vs Supply voltage	58
		vs Temperature	59
		vs Load capacitance	60
V_n	Equivalent input noise voltage	vs Frequency	61
	Phase shift	vs Frequency	56, 57

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE

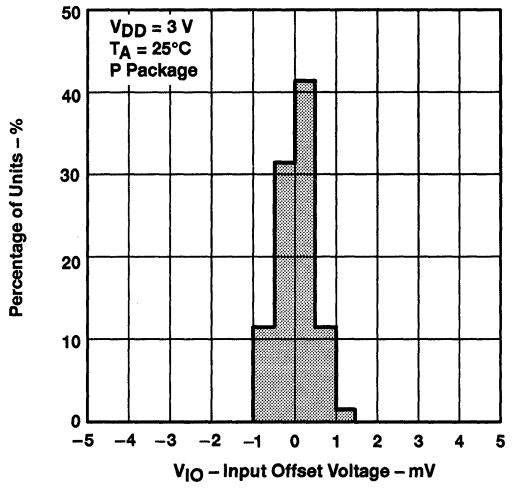


Figure 32

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE

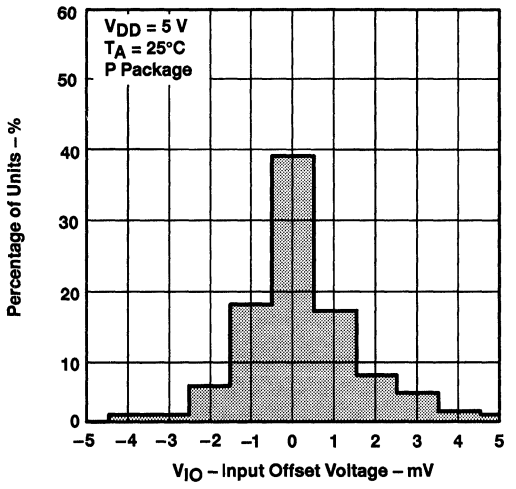


Figure 33

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

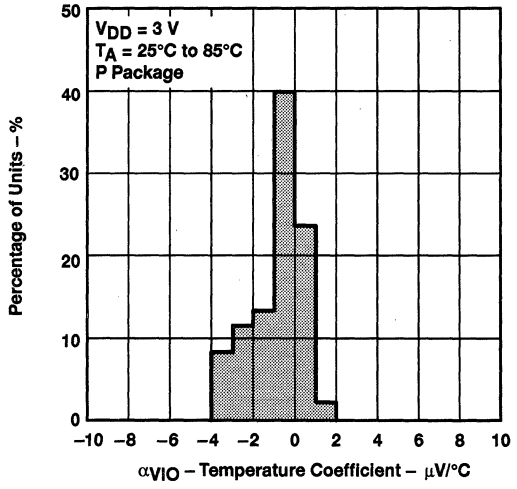


Figure 34

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

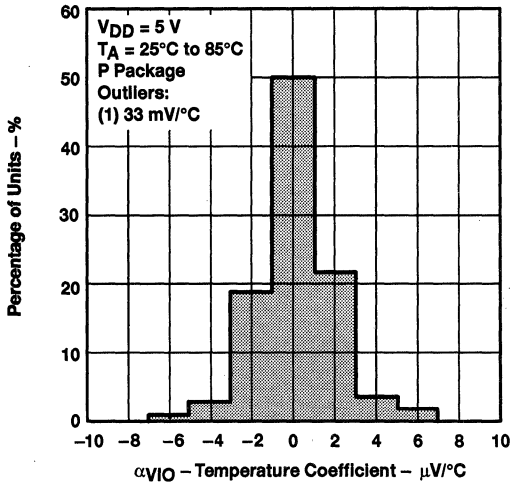


Figure 35

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

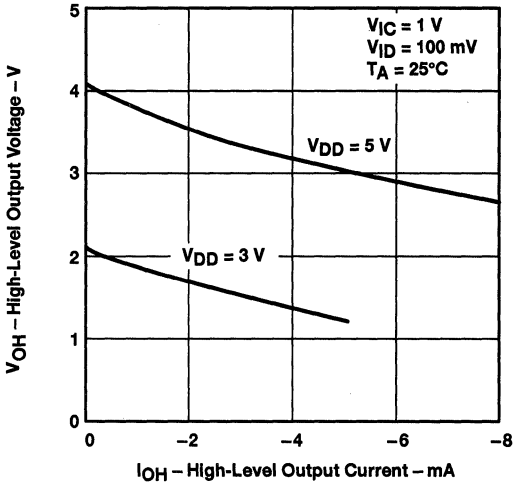


Figure 36

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

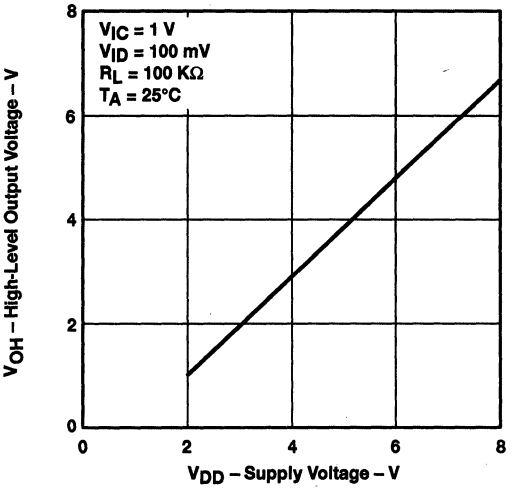


Figure 37

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

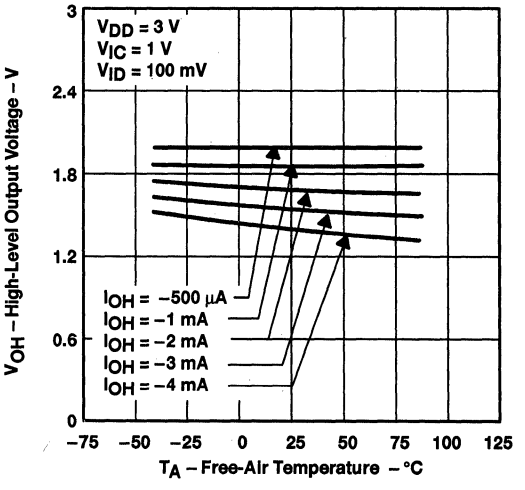


Figure 38

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

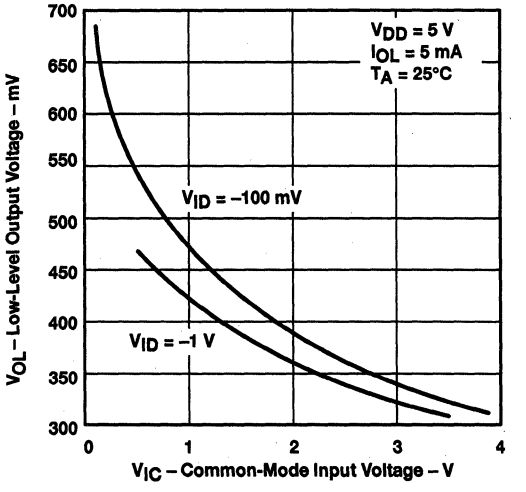


Figure 39

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

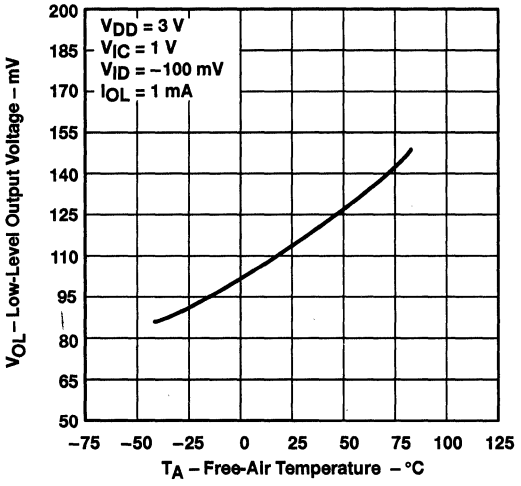


Figure 40

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

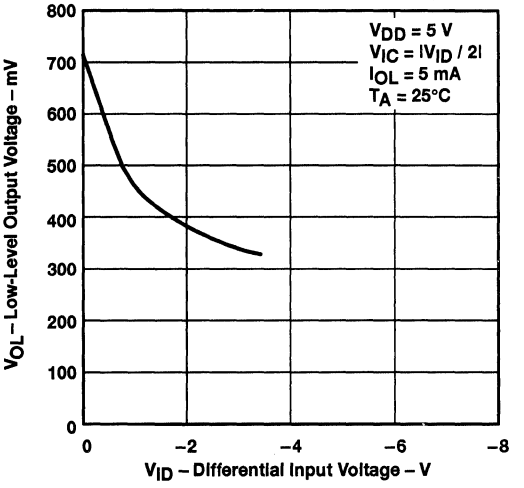


Figure 41

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

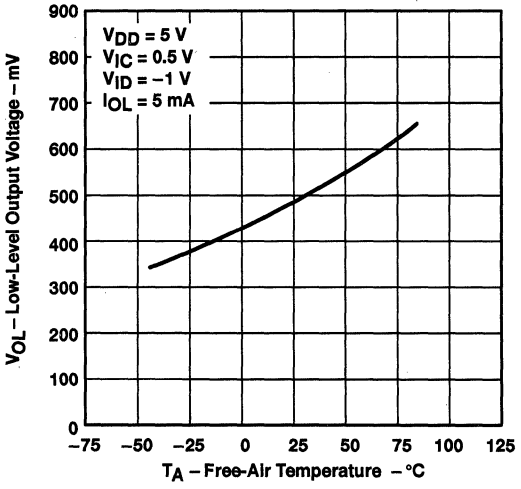


Figure 42

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

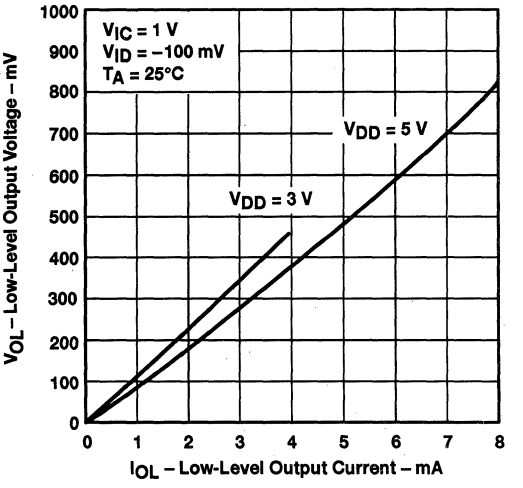


Figure 43

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

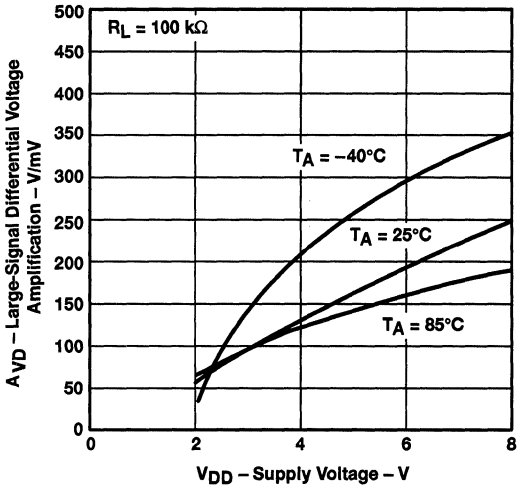


Figure 44

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

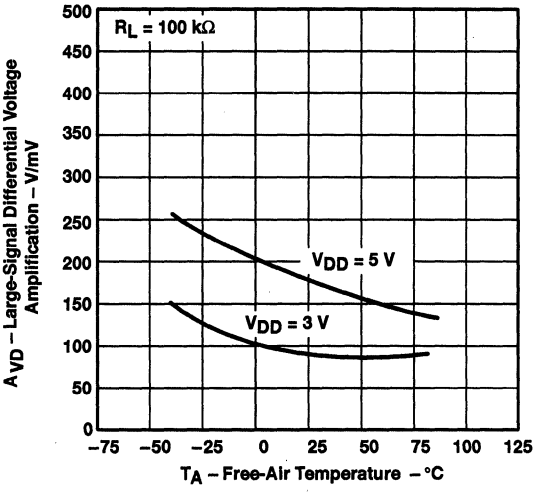


Figure 45

INPUT BIAS CURRENT AND INPUT
OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

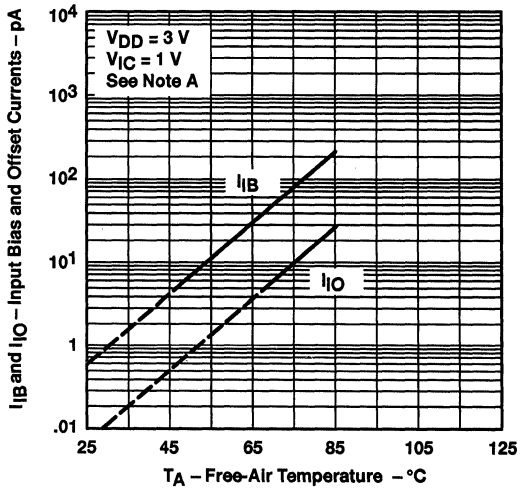


Figure 46

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

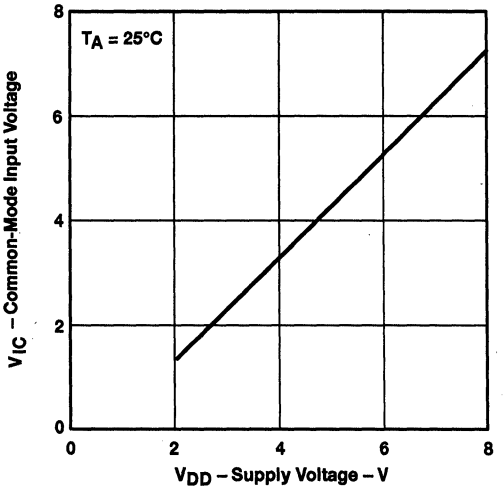


Figure 47

NOTE A: The typical values of input bias current and input offset current below 5 pA are determined mathematically.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

SUPPLY CURRENT vs SUPPLY VOLTAGE

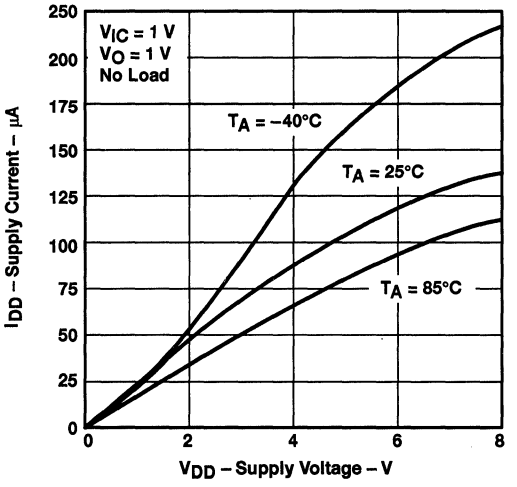


Figure 48

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

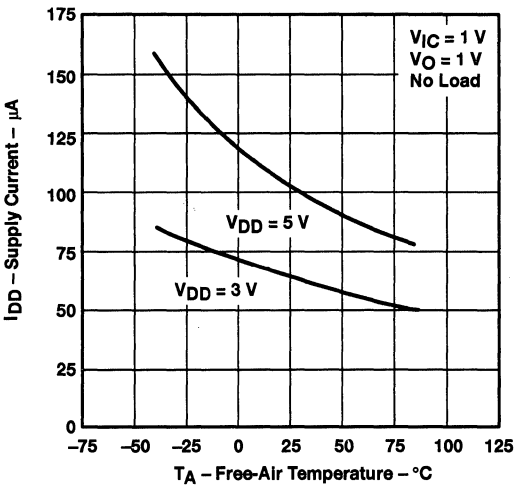


Figure 49

SLEW RATE vs SUPPLY VOLTAGE

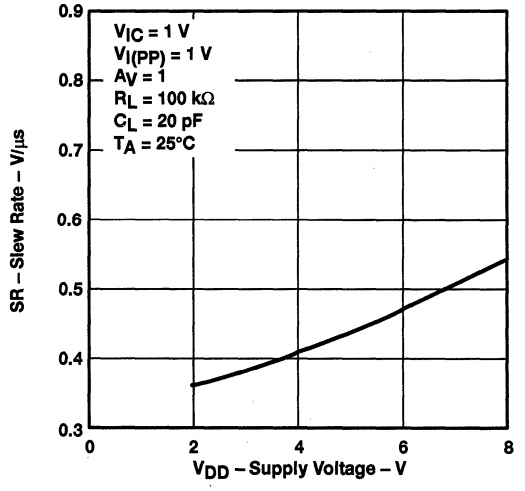


Figure 50

SLEW RATE vs FREE-AIR TEMPERATURE

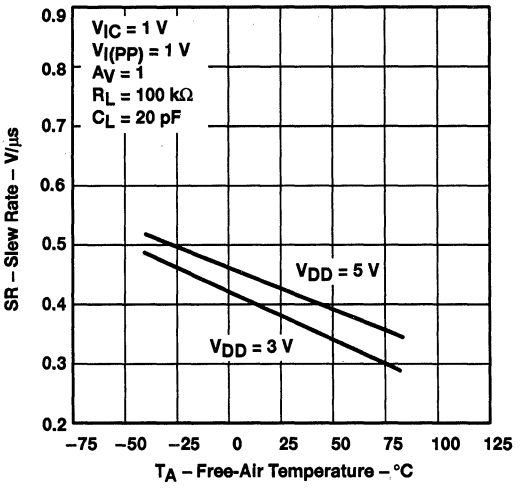


Figure 51

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

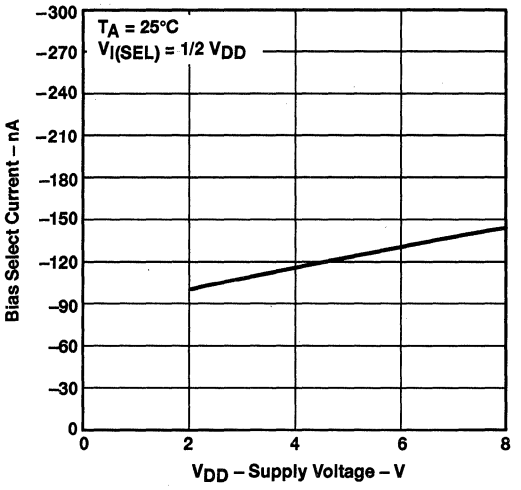


Figure 52

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

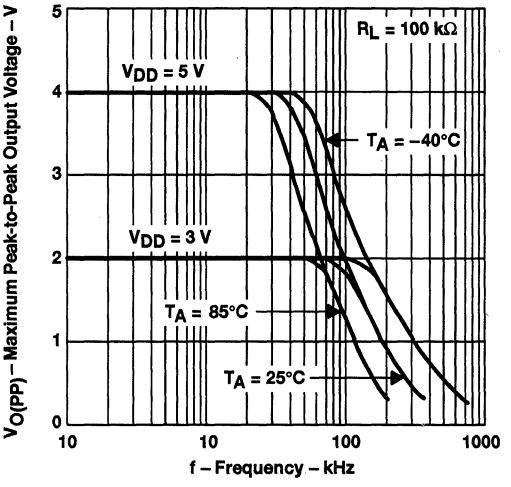


Figure 53

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

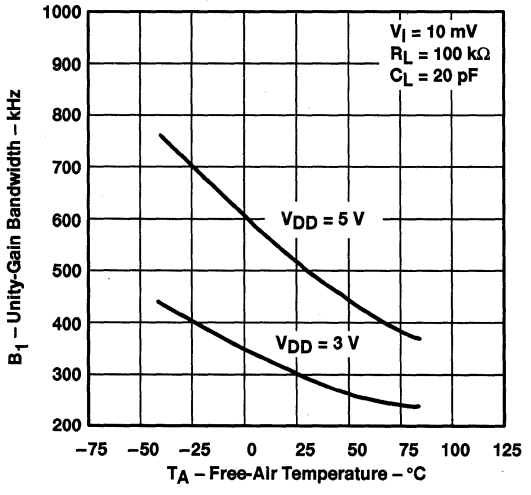


Figure 54

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

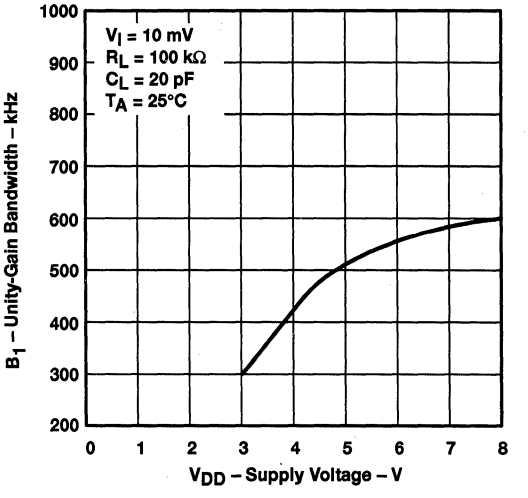


Figure 55

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

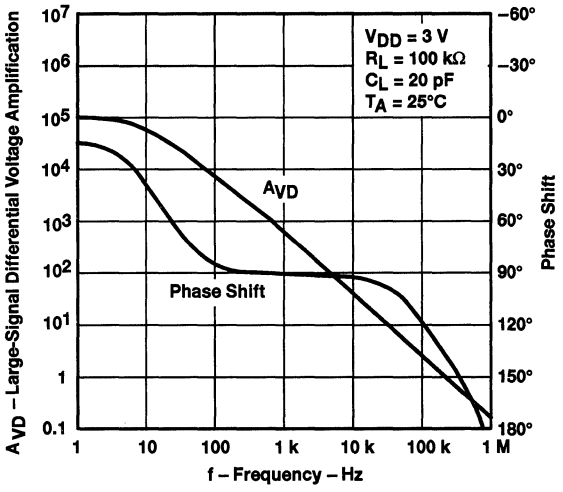


Figure 56

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

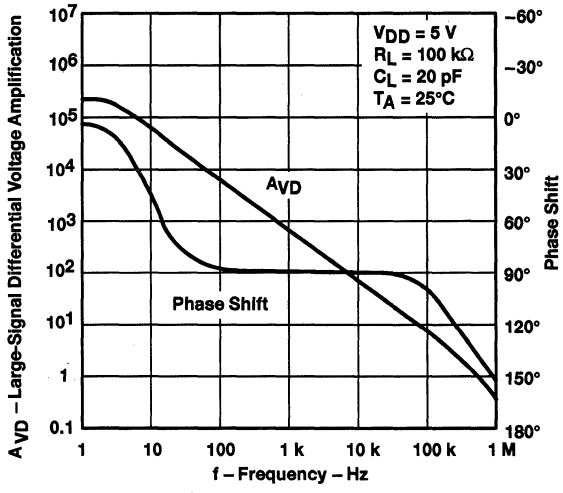


Figure 57

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

PHASE MARGIN vs SUPPLY VOLTAGE

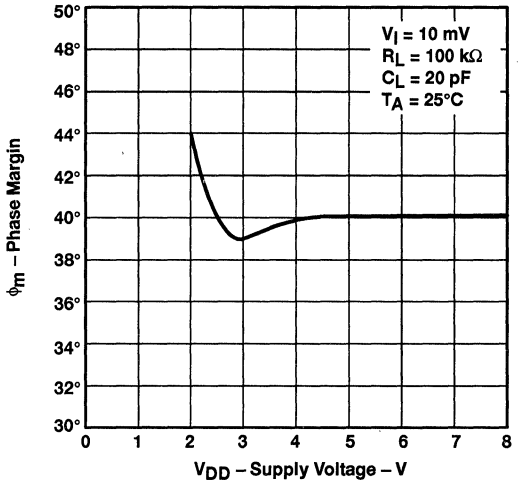


Figure 58

PHASE MARGIN vs FREE-AIR TEMPERATURE

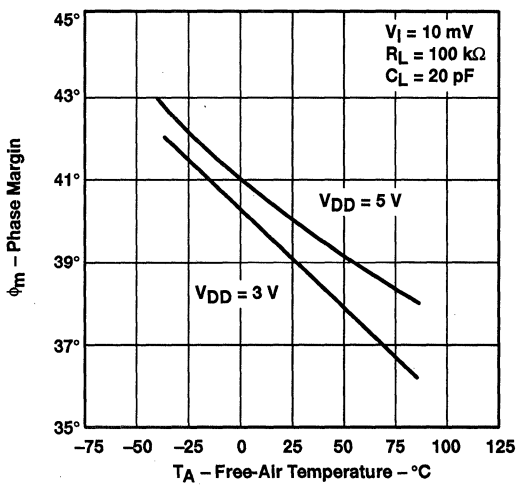


Figure 59

PHASE MARGIN vs LOAD CAPACITANCE

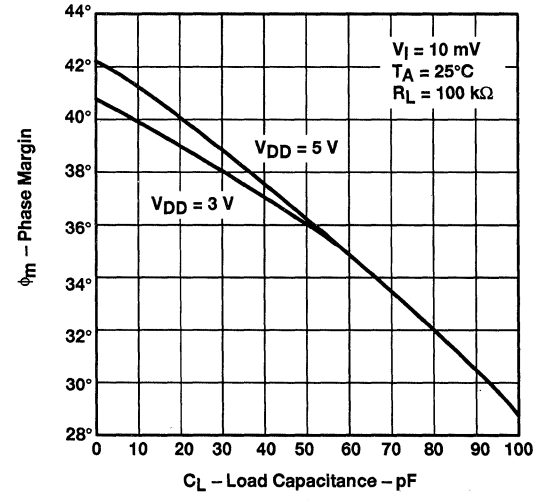


Figure 60

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

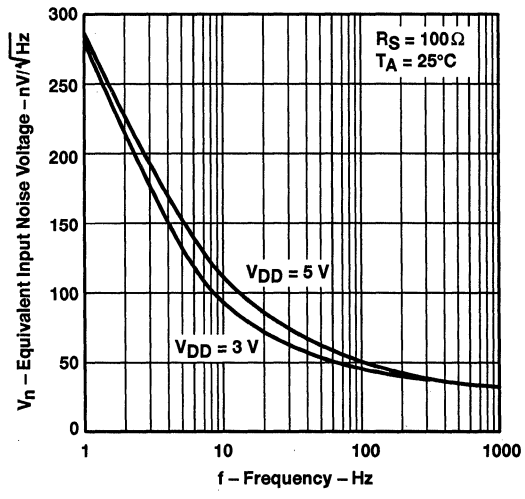


Figure 61

LOW-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2341I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.6	8		1.1	8	mV
			Full range			10			10	
α_{VIO}	Average temperature of input offset voltage		25°C to 85°C		1			1.1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.8		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	25°C	50	400		50	520		V/mV
			Full range	50			50			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	88		65	94		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	86		70	86		dB
			Full range	65			65			
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0	25°C		10			65		nA
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		5	17		10	17	μA
			Full range			27			27	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, $V_{O(PP)}$ = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

LOW-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2341I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, See Figure 92	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		0.02		V/μs
				85°C		0.02		
V_n	Equivalent input noise voltage	f = kHz, See Figure 93	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 92	25°C		2.5		kHz
				85°C		2		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 94	25°C		27		kHz
				85°C		21		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 94	f = B_1, R_L = 1 MΩ,	−40°C		39°		
				25°C		34°		
				85°C		28°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2341I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, C_L = 20 pF, See Figure 92	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				85°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				85°C		0.02		
V_n	Equivalent input noise voltage	f =1 kHz, See Figure 93	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 92	25°C		5		kHz
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 94	25°C		85		kHz
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 94	f = B_1, R_L = 1 MΩ,	−40°C		38°		
				25°C		34°		
				85°C		28°		

LOW-BIAS MODE

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLV2341Y						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, R_S = 50 Ω,	V_{IC} = 1 V, R_L = 1 MΩ		0.6	8		1.1	8	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)			−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, I_{OH} = −1 mA	V_{ID} = 100 mV,	1.75	1.9		3.2	3.8		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, I_{OL} = 1 mA	V_{ID} = −100 mV,		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, See Note 6	R_L = 1 MΩ,	50	400		50	520		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, R_S = 50 Ω	V_{IC} = V_{ICR}min,	65	88		65	94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	V_{DD} = 3 V to 5 V, V_O = 1 V,	V_{IC} = 1 V, R_S = 50 Ω	70	86		70	86		dB
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0			10			65		nA
I_{DD}	Supply current	V_O = 1 V, No load	V_{IC} = 1 V,		5	17		10	17	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	62, 63
α_{VIO}	Input offset voltage temperature coefficient	Distribution	64, 65
V_{OH}	High-level output voltage	vs Output current	66
		vs Supply voltage	67
		vs Temperature	68
V_{OL}	Low-level output voltage	vs Common-mode input voltage	69
		vs Temperature	70, 72
		vs Differential input voltage	71
		vs Low-level output current	73
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage	74
		vs Temperature	75
I_{IB}/I_{IO}	Input bias and offset currents	vs Temperature	76
V_{IC}	Common-mode input voltage	vs Supply voltage	77
I_{DD}	Supply current	vs Supply voltage	78
		vs Temperature	79
SR	Slew rate	vs Supply voltage	80
		vs Temperature	81
	Bias select current	vs Supply current	82
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	83
B_1	Unity-gain bandwidth	vs Temperature	84
		vs Supply voltage	85
A_{VD}	Large-signal differential voltage amplification	vs Frequency	86, 87
ϕ_m	Phase margin	vs Supply voltage	88
		vs Temperature	89
		vs Load capacitance	90
V_n	Equivalent input noise voltage	vs Frequency	91
	Phase shift	vs Frequency	86, 87

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE

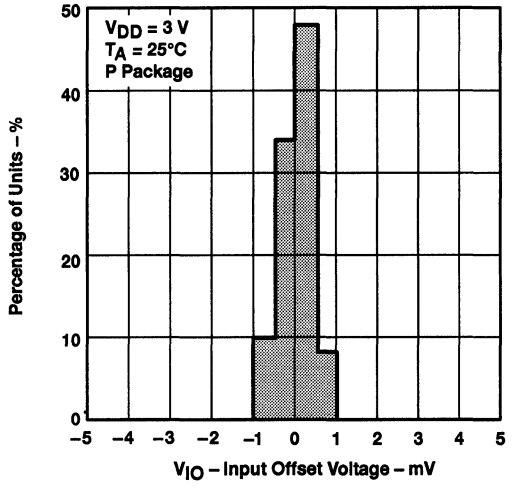


Figure 62

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE

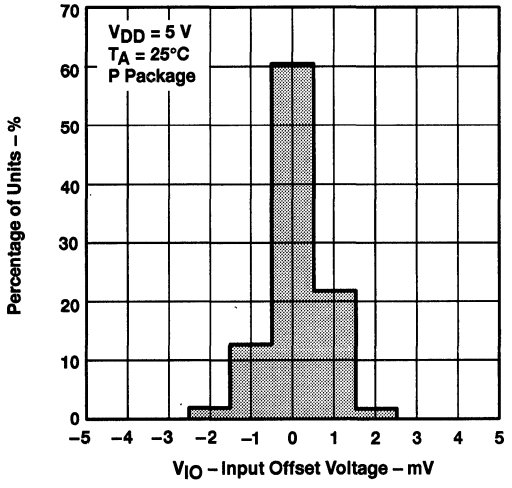


Figure 63

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

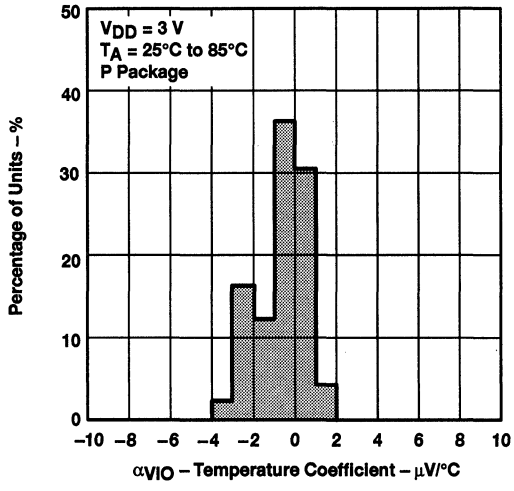


Figure 64

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

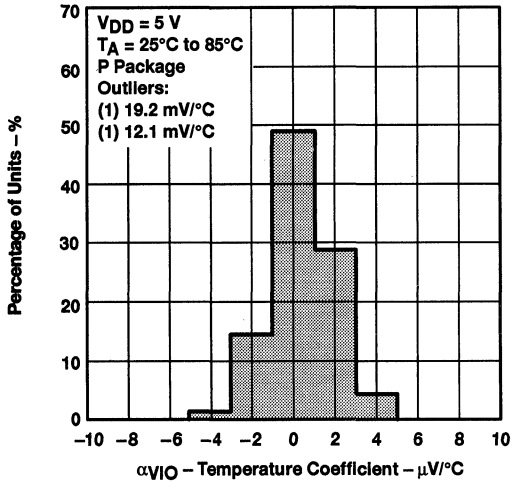


Figure 65

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

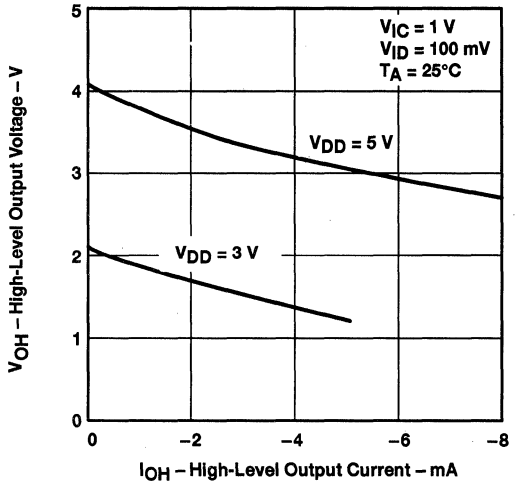


Figure 66

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

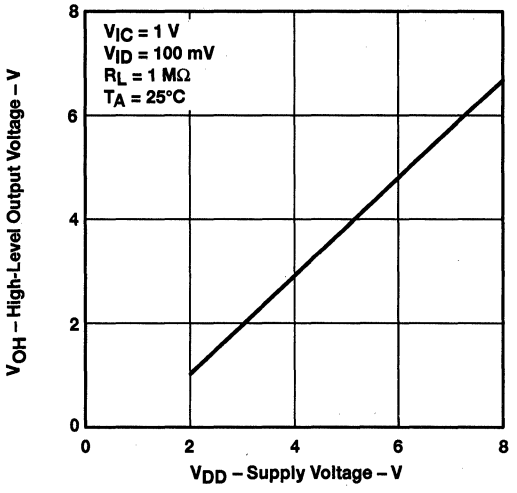


Figure 67

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

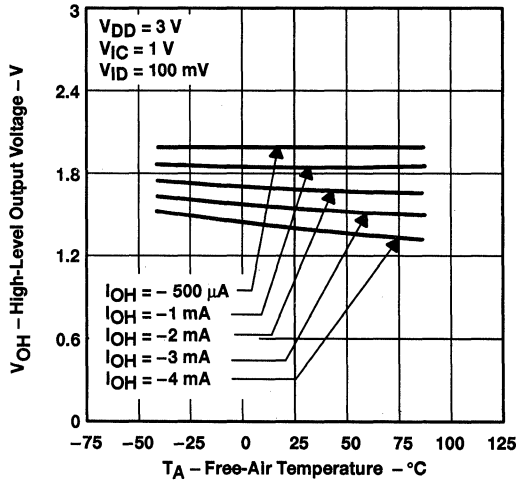


Figure 68

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

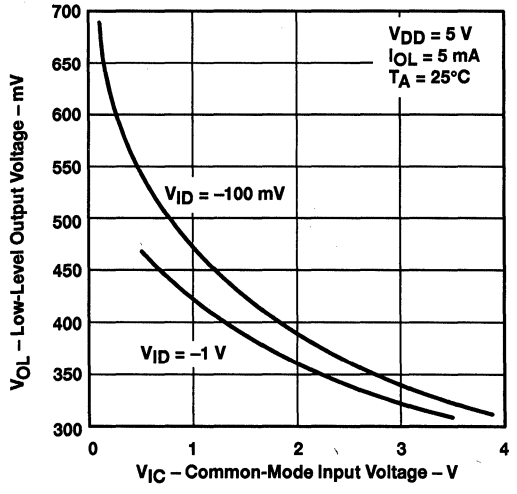


Figure 69

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

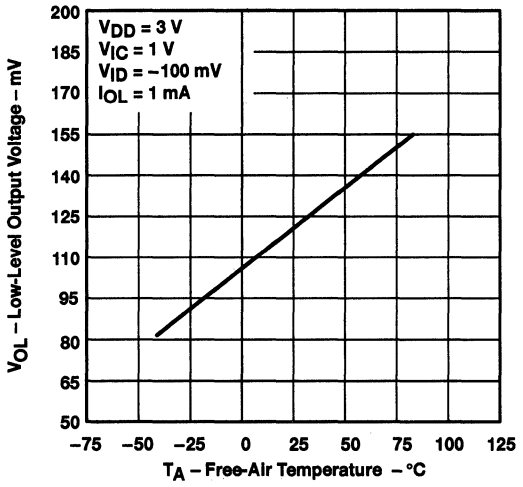


Figure 70

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

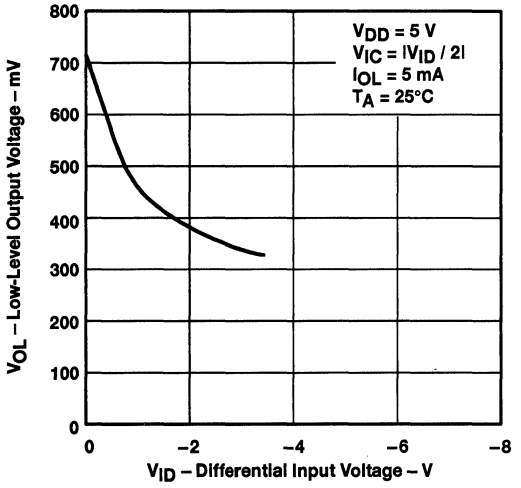


Figure 71

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

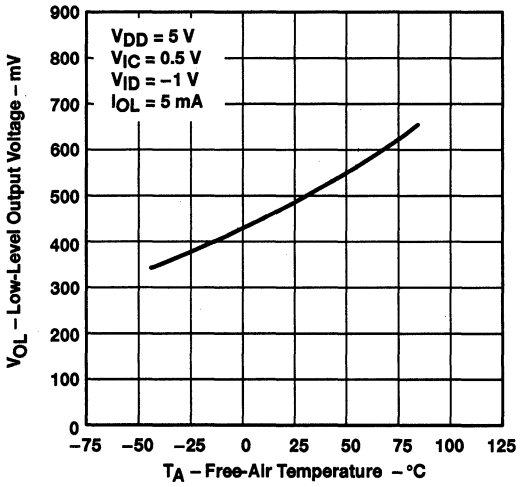


Figure 72

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

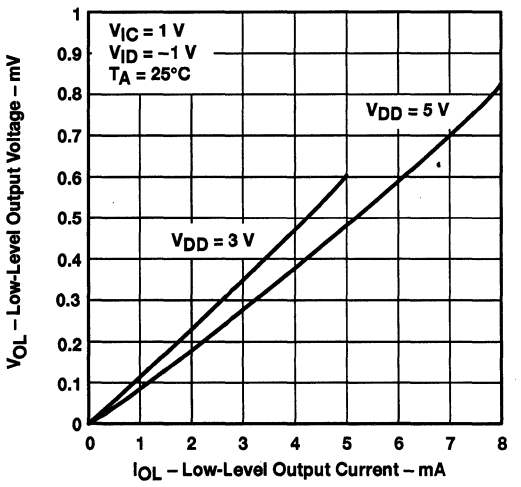


Figure 73

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

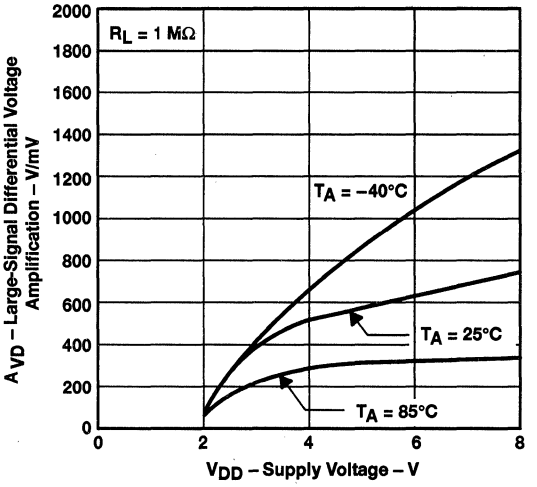


Figure 74

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

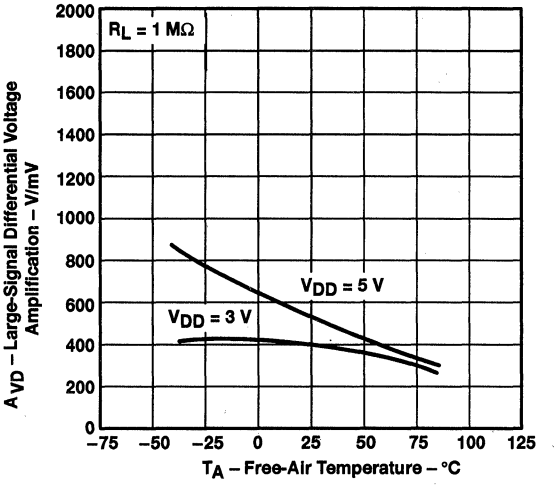


Figure 75

INPUT BIAS CURRENT AND INPUT OFFSET
CURRENT
vs
FREE-AIR TEMPERATURE

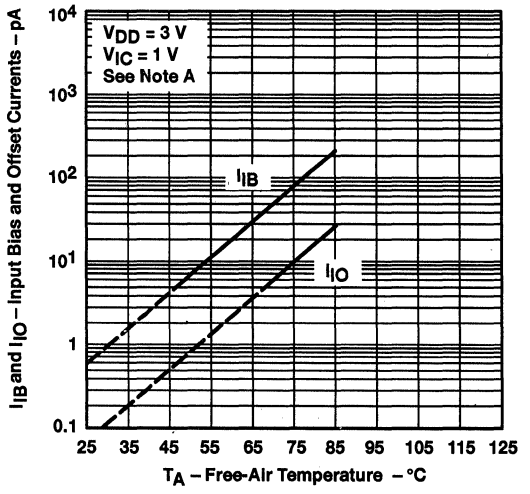


Figure 76

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

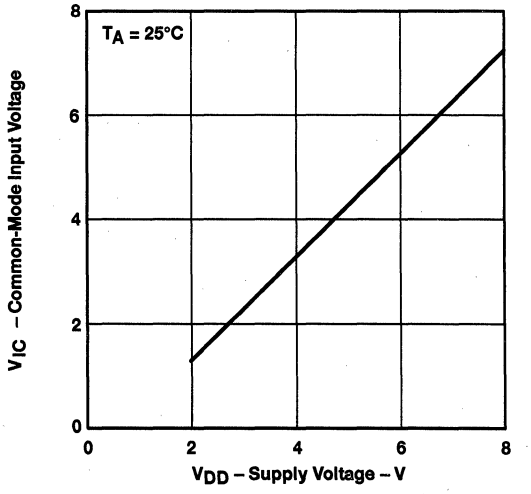


Figure 77

NOTE A: The typical values of input bias current and input offset current below 5 pA are determined mathematically.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

SUPPLY CURRENT vs SUPPLY VOLTAGE

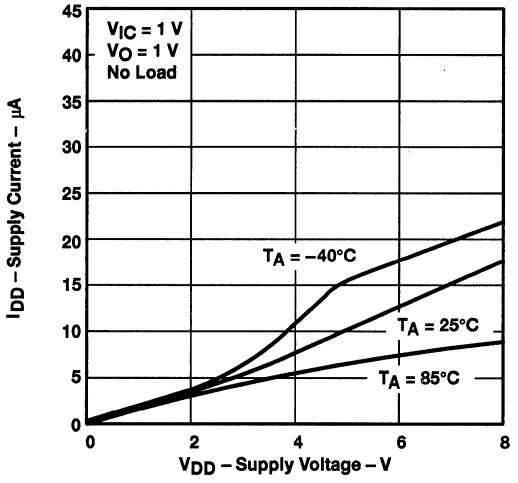


Figure 78

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

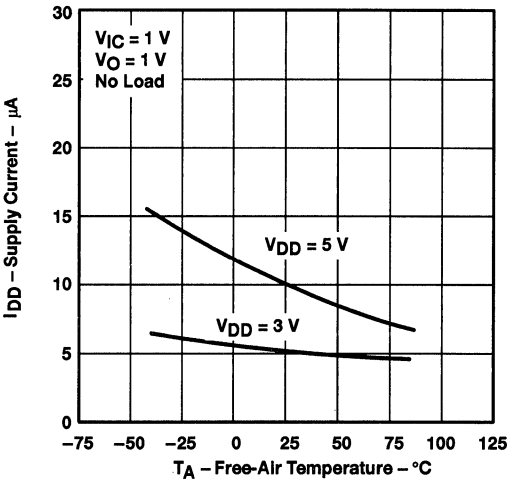


Figure 79

SLEW RATE vs SUPPLY VOLTAGE

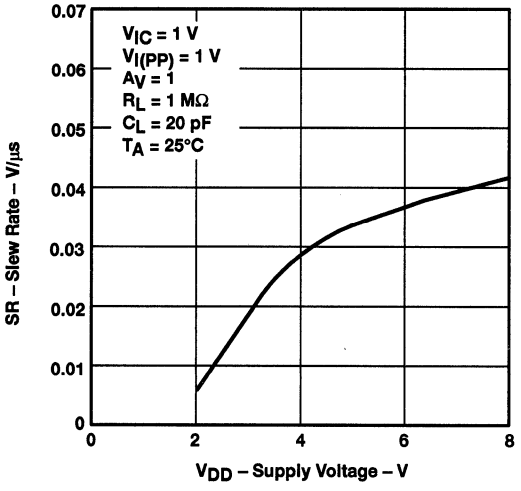


Figure 80

SLEW RATE vs FREE-AIR TEMPERATURE

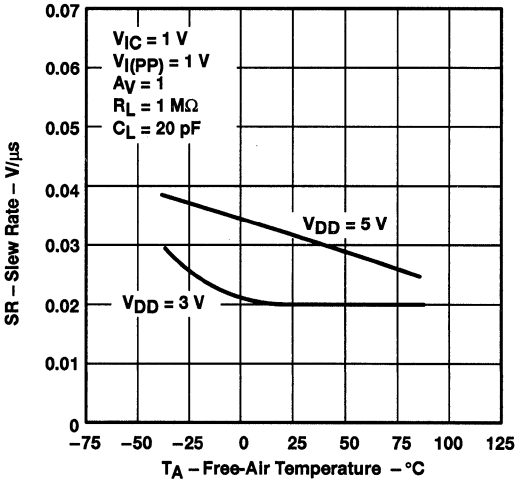


Figure 81

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

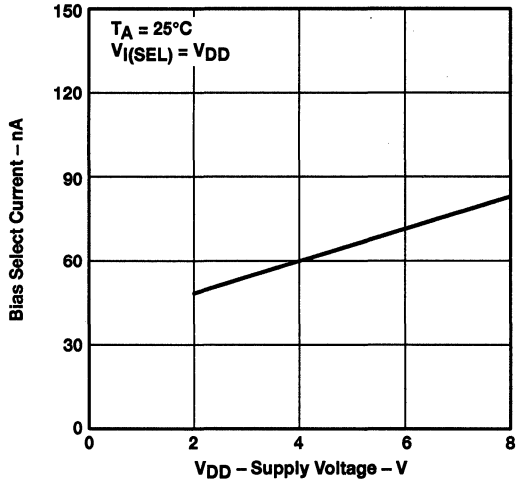


Figure 82

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

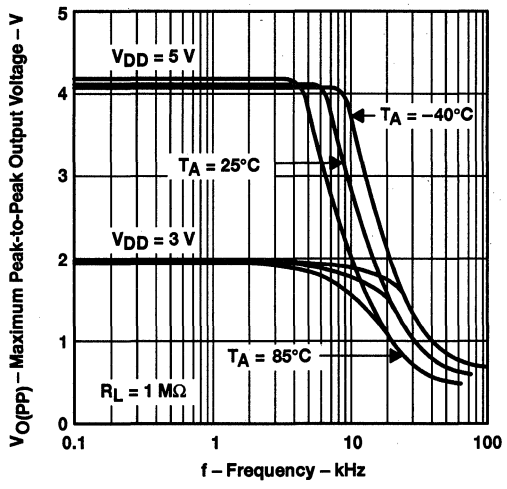


Figure 83

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

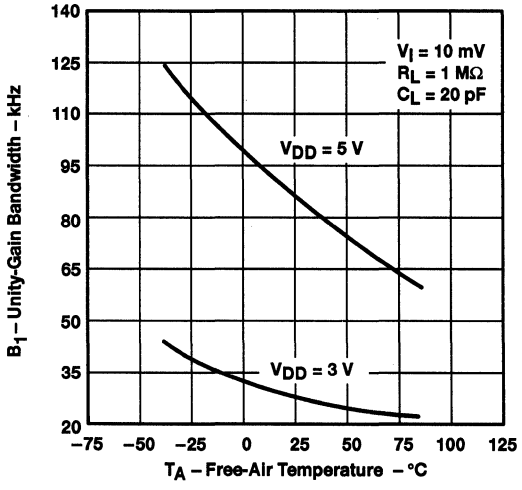


Figure 84

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

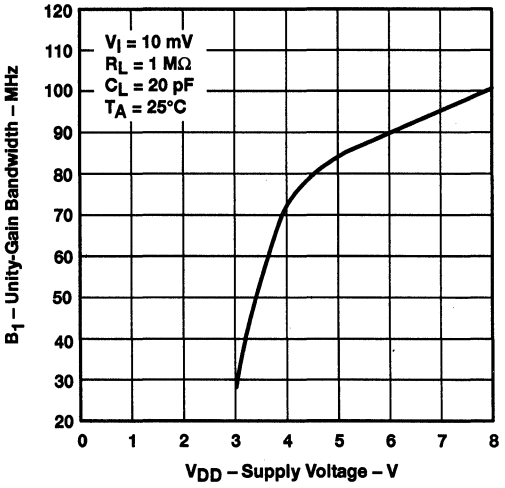


Figure 85

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

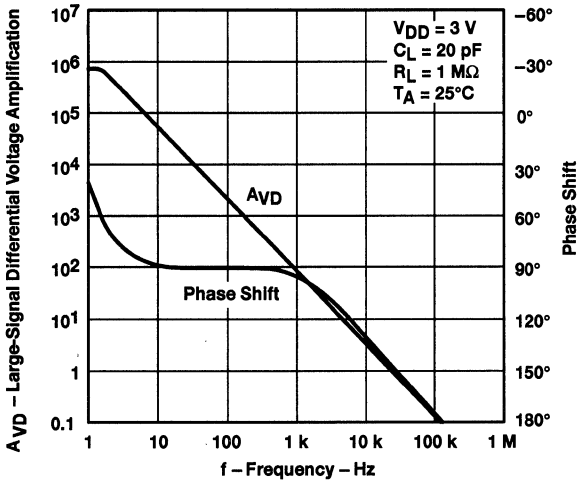


Figure 86

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

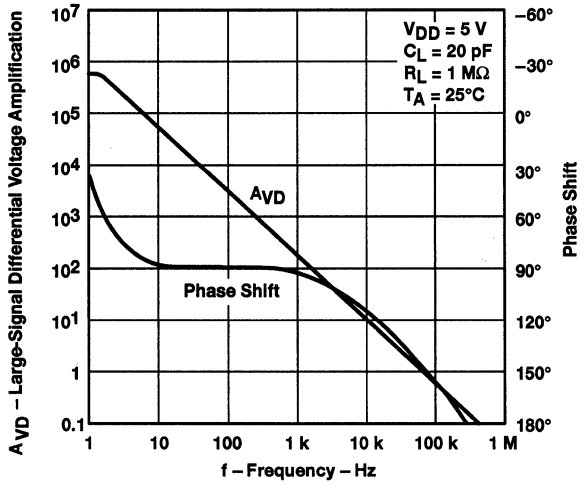


Figure 87

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

PHASE MARGIN
vs
SUPPLY VOLTAGE

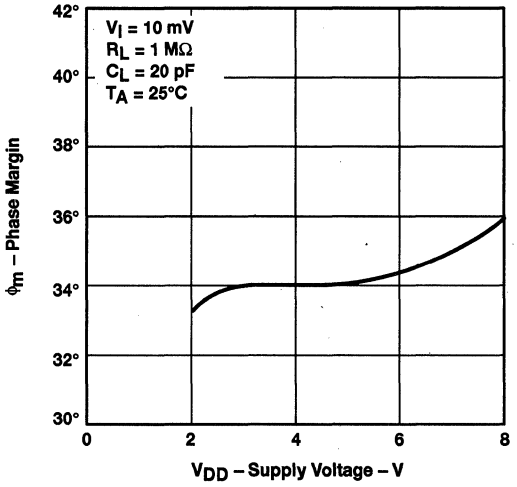


Figure 88

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

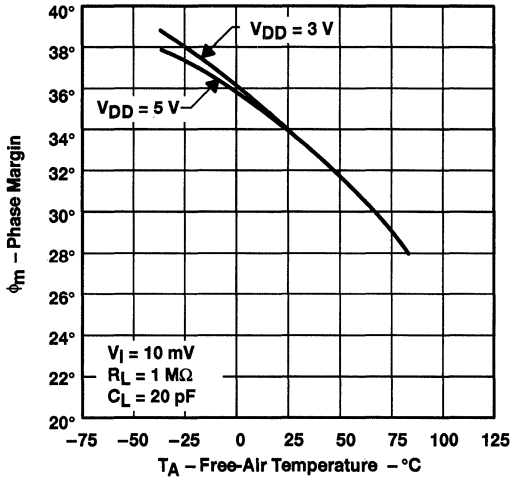


Figure 89

PHASE MARGIN
vs
LOAD CAPACITANCE

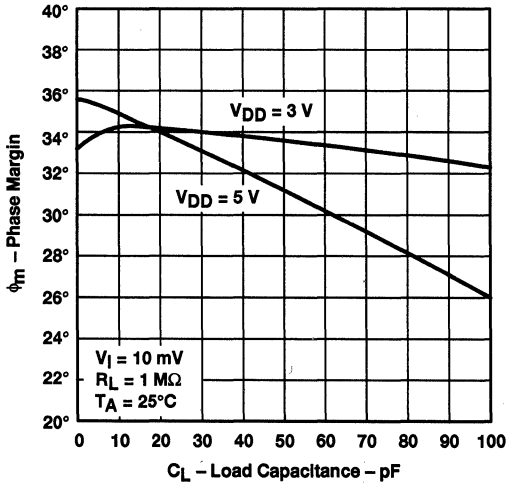


Figure 90

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

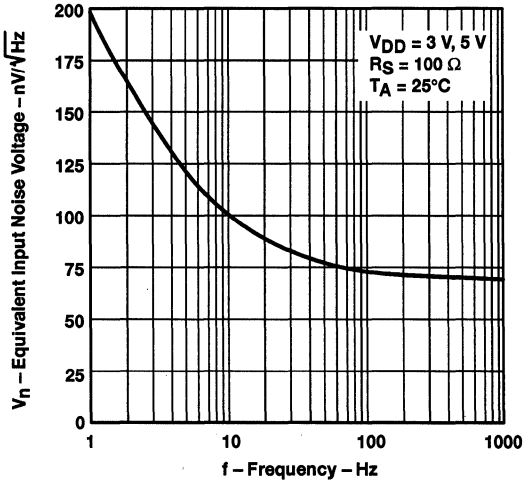
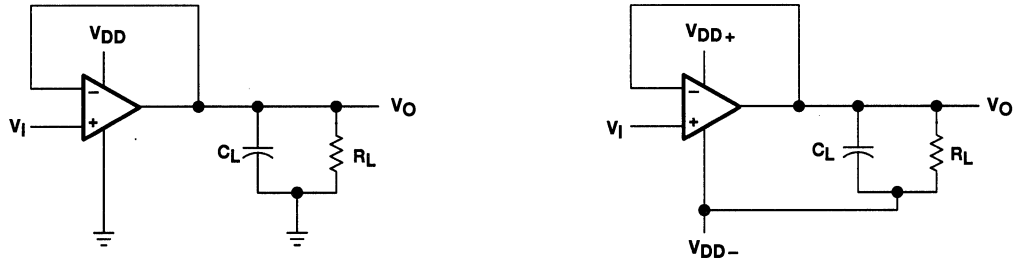


Figure 91

PARAMETER MEASUREMENT INFORMATION

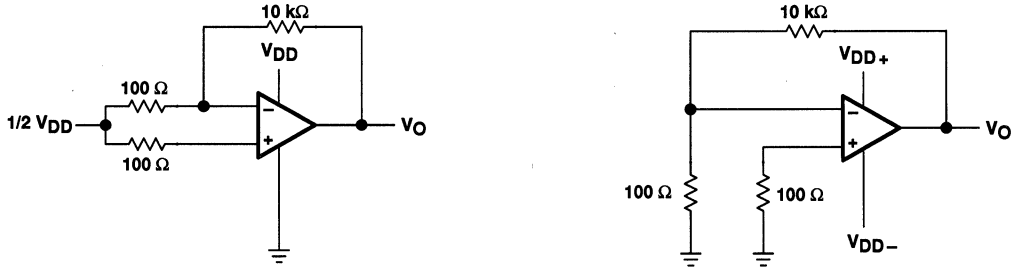
single-supply versus split-supply test circuits

Because the TLV2341 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



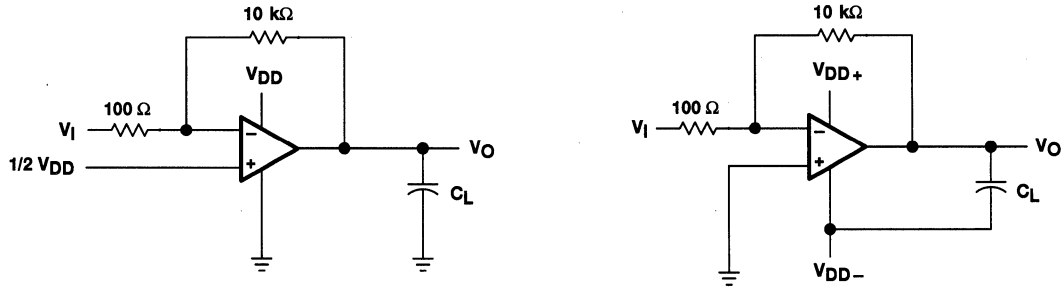
(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 92. Unity-Gain Amplifier



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 93. Noise Test Circuits



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 94. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2341 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 95). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

  Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

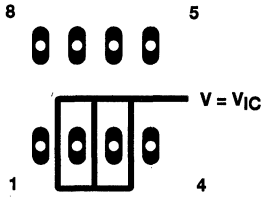


Figure 95. Isolation Metal Around Device Inputs (P Package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 92. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 96). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

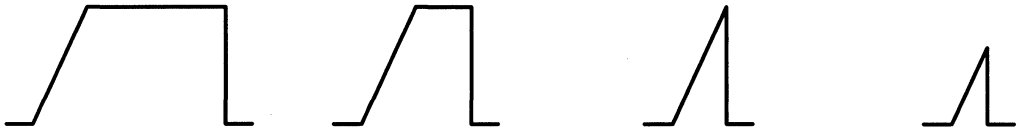


Figure 96. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2341 performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

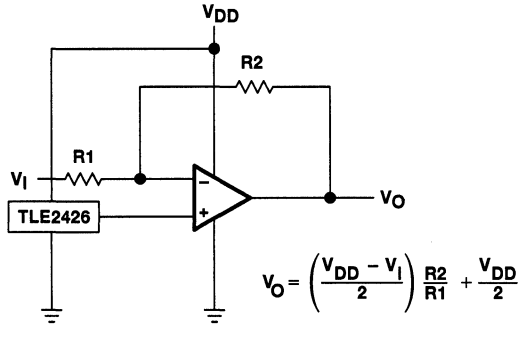


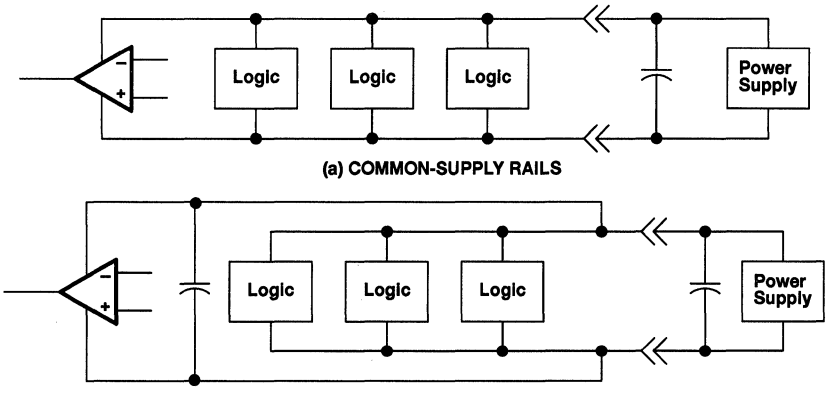
Figure 97. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)

The TLV2341 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 98); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) COMMON-SUPPLY RAILS

(b) SEPARATE-BYPASSED SUPPLY RAILS (PREFERRED)

Figure 98. Common Versus Separate Supply Rails

input offset voltage nulling

The TLV2341 offers external input offset null control. Nulling of the input offset voltage can be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected as shown in Figure 99. The amount of nulling range varies with the bias selection. In the high-bias mode, the nulling range allows the maximum offset voltage specified to be trimmed to zero. In low-bias and medium-bias modes, total nulling may not be possible.

(a) SINGLE SUPPLY

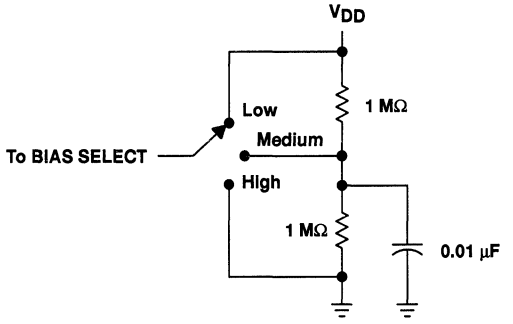
(b) SPLIT SUPPLY

Figure 99. Input Offset Voltage Null Circuit

APPLICATION INFORMATION

bias selection

Bias selection is achieved by connecting the bias-select pin to one of the three voltage levels (see Figure 100). For medium-bias applications, it is recommended that the bias-select pin be connected to the midpoint between the supply rails. This is a simple procedure in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode necessitates using a voltage divider as indicated. The use of large-value resistors in the voltage divider reduces the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the midpoint may be used if it is within the voltages specified in the following table.



BIAS MODE	BIAS-SELECT VOLTAGE (Single Supply)
Low	V_{DD}
Medium	1 V to V_{DD} –1 V
High	GND

Figure 100. Bias Selection for Single-Supply Applications

input characteristics

The TLV2341 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower the range limit includes the negative rail, while the upper range limit is specified at V_{DD} –1 V at T_A = 25°C and at V_{DD} –1.2 V at all other temperatures.

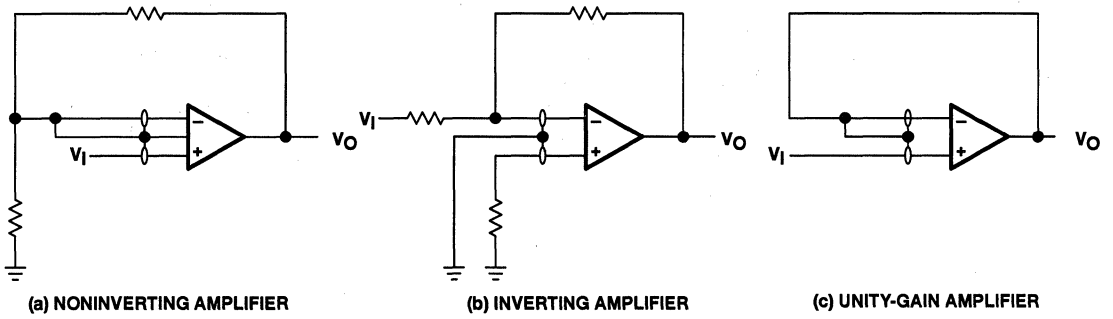
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2341 good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2341 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 95 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 101).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

APPLICATION INFORMATION

input characteristics (continued)



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 101. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifiers circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2341 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 102). The value of this capacitor is optimized empirically.

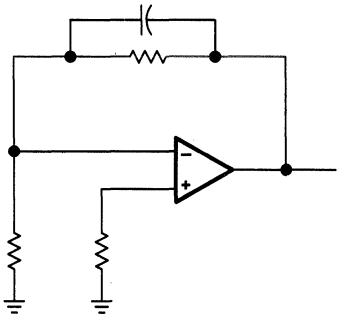


Figure 102. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV2341 incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2341 inputs and output are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by

APPLICATION INFORMATION

design be forward biased. Applied input and output voltage should not exceed the supply voltage by more that 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2341 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2341 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 103). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

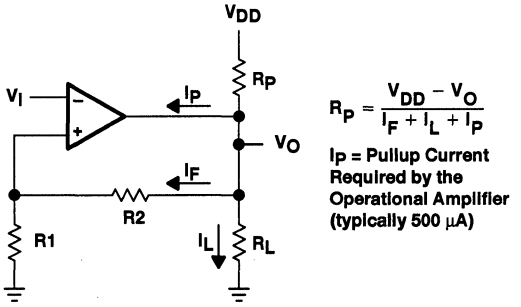


Figure 103. Resistive Pullup to Increase V_{OH}

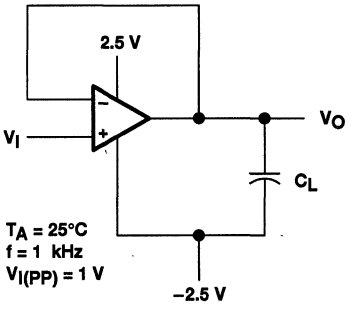
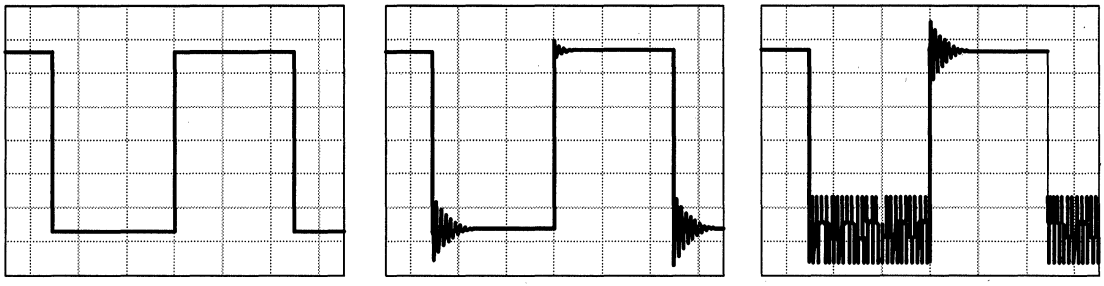


Figure 104. Test Circuit for Output Characteristics

All operating characteristics of the TLV2341 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figures 105, 106 and 107). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

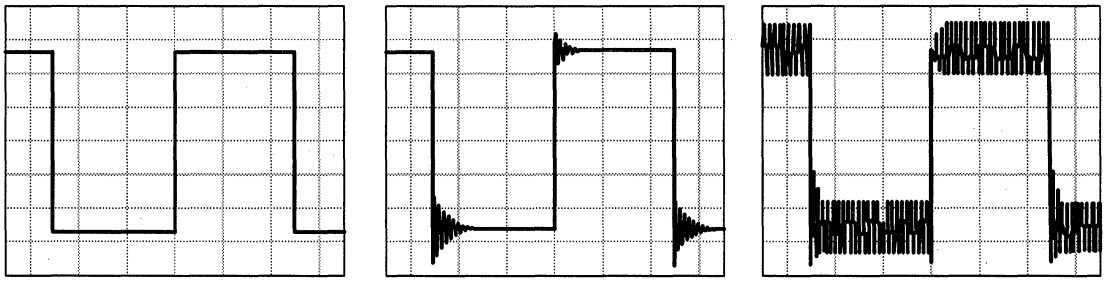
APPLICATION INFORMATION

output characteristics (continued)



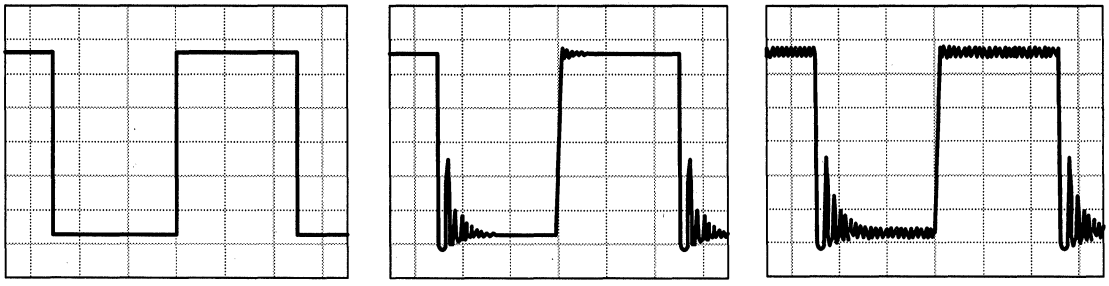
(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 130 pF, R_L = NO LOAD (c) C_L = 150 pF, R_L = NO LOAD

Figure 105. Effect of Capacitive Loads in High-Bias Mode



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 170 pF, R_L = NO LOAD (c) C_L = 190 pF, R_L = NO LOAD

Figure 106. Effect of Capacitive Loads in Medium-Bias Mode

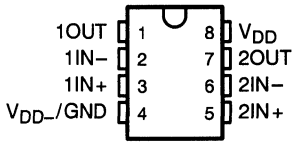


(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 260 pF, R_L = NO LOAD (c) C_L = 310 pF, R_L = NO LOAD

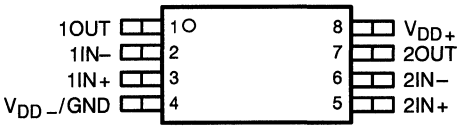
Figure 107. Effect of Capacitive Loads in Low-Bias Mode

- **Wide Range of Supply Voltages Over Specified Temperature Range: −40°C to 85°C . . . 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input-Voltage Range Extends Below the Negative Rail and Latch-Up to V_{DD} −1 V at 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)

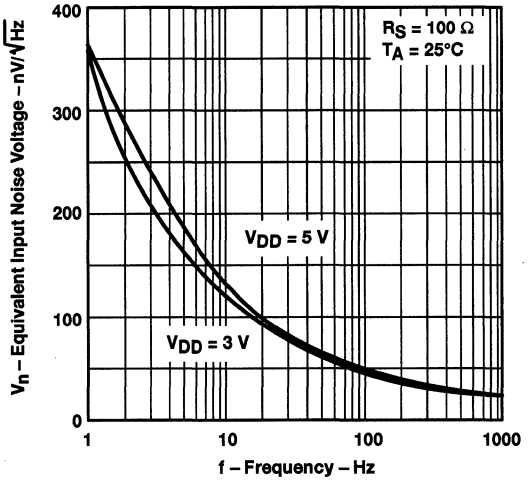


description

The TLV2342 dual operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage single-supply applications. Unlike other products in this family designed primarily to meet aggressive power consumption specifications, the TLV2342 was developed to offer ac performance approaching that of a BiFET operational amplifier while operating from a single-supply rail. At 3 V, the TLV2342 has a typical slew rate of 2.1 V/μs and 790-kHz unity-gain bandwidth.

Each amplifier is fully functional down to a minimum supply voltage of 2 V and is fully characterized, tested, and specified at both 3-V and 5-V power supplies over a temperature range of −40°C to 85°C. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



Low-voltage and low-power operation has been made possible by using Texas Instruments silicon-gate LinCMOS™ technology. The LinCMOS process also features extremely high input impedance and ultra-low input bias currents. These parameters combined with good ac performance make the TLV2342 effectual in applications such as high-frequency filters and wide-bandwidth sensors.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
−40°C to 85°C	9 mV	TLV2342ID	TLV2342IP	TLV2342IPWLE	TLV2342Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2342IDR).
The PW package is only available left-end taped and reeled (e.g., TLV2342IPWLE).

LinCMOS™ is a trademark of Texas Instruments Incorporated.

description (continued)

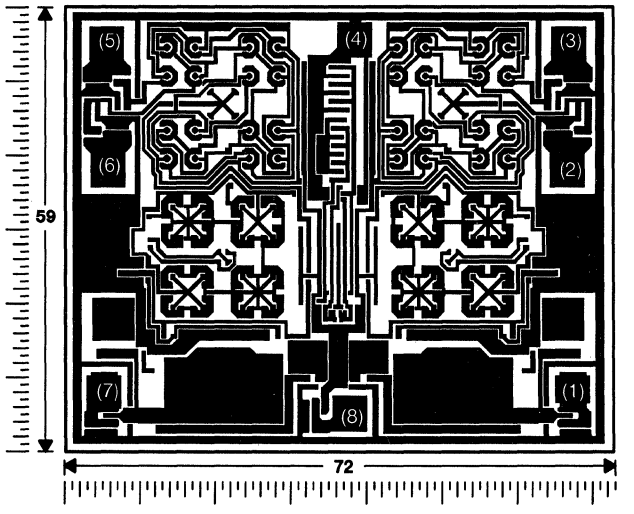
To facilitate the design of small portable equipment, the TLV2342 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

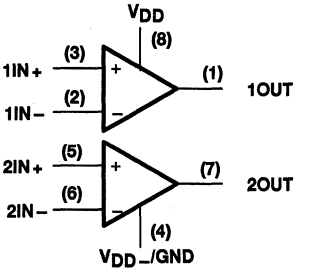
The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2342 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

TLV2342Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2342I. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

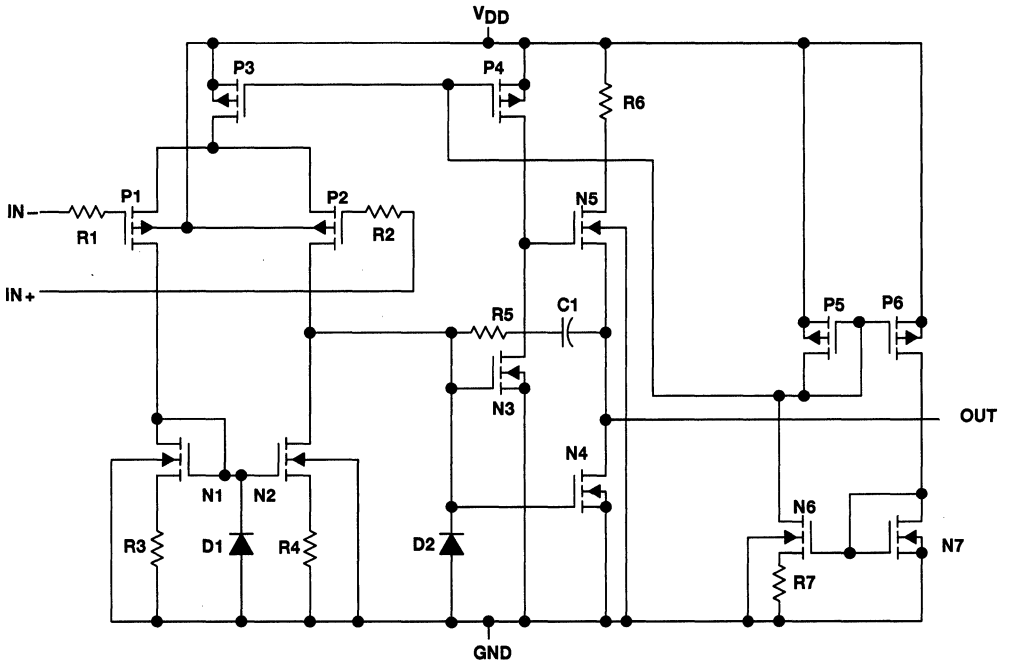
BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	54
Diodes	4
Resistors	14
Capacitors	2

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage (see Note 2) ..... $V_{DD\pm}$
Input voltage range, V_I (any input) ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
Output current, I_O ..... ±30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	725 mV	5.8 mW/°C	377 mW
P	1000 mV	8.0 mW/°C	520 mW
PW	525 mV	4.2 mW/°C	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	−0.2	1.8	V
	V_{DD} = 5 V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2342I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.6	9		1.1	9	mV
			Full range			11			11	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		2.7			2.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.7		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		120	150		90	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	25°C	3	11		5	23		V/mV
			Full range	2			3.5			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	78		65	80		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	95		70	95		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		0.65	3		1.4	3.2	mA
			Full range			4			4.4	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2342I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, See Figure 30	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		2.1		V/μs
				85°C		1.7		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 30	25°C		170		kHz
				85°C		145		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 10 kΩ,	C_L = 20 pF, See Figure 32	25°C		790		kHz
				85°C		690		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 10 kΩ,	−40°C		53°		
				25°C		49°		
				85°C		47°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2342I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, C_L = 20 pF, See Figure 30	$V_{I(PP)}$ = 1 V	25°C		3.6		V/μs
				85°C		2.8		
			$V_{I(PP)}$ = 2.5 V	25°C		2.9		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 30	25°C		320		kHz
				85°C		250		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 10 kΩ,	C_L = 20 pF, See Figure 32	25°C		1.7		kHz
				85°C		1.2		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 10 kΩ,	−40°C		49°		
				25°C		46°		
				85°C		43°		

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLV2342Y						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, R_S = 50 Ω,	V_{IC} = 1 V, R_L = 10 kΩ		0.6	9		1.1	9	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)			−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, I_{OH} = −1 mA	V_{ID} = 100 mV,	1.75	1.9		3.2	3.7		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, I_{OL} = 1 mA	V_{ID} = 100 mV,		120	150		90	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, See Note 6	R_L = 10 kΩ,	3	11		5	23		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, R_S = 50 Ω	V_{IC} = V_{ICR}min,	65	78		65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	V_O = 1 V, R_S = 50 Ω	V_{IC} = 1 V,	70	95		70	95		dB
I_{DD}	Supply current	V_O = 1 V, No load	V_{IC} = 1 V,		0.65	3		1.4	3.2	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current	5
		vs Supply voltage	6
		vs Temperature	7
V_{OL}	Low-level output voltage	vs Common-mode input voltage	8
		vs Temperature	9, 11
		vs Differential input voltage	10
		vs Low-level output current	12
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage	13
		vs Temperature	14
I_{IB}/I_{IO}	Input bias and offset currents	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply voltage	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
SR	Slew rate	vs Supply voltage	19
		vs Temperature	20
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Unity-gain bandwidth	vs Temperature	22
		vs Supply voltage	23
A_{VD}	Large-signal differential voltage amplification	vs Frequency	24, 25
ϕ_m	Phase margin	vs Supply voltage	26
		vs Temperature	27
		vs Load capacitance	28
V_n	Equivalent input noise voltage	vs Frequency	29
	Phase shift	vs Frequency	24, 25

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2342
INPUT OFFSET VOLTAGE

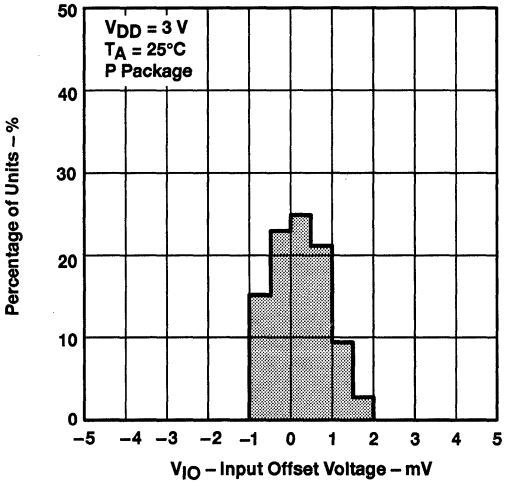


Figure 1

DISTRIBUTION OF TLV2342
INPUT OFFSET VOLTAGE

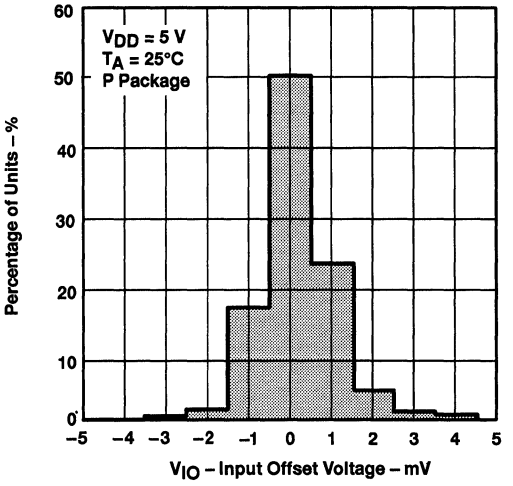


Figure 2

DISTRIBUTION OF TLV2342
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

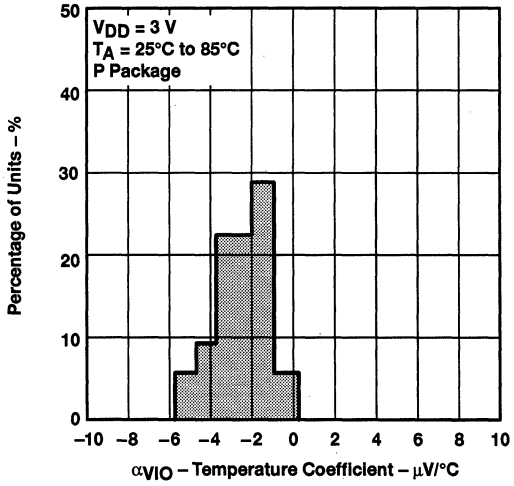


Figure 3

DISTRIBUTION OF TLV2342
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

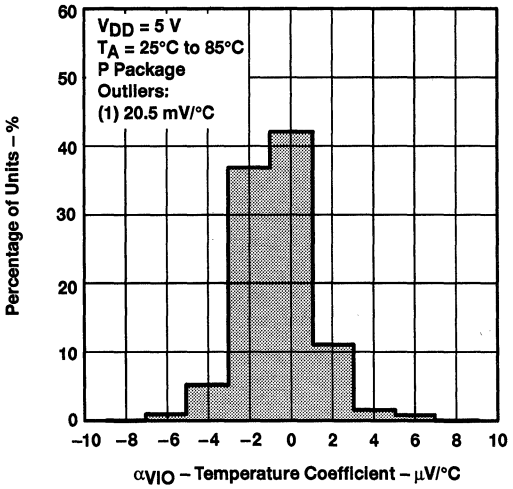


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

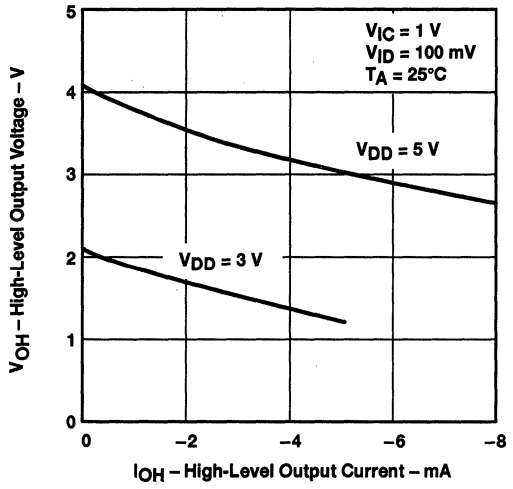


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

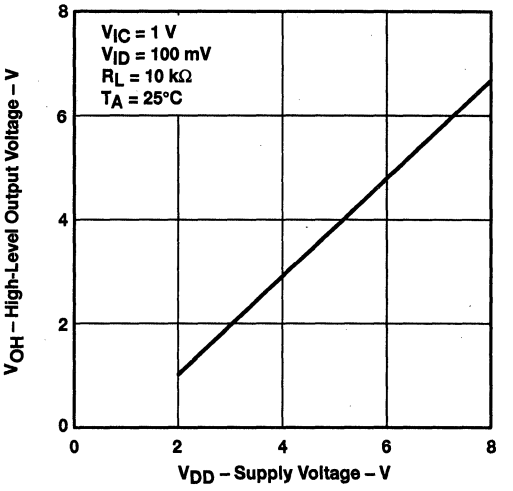


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

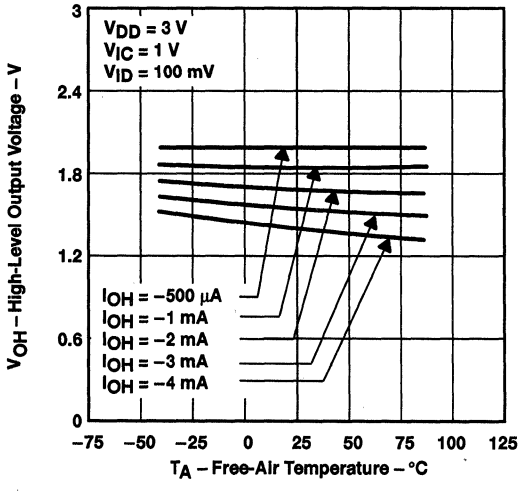


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

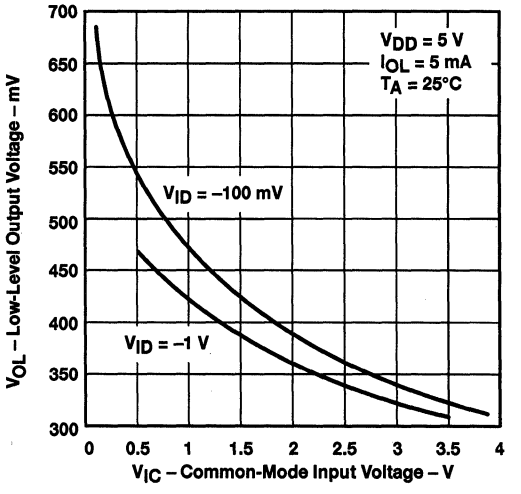


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

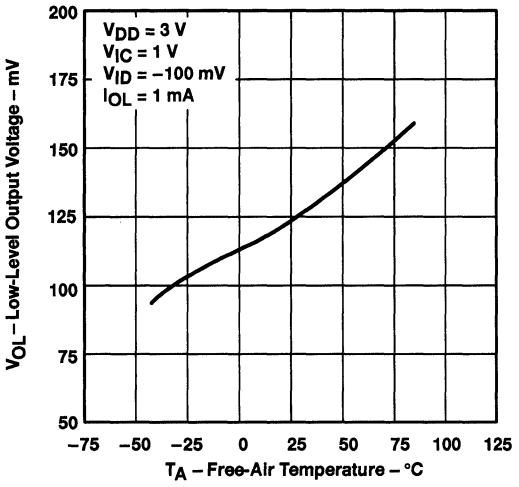


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

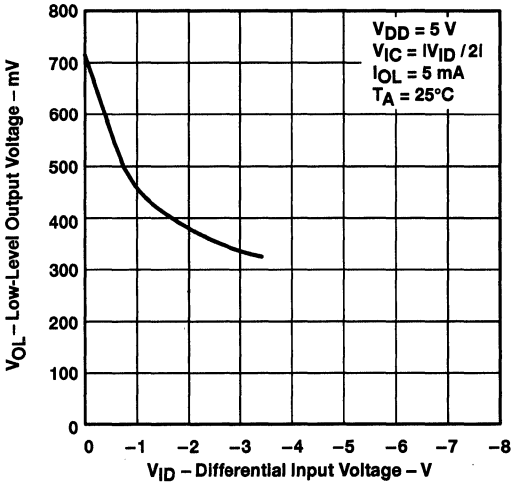


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

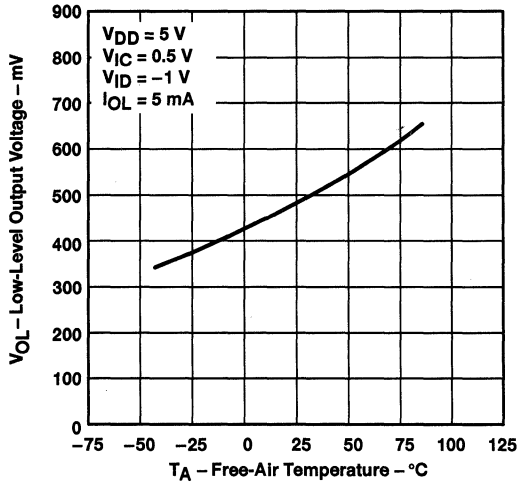


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

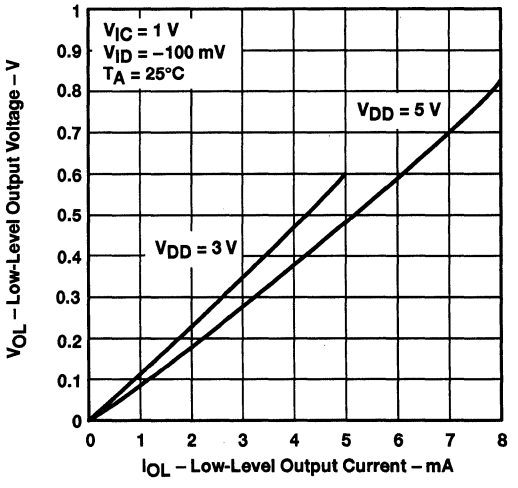


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

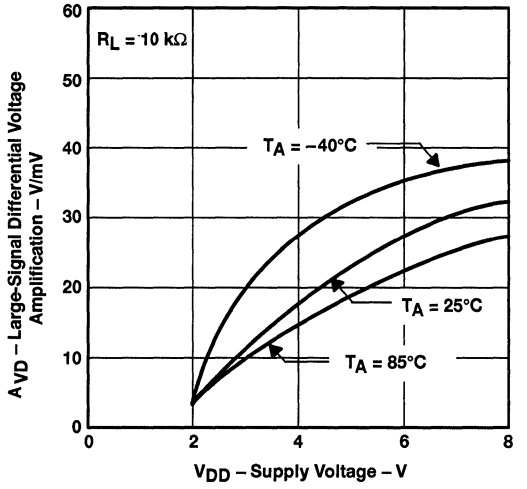


Figure 13

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

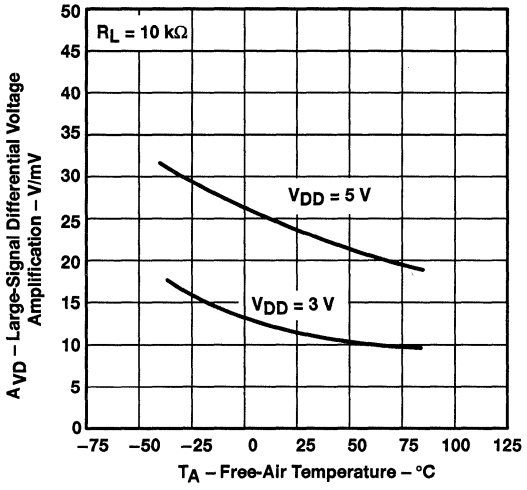
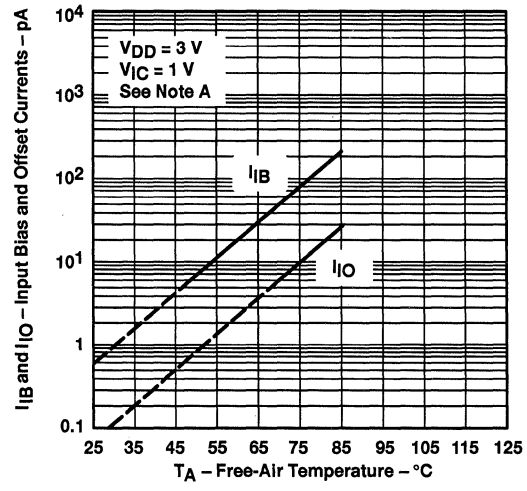


Figure 14

INPUT BIAS CURRENT AND INPUT
OFFSET CURRENT
vs
FREE-AIR TEMPERATURE



NOTE: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 15

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

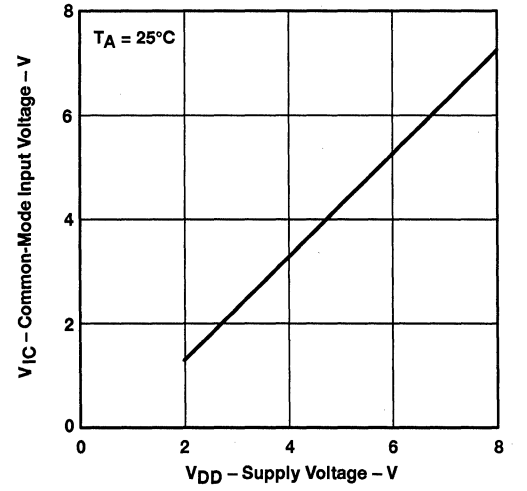


Figure 16

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

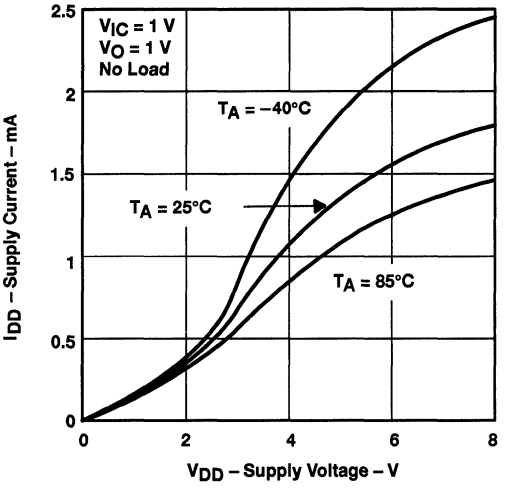


Figure 17

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

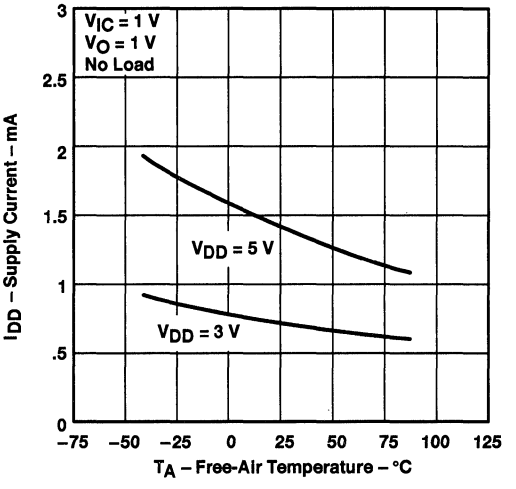


Figure 18

SLEW RATE vs SUPPLY VOLTAGE

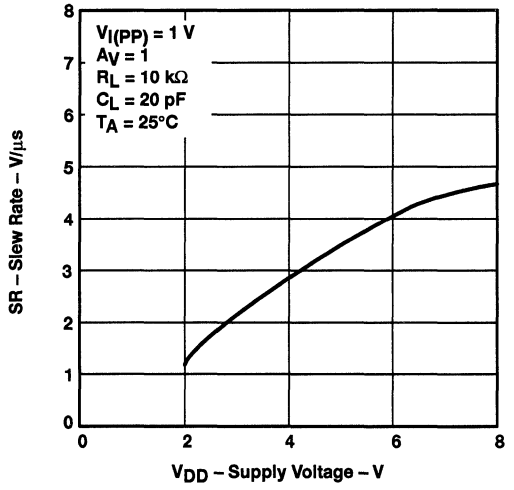


Figure 19

SLEW RATE vs FREE-AIR TEMPERATURE

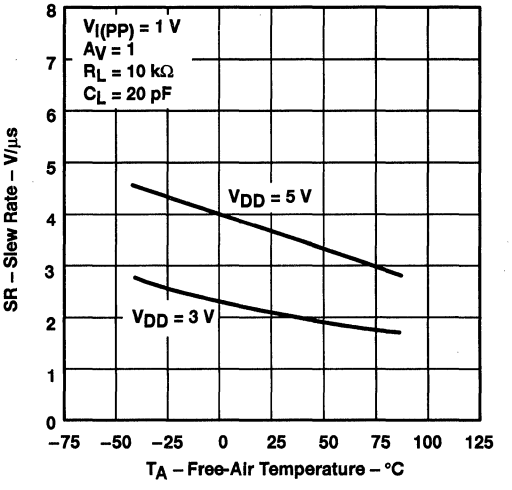


Figure 20

TYPICAL CHARACTERISTICS

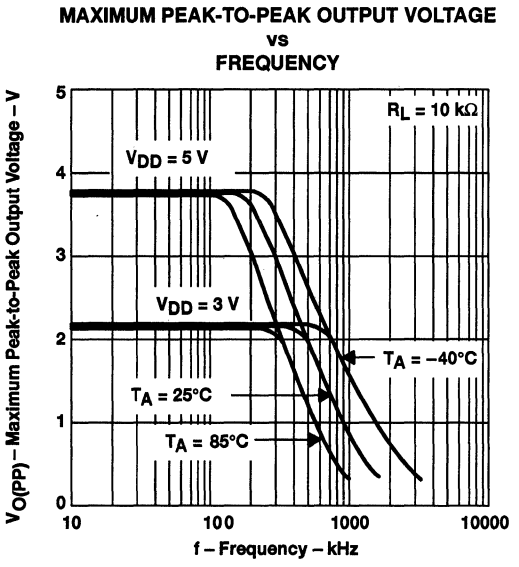


Figure 21

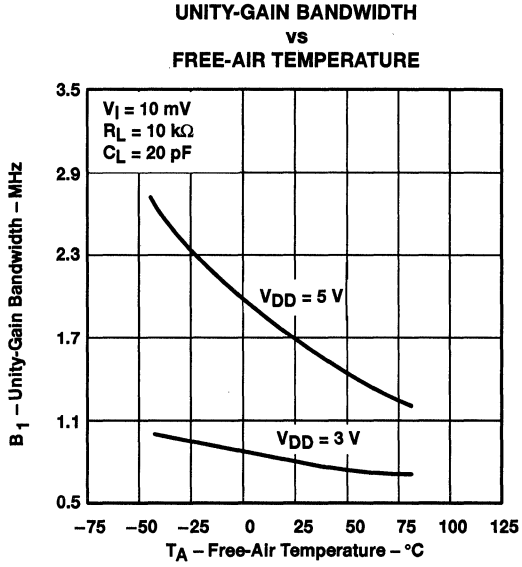


Figure 22

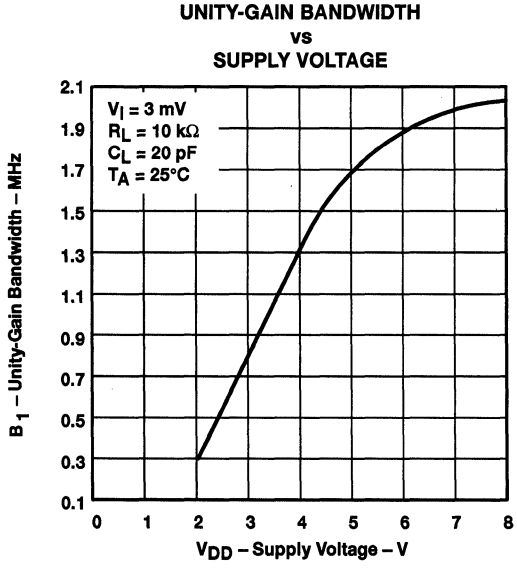


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

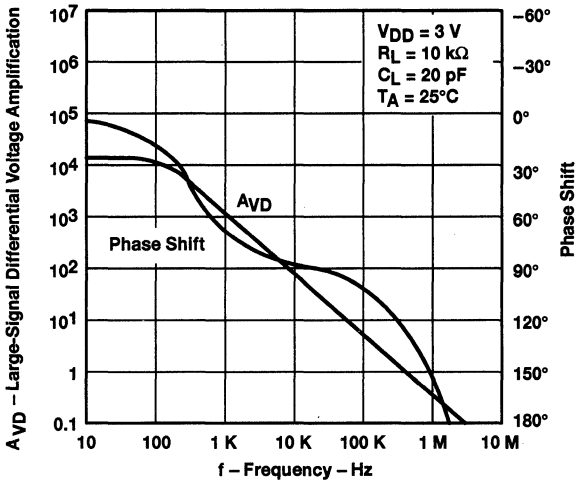


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

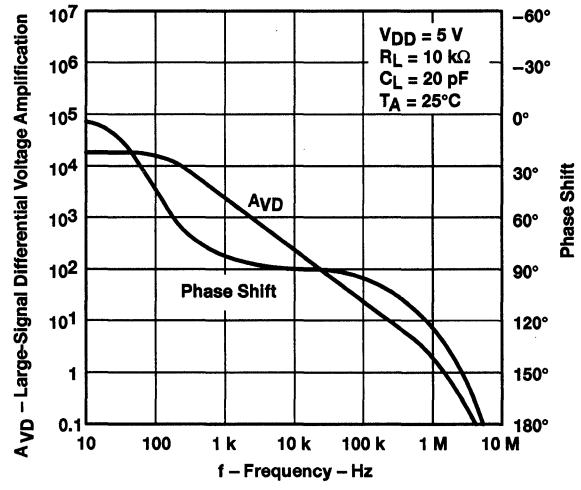


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN vs SUPPLY VOLTAGE

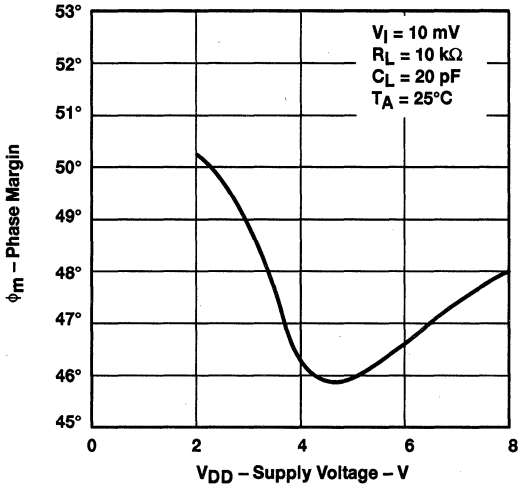


Figure 26

PHASE MARGIN vs FREE-AIR TEMPERATURE

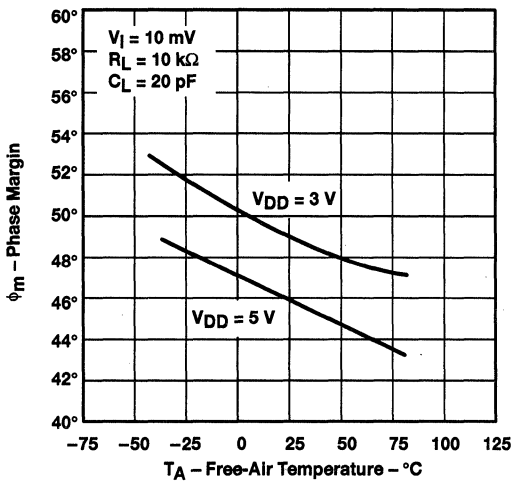


Figure 27

PHASE MARGIN vs LOAD CAPACITANCE

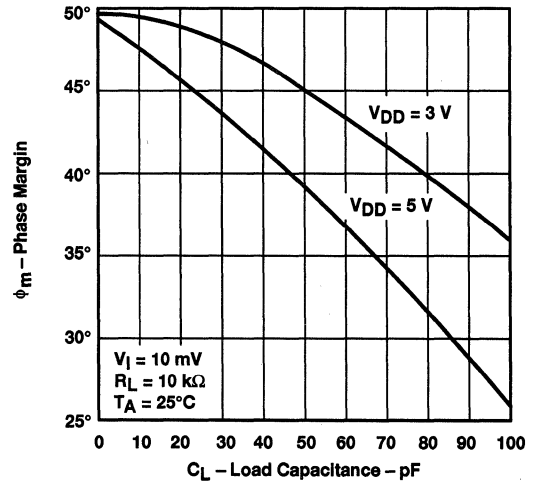


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

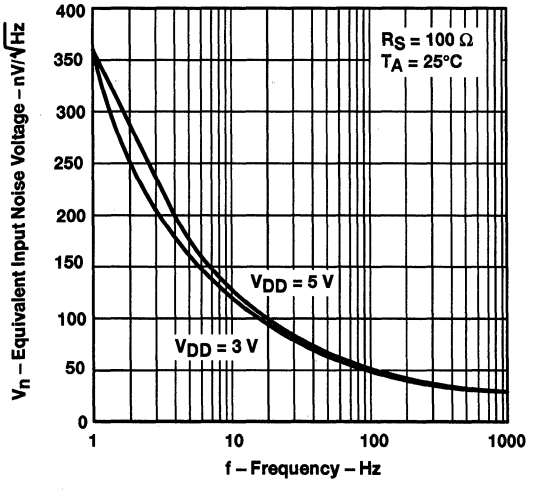


Figure 29

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2342 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

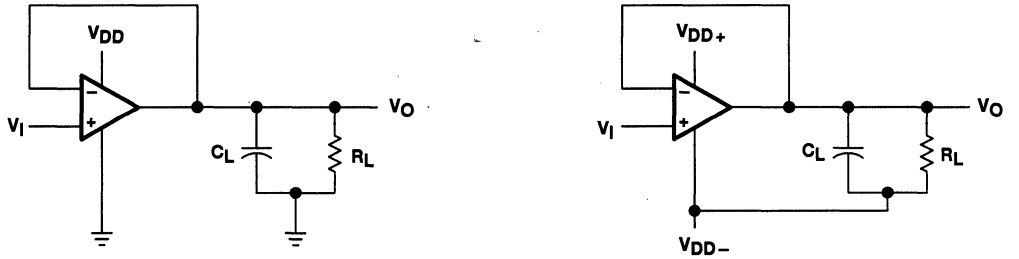


Figure 30. Unity-Gain Amplifier

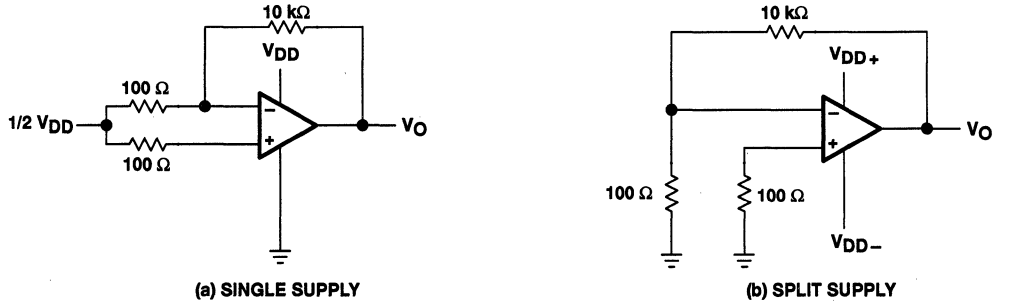


Figure 31. Noise Test Circuits

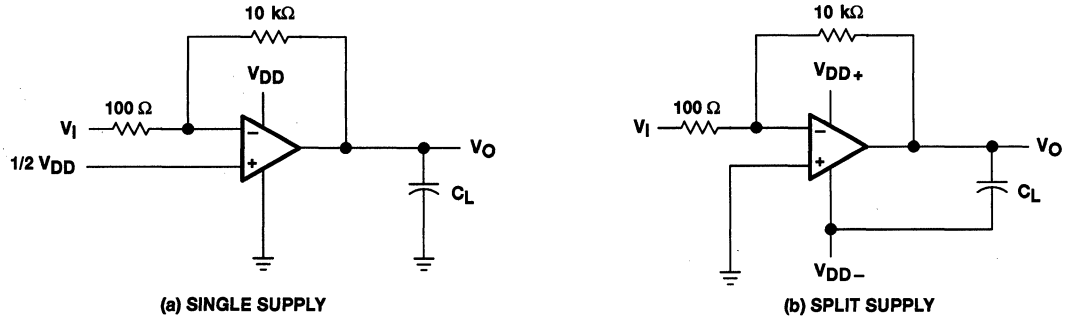


Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2342 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

  Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading: therefore, an open-socket reading is not feasible using this method.

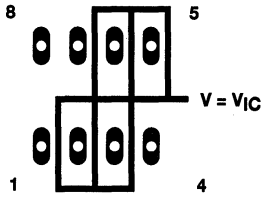


Figure 33. Isolation Metal Around Device Inputs (P Package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

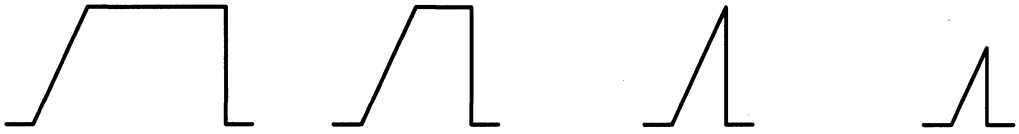


Figure 34. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2342 performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

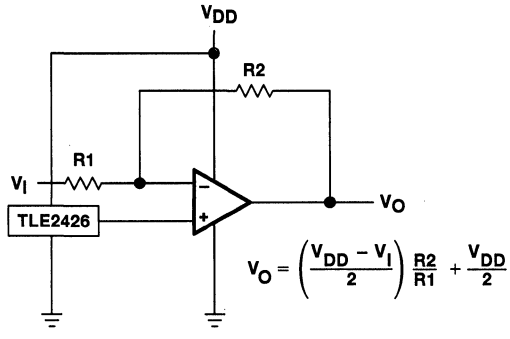


Figure 35. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)

The TLV2342 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

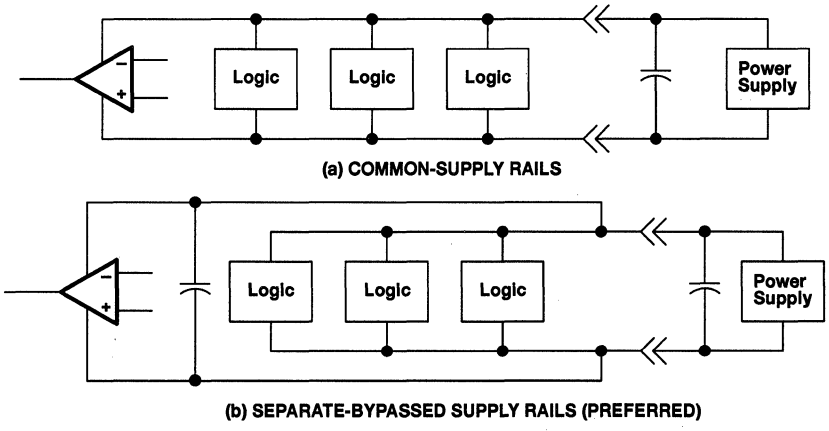


Figure 36. Common Versus Separate Supply Rails

input characteristics

The TLV2342 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower the range limit includes the negative rail, while the upper range limit is specified at V_{DD} –1 V at T_A = 25°C and at V_{DD}– 1.2 V at all other temperatures.

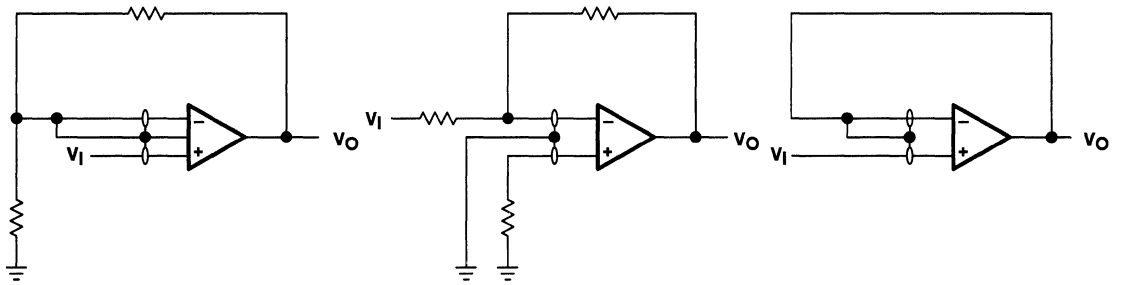
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2342 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2342 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

APPLICATION INFORMATION

input characteristics (continued)



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 37. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifiers circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2342 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

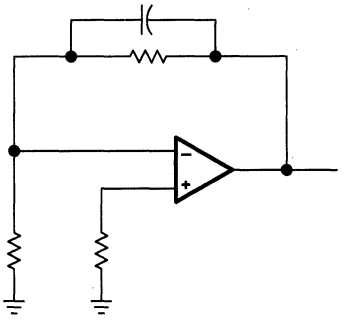


Figure 38. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV2342 incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2342 inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes

APPLICATION INFORMATION

should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2342 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2342 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

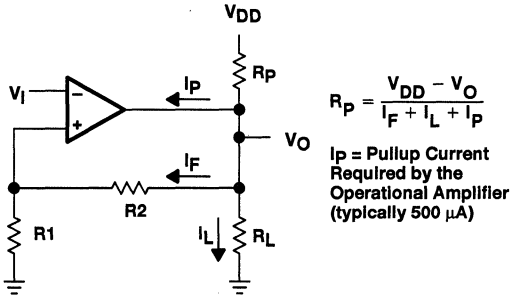


Figure 39. Resistive Pullup to Increase V_{OH}

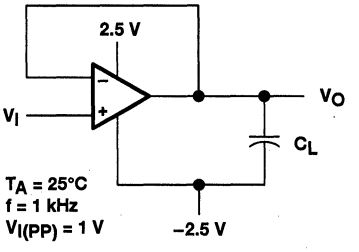
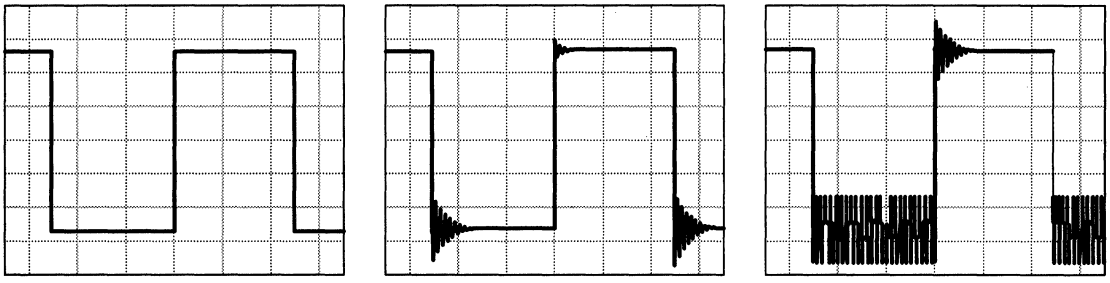


Figure 40. Test Circuit for Output Characteristics

All operating characteristics of the TLV2342 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figures 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

APPLICATION INFORMATION

output characteristics (continued)



(a) C_L = 20 pF, R_L = NO LOAD

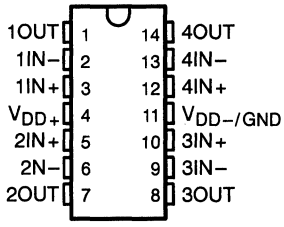
(b) C_L = 130 pF, R_L = NO LOAD

(c) C_L = 150 pF, R_L = NO LOAD

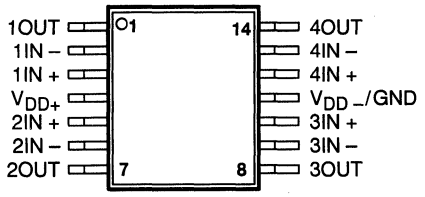
Figure 41. Effect of Capacitive Loads

- **Wide Range of Supply Voltages Over Specified Temperature Range: −40°C to 85°C . . . 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} −1 V at 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**

D OR N PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)

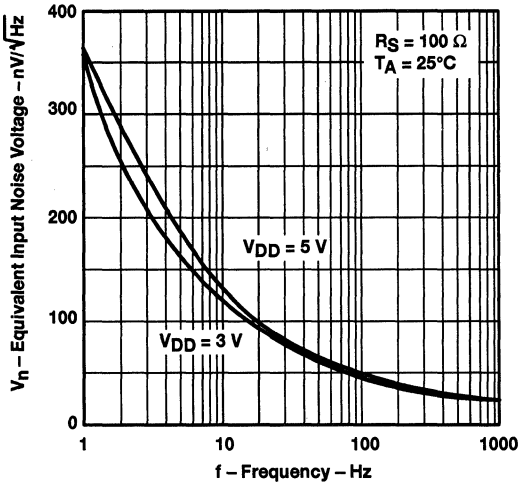


description

The TLV2344 quad operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage single-supply applications. Unlike other products in this family designed primarily to meet aggressive power consumption specifications, the TLV2344 is designed to offer ac performance approaching that of a BiFET operational amplifier while operating from a single-supply rail. At 3 V, the TLV2344 has a typical slew rate of 2.1 V/μs and 790-kHz unity-gain bandwidth.

Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies over a temperature range of −40°C to 85°C. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
−40°C to 85°C	10 mV	TLV2344ID	TLV2344IN	TLV2344IPWLE	TLV2344Y

Available in tape and reel. Add R suffix to the device type when ordering (e.g., TLV2344IDR).
The PW package is only available left-end taped and reeled (e.g., TLV2344IPWLE).

LinCMOS™ is a trademark of Texas Instruments Incorporated.

description (continued)

Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon-gate LinCMOS™ technology. The LinCMOS process also features extremely high input impedance and ultra-low input bias currents. These parameters combined with good ac performance make the TLV2344 effectual in applications such as high-frequency filters and wide-bandwidth sensors.

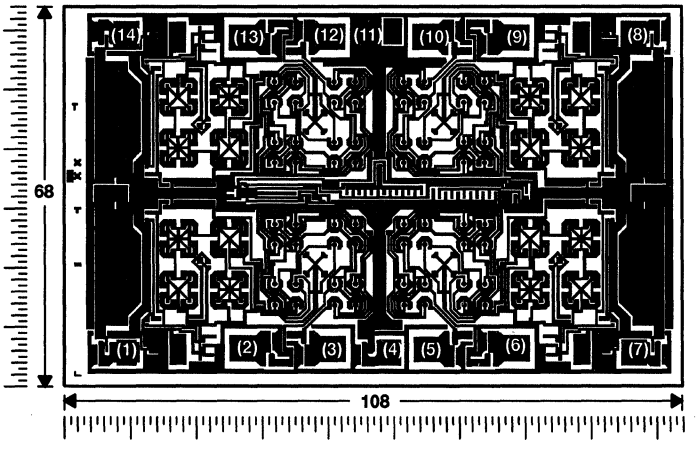
To facilitate the design of small portable equipment, the TLV2344 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

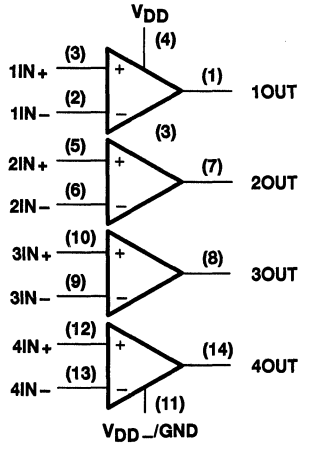
The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2344 incorporates internal ESD-protection circuits that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

TLV2344Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2344I. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

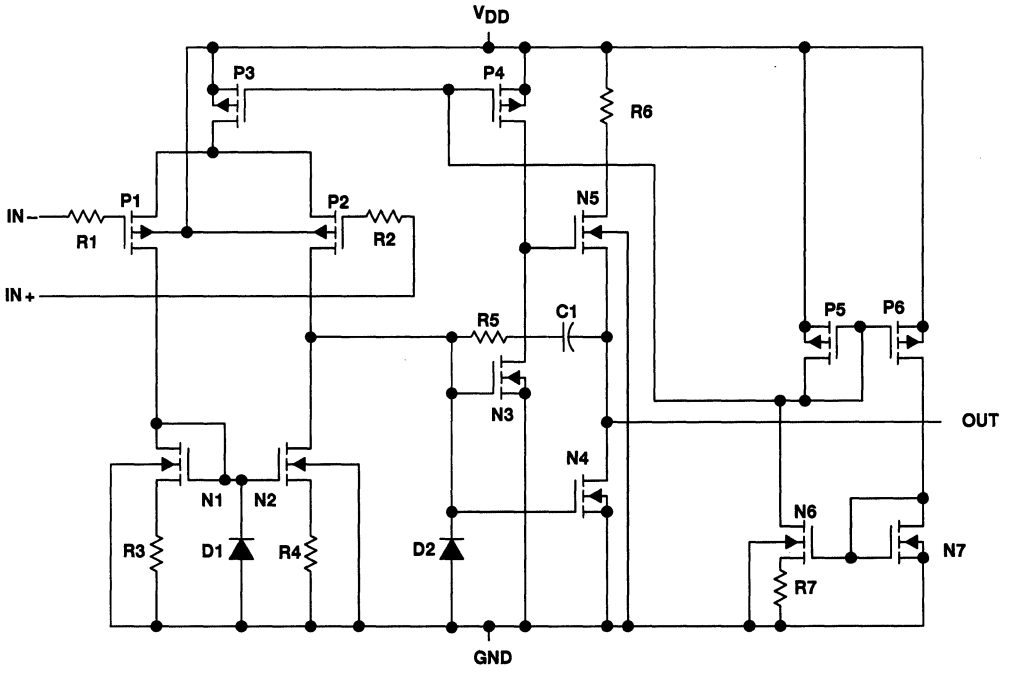
BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	8
Diodes	28
Resistors	4
Capacitors	108

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... $V_{DD\pm}$
Input voltage range, V_I (any input) ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
Output current, I_O ..... ±30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application selection).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1575 mW	5.6 mW/°C	364 mW
PW	700 mW	12.6 mW/°C	819 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	−0.2	1.8	V
	V_{DD} = 5 V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2344I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		2.7			2.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.7		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		120	150		90	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	25°C	3	11		5	23		V/MV
			Full range	2			3.5			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	78		65	80		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	95		70	95		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		1.3	6		2.7	6.4	mA
			Full range			8			8.8	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2344I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, See Figure 30	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		2.1		V/μs
				85°C		1.7		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 30	25°C		170		kHz
				85°C		145		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 10 kΩ,	C_L = 20 pF, See Figure 32	25°C		790		kHz
				85°C		690		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 10 kΩ,	−40°C		53°		
				25°C		49°		
				85°C		47°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2344I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, C_L = 20 pF, See Figure 30	$V_{I(PP)}$ = 1 V	25°C		3.6		V/μs
				85°C		2.8		
			$V_{I(PP)}$ = 2.5 V	25°C		2.9		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 30	25°C		320		kHz
				85°C		250		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 10 kΩ,	C_L = 20 pF, See Figure 32	25°C		1.7		MHz
				85°C		1.2		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 10 kΩ,	−40°C		49°		
				25°C		46°		
				85°C		43°		

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2344Y						UNIT
			V_{DD} = 3 V			V_{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ		1.1	10		1.1	10	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	1.75	1.9		3.2	3.7		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA		120	150		90	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	3	11		5	23		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	78		65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω	70	95		70	95		dB
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		1.3	6		2.7	6.4	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current	5
		vs Supply voltage	6
		vs Temperature	7
V_{OL}	Low-level output voltage	vs Common-mode input voltage	8
		vs Temperature	9, 11
		vs Differential input voltage	10
		vs Low-level output current	12
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage	13
		vs Temperature	14
I_{IB}/I_{IO}	Input bias and offset currents	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply voltage	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
SR	Slew rate	vs Supply voltage	19
		vs Temperature	20
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Unity-gain bandwidth	vs Temperature	22
		vs Supply voltage	23
A_{VD}	Large-signal differential voltage amplification	vs Frequency	24, 25
ϕ_m	Phase margin	vs Supply voltage	26
		vs Temperature	27
		vs Load capacitance	28
V_n	Equivalent input noise voltage	vs Frequency	29
	Phase shift	vs Frequency	24, 25

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2344
INPUT OFFSET VOLTAGE**

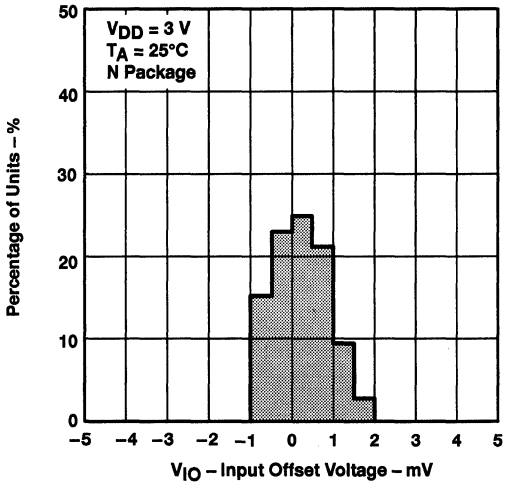


Figure 1

**DISTRIBUTION OF TLV2344
INPUT OFFSET VOLTAGE**

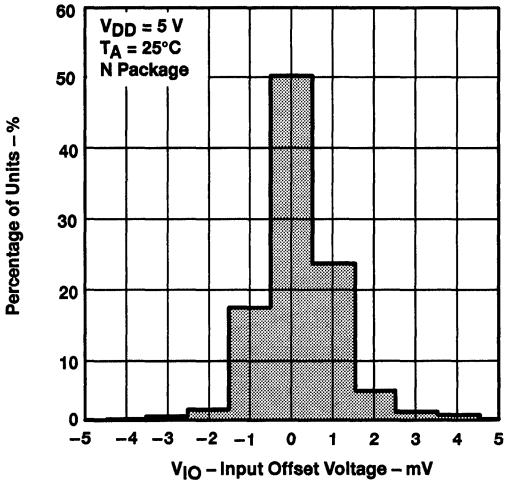


Figure 2

**DISTRIBUTION OF TLV2344
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

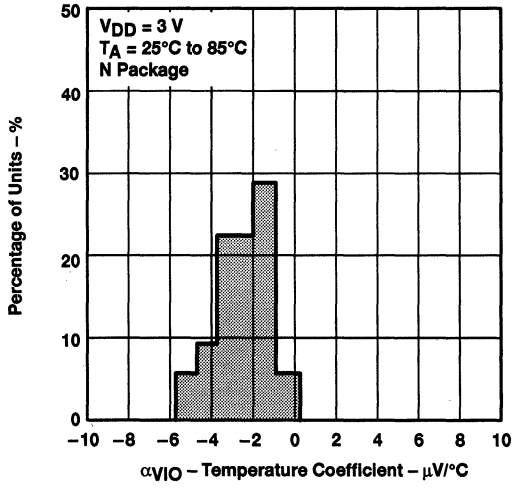


Figure 3

**DISTRIBUTION OF TLV2344
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

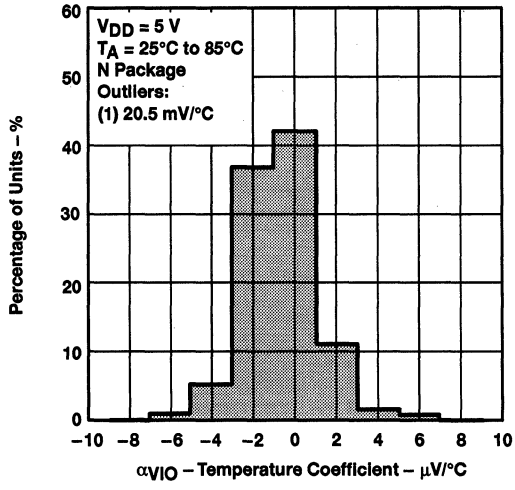


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

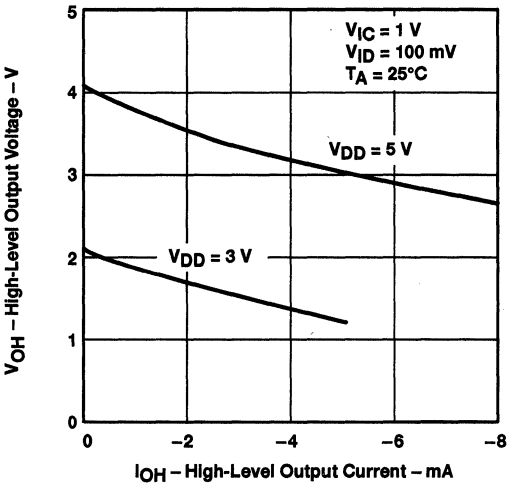


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

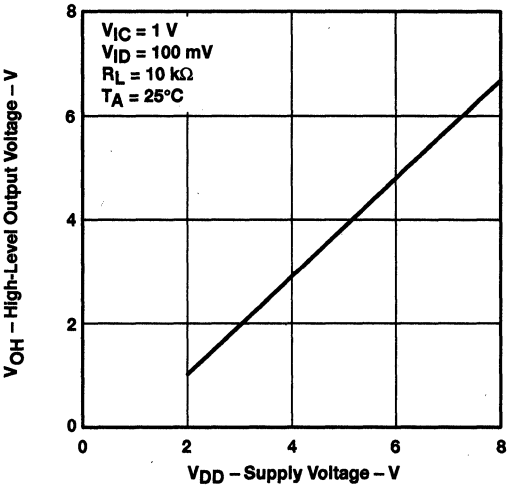


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

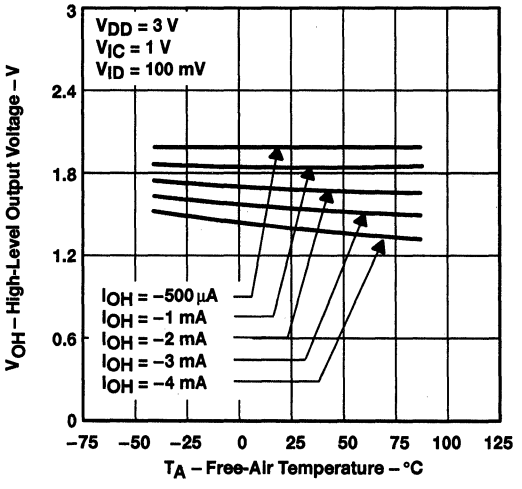


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

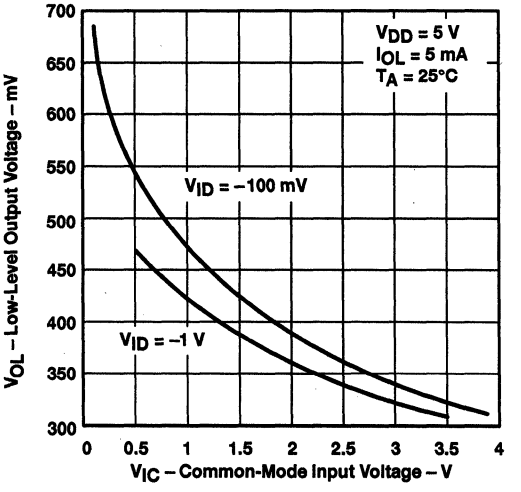


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

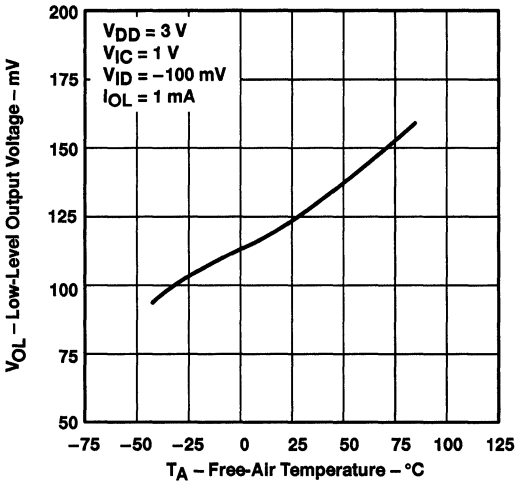


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

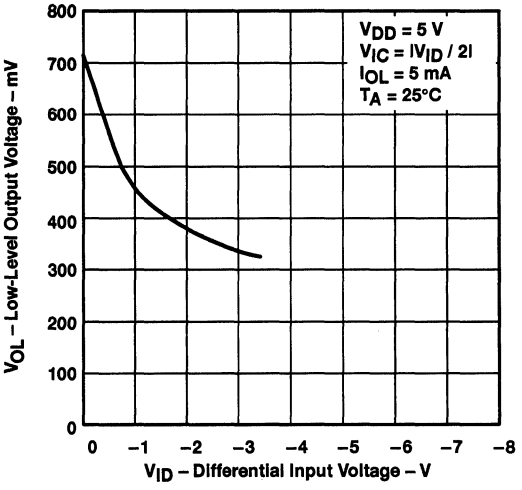


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

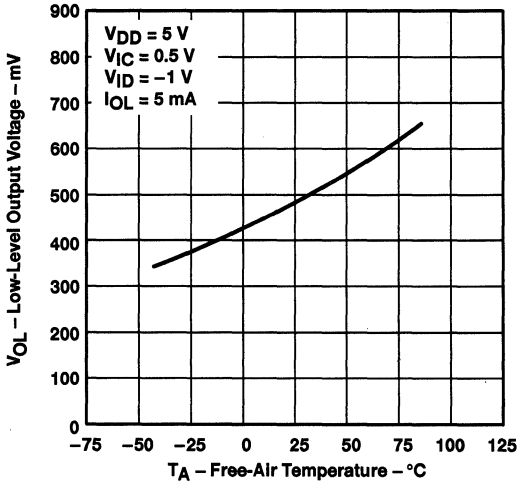


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

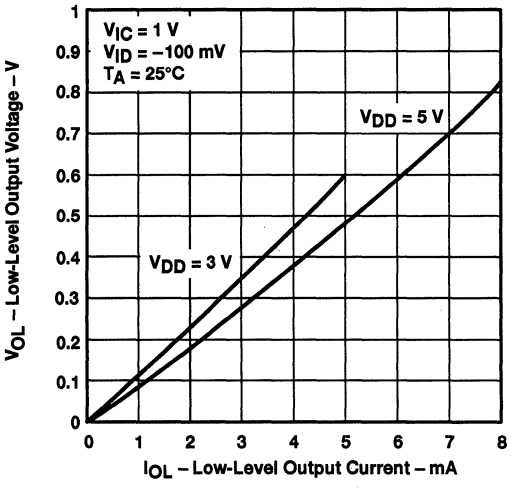


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

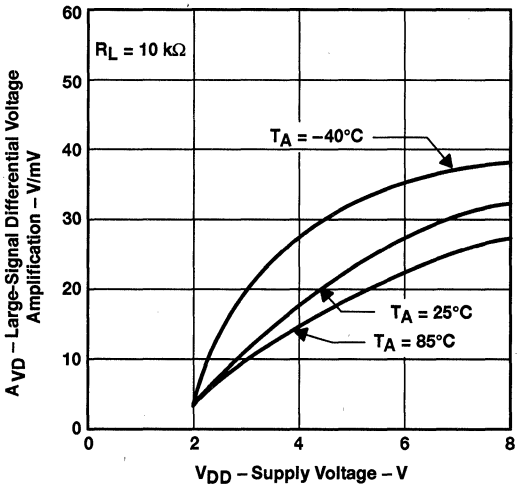


Figure 13

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

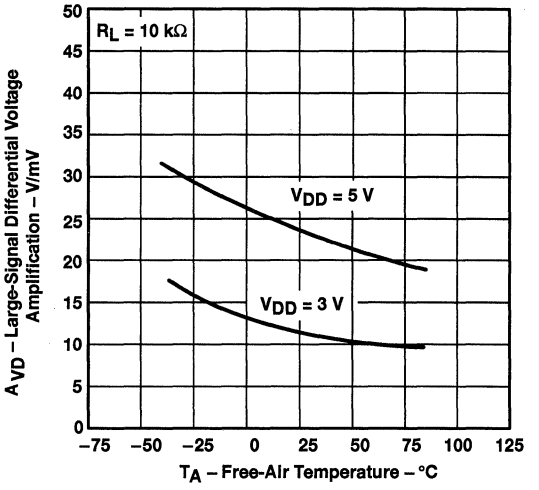
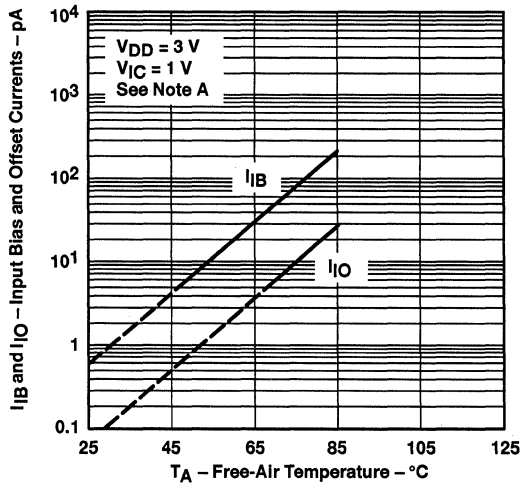


Figure 14

INPUT BIAS CURRENT AND INPUT OFFSET
CURRENT
vs
FREE-AIR TEMPERATURE



NOTE: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 15

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

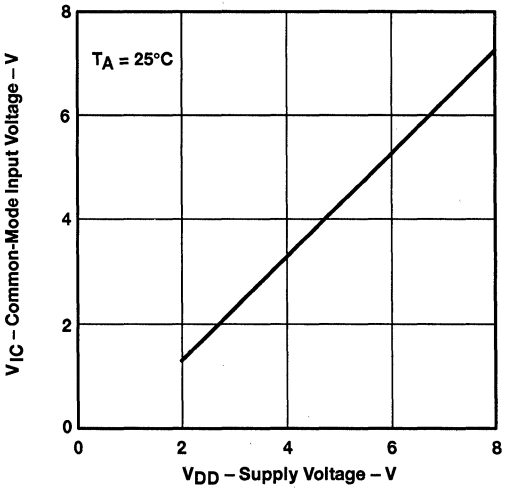


Figure 16

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

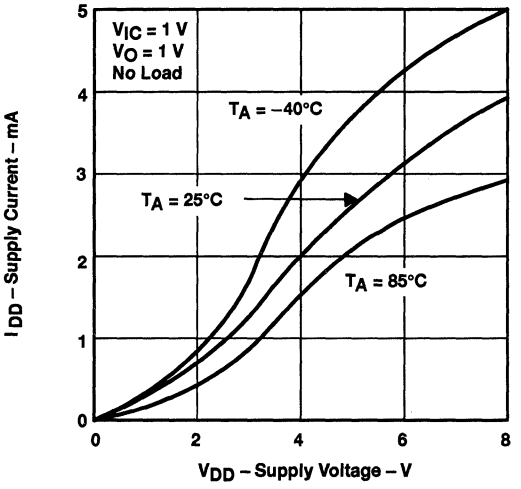


Figure 17

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

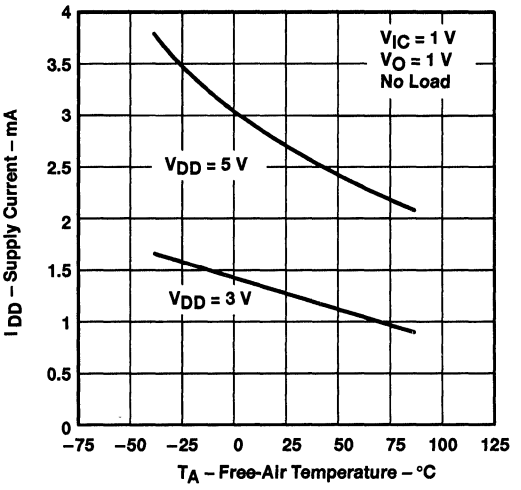


Figure 18

SLEW RATE vs SUPPLY VOLTAGE

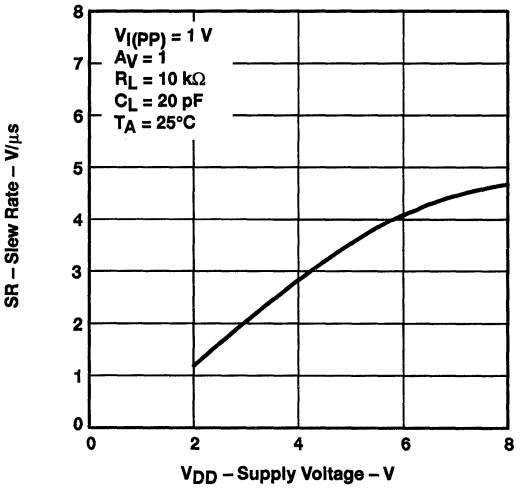


Figure 19

SLEW RATE vs FREE-AIR TEMPERATURE

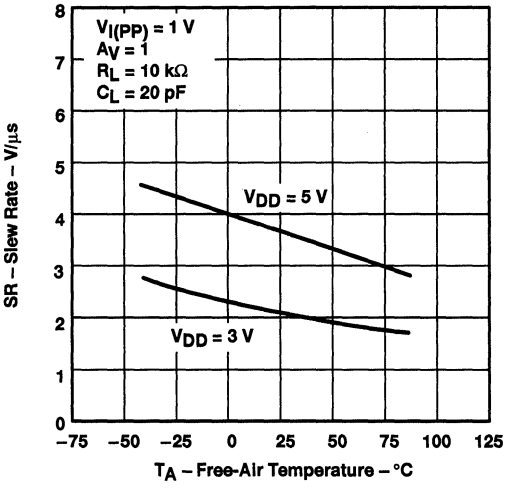


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

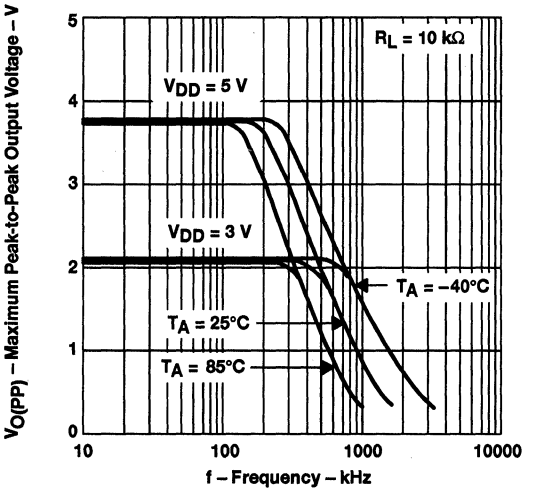


Figure 21

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

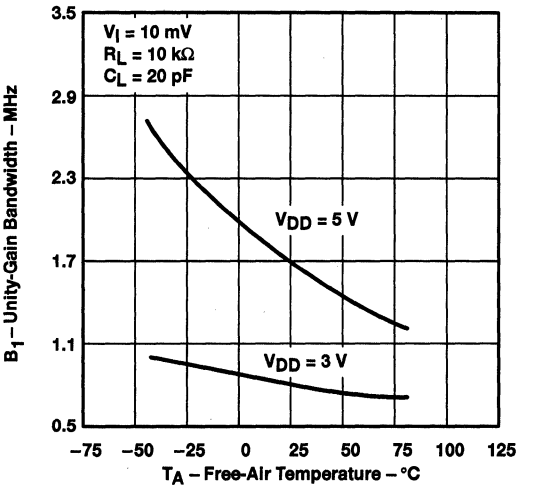


Figure 22

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

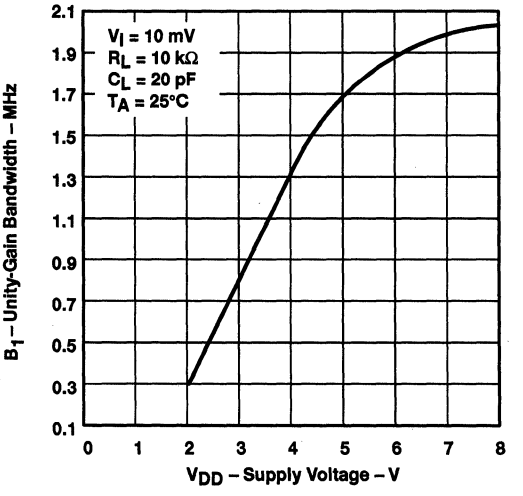


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY

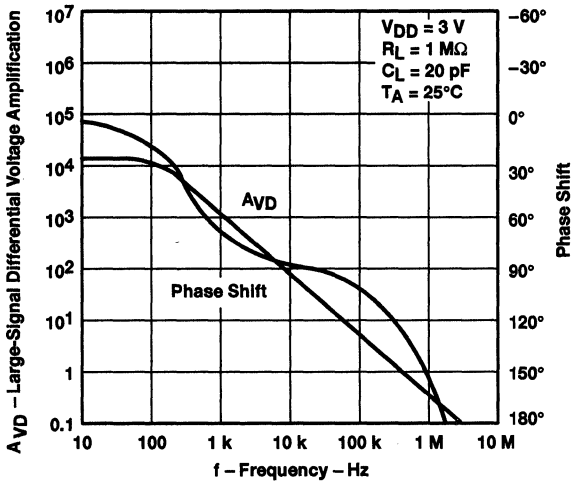


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY

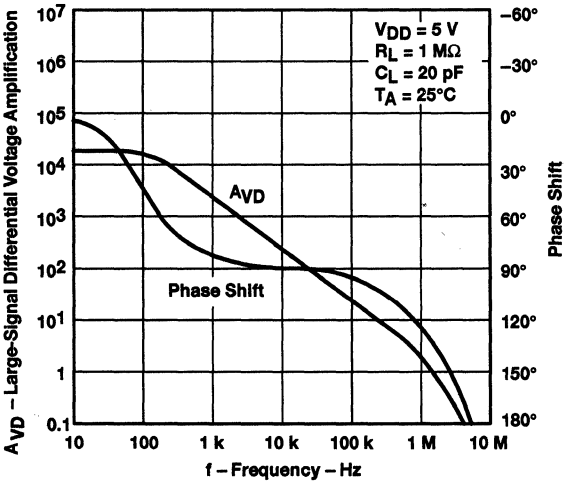


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

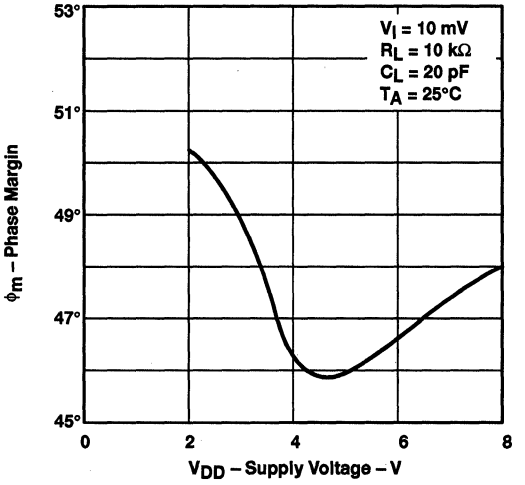


Figure 26

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

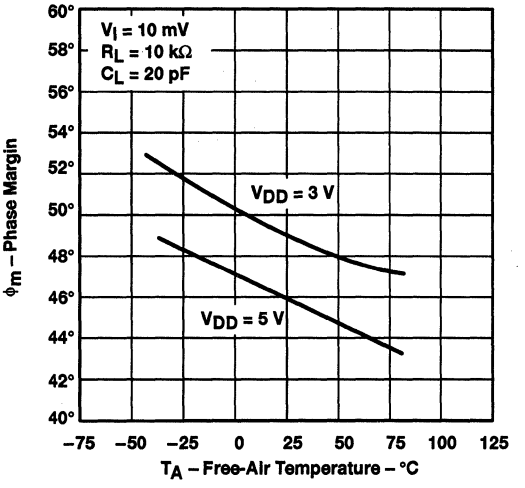


Figure 27

PHASE MARGIN
vs
LOAD CAPACITANCE

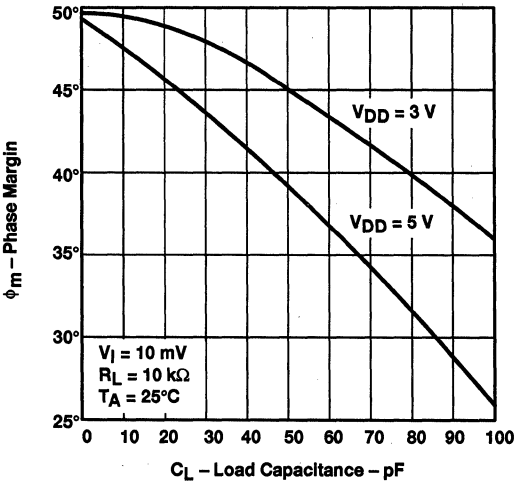


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

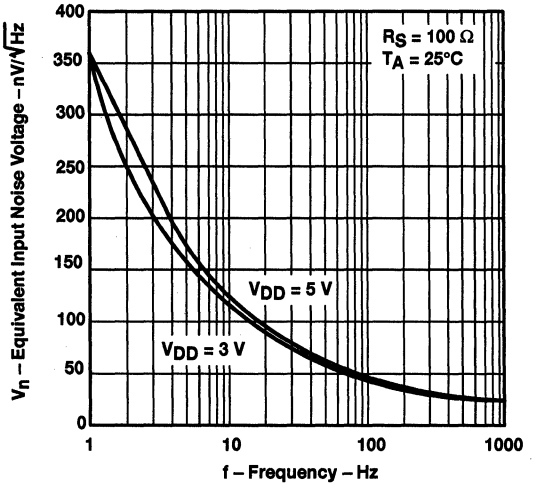


Figure 29

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2344 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.

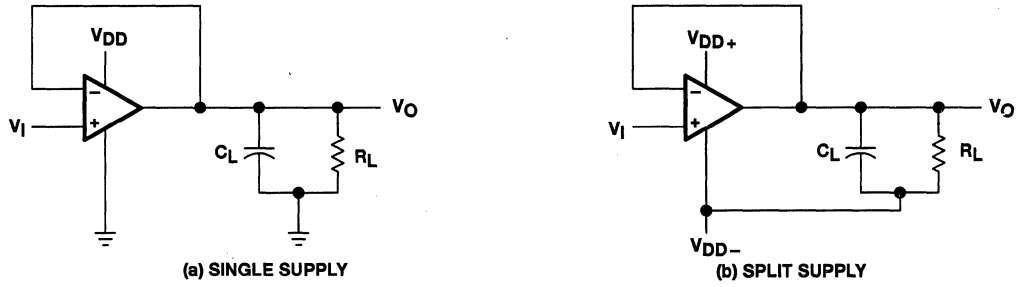


Figure 30. Unity-Gain Amplifier

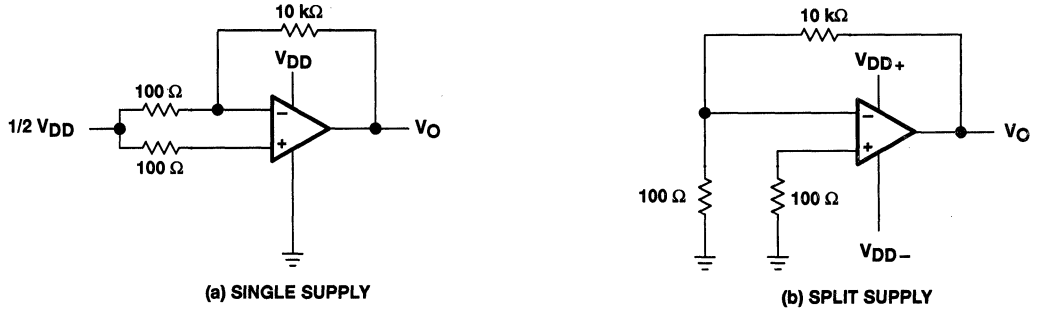


Figure 31. Noise Test Circuit

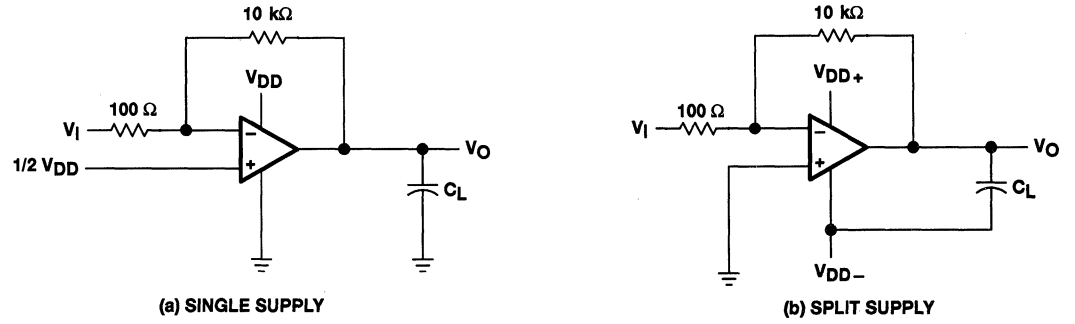


Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2344 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

  Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

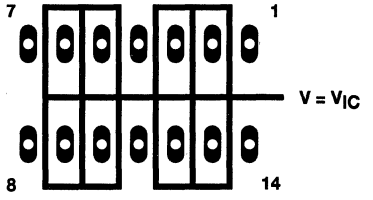


Figure 33. Isolation Metal Around Device Inputs
(N Package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

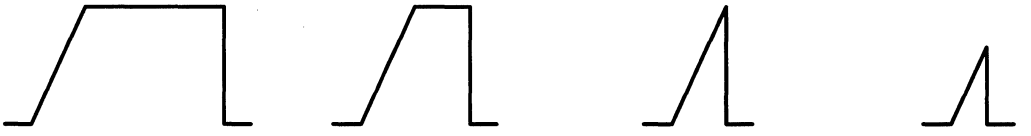


Figure 34. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2344 performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$ while consuming very little power and is suitable for supply voltages of greater than 4 V.

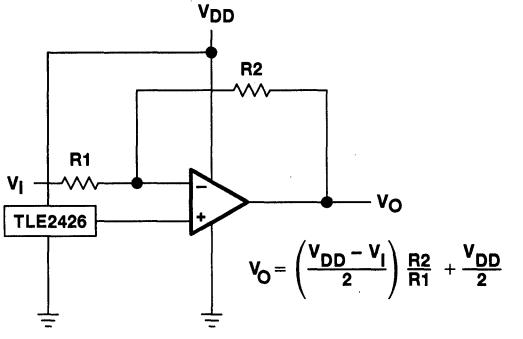


Figure 35. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)

The TLV2344 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

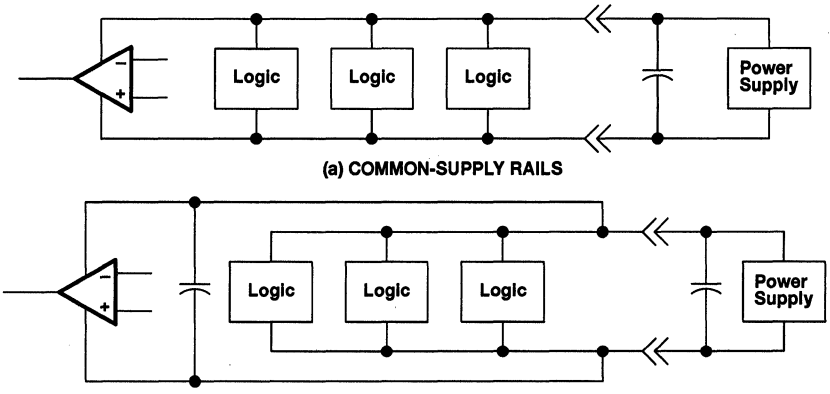


Figure 36. Common Versus Separate Supply Rails

input characteristics

The TLV2344 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.2 V at all other temperatures.

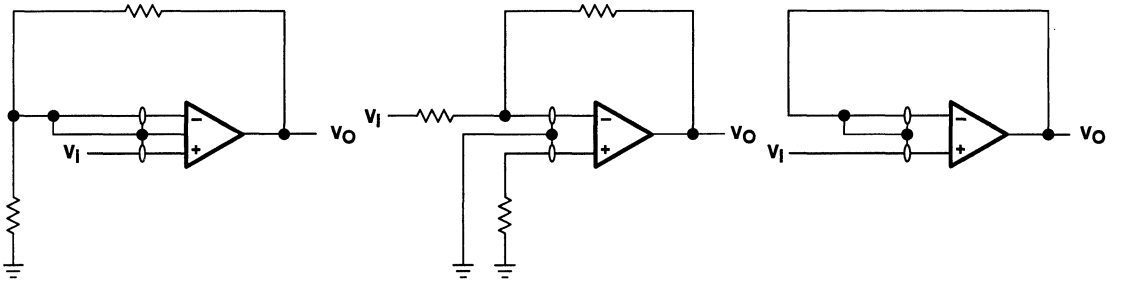
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2344 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2344 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

APPLICATION INFORMATION

input characteristics (continued)



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 37. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2344 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifiers circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

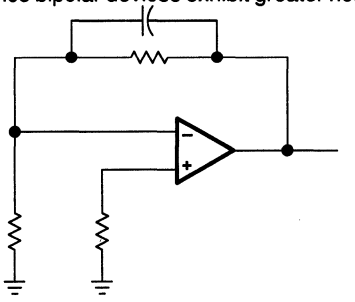


Figure 38. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV2344 incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C. Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2344 inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage

APPLICATION INFORMATION

by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2344 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2344 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

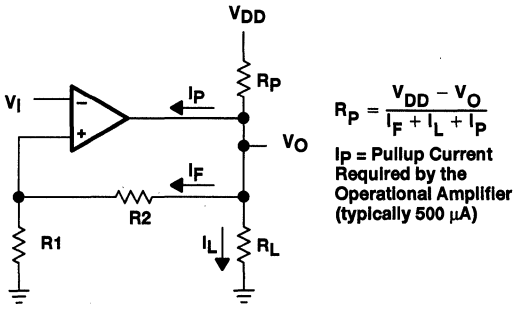


Figure 39. Resistive Pullup to Increase V_{OH}

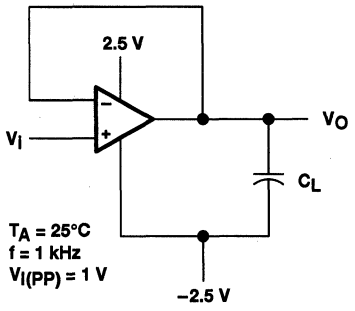
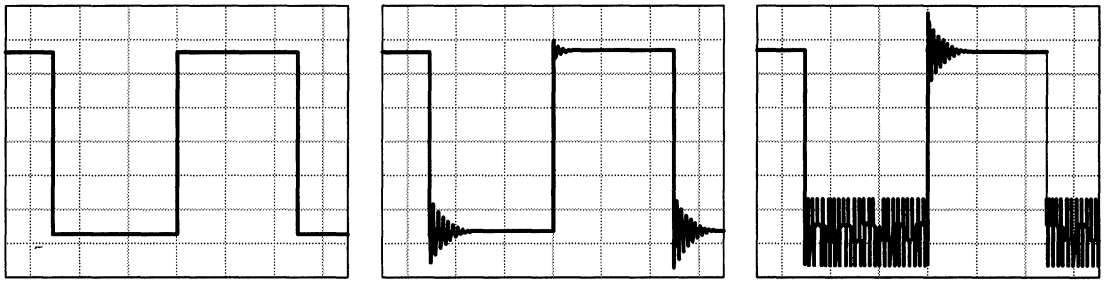


Figure 40. Test Circuit for Output Characteristics

All operating characteristics of the TLV2344 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

TYPICAL APPLICATION DATA

output characteristics (continued)



(a) C_L = 20 pF, R_L = NO LOAD

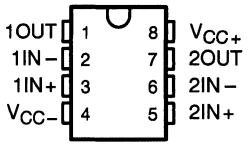
(b) C_L = 130 pF, R_L = NO LOAD

(c) C_L = 150 pF, R_L = NO LOAD

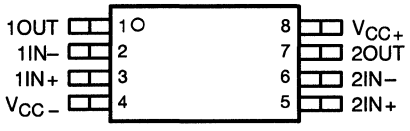
Figure 41. Effect of Capacitive Loads

- **Low Supply Voltage Operation**
  V_{CC} = ± 1 V Min
- **Wide Output Voltage Swing**
  ±2.4 V Typ at $V_{CC±}$ = ±2.5 V, R_L = 10 kΩ
- **Wide Bandwidth**
  7 MHz Typ at $V_{CC±}$ = 2.5 V
- **Low Noise . . . 8 nV/√Hz Typ at f = 1 kHz**
- **High Slew Rate**
  4 V/μsec Typ at $V_{CC±}$ = ±2.5 V
- **Available In Small TSSOP Packages**

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



description

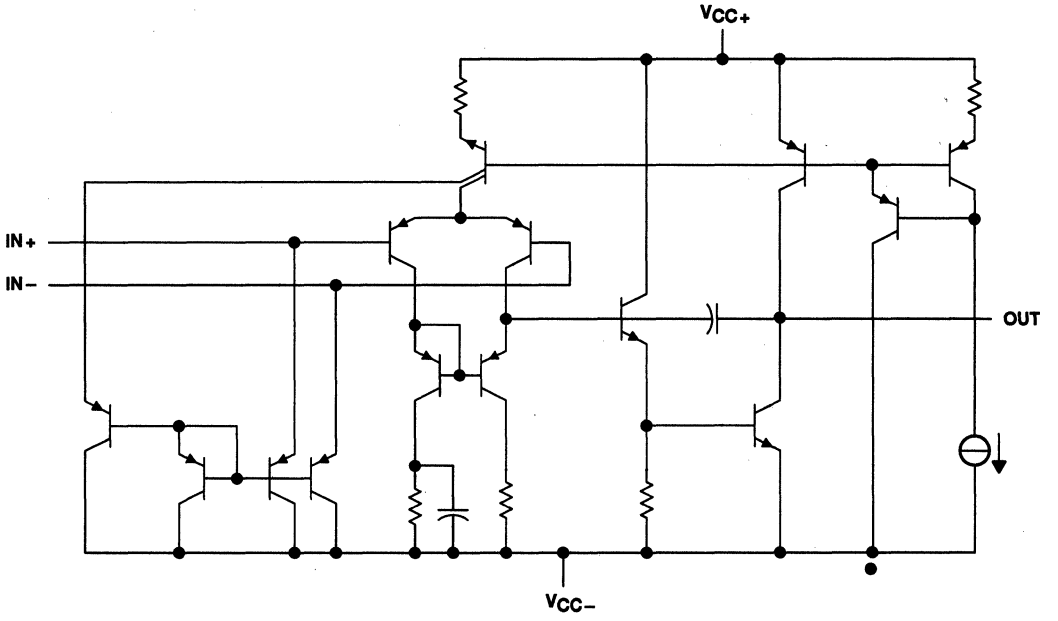
The TLV2362I is a high-performance dual operational amplifier built using an original Texas Instruments bipolar process. This device can be operated at a very low supply voltage (±1 V), while maintaining a wide output swing. The TLV2362I offers a dramatically improved dynamic range of signal conditioning in low-voltage systems. Coupled with this high performance, the TLV2362I provides a wider unity-gain bandwidth and higher slew rate than other general-purpose operational amplifiers. With its low distortion and low noise performance, this device is well suited for audio applications. The TLV2362I is available in the thin-shrink small-outline package (TSSOP) to reduce board space requirements.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–20°C TO 85°C	TLV2362ID	TLV2362IP	TLV2362IPWLE	TLV2362Y

The D packages are available taped and reeled. Add an R to the package suffix (e.g., TLV2362IDR).
The PW packages are only available left-ended taped and reeled, (e.g., TLV2362IPWLE).
Chip forms are specified for operation at 25°C only.

equivalent schematic (each amplifier)

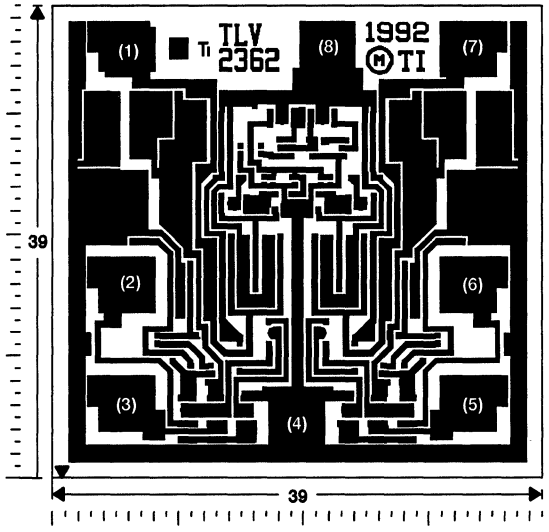


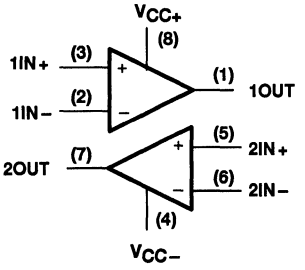
ACTUAL DEVICE COMPONENT COUNT	
Capacitors	4
Diodes	1
Resistors	11
J-FET	1
Transistors	46

TLV2362Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2362I. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) ..... 3.5 V
Supply voltage, V_{CC-} (see Note 1) ..... −3.5 V
Differential input voltage, V_{ID} (see Note 2) ..... ±3.5 V
Input voltage range, V_I (any input) (see Notes 1 and 3) ..... $V_{CC\pm}$
Output voltage, V_O ..... ±3.5 V
Output current, I_O ..... 20 mA
Duration of short-circuit current at (or below) 25°C (output shorted to GND) ..... unlimited
Continuous total dissipation, P_D ($T_A \leq 25°C$) ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −20°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package ..... 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. All input voltage values must not exceed V_{CC}.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	±1	±2.5	V
Operating free-air temperature, T_A	−20	85	°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A \leq 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

electrical characteristics, $V_{CC\pm}$ = ±1.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLV2362I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0,	V_{IC} = 0	25°C		1	6	mV
				–20°C to 85°C			7.5	
I_{IO}	Input offset current	V_O = 0,	V_{IC} = 0	25°C		5	100	nA
				–20°C to 85°C			150	
I_{IB}	Input bias current	V_O = 0,	V_{IC} = 0	25°C		20	150	nA
				–20°C to 85°C			250	
V_{ICR}	Common-mode input voltage	$\lvert V_{IO}\rvert \le$ 7.5 mV		25 °C	±0.5			V
				–20°C to 85°C	±0.5			
V_{OM+}	Maximum positive-peak output voltage	R_L = 10 kΩ		25°C	1.2	1.4		V
		$R_L \ge$ 10 kΩ		–20°C to 85°C	1.2			
V_{OM-}	Maximum negative-peak output voltage	R_L = 10 kΩ		25°C	–1.2	–1.4		V
		$R_L \ge$ 10 kΩ		–20°C to 85°C	–1.2			
I_{CC}	Supply current (both amplifiers)	V_O = 0,	No load	25°C		2.8	4.5	mA
				–20°C to 85°C			5.5	
A_{VD}	Large-signal differential voltage amplification	V_O = ± 1 V,	R_L = 10 kΩ	25°C		55		dB
CMRR	Common-mode rejection ratio	V_{IC} = ± 0.5 V		25°C		75		dB
k_{SVR}	Supply-voltage rejection ratio	$V_{CC\pm}$ = ± 1.5 V to ± 2.5 V		25°C		80		dB

operating characteristics, $V_{CC\pm}$ = ±1.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			TLV2362I			UNIT
					MIN	TYP	MAX	
SR	Slew rate	A_V = 1,	V_I = ±0.5 V			2.5		V/μs
B_1	Unity-gain bandwidth	A_V = 40,	R_L = 10 kΩ,	C_L = 100 pF		6		MHz
V_n	Equivalent input noise voltage	R_S = 20 Ω,	R_F = 2 kΩ,	f = 1 kHz		9		nV/√Hz

electrical characteristics, $V_{CC\pm}$ = ±2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLV2362I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0,	V_{IC} = 0	25°C		1	6	mV
				–20°C to 85°C			7.5	
I_{IO}	Input offset current	V_O = 0,	V_{IC} = 0	25°C		5	100	nA
				–20°C to 85°C			150	
I_{IB}	Input bias current	V_O = 0,	V_{IC} = 0	25°C		20	150	nA
				–20°C to 85°C			250	
V_{ICR}	Common-mode input voltage	$\lvert V_{IO}\rvert \le$ 7.5 mV		25 °C	±1.5			V
				–20°C to 85°C	±1.4			
V_{OM+}	Maximum positive-peak output voltage	R_L = 10 kΩ		25°C	2	2.4		V
		$R_L \ge$ 10 kΩ		–20°C to 85°C	2			
V_{OM-}	Maximum negative-peak output voltage	R_L = 10 kΩ		25°C	–2	–2.4		V
		$R_L \ge$ 10 kΩ		–20°C to 85°C	–2			
I_{CC}	Supply current (both amplifiers)	V_O = 0,	No load	25°C		3.5	5	mA
				–20°C to 85°C			6	
A_{VD}	Large-signal differential voltage amplification	V_O = ± 1 V,	R_L = 10 kΩ	25°C		60		dB
CMRR	Common-mode rejection ratio	V_{IC} = ± 0.5 V		25°C		85		dB
k_{SVR}	Supply-voltage rejection ratio	$V_{CC\pm}$ = ± 1.5 V to ± 2.5 V		25°C		80		dB

operating characteristics, $V_{CC\pm}$ = ±2.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			TLV2362I			UNIT
					MIN	TYP	MAX	
SR	Slew rate	A_V = 1,	V_I = ±0.5 V			3		V/μs
B_1	Unity-gain bandwidth	A_V = 40,	R_L = 10 kΩ,	C_L = 100 pF		7		MHz
V_n	Equivalent input noise voltage	R_S = 20 Ω,	R_F = 2 kΩ,	f = 1 kHz		8		nV/√Hz

electrical characteristics, $V_{CC\pm}$ = ±1.5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLV2362Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0		1	6	mV
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0		5	100	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0		20	150	nA
V_{ICR}	Common-mode input voltage	$\lvert V_{IO}\rvert \le$ 7.5 mV	±0.5			V
V_{OM+}	Maximum positive-peak output voltage	R_L = 10 kΩ	1.2	1.4		V
V_{OM-}	Maximum negative-peak output voltage	R_L = 10 kΩ	–1.2	–1.4		
I_{CC}	Supply current (both amplifiers)	V_O = 0, No load		2.8	4.5	mA
A_{VD}	Large-signal differential voltage amplification	V_O = ± 1 V, R_L = 10 kΩ		55		dB
CMRR	Common-mode rejection ratio	V_{IC} = ± 0.5 V		75		dB
k_{SVR}	Supply-voltage rejection ratio	$V_{CC\pm}$ = ± 1.5 V to ± 2.5 V		80		dB

operating characteristics, $V_{CC\pm}$ = ±1.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2362Y			UNIT
			MIN	TYP	MAX	
SR	Slew rate	A_V = 1, V_I = ±0.5 V		2.5		V/μs
B_1	Unity-gain bandwidth	A_V = 40, R_L = 10 kΩ, C_L = 100 pF		6		MHz
V_n	Equivalent input noise voltage	R_S = 20 Ω, R_F = 2 kΩ, f = 1 kHz		9		nV/√Hz

electrical characteristics, $V_{CC\pm}$ = ±2.5 V, T_A = 25°C (unless otherwise noted)

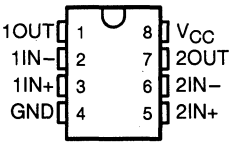
PARAMETER		TEST CONDITIONS	TLV2362Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0		1	6	mV
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0		5	100	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0		20	150	nA
V_{ICR}	Common-mode input voltage	$\lvert V_{IO}\rvert \le$ 7.5 mV	±1.5			V
V_{OM+}	Maximum positive-peak output voltage	R_L = 10 kΩ	2	2.4		V
V_{OM-}	Maximum negative-peak output voltage	R_L = 10 kΩ	–2	–2.4		
I_{CC}	Supply current (both amplifiers)	V_O = 0, No load		3.5	5	mA
A_{VD}	Large-signal differential voltage amplification	V_O = ± 1 V, R_L = 10 kΩ		60		dB
CMRR	Common-mode rejection ratio	V_{IC} = ± 0.5 V		85		dB
k_{SVR}	Supply-voltage rejection ratio	$V_{CC\pm}$ = ± 1.5 V to ± 2.5 V		80		dB

operating characteristics, $V_{CC\pm}$ = ±2.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2362Y			UNIT
			MIN	TYP	MAX	
SR	Slew rate	A_V = 1, V_I = ±0.5 V		3		V/μs
B_1	Unity-gain bandwidth	A_V = 40, R_L = 10 kΩ, C_L = 100 pF		7		MHz
V_n	Equivalent input noise voltage	R_S = 20 Ω, R_F = 2 kΩ, f = 1 kHz		8		nV/√Hz

- **Low-Voltage and Single-Supply Operation V_{CC} = 2 V to 7 V**
- **Common-Mode Voltage Range That Includes Ground**
- **Fast Response Time 450 ns Typ (TLV2393)**
- **Low Supply Current 0.7 mA Typ (TLV1393)**
- **Specified Fully at 3-V and 5-V Supply Voltages**

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)

description

The TLV1393 and the TLV2393 are dual differential comparators built using a new Texas Instruments developed low-voltage, high-speed bipolar process. These devices have been specifically developed for low-voltage, single-supply applications. Their enhanced performance makes them excellent replacements for the LM393 in today's improved 3-V and 5-V system designs.

The TLV1393, with its typical supply current of only 0.16 mA, is ideal for low-power systems. Response time has also been improved to 0.7 µs. For higher-speed applications, the TLV2393 features excellent ac performance with a response time of just 0.45 µs, three times that of the LM393.

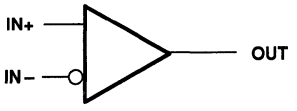
Package availability for these devices includes the TSSOP (thin-shrink small-outline package). With a maximum thickness of 1.1 mm and a package area that is 25% smaller than the standard surface-mount package, the TSSOP is ideal for high-density circuits, particularly in hand-held and portable equipment.

AVAILABLE OPTIONS

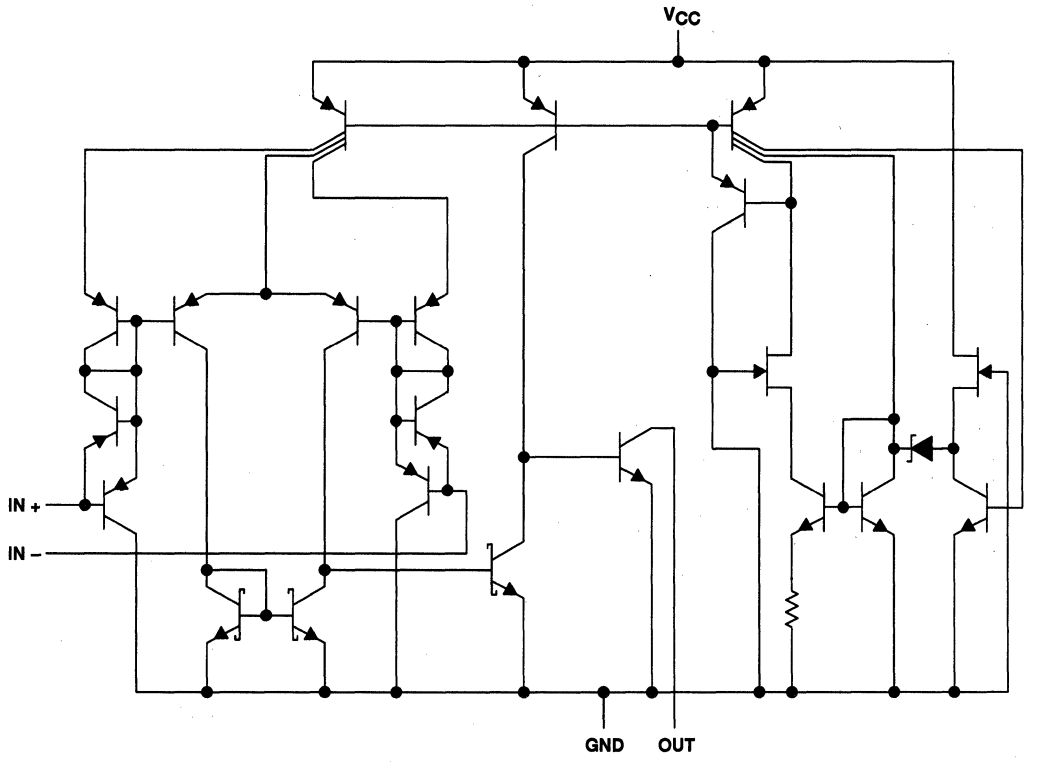
PACKAGED DEVICES						CHIP FORM (Y)
T_A	SUPPLY CURRENT (TYP)	RESPONSE TIME (TYP)	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 105°C	0.16 mA	0.7 µs	TLV1393ID	TLV1393IP	TL1393IPWLE	TLV1393Y
	1.1 mA	0.45 µs	TLV2393ID	TLV2393IP	TLV2393IPWLE	TLV2393Y

PW packages are only available left-ended taped and reeled, (e.g., TLV1393IPWLE).

symbol (each comparator)

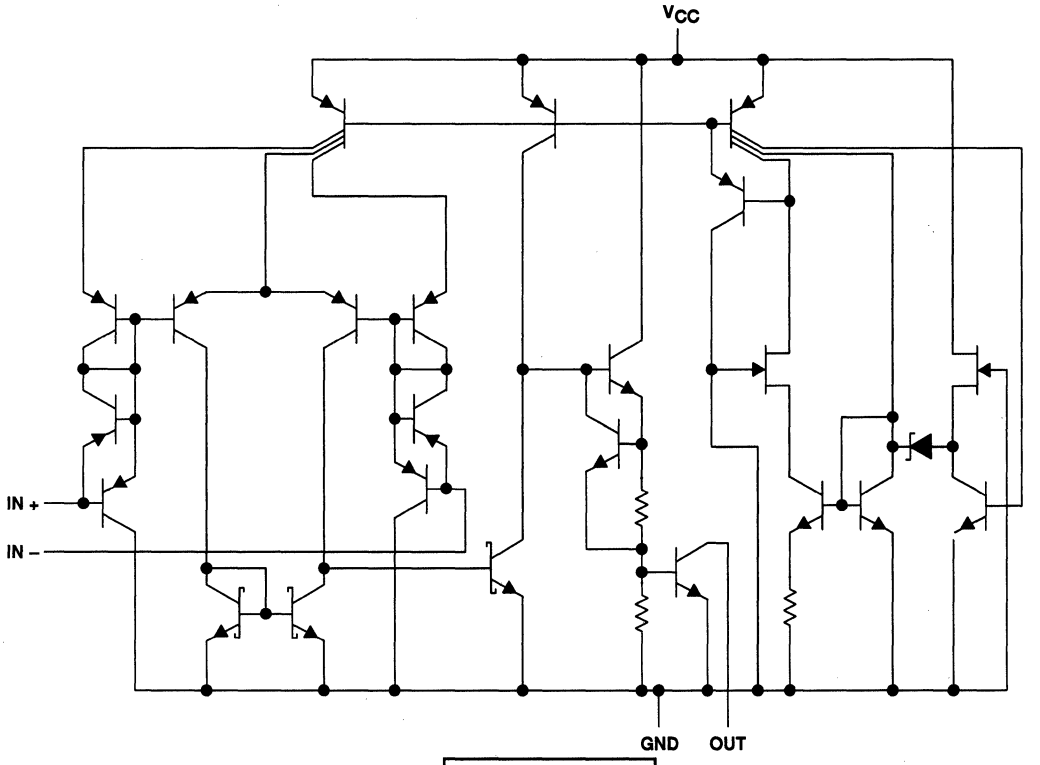


TLV1393, TLV1393Y equivalent schematic (each comparator)



COMPONENT COUNT	
Transistors	44
Resistors	1
Diodes	7
Epi-FET	2

TLV2393, TLV2393Y equivalent schematic (each comparator)

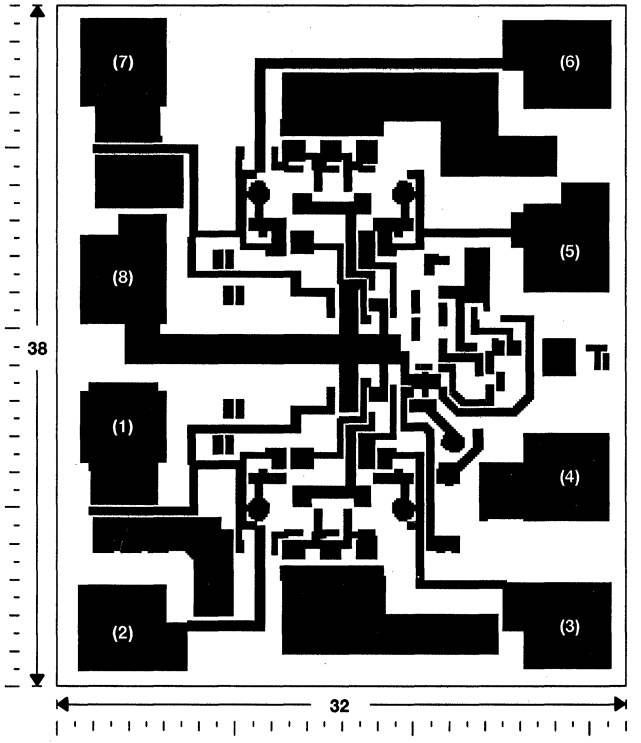


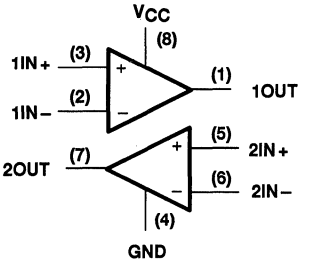
COMPONENT COUNT	
Transistors	44
Resistors	1
Diodes	7
Epi-FET	2

TLV1393Y chip information

These chips, when properly assembled, display characteristics similar to the TLV1393. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 13 TYPICAL

BONDING PADS: 3.54 × 3.54 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

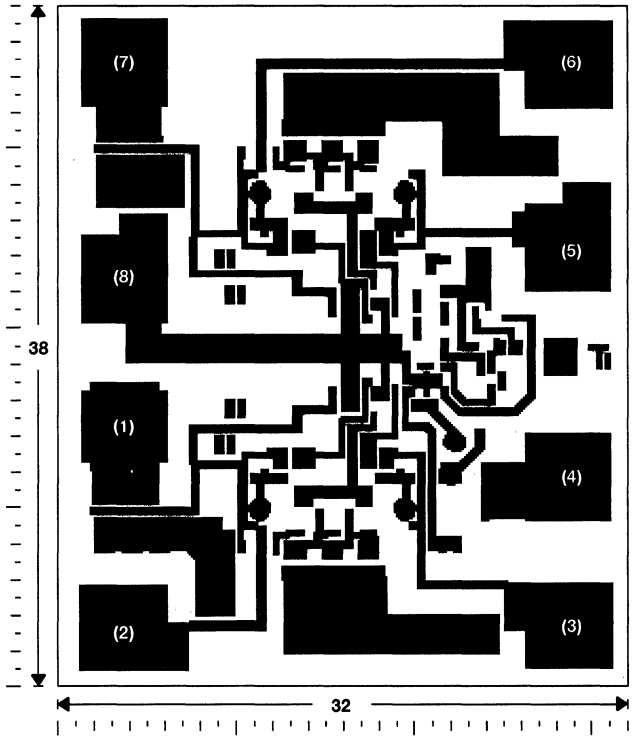
ALL DIMENSIONS ARE IN MILS.

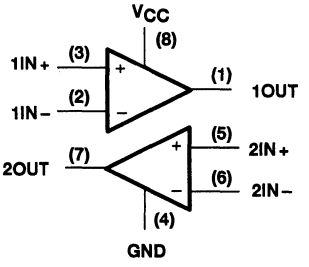
PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

TYLV2393Y chip information

These chips, when properly assembled, display characteristics similar to the TLV2393. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 3.6 × 3.6 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Differential input voltage, V_{ID} (see Note 2) ..... 7 V
Input voltage, V_I (any input) ..... 7 V
Output voltage, V_O ..... 7 V
Output current, I_O (each output) ..... 20 mA
Duration of short-circuit current to GND (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... –40°C to 105°C
Storage temperature range ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network GND.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. Short circuits from the outputs to V_{CC} can cause excessive heating and eventual destruction of the chip.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	2	7	V
Operating free-air temperature, T_A	–40	105	°C

electrical characteristics, V_{CC} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV1393			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V,	$V_{IC} = V_{ICR}$min	25°C		1.5	5	mV
				Full range		120	9	
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{CC} – 1.5	0 to V_{CC} –1.2		V
				Full range	0 to V_{CC} –2			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OL} = 500 µA	Full range		120	300	mV
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50	nA
				Full range			150	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–40	–250	nA
				Full range			–400	
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 3 V	25°C		0.1		nA
		V_{ID} = 1 V,	V_{OH} = 5 V	Full range			100	
I_{OL}	low-level output current	V_{ID} = –1 V,	V_{OL} = 1.5 V	25°C	500			µA
I_{CCH}	High-level supply current	$V_O = V_{OH}$		25°C		160	250	µA
				Full range			300	
I_{CCL}	Low-level supply current	$V_O = V_{OL}$		25°C		160	250	
				Full range			300	

† Full range is –40°C to 105°C.

switching characteristics, V_{CC} = 3 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV1393			UNIT
		MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive, R_L connected to 5 V through 5.1 kΩ		0.7		µs

electrical characteristics, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV1393			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V,	$V_{IC} = V_{ICR}$min	25°C		1.5	5	mV
				Full range			9	
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{CC} – 1.5	0 to V_{CC} – 1.2		V
				Full range	0 to V_{CC} – 2			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OL} = 500 µA	Full range		120	300	mV
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50	nA
				Full range			150	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–40	–250	nA
				Full range			–400	
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 3 V	25°C		0.1		nA
		V_{ID} = 1 V,	V_{OH} = 5 V	Full range			100	
I_{OL}	Low-level output current	V_{ID} = –1 V,	V_{OL} = 1.5 V	25°C	600			µA
I_{CCH}	High-level supply current	$V_O = V_{OH}$		25°C		200	300	µA
				Full range			350	
I_{CCL}	Low-level supply current	$V_O = V_{OL}$		25°C		200	300	
				Full range			350	

† Full range is –40°C to 105°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLV1393			UNIT
			MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive,	R_L connected to 5 V through 5.1 kΩ		0.65		µs
	TTL-level input step,	R_L connected to 5 V through 5.1 kΩ		0.18		

electrical characteristics, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLV1393Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = V_{ICR}min		1.5	5	mV
V_{ICR}	Common-mode input voltage range		0 to V_{CC} – 1.5	0 to V_{CC} – 1.2		V
I_{IO}	Input offset current	V_O = 1.4 V		5	50	nA
I_{IB}	Input bias current	V_O = 1.4 V		–40	–250	nA
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 3 V		0.1		nA
I_{OL}	low-level output current	V_{ID} = –1 V, V_{OL} = 1.5 V	500			µA
I_{CCH}	High-level supply current	V_O = V_{OH}		160	250	µA
I_{CCL}	Low-level supply current	V_O = V_{OL}		160	250	

switching characteristics, V_{CC} = 3 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV1393Y			UNIT
		MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive, R_L connected to 5 V through 5.1 kΩ		0.7		µs

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLV1393Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = V_{ICR}min		1.5	5	mV
V_{ICR}	Common-mode input voltage range		0 to V_{CC} – 1.5	0 to V_{CC} – 1.2		V
I_{IO}	Input offset current	V_O = 1.4 V		5	50	nA
I_{IB}	Input bias current	V_O = 1.4 V		–40	–250	nA
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 3 V		0.1		nA
I_{OL}	Low-level output current	V_{ID} = –1 V, V_{OL} = 1.5 V	600			µA
I_{CCH}	High-level supply current	V_O = V_{OH}		200	300	µA
I_{CCL}	Low-level supply current	V_O = V_{OL}		200	300	

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV1393Y			UNIT
		MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive, R_L connected to 5 V through 5.1 kΩ		0.65		µs
	TTL-level input step, R_L connected to 5 V through 5.1 kΩ		0.18		

electrical characteristics, V_{CC} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2393			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V,	$V_{IC} = V_{ICR}$min	25°C		1.5	5	mV
				Full range			9	
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{CC} – 1.5	0 to V_{CC} – 1.2		V
				Full range	0 to V_{CC} – 2			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OL} = 1 mA	25°C		80	300	mV
		V_{ID} = –1 V,	I_{OL} = 4 mA	Full range		250	700	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50	nA
				Full range			150	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–100	–250	nA
				Full range			–400	
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 3 V	25°C		0.1		nA
		V_{ID} = 1 V,	V_{OH} = 5 V	Full range			100	
I_{OL}	low-level output current	V_{ID} = –1 V,	V_{OL} = 1.5 V	25°C	4			mA
I_{CCH}	High-level supply current	$V_O = V_{OH}$		25°C		450	600	µA
				Full range			700	
I_{CCL}	Low-level supply current	$V_O = V_{OL}$		25°C		1.1	1.3	mA
				Full range			1.4	

† Full range is –40°C to 105°C.

switching characteristics, V_{CC} = 3 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV2393			UNIT
		MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive, R_L connected to 5 V through 5.1 kΩ		0.45	1	µs

electrical characteristics, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2393			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V,	$V_{IC} = V_{ICR}$min	25°C		1.5	5	mV
				Full range			9	
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{CC} – 1.5	0 to V_{CC} – 1.2		V
				Full range	0 to V_{CC} –2			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OL} = 1 mA	25°C		70	300	mV
		V_{ID} = –1 V,	I_{OL} = 4 mA	Full range		200	700	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50	nA
				Full range			150	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–100	–250	nA
				Full range			–400	
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 3 V	25°C		0.1		nA
		V_{ID} = 1 V,	V_{OH} = 5 V	Full range			100	
I_{OL}	low-level output current	V_{ID} = –1 V,	V_{OL} = 1.5 V	25°C	6			mA
I_{CCH}	High-level supply current	$V_O = V_{OH}$		25°C		550	700	µA
				Full range			800	
I_{CCL}	Low-level supply current	$V_O = V_{OL}$		25°C		1.2	1.5	mA
				Full range			1.6	

† Full range is –40°C to 105°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLV2393			UNIT
			MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive,	R_L connected to 5 V through 5.1 kΩ		0.4	0.8	µs
	TTL-level input step,	R_L connected to 5 V through 5.1 kΩ		0.15	0.3	

electrical characteristics, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLV2393Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = V_{ICR}min		1.5	5	mV
V_{ICR}	Common-mode input voltage range		0 to V_{CC} – 1.5	0 to V_{CC} – 1.2		V
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{OL} = 1 mA		80	300	mV
I_{IO}	Input offset current	V_O = 1.4 V		5	50	nA
I_{IB}	Input bias current	V_O = 1.4 V		–100	–250	nA
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 3 V		0.1		nA
I_{OL}	low-level output current	V_{ID} = –1 V, V_{OL} = 1.5 V	4			mA
I_{CCH}	High-level supply current	V_O = V_{OH}		450	600	µA
I_{CCL}	Low-level supply current	V_O = V_{OL}		1.1	1.3	mA

switching characteristics, V_{CC} = 3 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV2393Y			UNIT
		MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive, R_L connected to 5 V through 5.1 kΩ		0.45	1	µs

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLV2393Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = V_{ICR}min		1.5	5	mV
V_{ICR}	Common-mode input voltage range		0 to V_{CC} – 1.5	0 to V_{CC} – 1.2		V
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{OL} = 1 mA		70	300	mV
I_{IO}	Input offset current	V_O = 1.4 V		5	50	nA
I_{IB}	Input bias current	V_O = 1.4 V		–100	–250	nA
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 3 V		0.1		nA
I_{OL}	low-level output current	V_{ID} = –1 V, V_{OL} = 1.5 V	6			mA
I_{CCH}	High-level supply current	V_O = V_{OH}		550	700	µA
I_{CCL}	Low-level supply current	V_O = V_{OL}		1.2	1.5	mA

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV2393Y			UNIT
		MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive, R_L connected to 5 V through 5.1 kΩ		0.4	0.8	µs
	TTL-level input step, R_L connected to 5 V through 5.1 kΩ		0.15	0.3	

TYPICAL CHARACTERISTICS

LOW-TO HIGH-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

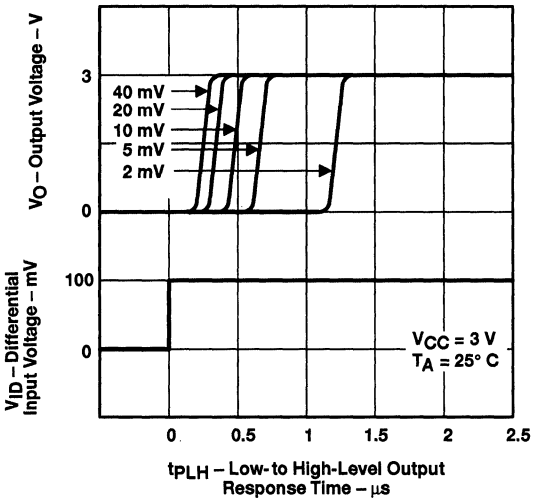


Figure 1

HIGH-TO LOW-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

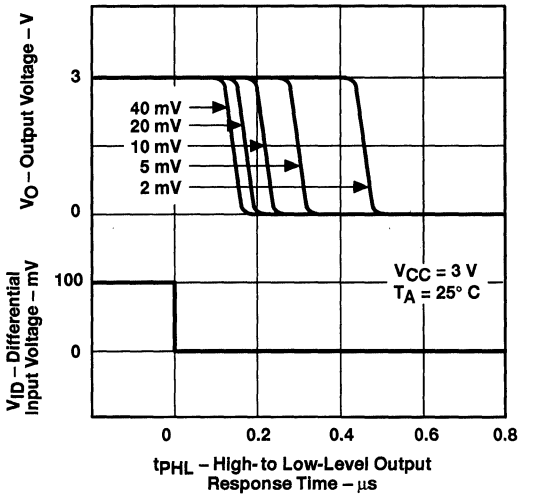


Figure 2

LOW-TO HIGH-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

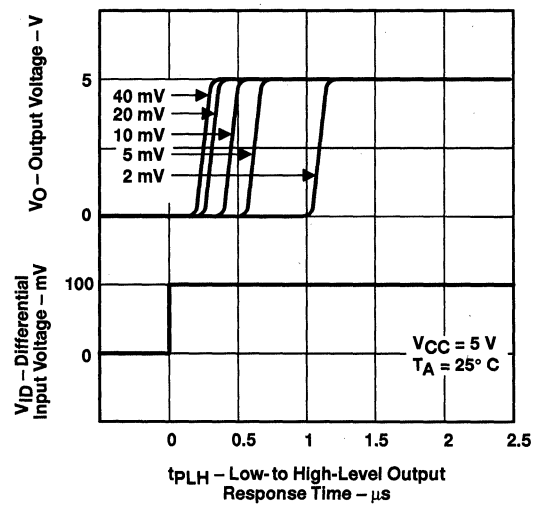


Figure 3

HIGH-TO LOW-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

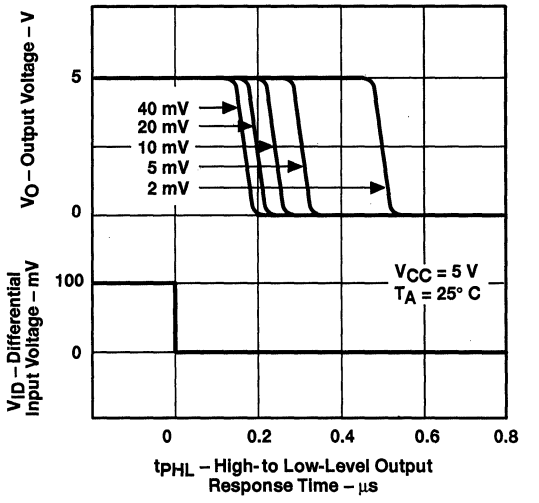


Figure 4

TYPICAL CHARACTERISTICS

LOW-TO HIGH-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

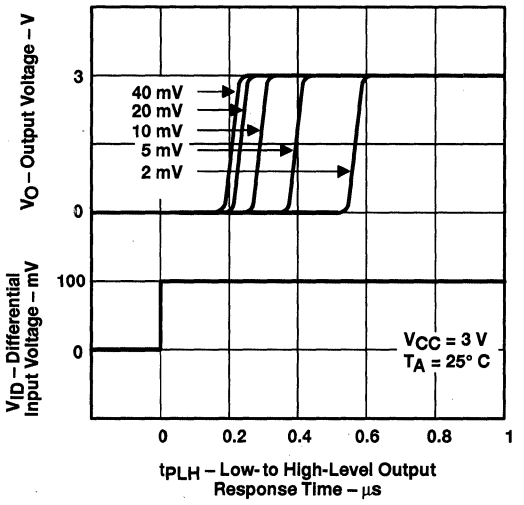


Figure 5

HIGH-TO LOW-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

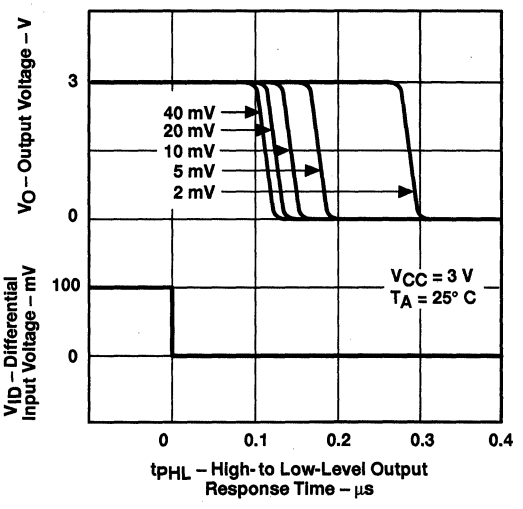


Figure 6

LOW-TO HIGH-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

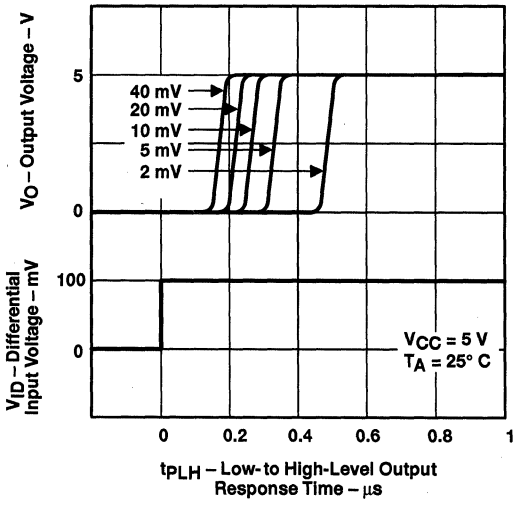


Figure 7

HIGH-TO LOW-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

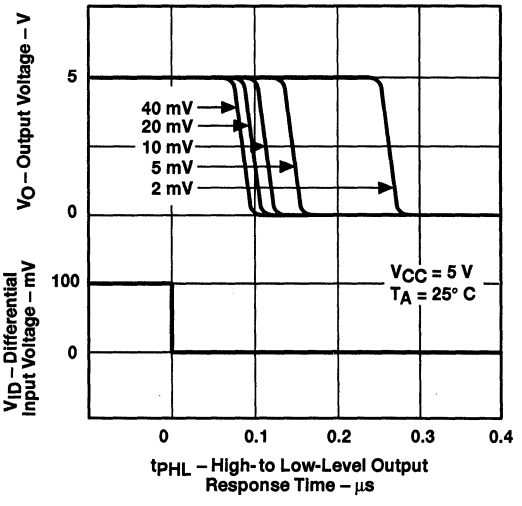


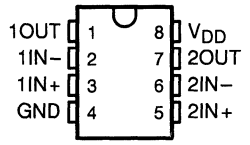
Figure 8

LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

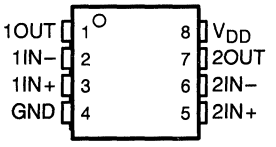
SLCS011 – MAY 1992

- **Wide Range of Supply Voltages 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Very-Low Supply-Current Drain 120 μA Typ at 3 V**
- **Output Compatible With TTL, MOS, and CMOS**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Common-Mode Input Voltage Range Includes Ground**
- **Built-In ESD Protection**

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)

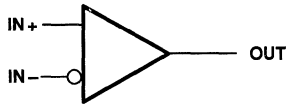


NC — No internal connection

description

The TLV2352 consists of two independent, low-power comparators specifically designed for single power-supply applications and to operate with power-supply rails as low as 2 V. When powered from a 3-V supply, the typical supply current is only 120 μA.

symbol (each comparator)



The TLV2352 is designed using the Texas Instruments LinCMOS™ technology and therefore features an extremely high input impedance (typically greater than 10^{12} Ω), which allows direct interfacing with high-impedance sources. The outputs are N-channel open-drain configurations that require an external pullup resistor to provide a positive output voltage swing, and they can be connected to achieve positive-logic wired-AND relationships. The TLV2352 is fully characterized at 3 V and 5 V for operation from – 40°C to 85°C.

The TLV2352 has internal electrostatic-discharge (ESD)-protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

AVAILABLE OPTIONS

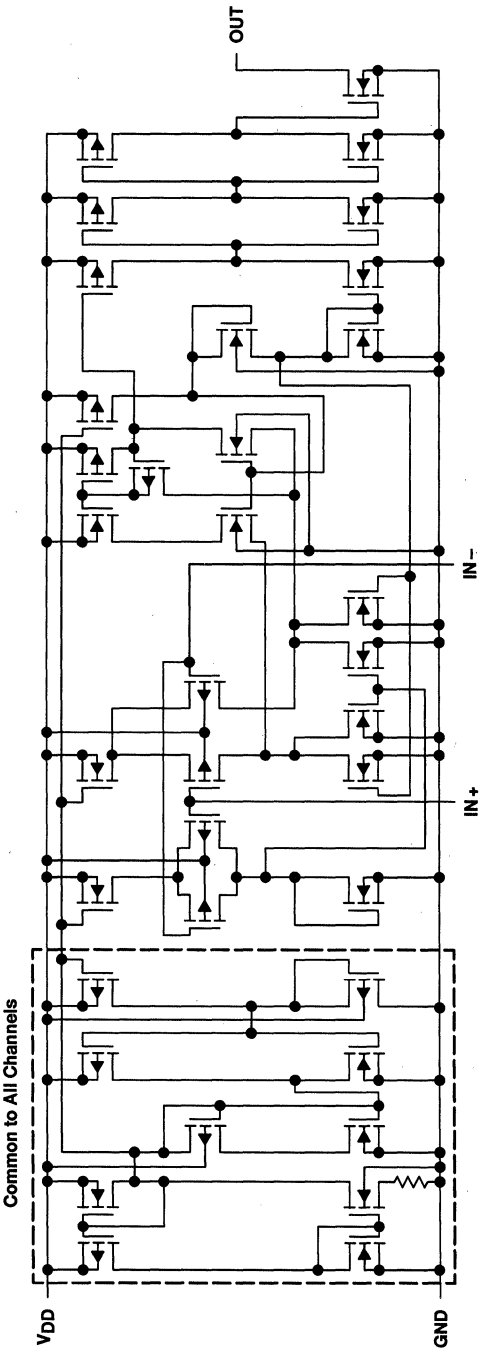
T_A	V_{IO}max at 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 85°C	5 mV	TLV2352ID	TLV2352IP	TLV2352IPWLE	TLV2352Y

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLV2352IDR).
PW packages are only available left-ended taped and reeled, (e.g., TLV2352IPWLE)

Caution. These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

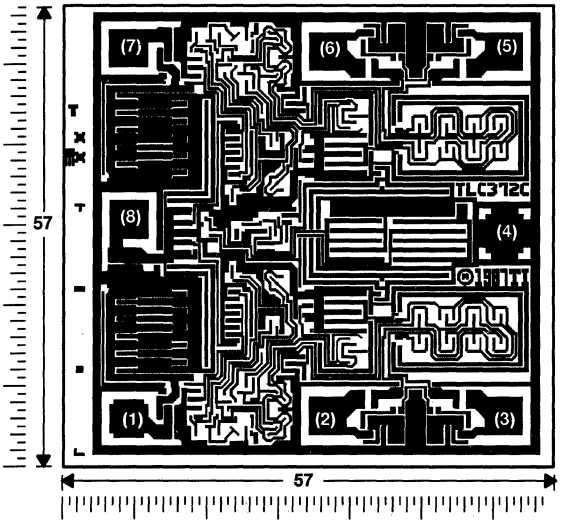
TLV2352I equivalent schematic

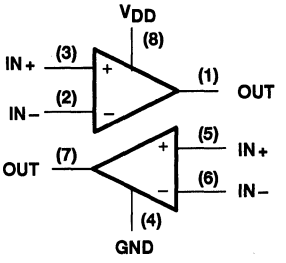


TLV2352Y chip information

These chips, when properly assembled, display characteristics similar to the TLV2352. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... ±8 V
Input voltage range, V_I ..... −0.3 to 8 V
Output voltage, V_O ..... 8 V
Input current, I_I ..... ±5 mA
Output current, I_O ..... 20 mA
Duration of output short-circuit current to GND (see Note 3) ..... unlimited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package ..... 260°C

† Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	0	1.75	V
	V_{DD} = 5 V	0	3.75	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature†

PARAMETER		TEST CONDITIONS		T_A‡	TLV2352I						UNIT
					V_{DD} = 3 V			V_{DD} = 5 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min,	See Note 4	25°C		1	5		1	5	mV
				Full range			7			7	
I_{IO}	Input offset current			25°C		1			1		pA
				85°C			1			1	nA
I_{IB}	Input bias current			25°C		5			5		pA
				85°C			2			2	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to 2			0 to 4			V
				Full range	0 to 1.75			0 to 3.75			
I_{OH}	High-level output current	V_{ID} = 1 V		25°C		0.1			0.1		nA
				Full range			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 2 mA	25°C		115	300		150	400	mV
				Full range			600			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		mA
I_{DD}	Supply current	V_{ID} = 1 V,	No load	25°C		120	250		140	300	µA
				Full range			350			400	

† All characteristics are measured with zero common-mode input voltages unless otherwise noted.
‡ Full range is −40°C to 85°C. IMPORTANT: See Parameter Measurement Information.
NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			TLV2352I			UNIT
				MIN	TYP	MAX	
Response time	R_L = 5.1 kΩ, C_L = 15 pF§,	See Note 5	100-mV input step with 5-mV overdrive		640		ns

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			TLV2352I			UNIT
				MIN	TYP	MAX	
Response time	R_L = 5.1 kΩ, C_L = 15 pF§,	See Note 5	100-mV input step with 5-mV overdrive		650		ns
			TTL-level input step		200		

§ C_L includes probe and jig capacitance.
NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or V_O = 1.4 V with V_{DD} = 5 V.

electrical characteristics at specified free-air temperature, T_A = 25°C†

PARAMETER		TEST CONDITIONS		TLV2352Y						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min,	See Note 4		1	5		1	5	mV
I_{IO}	Input offset current				1			1		pA
I_{IB}	Input bias current				5			5		pA
V_{ICR}	Common-mode input voltage range			0 to 2			0 to 4			V
I_{OH}	High-level output current	V_{ID} = 1 V			0.1			0.1		nA
V_{OL}	Low-level output voltage	V_{ID} = −1 V	I_{OL} = 2 mA		115	300		150	400	mV
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	6	16		6	16		mA
I_{DD}	Supply current	V_{ID} = 1 V	No load		120	250		140	300	μA

† All characteristics are measured with zero common-mode input voltages unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

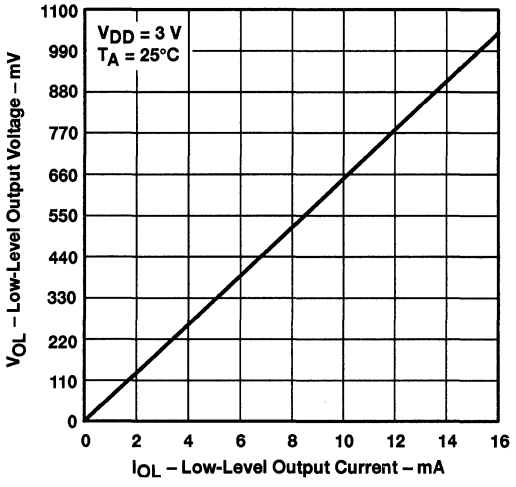


Figure 1

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

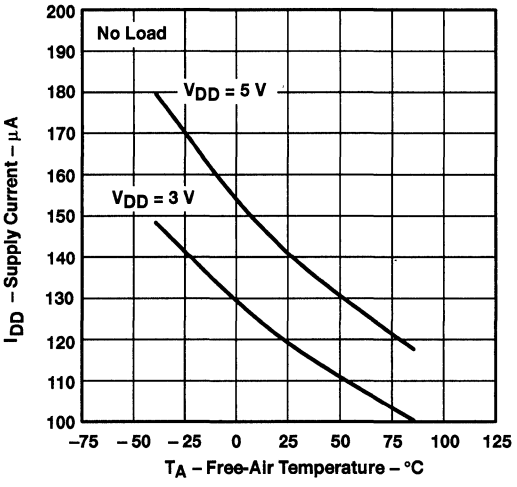


Figure 2

COMMON-MODE INPUT VOLTAGE RANGE vs FREE-AIR TEMPERATURE

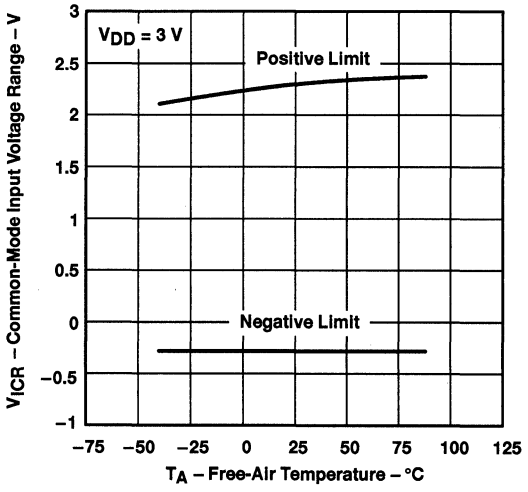


Figure 3

OUTPUT FALL TIME vs CAPACITIVE LOAD

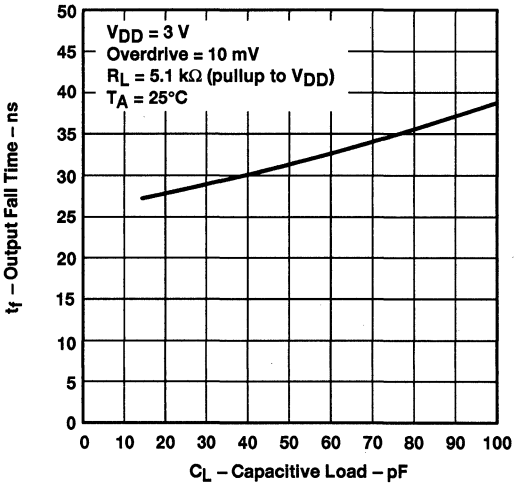


Figure 4

TYPICAL CHARACTERISTICS

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

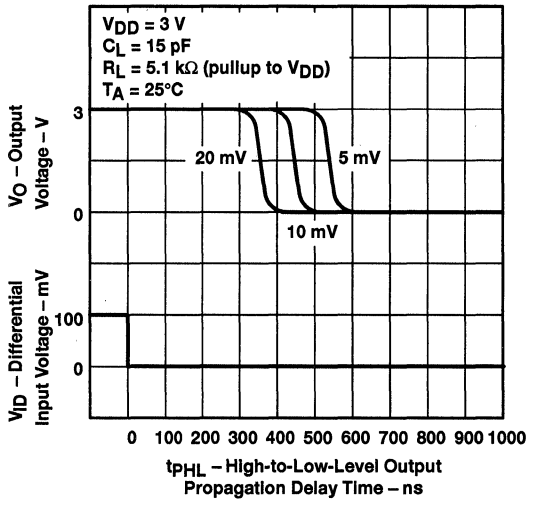


Figure 5

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS CAPACITIVE LOADS

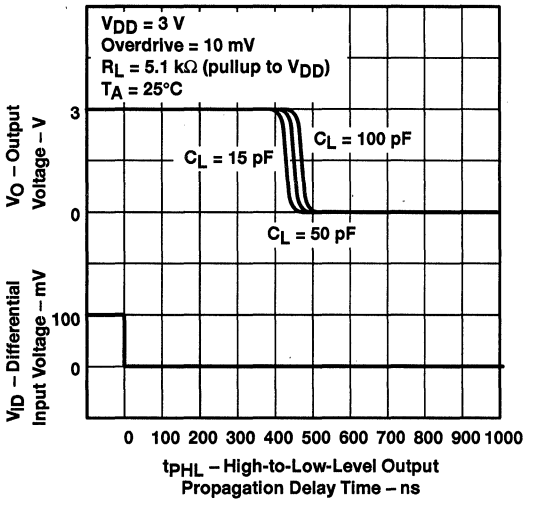


Figure 6

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

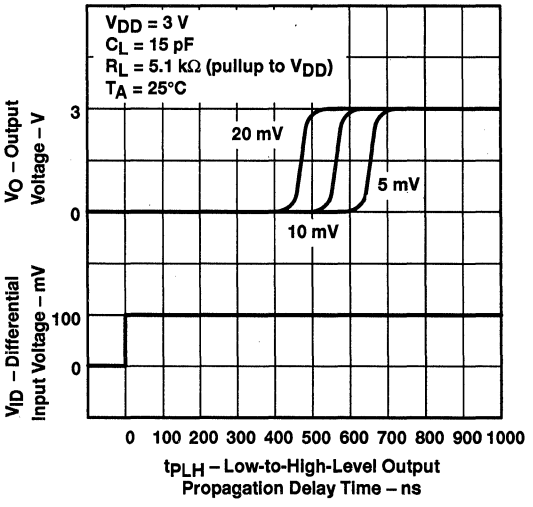


Figure 7

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS CAPACITIVE LOADS

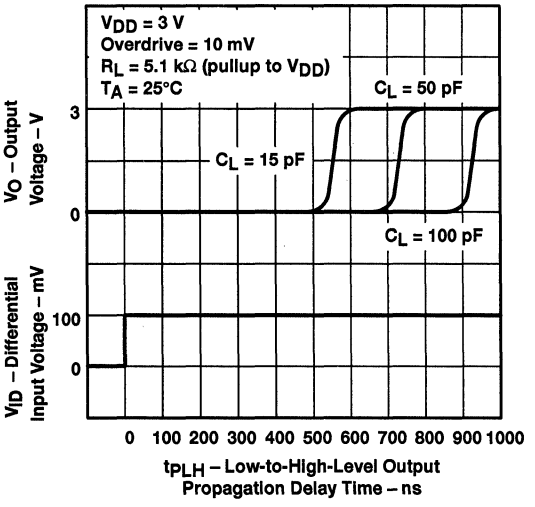


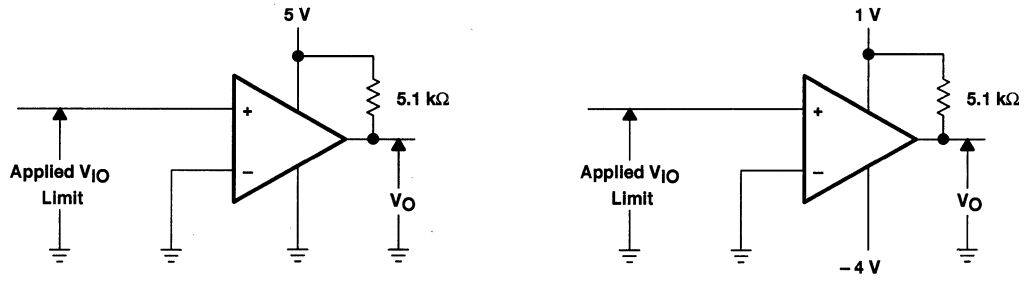
Figure 8

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLV2352 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 9(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 9(b) for the V_{ICR} test, rather than changing the input voltages to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0 (b) V_{IO} WITH V_{IC} = 4 V

Figure 9. Method for Verifying That Input Offset Voltage Is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes states.

PARAMETER MEASUREMENT INFORMATION

Figure 10 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage dividers R9 and R10 provide a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

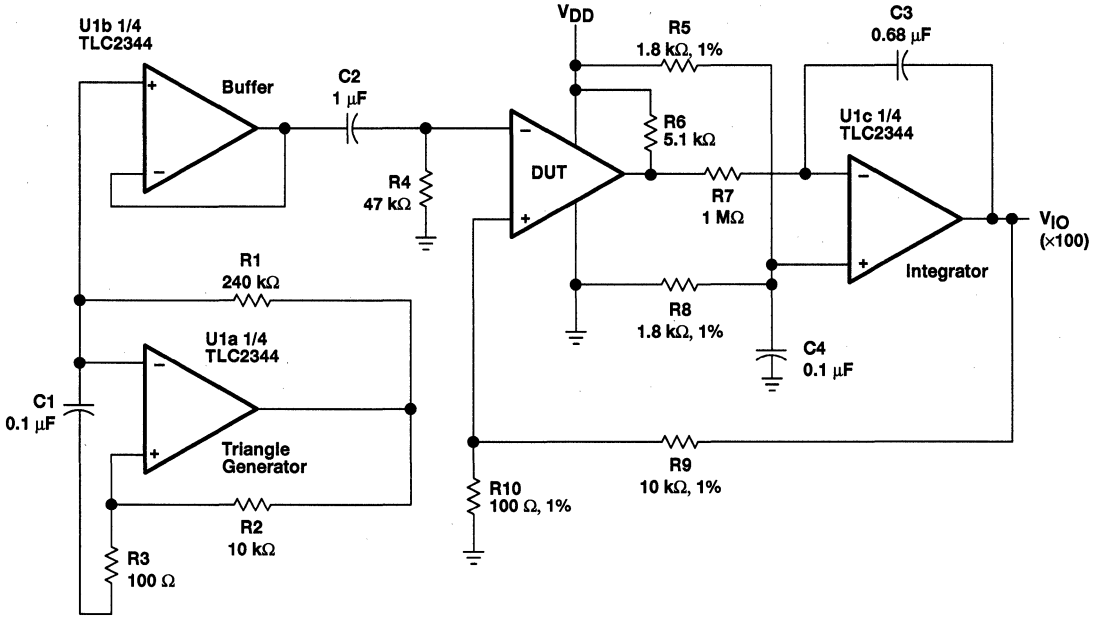


Figure 10. Circuit for Input Offset Voltage Measurement

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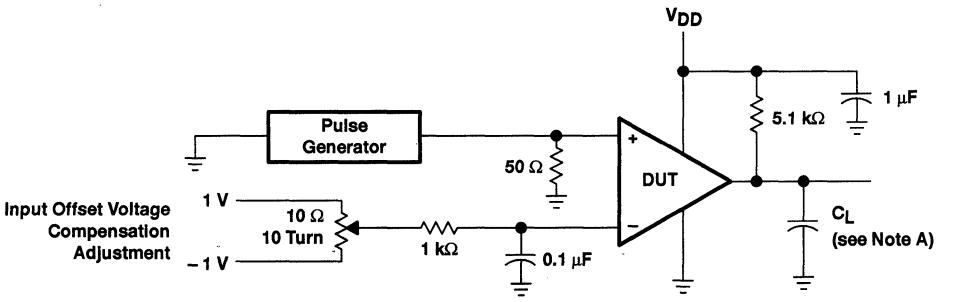
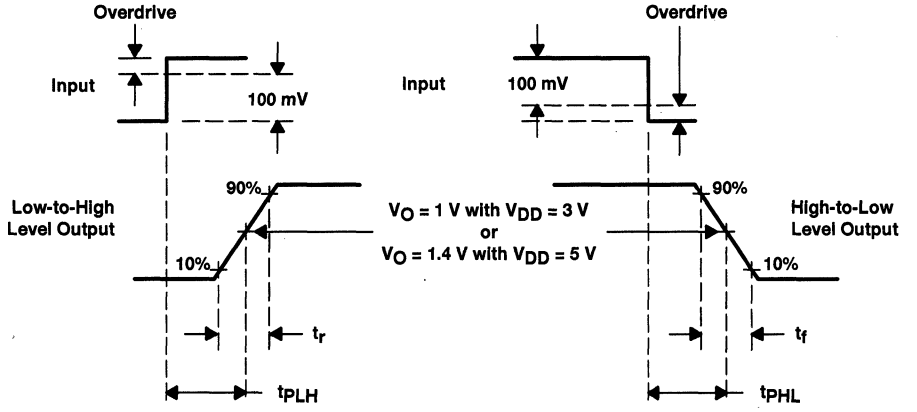
PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or when the output crosses V_O = 1.4 V with V_{DD} = 5 V. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation-delay-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 11) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change states.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

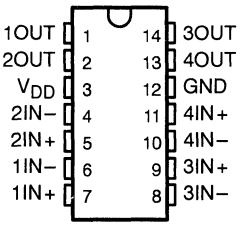
Figure 11. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms

LinCMOS™ QUADRUPLE LOW-VOLTAGE DIFFERENTIAL COMPARATORS

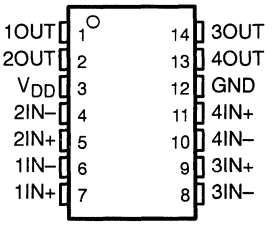
SLCS012 – MAY 1992

- **Wide Range of Supply Voltages 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Very-Low Supply-Current Drain 240 μA Typ at 3 V**
- **Common-Mode Input Voltage Range Includes Ground**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Output Compatible With TTL, MOS, and CMOS**
- **Built-In ESD Protection**

D OR N PACKAGE
(TOP VIEW)



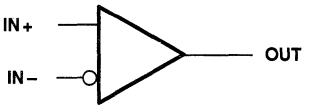
PW PACKAGE
(TOP VIEW)



description

The TLV2354 consists of four independent, low-power comparators specifically designed for single power-supply applications and to operate with power-supply rails as low as 2 V. When powered from a 3-V supply, the typical supply current is only 240 μA.

symbol (each comparator)



The TLV2354 is designed using the Texas Instruments LinCMOS™ technology and therefore features an extremely high input impedance (typically greater than 10^{12} Ω), which allows direct interfacing with high-impedance sources. The outputs are N-channel open-drain configurations that require an external pullup resistor to provide a positive output voltage swing, and they can be connected to achieve positive-logic wired-AND relationships. The TLV2354 is fully characterized for operation from – 40°C to 85°C.

The TLV2354 has internal electrostatic-discharge (ESD)-protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

AVAILABLE OPTIONS

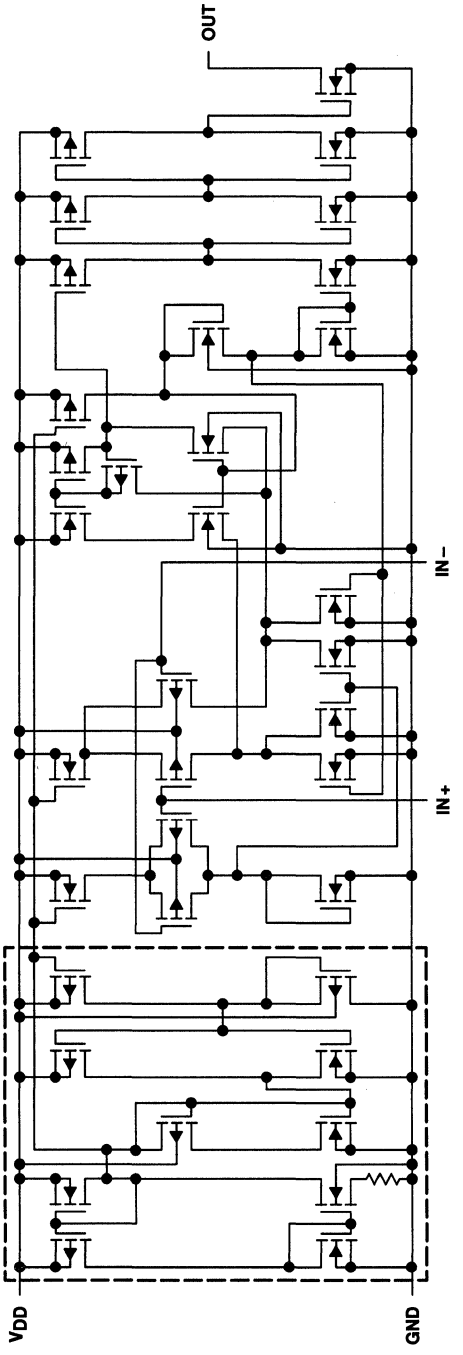
T_A	V_{IO}max at 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
–40°C to 85°C	5 mV	TLV2354ID	TLV2354IN	TLV2354IPWLE	TLV2354Y

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLV2352IDR).
PW packages are only available left-ended taped and reeled, (e.g., TLV2354IPWLE)

Caution. These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

LinCMOS is a trademark of Texas Instruments Incorporated.

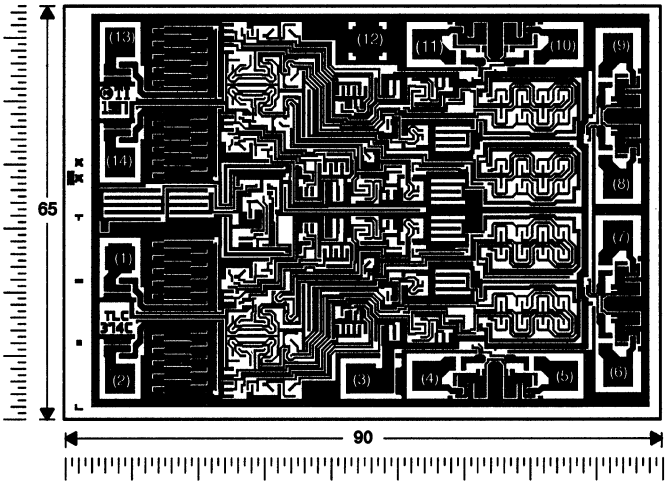
TLV2354I equivalent schematic

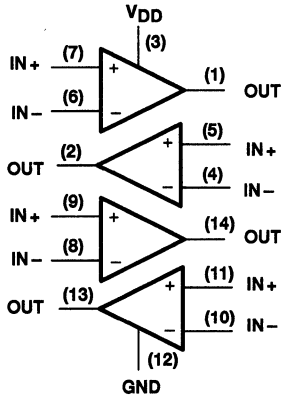


TLV2354Y chip information

These chips, when properly assembled, display characteristics similar to the TLV2354. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... ±8 V
Input voltage range, V_I ..... −0.3 to 8 V
Output voltage, V_O ..... 8 V
Input current, I_I ..... ±5 mA
Output current, I_O ..... 20 mA
Duration of output short-circuit current to GND (see Note 3) ..... unlimited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW
PW	700 mW	5.6 mW/°C	346 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	0	1.75	V
	V_{DD} = 5 V	0	3.75	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature†

PARAMETER		TEST CONDITIONS		T_A‡	TLV2354I						UNIT
					V_{DD} = 3 V			V_{DD} = 5 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min,	See Note 4	25°C		1	5		1	5	mV
				Full range			7			7	
I_{IO}	Input offset current			25°C		1			1		pA
				85°C			1			1	nA
I_{IB}	Input bias current			25°C		5			5		pA
				85°C			2			2	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to 2			0 to 4			V
				Full range	0 to 1.75			0 to 3.75			
I_{OH}	High-level output current	V_{ID} = 1 V		25°C		0.1			0.1		nA
				Full range			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 2 mA	25°C		115	300		150	400	mA
				Full range			600			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		mA
I_{DD}	Supply current	V_{ID} = 1 V,	No load	25°C		240	500		290	600	µA
				Full range			700			800	

† All characteristics are measured with zero common-mode input voltage unless otherwise noted.
‡ Full range is −40°C to 85°C. IMPORTANT: See Parameter Measurement Information.
NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			TLV2354I			UNIT
				MIN	TYP	MAX	
Response time	R_L = 5.1 kΩ, See Note 5	C_L = 15 pF§,	100-mV input step with 5-mV overdrive		640		ns

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			TLV2354I			UNIT
				MIN	TYP	MAX	
Response time	R_L = 5.1 kΩ, See Note 5	C_L = 15 pF§,	100-mV input step with 5-mV overdrive		650		ns
			TTL-level input step		200		

§ C_L includes probe and jig capacitance.
NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or when the output crosses V_O = 1.4 with V_{DD} = 5 V.

electrical characteristics at specified free-air temperature, T_A = 25°C†

PARAMETER		TEST CONDITIONS		TLV2354Y						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min,	See Note 4		1	5		1	5	mV
I_{IO}	Input offset current				1			1		pA
I_{IB}	Input bias current				5			5		pA
V_{ICR}	Common-mode input voltage range			0 to 2			0 to 4			V
I_{OH}	High-level output current	V_{ID} = 1 V			0.1			0.1		nA
V_{OL}	Low-level output voltage	V_{ID} = −1 V	I_{OL} = 2 mA		115	300		150	400	mV
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	6	16		6	16		mA
I_{DD}	Supply current	V_{ID} = 1 V	No load		240	500		290	600	µA

† All characteristics are measured with zero common-mode input voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

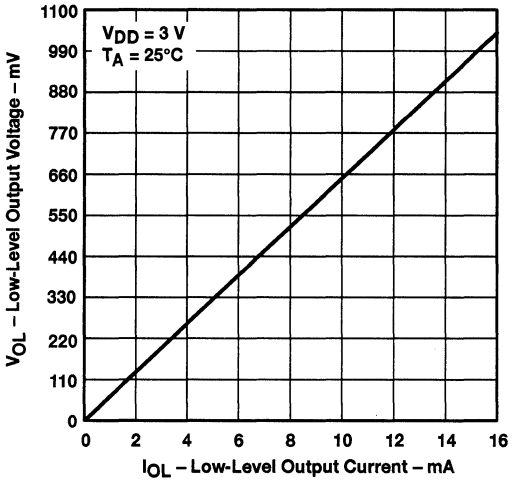


Figure 1

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

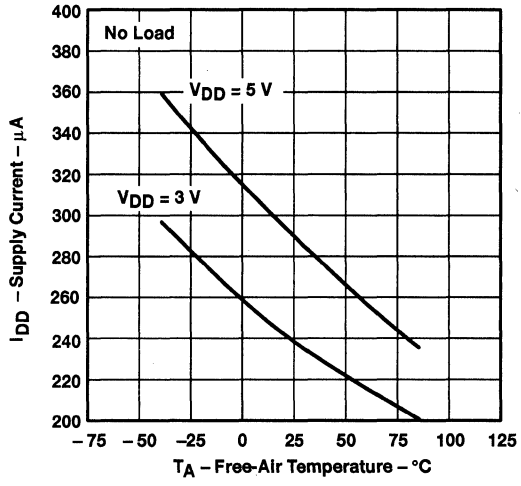


Figure 2

COMMON-MODE INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

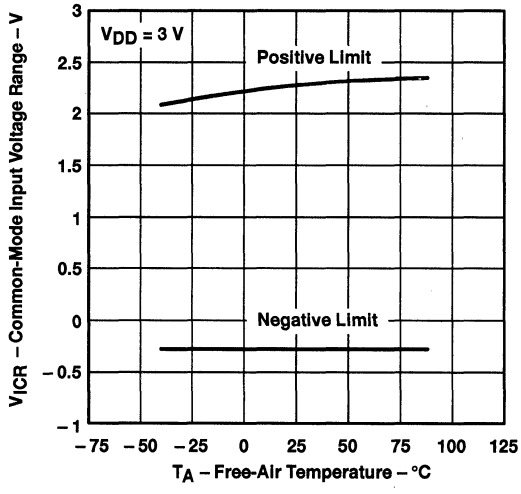


Figure 3

OUTPUT FALL TIME
vs
CAPACITIVE LOAD

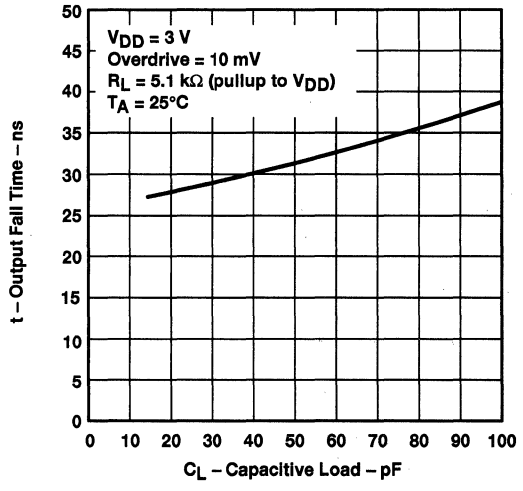


Figure 4

TYPICAL CHARACTERISTICS

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

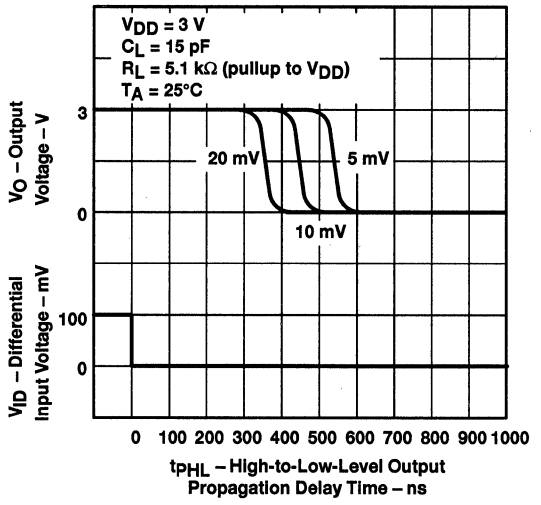


Figure 5

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS CAPACITIVE LOADS

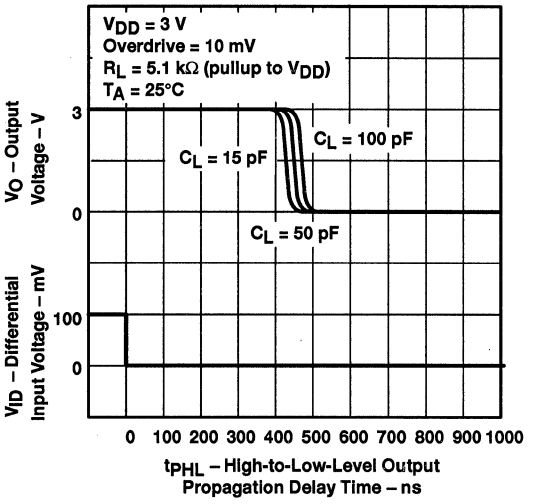


Figure 6

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

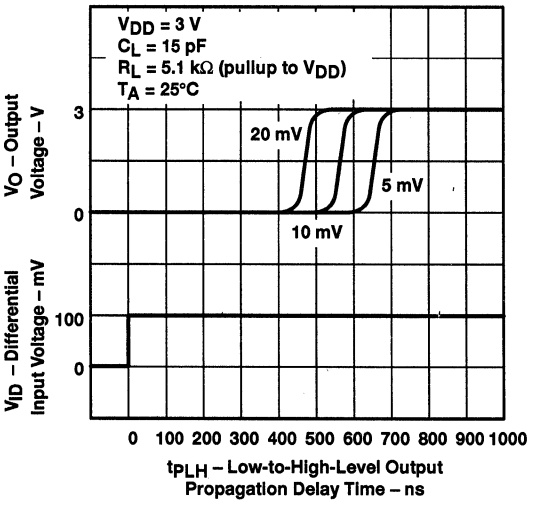


Figure 7

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS CAPACITIVE LOADS

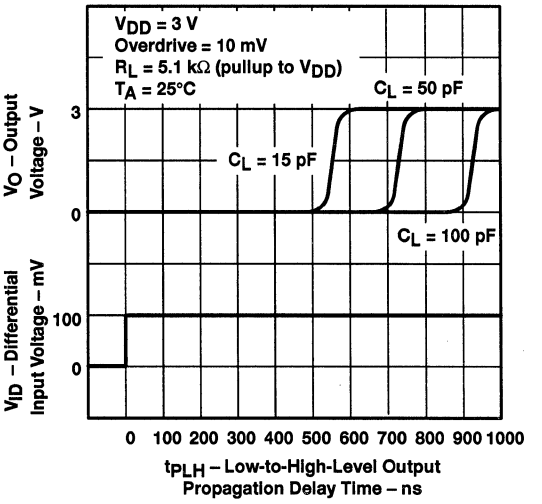


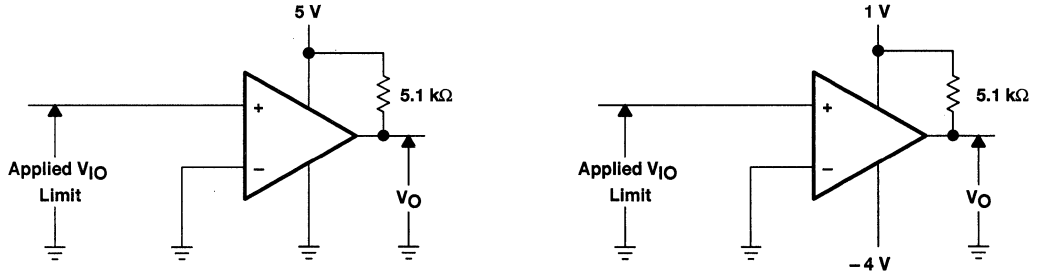
Figure 8

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLV2354 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 9(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 9(b) for the V_{ICR} test rather than changing the input voltages to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0 (b) V_{IO} WITH V_{IC} = 4 V

Figure 9. Method for Verifying That Input Offset Voltage Is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes states.

PARAMETER MEASUREMENT INFORMATION

Figure 10 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage dividers R9 and R10 provide a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

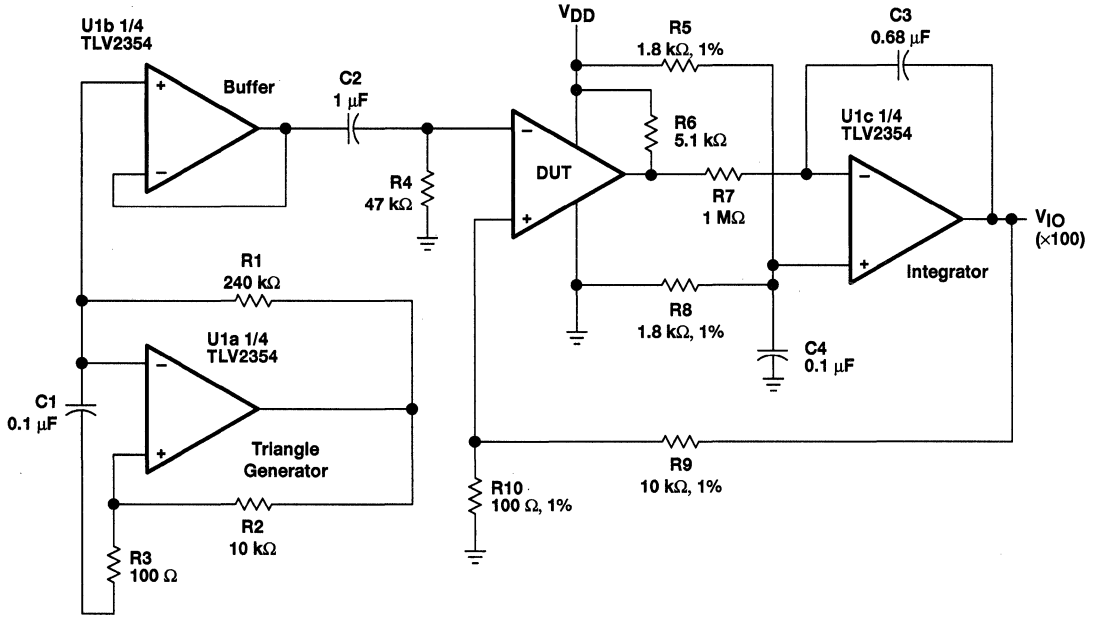
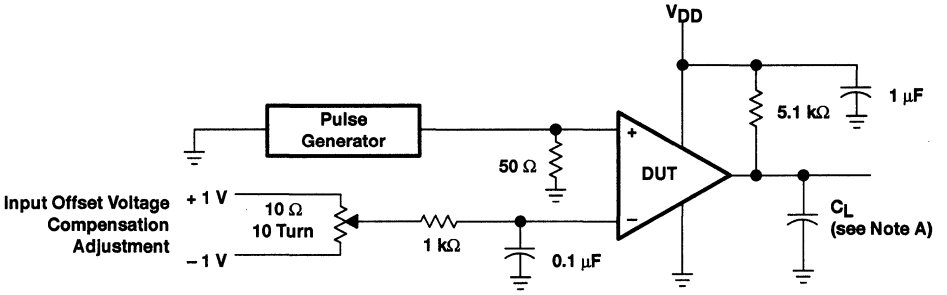


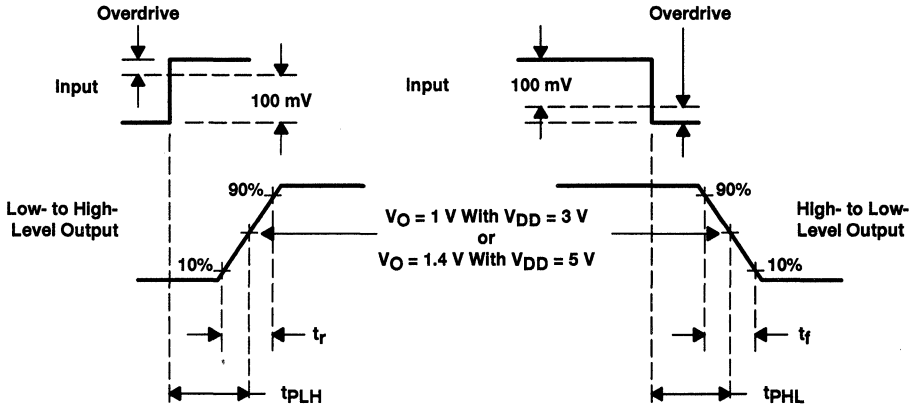
Figure 10. Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or when the output crosses V_O = 1.4 V with V_{DD} = 5 V. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation-delay-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, cause the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

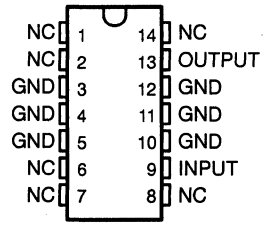
NOTE A: C_L includes probe and jig capacitance.

Figure 11. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms

SLVS067A – MARCH 1992 – REVISED NOVEMBER 1992

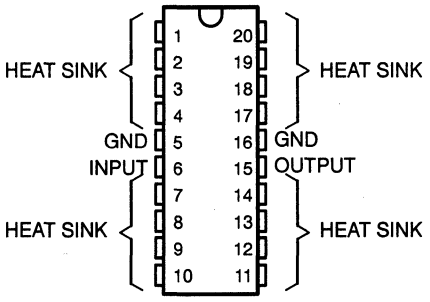
- **Fixed 3.3-V Output**
- **±1% Maximum Output Voltage Tolerance at T_J = 25°C**
- **500-mV Maximum Dropout Voltage at 500 mA**
- **500-mA Dropout Current**
- **±2% Absolute Output Voltage Variation**
- **Internal Overcurrent Limiting**
- **Internal Thermal-Overload Protection**
- **Internal Overvoltage Protection**

N PACKAGE
(TOP VIEW)



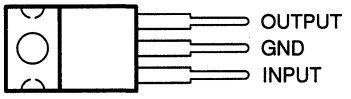
NC – No internal connection

PW PACKAGE
(TOP VIEW)



HEAT SINK – These pins have an internal resistive connection to ground and should be grounded.

KC PACKAGE
(TOP VIEW)



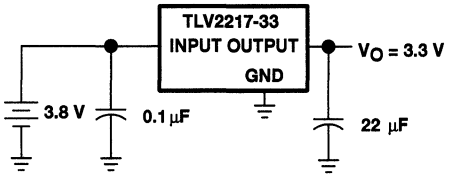
description

The TLV2217-33 is a low-dropout 3.3-V fixed voltage regulator. The regulator is capable of sourcing 500 mA of current with an input-output differential of 0.5 V or less. The TLV2217-33 provides internal overcurrent limiting, thermal-overload protection, and overvoltage protection.

The 0.5-V dropout for the TLV2217-33 makes it ideal for battery applications in 3.3-V logic systems. For example, battery input voltage to the regulator may drop as low as 3.8 V, and the TLV2217-33 will continue to regulate the system. For higher voltage systems, the TLV2217-33 may be operated with a continuous input voltage of 12 V.

The TLV2217-33N and TLV2217-33KC cannot be harmed by temporary mirror-image insertion. This regulator is characterized for operation from 0°C to 125°C virtual junction temperature.

application schematic



AVAILABLE OPTIONS

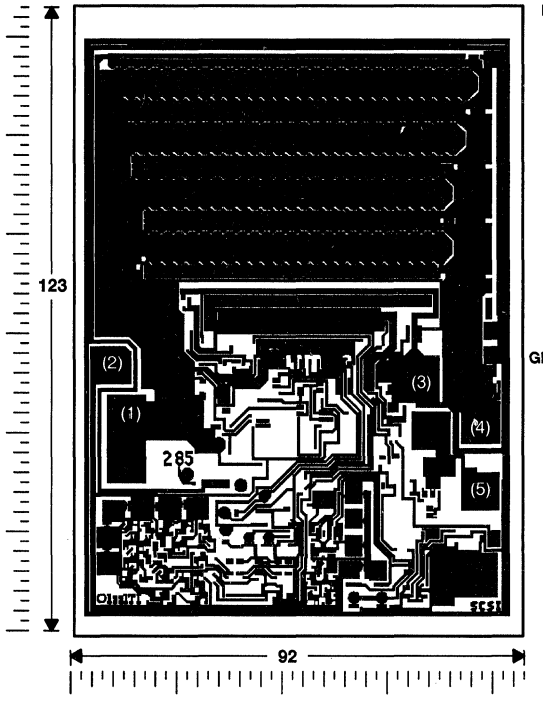
T_J	PACKAGED DEVICES			CHIP FORM (Y)
	PLASTIC POWER (KC)	PLASTIC DIP (N)	SURFACE MOUNT (PW)	
0°C to 125°C	TLV2217-33KC	TLV2217-33N	TLV2217-33PWLE	TLV2217-33Y

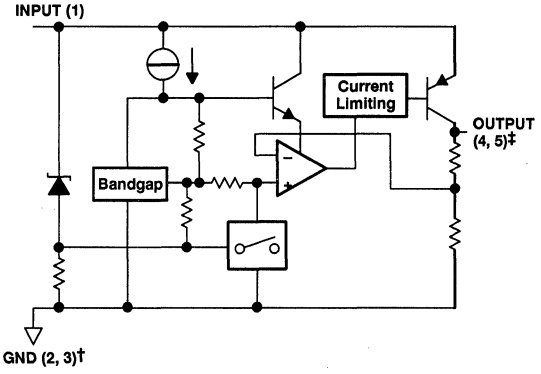
The PW package is only available left-end taped and reeled.

TLV2217-33Y chip information

These chips, when properly assembled, display characteristics similar to the TLV2217-33 (see electrical tables). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 11 TYPICAL

BONDING PADS: 7 × 7 MINIMUM

$T_J$max= 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

† Must connect pads 2 and 3 together

‡ Must connect pads 4 and 5 together

absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)

Continuous input voltage ..... 16 V
Continuous total dissipation (see Note 1) ..... See Dissipation Rating Table
Operating virtual junction temperature range ..... −55°C to 150°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: Refer to Figures 1 and 2 to avoid exceeding the design maximum virtual junction temperature; these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	T ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T = 25°C	T = 70°C POWER RATING	T = 85°C POWER RATING	T = 125°C POWER RATING
KC	T_A	2000 mW	16.0 mW/°C	1280 mW	1040 mW	400 mW
	T_C†	20000 mW	182.0 mW/°C	14540 mW	11810 mW	4645 mW
N	T_A	2250 mW	18.0 mW/°C	1440 mW	1170 mW	450 mW
	T_C	11850 mW	94.8 mW/°C	7584 mW	6162 mW	2370 mW
PW	T_A	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
	T_C	4625 mW	37.0 mW/°C	2960 mW	2405 mW	925 mW

† Derate above 40°C

DISSIPATION DERATING CURVE vs FREE-AIR TEMPERATURE

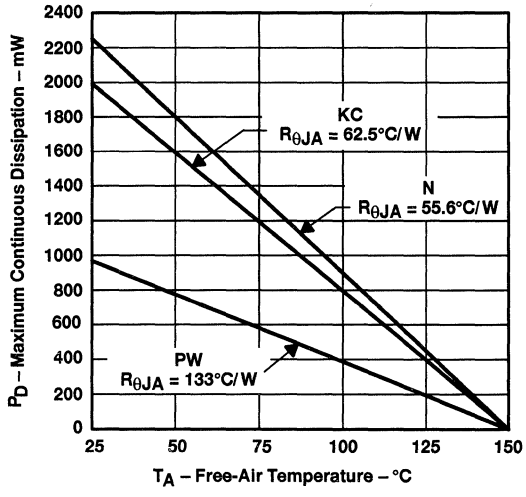


Figure 1

DISSIPATION DERATING CURVE vs CASE TEMPERATURE

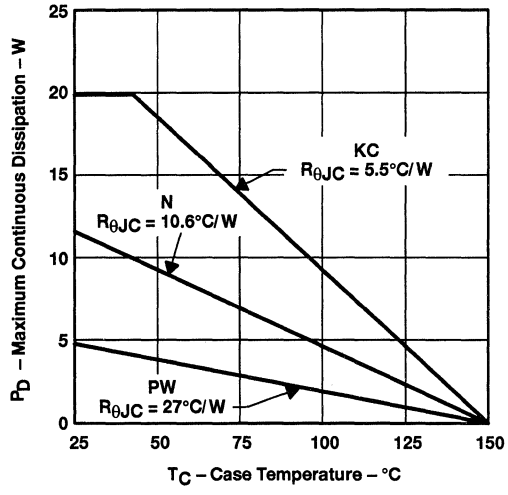


Figure 2

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	3.8	12	V
Output current, I_O	0	500	mA
Operating virtual junction temperature range, T_J	0	125	°C

electrical characteristics at V_I = 4.5 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TLV2217-33			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.8 V to 5.5 V	T_J = 25°C	3.267	3.30	3.333	V
		T_J = 0°C to 125°C	3.234		3.366	
Input regulation	V_I = 3.8 V to 5.5 V			5	15	mV
Ripple rejection	f = 120 Hz,	V_{ripple} = 1 V peak-to-peak		−62		dB
Output regulation	I_O = 20 mA to 500 mA			5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Dropout voltage	I_O = 250 mA				400	mV
	I_O = 500 mA				500	
Bias current	I_O = 0			2	5	mA
	I_O = 500 mA			19	49	

electrical characteristics at V_I = 4.5 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TLV2217-33Y			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 20 mA to 500 mA,	V_I = 3.8 V to 5.5 V	3.267	3.30	3.333	V
Input regulation	V_I = 3.8 V to 5.5 V			5	15	mV
Ripple rejection	f = 120 Hz,	V_{ripple} = 1 V peak-to-peak		−62		dB
Output regulation	I_O = 20 mA to 500 mA			5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Dropout voltage	I_O = 250 mA				400	mV
	I_O = 500 mA				500	
Bias current	I_O = 0			2	5	mA
	I_O = 500 mA			19	49	

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22-μF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.

COMPENSATION-CAPACITOR SELECTION INFORMATION

The TLV2217-33 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 3 and 4 can be used to establish the capacitance value and ESR range for best regulator performance.

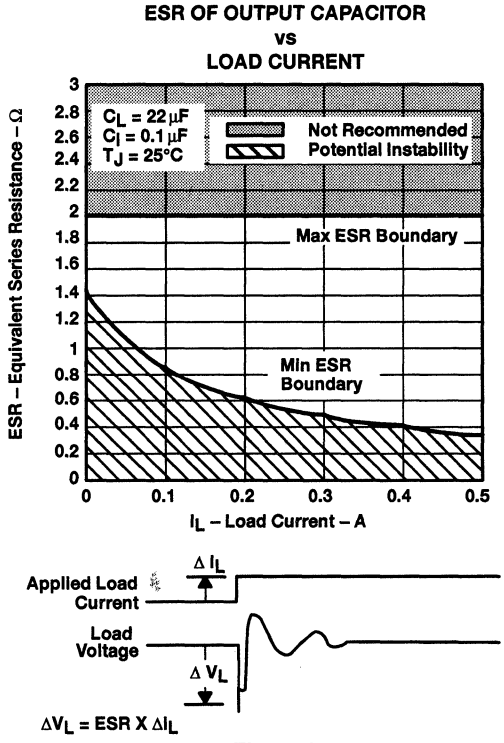


Figure 3

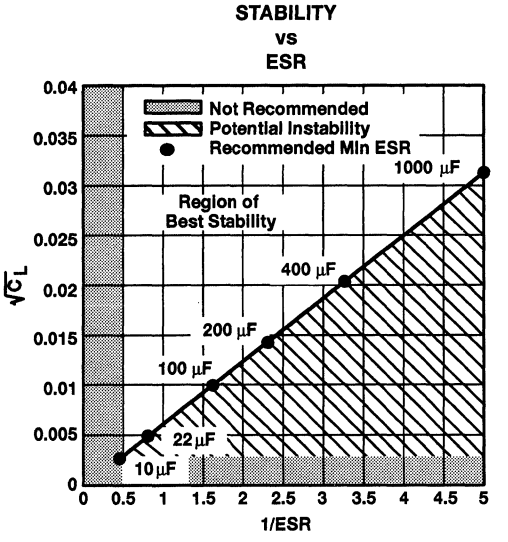
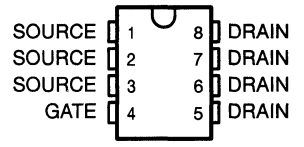


Figure 4

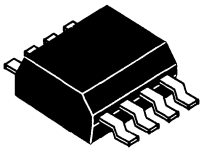
SLVS078A – DECEMBER 1993 – REVISED FEBRUARY 1994

- **Low $r_{DS(on)}$ . . . 0.18 Ω Typ at V_{GS} = −10 V**
- **3-V Compatible**
- **Requires No External V_{CC}**
- **TTL and CMOS Compatible Inputs**
- **$V_{GS(th)}$ = −1.5 V Max**
- **Available in Ultrathin TSSOP Package (PW)**
- **ESD Protected**

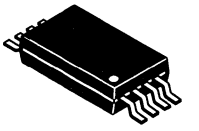
D OR PW PACKAGE
(TOP VIEW)



D PACKAGE



PW PACKAGE



description

The TPS1100 is a single p-channel enhancement-mode MOSFET. The device has been optimized for 3-V or 5-V power distribution in battery-powered systems by means of the Texas Instruments LinBiCMOS™ process. With a maximum $V_{GS(th)}$ of −1.5 V and an I_{DSS} of only 0.5 μA, the TPS1100 is the ideal high-side switch for low-voltage, portable battery-management systems where maximizing battery life is a primary concern. The low $r_{DS(on)}$ and excellent ac characteristics (rise time 10 ns typical) make the TPS1100 the logical choice for low-voltage switching applications such as power switches for pulse-width-modulated (PWM) controllers or motor/bridge drivers.

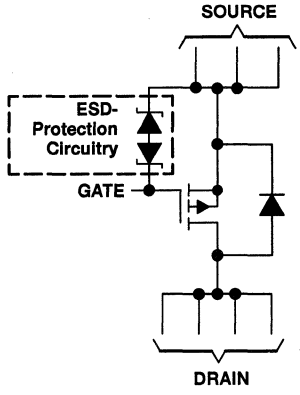
The ultrathin TSSOP (PW) version, with its smaller footprint and reduction in height, fits in places where other p-channel MOSFETs cannot. The size advantage is especially important where board real estate is at a premium and height restrictions do not allow for an SOIC package. Such applications include notebook computers, personal digital assistants (PDAs), cellular telephones, and PCMCIA cards. For existing designs, the D-packaged version has a pinout common with other p-channel MOSFETs in SOIC packages.

AVAILABLE OPTIONS

T_J	PACKAGED DEVICES†	
	SMALL OUTLINE (D)	TSSOP (PW)
−40°C to 150°C	TPS1100D	TPS1100PWLE

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1100DR). The PW package is available only left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS1100PWLE).

schematic



NOTE: For all applications, all source pins should be connected and all drain pins should be connected.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

absolute maximum ratings at T_A = 25°C (unless otherwise noted)†

					UNIT
Drain-to-source voltage, V_{DS}				–15	V
Gate-to-source voltage, V_{GS}				2, –15	V
Continuous drain current (T_J = 150°C), I_D‡	V_{GS} = –2.7 V	D package	T_A = 25°C	±0.41	A
			T_A = 125°C	±0.28	
		PW package	T_A = 25°C	±0.4	
			T_A = 125°C	±0.23	
	V_{GS} = –3 V	D package	T_A = 25°C	±0.6	
			T_A = 125°C	±0.33	
		PW package	T_A = 25°C	±0.53	
			T_A = 125°C	±0.27	
	V_{GS} = –4.5 V	D package	T_A = 25°C	±1	
			T_A = 125°C	±0.47	
		PW package	T_A = 25°C	±0.81	
			T_A = 125°C	±0.37	
	V_{GS} = –10 V	D package	T_A = 25°C	±1.6	
			T_A = 125°C	±0.72	
		PW package	T_A = 25°C	±1.27	
			T_A = 125°C	±0.58	
Pulsed drain current, I_{DM}‡				±7	A
Continuous source current (diode conduction), I_S				1	A
Storage temperature range, T_{stg}				–55 to 150	°C
Operating junction temperature range, T_J				–40 to 150	°C
Operating free-air temperature range, T_A				–40 to 125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 248°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq$ 25°C POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	791 mW	6.33 mW/°C	506 mW	411 mW	158 mW
PW	504 mW	4.03 mW/°C	323 mW	262 mW	100 mW

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 248°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

electrical characteristics at T_J = 25°C (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}$,	$I_D = -250$ µA		−1	−1.25	−1.50	V
V_{SD}	Source-to-drain voltage (diode forward voltage)†	$I_S = -1$ A,	$V_{GS} = 0$ V			−0.9		V
I_{GSS}	Reverse gate current, drain short circuited to source	$V_{DS} = 0$ V,	$V_{GS} = -12$ V				±100	nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -12$ V,	$V_{GS} = 0$ V	T_J = 25°C			−0.5	µA
				T_J = 125°C			−10	
$r_{DS(on)}$	Static drain-to-source on-state resistance†	$V_{GS} = -10$ V	$I_D = -1.5$ A			180		mΩ
		$V_{GS} = -4.5$ V	$I_D = -0.5$ A			291	400	
		$V_{GS} = -3$ V	$I_D = -0.2$ A			476	700	
		$V_{GS} = -2.7$ V				606	850	
g_{fs}	Forward transconductance†	$V_{DS} = -10$ V,	$I_D = -2$ A			2.5		S

† Pulse test: pulse duration ≤ 300 µs, duty cycle ≤ 2%

dynamic

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Q_g	Total gate charge	$V_{DS} = -10$ V,	$V_{GS} = -10$ V,	$I_D = -1$ A		5.45		nC
Q_{gs}	Gate-to-source charge					0.87		
Q_{gd}	Gate-to-drain charge					1.4		
$t_{d(on)}$	Turn-on delay time	$V_{DD} = -10$ V, $R_G = 6$ Ω,	$R_L = 10$ Ω, See Figures 1 and 2	$I_D = -1$ A,		4.5		ns
$t_{d(off)}$	Turn-off delay time					13		ns
t_r	Rise time					10		ns
t_f	Fall time					2		
$t_{rr(SD)}$	Source-to-drain reverse recovery time	$I_F = 5.3$ A,	di/dt = 100 A/µs			16		

PARAMETER MEASUREMENT INFORMATION

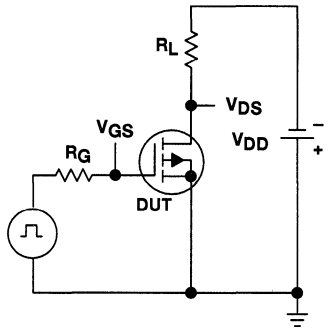


Figure 1. Switching-Time Test Circuit

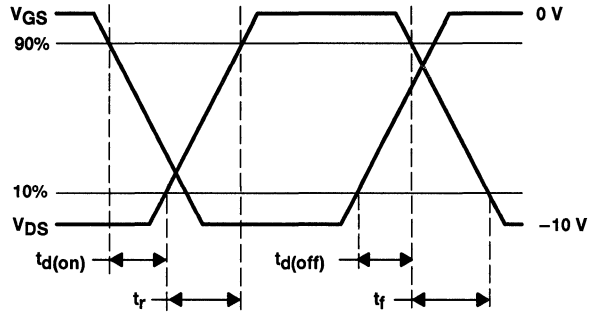


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

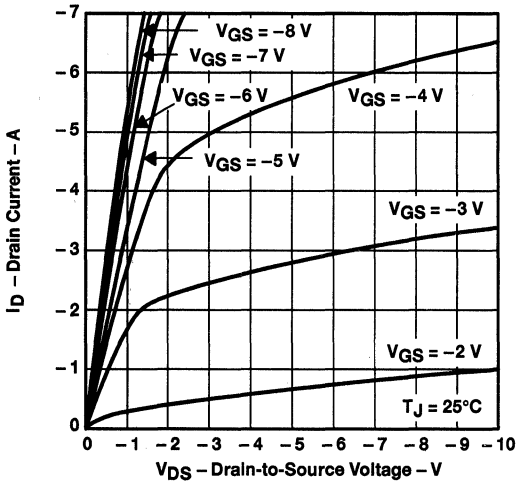


Figure 3

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

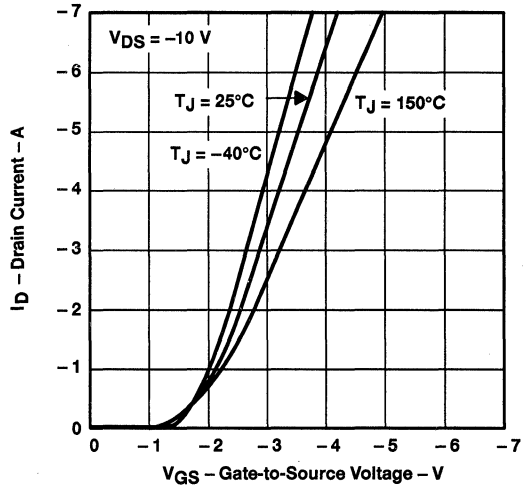


Figure 4

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

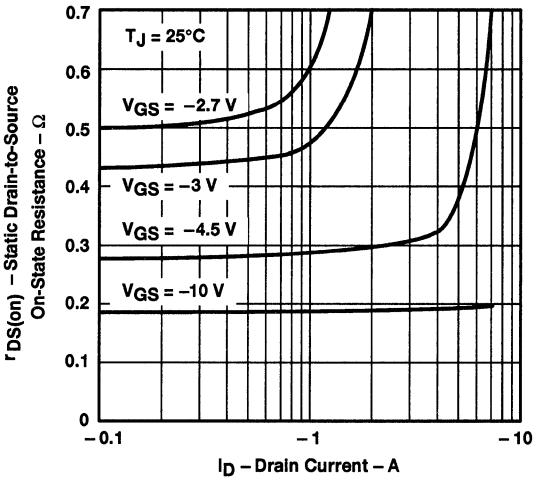
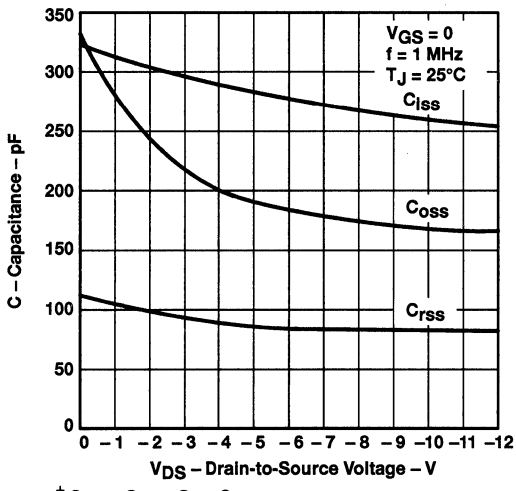


Figure 5

CAPACITANCE†
vs
DRAIN-TO-SOURCE VOLTAGE



† $C_{iss} = C_{gs} + C_{gd}$, $C_{ds(shorted)}$,

$$C_{rss} = C_{gd},\ C_{oss} = C_{ds} + \frac{C_{gs}\,C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$$

Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

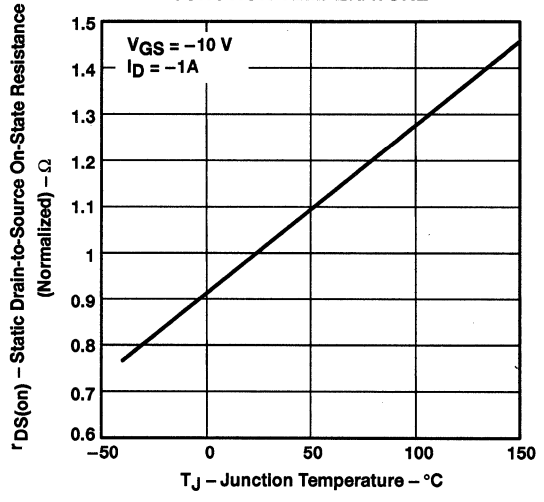


Figure 7

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

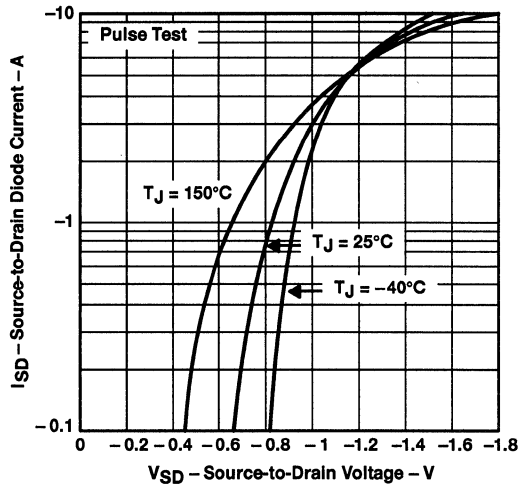


Figure 8

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs GATE-TO-SOURCE VOLTAGE

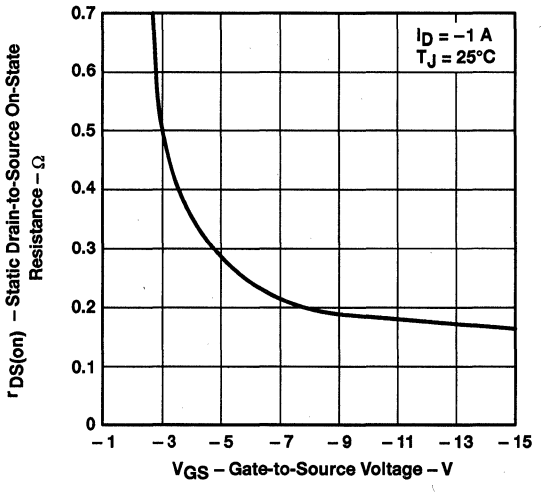


Figure 9

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

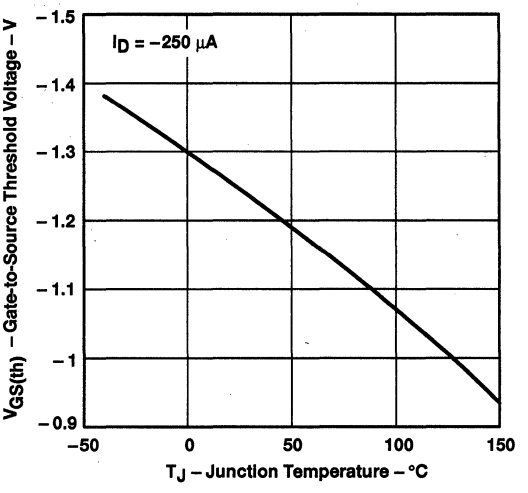


Figure 10

GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

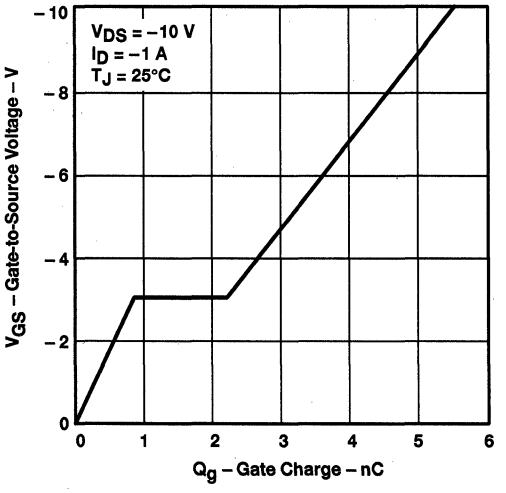


Figure 11

THERMAL INFORMATION

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

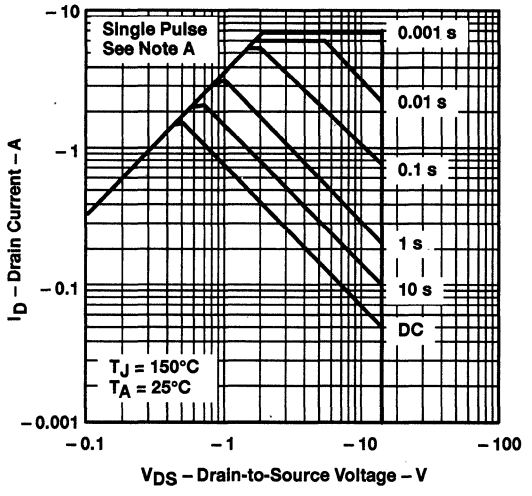


Figure 12

TRANSIENT JUNCTION-TO-AMBIENT
THERMAL IMPEDANCE
vs
PULSE DURATION

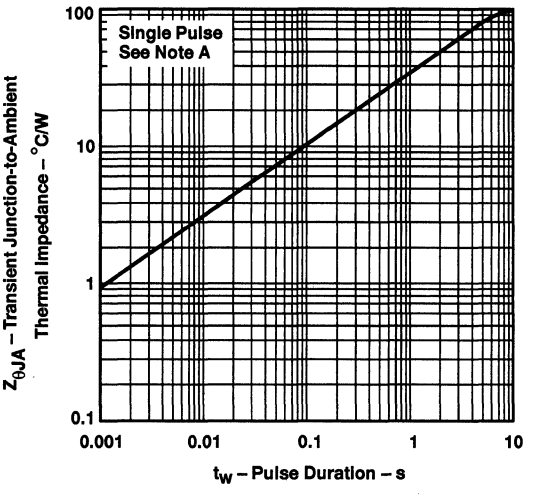


Figure 13

NOTE A: Values are for the D package and are FR4-board mounted only.

APPLICATION INFORMATION

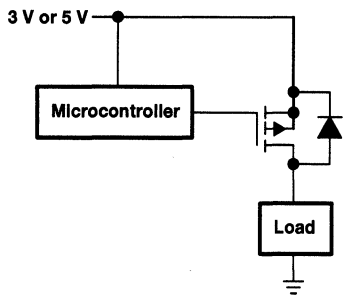


Figure 14. Notebook Load Management

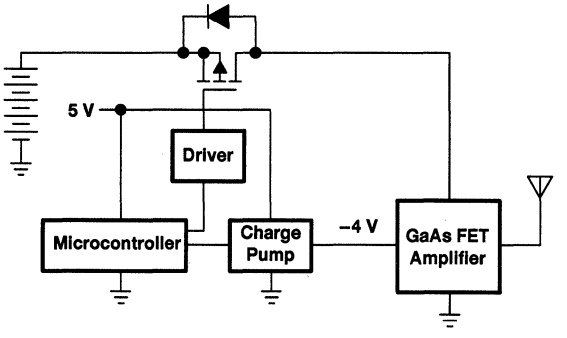
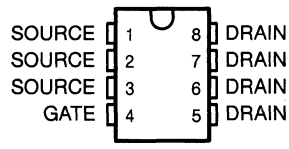


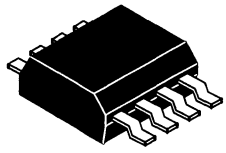
Figure 15. Cellular Phone Output Drive

SLVS079A – DECEMBER 1993 – REVISED FEBRUARY 1994

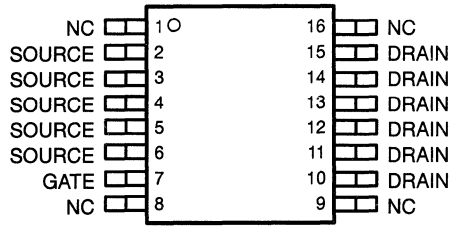
- **Low $r_{DS(on)}$ . . . 0.09 Ω Typ at V_{GS} = −10 V**
- **3-V Compatible**
- **Requires No External V_{CC}**
- **TTL and CMOS Compatible Inputs**
- **$V_{GS(th)}$ = −1.5 V Max**
- **Available in Ultrathin TSSOP Package (PW)**
- **ESD Protected**

D PACKAGE
(TOP VIEW)

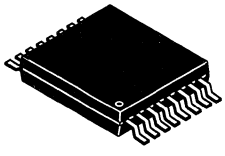




PW PACKAGE
(TOP VIEW)



NC – No internal connection



description

The TPS1101 is a single, low-$r_{DS(on)}$, p-channel, enhancement-mode MOSFET. The device has been optimized for 3-V or 5-V power distribution in battery-powered systems by means of the Texas Instruments LinBiCMOS™ process. With a maximum $V_{GS(th)}$ of −1.5 V and an I_{DSS} of only 0.5 μA, the TPS1101 is the ideal high-side switch for low-voltage, portable battery-management systems where maximizing battery life is a primary concern. The low $r_{DS(on)}$ and excellent ac characteristics (rise time 5.5 ns typical) of the TPS1101 make it the logical choice for low-voltage switching applications such as power switches for pulse-width-modulated (PWM) controllers or motor/bridge drivers.

The ultrathin TSSOP (PW) version fits in height-restricted places where other p-channel MOSFETs cannot. The size advantage is especially important where board height restrictions do not allow for an SOIC package. Such applications include notebook computers, personal digital assistants (PDAs), cellular telephones, and PCMCIA cards. For existing designs, the D-packaged version has a pinout common with other p-channel MOSFETs in SOIC packages.

AVAILABLE OPTIONS

T_J	PACKAGED DEVICES†	
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−40°C to 150°C	TPS1101D	TPS1101PWLE

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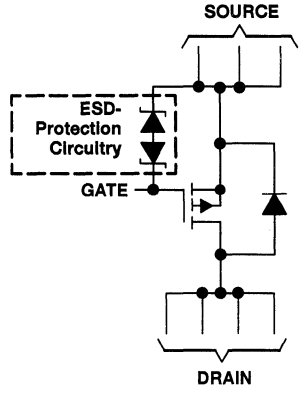
schematic



NOTE: For all applications, all source pins should be connected and all drain pins should be connected.

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absolute maximum ratings at T_A = 25°C (unless otherwise noted)†

					UNIT
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Gate-to-source voltage, V_{GS}				2, – 15	V
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			T_A = 125°C	±0.39	
		PW package	T_A = 25°C	±0.61	
			T_A = 125°C	±0.38	
	V_{GS} = –3 V	D package	T_A = 25°C	±0.88	
			T_A = 125°C	±0.47	
		PW package	T_A = 25°C	±0.86	
			T_A = 125°C	±0.45	
	V_{GS} = –4.5 V	D package	T_A = 25°C	±1.52	
			T_A = 125°C	±0.71	
		PW package	T_A = 25°C	±1.44	
			T_A = 125°C	±0.67	
	V_{GS} = –10 V	D package	T_A = 25°C	±2.30	
			T_A = 125°C	±1.04	
		PW package	T_A = 25°C	±2.18	
			T_A = 125°C	±0.98	
Pulsed drain current, I_{DM}‡				±10	A
Continuous source current (diode conduction), I_S				–1.1	A
Storage temperature range, T_{stg}				–55 to 150	°C
Operating junction temperature range, T_J				–40 to 150	°C
Operating free-air temperature range, T_A				–40 to 125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 176°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	791 mW	6.33 mW/°C	506 mW	411 mW	158 mW
PW	710 mW	5.68 mW/°C	454 mW	369 mW	142 mW

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 176°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

electrical characteristics at T_J = 25°C (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}$,	$I_D = -250$ µA		−1	−1.25	−1.5	V
V_{SD}	Source-to-drain voltage (diode forward voltage)†	$I_S = -1$ A,	$V_{GS} = 0$ V			−1.04		V
I_{GSS}	Reverse gate current, drain short circuited to source	$V_{DS} = 0$ V,	$V_{GS} = -12$ V				±100	nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -12$ V,	$V_{GS} = 0$ V	T_J = 25°C			−0.5	µA
				T_J = 125°C			−10	
$r_{DS(on)}$	Static drain-to-source on-state resistance†	$V_{GS} = -10$ V	$I_D = -2.5$ A			90		mΩ
		$V_{GS} = -4.5$ V	$I_D = -1.5$ A			134	190	
		$V_{GS} = -3$ V	$I_D = -0.5$ A			198	310	
		$V_{GS} = -2.7$ V				232	400	
g_{fs}	Forward transconductance†	$V_{DS} = -10$ V,	$I_D = -2$ A			4.3		S

† Pulse test: pulse duration ≤ 300 µs, duty cycle ≤ 2%.

dynamic

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Q_g	Total gate charge	$V_{DS} = -10$ V,	$V_{GS} = -10$ V,	$I_D = -1$ A		11.25		nC
Q_{gs}	Gate-to-source charge					1.5		
Q_{gd}	Gate-to-drain charge					2.6		
$t_{d(on)}$	Turn-on delay time	$V_{DD} = -10$ V, $R_G = 6\ \Omega$,	$R_L = 10\ \Omega$, See Figures 1 and 2	$I_D = -1$ A,		6.5		ns
$t_{d(off)}$	Turn-off delay time					19		ns
t_r	Rise time					5.5		ns
t_f	Fall time					13		
$t_{rr(SD)}$	Source-to-drain reverse recovery time	$I_F = 5.3$ A,	di/dt = 100 A/µs			16		

PARAMETER MEASUREMENT INFORMATION

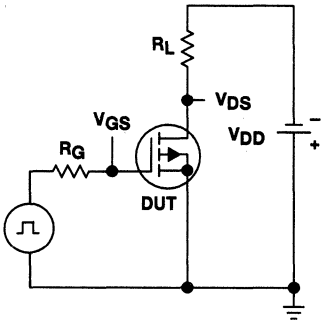


Figure 1. Switching-Time Test Circuit

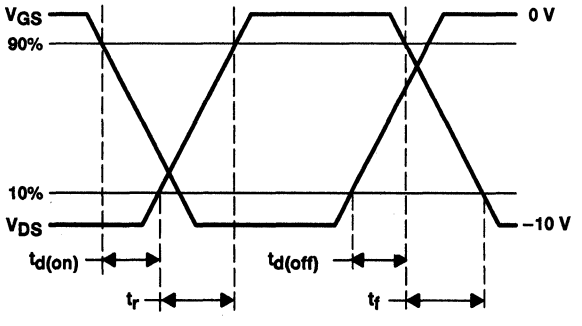


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

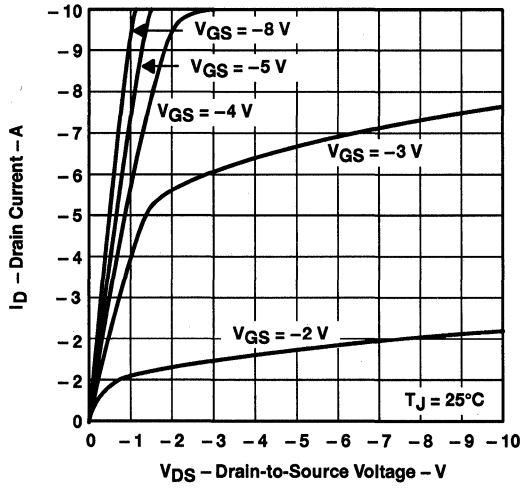


Figure 3

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

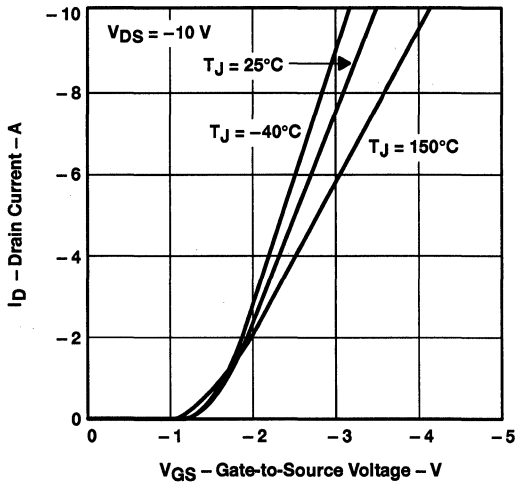


Figure 4

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

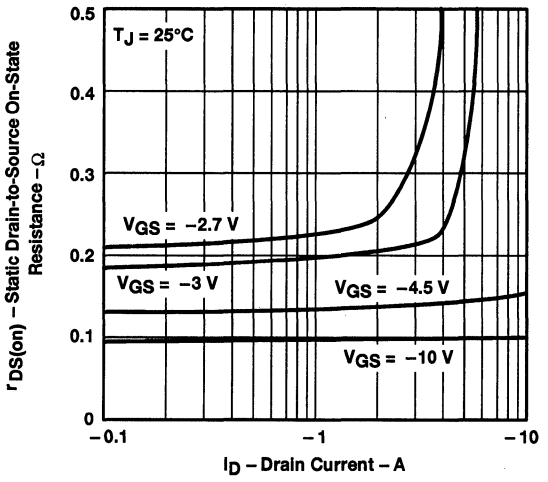
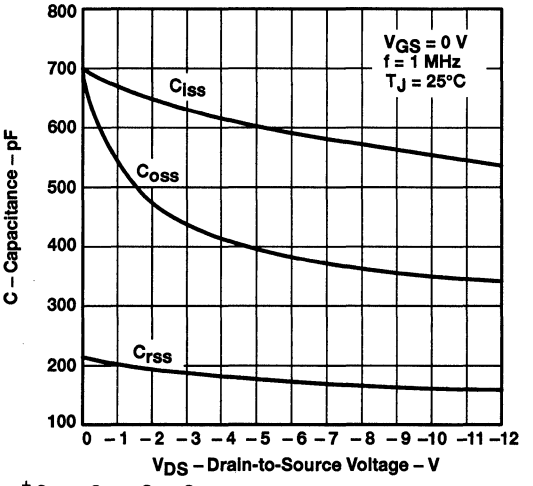


Figure 5

CAPACITANCE† vs DRAIN-TO-SOURCE VOLTAGE



† $C_{iss} = C_{gs} + C_{gd}$, $C_{ds(shorted)}$,

$C_{rss} = C_{gd}$, $C_{oss} = C_{ds} + \frac{C_{gs}\,C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$

Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

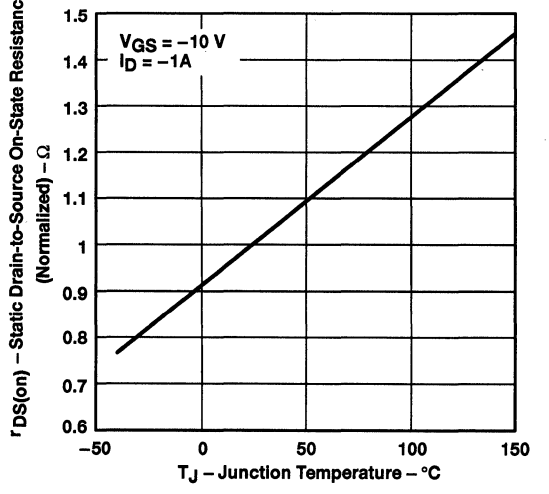


Figure 7

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

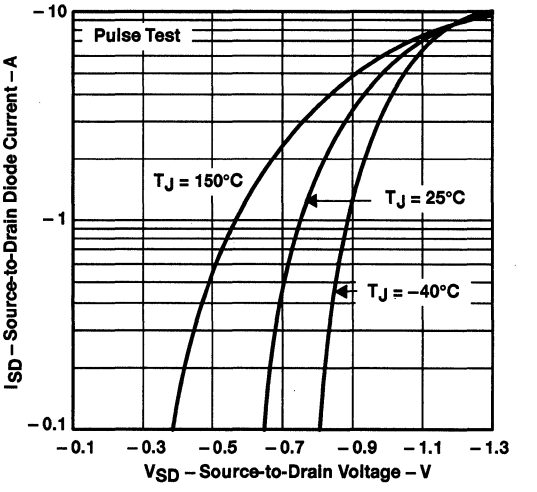


Figure 8

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
GATE-TO-SOURCE VOLTAGE

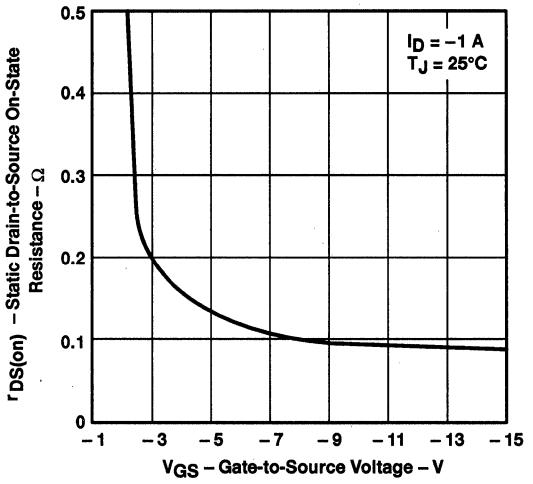


Figure 9

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

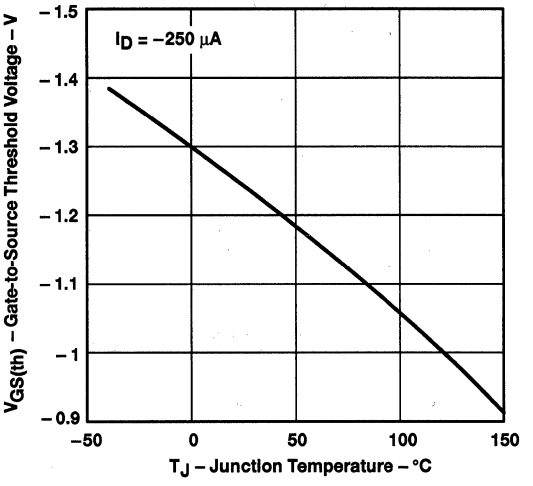


Figure 10

GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

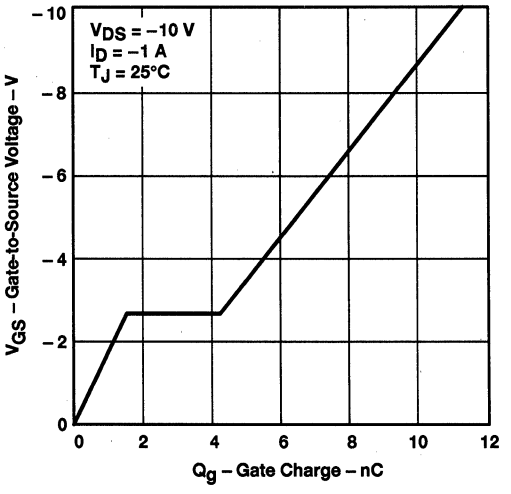


Figure 11

THERMAL INFORMATION

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

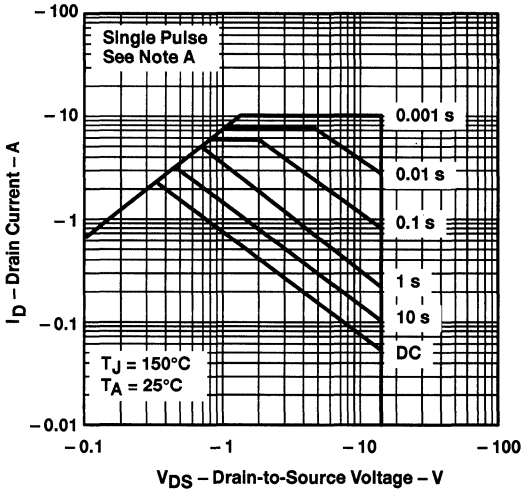


Figure 12

TRANSIENT JUNCTION-TO-AMBIENT
THERMAL IMPEDANCE
vs
PULSE DURATION

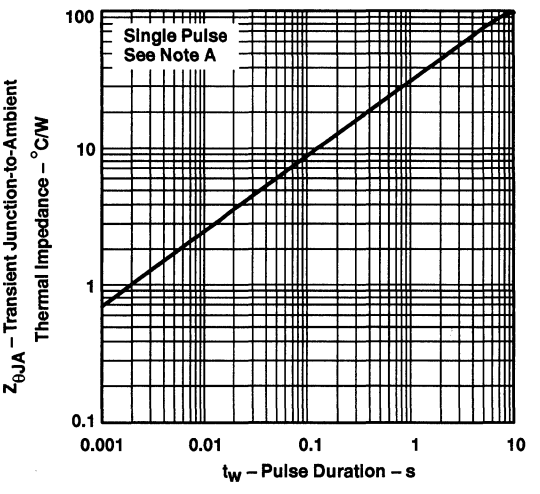


Figure 13

NOTE A: Values are for the D package and are FR4-board-mounted only.

APPLICATION INFORMATION

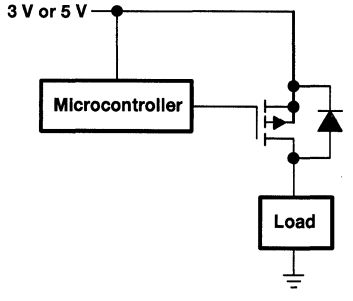


Figure 14. Notebook Load Management

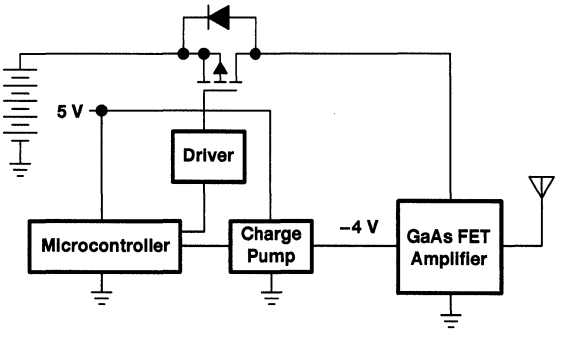
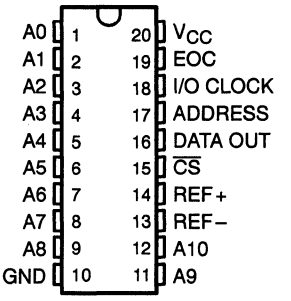


Figure 15. Cellular Phone Output Drive

- **Advanced LinEPIC™ Technology**
- **3.3-V Supply Operation**
- **10-Bit-Resolution A/D Converter**
- **11 Analog Input Channels**
- **Three Built-In Self-Test Modes**
- **Inherent Sample and Hold**
- **Total Unadjusted Error . . . ±1 LSB Max**
- **On-Chip System Clock**
- **End-of-Conversion (EOC) Output**
- **Pin Compatible With TLC1543**

DW, FK, J, OR N PACKAGE
(TOP VIEW)



description

The TLV1543C and TLV1543M are Advanced LinEPIC™ 10-bit, switched-capacitor, successive-approximation, analog-to-digital converters. These devices have three inputs and a 3-state output [chip select ($\overline{CS}$), input-output clock (I/O CLOCK), address input (ADDRESS), and data output (DATA OUT)] that provide a direct four-wire interface to the serial port of a host processor. The devices allow high-speed data transfers from the host.

In addition to a high-speed A/D converter and versatile control capability, these devices have an on-chip 14-channel multiplexer that can select any one of 11 analog inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of A/D conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the devices features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

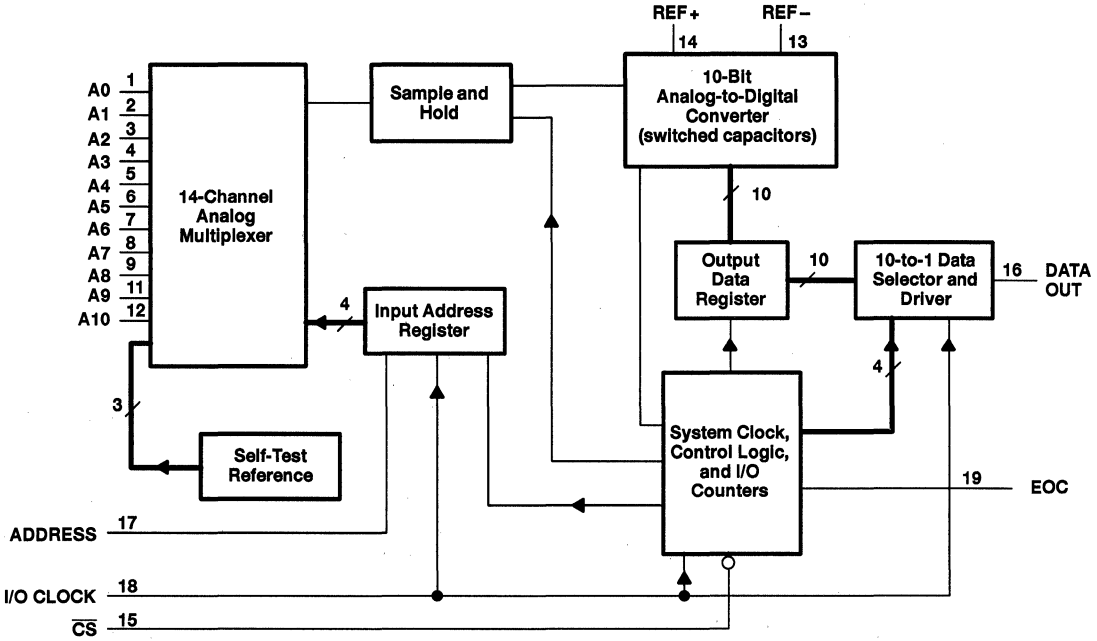
The TLV1543C is characterized for operation from 0°C to 70°C. The TLV1543M is characterized for operation over the full military temperature range of −55°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			
	SMALL OUTLINE (DW)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	TLV1543CDW	—	—	TLV1543CN
−55°C to 125°C	—	TLV1543MFK	TLV1543MJ	—

Advanced LinEPIC is a trademark of Texas Instruments Incorporated.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADDRESS	17	I	Serial address. A 4-bit serial address selects the desired analog input or test voltage that is to be converted next. The address data is presented with the MSB first and is shifted in on the first four rising edges of I/O CLOCK. After the four address bits have been read into the address register, this input is ignored for the remainder of the current conversion period.
A0–A10	1–9, 11, 12	I	Analog signal. The 11 analog inputs are applied to these terminals and are internally multiplexed. The driving source impedance should be less than or equal to 1 kΩ.
$\overline{CS}$	15	I	Chip select. A high-to-low transition on this input resets the internal counters and controls and enables DATA OUT, ADDRESS, and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables ADDRESS and I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OUT	16	O	The 3-state serial output for the A/D conversion result. This output is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives this output to the logic level corresponding to the next most significant bit, and the remaining bits are shifted out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs.
EOC	19	O	End of conversion. This output goes from a high- to a low- logic level on the trailing edge of the tenth I/O CLOCK and remains low until the conversion is complete and data are ready for transfer.
GND	10	I	The ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to this terminal.
I/O CLOCK	18	I	Input/output clock. This terminal receives the serial I/O CLOCK input and performs the following four functions: 1) It clocks the four input address bits into the address register on the first four rising edges of I/O CLOCK with the multiplex address available after the fourth rising edge. 2) On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 3) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 4) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF+	14	I	The upper reference voltage value (nominally V_{CC}) is applied to this terminal. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF– terminal.
REF–	13	I	The lower reference voltage value (nominally ground) is applied to this terminal.
V_{CC}	20	I	Positive supply voltage

detailed description

With chip select ($\overline{CS}$) inactive (high), the ADDRESS and I/O CLOCK inputs are initially disabled and DATA OUT is in the high-impedance state. When the serial interface takes $\overline{CS}$ active (low), the conversion sequence begins with the enabling of I/O CLOCK and ADDRESS and the removal of DATA OUT from the high-impedance state. The host then provides the 4-bit channel address to ADDRESS and the I/O CLOCK sequence to I/O CLOCK. During this transfer, the host serial interface also receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host. The first four I/O clocks load the address register with the 4-bit address on ADDRESS selecting the desired analog channel and the next six clocks providing the control timing for sampling the analog input.

detailed description (continued)

There are six basic serial interface timing modes that can be used with the device. These modes are determined by the speed of I/O CLOCK and the operation of $\overline{CS}$ as shown in Table 1. These modes are (1) a fast mode with a 10-clock transfer and $\overline{CS}$ inactive (high) between conversion cycles, (2) a fast mode with a 10-clock transfer and $\overline{CS}$ active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and $\overline{CS}$ inactive (high) between conversion cycles, (4) a fast mode with a 16-bit transfer and $\overline{CS}$ active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and $\overline{CS}$ inactive (high) between conversion cycles, and (6) a slow mode with a 16-clock transfer and $\overline{CS}$ active (low) continuously.

The MSB of the previous conversion appears on DATA OUT on the falling edge of $\overline{CS}$ in mode 1, mode 3, and mode 5, on the rising edge of EOC in mode 2 and mode 4, and following the 16th clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of I/O CLOCK. Ten bits of data are transmitted to the host through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the 10th clock falling edge, the EOC output goes low and returns to the high logic level when conversion is complete and the result can be read by the host. On the 10th clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLOCK transfer is more than ten clocks long.

Table 1 lists the operational modes with respect to the state of $\overline{CS}$, the number of I/O serial transfer clocks that can be used, and the timing edge on which the MSB of the previous conversion appears at the output.

Table 1. Mode Operation

MODES		$\overline{CS}$	NO. OF I/O CLOCKS	MSB AT DATA OUT†	TIMING DIAGRAM
Fast Modes	Mode 1	High between conversion cycles	10	$\overline{CS}$ falling edge	Figure 9
	Mode 2	Low continuously	10	EOC rising edge	Figure 10
	Mode 3	High between conversion cycles	11 to 16‡	$\overline{CS}$ falling edge	Figure 11
	Mode 4	Low continuously	16‡	EOC rising edge	Figure 12
Slow Modes	Mode 5	High between conversion cycles	11 to 16‡	$\overline{CS}$ falling edge	Figure 13
	Mode 6	Low continuously	16‡	16th clock falling edge	Figure 14

† These edges also initiate serial interface communication.
‡ No more than 16 clocks should be used.

fast modes

The device is in a fast mode when the serial I/O CLOCK data transfer is completed before the conversion is completed. With a 10-clock serial transfer, the device can only run in a fast mode since a conversion does not begin until the falling edge of the 10th I/O CLOCK.

mode 1: fast mode, $\overline{CS}$ inactive (high) between conversion cycles, 10-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer is ten clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 2: fast mode, $\overline{CS}$ active (low) continuously, 10-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer is ten clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

mode 3: fast mode, $\overline{CS}$ inactive (high) between conversion cycles, 11- to 16-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 4: fast mode, $\overline{CS}$ active (low) continuously, 16-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

slow modes

In a slow mode, the conversion is completed before the serial I/O CLOCK data transfer is completed. A slow mode requires a minimum 11-clock transfer into I/O CLOCK, and the rising edge of the 11th clock must occur before the conversion period is complete; otherwise, the device loses synchronization with the host serial interface, and $\overline{CS}$ has to be toggled to initialize the system. The 11th rising edge of the I/O CLOCK must occur within 9.5 μs after the 10th I/O clock falling edge.

mode 5: slow mode, $\overline{CS}$ inactive (high) between conversion cycles, 11- to 16-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 6: slow mode, $\overline{CS}$ active (low) continuously, 16-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions. The falling edge of the 16th I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16-clock transfer initiated by the serial interface.

address bits

The 4-bit analog channel-select address for the next conversion cycle is presented to the ADDRESS terminal (MSB first) and is clocked into the address register on the first four leading edges of I/O CLOCK. This address selects one of 14 inputs (11 analog inputs or 3 internal test inputs).

analog inputs and test modes

The 11 analog inputs and the 3 internal test inputs are selected by the 14-channel multiplexer according to the input address as shown in Tables 2 and 3. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching.

Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK, and sampling continues for six I/O CLOCK periods. The sample is held on the falling edge of the 10th I/O CLOCK. The three test inputs are applied to the multiplexer, sampled, and converted in the same manner as the external analog inputs.

Table 2. Analog-Channel-Select Address

ANALOG INPUT SELECTED	VALUE SHIFTED INTO ADDRESS INPUT	
	BINARY	HEX
A0	0000	0
A1	0001	1
A2	0010	2
A3	0011	3
A4	0100	4
A5	0101	5
A6	0110	6
A7	0111	7
A8	1000	8
A9	1001	9
A10	1010	A

Table 3. Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED†	VALUE SHIFTED INTO ADDRESS INPUT		OUTPUT RESULT (HEX)‡
	BINARY	HEX	
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	B	200
V_{ref-}	1100	C	000
V_{ref+}	1101	D	3FF

† V_{ref+} is the voltage applied to the REF+ input, and V_{ref-} is the voltage applied to the REF– input.

‡ The output results shown are the ideal values and vary with the reference stability and with internal offsets.

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half the V_{CC} voltage), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and the 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are counted.

converter and analog input (continued)

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.

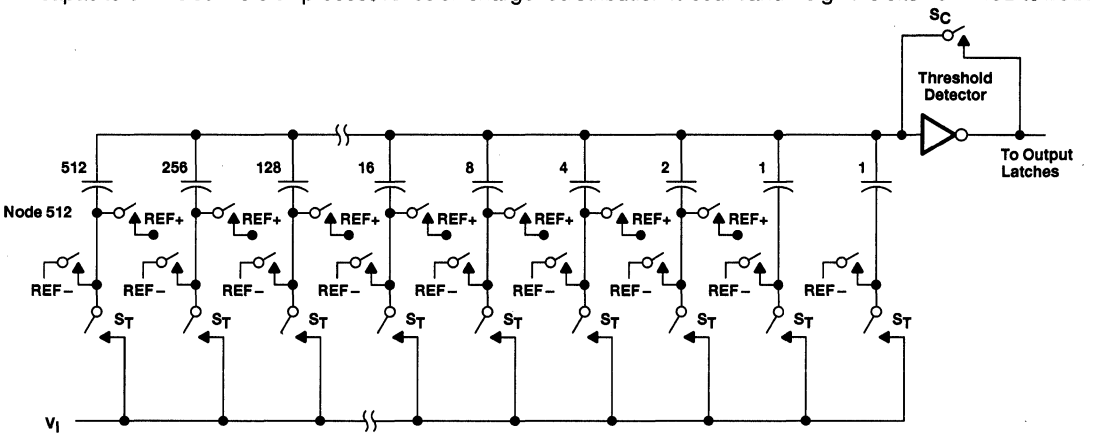


Figure 1. Simplified Model of the Successive-Approximation System

chip-select operation

The trailing edge of $\overline{CS}$ starts all modes of operation, and $\overline{CS}$ can abort a conversion sequence in any mode. A high-to-low transition on $\overline{CS}$ within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Exercise care to prevent $\overline{CS}$ from being taken low close to completion of conversion because the output data can be corrupted.

reference voltage inputs

There are two reference inputs used with these devices: REF+ and REF–. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading, respectively. The values of REF+, REF–, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF–.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1): TLV1543C ..... −0.5 V to 6.5 V
TLV1543M ..... −0.5 V to 6 V
Input voltage range, V_I (any input) ..... −0.3 V to V_{CC} + 0.3 V
Output voltage range ..... −0.3 V to V_{CC} + 0.3 V
Positive reference voltage, V_{ref+} ..... V_{CC} + 0.1 V
Negative reference voltage, V_{ref-} ..... −0.1 V
Peak input current (any input) ..... ±20 mA
Peak total input current (all inputs) ..... ±30 mA
Operating free-air temperature range, T_A: TLV1543C ..... 0°C to 70°C
TLV1543M ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	TLV1543C		3	3.3	5.5	V
	TLV1543M		3	3.3	3.6	V
Positive reference voltage, V_{ref+} (see Note 2)				V_{CC}		V
Negative reference voltage, V_{ref-} (see Note 2)				0		V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)			2.5	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	V
High-level control input voltage, V_{IH}	TLV1543C	V_{CC} = 3 V to 5.5 V	2			V
	TLV1543M	V_{CC} = 3 V to 3.6 V	2			V
Low-level control input voltage, V_{IL}	TLV1543C	V_{CC} = 3 V to 5.5 V			0.6	V
	TLV1543M	V_{CC} = 3 V to 3.6 V			0.8	V
Setup time, address bits at data input before I/O CLOCK↑, $t_{su(A)}$			100			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$			0			ns
Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_{h(CS)}$			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			1.425			µs
Clock frequency at I/O CLOCK (see Note 4)	TLC1543C		0		1.1	MHz
	TLC1543M		0		2.1	
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$			190			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$			190			ns
Transition time, I/O CLOCK, $t_{t(I/O)}$ (see Note 5)					1	µs
Transition time, ADDRESS and $\overline{CS}$, $t_{t(CS)}$					10	µs
Operating free-air temperature, T_A	TLV1543C		0		70	°C
	TLV1543M		−55		125	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF– convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.

3. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}$↓ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.
4. For 11- to 16-bit transfers, after the 10th I/O CLOCK falling edge (≤ 2 V), at least 1 I/O clock rising edge (≥ 2 V) must occur within 9.5 µs.
5. This is the time required for the clock input signal to fall from V_{IH}min to V_{IL}max or to rise from V_{IL}max to V_{IH}min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = V_{ref+} = 3 V to 5.5 V, I/O CLOCK frequency = 1.1 MHz for the TLV1543C, V_{CC} = V_{ref+} = 3 V to 3.6 V, I/O CLOCK frequency = 2.1 MHz for the TLV1543M (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	TLV1543C	V_{CC} = 3 V,	I_{OH} = −1.6 mA	2.4			V
			V_{CC} = 3 V to 5.5 V,	I_{OH} = 20 μA	V_{CC}−0.1			V
		TLV1543M	V_{CC} = 3 V,	I_{OH} = −1.6 mA	2.4			V
			V_{CC} = 3 V to 3.6 V,	I_{OH} = 20 μA	V_{CC}−0.1			V
V_{OL}	Low-level output voltage	TLV1543C	V_{CC} = 3 V,	I_{OL} = 1.6 mA			0.4	V
			V_{CC} = 3 V to 5.5 V,	I_{OL} = 20 μA			0.1	V
		TLV1543M	V_{CC} = 3 V,	I_{OL} = 1.6 mA			0.4	V
			V_{CC} = 3 V to 3.6 V,	I_{OL} = 20 μA			0.1	V
I_{OZ}	Off-state (high-impedance-state) output current		V_O = V_{CC},	$\overline{CS}$ at V_{CC}			10	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		V_I = V_{CC}			0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0			−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			0.8	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC},	Unselected channel at 0 V			1	μA
			Selected channel at 0 V,	Unselected channel at V_{CC}			−1	
	Maximum static analog reference current into REF+		V_{ref+} = V_{CC},	V_{ref-} = GND			10	μA
C_i	Input capacitance, Analog inputs	TLV1543C				7	55	pF
		TLV1543M				7		
	Input capacitance, Control inputs	TLV1543C				5	15	pF
		TLV1543M				5		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 3 V to 5.5 V, I/O CLOCK frequency = 1.1 MHz for the TLV1543C, $V_{CC} = V_{ref+}$ = 3 V to 3.6 V, I/O CLOCK frequency = 2.1 MHz for the TLV1543M

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Linearity error (see Note 6)				±1	LSB
	Zero error (see Note 7)	See Note 2			±1	LSB
	Full-scale error (see Note 7)	See Note 2			±1	LSB
	Total unadjusted error (see Note 8)				±1	LSB
	Self-test output code (see Table 3 and Note 9)	ADDRESS = 1011		512		
		ADDRESS = 1100		0		
		ADDRESS = 1101		1023		
t_{conv}	Conversion time	See timing diagrams			21	µs
t_c	Total cycle time (access, sample, and conversion)	See timing diagrams and Note 10			21 +10 I/O CLOCK periods	µs
t_{acq}	Channel acquisition time (sample)	See timing diagrams and Note 10			6	I/O CLOCK periods
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 6	10			ns
$t_{d(I/O-DATA)}$	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 6			240	ns
$t_{d(I/O-EOC)}$	Delay time, 10th I/O CLOCK↓ to EOC↓	See Figure 7		70	240	ns
$t_{d(EOC-DATA)}$	Delay time, EOC↑ to DATA OUT (MSB)	See Figure 8			100	ns
t_{PZH}, t_{PZL}	Enable time, $\overline{CS}$↓ to DATA OUT (MSB driven)	See Figure 3			1.3	µs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{CS}$↑ to DATA OUT (high impedance)	See Figure 3			150	ns
$t_{r(EOC)}$	Rise time, EOC	See Figure 8			300	ns
$t_{f(EOC)}$	Fall time, EOC	See Figure 7			300	ns
$t_{r(bus)}$	Rise time, data bus	See Figure 6			300	ns
$t_{f(bus)}$	Fall time, data bus	See Figure 6			300	ns
$t_{d(I/O-CS)}$	Delay time, 10th I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion (see Note 11)				9	µs

† All typical values are at T_A = 25°C.

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF– convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.

6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Zero error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
8. Total unadjusted error comprises linearity, zero, and full-scale errors.
9. Both the input address and the output codes are expressed in positive logic.
10. I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 6).
11. Any transitions of $\overline{CS}$ are recognized as valid only if the level is maintained for a setup time plus two falling edges of the internal clock (1.425 µs) after the transition.

PARAMETER MEASUREMENT INFORMATION

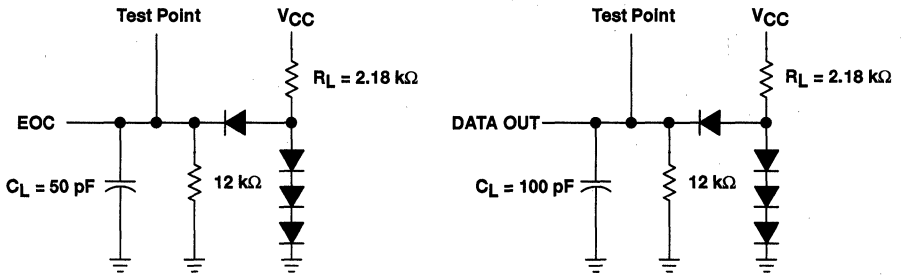


Figure 2. Load Circuits

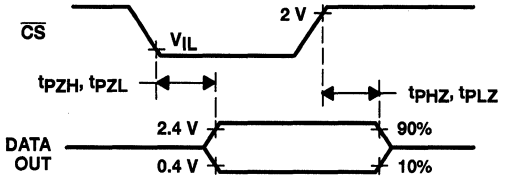


Figure 3. DATA OUT to Hi-Z Voltage Waveforms

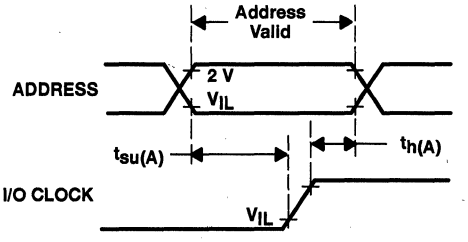


Figure 4. ADDRESS Setup Voltage Waveforms

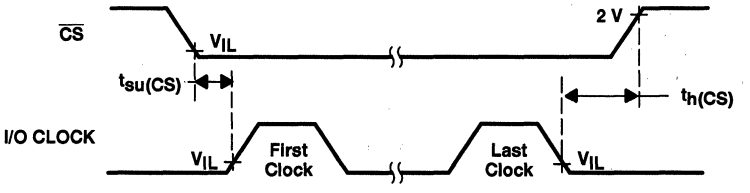


Figure 5. $\overline{CS}$ and I/O CLOCK Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

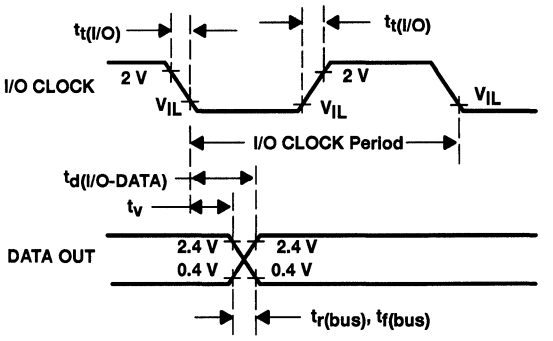


Figure 6. DATA OUT and I/O CLOCK Voltage Waveforms

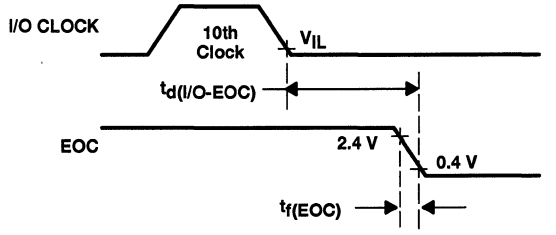


Figure 7. I/O CLOCK and EOC Voltage Waveforms

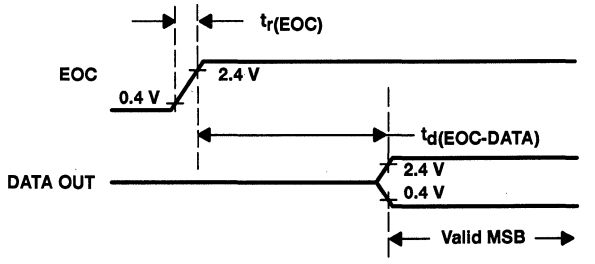


Figure 8. EOC and DATA OUT Voltage Waveforms

timing diagrams

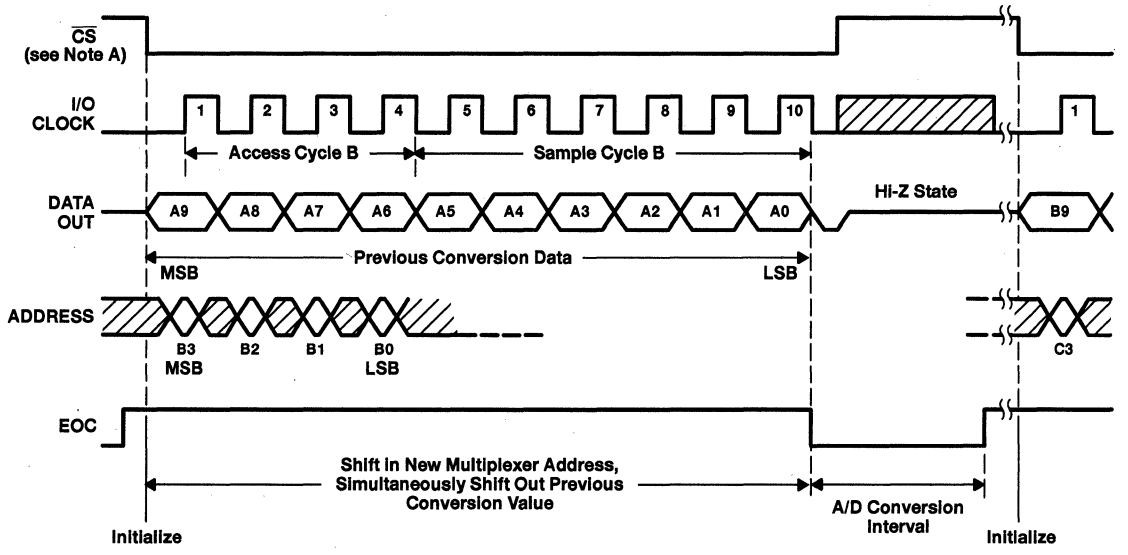


Figure 9. Timing for 10-Clock Transfer Using $\overline{CS}$

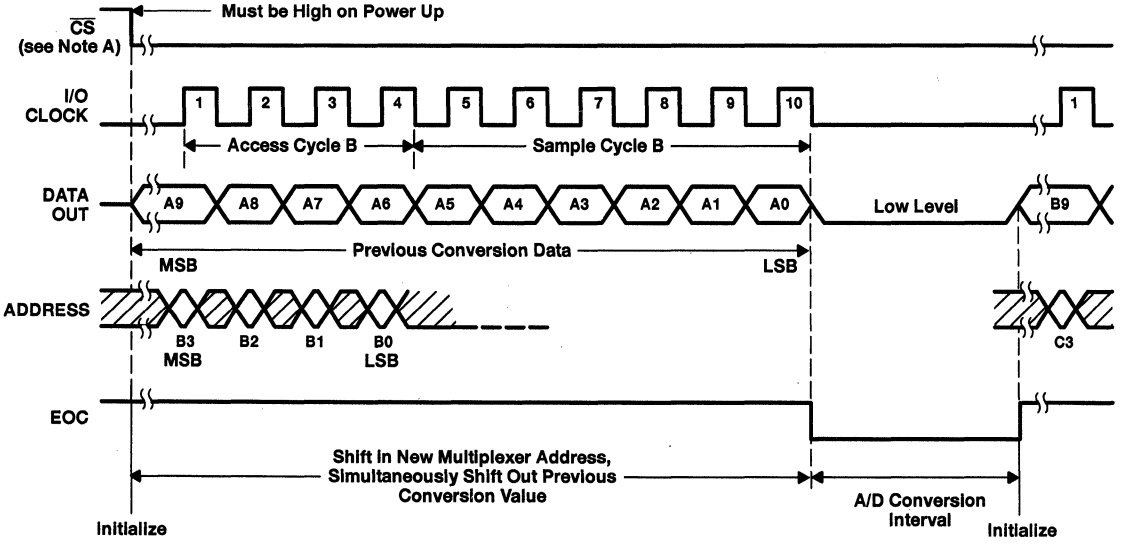


Figure 10. Timing for 10-Clock Transfer Not Using $\overline{CS}$

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

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timing diagrams (continued)

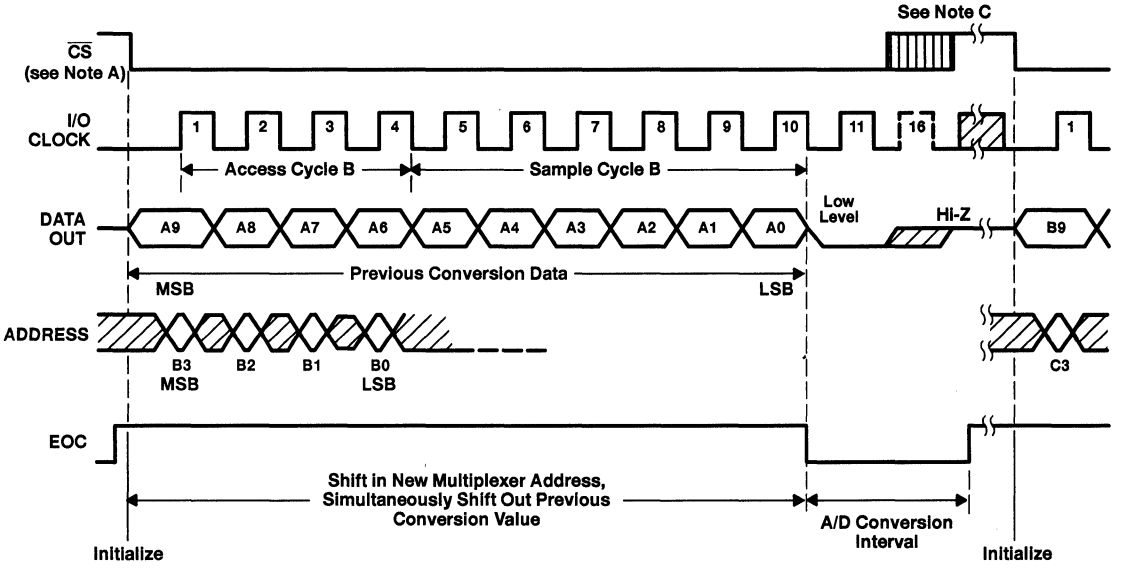


Figure 11. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Interval Shorter Than Conversion)

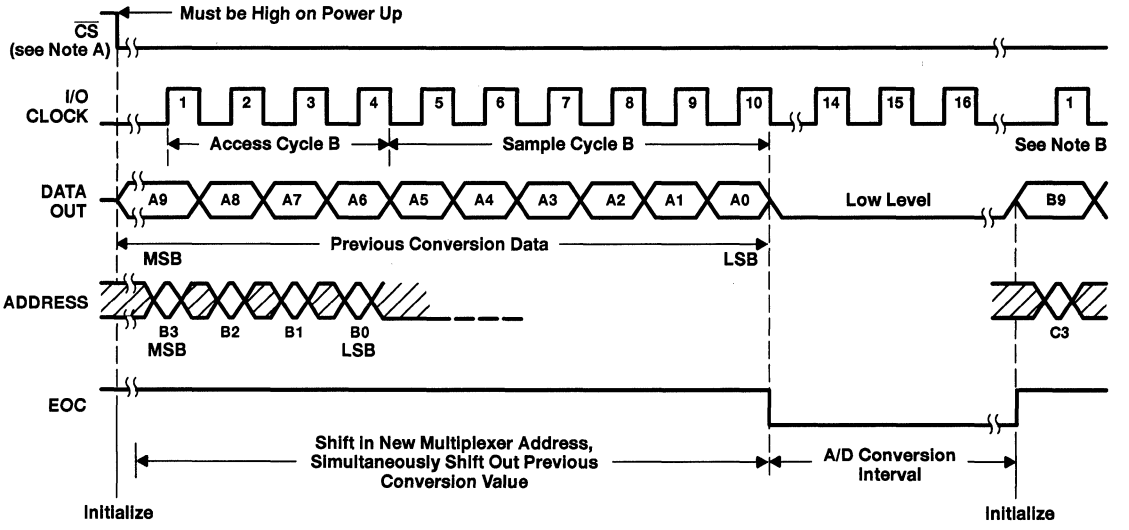


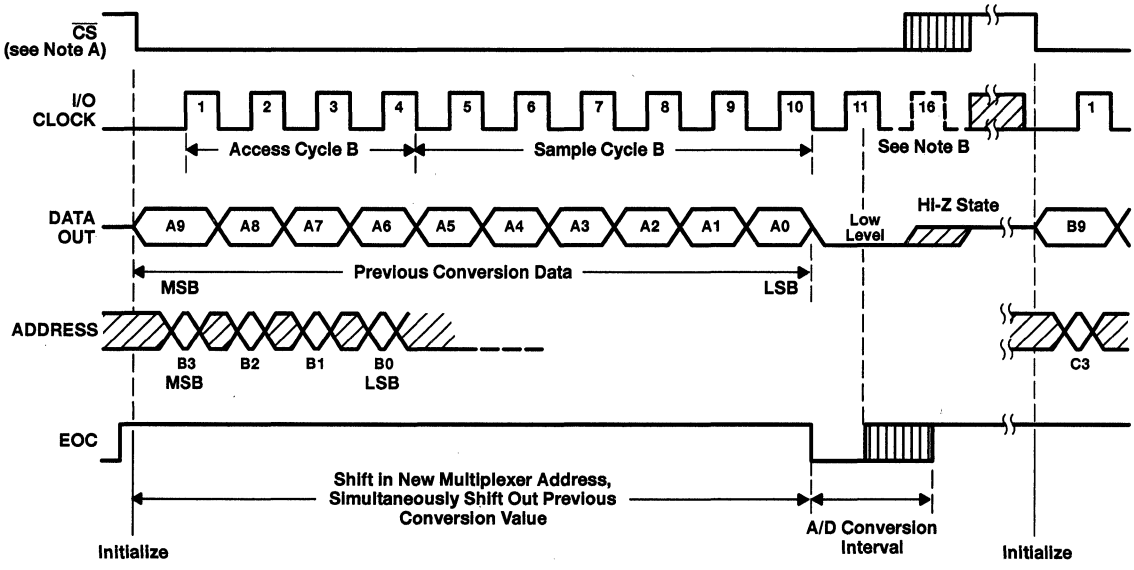
Figure 12. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Interval Shorter Than Conversion)

NOTES: A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set up time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

B. The first I/O CLOCK must occur after the rising edge of EOC.

C. A low-to-high transition of $\overline{CS}$ disables ADDRESS and the I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

timing diagrams (continued)

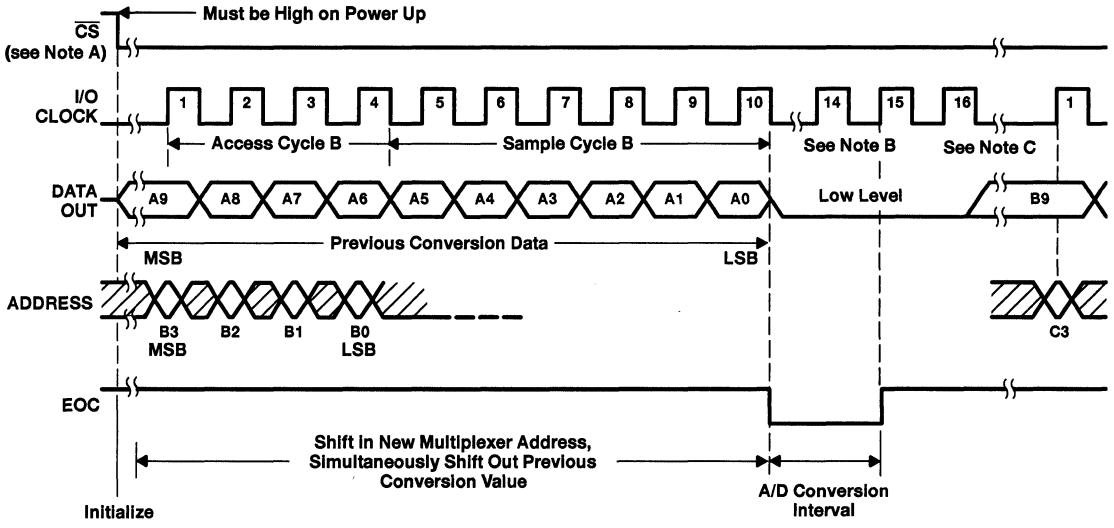


NOTES: A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set up time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

B. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.

Figure 13. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Interval Longer Than Conversion)

timing diagrams (continued)



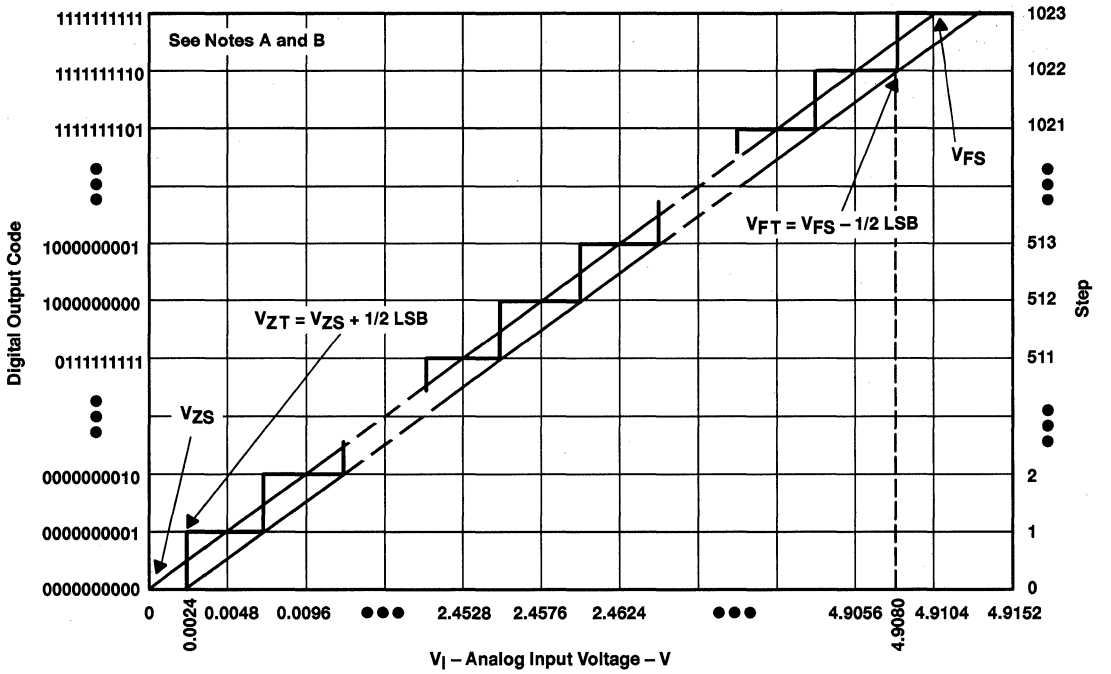
NOTES: A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set up time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum chip $\overline{CS}$ setup time has elapsed.

B. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.

C. The I/O CLOCK sequence is exactly 16 clock pulses long.

Figure 14. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Interval Longer Than Conversion)

APPLICATION INFORMATION



NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0024 V and the transition to full scale (V_{FT}) is 4.908 V. 1 LSB = 4.8 mV.

B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 15. Ideal Conversion Characteristics

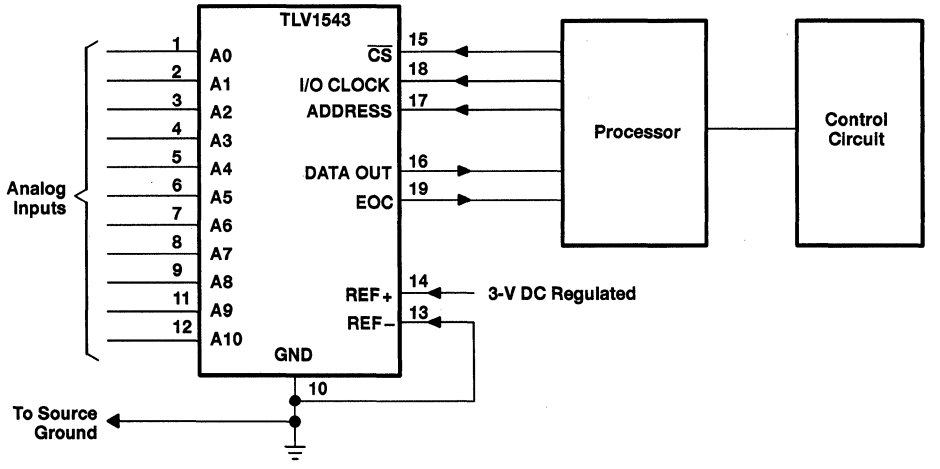


Figure 16. Serial Interface

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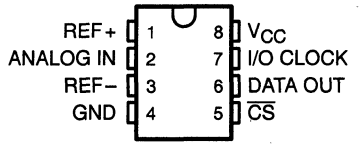
- **Advanced LinEPIC™ Technology**
- **3.3-V Supply Operation**
- **10-Bit-Resolution A/D Converter**
- **Inherent Sample and Hold**
- **Total Unadjusted Error . . . ±1 LSB Max**
- **On-Chip System Clock**
- **Pin Compatible With TLC1549**

D OR P PACKAGE
(TOP VIEW)



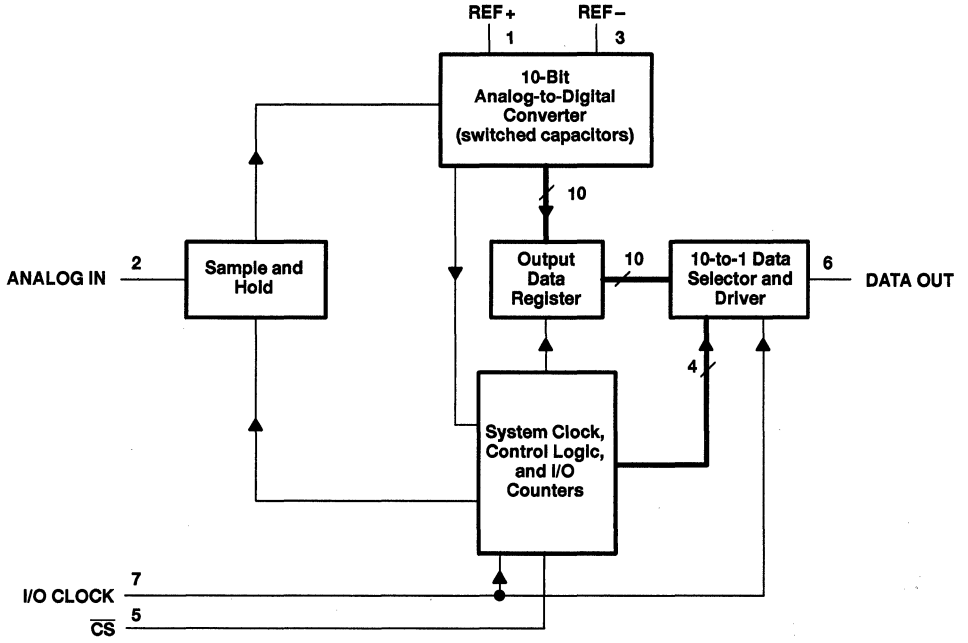
description

The TLV1549C is a 10-bit, switched-capacitor, successive-approximation analog-to-digital converter. The device has two digital inputs and a 3-state output [chip select ($\overline{CS}$), input-output clock (I/O CLOCK), and data output (DATA OUT)] that provide a three-wire interface to the serial port of a host processor.

The sample-and-hold function is automatic. The converter incorporated in the device features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

The TLV1549C is characterized for operation from 0°C to 70°C.

functional block diagram



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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ANALOG IN	2	I	Analog signal. The driving source impedance should be ≤ 1 kΩ. The external driving source to ANALOG IN should have a current capability ≥ 10 mA.
$\overline{CS}$	5	I	Chip select. A high-to-low transition on this input resets the internal counters and controls and enables DATA OUT and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OUT	6	O	This 3-state serial output for the A/D conversion result is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives this output to the logic level corresponding to the next most significant bit, and the remaining bits are shifted out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs.
GND	4	I	The ground return for internal circuitry. Unless otherwise noted, all voltage measurements are with respect to this terminal.
I/O CLOCK	7	I	The input/output clock receives the serial I/O CLOCK input and performs the following three functions: 1) On the third falling edge of I/O CLOCK, the analog input voltage begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 2) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 3) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF+	1	I	The upper reference voltage value (nominally V_{CC}) is applied to this terminal. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to REF–.
REF–	3	I	The lower reference voltage value (nominally ground) is applied to this terminal.
V_{CC}	8	I	Positive supply voltage

detailed description

With chip select ($\overline{CS}$) inactive (high), the I/O CLOCK input is initially disabled and DATA OUT is in the high-impedance state. When the serial interface takes $\overline{CS}$ active (low), the conversion sequence begins with the enabling of I/O CLOCK and the removal of DATA OUT from the high-impedance state. The serial interface then provides the I/O CLOCK sequence to I/O CLOCK and receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host serial interface. The first ten I/O clocks provide the control timing for sampling the analog input.

There are six basic serial interface timing modes that can be used with the TLV1549. These modes are determined by the speed of I/O CLOCK and the operation of $\overline{CS}$ as shown in Table 1. These modes are (1) a fast mode with a 10-clock transfer and $\overline{CS}$ inactive (high) between transfers, (2) a fast mode with a 10-clock transfer and $\overline{CS}$ active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and $\overline{CS}$ inactive (high) between transfers, (4) a fast mode with a 16-bit transfer and $\overline{CS}$ active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and $\overline{CS}$ inactive (high) between transfers, and (6) a slow mode with a 16-clock transfer and $\overline{CS}$ active (low) continuously.

The MSB of the previous conversion appears on DATA OUT on the falling edge of $\overline{CS}$ in mode 1, mode 3, and mode 5, within 21 µs from the falling edge of the tenth I/O CLOCK in mode 2 and mode 4, and following the 16th clock falling edge in Mode 6. The remaining nine bits are shifted out on the next nine falling edges of the I/O CLOCK. Ten bits of data are transmitted to the host serial interface through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the tenth clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLOCK transfer is more than ten clocks long.

detailed description (continued)

Table 1 lists the operational modes with respect to the state of $\overline{CS}$, the number of I/O serial transfer clocks that can be used, and the timing on which the MSB of the previous conversion appears at the output.

Table 1. Mode Operation

MODES		$\overline{CS}$	NO. OF I/O CLOCKS	MSB AT DATA OUT†	TIMING DIAGRAM
Fast Modes	Mode 1	High between conversion cycles	10	$\overline{CS}$ falling edge	Figure 6
	Mode 2	Low continuously	10	Within 21 μs	Figure 7
	Mode 3	High between conversion cycles	11 to 16‡	$\overline{CS}$ falling edge	Figure 8
	Mode 4	Low continuously	16‡	Within 21 μs	Figure 9
Slow Modes	Mode 5	High between conversion cycles	11 to 16‡	$\overline{CS}$ falling edge	Figure 10
	Mode 6	Low continuously	16‡	16th clock falling edge	Figure 11

† This timing also initiates serial interface communication.
‡ No more than 16 clocks should be used.

All the modes require a minimum period of 21 μs after the falling edge of the 10th I/O CLOCK before a new transfer sequence can begin. During a serial I/O CLOCK data transfer, $\overline{CS}$ must be active (low) so that the I/O CLOCK input is enabled. When $\overline{CS}$ is toggled between data transfers (modes 1, 3, and 5), the transitions at $\overline{CS}$ are recognized as valid only if the level is maintained for a minimum period of 1.425 μs after the transition. If the transfer is more than 10 I/O clocks (modes 3, 4, 5, and 6), the rising edge of the 11th clock must occur within 9.5 μs after the falling edge of the 10th I/O CLOCK; otherwise, the device could lose synchronization with the host serial interface and $\overline{CS}$ has to be toggled to restore proper operation.

fast modes

The device is in a fast mode when the serial I/O CLOCK data transfer is completed within 21 μs from the falling edge of the tenth I/O CLOCK. With a 10-clock serial transfer, the device can only run in a fast mode.

mode 1: fast mode, $\overline{CS}$ inactive (high) between transfers, 10-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O-CLOCK transfers, and each transfer is ten clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 2: fast mode, $\overline{CS}$ active (low) continuously, 10-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O-CLOCK transfers and each transfer is 10 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions. Within 21 μs after the falling edge of the 10th I/O CLOCK, the MSB of the previous conversion appears at DATA OUT.

mode 3: fast mode, $\overline{CS}$ inactive (high) between transfers, 11- to 16-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O-CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 4: fast mode, $\overline{CS}$ active (low) continuously, 16-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O-CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions. Within 21 μs after the falling edge of the tenth I/O CLOCK, the MSB of the previous conversion appears at DATA OUT.

slow modes

In a slow mode, the serial I/O CLOCK data transfer is completed after 21 µs from the falling edge of the 10th I/O CLOCK.

mode 5: slow mode, $\overline{CS}$ active (high) between transfers, 11- to 16-clock transfer

In this mode, $\overline{CS}$ is active (high) between serial I/O-CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 6: slow mode, $\overline{CS}$ active (low) continuously, 16-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O-CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions. The falling edge of the 16th I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16-clock transfer initiated by the serial interface.

analog input sampling

Sampling of the analog input starts on the falling edge of the third I/O CLOCK, and sampling continues for seven I/O CLOCK periods. The sample is held on the falling edge of the tenth I/O CLOCK.

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and this 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are determined.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.

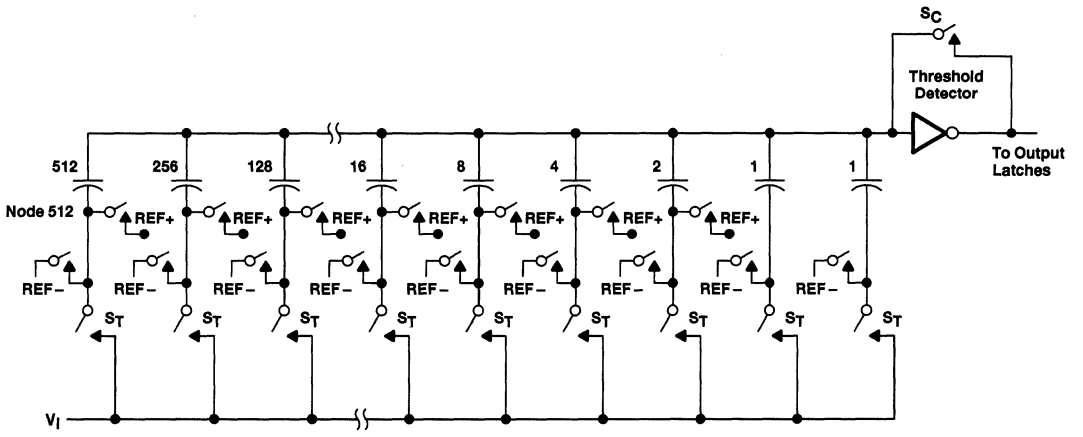

Figure 1. Simplified Model of the Successive-Approximation System

chip-select operation

The trailing edge of $\overline{CS}$ starts all modes of operation, and $\overline{CS}$ can abort a conversion sequence in any mode. A high-to-low transition on $\overline{CS}$ within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Exercise care to prevent $\overline{CS}$ from being taken low close to completion of conversion because the output data may be corrupted.

reference voltage inputs

There are two reference inputs used with the TLV1549: REF+ and REF–. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading, respectively. The values of REF+, REF–, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF–.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.5 V to 6.5 V
Input voltage range, V_I (any input)	−0.3 V to V_{CC} + 0.3 V
Output voltage range	−0.3 V to V_{CC} + 0.3 V
Positive reference voltage, V_{ref+}	V_{CC} + 0.1 V
Negative reference voltage, V_{ref-}	−0.1 V
Peak input current (any input)	±20 mA
Peak total input current (all inputs)	±30 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to ground with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Positive reference voltage, V_{ref+} (see Note 2)			V_{CC}		V
Negative reference voltage, V_{ref-} (see Note 2)			0		V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)		2.5	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)		0		V_{CC}	V
High-level control input voltage, V_{IH}	V_{CC} = 3 V to 3.6 V	2			V
Low-level control input voltage, V_{IL}	V_{CC} = 3 V to 3.6 V			0.6	V
Clock frequency at I/O CLOCK (see Note 3)		0		2.1	MHz
Setup time, $\overline{CS}$ low before first I/O CLOCK↑, $t_{su(CS)}$ (see Note 4)		1.425			µs
Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_{h(CS)}$		0			ns
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$		190			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$		190			ns
Transition time, I/O CLOCK, $t_{t(I/O)}$ (see Note 5 and Figure 5)				1	µs
Transition time, $\overline{CS}$, $t_{t(CS)}$				10	µs
Operating free-air temperature, T_A		0		70	°C

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF– convert as all zeros (0000000000). The TLV1549 is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.

3. For 11- to 16-bit transfers, after the tenth I/O CLOCK falling edge (≤ 2 V), at least one I/O CLOCK rising edge (≥ 2 V) must occur within 9.5 µs.

4. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}$↓ before responding to the I/O CLOCK. Therefore, no attempt should be made to clock out the data until the minimum $\overline{CS}$ setup time has elapsed.

5. This is the time required for the clock input signal to fall from V_{IH}min to V_{IL}max or to rise from V_{IL}max to V_{IH}min. In the vicinity of normal room temperature, the device functions with input clock transition time as slow as 1 µs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 3 V to 3.6 V, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 3 V,	I_{OH} = –1.6 mA	2.4			V
			V_{CC} = 3 V to 3.6 V,	I_{OH} = –20 µA	V_{CC}–0.1			
V_{OL}	Low-level output voltage		V_{CC} = 3 V,	I_{OL} = 1.6 mA			0.4	V
			V_{CC} = 3 V to 3.6 V,	I_{OL} = 20 µA			0.1	
I_{OZ}	Off-state (high-impedance-state) output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}			10	µA
			V_O = 0,	$\overline{CS}$ at V_{CC}			–10	
I_{IH}	High-level input current		$V_I = V_{CC}$			0.005	2.5	µA
I_{IL}	Low-level input current		V_I = 0			–0.005	–2.5	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			0.4	2.5	mA
	Analog input leakage current		$V_I = V_{CC}$				1	µA
			V_I = 0				–1	
	Maximum static analog reference current into REF+		$V_{ref+} = V_{CC}$,	V_{ref-} = GND			10	µA
C_i	Input capacitance	Analog input	During sample cycle			30	55	pF
		Control inputs				5	15	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 3$ V to 3.6 V, I/O CLOCK frequency = 2.1 MHz

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
	Linearity error (see Note 6)			±1	LSB
	Zero error (see Note 7)	See Note 2		±1	LSB
	Full-scale error (see Note 7)	See Note 2		±1	LSB
	Total unadjusted error (see Note 8)			±1	LSB
t_{conv}	Conversion time	See timing diagrams		21	µs
t_c	Total cycle time (access, sample, and conversion)	See timing diagrams and Note 9		21 +10 I/O CLOCK periods	µs
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 5	10		ns
$t_{d(I/O-DATA)}$	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 5		240	ns
t_{PZH}, t_{PZL}	Enable time, $\overline{CS}$↓ to DATA OUT (MSB driven)	See Figure 3		1.3	µs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{CS}$↑ to DATA OUT (high impedance)	See Figure 3		180	ns
$t_{r(bus)}$	Rise time, data bus	See Figure 5		300	ns
$t_{f(bus)}$	Fall time, data bus	See Figure 5		300	ns
$t_{d(I/O-CS)}$	Delay time, 10th I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion (see Note 10)			9	µs

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF– convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.

6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Zero error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
8. Total unadjusted error comprises linearity, zero, and full-scale errors.
9. I/O CLOCK period = 1/(I/O CLOCK frequency). Sampling begins on the falling edge of the third I/O CLOCK, continues for seven I/O CLOCK periods, and ends on the falling edge of the tenth I/O CLOCK (see Figure 5).
10. Any transitions of $\overline{CS}$ are recognized as valid only if the level is maintained for a minimum of a setup time plus two falling edges of the internal clock (1.425 µs) after the transition.

PARAMETER MEASUREMENT INFORMATION

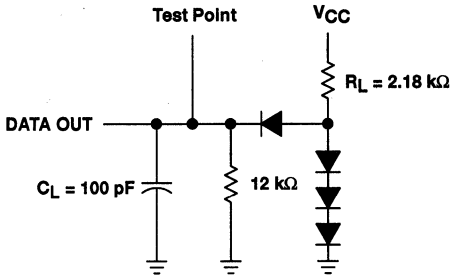

Figure 2. Load Circuit

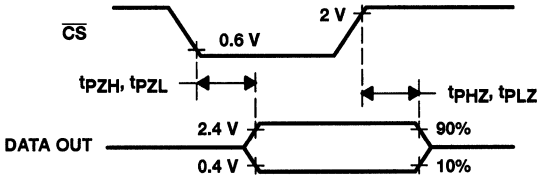

Figure 3. DATA OUT to Hi-Z Voltage Waveforms

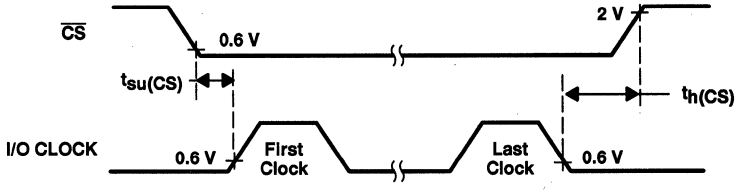

Figure 4. $\overline{CS}$ to I/O CLOCK Voltage Waveforms

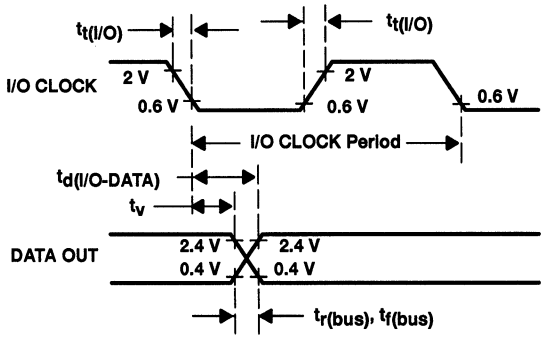

Figure 5. I/O CLOCK and DATA OUT Voltage Waveforms

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timing diagrams

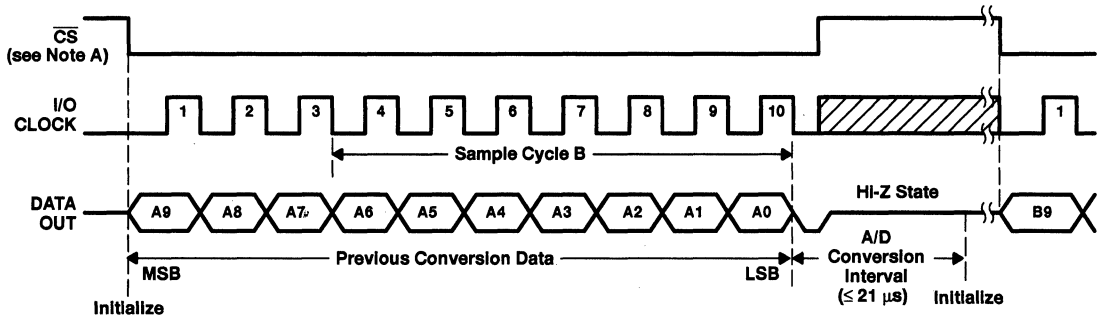


Figure 6. Timing for 10-Clock Transfer Using $\overline{CS}$

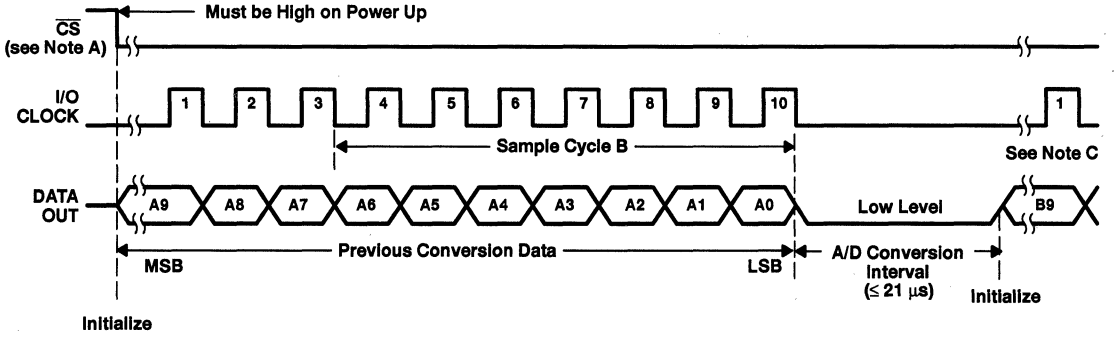


Figure 7. Timing for 10-Clock Transfer Not Using $\overline{CS}$

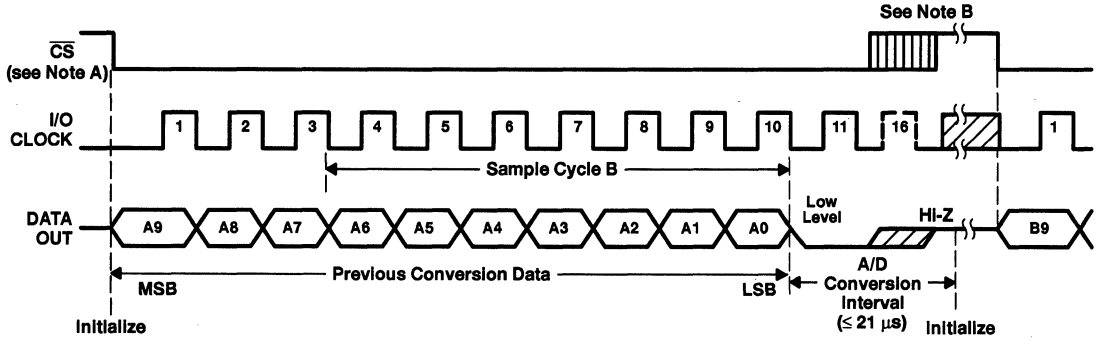


Figure 8. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Completed Within 21 µs)

NOTES: A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to the I/O CLOCK. Therefore, no attempt should be made to clock out the data until the minimum $\overline{CS}$ setup time has elapsed.

B. A low-to-high transition of $\overline{CS}$ disables I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

C. The first I/O CLOCK must occur after the end of the previous conversion.

timing diagrams (continued)

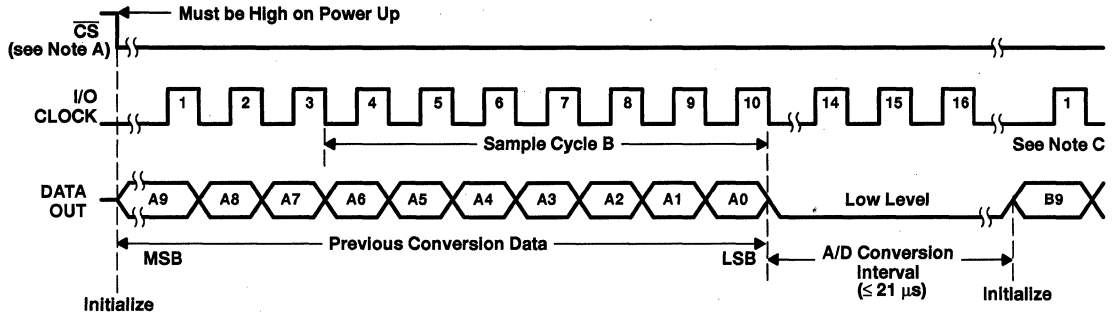


Figure 9. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Completed Within 21 μs)

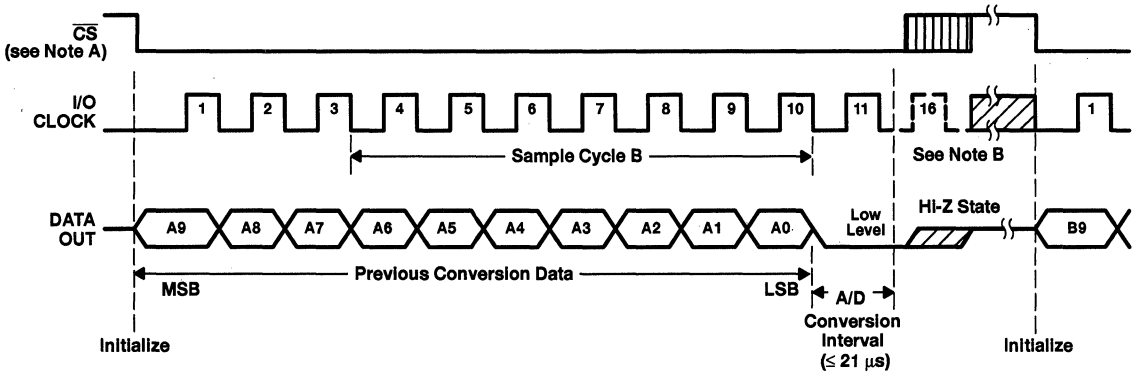


Figure 10. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Completed After 21 μs)

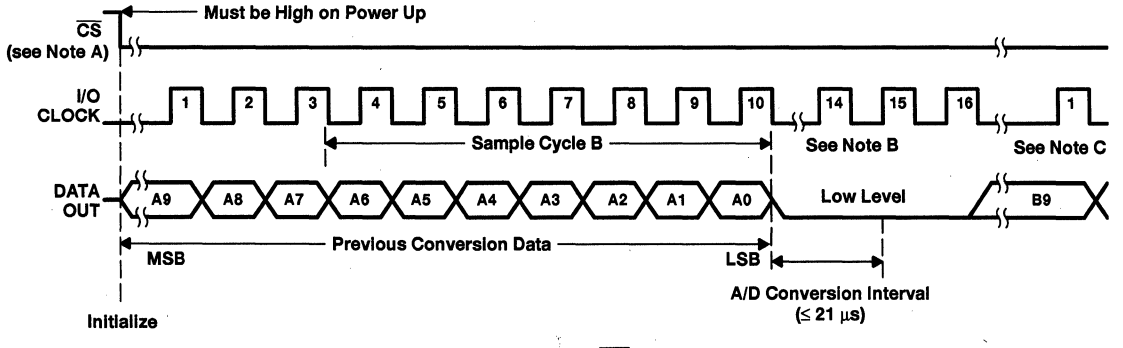


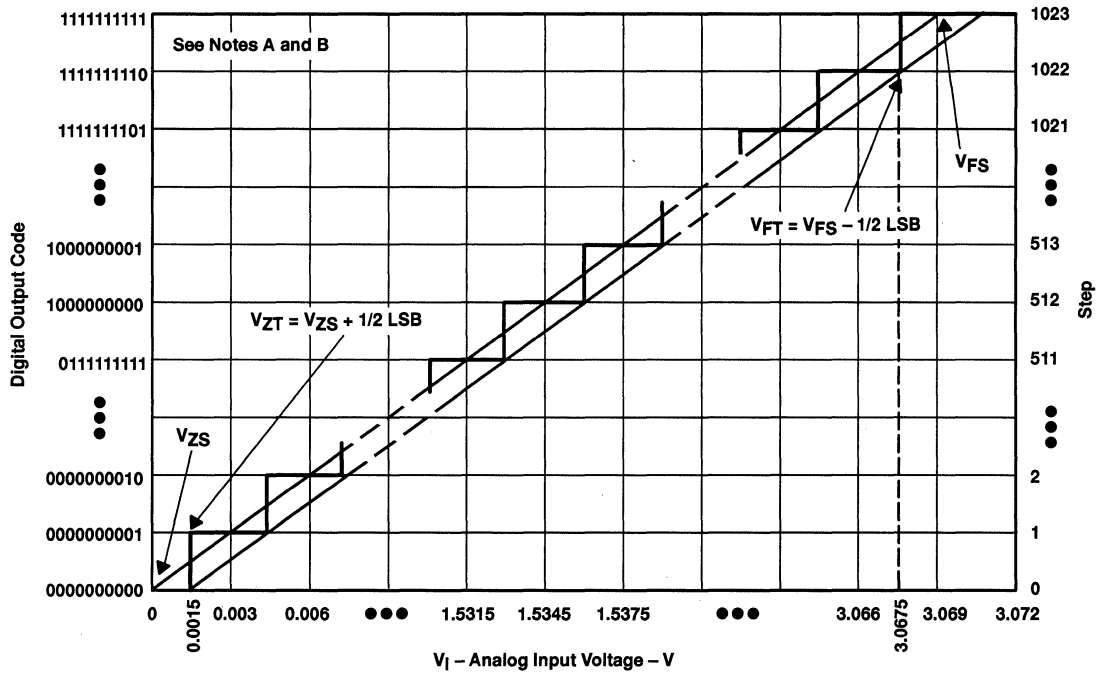
Figure 11. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Completed After 21 μs)

NOTES: A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set up time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to the I/O CLOCK. Therefore, no attempt should be made to clock out the data until the minimum $\overline{CS}$ setup time has elapsed.

B. A low-to-high transition of $\overline{CS}$ disables I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

C. The first I/O CLOCK must occur after the end of the previous conversion.

APPLICATION INFORMATION



NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0015 V and the transition to full scale (V_{FT}) is 3.0675 V. 1 LSB = 3 mV.

B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 12. Ideal Conversion Characteristics

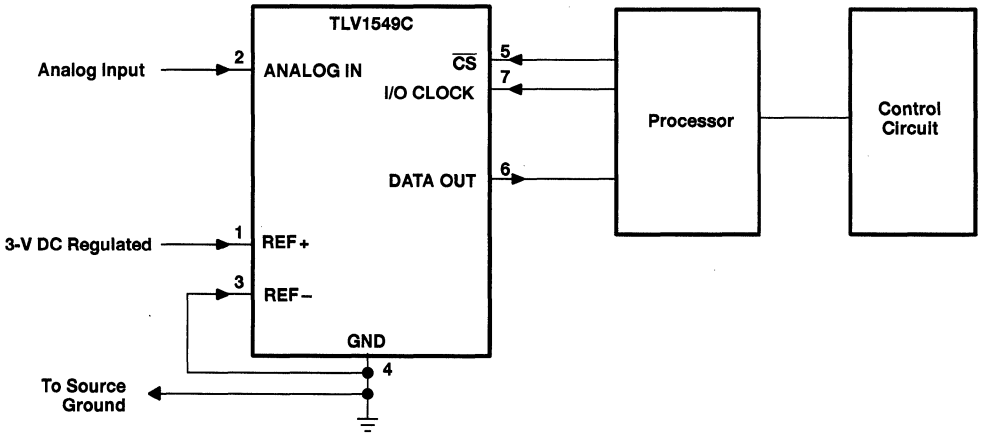
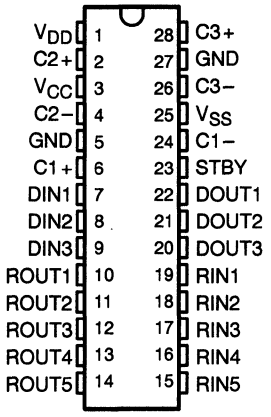


Figure 13. Typical Serial Interface

SLLS135D – FEBRUARY 1992 – REVISED FEBRUARY 1994

- **Meets ANSI/EIA-232-D-1986 Specifications (Revision of EIA Standard RS-232-C)**
- **Operates With Single 3.3-V Power Supply**
- **LinBiCMOS™ Process Technology**
- **Three Drivers and Five Receivers**
- **±30-V Input Levels (Receiver)**
- **ESD Protection on RS-232 Lines Exceeds 6 kV Per MIL-STD-883C, Method 3015**
- **Applications**
  - **EIA-232 Interface**
  - **Battery-Powered Systems**
  - **Notebook PC**
  - **Computers**
  - **Terminals**
  - **Modems**
- **Voltage Converter Operates With Low Capacitance . . . 0.47 μF Min**

DB PACKAGE
(TOP VIEW)



description

The SN75LV4735† is a low-power 3.3-V multichannel RS232 line driver/receiver. It includes three independent RS232 drivers and five independent RS232 receivers. It is designed to operate off a single 3.3-V supply and has an internal switched-capacitor voltage converter to generate the RS232 output levels. The SN75LV4735 provides a single integrated circuit and single 3.3-V supply interface between the asynchronous communications element (ACE or UART) and the serial-port connector of the data terminal equipment (DTE). This device has been designed to conform to standard ANSI/EIA-232-D-1986.

The switched-capacitor voltage converter of the SN75LV4735 uses five small external capacitors to generate the positive and negative voltages required by EIA-232 line drivers from a single 3.3-V input. The drivers feature output slew-rate limiting to eliminate the need for external filter capacitors. The receivers can accept ±30 V without damage.

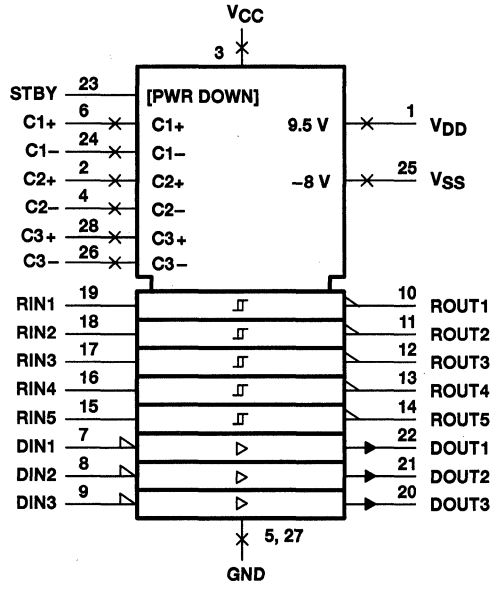
The device also features a reduced power or standby mode that cuts the quiescent power to the integrated circuits when not transmitting data between the CPU and peripheral equipment. The STBY input is driven high for standby (reduced power) mode and driven low for normal operating mode. When in the standby mode, all driver outputs (DOUT1–3) and receiver outputs (ROUT1–5) are in the high-impedance state. If the standby feature is not used in an application, STBY should be tied to GND.

The SN75LV4735 has been designed using LinBiCMOS™ technology and cells contained in the Texas Instruments LinASIC™ library. The SN75LV4735 is characterized for operation from 0°C to 70°C.

† Patent-pending design

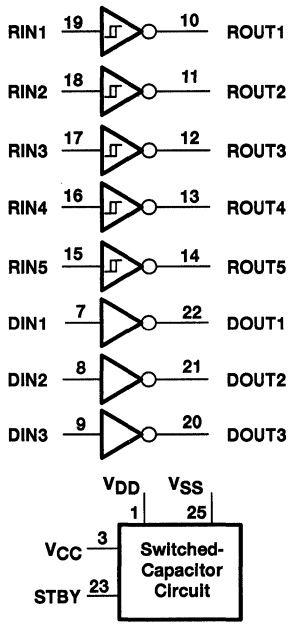
LinBiCMOS and LinASIC are trademarks of Texas Instruments Incorporated.

logic symbol†

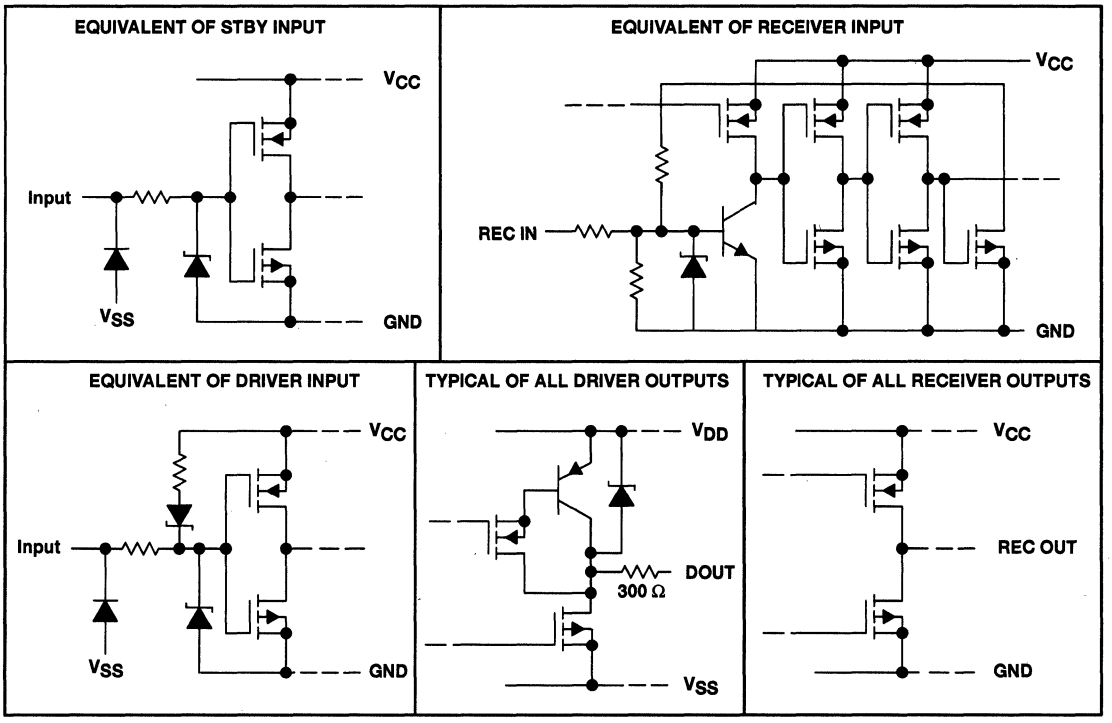


† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... 4 V
Positive output supply voltage, V_{DD} (see Note 1) ..... 15 V
Negative output supply voltage, V_{SS} ..... −15 V
Input voltage range, V_I: DIN1−DIN3, STBY ..... −0.3 to 7 V
RIN1−RIN5 ..... −30 V to 30 V
Output voltage range, V_O: DOUT1−DOUT3 ..... V_{SS} − 0.3 V to V_{DD} + 0.3 V
ROUT1−ROUT5 ..... −0.3 V to 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DB	668 mW	5.3 mW/°C	430 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Positive output supply voltage, V_{DD}		8	10		V
Negative output supply voltage, V_{SS}		−7	−8		V
Input voltage, V_I (see Note 2)	RIN1–5			±30	V
High-level input voltage, V_{IH}	DIN1–3, STBY	2			V
Low-level input voltage, V_{IL}	DIN1–3, STBY			0.8	V
External capacitor		0.47	1		µF
Operating free-air temperature, T_A		0		70	°C

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if −10 V is a maximum, the typical value is a more negative voltage.

supply currents

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current from V_{CC} (normal operating mode)	No load, STBY at 0 V, All other inputs open		8.5	20	mA
I_{CC}	Supply current (standby mode)	No load, STBY at V_{CC}, All other inputs open			10	µA

DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{CC} = 3.3 V ±0.3 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		R_L = 3 kΩ	5.5	7		V
V_{OL}	Low-level output voltage (see Note 2)		R_L = 3 kΩ	−5	−5.5		V
I_{IH}	High-level input current		V_I at V_{CC}			1	µA
I_{IL}	Low-level input current	STBY	V_I at GND			−1	µA
		Other inputs	V_I at GND			−10	µA
$I_{OS(H)}$	High-level short-circuit output current (see Note 3)		V_{CC} = 3.6 V, V_O = 0		−10	−20	mA
$I_{OS(L)}$	Low-level short-circuit output current (see Note 3)		V_{CC} = 3.6 V, V_O = 0		10	20	mA
r_o	Output resistance		V_{CC} = V_{DD} = V_{SS} = 0, V_O = −2 V to 2 V, See Note 4	300			Ω

NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.
3. Not more than one output should be shorted at one time.
4. Test conditions are those specified by EIA-232-D.

switching characteristics, V_{CC} = 3.3 V ±0.3 V, T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 3 kΩ to GND, C_L = 50 pF, See Figure 2	200	400	600	ns
t_{PHL}	Propagation delay time, high-to-low-level output		100	200	350	ns
t_{PZL}	Output enable time to low level (see Note 5)	R_L = 3 kΩ to GND, C_L = 50 pF, See Figure 3		3	7	ms
t_{PZH}	Output enable time to high level (see Note 5)			1	5	ms
t_{PHZ}	Output disable time from high level (see Note 5)			1	3	µs
t_{PLZ}	Output disable time from low level (see Note 5)			0.5	3	µs
SR	Output slew rate (see Note 6)	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF, See Figure 2	3		30	V/µs
SR(tr)	Transition region slew rate	R_L = 3 kΩ to GND, C_L = 2500 pF, See Figure 4		3		V/µs

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTES: 5. Output enable occurs when STBY is driven low. Output disable occurs when STBY is driven high.
6. Measured between 3-V and −3-V points of output waveform (EIA-232-D conditions); all unused inputs are tied either high or low.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			2.2	2.6	V
V_{IT-}	Negative-going input threshold voltage		0.6	1		V
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)		0.5	1.2	1.8	V
V_{OH}	High-level output voltage	I_{OH} = −2 mA, See Note 7	2.4	2.6		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA		0.2	0.4	V
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

NOTE 7: If the inputs are left unconnected, the receiver interprets this as an input low, and the receiver outputs remains in the high state.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 3 kΩ to GND, See Figure 5	45	80	130	ns
t_{PHL}	Propagation delay time, high-to-low-level output		70	100	170	ns
t_{PZL}	Output enable time to low level (see Note 5)	R_L = 3 kΩ to GND, See Figure 6		160	250	ns
t_{PZH}	Output enable time to high level (see Note 5)			4	10	µs
t_{PHZ}	Output disable time from high level (see Note 5)			300	500	ns
t_{PLZ}	Output disable time from low level (see Note 5)			140	200	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
NOTE 5: Output enable occurs when STBY is driven low. Output disable occurs when STBY input is driven high.

APPLICATION INFORMATION

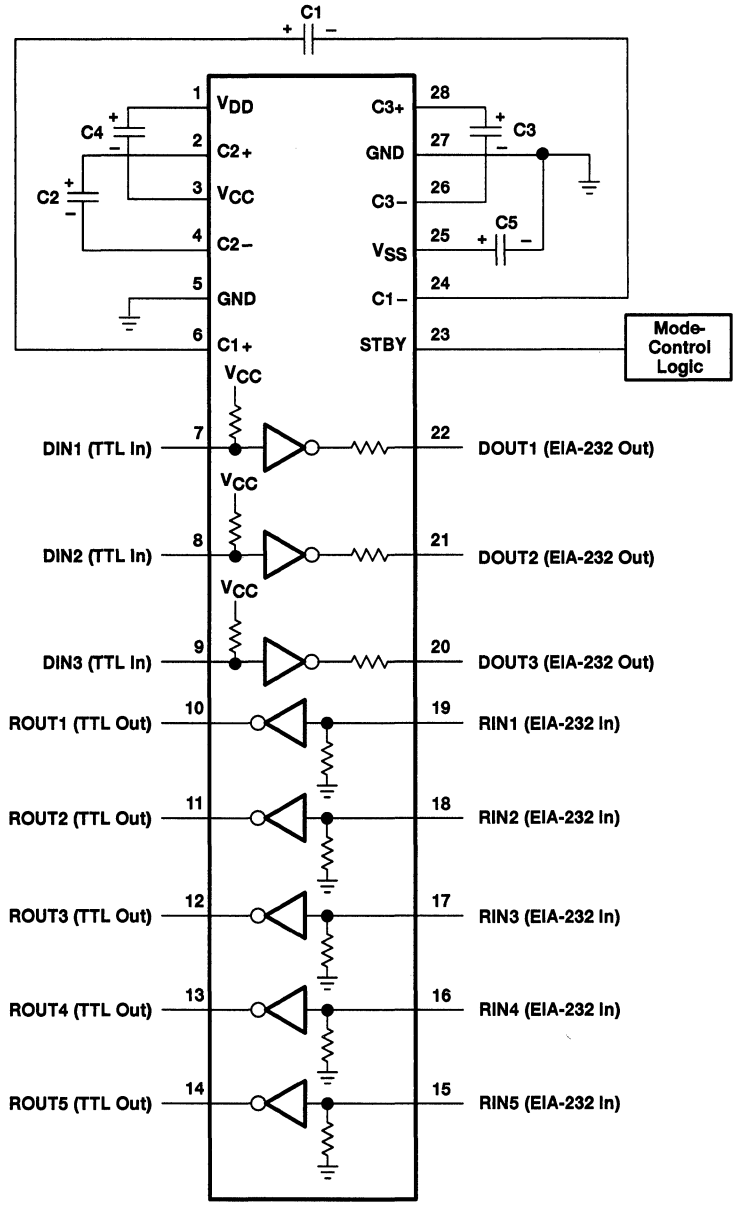
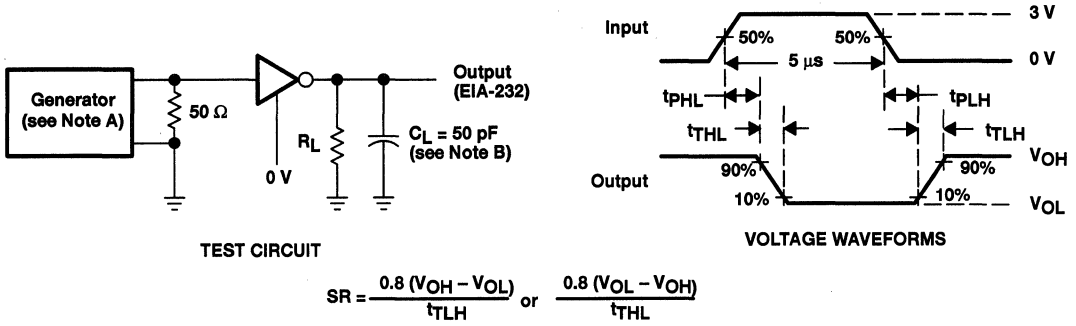


Figure 1. Typical Operating Circuit

PARAMETER MEASUREMENT INFORMATION



$$SR = \frac{0.8\,(V_{OH} - V_{OL})}{t_{TLH}} \text{ or } \frac{0.8\,(V_{OL} - V_{OH})}{t_{THL}}$$

Figure 2. Driver Test Circuit and Voltage Waveforms, Slew Rate at 5-μs Input

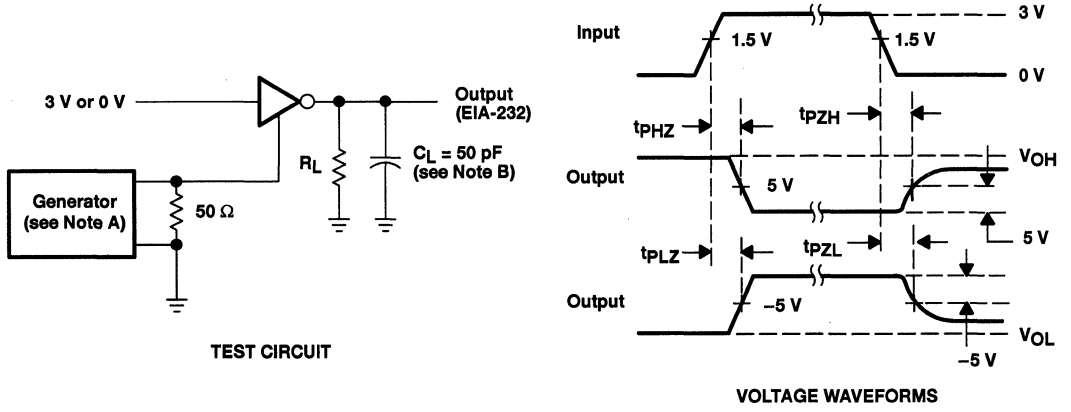
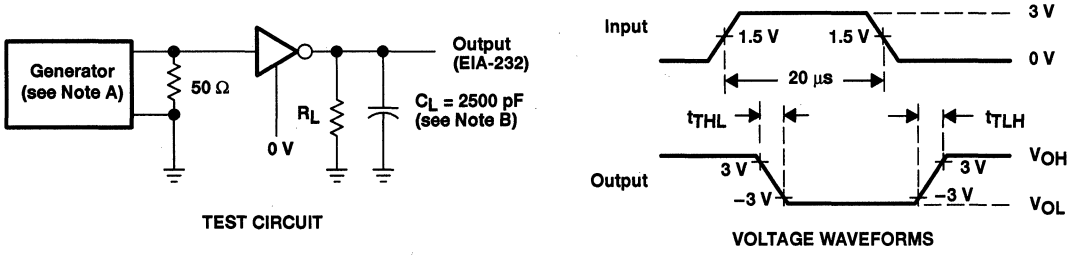


Figure 3. Driver Test Circuit and Voltage Waveforms



$$SR = \frac{6\text{ V}}{t_{THL} \text{ or } t_{TLH}}$$

Figure 4. Driver Test Circuit and Voltage Waveforms, Slew Rate at 20-μs Input

NOTES: A. The pulse generator has the following characteristics: 50% duty cycle, $t_r \le 10$ ns, $t_f = 10$ ns.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

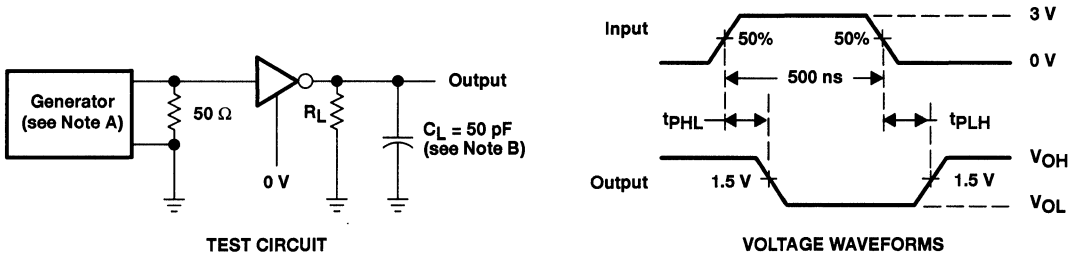


Figure 5. Receiver Test Circuit and Voltage Waveforms

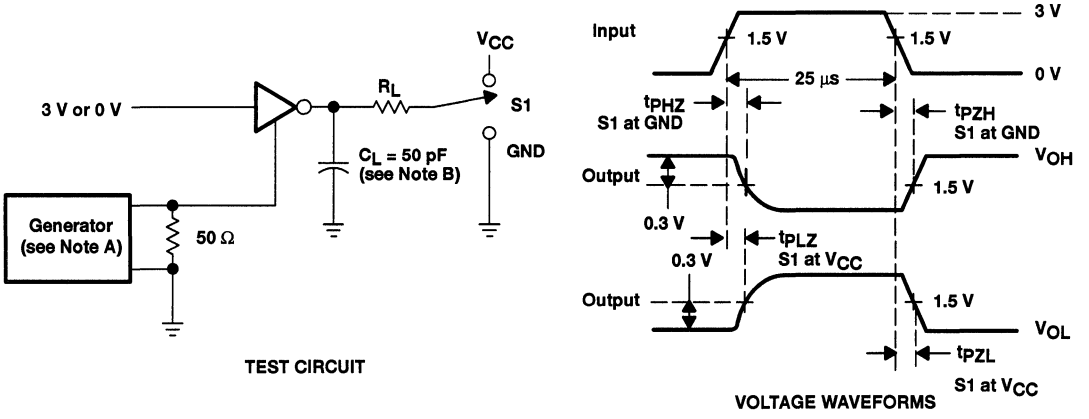


Figure 6. Receiver Test Circuit and Voltage Waveforms Enable and Disable Times

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f = 10$ ns.
B. C_L includes probe and jig capacitance.

MARCH 1994

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as shown in the following example.

Example:	SN	75189	N	-00

Prefix

MUST CONTAIN TWO, THREE, OR FOUR LETTERS

SN ..... TI Special Functions or Interface Products
TL ..... TI Linear Products

STANDARD SECOND-SOURCE PREFIXES

AM ..... Advanced Micro Devices
DP or DS ..... National
LT ..... Linear Technology
MAX ..... Maxim Integrated Products
MC ..... Motorola
N8T ..... Signetics
uA ..... Fairchild/National

Unique Circuit Description

MUST CONTAIN THREE TO EIGHT CHARACTERS
(From Individual Data Sheets)

Examples: 232 75160B
3695 75C1154
75115 75ALS180

Package

MUST CONTAIN ONE OR TWO LETTERS

D, DW, FK, J, KC, N, P, PW
(From Pin-Connection Diagrams on Individual Data Sheet)

Instructions (Dash No.)

MUST CONTAIN TWO NUMBERS

-00 No special instructions
-10 Solder-dipped leads (N, package only)

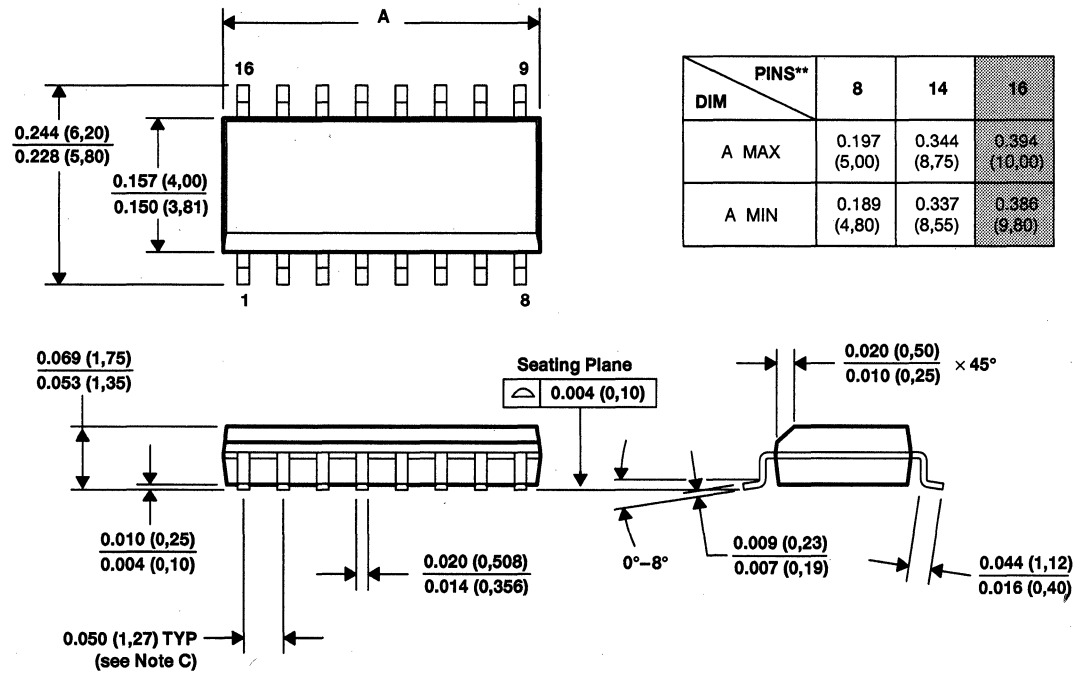
Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped via the most practical carrier.

Dual-In-Line (D, DW, J, N, P, PW)
- Slide Magazines
- A-Channel Plastic Tubing
- Sectioned Cardboard Box
- Individual Cardboard Box
- Anti-Static Plastic Tubing
- Flat
- Wells Carrier

MARCH 1994

D/R-PDSO-G** **PLASTIC NARROW-BODY SMALL-OUTLINE PACKAGE**

16-PIN SHOWN



DIM \ PINS**	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,127) radius of true position at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold protrusion shall not exceed 0.006 (0,15).

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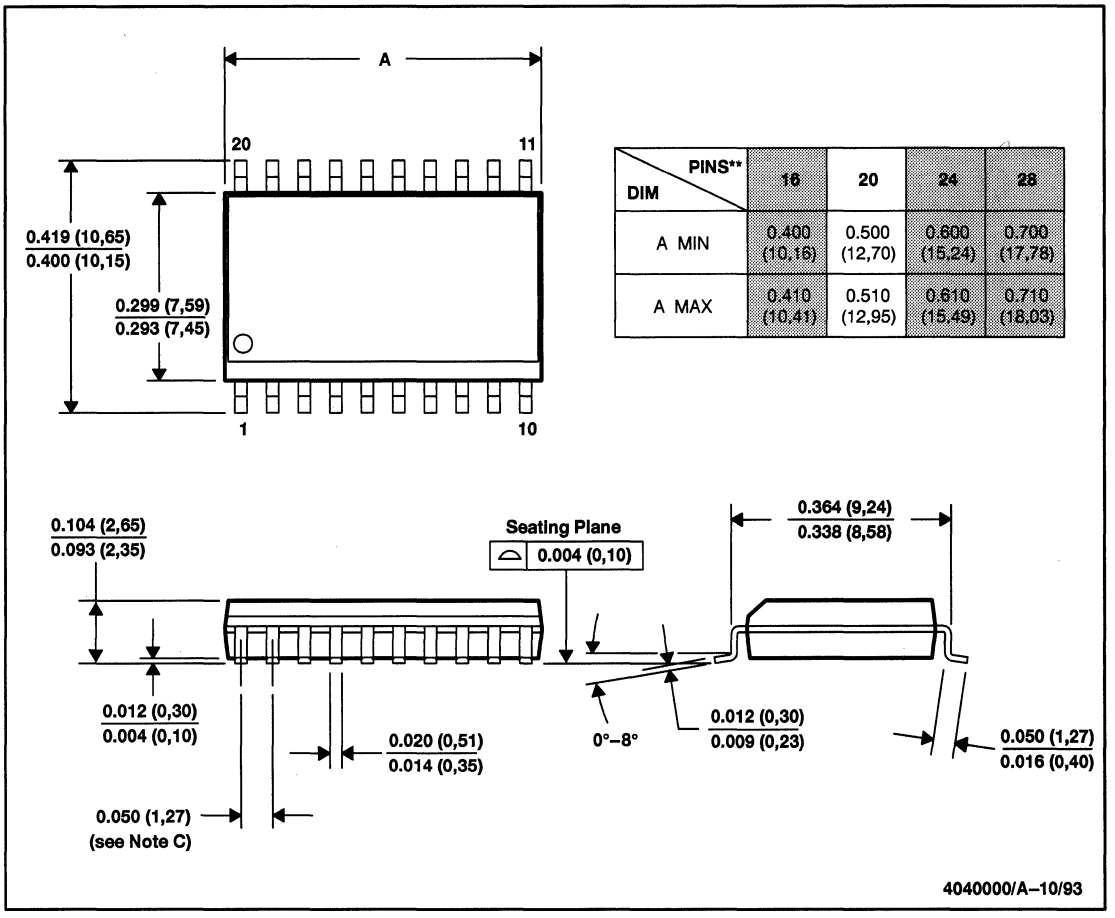
MARCH 1994

DW/R-PDSO-G**

PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE

20-PIN SHOWN



DIM \ PINS**	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)

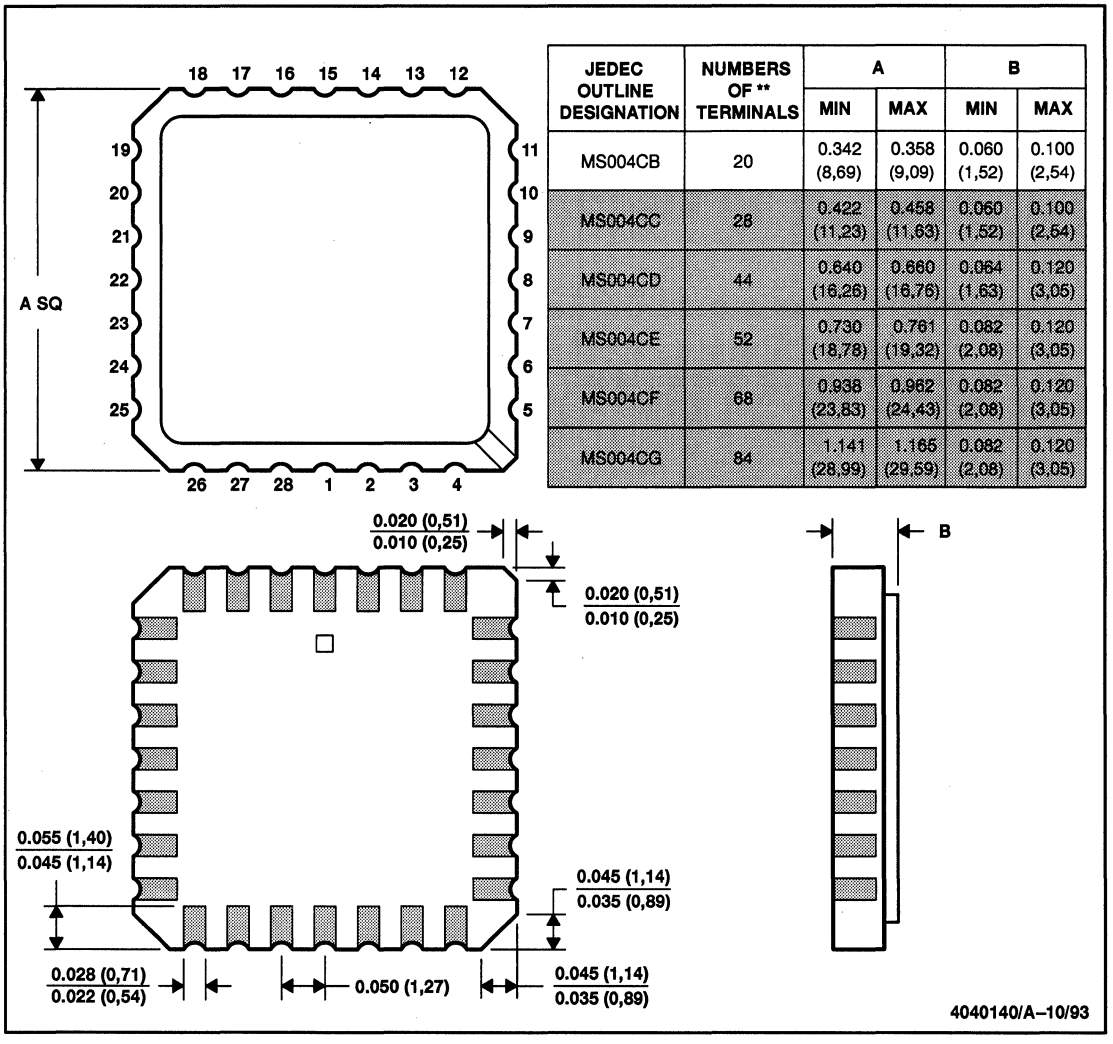
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,127) radius of true position at maximum material condition.
D. Body dimensions do not include mold flash or protrusion not exceed 0.006 (0,15).

MARCH 1994

FK/S-CQCC-N**

LEADLESS CERAMIC CHIP CARRIER PACKAGE

28-TERMINAL PACKAGE SHOWN



JEDEC OUTLINE DESIGNATION	NUMBERS OF ** TERMINALS	A		B	
		MIN	MAX	MIN	MAX
MS004CB	20	0.342 (8,69)	0.358 (9,09)	0.060 (1,52)	0.100 (2,54)
MS004CC	28	0.422 (11,23)	0.458 (11,63)	0.060 (1,52)	0.100 (2,64)
MS004CD	44	0.640 (16,26)	0.660 (16,76)	0.064 (1,63)	0.120 (3,05)
MS004CE	52	0.730 (18,78)	0.761 (19,32)	0.082 (2,08)	0.120 (3,05)
MS004CF	68	0.938 (23,83)	0.962 (24,43)	0.082 (2,08)	0.120 (3,05)
MS004CG	84	1.141 (28,99)	1.165 (29,59)	0.082 (2,08)	0.120 (3,05)

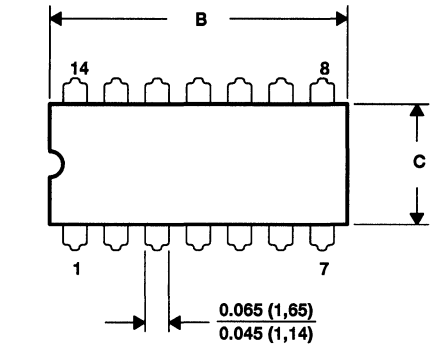
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.

MARCH 1994

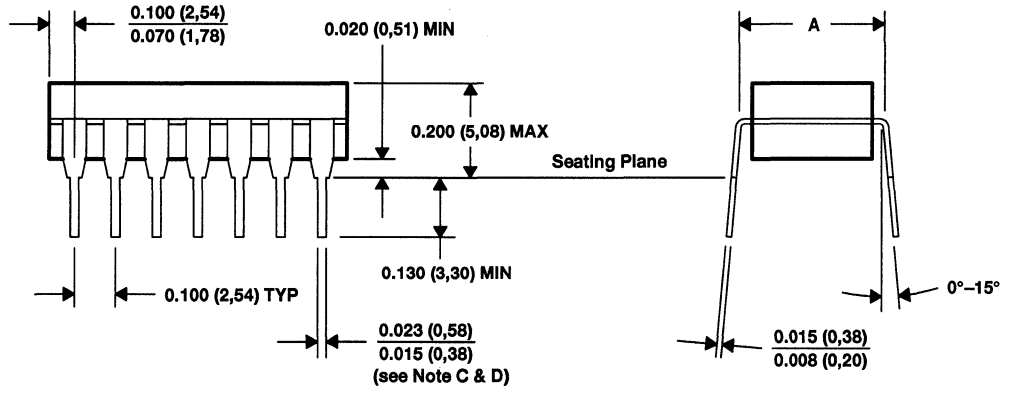
J/R-GDIP-T**

CERAMIC DUAL-IN-LINE PACKAGE

14-PIN SHOWN



DIM \ PINS**	14	16	18	20	22
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.410 (10,41)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.390 (9,91)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)	1.100 (28,00)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)	—
C MAX	0.280 (7,11)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.388 (9,65)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	—

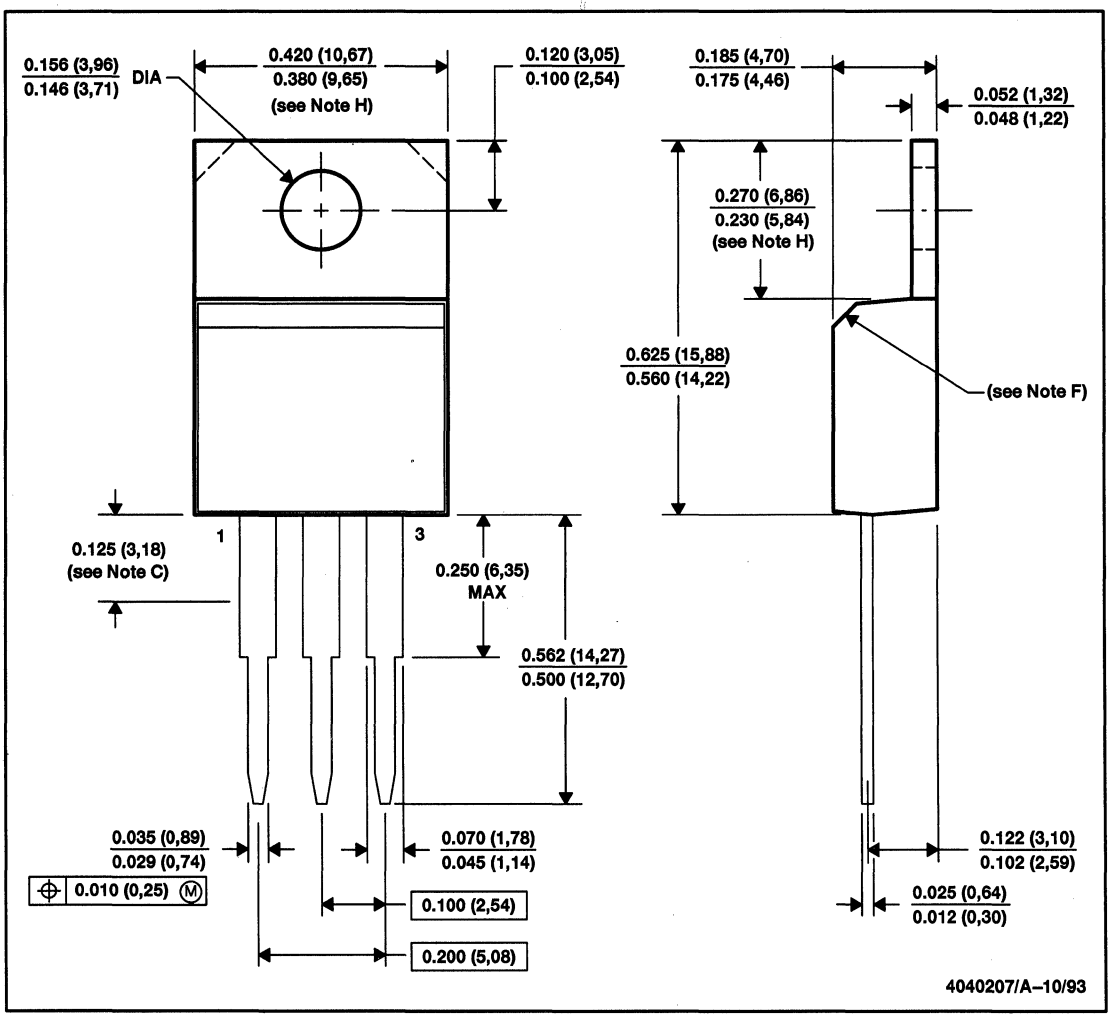


4040083/A–10/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.

MARCH 1994

KC/R-PSFM-T3 **PLASTIC FLANGE-MOUNT PACKAGE**



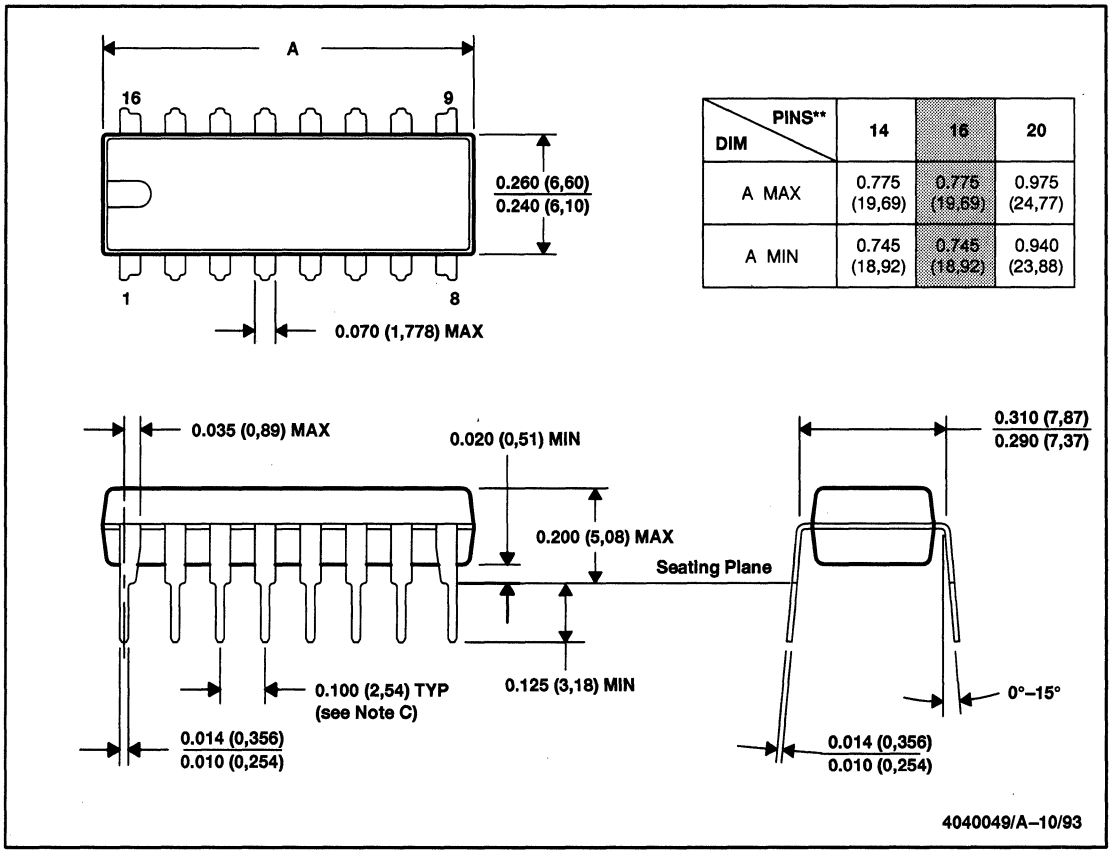
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. All lead dimensions apply before solder dip.
E. The center lead is in electrical contact with the mounting tab.
F. Chamfer optional
G. Falls within JEDEC TO-220AB
H. Tab contour optional within these dimensions

MARCH 1994

N/R-PDIP-T**

PLASTIC DUAL-IN-LINE PACKAGE

16-PIN SHOWN

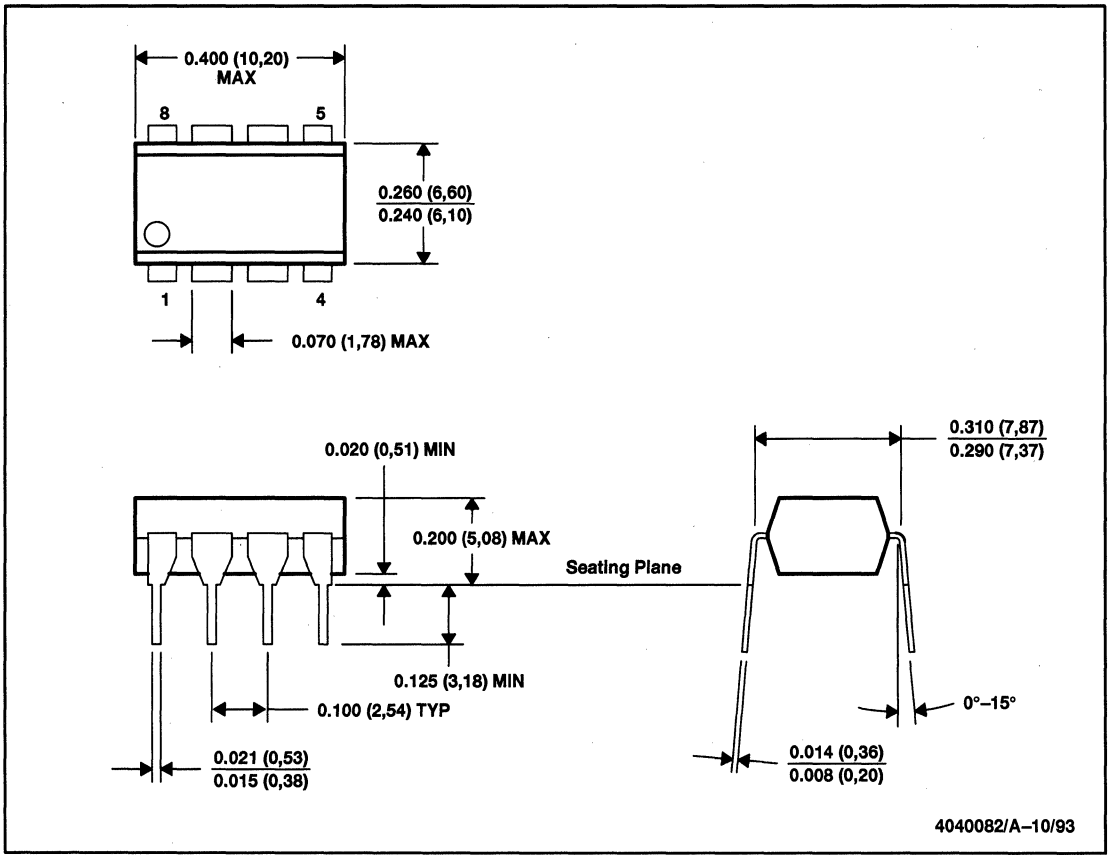


DIM \ PINS**	14	16	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.940 (23,88)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each lead centerline is located within 0.010 (0,254) of its true longitudinal position.

MARCH 1994

P/R-PDIP-T8 **PLASTIC DUAL-IN-LINE PACKAGE**



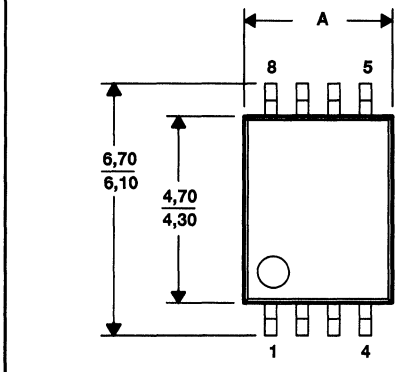
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

MARCH 1994

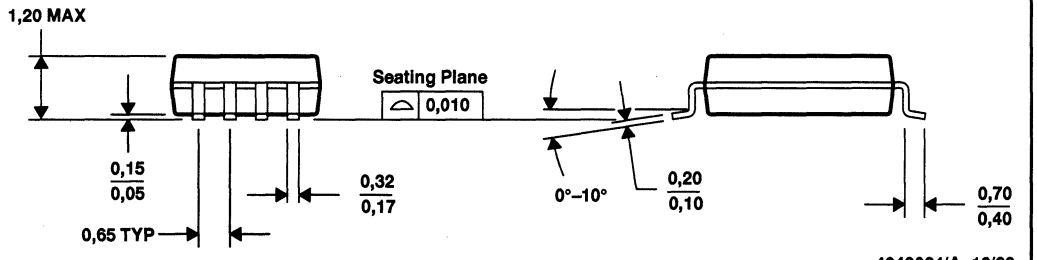
PW/R-PDSO-G**

PLASTIC THIN SHRINK SMALL-OUTLINE PACKAGE

8-PIN SHOWN



DIM \ PINS**	8	14	16	20	24	28
A MAX	3,30	5,30	5,30	6,80	8,10	10,00
A MIN	2,90	4,90	4,90	6,40	7,70	9,60



4040064/A–10/93

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Leads are within 0,127 radius of true position at maximum material condition.
D. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

NOTES

NOTES

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